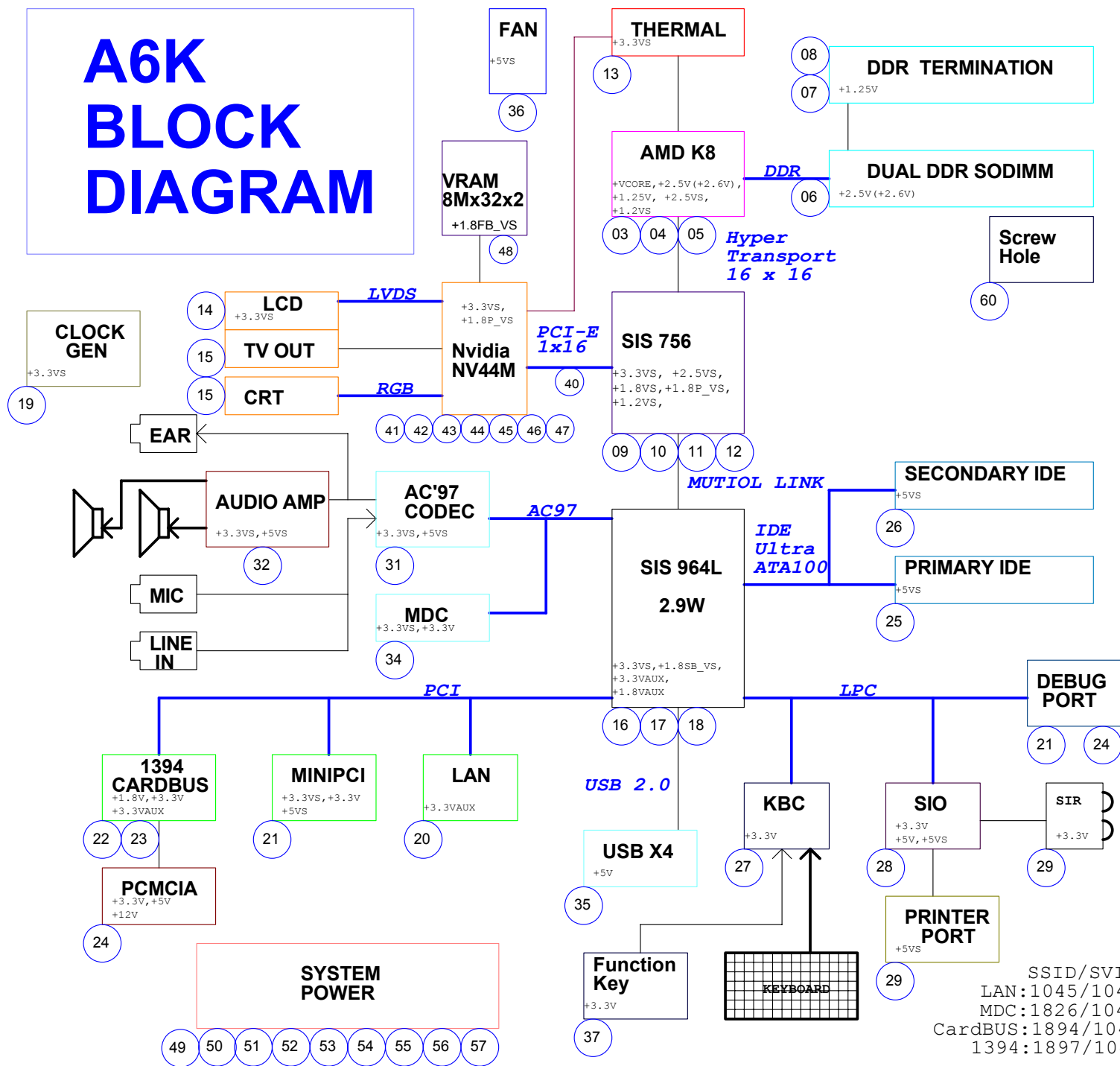


A6K BLOCK DIAGRAM



FILE LIST 01

- 01_BLOCK DIAGRAM
- 02_POWER DIAGRAM
- 03_CPU-AMD K8(HOST)
- 04_CPU-AMD K8(DDR)
- 05_CPU-AMD K8(POWER)
- 06_DDR CON
- 07_DDR BYPASS & BUFFER
- 08_DDR TERMINATOR
- 09_SiS756-1(Host/PEI-E)
- 10_SiS756-2 (for MUTIOL)
- 11_SiS756-3 (GND)
- 12_SiS756-4 (Power)
- 13_THERMAL
- 14_LVDS & BACKLIGHT
- 15_CRT/TV CONNECTOR
- 16_SiS964L (1) PCI/ZIP/IDE
- 17_SiS964L (2) LPC/GPIO
- 18_SiS964L (3) USB
- 19_CLOCK-ICS953805BF
- 20_LAN-RTL8100CL
- 21_MINIPCI
- 22_CB1394-R5C593 (1)
- 23_CB1394-R5C593 (2)
- 24_PCPCIA SOCKET
- 25_IDE-HDD
- 26_IDE-ODD
- 27_KBC-M38857
- 28_SIO-SMSC LPC47N417&BIOS
- 29_IR & LPT_PORT
- 30_Discharge circuit
- 31_CODEC-ALC650
- 32_AUDIO AMP
- 33_MIC
- 34_MDC & RJ45 & RJ11
- 35_USB
- 36_BT-UGPZ5
- 37_FAN&Audio DJ
- 38_FUNCTION KEY
- 39_PWR & RESET SEQ
- 40_PCPCIA Debug MUX
- 41_PCI-E AC Coupling
- 42_NV44 PEX I/F
- 43_NV44 Strapping
- 44_NV44 VGA/TV OUT
- 45_NV44 LVDS I/F
- 46_NV44 Spread Spectrum
- 47_NV44 FB I/F (A)
- 48_NV44 FB I/F (C)
- 49_VRAM(1)
- 50_Vcore
- 51_1.25V&1.2V
- 52_2.5V&1.8V
- 53_SYSTEM
- 54_LOAD SWITCH
- 55_CHARGER
- 56_PIC16C54
- 57_BATLOW/SD#
- 58_VGA CORE
- 59_SCREWHOLE
- 60_POWER SEQUENCE
- 61_GPIO SETTING
- 62_SECOND SOURCE
- 63_Revision(1)
- 64_Revision(2)

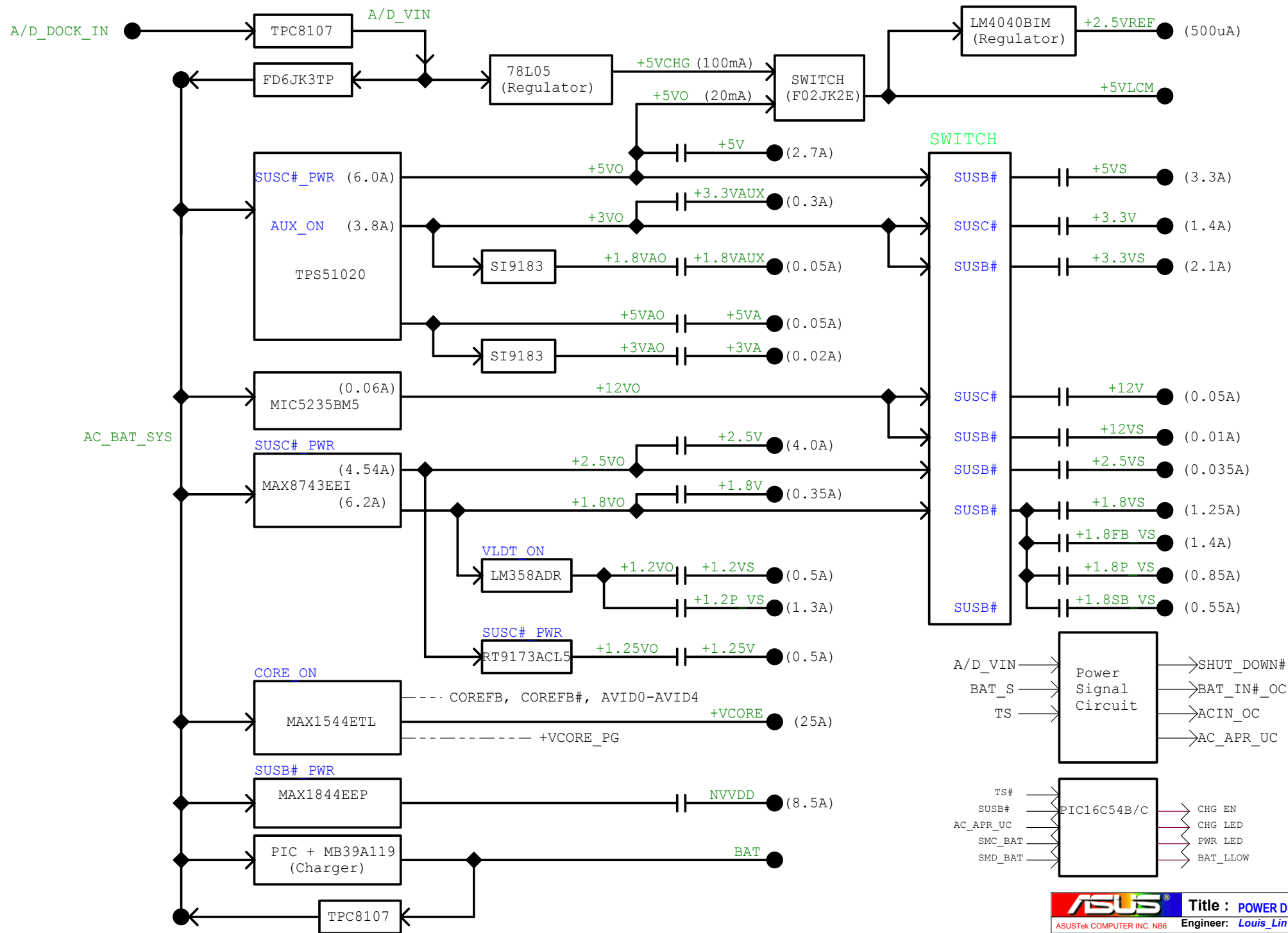
ASUS Title : BLOCK DIAGRAM

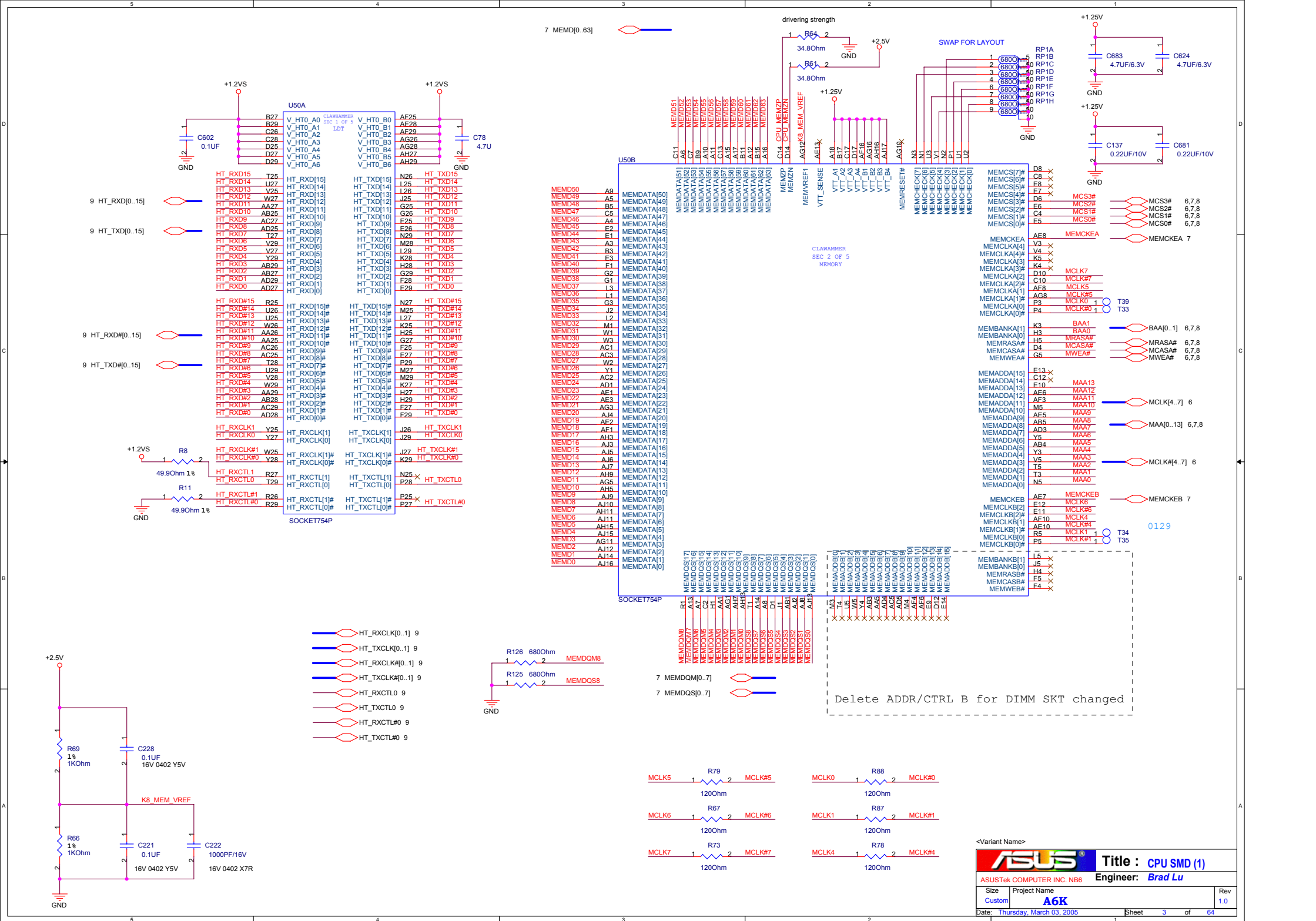
ASUSTek COMPUTER INC. NB6 Engineer: Brad Lu

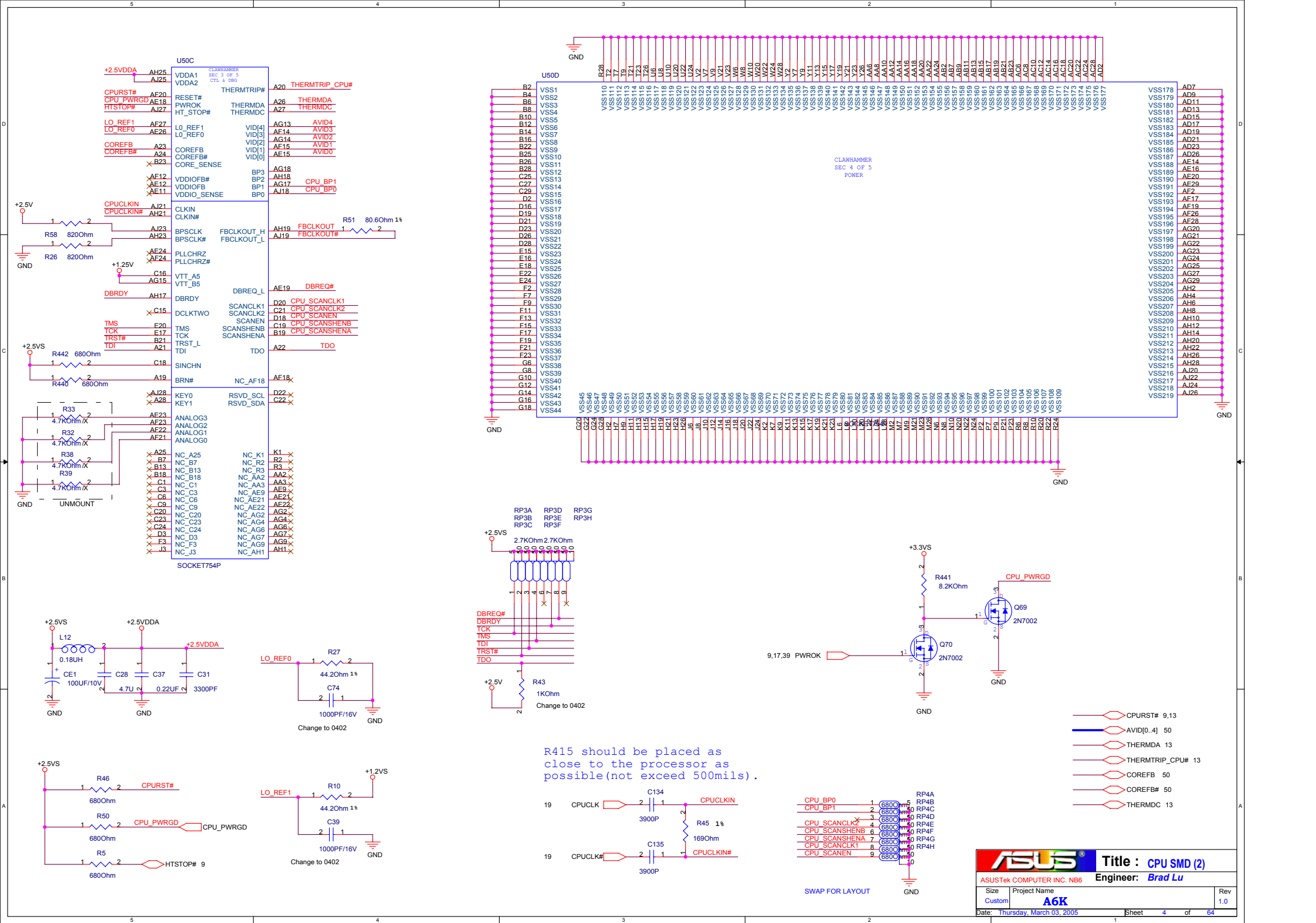
Size Project Name Rev

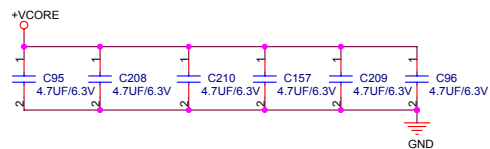
Custom A6K 1.0

Date: Thursday, March 03, 2005 Sheet 1 of 64

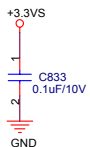






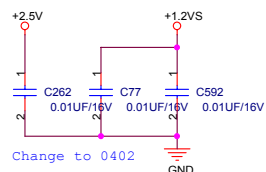
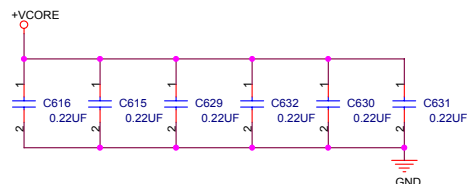
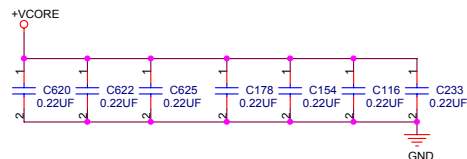


Link plane for EMI

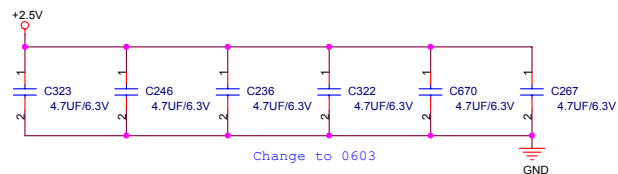


+2.5V (VDDIO, MAX) : 3A
+1.2VS (VLDT, MAX) : 500mA
+1.25V (VTT, MAX) : 250mA
+VCORE (VDD, MAX) : 27A
+2.5VS (VDDA, MAX) : 35mA

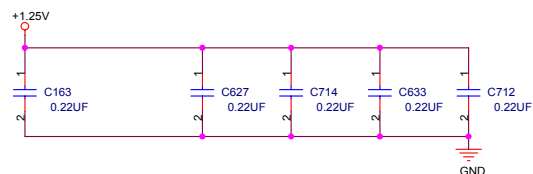
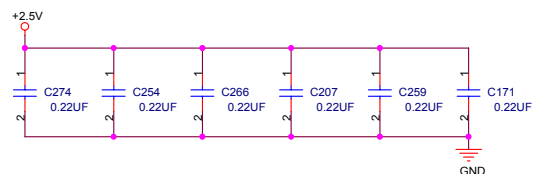
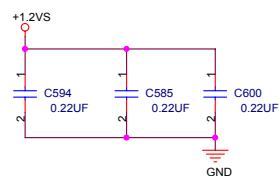
VDDIO: Up to 2.6V to support DDR400 (3A)



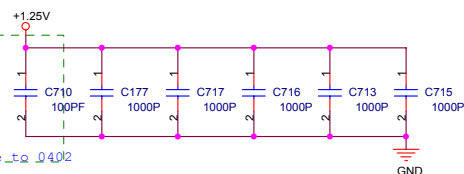
Change to 0402



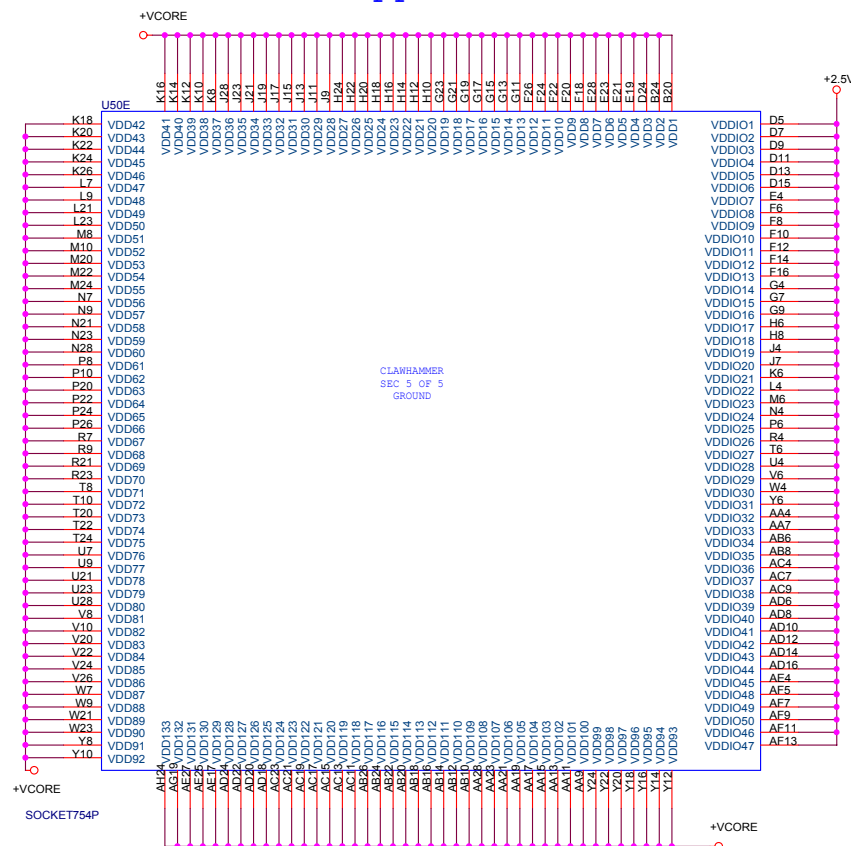
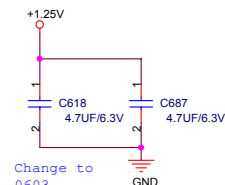
Change to 0603



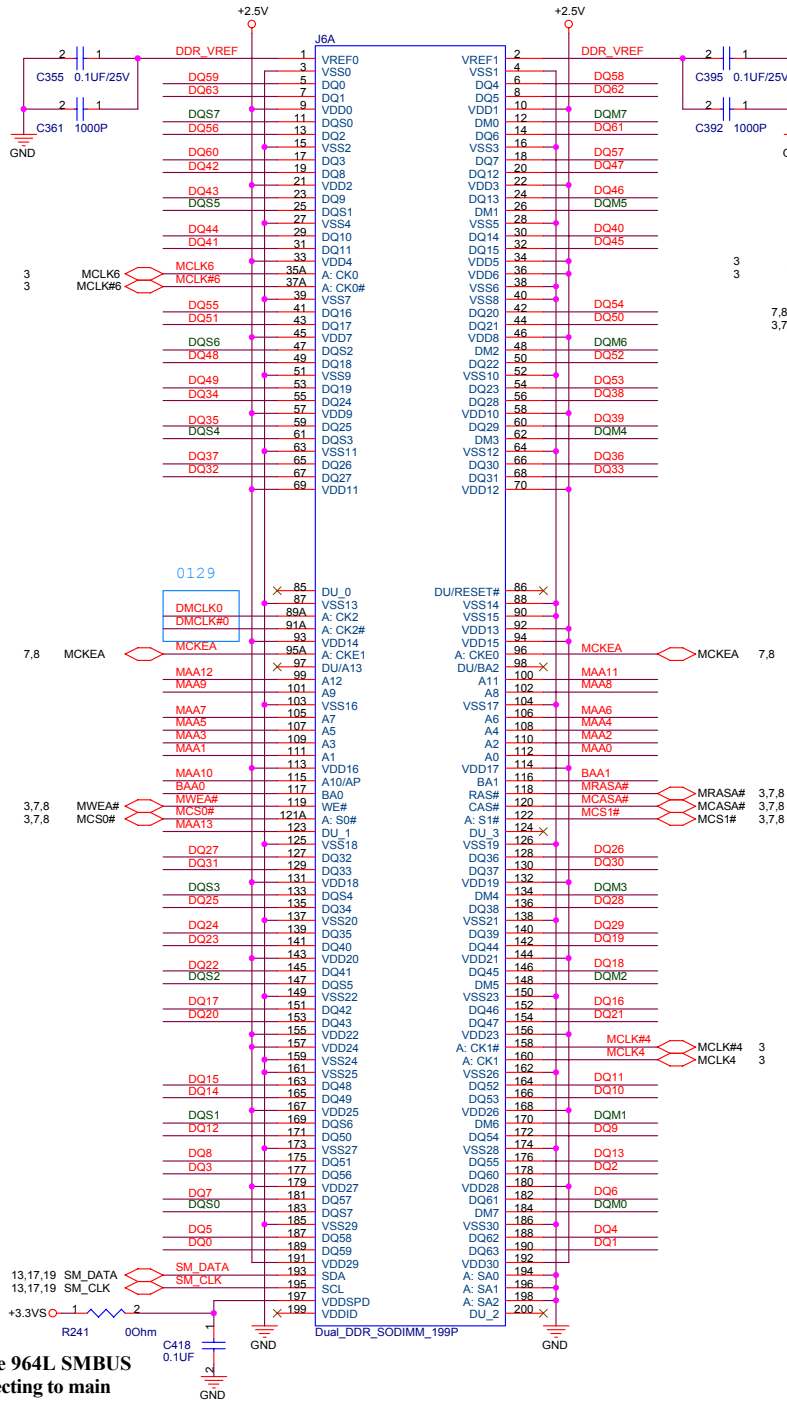
Change to 0402



Change to
0603



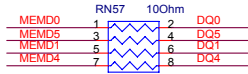
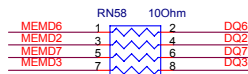
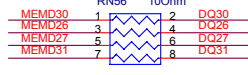
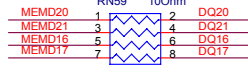
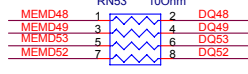
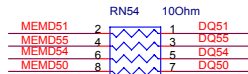
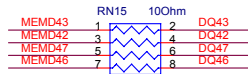
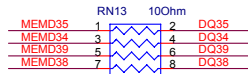
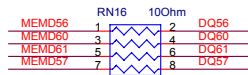
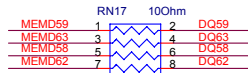
CLAWHAMMER
SEC 5 OF 5
GROUND



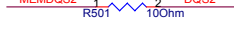
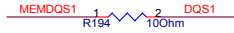
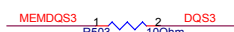
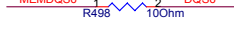
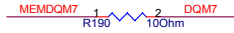
3 MEMD[0..63] 
6,8 DQ[0..63] 

3 MEMDQS[0..7] 
6,8 DQS[0..7] 
3,6,8 MAA[0..13] 

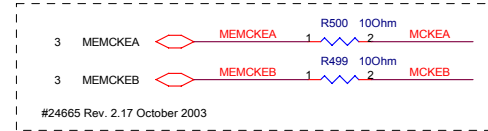
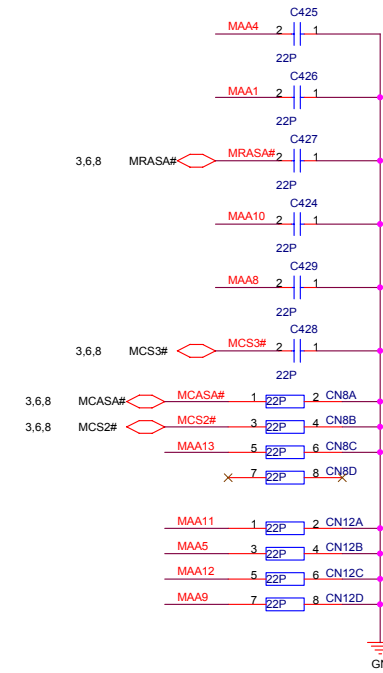
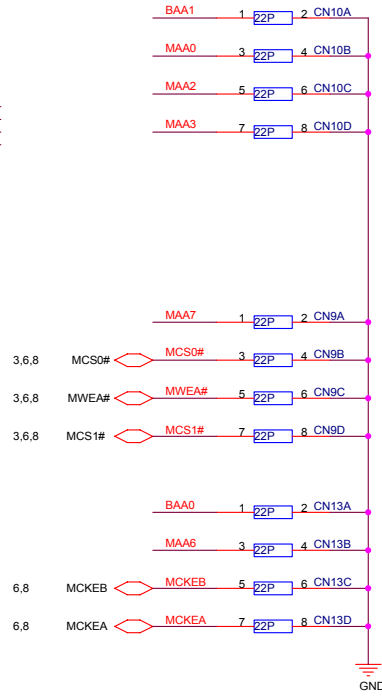
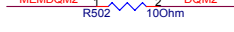
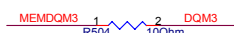
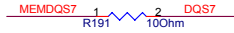
3,6,8 BAA[0..1] 
6,8 DQM[0..7] 
3 MEMDQM[0..7] 



TO fine tune DQS



TO fine tune DQM

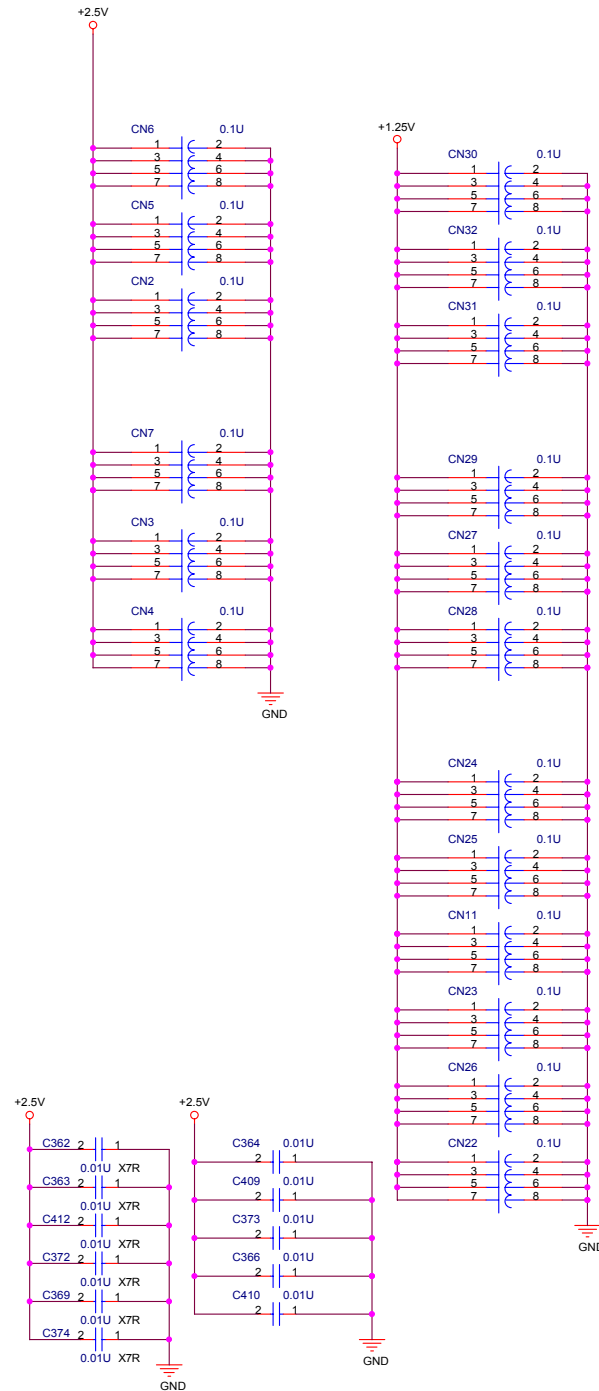
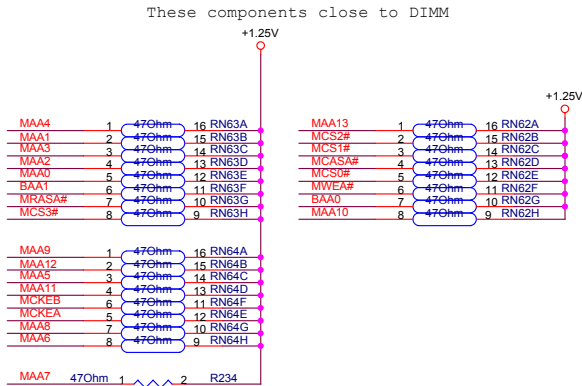
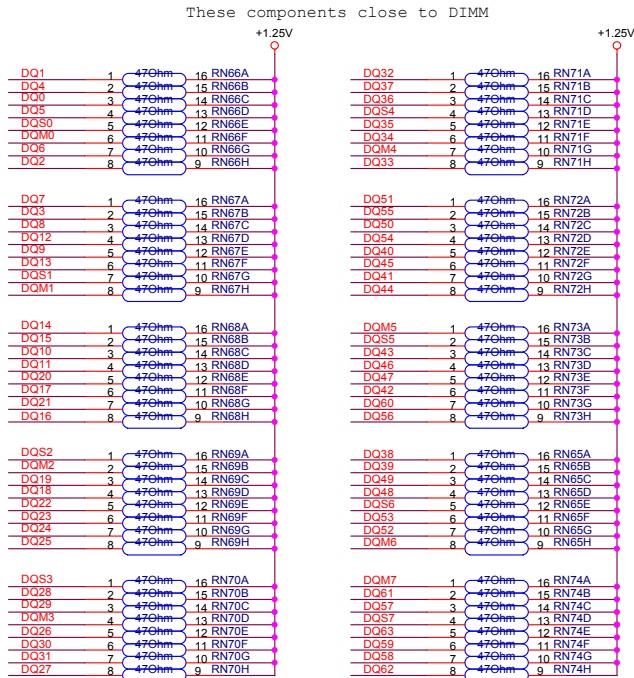


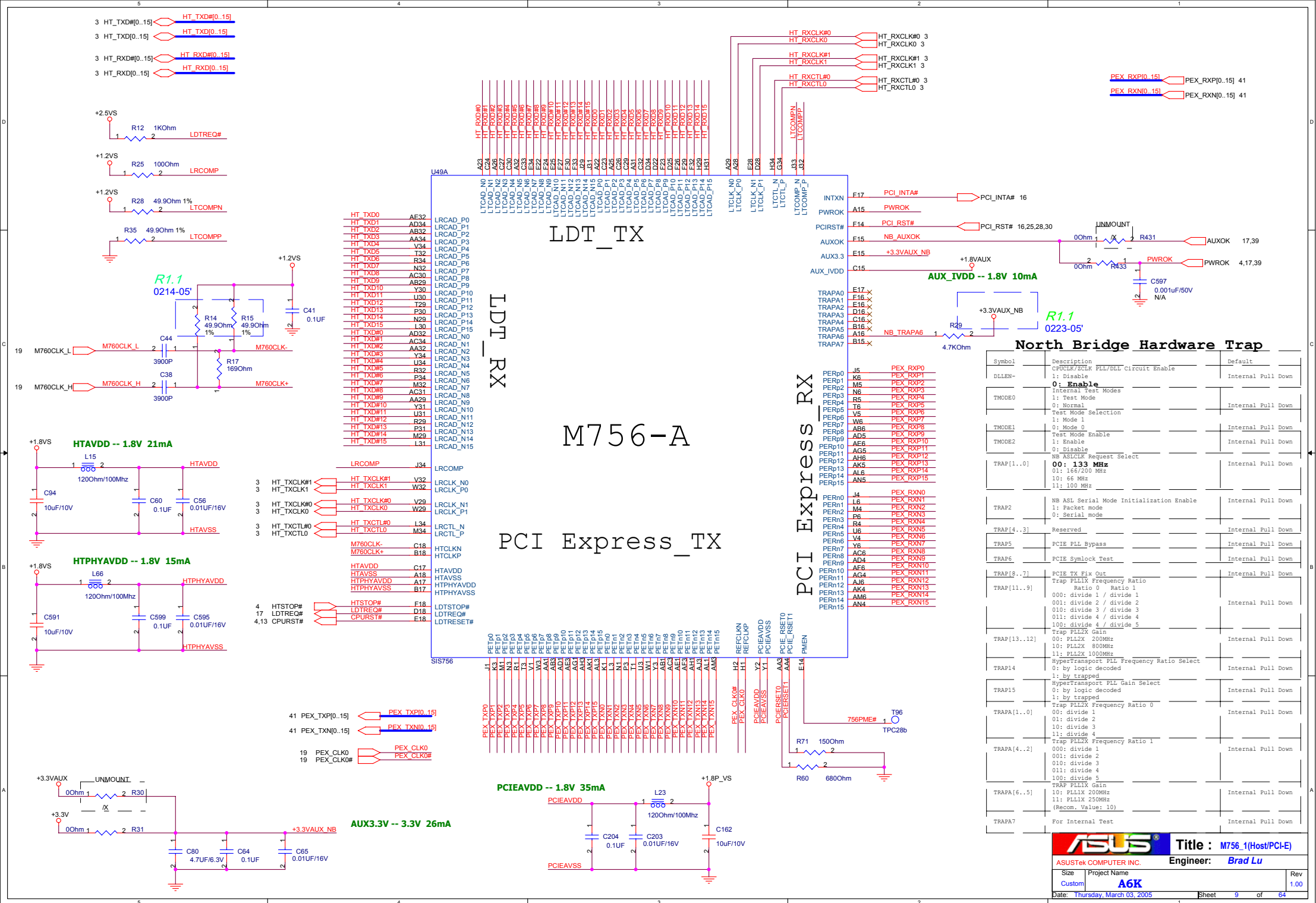
6,7 DQM[0..7]
6,7 DQ[0..63]
6,7 DQS[0..7]
3,6,7 MAA[0..13]
3,6,7 BAA[0..1]

6,7 MCKEA
6,7 MCKEB
3,6,7 MRASA#
3,6,7 MCASA#

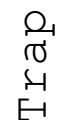
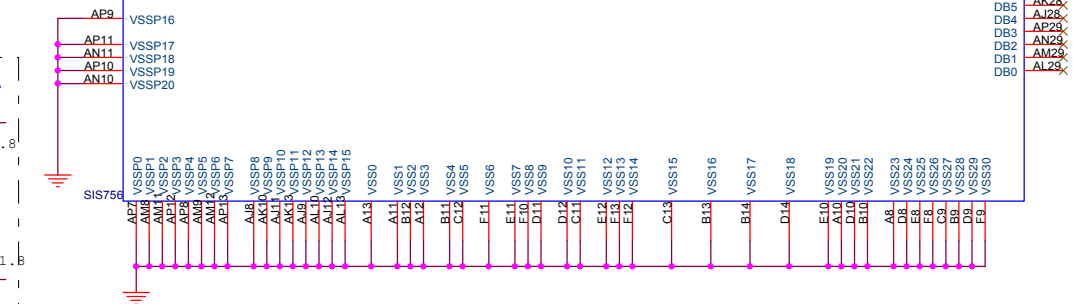
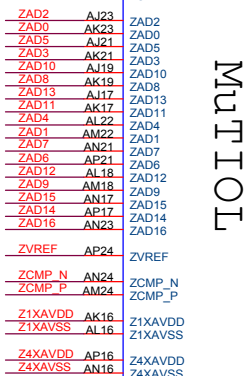
3,6,7 MWEA#

3,6,7 MCS0#
3,6,7 MCS1#
3,6,7 MCS2#
3,6,7 MCS3#



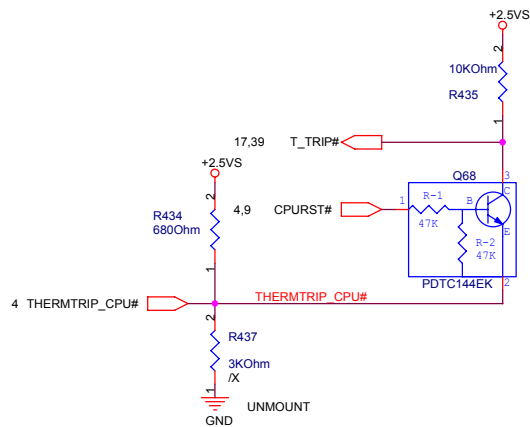
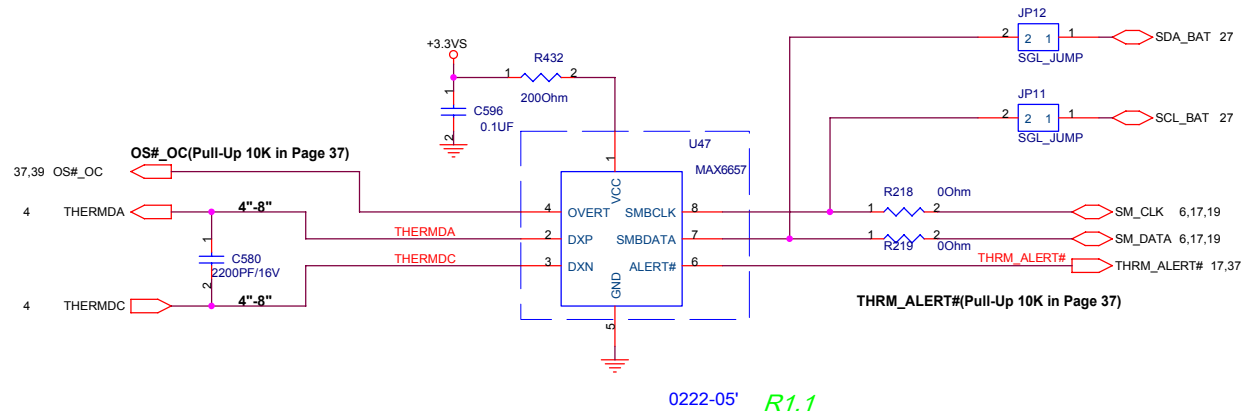


Pin	Signal	Package Pin	Function
19	CLK_ZIP_NB	AM16	ZCLK
16	ZUREQ	AL24	ZUREQ
16	ZDREQ	AP23	ZDREQ
16	ZSTB0#	AL20	ZSTB#0
16	ZSTB0	AM20	ZSTB0
16	ZSTB1#	AN19	ZSTB#1
16	ZSTB1	AP19	ZSTB1



M756-3

Ground



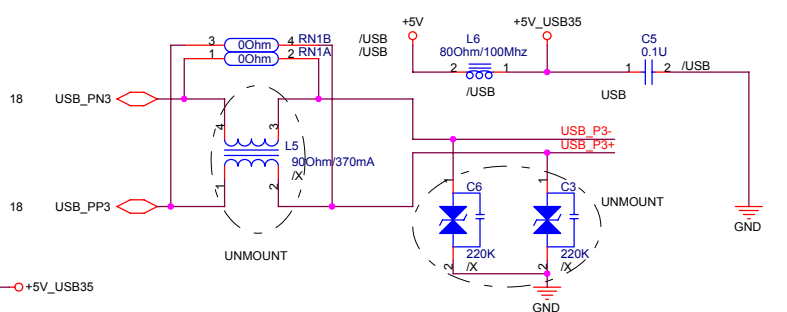
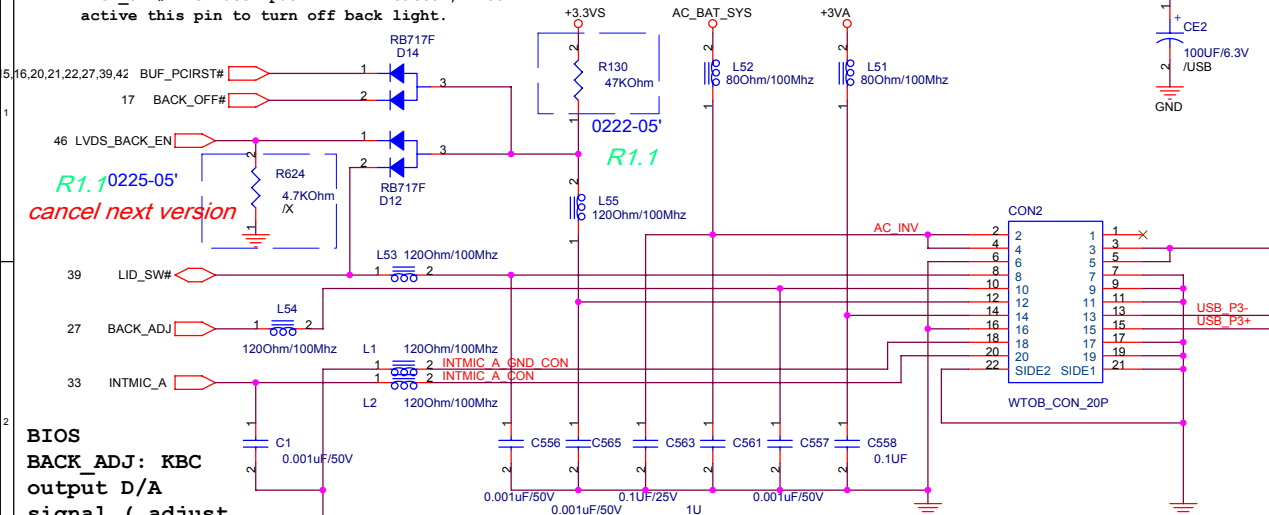
THERMAL

Route H_THERMDA and H_THERMDC on the same layer

-----OTHER SIGNALS
 12 mils
 =====GND
 10 mils
 =====H_THERMDA(10 mils)
 10 mils
 =====H_THERMDC(10 mils)
 10 mils
 =====GND
 12 mils
 -----OTHER SIGNALS

Avoid BPSB,Power

BIOS
BACK OFF#:When user push "Fn+F7" button, BIOS
active this pin to turn off back light.

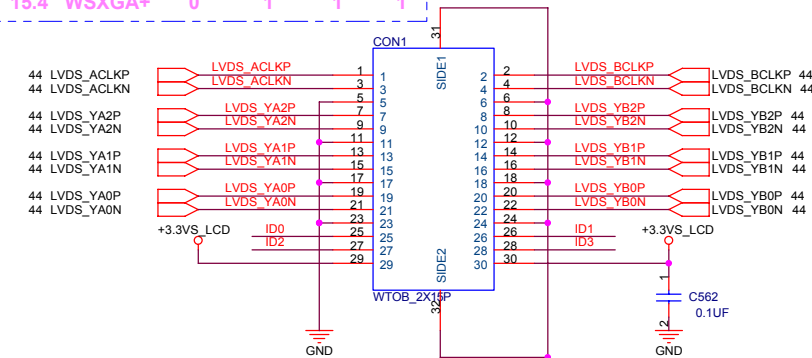


USB PORT 3 for CAMERA

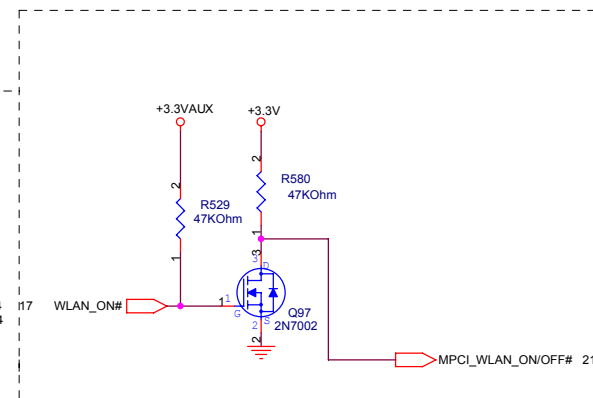
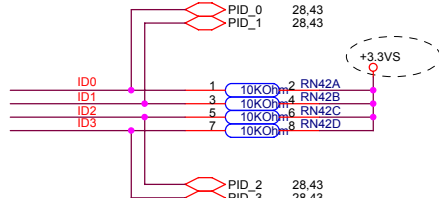
BIOS
BACK_ADJ: KBC
output D/A
signal (adjust
voltage level)
to adjust Back
light.

A3K used D1 R:1.0
Inverter Board

LCD CABLE ID: PID3	PID2	PID1	PID0
15.1 XGA	1	1	0
15.1 SXGA+	1	0	1
15.4 WXGA	1	1	0
15.4 WSXGA+	0	1	1

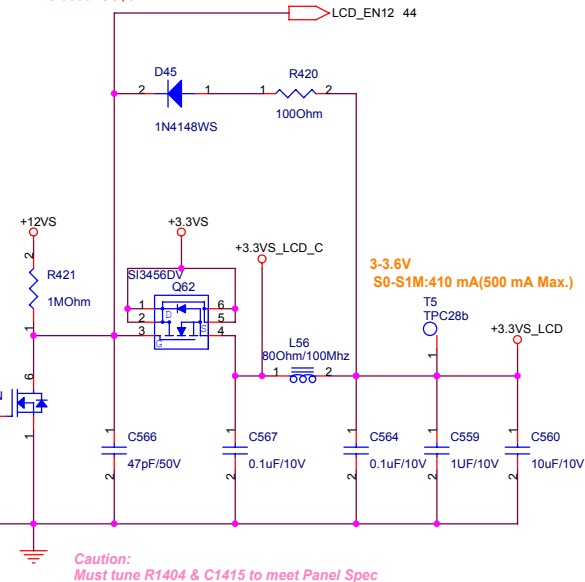


0114-05' CON1 Changed to
"12-17001030A"

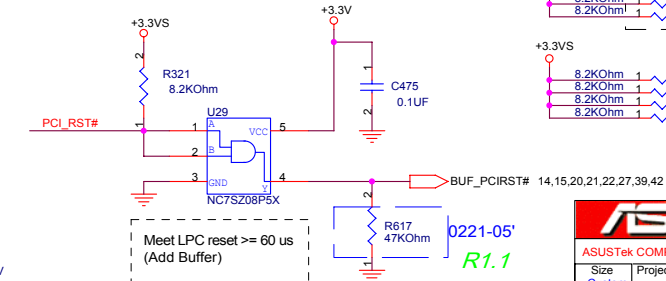


LCD Power

SI3865: US\$0.22



Caution:
Must tune R1404 & C1415 to meet Panel Spec

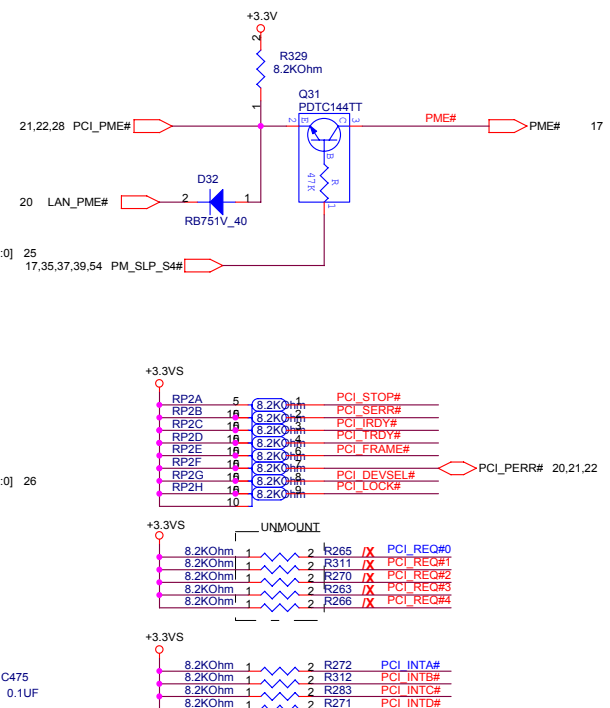


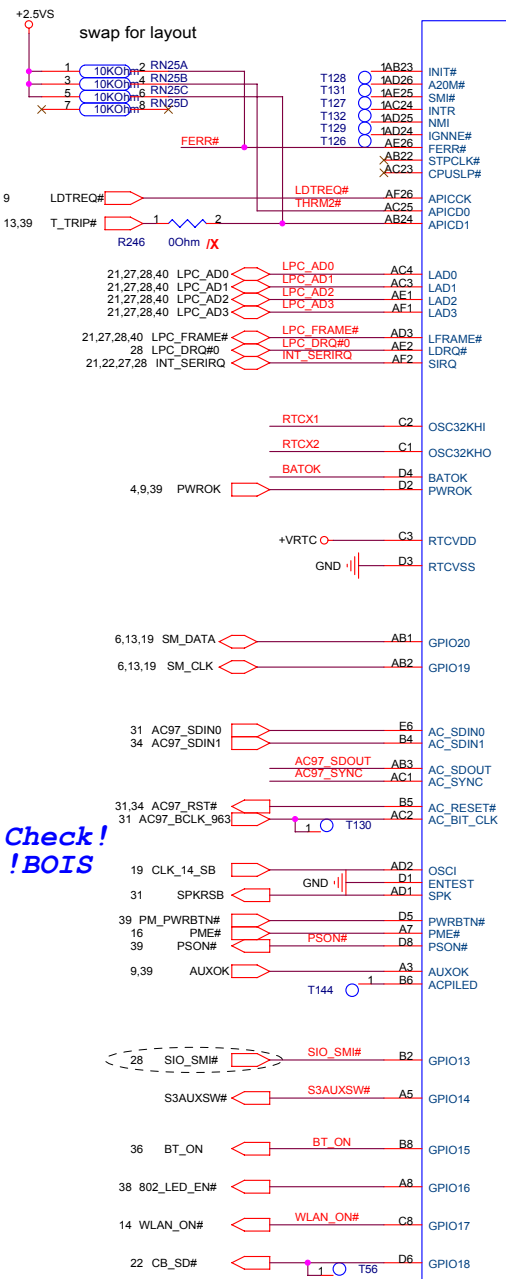
Check!

UNMOUNT

GND

pull up to VccSus3_3
by internal pull-up
resistor

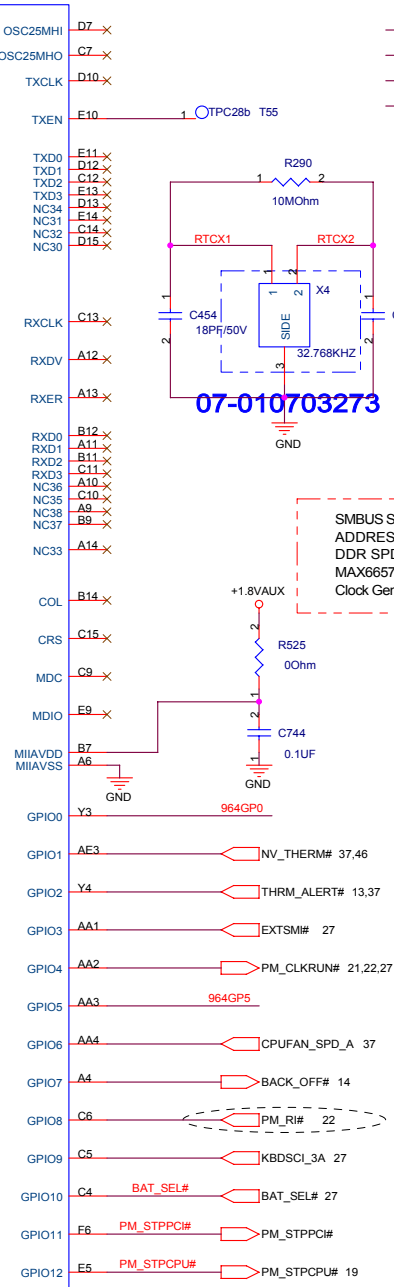




SiS 964L GPI/O Power Plan

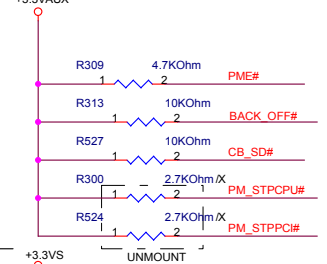
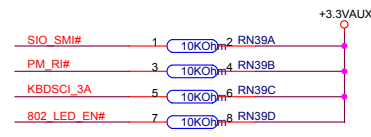
GPIO[6:0]: I/O-M
GPIO[16:7]: I/O-AUX
GPIO[18:16]: O-AUX
GPIO[20:19]: OD-AUX
GPIO[24:21]: I-AUX

U19B SIS964L

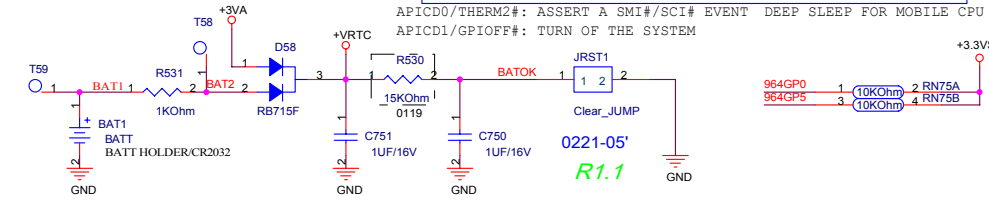
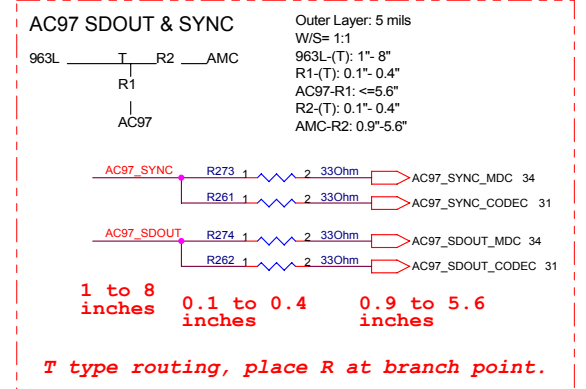
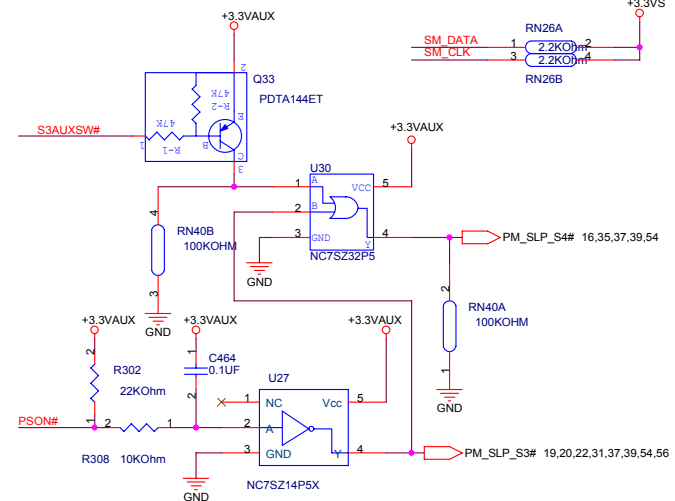
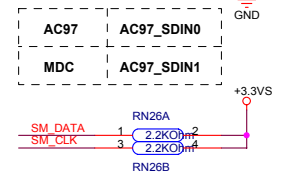
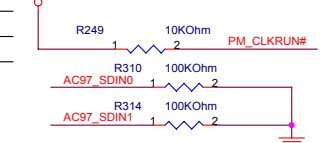


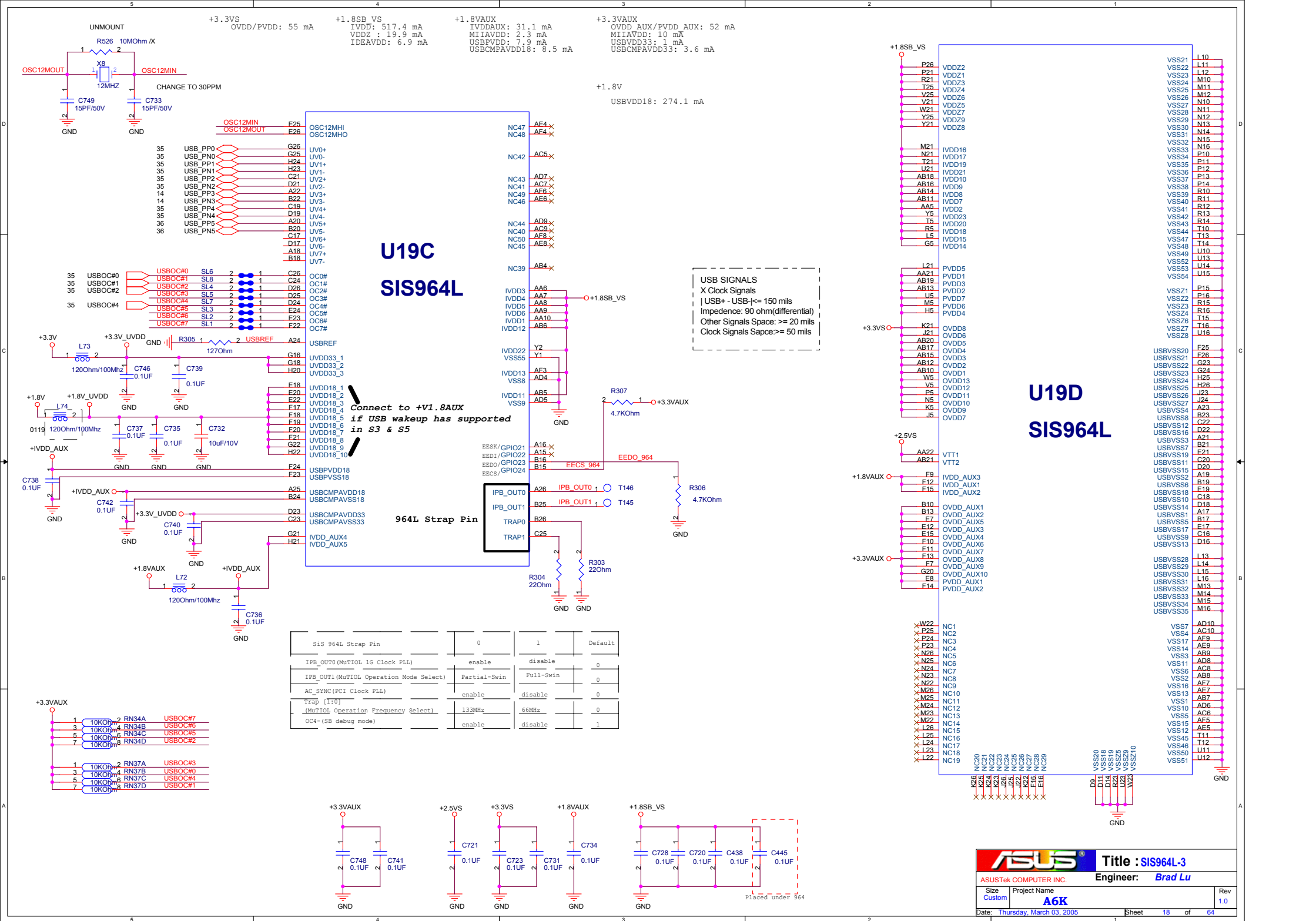
SMBUS SLAVE
ADDRESS
DDR SPD: A0
MAX6657: 98
Clock Gen: D2

Check!
!BOIS



	S1	S3	S5
S3AUXSW#	1	0	1
PS0N#	0	1	1
PM_SLP_S3#	1	0	0
PM_SLP_S4#	1	1	0

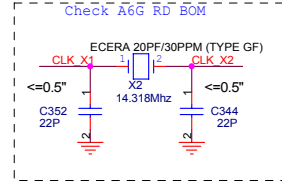
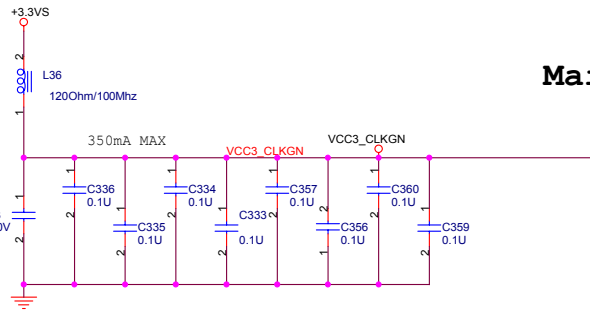




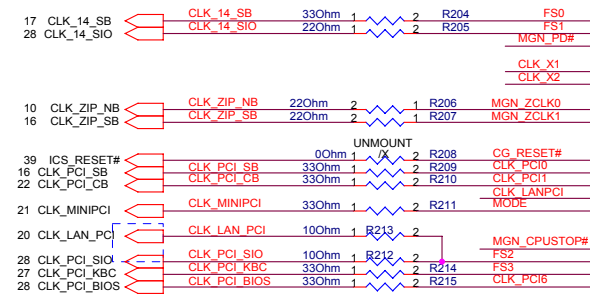
Main Clock Generator

CLK33 GROUP:
 In L3
 Breakout:
 Group Space >= 25 mils
 Length Match: same as CLK66

CLK66 GROUP:
 In L3
 Breakout:
 (<=0.3")
 Group Space >= 25 mils
 Length Match: +/- 100 mils

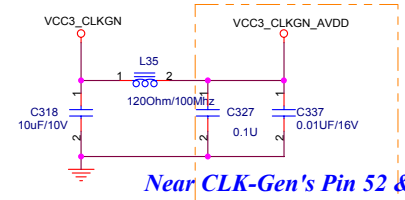
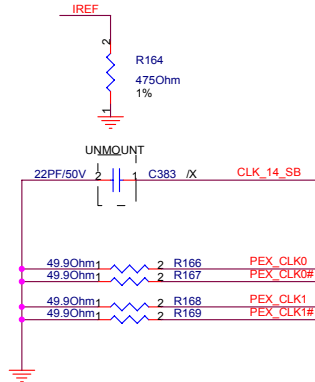
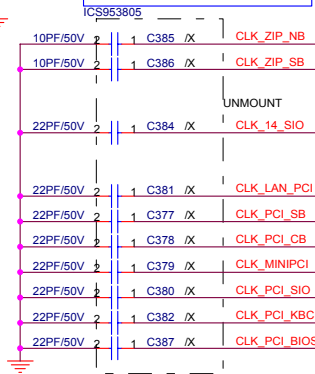
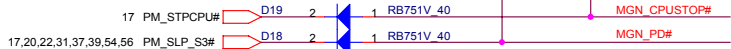
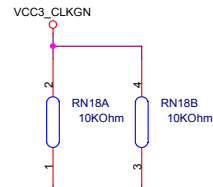


Damping Resistors
 Place near to the
 Clock Outputs.



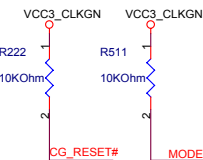
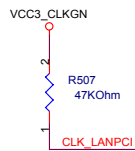
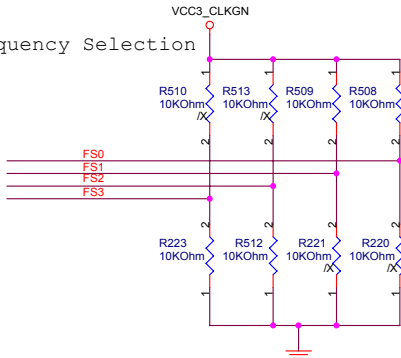
Watch out length mismatch!

BIOS need to disable PIN 26,27,SRCLK, PCIE2-4



Near CLK-Gen's Pin 52 & 49.

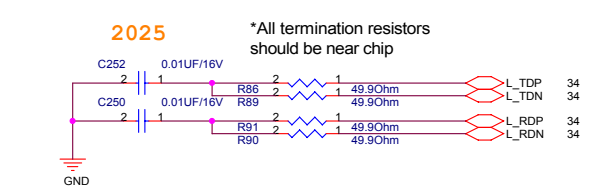
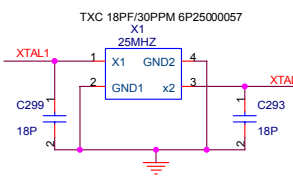
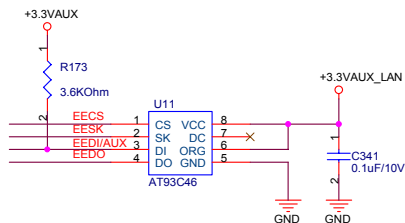
Frequency Selection



CLK Table for SiS M756 (ICS-953805)

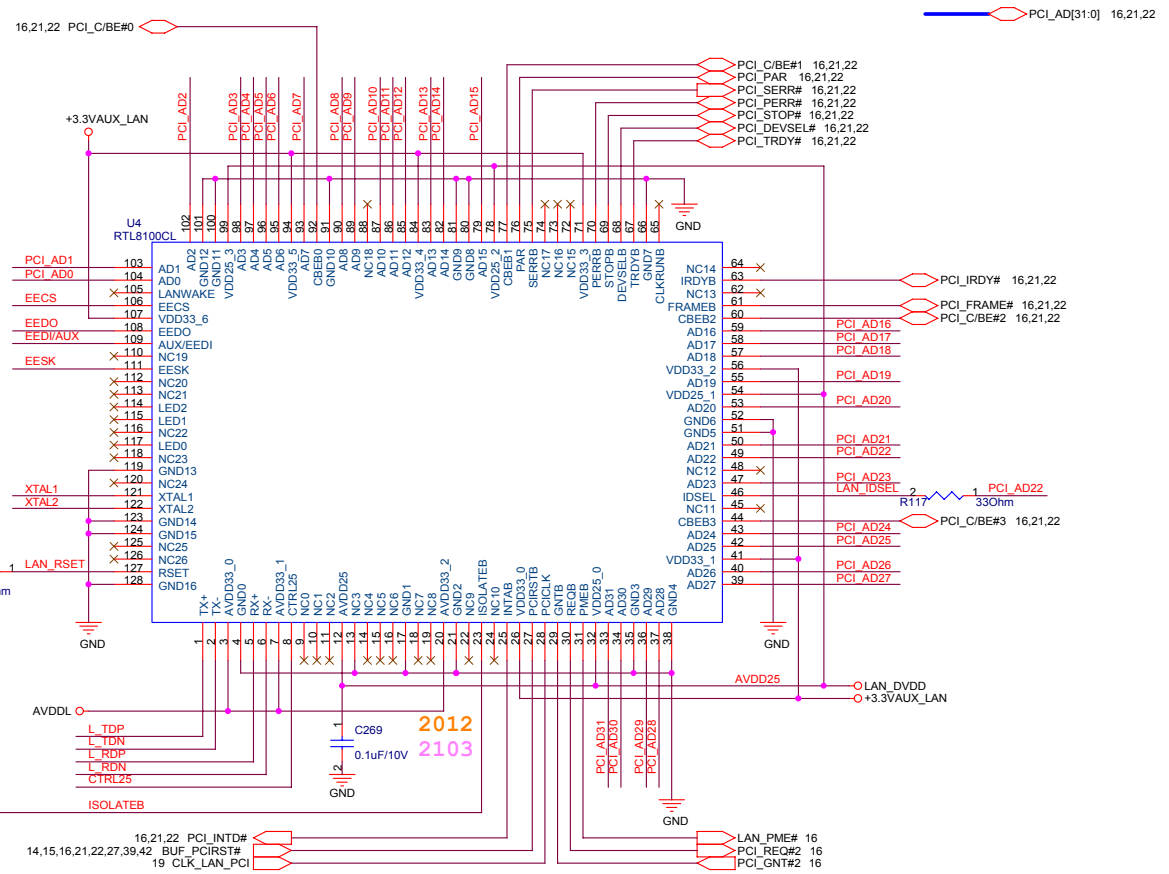
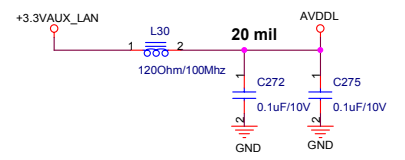
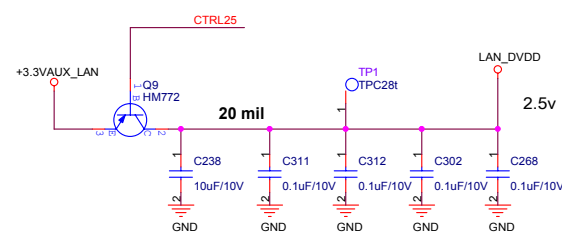
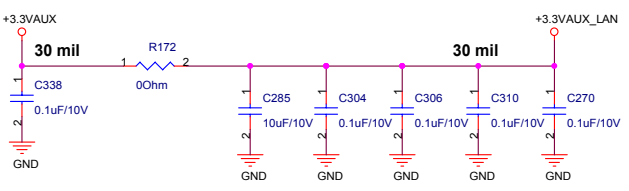
SiS M760 CLOCK											
(FS3)	(FS2)	(FS1)	(FS0)	CPU	NB CLK	ZCLK	PCIE X	PCIE L			
				(MHz)	(MHz)	(MHz)	(MHz)	(MHz)			
0	0	0	0	100	100	133.33	100.00	33.33			
0	0	0	1	133.33	133.33	133.33	100.00	33.33			
0	0	1	0	166.66	166.66	133.33	100.00	33.33			
0	0	1	1	200.00	200.00	133.33	100.00	33.33			
0	1	0	0	250.00	250.00	100.00	100.00	33.33			
0	1	0	1	266.66	266.66	133.33	100.00	33.33			
0	1	1	0	100.00	125.00	133.33	100.00	33.33			
0	1	1	1	133.33	166.66	133.33	100.00	33.33			
1	0	0	0	166.66	222.22	133.33	100.00	33.33			
1	0	0	1	200.00	250.00	133.33	100.00	33.33			
1	0	1	0	250.00	333.33	133.33	100.00	33.33			
1	0	1	1	266.66	400.00	133.33	100.00	33.33			
1	1	0	0	202.00	202.00	134.66	100.00	33.66			
1	1	0	1	204.00	204.00	136.00	100.00	34.00			
1	1	1	0	206.00	206.00	137.33	100.00	34.33			
1	1	1	1	208.00	208.00	138.66	100.00	34.66			

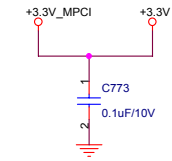
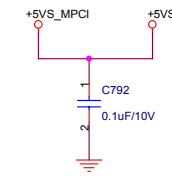
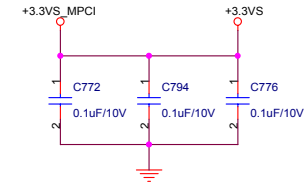
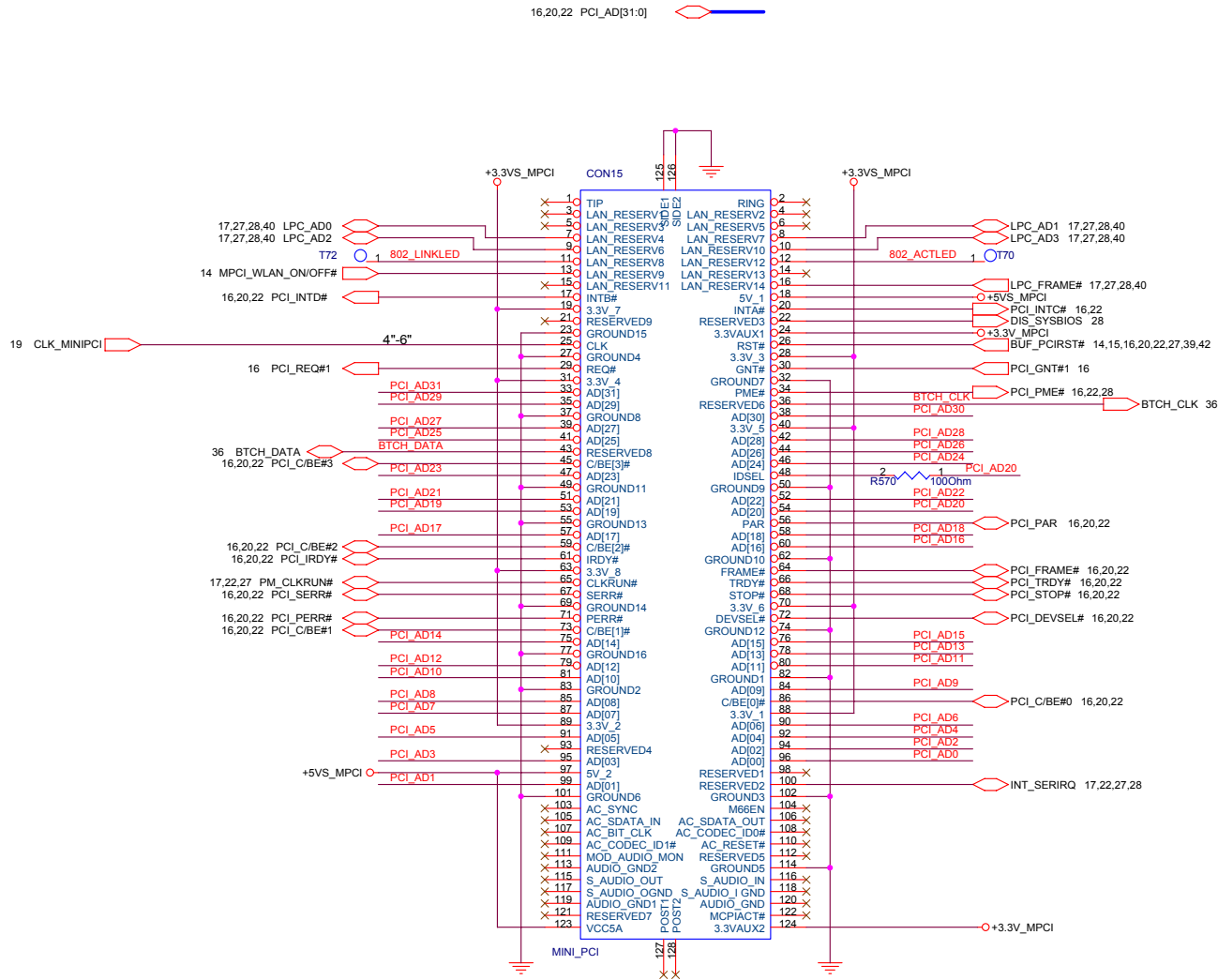
Trap Default



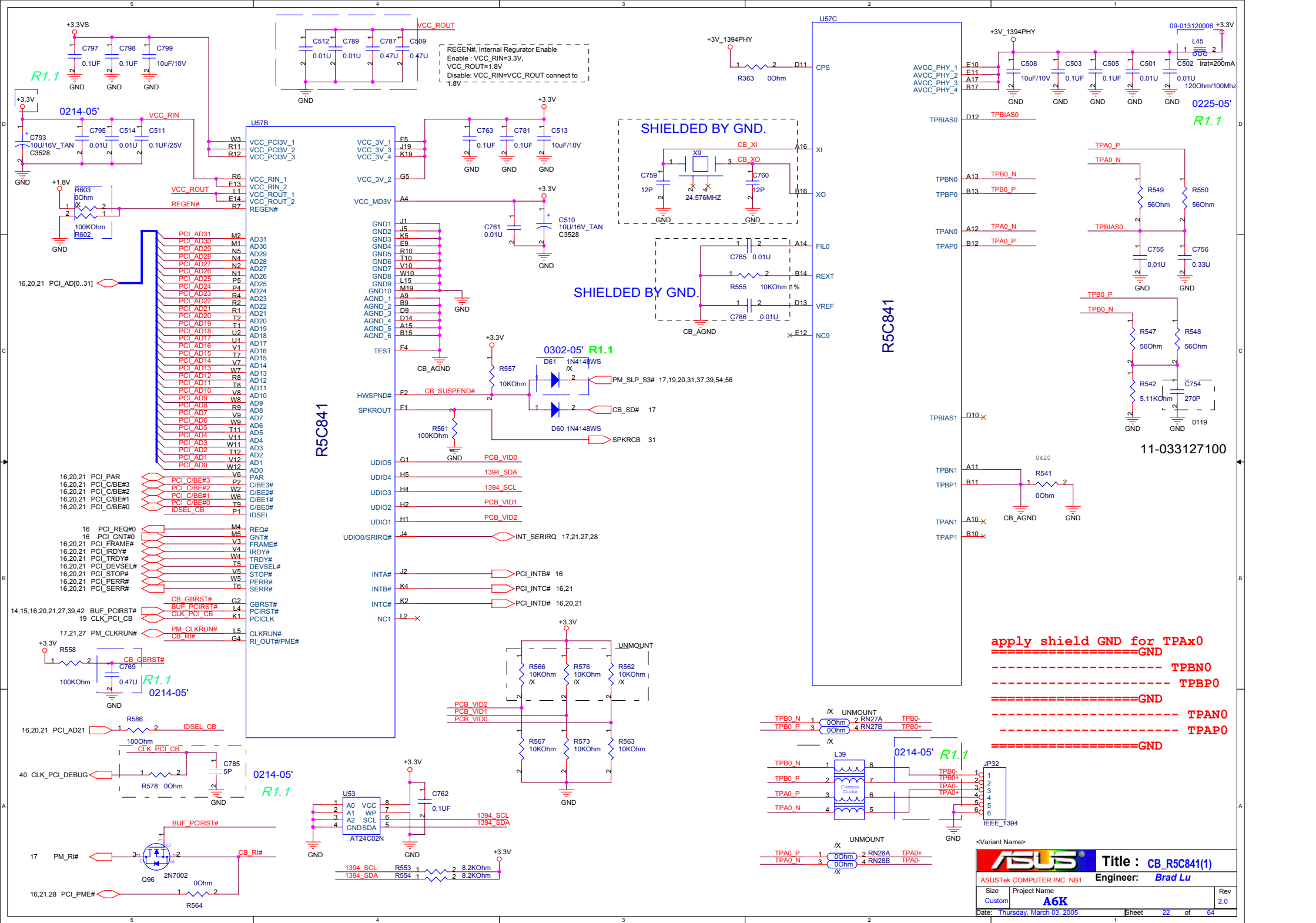
2025

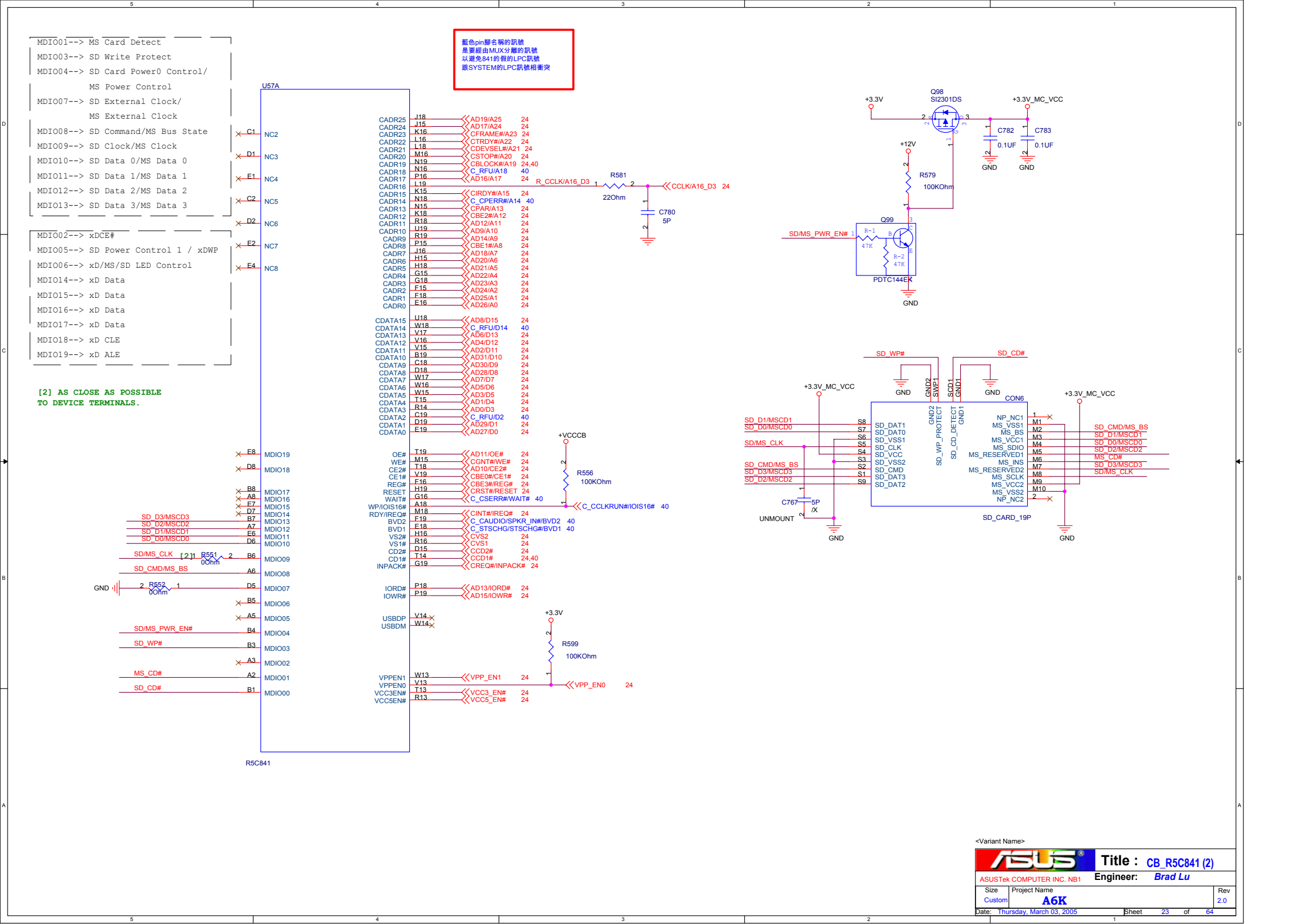
*All termination resistors should be near chip





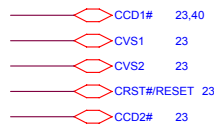
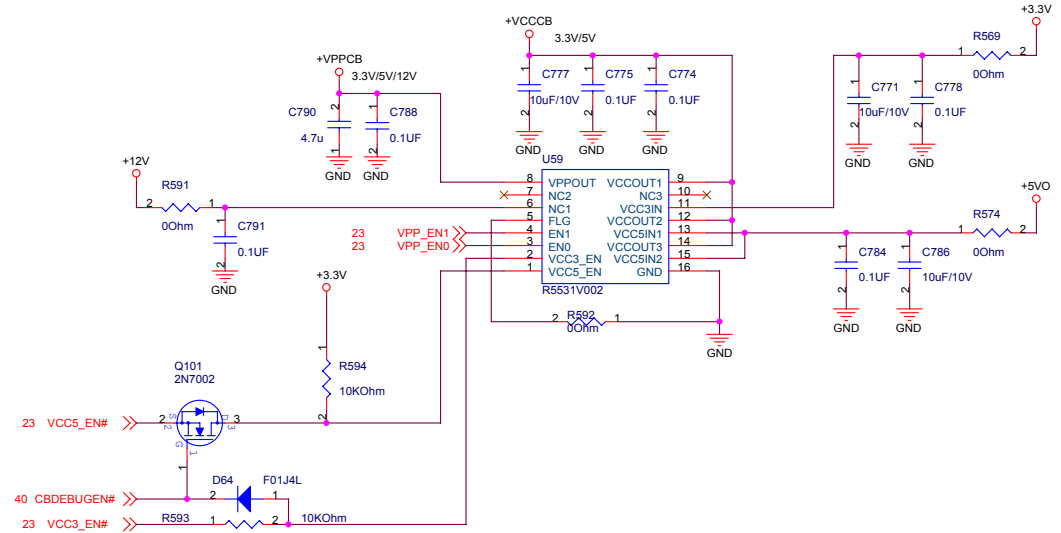
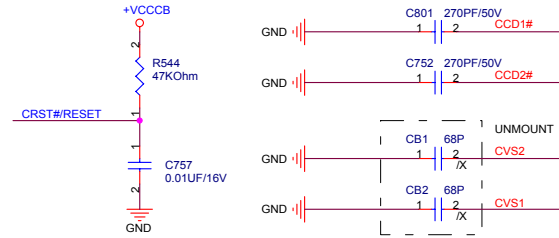
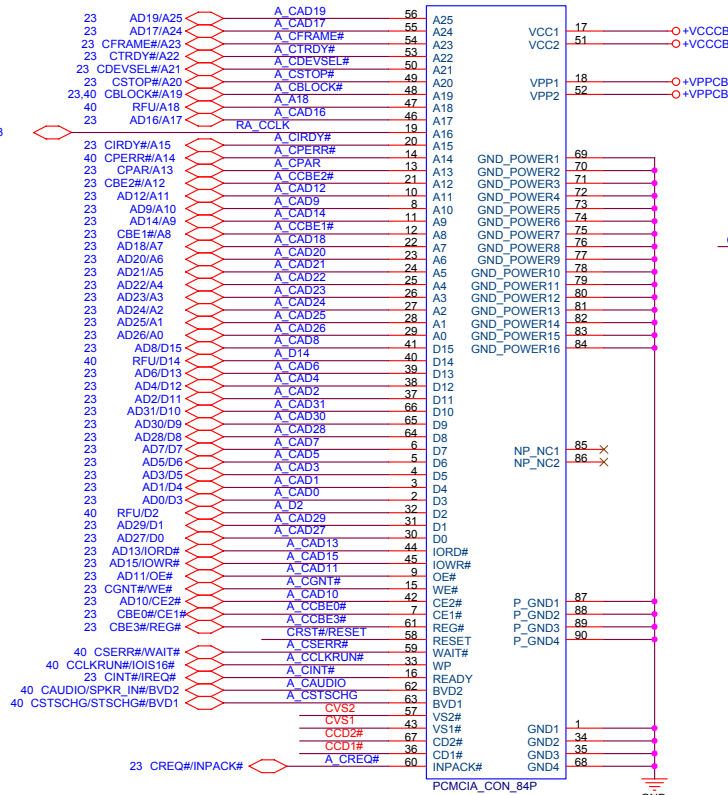
Intel Calexico(802.11a+802.11b)
 802.11b
 Tx: 500-526 mA
 Rx: 280-299 mA
 Sleep: 30 mA



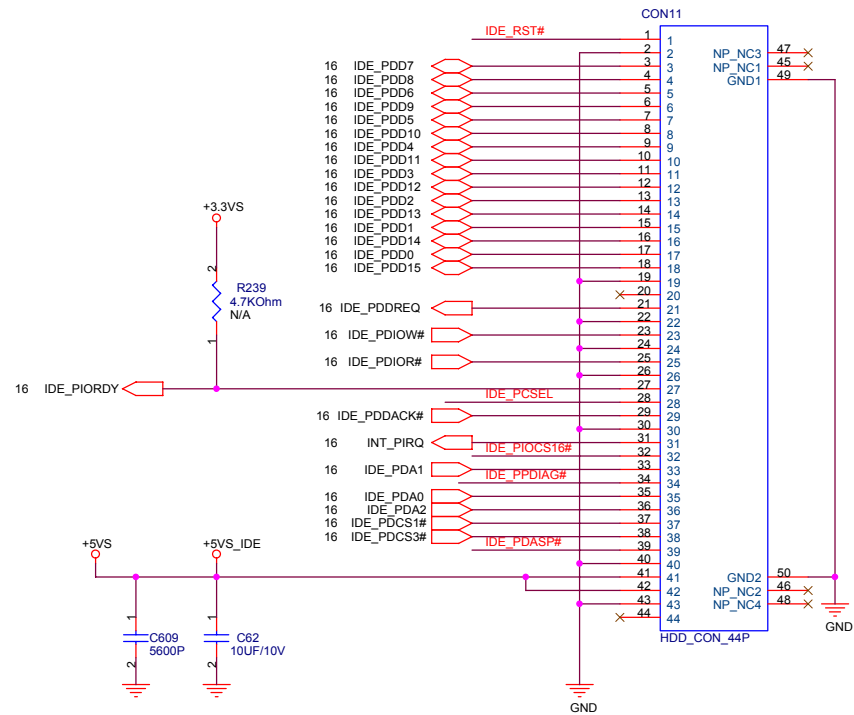
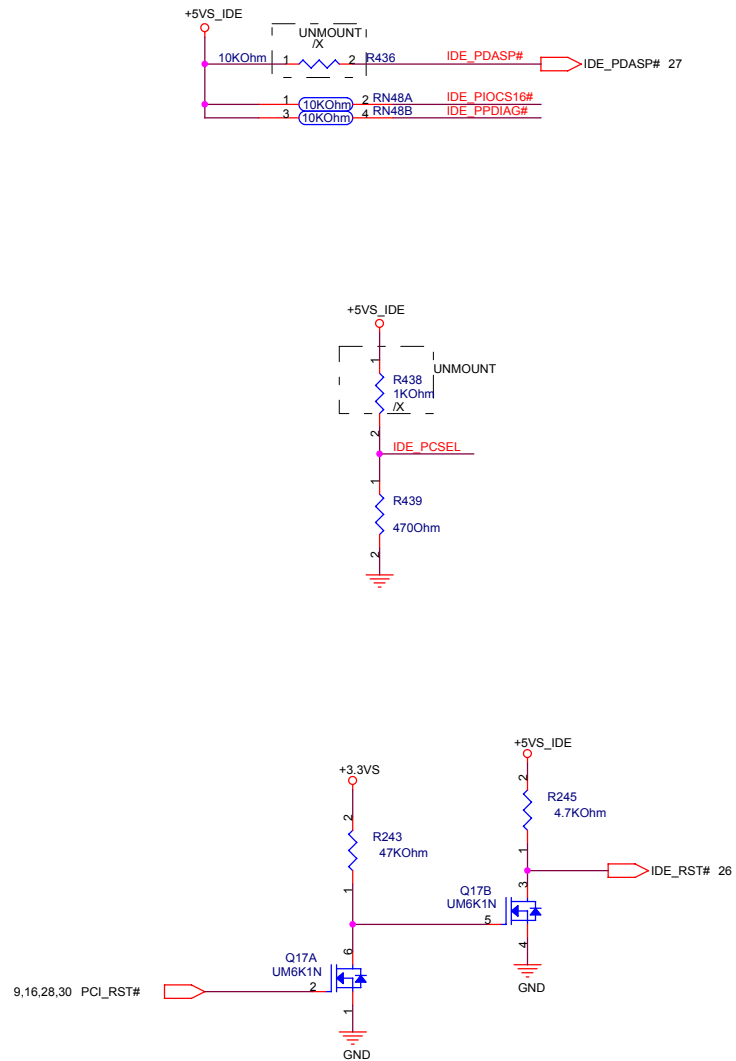


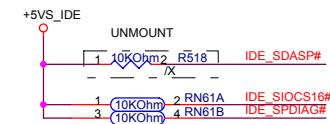
PCMCIA SOCKET

CON14

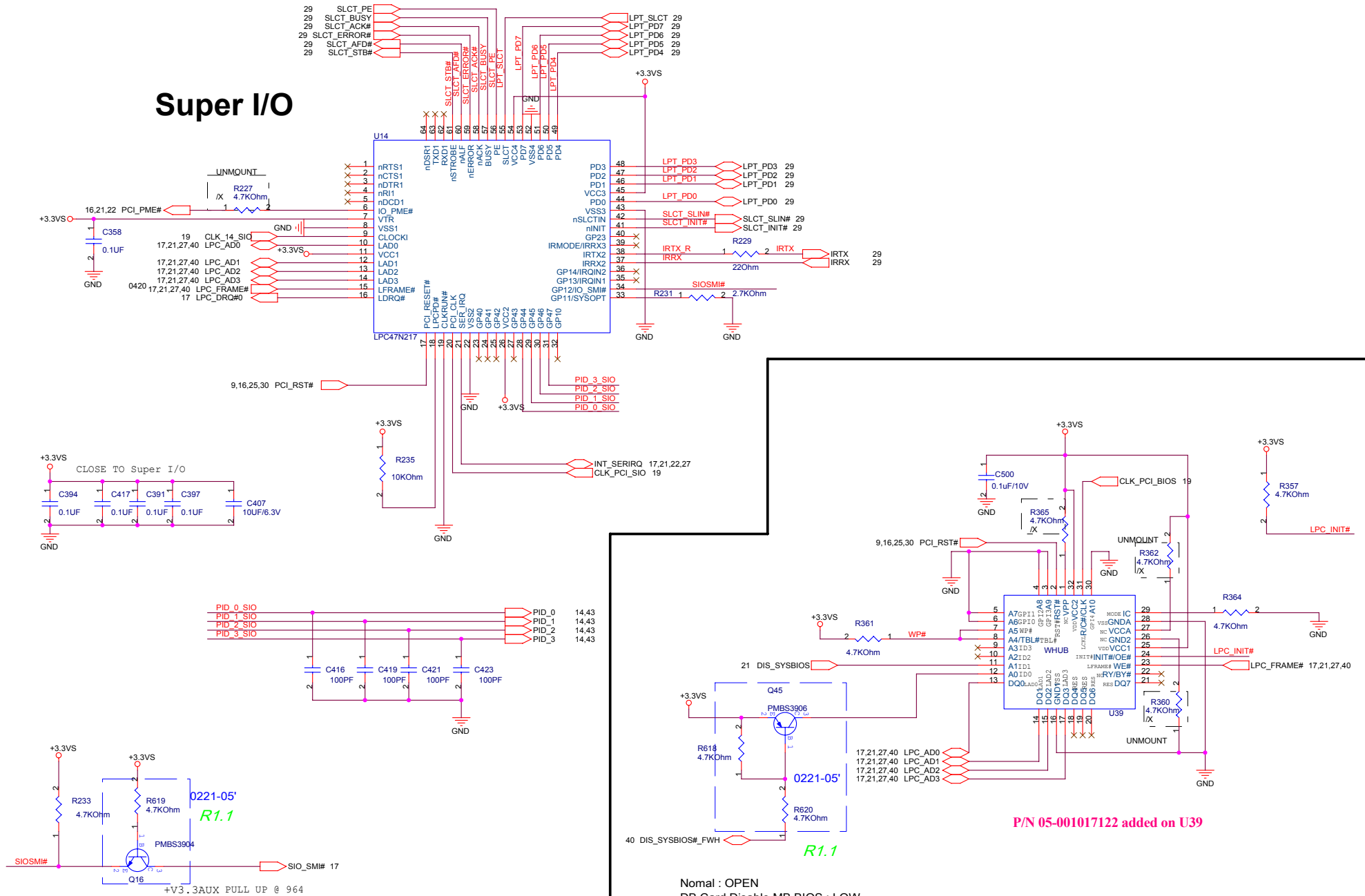


<Variant Name>

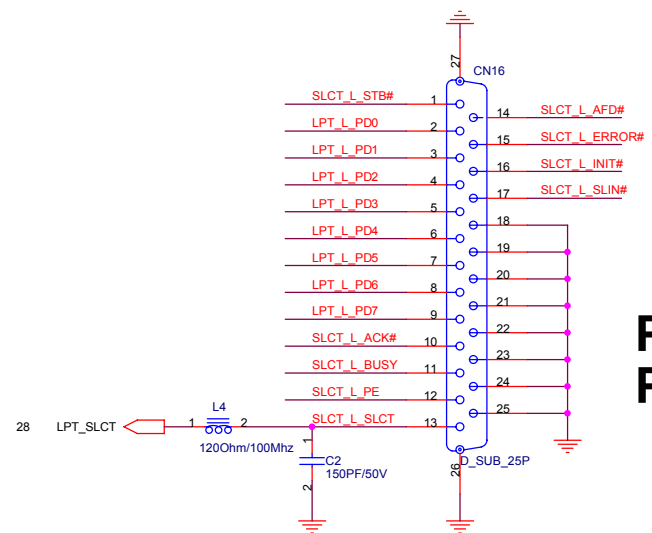
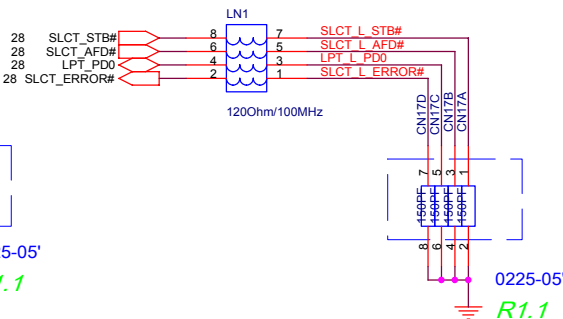
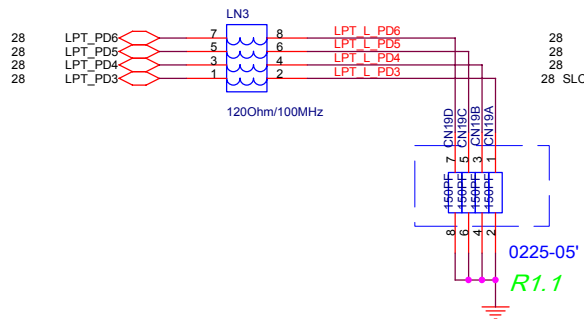
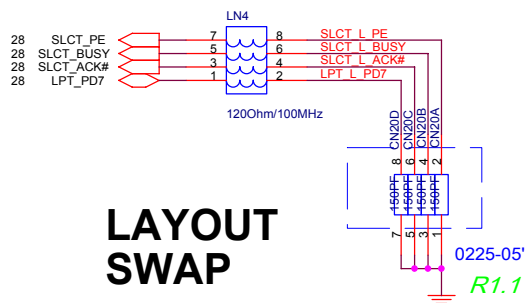
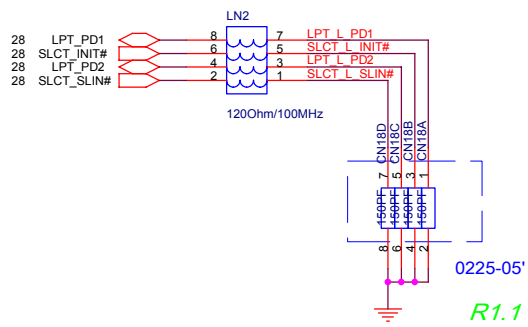




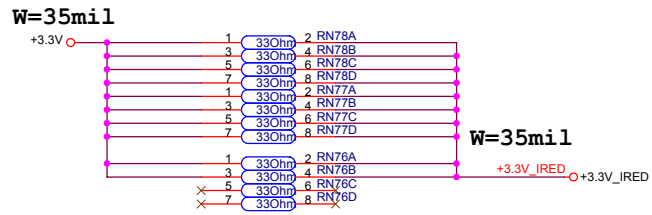
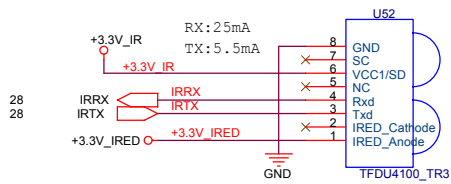
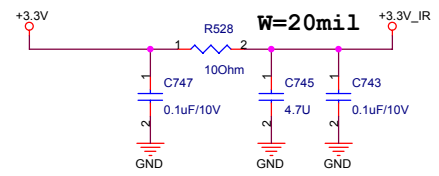
Super I/O



Normal : OPEN
DB Card Disable MB BIOS : LOW
DB Card Enable MB BIOS : HI
ID[0:3] : internal Pull-down 20K~100K



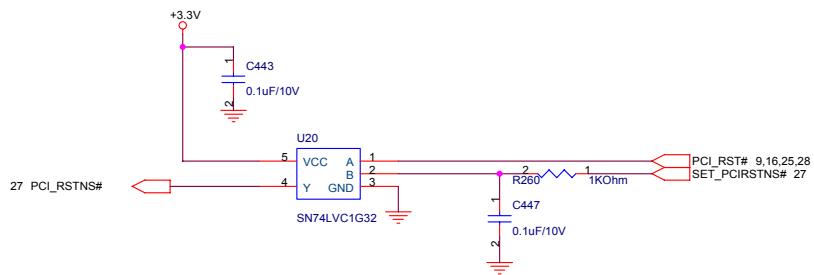
**PRINT
PORT**



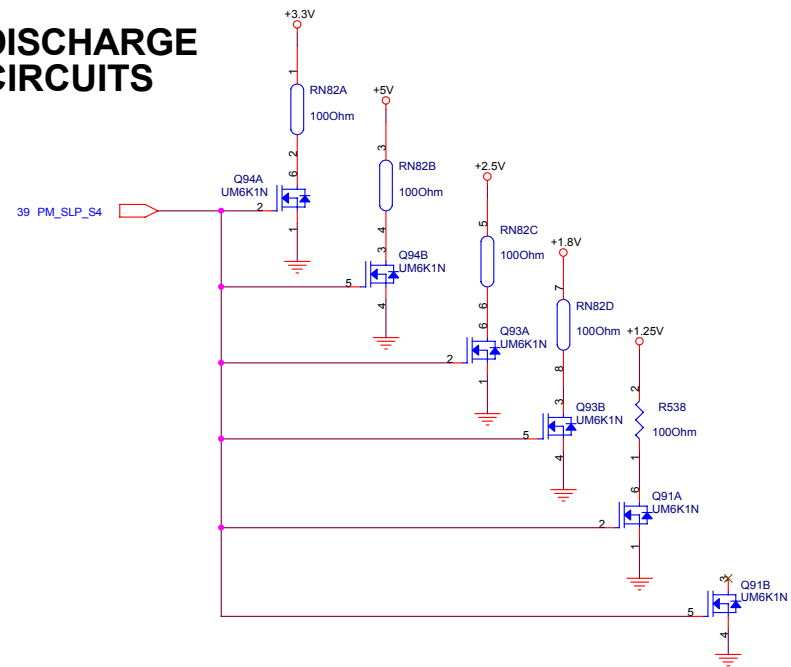
PCMCIA DEBUG Card

1105

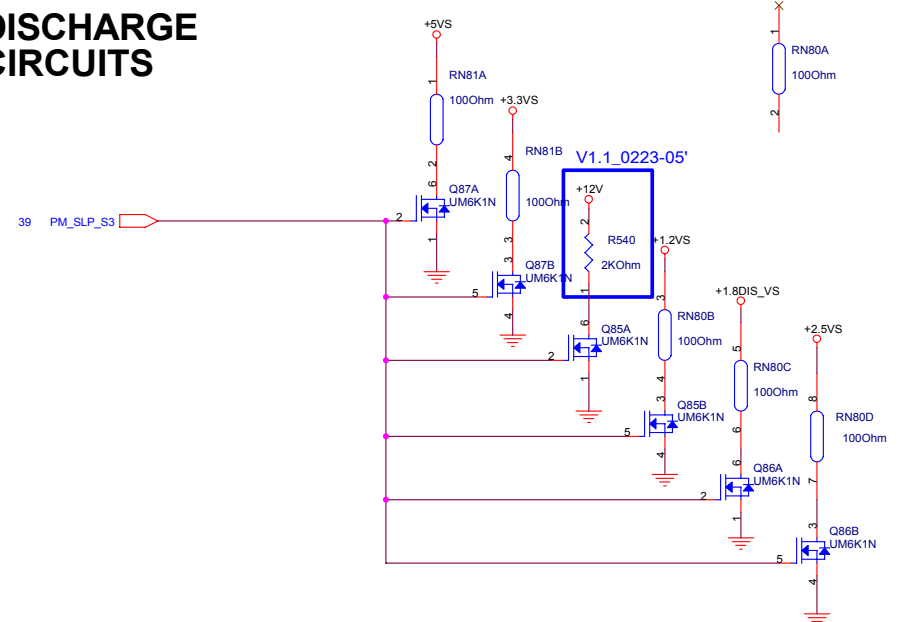
PCI_RSTNS# Gen Circuit

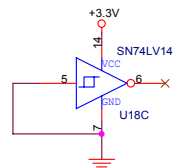


DISCHARGE CIRCUITS



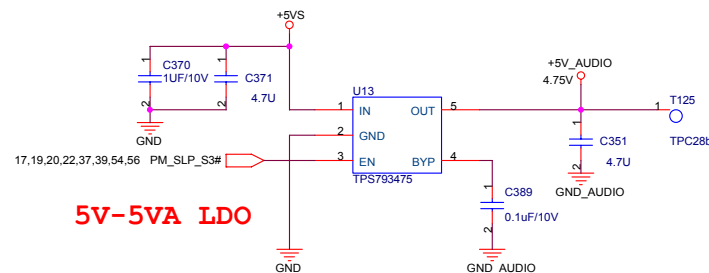
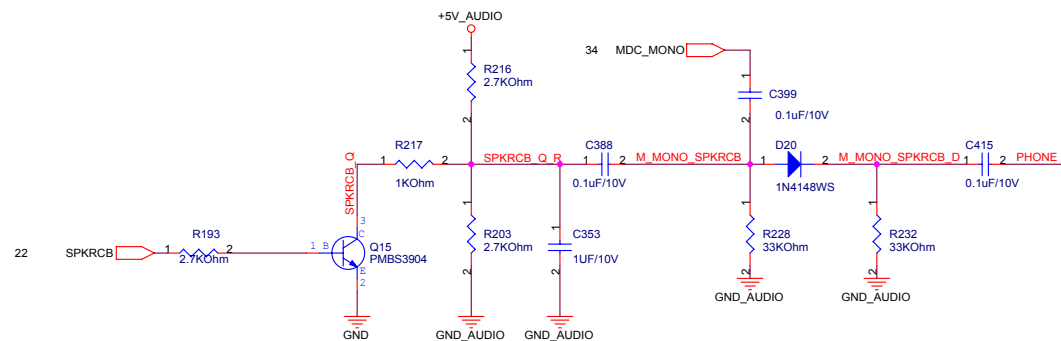
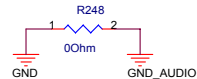
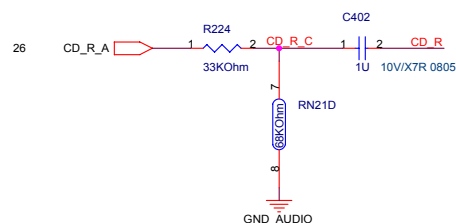
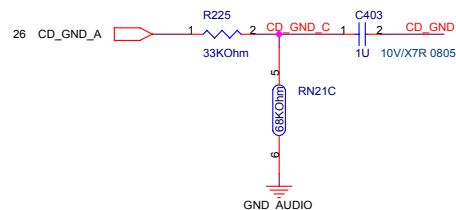
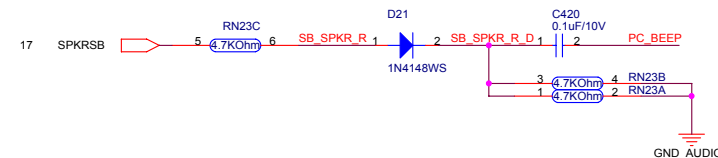
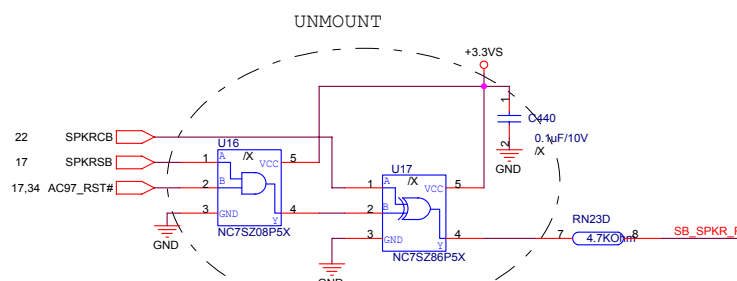
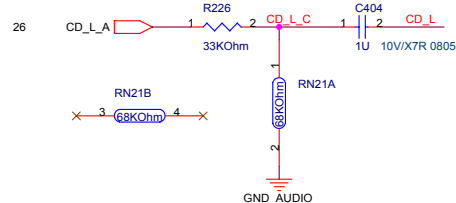
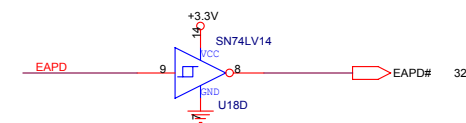
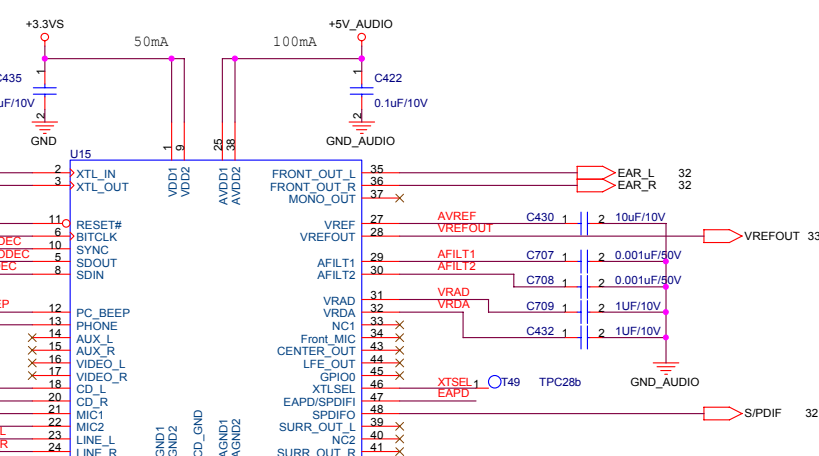
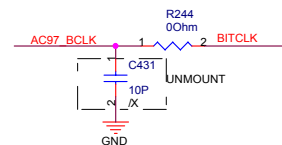
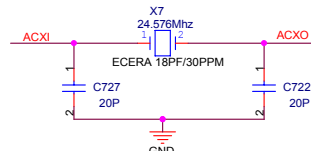
DISCHARGE CIRCUITS



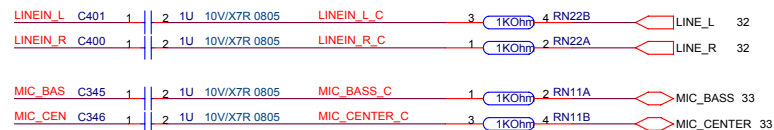


0.9 to 5.6
inches

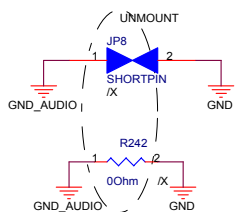
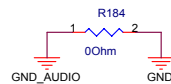
T type routing, place R at branch point.



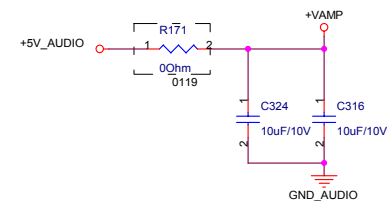
swap for layout



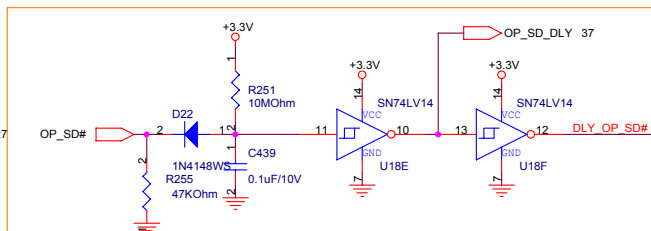
5V-5VA LDO



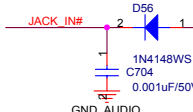
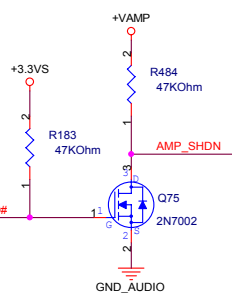
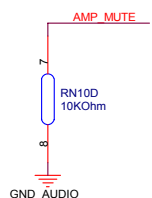
$f(\text{highpass}) = \frac{1}{2\pi \cdot 3.14 \cdot R \cdot C} = 73$
 $R = 32 \text{ Ohm}$ for Headphone, so $C = 68\mu\text{F}$
 But in order to reduce component type, use $100\mu\text{F}/6.3\text{V}$ (11-041210721), but $100\mu\text{F}$ is too big for A3N, so change to $47\mu\text{F}$.



LOSS U3202A~D



For reduce "POP" noise when system enter S3(suspend to RAM) or resume from S3. Net "OP_SD#" should be pull low by KBC controller when system at S3 mode.

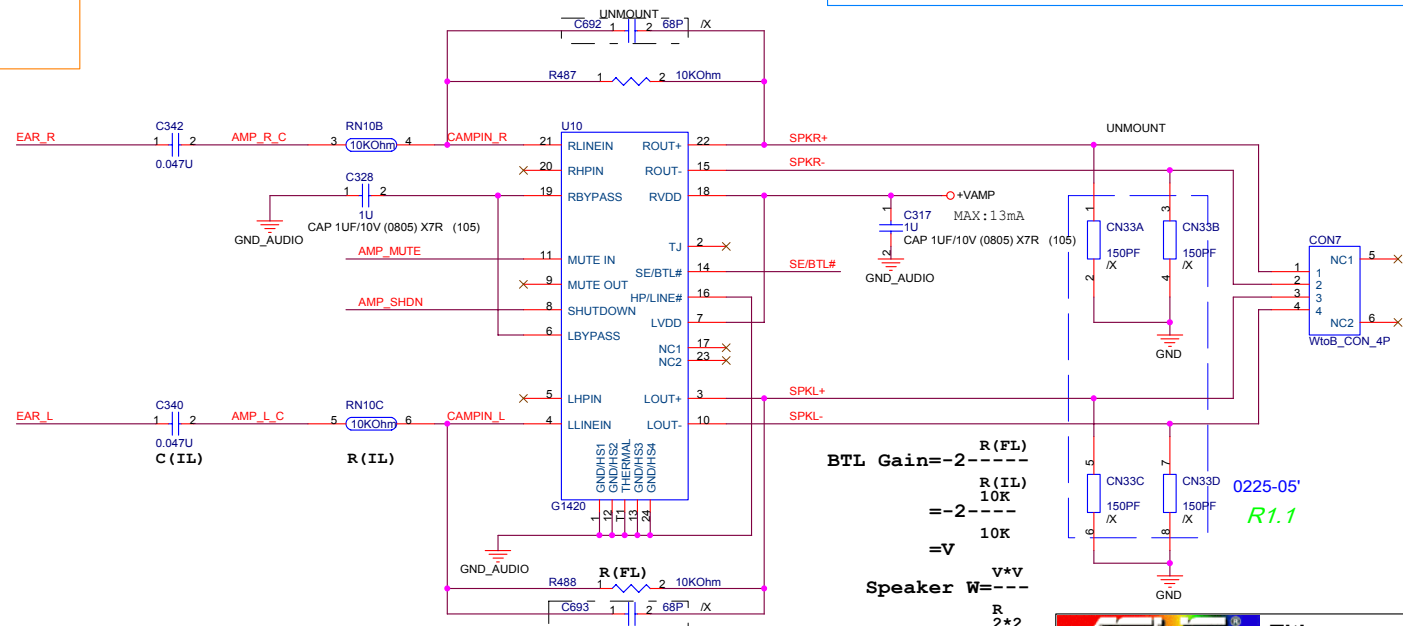
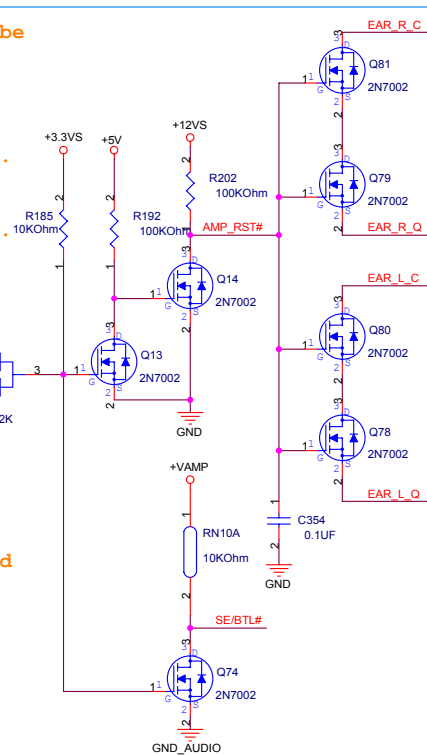


$$f(\text{highpass}) = \frac{1}{2\pi \cdot 3.14 \cdot C(\text{IL}) \cdot R(\text{IL})} = 500$$

$$f(\text{lowpass}) = \frac{1}{2\pi \cdot 3.14 \cdot C(150\text{P}) \cdot R(10\text{K})} = 106\text{K}$$

Pop noise can be heard via headphone when system boot, restart and resume from S3. Add OP_SD# to control the turn-on timing.

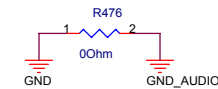
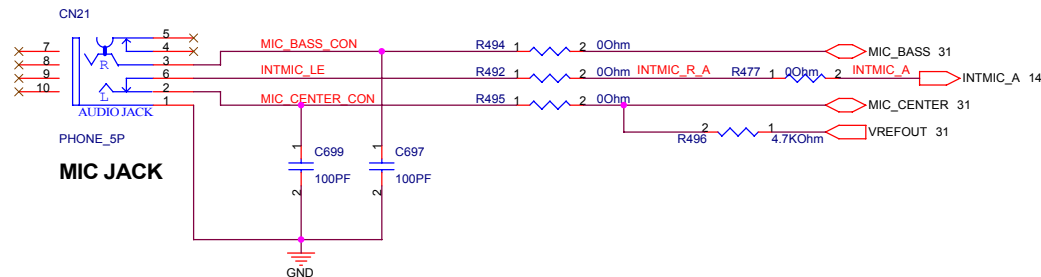
But when system resume from S3, pop noise is behind OP_SD# pull high. Add a delay circuit to prevent it.



BTL Gain = -2
 $R(\text{FL}) = 10\text{K}$
 $R(\text{IL}) = 10\text{K}$
 $= -2$
 $= V$
 Speaker $W = \frac{V^2}{R}$
 $R = 2 \times 2 = 4\text{ohm}$
 $= 1\text{W}$
 Can use 1W(4ohm) speaker

MIC OP CIRCUIT

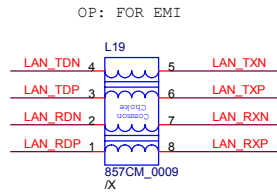
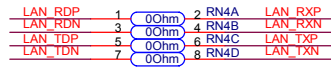
MIC JACK



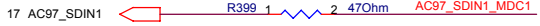
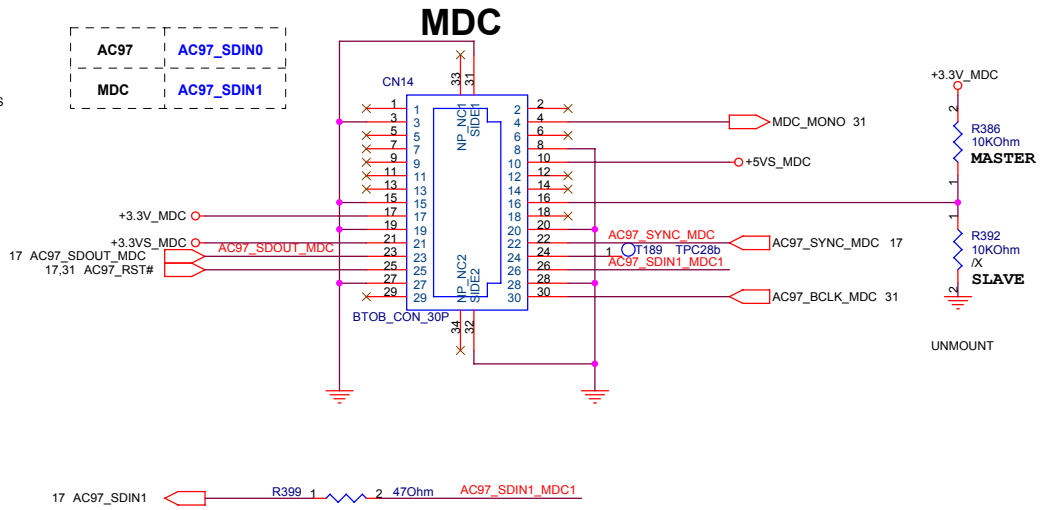
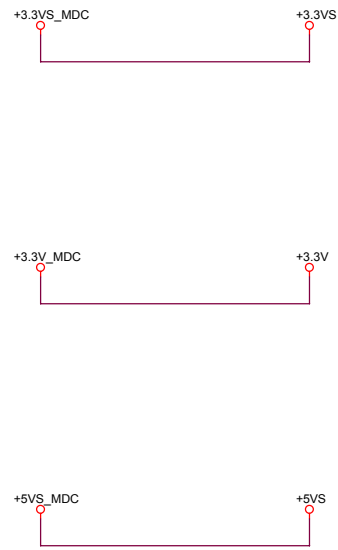
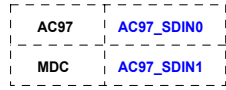
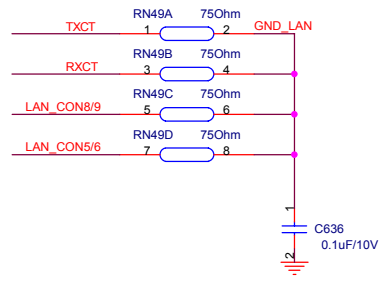
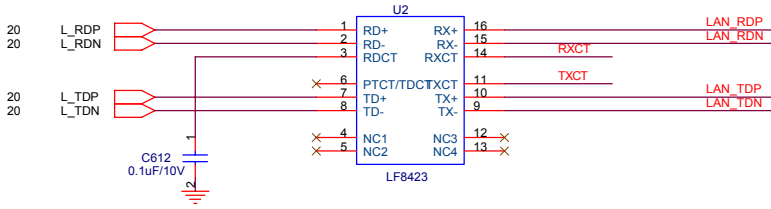
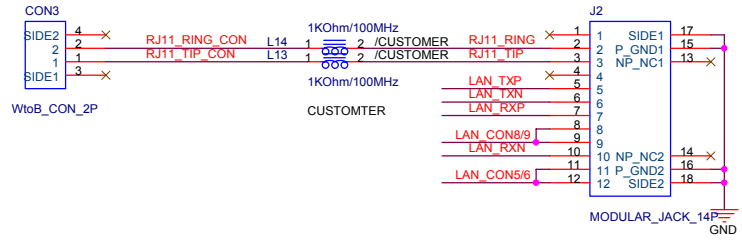
INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils

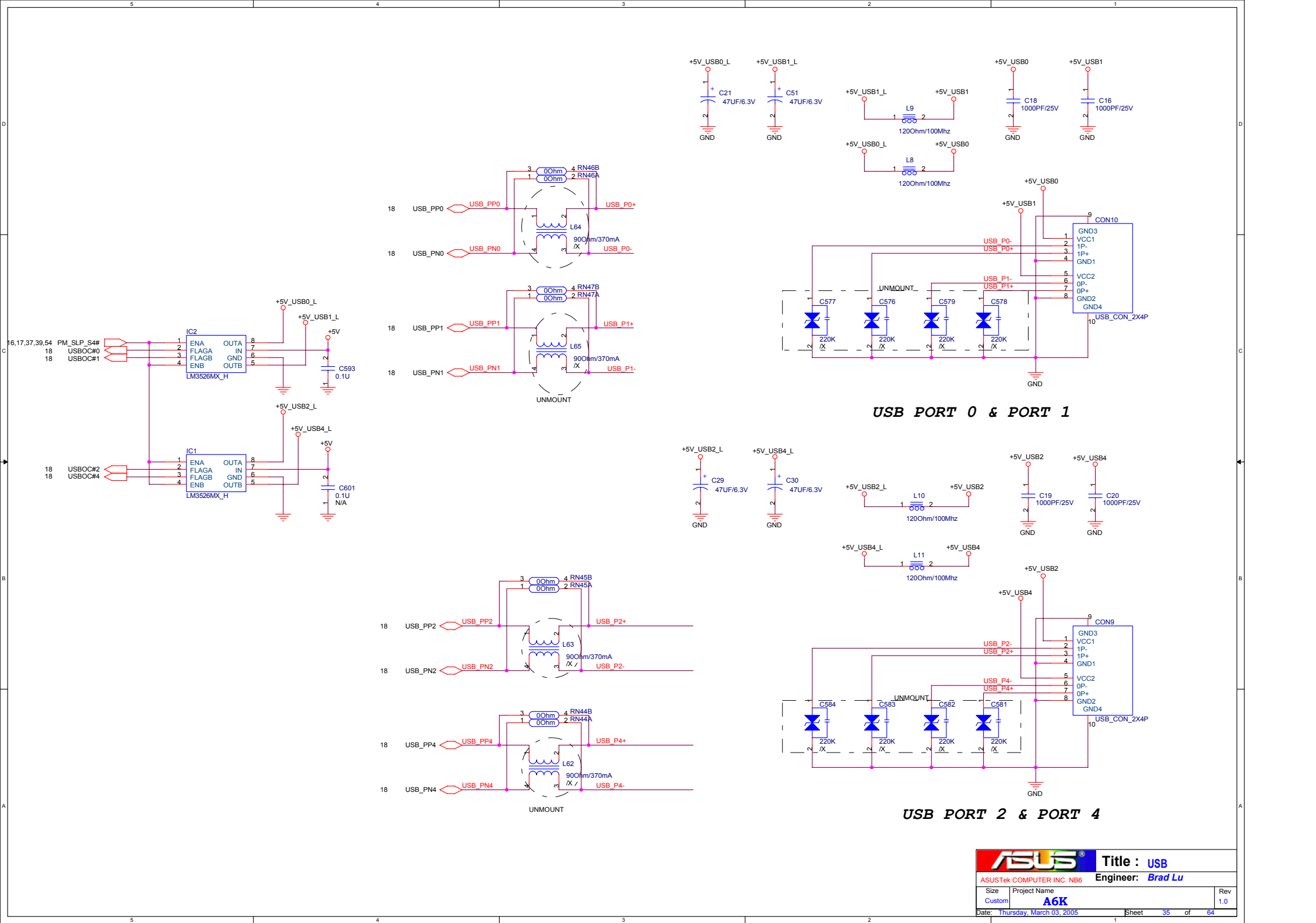
R111 & R112
change to
09-013103013
in R1.2 BOM

ASUS		Title : MIC	
ASUSTek COMPUTER INC. NB6		Engineer: Brad Lu	
Size Custom	Project Name A6K	Date: Thursday, March 03, 2005	Rev 1.0
Sheet 33 of 64			

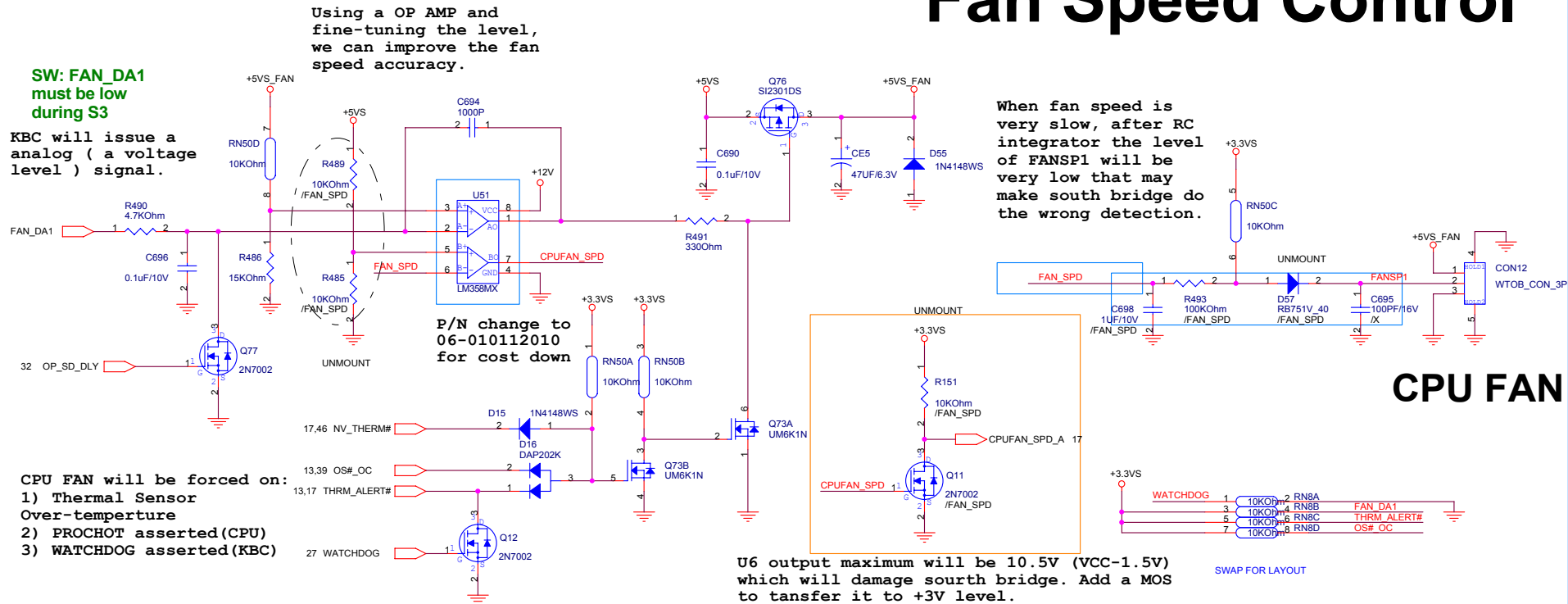


UNMOUNT





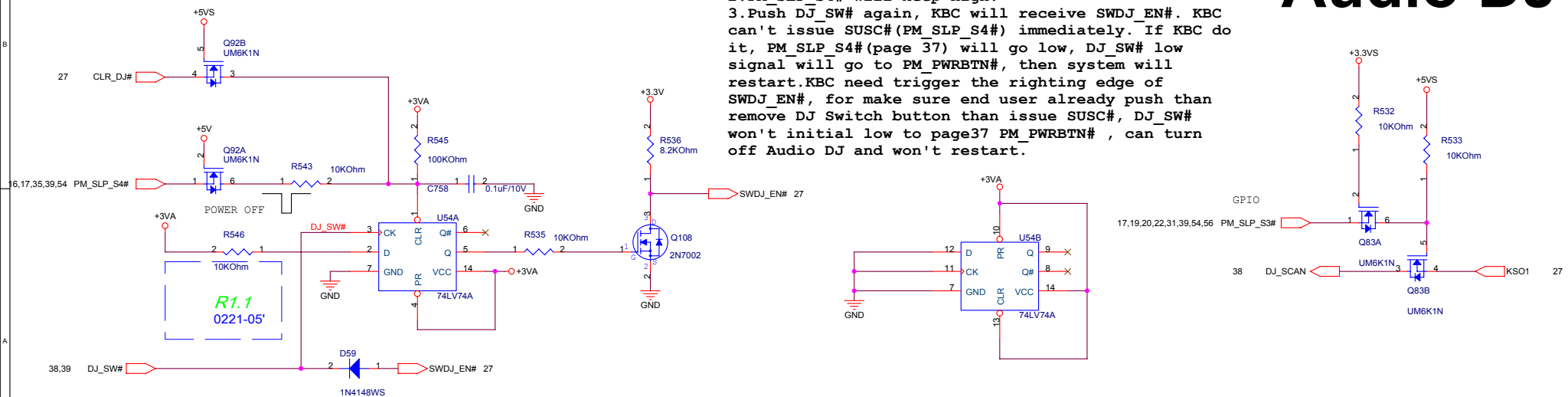
Fan Speed Control

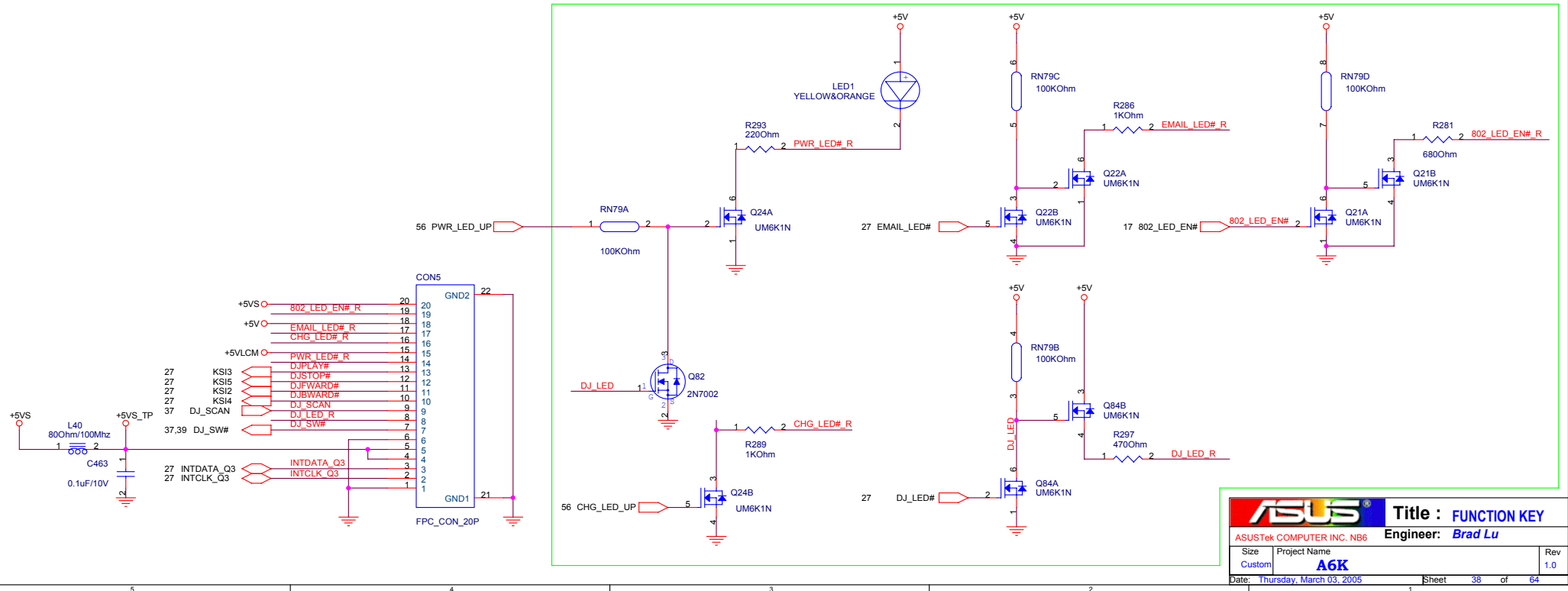
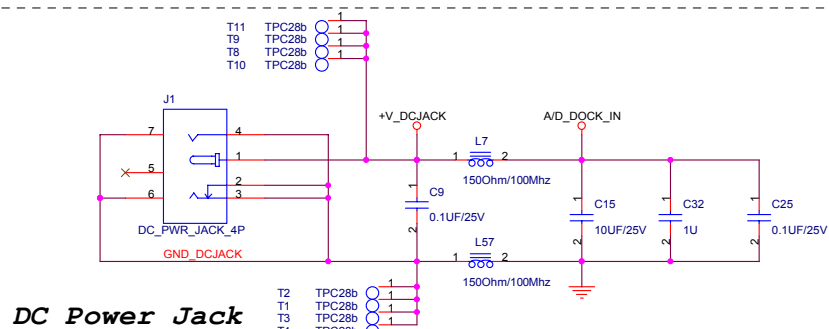
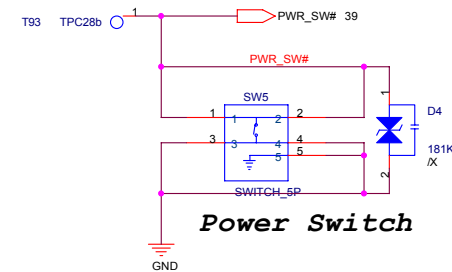
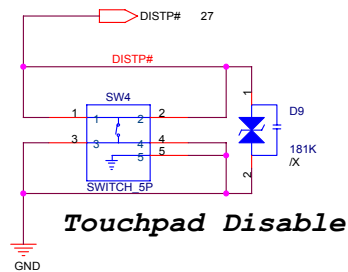
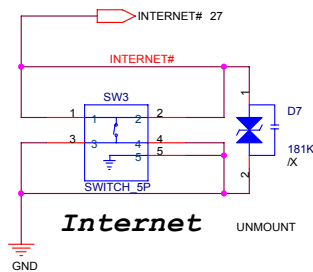
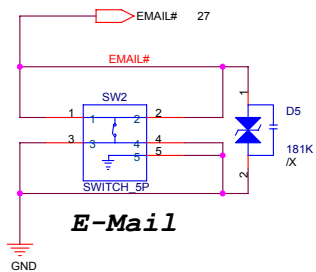
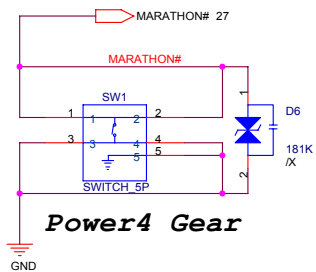


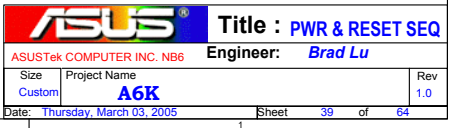
Audio DJ

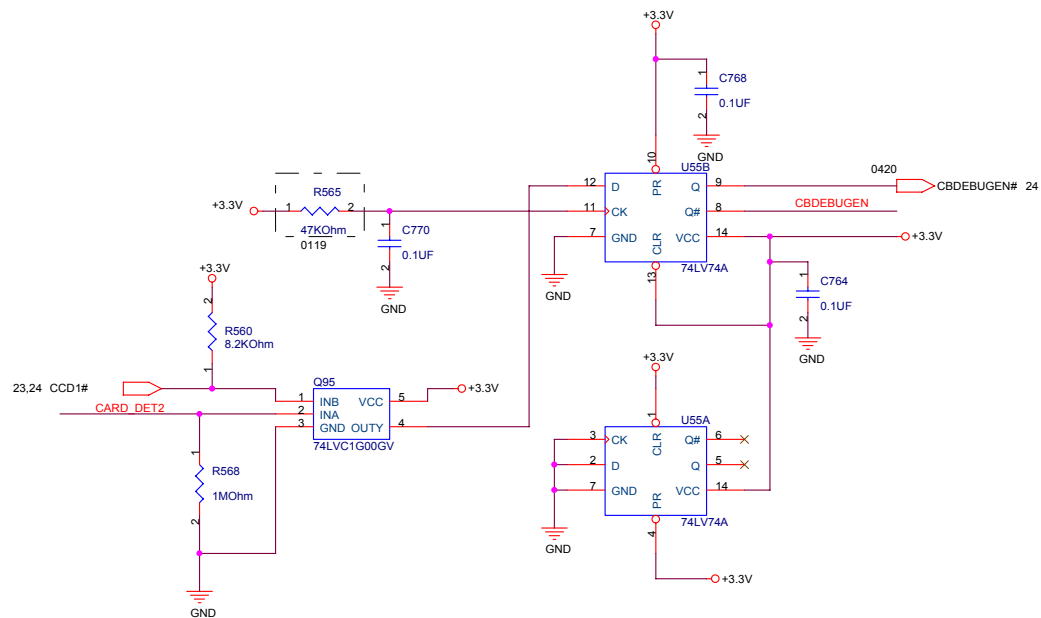
SWDJ_EN# function :

- 1.Push DJ_SW#, turn on Audio DJ.
- 2.PM_SLP_S4# will keep high.
- 3.Push DJ_SW# again, KBC will receive SWDJ_EN#. KBC can't issue SUSC#(PM_SLP_S4#) immediately. If KBC do it, PM_SLP_S4#(page 37) will go low, DJ_SW# low signal will go to PM_PWRBTN#, then system will restart.KBC need trigger the righting edge of SWDJ_EN#, for make sure end user already push than remove DJ Switch button than issue SUSC#, DJ_SW# won't initial low to page37 PM_PWRBTN# , can turn off Audio DJ and won't restart.







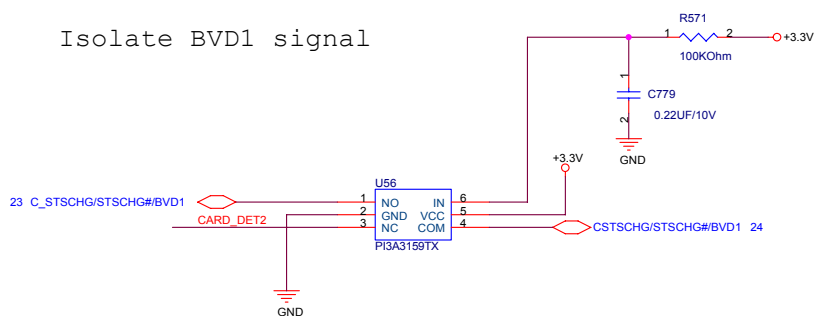


PCMCIA DEBUG PORT

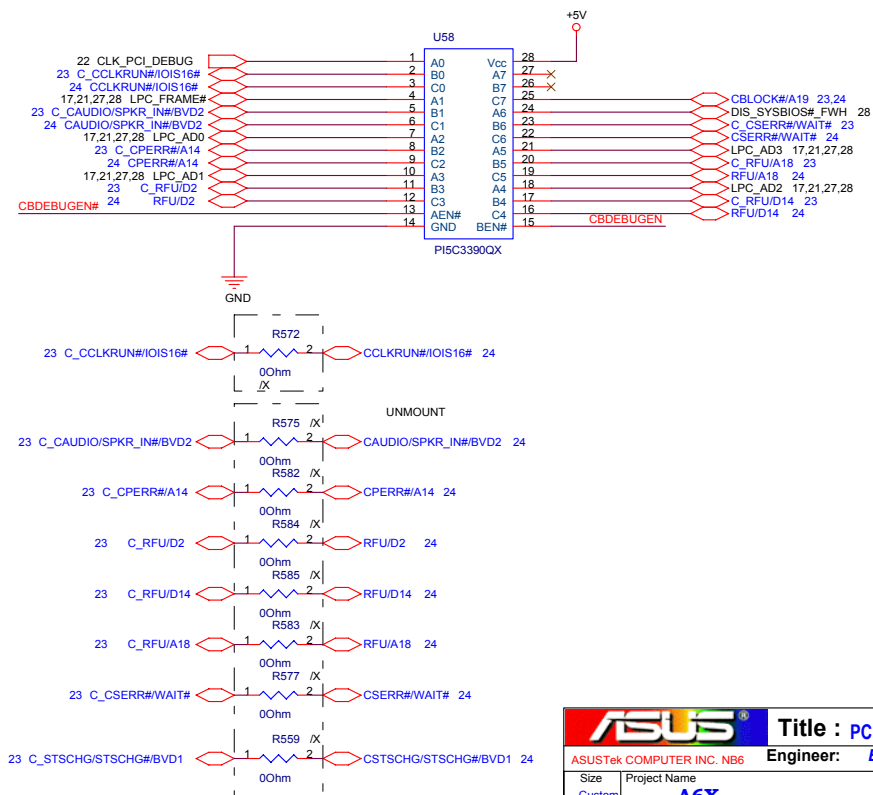
Isolate card bus control and slot signal when debug card plug in

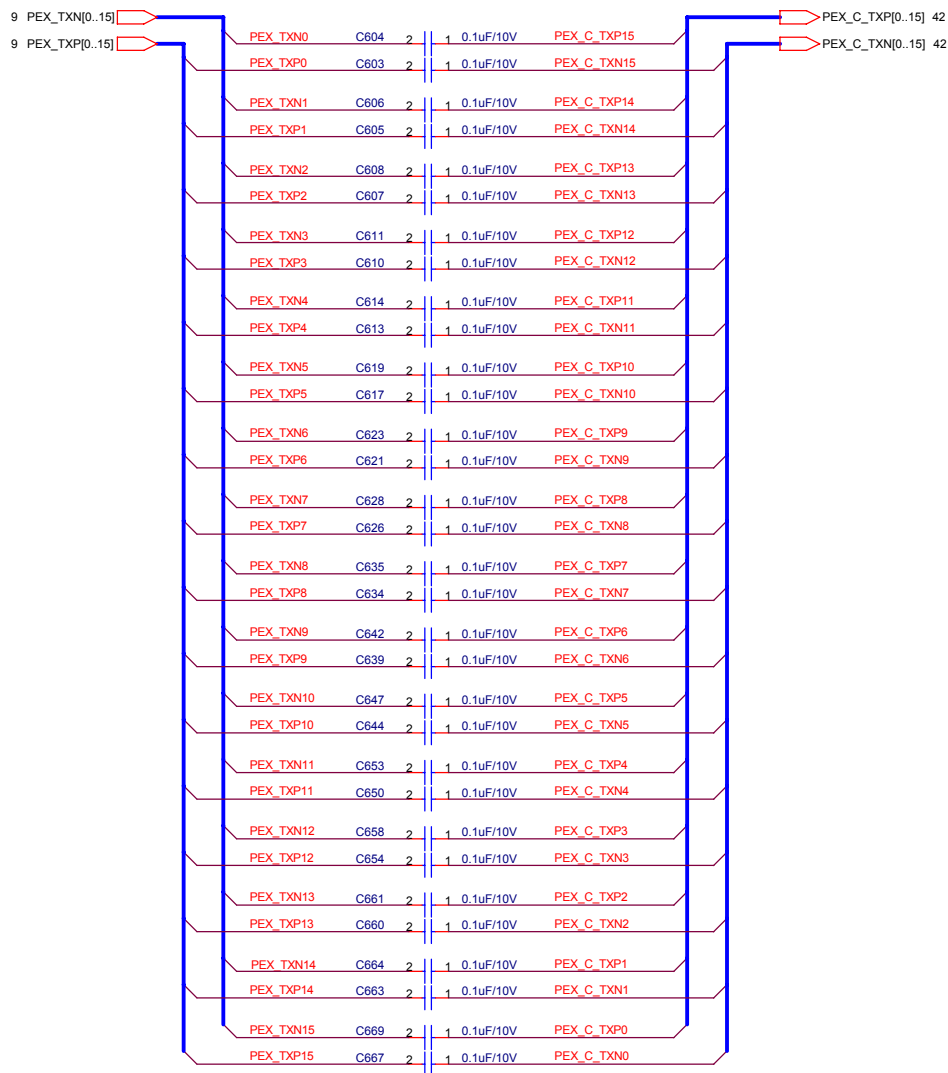
RC value may need to be tuned for each product.

Isolate BVD1 signal



When +3V on, select BVD1 to CARD_DET2 for RC delay time





PLACE these 0402 AC coupling caps close to sis756.

TX P&N [0..15] PIN SWAP FOR LAYOUT

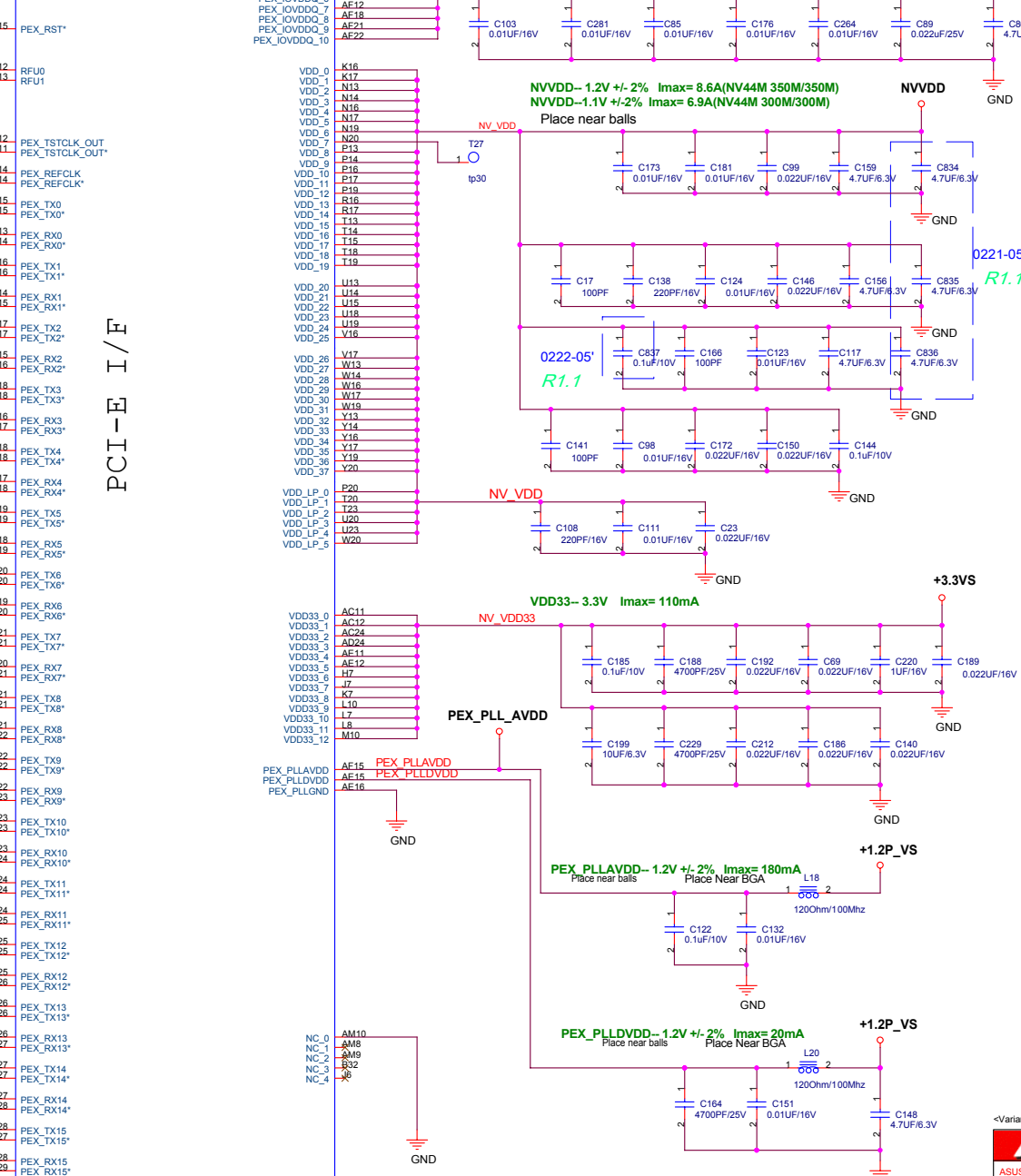
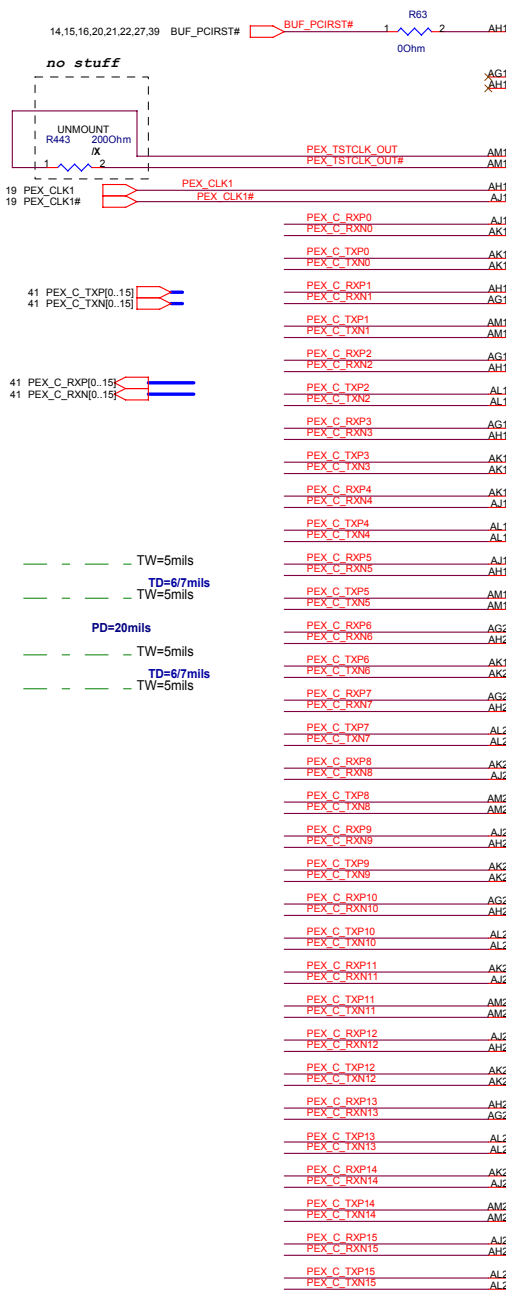


PLACE these 0402 AC coupling caps close to nv44m

RX P&N 0.2.7.9.11.13.14.15 PIN SWAP FOR LAYOUT

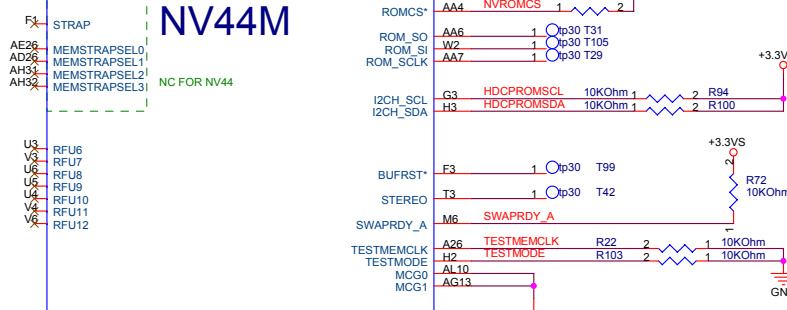
NV44M

PCI-E I/F



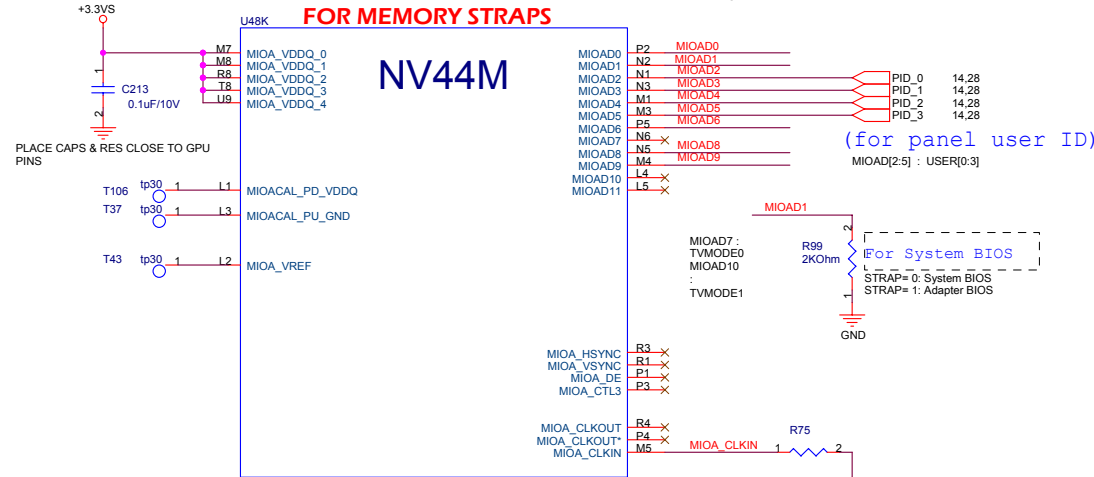
FOR MEMORY STRAPS

NV44M



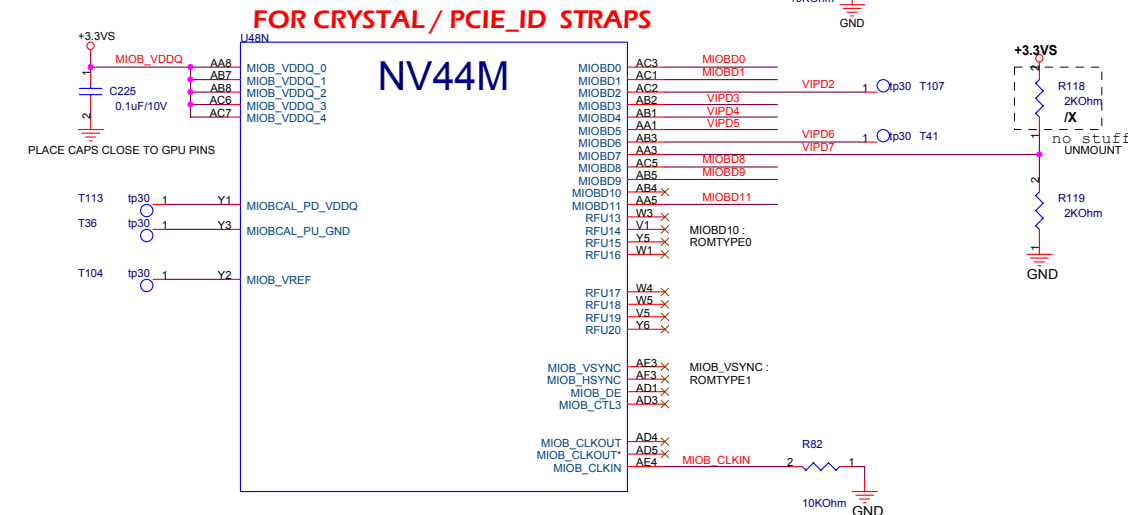
FOR MEMORY STRAPS

NV44M



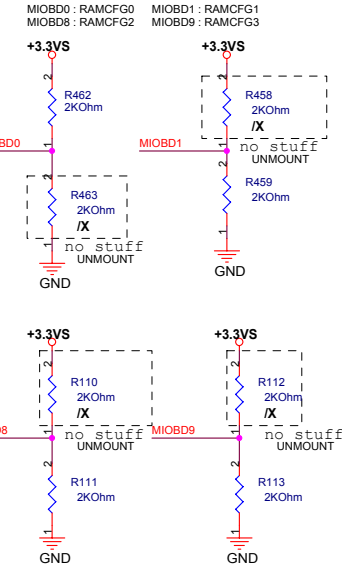
FOR CRYSTAL / PCIE_ID STRAPS

NV44M



MEM TYPE STRAP

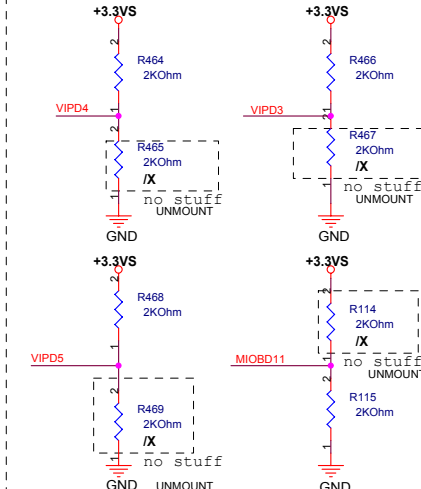
NV44M memory strap setting:
01 (0001) SAMSUNG 8MX32X2 64MB (two VRAM) -> 1.8V
01 (0001) HYNIX 8MX32X2 64MB (two VRAM) -> 1.8V
04 (0100) SAMSUNG 4MX32X2 32MB (two VRAM) -> 1.8V
09 (1001) HYNIX 4MX32X1 32MB (one VRAM) -> 1.8V
0C (1100) SAMSUNG 4MX32X1 16MB (one VRAM) -> 1.8V



(PCI_DEVICE_ID)

MIOBD4 : PCI_DEVICE0
MIOBD5 : PCI_DEVICE1
MIOBD3 : PCI_DEVICE2
MIOBD11 : PCI_DEVICE3

NV44M - ID 0X0168
NV44M-V- ID 0X0167

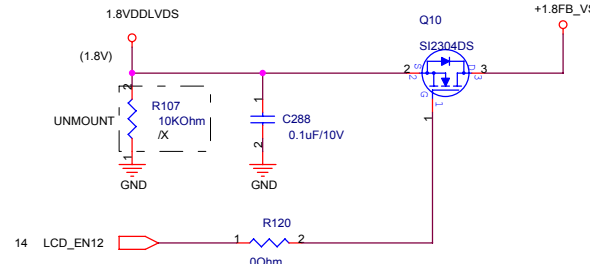
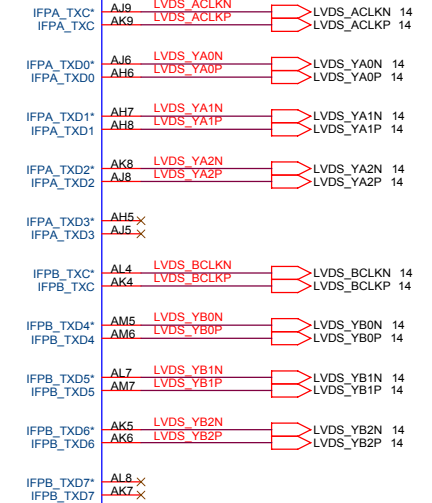
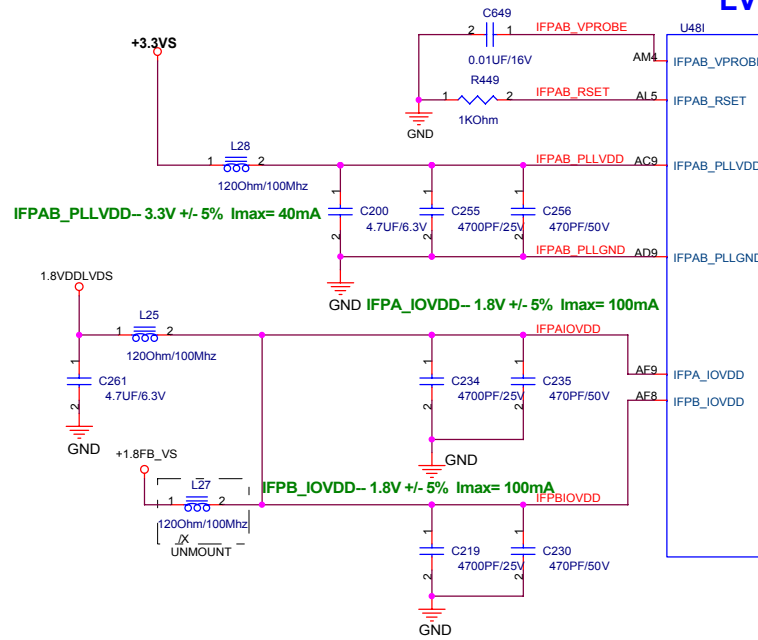


NV44M

GND

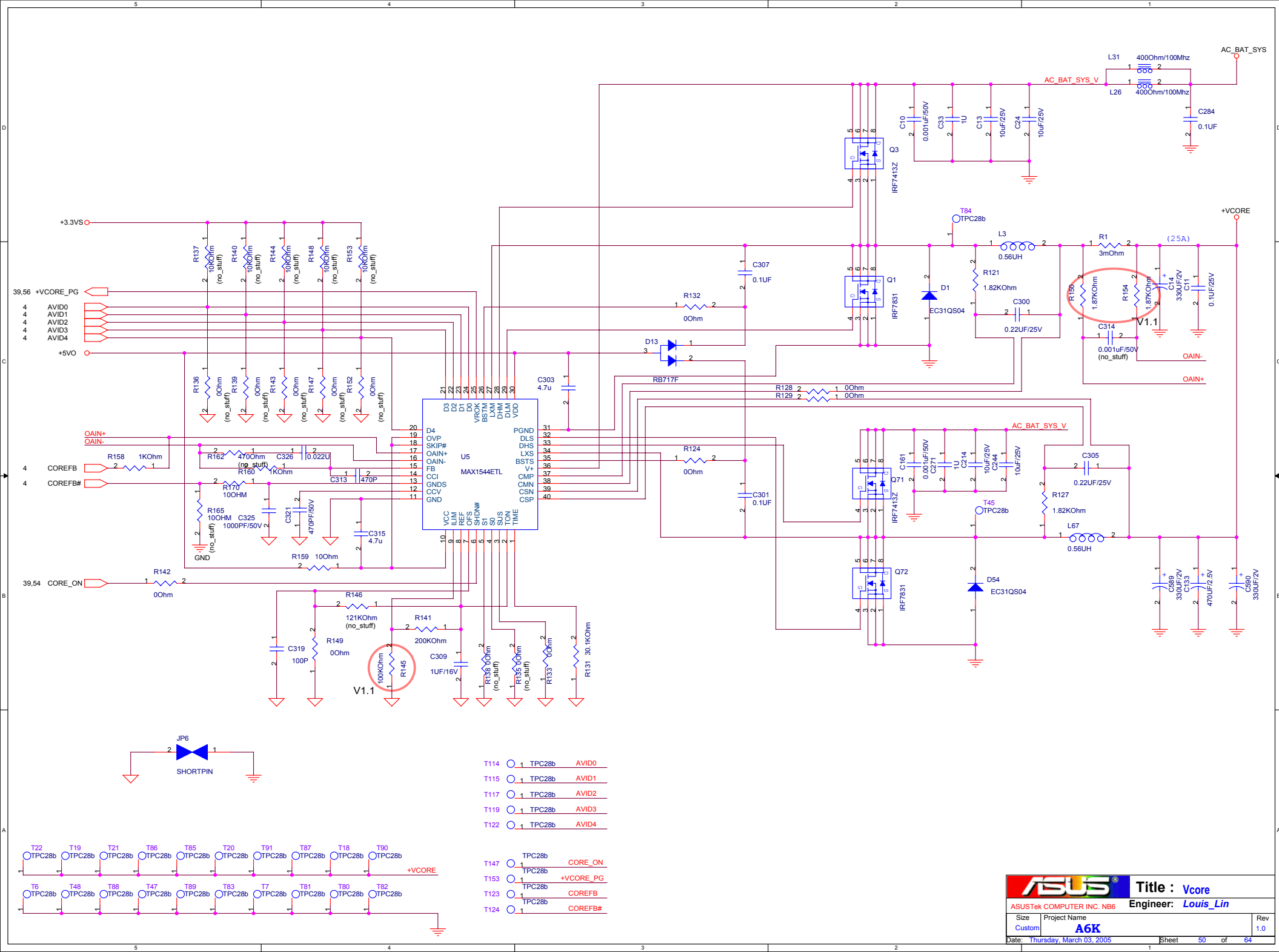
LVDS/Panel control

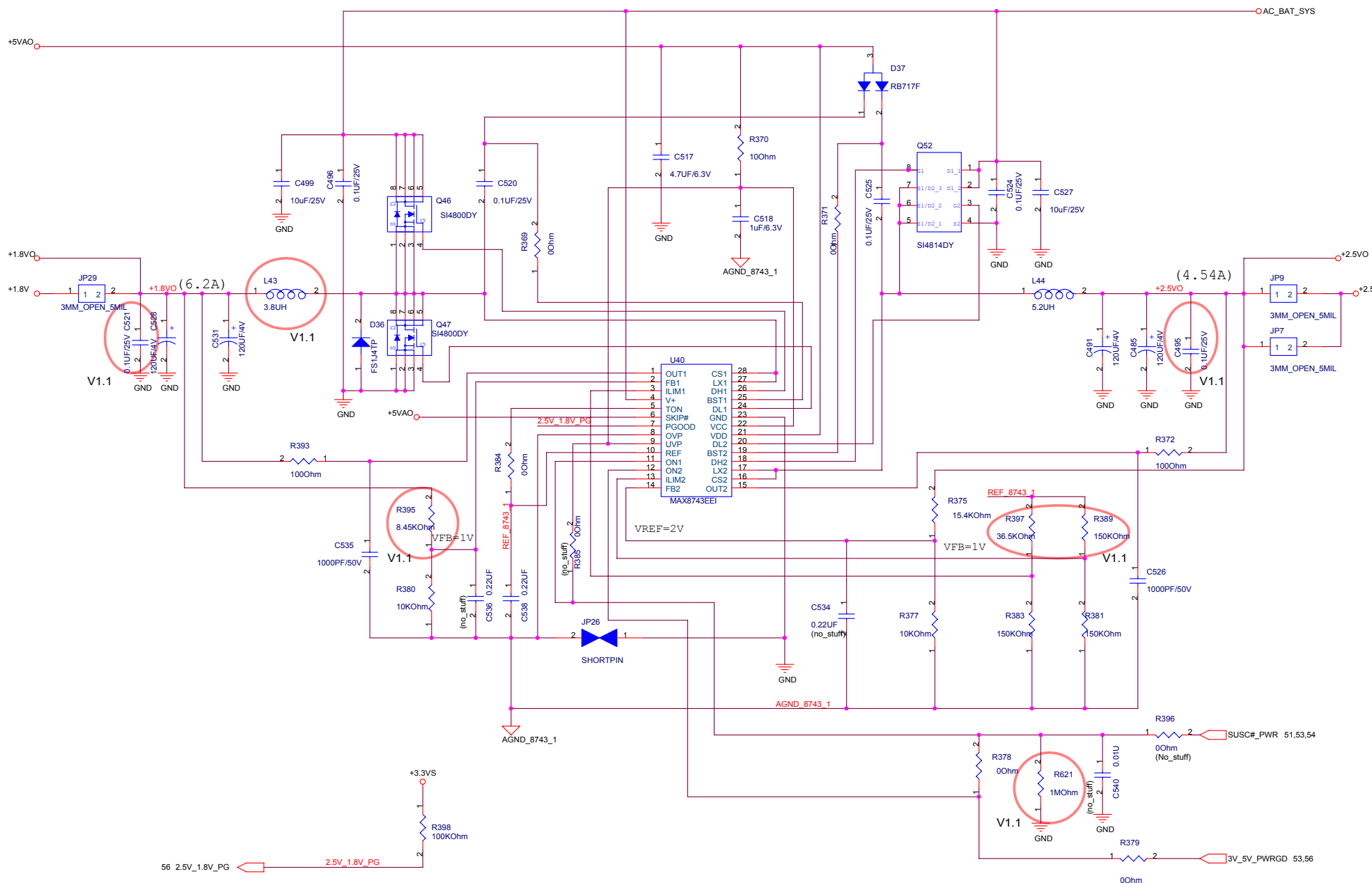
NV44M

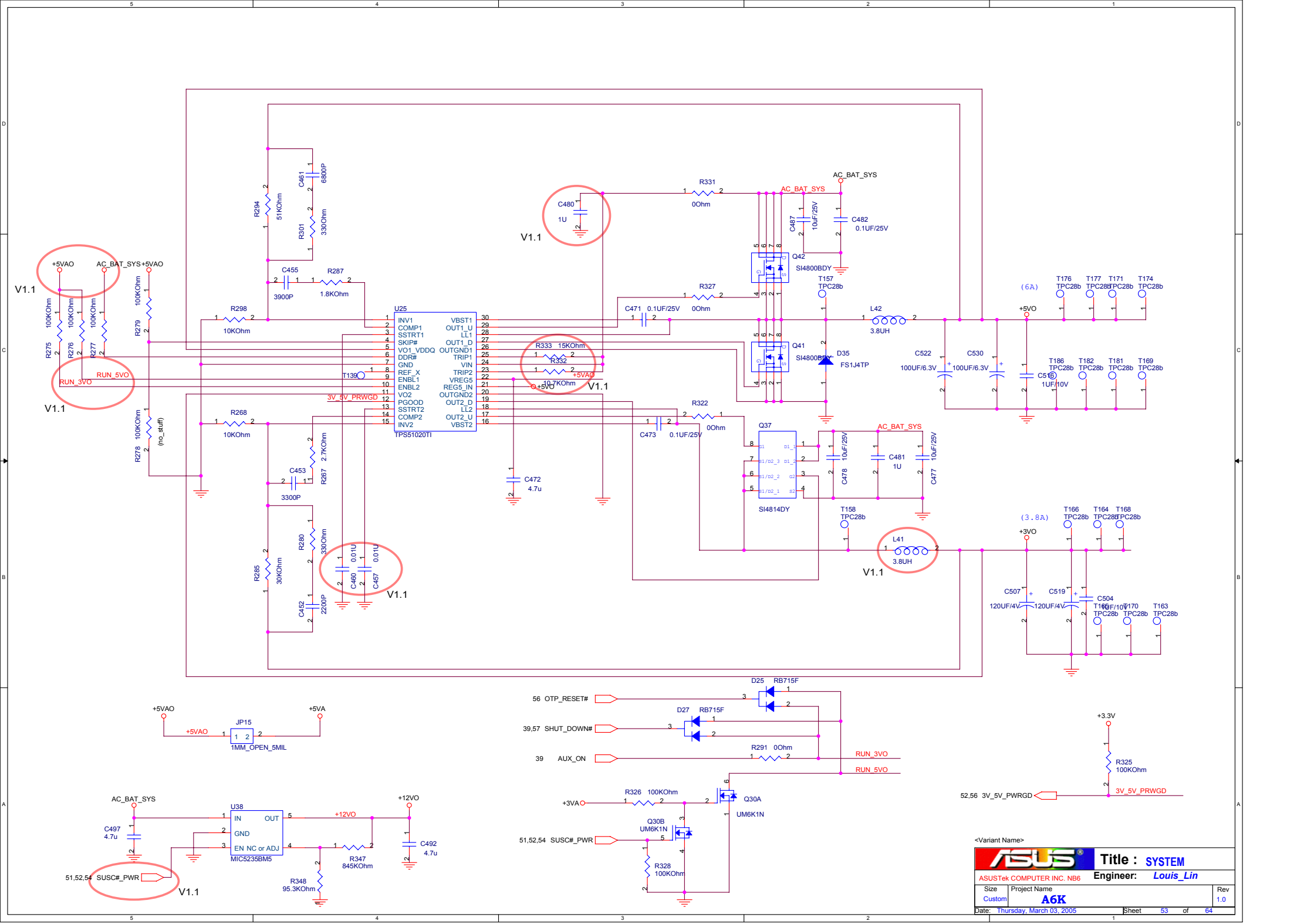


<Variant Name>

		Title : NV44M LVDS	
ASUSTek COMPUTER INC		Engineer: Brad Lu	
Size	Project Name		Rev 1.0
Custom	A6K		
Date: Thursday, March 03, 2005		Sheet 44	of 64







$$+V_{bat} = (R1+R2) / R2 * 4.2$$

$$+V_{bat} = (30k+10k) / 10k * 4.2 = 16.8V$$

$$V+INE2 = 24.5 * I_{chg}(A) * R_{s1}$$

$$V+INE2 = 24.5 * 2.5(A) * 0.050 = 3.062V \quad V_{ref} = 5.000V$$

$$DEFAULT \ R(1ow) = 100K$$

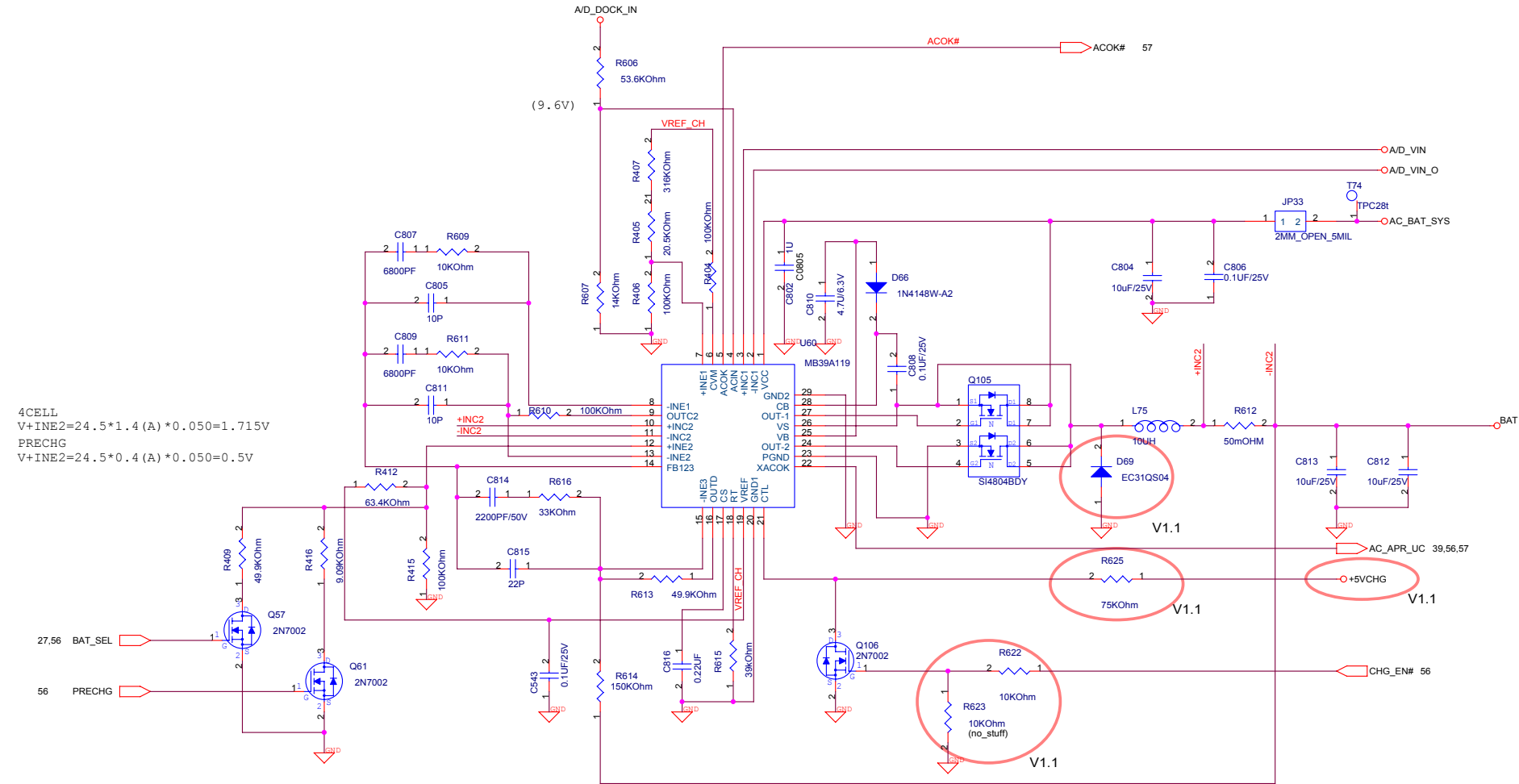
$$R(hi) = (5/3.062-1) * 100K = 63.3K$$

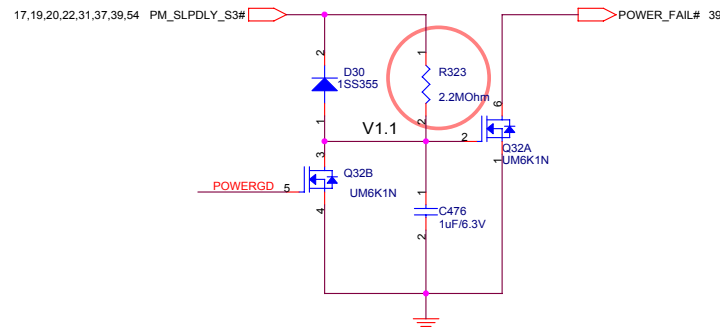
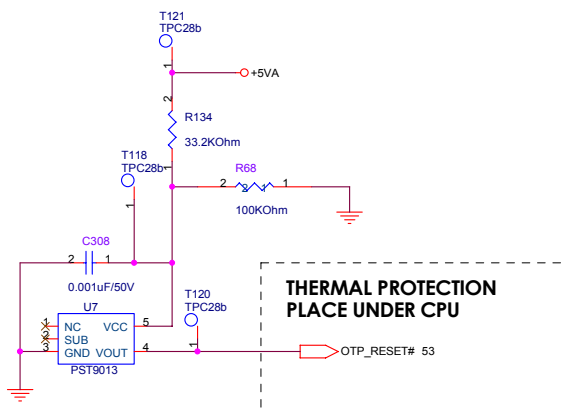
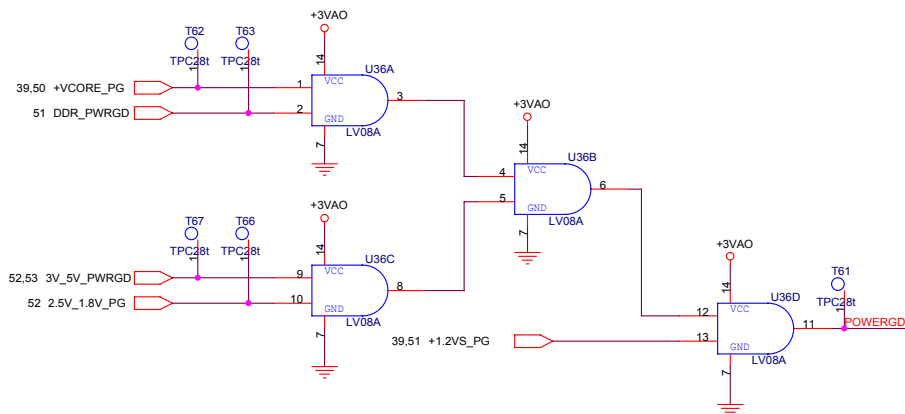
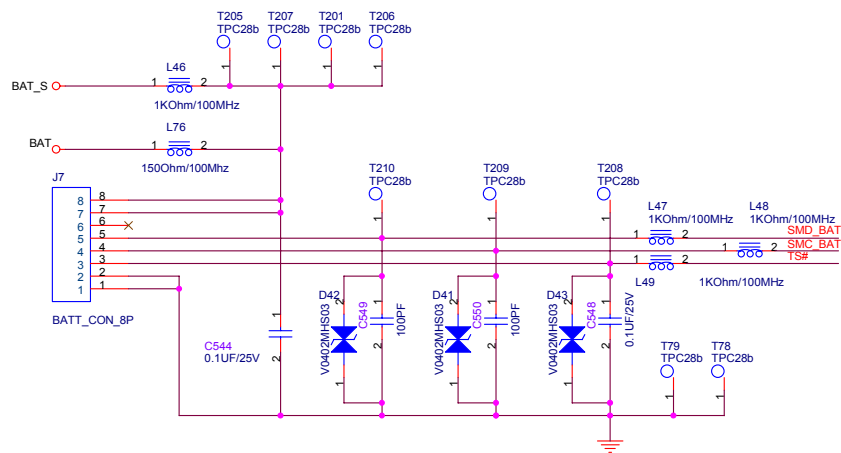
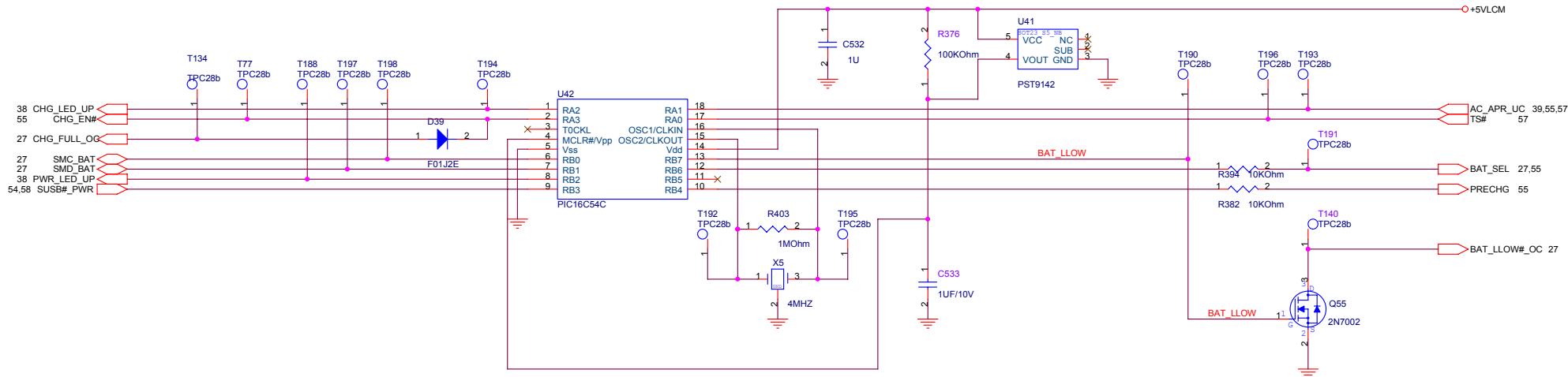
$$V+INE1 = 25 * I_{in}(A) * R_{s2}$$

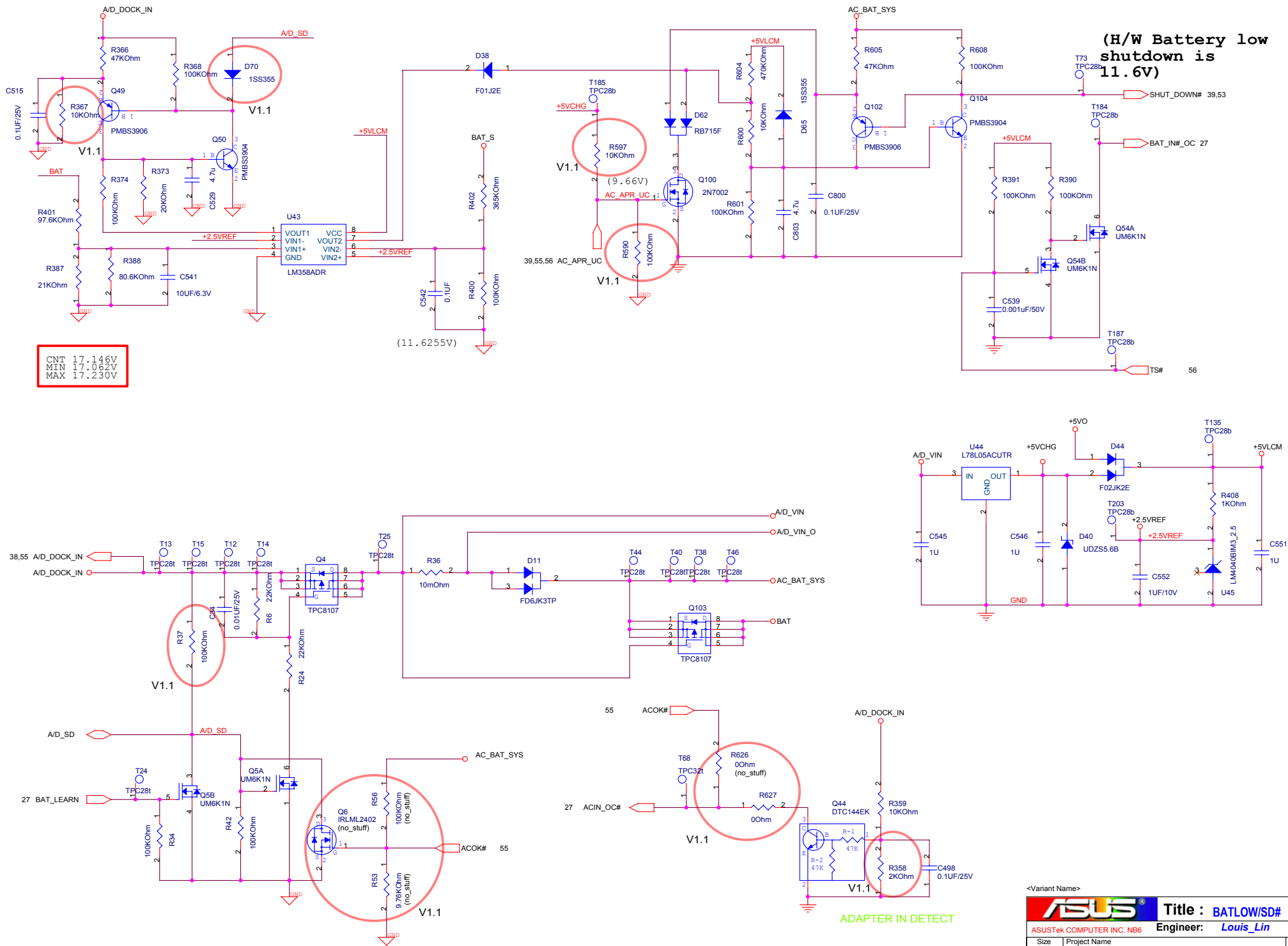
$$V+INE1 = 25 * 4.58(A) * 0.010 = 1.145V$$

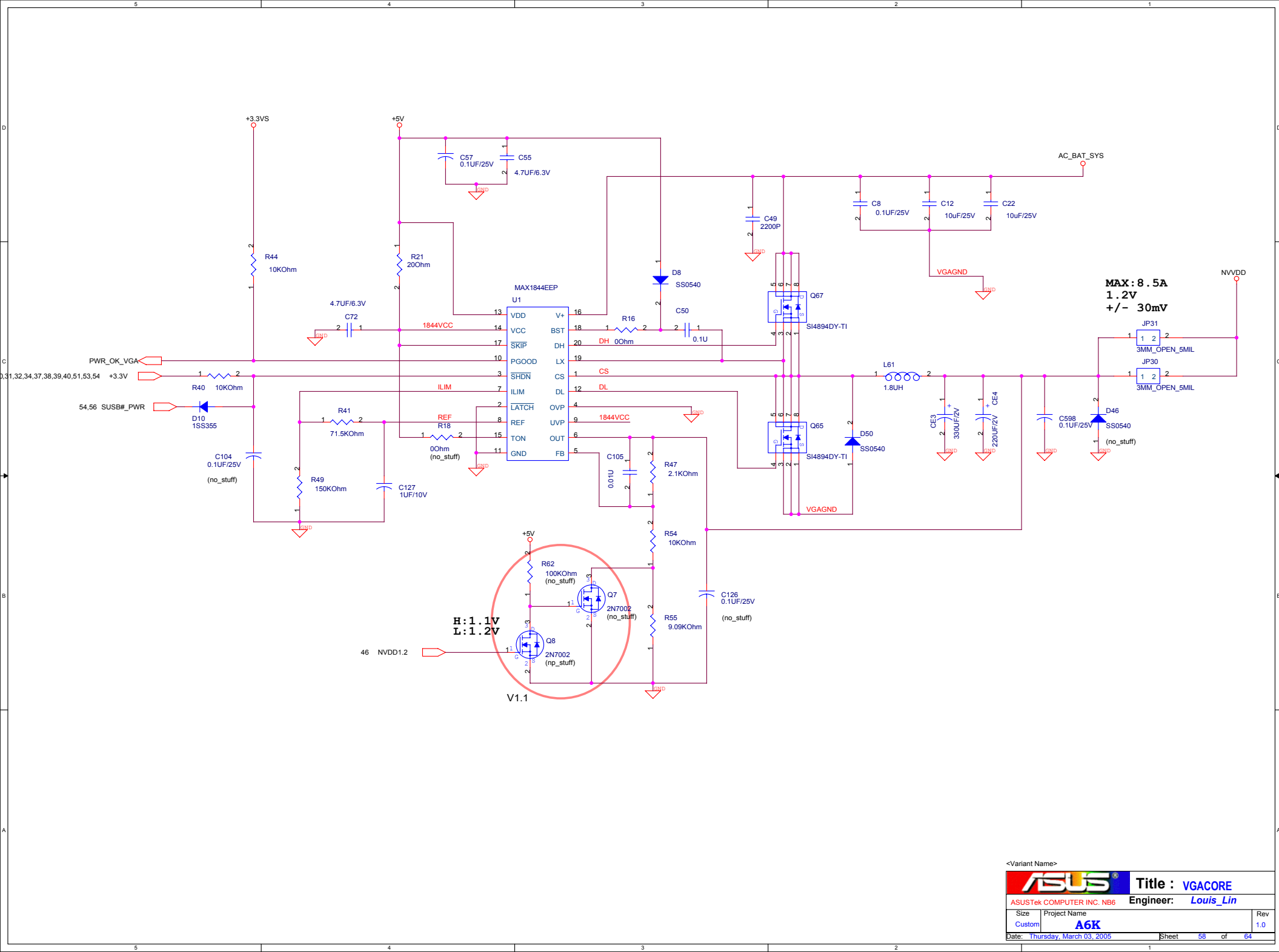
$$DEFAULT \ R(1ow) = 100K$$

$$R(hi) = (5/1.145-1) * 10K = 336.68K$$

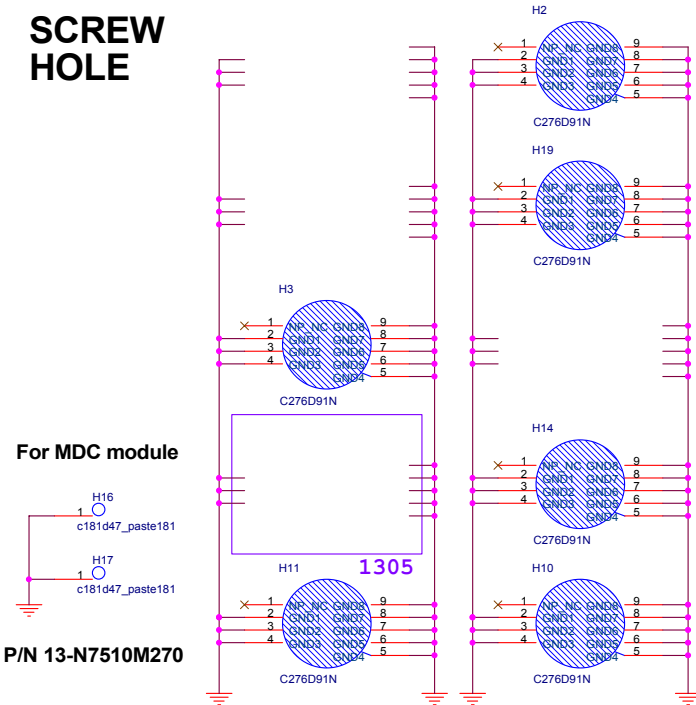








SCREW HOLE



For MDC module

P/N 13-N7510M270

For NB fix sink

P/N 13-NCF10M010

For NV44M-V fix sink

CPU Throttling(BIOS setting): 90 degree C.
System shutdown(BIOS setting) : 100 degree C.
H/W shutdown(page 44, U47 , no load) : 105 degree C.

Short Pad location:
Page39: JP4,5,15,16,19,26,27
Page40: JP6,7,9,22,24
Page42: JP13,14,17,18,28,29

Don't Short Pad: JP26

JP4:+V2.5 --Power In
JP5:+V1.25S
JP6:+V2.5
JP7:+V1.2S
JP9:+VCCP
JP13:+V5S
JP14:+V5
JP15:+V1.5SUS
JP16:+V2.5 --Power IN
JP17:+V1.8S
JP18:+V12
JP19:+V1.8
JP22:+V1.5S
JP24: VREF5-->+V5A
JP26:+3VALWAYS_T-->+V3.3A (open)
JP27:+3VALWAYS_M-->+V3.3A (short)
JP28:+V3.3S
JP29:+V3.3

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP
L2 VCC
L3 GND
L4 BOT

IMPEDENCE

Single-Ended

27.4 OHM WIDTH

TOP/BOT 20 mils

37.5 OHM WIDTH

TOP/BOT 12 mils

42 OHM WIDTH

TOP/BOT 10 mils

55 OHM WIDTH

TOP/BOT 5 mils

Differential

70 OHM WIDTH/SPACE

TOP/BOT 9 mils/ 5 mils

90 OHM WIDTH/SPACE

TOP/BOT 7 mils/ 10 mils

100 OHM WIDTH/SPACE

TOP/BOT 5 mils/ 7 mils

PCI INTERFACE

PCI_REQ#

CB&1394 PCI_REQ#0
MINIPCI PCI_REQ#1
LAN PCI_REQ#2

PCI_GNT#

CB&1394 PCI_REQ#0
MINIPCI PCI_REQ#1
LAN PCI_REQ#2

IDSEL

CB&1394 PCI_AD21
MINIPCI PCI_AD20
LAN PCI_AD16

PCI_INT#

CB&1394 PCI_INTB/A/D#
MINIPCI PCI_INTC/D#
LAN PCI_INTC#

POWER INTERFACE

SIGNALS	TYPE	POWER
CLK_EN#	I	+V3.3S_CLK
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
CPU_VRON	O	+V3.3SUS
VRM_PWRGD	I	+V3.3S
PM_STPCPU#	O	+V3.3S
CHG_LED	I	+5VLCM
RST_BTN#	O	OD
OTP_RESET#	I	+V5
SHUT_DOWN#	I	AC_BAT_SYS
+5VLCM	PWR	+V5
PM_SLPDLY_S3#	O	+V3.3
PM_SLP_S4#	O	+V3.3SUS
BAT_LEARN	I	+V3.3
BAT_LLOW#_OC	I	+V3.3
BAT_IN#_OC	I	+V3.3
ACIN_OC	I	+V3.3
CHG_FULL_OC	I	+V3.3
PM DPRSLPVR	O	+V3.3S
AC_APR_UC	I	+V5A
+V5A	PWR	VREF5
3V_ON	O	OD
AC_BAT_SYS	PWR	DC
A/D_DOCK_IN	PWR	DC
SMC_BAT	IO	+V3.3
SMD_BAT	IO	+V3.3

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	1.46V	25A
+VCCP	1.05V	2.4A(Max),1A(Real)
+V1.2S	1.2V	2.5A
+V1.25S	1.25V	0.5A
+V1.5S	1.5V	1.32A
+V1.5SUS	1.5V	64 mA
+V1.8	1.8V	0.14A
+V1.8S	1.8V	0.3 A
+V2.5	2.5V	6.68A
+V3.3S	3.3V	1.732A
+V3.3	3.3V	1.515A
+V3.3SUS	3.3V	14 mA
+V5S	5V	2.5A
+V5	5V	3.75A
+V5SUS	5V	0.5A
+V12	12V	0.25A
+V12S	12V	0.25A

<Variant Name>

		Title : SCREW HOLE	
ASUSTek COMPUTER INC. NB6		Engineer:	
Size	Project Name	Rev	
Custom	A6U	1.0	
Date: Thursday, March 03, 2005		Sheet	59 of 64

PCI Device	IDSEL#	REQ/GNT#	Interrupts
LAN_RTL8100CL	AD22	2	D
CARD READER	AD21	0	B
CARDBUS	AD21	0	C
1394	AD21	0	D
MINIPCI (802.11a/b/g)	AD20	1	C,D

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010010x (A4)
Thermal Sensor (SA56004)	0101110x (5C)
PIC	1001001x (92)

SIS964L GPIO	SIGNAL NAME	I/O	Volt
GPIO 0		P-U	+3.3VS
GPIO 1	NV_THERM#	INPUT	+3.3VS
GPIO 2	THRM_ALERT#	INPUT	+3.3VS
GPIO 3	EXTSMI#	INPUT	+3.3VS
GPIO 4	PM_CLKRUN#	OUTPUT	+3.3VS
GPIO 5		P-U	+3.3VS
GPIO 6	CPUFAN_SPD_A	INPUT	+3.3VS
GPIO 7	BACK_OFF#	OUTPUT	+3.3VAUX
GPIO 8	PM_RI#	INPUT	+3.3VAUX
GPIO 9	KBDSCI_3A	INPUT	+3.3VAUX
GPIO 10	LID_963#_3A	INPUT	+3.3VAUX
GPIO 11	PM_STPPCI#	OUTPUT	+3.3VAUX
GPIO 12	PM_STPCPU#	OUTPUT	+3.3VAUX
GPIO 13	SIO_SMI#	INPUT	+3.3VAUX
GPIO 14	S3AUXSW#	OUTPUT	+3.3VAUX
GPIO 15	BT_ON	P-L	+3.3VAUX
GPIO 16	802_LED_EN#	OUTPUT	+3.3VAUX
GPIO 17	WLAN_ON#	OUTPUT	+3.3VAUX
GPIO 18	CB_SD#	OUTPUT	+3.3VAUX
GPIO 19	SM_CLK	OUTPUT	+3.3VS
GPIO 20	SM_DATA	I/O	+3.3VS
GPIO 21		NC	+3.3VAUX
GPIO 22		NC	+3.3VAUX
GPIO 23		P-L	+3.3VAUX
GPIO 24		P-U	+3.3VAUX

KBC GPIO	A6K	
P23	OP_SD#	
P22	BAT_LEARN	
P21	(KB_P21)	
P20	KBCRSM	
P42	(WATCHDOG)	
P43	CHG_FULL_OC	
P44	KB_CPURST	
P45	KB_GATEA20	
P46	KBCSCI	
P47	PM_CLKRUN#	
P50	KBC_BAT_LLOW#	
P51	KEYDETECT1	
P52	KEYDETECT2	
P53	CLR_DJ#	
P54	BAT_SEL	
P55	BAT1_IN#_OC	
P56	(FAN_DA1)	
P57	ADJ_BL	
P67	DJ_LED#	
P66	SWDJ_EN#	
P65	+VCORE	
P64	ACIN_OC	
P63	DISTP	
P62	MARATHON#	
P61	INTERNET#	
P60	EMAIL#	
P75	(KB_CLK)	
P74	(MS_CLK)	
P73	TPAD_CLK	
P72	(KB_DAT)	
P71	(MS_DAT)	
P70	TPAD_DAT	
P77	BAT_SMC	
P76	BAT_SMD	
P27	SCROLLLOCK#	
P26	NUM_LED#	
P25	CAP_LED#	
P24	SET_PLTRSTNS#	
P40	EXT_SMI	
P41	EMAIL_LED#	

FIRST SOURCE	SECOND SOURCE	NOTE
05-001005111	05-001017122	L5 NA10643
	05-001005310	
06-006002411	06-006002001	
06-010008000	06-010008100	L5 NA10601
06-017001000	06-017001200	
07-005000010	07-005000210	L5 NA10473
	07-005000410	
07-005261010	07-005357010	Power RD Request
07-010303271	07-010303273	L5 NA10603
07-010Q02501	07-010812500	
07-014150220	07-014150120	
	07-016202032	
07-016202032	07-016402032	
	07-016102032	
09-013103013	09-013103010	L5 NA10512
09-091090000	09-091090001	L5 NA10512
	09-091090005	
10-0931111041	10-0931111040	L5 NA10334
10-124901000	10-12490100A	L5 NA10298
10-12490560A	10-124905600	
11-032310661	11-032310662	For MC request
	11-032310663	
11-033410400	11-033410401	Follow L5G R2.0 2nd source
	11-033410405	
	11-033410406	
11-033410500	11-033410502	
11-03B210620	11-031110621	L5 NA10407
	11-031210621	*11-03B110623 for Power RD Request
	11-03B110621	
	11-03B110622	
	11-03B210621	
	11-03B110623	

REVISION LIST

POWER INTERFACE

SIGNALS TYPE POWER

IMPEDENCE

Single-Ended

27.4 OHM WIDTH

TOP/BOT 22 mils
IN1/IN3 16 mils

37.5 OHM WIDTH

TOP/BOT 13.5 mils
IN1/IN3 10 mils

42 OHM WIDTH

TOP/BOT 11 mils
IN1/IN3 8.5 mils

55 OHM WIDTH

TOP/BOT 6 mils
IN1/IN3 5 mils

75 OHM WIDTH

TOP/BOT 2.5 mils
IN1/IN3 2 mils

Differential

70 OHM WIDTH/SPACE

TOP/BOT 8 mils/ 4 mils
IN1/IN3 8 mils/ 3.5 mils

90 OHM WIDTH/SPACE

TOP/BOT 5 mils/ 5 mils
IN1/IN3 5 mils/ 5 mils

100 OHM WIDTH/SPACE

TOP/BOT 4 mils/ 6 mils
IN1/IN3 4.25 mils/ 5.75 mils

PCI INTERFACE

PCI_REQ#

CB&1394 PCI_REQ#0

MINIPCI PCI_REQ#1

LAN PCI_REQ#2

IDSEL

CB&1394 PCI_AD21

MINIPCI PCI_AD20

LAN PCI_AD22

PCIe Device

PEG

NVIDIA NV44M

PCIe Giga NIC

N/A

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP

L2 VCC

L3 IN1

L4 IN2

L5 GND

L6 BOT

SIGNAL IN: AVIDT0;4] PAGE 49
CORE_ON
COREFB
COREFB#

OUT: +VCORE_PG

POWER IN: AC_BAT_SYS
+5V0
+3.3VS

OUT: +VCORE

SIGNAL IN: VLDT_ON PAGE 50
+2.5VREF
SUSC#_PWR
DDR_PWRGD
+1.2VS_PG

POWER IN: +5VAO
+12V
+3VO
+3VAUX
+2.5VO
+1.25V
+3.3V
+5VO
+1.8VO

OUT: +3VA
+1.8VAUX
+1.25V
+1.2VS
+1.2VS_VS

SIGNAL IN: SUSC#_PWR PAGE 51
OUT: 2.5V_1.8V_PG

POWER IN: AC_BAT_SYS
+3.3VS
+5VAO

OUT: +2.5V
+1.8V

SIGNAL IN: SUSC#_PWR PAGE 52
OTP_RESET#
SHUT_DOWN#
AUX_ON

OUT: 3V_5V_PWRGD

POWER IN: AC_BAT_SYS
+3VA
+3.3VS
+VCC_GMCH_CORE
+5VAO

OUT: +5VA
+5VO
+12VO
+3VQ

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	0.7 - 1.55V	27.3A
+1.25V	1.25V	0.725A
NVVDD	1.1/1.2V	8.62A
+2.5V	2.5V	5.55A
+1.8VAUX	1.8V	50mA
+1.2P_VS	1.2V	1.875A
+1.2VS	1.2V	635mA
+1.8VS	1.8V	2.521A
+1.8V	1.8V	415 mA
+1.8FB_VS	1.8V	2A
+2.5VS	2.5V	0.035A
+3.3V	3.3V	1.925A
+3.3VS	3.3V	2.955A
+5VS	5V	4.7A
+5V	5V	3.865A
+5VA	5V	0.05A
+12V	12V	0.05A
+12VS	12V	0.01A
+3.3VAUX	3.3V	0.417A
+3VA	3.3V	0.02A

Rev	Date	Description
R1.00	04/6/28	1. Initial release.
R1.1	02/14/05'	1.R14&R15 be changed from 75 ohm to 49.9 ohm,P-9.follow SIS. 2.Q26A be changed to "D67" to prevent body diode leakage current,p-39. 3.Q26B be changed to "Q107",P-39. 4.R453&R475 be changed from 10kohm to 6.81kohm,P-49.follow NVIDIA. 5.R578 & C758 be changed to mounting. 6.JP32 CON pin definition be corrected. 7.Enable R5C841 internal regulator,P-22. VCC_RIN= +3.3V 8.C769 be changed from 0.1uf to 0.47uf,P-22. globe reset timing. 9.Audio Jack "J5" be changed from "12-140001088" to "12-140001081",P-32. 10.C665,C666,C659,C655,C643,C648 be changed from 330pf to 5pf,P-15. 11.C4 & C7 be changed from 5pf to 27pf and mounted,P-15
	02/21/05'	1.Added C834,C835,C836 at NVVDD,P-42. reduce ripple. 2.Added R587 and U61 ,P-39. meet K8 CPU power off sequency. 3.Changed U28 power source from +5VA to +3VA,P-39.prevent quiescent current. 4.Changed RN28B pull up power source from +3.3VAUX to +3VA,P-39.prevent quiescent current. 5.Removed Q88B ,P-37.DJ_SW# latched sequency . 6.Q16 and Q45 be changed ,P-28.parts Preparing. 7.Added D68 ,P27.LED flash when ODD running. 8.Added JRST1,P-17. subbattery reset asserted. 9.Added R617 47KOHM pull low ,P-16
	02/22/05'	1.Added R624 and changed R130 from 10k ohm to 47kohm,P-14. white screen when entry and resuming in S3. 2.Added C837,P-42.EMI 3.Changed thermal sensor for cost.
	02/23/05'	1.Changed R29 pin2 power source from +3.3VAUX to +3.3VAUX_NB,P-9.
	02/25/05'	1.CN17/CN18/CN19/CN20/CN33 parts be changed for cost! 2.R264 unmount,p-9.duplicate

Rev	Date	Description