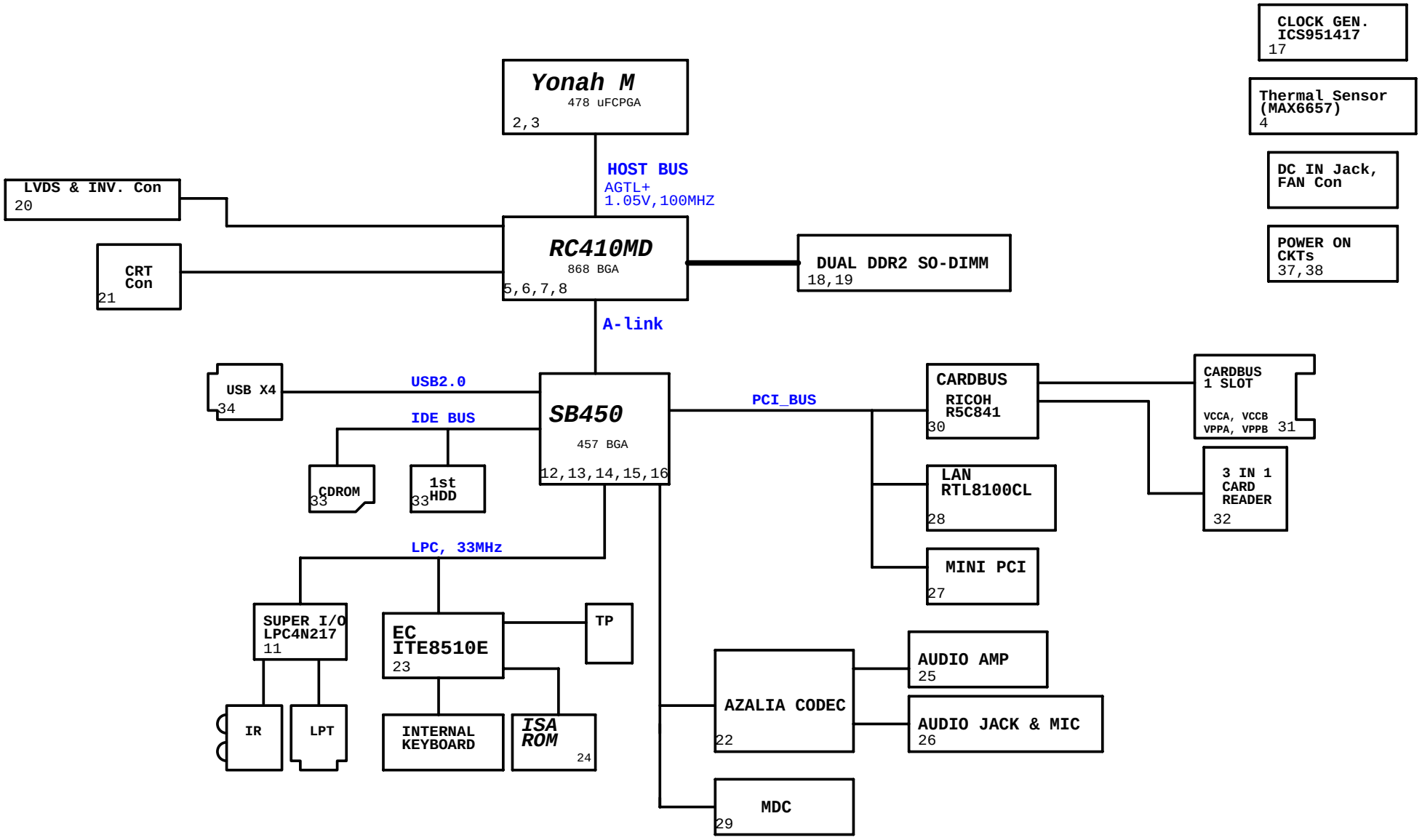
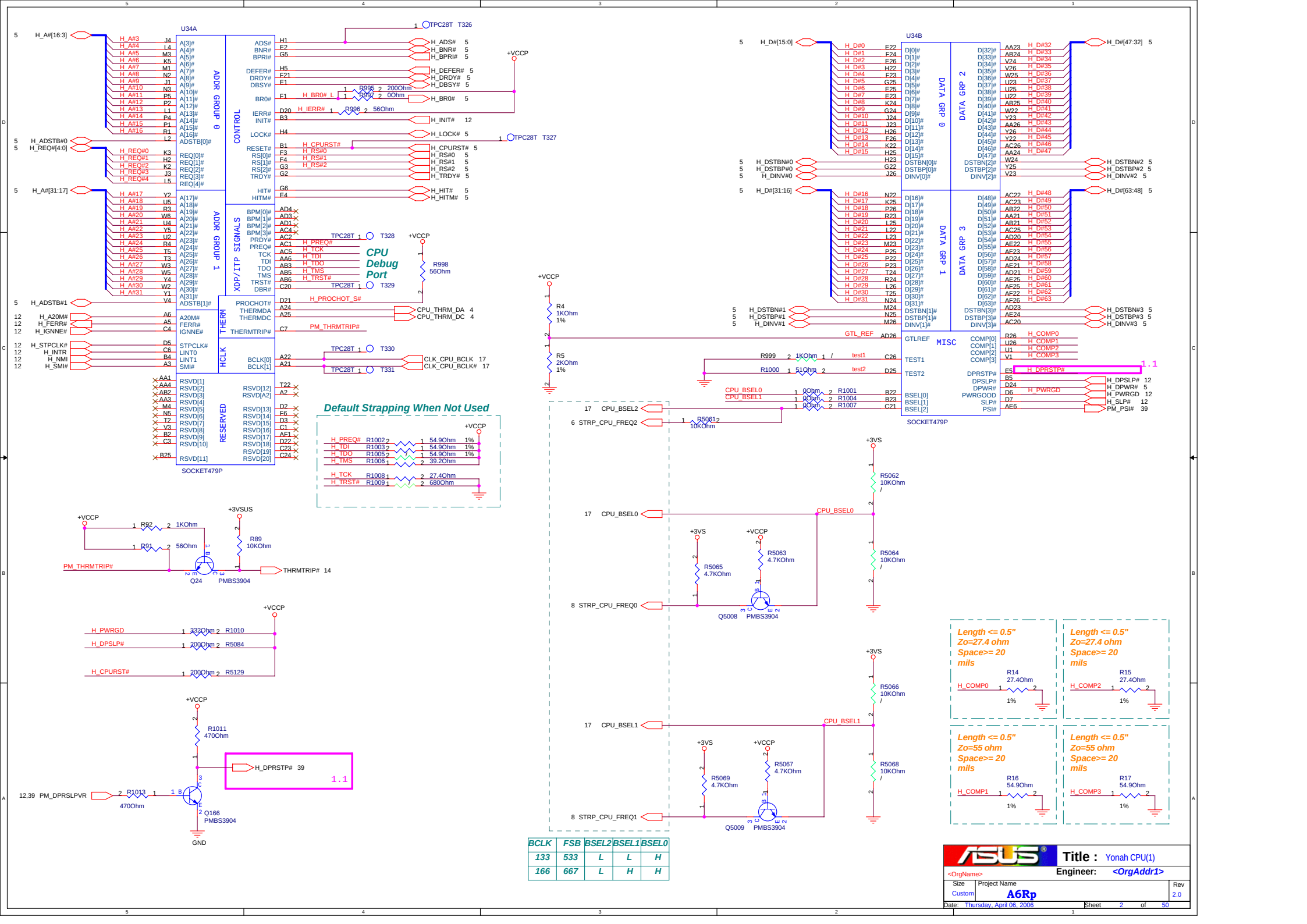
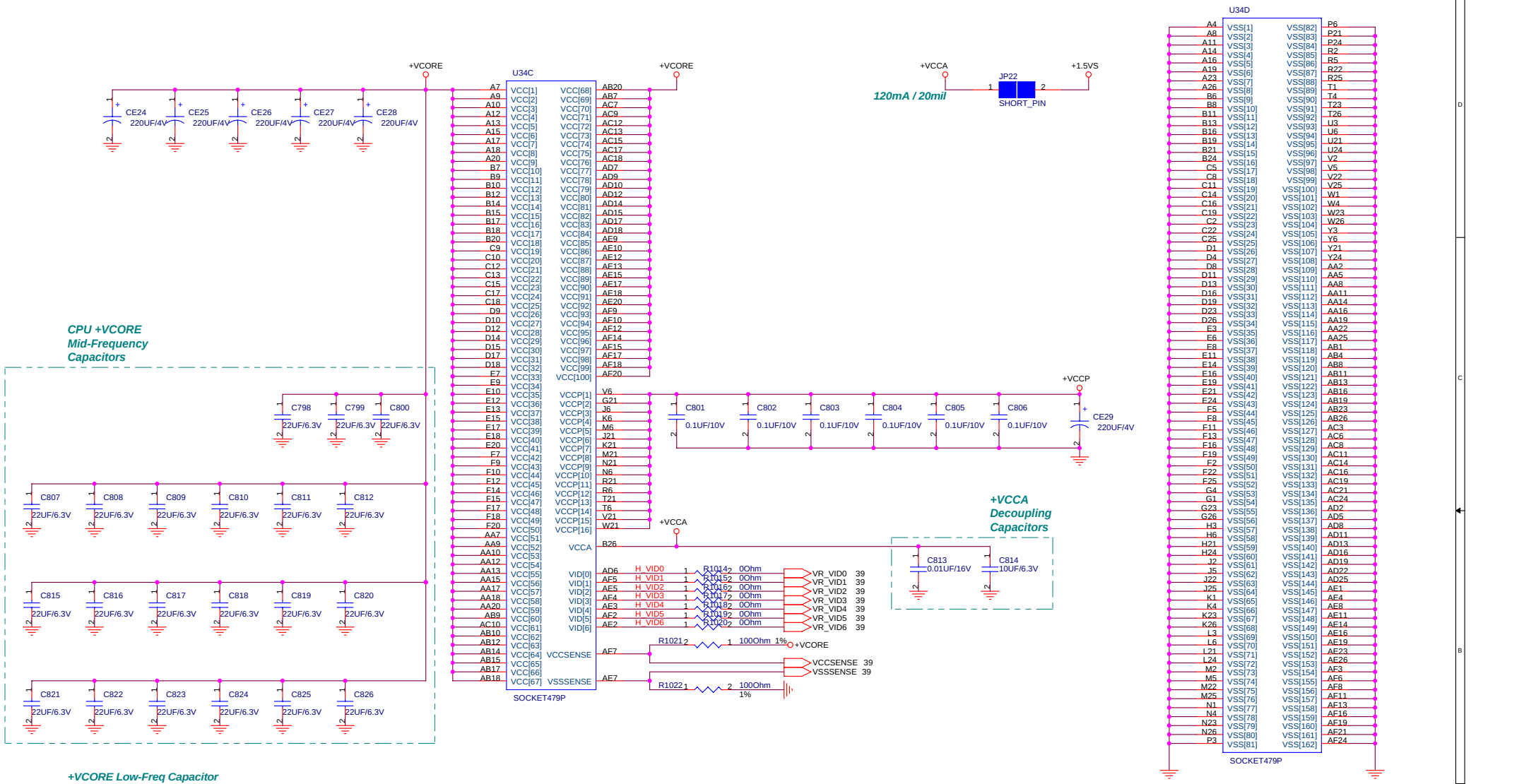
Yonah/RC410MD/IXP450 BLOCK DIAGRAM



Title : BLOCK DIAGRAM		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 1 of 50	


U34A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
HCLK
RESERVED
SOCKET479P
CPU Debug Port
Default Strapping When Not Used
U34B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
SOCKET479P
Length <= 0.5" Zo=27.4 ohm Space>= 20 mils
Length <= 0.5" Zo=55 ohm Space>= 20 mils
Title : Yonah CPU(1)
Engineer: <OrgAddr1>
<OrgName>
Project Name A6Rp
Size Custom
Rev 2.0
Date: Thursday, April 06, 2006
Sheet 2 of 50



+VCORE Low-Freq Capacitor
- Intel: 330UF *6
- ATI: 330UF *6
- R1F: 330UF *4
- A7J: 330UF *5

+VCORE Mid-Frequency Capacitor
- Intel: 22UF *32
- ATI: 10UF *26
- R1F: 22UF *16
- A7J: 22UF*29 use 19
- A6RF: 22UF*21 use 21

+VCCP Decoupling Capacitor
- Intel: 270UF *1, 0.1UF *6
- R1F: 220UF *1, 0.1UF *4
- A7J: 220UF *1, 0,1UF *6
- A6RF: 220UF *1, 0,1UF *6

Title : Yonah CPU(2)		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 3 of 50	

Fan Speed Control

KBC will issue a analog (a voltage level) signal.

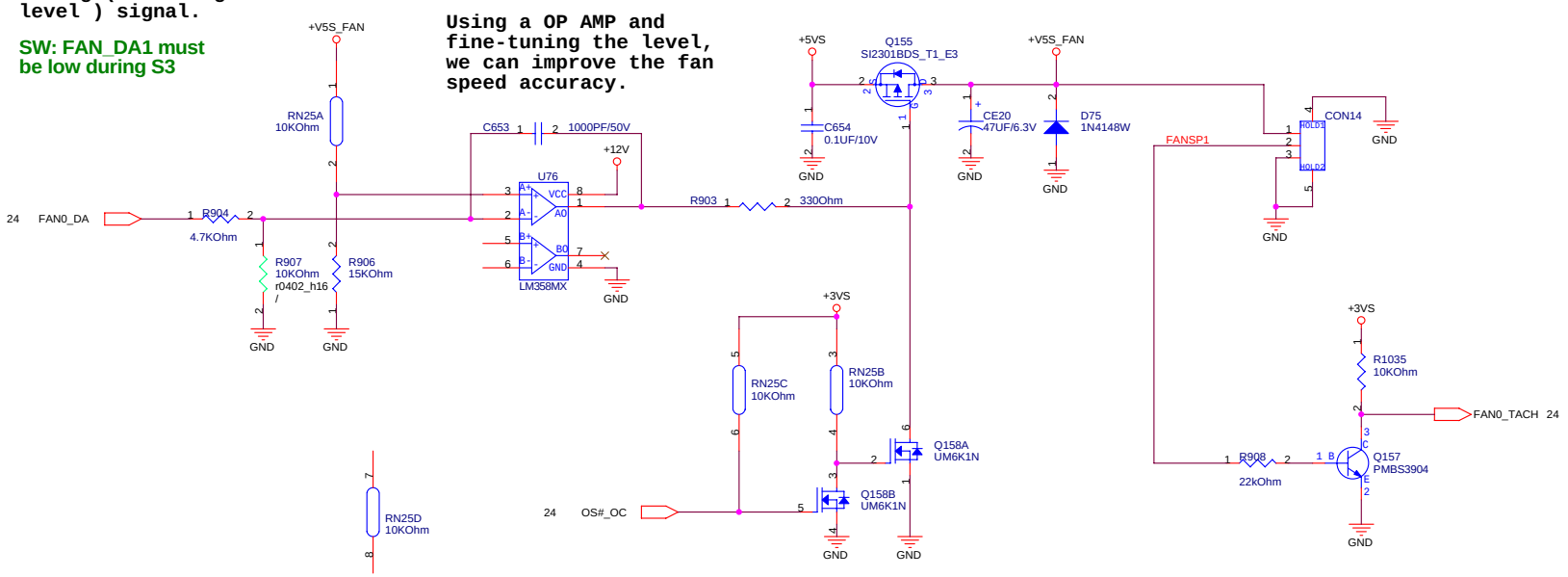
SW: FAN_DA1 must be low during S3

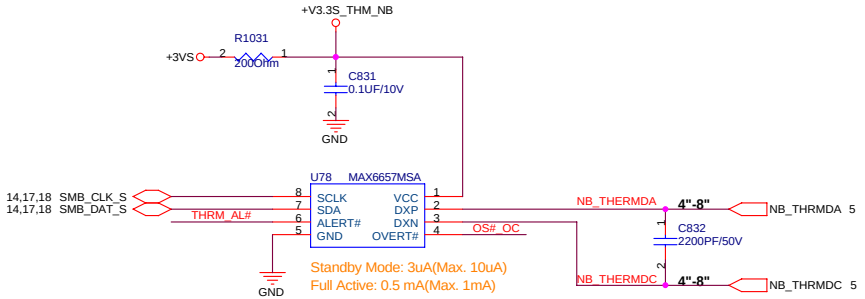
Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

Route H_THERMDA and H_THERMDC on the same layer

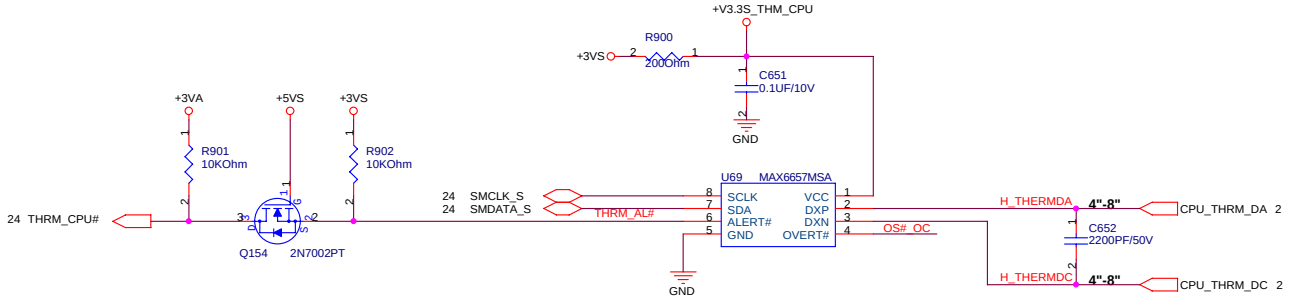
----------OTHER SIGNALS
12 mils
==========GND
10 mils
========H_THERMDA(10 mils)
10 mils
========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power



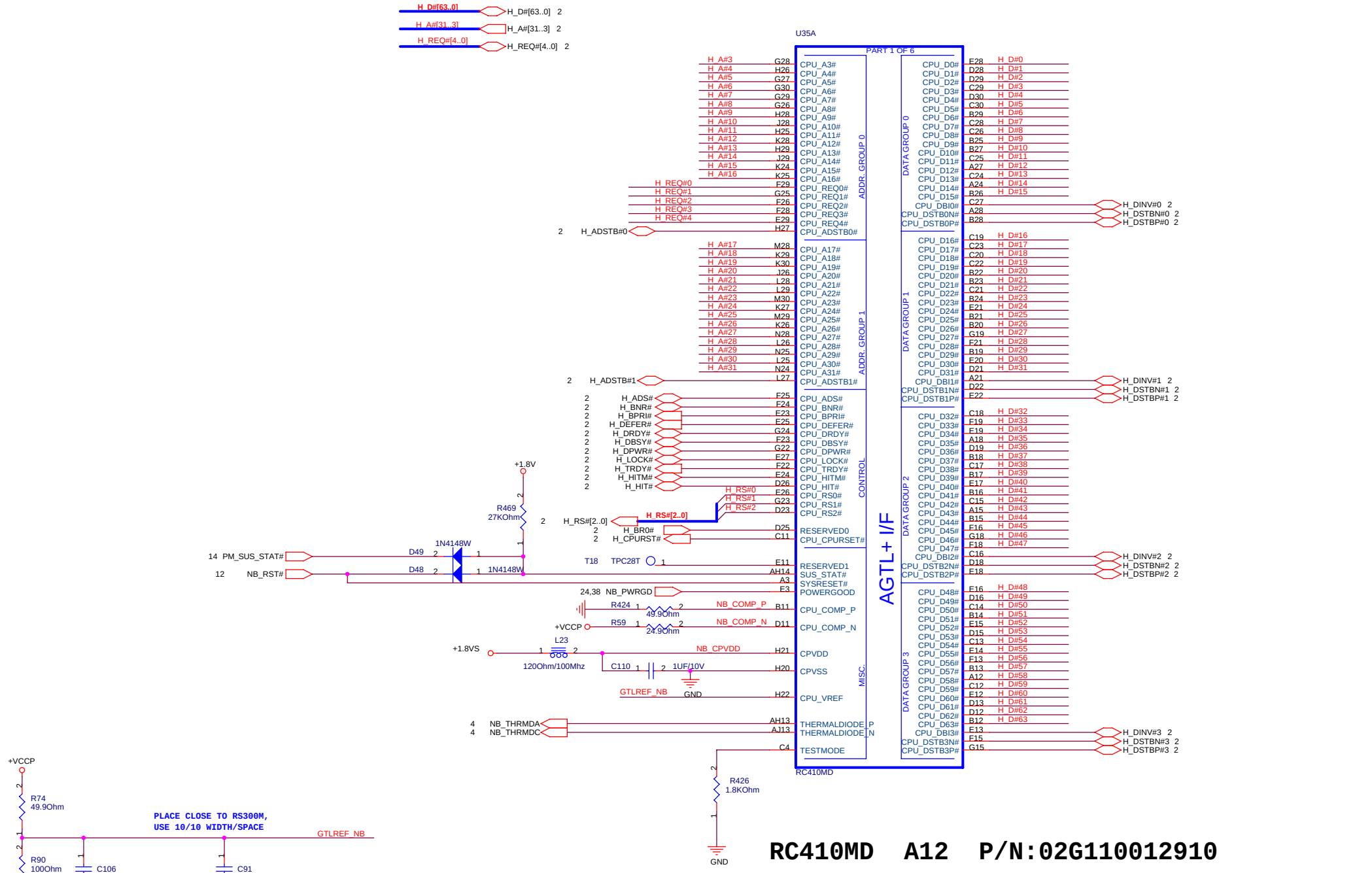


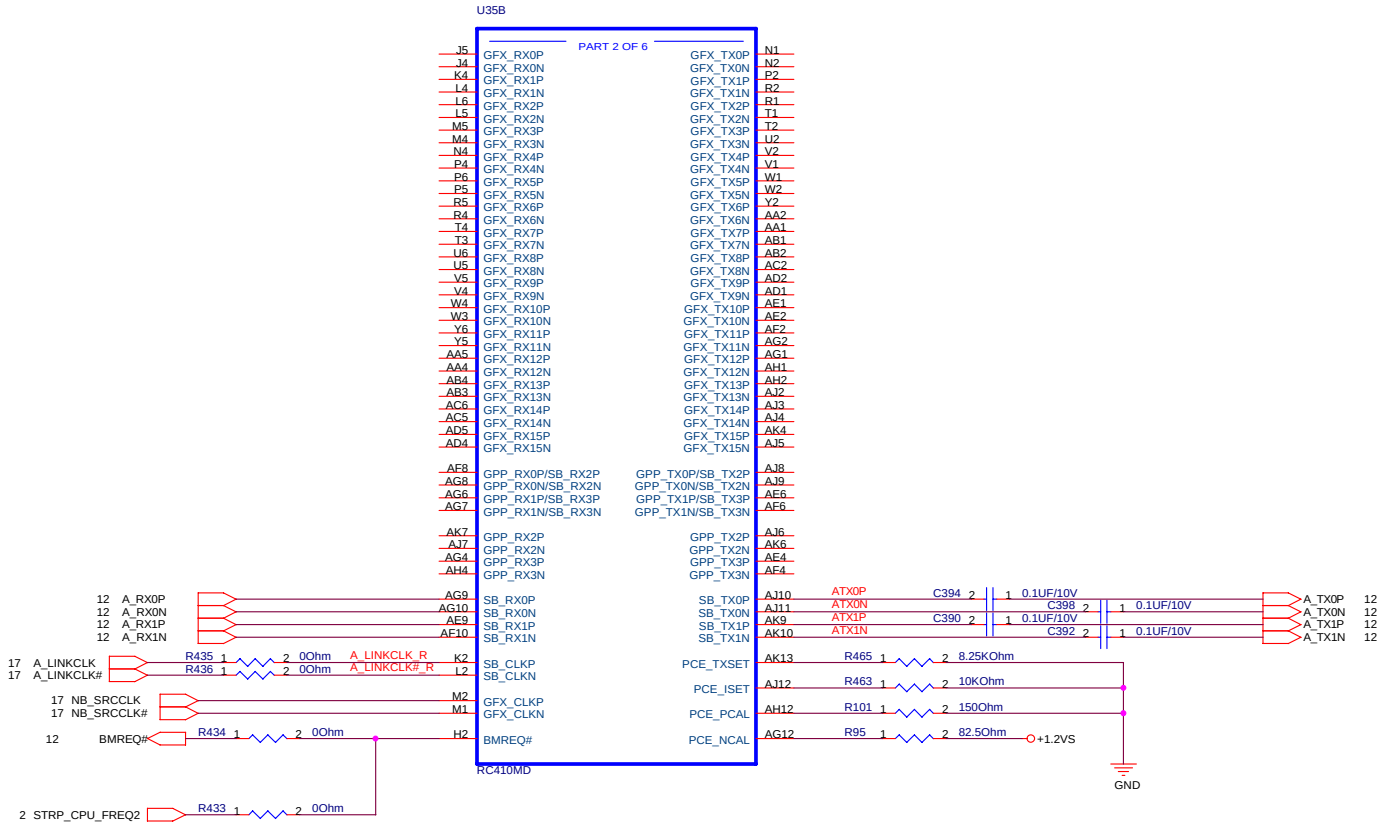
NB Detect



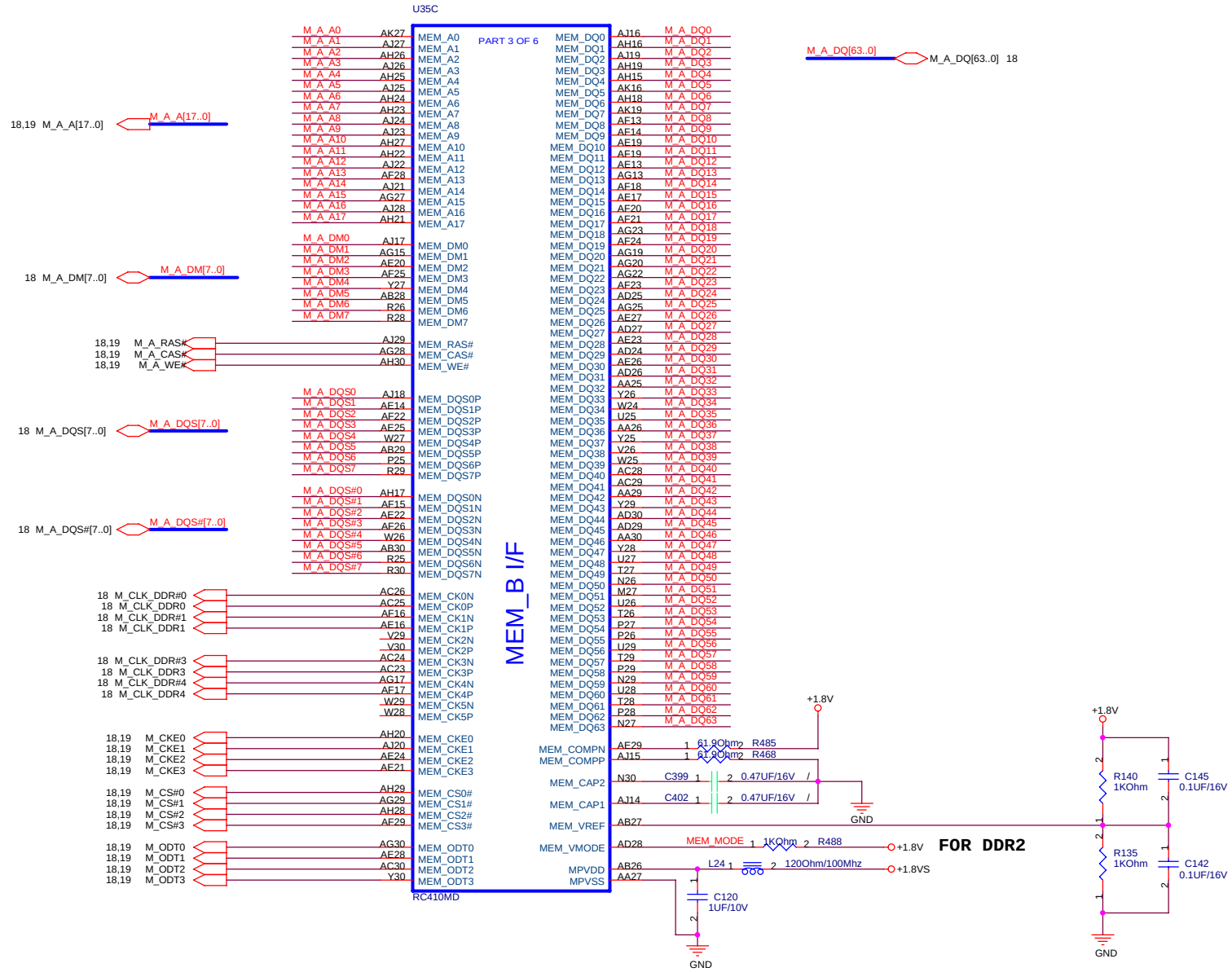
CPU Detect

ASUS	Title : THERMAL SERSOR,FAN	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 4 of 50	

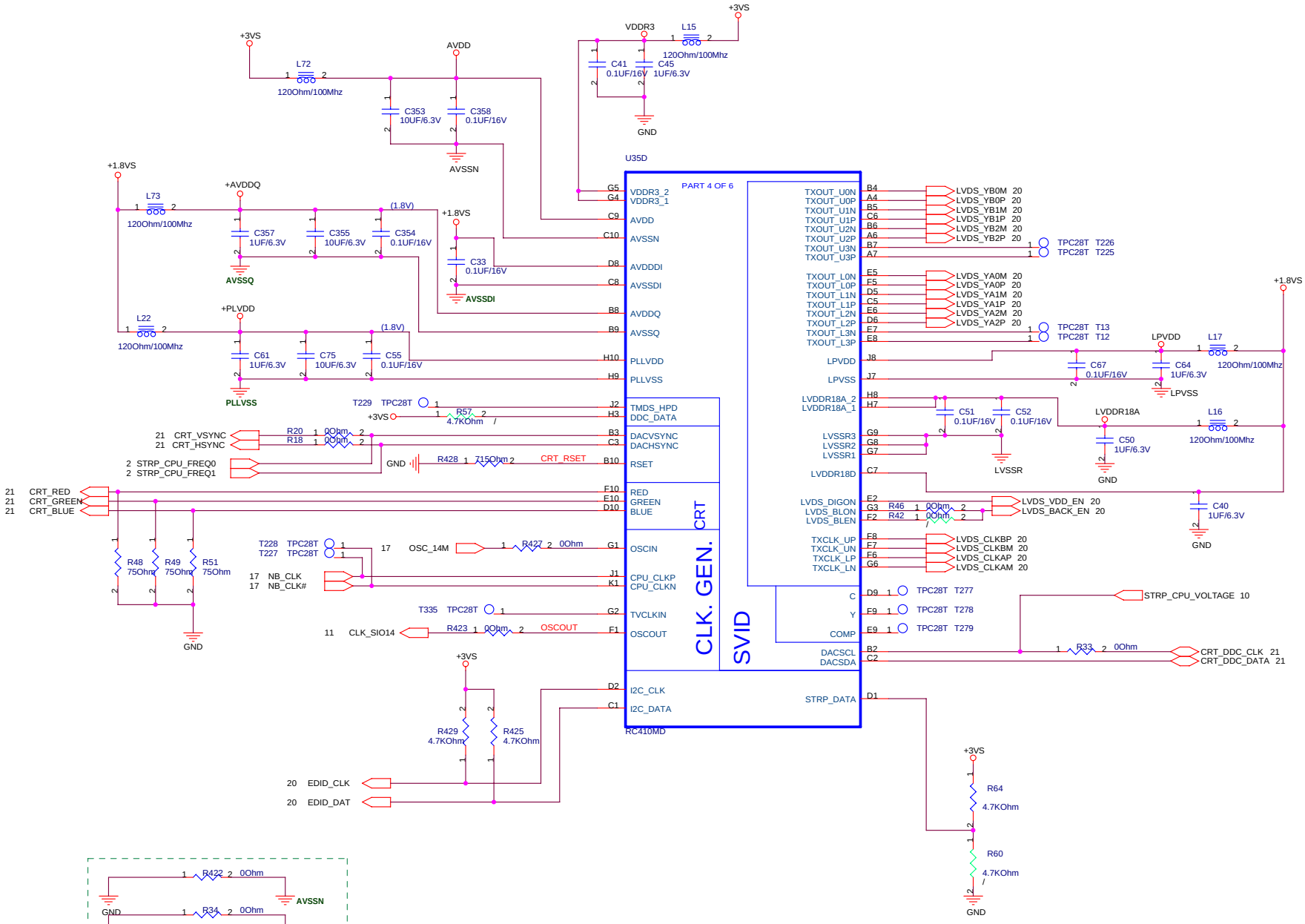

H_D#[63..0]
H_A#[31..3]
H_REQ#[4..0]
H_D#[63..0] 2
H_A#[31..3] 2
H_REQ#[4..0] 2
U35A
PART 1 OF 6
AGTL+ I/F
ADDR GROUP 0
ADDR GROUP 1
CONTROL
MISC
DATA GROUP 0
DATA GROUP 1
DATA GROUP 2
DATA GROUP 3
RC410MD
H_ADSTB#0
H_ADSTB#1
H_RS#[2..0]
+1.8V
R469 27KOhm
1N4148W
D49
D48
PM_SUS_STAT#
NB_RST#
TPC28T
NB_PWRGD
R424 49.9Ohm
R59 24.9Ohm
NB_COMP_P
NB_COMP_N
+VCCP
+1.8VS
L23
120Ohm/100Mhz
C110 1UF/10V
NB_CPVDD
GTLREF_NB
GND
NB_THRMDA
NB_THRMDC
R426 1.8KOhm
+VCCP
R74 49.9Ohm
PLACE CLOSE TO RS300M,
USE 10/10 WIDTH/SPACE
GTLREF_NB
R90 100Ohm 1%
C106 1UF/10V
C91 22PF/50V
GND
GND
GND
RC410MD A12 P/N:02G110012910
Title : RC410MD AGTL I/F(1)
<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name A6Rp
Rev 2.0
Date: Thursday, April 06, 2006
Sheet 5 of 50



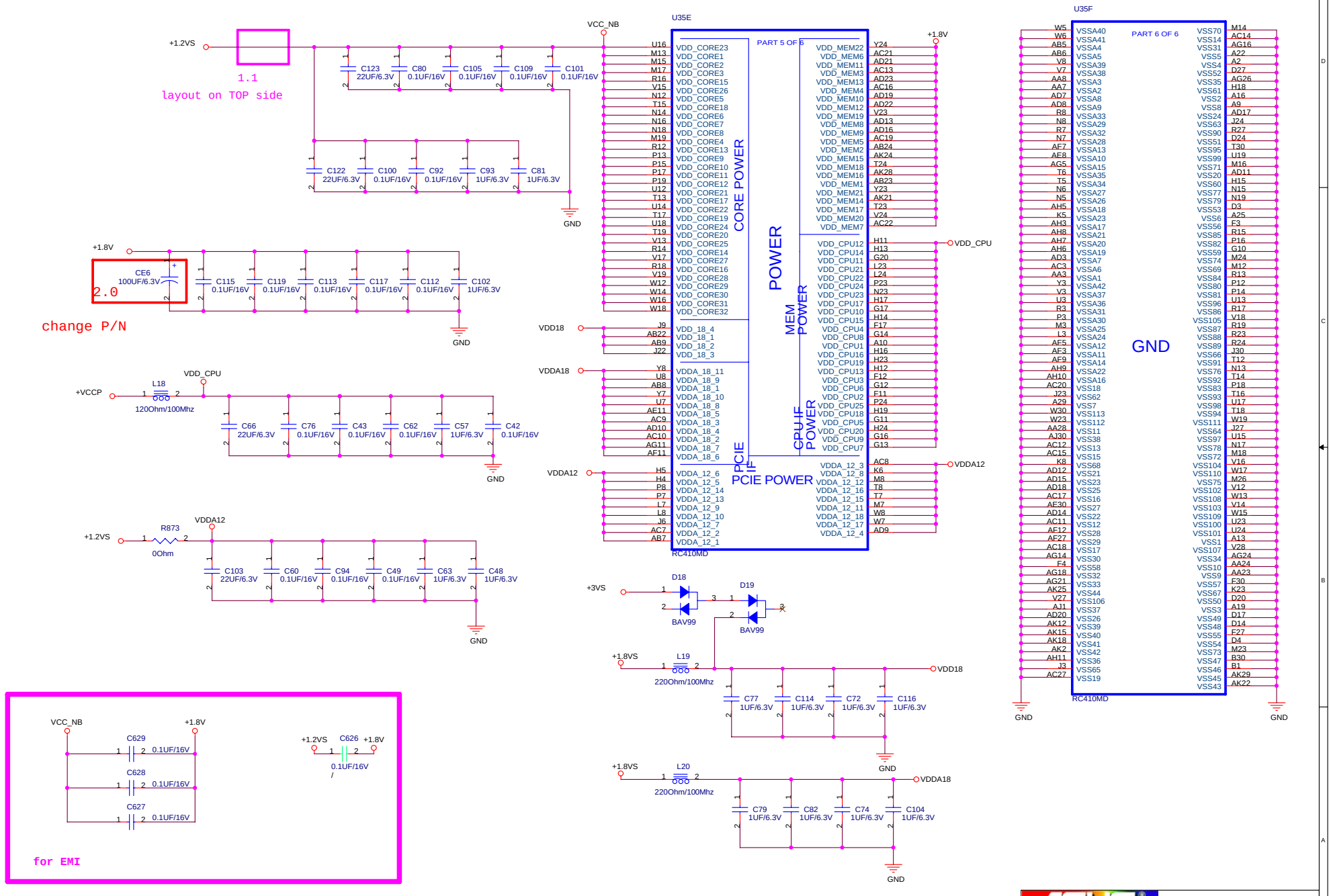
Title : RC410MD PCIE & A-Link(2)		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 6 of 50	



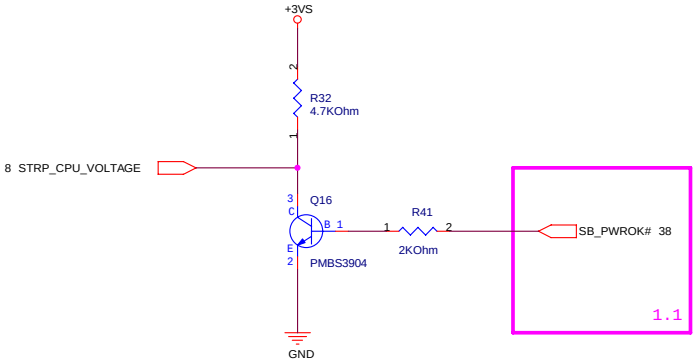
Title :	RC410MD DDR2 I/F (3)	
<OrgName>	Engineer:	<OrgAddr1>
Size: Custom	Project Name: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 7 of 50	



ASUS	Title :	RC410MB VIDEO I/F (5)
<OrgName>	Engineer:	<OrgAddr1>
Size: Custom	Project Name: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 8 of 50	



Title : RC410MD POWER (4)			
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6Rp		Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 9 of 50		



STRP_CPU_VOLTAGE: CPU VCC
0: MOBILE CPU
1: DESKTOP CPU
DEFAULT:0

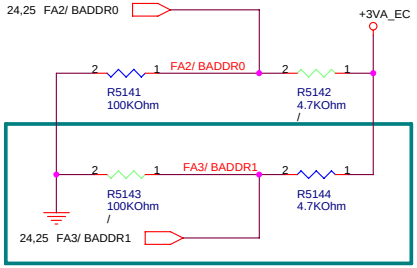
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

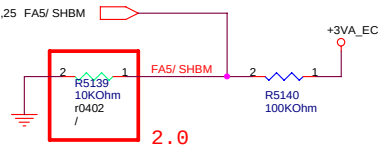


Note: Sampled at VSTBY Power Up Reset

FA5/ SHBM

0: Disable Shared Memory with Host BIOS

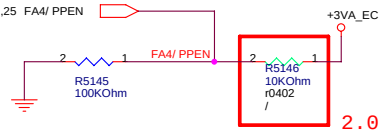
1: Enable Shared Memory with Host BIOS



FA4/ PPEN

0: Normal

1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

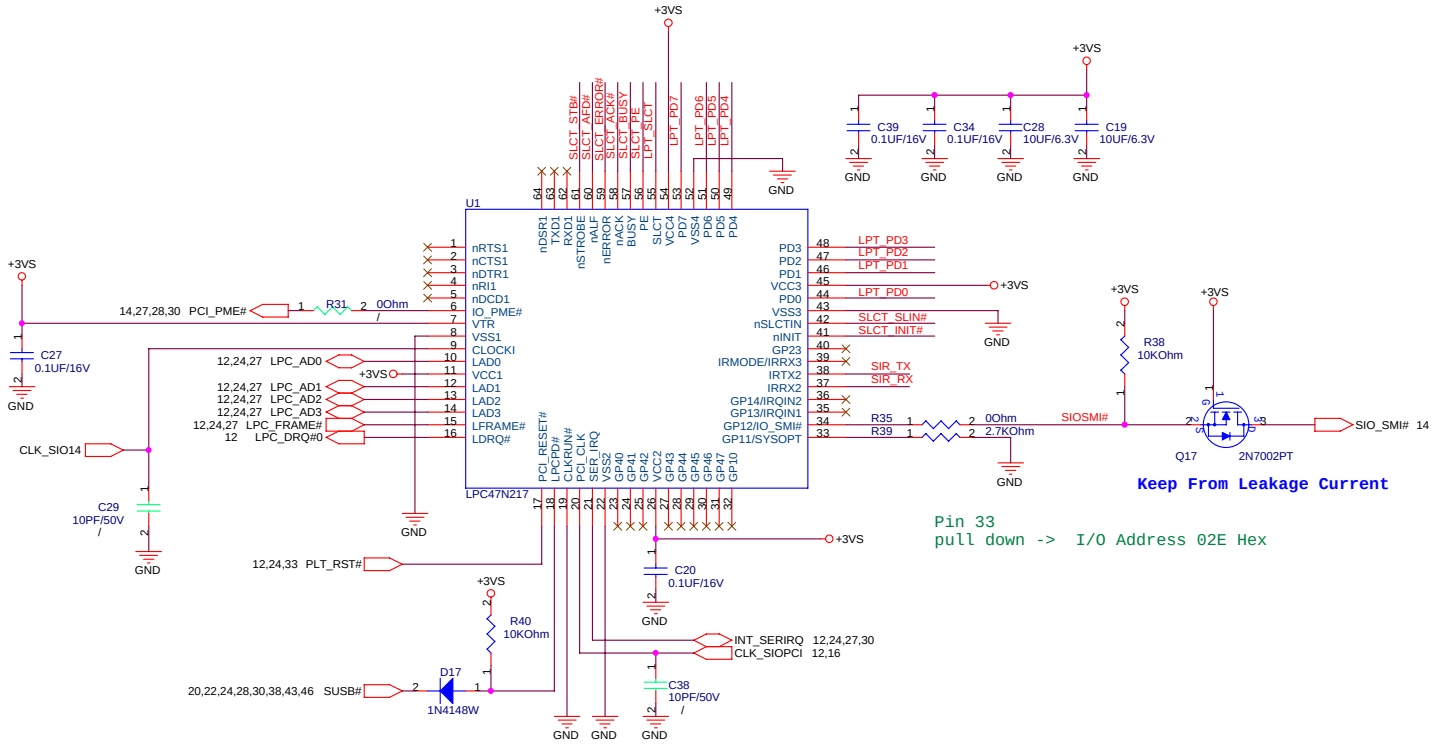


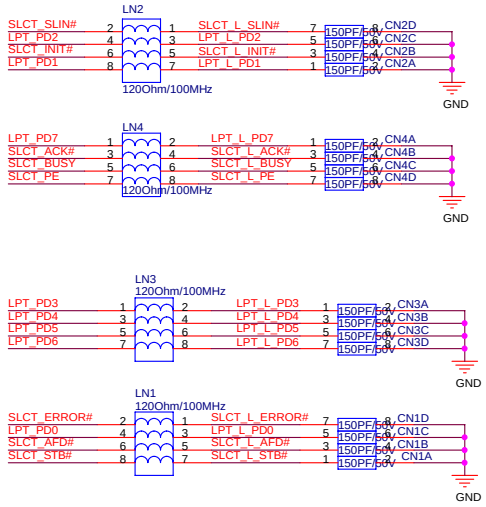
1.1

EC Hardware Strapping

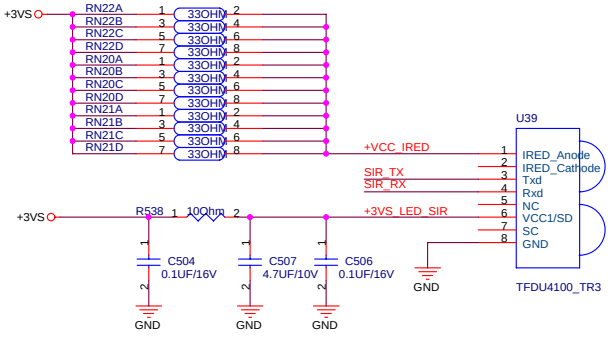
ASUS	Title : FSB SELECTION	
<OrgName>	Engineer: *<OrgAddr1>*	
Size: Custom	Project Name: **A6Rp**	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 10 of 50	

Super I/O

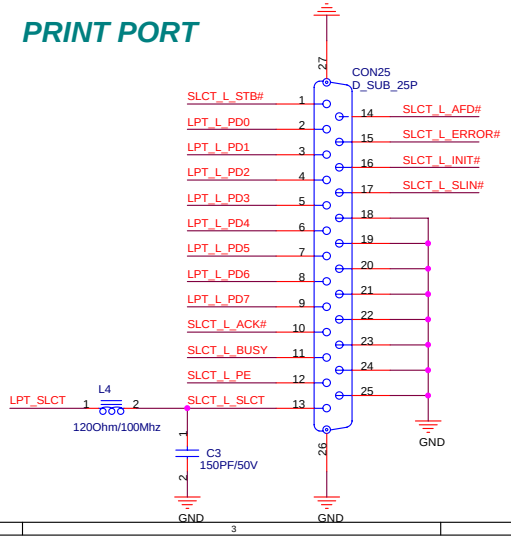


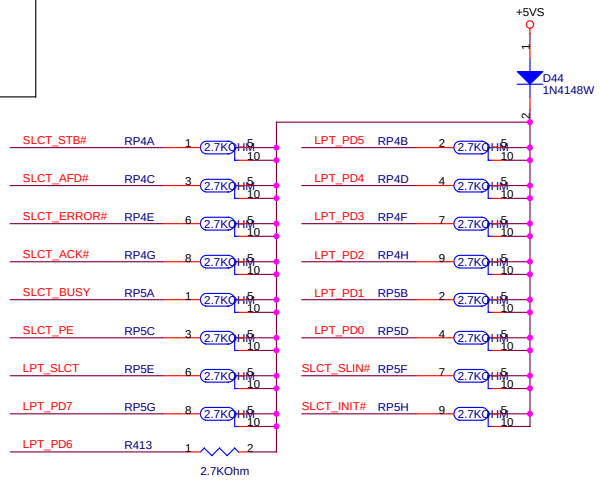


SIR



PRINT PORT





ASUS

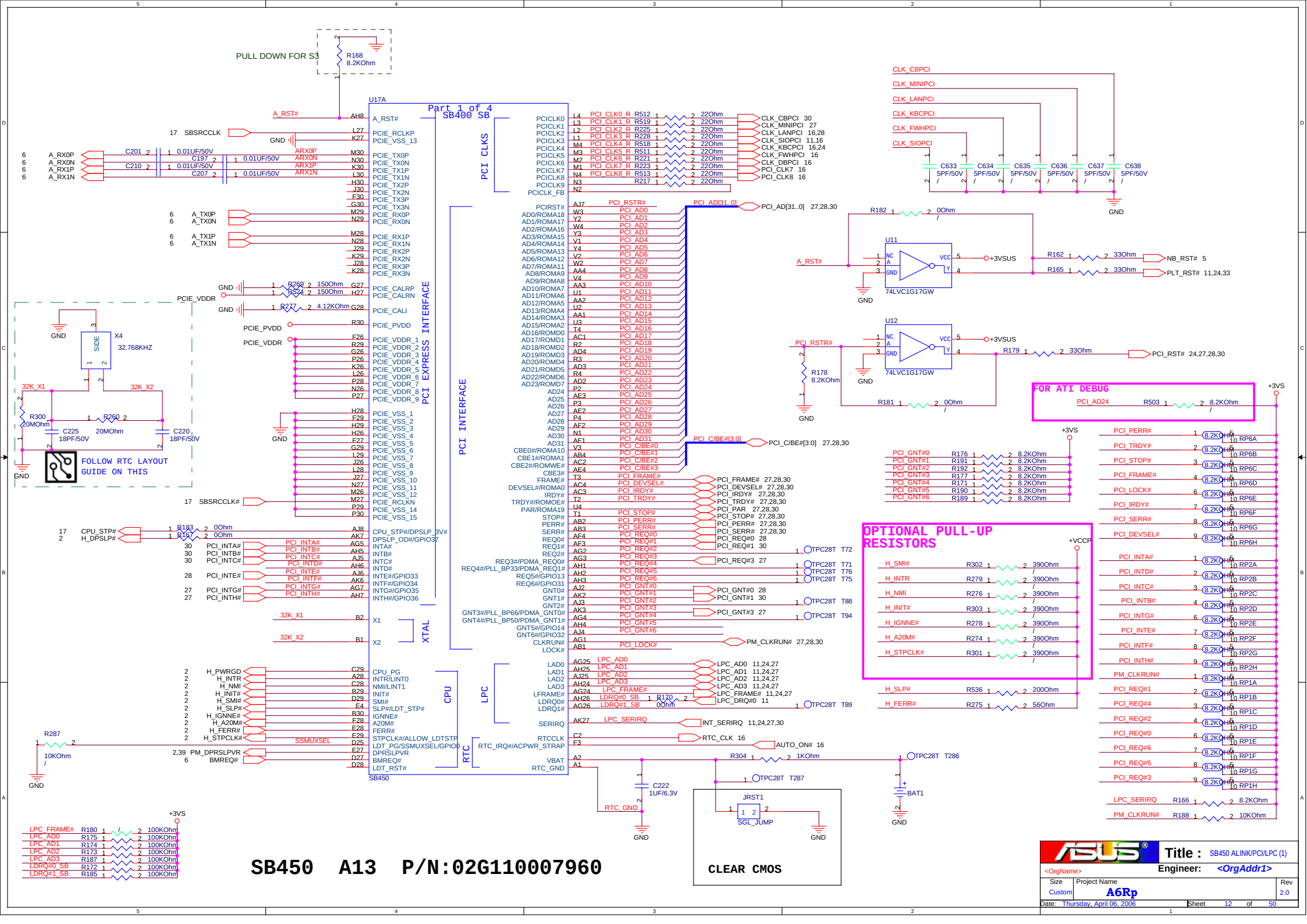
Title : SIO & SIR & PRINTER PORT

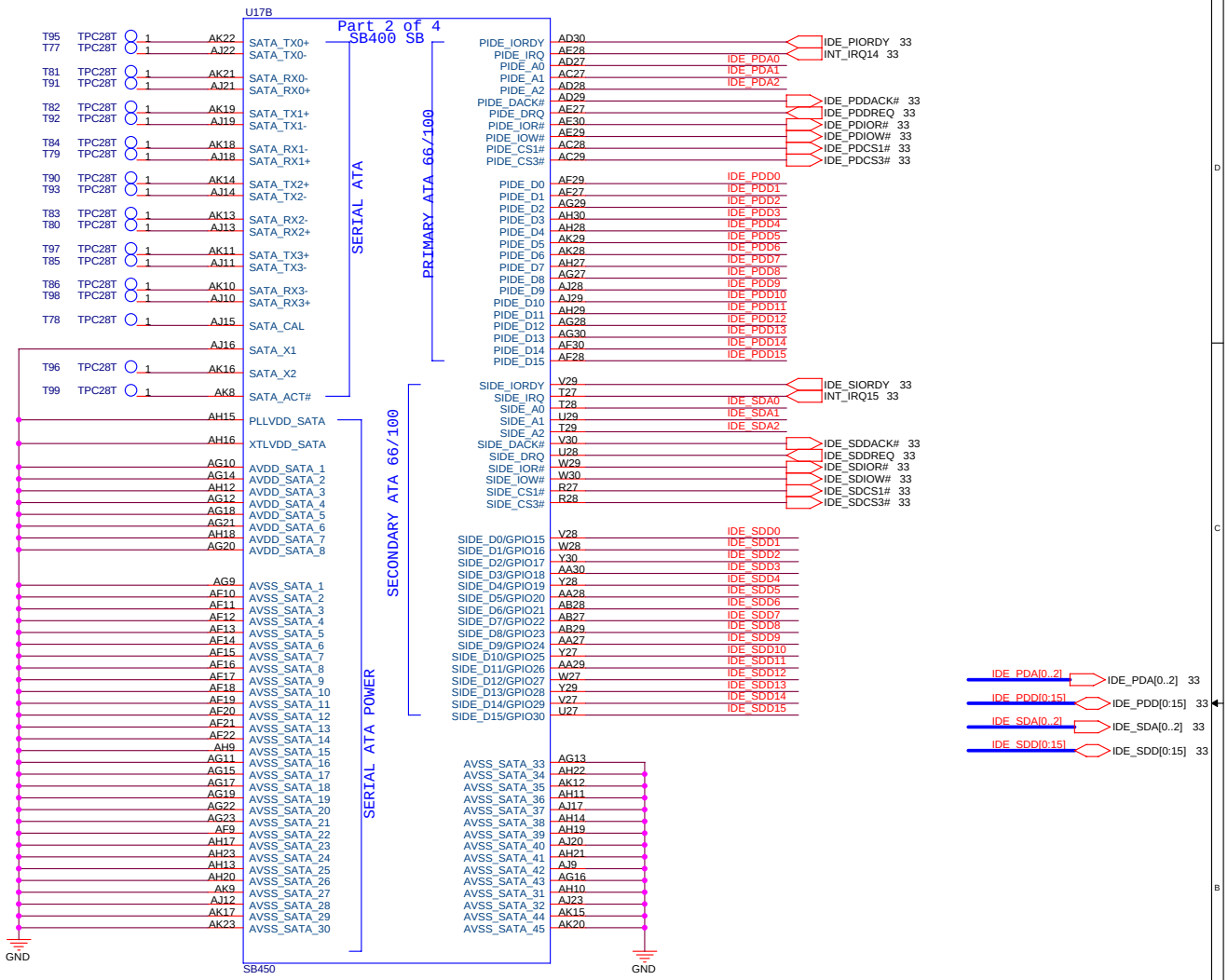
<OrgName>

Engineer: <OrgAddr1>

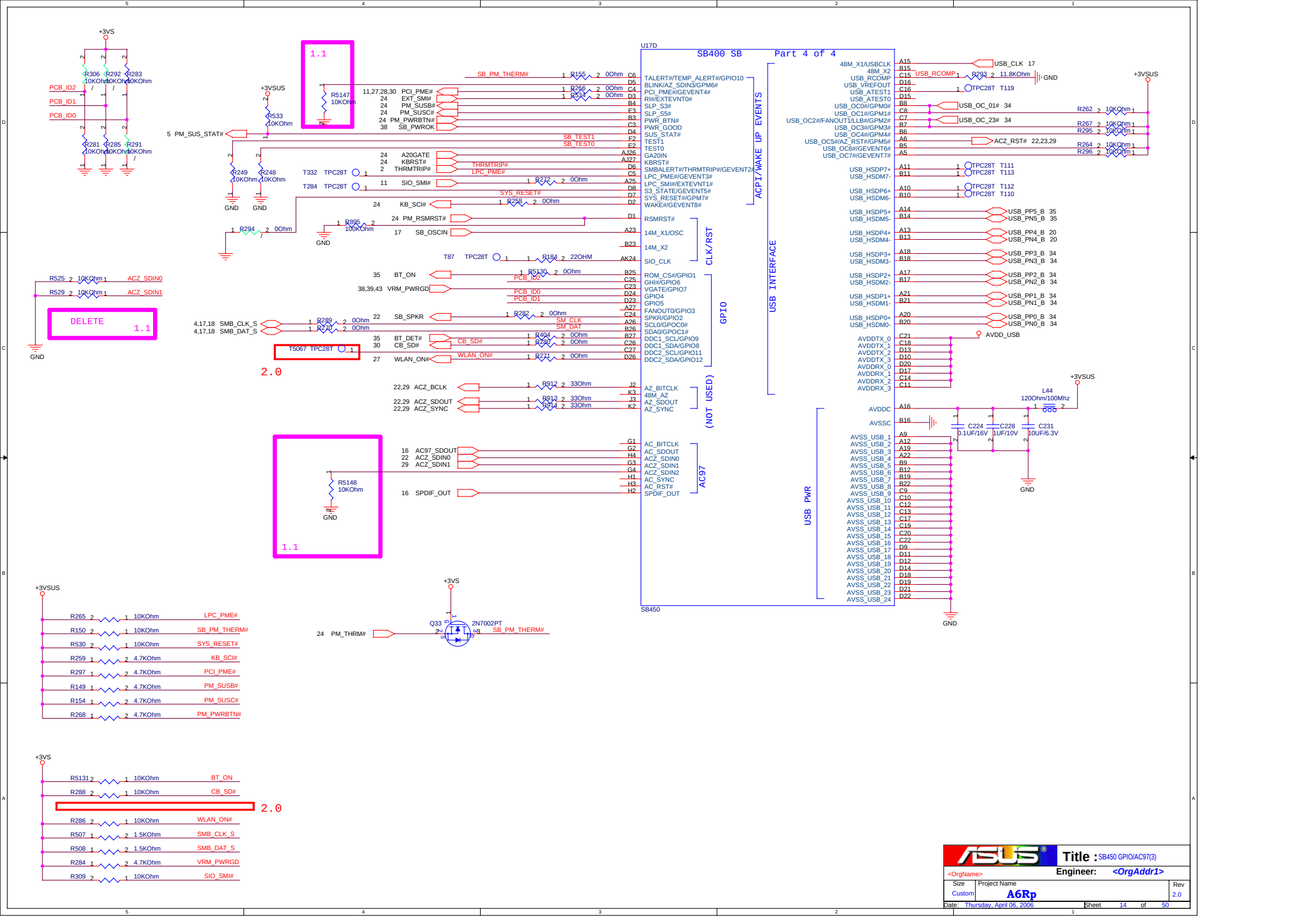
Size	Project Name	Rev
Custom	A6Rp	2.0

Date: Thursday, April 06, 2006 Sheet 11 of 50


PULL DOWN FOR S3
R168 8.2KOhm
U17A
Part 1 of 4
SB400 SB
A_RST#
SBSRCCLK
A_RX0P
A_RX0N
A_RX1P
A_RX1N
A_TX0P
A_TX0N
A_TX1P
A_TX1N
PCI EXPRESS INTERFACE
PCI CLKS
PCI INTERFACE
CPU
LPC
RTC
XTAL
SB450
X4
32.768KHZ
32K_X1
32K_X2
FOLLOW RTC LAYOUT GUIDE ON THIS
SBSRCCLK#
CPU_STP#
H_DPSLP#
PCI_INTA#
PCI_INTB#
PCI_INTC#
PCI_INTD#
PCI_INTE#
PCI_INTF#
PCI_INTG#
PCI_INTH#
H_PWRGD
H_INTR
H_NMI
H_INIT#
H_SMI#
H_SLP#
H_IGNNE#
H_A20M#
H_FERR#
H_STPCLK#
SSMUXSEL
PM_DPRSLPVR
BMREQ#
R287
10KOhm
CLK_CBPCI
CLK_MINIPCI
CLK_LANPCI
CLK_KBCPCI
CLK_FWHPCI
CLK_SIOPCI
C633 5PF/50V
C634 5PF/50V
C635 5PF/50V
C636 5PF/50V
C637 5PF/50V
C638 5PF/50V
PCI_AD[31..0]
PCI_C/BE#[3:0]
PCI_FRAME#
PCI_DEVSEL#
PCI_IRDY#
PCI_TRDY#
PCI_PAR
PCI_STOP#
PCI_PERR#
PCI_SERR#
PCI_REQ#0
PCI_REQ#1
PCI_REQ#2
PCI_REQ#3
PCI_GNT#0
PCI_GNT#1
PCI_GNT#2
PCI_GNT#3
PCI_GNT#4
PCI_GNT#5
PCI_GNT#6
PCI_LOCK#
PM_CLKRUN#
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
LPC_DRQ#0
LPC_SERIRQ
INT_SERIRQ
RTC_CLK
AUTO_ON#
RTC_IRQ#/ACPWR_STRAP
RTC_GND
C222 1UF/6.3V
R304 1KOhm
BAT1
JRST1
SGL_JUMP
CLEAR CMOS
NB_RST#
PLT_RST#
PCI_RST#
U11
U12
74LVC1G17GW
+3VSUS
R182 0Ohm
R162 33Ohm
R165 33Ohm
R178 8.2KOhm
R179 33Ohm
R181 0Ohm
FOR ATI DEBUG
PCI_AD24
R503 8.2KOhm
+3VS
+VCCP
OPTIONAL PULL-UP RESISTORS
H_SMI#
H_INTR
H_NMI
H_INIT#
H_IGNNE#
H_A20M#
H_STPCLK#
H_SLP#
H_FERR#
390Ohm
200Ohm
56Ohm
RP6A
RP6B
RP6C
RP6D
RP6E
RP6F
RP6G
RP6H
RP2A
RP2B
RP2C
RP2D
RP2E
RP2F
RP2G
RP2H
RP1A
RP1B
RP1C
RP1D
RP1E
RP1F
RP1G
RP1H
LPC_SERIRQ
PM_CLKRUN#
8.2KOhm
10KOhm
100KOhm
SB450 A13 P/N:02G110007960
Title : SB450 ALINK/PCI/LPC (1)
Engineer: <OrgAddr1>
<OrgName>
Project Name
A6Rp
Size
Custom
Rev
2.0
Date: Thursday, April 06, 2006
Sheet 12 of 50

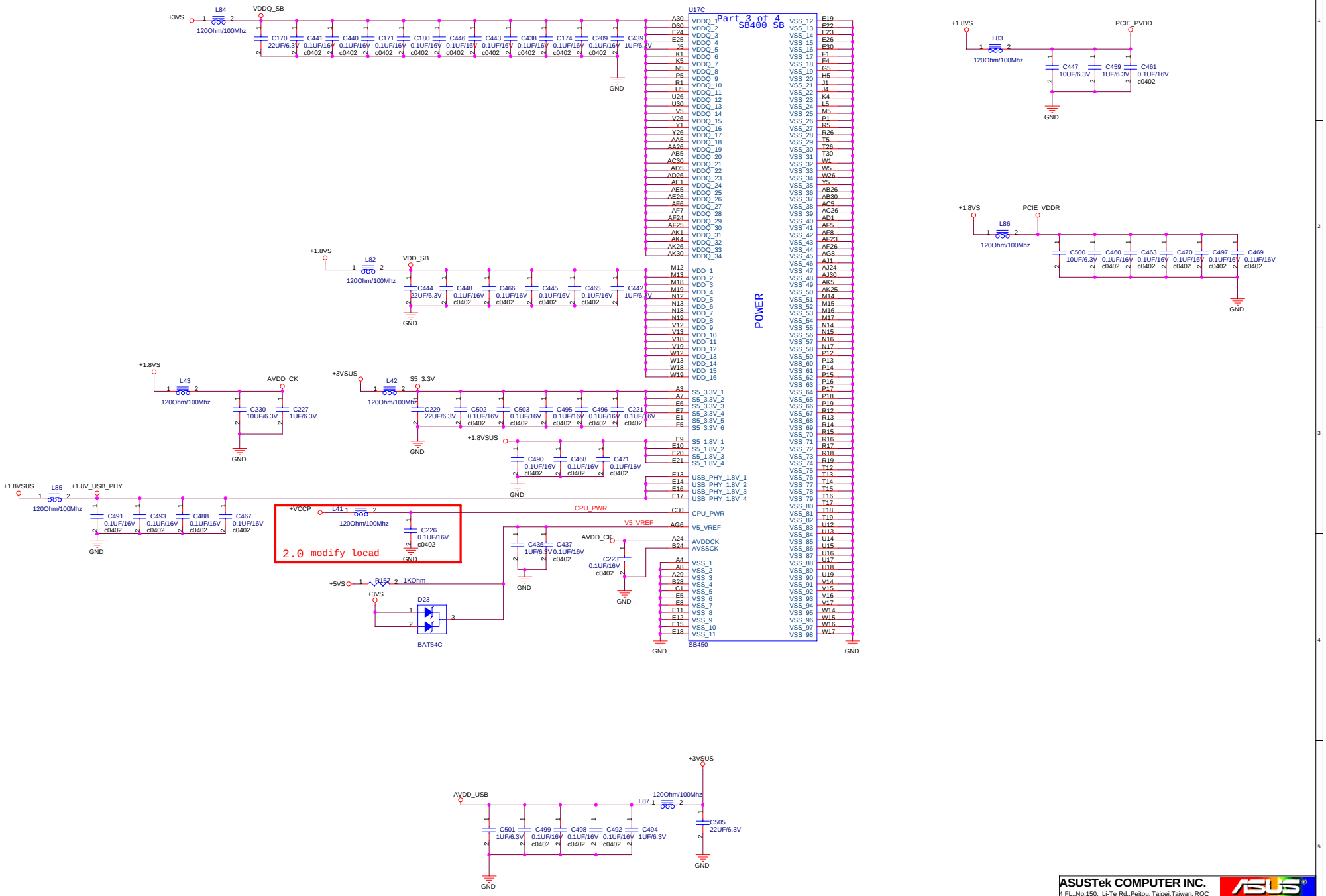


Title : SB450 IDE/USB/MII (2)		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 13 of 50	



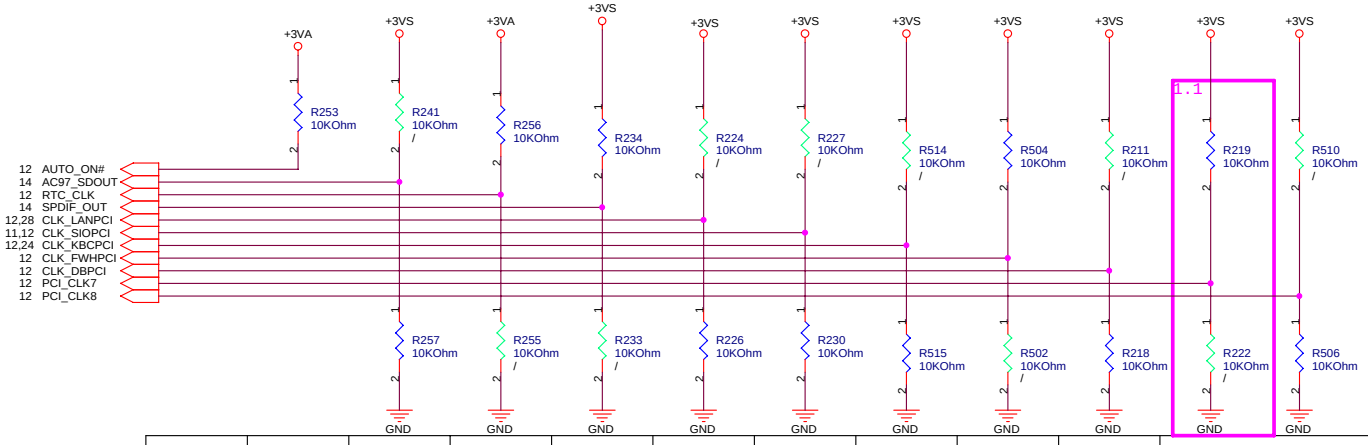
<OrgName>		Engineer:	<OrgAddr1>
Size	Project Name		Rev
Custom	A6Rp		2.0
Date: Thursday, April 06, 2006		Sheet 14 of 50	

Title : SB450 GPIO/AC97(3)



ASUSTek COMPUTER INC.		
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC		
Title: SB450 PWR/DECOUPLING(4)		
Size: Custom	Document Number: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 15 of 50	

REQUIRED STRAPS



	AUTO_ON#	AC_SDOUT	RTC_CLK	SPDIF_OUT	CLK_LANPCI	CLK_SIOPCI	CLK_KBCPCI	CLK_FWHPCI	CLK_DBPCI	PCI_CLK7 PCI_CLK8
PULL HIGH	MANUAL PWR ON	USE DEBUG STRAPS	INTERNAL RTC	SIO 24MHz	SEE NOTE1	USB PHY PWRDOWN DISABLE	USE USB PLL	SEE NOTE2	CPU I/F = K8	ROM TYPE H,H = PCI ROM H,L = LPC ROM I DEFAULT LPC Address Mapped below 1M L,H = LPC ROM II LPC Address Mapped to top 4G L,L = FWH ROM
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz		USB PHY PWRDOWN ENABLE	BYPASS USB PLL		CPU I/F = P4	

NOTE

1. USB CLK STRAPPING CHANGE

	A21,A22,A23	A31 AND NEWER
10K PULL UP	OSC/CLOCK BUFFER	CRYSTAL PAD
10K PULL DOWN	CRYSTAL PAD	OSC/CLOCK BUFFER

2. 14MHz CLOCK TYPE STRAPPING

	A11~A31	A32 AND ABOVE
	14MHz CLOCK PAD IS CRYSTAL PAD	PCIE COMMON MODE SETTING
10K PULL UP	CLOCK INPUT BUFFER	PCIE CM_SET LOW
10K PULL DOWN	CRYSTAL PAD	PCIE CM_SET HIGH

ASUS

Title : SB450 STRAPS(5)

<OrgName> Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	A6Rp	2.0

Date: Thursday, April 06, 2006 Sheet 16 of 50

PLACE termination close to source IC

CLK_CPU_BCLK R107 49.9Ohm
CLK_CPU_BCLK# R102 49.9Ohm
NB_CLK R96 49.9Ohm
NB_CLK# R94 49.9Ohm
A_LINKCLK R87 49.9Ohm
A_LINKCLK# R79 49.9Ohm
SBSRCCLK R444 49.9Ohm
SBSRCCLK# R442 49.9Ohm
NB_SRCCLK R76 49.9Ohm
NB_SRCCLK# R70 49.9Ohm
GND

CLKREQB# R875 4.7KOhm +3VS

+3VS L29 120Ohm/100Mhz CLK_VDD
C140 22UF/6.3V
C141 0.1UF/25V
C397 0.1UF/25V
C388 0.1UF/25V
C391 0.1UF/25V
C376 0.1UF/25V
C381 0.1UF/25V
C125 0.1UF/25V
L25 120Ohm/100Mhz CLK_VDD_USB
C129 0.1UF/25V
GND

CLK_VDD
CLK_VDD_USB
U6
VDDCPU 45
VDDSRC3 35
VDDATI 32
VDDSRC2 21
VDDSRC1 14
VDD48 3
VDDPCI 51
VDDREF 56
GNDCPU 44
GNDSRC4 36
GNDATI 31
GNDSRC3 26
GNDSRC2 20
GNDPCI 49
GNDSRC1 15
GND2 55
GND1 5
X2 2
X1 1
VTTPWR_GD/PD# 6
SCLK 7
SDATA 8
IREF 37
ICS951417AFLFT

X2 14.318Mhz
C133 47PF/50V
C132 47PF/50V
XIN_CLKGEN
XOUT_CLKGEN

R114 0Ohm
4,14,18 SMB_CLK_S
4,14,18 SMB_DAT_S
R449 475Ohm

VDDA L28 120Ohm/100Mhz +3VS
C107 0.1UF/25V
C139 22UF/6.3V
VDDA 39
GNDA 38

CPUCLKT0 47 CPUCLKT0 R106 33Ohm CLK_CPU_BCLK → CLK_CPU_BCLK 2
CPUCLKC0 46 CPUCLKC0 R103 33Ohm CLK_CPU_BCLK# → CLK_CPU_BCLK# 2
CPUCLKT1 43 CPUCLKT1 R104 33Ohm NB_CLK → NB_CLK 8
CPUCLKC1 42 CPUCLKC1 R97 33Ohm NB_CLK# → NB_CLK# 8
CPUCLKT2_ITP 41 2.0 TPC28T T237
CPUCLKC2_ITP 40 TPC28T T234
CPU_STOP# 48 CPUSTOP# R108 0Ohm → CPU_STP# 12

SRCCLKT0 34 SRCCLKT0 R88 33Ohm A_LINKCLK → A_LINKCLK 6
SRCCLKC0 33 SRCCLKC0 R80 33Ohm A_LINKCLK# → A_LINKCLK# 6
SRCCLKT3 24 SRCCLKT3 R78 33Ohm SBSRCCLK → SBSRCCLK 12
SRCCLKC3 25 SRCCLKC3 R72 33Ohm SBSRCCLK# → SBSRCCLK# 12
SRCCLKT4 22 TPC28T T42
SRCCLKC4 23 TPC28T T43
SRCCLKT5 18 TPC28T T48
SRCCLKC5 19 TPC28T T49
SRCCLKT6 16 TPC28T T52
SRCCLKC6 17 2.0
SRCCLKT7 12 2.0 TPC28T T54
SRCCLKC7 13 TPC28T T55

ATIGCLKT0 30 ATIGCLKT0 R77 33Ohm / NB_SRCCLK → NB_SRCCLK 6
ATIGCLKC0 29 ATIGCLKC0 R71 33Ohm / NB_SRCCLK# → NB_SRCCLK# 6
ATIGCLKT1 27 TPC28T T26
ATIGCLKC1 28 TPC28T T27 2.0

CLKREQA# 10 R459 0Ohm / GND
DOC/CLKREQB# 11 CLKREQB# R457 0Ohm / GND
CK410#/PCICLK0 50 R113 33Ohm
DOCEN/USB_48MHz 4 USB_48MHZ R117 33Ohm → USB_CLK 14
RESET# 9

FSLB/REF1 53 REF1 R115 4.7KOhm → CPU_BSEL1 2
FSLA/REF0 54 REF0 R123 4.7KOhm → CPU_BSEL0 2
FSLC/REF2 52 REF2 R110 4.7KOhm → CPU_BSEL2 2

R876 4.7KOhm GND

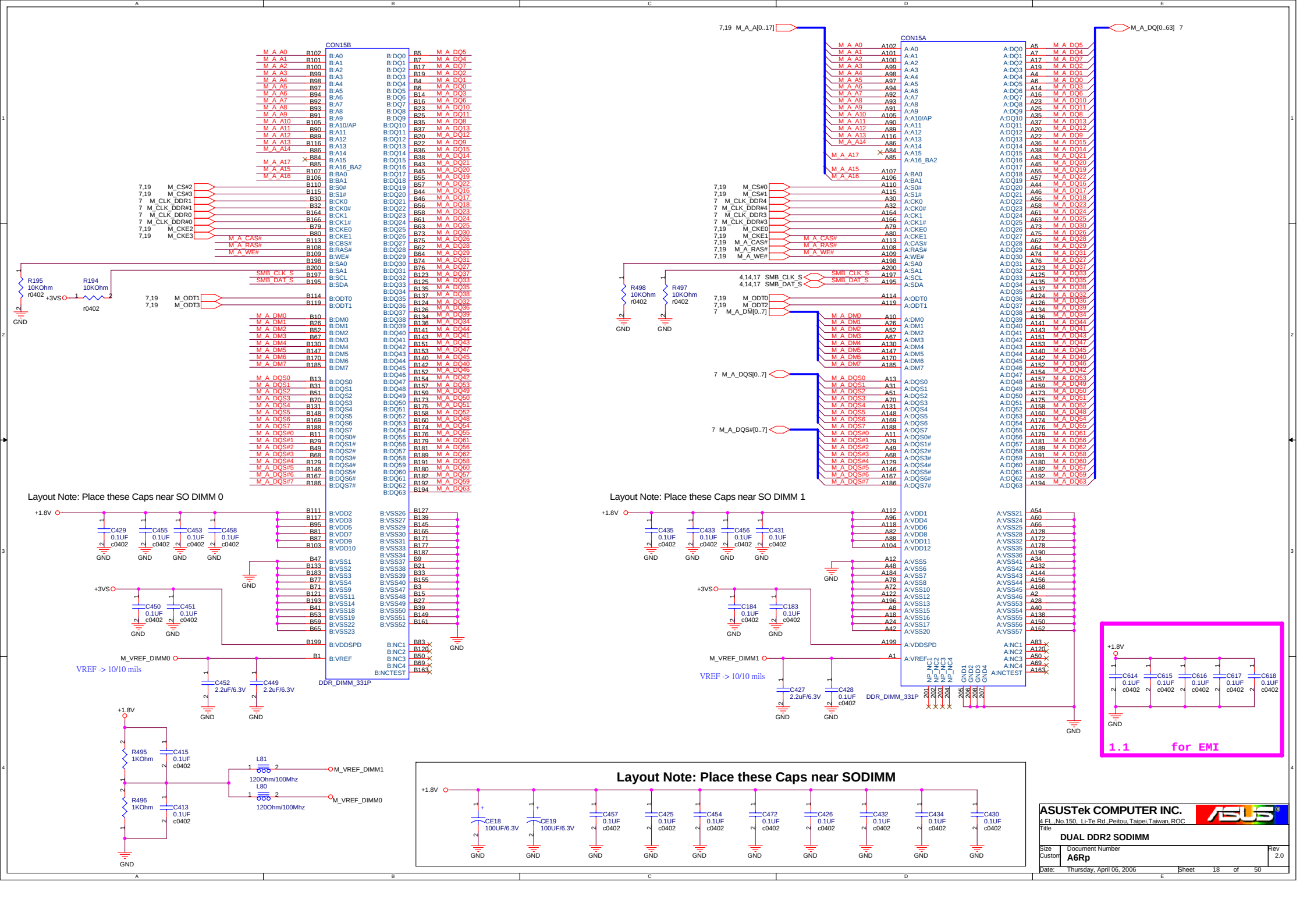
BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

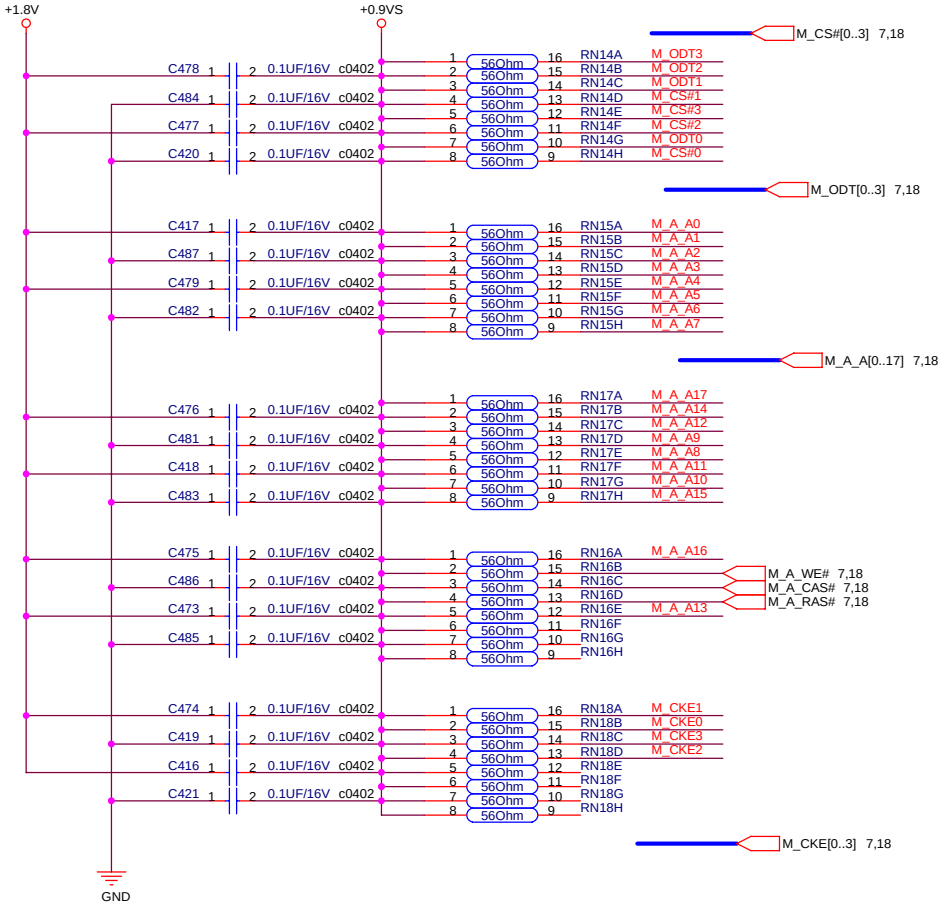
R128 33Ohm → OSC_14M 8
R111 33Ohm → SB_OSCIN 14

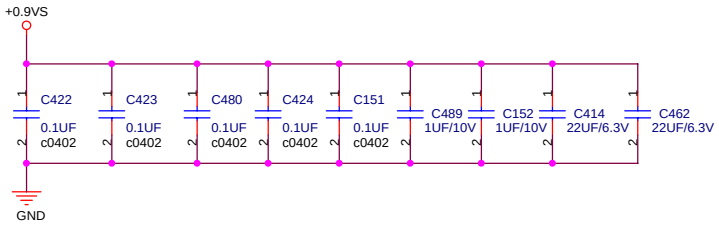
+3VS R229 4.7KOhm
39 CLK_EN# Q75 2N7002PT
R5158 0Ohm /
GND
1.1

<OrgName>		Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6Rp			Rev: 2.0
Date: Thursday, April 06, 2006		Sheet 17 of 50		

Title : CLOCK GENERATOR


CON15B
CON15A
DDR_DIMM_331P
DDR_DIMM_331P
Layout Note: Place these Caps near SO DIMM 0
Layout Note: Place these Caps near SO DIMM 1
Layout Note: Place these Caps near SODIMM
VREF -> 10/10 mils
VREF -> 10/10 mils
1.1 for EMI
ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC
DUAL DDR2 SODIMM
A6Rp
2.0
Thursday, April 06, 2006
18
50

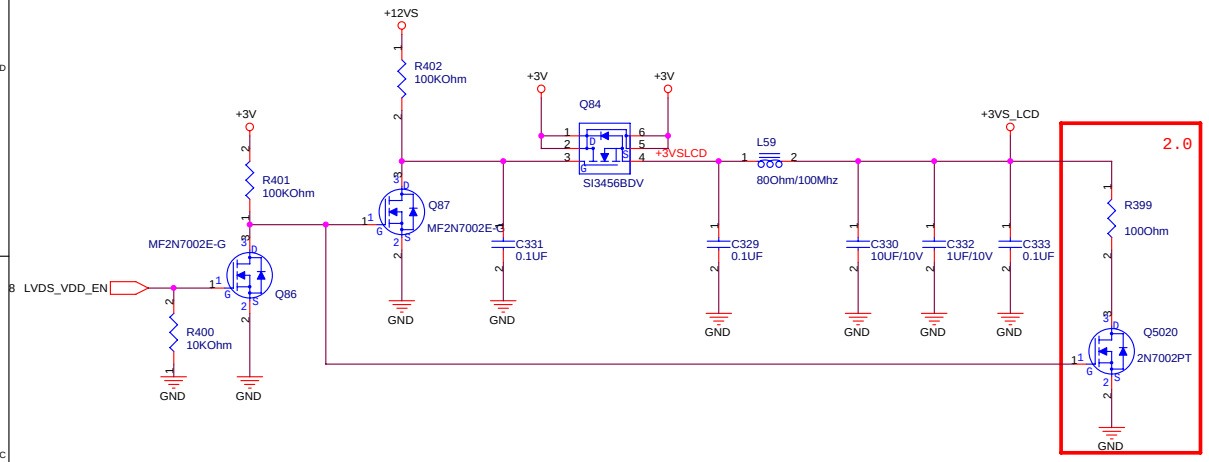




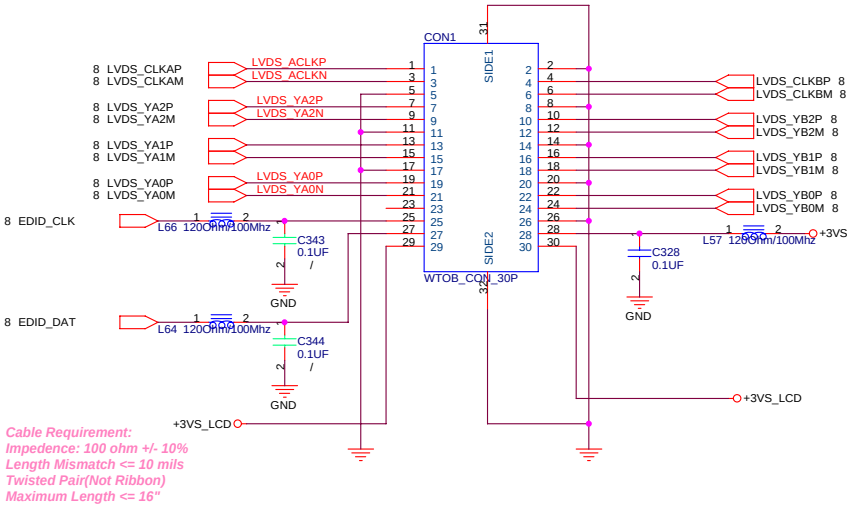
Title : DDR2 TERMINATION		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 19 of 50	

LCD Power

3V-3.6V
Full Active: 410 mA(Max. 500 mA)



LCD LVDS Interface

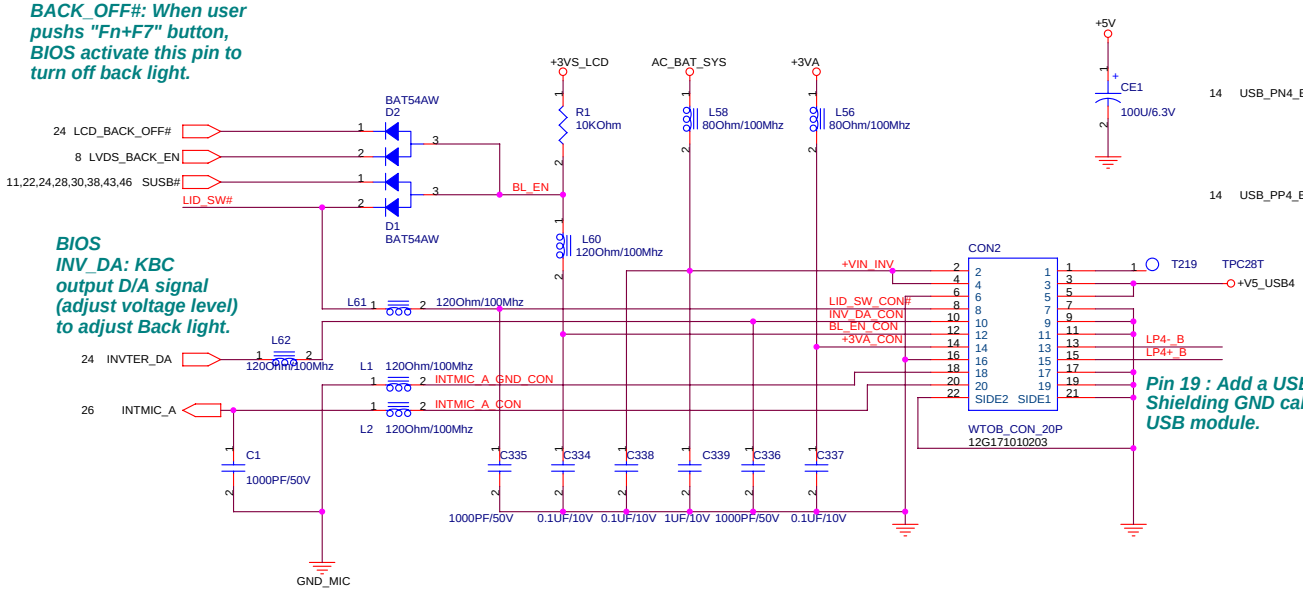


Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

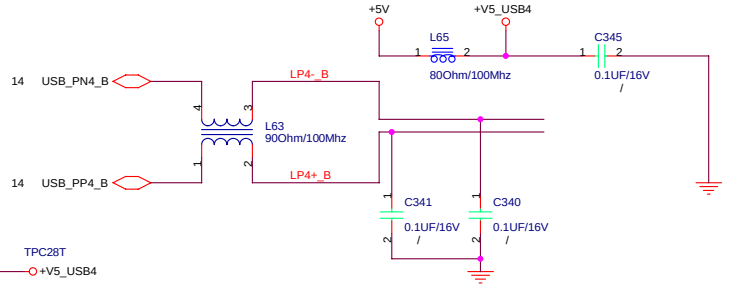
INVERTER Interface

BIOS
BACK_OFF#: When user pushs "Fn+F7" button, BIOS activate this pin to turn off back light.

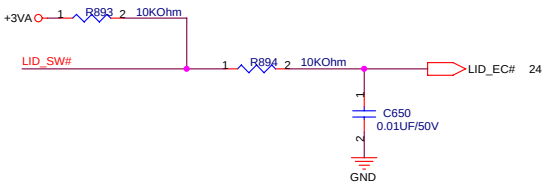
BIOS
INV_DA: KBC output D/A signal (adjust voltage level) to adjust Back light.



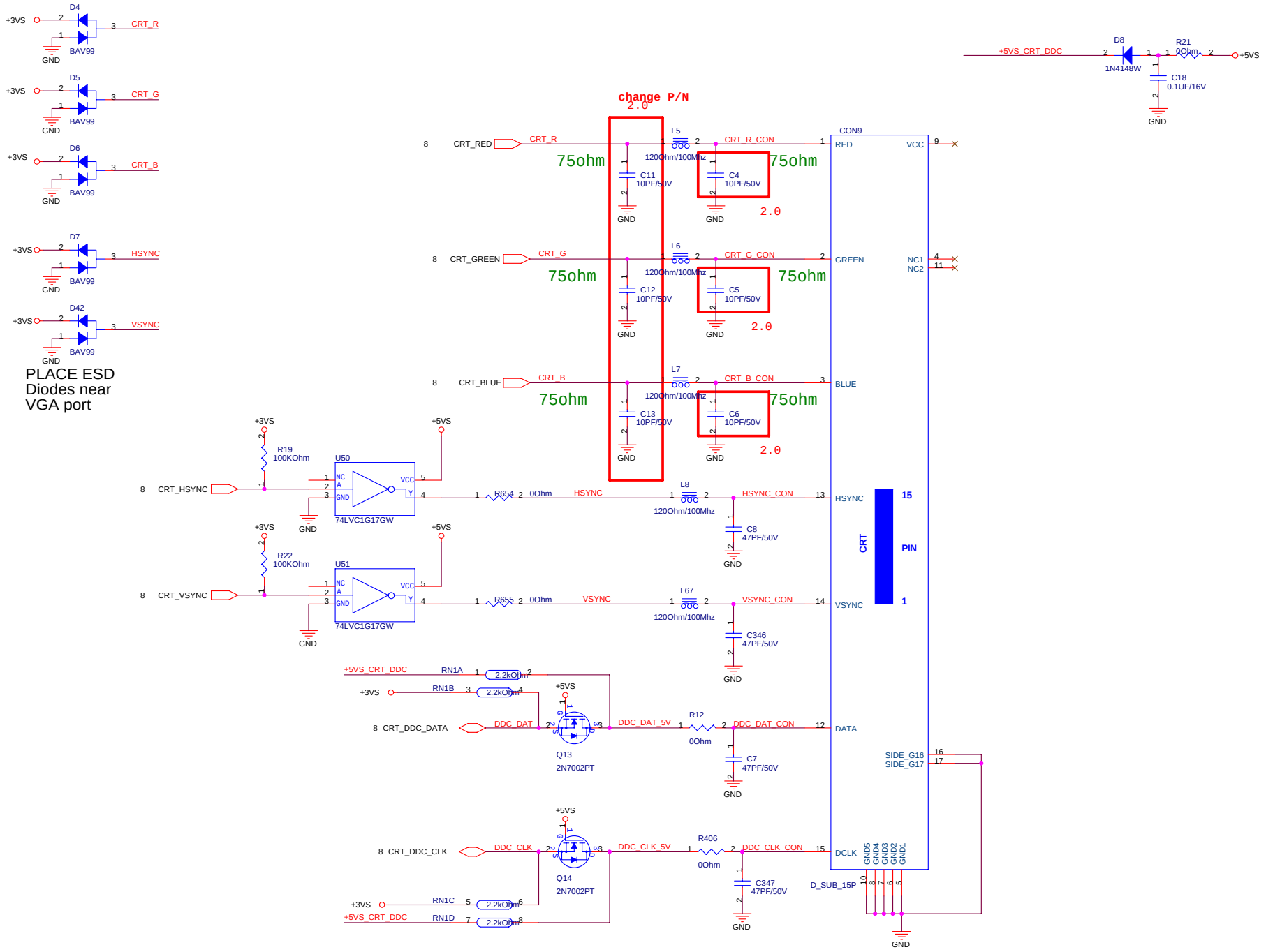
Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.



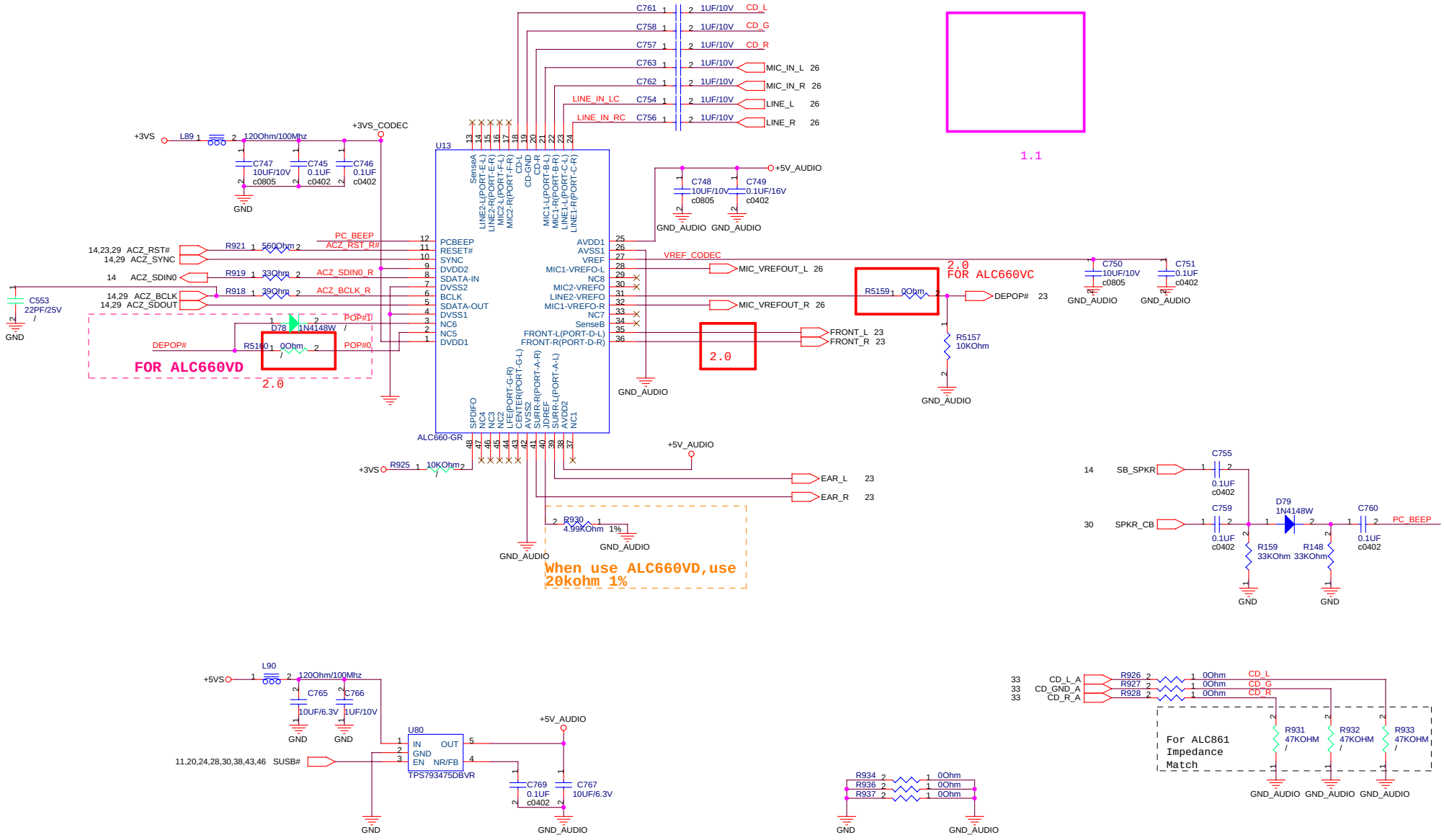
USB PORT 4 for USB CAMERA



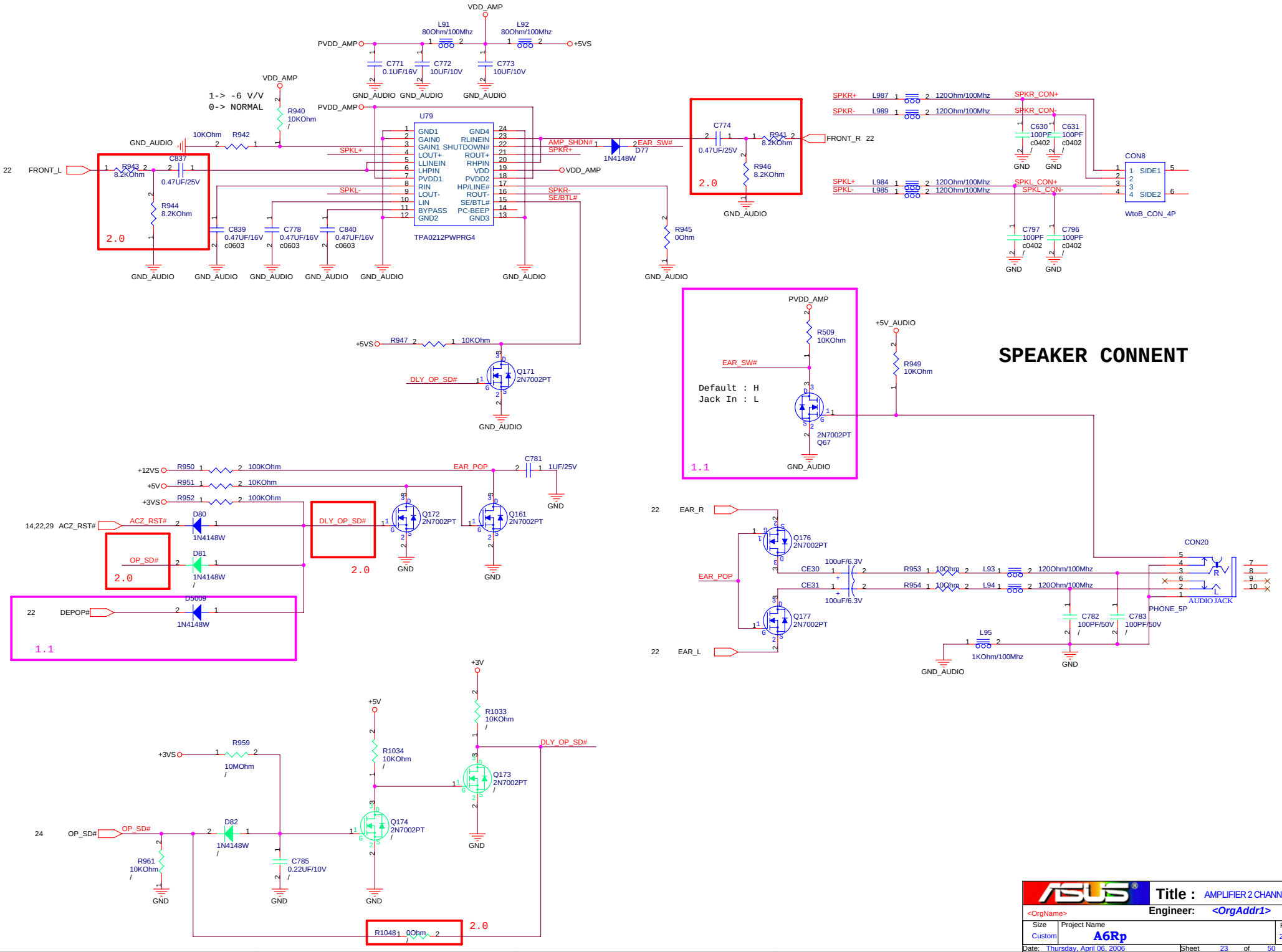
ASUS	Title :	LVDS & INVERTER (CAMERA)
<OrgName>	Engineer:	<OrgAddr1>
Size: Custom	Project Name: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 20 of 50	

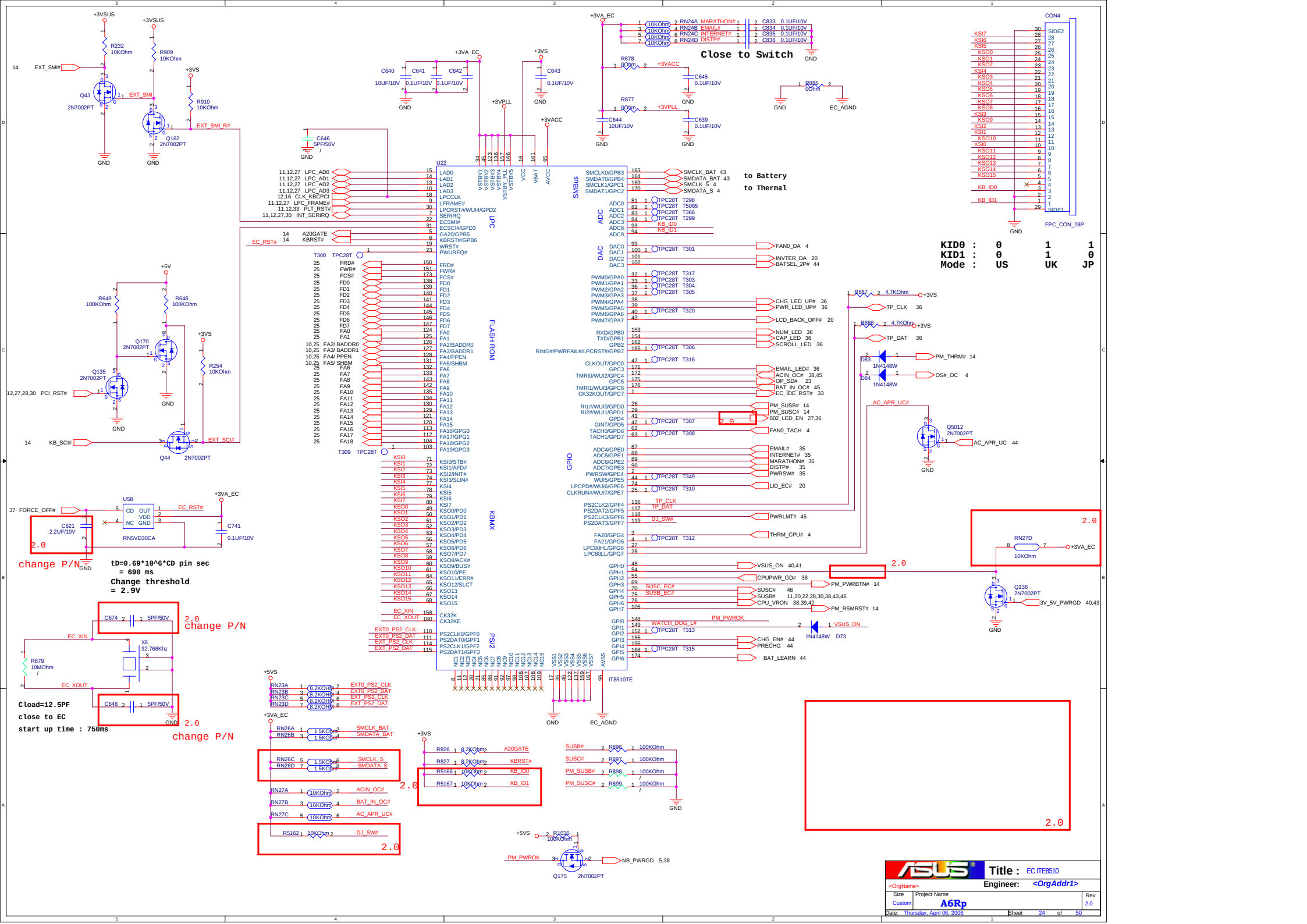


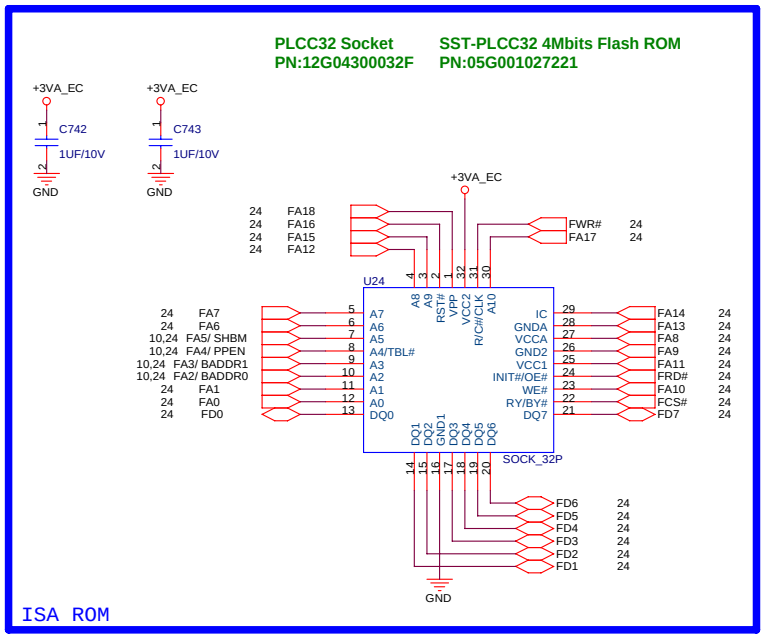
Title : CRT CONNECTOR			
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6Rp		Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 21 of 50		



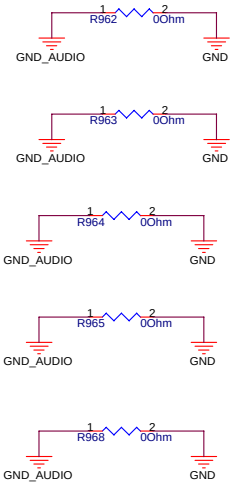
Title : AZALIA		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 22 of 50	


SPEAKER CONNENT
VDD_AMP
PVDD_AMP
+5VS
L91 80Ohm/100Mhz
L92 80Ohm/100Mhz
C771 0.1UF/16V
C772 10UF/10V
C773 10UF/10V
GND_AUDIO
1-> -6 V/V
0-> NORMAL
R940 10KOhm
R942 10KOhm
R943 8.2KOhm
C837 0.47UF/25V
R944 8.2KOhm
22 FRONT_L
U79
TPA0212PWPRG4
GND1 GND4
GAIN0 RLINEIN
GAIN1 SHUTDOWN#
LOUT+ ROUT+
LLINEIN RHPIN
LHPIN VDD
PVDD1 PVDD2
RIN HP/LINE#
LOUT- ROUT-
LIN SE/BTL#
BYPASS PC-BEEP
GND2 GND3
SPKL+
SPKL-
SPKR-
SE/BTL#
AMP_SHDN#
SPKR+
EAR_SW#
D77 1N4148W
C839 0.47UF/16V c0603
C778 0.47UF/16V c0603
C840 0.47UF/16V c0603
R945 0Ohm
C774 0.47UF/25V
R941 8.2KOhm
R946 8.2KOhm
2.0
FRONT_R 22
SPKR+ L987 120Ohm/100Mhz
SPKR- L989 120Ohm/100Mhz
SPKR_CON+
SPKR_CON-
C630 100PF c0402
C631 100PF c0402
SPKL+ L984 120Ohm/100Mhz
SPKL- L985 120Ohm/100Mhz
SPKL_CON+
SPKL_CON-
C797 100PF c0402
C796 100PF c0402
CON8
SIDE1
SIDE2
WtoB_CON_4P
+5VS R947 10KOhm
DLY_OP_SD#
Q171 2N7002PT
PVDD_AMP
R509 10KOhm
EAR_SW#
Default : H
Jack In : L
Q67 2N7002PT
1.1
+5V_AUDIO
R949 10KOhm
+12VS R950 100KOhm
+5V R951 10KOhm
+3VS R952 100KOhm
EAR_POP
C781 1UF/25V
14,22,29 ACZ_RST#
D80 1N4148W
OP_SD#
D81 1N4148W
Q172 2N7002PT
Q161 2N7002PT
22 DEPOP#
D5009 1N4148W
22 EAR_R
22 EAR_L
Q176 2N7002PT
Q177 2N7002PT
CE30 100uF/6.3V
CE31 100uF/6.3V
R953 10Ohm
R954 10Ohm
L93 120Ohm/100Mhz
L94 120Ohm/100Mhz
L95 1KOhm/100Mhz
CON20
R
L
AUDIO JACK
PHONE_5P
C782 100PF/50V
C783 100PF/50V
+3V
+5V
R959 10MOhm
R1033 10KOhm
R1034 10KOhm
24 OP_SD#
D82 1N4148W
Q173 2N7002PT
Q174 2N7002PT
C785 0.22UF/10V
R961 10KOhm
R1048 0Ohm
Title : AMPLIFIER 2 CHANNEL
Engineer: <OrgAddr1>
<OrgName>
Size Custom
Project Name A6Rp
Rev 2.0
Date: Thursday, April 06, 2006
Sheet 23 of 50

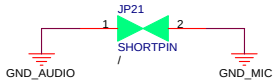

Close to Switch
to Battery
to Thermal
KID0 : 0 1 1
KID1 : 0 1 0
Mode : US UK JP
change P/N
tD=0.69*10^6*CD pin sec
= 690 ms
Change threshold
= 2.9V
Cload=12.5PF
close to EC
start up time : 750ms
Title : EC ITE8510
Engineer: <OrgAddr1>
<OrgName>
Project Name A6Rp
Size Custom
Rev 2.0
Date: Thursday, April 06, 2006
Sheet 24 of 50

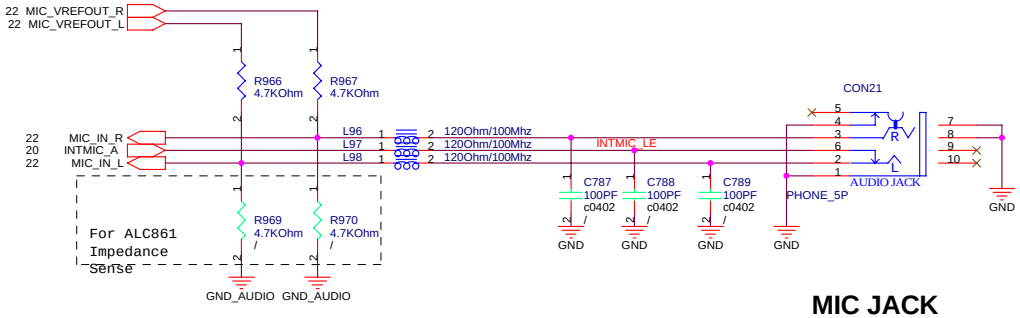


ASUS	Title : ISA ROM & SPI ROM	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 25 of 50	

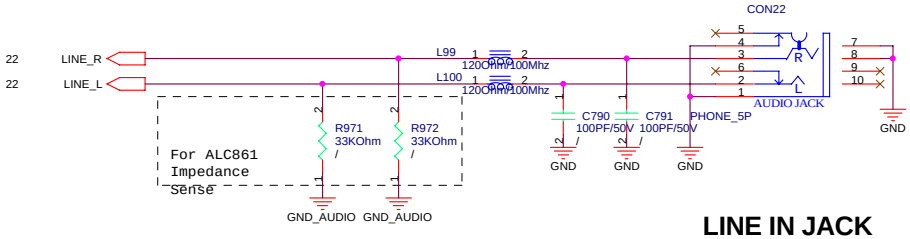


INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils



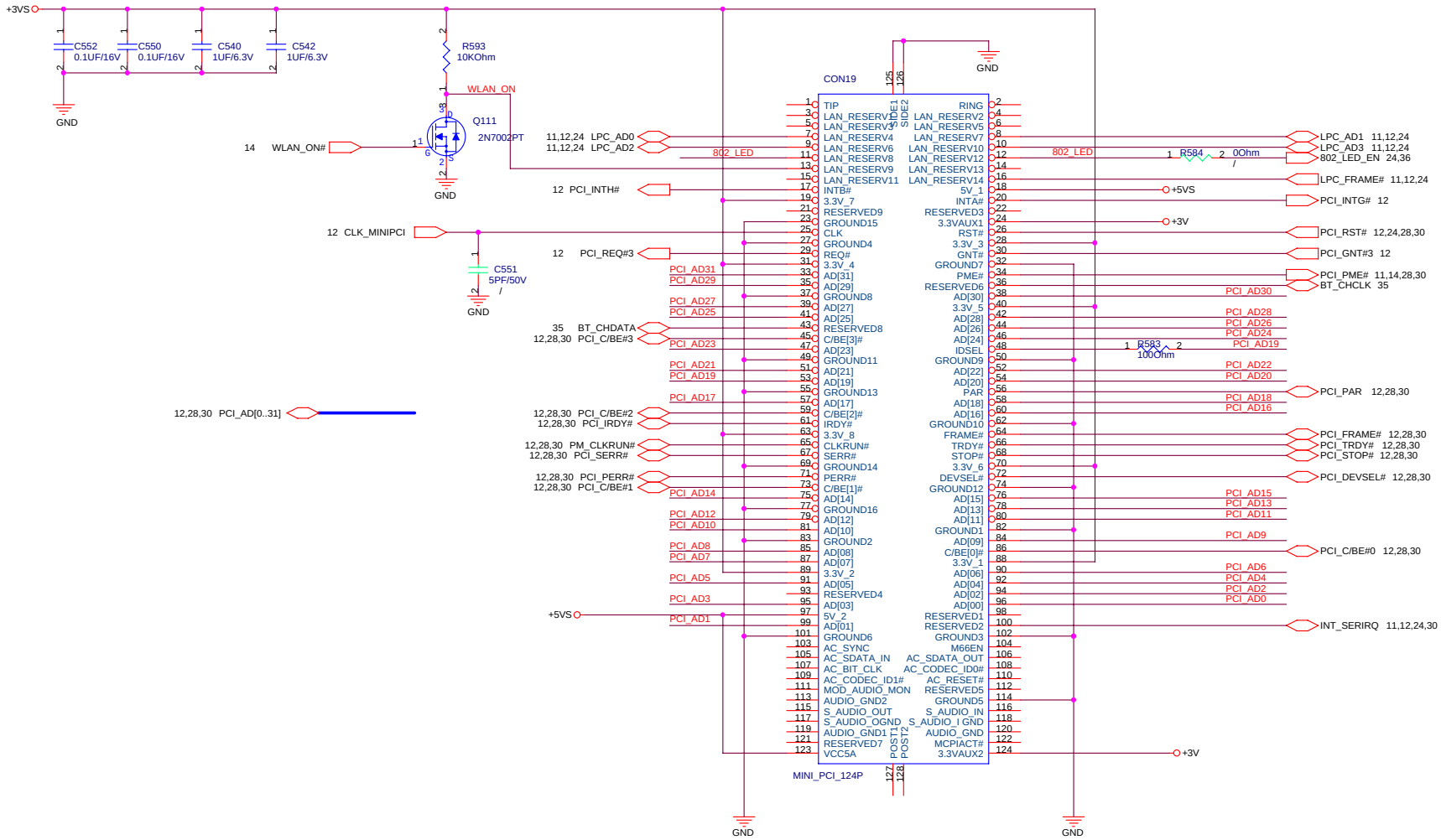


MIC JACK

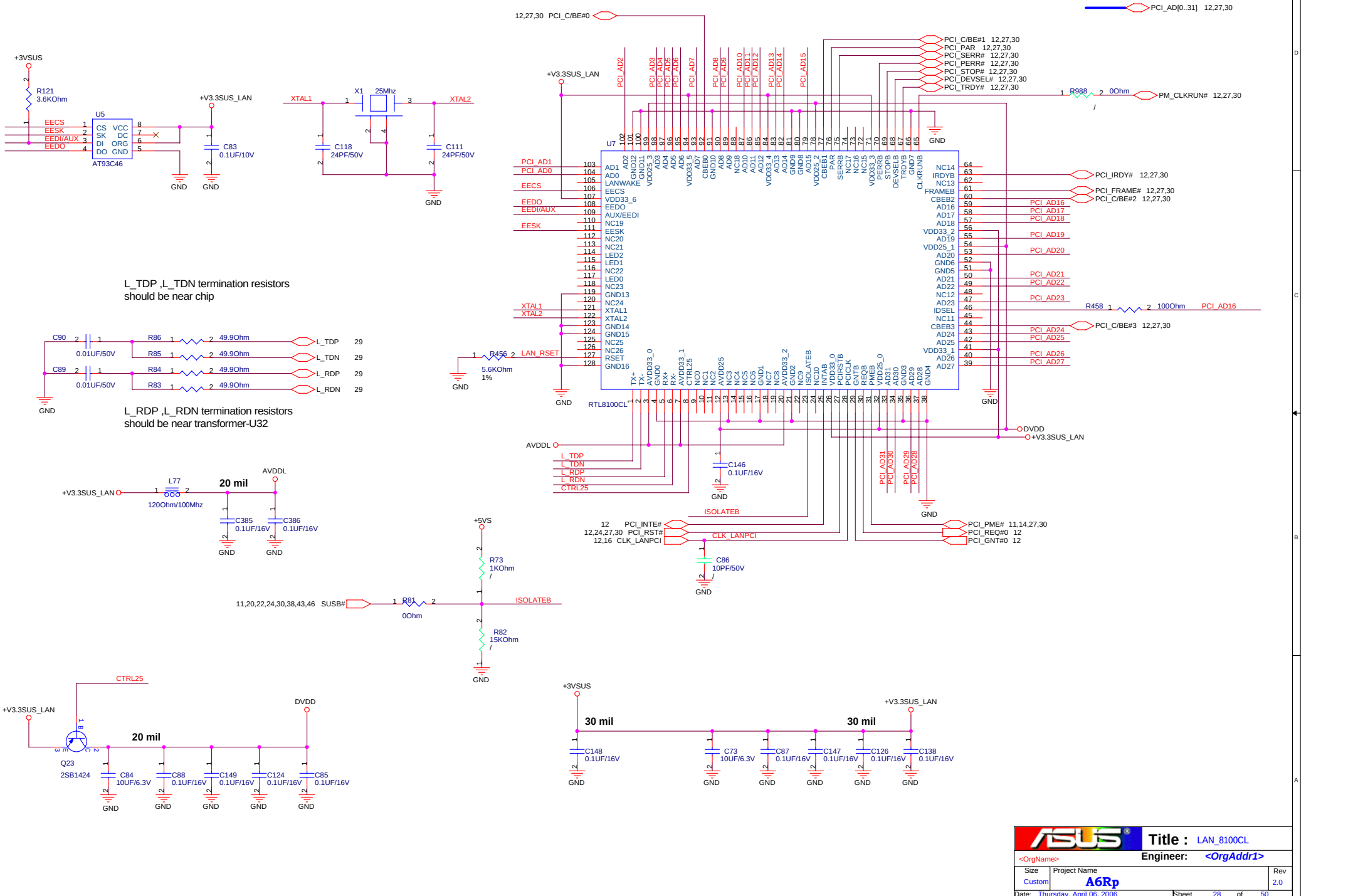


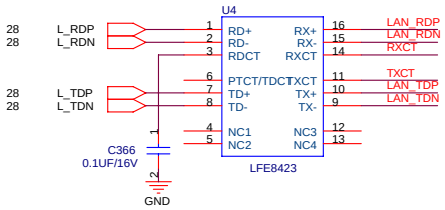
LINE IN JACK

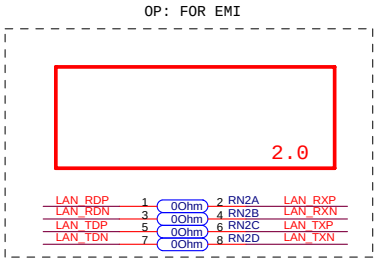
Title : MIC,LINE-IN JACK		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 26 of 50	

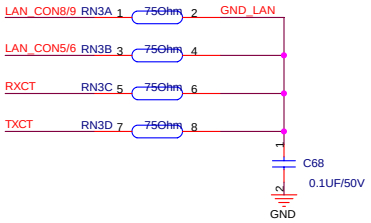


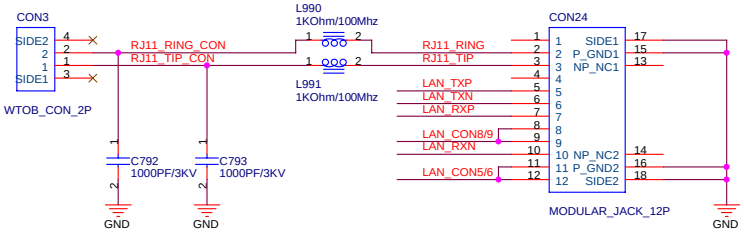
ASUS	Title : MINIPCI_WIRELESS		
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6Rp		Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 27 of 50		

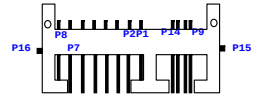

+3VSUS
R121
3.6KOhm
EECS
EESK
EEDI/AUX
EEDO
U5
CS VCC
SK DC
DI ORG
DO GND
AT93C46
+V3.3SUS_LAN
C83
0.1UF/10V
GND
XTAL1
X1
25Mhz
XTAL2
C118
24PF/50V
C111
24PF/50V
L_TDP ,L_TDN termination resistors
should be near chip
C90
0.01UF/50V
C89
0.01UF/50V
R86
R85
R84
R83
49.9Ohm
L_TDP
L_TDN
L_RDP
L_RDN
29
L_RDP ,L_RDN termination resistors
should be near transformer-U32
L77
120Ohm/100Mhz
20 mil
AVDDL
C385
C386
0.1UF/16V
+5VS
R73
1KOhm
R82
15KOhm
11,20,22,24,30,38,43,46 SUSB#
R81
0Ohm
ISOLATEB
CTRL25
DVDD
Q23
2SB1424
C84
10UF/6.3V
C88
C149
C124
C85
0.1UF/16V
12,27,30 PCI_C/BE#0
PCI_AD[0..31] 12,27,30
PCI_C/BE#1 12,27,30
PCI_PAR 12,27,30
PCI_SERR# 12,27,30
PCI_PERR# 12,27,30
PCI_STOP# 12,27,30
PCI_DEVSEL# 12,27,30
PCI_TRDY# 12,27,30
R988
0Ohm
PM_CLKRUN# 12,27,30
+V3.3SUS_LAN
U7
RTL8100CL
PCI_AD1
PCI_AD0
EECS
EEDO
EEDI/AUX
EESK
XTAL1
XTAL2
LAN_RSET
R456
5.6KOhm
1%
PCI_IRDY# 12,27,30
PCI_FRAME# 12,27,30
PCI_C/BE#2 12,27,30
PCI_AD16
PCI_AD17
PCI_AD18
PCI_AD19
PCI_AD20
PCI_AD21
PCI_AD22
PCI_AD23
PCI_AD24
PCI_AD25
PCI_AD26
PCI_AD27
R458
100Ohm
PCI_C/BE#3 12,27,30
DVDD
+V3.3SUS_LAN
C146
0.1UF/16V
L_TDP
L_TDN
L_RDP
L_RDN
CTRL25
ISOLATEB
12 PCI_INTE#
12,24,27,30 PCI_RST#
12,16 CLK_LANPCI
CLK_LANPCI
C86
10PF/50V
PCI_PME# 11,14,27,30
PCI_REQ#0 12
PCI_GNT#0 12
+3VSUS
+V3.3SUS_LAN
30 mil
30 mil
C148
C73
10UF/6.3V
C87
C147
C126
C138
0.1UF/16V
GND
Title : LAN_8100CL
<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name A6Rp
Rev 2.0
Date: Thursday, April 06, 2006
Sheet 28 of 50







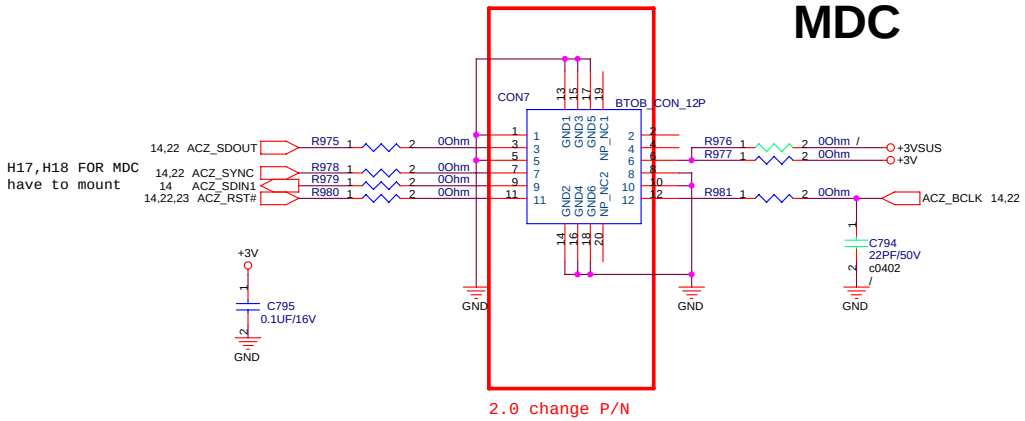




RJ 45 & RJ 11
BOTTOM VIEW

LAN PORT

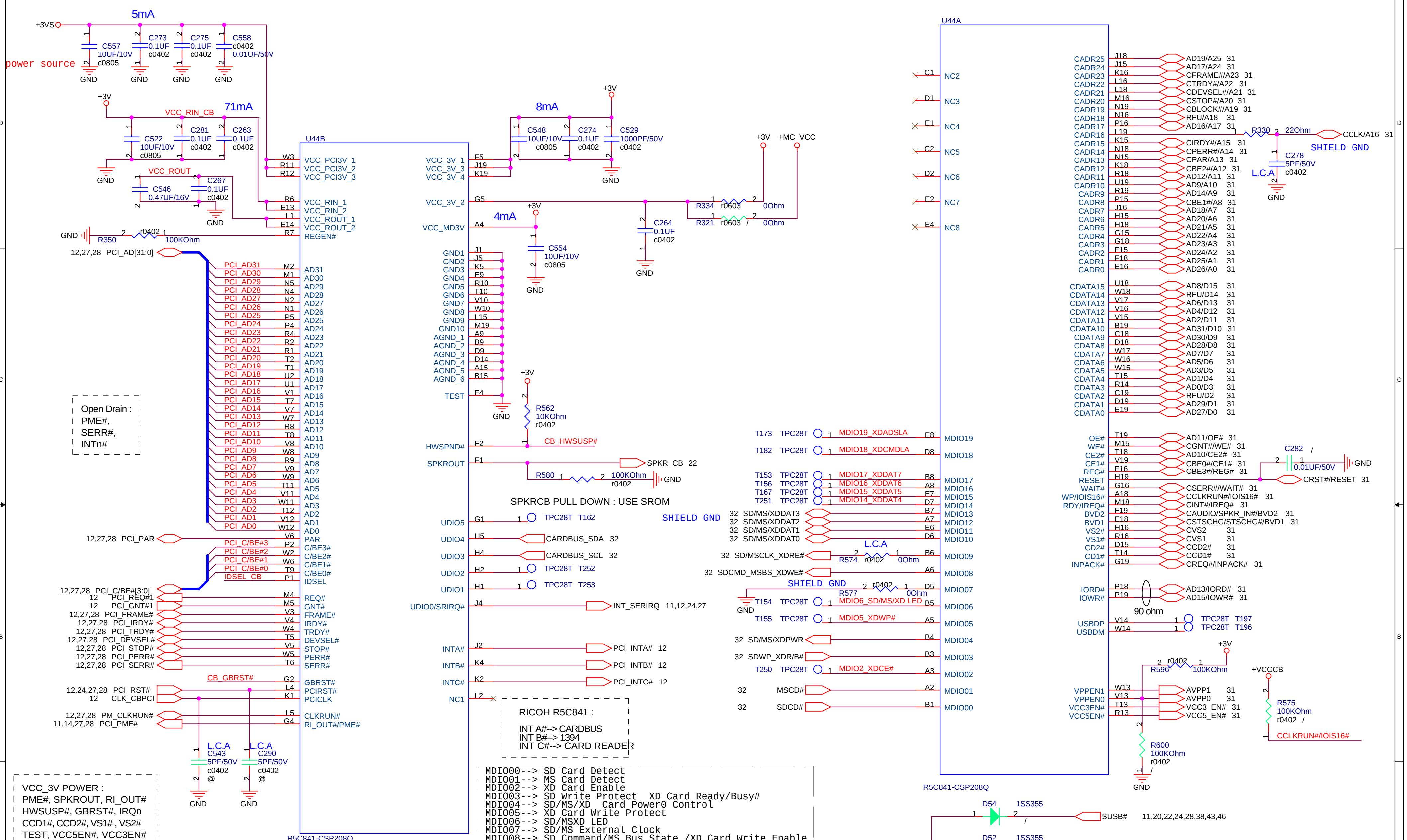
MDC



2.0 change P/N

MDC

ASUS	Title : RJ11+45 & MDC		
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6Rp		Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 29 of 50		



VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1#, VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F

VCCPCI POWER :
PCI BUS

VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG

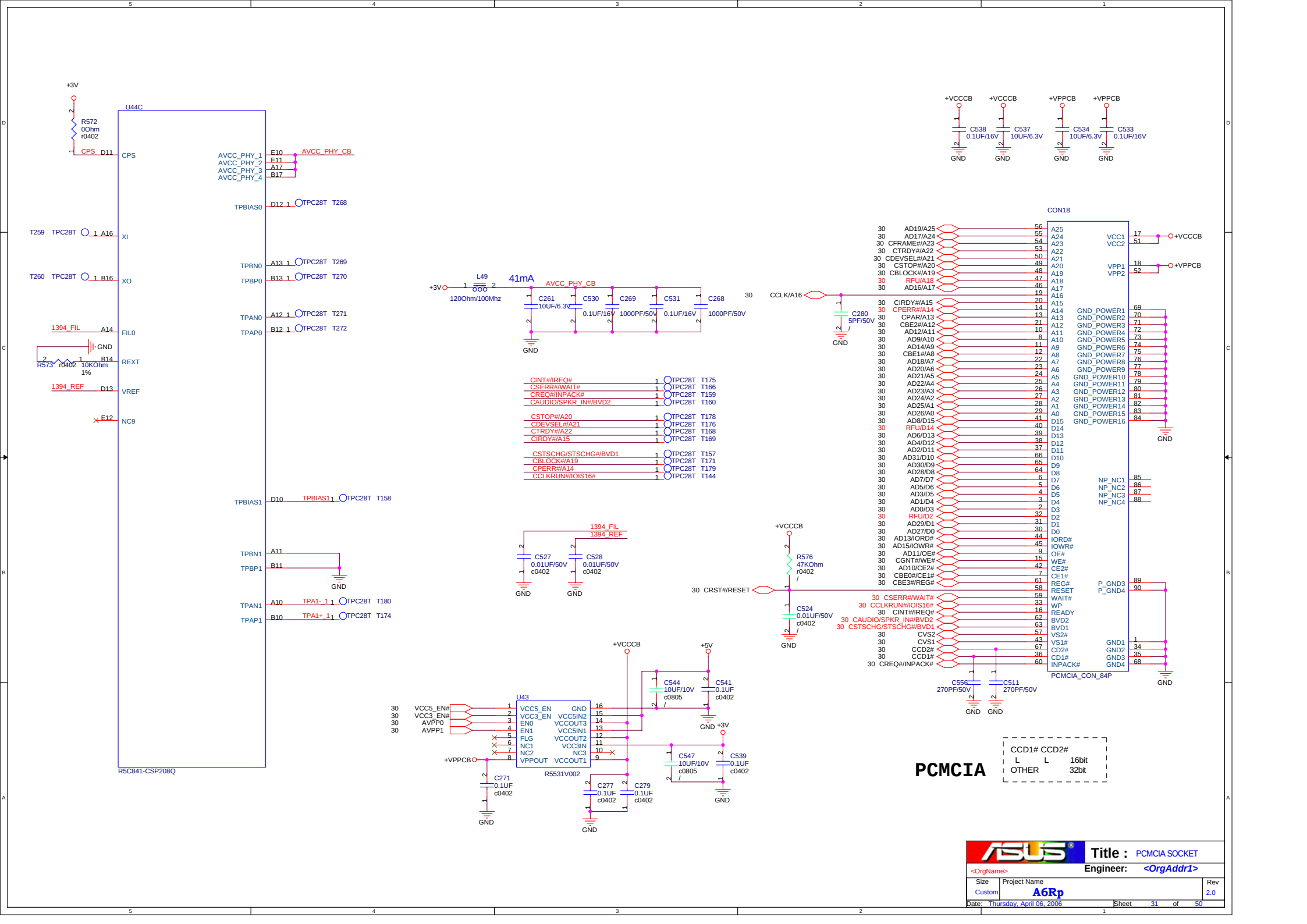
```
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect  XD Card Ready/Busy#
MDIO04--> SD/MS/XD  Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14-->       XD Data 4
MDIO15-->       XD Data 5
MDIO16-->       XD Data 6
MDIO17-->       XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
```

GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#

H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI

UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD

ASUS	Title : CARDBUS RICHO R5C841
<OrgName>	Engineer: <OrgAddr1>
Size: Custom	Project Name: A6Rp — Rev 2.0
Date: Thursday, April 06, 2006	Sheet 30 of 50


+3V
R572
0Ohm
r0402
U44C
CPS D11
CPS
XI
XO
FIL0
REXT
VREF
NC9
R5C841-CSP208Q
AVCC_PHY_1 E10
AVCC_PHY_2 E11
AVCC_PHY_3 A17
AVCC_PHY_4 B17
AVCC_PHY_CB
TPBIAS0 D12
TPBN0 A13
TPBP0 B13
TPAN0 A12
TPAP0 B12
TPBIAS1 D10
TPBN1 A11
TPBP1 B11
TPAN1 A10
TPAP1 B10
T259 TPC28T A16
T260 TPC28T B16
1394_FIL A14
GND
R573 r0402 10KOhm 1% B14
1394_REF D13
E12
TPBIAS1
TPA1- TPA1+
T268 T269 T270 T271 T272 T158 T180 T174
L49
120Ohm/100Mhz
41mA
C261 10UF/6.3V
C530 0.1UF/16V
C269 1000PF/50V
C531 0.1UF/16V
C268 1000PF/50V
CINT#/IREQ#
CSERR#/WAIT#
CREQ#/INPACK#
CAUDIO/SPKR_IN#/BVD2
CSTOP#/A20
CDEVSEL#/A21
CTRDY#/A22
CIRDY#/A15
CSTSCHG/STSCHG#/BVD1
CBLOCK#/A19
CPERR#/A14
CCLKRUN#/IOIS16#
T175 T166 T159 T160 T178 T176 T168 T169 T157 T171 T179 T144
C527 0.01UF/50V c0402
C528 0.01UF/50V c0402
U43
VCC5_EN VCC3_EN EN0 EN1 FLG NC1 NC2 VPPOUT
GND VCC5IN2 VCCOUT3 VCC5IN1 VCCOUT2 VCC3IN NC3 VCCOUT1
R5531V002
VCC5_EN# VCC3_EN# AVPP0 AVPP1
+VPPCB
C271 0.1UF c0402
C544 10UF/10V c0805
C541 0.1UF c0402
C277 0.1UF c0402
C279 0.1UF c0402
C547 10UF/10V c0805
C539 0.1UF c0402
+VCCCB
+5V
+3V
C280 5PF/50V
CCLK/A16
R576 47KOhm r0402
CRST#/RESET
C524 0.01UF/50V c0402
C538 0.1UF/16V
C537 10UF/6.3V
C534 10UF/6.3V
C533 0.1UF/16V
+VCCCB +VCCCB +VPPCB +VPPCB
CON18
AD19/A25 AD17/A24 CFRAME#/A23 CTRDY#/A22 CDEVSEL#/A21 CSTOP#/A20 CBLOCK#/A19 RFU/A18 AD16/A17
CIRDY#/A15 CPERR#/A14 CPAR/A13 CBE2#/A12 AD12/A11 AD9/A10 AD14/A9 CBE1#/A8 AD18/A7 AD20/A6 AD21/A5 AD22/A4 AD23/A3 AD24/A2 AD25/A1 AD26/A0 AD8/D15 RFU/D14 AD6/D13 AD4/D12 AD2/D11 AD31/D10 AD30/D9 AD28/D8 AD7/D7 AD5/D6 AD3/D5 AD1/D4 AD0/D3 RFU/D2 AD29/D1 AD27/D0 AD13/IORD# AD15/IOWR# AD11/OE# CGNT#/WE# AD10/CE2# CBE0#/CE1# CBE3#/REG#
CSERR#/WAIT# CCLKRUN#/IOIS16# CINT#/IREQ# CAUDIO/SPKR_IN#/BVD2 CSTSCHG/STSCHG#/BVD1 CVS2 CVS1 CCD2# CCD1# CREQ#/INPACK#
A25 A24 A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 IORD# IOWR# OE# WE# CE2# CE1# REG# RESET WAIT# WP READY BVD2 BVD1 VS2# VS1# CD2# CD1# INPACK#
VCC1 VCC2 VPP1 VPP2 GND_POWER1 GND_POWER2 GND_POWER3 GND_POWER4 GND_POWER5 GND_POWER6 GND_POWER7 GND_POWER8 GND_POWER9 GND_POWER10 GND_POWER11 GND_POWER12 GND_POWER13 GND_POWER14 GND_POWER15 GND_POWER16 NP_NC1 NP_NC2 NP_NC3 NP_NC4 P_GND3 P_GND4 GND1 GND2 GND3 GND4
PCMCIA_CON_84P
C556 270PF/50V
C511 270PF/50V
PCMCIA
CCD1# CCD2#
L L 16bit
OTHER 32bit
Title : PCMCIA SOCKET
<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name A6Rp
Rev 2.0
Date: Thursday, April 06, 2006
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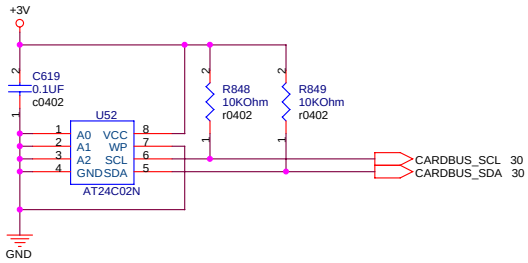

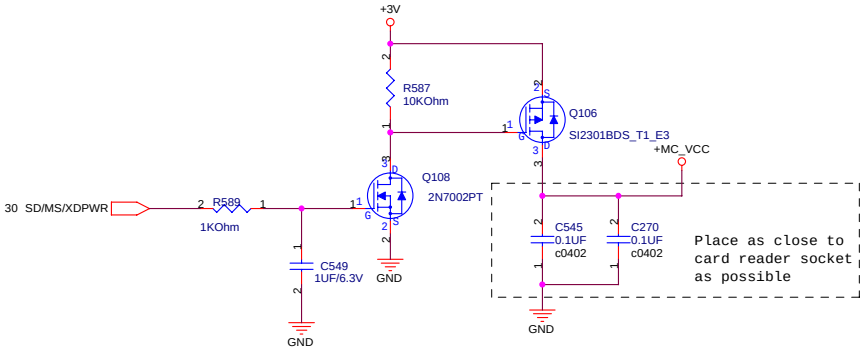

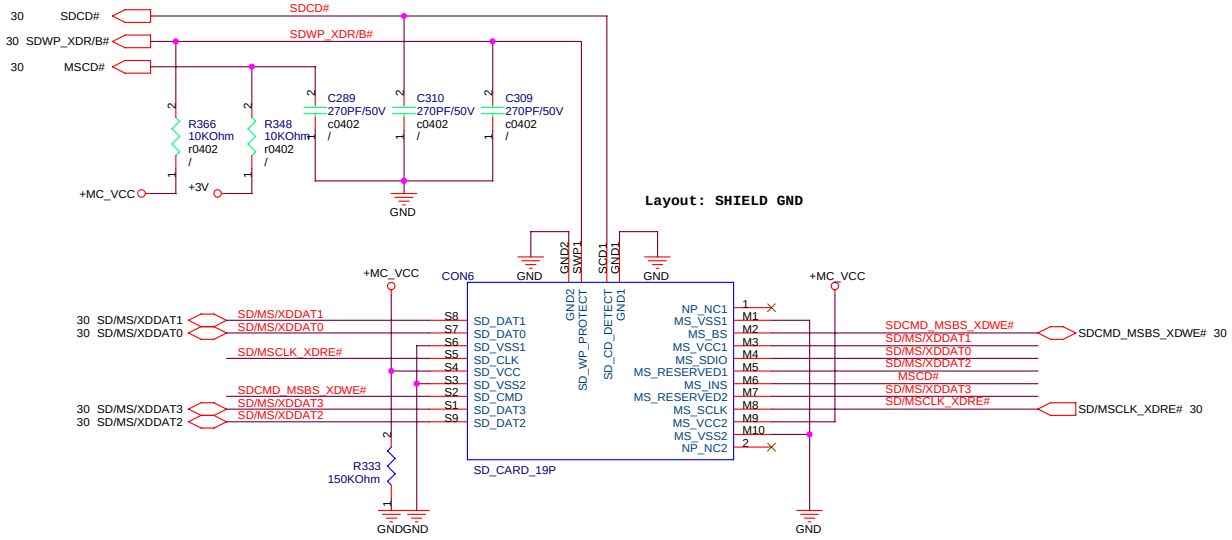

ASUS	Title : 4 IN 1 CON	
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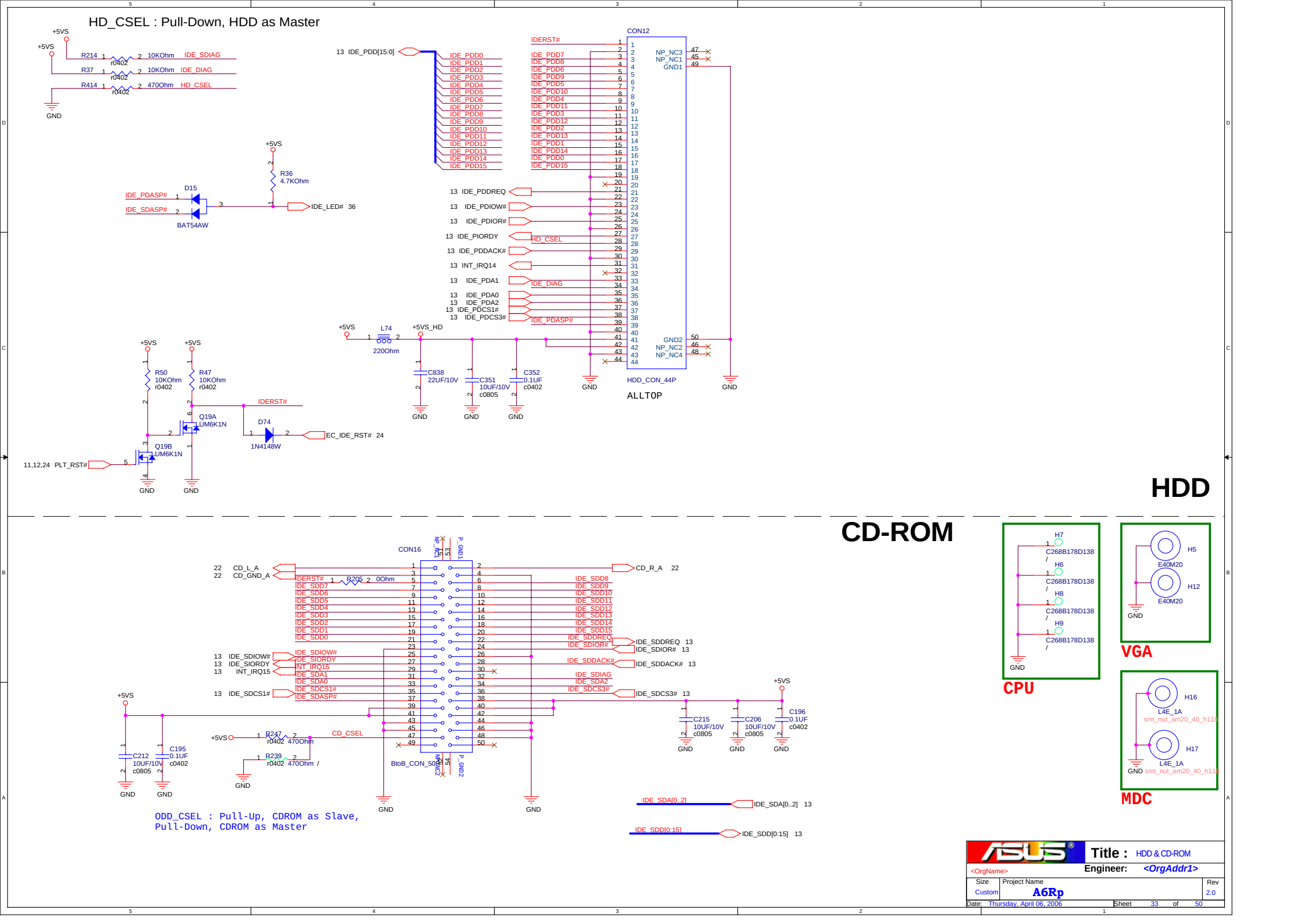
Size: Custom	Project Name: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 32 of 50	


HD_CSEL : Pull-Down, HDD as Master
+5VS
R214 r0402 10KOhm IDE_SDIAG
R37 r0402 10KOhm IDE_DIAG
R414 r0402 470Ohm HD_CSEL
GND
13 IDE_PDD[15:0]
IDE_PDD0 IDE_PDD1 IDE_PDD2 IDE_PDD3 IDE_PDD4 IDE_PDD5 IDE_PDD6 IDE_PDD7 IDE_PDD8 IDE_PDD9 IDE_PDD10 IDE_PDD11 IDE_PDD12 IDE_PDD13 IDE_PDD14 IDE_PDD15
CON12
IDERST#
NP_NC3 NP_NC1 GND1 GND2 NP_NC2 NP_NC4
HDD_CON_44P
ALLTOP
R36 4.7KOhm
D15
IDE_PDASP# IDE_SDASP#
BAT54AW
IDE_LED# 36
13 IDE_PDDREQ
13 IDE_PDIOW#
13 IDE_PDIOR#
13 IDE_PIORDY
13 IDE_PDDACK#
13 INT_IRQ14
13 IDE_PDA1
13 IDE_PDA0
13 IDE_PDA2
13 IDE_PDCS1#
13 IDE_PDCS3#
HD_CSEL
IDE_DIAG
IDE_PDASP#
+5VS_HD
L74 220Ohm
C838 22UF/10V
C351 10UF/10V c0805
C352 0.1UF c0402
R50 10KOhm r0402
R47 10KOhm r0402
Q19A UM6K1N
Q19B UM6K1N
D74 1N4148W
IDERST#
EC_IDE_RST# 24
11,12,24 PLT_RST#
HDD
CD-ROM
CON16
BtoB_CON_50P
22 CD_L_A
22 CD_GND_A
CD_R_A 22
R205 0Ohm
IDE_SDD0 IDE_SDD1 IDE_SDD2 IDE_SDD3 IDE_SDD4 IDE_SDD5 IDE_SDD6 IDE_SDD7 IDE_SDD8 IDE_SDD9 IDE_SDD10 IDE_SDD11 IDE_SDD12 IDE_SDD13 IDE_SDD14 IDE_SDD15
IDE_SDDREQ 13
IDE_SDIOR# 13
IDE_SDDACK# 13
IDE_SDIAG
IDE_SDA2
IDE_SDCS3# 13
13 IDE_SDIOW#
13 IDE_SIORDY
13 INT_IRQ15
13 IDE_SDCS1#
IDE_SDA1 IDE_SDA0 IDE_SDCS1# IDE_SDASP#
CD_CSEL
R247 470Ohm
R239 470Ohm
C212 10UF/10V c0805
C195 0.1UF c0402
C215 10UF/10V c0805
C206 10UF/10V c0805
C196 0.1UF c0402
IDE_SDA[0..2] IDE_SDA[0..2] 13
IDE_SDD[0:15] IDE_SDD[0:15] 13
ODD_CSEL : Pull-Up, CDROM as Slave,
Pull-Down, CDROM as Master
CPU
H7 H6 H8 H9
C268B178D138
VGA
H5 H12
E40M20
MDC
H16 H17
L4E_1A
smt_nut_am20_40_h118
Title : HDD & CD-ROM
Engineer: <OrgAddr1>
<OrgName>
Size Custom
Project Name A6Rp
Rev 2.0
Date: Thursday, April 06, 2006
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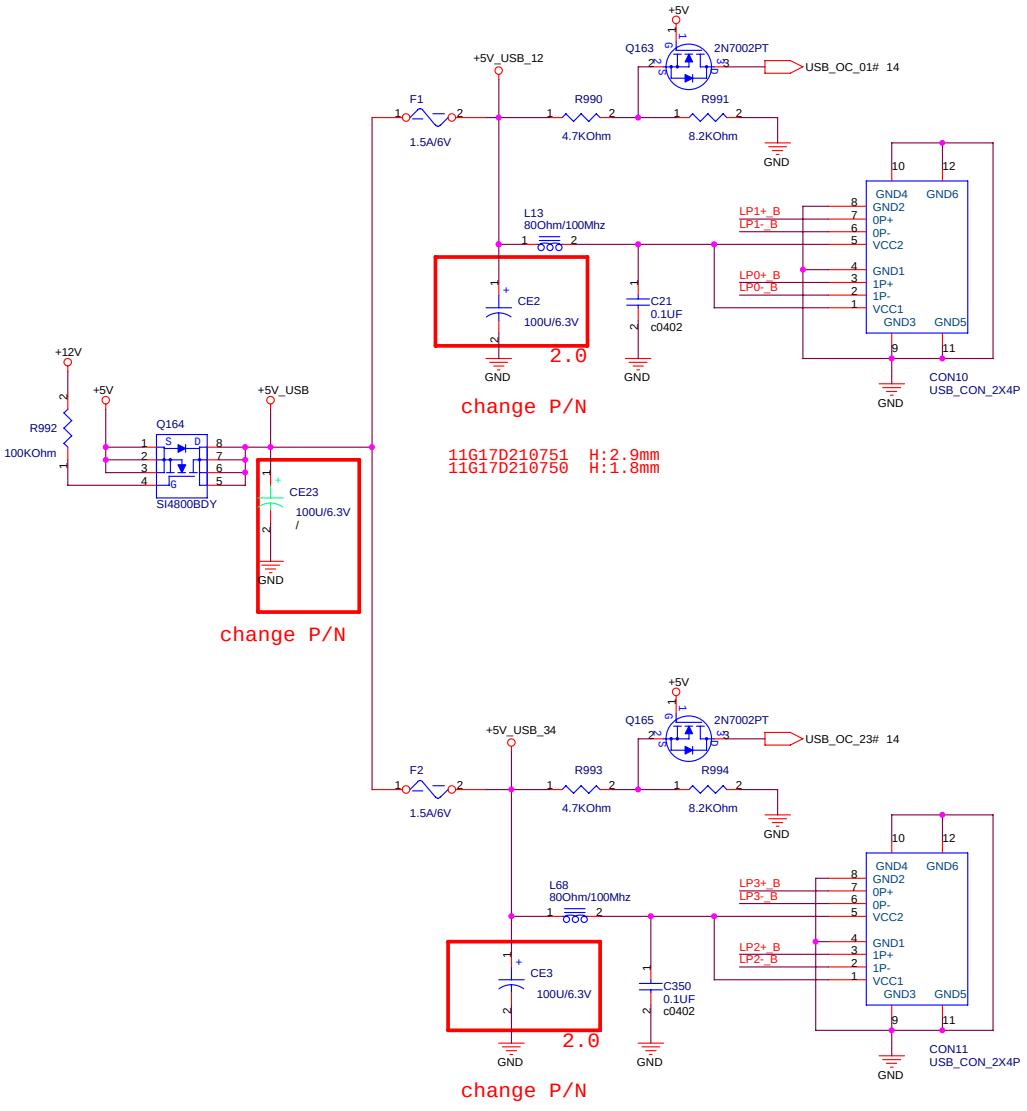
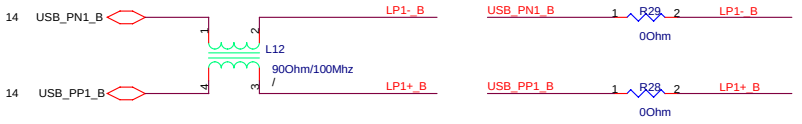
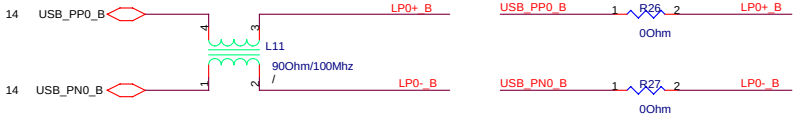
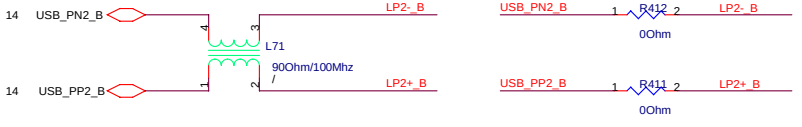
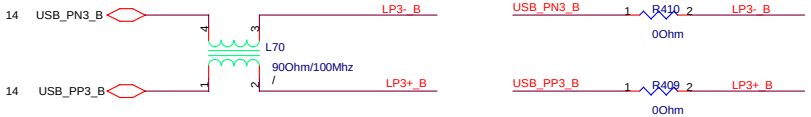
USB

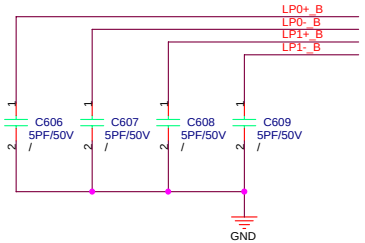


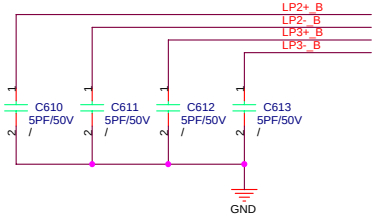












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Size: Custom	Project Name: A6Rp	Rev: 2.0
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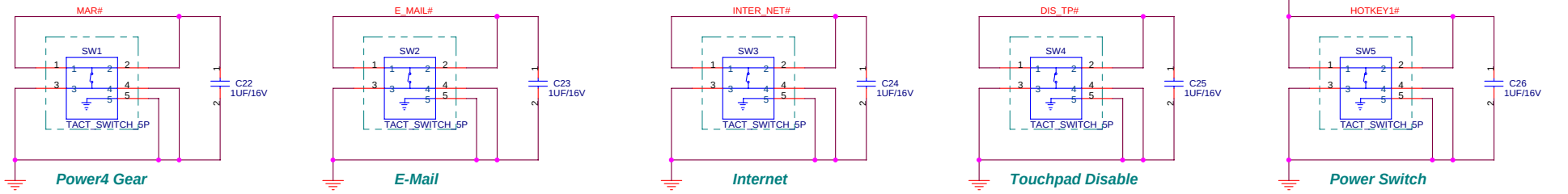
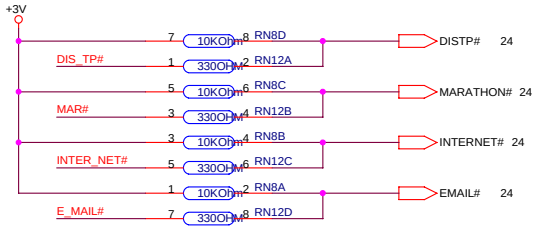
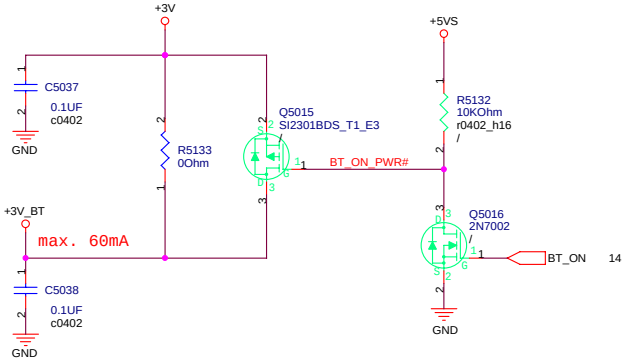
FUNCTION KEY

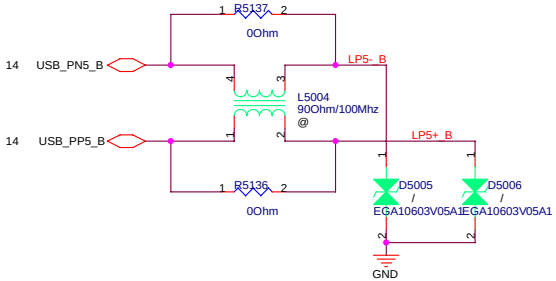




Uses 5-pin switch to improve ESD margin.

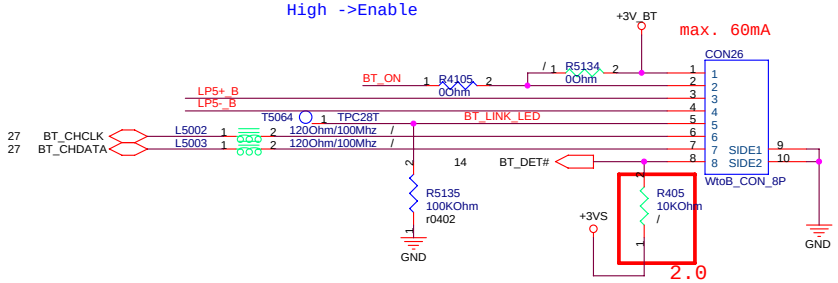
BT ON/OFF Control





Bluetooth Module

Low -> Diable
High ->Enable



ASUS	Title : FUNCTION KEY & BT	
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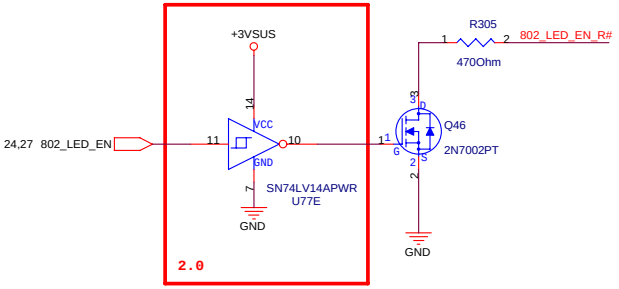
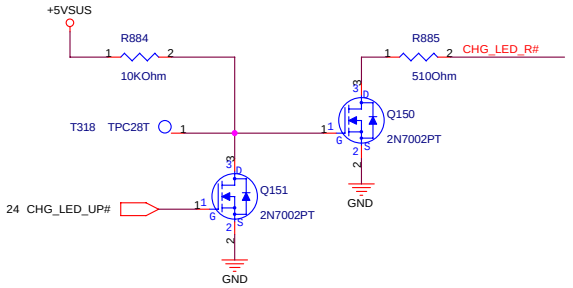
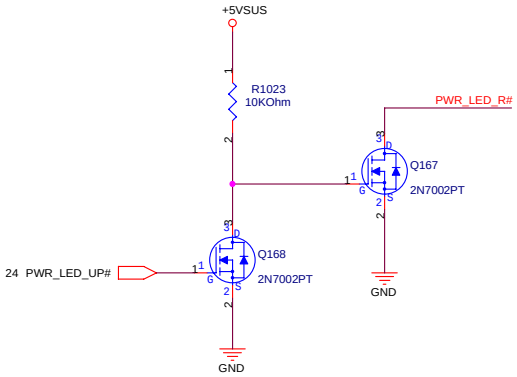
Size: Custom	Project Name: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 35 of 50	



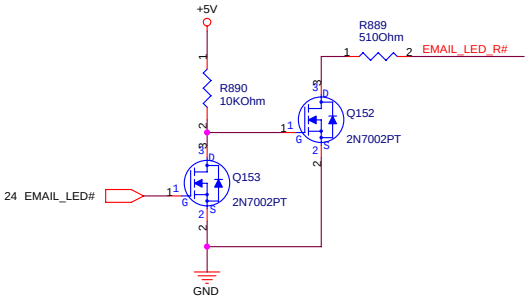
802_LED



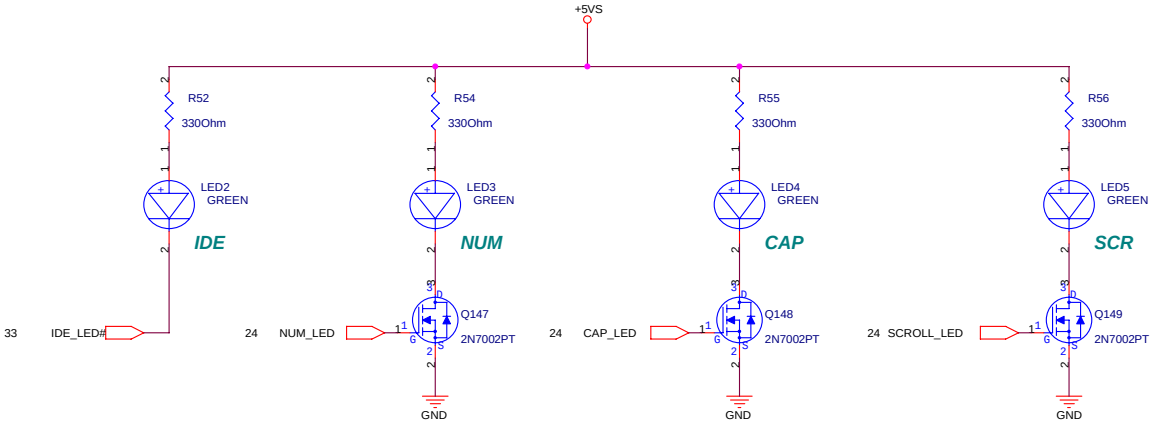
CHG_LED

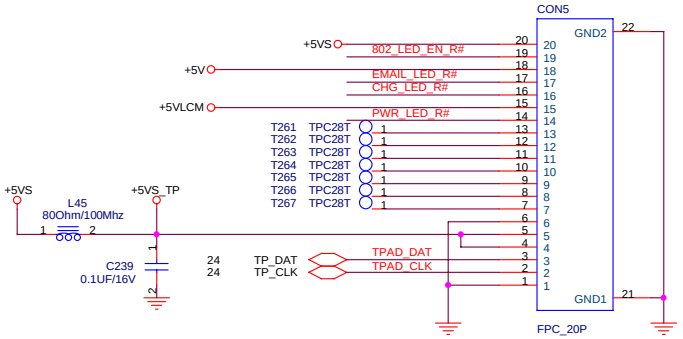


POWER_LED



EMAIL_LED





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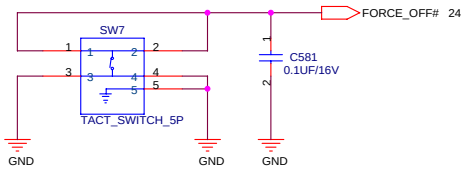
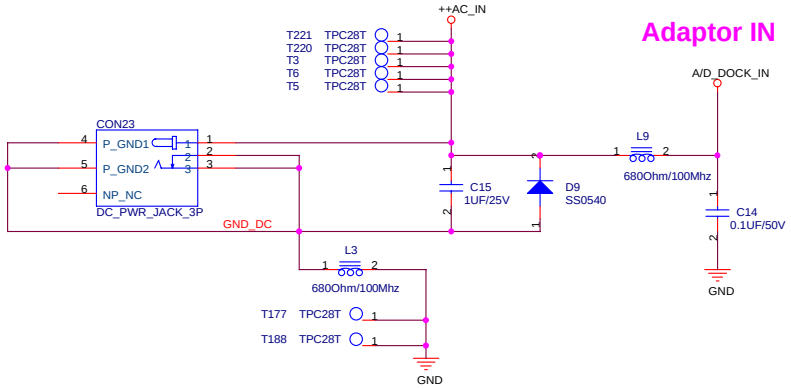
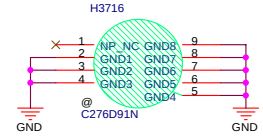
Size: Custom	Project Name: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 36 of 50	

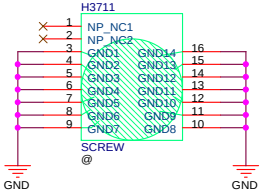


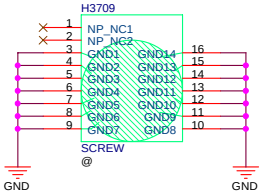
RESET SW.

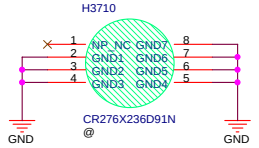


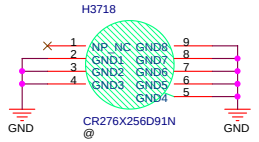
Adaptor IN

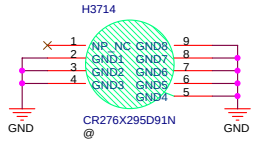


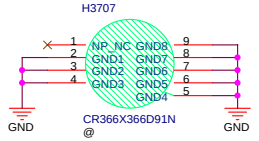


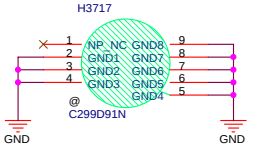


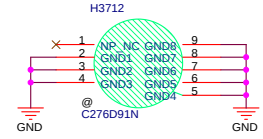


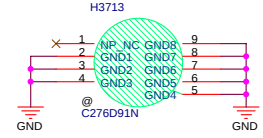


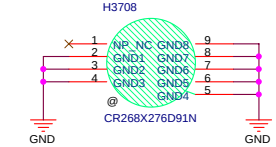












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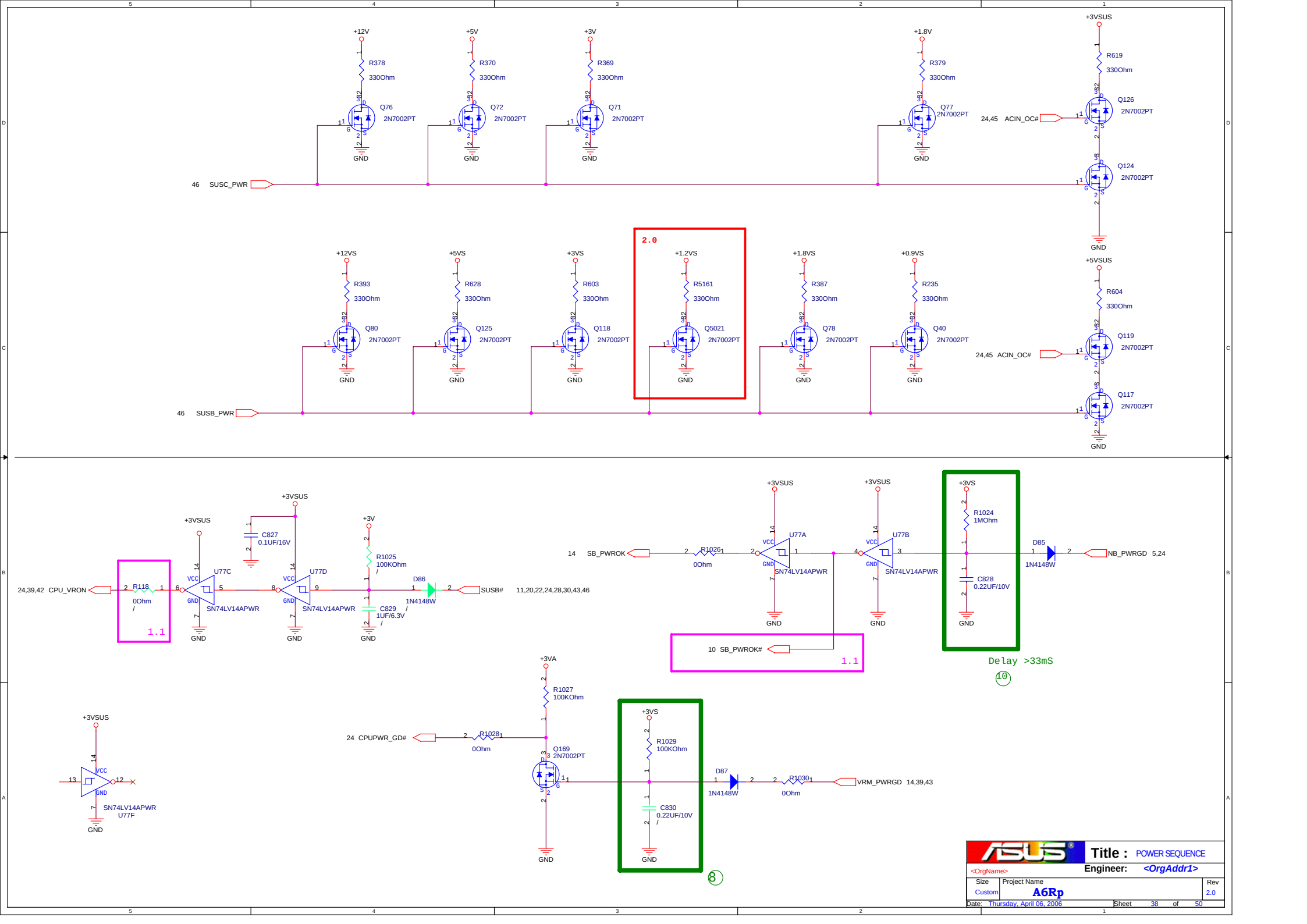
Size: Custom	Project Name: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 37 of 50	



ASUS

Title : POWER SEQUENCE

<OrgName>

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	A6Rp	2.0

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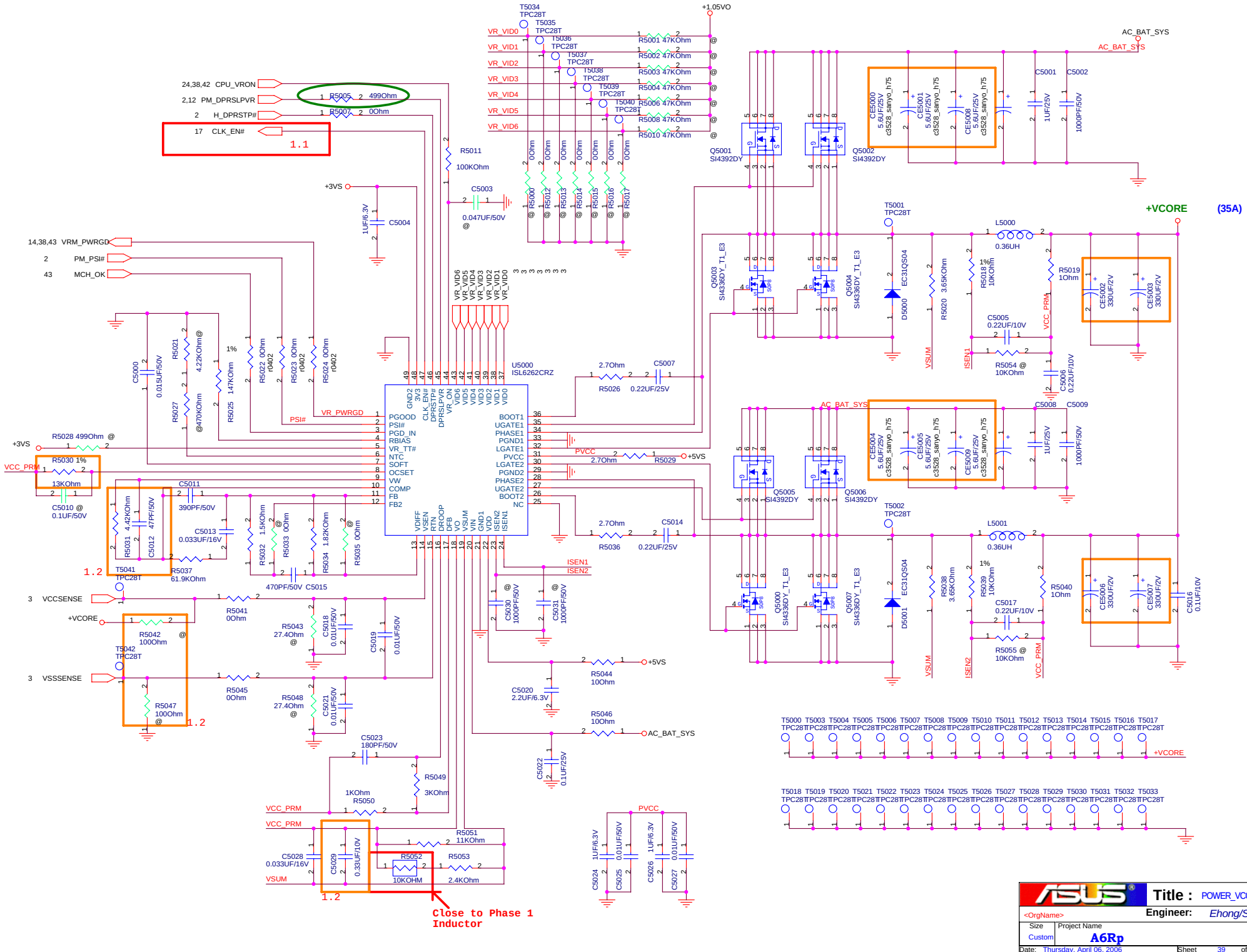
+VCORE (35A)
AC_BAT_SYS
+1.05VO
+3VS
+5VS
PVCC
U5000 ISL6262CRZ
PGOOD
PSI#
PGD_IN
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
FB2
BOOT1
UGATE1
PHASE1
PGND1
LGATE1
PVCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
NC
VR_PWRGD
CLK_EN#
DPRSTP#
DPRSLPVR
VR_ON
VID6
VID5
VID4
VID3
VID2
VID1
VID0
24,38,42 CPU_VRON
2,12 PM_DPRSLPVR
2 H_DPRSTP#
17 CLK_EN#
14,38,43 VRM_PWRGD
2 PM_PSI#
43 MCH_OK
3 VCCSENSE
3 VSSSENSE
VCC_PRM
VSUM
ISEN1
ISEN2
Q5001 SI4392DY
Q5002 SI4392DY
Q5003 SI4336DY_T1_E3
Q5004 SI4336DY_T1_E3
Q5005 SI4392DY
Q5006 SI4392DY
Q5007 SI4336DY_T1_E3
Q5000 SI4336DY_T1_E3
D5000 EC31QS04
D5001 EC31QS04
L5000 0.36UH
L5001 0.36UH
T5001 TPC28T
T5002 TPC28T
T5034 TPC28T
T5035 TPC28T
T5036 TPC28T
T5037 TPC28T
T5038 TPC28T
T5039 TPC28T
T5040 TPC28T
T5041 TPC28T
T5042 TPC28T
T5000 T5003 T5004 T5005 T5006 T5007 T5008 T5009 T5010 T5011 T5012 T5013 T5014 T5015 T5016 T5017 TPC28T
T5018 T5019 T5020 T5021 T5022 T5023 T5024 T5025 T5026 T5027 T5028 T5029 T5030 T5031 T5032 T5033 TPC28T
Close to Phase 1 Inductor
1.1
1.2
1.2
Title : POWER_VCORE
Engineer: Ehong/Stan
<OrgName>
Size Custom
Project Name A6Rp
Rev 2.0
Date: Thursday, April 06, 2006
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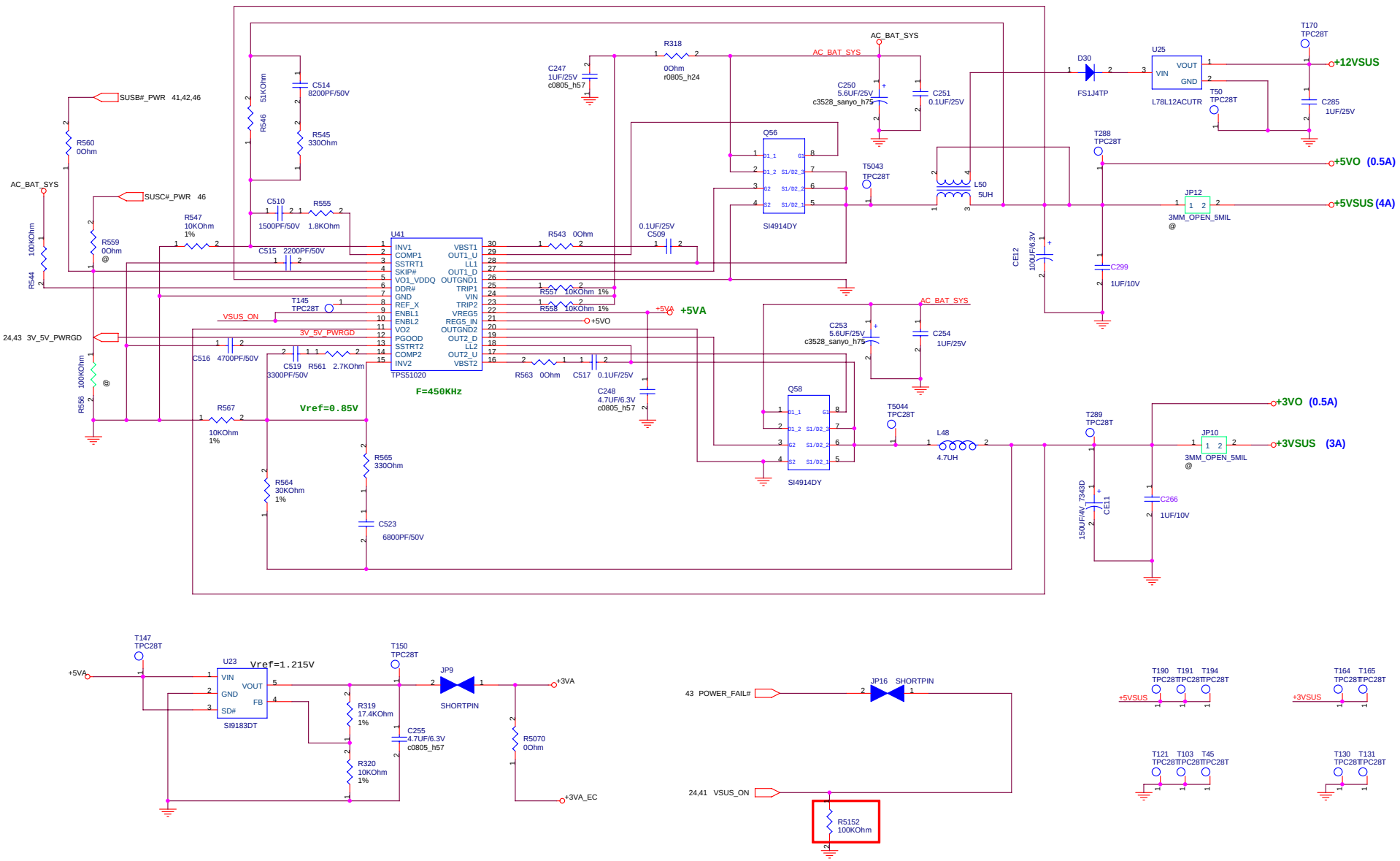
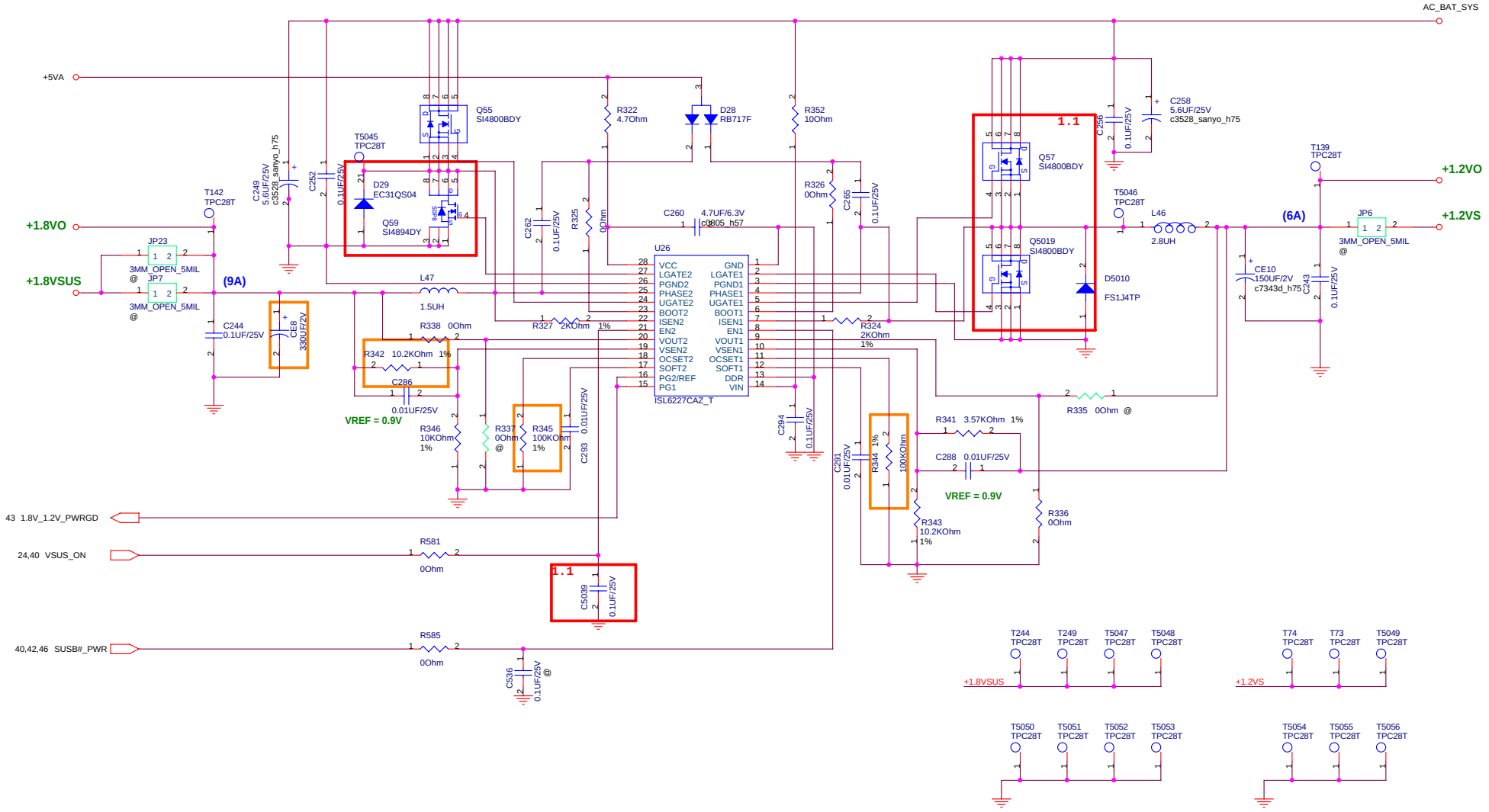
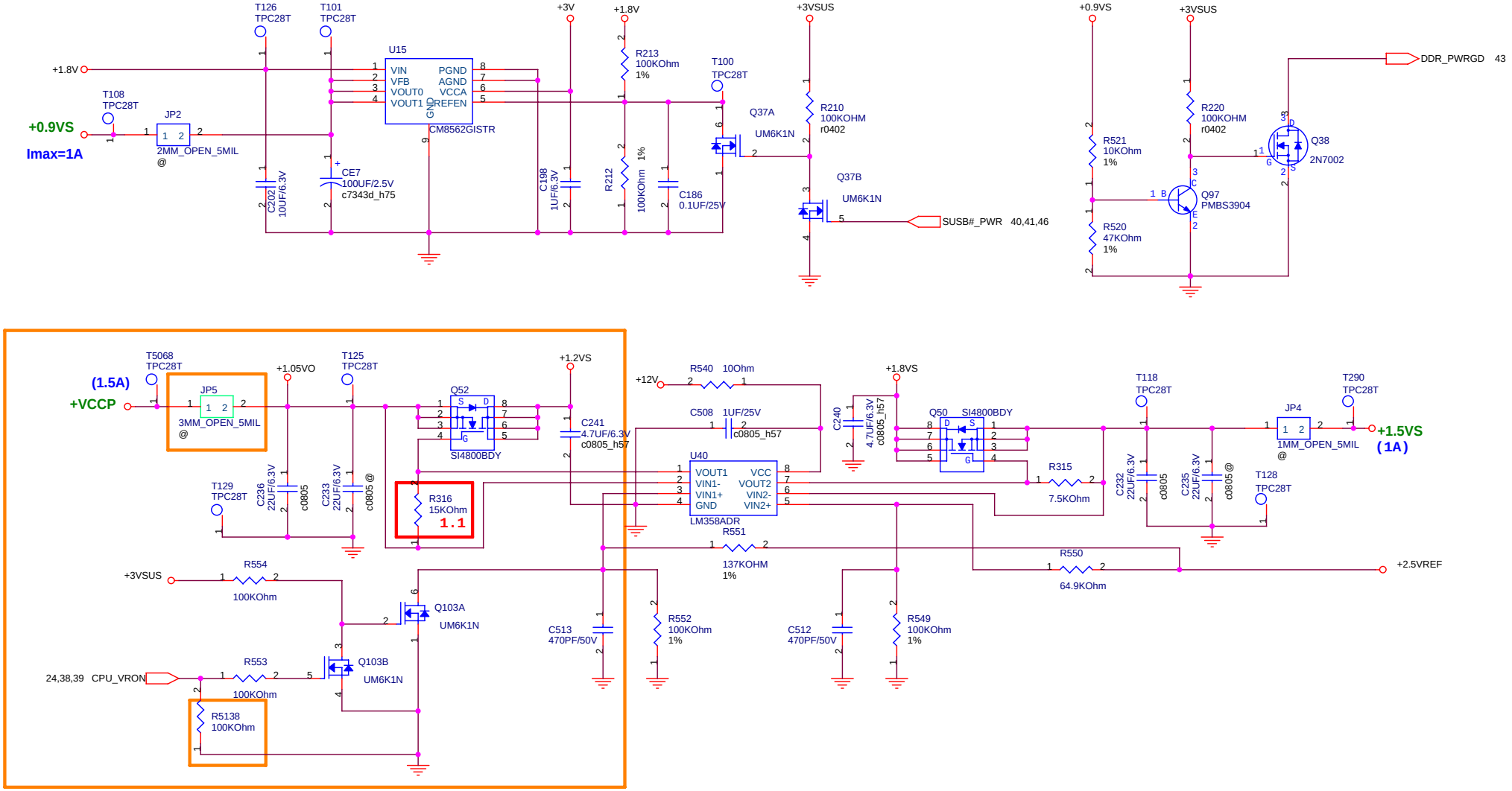

SUSB#_PWR 41,42,46
SUSC#_PWR 46
AC_BAT_SYS
24,43 3V_5V_PWRGD
VSUS_ON
U41
TPS51020
F=450KHz
Vref=0.85V
+5VA
+5VO
+12VSUS
+5VO (0.5A)
+5VSUS (4A)
+3VO (0.5A)
+3VSUS (3A)
SI4914DY
FS1J4TP
L78L12ACUTR
U23
Vref=1.215V
SI9183DT
SHORTPIN
43 POWER_FAIL#
24,41 VSUS_ON
R5152
100KOhm
Title : SYSTEM_+5VA & +3VA
Engineer: <OrgAddr1>
A6Rp
Thursday, April 06, 2006



<OrgName>	Title : 1.8V&1.2VS	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 41 of 50	



ASUS

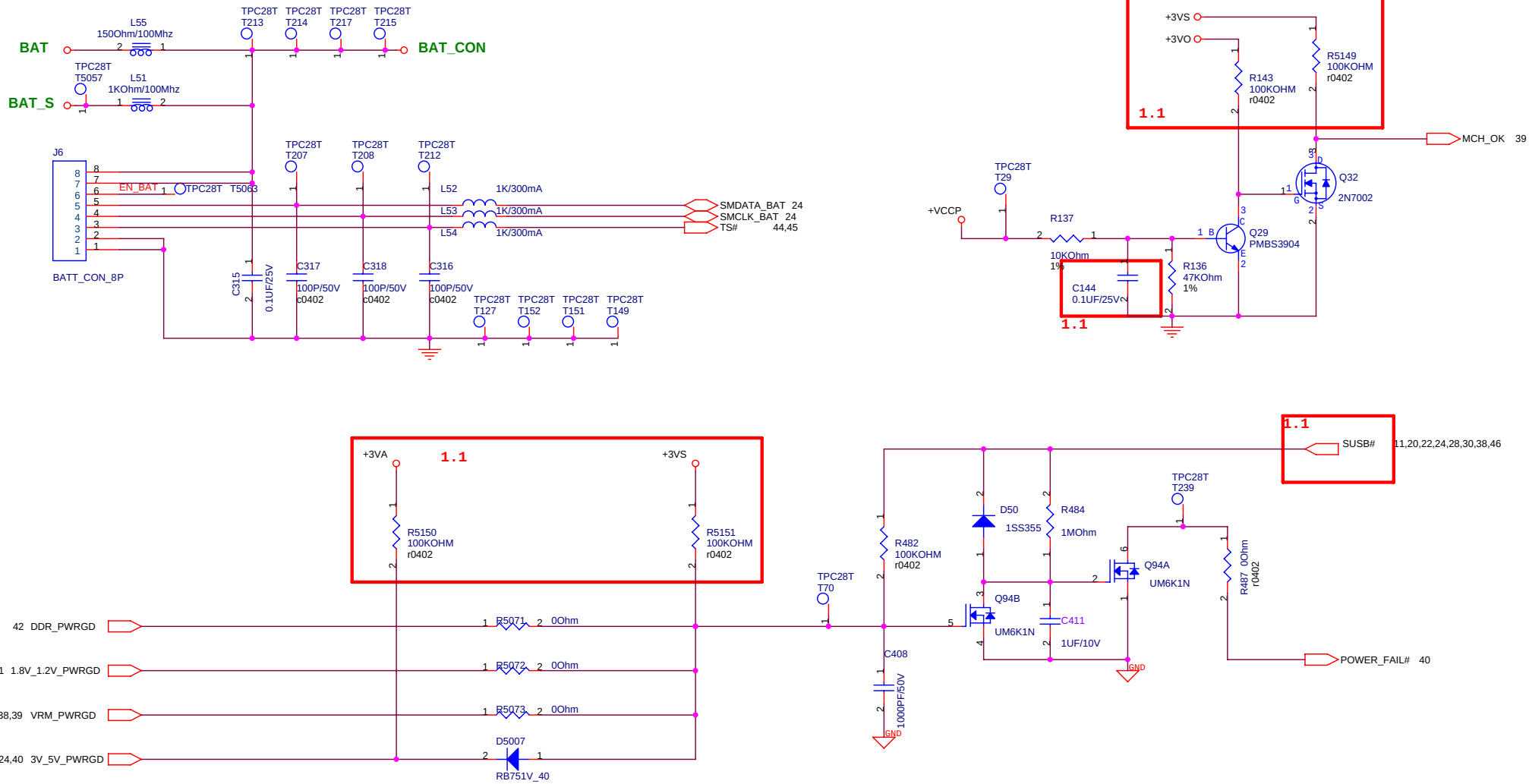
Title : 1.05VA & +0.9VS

<OrgName>

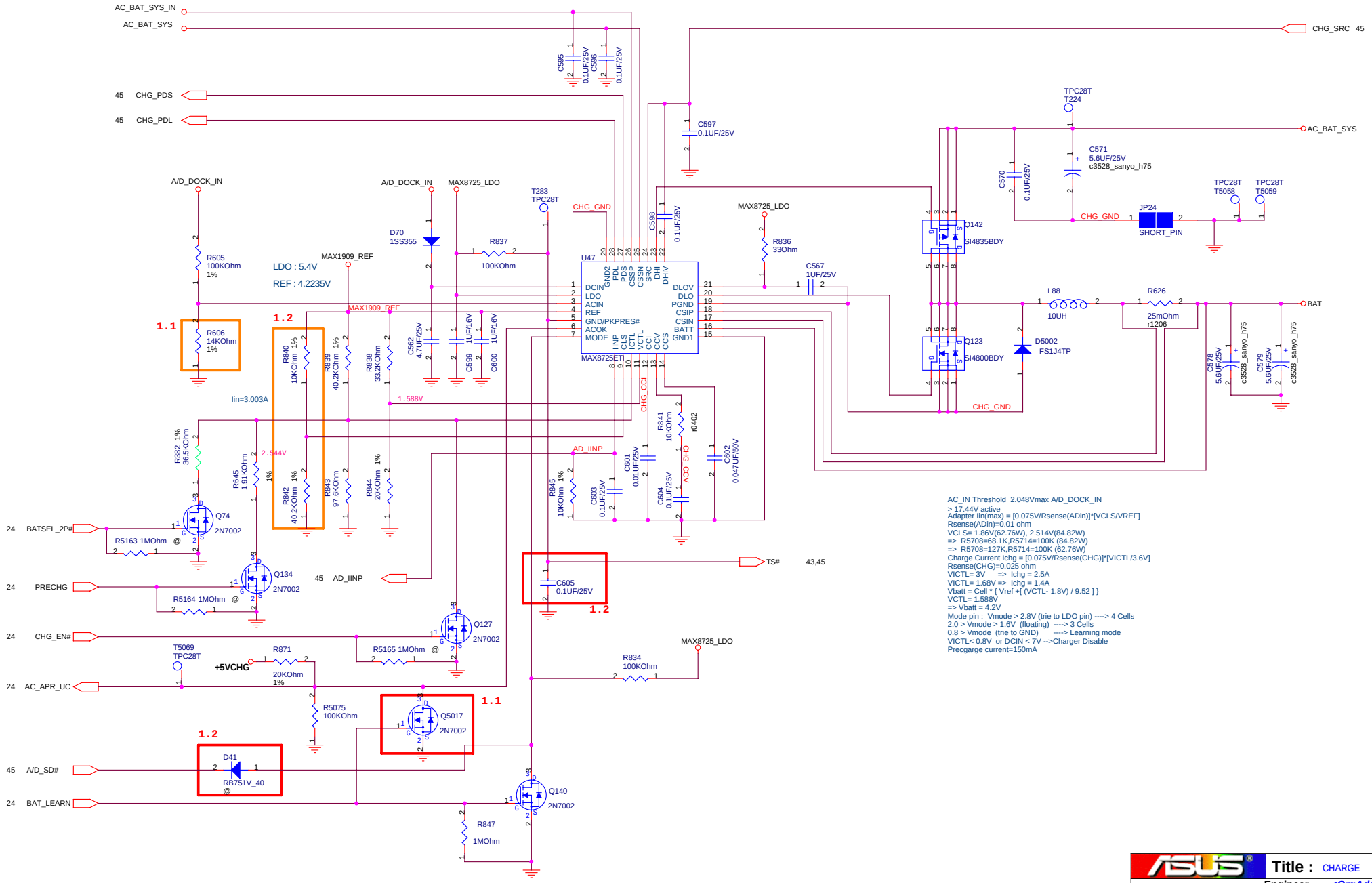
Engineer: <OrgAddr1>

Size	Project Name	Rev
B	A6R	2.0

Date: Thursday, April 06, 2006 Sheet 42 of 50



ASUS	Title : PIC/BAT CON/PWOK	
<OrgName>	Engineer: <OrgAddr1>	
Size: B	Project Name: A6R	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 43 of 50	


AC_BAT_SYS_IN
AC_BAT_SYS
CHG_SRC 45
45 CHG_PDS
45 CHG_PDL
C595 0.1UF/25V
C596 0.1UF/25V
C597 0.1UF/25V
TPC28T T224
AC_BAT_SYS
C571 5.6UF/25V c3528_sanyo_h75
C570 0.1UF/25V
TPC28T T5058
TPC28T T5059
JP24 SHORT_PIN
CHG_GND
A/D_DOCK_IN
MAX8725_LDO
T283 TPC28T
D70 1SS355
R837 100KOhm
R836 33Ohm
C567 1UF/25V
Q142 SI4835BDY
Q123 SI4800BDY
L88 10UH
R626 25mOhm r1206
D5002 FS1J4TP
BAT
C578 5.6UF/25V c3528_sanyo_h75
C579 5.6UF/25V c3528_sanyo_h75
R605 100KOhm 1%
R606 14KOhm 1%
MAX1909_REF
LDO : 5.4V
REF : 4.2235V
1.1
1.2
R840 10KOhm 1%
R839 40.2KOhm 1%
R838 33.2KOhm
C562 4.7UF/25V
C599 1UF/16V
C600 1UF/16V
U47
MAX8725ETI
DCIN
LDO
ACIN
REF
GND/PKPRES#
ACOK
MODE
DLOV
DLO
PGND
CSIP
CSIN
BATT
GND1
C598 0.1UF/25V
lin=3.003A
1.588V
2.544V
R382 1% 36.5KOhm
R645 1.91KOhm 1%
R842 40.2KOhm 1%
R843 97.6KOhm
R844 20KOhm 1%
R841 10KOhm
C602 0.047UF/50V
AD_IINP
R845 10KOhm 1%
C603 0.1UF/25V
C601 0.01UF/25V
C604 0.1UF/25V
24 BATSEL_2P#
Q74 2N7002
R5163 1MOhm @
24 PRECHG
Q134 2N7002
R5164 1MOhm @
45 AD_IINP
C605 0.1UF/25V
TS# 43,45
24 CHG_EN#
Q127 2N7002
R5165 1MOhm @
T5069 TPC28T
+5VCHG
R871 20KOhm 1%
24 AC_APR_UC
R5075 100KOhm
Q5017 2N7002
R834 100KOhm
MAX8725_LDO
45 A/D_SD#
D41 RB751V_40 @
24 BAT_LEARN
Q140 2N7002
R847 1MOhm
AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.01 ohm
VCLS= 1.86V(62.76W), 2.514V(84.82W)
=> R5708=68.1K,R5714=100K (84.82W)
=> R5708=127K,R5714=100K (62.76W)
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A
Vbatt = Cell * [Vref +[(VCTL- 1.8V) / 9.52]]
VCTL= 1.588V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable
Precgarge current=150mA
Title : CHARGE
<OrgName>
Engineer: <OrgAddr1>
Size Custom
Project Name A6R
Rev 2.0
Date: Thursday, April 06, 2006
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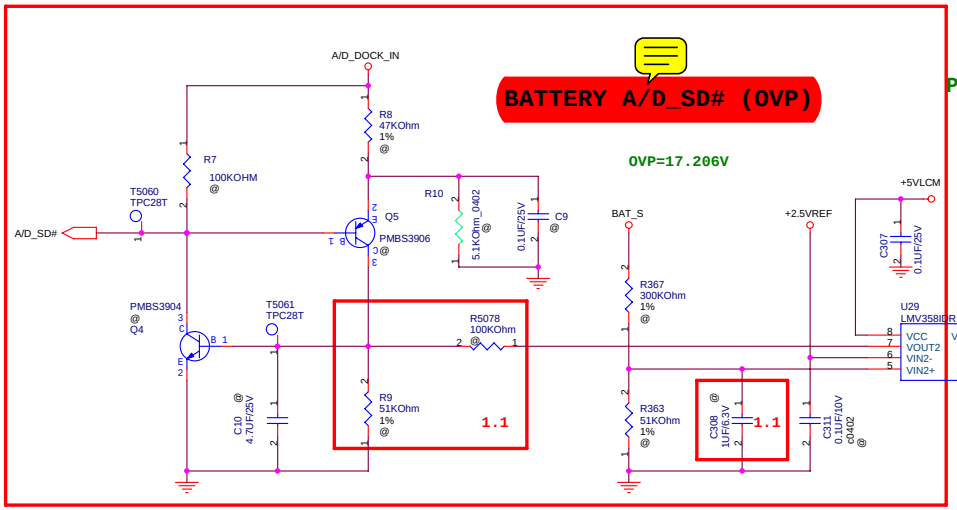
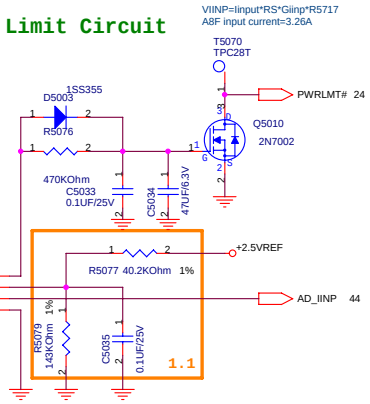
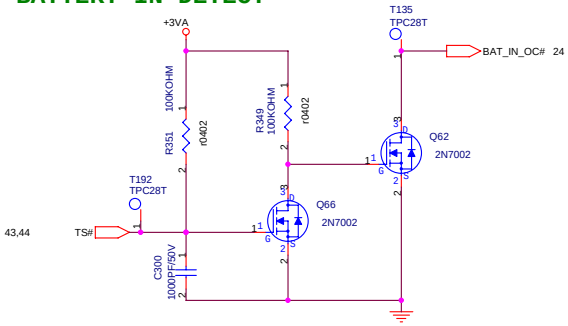
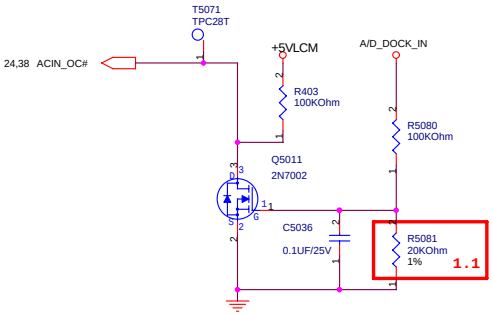


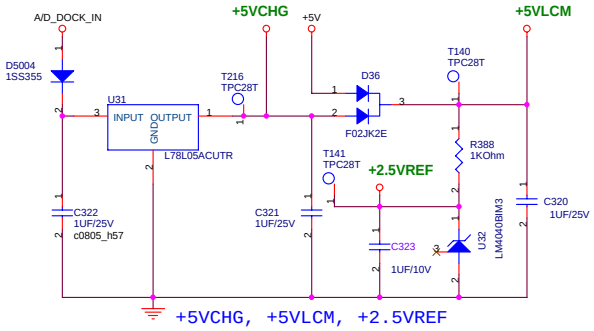
Power Limit Circuit



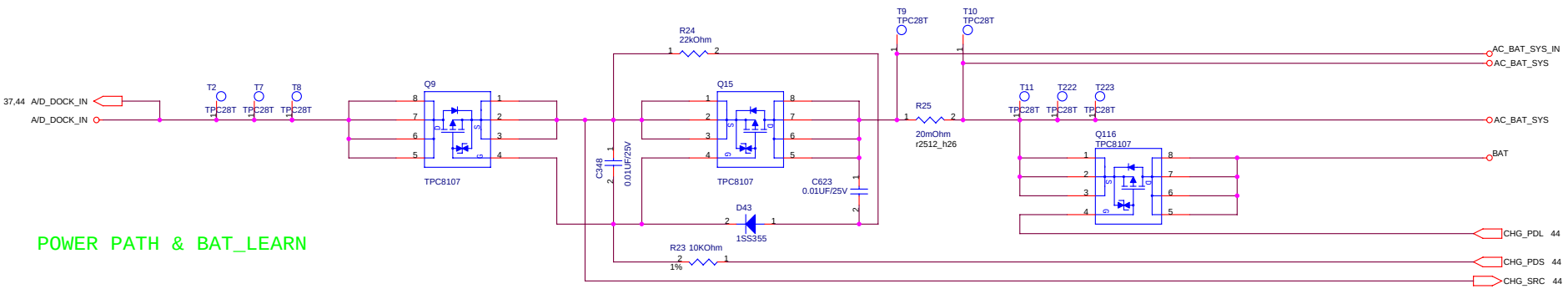
BATTERY IN DETECT





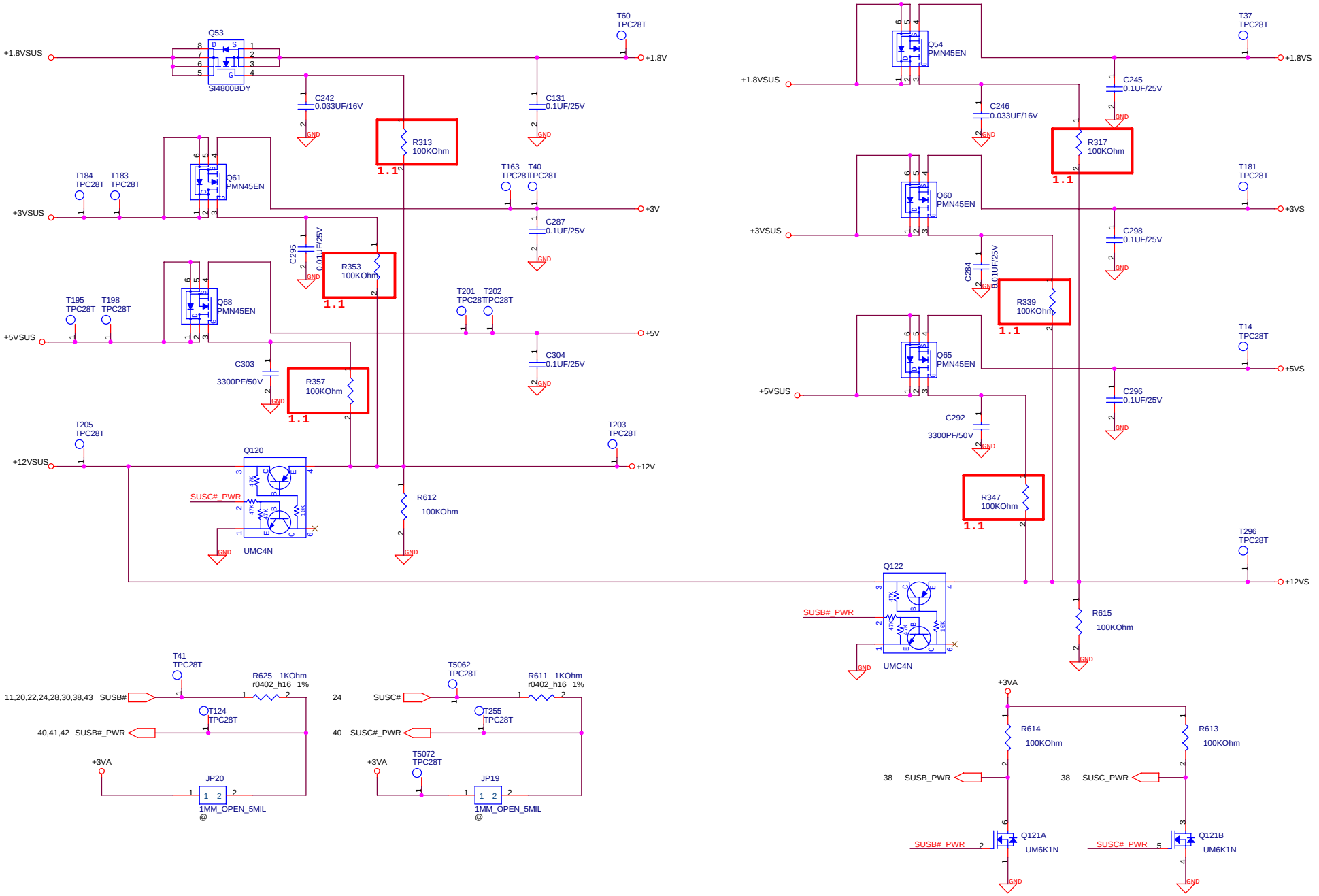


+5VCHG, +5VLCM, +2.5VREF

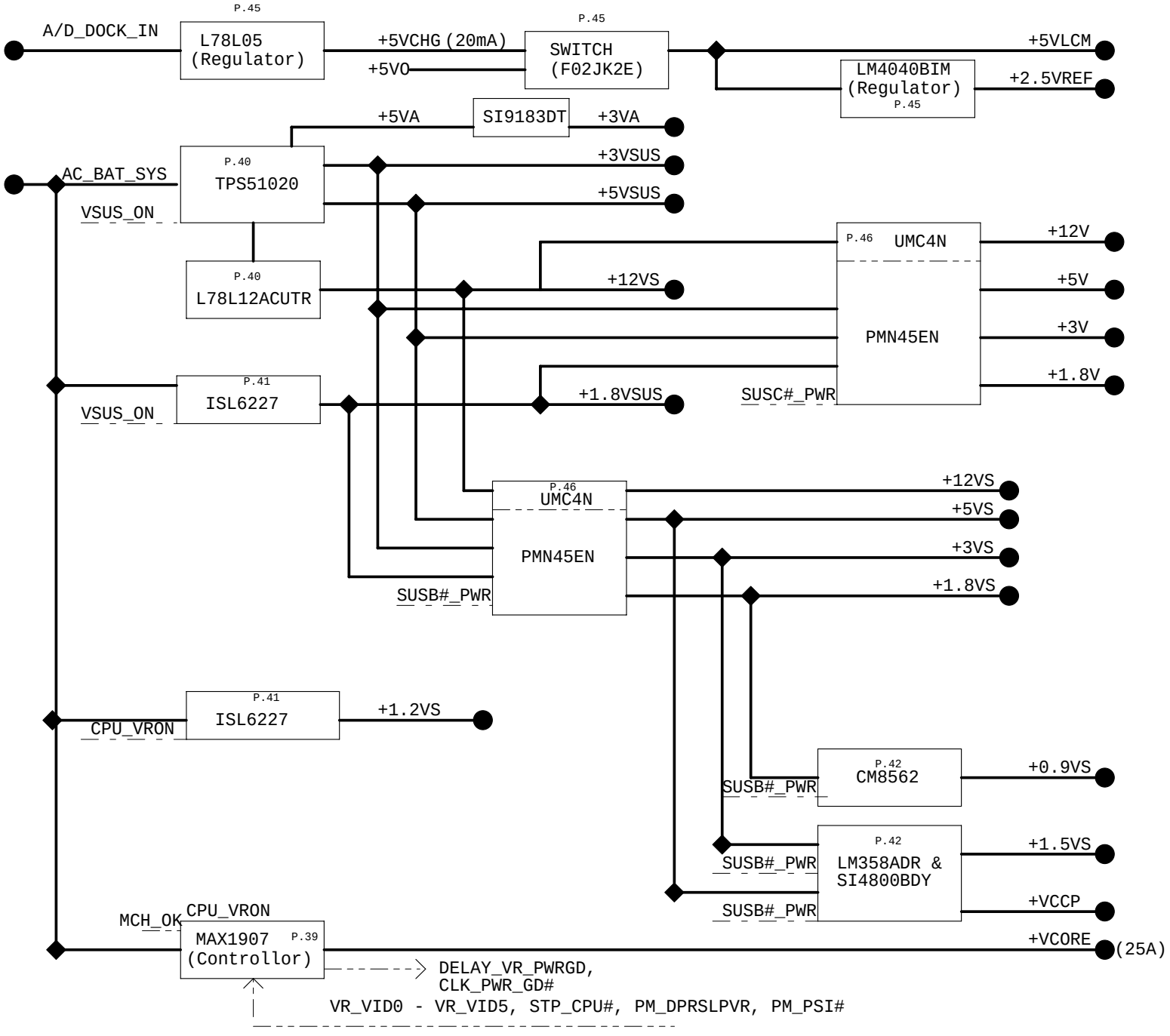


POWER PATH & BAT_LEARN

ASUS	Title : BATLOW/SD#		
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: A6R		Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 45 of 50		



<OrgName>	Title : LOAD SWITCH	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6R	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 46 of 50	



Title : POWER BLOCK DIAGRAM		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 47 of 50	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 LAN	AD16	0	E
CARD READER	AD17	1	C
CARDBUS	AD17	1	A
1394	AD17	1	B
MINIPCI (802.11a/b/g)	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)
PIC	1001001x (92)

SB400 GPIO TABLE

GPIO	TYPE	POWER DOMAIN	FUNCTION
GPIO 0	I/OD	S0	
GPIO 1	I/O	S0	
GPIO 2	I/O	S0	SB_SPKR
GPIO 3	I/O	S0	FWH_WP#
GPIO 4	I/O	S0	PCB_ID0
GPIO 5	I/O	S0	PCB_ID1
GPIO 6	I/OD	S0	PCB_ID2
GPIO 7	I/O	S0	VRM_PWRGD
GPIO 8	I/O	S0	CB_SD#
GPIO 9	I/O	S0	BACK_OFF#
GPIO 10	I/O	S5	SB_PM_THERM#
GPIO 11	I/O	S0	802_LED_EN
GPIO 12	I/O	S0	WLAN_ON#
GPIO 13	I/O	S0	
GPIO 14	I/O	S0	PCI_GNT#5
GPIO 31	I/O	S0	
GPIO 32	I/O	S0	PCI_GNT#6
GPIO 33	I/O	S0	PCI_INTE#
GPIO 34	I/O	S0	PCI_INTF#
GPIO 35	I/O	S0	PCI_INTG#
GPIO 36	I/O	S0	PCI_INTH#
GPM 0	I	S5	
GPM 1	I	S5	
GPM 2	I/O	S5	
GPM 3	I	S5	
GPM 4	I	S5	
GPM 5	I	S5	
GPM 6	I/OD	S5	PWRLED_1HZ
GPM 7	I	S5	SYS_RESET#
GEVENT 0	I	S5	
GEVENT 1	I	S0	
GEVENT 2	I	S5	THRMTRIP#
GEVENT 3	I	S5	LPC_PME#
GEVENT 4	I	S5	PCI_PME#
GEVENT 5	I	S5	H_PROCHOT#
GEVENT 6	I	S5	
GEVENT 7	I	S5	
GEVENT 8			KB_SCI
EXTEVENT#0			EXT_SMI#
EXTEVENT#1			SIO_SMI#

KBC GPIO	W1V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	LID_EC#	
P20(Pin 38)	KBCRSM	
P42(Pin 23)		
P43(Pin 22)	OP_SD#	
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI#	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID0	
P52(Pin 15)	KID1	
P53(Pin 14)	CLR_DJ#	
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)		
P57(Pin 10)	INV_DA	
P67(Pin 74)	DJ_LED#	
P66(Pin 75)	SWDJ_EN#	
P65(Pin 76)	GAIN_AMP_K#	0->-6 V/V 1->NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)	SCROLL_LED#	
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

ASUS

Title : SYSTEM RESOURCE

<OrgName>

Engineer: <OrgAddr1>

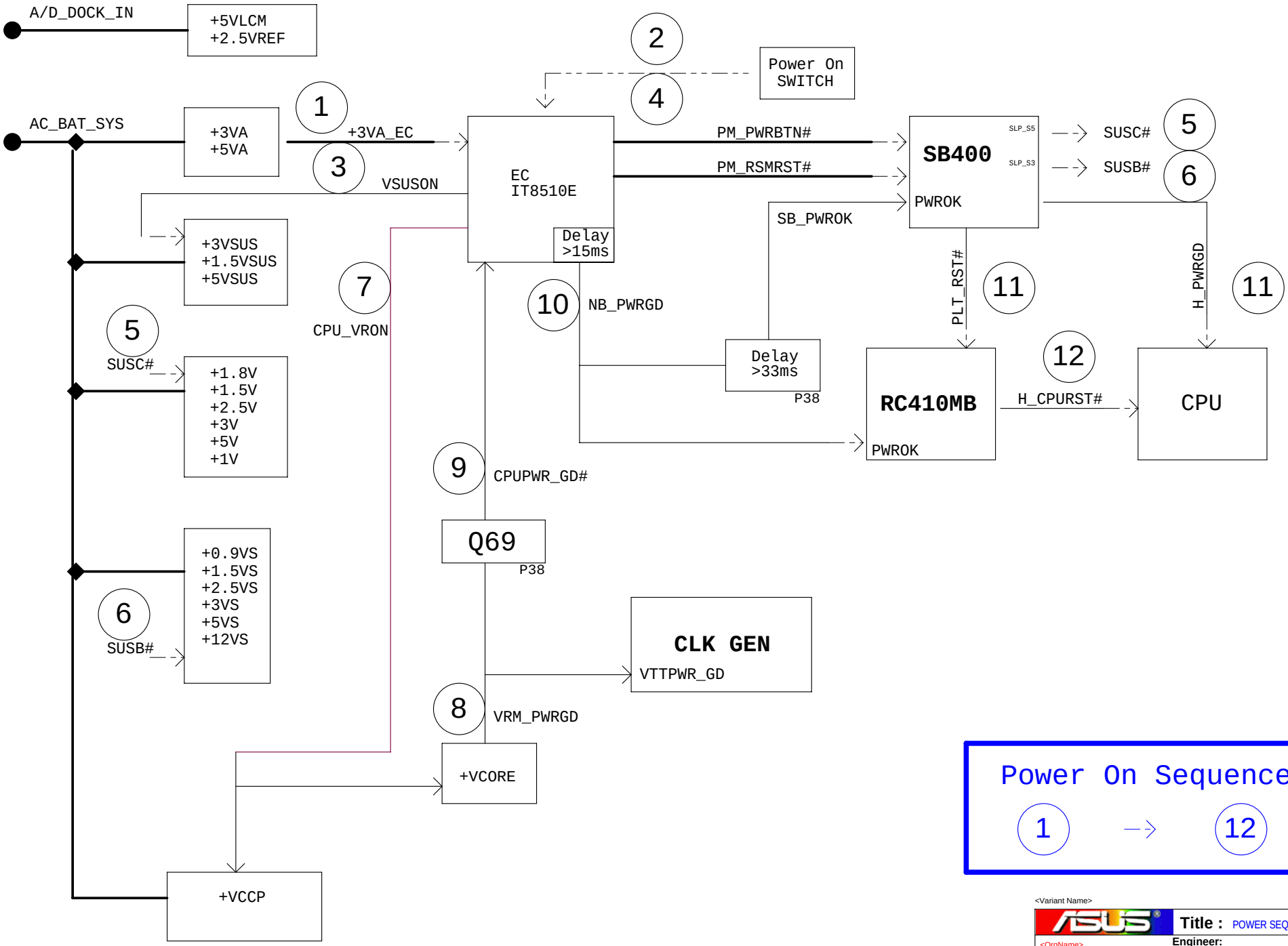
Size	Project Name	Rev
Custom	A6Rp	2.0

Date: Thursday, April 06, 2006 Sheet 48 of 50

Rev	Date	Description
1.0	05/03/01	1. Initial release.

Rev	Date	Description

ASUS	Title : HISTORY	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A6Rp	Rev: 2.0
Date: Thursday, April 06, 2006	Sheet 49 of 50	



<Variant Name>

Title : POWER SEQUENCY

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	A6Rp	2.0

Date: Thursday, April 06, 2006 Sheet 50 of 50