Columbia/Tangiz Block Diagram

Project code: 91.4T301.001
PCB P/N : 48.4T301.0SA
REVISION : 06236-SA

CLK GEN.
ICS 9LPRS502
(RTM875T-605) 3
71.09502.00W

Mobile CPU
Merom 479
2G/2.33G
2.0G : 71.MEROM.A0U
2.33G : 71.MEROM.B0U
4, 5

G792
20

HOST BUS 667/800MHz@1.05V

DDR2
533/667 MHz
12,13

DDR2
533/667 MHz
12,13

533/667MHz

533/667MHz

Crestline
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
71.CREST.00U
6,7,8,9,10,11

X4 DMI
400MHz

C-Link0

TV Out 14
CRT 15
LCD 14
DVI 44
VGA Borad 28

PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

Line In
MIC In
14
31
INT.SPKR
Line Out
(No-SPDIF)

Codec
ALC268
30

AZALIA

OP AMP
G1431Q 31

OP AMP
G1412 31

MODEM
MDC Card
22

RJ11

ICH8M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 1.1
3 SATA
1 PATA 66/100
10 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
71.0ICH8.A0U
16,17,18,19

PCI BUS

TI
PCI7412
Cardbus
Cardreader
25/26

PCMCIA I/F

PWR SW
CP2211F 26

PCMCIA
SLOT
Support
TypeII 27

1394
CONN 27

MS/MS Pro/xD/
MMC/SD
5 in 1 27

LAN
GIGA
BCM5787M 23

TXFM 24

RJ45 24

PCIex1

Mini Card
Kedron a/b/g/n 29

LPC BUS

New card 29

PCI Express

SATA

PATA

USB

P2231NFC1 29

HDD 21

CDROM 21

MINI USB
BlueTooth 22

Finger print 34

USB
4 Port 22

CAMERA 13

KBC
Winbond
WPC8768L 32

SPI I/F

BIOS
W25X80-VSS 34

LPC
DEBUG
CONN. 35

Touch
Pad 33

INT.
KB 33

FIR 32

SYSTEM DC/DC
MAX8744 38

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A)

SYSTEM DC/DC
Max8717 39

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9.5A) 1D8V_S3(8.5A)

TPS51100 41

1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3

APL5915 41

1D8V_S3	1D25V_S0 (2A)

APL531230

3D3V_S0	2D5V_S0 (300mA)

APW5912 40

3D3V_S5	1D5V_S3 (7.5A)

ISL CHARGER
ISL6255 41

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC
MAX8770 35,36

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

<Core Design>

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Title: BLOCK DIAGRAM

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ICH8M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Crestline Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode **1 = Low Power mode** (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

History

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1

UMA

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Title: Reference

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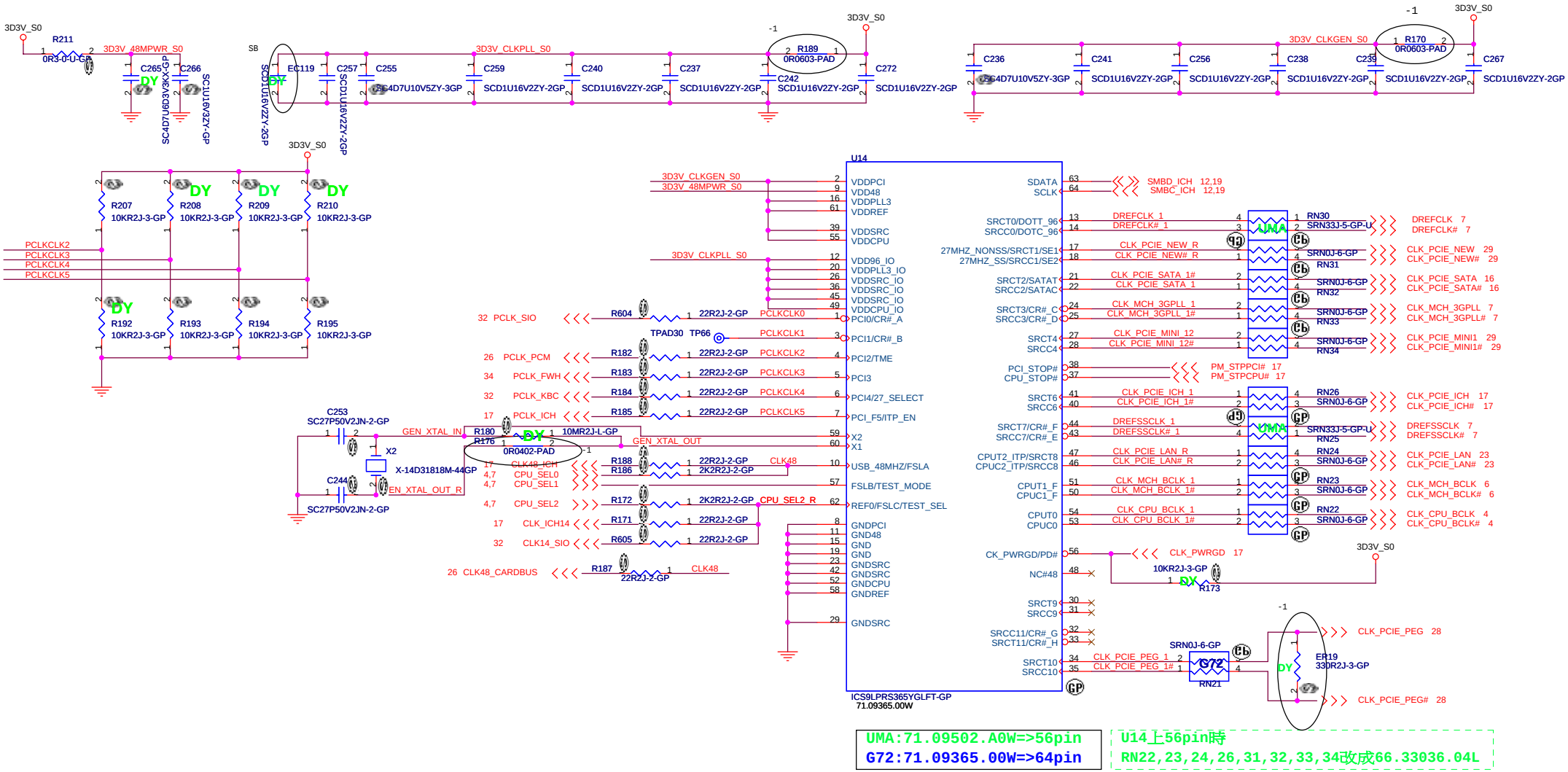

ICS9LPR502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

UMA

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Title: Clock Generator

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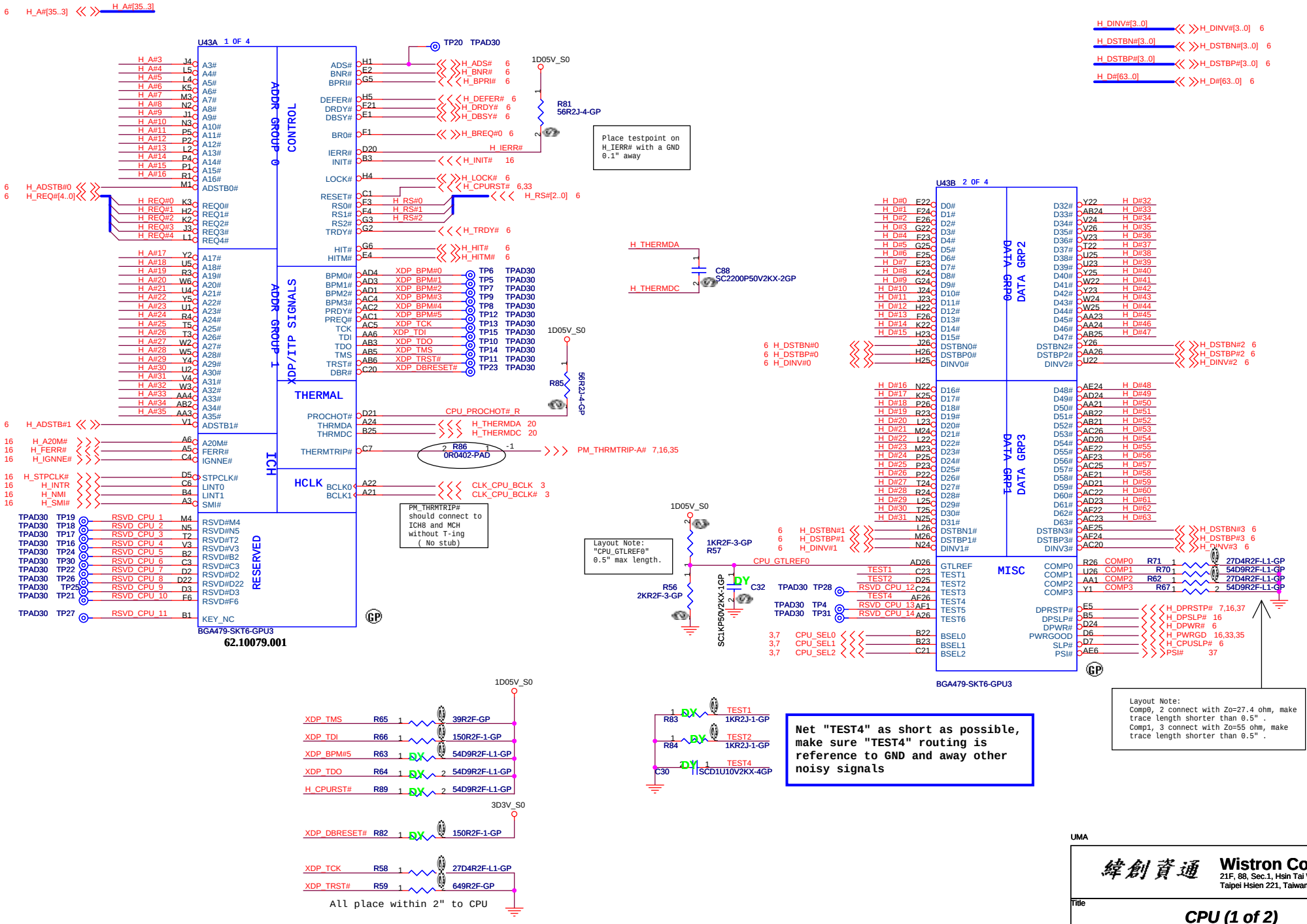
U43A 1 OF 4
ADDR GROUP 0
CONTROL
ADDR GROUP 1
XDP/ITP SIGNALS
THERMAL
HCLK
ICH
RESERVED
BGA479-SKT6-GPU3
62.10079.001
U43B 2 OF 4
DATA GRP2
DATA GRP0
DATA GRP3
DATA GRP1
MISC
BGA479-SKT6-GPU3
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH8 and MCH without T-ing (No stub)
Layout Note: "CPU_GTLREF0" 0.5" max length.
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
All place within 2" to CPU
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
UMA
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CPU (1 of 2)
Columbia/Tangiz
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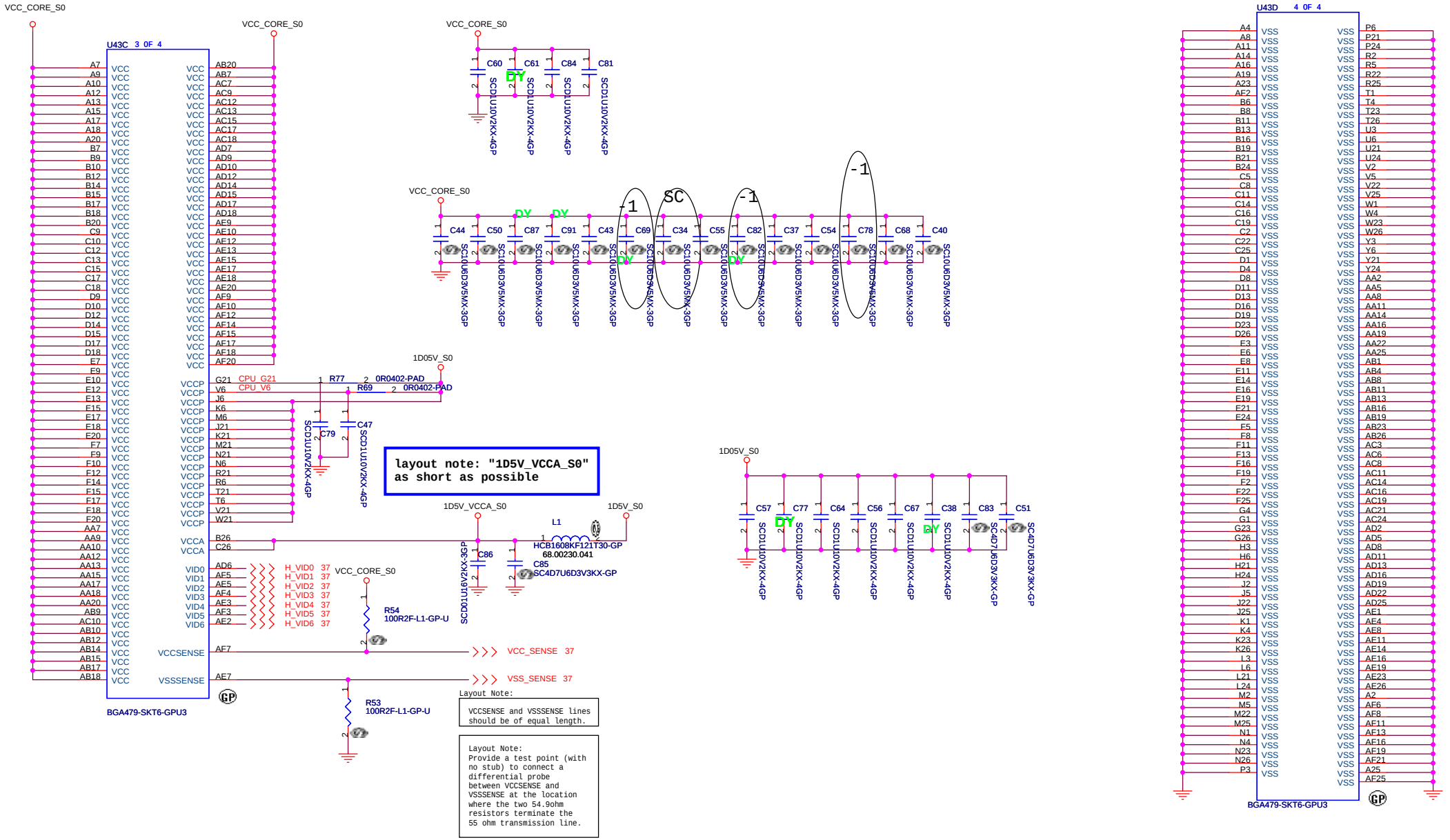

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Title	***CPU (2 of 2)***	
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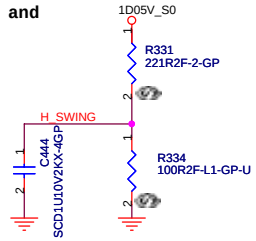
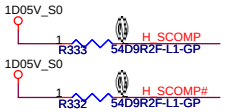
H_SWING routing Trace width and Spacing use 10 / 20 mil

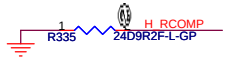
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)

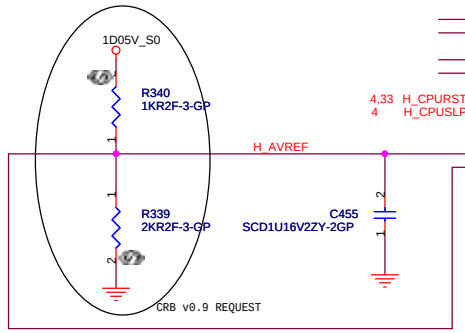


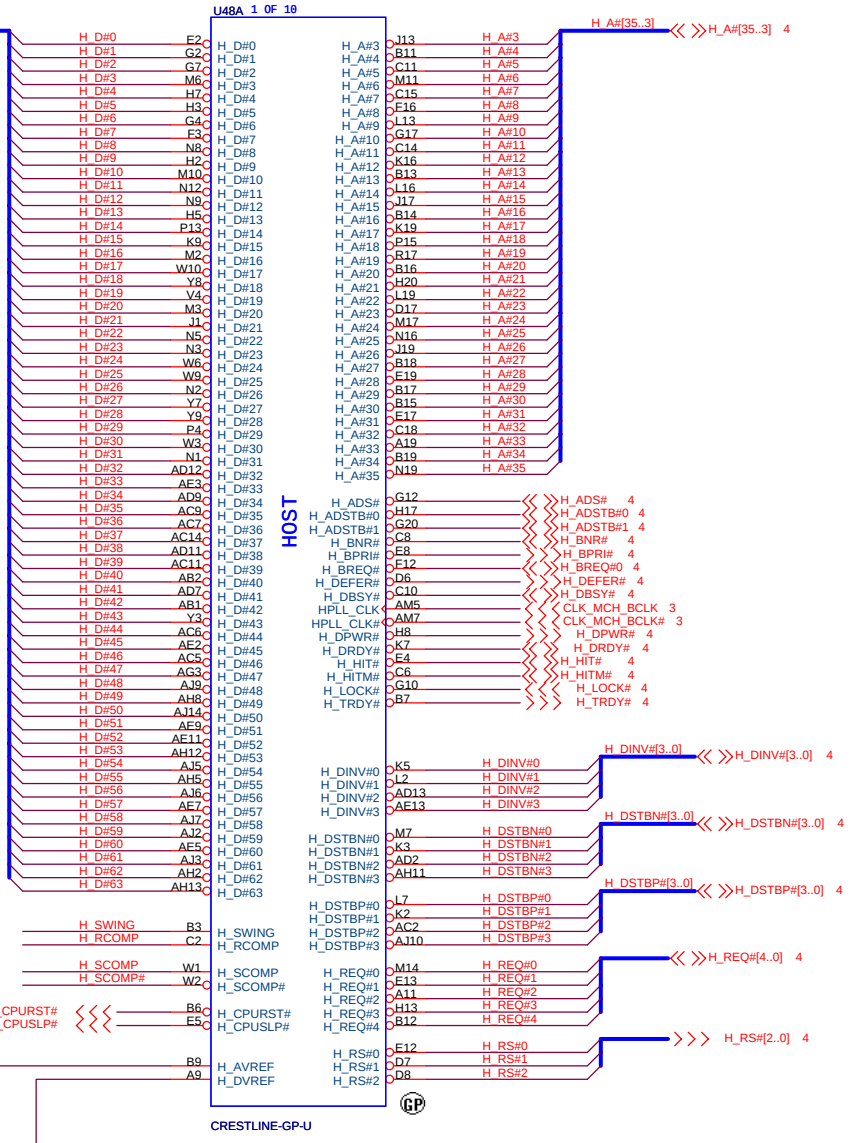
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

H_REF Decoupling Crestline close Crestline 100 mil





UMA

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Title: GMCH (1 of 6)

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RSVD
RSVD#P36
RSVD#P37
RSVD#R35
RSVD#N35
RSVD#AR12
RSVD#AR13
RSVD#AM12
RSVD#AN13
RSVD#J12
RSVD#AR37
RSVD#AM36
RSVD#AL36
RSVD#AM37
RSVD#D20
RSVD#H10
RSVD#B51
RSVD#BJ20
RSVD#BK22
RSVD#BF19
RSVD#BH20
RSVD#BK18
RSVD#BJ18
RSVD#BF23
RSVD#BG23
RSVD#BC23
RSVD#BD24
RSVD#BH39
RSVD#AW20
RSVD#BK20
RSVD#B44
RSVD#C44
RSVD#A35
RSVD#B37
RSVD#B36
RSVD#B34
RSVD#C34

DDR MUXING
SM_CK0 SM_CK1 SM_CK3 SM_CK4
SM_CK#0 SM_CK#1 SM_CK#3 SM_CK#4
SM_CKE0 SM_CKE1 SM_CKE3 SM_CKE4
SM_CS#0 SM_CS#1 SM_CS#2 SM_CS#3
SM_ODT0 SM_ODT1 SM_ODT2 SM_ODT3
SM_RCOMP_VOH SM_RCOMP_VOL SM_RCOMP SM_RCOMP# SM_VREF#AR49 SM_VREF#AW4
M_CLK_DDR0 M_CLK_DDR1 M_CLK_DDR2 M_CLK_DDR3
M_CLK_DDR#0 M_CLK_DDR#1 M_CLK_DDR#2 M_CLK_DDR#3
M_CKE0 M_CKE1 M_CKE2 M_CKE3
M_CS0# M_CS1# M_CS2# M_CS3#
M_ODT0 M_ODT1 M_ODT2 M_ODT3
M_RCOMPP M_RCOMPN
DDR_VREF_S3

CLK
DPLL_REF_CLK DPLL_REF_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK#
DREFCLK DREFCLK# DREFSSCLK DREFSSCLK#
PEG_CLK PEG_CLK#
CLK_MCH_3GPLL CLK_MCH_3GPLL#

DMI
DMI_RXN0 DMI_RXN1 DMI_RXN2 DMI_RXN3
DMI_RXP0 DMI_RXP1 DMI_RXP2 DMI_RXP3
DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3
DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3

CFG
CFG0 CFG1 CFG2 CFG3 CFG4 CFG5 CFG6 CFG7 CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG14 CFG15 CFG16 CFG17 CFG18 CFG19 CFG20
CPU_SEL0 CPU_SEL1 CPU_SEL2

GRAPHICS VID
GFX_VID0 GFX_VID1 GFX_VID2 GFX_VID3 GFX_VR_EN
TP48 TP51 TP116 TP49 TP50
TPAD28

PM
PM_BM_BUSY# PM_DPRSTP# PM_EXT_TS#0 PM_EXT_TS#1 PWROK RSTIN# THERMTRIP# DPRSLPVR
PM_BMBUSY# PM_EXTTS#0 PM_EXTTS#1 NB_THERMTRIP# PM_DPRSLPVR

ME
CL_CLK CL_DATA CL_PWROK CL_RST# CL_VREF
CL_CLK0 CL_DATA0 CL_RST#0
CLPWROK_MCH MCH_CLVREF

MISC
SDVO_CTRL_CLK SDVO_CTRL_DATA CLKREQ# ICH_SYNC#
CLK_3GPLLREQ# MCH_ICH_SYNC#
TEST1 TEST2 TEST2_GMCH

NC
NC#BJ51 NC#BK51 NC#BK50 NC#BK50 NC#BL50 NC#BL49 NC#BL3 NC#BL2 NC#BK1 NC#BK1 NC#BJ1 NC#E1 NC#E1 NC#A5 NC#C51 NC#B50 NC#A50 NC#A49 NC#BK2

CRESTLINE-GP-U

UMA
U48C 3 OF 10

LVDS
L_BKLT_CTRL L_BKLT_EN L_CTRL_CLK L_CTRL_DATA L_DDC_CLK L_DDC_DATA L_VDD_EN
LIBG L_LVBG
LVDS_IBG LVDS_VBG LVDS_VREFH LVDS_VREFL
LVDSA_CLK# LVDSA_CLK
LVDSB_CLK# LVDSB_CLK
LVDSA_DATA#0 LVDSA_DATA#1 LVDSA_DATA#2 LVDSA_DATA#3
LVDSA_DATA0 LVDSA_DATA1 LVDSA_DATA2 LVDSA_DATA3
LVDSB_DATA#0 LVDSB_DATA#1 LVDSB_DATA#2
LVDSB_DATA0 LVDSB_DATA1 LVDSB_DATA2
L_BKLT_CTRL L_BKLT_EN L_CTRL_CLK L_CTRL_DATA L_DDC_CLK L_DDC_DATA L_VDD_EN

TV
TVA_DAC TVB_DAC TVC_DAC
TVA_RTN TVB_RTN TVC_RTN
TV_DCONSEL0 TV_DCONSEL1

VGA
CRT_BLUE CRT_BLUE# CRT_GREEN CRT_GREEN# CRT_RED CRT_RED#
CRT_DDC_CLK CRT_DDC_DATA CRT_VSYNC CRT_TVO_IREF CRT_HSYNC

PCI_EXPRESS GRAPHICS
PEG_COMPI PEG_COMPO
PEG_RX#0 PEG_RX#1 PEG_RX#2 PEG_RX#3 PEG_RX#4 PEG_RX#5 PEG_RX#6 PEG_RX#7 PEG_RX#8 PEG_RX#9 PEG_RX#10 PEG_RX#11 PEG_RX#12 PEG_RX#13 PEG_RX#14 PEG_RX#15
PEG_RXN0 PEG_RXN1 PEG_RXN2 PEG_RXN3 PEG_RXN4 PEG_RXN5 PEG_RXN6 PEG_RXN7 PEG_RXN8 PEG_RXN9 PEG_RXN10 PEG_RXN11 PEG_RXN12 PEG_RXN13 PEG_RXN14 PEG_RXN15
PEG_RXN[15..0]
PEG_RX0 PEG_RX1 PEG_RX2 PEG_RX3 PEG_RX4 PEG_RX5 PEG_RX6 PEG_RX7 PEG_RX8 PEG_RX9 PEG_RX10 PEG_RX11 PEG_RX12 PEG_RX13 PEG_RX14 PEG_RX15
PEG_RXP0 PEG_RXP1 PEG_RXP2 PEG_RXP3 PEG_RXP4 PEG_RXP5 PEG_RXP6 PEG_RXP7 PEG_RXP8 PEG_RXP9 PEG_RXP10 PEG_RXP11 PEG_RXP12 PEG_RXP13 PEG_RXP14 PEG_RXP15
PEG_RXP[15..0]
PEG_TX#0 PEG_TX#1 PEG_TX#2 PEG_TX#3 PEG_TX#4 PEG_TX#5 PEG_TX#6 PEG_TX#7 PEG_TX#8 PEG_TX#9 PEG_TX#10 PEG_TX#11 PEG_TX#12 PEG_TX#13 PEG_TX#14 PEG_TX#15
GTXN0 GTXN1 GTXN2 GTXN3 GTXN4 GTXN5 GTXN6 GTXN7 GTXN8 GTXN9 GTXN10 GTXN11 GTXN12 GTXN13 GTXN14 GTXN15
PEG_TXN0 PEG_TXN1 PEG_TXN2 PEG_TXN3 PEG_TXN4 PEG_TXN5 PEG_TXN6 PEG_TXN7 PEG_TXN8 PEG_TXN9 PEG_TXN10 PEG_TXN11 PEG_TXN12 PEG_TXN13 PEG_TXN14 PEG_TXN15
PEG_TXN[15..0]
PEG_TX0 PEG_TX1 PEG_TX2 PEG_TX3 PEG_TX4 PEG_TX5 PEG_TX6 PEG_TX7 PEG_TX8 PEG_TX9 PEG_TX10 PEG_TX11 PEG_TX12 PEG_TX13 PEG_TX14 PEG_TX15
GTXP0 GTXP1 GTXP2 GTXP3 GTXP4 GTXP5 GTXP6 GTXP7 GTXP8 GTXP9 GTXP10 GTXP11 GTXP12 GTXP13 GTXP14 GTXP15
PEG_TXP0 PEG_TXP1 PEG_TXP2 PEG_TXP3 PEG_TXP4 PEG_TXP5 PEG_TXP6 PEG_TXP7 PEG_TXP8 PEG_TXP9 PEG_TXP10 PEG_TXP11 PEG_TXP12 PEG_TXP13 PEG_TXP14 PEG_TXP15
PEG_TXP[15..0]

1D8V_S3
R350 20R2J-2-GP M_RCOMPP
R348 20R2J-2-GP M_RCOMPN

3D3V_S0
R110 R104 R133 R106 R126 R117 R101 R121 R108 R107 R125 R122 R131 R124 R102 R120 R109 R127
DUMMY-R2 CFG18 CFG19 CFG20 CFG3 CFG4 CFG5 CFG6 CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG14 CFG15 CFG16 CFG17

1D05V_S0
R155 24D9R2F-L-GP
PEG_CMP

TPAD30 TP52
TPAD30 TP53
TPAD30 TP54

3D3V_S0
RN15 SRN2K2J-6-GP
TV_DCONSEL0 TV_DCONSEL1

UMA
15 GMCH_BLUE GMCH_BLUE
15 GMCH_GREEN GMCH_GREEN
15 GMCH_RED GMCH_RED
15 GMCH_DDCCLK GMCH_DDCCLK
15 GMCH_DDCDATA GMCH_DDCDATA
15 GMCH_VSYNC GMCH_VS
15 GMCH_HSYNC GMCH_HS
R369 33R2F-3-GP
R368 33R2F-3-GP
CRT_IREF
R360 1K3R2F-1-GP
CRESTLINE-GP-U

1D25V_S0
R161 1KR2F-3-GP
R157 392R2F-GP
C209 SCD01U10V2KX-4GP
-1

FOR Calero: 255 ohm
Crestline: 1.3k ohm
CRT_IREF routing Trace width use 20 mil

1D8V_S3
R353 1KR2F-3-GP
R356 3K01R2F-3-GP
R358 1KR2F-3-GP
C468 C473 SCD01U16V2KX-3GP
C465 C474 SC2D2U6D3V3MX-1-GP
SM_RCOMP_VOH
SM_RCOMP_VOL

UMA
R142 150R2F-1-GP
R139 150R2F-1-GP
R137 150R2F-1-GP
GMCH_BLUE GMCH_GREEN GMCH_RED

FOR Discrete change R137, R139 & R142 to 0 ohm

SB
R128 R129 R130 150R2F-1-GP
TV_DACA TV_DACB TV_DACC

UMA
GMCH_BL_ON R149 100KR2J-1-GP
GMCH_LCDVDD_ON R138 100KR2J-1-GP
LIBG R154 2K4R2F-GP
GMCH_VS R153 0R2J-2-GP
GMCH_HS R148 0R2J-2-GP
G72

3D3V_S0
RN20 SRN10KJ-6-GP
LCTLB_DATA LCTLA_CLK PM_EXTTS#0 PM_EXTTS#1

3D3V_S0
R141 10KR2J-3-GP
CLK_3GPLLREQ#

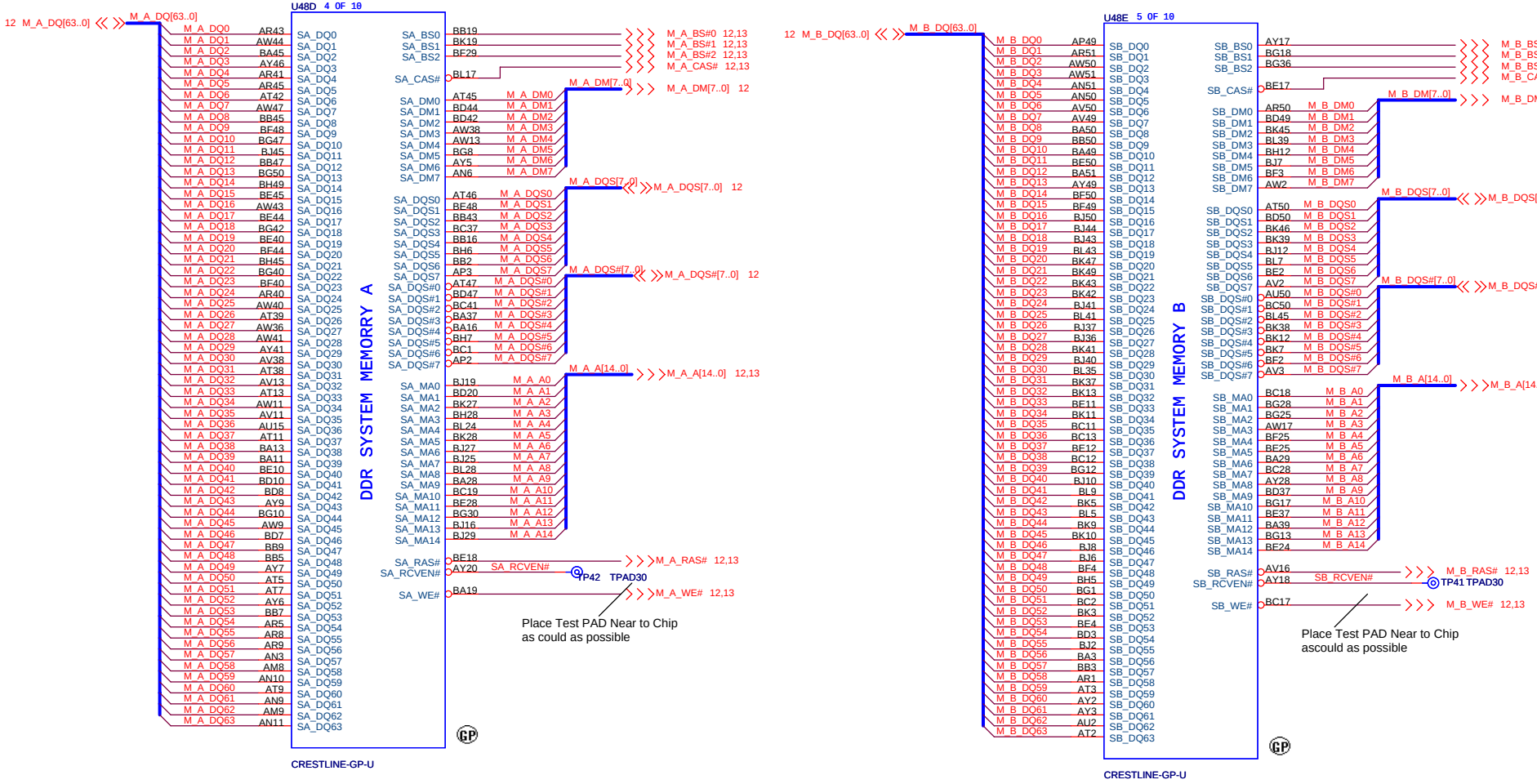
R135 20KR2J-L2-GP

SC100P50V2JN-3GP C153
R103 R134 0R0402-PAD
4,16,35 PM_THRMTRIP-A#
17,37 PM_DPRSLPVR

R152 R159 R158 R105 0R0402-PAD
100R2J-2-GP
4,16,37 H_DPRSTP#
17,37 VGATE_PWRGD
17,20 PWROK
17,21,23,28,29,32,34 PLT_RST1#

蜂創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (2 of 6)
Size: Document Number: Columbia/Tangiz Rev: -1
Date: Monday, February 26, 2007 Sheet 7 of 45



緯創資通 **Wistron Corporation**
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Title: ***GMCH (3 of 6)***

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VCC_NCTF + VCC=1573mA

1573mA

U48F 6 OF 10

VCC CORE

R143 0R0402-PAD

POWER

3138mA

VCC SM

VCC GFX NCTF

VCC_AXG_NCTF + VCC_AXG=7700mA

UMA

SB:Remove R123,R132,R136,R144

SB:DIS remove 0 ohm on C129,C210,C158,C161

VCC GFX

VCC SM LF

CRESTLINE-GP-U

FOR VCC CORE AND VCC NCTF

DY

ST220U2D5VBM-2GP

308 mils from the Edge

Coupling CAP

U48G 7 OF 10

VCC NCTF

VSS NCTF

FOR VCC CORE

Coupling CAP 370 mils from the Edge

POWER

VSS SCB

VCC_AXM_S3

FOR VCC AXM NCTF AND VCC AXM

R147 0R1206-PAD

Place on the Edge

VCC_AXM_NCTF + VCC_AXM=540mA

VSS AXM

VSS AXM NCTF

CRESTLINE-GP-U

Place CAP where LVDS and DDR2 taps

FOR VCC SM

Place on the Edge

Wistron Corporation
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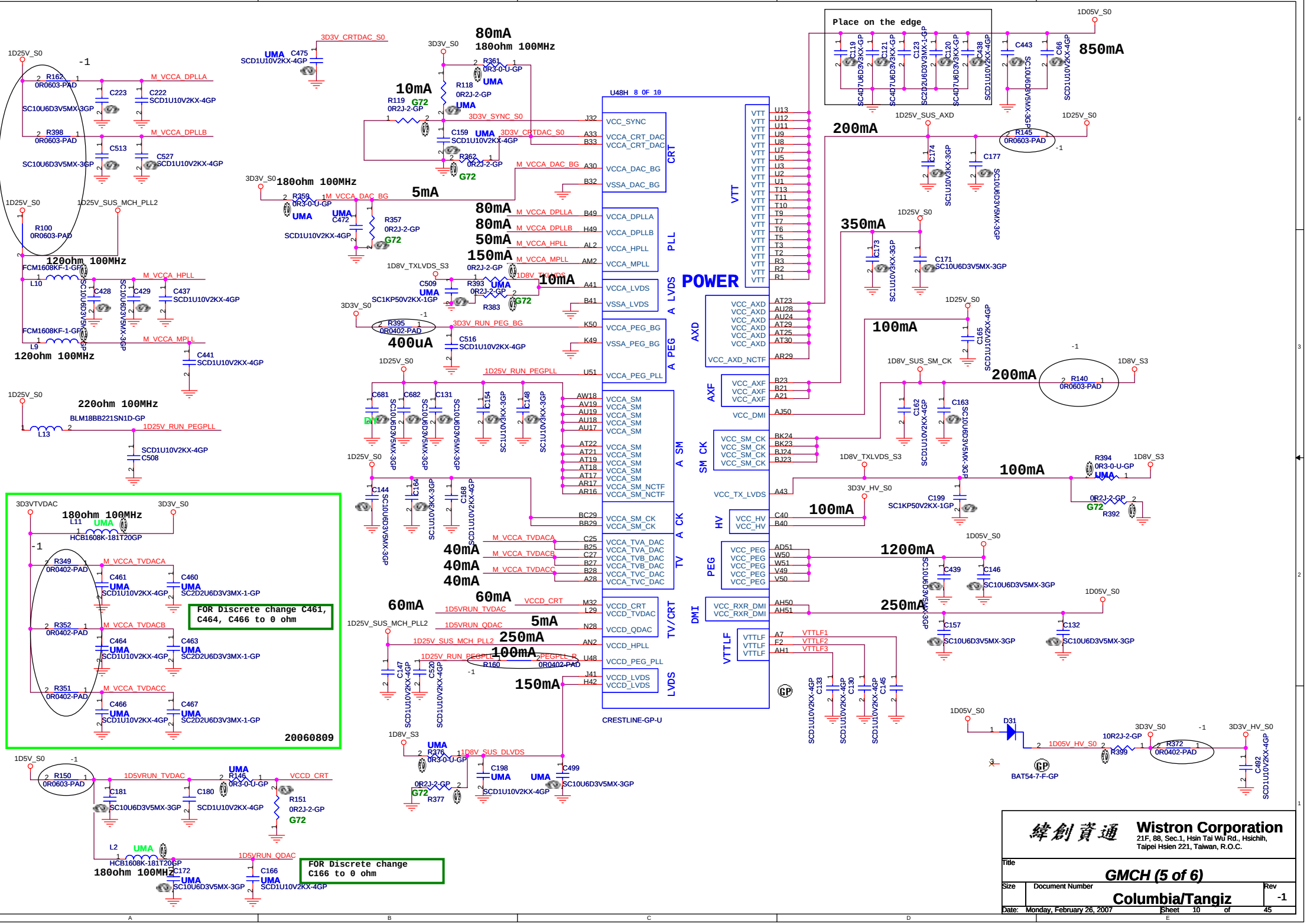
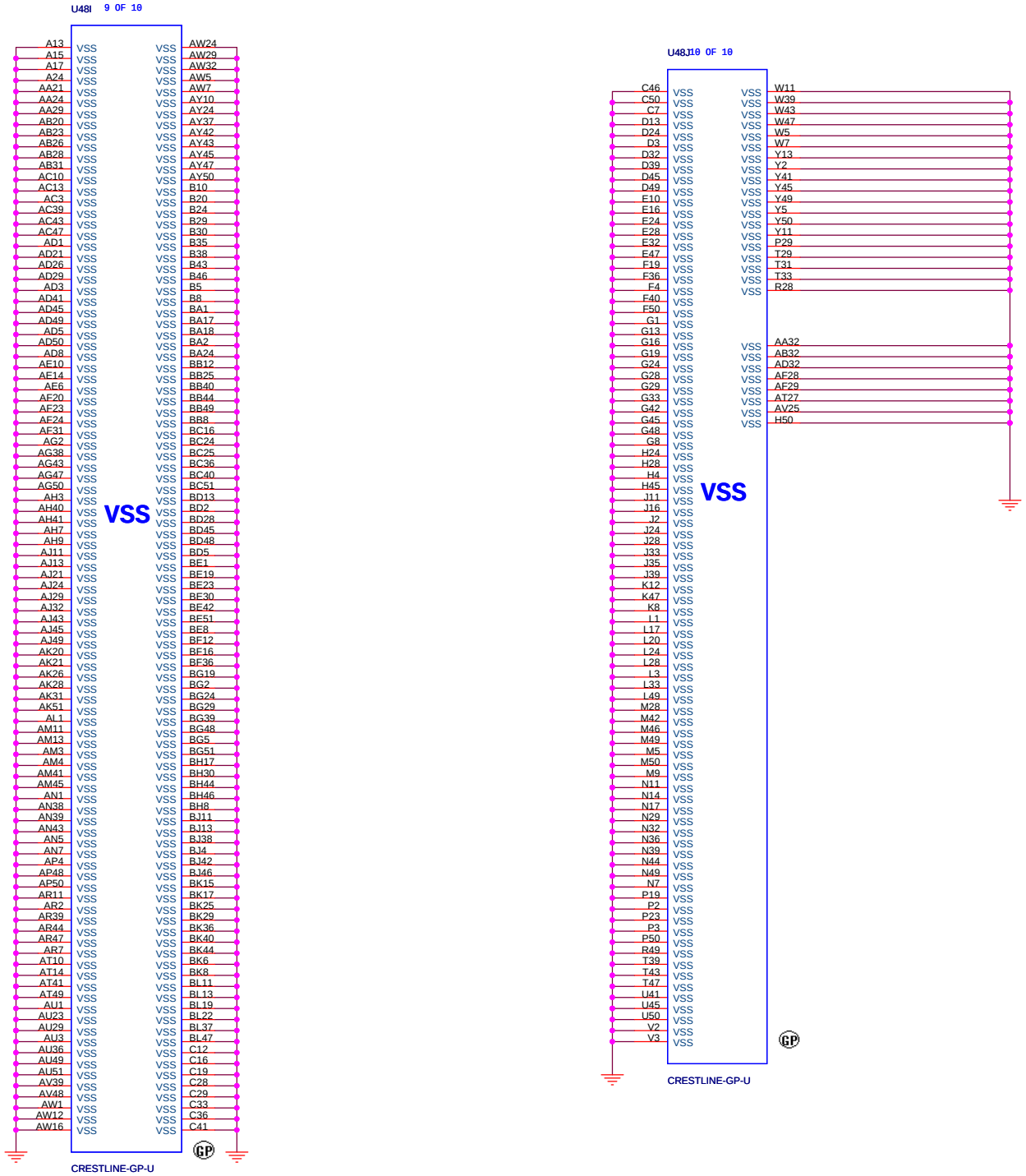
Title: GMCH (4 of 6)

Size: Document Number: Columbia/Tangiz Rev: -1

Date: Monday, February 26, 2007 Sheet 9 of 45


Place on the edge
POWER
CRESTLINE-GP-U
U48H 8 OF 10
120ohm 100MHz
220ohm 100MHz
180ohm 100MHz
400uA
850mA
200mA
350mA
100mA
1200mA
250mA
80mA
10mA
5mA
50mA
150mA
40mA
60mA
FOR Discrete change C461, C464, C466 to 0 ohm
FOR Discrete change C166 to 0 ohm
20060809
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
GMCH (5 of 6)
Columbia/Tangiz
Monday, February 26, 2007



緯創資通 **Wistron Corporation**
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Title: ***GMCH (6 of 6)***

Size	Document Number	Rev
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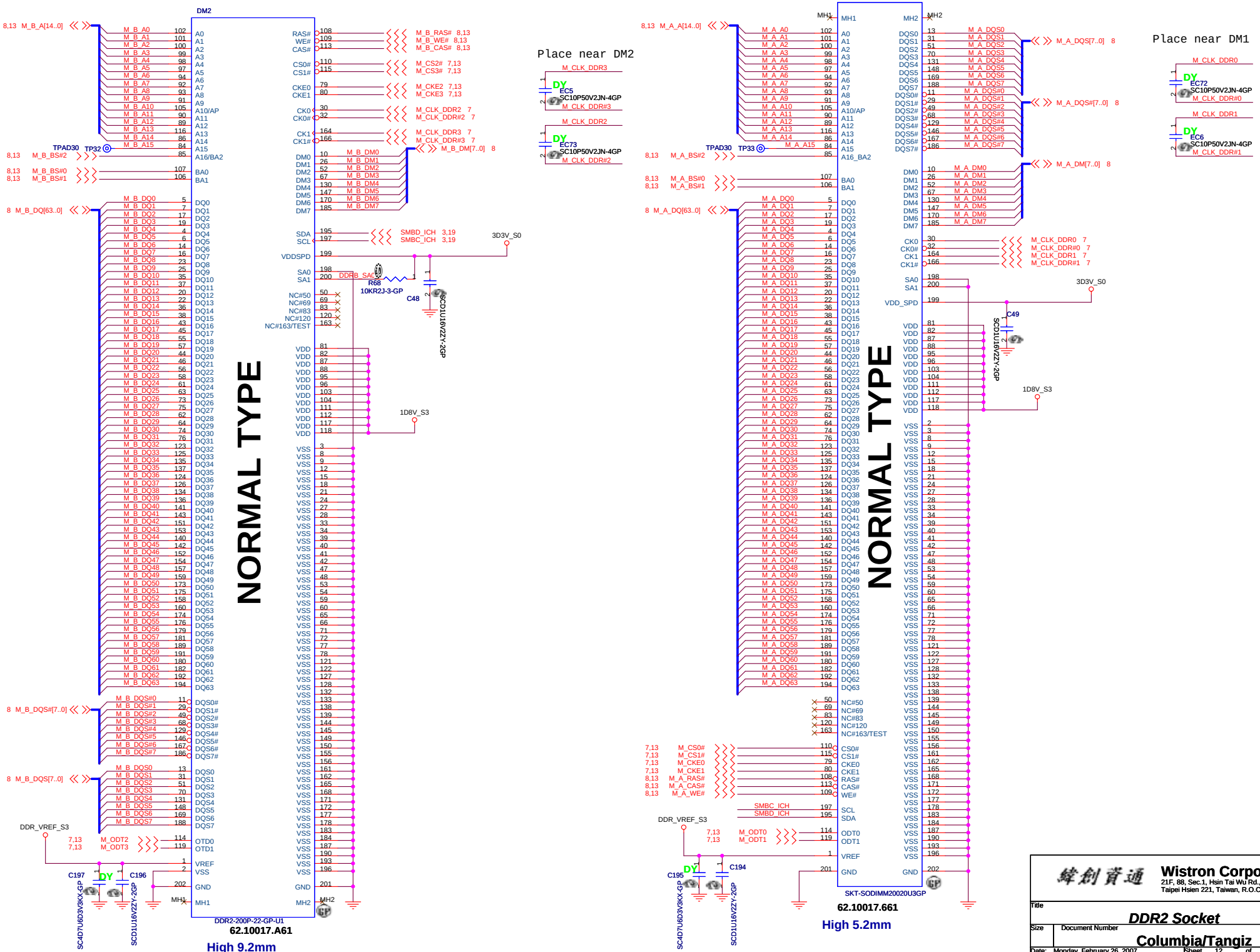
DM2
NORMAL TYPE
DDR2-200P-22-GP-U1
62.10017.A61
High 9.2mm
DM1
NORMAL TYPE
SKT-SODIMM20020U3GP
62.10017.661
High 5.2mm
Place near DM2
Place near DM1
M_CLK_DDR3
M_CLK_DDR#3
M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
EC5
EC73
EC72
EC6
SC10P50V2JN-4GP
DY
R68
10KR2J-3-GP
C48
C49
C194
C195
C196
C197
SCD1U16V2ZY-2GP
SC4D7U6D3V3KX-GP
SCD1U16V2ZY-2GP
3D3V_S0
1D8V_S3
DDR_VREF_S3
SMBC_ICH
SMBD_ICH
DDRB_SA0
TPAD30
TP32
TP33
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR2 Socket
Size
Document Number
Columbia/Tangiz
Rev
-1
Date: Monday, February 26, 2007
Sheet 12 of 45

PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

RN13 SRN56J-5-GP: M_A_A12, M_A_A8 → M_CKE0 7,12; M_A_BS#2 8,12

RN12 SRN56J-5-GP: M_B_A8, M_B_A9, M_B_A5

RN14 SRN56J-5-GP: M_B_A12 → M_CKE3 7,12; M_B_BS#2 8,12; M_CKE2 7,12

RN7 SRN56J-5-GP: M_B_A3, M_B_A1, M_B_A10 → M_B_WE# 8,12

RN1 SRN56J-5-GP: M_B_A13 → M_ODT2 7,12; M_ODT3 7,12; M_B_RAS# 8,12

RN5 SRN56J-5-GP: M_B_A2, M_B_A0, M_B_A4 → M_B_BS#1 8,12

RN9 SRN56J-5-GP: M_B_A14, M_B_A11, M_B_A7, M_B_A6

RN4 SRN56J-5-GP: M_B_BS#0 8,12; M_B_CAS# 8,12; M_CS3# 7,12; M_CS2# 7,12

RN3 SRN56J-5-GP: M_A_A13 → M_ODT0 7,12; M_CS0# 7,12; M_A_RAS# 8,12

RN8 SRN56J-5-GP: M_A_A0, M_A_A2, M_A_A4 → M_A_BS#1 8,12

RN2 SRN56J-5-GP: → M_A_CAS# 8,12; M_ODT1 7,12; M_CS1# 7,12

RN10 SRN56J-5-GP: M_A_A9, M_A_A14, M_A_A5, M_A_A3

RN11 SRN56J-5-GP: M_A_A6, M_A_A7, M_A_A11 → M_CKE1 7,12

RN6 SRN56J-5-GP: M_A_A1, M_A_A10 → M_A_BS#0 8,12; M_A_WE# 8,12

M_A_A[14..0] ≪≫ M_A_A[14..0] 8,12

M_B_A[14..0] ≪≫ M_B_A[14..0] 8,12

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

C110 C134 C117 C109 C103 C115 C125 C112 C97 C118 C128 — SCD1U16V2ZY-2GP (DY)

C138 C104 C98 C106 C107 C127 C105 C101 C99 C137 C102 — SCD1U16V2ZY-2GP (DY)

Place these Caps near DM1

1D8V_S3

C446 C436 C432 C424 C417 — SC2D2U6D3V3MX-1GP

C421 C427 C434 C442 — SCD1U16V2ZY-2GP (DY)

Place these Caps near DM2

1D8V_S3

C447 C440 C433 C426 C418 — SC2D2U6D3V3MX-1GP

C445 C435 C431 C423 — SCD1U16V2ZY-2GP (DY)

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
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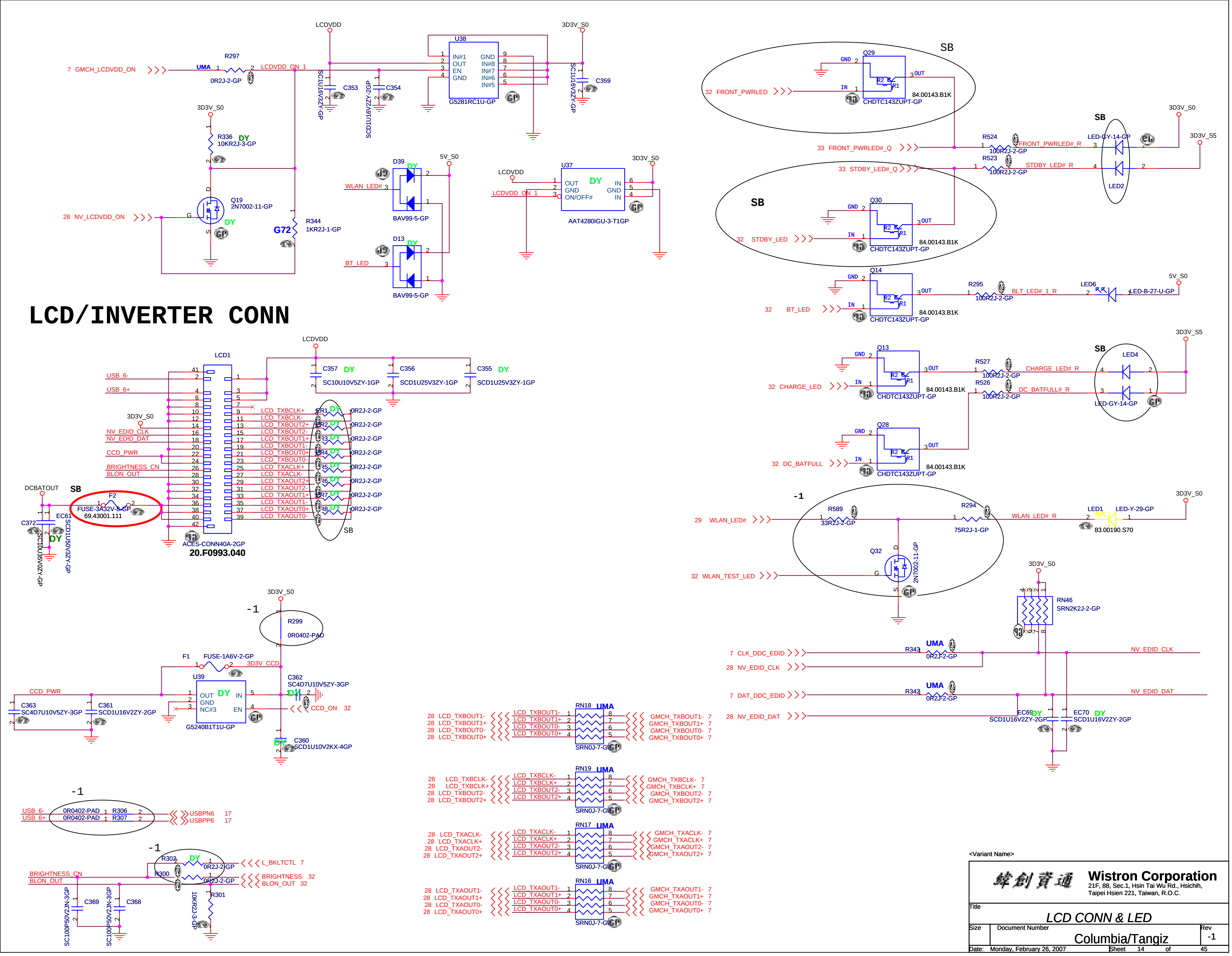
LCD/INVERTER CONN
LCDVDD
3D3V_S0
U38
G5281RC1U-GP
IN#1 OUT EN GND
GND IN#8 IN#7 IN#6 IN#5
7 GMCH_LCDVDD_ON
UMA
R297
0R2J-2-GP
LCDVDD_ON_1
C353
SC1U6V3ZY-GP
C354
SCD1U16V2ZY-GP
C359
SC1U16V3ZY-GP
R336 DY
10KR2J-3-GP
Q19
2N7002-11-GP
28 NV_LCDVDD_ON
G72
R344
1KR2J-1-GP
D39 DY
5V_S0
WLAN_LED#
BAV99-5-GP
D13 DY
BT_LED
U37 DY
AAT4280IGU-3-T1GP
OUT GND ON/OFF#
IN GND IN
LCDVDD_ON
SB
Q29
CHDTC143ZUPT-GP
84.00143.B1K
32 FRONT_PWRLED
33 FRONT_PWRLED#_Q
R524
100R2J-2-GP
FRONT_PWRLED#_R
LED-GY-14-GP
LED2
3D3V_S5
R523
100R2J-2-GP
33 STDBY_LED#_Q
STDBY_LED#_R
Q30
32 STDBY_LED
Q14
32 BT_LED
R295
100R2J-2-GP
BLT_LED#_1_R
LED6
LED-B-27-U-GP
Q13
32 CHARGE_LED
R527
100R2J-2-GP
CHARGE_LED#_R
LED4
R526
100R2J-2-GP
DC_BATFULL#_R
LED-GY-14-GP
Q28
32 DC_BATFULL
-1
29 WLAN_LED#
R589
33R2J-2-GP
R294
75R2J-1-GP
WLAN_LED#_R
LED1
LED-Y-29-GP
83.00190.S70
Q32
2N7002-11-GP
32 WLAN_TEST_LED
RN46
SRN2K2J-2-GP
7 CLK_DDC_EDID
R343 UMA
0R2J-2-GP
28 NV_EDID_CLK
NV_EDID_CLK
7 DAT_DDC_EDID
R342 UMA
0R2J-2-GP
28 NV_EDID_DAT
NV_EDID_DAT
EC69 DY
SCD1U16V2ZY-GP
EC70 DY
SCD1U16V2ZY-GP
LCD1
ACES-CONN40A-2GP
20.F0993.040
USB_6-
USB_6+
NV_EDID_CLK
NV_EDID_DAT
CCD_PWR
BRIGHTNESS_CN
BLON_OUT
LCD_TXBCLK+
LCD_TXBCLK-
LCD_TXBOUT2+
LCD_TXBOUT2-
LCD_TXBOUT1+
LCD_TXBOUT1-
LCD_TXBOUT0+
LCD_TXBOUT0-
LCD_TXACLK+
LCD_TXACLK-
LCD_TXAOUT2+
LCD_TXAOUT2-
LCD_TXAOUT1+
LCD_TXAOUT1-
LCD_TXAOUT0+
LCD_TXAOUT0-
0R2J-2-GP
C357 DY
SC10U10V5ZY-1GP
C356
SCD1U25V3ZY-1GP
C355 DY
SCD1U25V3ZY-1GP
DCBATOUT
F2
FUSE-3A32V-8-GP
69.43001.111
C372
SC10U35V0ZY-GP
EC61 DY
SCD1U50V3ZY-GP
R299
0R0402-PAD
F1
FUSE-1A6V-2-GP
3D3V_CCD
U39
G5240B1T1U-GP
OUT GND NC#3
IN EN
C362
SC4D7U10V5ZY-3GP
CCD_ON 32
C363
SC4D7U10V5ZY-3GP
C361
SCD1U16V2ZY-GP
C360
SCD1U10V2KX-4GP
USB_6-
USB_6+
0R0402-PAD
R306
R307
USBPN6 17
USBPP6 17
R302 DY
0R2J-2-GP
L_BKLTCTL 7
R300
BRIGHTNESS 32
BLON_OUT 32
R301
10KR2J-3-GP
C369
SC100P50V2JN-3GP
C368
SC100P50V2JN-3GP
RN18 UMA
RN19 UMA
RN17 UMA
RN16 UMA
SRN0J-7-GP
28 LCD_TXBOUT1-
28 LCD_TXBOUT1+
28 LCD_TXBOUT0-
28 LCD_TXBOUT0+
GMCH_TXBOUT1- 7
GMCH_TXBOUT1+ 7
GMCH_TXBOUT0- 7
GMCH_TXBOUT0+ 7
28 LCD_TXBCLK-
28 LCD_TXBCLK+
28 LCD_TXBOUT2-
28 LCD_TXBOUT2+
GMCH_TXBCLK- 7
GMCH_TXBCLK+ 7
GMCH_TXBOUT2- 7
GMCH_TXBOUT2+ 7
28 LCD_TXACLK-
28 LCD_TXACLK+
28 LCD_TXAOUT2-
28 LCD_TXAOUT2+
GMCH_TXACLK- 7
GMCH_TXACLK+ 7
GMCH_TXAOUT2- 7
GMCH_TXAOUT2+ 7
28 LCD_TXAOUT1-
28 LCD_TXAOUT1+
28 LCD_TXAOUT0-
28 LCD_TXAOUT0+
GMCH_TXAOUT1- 7
GMCH_TXAOUT1+ 7
GMCH_TXAOUT0- 7
GMCH_TXAOUT0+ 7
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
LCD CONN & LED
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CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

28 NV_RED
7 GMCH_RED
28 NV_GREEN
7 GMCH_GREEN
28 NV_BLUE
7 GMCH_BLUE
R113 R112 R111 UMA 0R2J-2-GP
R328 R325 R323 150R2F-1-GP
C416 C411 C407 SC22P50V2JN-4GP DY
L8 L7 L6 FCB1608CF-GP
CRT_R CRT_G CRT_B
C420 C413 C409 SC6D8P50V2DN-GP UMA
-1
SC

For DIS
C420--->78.15034.1FL
C413,C409--->78.18034.1FL

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT1
VIDEO-15-21-U4-GP
20.20334.015
CRT_R CRT_G CRT_B CRT_HSYNC1 5V_CRT_S0 CLK_DDC1_5 CRT_VSYNC1 DAT_DDC1_5
C415 SC100P50V2JN-3GP
C405 SC18P50V2JN-1-GP
C419 SCD01U16V2KX-3GP
C406 SC18P50V2JN-1-GP
C414 SC100P50V2JN-3GP
MH1 MH2

32 CRT_DEC#
R321 470R2J-2-GP
C404 SC100P50V2JN-3GP
D1 BAV99-5-GP DY
5V_S0

Hsync & Vsync level shift

7 GMCH_HSYNC
28 NV_HSYNC
7 GMCH_VSYNC
28 NV_VSYNC
R363 R364 UMA 0R2J-2-GP
C108 SCD1U16V2ZY-2GP
C412 C408 SC18P50V2JN-1-GP DY
U44A U44B TSAHCT125PW-GP
CRT_HSYNC1_R CRT_VSYNC1_R
R324 R322 0R0402-PAD
CRT_HSYNC1 CRT_VSYNC1
-1

DDC_CLK & DATA level shift

28 NV_DDCDAT
7 GMCH_DDCDATA
28 NV_DDCCLK
7 GMCH_DDCCLK
R366 R365 0R2J-2-GP UMA
NV_DDCDAT NV_DDCCLK
RN44 SRN2K2J-2-GP
SRN10KJ-6-GP RN43
Q16 2N7002DW-1-GP
CH751H-40PT D23
3D3V_S0 5V_CRT_S0 5V_S0
CRT_DEC# DAT_DDC1_5 CLK_DDC1_5

TV CONN

28 NV_TV_LUMA
7 TV_DACB
28 NV_TV_CRMA
7 TV_DACC
28 NV_TV_COMP
7 TV_DACA
R115 R116 R114 UMA 0R2J-2-GP
R430 R413 R423 150R2F-1-GP
C565 C545 C554 SC33P50V2JN-3GP
L17 L15 L16 IND-1D2UH-5-GP
C570 C544 C558 SC150P50V2JN-3GP
C566 C546 C555 SC270P50V2JN-2GP
LUMA_1 CRMA_1 COMP_1
MINDIN7-22-GP TVOUT1
22.10021.I81

D11 D8 D9 BAV99-5-GP DY 5V_S0
D5 D3 D2 BAV99-5-GP DY 5V_S0

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*CRT/TV Connector*	
Size	Document Number: Columbia/Tangiz	Rev: -1
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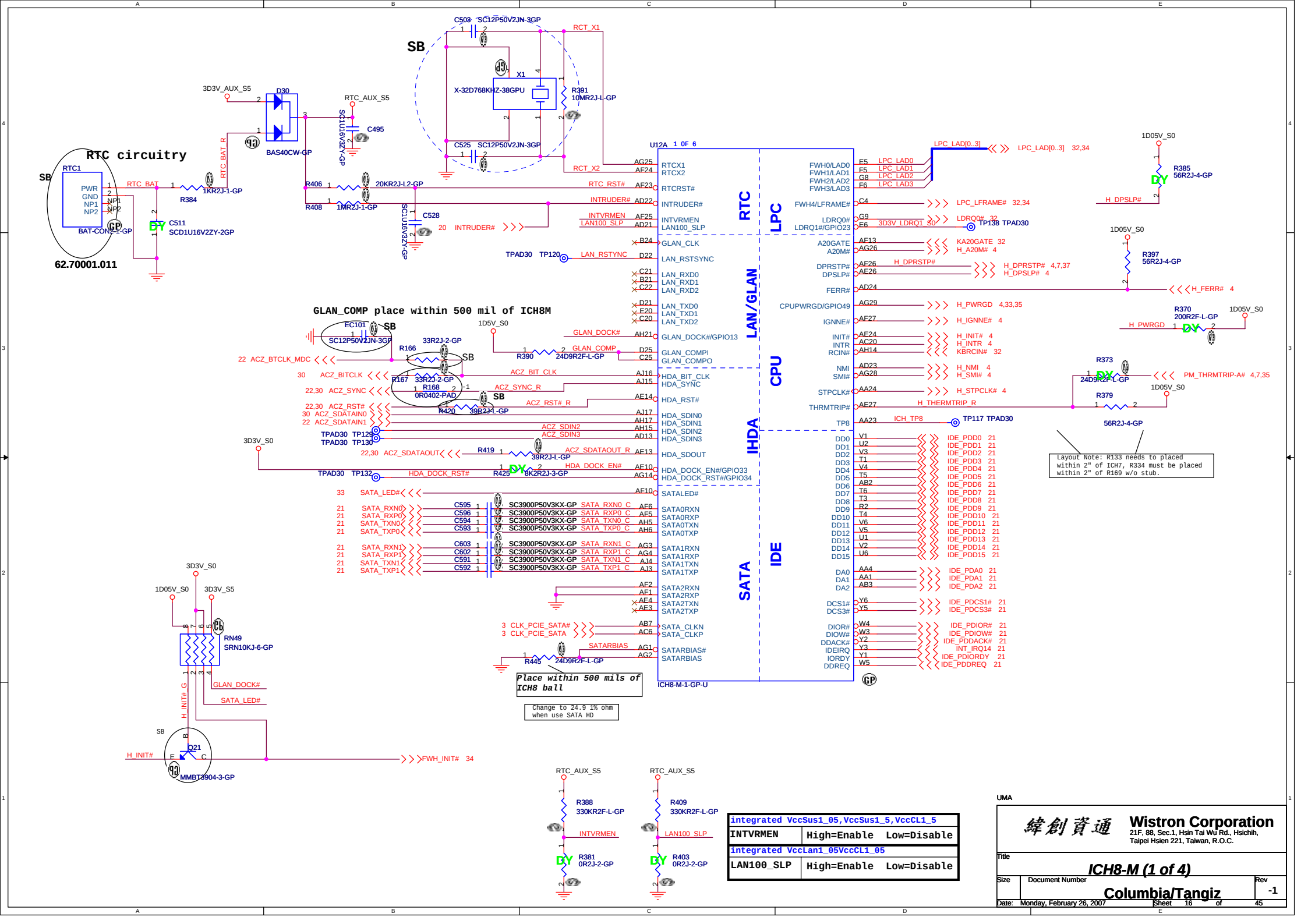
RTC circuitry
62.70001.011
GLAN_COMP place within 500 mil of ICH8M
Place within 500 mils of ICH8 ball
Change to 24.9 1% ohm when use SATA HD
Layout Note: R133 needs to placed within 2" of ICH7, R334 must be placed within 2" of R169 w/o stub.
U12A 1 OF 6
ICH8-M-1-GP-U
RTC
LPC
LAN/GLAN
CPU
IHDA
SATA
IDE
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8-M (1 of 4)
Size
Document Number
Columbia/Tangiz
Rev
-1
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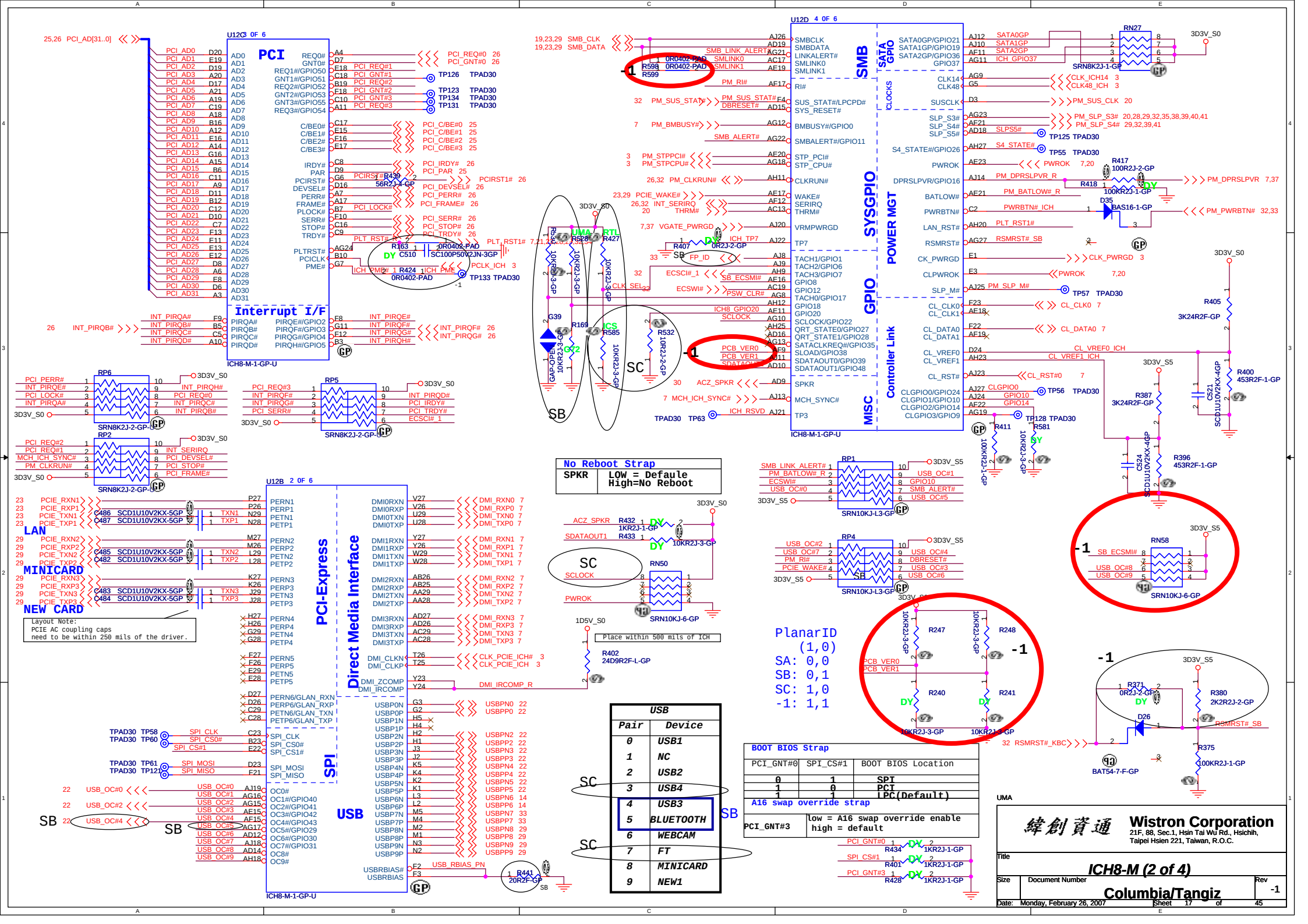
U12C 3 OF 6
PCI
Interrupt I/F
ICH8-M-1-GP-U
U12D 4 OF 6
SMB
SATA GPIO
CLOCKS
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
ICH8-M-1-GP-U
U12B 2 OF 6
PCI-Express
Direct Media Interface
SPI
USB
ICH8-M-1-GP-U
LAN
MINICARD
NEW CARD
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
Place within 500 mils of ICH
PlanarID
(1,0)
SA: 0,0
SB: 0,1
SC: 1,0
-1: 1,1
USB
Pair
Device
0
USB1
1
NC
2
USB2
3
USB4
4
USB3
5
BLUETOOTH
6
WEBCAM
7
FT
8
MINICARD
9
NEW1
BOOT BIOS Strap
PCI_GNT#0
SPI_CS#1
BOOT BIOS Location
0
1
SPI
1
0
PCI
1
1
LPC(Default)
A16 swap override strap
PCI_GNT#3
low = A16 swap override enable
high = default
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8-M (2 of 4)
Size
Document Number
Columbia/Tangiz
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-1
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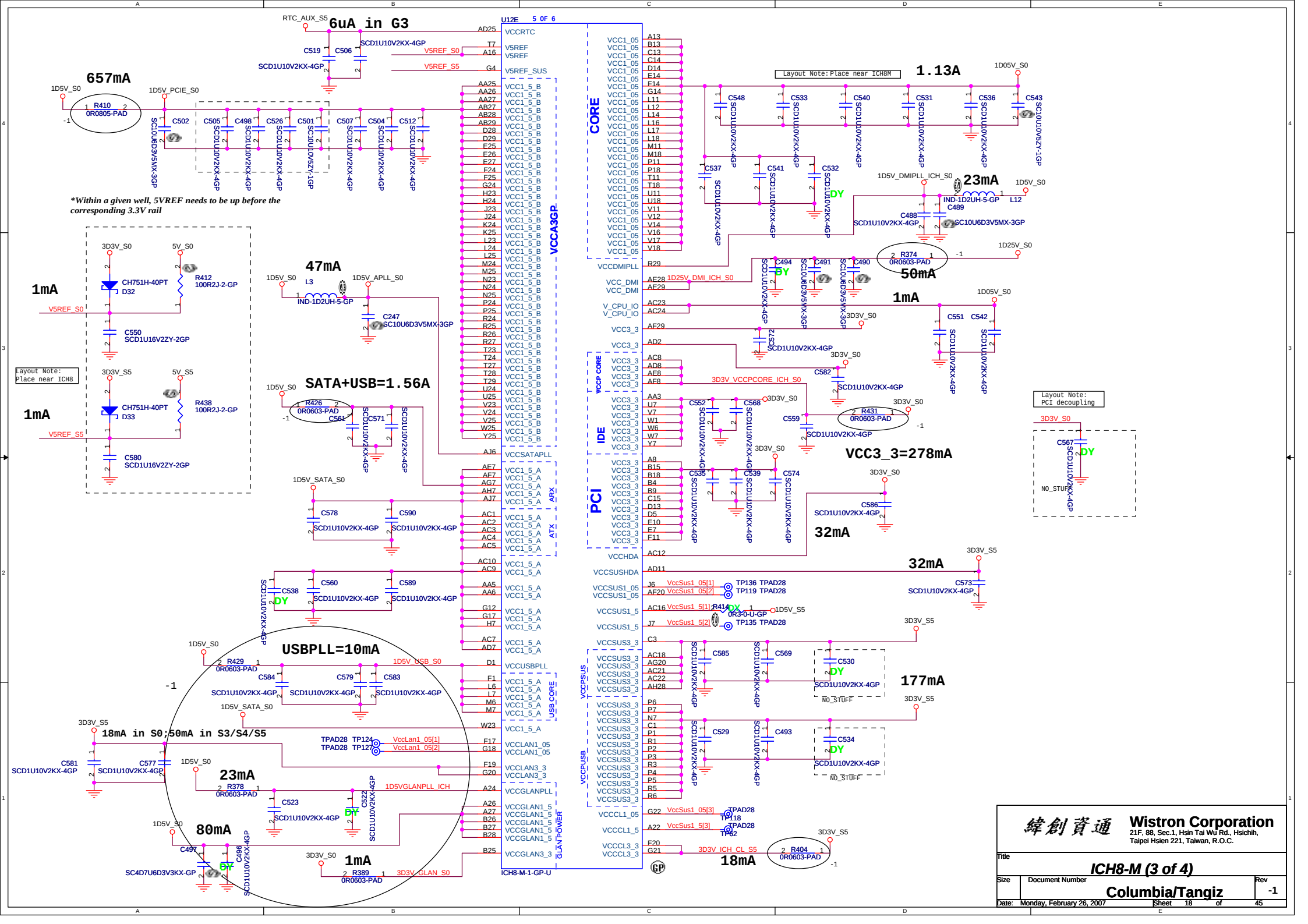
6uA in G3
657mA
1mA
47mA
SATA+USB=1.56A
1mA
1mA
USBPLL=10mA
18mA in S0;50mA in S3/S4/S5
23mA
80mA
1mA
1.13A
23mA
50mA
1mA
VCC3_3=278mA
32mA
32mA
177mA
18mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near ICH8M
Layout Note: Place near ICH8
Layout Note: PCI decoupling
U12E 5 OF 6
ICH8-M-1-GP-U
CORE
PCI
IDE
VCCA3GP
USB CORE
GLAN POWER
VCCP CORE
Wistron Corporation
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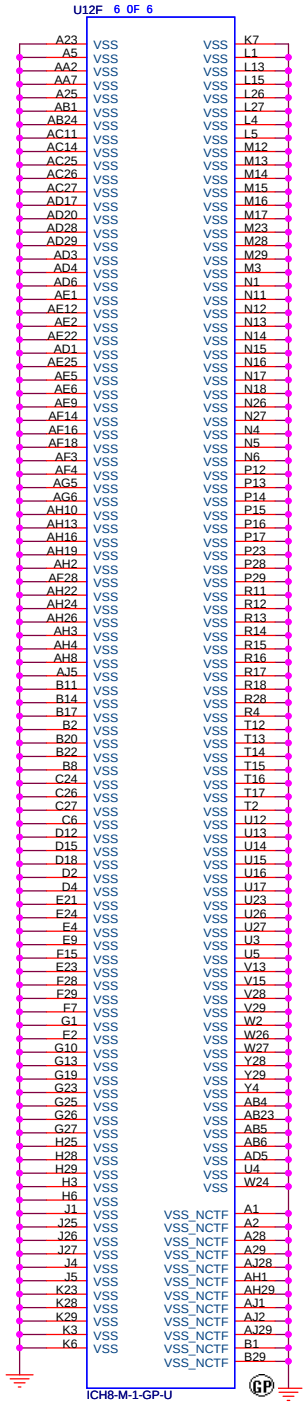
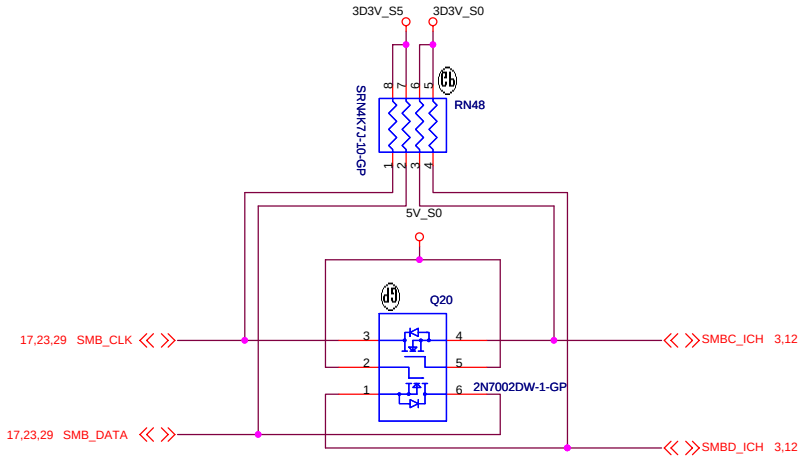
Title
ICH8-M (3 of 4)
Size
Document Number
Columbia/Tangiz
Rev
-1
Date: Monday, February 26, 2007
Sheet 18 of 45





Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

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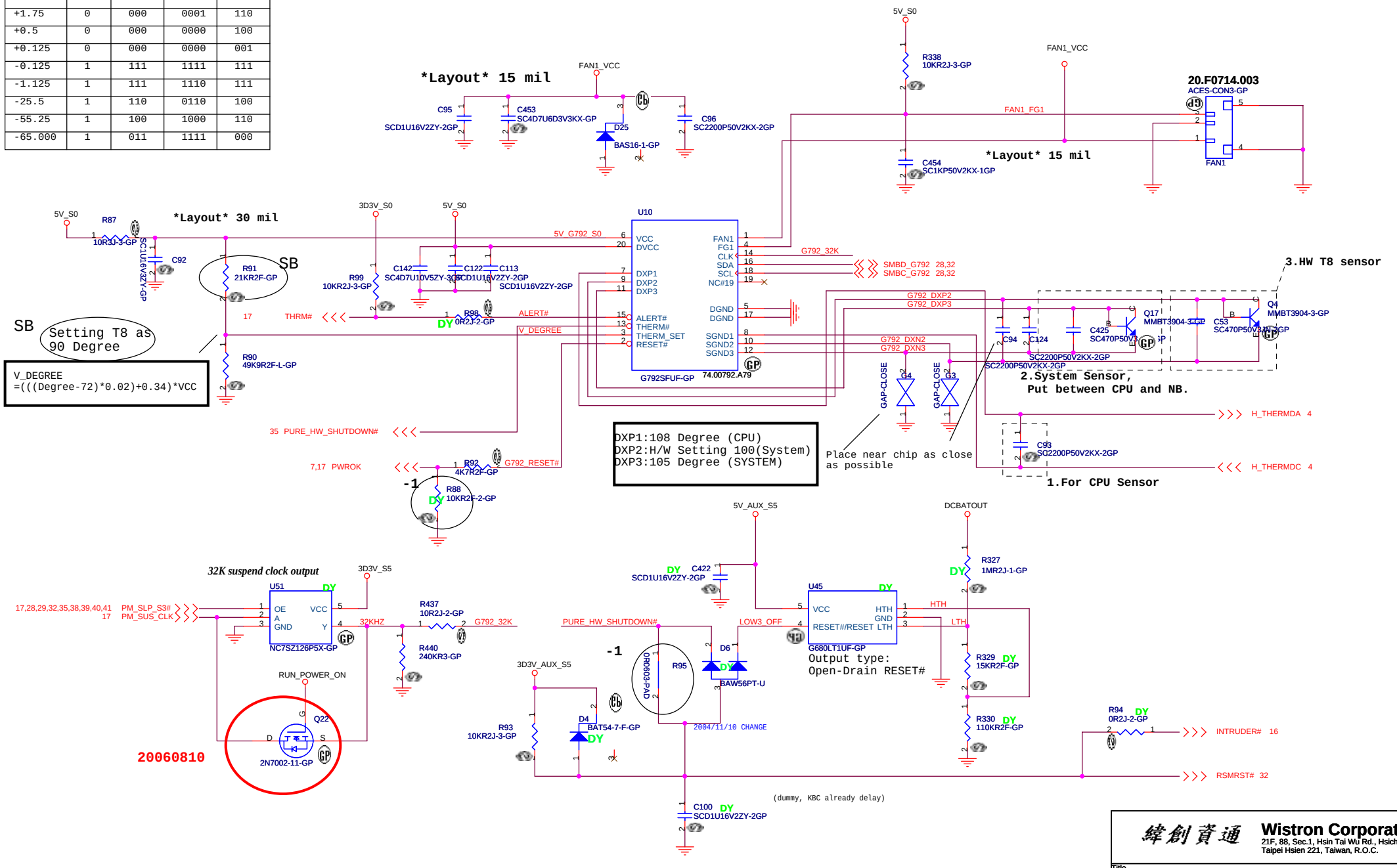
Taipei Hsien 221, Taiwan, R.O.C.

Title	*ICH8-M (4 of 4)*	
Size	Document Number: **Columbia/Tangiz**	Rev: -1
Date: Monday, February 26, 2007	Sheet 19 of 45	

TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



緯創資通 **Wistron Corporation**
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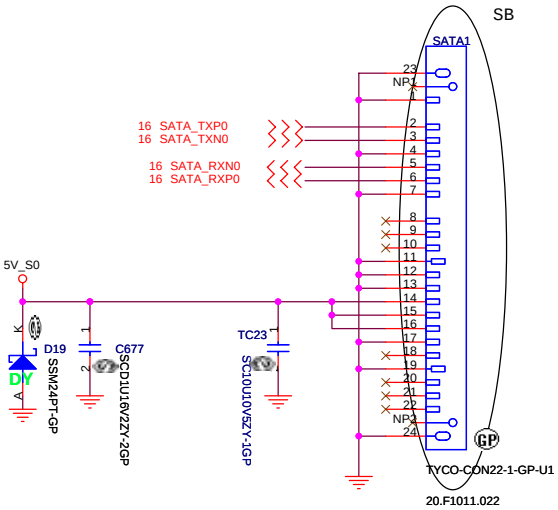
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor***

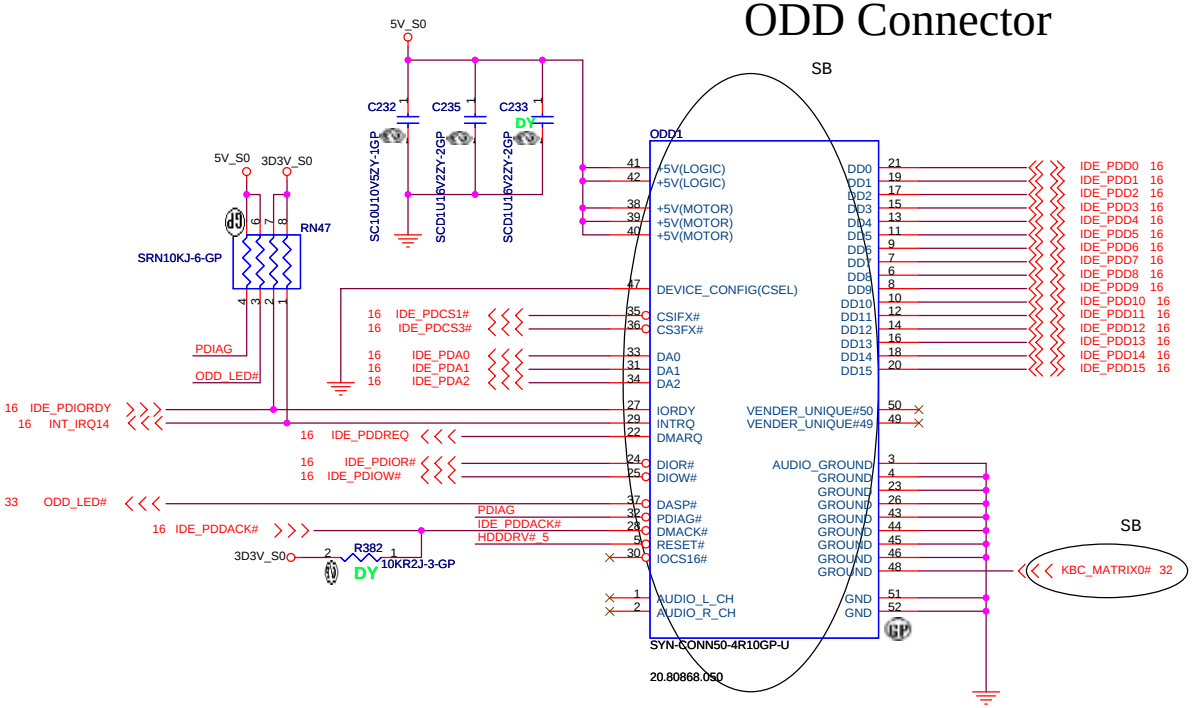
Size	Document Number	Rev
	Columbia/Tangiz	-1

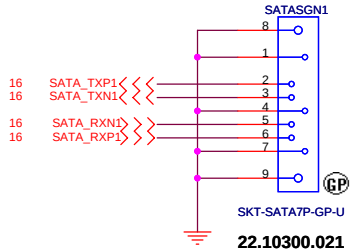
Date: Monday, February 26, 2007 Sheet 20 of 45

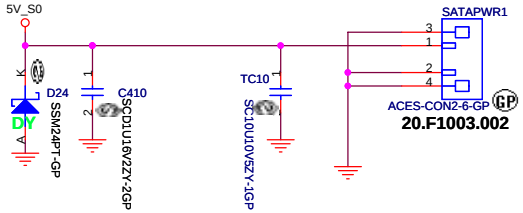
SATA HD Connector

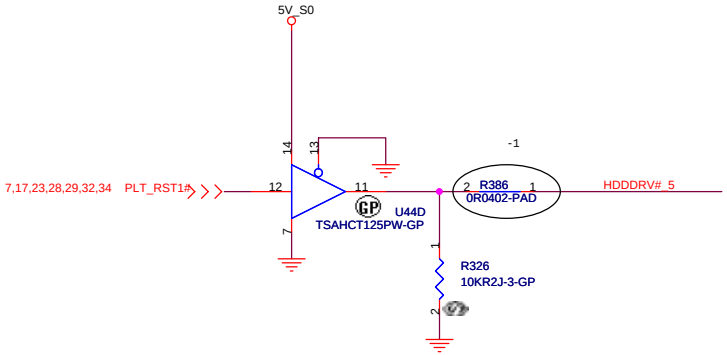


ODD Connector









bom1

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Title: **HDD and CDROM**

Size	Document Number	Rev
	Columbia/Tangiz	-1

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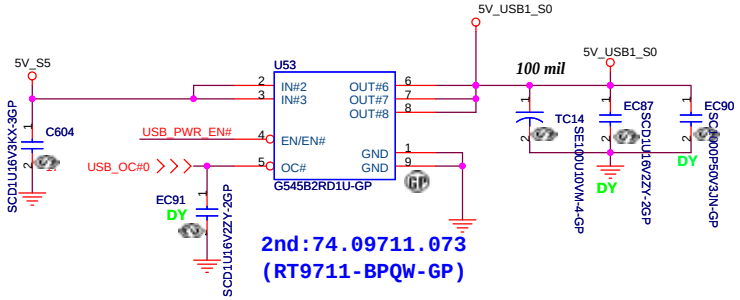
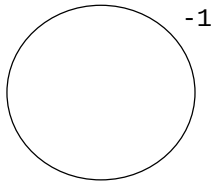
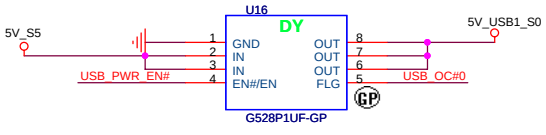
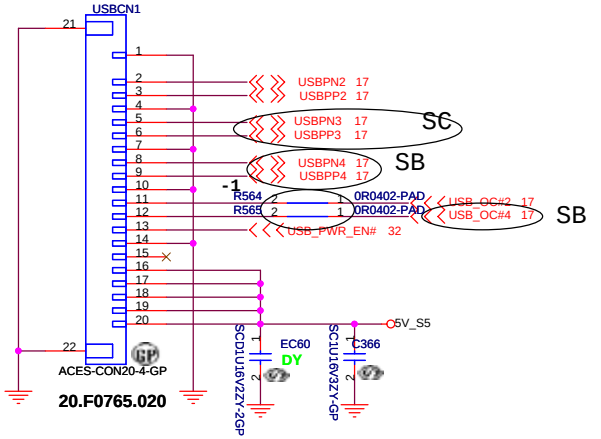


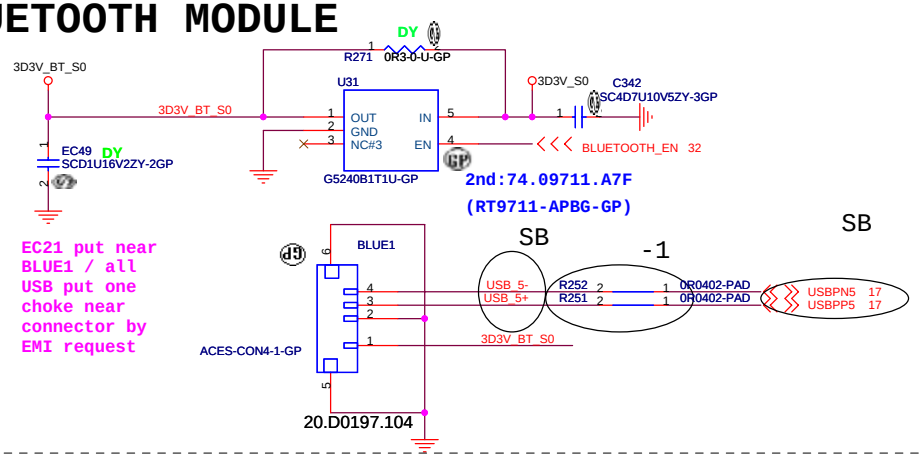




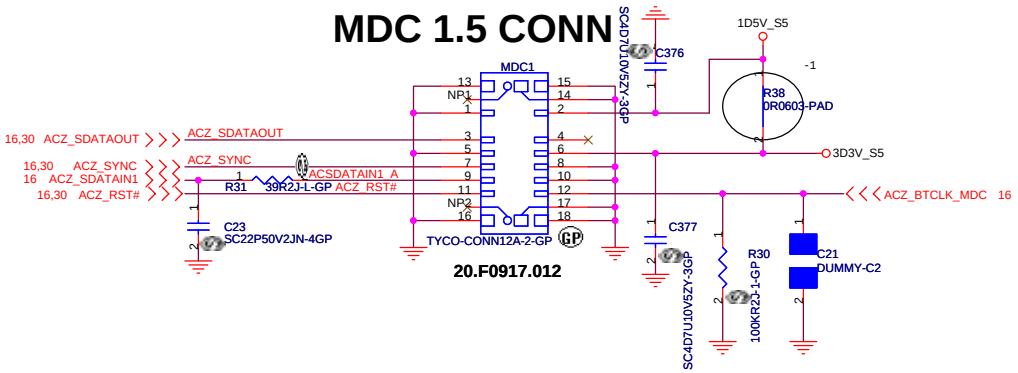
2nd:74.09711.07D
(RT9711-BPS-GP)

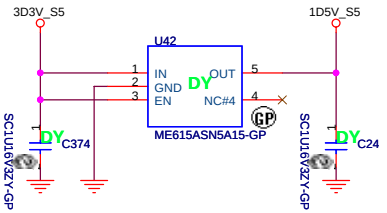


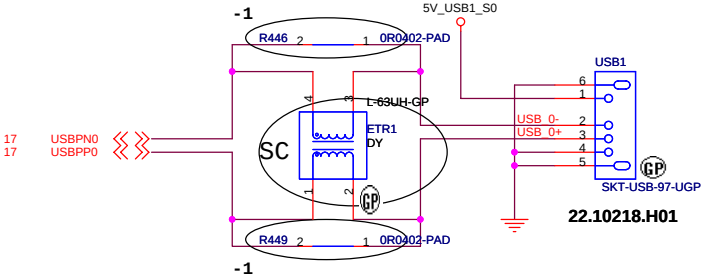
BLUETOOTH MODULE



MDC 1.5 CONN







bom1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: USB / MDC / BLUETOOTH

Size	Document Number	Rev
	Columbia/Tangiz	-1

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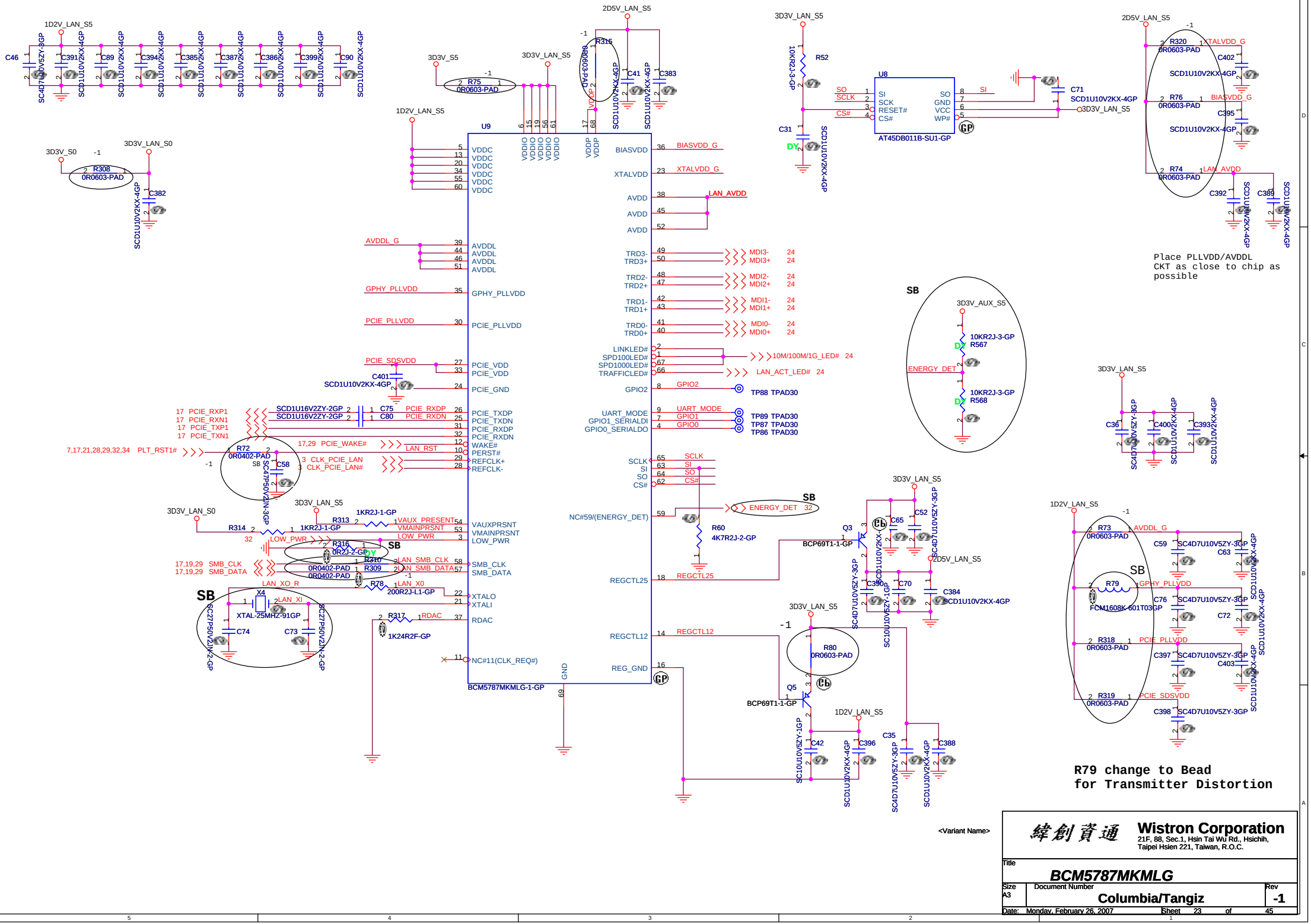
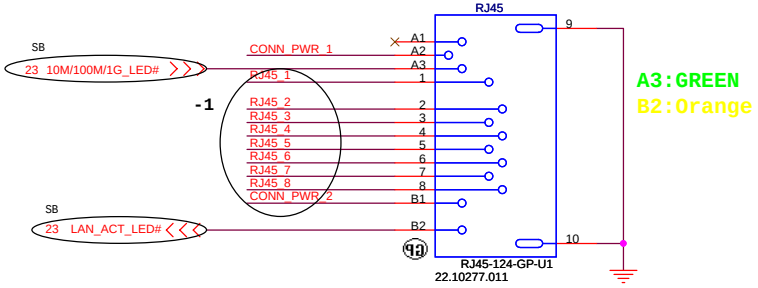
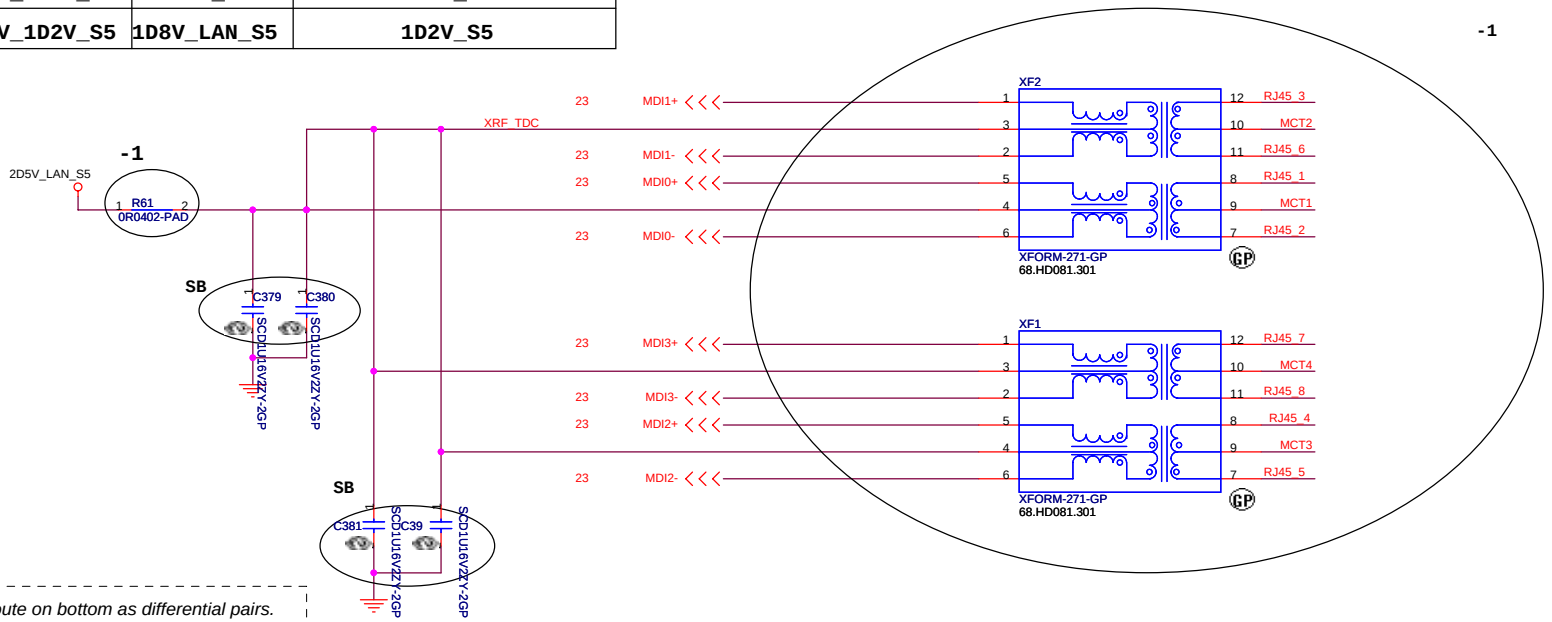

BCM5787MKMLG-1-GP
U9
Place PLLVDD/AVDDL CKT as close to chip as possible
R79 change to Bead for Transmitter Distortion
SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5787MKMLG
Size A3
Document Number
Columbia/Tangiz
Rev -1
Date: Monday, February 26, 2007
Sheet 23 of 45
<Variant Name>

LAN Connector

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

GIGA Lan Transformer





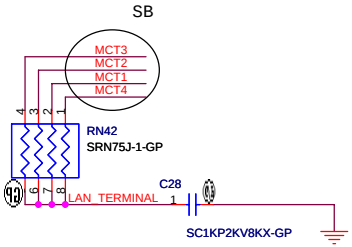
LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

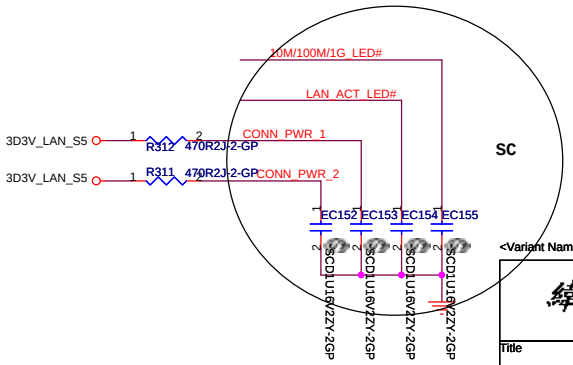
LAN Data: Yellow(B2), when LAN is transfering data.

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers





10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

<Variant Name>

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Title: LAN Connector
Size: A3 | Document Number: Columbia/Tangiz | Rev: -1
Date: Monday, February 26, 2007 | Sheet 24 of 45

C782 should close Pin-P15
and Pin-R17.

TI PCI7412

U54A

1 0F 2

71.07412.B0U

PCI7412ZHK-GP

* All 1394 signals must be routed on top side only
* Differential pairs of each ports should have equal trace length
* Stubs must be keep as short as possible

Bypass/Decupoling Capacitors
Should be places as close to
PCI7412 as possible

<Variant Name>

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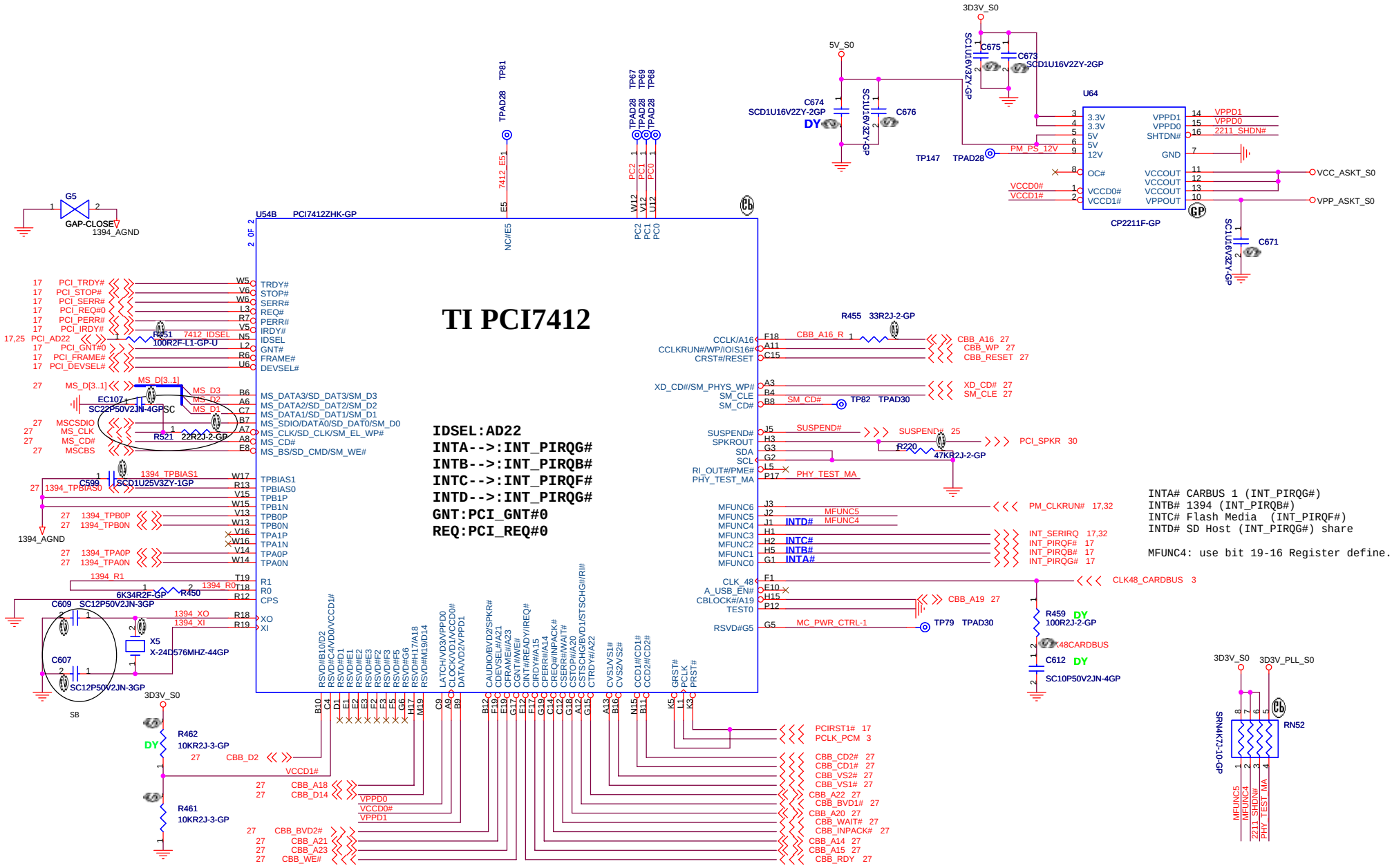
Title: TI PCI7412 (1 of 2)

Size | Document Number: Columbia/Tangiz | Rev: -1

Date: Monday, February 26, 2007 | Sheet 25 of 45



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: TI PCI7412 (2 of 2)

Size | Document Number: Columbia/Tangiz | Rev: -1

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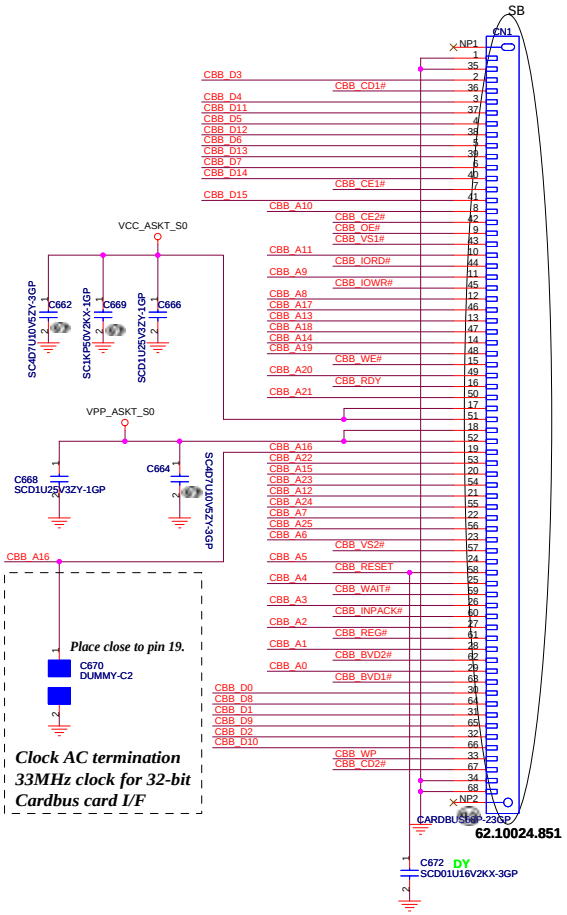
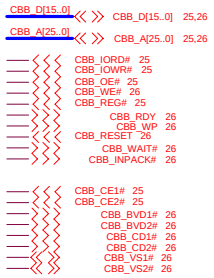
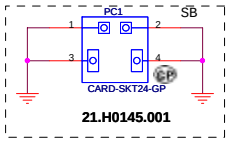
PCMCIA Socket

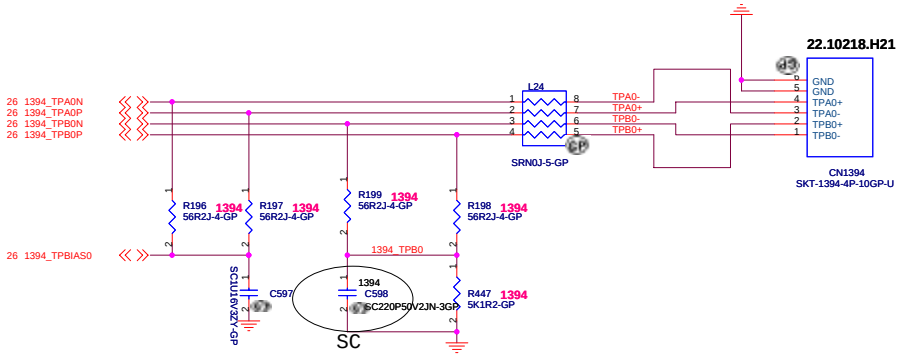


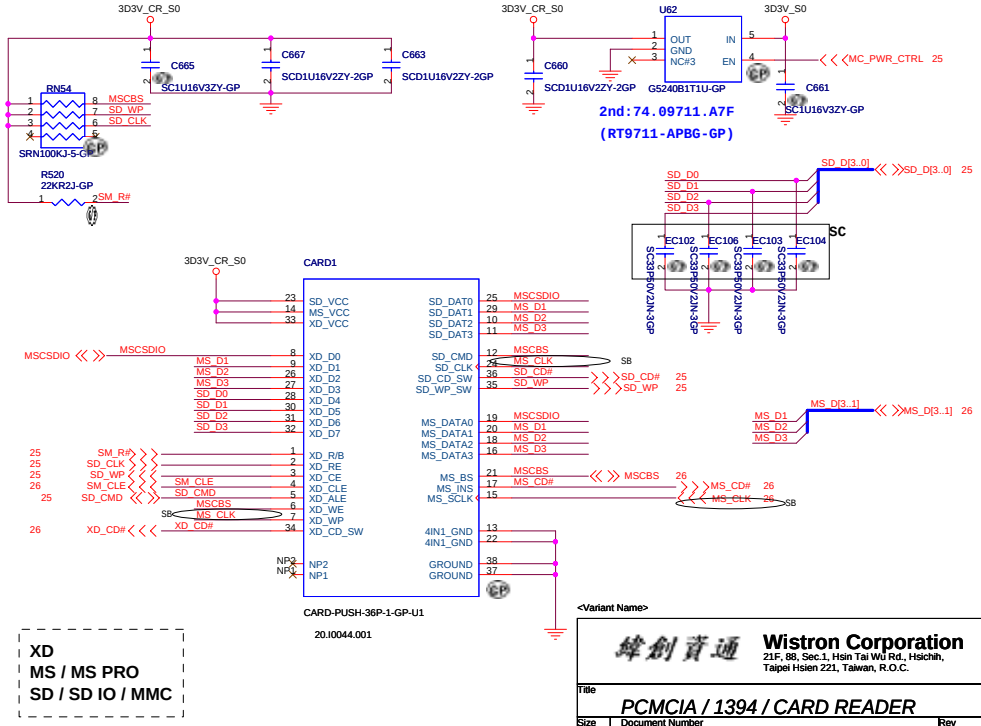
Cardbus I/F





1394 Connector





<variant_name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA / 1394 / CARD READER

Size | Document Number: Columbia/Tangiz | Rev: -1

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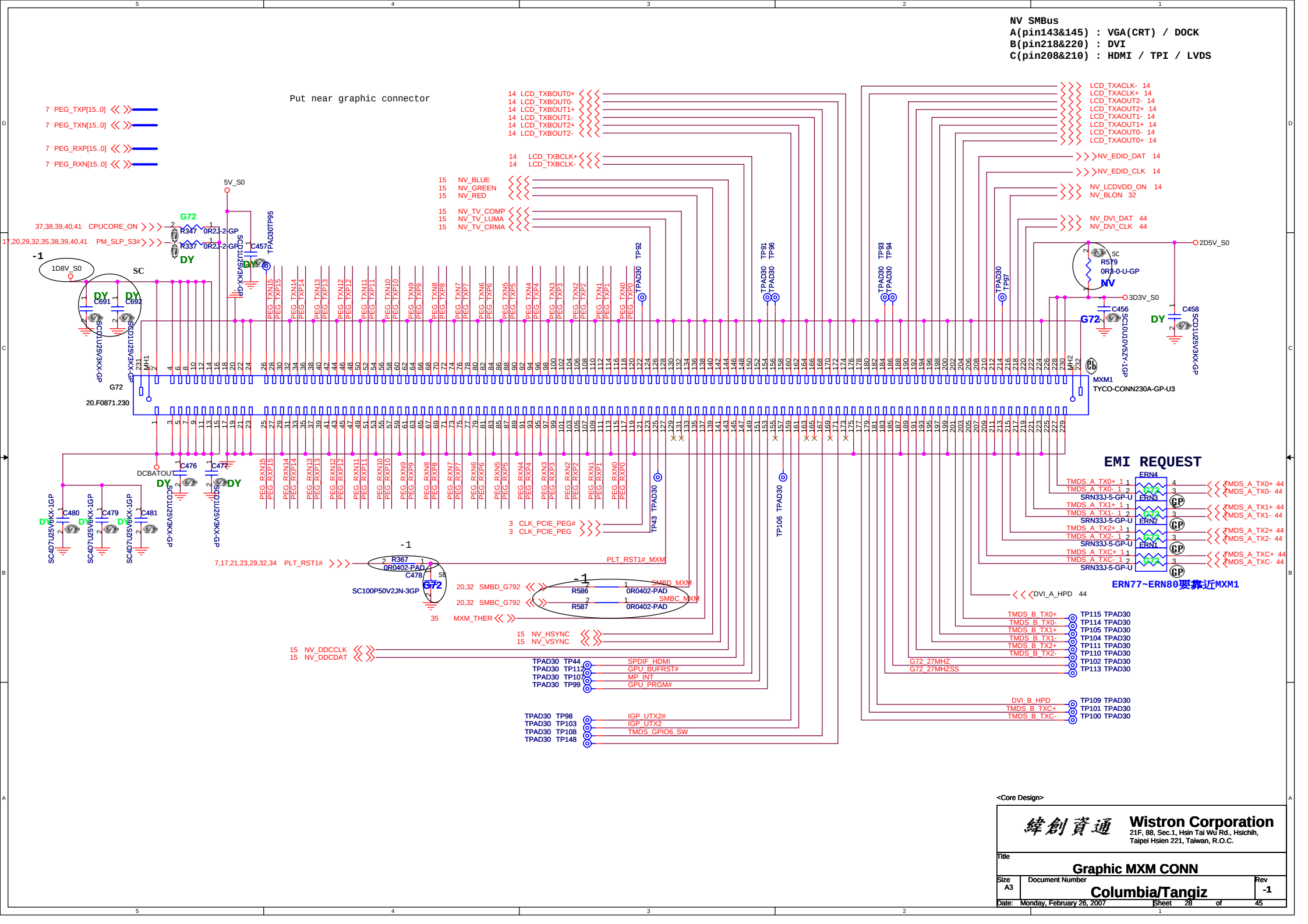

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Graphic MXM CONN

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A3	Columbia/Tangiz	-1

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Mini Card Connector

NEWCARD Connector

SB

SK1
CARDBUS-SKT91-GP

Reserve the symbol for bottom side connector

CARDBUS26P-8GP
NEW1
SB

17 PCIE_TXP3
17 PCIE_TXN3
17 PCIE_RXP3
17 PCIE_RXN3
3 CLK_PCIE_NEW
3 CLK_PCIE_NEW#
CPPE#
NEWCARD_TEST
TP146
3D3V_NEW_S0
EC97
SCD1U10V2KX-4GP
3D3V_NEW_LAN_S5
EC96
17,23 PCIE_WAKE#
1D5V_NEW_S0
R497 0R2J-2-GP
PCIE_WAKE# R
SRN33J-5-GP-U
TPS2231_PERST#
17,19,23 SMB_DATA
17,19,23 SMB_CLK
SMB_DATA_NEW
SMB_CLK_NEW
CONN_TP1
CONN_TP2
TP144
TP145
RN53
CPUTSB#
17 USBPP9
17 USBPN9

62.10024.881

SB

SKT-MINI52P-13-GP
MINIC1
NP1
NP2

3D3V_S0
3D3V_S5
SC
DY R582 0R3-0-U-GP
R583 0R3-0-U-GP
3D3V_S0_MINI
MINI_WAKE#
TP3 TPAD30
1D5V_S0
R39 DY 10KR2J-3-GP
32 WIRELESS_EN
7,17,21,23,28,32,34 PLT_RST1#
CLK_PCIE_MINI1# 3
CLK_PCIE_MINI1 3
E51_RxD 32
E51_TxD 32
PCIE_RXN2 17
PCIE_RXP2 17
PCIE_TXN2 17
PCIE_TXP2 17
17,19,23 SMB_CLK
17,19,23 SMB_DATA
0R2J-2-GP
R13 1D5V_S0
SMB_CLK_MINI
SMB_DATA_MINI
R12
17 USBPN8
17 USBPP8
TP1
LED_WPAN#
TPAD28
WLAN_LED#
14 WLAN_LED#
TP2
TPAD28
5V_AUX_S5_MINI
R563 0R0603-PAD
5V_S5
-1

62.10043.461

2nd:74.00577.073 (G577R9U-GP)

1D5V_NEW_S0
1D5V_S0
3D3V_NEW_LAN_S5
W83L351YG-GP
U61
3D3V_S5
R518 DY 100KR2J-1-GP
R477 DY 100KR2J-1-GP
CPPE#
CPUSB#
TPS2231_PERST#
PERST#
NEW_PLT_RST1#
PM_SLP_S4# 17,32,39,41
SB
-1
7,17,21,23,28,32,34 PLT_RST1#
R516 0R0402-PAD
C658 DY
SC100P50V2JN-3GP
PM_SLP_S3# 17,20,28,32,35,38,39,40,41
3D3V_S0
3D3V_NEW_S0

3D3V_S0
3D3V_S5
SC
R55 0R5J-5-GP
DY R584 0R5J-5-GP
3D3V_S0_MINI
1D5V_S0
TC9 DY
C33 DY
C351
C378
C375 DY
C20 DY
C358
C22 DY
C373
ST220U6D3VDM-13GP
SCD1U10D3V5MX-3GP
SCD1U16V3ZY-GP
SCD1U16V2ZY-2GP

Place near MINIC1

3D3V_S0
C656
SCD1U16V2ZY-2GP

Place them Near to Chip

3D3V_NEW_S0
1D5V_NEW_S0
3D3V_NEW_LAN_S5
C657
C655
C647
C646
C654 SCD1U16V2ZY-2GP
SCD1U16V3ZY-GP
SCD1U16V2ZY-2GP

Place them Near to Connector

bom1

緯創資通 Wistron Corporation
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Title: MINI CARD / NEW CARD
Size:
Document Number: Columbia/Tangiz
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Date: Monday, February 26, 2007
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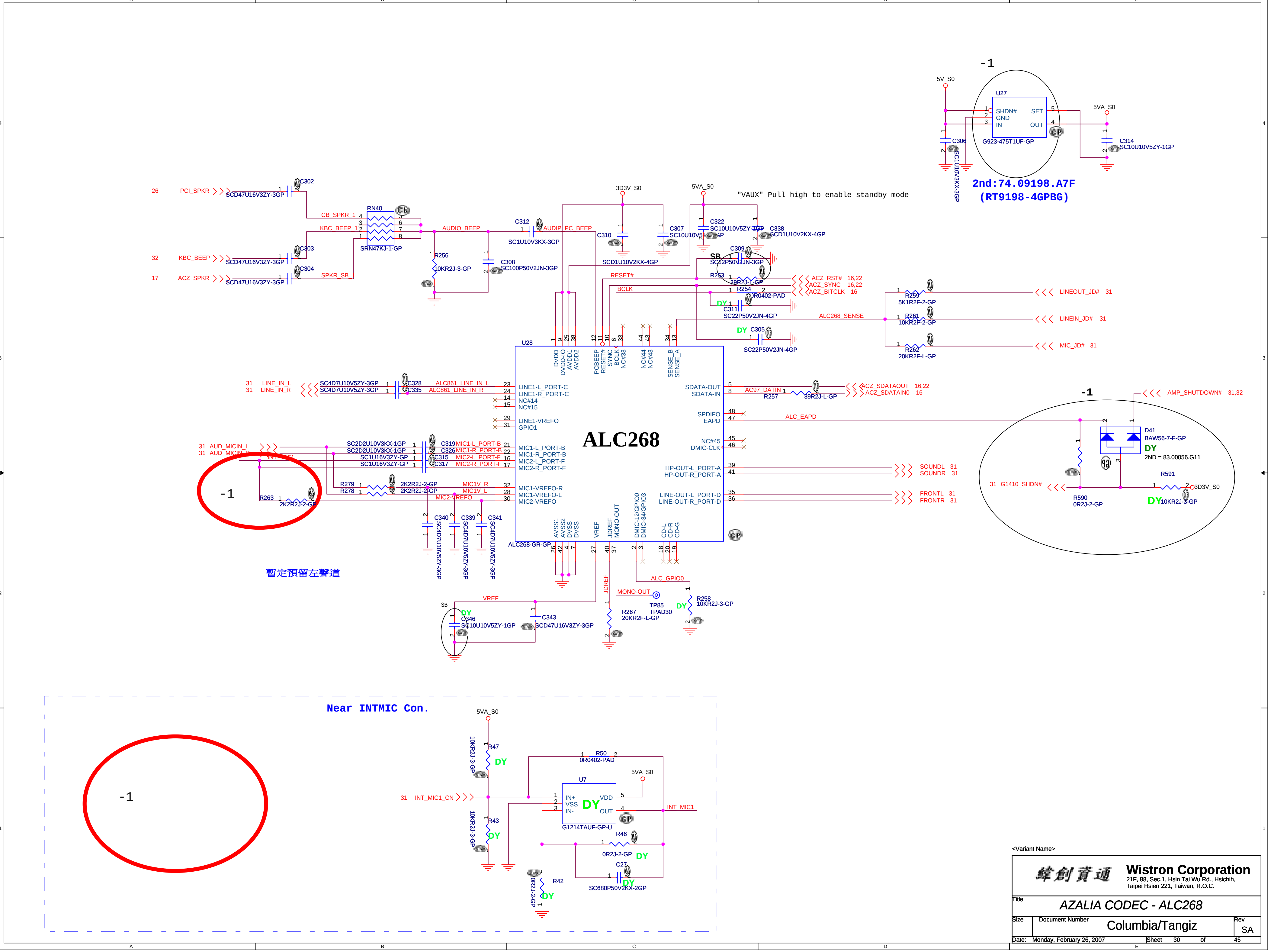

-1
U27
5V_S0
SHDN#
GND
IN
SET
OUT
5VA_S0
C306
SC1U10V3KX-3GP
G923-475T1UF-GP
C314
SC10U10V5ZY-1GP
2nd:74.09198.A7F
(RT9198-4GPBG)
"VAUX" Pull high to enable standby mode
3D3V_S0
5VA_S0
PCI_SPKR
C302
SCD47U16V3ZY-3GP
RN40
CB_SPKR_1
KBC_BEEP_1
SRN47KJ-1-GP
AUDIO_BEEP
C312
AUDIO_PC_BEEP
SC1U10V3KX-3GP
C310
C307
C322
SC10U10V5ZY-1GP
C338
SCD1U10V2KX-4GP
KBC_BEEP
C303
SCD47U16V3ZY-3GP
R256
10KR2J-3-GP
C308
SC100P50V2NJ-3GP
SCD1U10V2KX-4GP
SB
C309
SC12P50V2NJ-3GP
ACZ_SPKR
C304
SPKR_SB_1
RESET#
R253
39R2J-L-GP
ACZ_RST# 16,22
ACZ_SYNC 16,22
ACZ_BITCLK 16
BCLK
R254
0R0402-PAD
DY
C311
SC22P50V2JN-4GP
R259
5K1R2F-2-GP
LINEOUT_JD# 31
ALC268_SENSE
R261
10KR2F-2-GP
LINEIN_JD# 31
DY
C305
SC22P50V2JN-4GP
R262
20KR2F-L-GP
MIC_JD# 31
U28
ALC268
LINE_IN_L
LINE_IN_R
SC4D7U10V5ZY-3GP
C328
C335
ALC861_LINE_IN_L
ALC861_LINE_IN_R
LINE1-L_PORT-C
LINE1-R_PORT-C
NC#14
NC#15
LINE1-VREFO
GPIO1
SDATA-OUT
SDATA-IN
AC97_DATIN
R257
39R2J-L-GP
ACZ_SDATAOUT 16,22
ACZ_SDATAIN0 16
SPDIFO
EAPD
ALC_EAPD
AMP_SHUTDOWN# 31,32
D41
BAW56-7-F-GP
DY
2ND = 83.00056.G11
R591
3D3V_S0
G1410_SHDN#
R590
0R2J-2-GP
10KR2J-3-GP
NC#45
DMIC-CLK
AUD_MICIN_L
AUD_MICIN_R
INT_MIC1
SC2D2U10V3KX-1GP
SC1U16V3ZY-GP
C319
C326
C315
C317
MIC1-L_PORT-B
MIC1-R_PORT-B
MIC2-L_PORT-F
MIC2-R_PORT-F
HP-OUT-L_PORT-A
HP-OUT-R_PORT-A
SOUNDL 31
SOUNDR 31
R279
R278
2K2R2J-2-GP
MIC1V_R
MIC1V_L
MIC2-VREFO
MIC1-VREFO-R
MIC1-VREFO-L
MIC2-VREFO
LINE-OUT-L_PORT-D
LINE-OUT-R_PORT-D
FRONTL 31
FRONTR 31
R263
C340
C339
C341
SC4D7U10V5ZY-3GP
ALC268-GR-GP
暫定預留左聲道
ALC_GPIO0
MONO-OUT
TP85
TPAD30
R258
10KR2J-3-GP
JDREF
R267
20KR2F-L-GP
VREF
C346
SC10U10V5ZY-1GP
C343
SCD47U16V3ZY-3GP
Near INTMIC Con.
R47
10KR2J-3-GP
R50
0R0402-PAD
U7
INT_MIC1_CN
IN+
VSS
IN-
VDD
OUT
G1214TAUF-GP-U
INT_MIC1
R43
R46
0R2J-2-GP
C27
SC680P50V2KX-2GP
R42
0R2J-2-GP
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
AZALIA CODEC - ALC268
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SA
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AUDIO OP AMPLIFIER

R,L 1.5W Speaker
mount R274,R281
R269->63.36334.1DL
R268->63.33334.1DL

R,L 1W Speaker
mount R280,R281
R269->63.15334.1DL
R268->63.12334.1DL

R,L 1.2W Speaker
mount R280,R281
R269->63.10334.1DL
R268->63.68234.1DL

KBC_MUTE_GPIO8

SB:U30 trace modify

LINE IN

Internal Microphone

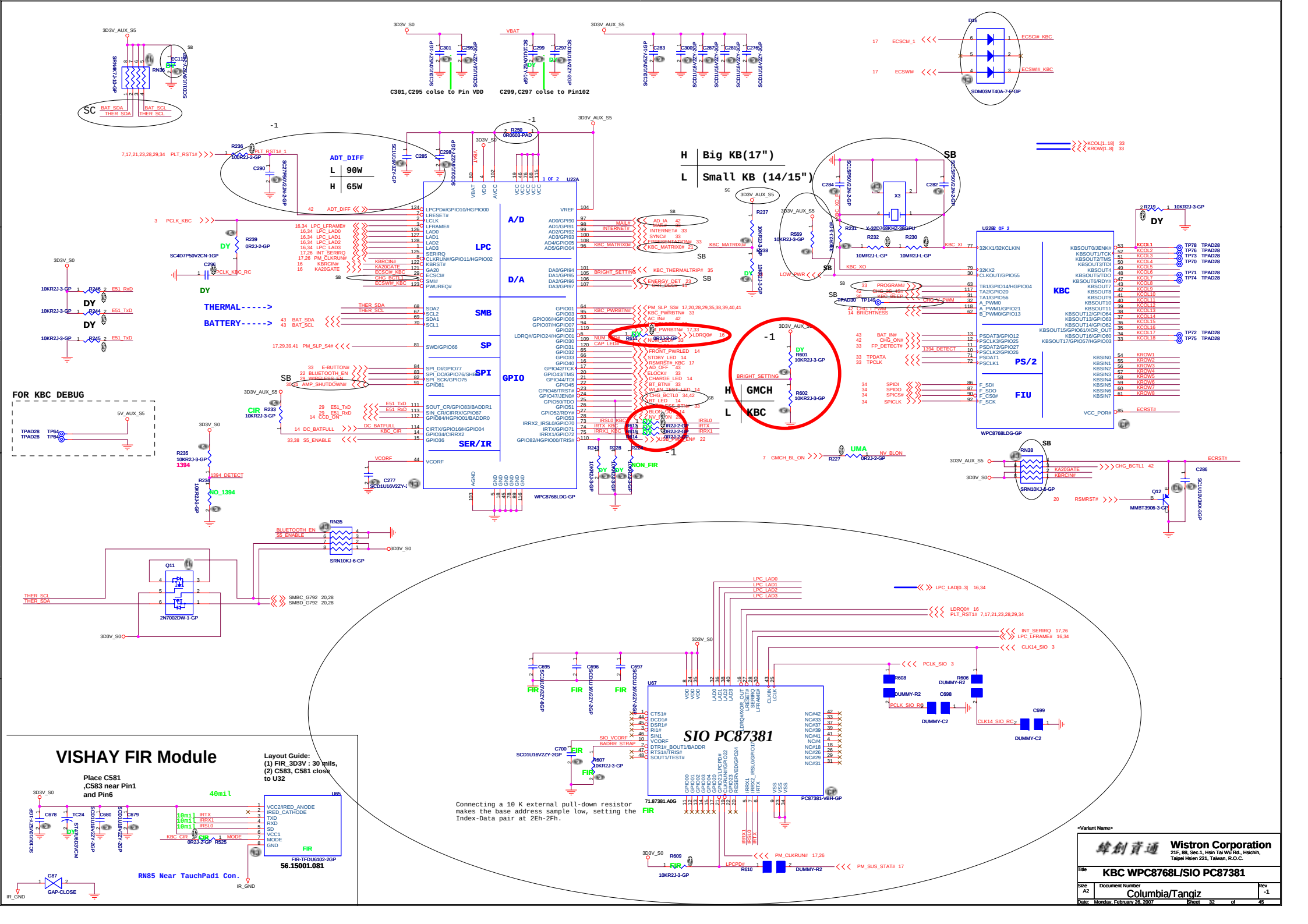
Internal Speaker

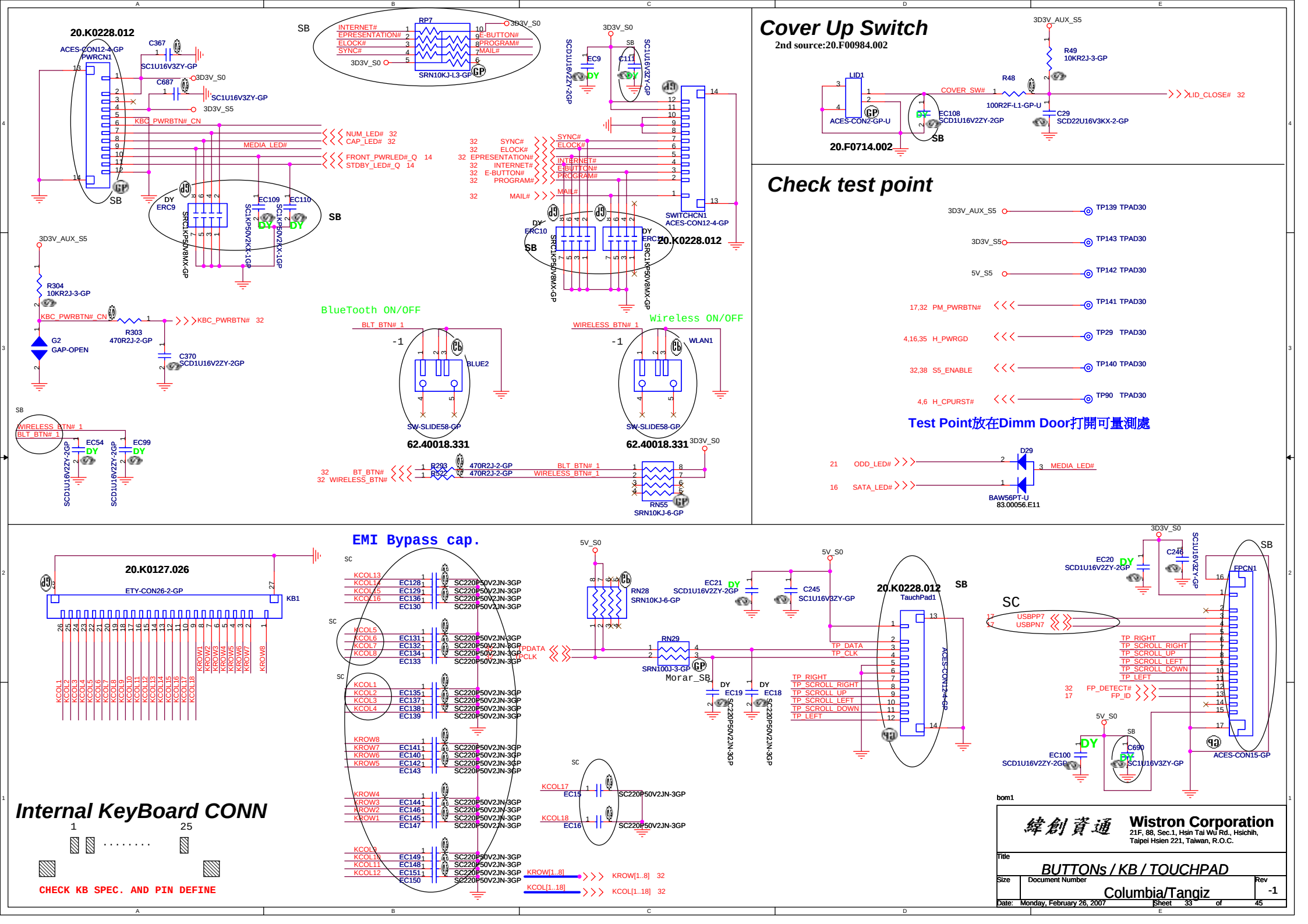
MIC IN

LINE OUT

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP AND JACK
Size: | Document Number: Columbia/Tangiz | Rev: -1
Date: Monday, February 26, 2007 | Sheet 31 of 45


C301,C295 colse to Pin VDD
C299,C297 colse to Pin102
ADT_DIFF
L 90W
H 65W
H Big KB(17")
L Small KB (14/15")
H GMCH
L KBC
THERMAL----->
BATTERY----->
FOR KBC DEBUG
SIO PC87381
Connecting a 10 K external pull-down resistor makes the base address sample low, setting the Index-Data pair at 2Eh-2Fh.
VISHAY FIR Module
Place C581 ,C583 near Pin1 and Pin6
Layout Guide: (1) FIR_3D3V : 30 mils, (2) C583, C581 close to U32
RN85 Near TauchPad1 Con.
FIR-TFDU6102-2GP
56.15001.081
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8768L/SIO PC87381
Columbia/Tangiz
Monday, February 26, 2007


20.K0228.012
ACES-CON12-4-GP
PWRCN1
C367
SC1U16V3ZY-GP
C687
SC1U16V3ZY-GP
3D3V_S0
3D3V_S5
KBC_PWRBTN#_CN
NUM_LED# 32
CAP_LED# 32
MEDIA_LED#
FRONT_PWRLED#_Q 14
STDBY_LED#_Q 14
SB
DY
ERC9
SRC1KP50V8MX-GP
EC109
EC110
SC1KP50V2KX-1GP
SC1KP50V2KX-1GP
3D3V_AUX_S5
R304
10KR2J-3-GP
KBC_PWRBTN#_CN
KBC_PWRBTN# 32
R303
470R2J-2-GP
G2
GAP-OPEN
C370
SCD1U16V2ZY-2GP
WIRELESS_BTN# 1
BLT_BTN# 1
EC54
EC99
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
SB
RP7
INTERNET#
EPRESENTATION#
ELOCK#
SYNC#
3D3V_S0
E-BUTTON#
PROGRAM#
MAIL#
SRN10KJ-L3-GP
SCD1U16V2ZY-2GP
EC9
C111
SC1U16V3ZY-GP
SWITCHCN1
ACES-CON12-4-GP
SYNC#
ELOCK#
EPRESENTATION#
INTERNET#
E-BUTTON#
PROGRAM#
MAIL#
ERC10
ERC11
SRC1KP50V8MX-GP
20.K0228.012
BlueTooth ON/OFF
BLT_BTN# 1
-1
BLUE2
SW-SLIDE58-GP
62.40018.331
Wireless ON/OFF
WIRELESS_BTN# 1
-1
WLAN1
SW-SLIDE58-GP
62.40018.331
3D3V_S0
32 BT_BTN#
32 WIRELESS_BTN#
R293
R522
470R2J-2-GP
470R2J-2-GP
BLT_BTN# 1
WIRELESS_BTN# 1
RN55
SRN10KJ-6-GP
Cover Up Switch
2nd source:20.F00984.002
3D3V_AUX_S5
R49
10KR2J-3-GP
LID1
ACES-CON2-GP-U
COVER_SW#
R48
100R2F-L1-GP-U
LID_CLOSE# 32
EC108
SCD1U16V2ZY-2GP
C29
SCD22U16V3KX-2-GP
20.F0714.002
SB
Check test point
3D3V_AUX_S5
TP139 TPAD30
3D3V_S5
TP143 TPAD30
5V_S5
TP142 TPAD30
17,32 PM_PWRBTN#
TP141 TPAD30
4,16,35 H_PWRGD
TP29 TPAD30
32,38 S5_ENABLE
TP140 TPAD30
4,6 H_CPURST#
TP90 TPAD30
Test Point放在Dimm Door打開可量測處
21 ODD_LED#
16 SATA_LED#
D29
MEDIA_LED#
BAW56PT-U
83.00056.E11
20.K0127.026
ETY-CON26-2-GP
KB1
KROW1
KROW2
KROW3
KROW4
KROW5
KROW6
KROW7
KROW8
KCOL1
KCOL2
KCOL3
KCOL4
KCOL5
KCOL6
KCOL7
KCOL8
KCOL9
KCOL10
KCOL11
KCOL12
KCOL13
KCOL14
KCOL15
KCOL16
KCOL17
KCOL18
Internal KeyBoard CONN
1
25
CHECK KB SPEC. AND PIN DEFINE
EMI Bypass cap.
SC
SC220P50V2JN-3GP
5V_S0
RN28
SRN10KJ-6-GP
RN29
SRN100J-3-GP
Morar_SB
EC21
SCD1U16V2ZY-2GP
C245
SC1U16V3ZY-GP
EC19
EC18
SC220P50V2JN-3GP
SC220P50V2JN-3GP
20.K0228.012
TauchPad1
SB
TP_DATA
TP_CLK
TP_RIGHT
TP_SCROLL_RIGHT
TP_SCROLL_UP
TP_SCROLL_LEFT
TP_SCROLL_DOWN
TP_LEFT
ACES-CON12-4-GP
3D3V_S0
EC20
SCD1U16V2ZY-2GP
C246
SC1U16V2ZY-GP
FPCN1
USBPP7
USBPN7
FP_DETECT#
FP_ID
EC100
SCD1U16V2ZY-2GP
C690
SC1U16V3ZY-GP
ACES-CON15-GP
KROW[1..8] 32
KCOL[1..18] 32
bom1
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BUTTONs / KB / TOUCHPAD
Size
Document Number
Columbia/Tangiz
Rev
-1
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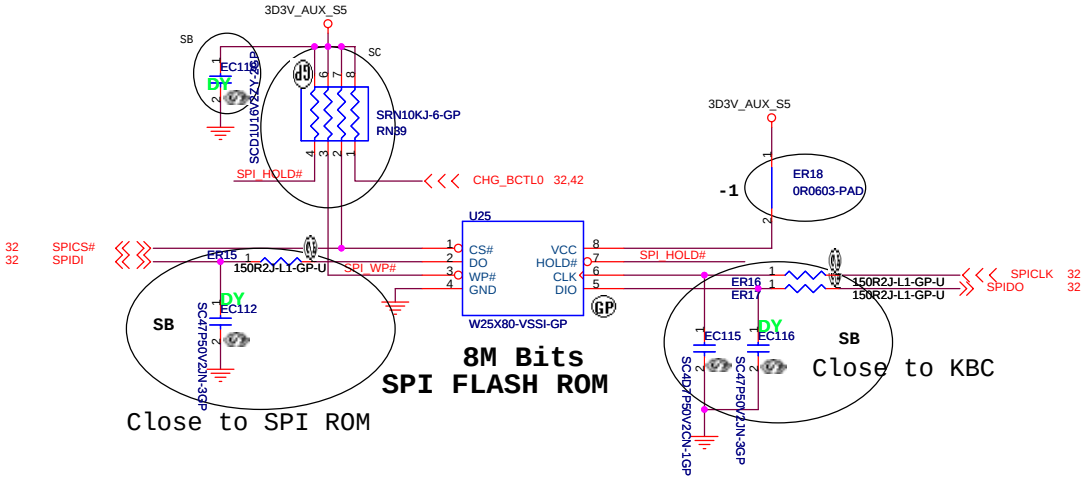
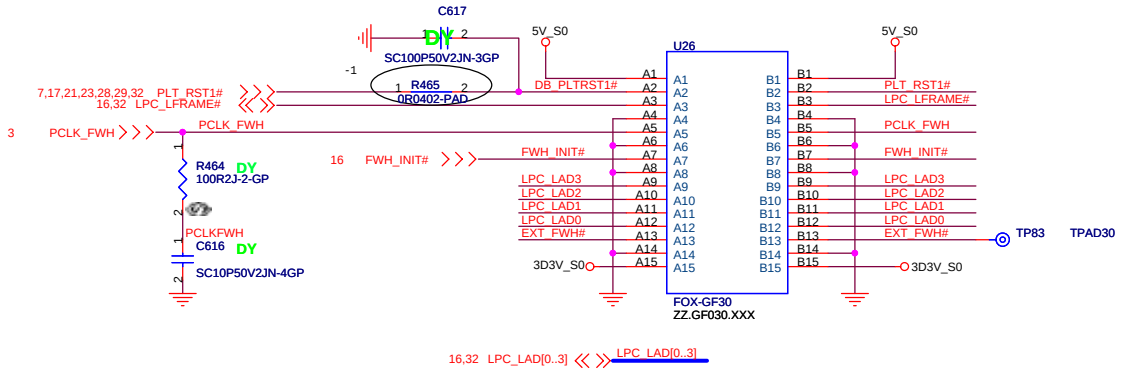


GOLDEN FINGER FOR DEBUG BOARD



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS		
Size: A3	Document Number: Columbia/Tangiz	Rev: -1
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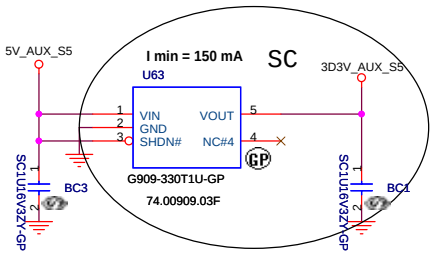
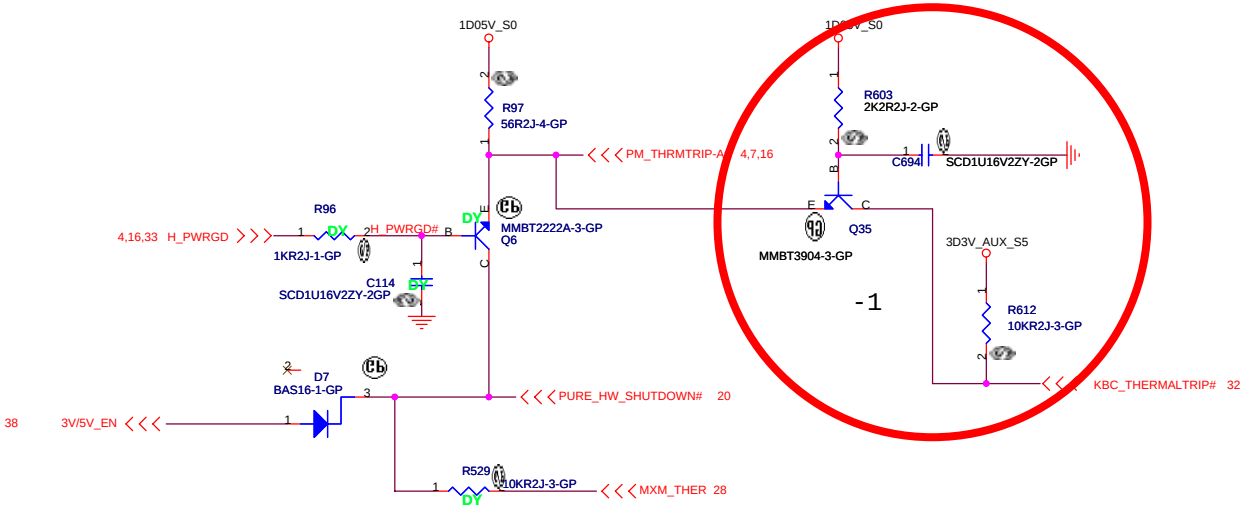
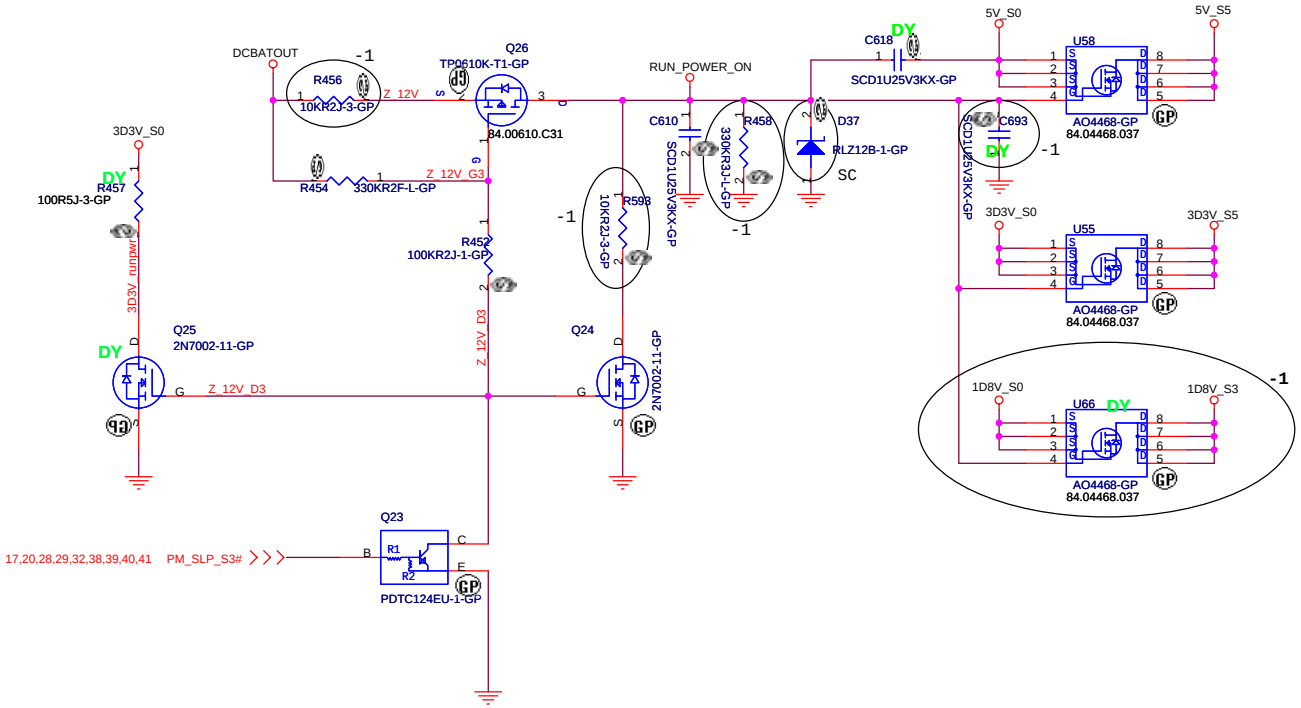
Aux Power 3D3V_AUX_S5





Run Power



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RUN POWER and 3D3V_AUX_S5	
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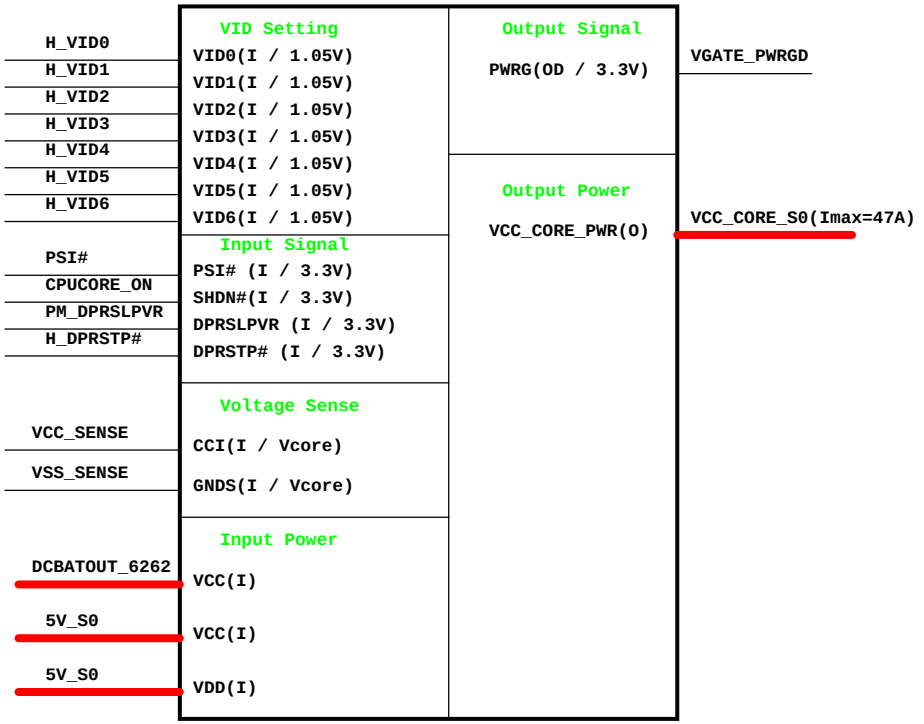
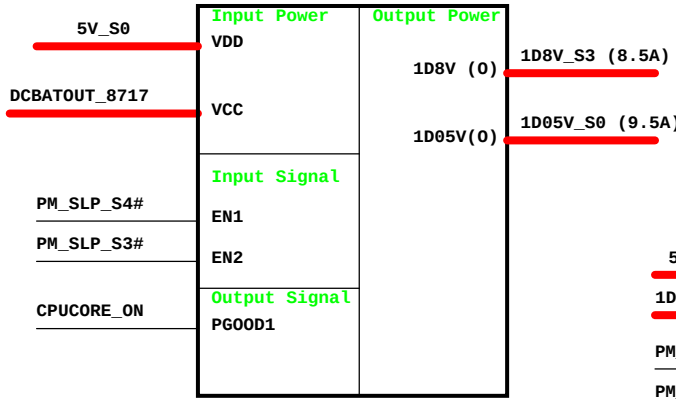
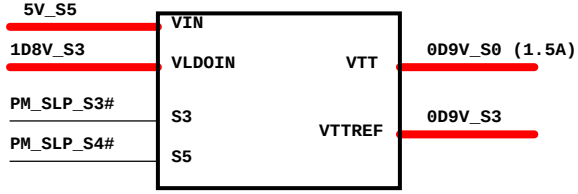
CPU_CORE
MAX8770



MAX8717
1D8V/1D05V

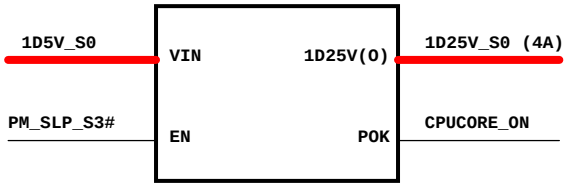


0D9V_S0



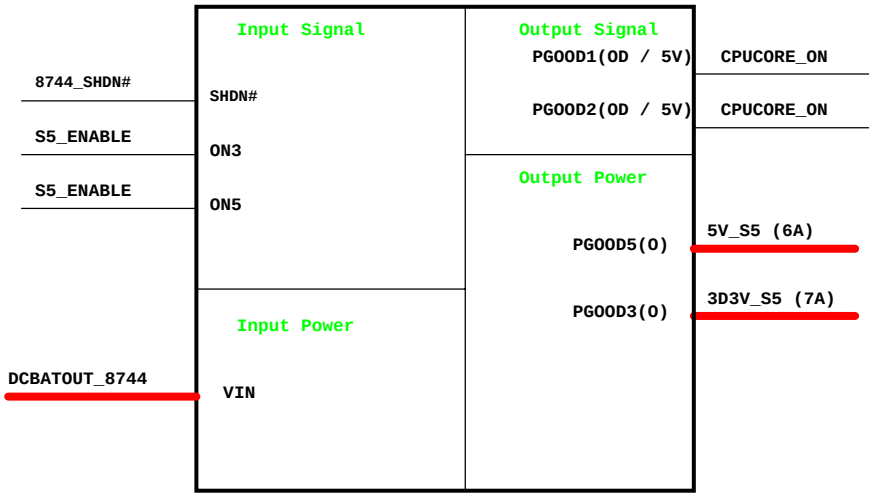
TPS51100

1D25V_S0

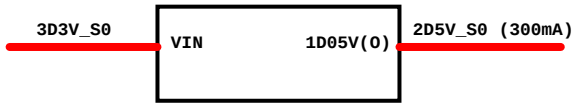


APL5915

MAX8744
5V/3D3V

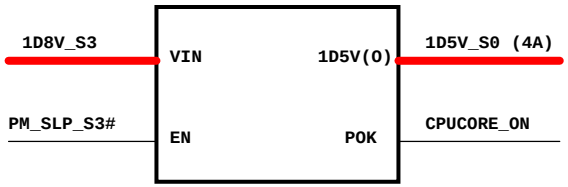


2D5V_S0



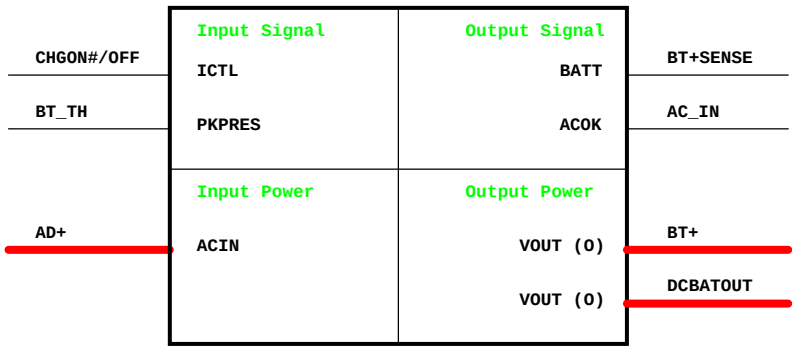
APL5308

1D5V_S0



APL5912

Charger ISL6255



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

Size	Document Number	Rev
A3	Columbia/Tangiz	-1

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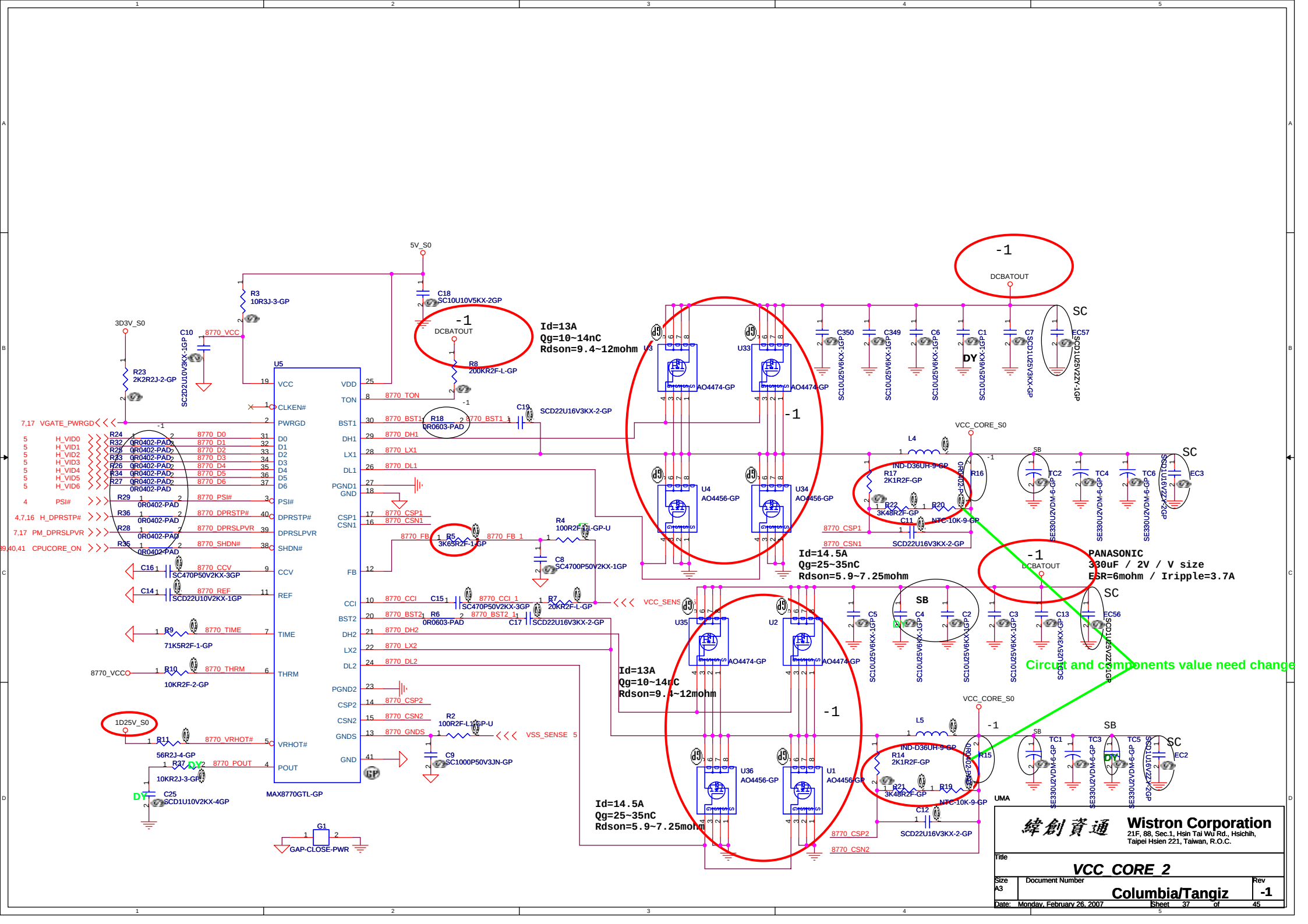
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
PANASONIC
330uF / 2V / V size
ESR=6mohm / Iripple=3.7A
Circuit and components value need change
MAX8770GTL-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
VCC_CORE_2
Columbia/Tangiz
Size A3
Rev -1
Date: Monday, February 26, 2007
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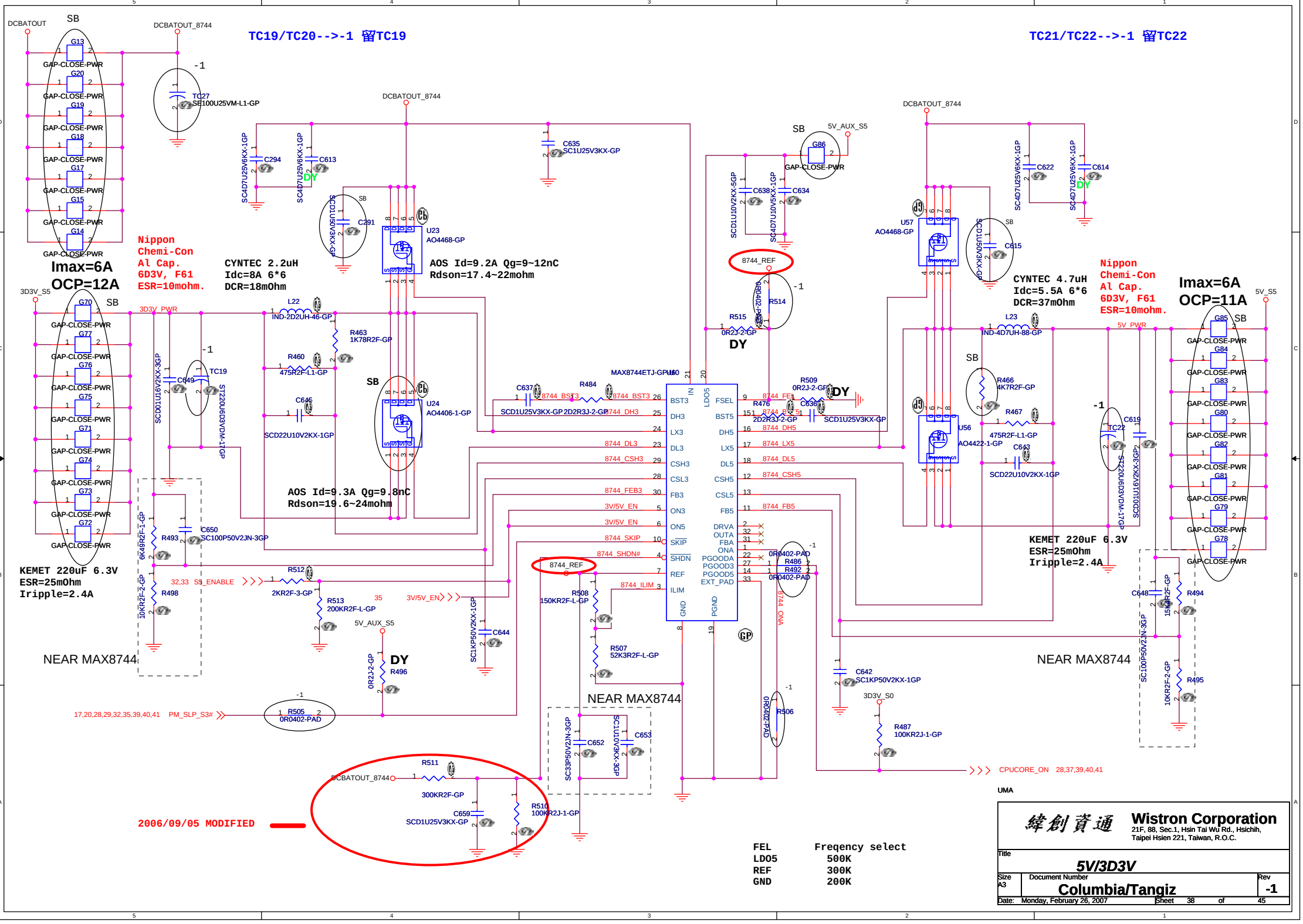
TC19/TC20-->-1 留TC19
TC21/TC22-->-1 留TC22
Imax=6A
OCP=12A
Nippon Chemi-Con Al Cap. 6D3V, F61 ESR=10mohm.
CYNTEC 2.2uH Idc=8A 6*6 DCR=18mOhm
AOS Id=9.2A Qg=9~12nC Rdson=17.4~22mohm
AOS Id=9.3A Qg=9.8nC Rdson=19.6~24mohm
KEMET 220uF 6.3V ESR=25mOhm Iripple=2.4A
NEAR MAX8744
CYNTEC 4.7uH Idc=5.5A 6*6 DCR=37mOhm
Imax=6A
OCP=11A
Nippon Chemi-Con Al Cap. 6D3V, F61 ESR=10mohm.
KEMET 220uF 6.3V ESR=25mOhm Iripple=2.4A
NEAR MAX8744
2006/09/05 MODIFIED
FEL Freqency select
LDO5 500K
REF 300K
GND 200K
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
5V/3D3V
Size A3
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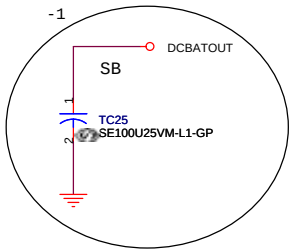
TC15/TC16-->-1 留TC15

TC17/TC18-->-1 留TC17



1D05V Iomax=12A
OCP>19A

Vcal.=1.0511V

CYNTEC 1uH
Idc=11A,Isat=22A
DCR=9mOhm

Rs2 = L / DCR / Cs2

Vout=(1+Ra/Rb)*1

Panasonic 330uF
2.5V ESR=15mOhm
Iripple=3.1A

Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=10mohm

Id=13A
Qg=10~14nC,
Rdson=9.4~12mohm

Id=14.5A
Qg=25~35nC,
Rdson=13.5~16.5mohm

Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm

Id=9.6A
Qg=18nC,
Rdson=13.5~16.5mohm

2006.0928 add

1D8V Iomax=9.5A
OCP>17A

Vcal.=1.8V

CYNTEC 2.2uH
Irms=14A Isat=16A
DCR=5.8~7mOhm

Rs1 = L / DCR / Cs1

Panasonic 220uF
2.5V ESR=25mOhm
Iripple=1.8A

Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=10mohm

Vout=[1+(Rc/Rd)]*1

SKIP
VCC=Force PWM
REF=Low noise
GND=Pulse Skipping

FSET
GND f = 200KHz
REF f = 300KHz
VCC f = 500KHz

Adjust the current limit threshold from R14, R15

VILIM = 0.5V~2.0V

Output Current =
ILIM / 10 / LDCR - dI/2

MAX8717ETI-T-GP

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MAX8717 1D8V 1D05V

Size: A3 | Document Number: Columbia/Tangiz | Rev: -1

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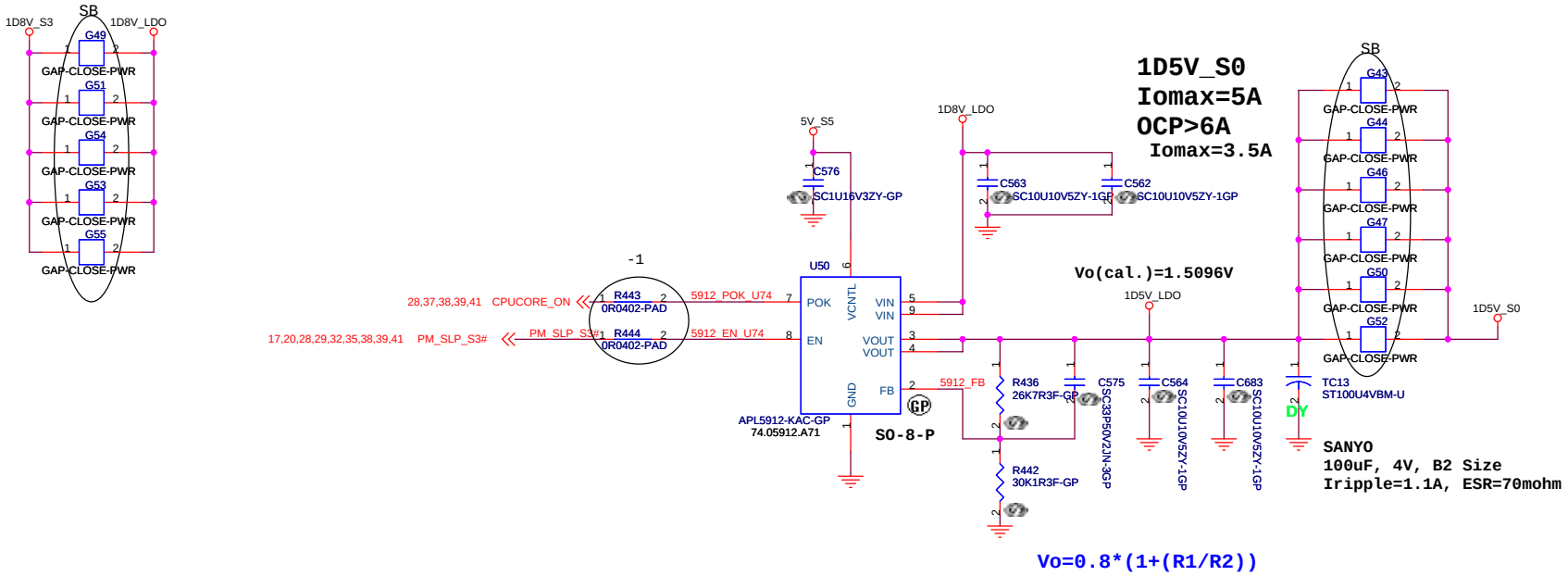

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***APW5912_1D5V***	
Size	Document Number **Columbia/Tangiz**	Rev -1
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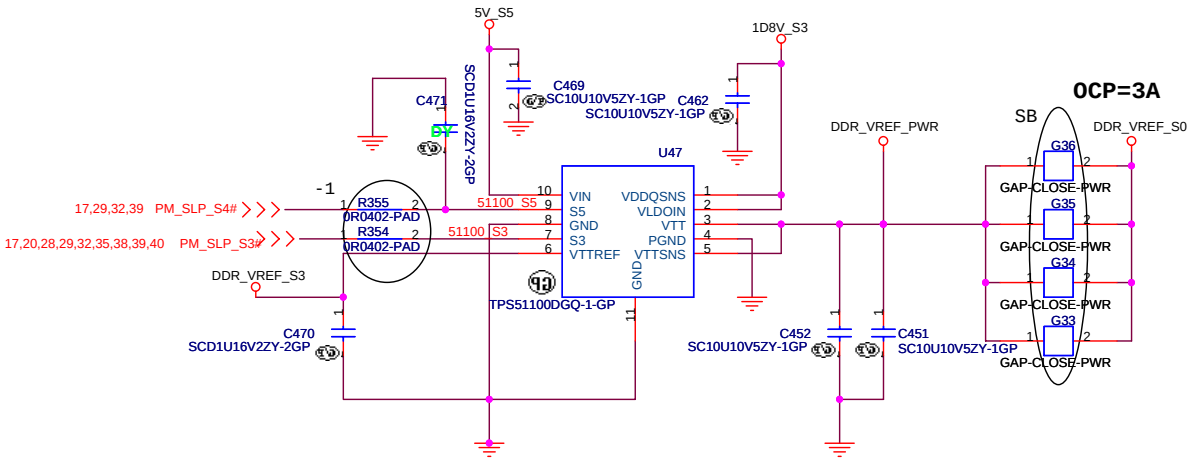
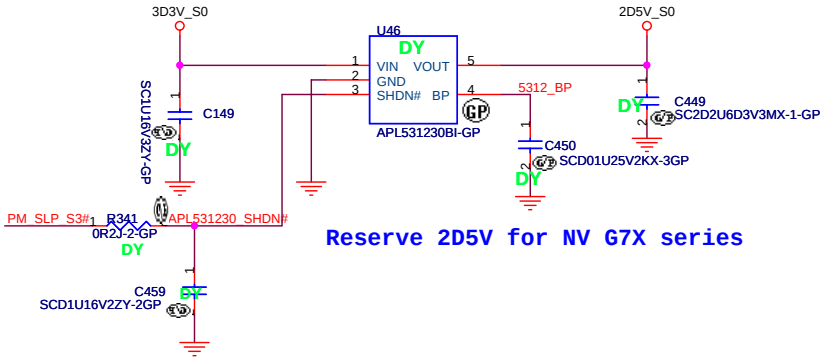
0D9V_S3
Iomax=1.2A

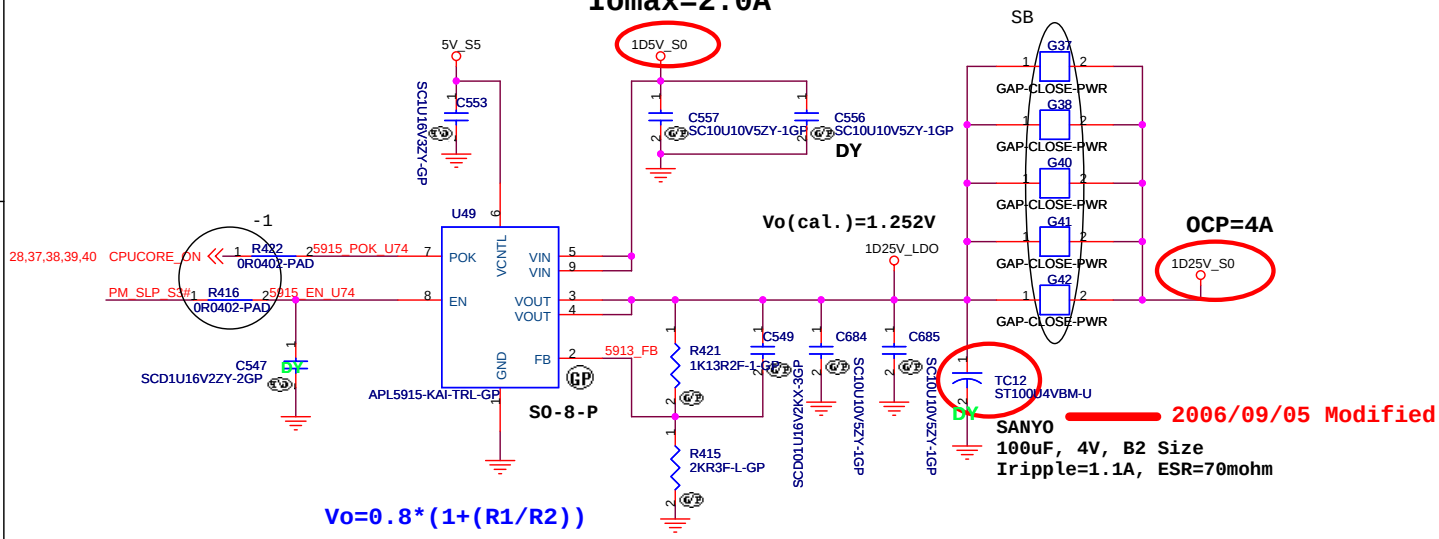


2D5V
Iomax=130mA



Reserve 2D5V for NV G7X series

1D25V_S0
Iomax=2.0A



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 1D25V/2D5V//1D05V/0D9V		
Size: B	Document Number: Columbia/Tangiz	Rev: -1
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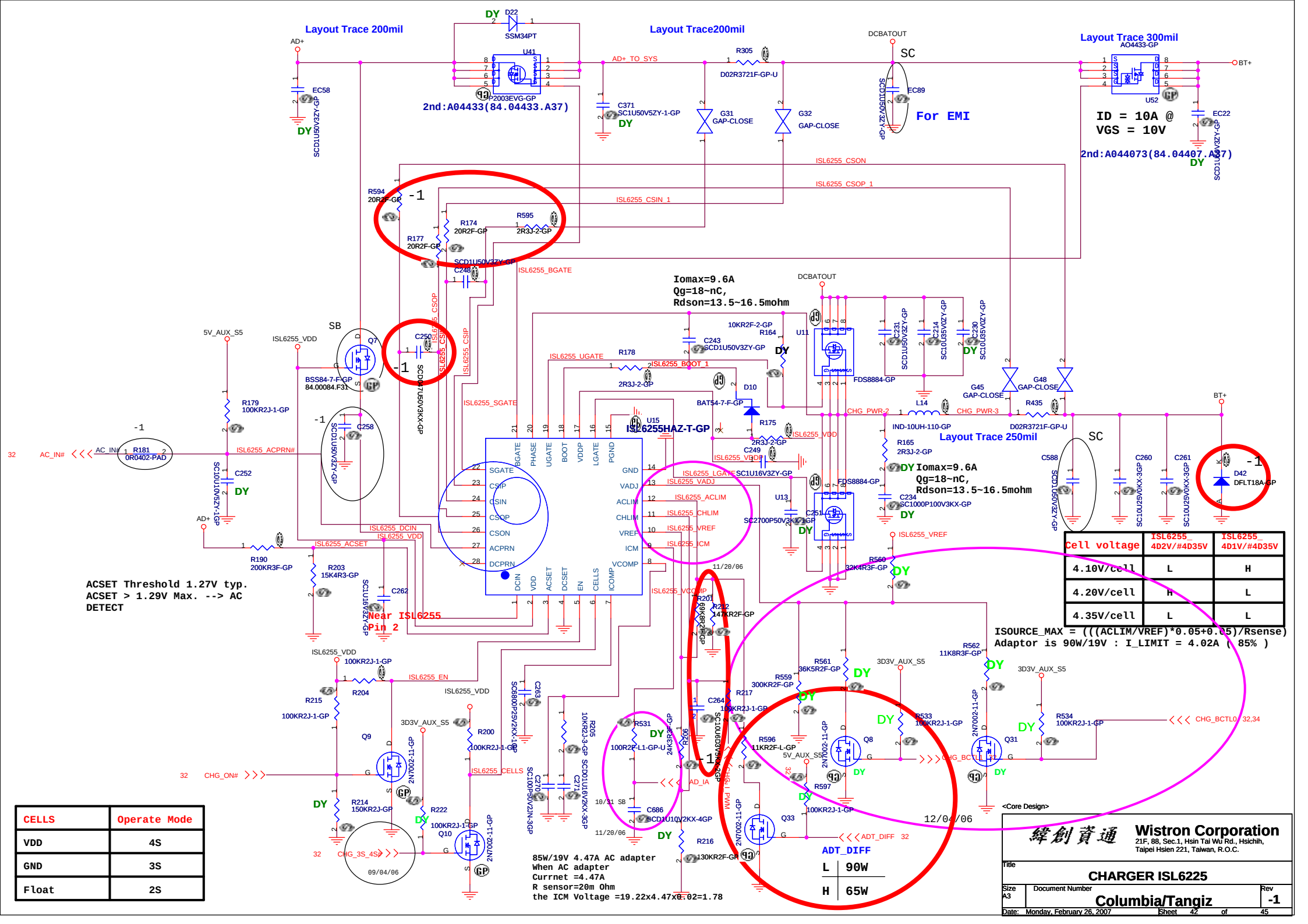
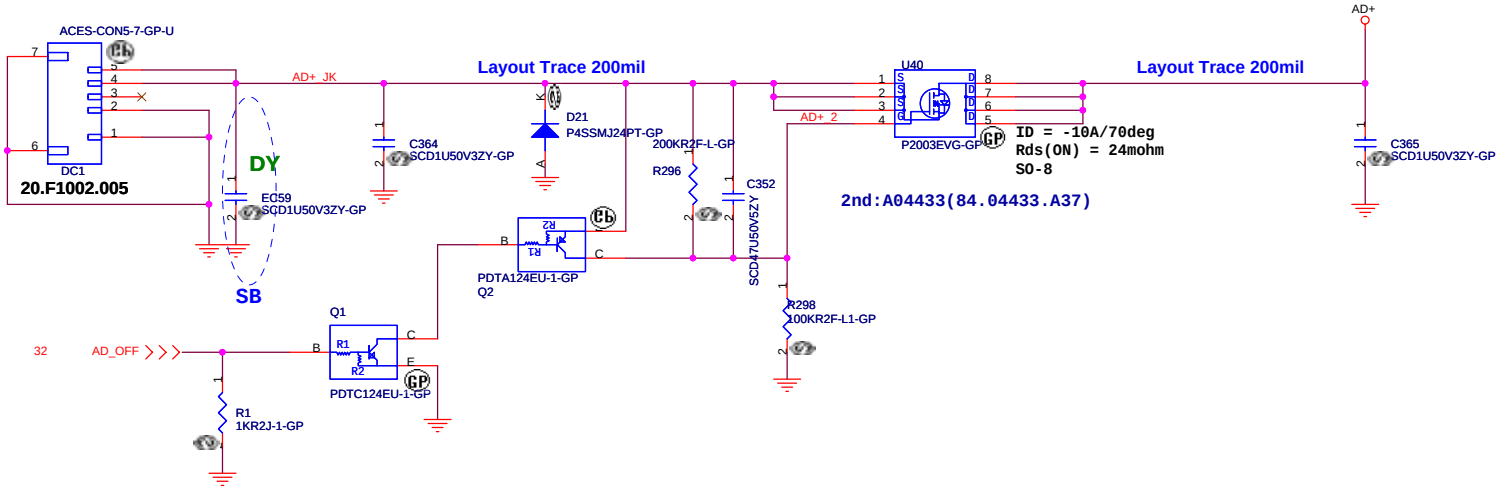


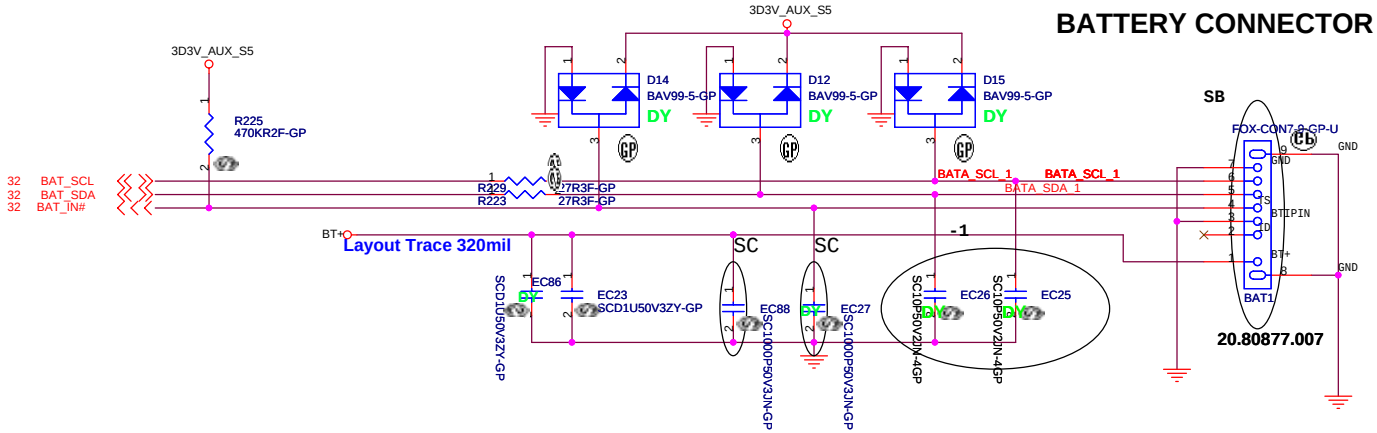
Cell voltage	ISL6255_4D2V/#4D35V	ISL6255_4D1V/#4D35V
4.10V/cell	L	H
4.20V/cell	H	L
4.35V/cell	L	L

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Variant Name>

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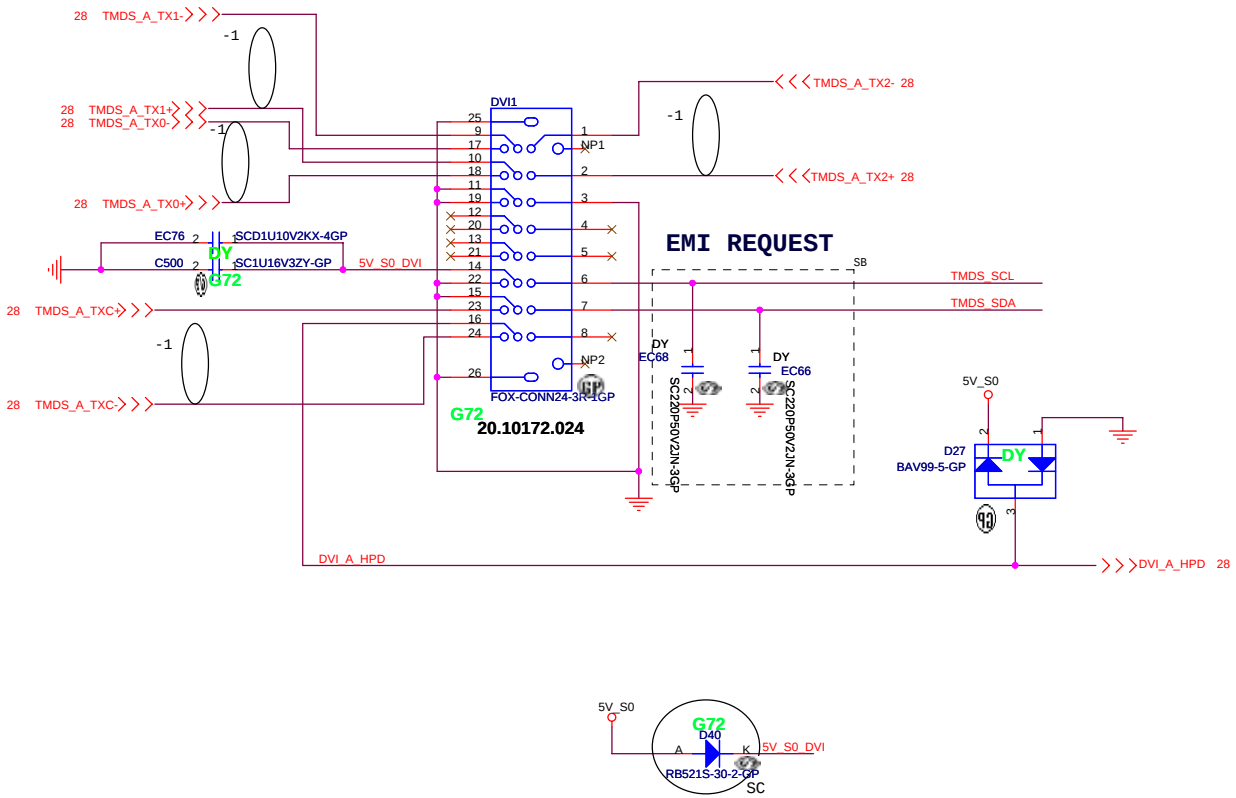

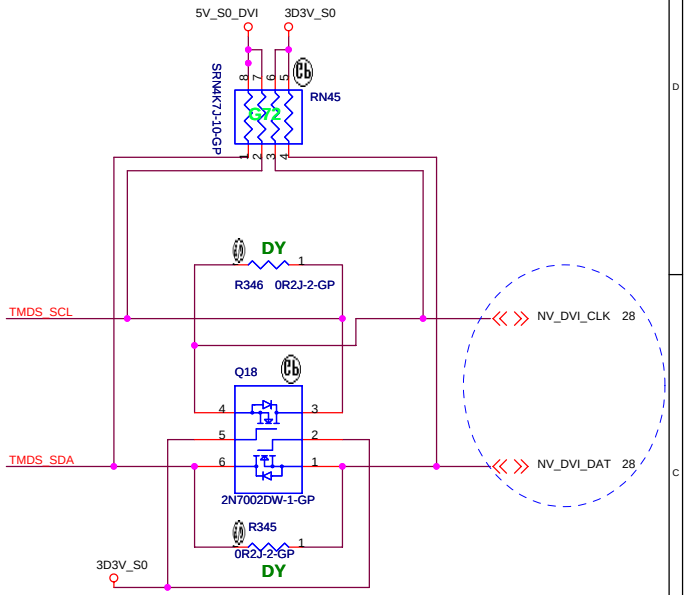

<Variant Name>

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Title: DVI CONNECTOR		
Size: A3	Document Number: Columbia/Tangiz	Rev: -1
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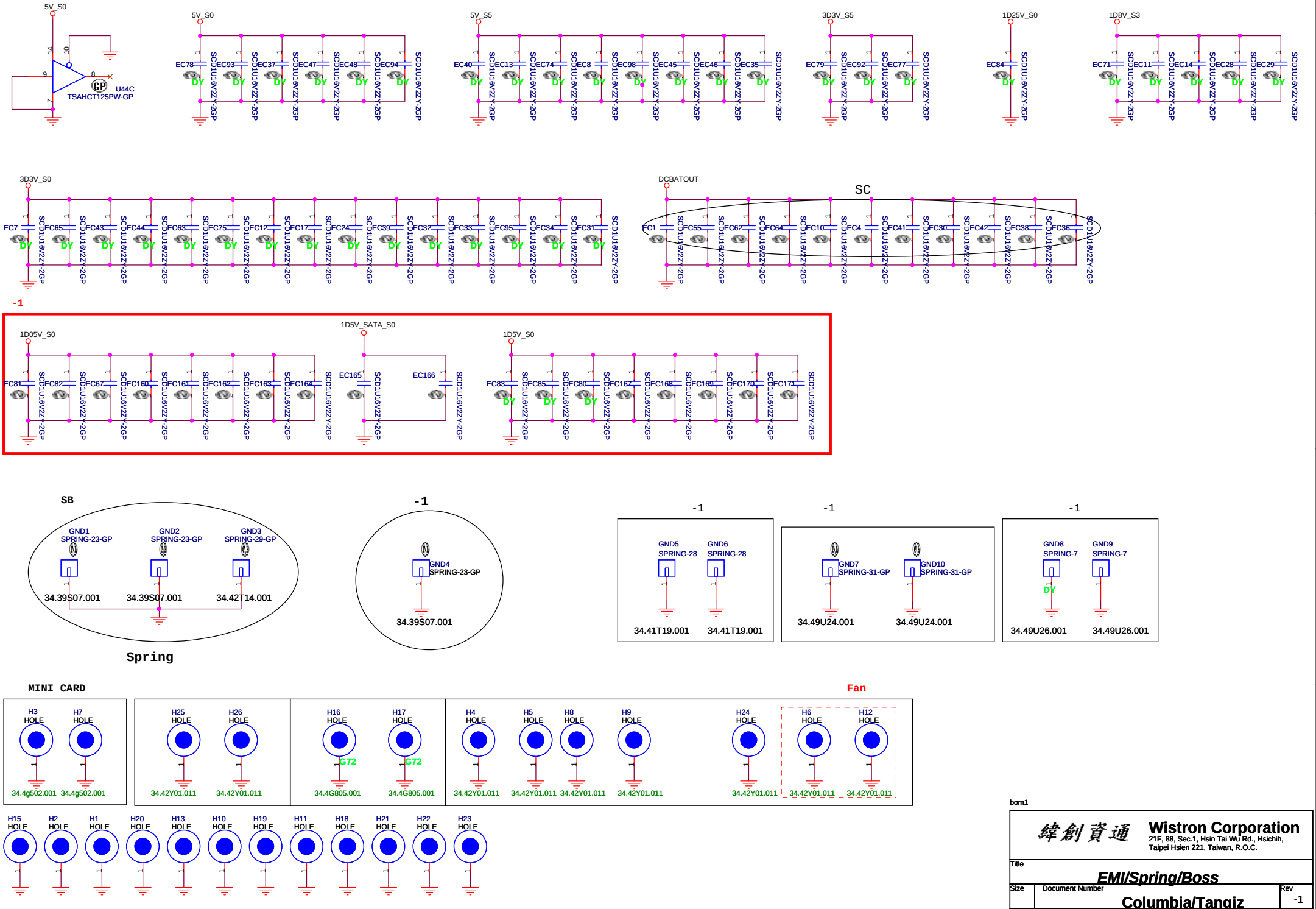

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