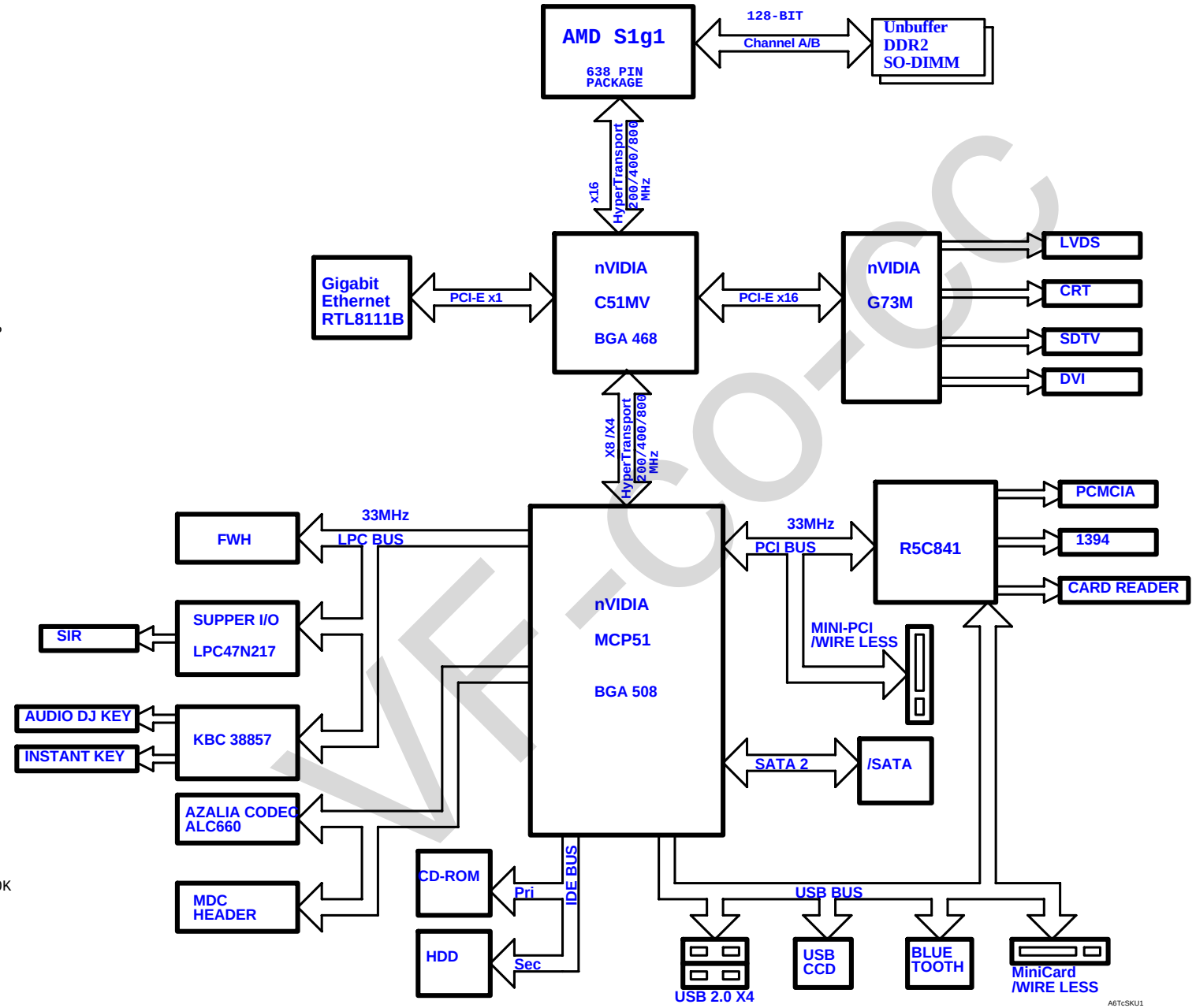
A6T

REVISION: 1.01

01.BLOCK DIAGRAM
02.RESET MAP
03.CLOCK MAP
04.S1_HT_C51
05.S1_DDR2
06.S1_CNTL/DEBUG/THERM
07.S1_POWER
08.DDR2_SODIMM
09.DDR2 TER/FETGAGE
10.C51_HT_CPU
11.C51_HT_MCP
12.C51_PCIE
13.C51_VIDEO
14.C51_VCC_GND
15.FAN/THERM SENSOR
16.MCP51_HT
17.MCP51_PCI/LPC
18.MCP51_IDE/SATA
19.MCP51_USB/AC97/SMB
20.MCP51_RGMI/XTAL
21.MCP51_VCC
22.G73M_PCIE
23.G73M_FB I/F
24.G73M_LVDS/GND
25.G73M_VGA/TV
26.G73M_TMDS/GPIO
27.G73M_XTAL/ROM STRAP
28.G73M_STRAPS
29.G73M_MEM_PART1
30.G73M_MEM_PART2
31.HDD/CDROM
32.MINI PCI
33.CARD BUS
34.PCMCIA
35.1394/SD_CARD
36.SIO/SIR
37.FWH
38.KBC
39.USB/BLUE TOOTH
40.CRT/TV CON
41.LVDS/INVERTER
42.ALC880
43.AMP
44.MIC/LINE-IN JACK
45.RJ45/11/MDC
46.LAN
47.BLANK
48.FUNCTION KEY
49.LED
50.POWER SEQEUNCE(1)
51.POWER SEQUENCE(2)
52.SCREW HOLE
53.Battery
54.CHARGE
55.BATLOW/SD#
56.LOAD SWITCH
57.BLANK
58.BLANK
59.BLANK
60.POWER SEQUENCE BLCOK
61.POWER BUDGET BLOCK
62.BLANK



A6TcSKU1

ASUSTECH CO.,LTD

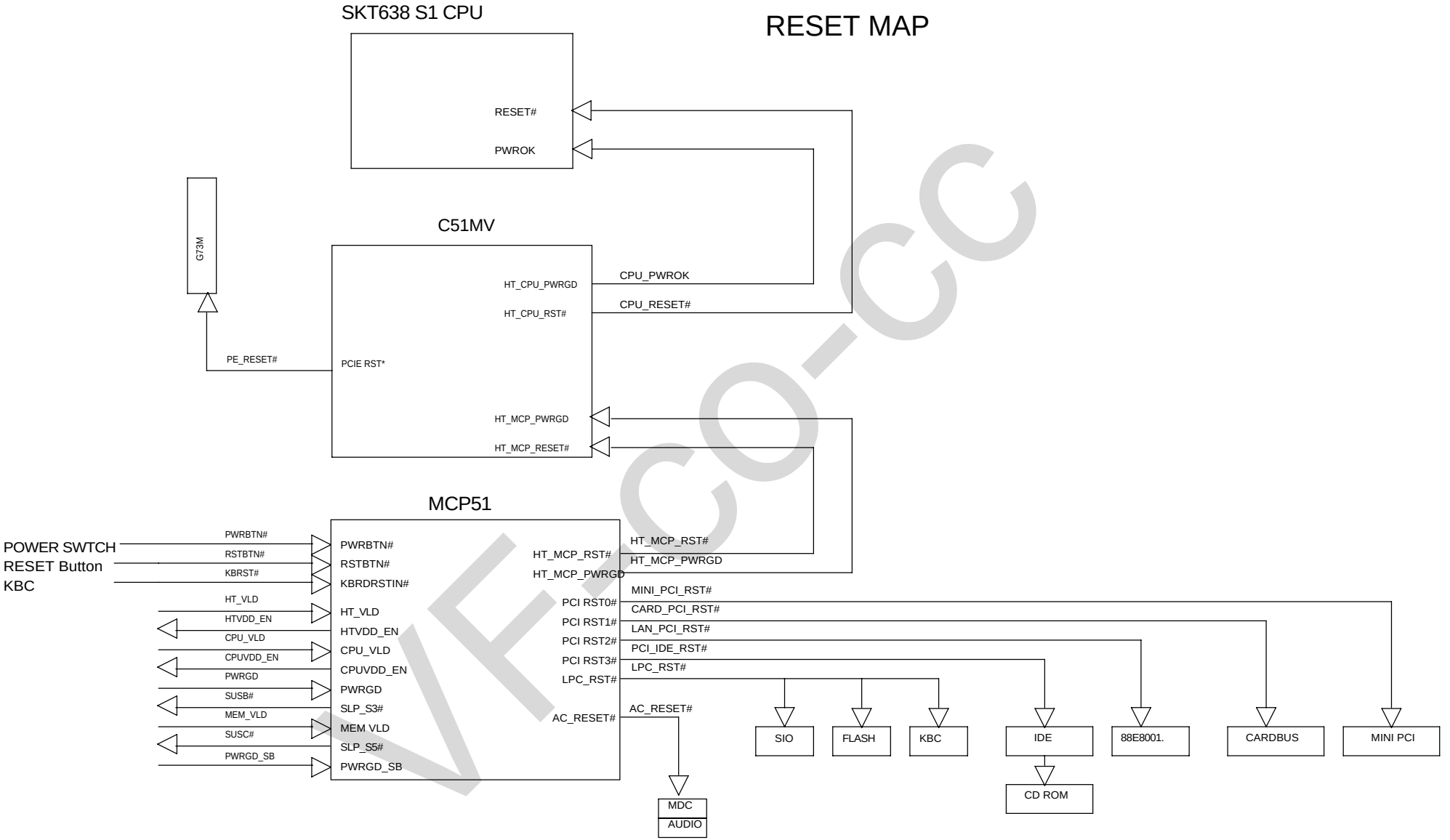
Title : BLOCK DIAGRAM

Engineer: Jefing_Li

Size	Project Name	Rev
C	A6T	1.01

Date: Wednesday, March 08, 2006 Sheet 1 of 72

RESET MAP



A6TcSKU1

ASUSTECH CO.,LTD.

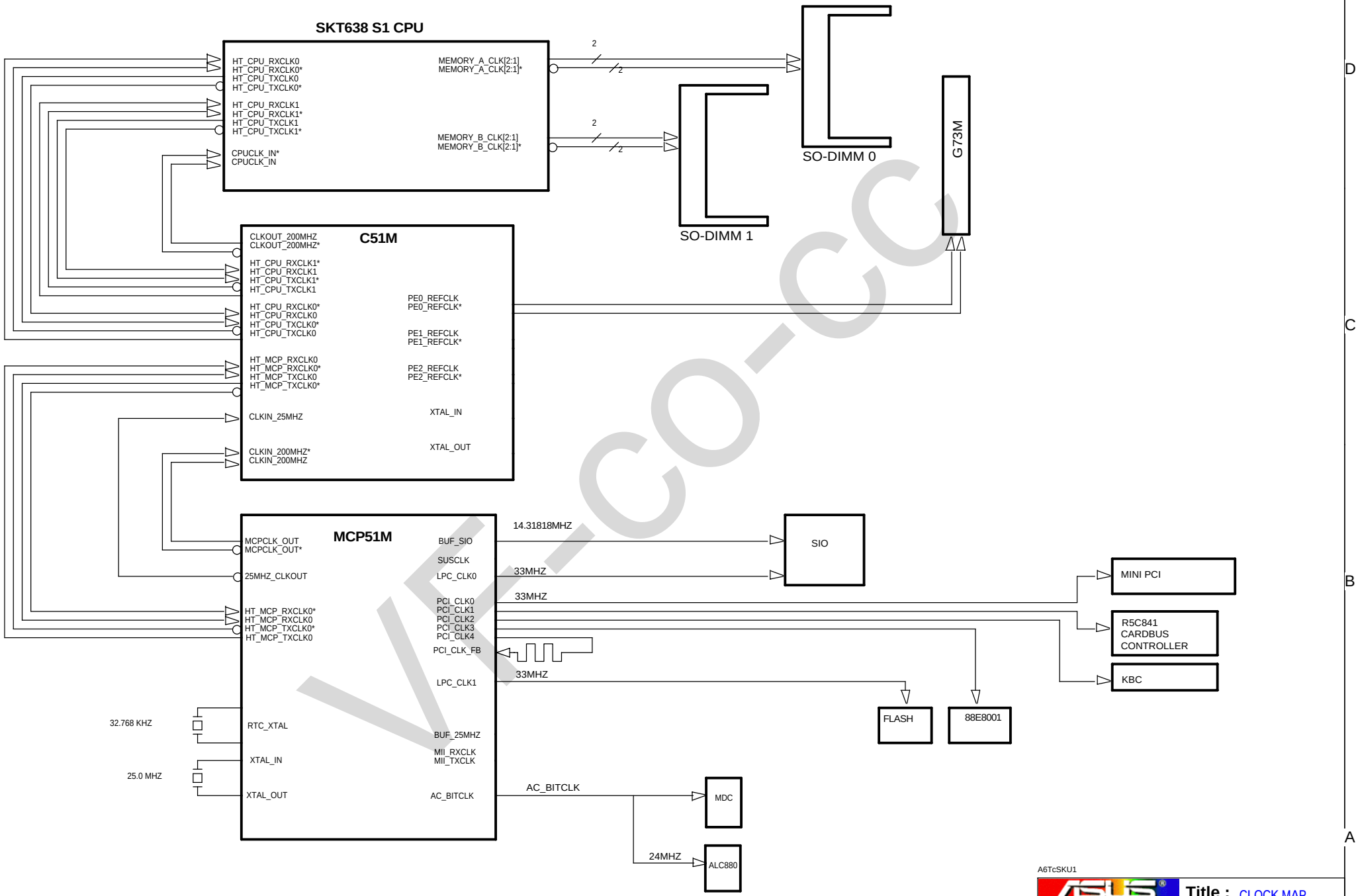
Title : RESET MAP

Engineer: Jefing_Li

Size	Project Name	Rev
A3	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 2 of 72

CLOCK MAP



A6TcSKU1

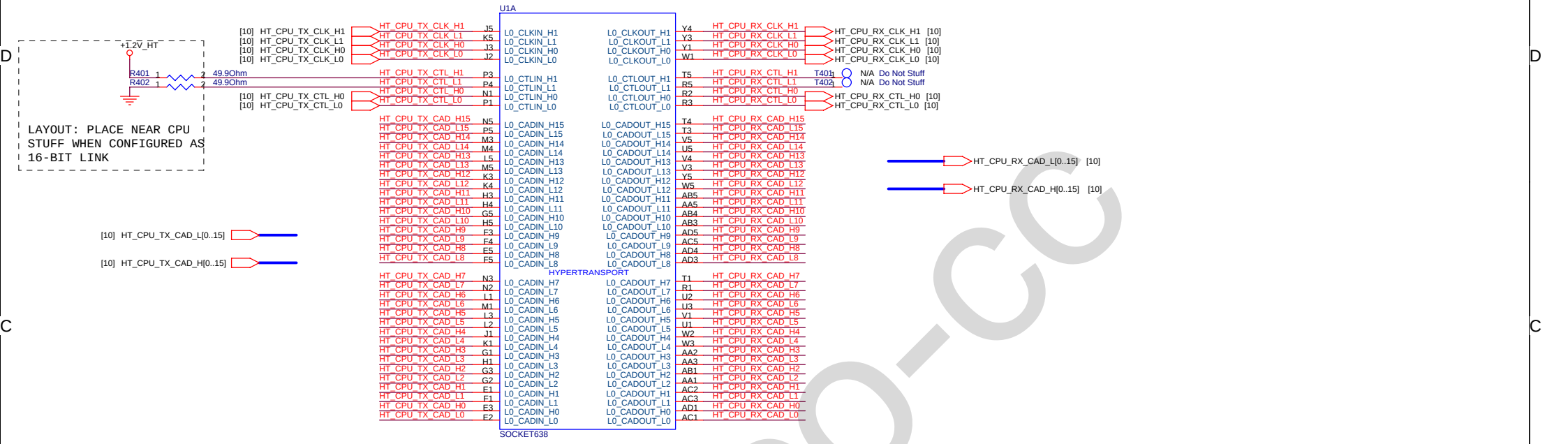
ASUSTECH CO.,LTD.

Title : CLOCK MAP

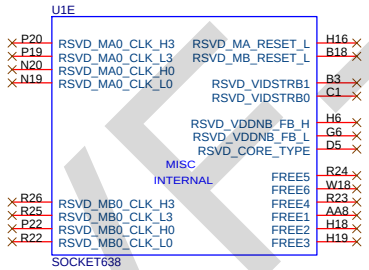
Engineer: Jefing_Li

Size	Project Name	Rev
A3	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 3 of 72



Do not cross plane.



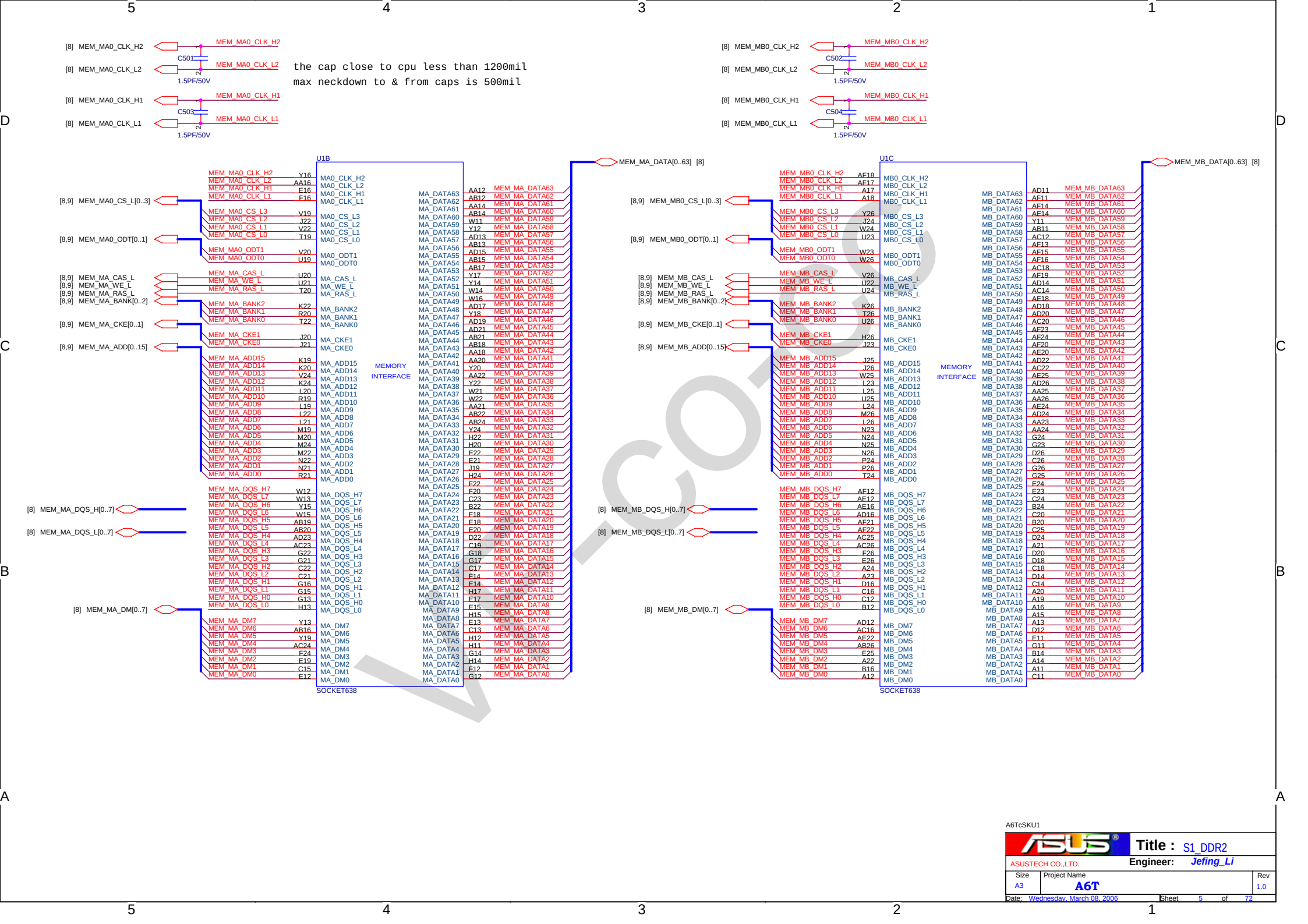
A6TcSKU1

Title : S1_HT_C51

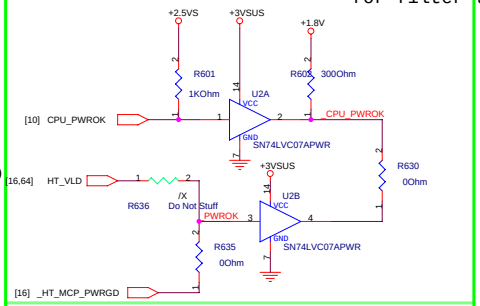
ASUSTECH CO.,LTD. Engineer: Jefing_Li

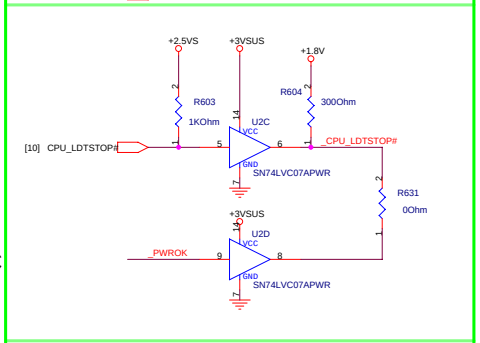
Size	Project Name	Rev
A3	A6T	1.0

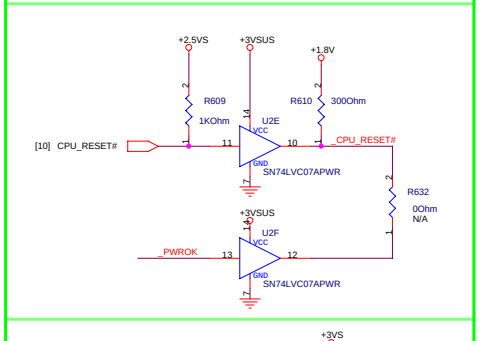
Date: Wednesday, March 08, 2006 Sheet 4 of 72

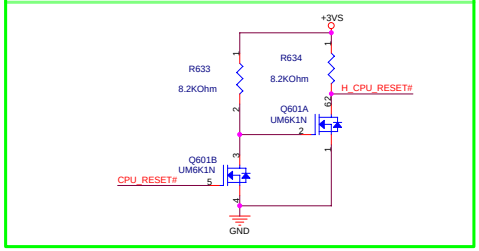

the cap close to cpu less than 1200mil
max neckdown to & from caps is 500mil
C501
C502
C503
C504
1.5PF/50V
U1B
U1C
MEMORY INTERFACE
SOCKET638
MEM_MA_DATA[0..63]
MEM_MB_DATA[0..63]
MEM_MA_DQS_H[0..7]
MEM_MA_DQS_L[0..7]
MEM_MA_DM[0..7]
MEM_MB_DQS_H[0..7]
MEM_MB_DQS_L[0..7]
MEM_MB_DM[0..7]
A6TcSKU1
Title : S1_DDR2
ASUSTECH CO.,LTD.
Engineer: Jefing_Li
Size A3
Project Name A6T
Rev 1.0
Date: Wednesday, March 08, 2006
Sheet 5 of 72

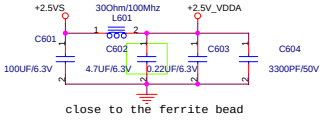
for filter the glitch









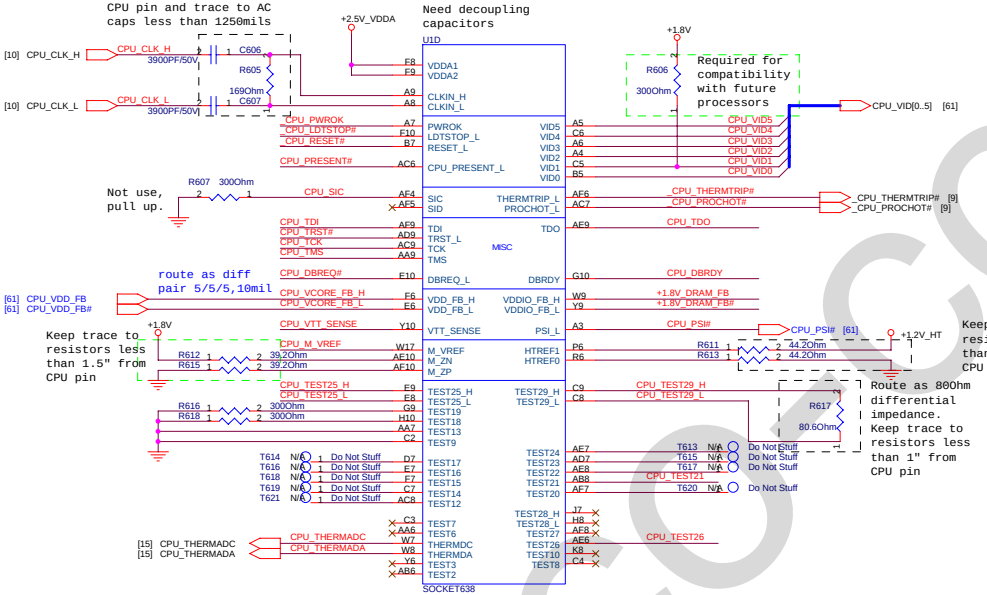


close to the ferrite bead

VDDIO +1.8V

Keep trace to resistors less than 600mils from CPU pin and trace to AC caps less than 1250mils

Need decoupling capacitors



Required for compatibility with future processors

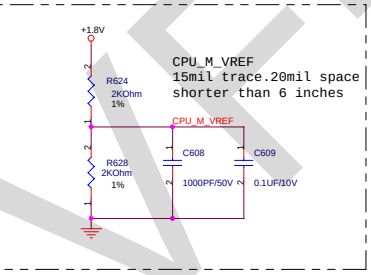
Not use, pull up.

route as diff pair 5/5/5,10mil

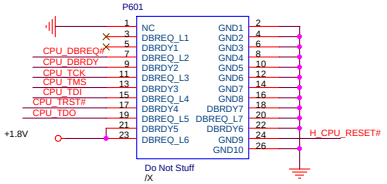
Keep trace to resistors less than 1.5" from CPU pin

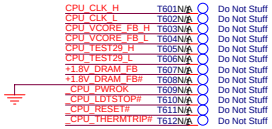
Route as 80Ohm differential impedance. Keep trace to resistors less than 1" from CPU pin

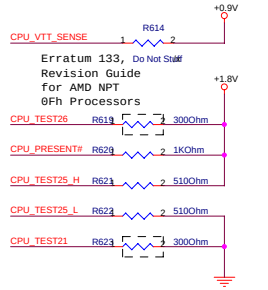
Keep trace to resistors less than 1.5" from CPU pin



CPU_M_VREF
15mil trace.20mil space
shorter than 6 inches







A6TcSKU1

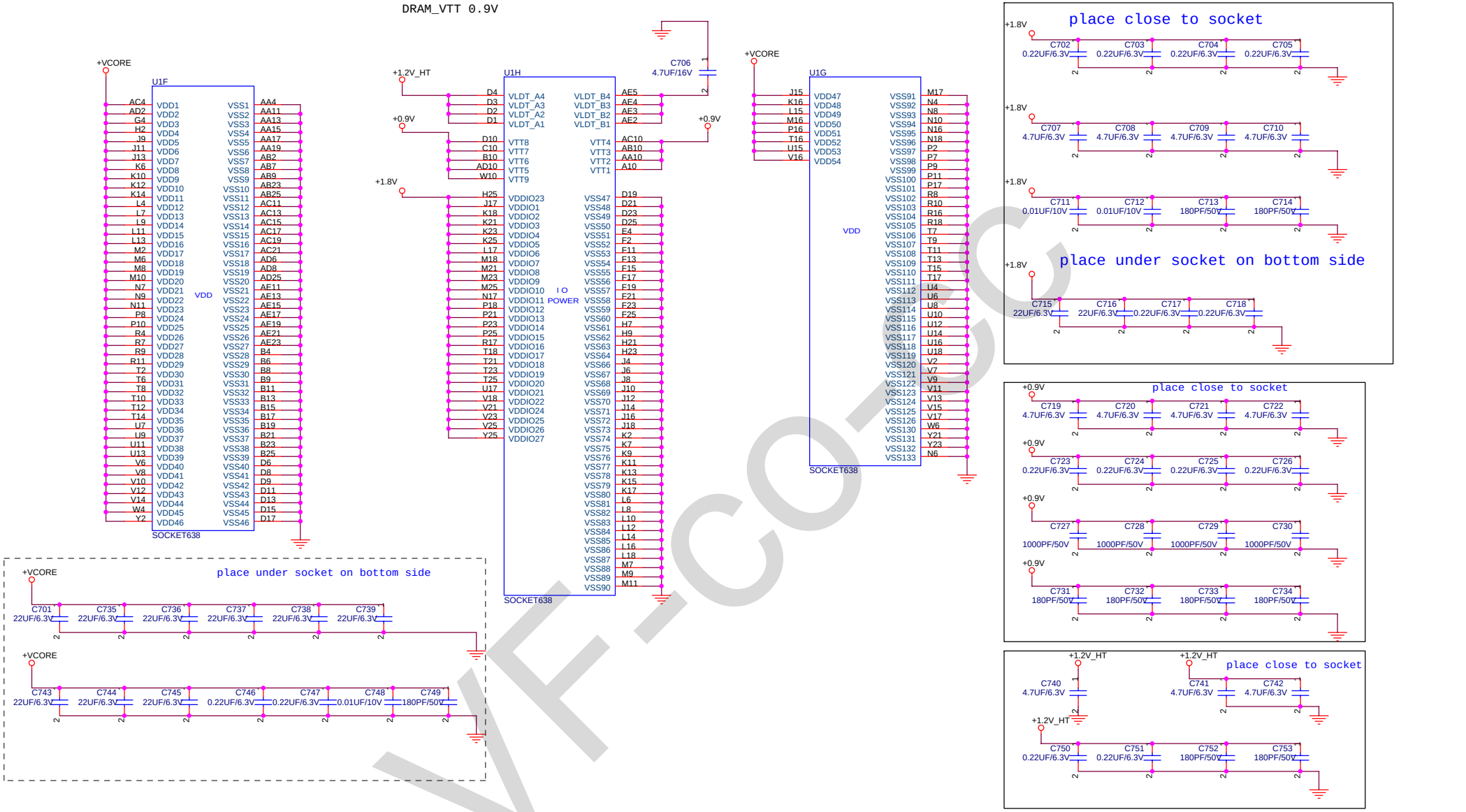
Title : S1_CNTL/DEBUG/THERM

ASUSTECH CO.,LTD.

Engineer: Jefing_Li

Size	Project Name	Rev
C	A6T	1.01

Date: Wednesday, March 08, 2006 Sheet 6 of 72



A6TcSKU1

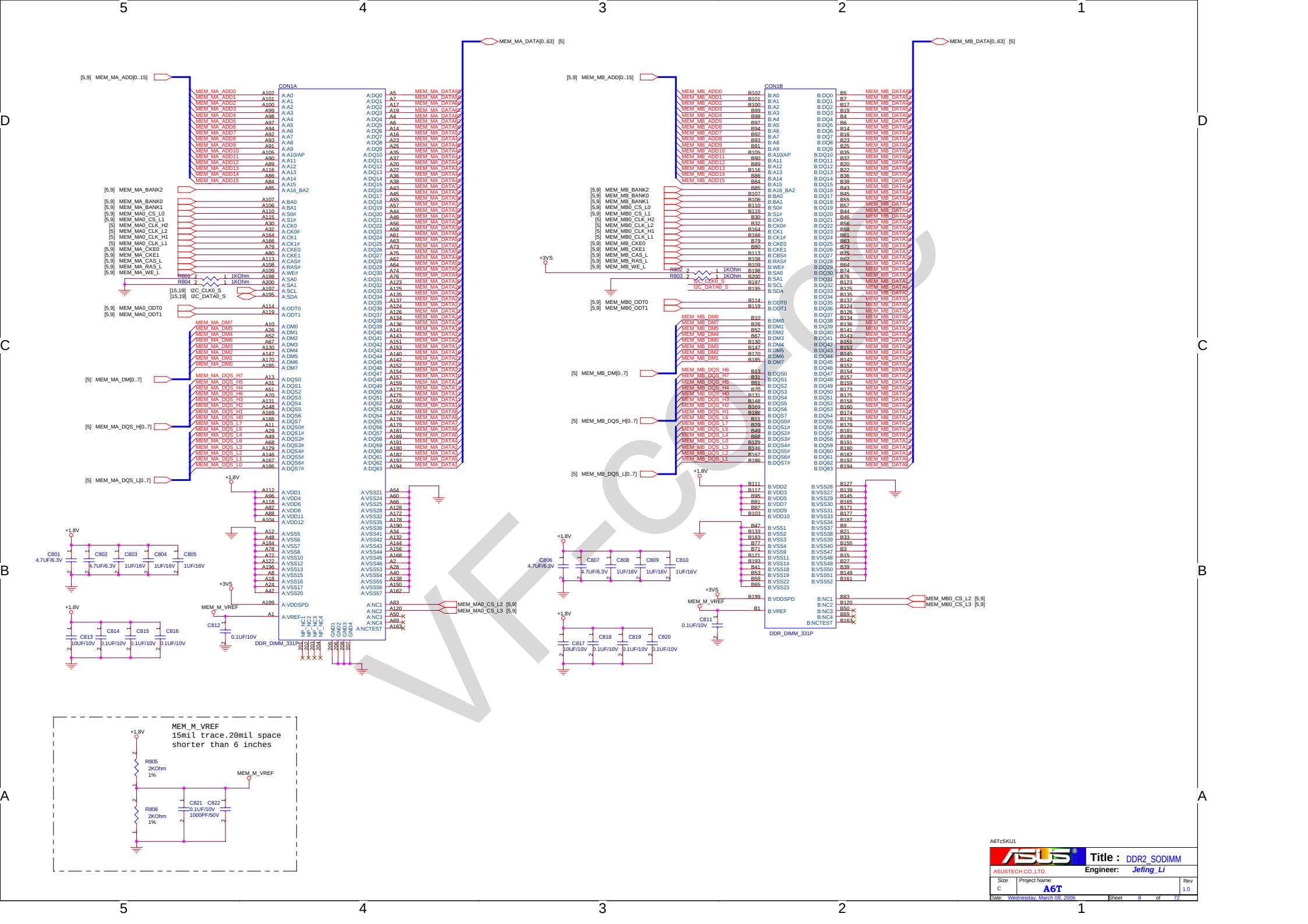
ASUSTECH CO.,LTD.

Title : S1_POWER

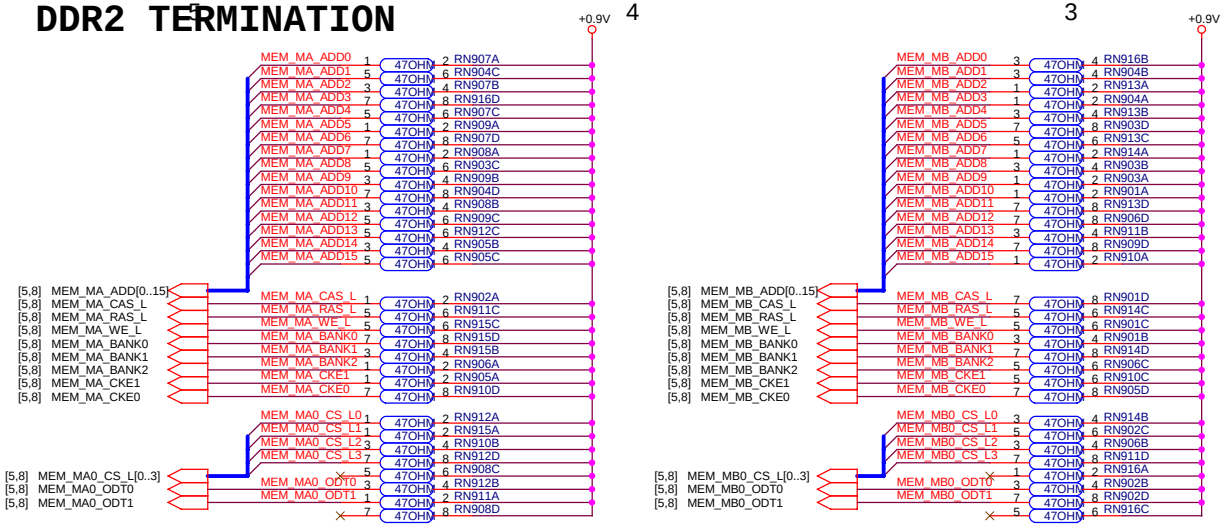
Engineer: Jefing_Li

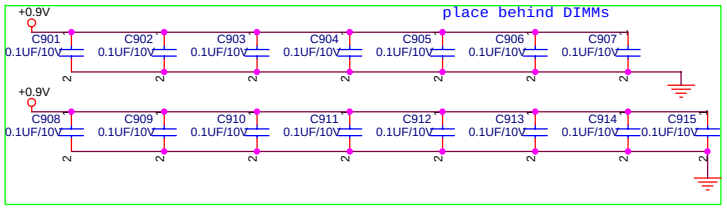
Size	Project Name	Rev
A3	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 7 of 72

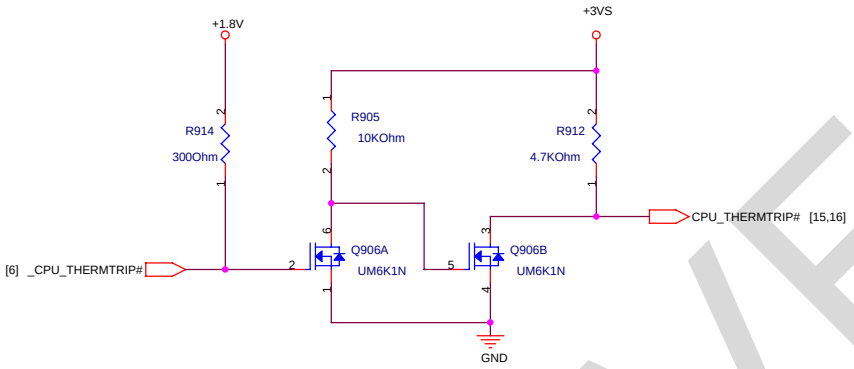

MEM_MA_DATA[0..63] [5]
MEM_MB_DATA[0..63] [5]
CON1A
CON1B
DDR_DIMM_331P
MEM_M_VREF
15mil trace.20mil space
shorter than 6 inches
A6TcSKU1
Title : DDR2_SODIMM
ASUSTECH CO.,LTD.
Engineer: Jefing_Li
Project Name
A6T
Rev
1.0
Date: Wednesday, March 08, 2006
Sheet 8 of 72

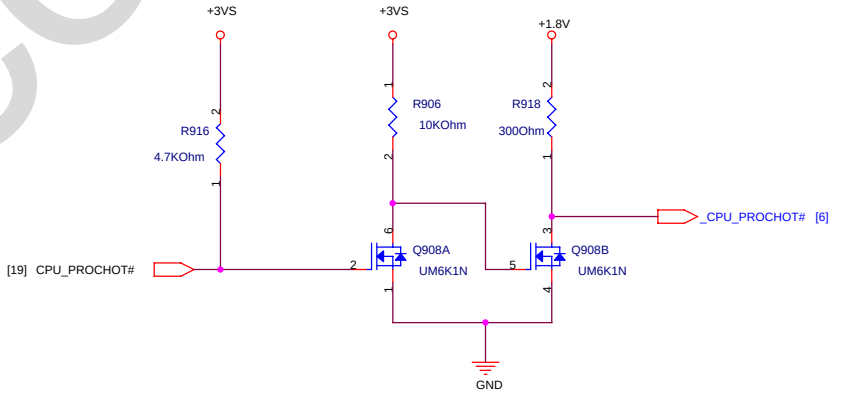
DDR2 TERMINATION





LAYOUT :COULD BE SWAP





A6TcSKU1

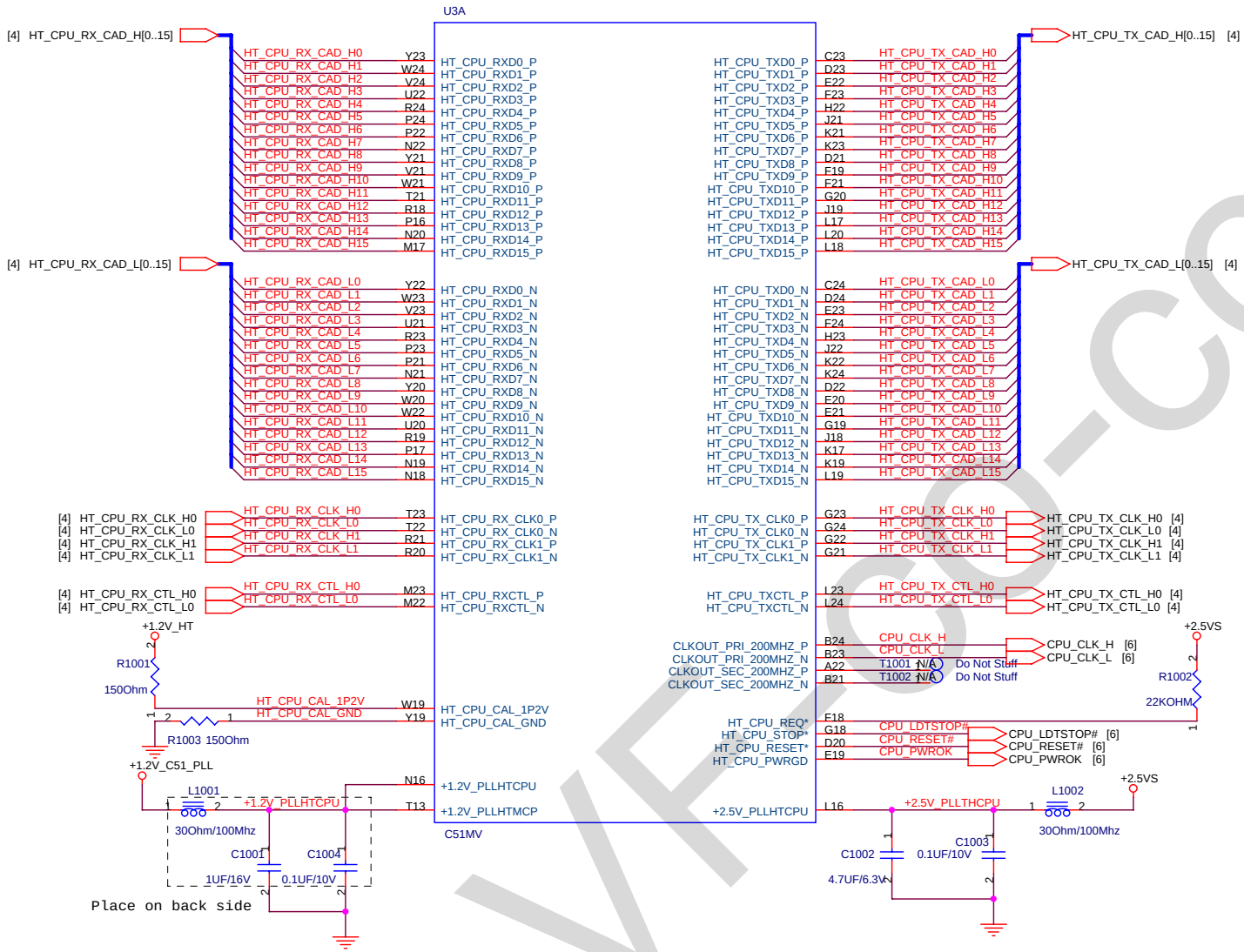
ASUSTECH CO.,LTD.

Title : DDR2 TER/FETGAGE

Engineer: Jefing_Li

Size	Project Name	Rev
A3	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 9 of 72



A6TcSKU1

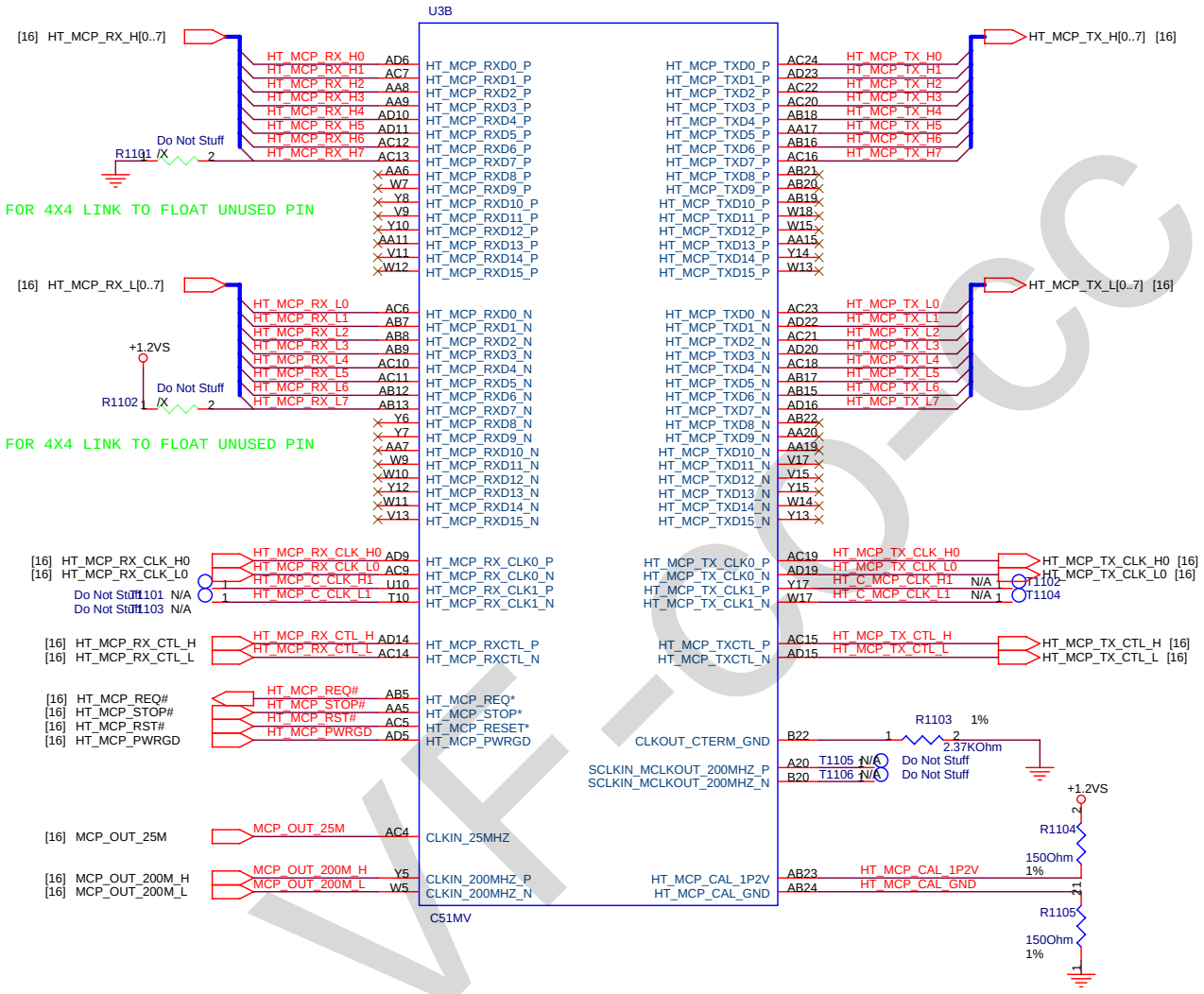
ASUSTECH CO.,LTD.

Title : C51_HT_CPU

Engineer: Jefing_Li

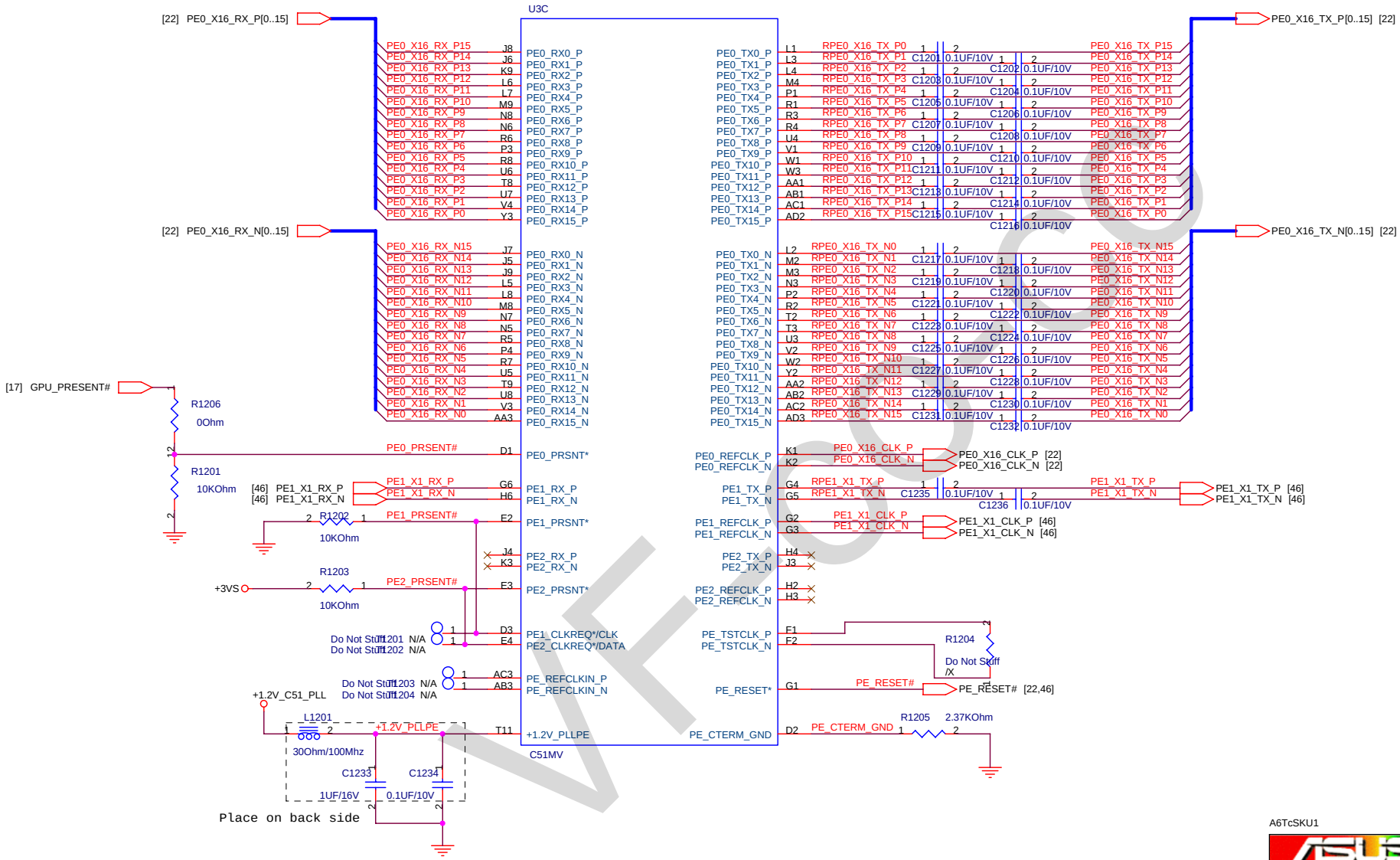
Size	Project Name	Rev
B	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 10 of 72



A6TcSKU1

ASUSTECH CO.,LTD.	Title : C51_HT_MCP	
	Engineer: Jefing_Li	
Size: B	Project Name: A6T	Rev: 1.0
Date: Wednesday, March 08, 2006	Sheet 11 of 72	



A6TcSKU1

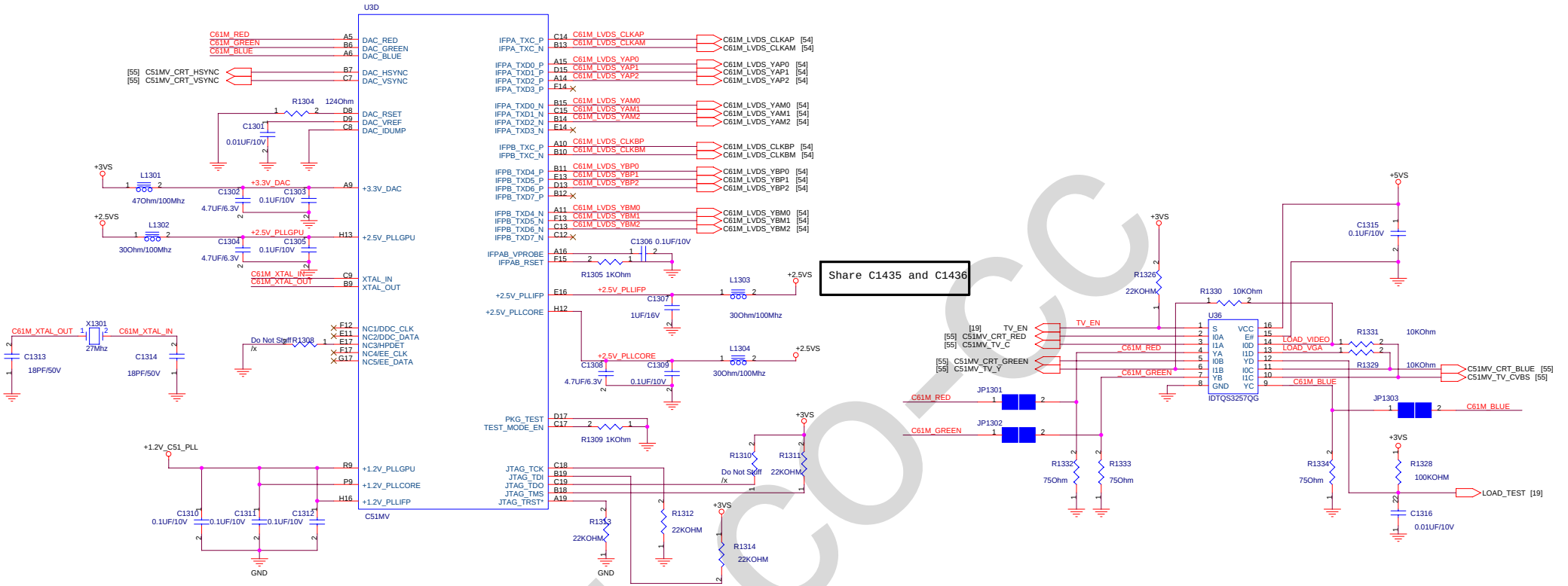
ASUSTECH CO.,LTD.

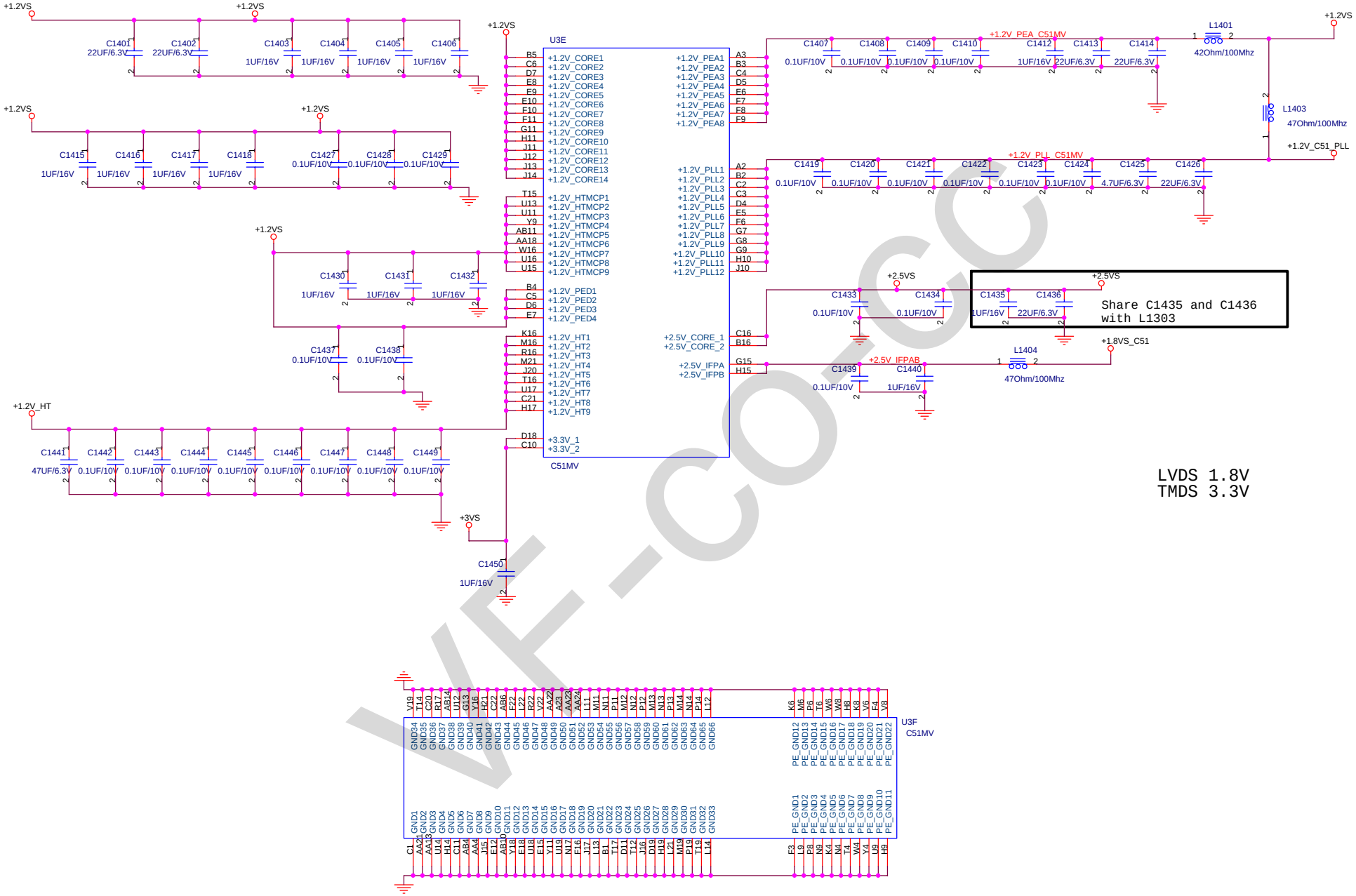
Title : C51_PCIE

Engineer: Jefing_Li

Size	Project Name	Rev
B	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 12 of 72


U3D
C51MV
DAC_RED
DAC_GREEN
DAC_BLUE
DAC_HSYNC
DAC_VSYNC
DAC_RSET
DAC_VREF
DAC_IDUMP
+3.3V_DAC
+2.5V_PLLGPU
XTAL_IN
XTAL_OUT
NC1/DDC_CLK
NC2/DDC_DATA
NC3/HPDET
NC4/EE_CLK
NC5/EE_DATA
+2.5V_PLLIFP
+2.5V_PLLCORE
PKG_TEST
TEST_MODE_EN
+1.2V_PLLGPU
+1.2V_PLLCORE
+1.2V_PLLIFP
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TRST*
IFPA_TXC_P
IFPA_TXC_N
IFPA_TXD0_P
IFPA_TXD1_P
IFPA_TXD2_P
IFPA_TXD3_P
IFPA_TXD0_N
IFPA_TXD1_N
IFPA_TXD2_N
IFPA_TXD3_N
IFPB_TXC_P
IFPB_TXC_N
IFPB_TXD4_P
IFPB_TXD5_P
IFPB_TXD6_P
IFPB_TXD7_P
IFPB_TXD4_N
IFPB_TXD5_N
IFPB_TXD6_N
IFPB_TXD7_N
IFPAB_VPROBE
IFPAB_RSET
C61M_LVDS_CLKAP
C61M_LVDS_CLKAM
C61M_LVDS_YAP0
C61M_LVDS_YAP1
C61M_LVDS_YAP2
C61M_LVDS_YAM0
C61M_LVDS_YAM1
C61M_LVDS_YAM2
C61M_LVDS_CLKBP
C61M_LVDS_CLKBM
C61M_LVDS_YBP0
C61M_LVDS_YBP1
C61M_LVDS_YBP2
C61M_LVDS_YBM0
C61M_LVDS_YBM1
C61M_LVDS_YBM2
Share C1435 and C1436
Do Not Stuff
/x
U36
IDTQS3257QG
TV_EN
LOAD_VIDEO
LOAD_VGA
LOAD_TEST
C51MV_CRT_BLUE
C51MV_TV_CVBS
JP1301
JP1302
JP1303
A6TcSKU1
ASUSTECH CO.,LTD.
Title : C51_VIDEO
Engineer: Jefing_Li
Size: Custom
Project Name: A6T
Rev: 1.0
Date: Wednesday, March 08, 2006
Sheet 13 of 72



A6TcSKU1

ASUSTECH CO.,LTD.	Title : C51_VCC_GND	
	Engineer: Jefing_Li	
Size: A3	Project Name: A6T	Rev: 1.0
Date: Wednesday, March 08, 2006	Sheet 14 of 72	

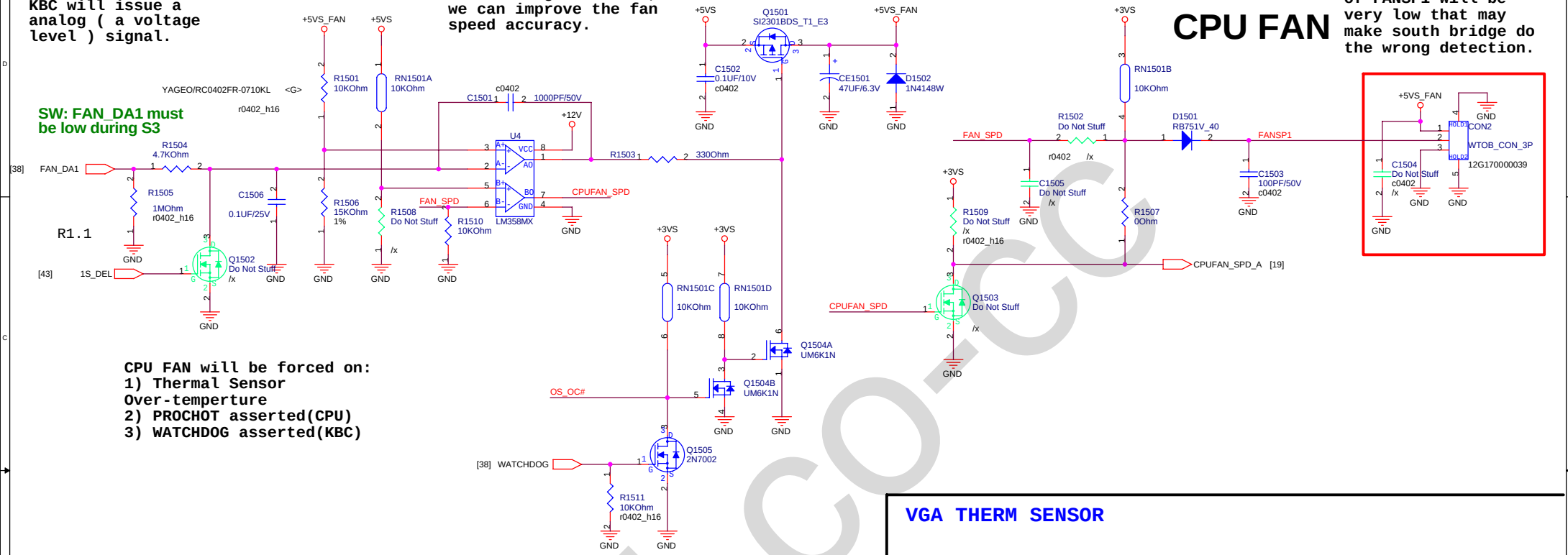
Fan Speed Control

KBC will issue a analog (a voltage level) signal.

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

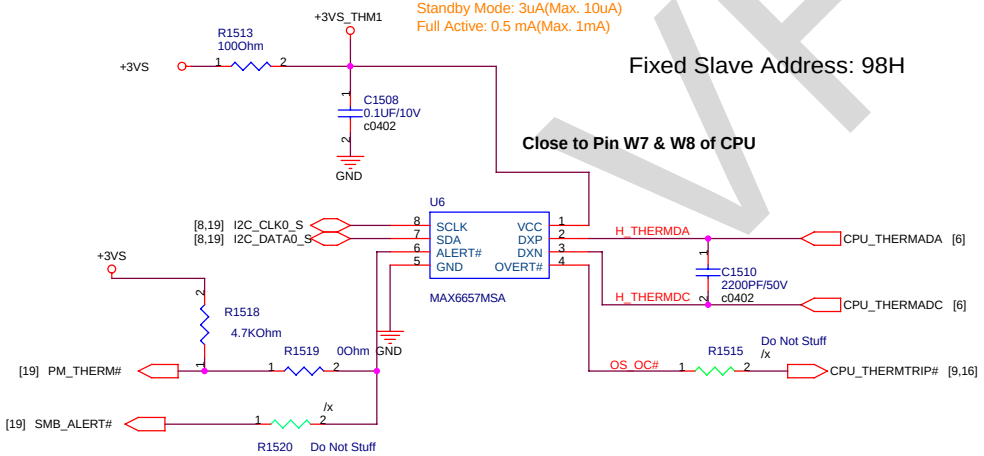
When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

CPU FAN

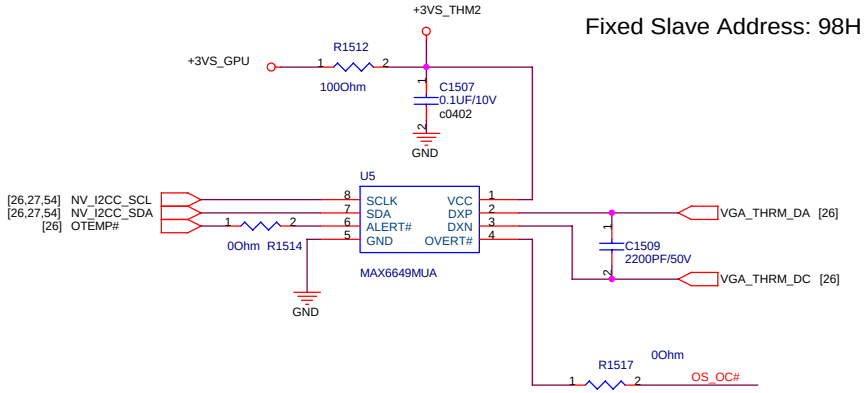


CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) PROCHOT asserted(CPU)
3) WATCHDOG asserted(KBC)

CPU THERM SENSOR



VGA THERM SENSOR



A6TcSKU1

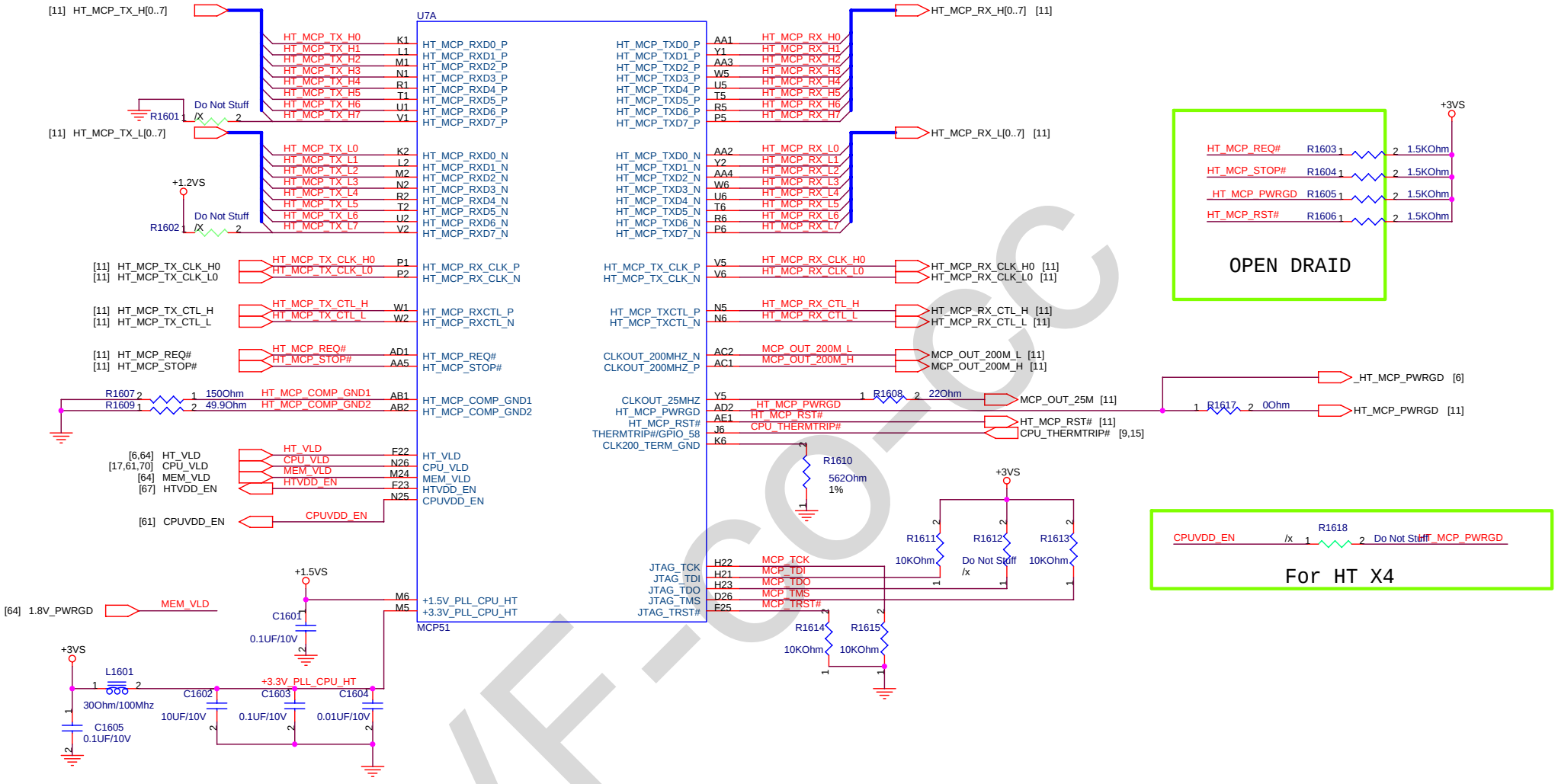
ASUSTECH CO.,LTD.

Title : FAN/THERM SENSOR

Engineer: Jefing_Li

Size	Project Name	Rev
A3	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 15 of 72



A6TcSKU1

ASUSTECH CO.,LTD.

Title : MCP51_HT

Engineer: Jefing_Li

Size	Project Name	Rev
B	A6T	1.0

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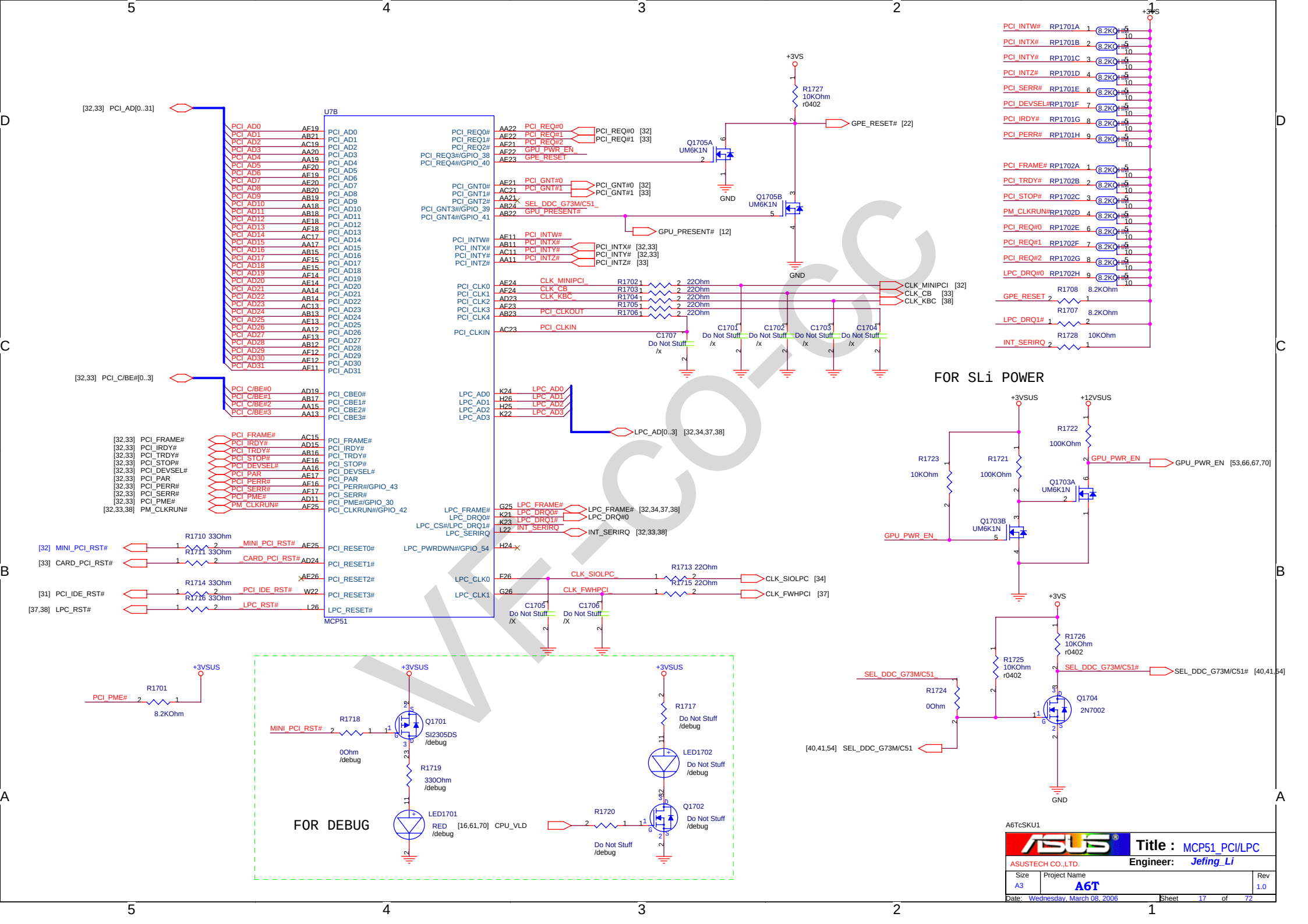
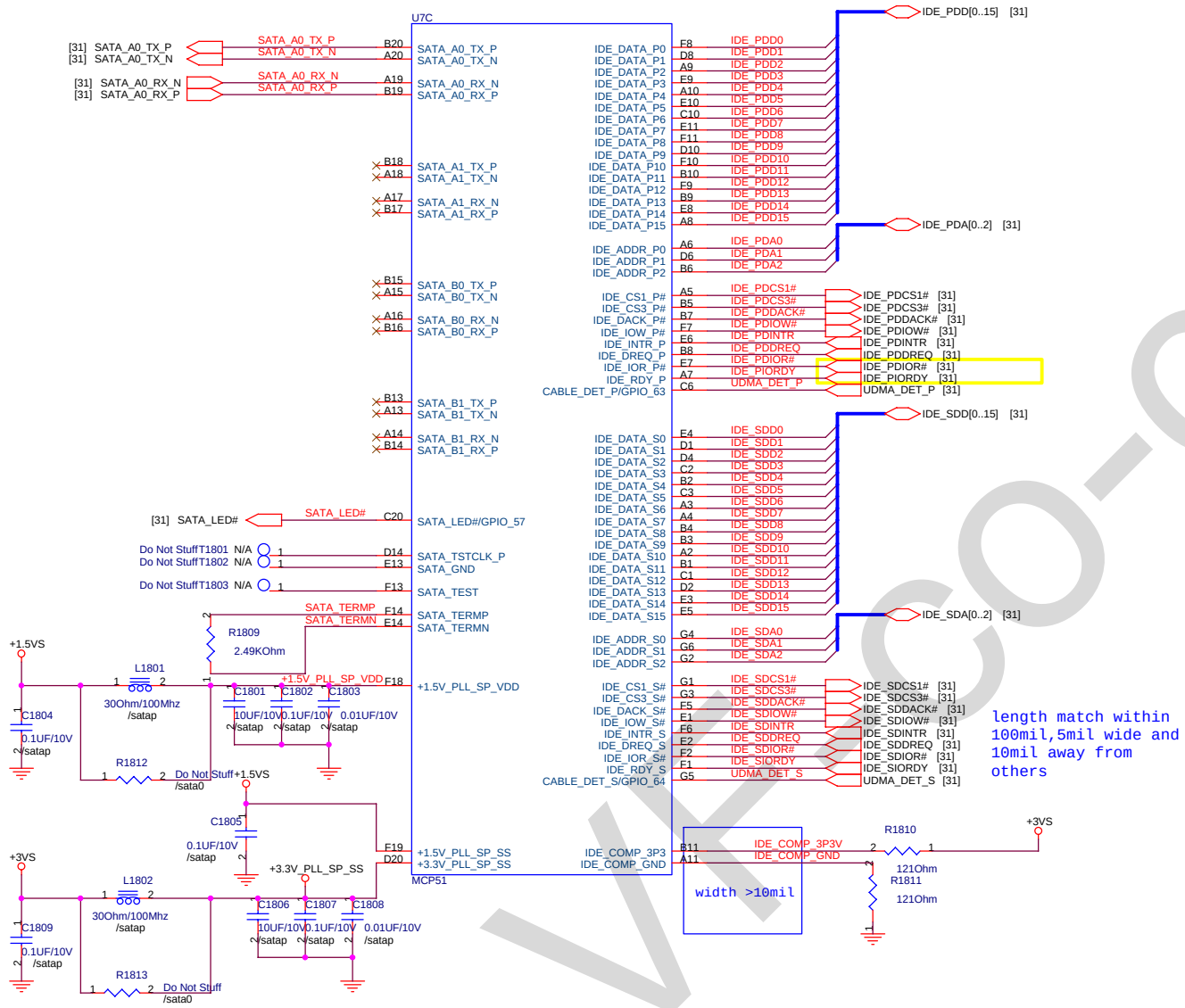

U7B
MCP51
PCI_AD0
PCI_AD1
PCI_AD2
PCI_AD3
PCI_AD4
PCI_AD5
PCI_AD6
PCI_AD7
PCI_AD8
PCI_AD9
PCI_AD10
PCI_AD11
PCI_AD12
PCI_AD13
PCI_AD14
PCI_AD15
PCI_AD16
PCI_AD17
PCI_AD18
PCI_AD19
PCI_AD20
PCI_AD21
PCI_AD22
PCI_AD23
PCI_AD24
PCI_AD25
PCI_AD26
PCI_AD27
PCI_AD28
PCI_AD29
PCI_AD30
PCI_AD31
PCI_CBE0#
PCI_CBE1#
PCI_CBE2#
PCI_CBE3#
PCI_FRAME#
PCI_IRDY#
PCI_TRDY#
PCI_STOP#
PCI_DEVSEL#
PCI_PAR
PCI_PERR#
PCI_SERR#
PCI_PME#
PCI_RESET0#
PCI_RESET1#
PCI_RESET2#
PCI_RESET3#
LPC_RESET#
PCI_REQ0#
PCI_REQ1#
PCI_REQ2#
PCI_REQ3#/GPIO_38
PCI_REQ4#/GPIO_40
PCI_GNT0#
PCI_GNT1#
PCI_GNT2#
PCI_GNT3#/GPIO_39
PCI_GNT4#/GPIO_41
PCI_INTW#
PCI_INTX#
PCI_INTY#
PCI_INTZ#
PCI_CLK0
PCI_CLK1
PCI_CLK2
PCI_CLK3
PCI_CLK4
PCI_CLKIN
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
LPC_DRQ0#
LPC_CS#/LPC_DRQ1#
LPC_SERIRQ
LPC_PWRDWN#/GPIO_54
LPC_CLK0
LPC_CLK1
[32,33] PCI_AD[0..31]
[32,33] PCI_C/BE#[0..3]
[32,33] PCI_FRAME#
[32,33] PCI_IRDY#
[32,33] PCI_TRDY#
[32,33] PCI_STOP#
[32,33] PCI_DEVSEL#
[32,33] PCI_PAR
[32,33] PCI_PERR#
[32,33] PCI_SERR#
[32,33] PCI_PME#
[32,33,38] PM_CLKRUN#
[32] MINI_PCI_RST#
[33] CARD_PCI_RST#
[31] PCI_IDE_RST#
[37,38] LPC_RST#
R1710 33Ohm
R1711 33Ohm
R1714 33Ohm
R1716 33Ohm
MINI_PCI_RST#
CARD_PCI_RST#
PCI_IDE_RST#
LPC_RST#
[34] CLK_SIOLPC
[37] CLK_FWHPCI
R1713 22Ohm
R1715 22Ohm
C1705 Do Not Stuff /X
C1706 Do Not Stuff /X
[32,34,37,38] LPC_FRAME#
LPC_DRQ0#
INT_SERIRQ [32,33,38]
LPC_AD[0..3] [32,34,37,38]
[32,33] PCI_CLKOUT
R1702 22Ohm
R1703 22Ohm
R1704 22Ohm
R1705 22Ohm
R1706 22Ohm
CLK_MINIPCI [32]
CLK_CB [33]
CLK_KBC [38]
C1707 Do Not Stuff /x
C1701 Do Not Stuff /x
C1702 Do Not Stuff /x
C1703 Do Not Stuff /x
C1704 Do Not Stuff /x
+3VS
R1727 10KOhm r0402
GPE_RESET# [22]
Q1705A UM6K1N
Q1705B UM6K1N
GND
GPU_PRESENT# [12]
PCI_REQ#0 [32]
PCI_REQ#1 [33]
PCI_GNT#0 [32]
PCI_GNT#1 [33]
SEL_DDC_G73M/C51_
GPU_PRESENT#
PCI_INTX# [32,33]
PCI_INTY# [32,33]
PCI_INTZ# [33]
RP1701A PCI_INTW#
RP1701B PCI_INTX#
RP1701C PCI_INTY#
RP1701D PCI_INTZ#
RP1701E PCI_SERR#
RP1701F PCI_DEVSEL#
RP1701G PCI_IRDY#
RP1701H PCI_PERR#
RP1702A PCI_FRAME#
RP1702B PCI_TRDY#
RP1702C PCI_STOP#
RP1702D PM_CLKRUN#
RP1702E PCI_REQ#0
RP1702F PCI_REQ#1
RP1702G PCI_REQ#2
RP1702H LPC_DRQ#0
8.2KOhm
R1708 8.2KOhm
R1707 8.2KOhm
R1728 10KOhm
GPE_RESET
LPC_DRQ1#
INT_SERIRQ
FOR SLi POWER
+3VSUS
+12VSUS
R1722 100KOhm
R1723 10KOhm
R1721 100KOhm
GPU_PWR_EN
GPU_PWR_EN [53,66,67,70]
Q1703A UM6K1N
Q1703B UM6K1N
R1726 10KOhm r0402
R1725 10KOhm r0402
R1724 0Ohm
SEL_DDC_G73M/C51
SEL_DDC_G73M/C51# [40,41,54]
[40,41,54] SEL_DDC_G73M/C51
Q1704 2N7002
R1701 8.2KOhm
PCI_PME#
FOR DEBUG
R1718 0Ohm /debug
Q1701 SI2305DS /debug
R1719 330Ohm /debug
LED1701 RED /debug
[16,61,70] CPU_VLD
R1720 Do Not Stuff /debug
R1717 Do Not Stuff /debug
LED1702 Do Not Stuff /debug
Q1702 Do Not Stuff /debug
A6TcSKU1
Title : MCP51_PCI/LPC
ASUSTECH CO.,LTD.
Engineer: Jefing_Li
Size A3
Project Name A6T
Rev 1.0
Date: Wednesday, March 08, 2006
Sheet 17 of 72



A6TcSKU1

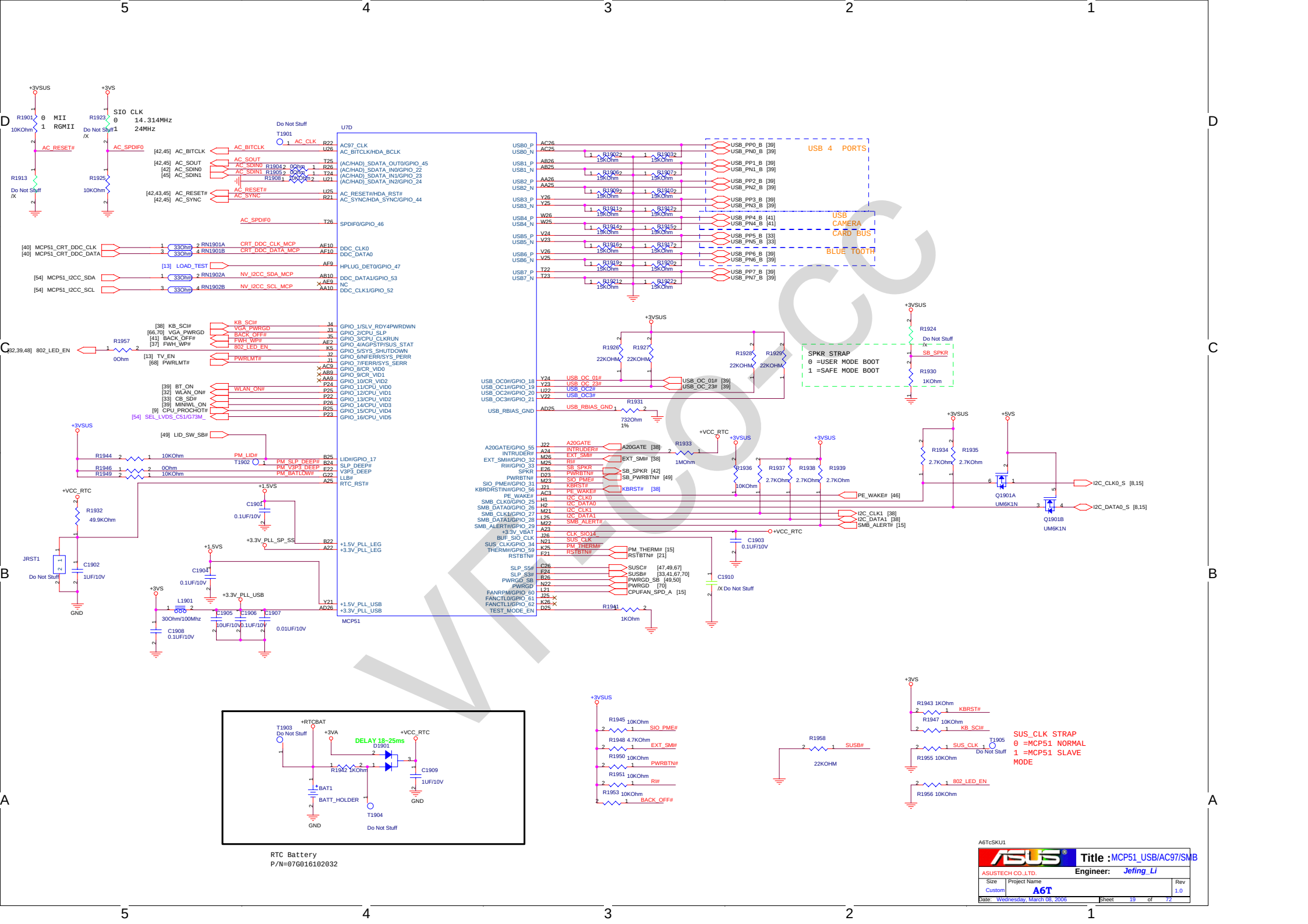
ASUSTECH CO.,LTD.

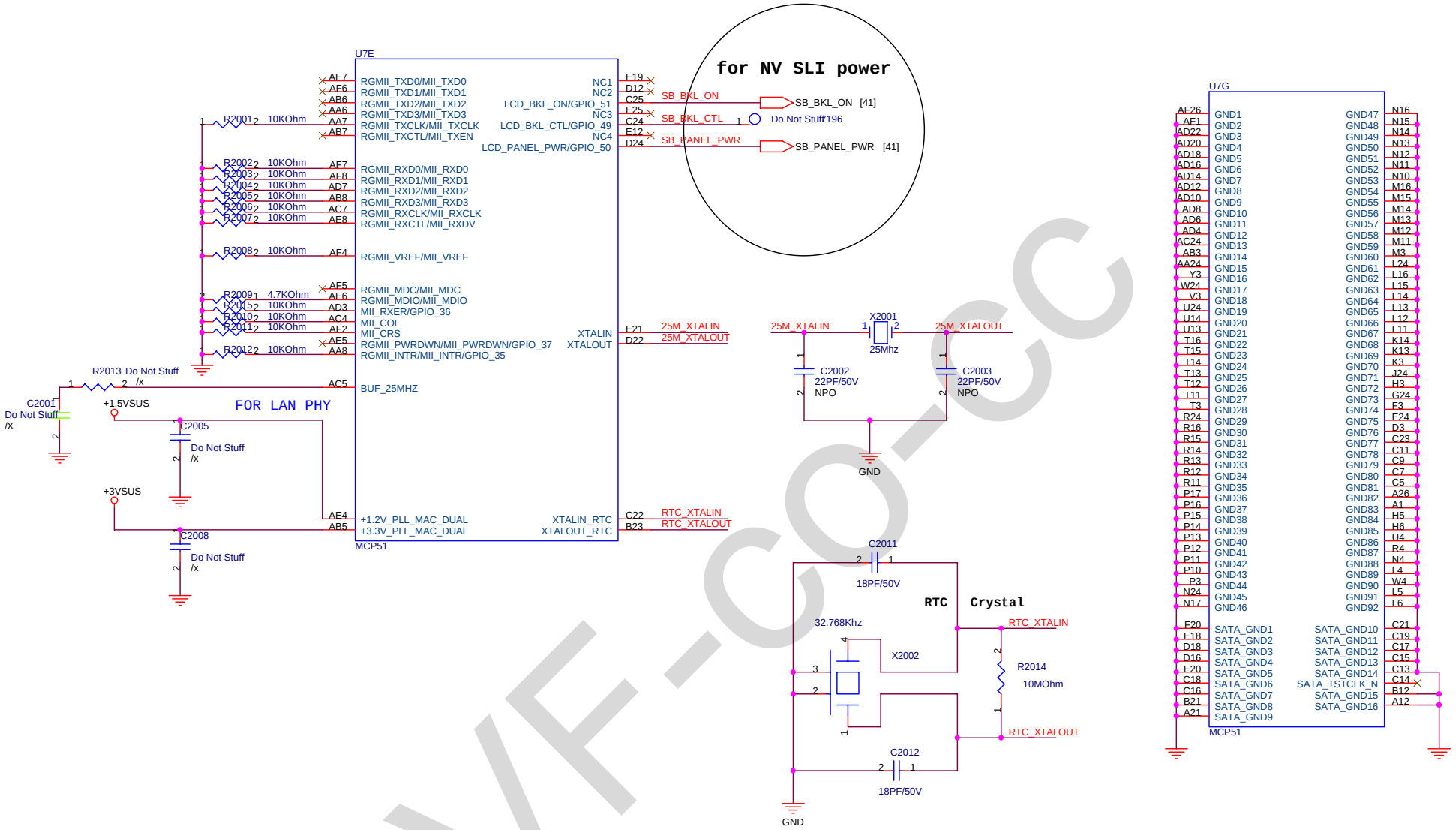
Title : MCP51_IDE/SATA

Engineer: Jefing_Li

Size	Project Name	Rev
A3	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 18 of 72


SIO CLK
0 14.314MHz
1 24MHz
0 MII
1 RGMII
U7D
MCP51
USB 4 PORTS
USB CAMERA
CARD BUS
BLUE TOOTH
SPKR STRAP
0 =USER MODE BOOT
1 =SAFE MODE BOOT
SUS_CLK STRAP
0 =MCP51 NORMAL
1 =MCP51 SLAVE MODE
DELAY 18~25ms
RTC Battery
P/N=07G016102032
Title : MCP51_USB/AC97/SMB
ASUSTECH CO.,LTD.
Engineer: Jefing_Li
A6T
A6TcSKU1
Date: Wednesday, March 08, 2006
Sheet 19 of 72



A6TcSKU1

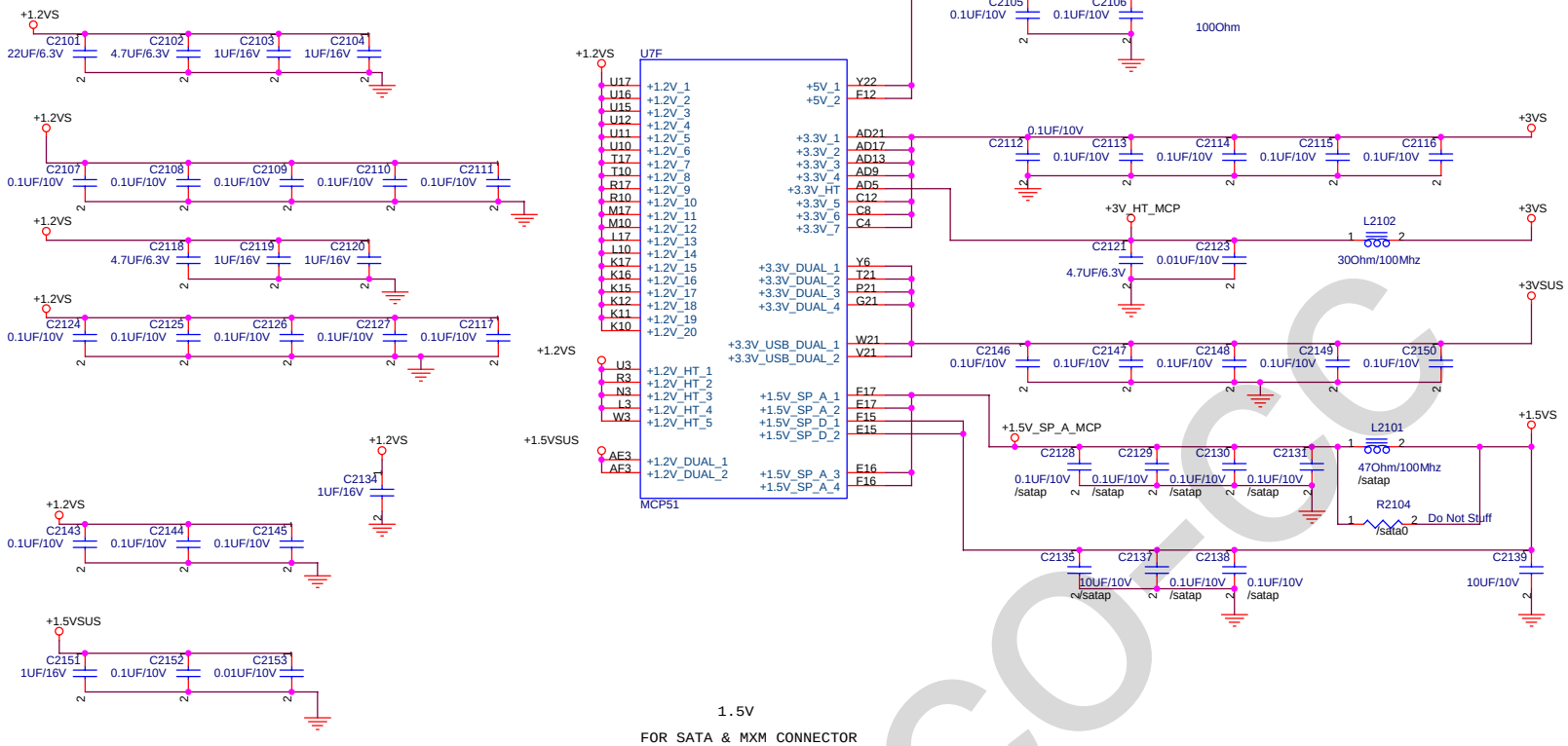
ASUSTECH CO.,LTD.

Title : MCP51_RGMI/XTAL

Engineer: Jefing_Li

Size	Project Name	Rev
B	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 20 of 72

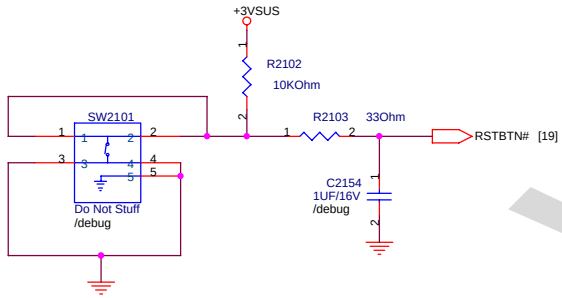


1.5V

FOR SATA & MXM CONNECTOR

1.5V_SP_A	@440MA
1.5V_SP_D	@164MA
1.5V_PLL_SP_DVDD	@20MA
1.5V_PLL_SP_AVDD	@160MA
1.5V_PLL_CPU_HT	@71MA
1.5V_PLL_SP_SS	@10MA
1.5V_PLL_LEG	@4MA
1.5V_PLL_USB_CORE	@16MA

/RESET button



A6TcSKU1

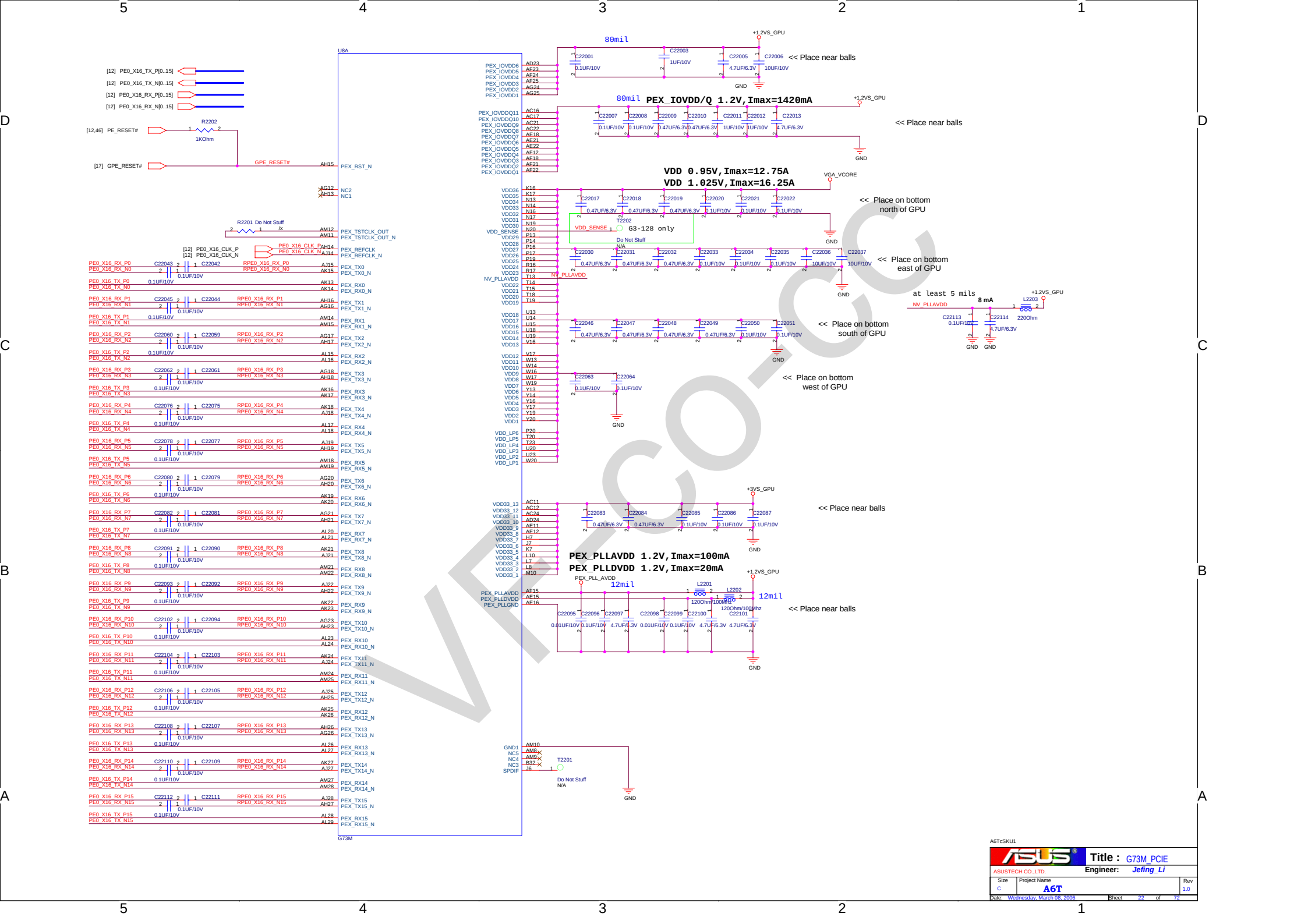
ASUSTECH CO.,LTD.

Title : MCP51_VCC

Engineer: Jefing_Li

Size	Project Name	Rev
A3	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 21 of 72



A6TcSKU1

ASUSTECH CO.,LTD.

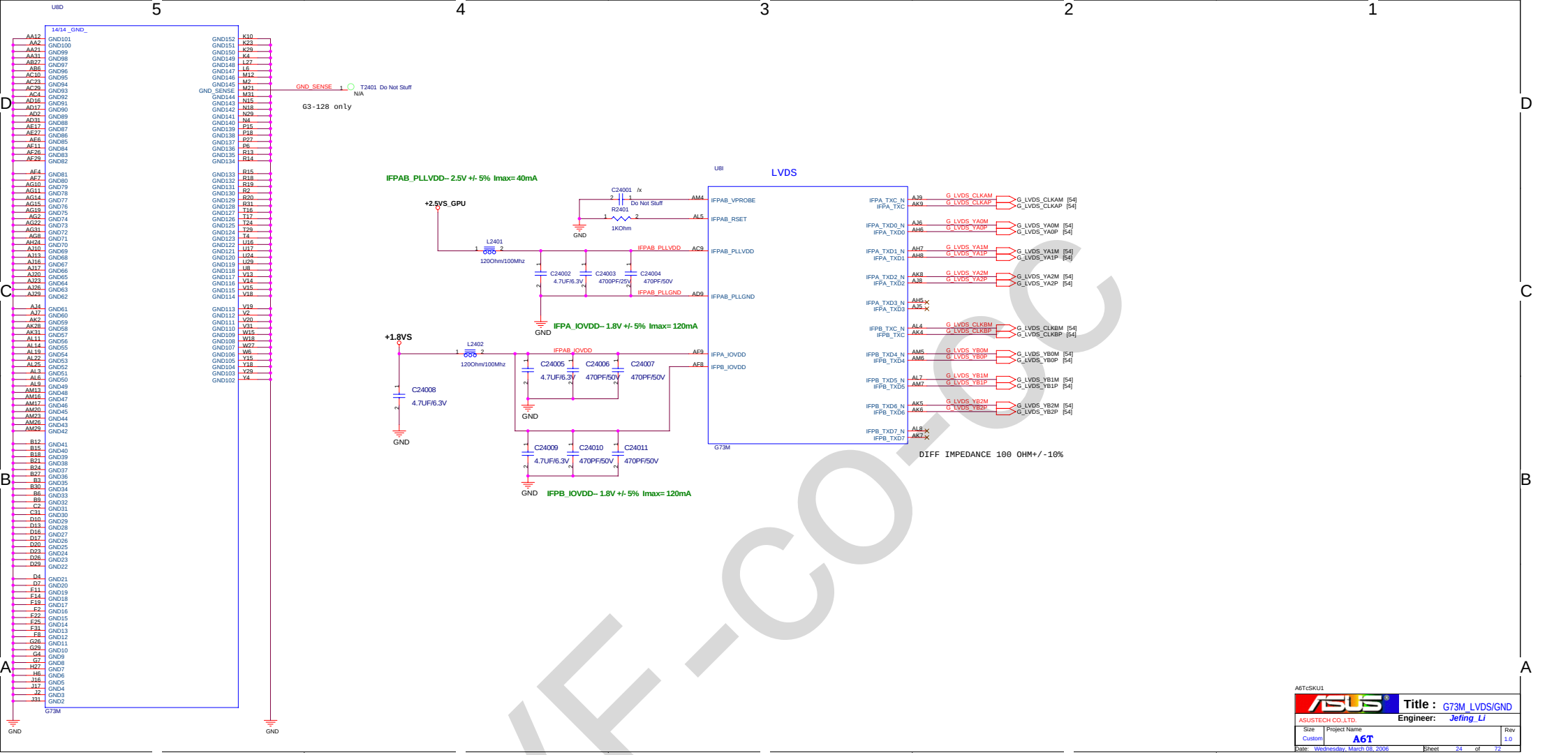
Title : G73M_PCIE

Engineer: Jefing_Li

Size	Project Name	Rev
C	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 22 of 72


CLOSE TO THE BGA
FBVDD/Q 1.8V,Imax=3300~3600mA
CLOSE TO THE BGA
NVVDD is a Variable,range from 0.95 to 1.025V for G73M
144 BGA CMD MAPPING
CMD ADDR
CMD0 A3
CMD1 A0
CMD2 A2
CMD3 A1
CMD4 A3
CMD5 A4
CMD6 A5
CMD7 CS1# not use
CMD8 CS0
CMD9 WE#
CMD10 BA0
CMD11 CKE
CMD12 RESET
CMD13 A2
CMD14 A12
CMD15 RAS#
CMD16 A11
CMD17 A10
CMD18 BA1
CMD19 A8
CMD20 A9
CMD21 A6
CMD22 A5
CMD23 A7
CMD24 A4
CMD25 CAS# not use
0.5*FBVDDQ FOR DDR 4DDR2
0.7*FBVDDQ FOR DDR3
Title : G73M_FB I/F
ASUSTECH CO.,LTD.
Engineer: Jefing_Li
A6TcSKU1
Size A2
Project Name A6T
Rev 1.0
Date: Wednesday, March 08, 2006
Sheet 23 of 72



A6TcSKU1

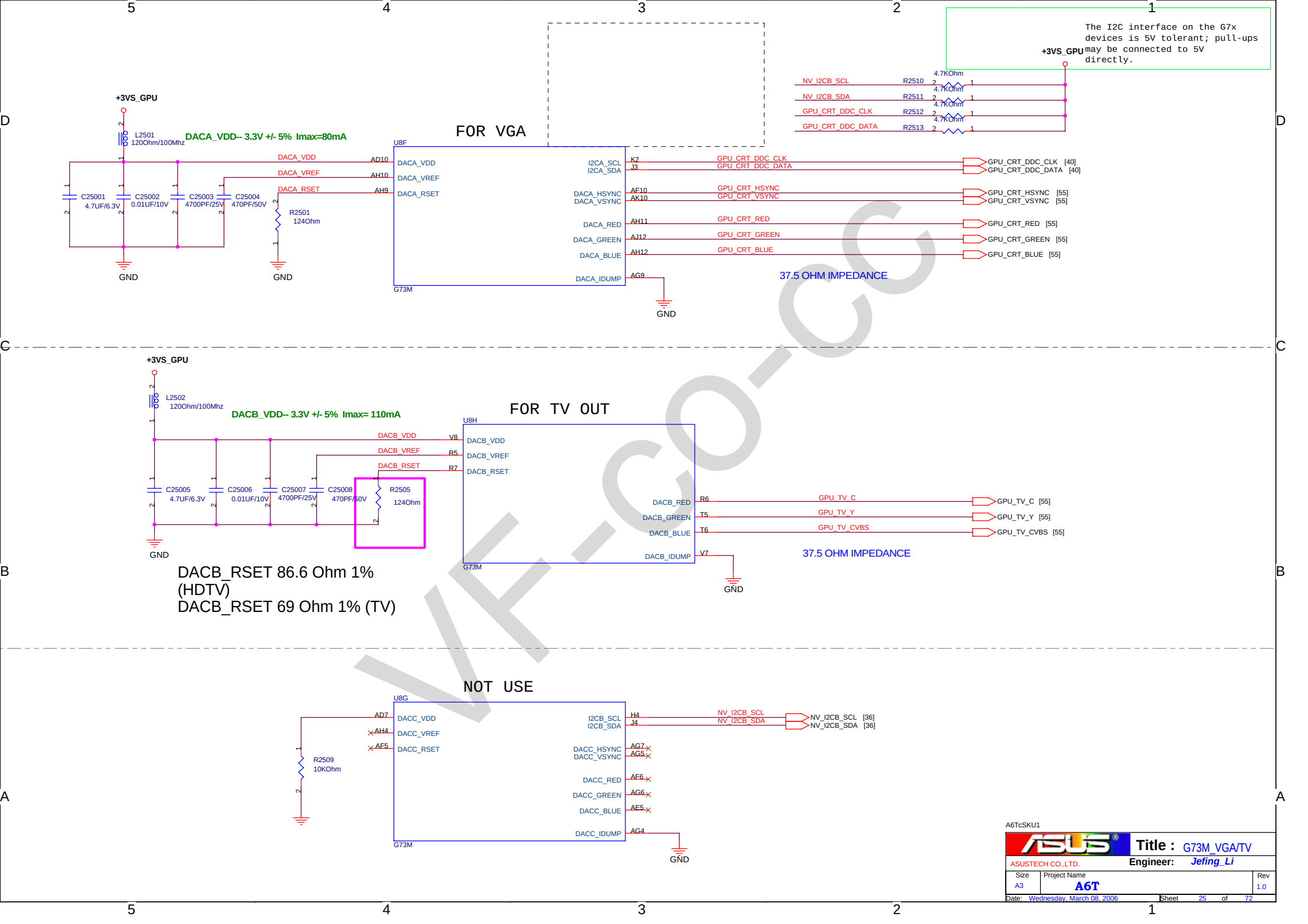
ASUSTECH CO.,LTD.

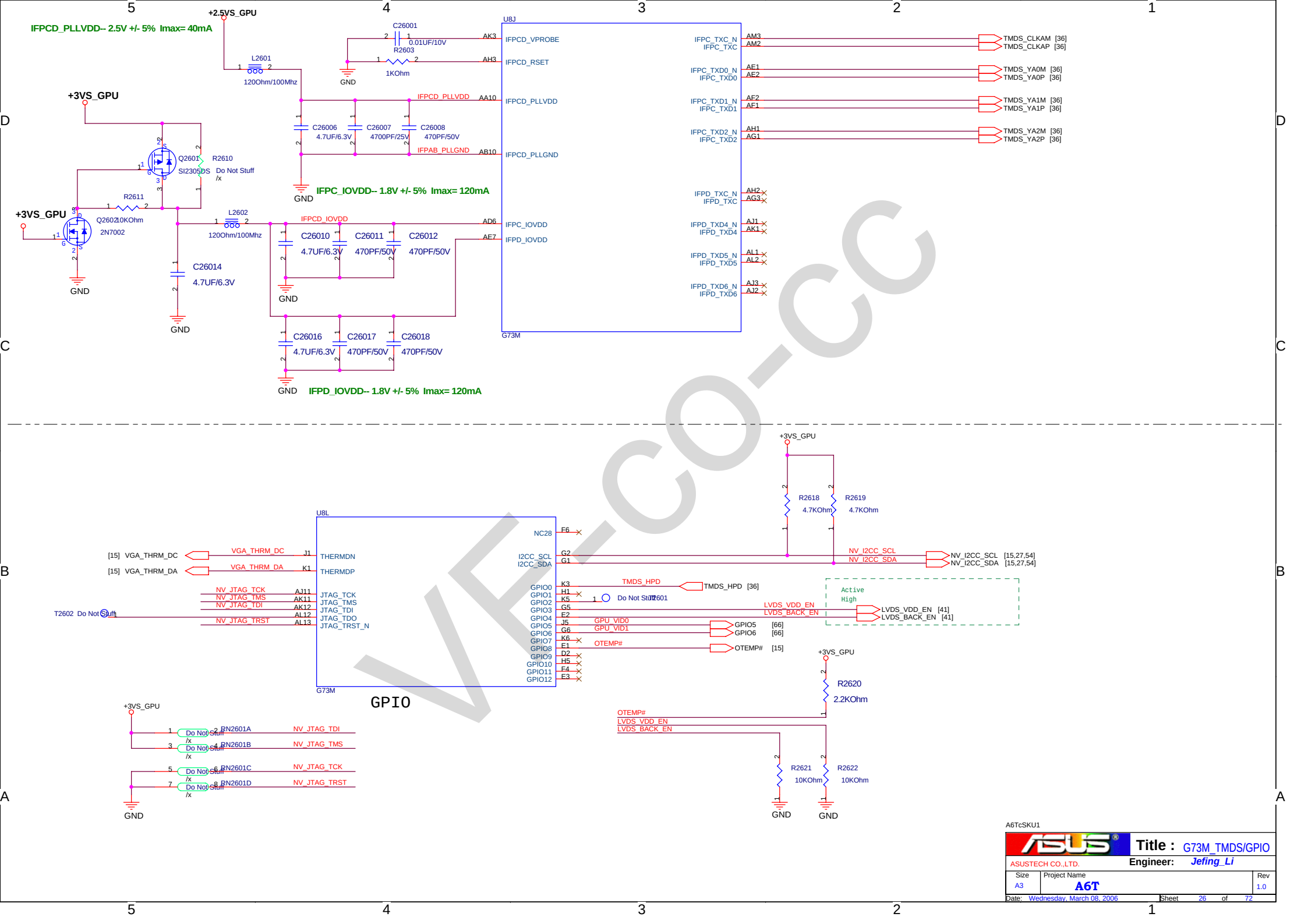
Title : G73M_LVDS/GND

Engineer: Jefing_Li

Size	Project Name	Rev
Custom	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 24 of 72


The I2C interface on the G7x devices is 5V tolerant; pull-ups may be connected to 5V directly.
+3VS_GPU
NV_I2CB_SCL R2510 4.7KOhm
NV_I2CB_SDA R2511 4.7KOhm
GPU_CRT_DDC_CLK R2512 4.7KOhm
GPU_CRT_DDC_DATA R2513 4.7KOhm
FOR VGA
+3VS_GPU
L2501 120Ohm/100Mhz
DACA_VDD-- 3.3V +/- 5% Imax=80mA
C25001 4.7UF/6.3V
C25002 0.01UF/10V
C25003 4700PF/25V
C25004 470PF/50V
R2501 124Ohm
GND
U8F
DACA_VDD AD10
DACA_VREF AH10
DACA_RSET AH9
I2CA_SCL K2
I2CA_SDA J3
DACA_HSYNC AF10
DACA_VSYNC AK10
DACA_RED AH11
DACA_GREEN AJ12
DACA_BLUE AH12
DACA_IDUMP AG9
G73M
GPU_CRT_DDC_CLK [40]
GPU_CRT_DDC_DATA [40]
GPU_CRT_HSYNC [55]
GPU_CRT_VSYNC [55]
GPU_CRT_RED [55]
GPU_CRT_GREEN [55]
GPU_CRT_BLUE [55]
37.5 OHM IMPEDANCE
FOR TV OUT
+3VS_GPU
L2502 120Ohm/100Mhz
DACB_VDD-- 3.3V +/- 5% Imax= 110mA
C25005 4.7UF/6.3V
C25006 0.01UF/10V
C25007 4700PF/25V
C25008 470PF/50V
R2505 124Ohm
U8H
DACB_VDD V8
DACB_VREF R5
DACB_RSET R7
DACB_RED R6
DACB_GREEN T5
DACB_BLUE T6
DACB_IDUMP V7
GPU_TV_C [55]
GPU_TV_Y [55]
GPU_TV_CVBS [55]
37.5 OHM IMPEDANCE
DACB_RSET 86.6 Ohm 1% (HDTV)
DACB_RSET 69 Ohm 1% (TV)
NOT USE
R2509 10KOhm
U8G
DACC_VDD AD7
DACC_VREF AH4
DACC_RSET AE5
I2CB_SCL H4
I2CB_SDA J4
DACC_HSYNC AG7
DACC_VSYNC AG5
DACC_RED AF6
DACC_GREEN AG6
DACC_BLUE AE5
DACC_IDUMP AG4
NV_I2CB_SCL [36]
NV_I2CB_SDA [36]
A6TcSKU1
Title : G73M_VGA/TV
ASUSTECH CO.,LTD.
Engineer: Jefing_Li
Size A3
Project Name A6T
Rev 1.0
Date: Wednesday, March 08, 2006
Sheet 25 of 72



A6TcSKU1

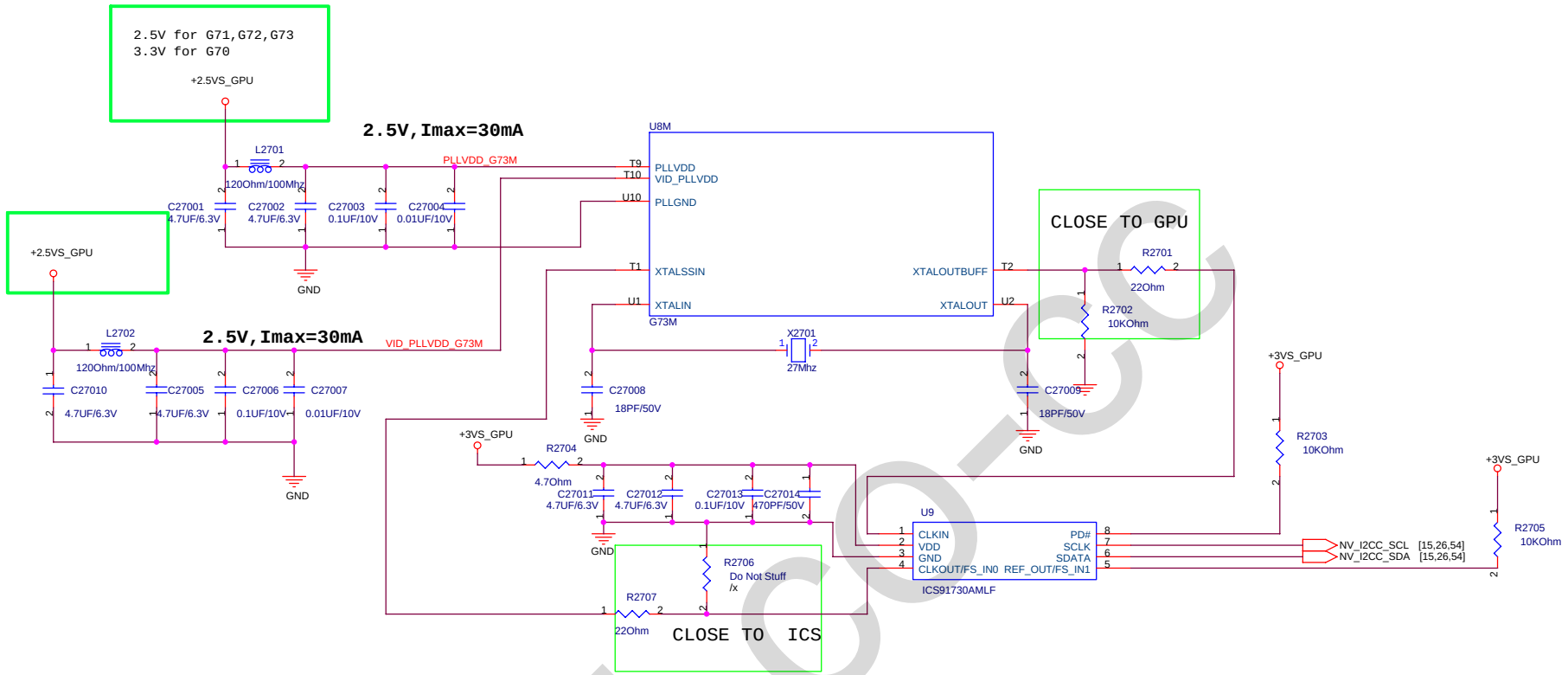
ASUSTECH CO.,LTD.

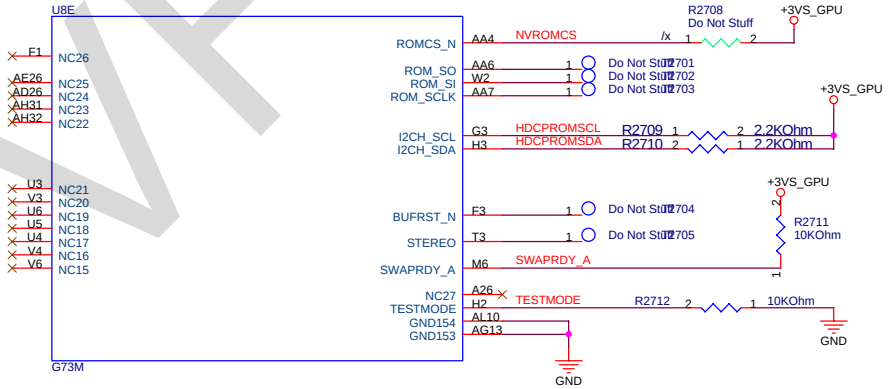
Title : G73M_TMDS/GPIO

Engineer: Jefing_Li

Size	Project Name	Rev
A3	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 26 of 72





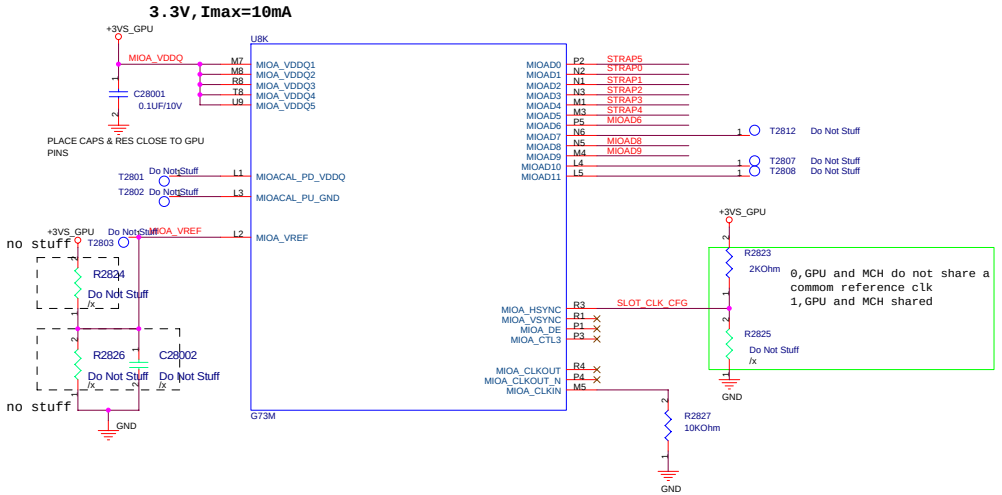
A6TcSKU1

Title : G73M_XTAL/ROM STRAP

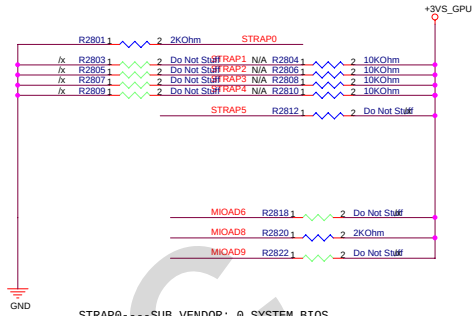
ASUSTECH CO.,LTD. Engineer: Jefing_Li

Size	Project Name	Rev
A3	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 27 of 72



STRAPS



STRAP0----SUB_VENDOR: 0,SYSTEM BIOS
1,ADAPTER BIOS

STRAP1----USER0
STRAP2----USER1
STRAP3----USER2
STRAP4----USER3

0000,XGA -/-
0001,XGA +/+
0010,SXGA +/+
0011,SXGA+ -/-
0100, UXGA +/+

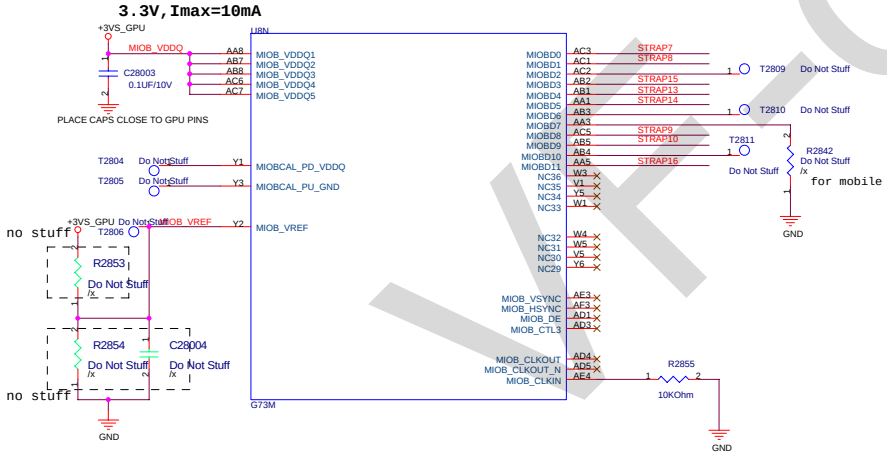
STRAP5---PEX_PLL_TERM100EN#: 0,ENABLE INTERNAL TERMINATION 100 OHM
1,DISABLE

STRAP19----TVMODE0
STRAP20----TVMODE1

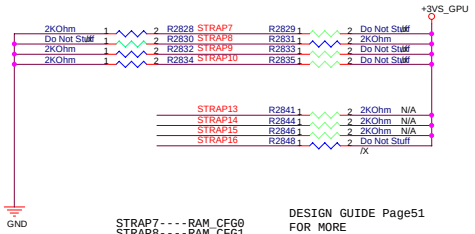
00, SECAM
01, NTSC
10, PAL
11, CRT

MIOAD6----3GIO_PADCFG0
MIOAD8----3GIO_PADCFG1
MIOAD9----3GIO_PADCFG2

001,FOR NV43/NV44;
010,FOR G7x,NV42



STRAP



STRAP7----RAM_CFG0
STRAP8----RAM_CFG1
STRAP9----RAM_CFG2
STRAP10----RAM_CFG3

DESIGN GUIDE Page51
FOR MORE
INFORMATION
0,FULL WIDTH 1,HALF WIDTH

STRAP11----CRYSTAL0
STRAP12----CRYSTAL1

00,13.5MHZ
01,14.318MHZ
10,27MHZ
11,RESERVED

STRAP13----PCI_DEVID0
STRAP14----PCI_DEVID1
STRAP15----PCI_DEVID2
STRAP16----PCI_DEVID3

0000,NV41-U
0001,NV41
0010,NV41-V
1000,NV41M
1001,NV41M-U
1110,NV41-GL

0111,G72M-V
1000,G73M

STRAP17----ROMTYPE0
STRAP18----ROMTYPE1

00,PARALLEL
01,SERIAL AT25F
10,SERIAL SST45VF
11,RESERVED

A6TcSKU1

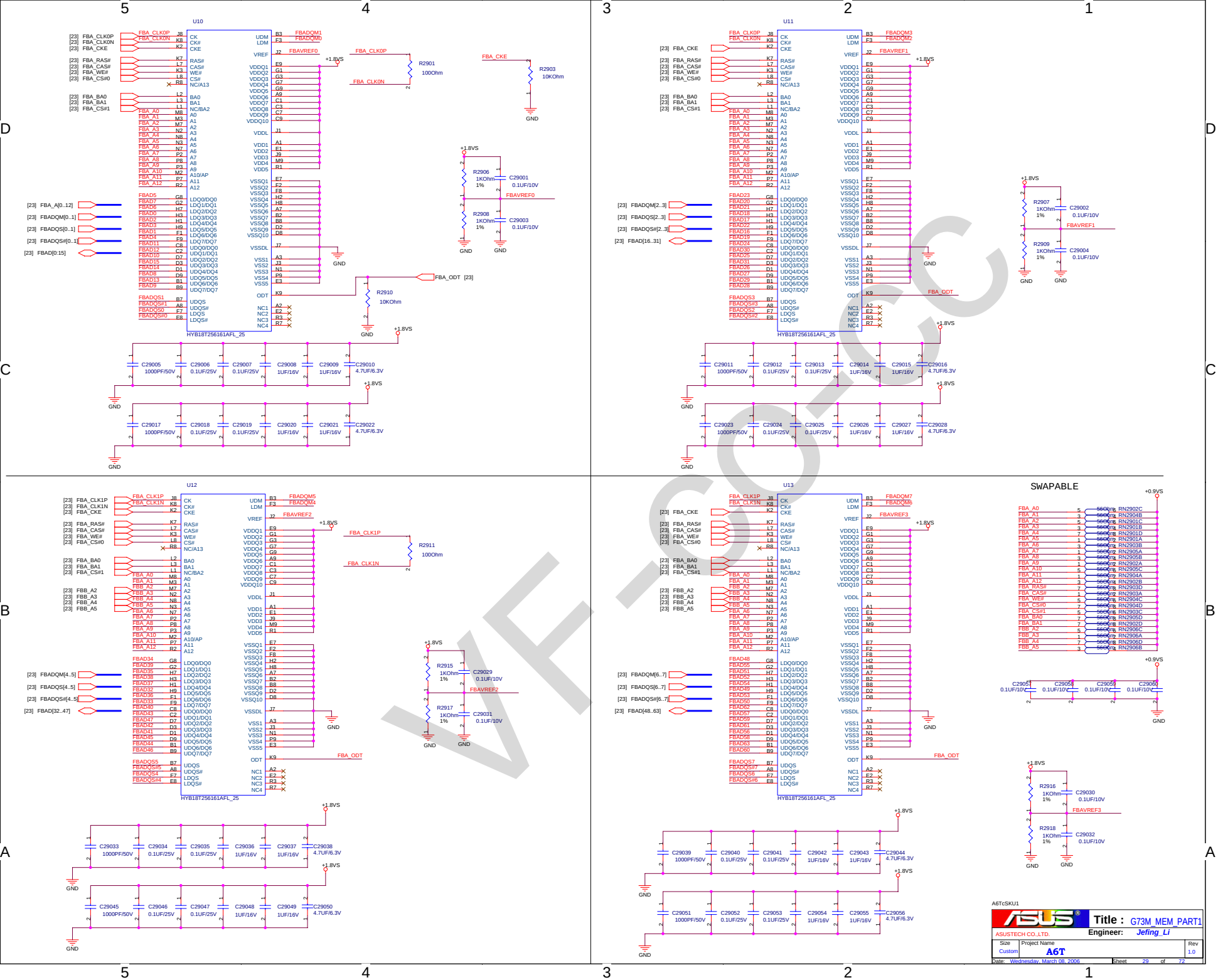
ASUSTECH CO.,LTD.

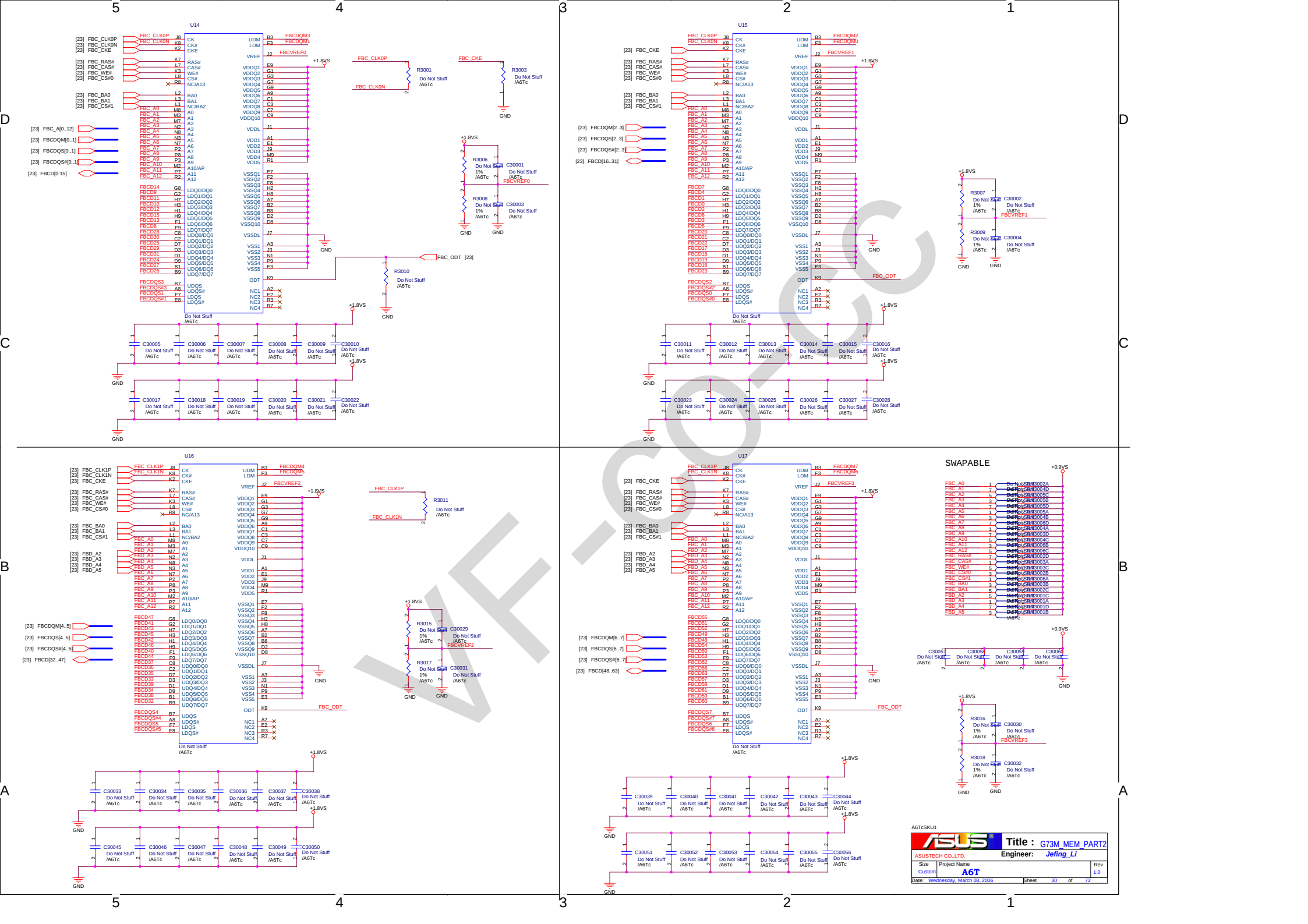
Title : G73M_STRAPS

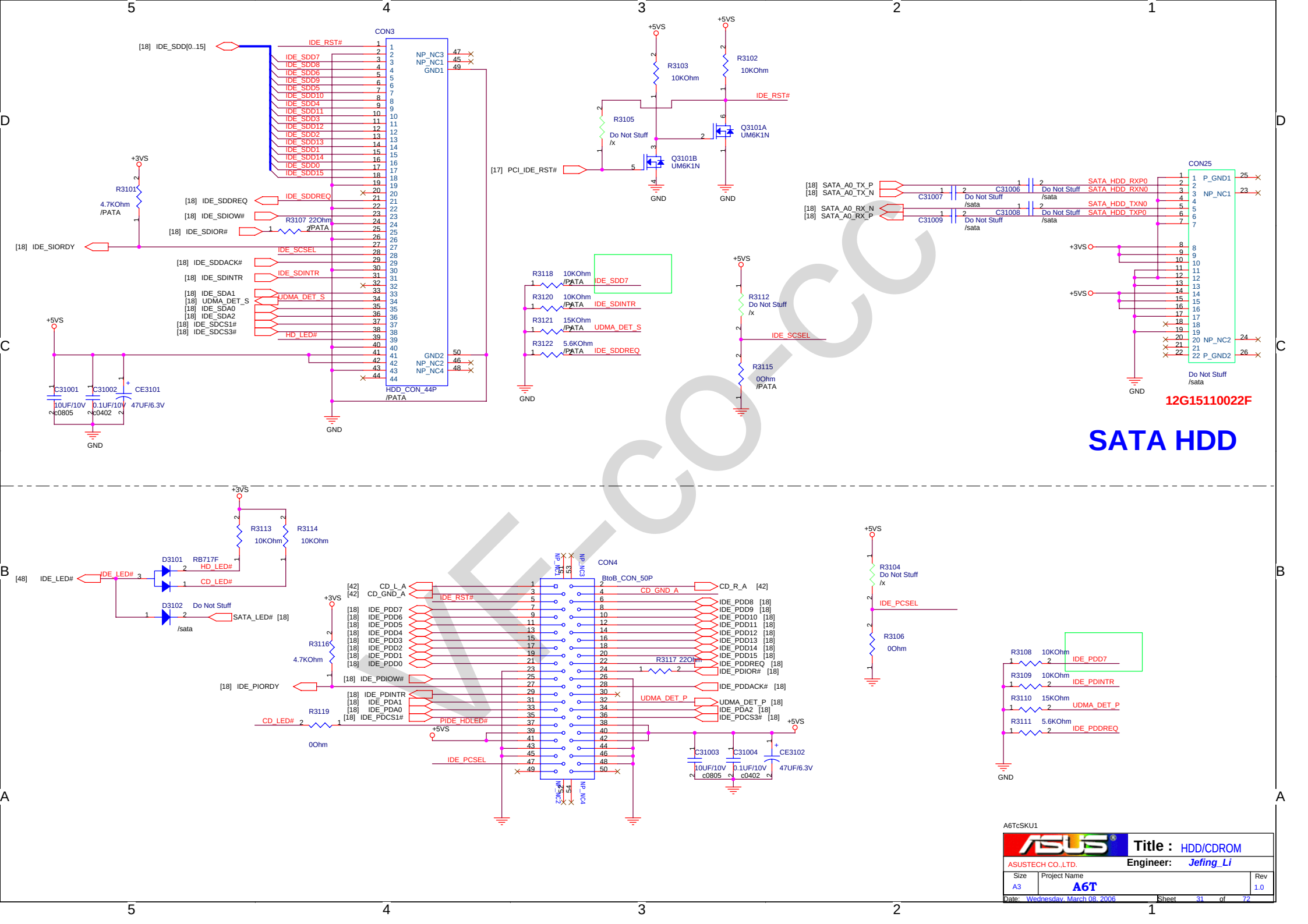
Engineer: Jefing_Li

Size	Project Name	Rev
C	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 28 of 72


U10
HYB18T256161AFL_25
U11
HYB18T256161AFL_25
U12
HYB18T256161AFL_25
U13
HYB18T256161AFL_25
SWAPABLE
Title : G73M_MEM_PART1
Engineer: Jefing_Li
ASUSTECH CO.,LTD.
Size Custom
Project Name A6T
Rev 1.0
Date: Wednesday, March 08, 2006
Sheet 29 of 72
A6TcSKU1


U14
U15
U16
U17
SWAPABLE
Title : G73M_MEM_PART2
Engineer: Jefing_Li
ASUSTECH CO.,LTD.
A6T
Wednesday, March 08, 2006
Do Not Stuff /A6Tc
+1.8VS
+0.9VS
GND


CON3
HDD_CON_44P
/PATA
R3101
4.7KOhm
/PATA
R3107 22Ohm
/PATA
R3103
10KOhm
R3102
10KOhm
R3105
Do Not Stuff
/x
Q3101A
UM6K1N
Q3101B
UM6K1N
R3118 10KOhm /PATA
R3120 10KOhm /PATA
R3121 15KOhm /PATA
R3122 5.6KOhm /PATA
R3112
Do Not Stuff
/x
R3115
0Ohm
/PATA
CON25
C31006
C31007
C31008
C31009
Do Not Stuff
/sata
C31001
C31002
CE3101
10UF/10V c0805
0.1UF/10V c0402
47UF/6.3V
12G15110022F
SATA HDD
D3101 RB717F
D3102 Do Not Stuff
/sata
R3113
10KOhm
R3114
10KOhm
R3116
4.7KOhm
R3119
0Ohm
CON4
BtoB_CON_50P
R3117 22Ohm
R3104
Do Not Stuff
/x
R3106
0Ohm
R3108 10KOhm IDE_PDD7
R3109 10KOhm IDE_PDINTR
R3110 15KOhm UDMA_DET_P
R3111 5.6KOhm IDE_PDDREQ
C31003
C31004
CE3102
10UF/10V c0805
0.1UF/10V c0402
47UF/6.3V
A6TcSKU1
Title : HDD/CDROM
ASUSTECH CO.,LTD.
Engineer: Jefing_Li
Size A3
Project Name A6T
Rev 1.0
Date: Wednesday, March 08, 2006
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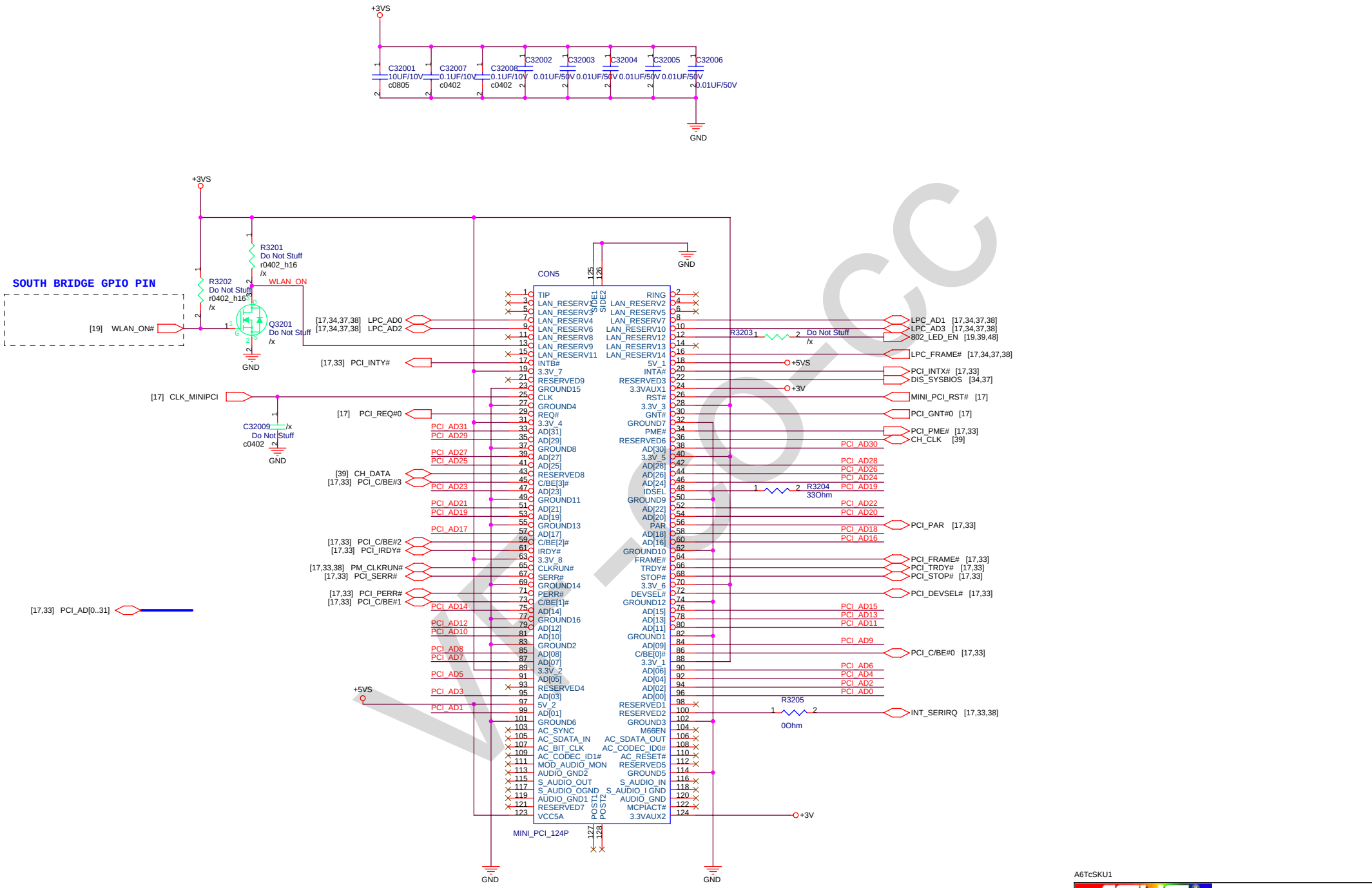
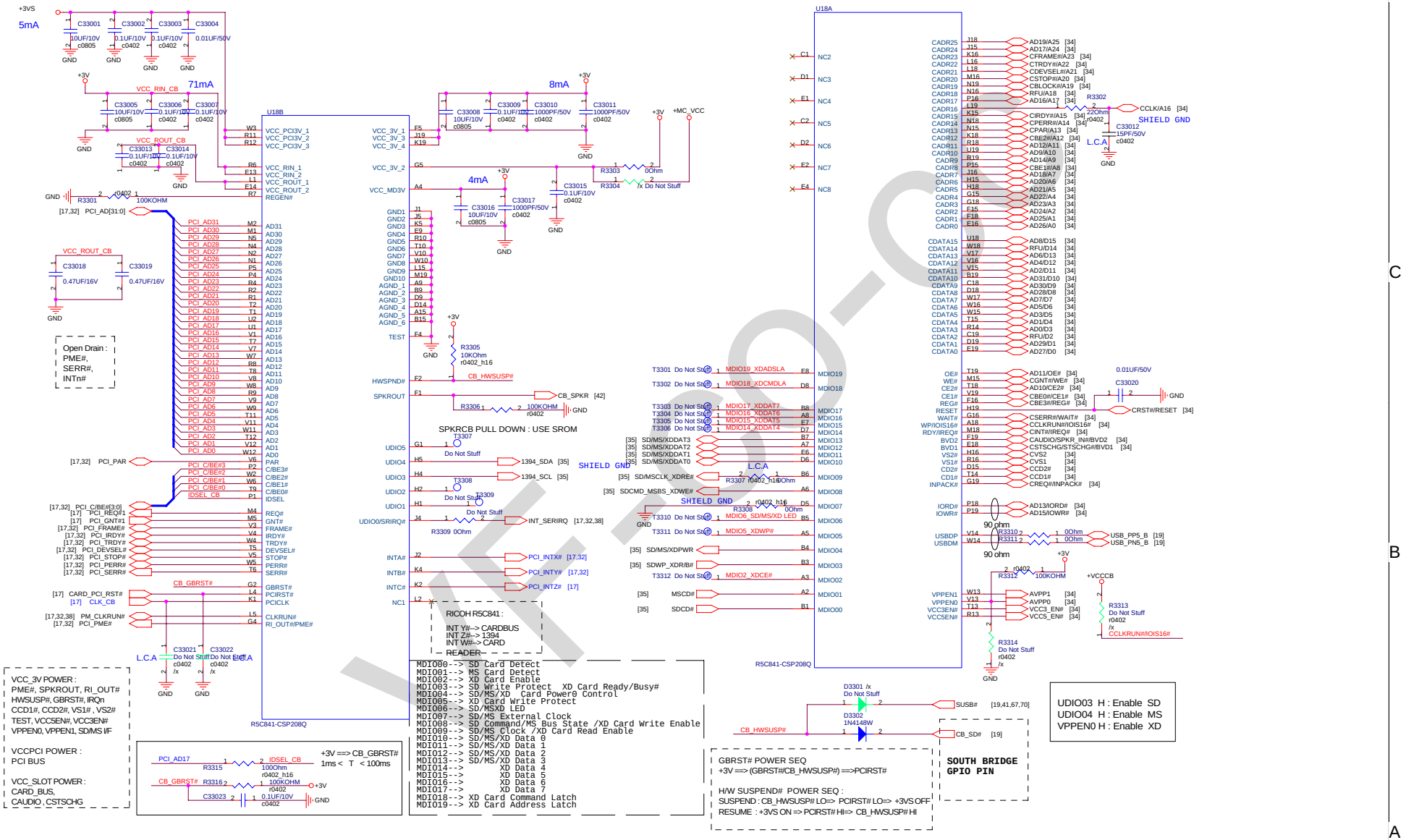


A6TcSKU1

ASUSTECH CO.,LTD.	Title : MINI PCI	
	Engineer: Jefing_Li	
Size: A3	Project Name: A6T	Rev: 1.0
Date: Wednesday, March 08, 2006	Sheet 32 of 72	



A6TcSKU1

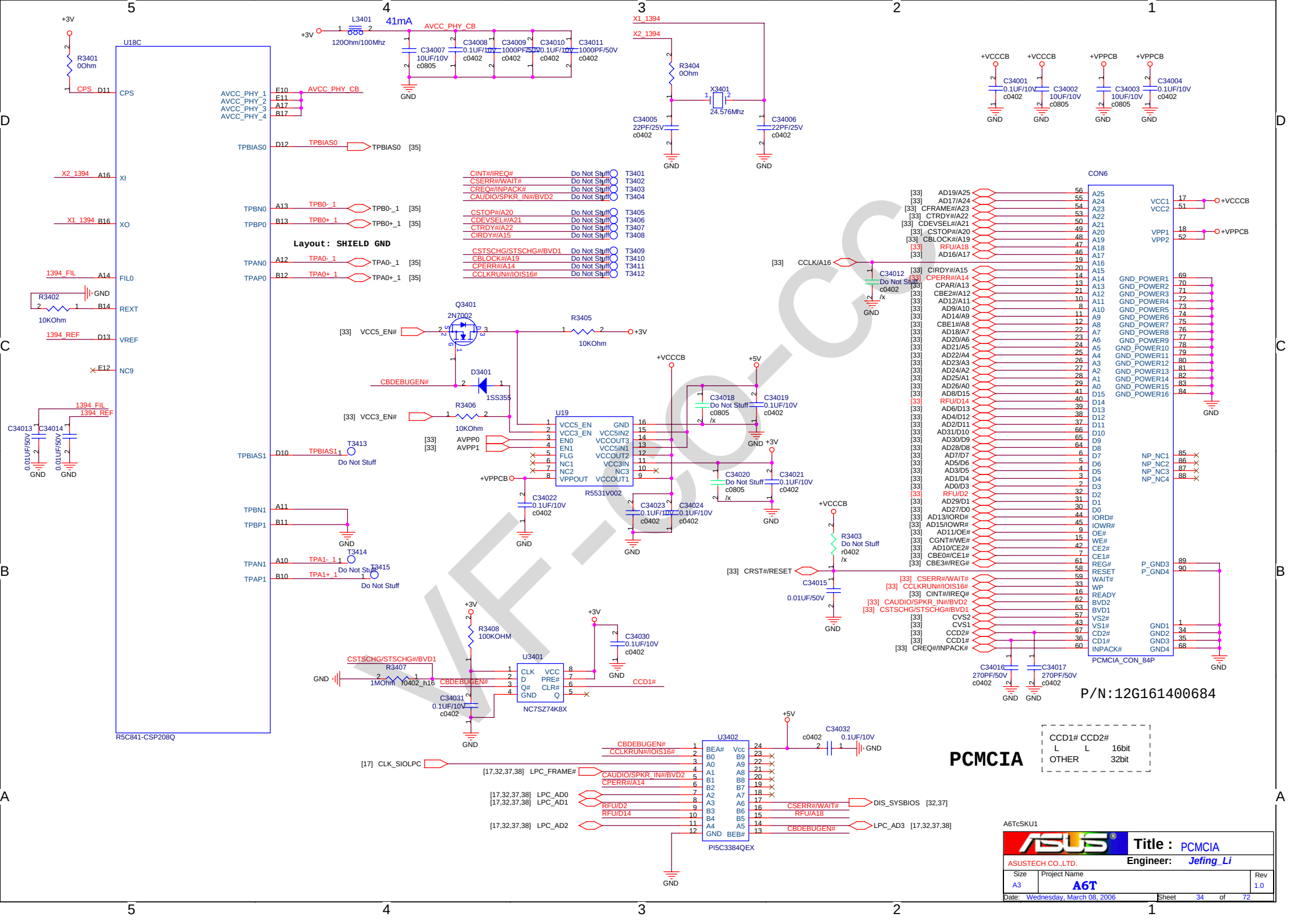
ASUSTECH CO.,LTD.

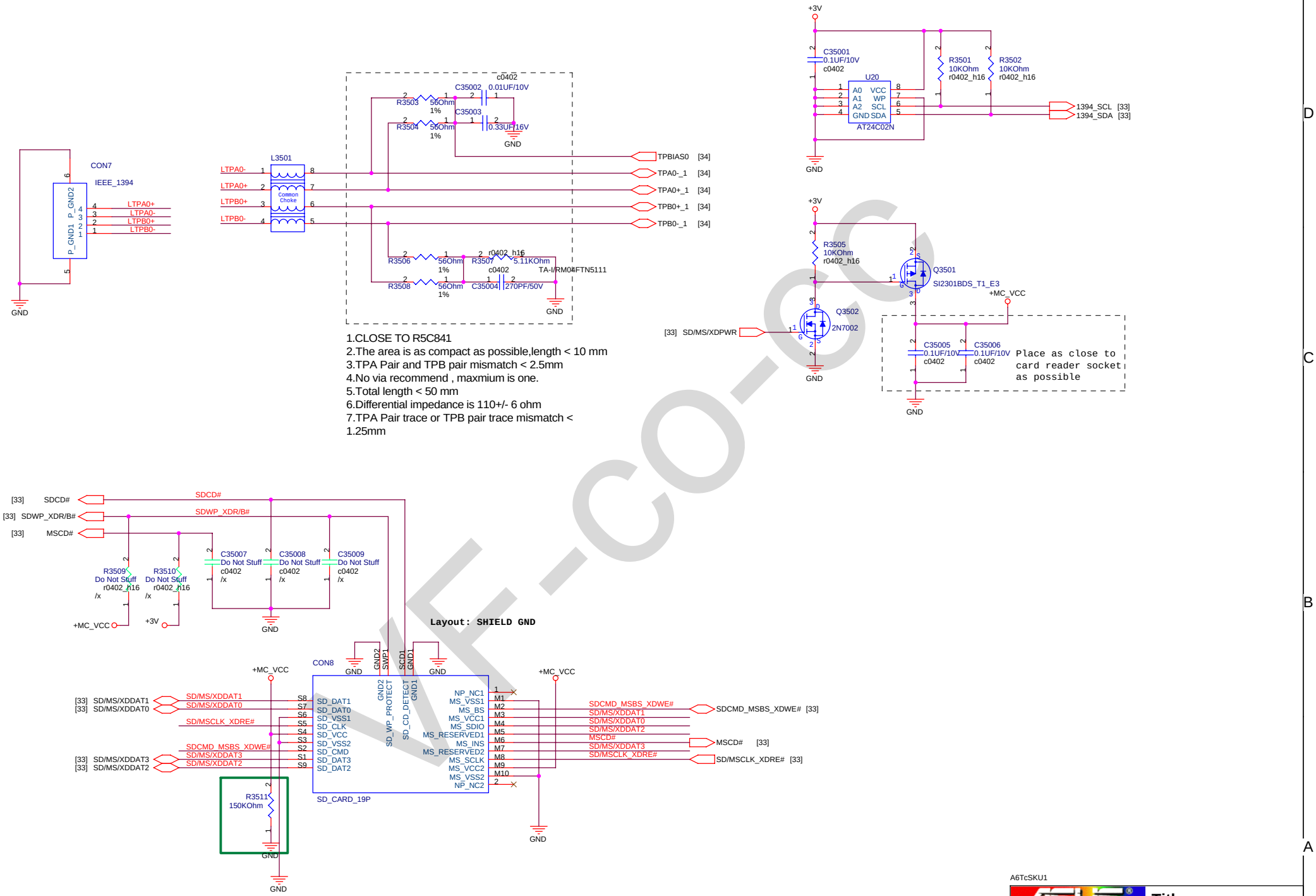
Title : CARD BUS

Engineer: Jefing_Li

Size	Project Name	Rev
C	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 33 of 72

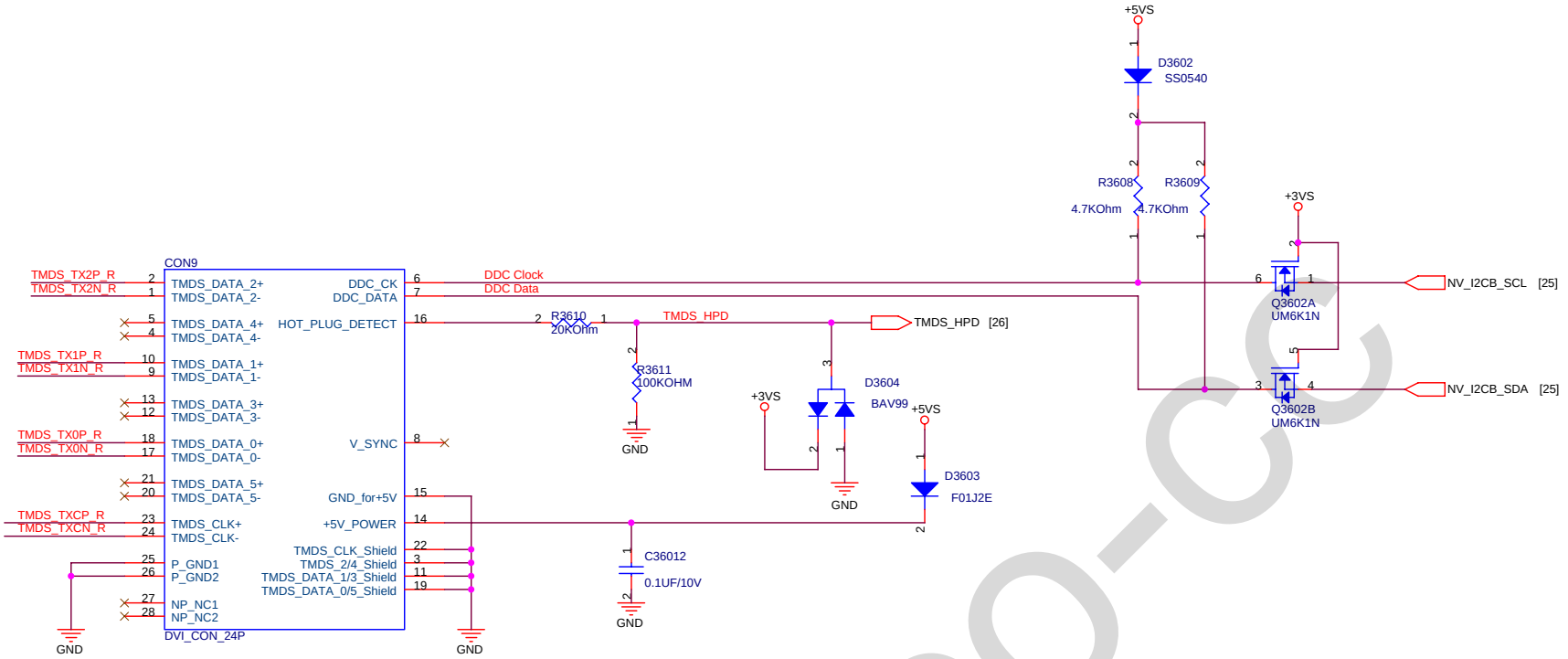

PCMCIA
P/N:12G161400684
Layout: SHIELD GND
41mA
R5C841-CSP208Q
U18C
CON6
PCMCIA_CON_84P
R5531V002
NC7SZ74K8X
PI5C3384QEX
CCD1# CCD2#
L L 16bit
OTHER 32bit
Title : PCMCIA
ASUSTECH CO.,LTD.
Engineer: Jefing_Li
Project Name A6T
Size A3
Rev 1.0
Date: Wednesday, March 08, 2006
Sheet 34 of 72
A6TcSKU1

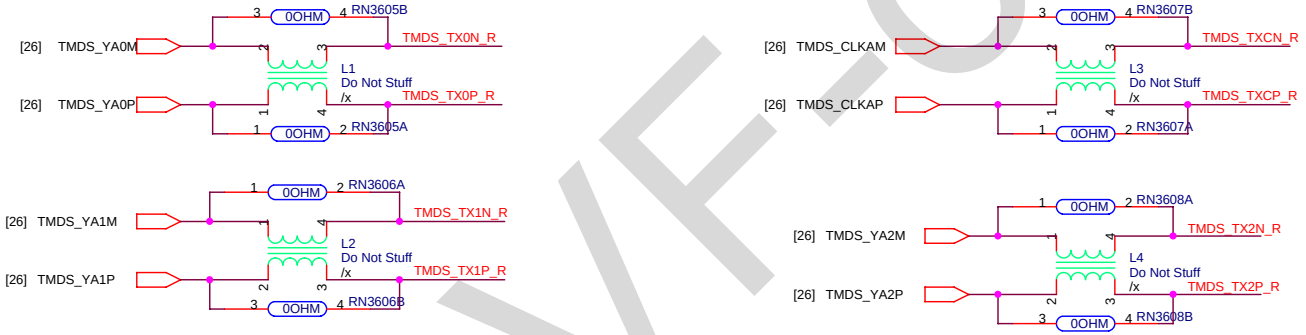


1.CLOSE TO R5C841
2.The area is as compact as possible,length < 10 mm
3.TPA Pair and TPB pair mismatch < 2.5mm
4.No via recommend , maxmium is one.
5.Total length < 50 mm
6.Differential impedance is 110+/- 6 ohm
7.TPA Pair trace or TPB pair trace mismatch < 1.25mm

A6TcSKU1

ASUSTECH CO.,LTD.	Title : 1394/SD_CARD	
	Engineer: Jefing_Li	
Size: A3	Project Name: A6T	Rev: 1.0
Date: Wednesday, March 08, 2006	Sheet 35 of 72	





A6TcSKU1

ASUSTECH CO.,LTD.

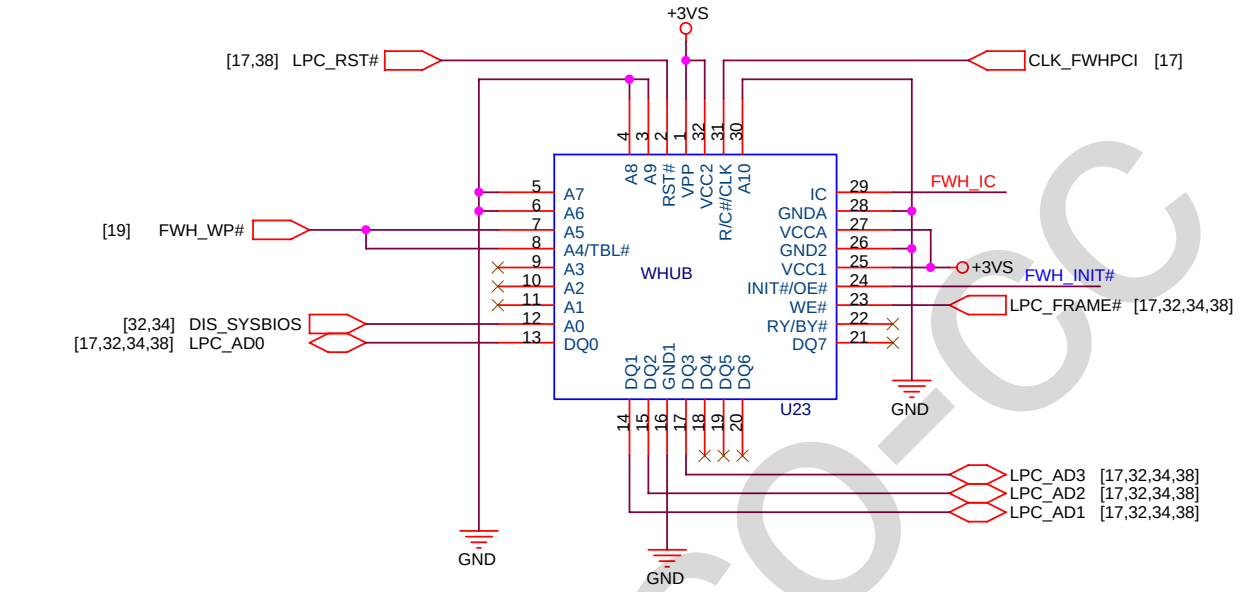
Title : SIO/SIR/DVI

Engineer: Jefing_Li

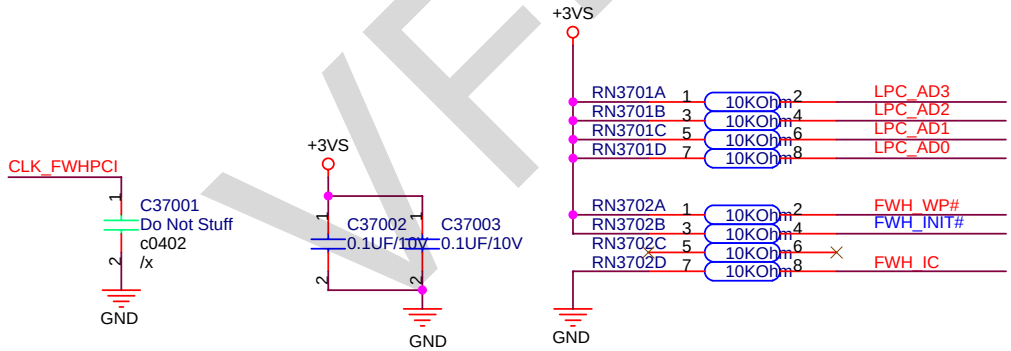
Size	Project Name	Rev
B	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 36 of 72

FWH



PLCC32 Socket Part Number : 12-043000323
SST FWH/LPC Part Number :
05G00101712L(燒)



A6TcSKU1

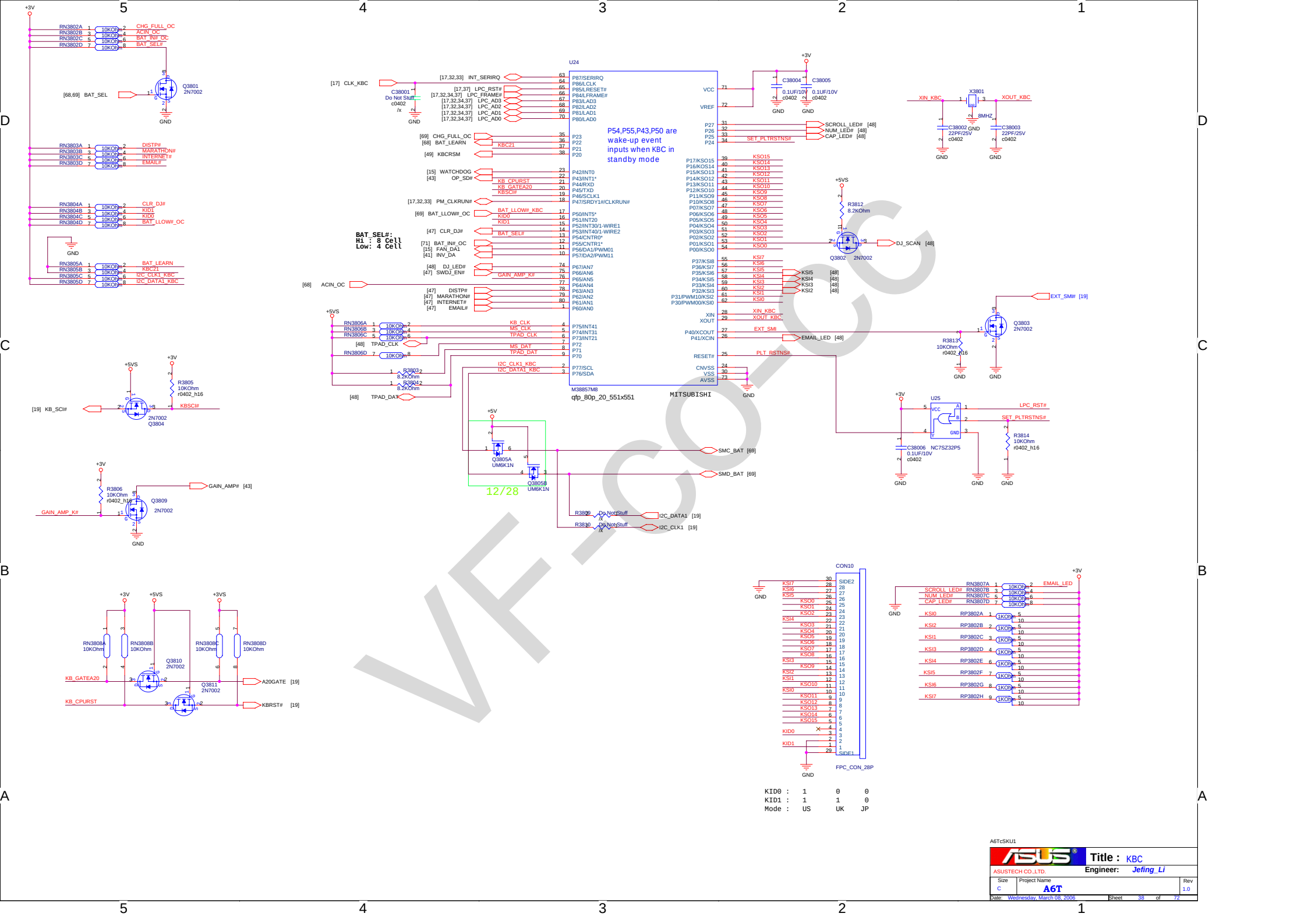
ASUSTECH CO.,LTD.

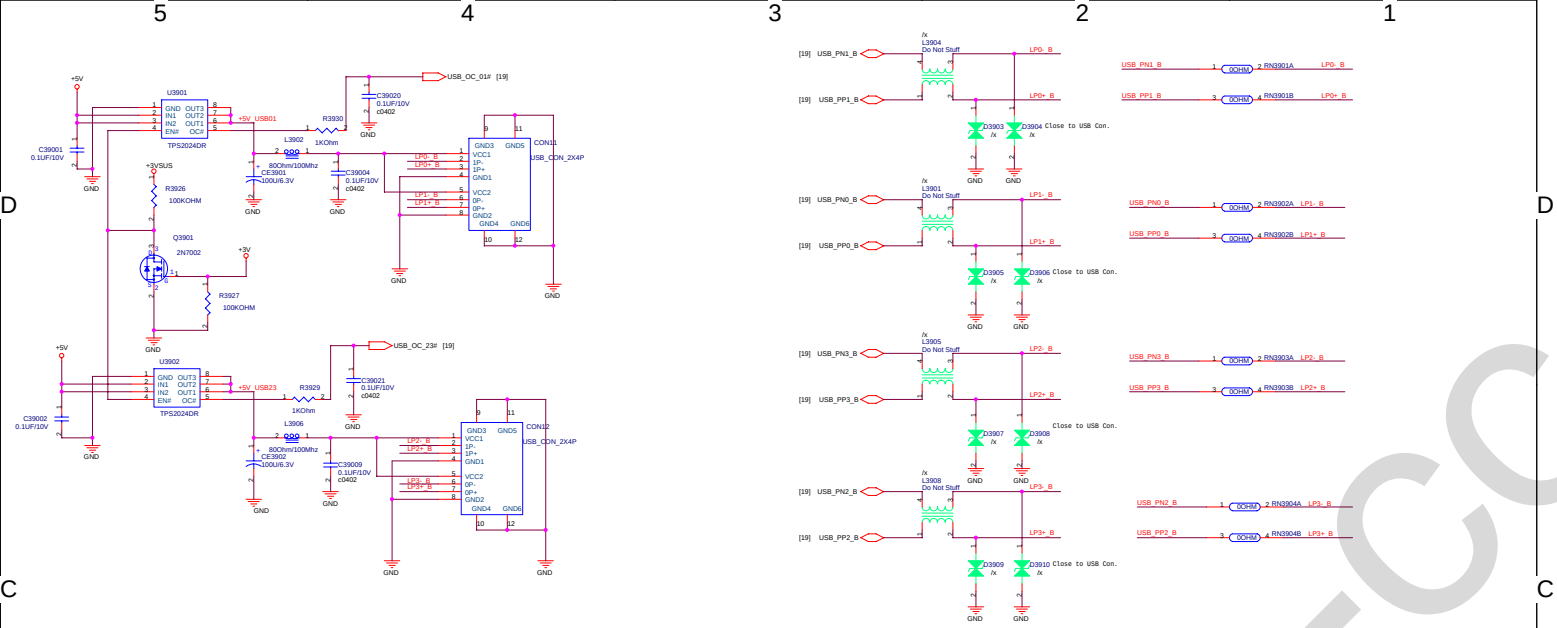
Title : FWH

Engineer: Jefing_Li

Size	Project Name	Rev
A4	A6T	1.0

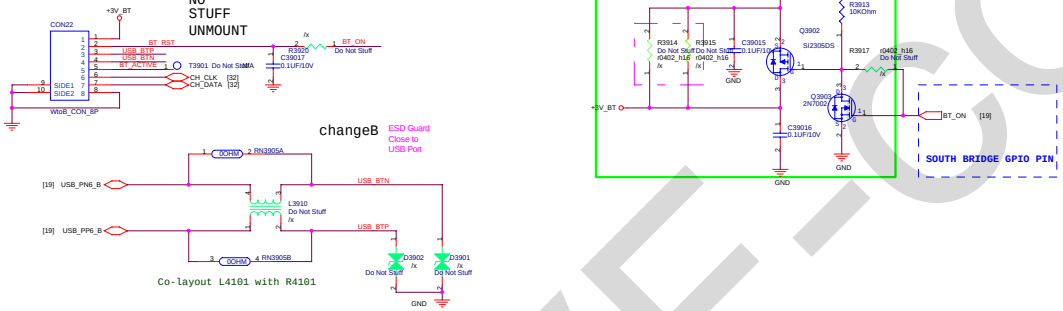
Date: Wednesday, March 08, 2006 Sheet 37 of 72


U24
M38857M8
qfp_80p_20_551x551
MITSUBISHI
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
BAT_SEL#:
Hi : 8 Cell
Low: 4 Cell
KID0 : 1 0 0
KID1 : 1 1 0
Mode : US UK JP
12/28
A6TcSKU1
Title : KBC
ASUSTECH CO.,LTD.
Engineer: Jefing_Li
Project Name
A6T
Date: Wednesday, March 08, 2006
Sheet 38 of 72
VF-CO-CC

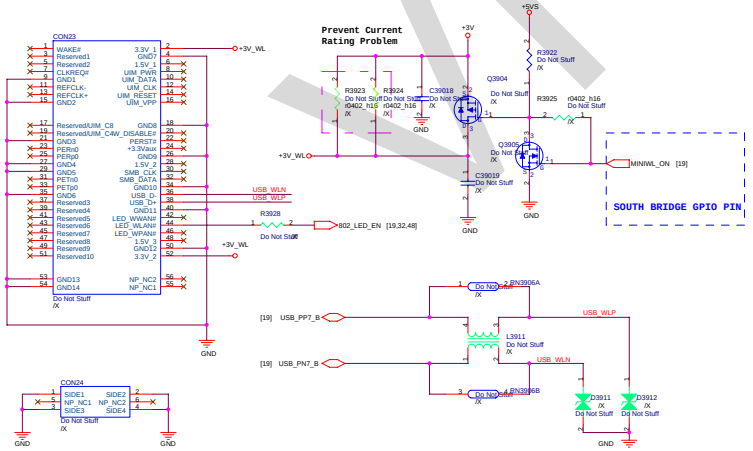


BLUE TOOTH MOLUDE

NO STUFF UNMOUNT



USB WIRELESS LAN



A6TcSKU1

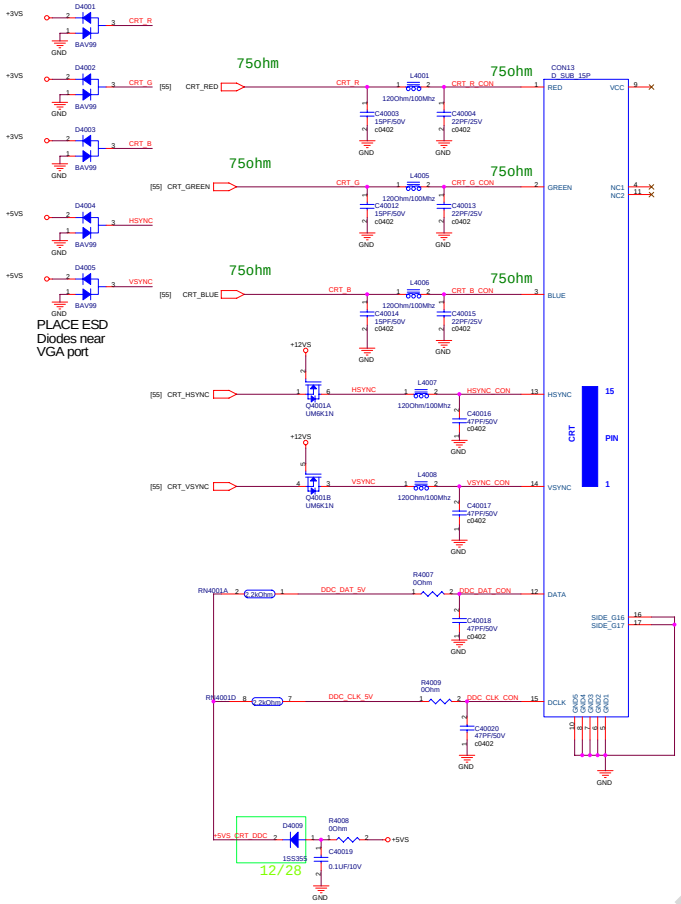
ASUSTeK COMPUTER INC.

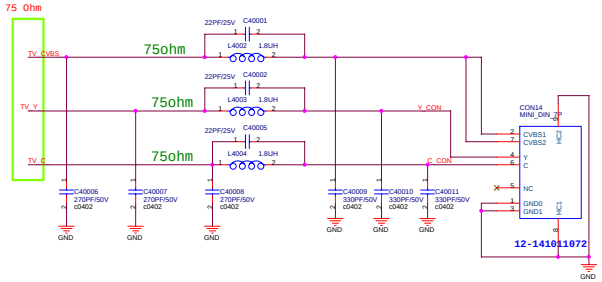
Title : USB/BLUE TOOTH

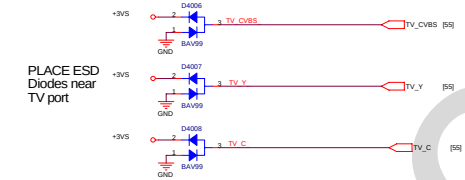
Engineer: Jefing_Li

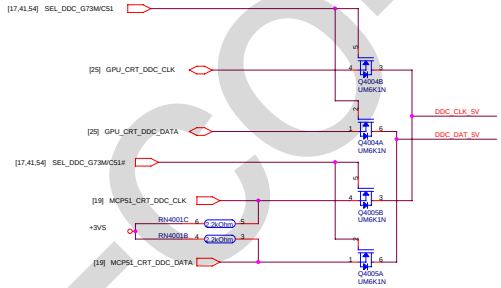
Size	Project Name	Rev
Custom	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 39 of 72









A6TcSKU1

ASUSTeK COMPUTER INC.

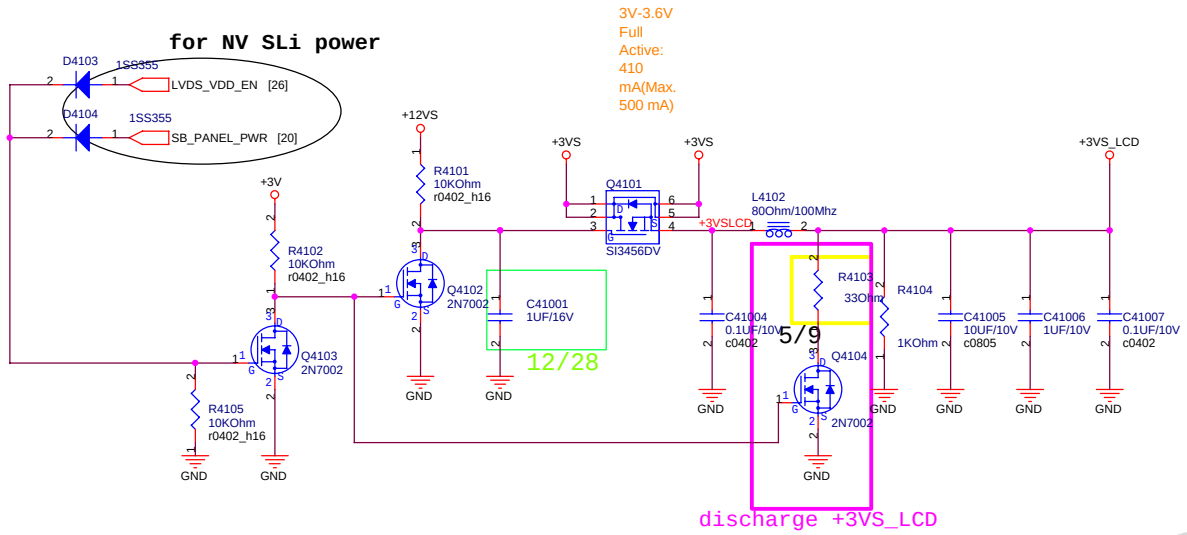
Title : CRT/TV CON

Engineer: Jefing_Li

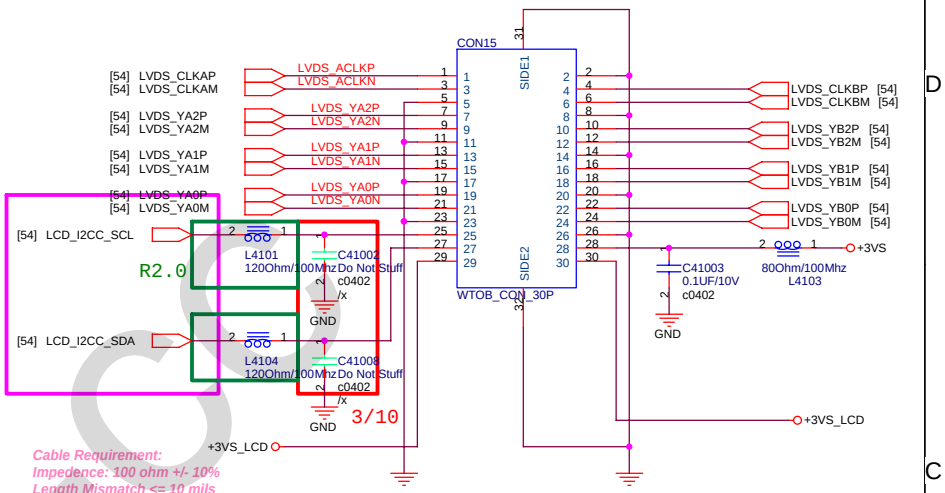
Size	Project Name	Rev
Custom	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 40 of 72

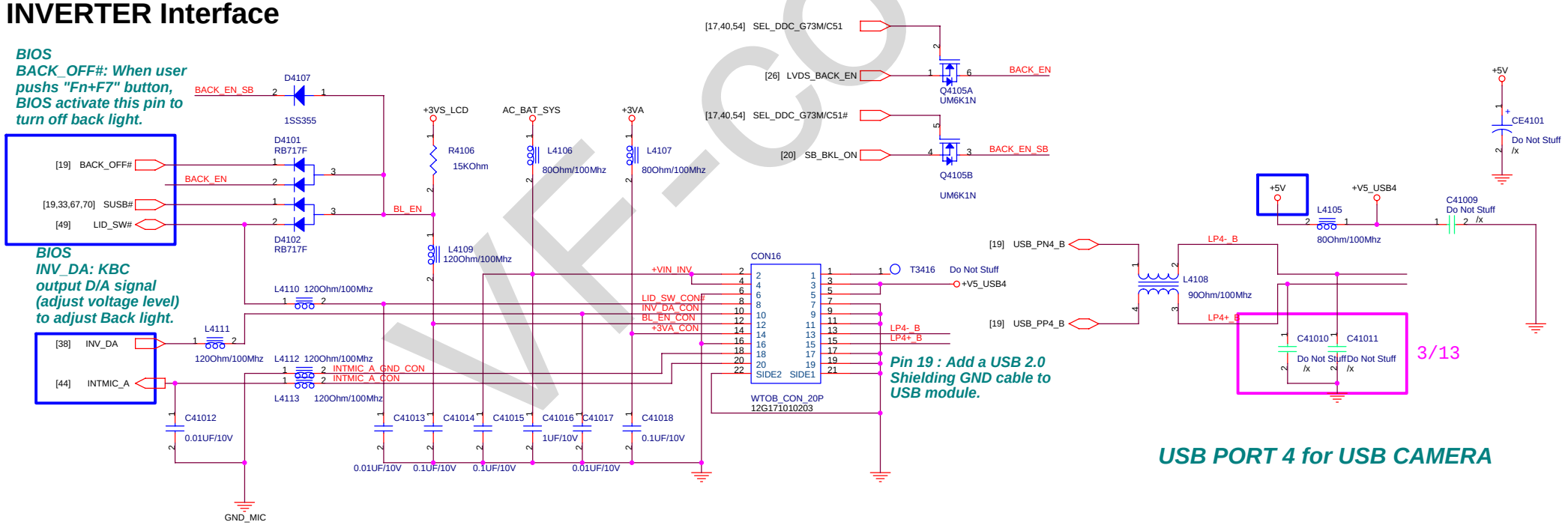
LCD Power



LCD LVDS Interface



INVERTER Interface



A6TcSKU1

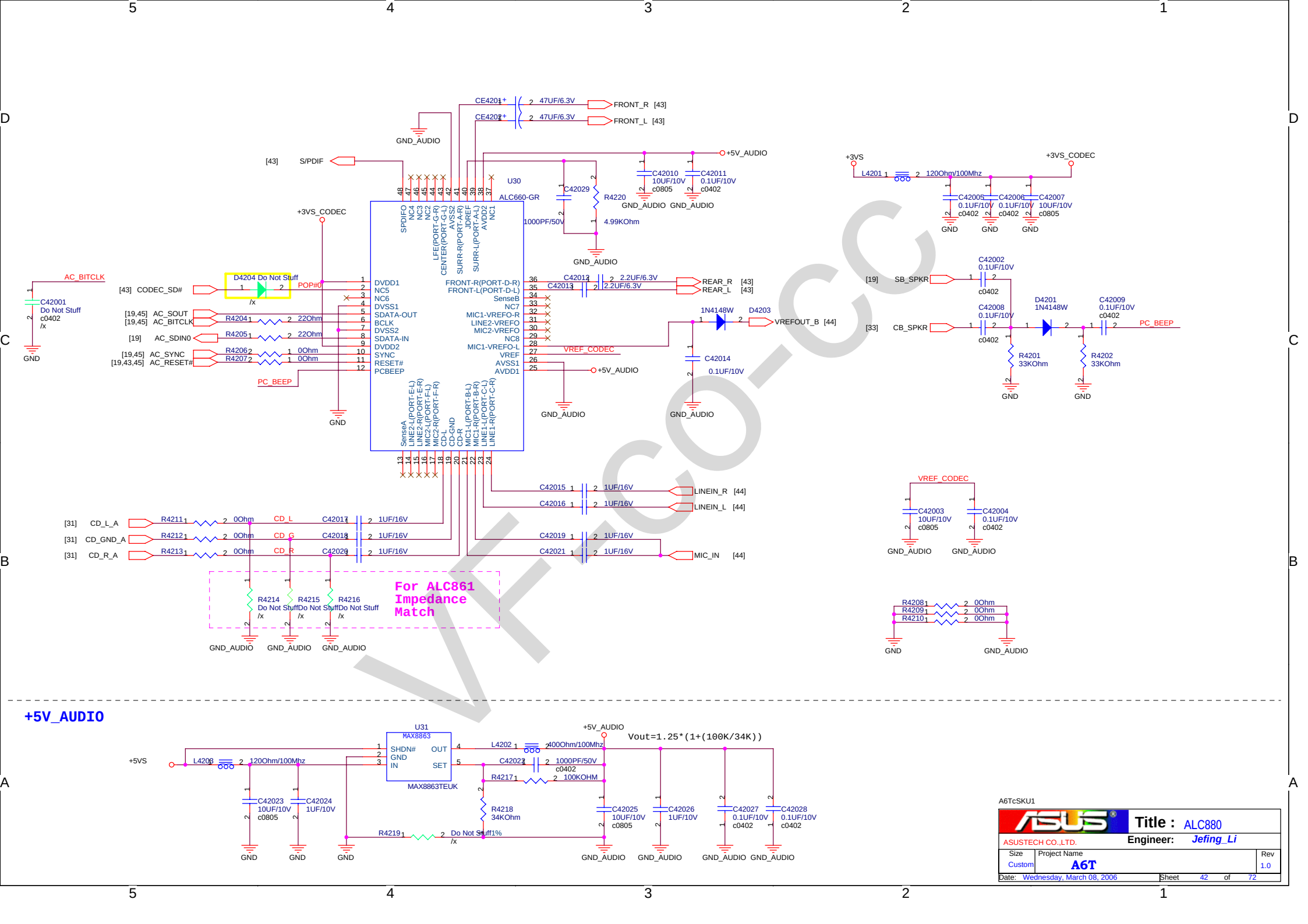
ASUSTECH CO.,LTD.

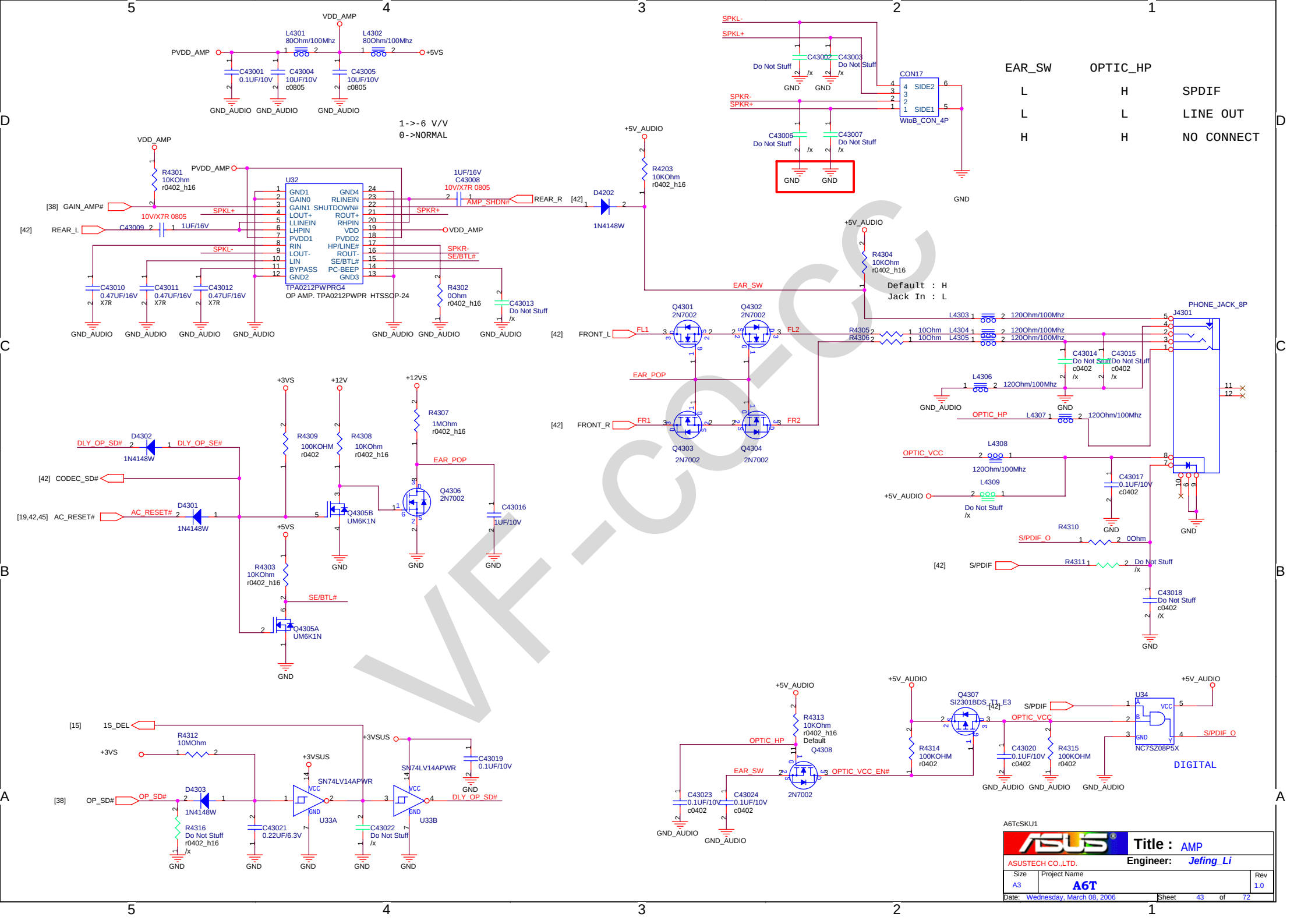
Title : LVDS/INVERTER

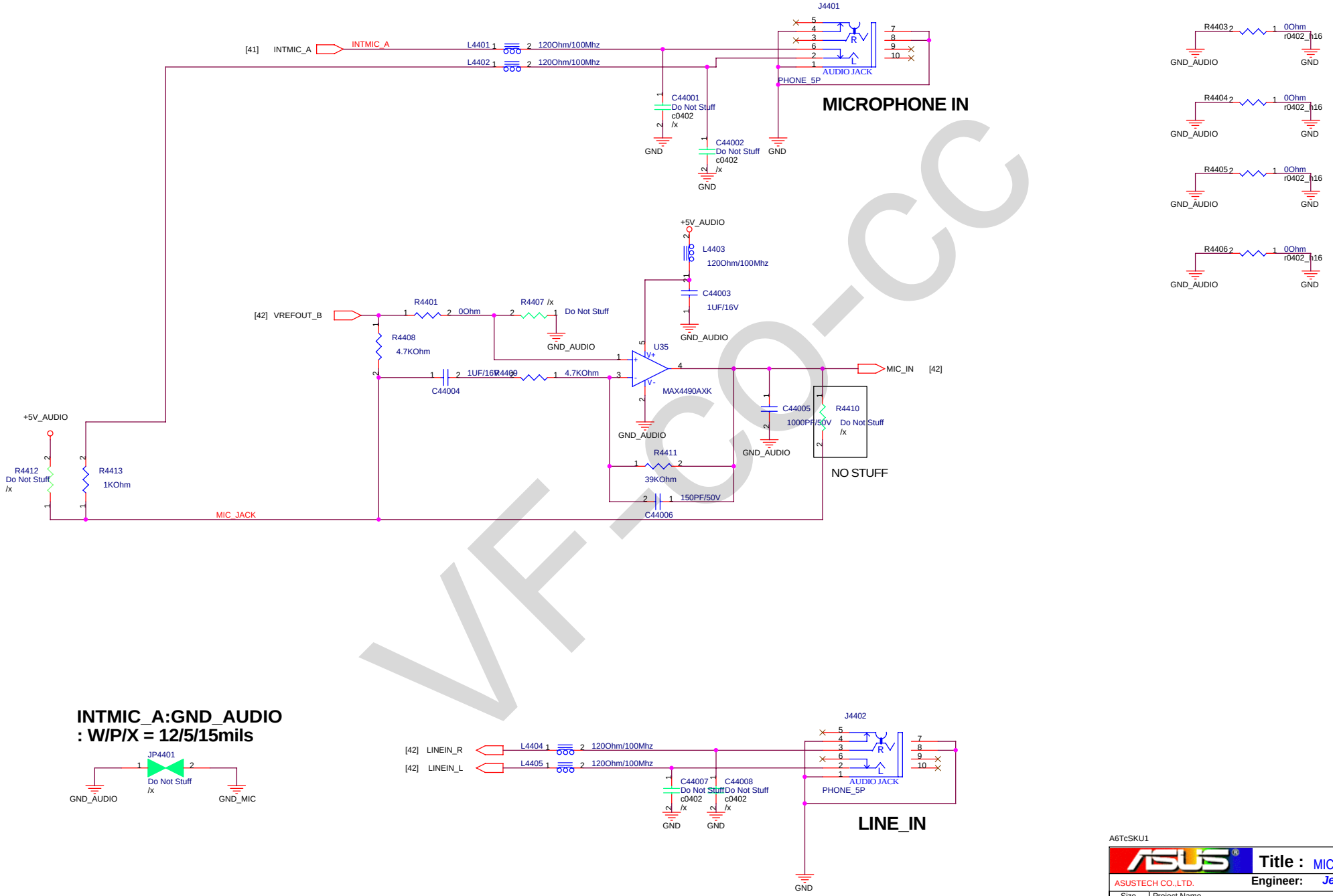
Engineer: Jefing_Li

Size	Project Name	Rev
A3	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 41 of 72


U30
ALC660-GR
U31
MAX8863
MAX8863TEUK
+5V_AUDIO
Vout=1.25*(1+(100K/34K))
For ALC861
Impedance
Match
VF-CO-CC
A6TcSKU1
Title : ALC880
ASUSTECH CO.,LTD.
Engineer: Jefing_Li
Project Name A6T
Rev 1.0
Date: Wednesday, March 08, 2006
Sheet 42 of 72

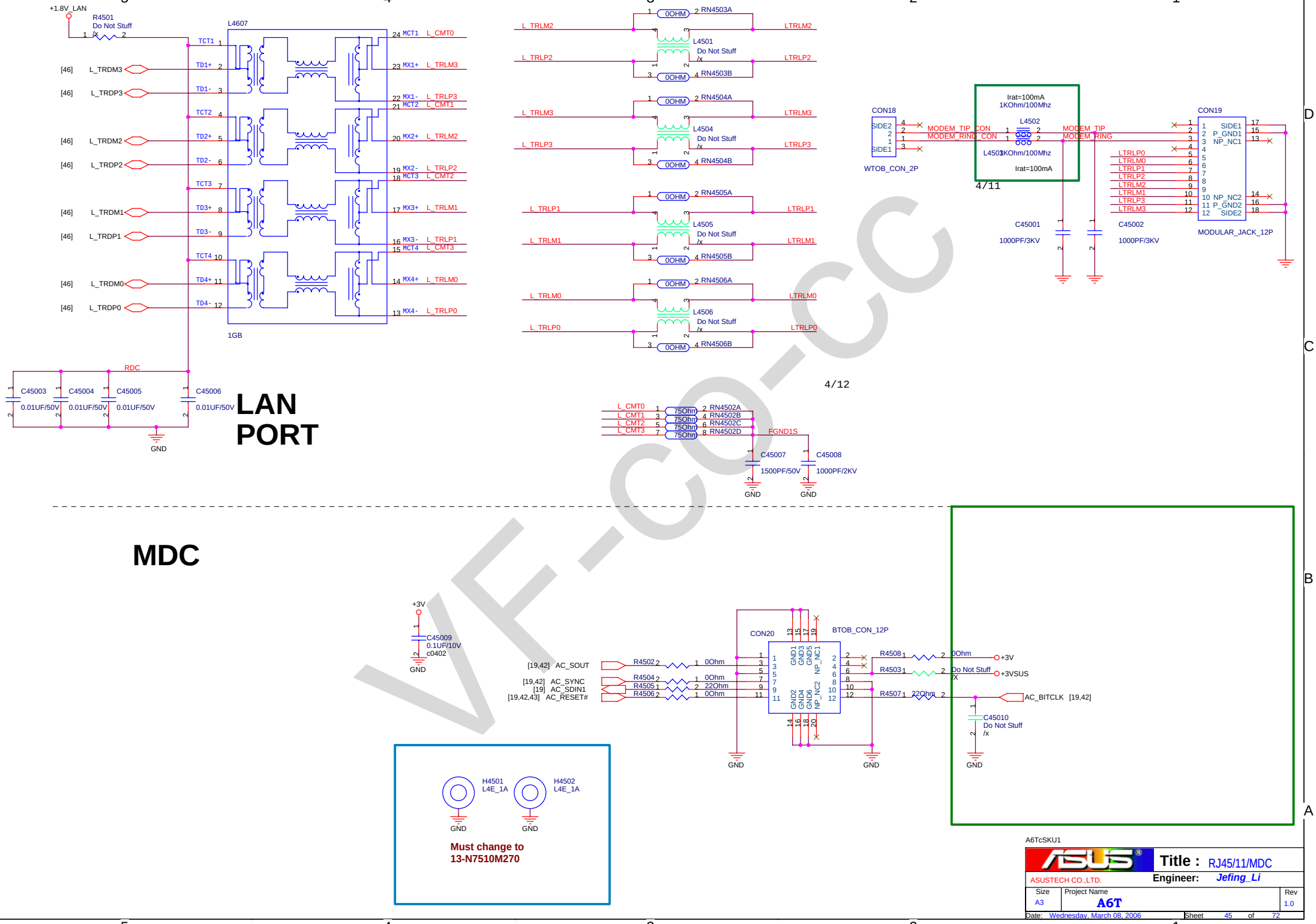

VDD_AMP
L4301 80Ohm/100Mhz
L4302 80Ohm/100Mhz
PVDD_AMP
+5VS
C43001 0.1UF/10V
C43004 10UF/10V c0805
C43005 10UF/10V c0805
GND_AUDIO
1->-6 V/V
0->NORMAL
R4301 10KOhm r0402_h16
U32
TPA0212PWPRG4
OP AMP. TPA0212PWPR HTSSOP-24
[38] GAIN_AMP#
[42] REAR_L
SPKL+
SPKL-
SPKR+
SPKR-
SE/BTL#
AMP_SHDN#
REAR_R
C43009 1UF/16V
10V/X7R 0805
C43010 0.47UF/16V X7R
C43011 0.47UF/16V X7R
C43012 0.47UF/16V X7R
1UF/16V C43008 10V/X7R 0805
R4302 0Ohm r0402_h16
C43013 Do Not Stuff /x
+5V_AUDIO
R4203 10KOhm r0402_h16
D4202 1N4148W
SPKL-
SPKL+
SPKR-
SPKR+
C43002 Do Not Stuff /x
C43003 Do Not Stuff /x
C43006 Do Not Stuff /x
C43007 Do Not Stuff /x
CON17
WtoB_CON_4P
SIDE1
SIDE2
EAR_SW
R4304 10KOhm r0402_h16
Default : H
Jack In : L
EAR_SW OPTIC_HP
L H SPDIF
L L LINE OUT
H H NO CONNECT
[42] FRONT_L
[42] FRONT_R
FL1
FL2
FR1
FR2
Q4301 2N7002
Q4302 2N7002
Q4303 2N7002
Q4304 2N7002
EAR_POP
R4305 10Ohm
R4306 10Ohm
L4303 120Ohm/100Mhz
L4304 120Ohm/100Mhz
L4305 120Ohm/100Mhz
L4306 120Ohm/100Mhz
L4307 120Ohm/100Mhz
L4308 120Ohm/100Mhz
L4309 Do Not Stuff /x
C43014 Do Not Stuff c0402 /x
C43015 Do Not Stuff c0402 /x
C43017 0.1UF/10V c0402
OPTIC_HP
OPTIC_VCC
PHONE_JACK_8P
J4301
R4310 0Ohm
R4311 Do Not Stuff /x
C43018 Do Not Stuff c0402 /x
S/PDIF_O
[42] S/PDIF
+3VS
+12V
+12VS
R4307 1MOhm r0402_h16
R4309 100KOHM r0402
R4308 10KOhm r0402_h16
R4303 10KOhm r0402_h16
D4302 1N4148W
D4301 1N4148W
DLY_OP_SD#
DLY_OP_SE#
[42] CODEC_SD#
[19,42,45] AC_RESET#
Q4305B UM6K1N
Q4305A UM6K1N
Q4306 2N7002
C43016 1UF/10V
[15] 1S_DEL
R4312 10MOhm
+3VSUS
SN74LV14APWR
U33A
U33B
D4303 1N4148W
[38] OP_SD#
R4316 Do Not Stuff r0402_h16 /x
C43021 0.22UF/6.3V
C43022 Do Not Stuff /x
C43019 0.1UF/10V
DLY_OP_SD#
R4313 10KOhm r0402_h16 Default
Q4308 2N7002
C43023 0.1UF/10V c0402
C43024 0.1UF/10V c0402
Q4307 SI2301BDS-T1-E3
R4314 100KOHM r0402
R4315 100KOHM r0402
C43020 0.1UF/10V c0402
U34
NC7SZ08P5X
DIGITAL
A6TcSKU1
ASUSTECH CO.,LTD.
Title : AMP
Engineer: Jefing_Li
Size A3
Project Name A6T
Rev 1.0
Date: Wednesday, March 08, 2006
Sheet 43 of 72



INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils

A6TcSKU1

ASUSTECH CO.,LTD.	Title : MIC/LINE-IN JACK	
	Engineer: Jefing_Li	
Size: A3	Project Name: A6T	Rev: 1.0
Date: Wednesday, March 08, 2006	Sheet 44 of 72	


+1.8V_LAN
R4501
Do Not Stuff
/x
L4607
TCT1
TD1+
TD1-
TCT2
TD2+
TD2-
TCT3
TD3+
TD3-
TCT4
TD4+
TD4-
[46] L_TRDM3
[46] L_TRDP3
[46] L_TRDM2
[46] L_TRDP2
[46] L_TRDM1
[46] L_TRDP1
[46] L_TRDM0
[46] L_TRDP0
MCT1 L_CMT0
MX1+ L_TRLM3
MX1- L_TRLP3
MCT2 L_CMT1
MX2+ L_TRLM2
MX2- L_TRLP2
MCT3 L_CMT2
MX3+ L_TRLM1
MX3- L_TRLP1
MCT4 L_CMT3
MX4+ L_TRLM0
MX4- L_TRLP0
1GB
RDC
C45003 0.01UF/50V
C45004 0.01UF/50V
C45005 0.01UF/50V
C45006 0.01UF/50V
GND
LAN PORT
L_TRLM2 0OHM RN4503A LTRLM2
L_TRLP2 0OHM RN4503B LTRLP2
L4501 Do Not Stuff /x
L_TRLM3 0OHM RN4504A LTRLM3
L_TRLP3 0OHM RN4504B LTRLP3
L4504 Do Not Stuff /x
L_TRLP1 0OHM RN4505A LTRLP1
L_TRLM1 0OHM RN4505B LTRLM1
L4505 Do Not Stuff /x
L_TRLM0 0OHM RN4506A LTRLM0
L_TRLP0 0OHM RN4506B LTRLP0
L4506 Do Not Stuff /x
4/12
L_CMT0 75Ohm RN4502A
L_CMT1 75Ohm RN4502B
L_CMT2 75Ohm RN4502C
L_CMT3 75Ohm RN4502D
FGND1S
C45007 1500PF/50V
C45008 1000PF/2KV
GND
CON18
SIDE2
SIDE1
WTOB_CON_2P
MODEM_TIP_CON
MODEM_RING_CON
Irat=100mA
1KOhm/100Mhz
L4502
L4503
MODEM_TIP
MODEM_RING
4/11
C45001 1000PF/3KV
C45002 1000PF/3KV
CON19
SIDE1
P_GND1
NP_NC1
NP_NC2
P_GND2
SIDE2
LTRLP0
LTRLM0
LTRLP1
LTRLP2
LTRLM2
LTRLM1
LTRLP3
LTRLM3
MODULAR_JACK_12P
MDC
+3V
C45009 0.1UF/10V c0402
GND
[19,42] AC_SOUT
[19,42] AC_SYNC
[19] AC_SDIN1
[19,42,43] AC_RESET#
R4502 0Ohm
R4504 0Ohm
R4505 22Ohm
R4506 0Ohm
CON20
BTOB_CON_12P
GND1
GND3
GND5
NP_NC1
GND2
GND4
GND6
NP_NC2
R4508 0Ohm +3V
R4503 Do Not Stuff +3VSUS
X
R4507 22Ohm AC_BITCLK [19,42]
C45010 Do Not Stuff /x
H4501 L4E_1A
H4502 L4E_1A
Must change to
13-N7510M270
A6TcSKU1
Title : RJ45/11/MDC
ASUSTECH CO.,LTD.
Engineer: Jefing_Li
Size A3
Project Name A6T
Rev 1.0
Date: Wednesday, March 08, 2006
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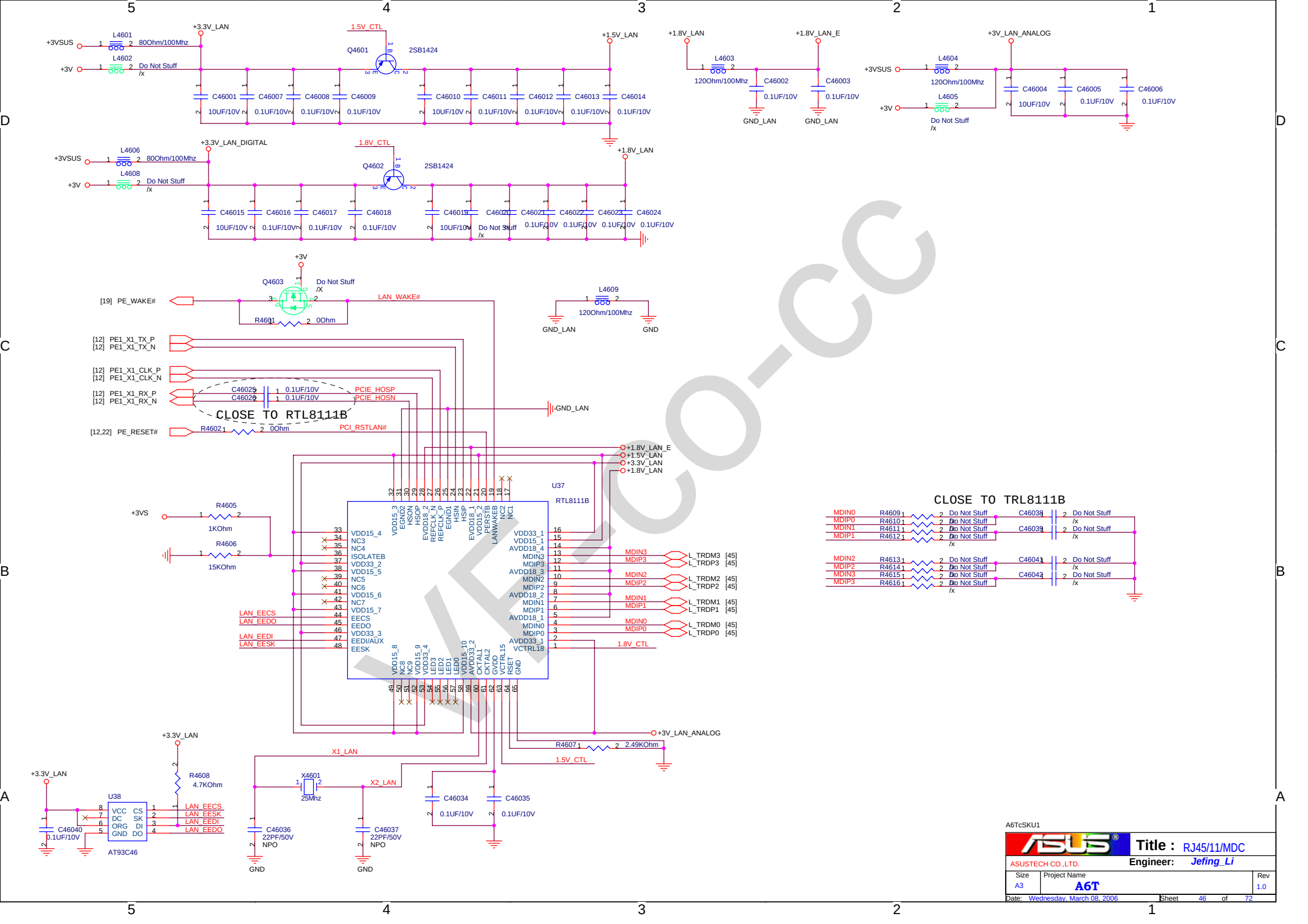


A6TcSKU1

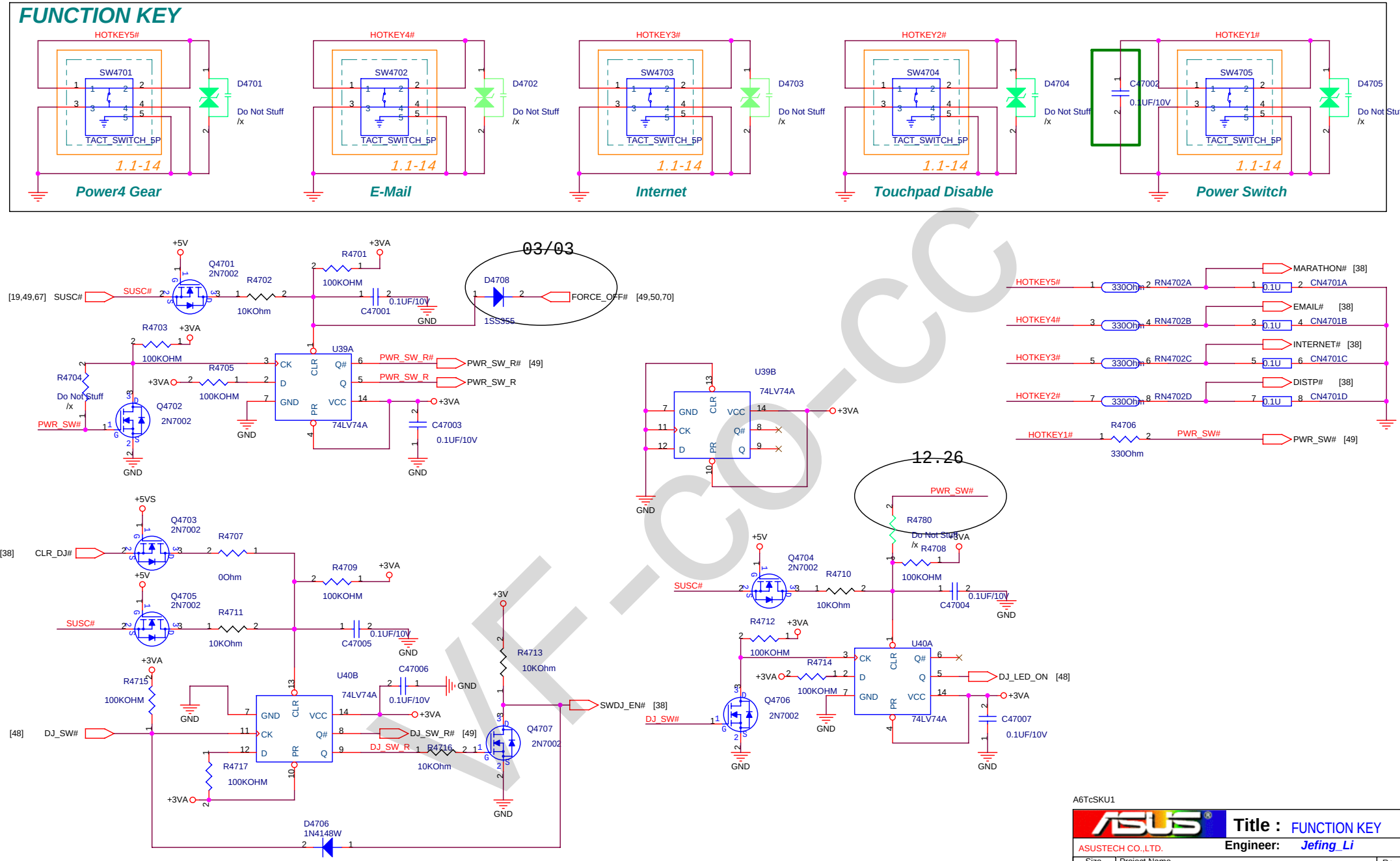
ASUSTECH CO.,LTD.

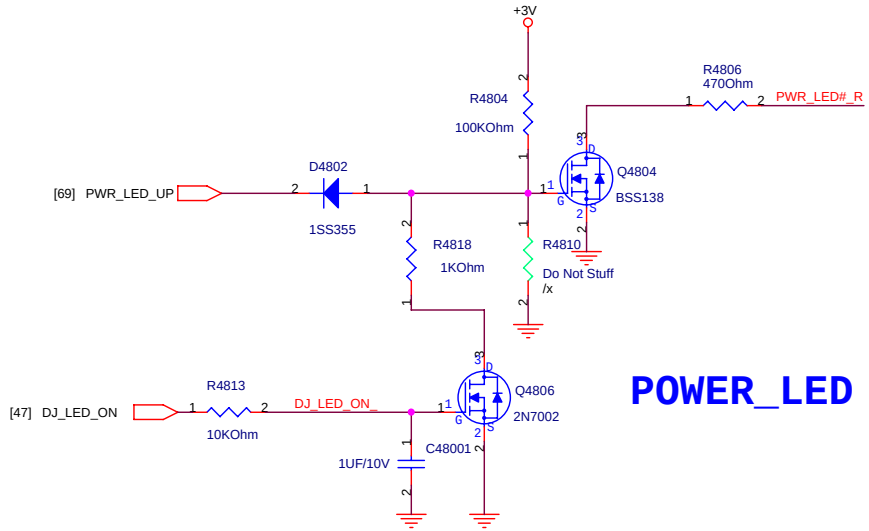
Title : RJ45/11/MDC

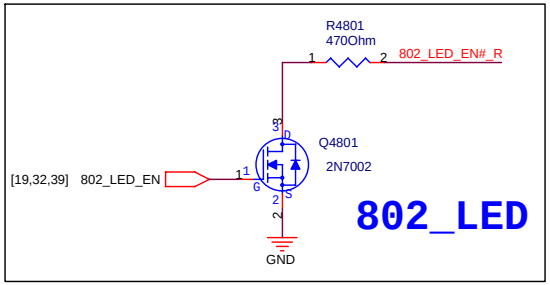
Engineer: Jefing_Li

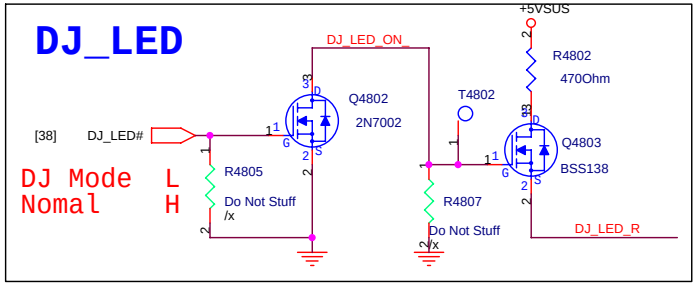
Size	Project Name	Rev
A3	A6T	1.0

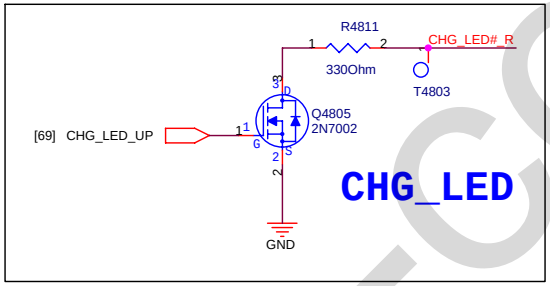
Date: Wednesday, March 08, 2006 Sheet 46 of 72

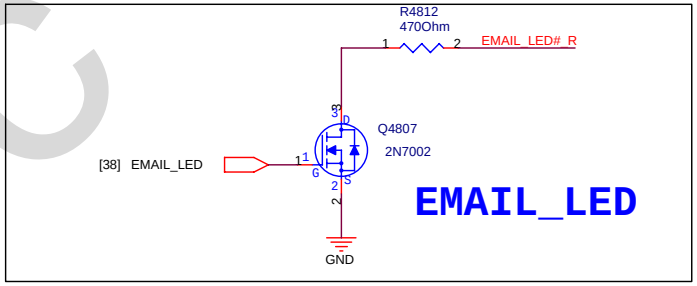

FUNCTION KEY
HOTKEY5#
SW4701
TACT_SWITCH_5P
D4701
Do Not Stuff
/x
1.1-14
Power4 Gear
HOTKEY4#
SW4702
TACT_SWITCH_5P
D4702
Do Not Stuff
/x
1.1-14
E-Mail
HOTKEY3#
SW4703
TACT_SWITCH_5P
D4703
Do Not Stuff
/x
1.1-14
Internet
HOTKEY2#
SW4704
TACT_SWITCH_5P
D4704
Do Not Stuff
/x
1.1-14
Touchpad Disable
C47002
0.1UF/10V
HOTKEY1#
SW4705
TACT_SWITCH_5P
D4705
Do Not Stuff
/x
1.1-14
Power Switch
03/03
12.26
Q4701
2N7002
R4702
10KOhm
R4701
100KOHM
C47001
0.1UF/10V
D4708
1SS355
FORCE_OFF#
[19,49,67] SUSC#
SUSC#
[49,50,70]
R4703
100KOHM
R4705
100KOHM
R4704
Do Not Stuff
/x
Q4702
2N7002
PWR_SW#
U39A
74LV74A
PWR_SW_R#
PWR_SW_R#
[49]
PWR_SW_R
PWR_SW_R
C47003
0.1UF/10V
U39B
74LV74A
HOTKEY5#
330Ohm
RN4702A
MARATHON#
[38]
CN4701A
HOTKEY4#
330Ohm
RN4702B
EMAIL#
[38]
CN4701B
HOTKEY3#
330Ohm
RN4702C
INTERNET#
[38]
CN4701C
HOTKEY2#
330Ohm
RN4702D
DISTP#
[38]
CN4701D
HOTKEY1#
R4706
330Ohm
PWR_SW#
PWR_SW#
[49]
Q4703
2N7002
R4707
0Ohm
[38] CLR_DJ#
Q4705
2N7002
R4711
10KOhm
SUSC#
R4709
100KOHM
C47005
0.1UF/10V
R4715
100KOHM
R4717
100KOHM
U40B
74LV74A
C47006
0.1UF/10V
[48] DJ_SW#
DJ_SW_R#
[49]
DJ_SW_R
R4716
10KOhm
R4713
10KOhm
SWDJ_EN#
[38]
Q4707
2N7002
D4706
1N4148W
R4780
Do Not Stuff
/x
PWR_SW#
R4708
100KOHM
Q4704
2N7002
R4710
10KOhm
SUSC#
C47004
0.1UF/10V
R4712
100KOHM
R4714
100KOHM
Q4706
2N7002
DJ_SW#
U40A
74LV74A
DJ_LED_ON
[48]
C47007
0.1UF/10V
A6TcSKU1
Title : FUNCTION KEY
ASUSTECH CO.,LTD.
Engineer: Jefing_Li
Size B
Project Name A6T
Rev 1.0
Date: Wednesday, March 08, 2006
Sheet 47 of 72

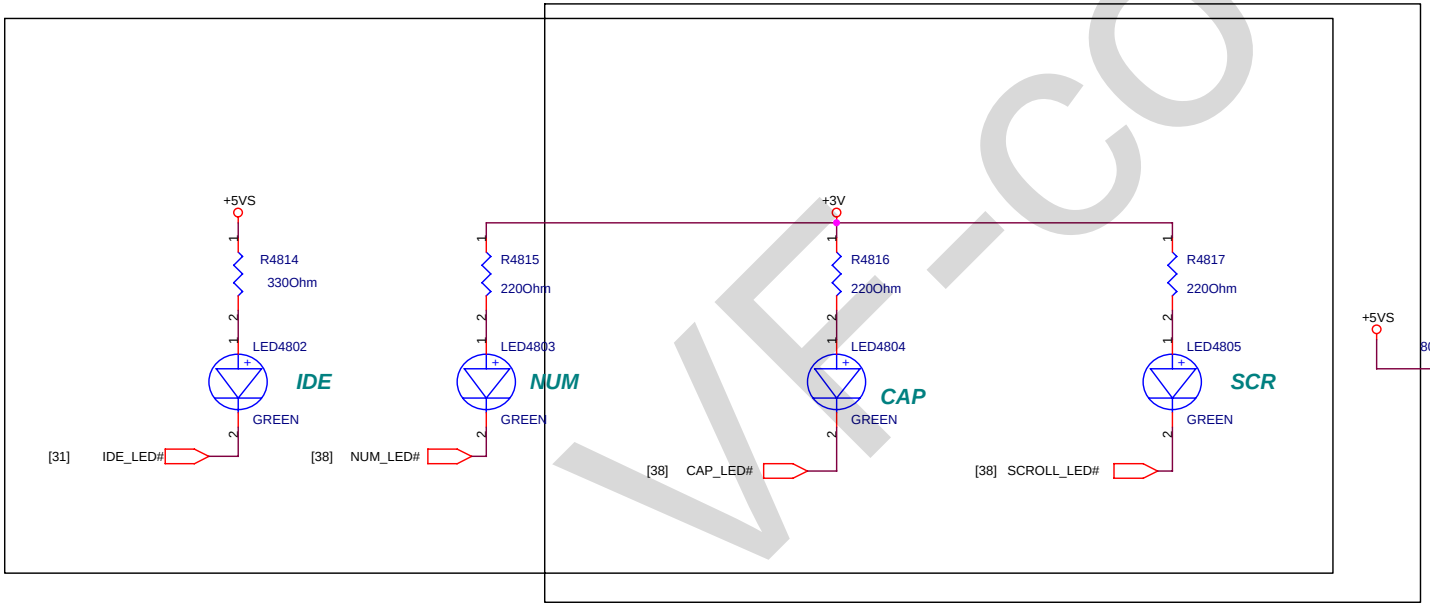


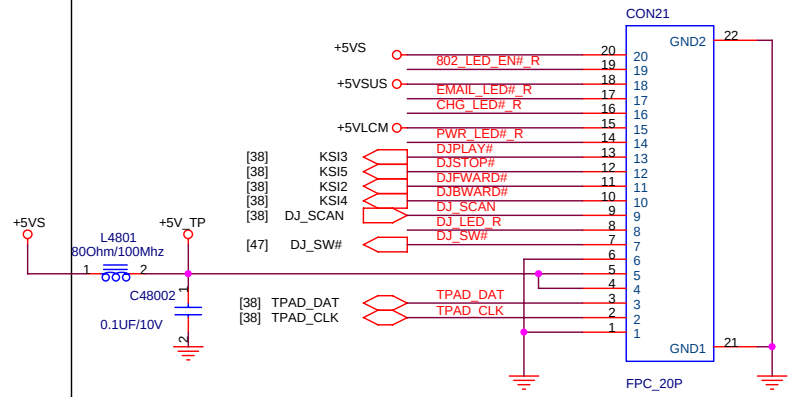












A6TcSKU1

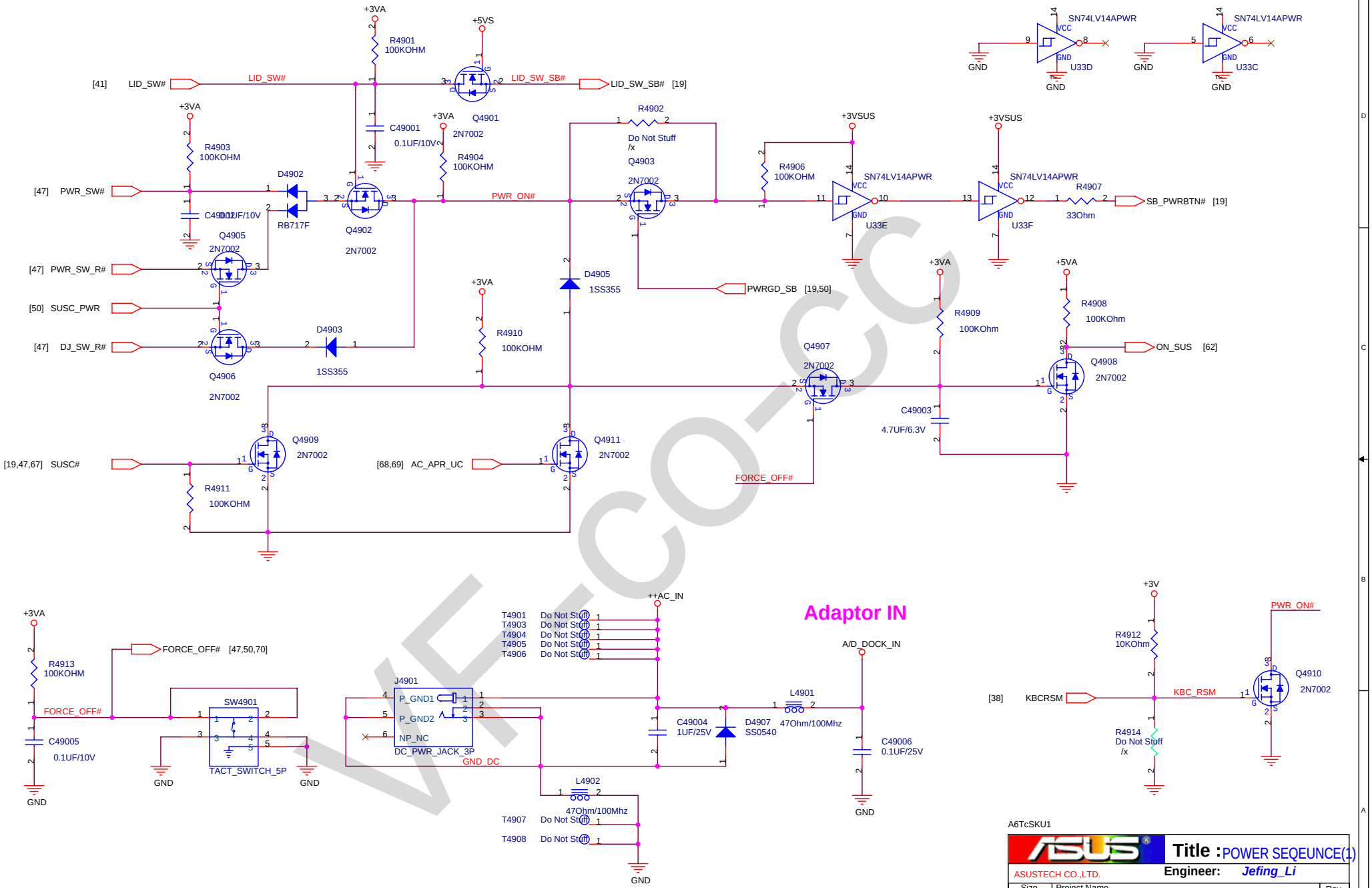
ASUSTECH CO.,LTD.

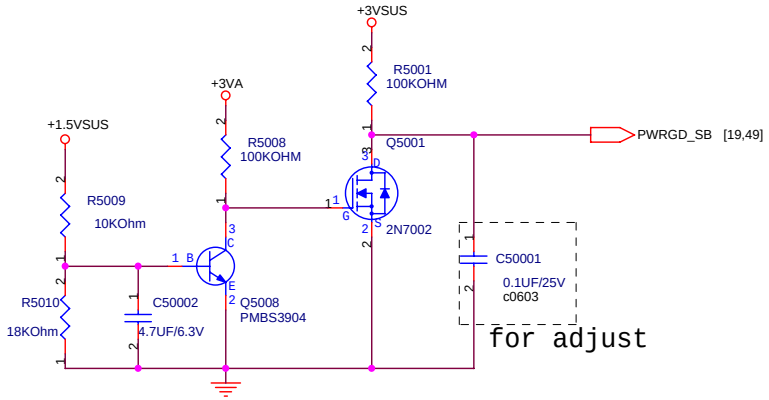
Title : LED

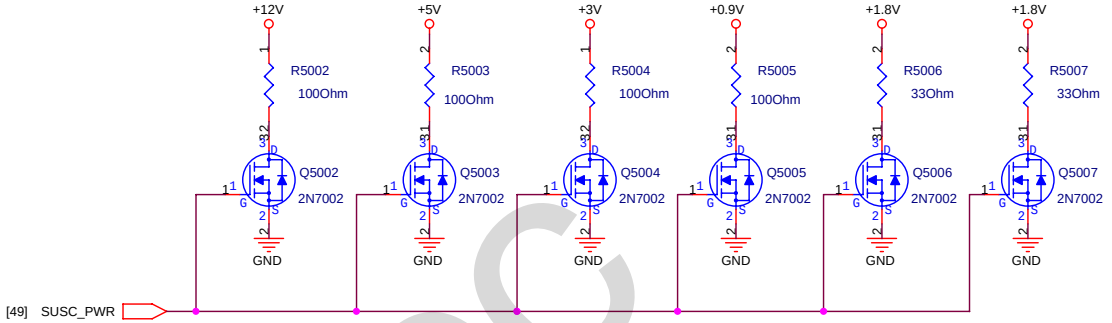
Engineer: Jefing_Li

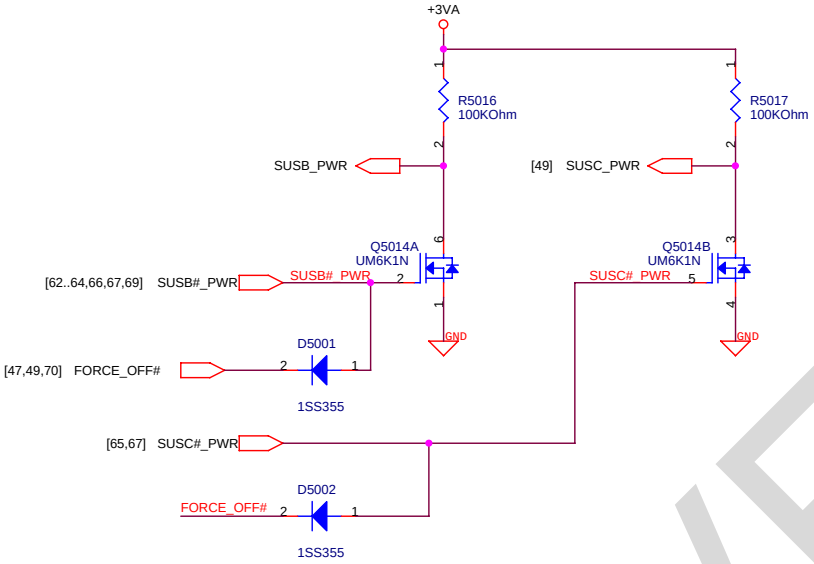
Size	Project Name	Rev
B	A6T	1.0

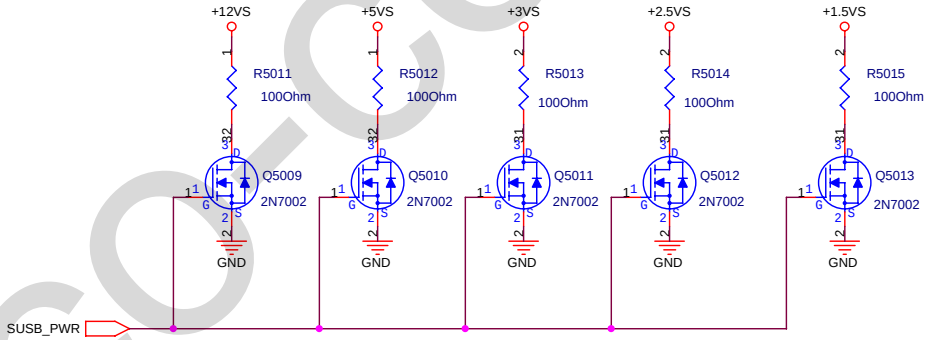
Date: Wednesday, March 08, 2006 Sheet 48 of 72


+3VA
+5VS
R4901
100KOHM
[41] LID_SW#
LID_SW#
LID_SW_SB#
LID_SW_SB# [19]
C49001
0.1UF/10V
Q4901
2N7002
R4904
100KOHM
R4902
Do Not Stuff
/x
Q4903
2N7002
PWR_ON#
R4903
100KOHM
D4902
RB717F
[47] PWR_SW#
C49002
0.1UF/10V
Q4902
2N7002
Q4905
2N7002
[47] PWR_SW_R#
[50] SUSC_PWR
[47] DJ_SW_R#
D4903
1SS355
Q4906
2N7002
D4905
1SS355
PWRGD_SB [19,50]
R4910
100KOHM
+3VSUS
R4906
100KOHM
SN74LV14APWR
U33E
U33F
R4907
33Ohm
SB_PWRBTN# [19]
GND
SN74LV14APWR
U33D
U33C
+3VA
R4909
100KOhm
+5VA
R4908
100KOhm
ON_SUS [62]
Q4907
2N7002
Q4908
2N7002
C49003
4.7UF/6.3V
FORCE_OFF#
[19,47,67] SUSC#
Q4909
2N7002
R4911
100KOHM
[68,69] AC_APR_UC
Q4911
2N7002
Adaptor IN
++AC_IN
T4901 Do Not Stuff
T4903 Do Not Stuff
T4904 Do Not Stuff
T4905 Do Not Stuff
T4906 Do Not Stuff
J4901
P_GND1
P_GND2
NP_NC
DC_PWR_JACK_3P
GND_DC
C49004
1UF/25V
D4907
SS0540
L4901
47Ohm/100Mhz
A/D_DOCK_IN
C49006
0.1UF/25V
L4902
47Ohm/100Mhz
T4907 Do Not Stuff
T4908 Do Not Stuff
+3VA
R4913
100KOHM
FORCE_OFF# [47,50,70]
SW4901
TACT_SWITCH_5P
C49005
0.1UF/10V
+3V
R4912
10KOhm
PWR_ON#
[38] KBCRSM
KBC_RSM
Q4910
2N7002
R4914
Do Not Stuff
/x
A6TcSKU1
Title : POWER SEQEUNCE(1)
ASUSTECH CO.,LTD.
Engineer: Jefing_Li
Size B
Project Name A6T
Rev 1.0
Date: Wednesday, March 08, 2006
Sheet 49 of 72









A6TcSKU1

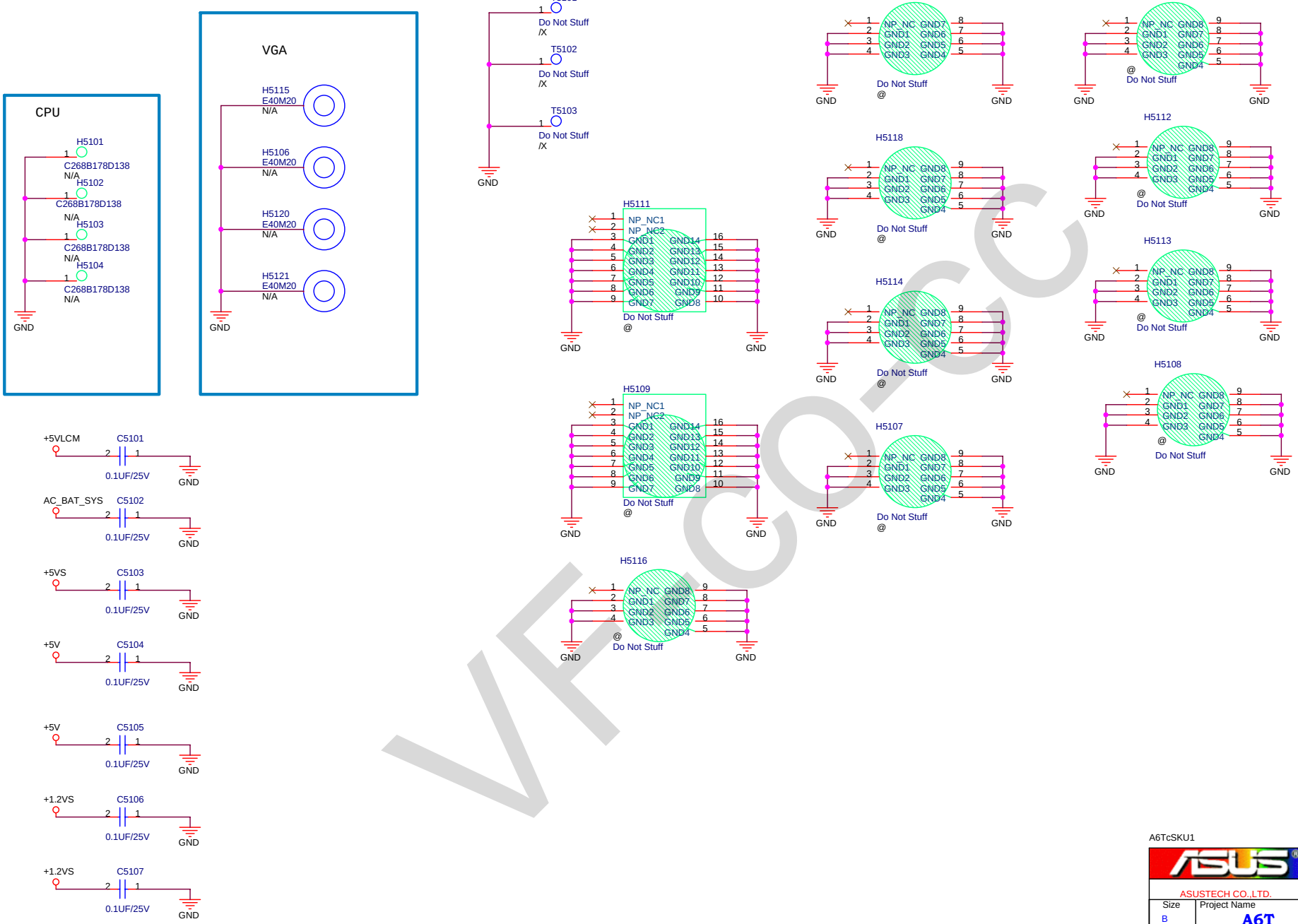
ASUSTECH CO.,LTD.

Title : POWER SEQUENCE(2)

Engineer: Jefing_Li

Size	Project Name	Rev
B	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 50 of 72



A6TcSKU1

Title : SCREW HOLE

Engineer: Jefing_Li

ASUSTECH CO.,LTD.

Size	Project Name	Rev
B	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 51 of 72

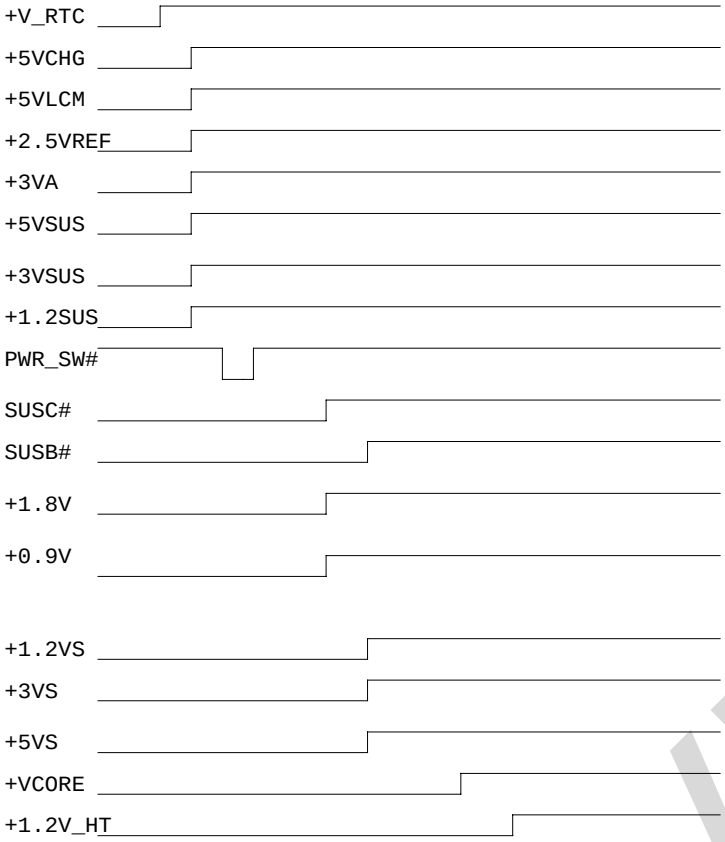
RUN S0-S1 This voltage rail is present when the system is “running”

SUS S0-S1-S3 This voltage rail is present when the system is running or in suspend-to-RAM

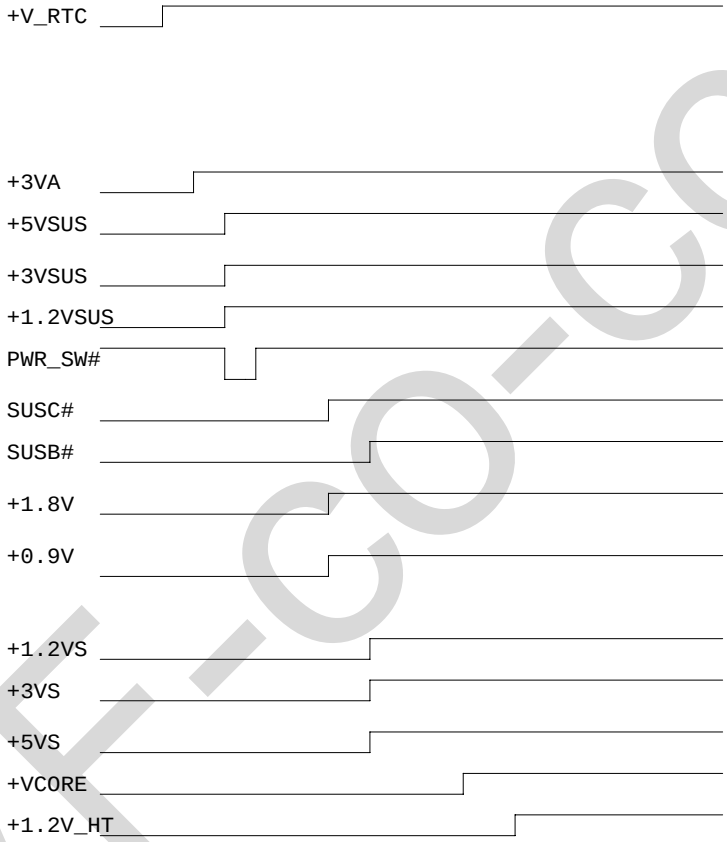
ALWAYS S0-S1-S3-S4-S5 This voltage rail is always present as long as there is main power, whether in the form of a system battery, an AC adapter, or other type of main power supply

RTC S0-S5, G3 This voltage rail is always present for the Real Time Clock and CMOS RAM circuitry even in the mechanical off state as long as the coin cell is present and not discharged.

AC MODE



BAT MODE



A6TcSKU1

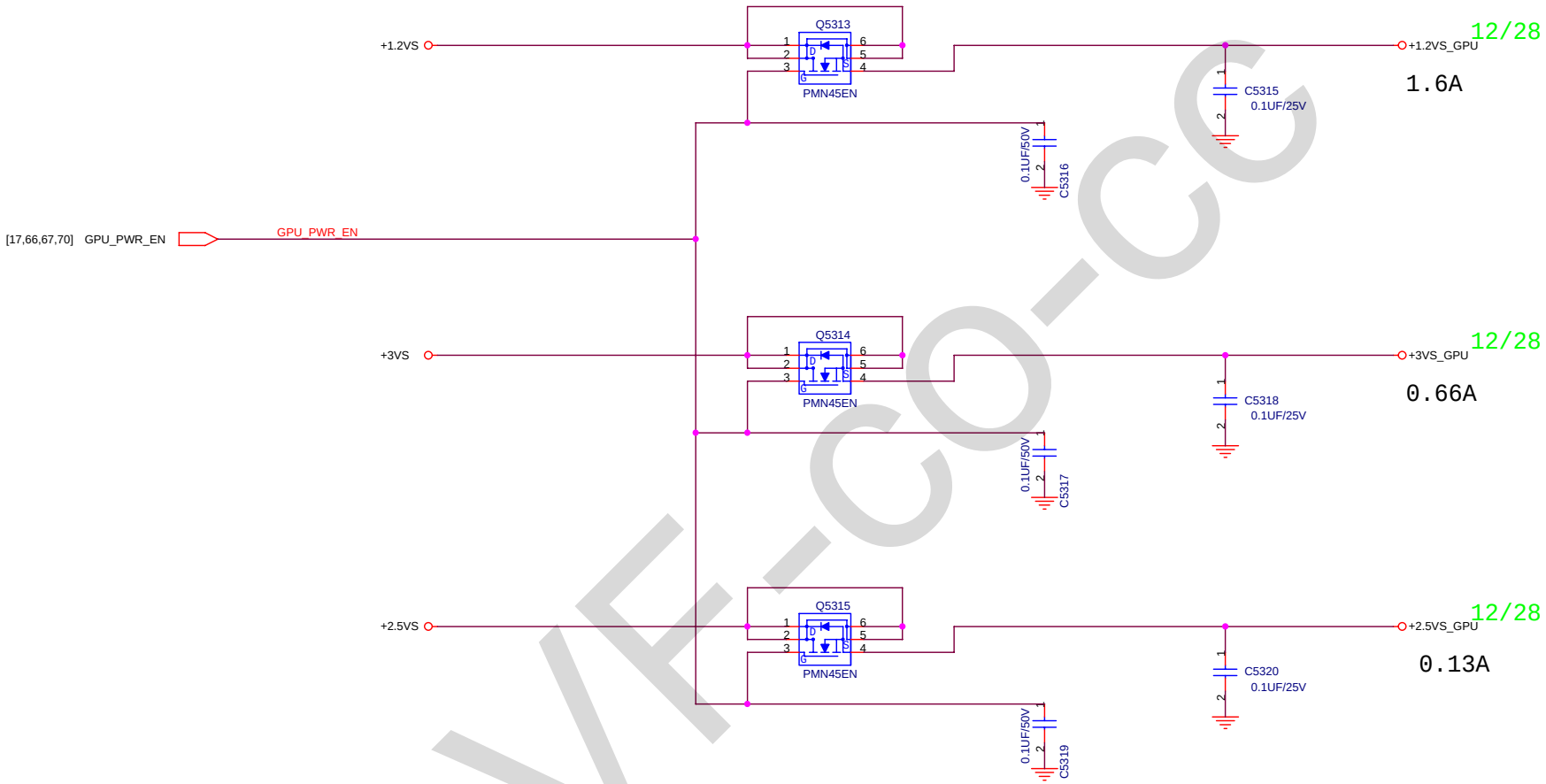
ASUSTECH CO.,LTD.

Title :POWER SEQUENCE BLCOK

Engineer: Jefing_Li

Size	Project Name	Rev
Custom	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 52 of 72



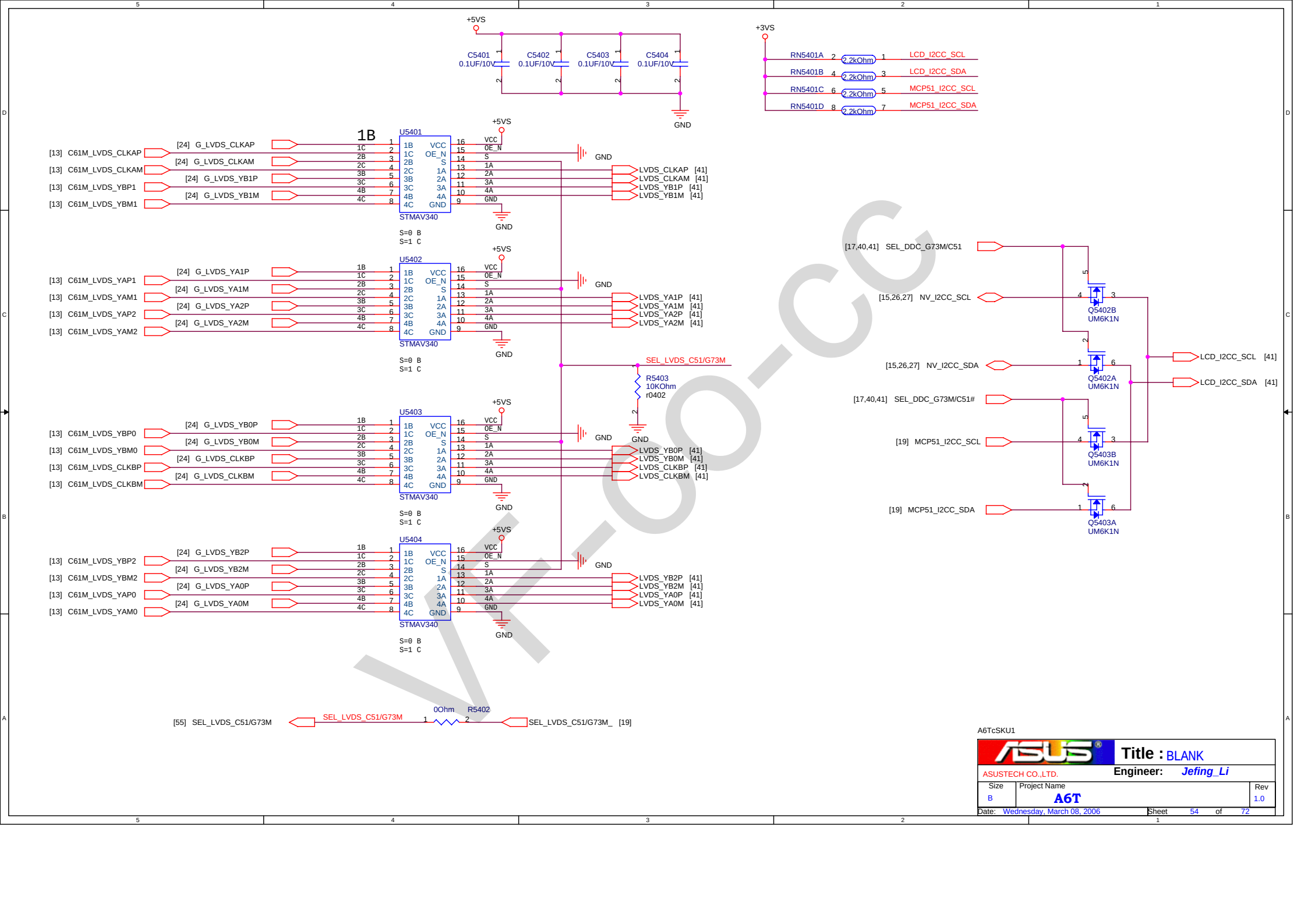
A6TcSKU1

Title : BLANK

ASUSTECH CO.,LTD. Engineer: Jefing_Li

Size	Project Name	Rev
B	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 53 of 72



A6TcSKU1

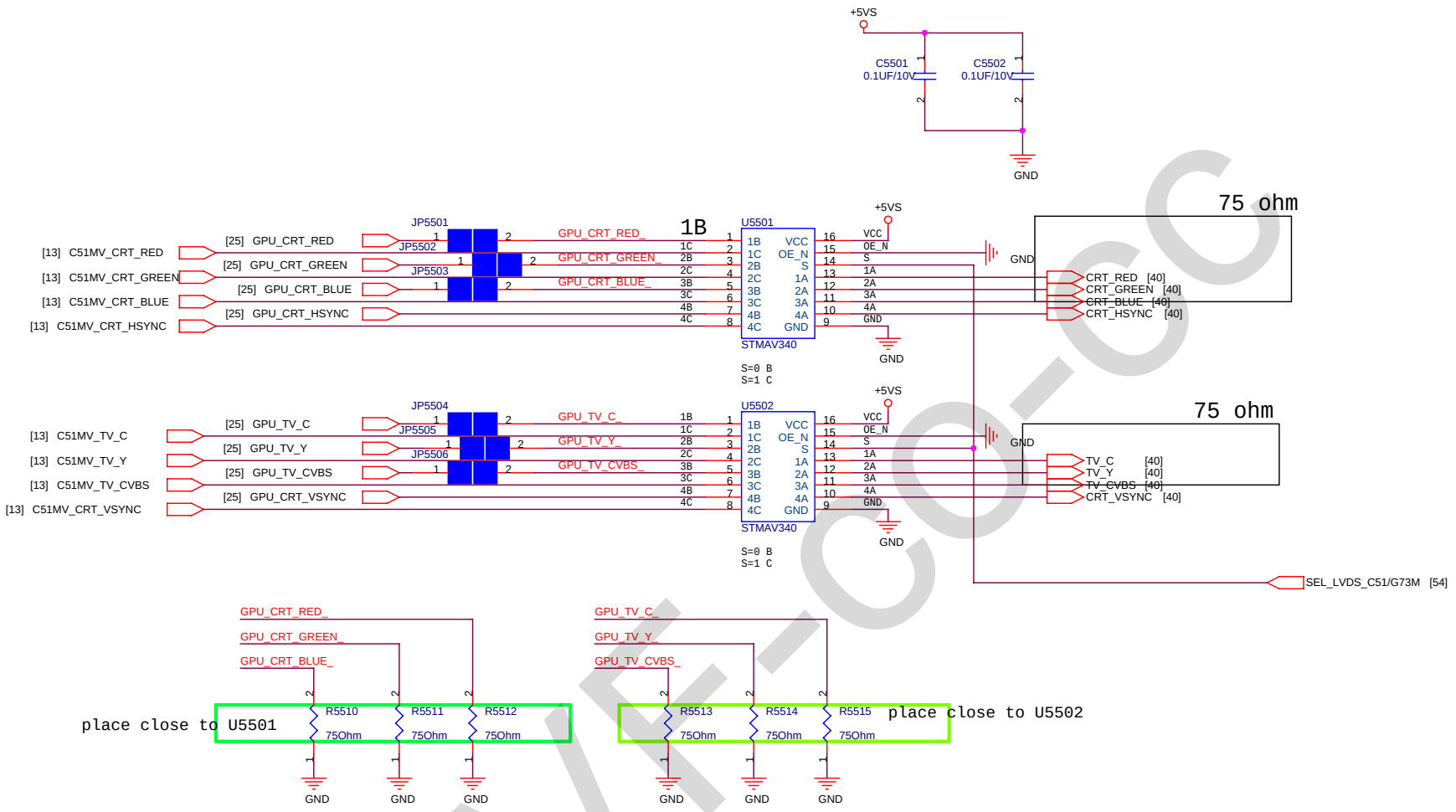
ASUSTECH CO.,LTD.

Title : BLANK

Engineer: Jefing_Li

Size	Project Name	Rev
B	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 54 of 72



A6TcSKU1

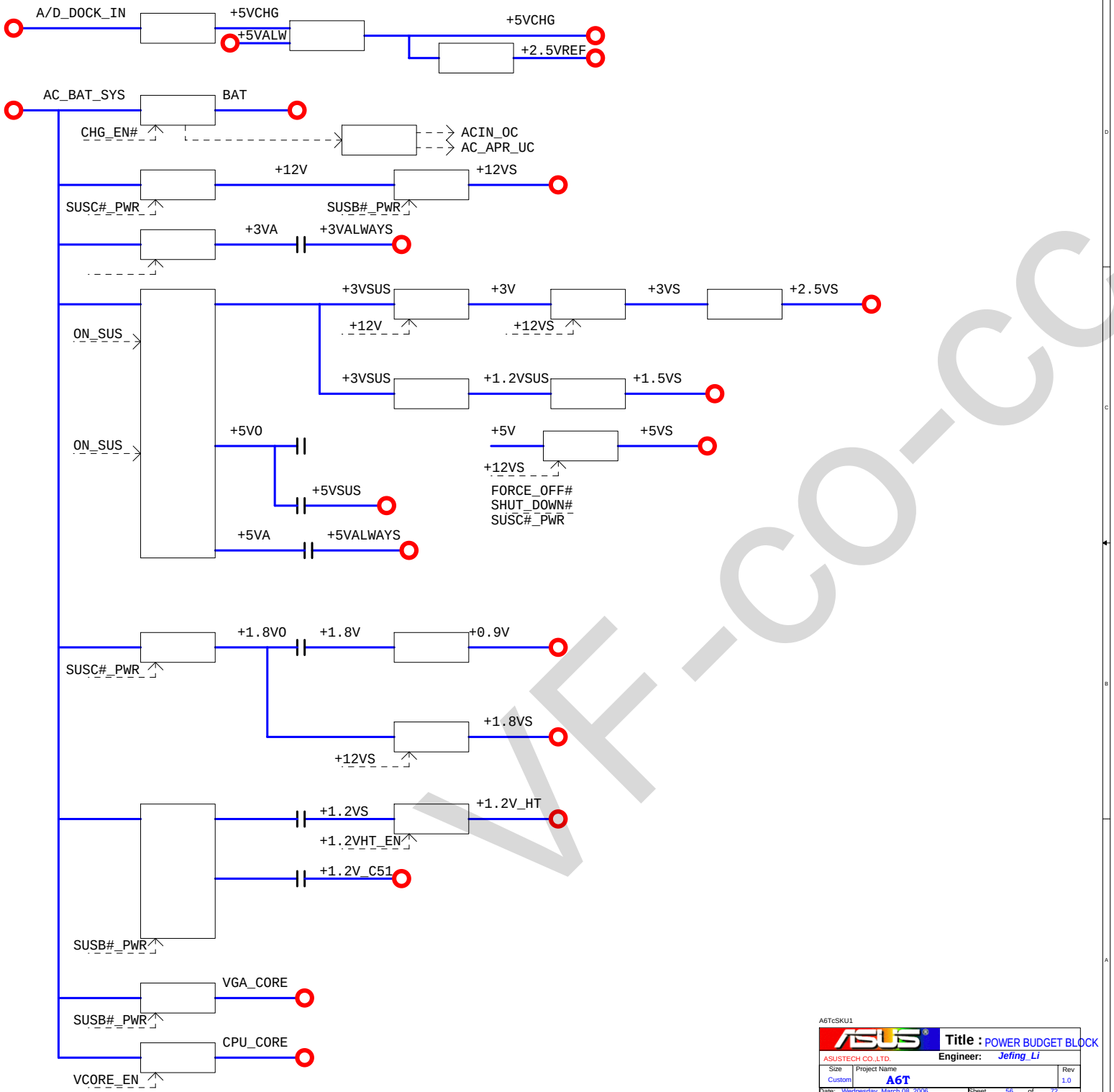
ASUSTECH CO.,LTD.

Title : BLANK

Engineer: Jefing_Li

Size	Project Name	Rev
B	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 55 of 72



A6TcSKU1

ASUSTECH CO.,LTD.

Title : POWER BUDGET BLOCK

Engineer: Jefing_Li

Size	Project Name	Rev
Custom	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 56 of 72

A6TcSKU1

Title : BLANK

ASUSTECH CO.,LTD.

Engineer: Jefing_Li

Size	Project Name	Rev
B	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 57 of 72

A6TcSKU1

Title : BLANK

ASUSTECH CO.,LTD.

Engineer: Jefing_Li

Size	Project Name	Rev
B	A6T	1.0

Date: Wednesday, March 08, 2006 Sheet 58 of 72

A6TcSKU1

Title : BLANK

ASUSTECH CO.,LTD.

Engineer: Jefing_Li

Size	Project Name	Rev
B	A6T	1.0

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A6TcSKU1

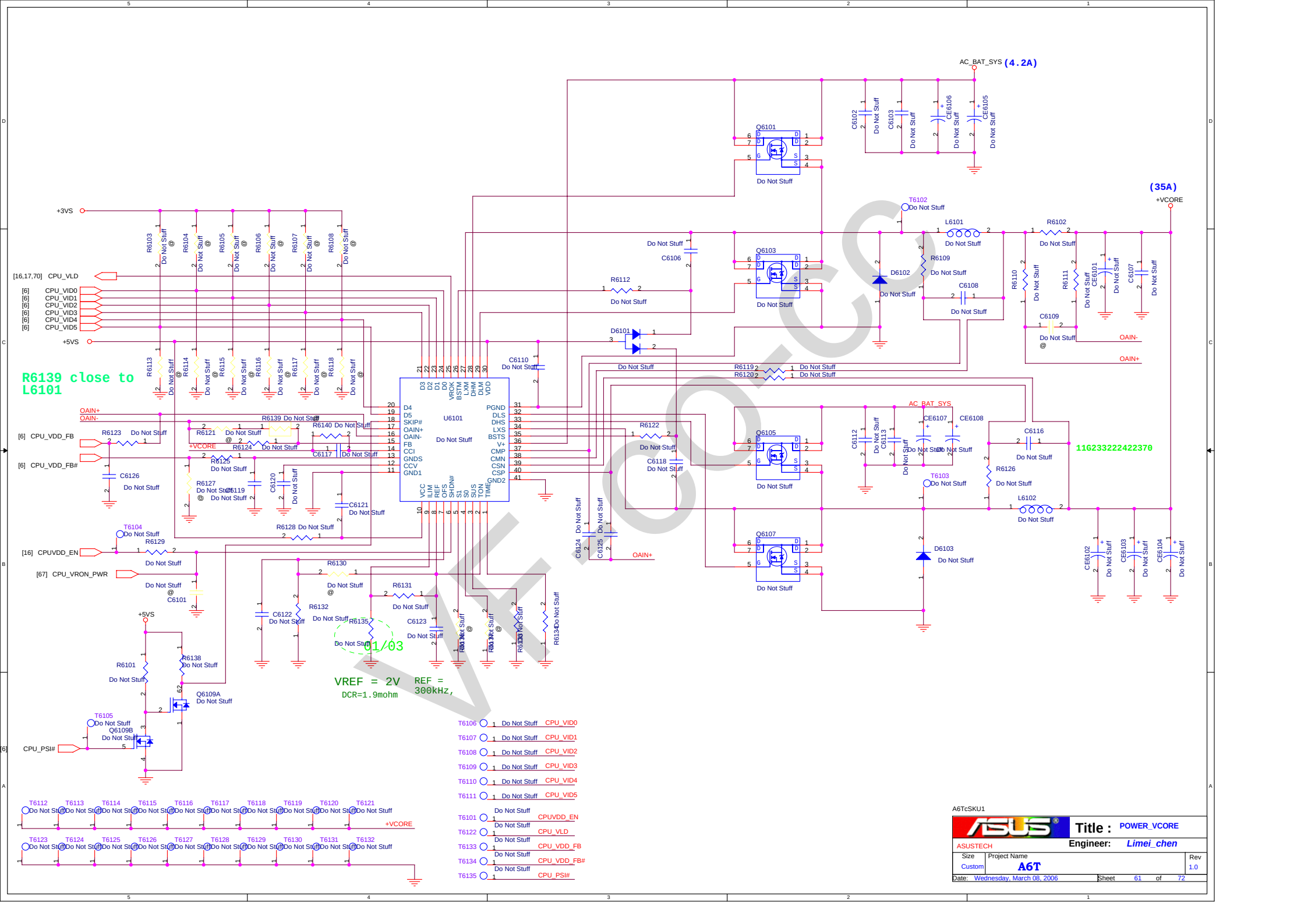
Title : BLANK

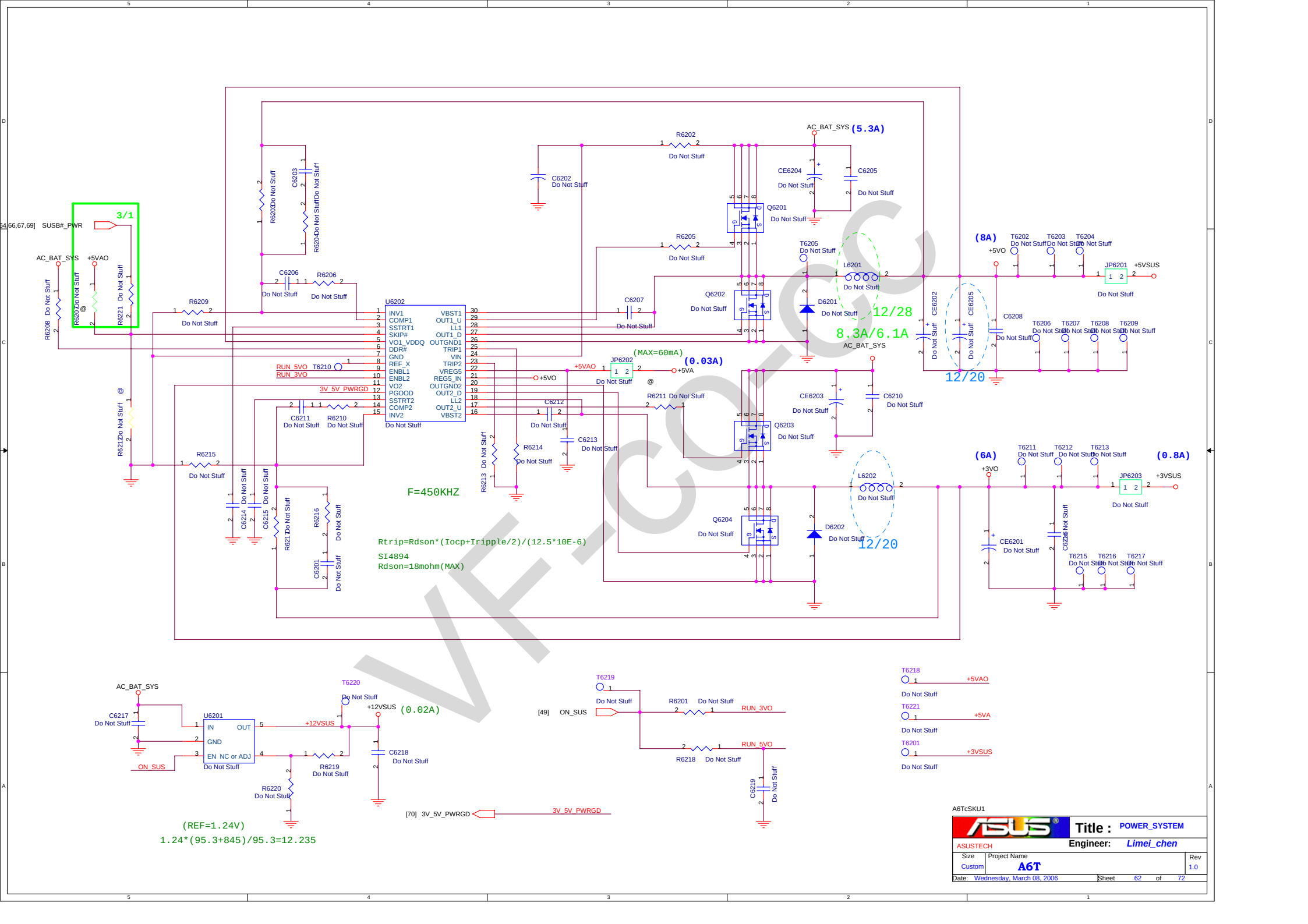
ASUSTECH CO.,LTD.

Engineer: Jefing_Li

Size	Project Name	Rev
B	A6T	1.0

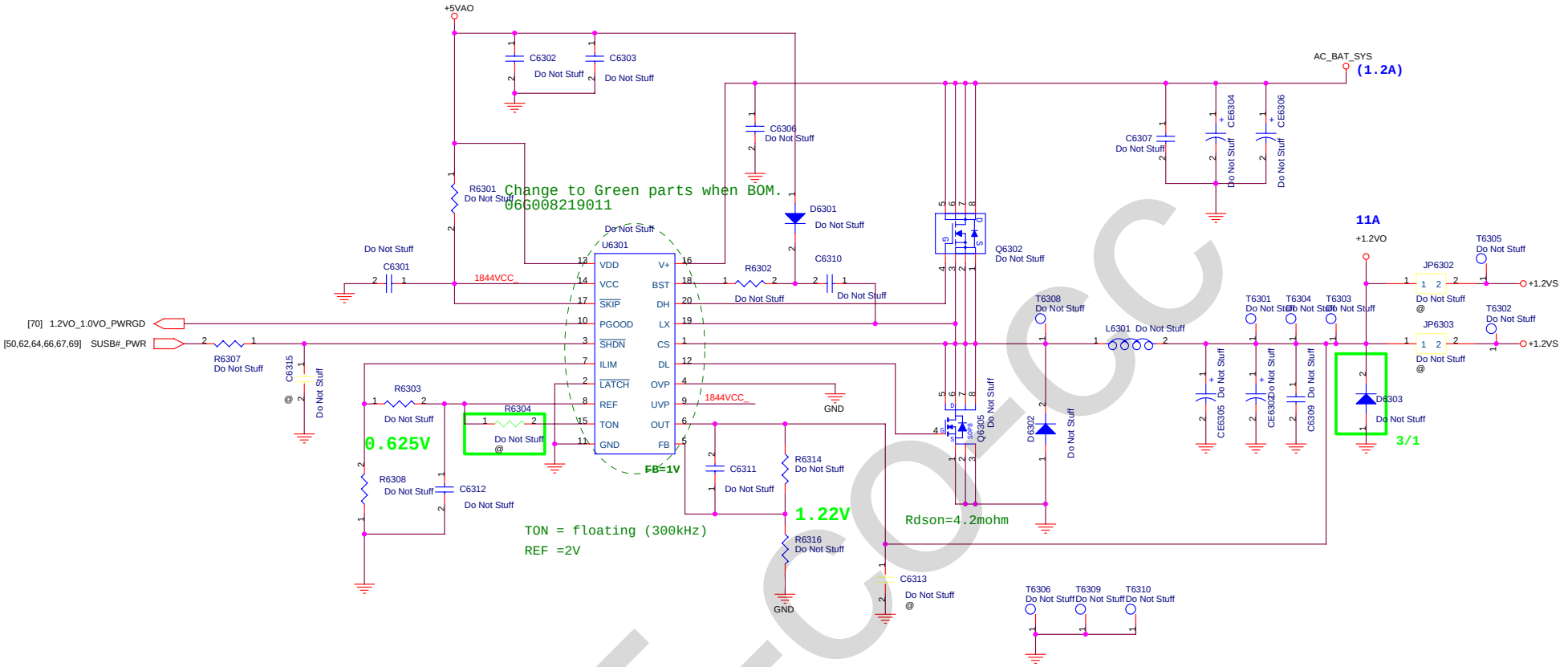
Date: Wednesday, March 08, 2006 Sheet 60 of 72


AC_BAT_SYS (4.2A)
(35A)
+VCORE
+3VS
+5VS
[16,17,70] CPU_VLD
[6] CPU_VID0
[6] CPU_VID1
[6] CPU_VID2
[6] CPU_VID3
[6] CPU_VID4
[6] CPU_VID5
R6139 close to L6101
U6101
[6] CPU_VDD_FB
[6] CPU_VDD_FB#
[16] CPUVDD_EN
[67] CPU_VRON_PWR
CPU_PSI#
OAIN+
OAIN-
VREF = 2V
DCR=1.9mohm
REF = 300kHz,
01/03
Do Not Stuff
A6TcSKU1
ASUSTECH
Title : POWER_VCORE
Engineer: Limei_chen
Project Name A6T
Size Custom
Rev 1.0
Date: Wednesday, March 08, 2006
Sheet 61 of 72



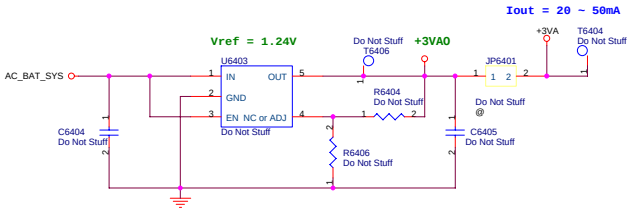
A6TcSKU1

ASUSTECH	Title : POWER_SYSTEM	
	Engineer: Limei_chen	
Size: Custom	Project Name: A6T	Rev: 1.0
Date: Wednesday, March 08, 2006	Sheet 62 of 72	

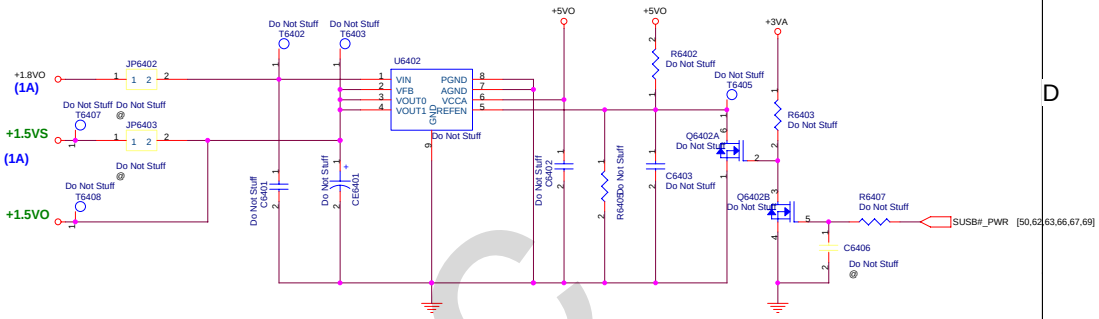


A6TcSKU1

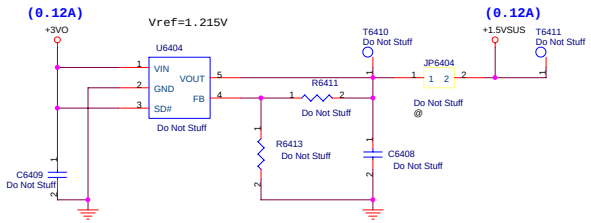
ASUSTECH	Title : POWER_I/O_1.2V&1.0V	
	Engineer: Limei_chen	
Size: Custom	Project Name: A6T	Rev: 1.0
Date: Wednesday, March 08, 2006	Sheet 63 of 72	



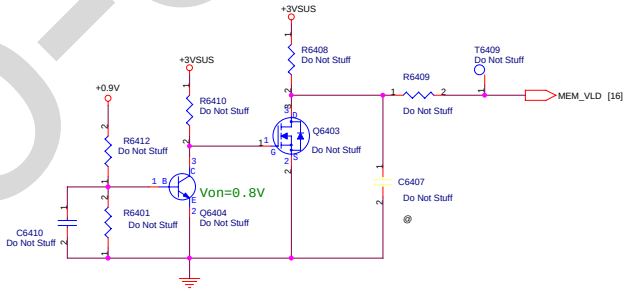
+3VA

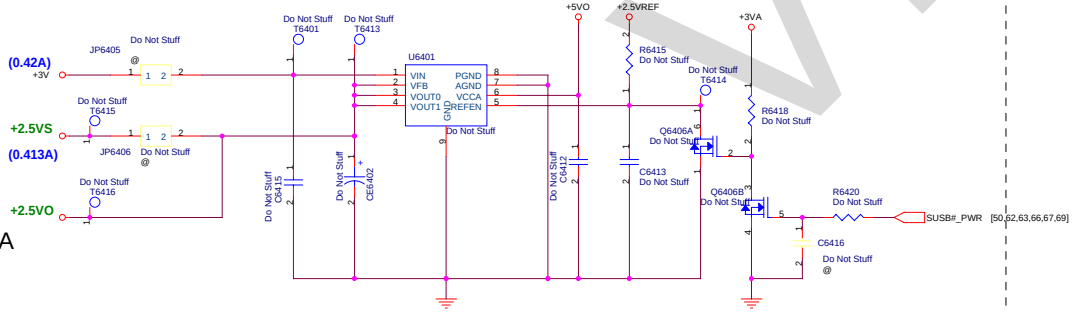


+1.5VS

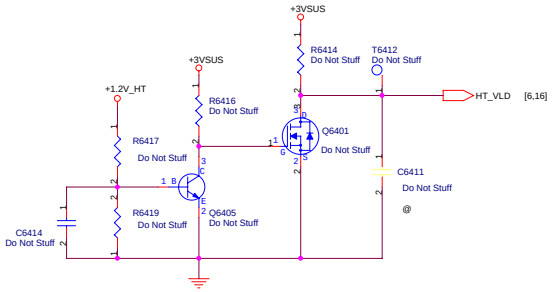


+1.5VSUS



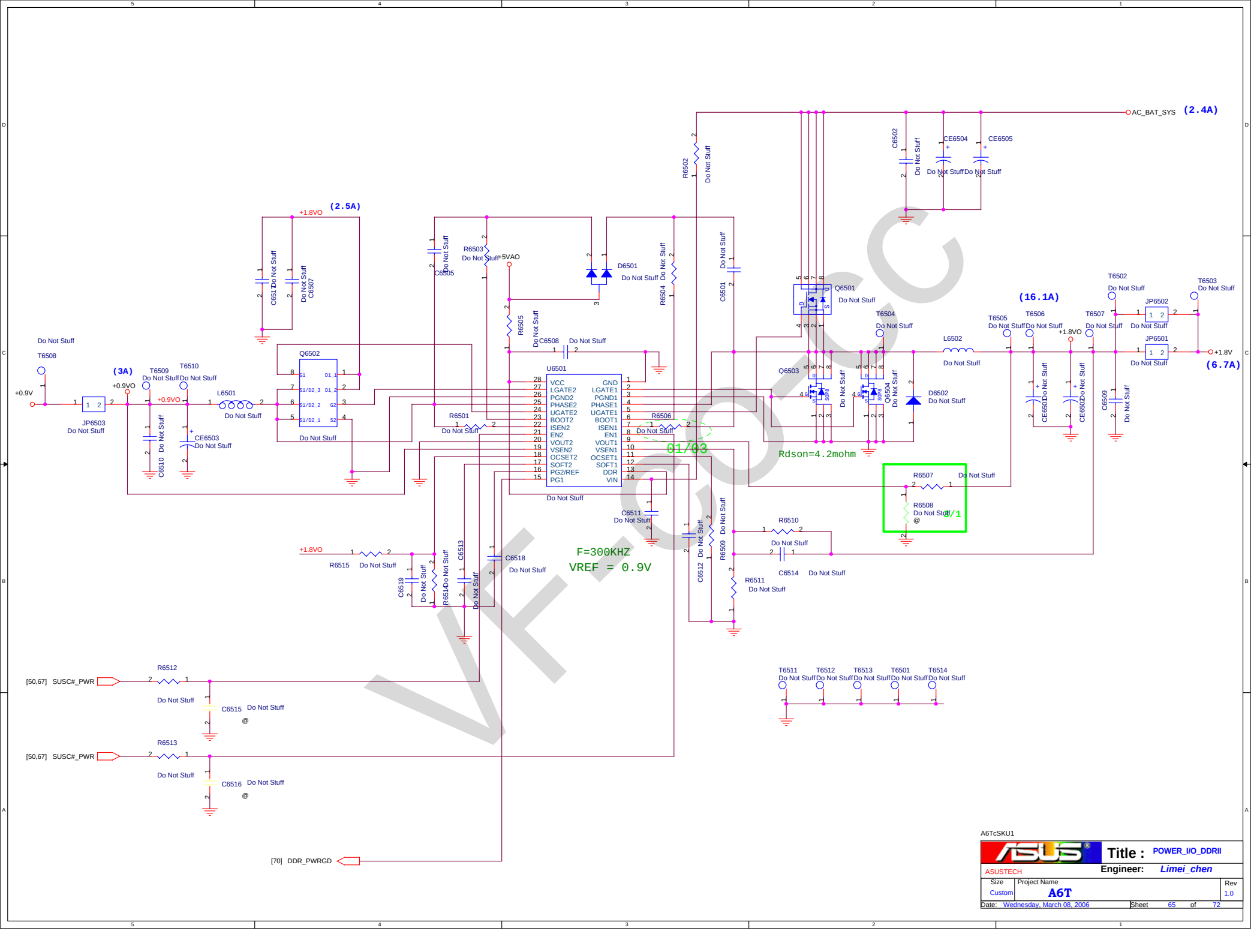


+2.5VS



A6TcSKU1

ASUSTECH	Title : POWER_I/O_LDO	
	Engineer: Limei_chen	
Size: C	Project Name: A6T	Rev: 1.0
Date: Wednesday, March 08, 2006	Sheet 64 of 72	


AC_BAT_SYS (2.4A)
+1.8VO (2.5A)
+0.9VO (3A)
+1.8V (6.7A)
(16.1A)
+5VAO
U6501
VCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
ISEN2
EN2
VOUT2
VSEN2
OCSET2
SOFT2
PG2/REF
PG1
GND
LGATE1
PGND1
PHASE1
UGATE1
BOOT1
ISEN1
EN1
VOUT1
VSEN1
OCSET1
SOFT1
DDR
VIN
Q6501
Q6502
Q6503
Q6504
D6501
D6502
L6501
L6502
JP6503
JP6502
JP6501
R6501
R6502
R6503
R6504
R6505
R6506
R6507
R6508
R6509
R6510
R6511
R6512
R6513
R6514
R6515
C6501
C6502
C6505
C6507
C6508
C6509
C6510
C6511
C6512
C6513
C6514
C6515
C6516
C6518
C6519
CE6502
CE6503
CE6504
CE6505
T6501
T6502
T6503
T6504
T6505
T6506
T6507
T6508
T6509
T6510
T6511
T6512
T6513
T6514
Do Not Stuff
01/03
Rdson=4.2mohm
F=300KHZ
VREF = 0.9V
0/1
[50,67] SUSC#_PWR
[50,67] SUSC#_PWR
[70] DDR_PWRGD
A6TcSKU1
Title : POWER_I/O_DDRII
ASUSTECH
Engineer: Limei_chen
Size Custom
Project Name A6T
Rev 1.0
Date: Wednesday, March 08, 2006
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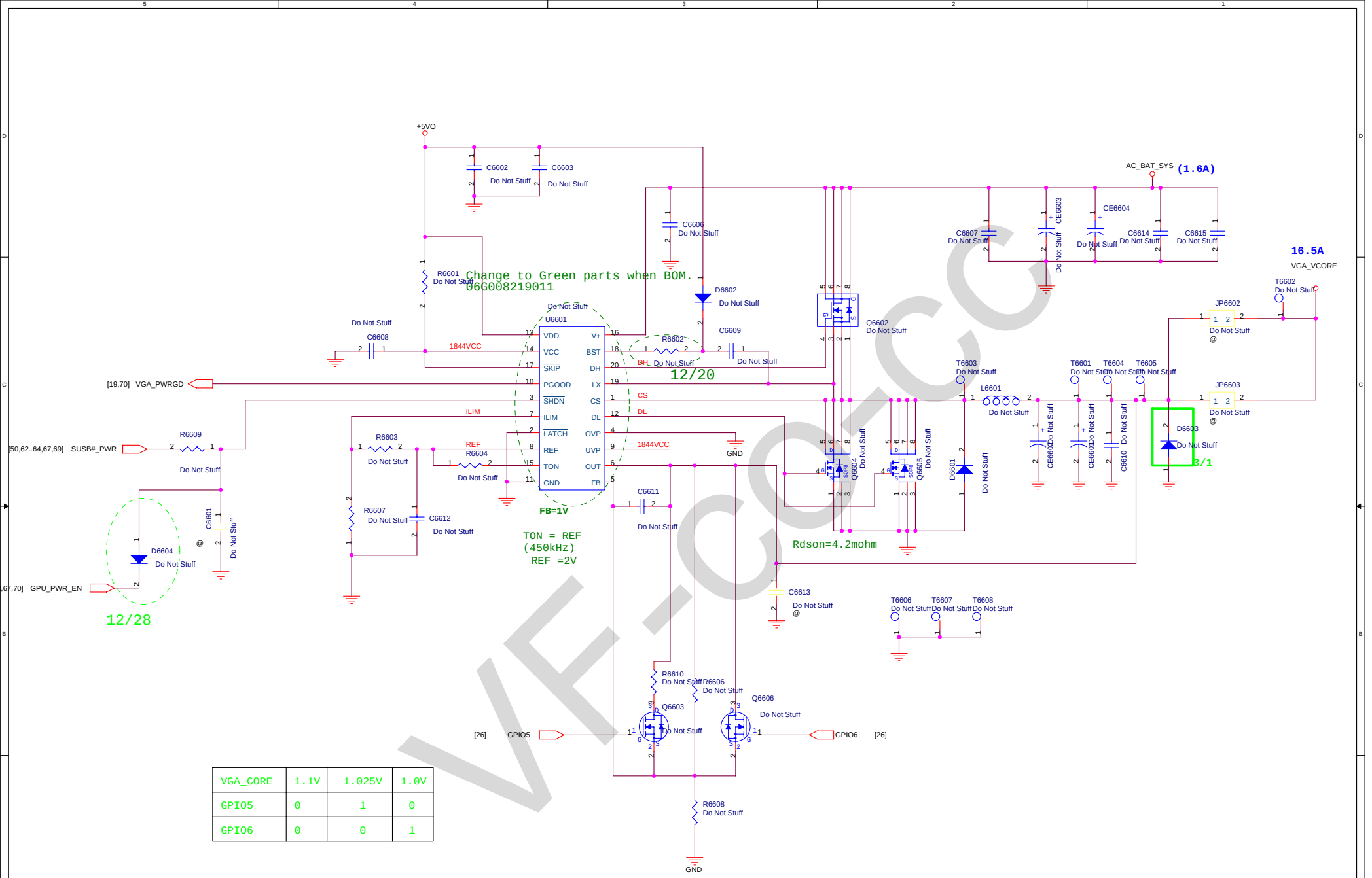
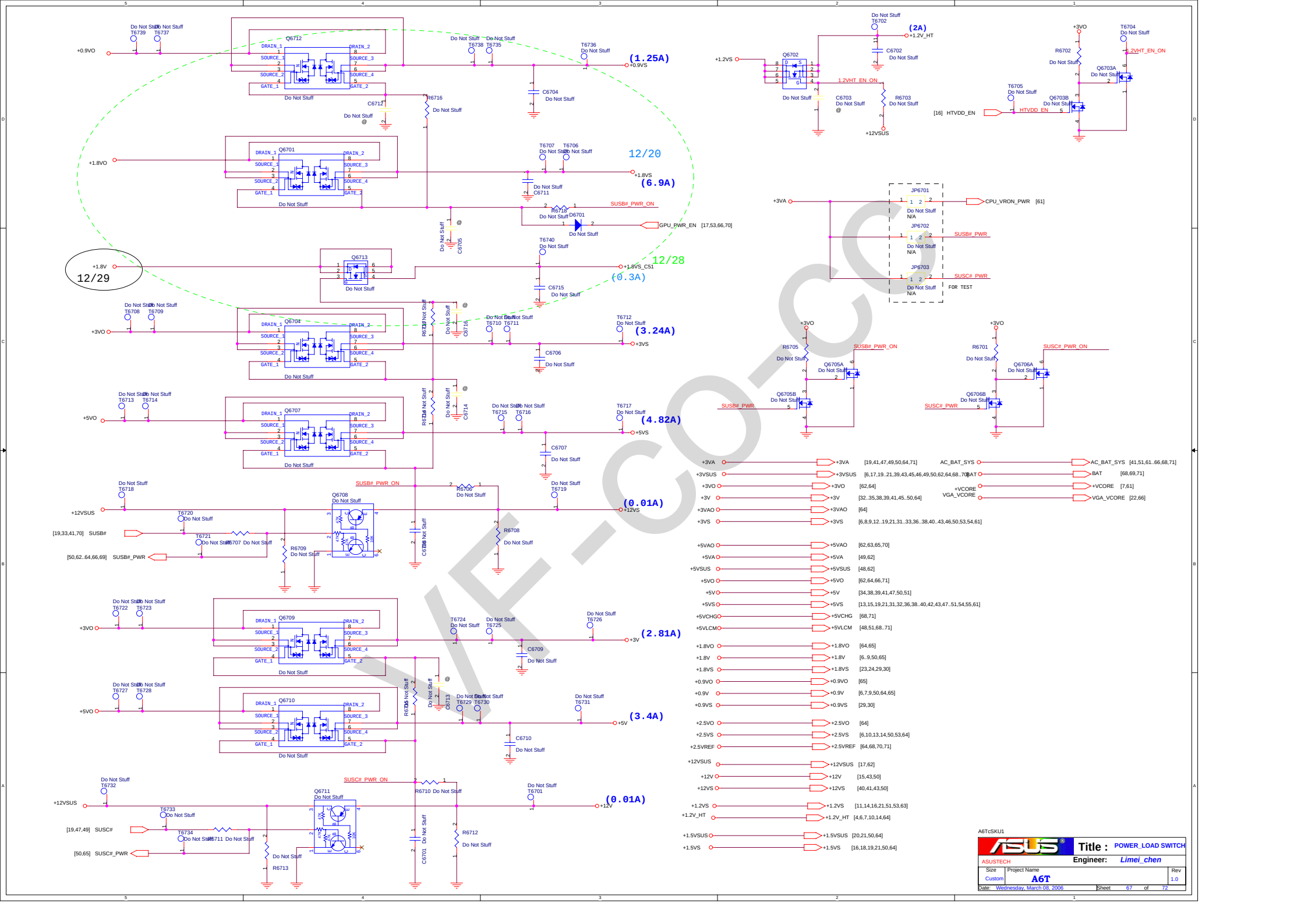


VGA_CORE	1.1V	1.025V	1.0V
GPIO5	0	1	0
GPIO6	0	0	1

A6TcSKU1

ASUSTECH	Title : POWER_VGACORE	
	Engineer: Limei_chen	
Size: Custom	Project Name: A6T	Rev: 1.0
Date: Wednesday, March 08, 2006	Sheet 66 of 72	


+0.9VO
Q6712
+0.9VS
(1.25A)
+1.8VO
Q6701
+1.8VS
(6.9A)
12/20
+1.8V
12/29
Q6713
+1.8VS_C51
12/28
(0.3A)
+3VO
Q6704
+3VS
(3.24A)
+5VO
Q6707
+5VS
(4.82A)
+12VSUS
Q6708
+12VS
(0.01A)
+3VO
Q6709
+3V
(2.81A)
+5VO
Q6710
+5V
(3.4A)
+12VSUS
Q6711
+12V
(0.01A)
Q6702
(2A)
+1.2V_HT
+12VSUS
+3VO
R6702
Q6703A
Q6703B
T6705
[16] HTVDD_EN
HTVDD_EN
+3VA
JP6701
CPU_VRON_PWR [61]
JP6702
SUSB#_PWR
JP6703
SUSC#_PWR
FOR TEST
R6705
Q6705A
Q6705B
SUSB#_PWR_ON
R6701
Q6706A
Q6706B
SUSC#_PWR_ON
GPU_PWR_EN [17,53,66,70]
[19,33,41,70] SUSB#
[50,62..64,66,69] SUSB#_PWR
[19,47,49] SUSC#
[50,65] SUSC#_PWR
+3VA [19,41,47,49,50,64,71]
+3VSUS [6,17,19..21,39,43,45,46,49,50,62,64,68..70]
+3VO [62,64]
+3V [32..35,38,39,41,45..50,64]
+3VAO [64]
+3VS [6,8,9,12..19,21,31..33,36..38,40..43,46,50,53,54,61]
+5VAO [62,63,65,70]
+5VA [49,62]
+5VSUS [48,62]
+5VO [62,64,66,71]
+5V [34,38,39,41,47,50,51]
+5VS [13,15,19,21,31,32,36,38..40,42,43,47..51,54,55,61]
+5VCHG [68,71]
+5VLCM [48,51,68..71]
+1.8VO [64,65]
+1.8V [6..9,50,65]
+1.8VS [23,24,29,30]
+0.9VO [65]
+0.9V [6,7,9,50,64,65]
+0.9VS [29,30]
+2.5VO [64]
+2.5VS [6,10,13,14,50,53,64]
+2.5VREF [64,68,70,71]
+12VSUS [17,62]
+12V [15,43,50]
+12VS [40,41,43,50]
+1.2VS [11,14,16,21,51,53,63]
+1.2V_HT [4,6,7,10,14,64]
+1.5VSUS [20,21,50,64]
+1.5VS [16,18,19,21,50,64]
AC_BAT_SYS [41,51,61..66,68,71]
BAT [68,69,71]
+VCORE [7,61]
VGA_VCORE [22,66]
A6TcSKU1
Title : POWER_LOAD SWITCH
ASUSTECH
Engineer: Limei_chen
Size Custom
Project Name A6T
Rev 1.0
Date: Wednesday, March 08, 2006
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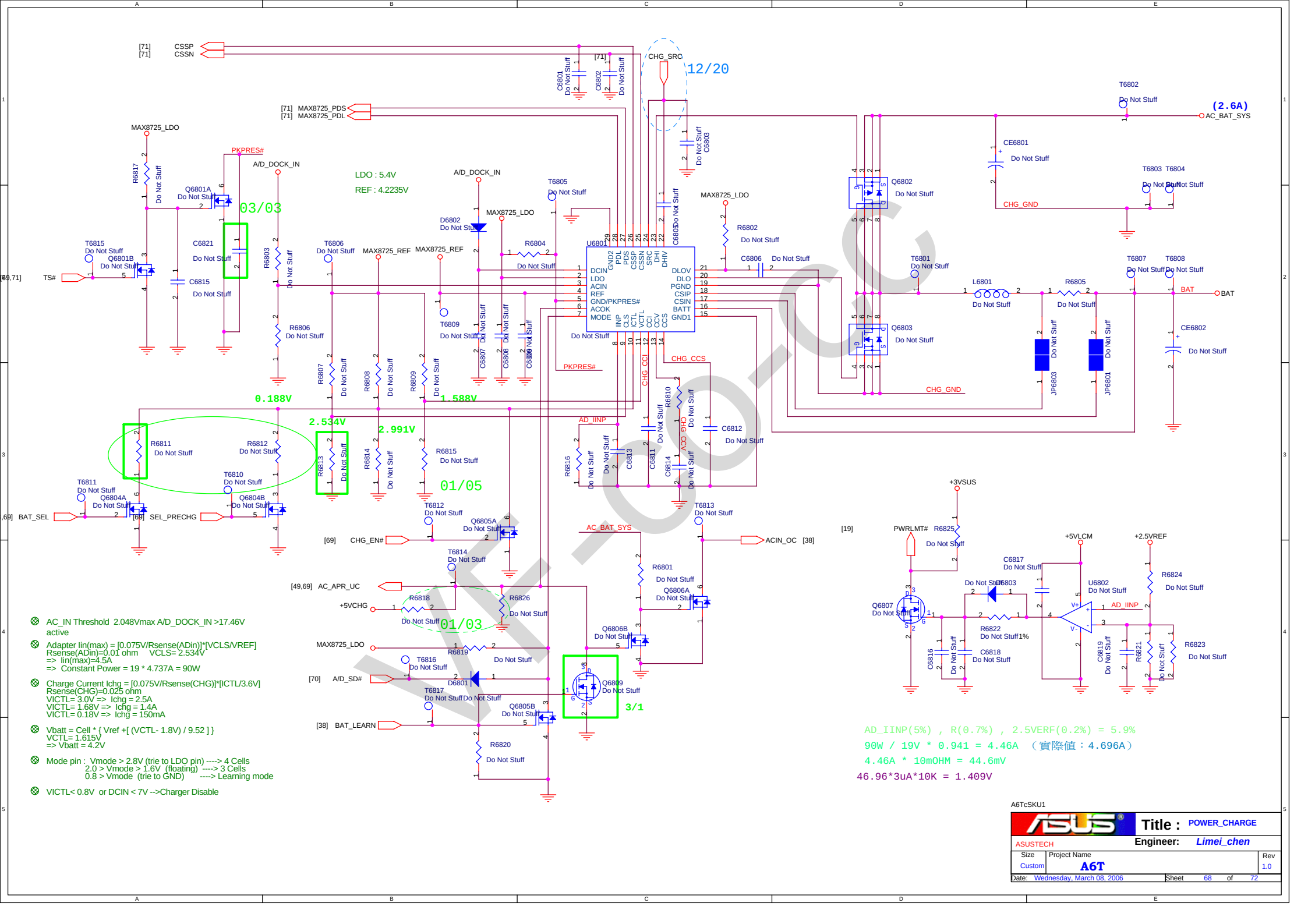
[71] CSSP
[71] CSSN
CHG_SRC
12/20
[71] MAX8725_PDS
[71] MAX8725_PDL
MAX8725_LDO
PKPRES#
A/D_DOCK_IN
LDO : 5.4V
REF : 4.2235V
03/03
01/05
01/03
3/1
0.188V
2.534V
2.991V
1.588V
U6801
DCIN
LDO
ACIN
REF
GND/PKPRES#
ACOK
MODE
DLOV
DLO
PGND
CSIP
CSIN
BATT
GND1
CHG_CCI
CHG_CCS
AD_IINP
CHG_CCV
TS#
BAT_SEL
SEL_PRECHG
CHG_EN#
AC_APR_UC
A/D_SD#
BAT_LEARN
ACIN_OC [38]
AC_BAT_SYS
CHG_GND
BAT
(2.6A)
AC_BAT_SYS
+3VSUS
+5VLCM
+2.5VREF
+5VCHG
PWRLMT# R6825
AD_IINP
AD_IINP(5%) , R(0.7%) , 2.5VERF(0.2%) = 5.9%
90W / 19V * 0.941 = 4.46A （實際值：4.696A）
4.46A * 10mOHM = 44.6mV
46.96*3uA*10K = 1.409V
AC_IN Threshold 2.048Vmax A/D_DOCK_IN >17.46V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.01 ohm VCLS= 2.534V
=> Iin(max)=4.5A
=> Constant Power = 19 * 4.737A = 90W
Charge Current Ichg = [0.075V/Rsense(CHG)]*[ICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3.0V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A
VICTL= 0.18V => Ichg = 150mA
Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }
VCTL= 1.615V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable
A6TcSKU1
Title : POWER_CHARGE
ASUSTECH
Engineer: Limei_chen
Size Custom
Project Name A6T
Rev 1.0
Date: Wednesday, March 08, 2006
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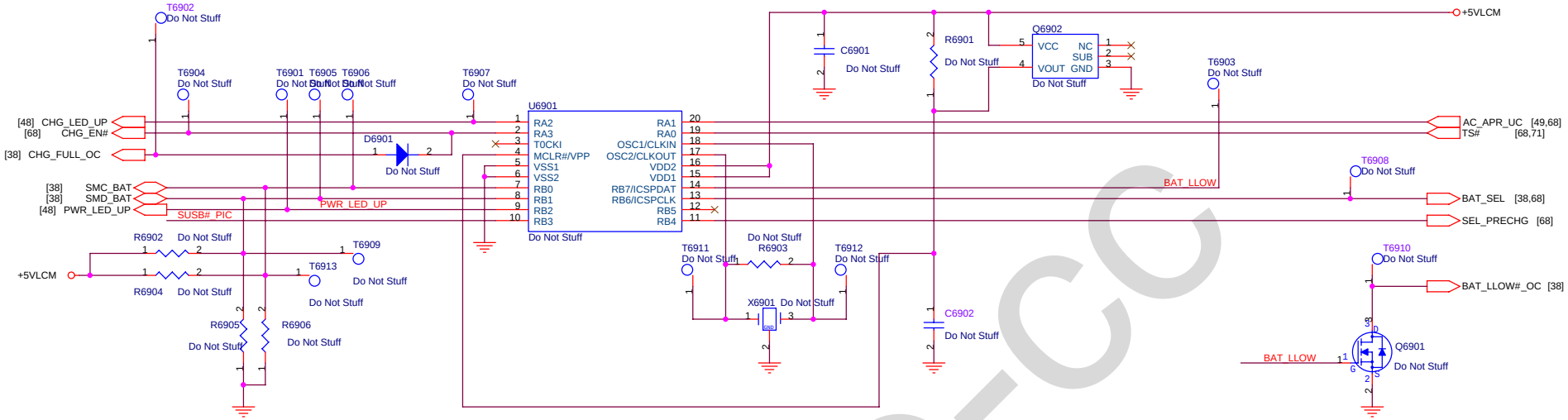

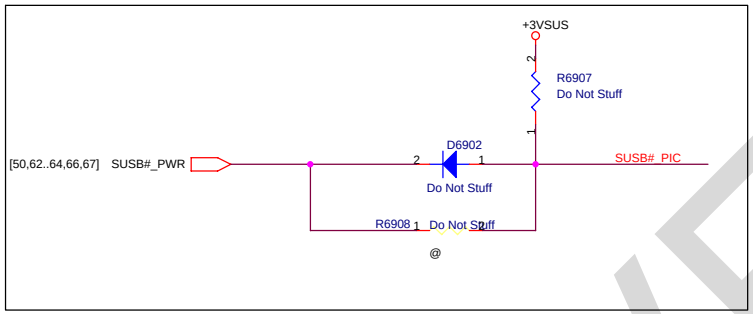

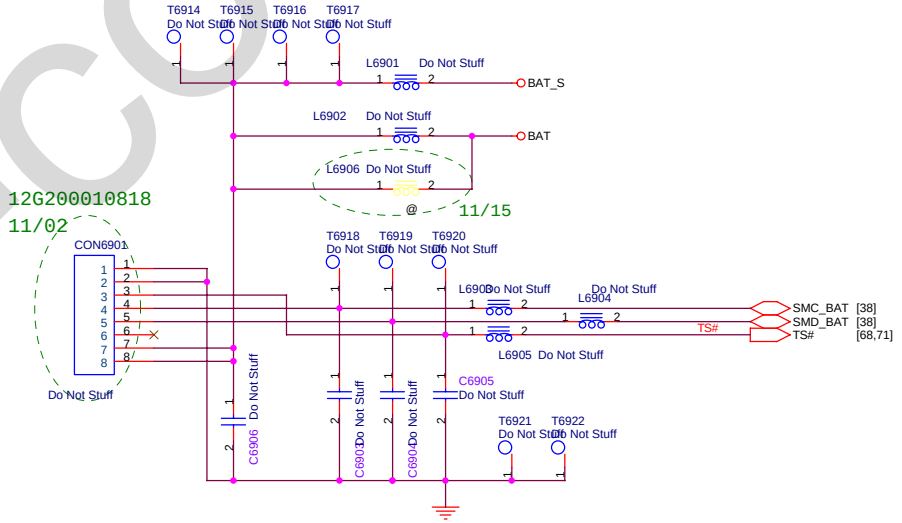

A6TcSKU1

ASUSTECH

Title : POWER_PIC

Engineer: Limei_chen

Size	Project Name	Rev
Custom	A6T	1.0

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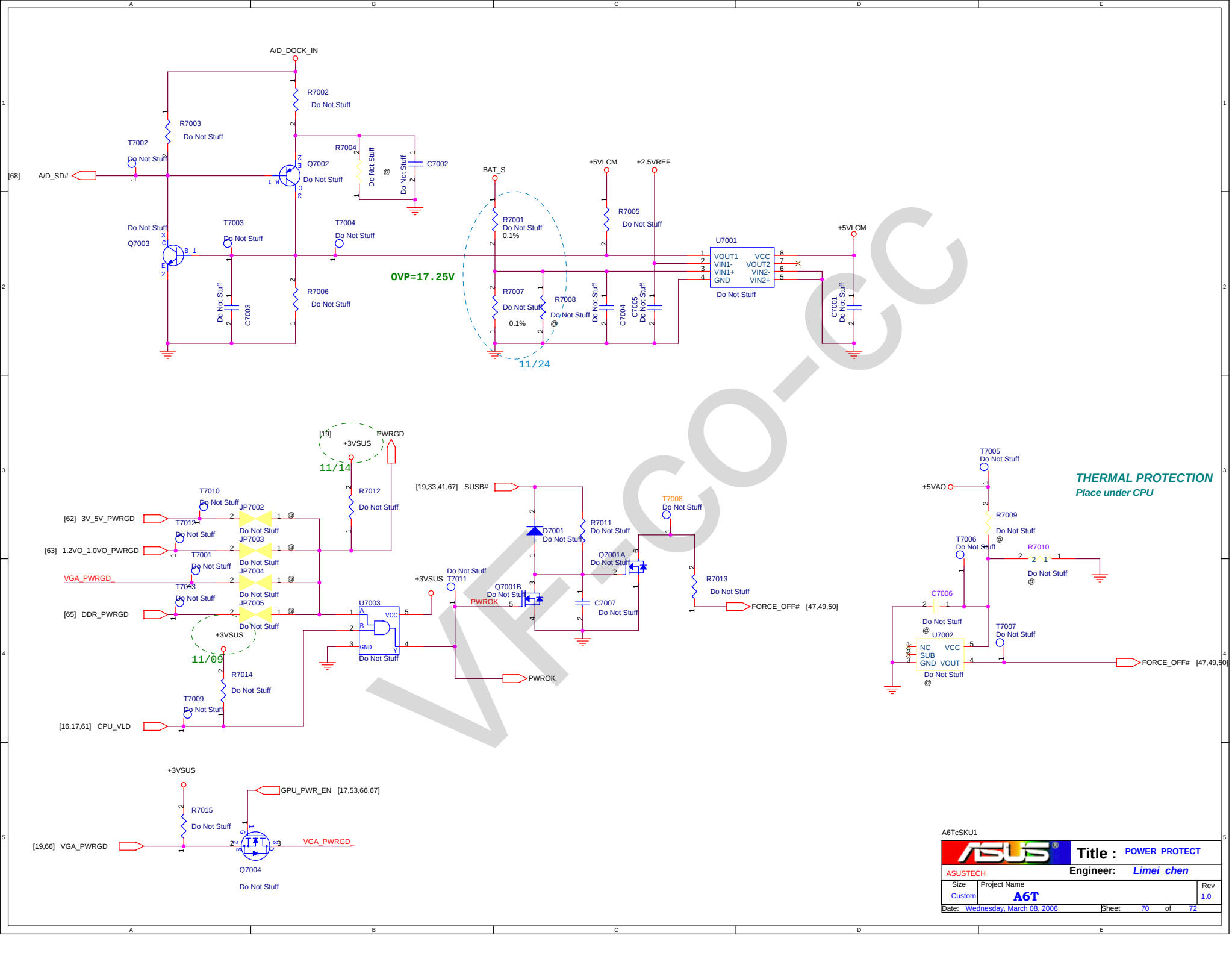

A6TcSKU1

ASUSTECH

Title : POWER_PROTECT

Engineer: Limei_chen

Size	Project Name	Rev
Custom	A6T	1.0

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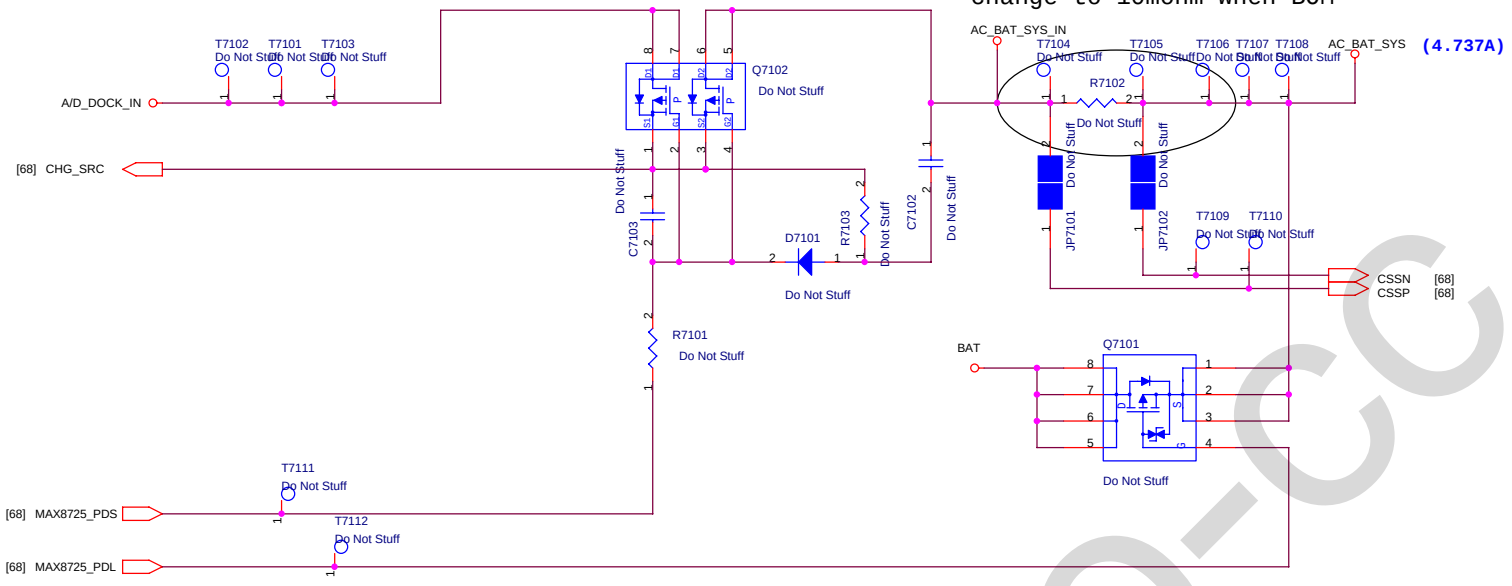
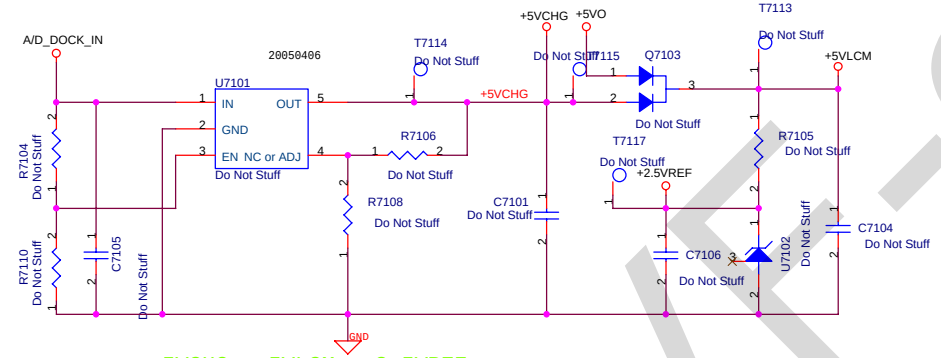
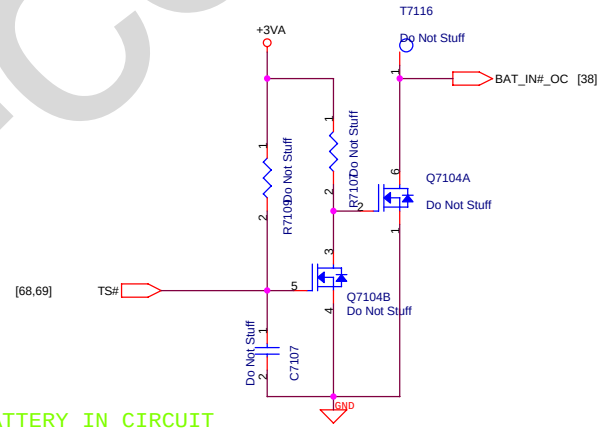
change to 10mohm when BOM





+5VCHG, +5VLCM, +2.5VREF

Ref: 1.24V
ON: EN>2V (A/D_DOCK_IN:17V)
OFF: EN<0.6V(A/D_DOCK_IN:5.1V)



BATTERY IN CIRCUIT

A6TcSKU1

ASUSTECH	Title : POWER_SWITCH_5VLCM	
	Engineer: Limei_chen	
Size: Custom	Project Name: A6T	Rev: 1.0
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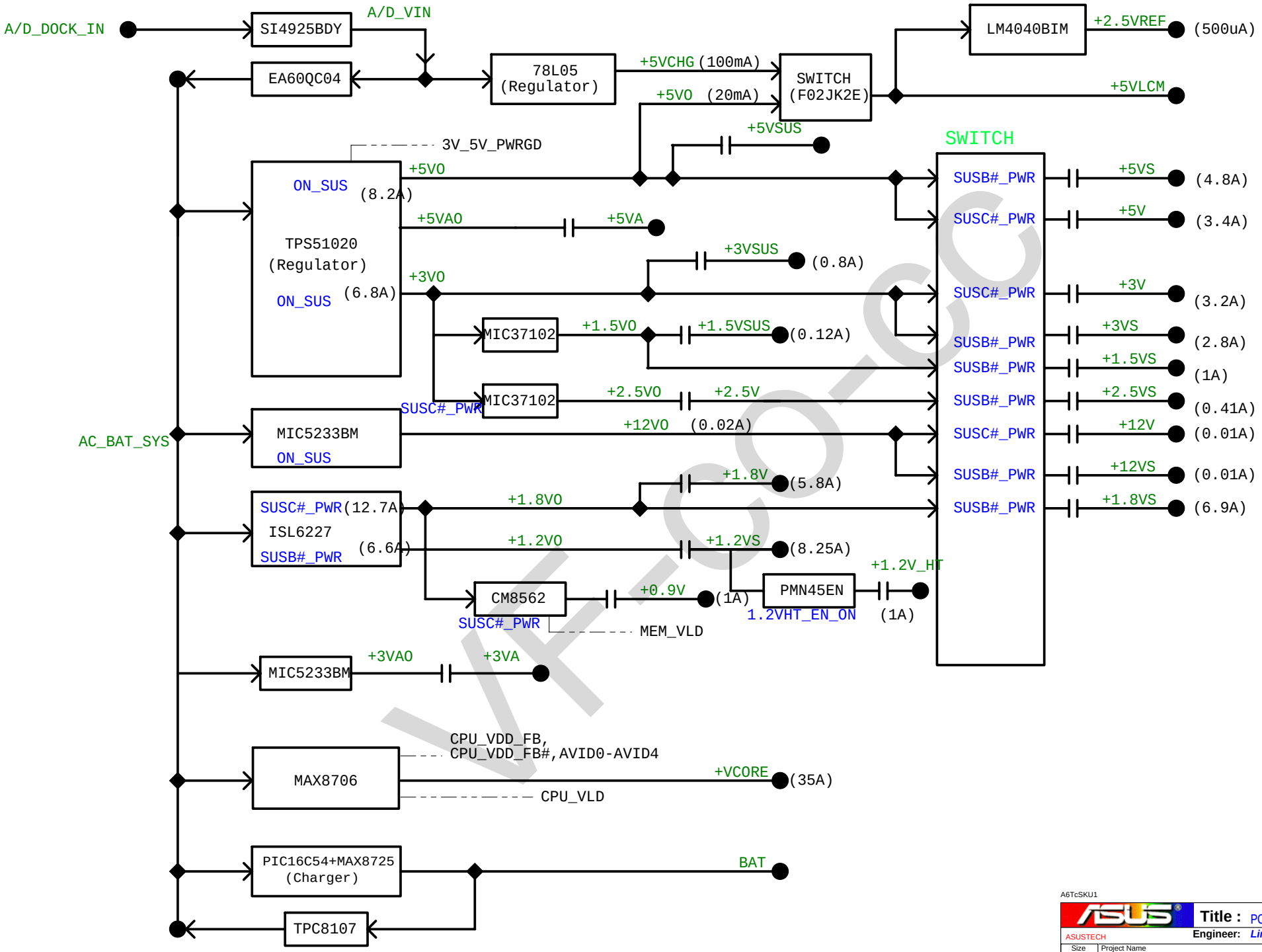

A6TcSKU1

ASUSTECH

Title : POWER DIAGRAM

Engineer: Limei_chen

Size	Project Name	Rev
Custom	A6T	1.0

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12/20	P62	Add CE6205 100UF/6.3V(the high trancient ripple)
	P62	change L6202 from 1.8uh to 3.7uh (because of the low enficiency and the thermal issue)
	P63	change R6312 from 1K to 6.81K
	P63	change R6315 from 9.09K to 20K
	P66	Add C6614 1UF/25V(due to bad Highside Gate)
	P66	change R6602 from 0ohm to 2.7ohm(due to bad Highside Gate)
	P67	exchange 0.9VS &1.8VS
	P67	change Q6702 to SI4800(due to the Voltage is low)
	P67	change Q6702 from PMN45EN(Rdson=40mohm-max)to SI4800(Rdson=18.5mohm-max)
	P68	change C6807 from 1UF/25V to 4.7UF/25V
	P68	change A/D_DOCK_in to CHG_SRC
	P71	change C7105 from 1UF/25V to 4.7UF／25V
12/28	P66	Add D6604& net GPU_PWR_EN
	P67	Add Q6713,R6717,C6716,C6715,R6718,D6701
	P67	add net GPU_PWR__EN,+1.8VS_C51
	P62	change L6201 from 1.8uh to 2.8uh (because of the low enficiency and the thermal issue)
	P63	change R6314 from 6.81K to 7.5K(becouse of the low voltage in device side)
12/29	P67	change 1.8VO to 1.8V(EE)
12/30	P68	Add R6826(due to D7103's leakage current is high when the tempreture is high,thermal team 49 degree)
01/03	P61	change R6135 from 100Kohm to 120kohm(due to OCP)
	P65	change R6506 from 330ohm to 402ohm(due to OCP)
	P68	change R6818 from 49.9Kohm to 4.7Kohm
	P68	Add R6826 15Kohm
01/04	P68	connect R6807.2,R6808.2,R6809.2 to MAX8725_REF(due to REF+-0.5%,but LDO +-2.8%)
	P68	change R6807,R6812,R6807,R6808,R6809,R6813,R6814,R6815(due to MAX8725_REF)

A6TcSKU1

ASUSTEK COMPUTER INC

Title : History

Engineer: Rui-xing

Size	Project Name	Rev
C	History	1.00

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