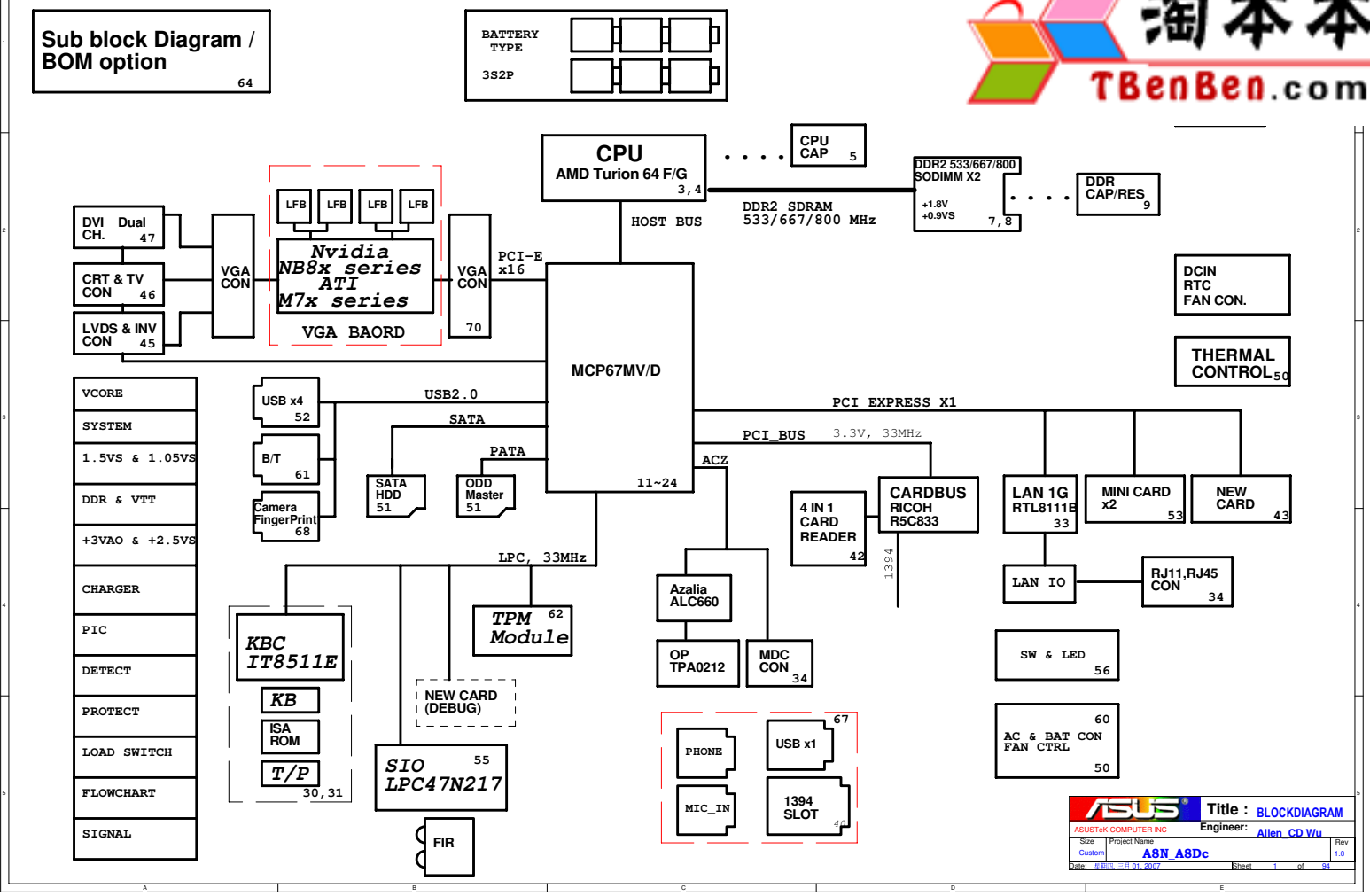
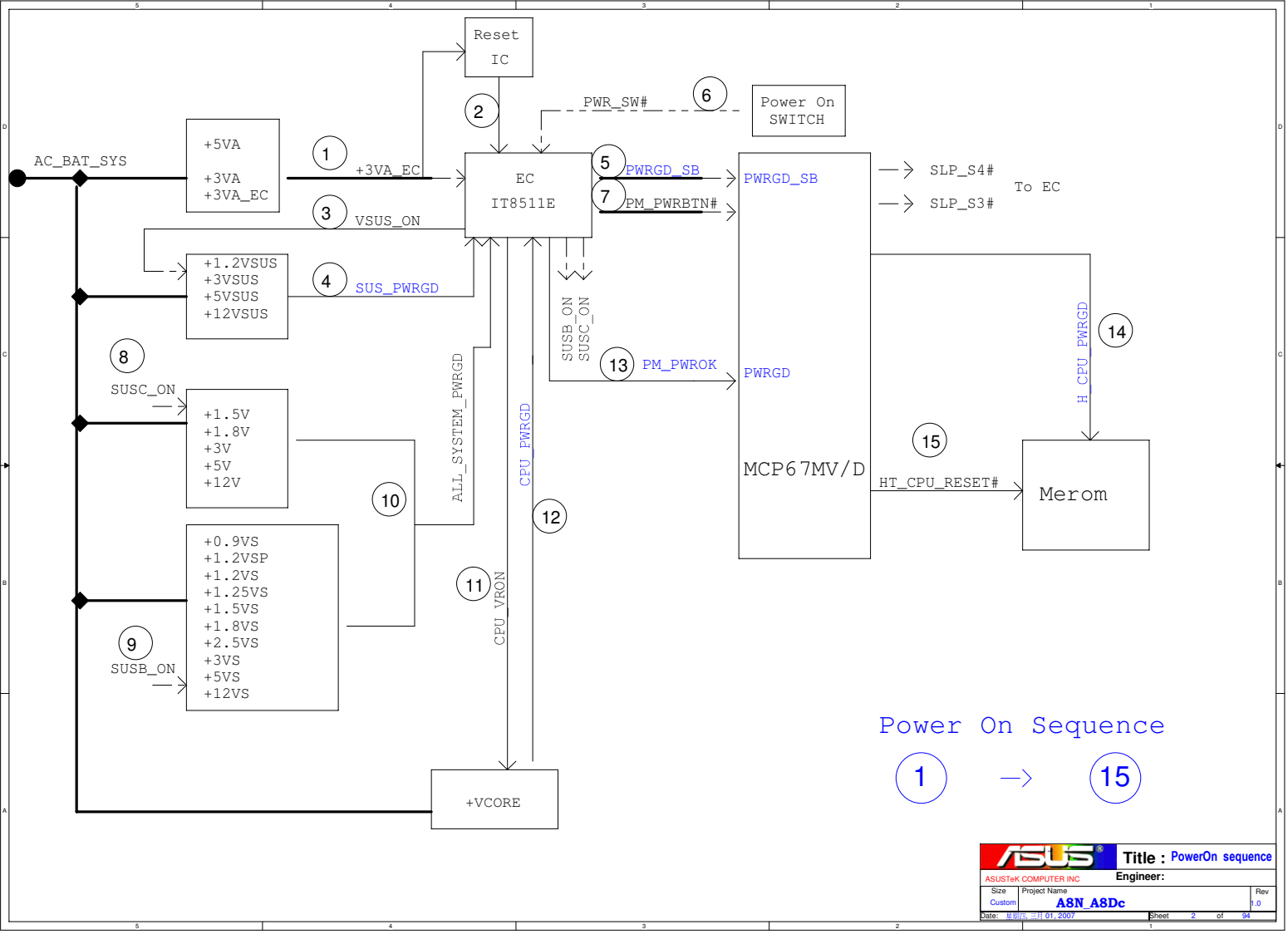
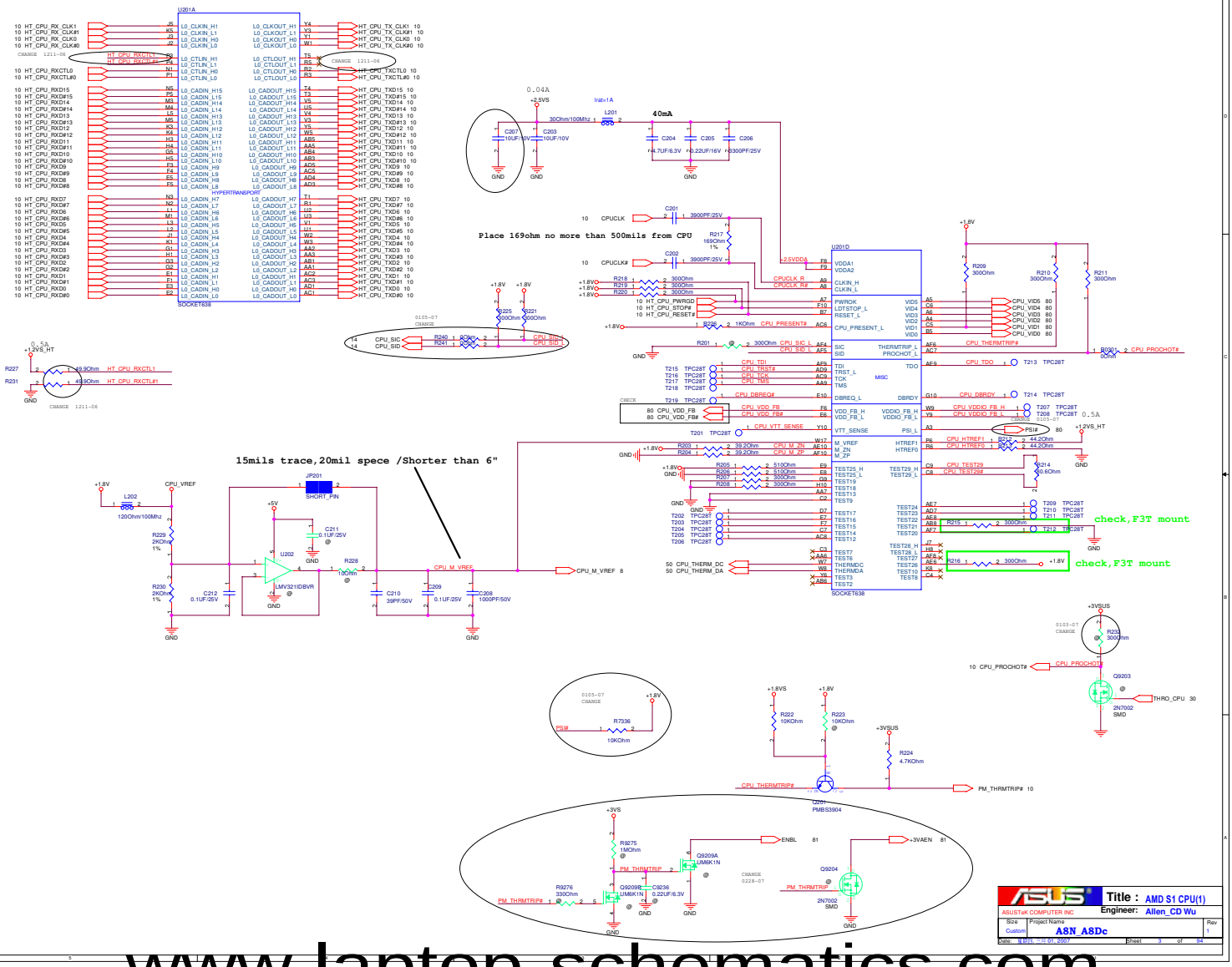
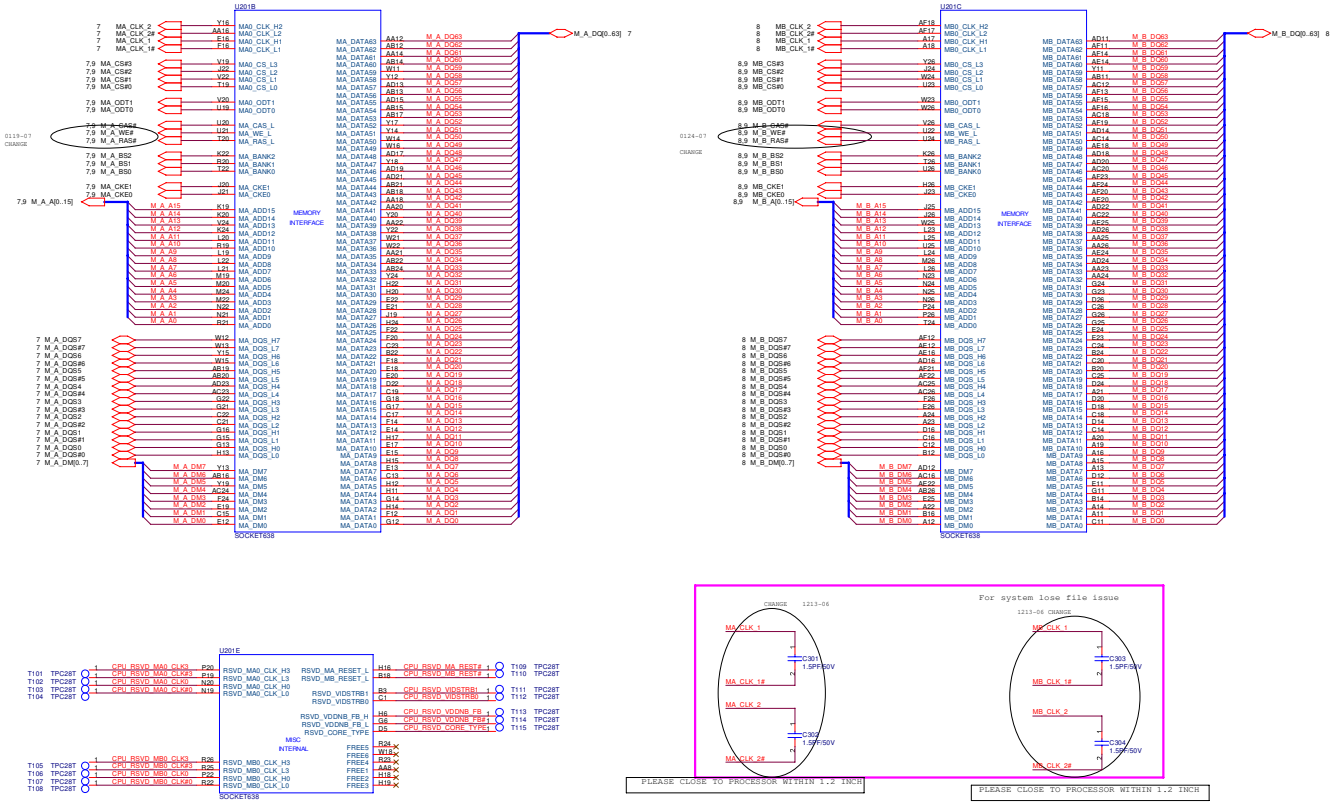
A8N_A8Dc AMD/MCP67MV/MCP67D BLOC

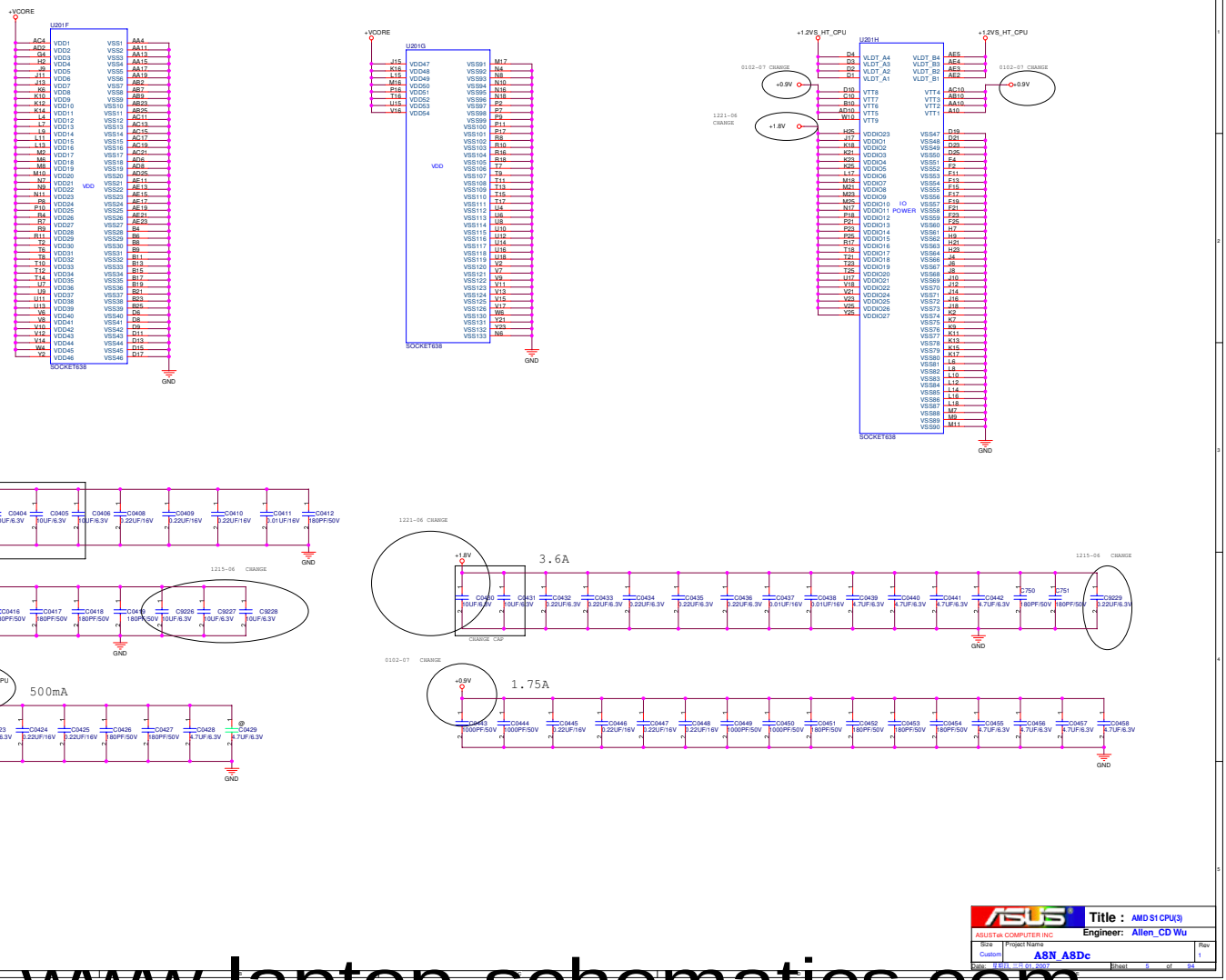




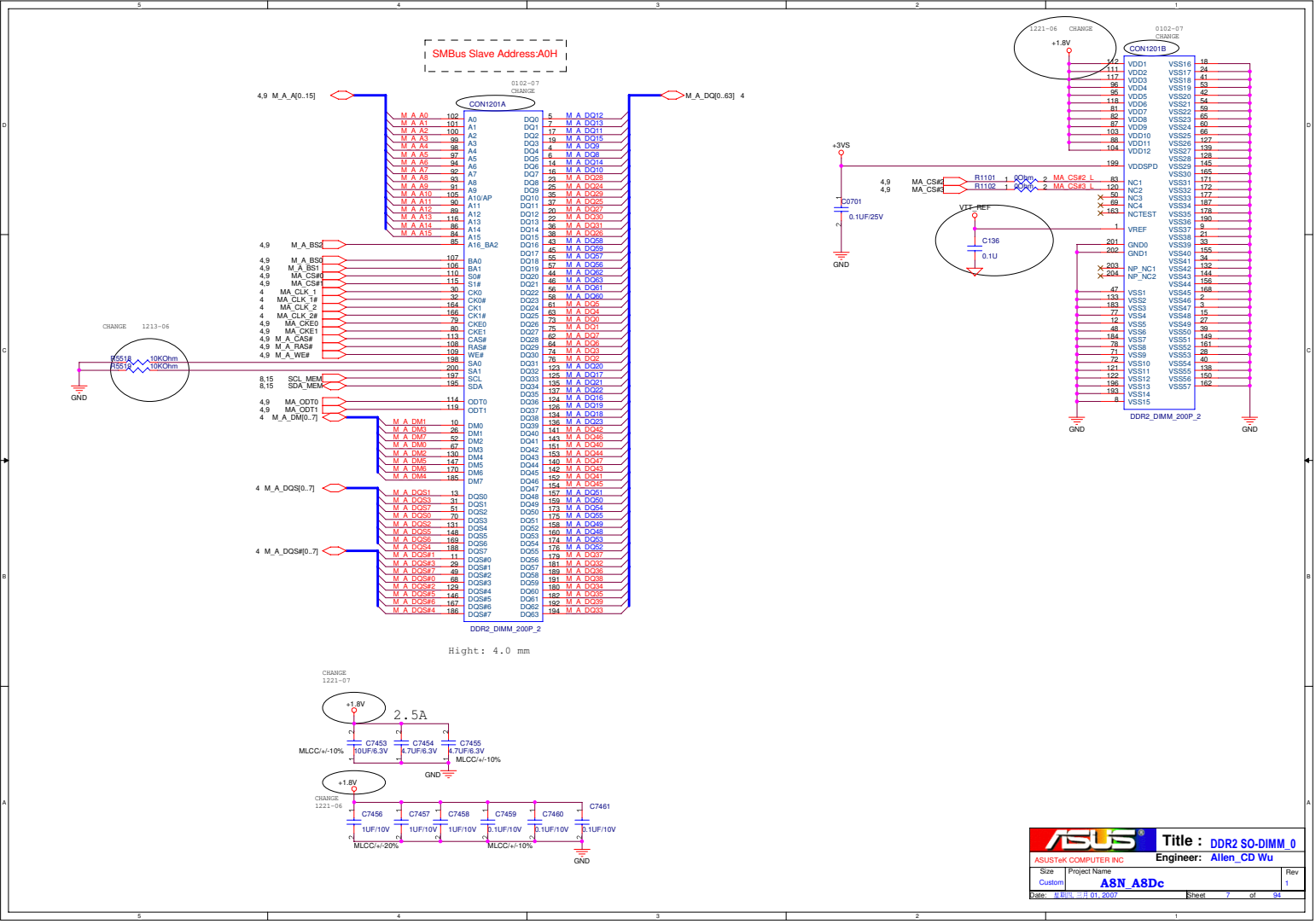


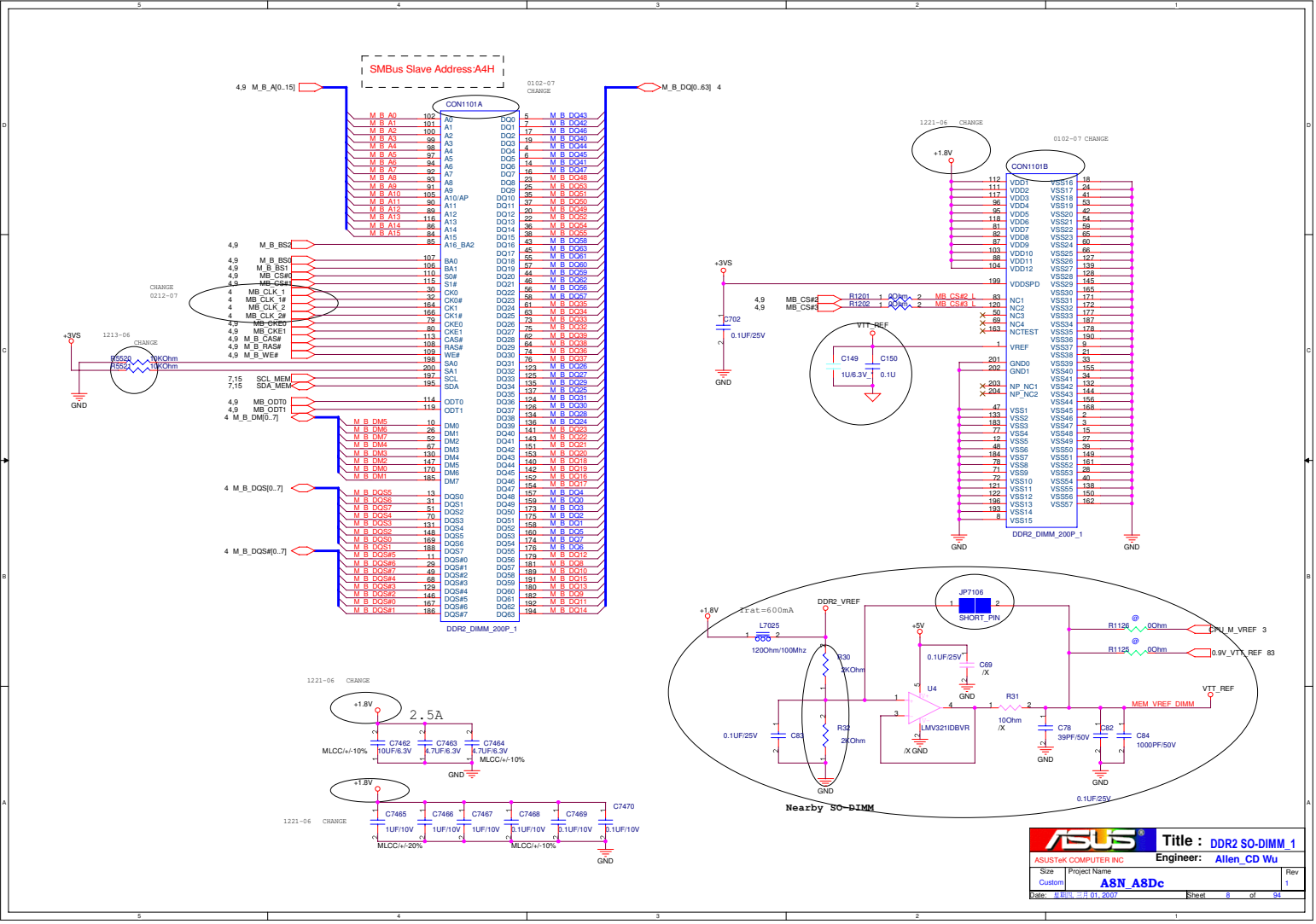


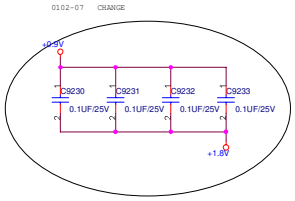
Title :	AMD S1 CPU(2)
ASUSTeK COMPUTER INC	
Engineer:	Allen_CD Wu
Size: Custom	Project Name: A8N_A8Dc
Rev: 1	
Date: 星期日 28 01, 2007	Sheet 4 of 34



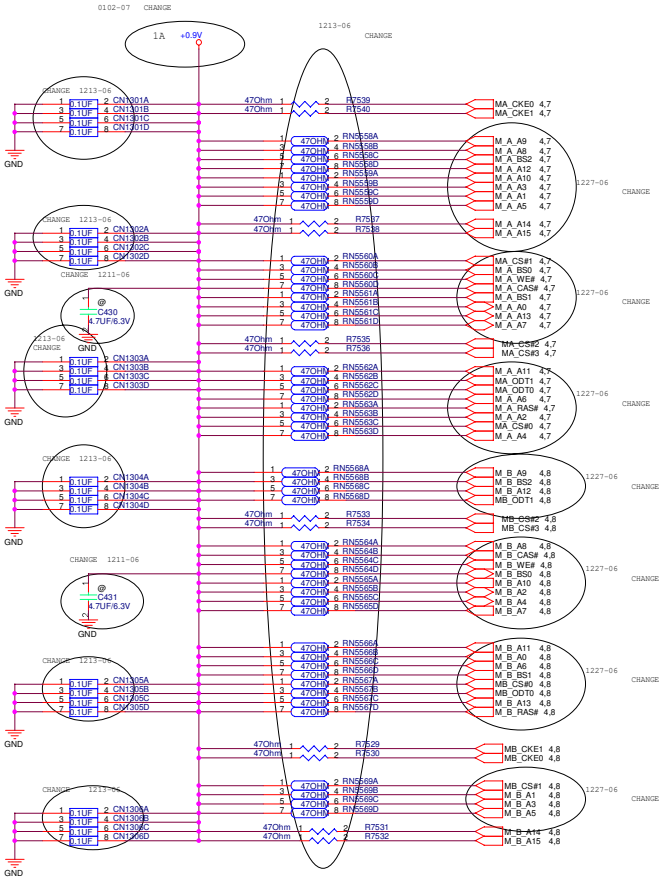
ASUSTek COMPUTER INC	Title : AMD S1 CPU(3)		
	Engineer: Allen_CD Wu		
Size: Custom	Project Name: A8N_A8Dc		Rev: 1
Date: 星期日 28 01, 2007	Sheet 5 of 94		





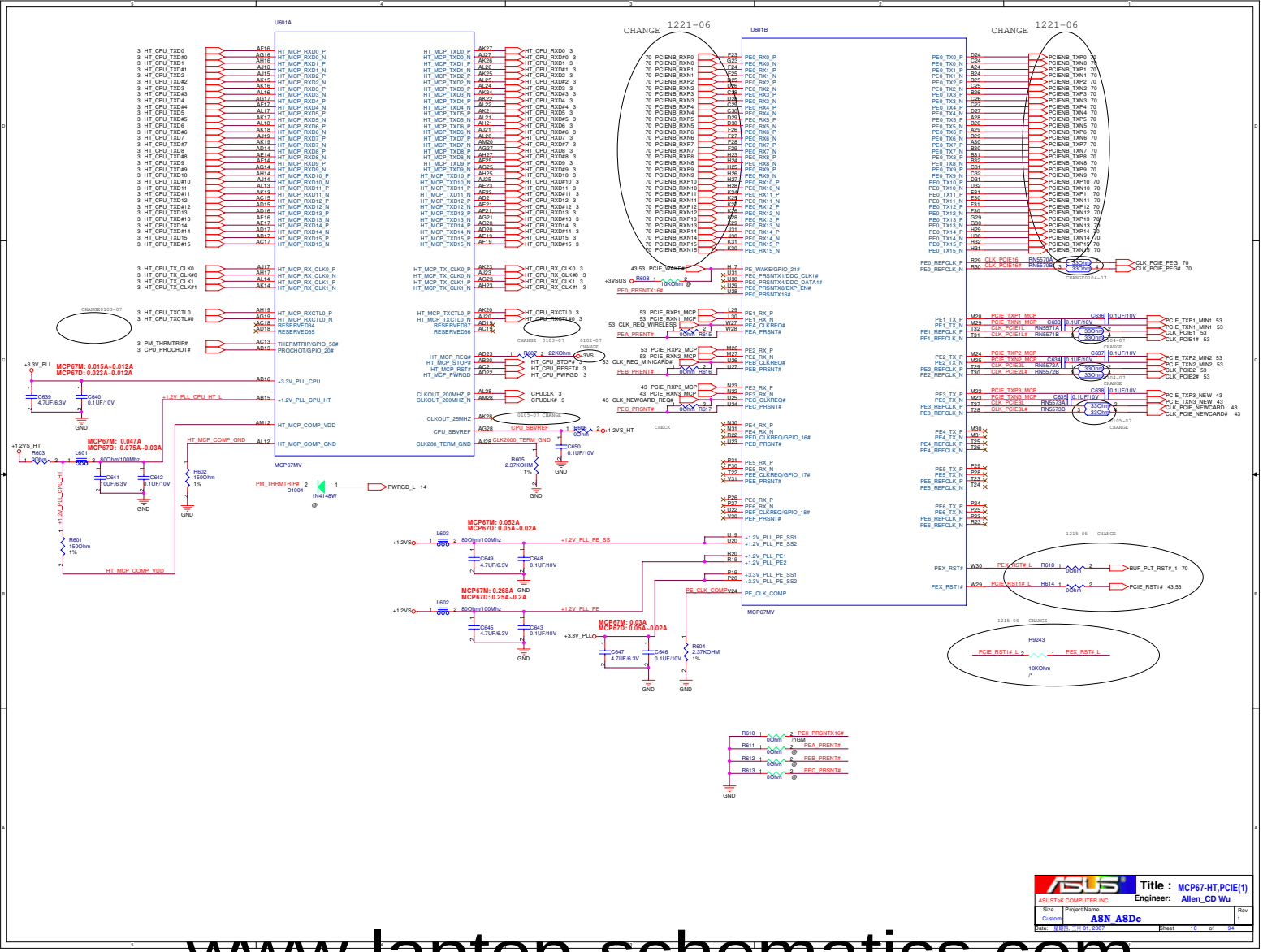


For Address/Command close to the area of plane switched

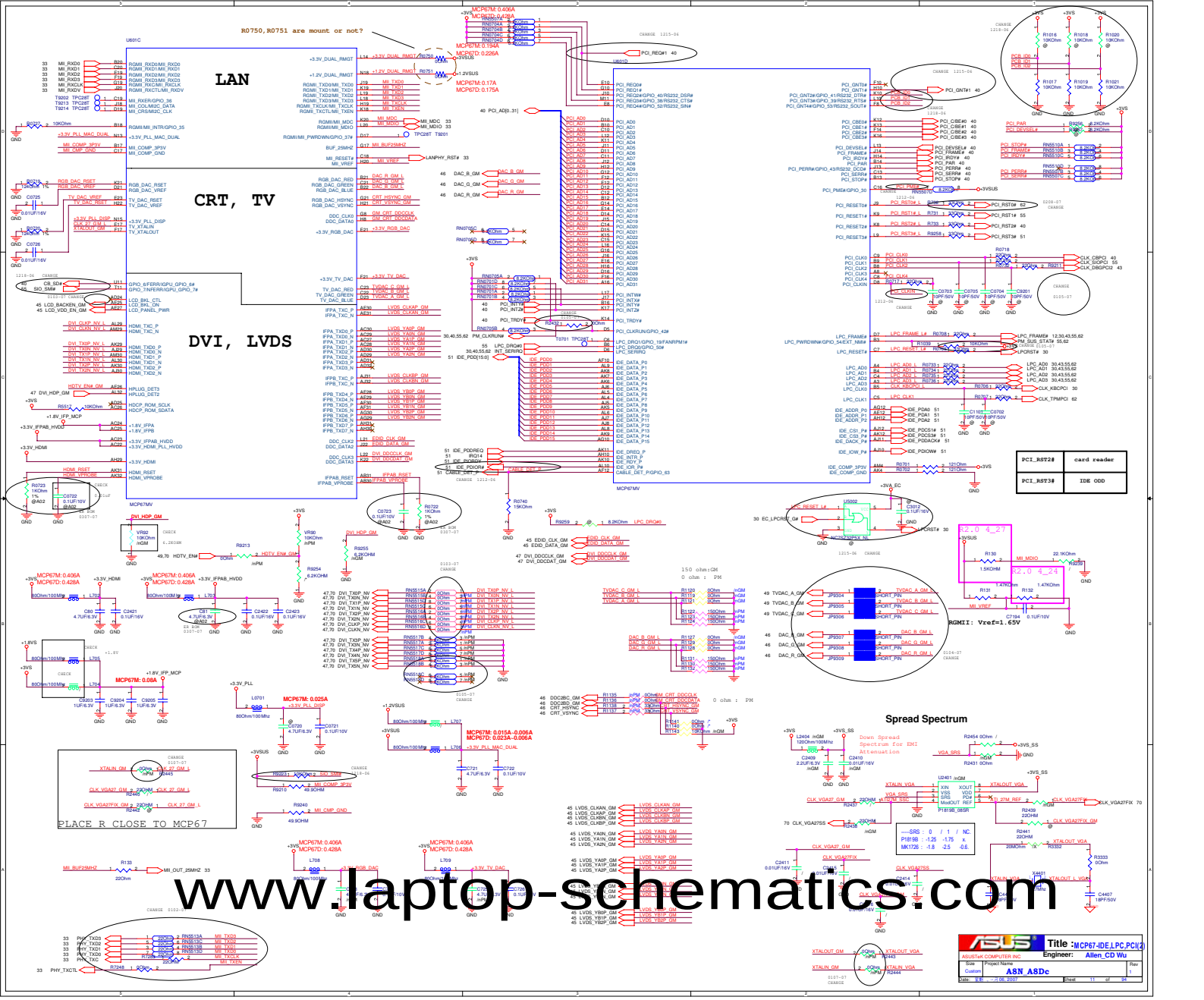


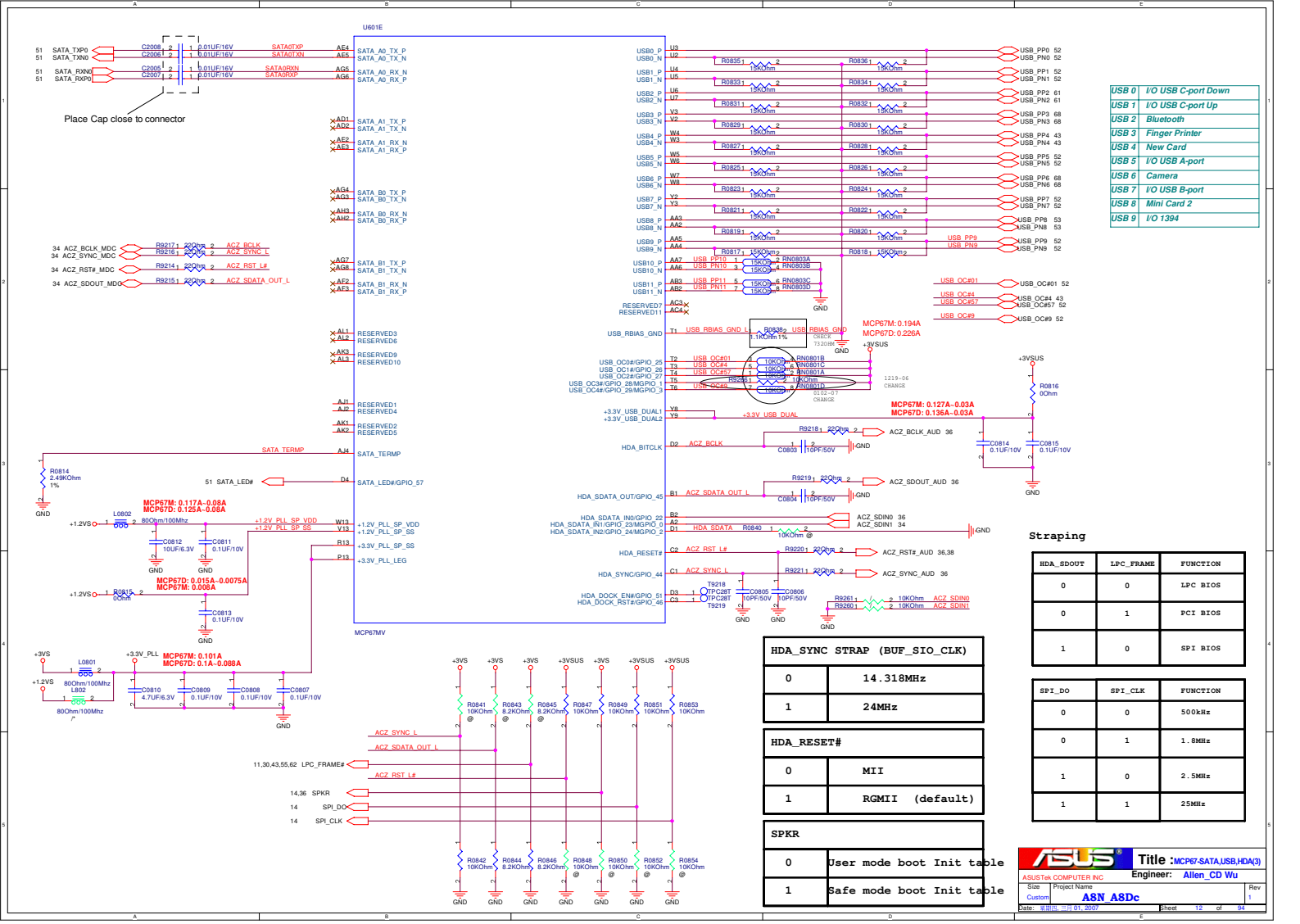
Layout note: Place array cap close to each pullup resistorsterminated to +0.9V

ASUSTeK COMPUTER INC	Title : DDR2 TERMINATION		
	Engineer: Allen_CD Wu		
Size: Custom	Project Name: A8N_A8Dc		Rev: 1
Date: 星期四, 三月 01, 2007	Sheet 9 of 94		



Title :	MCP67-HT,PCIE(1)
ASUSTeK COMPUTER INC	Engineer: Allen_CD Wu
Size: Custom	Project Name: A8N_A8Dc
Rev: 1	
Date: 日期, 一月 01, 2007	Sheet 10 of 34





USB 0	I/O USB C-port Down
USB 1	I/O USB C-port Up
USB 2	Bluetooth
USB 3	Finger Printer
USB 4	New Card
USB 5	I/O USB A-port
USB 6	Camera
USB 7	I/O USB B-port
USB 8	Mini Card 2
USB 9	I/O 1394

Straping

HDA_SDOUT	LPC_FRAME	FUNCTION
0	0	LPC BIOS
0	1	PCI BIOS
1	0	SPI BIOS

SPI_DO	SPI_CLK	FUNCTION
0	0	500kHz
0	1	1.8MHz
1	0	2.5MHz
1	1	25MHz

HDA_SYNC STRAP (BUF_SIO_CLK)	
0	14.318MHz
1	24MHz

HDA_RESET#	
0	MII
1	RGMII (default)

SPKR	
0	User mode boot Init table
1	Safe mode boot Init table

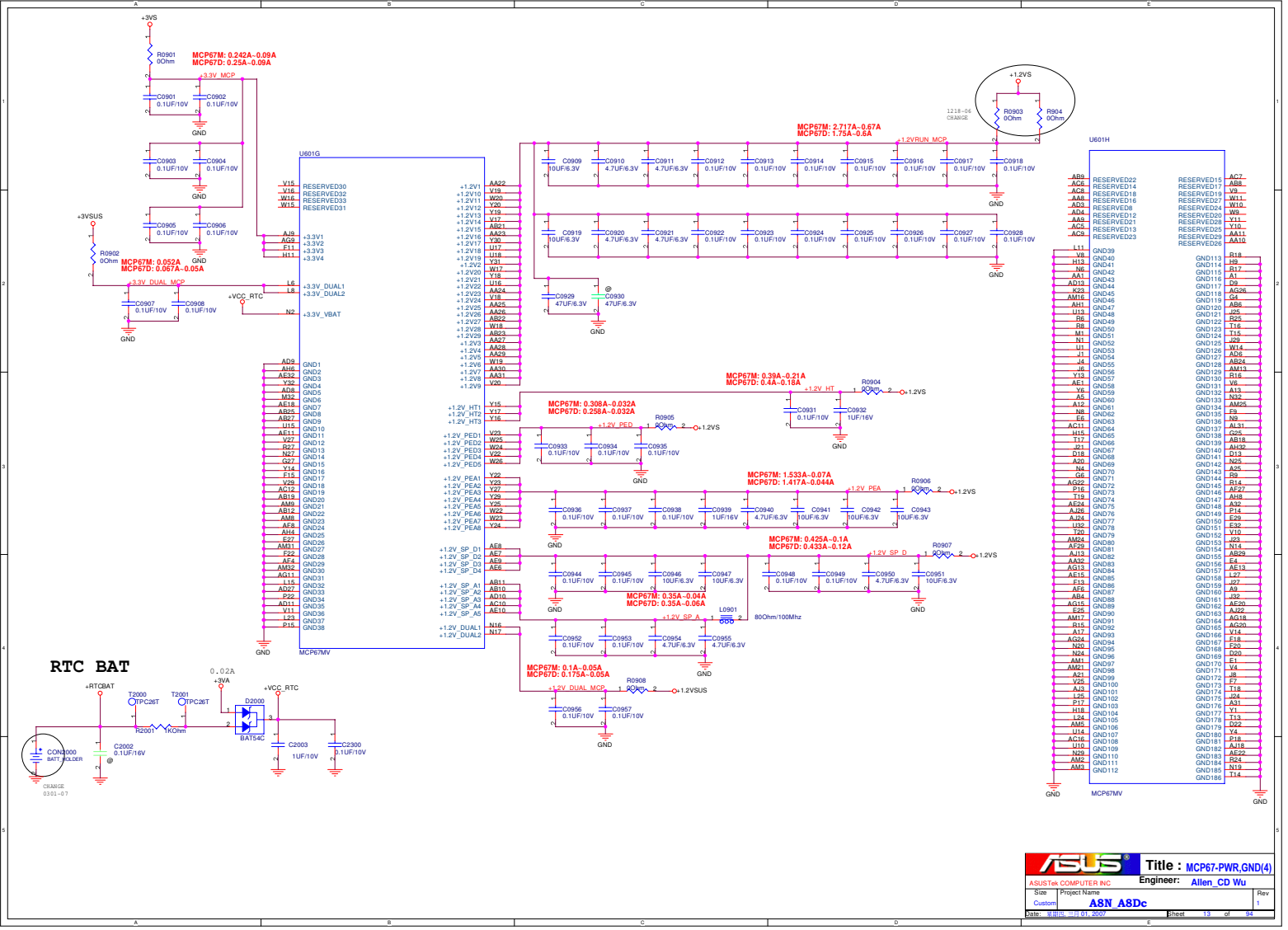
ASUSTeK COMPUTER INC

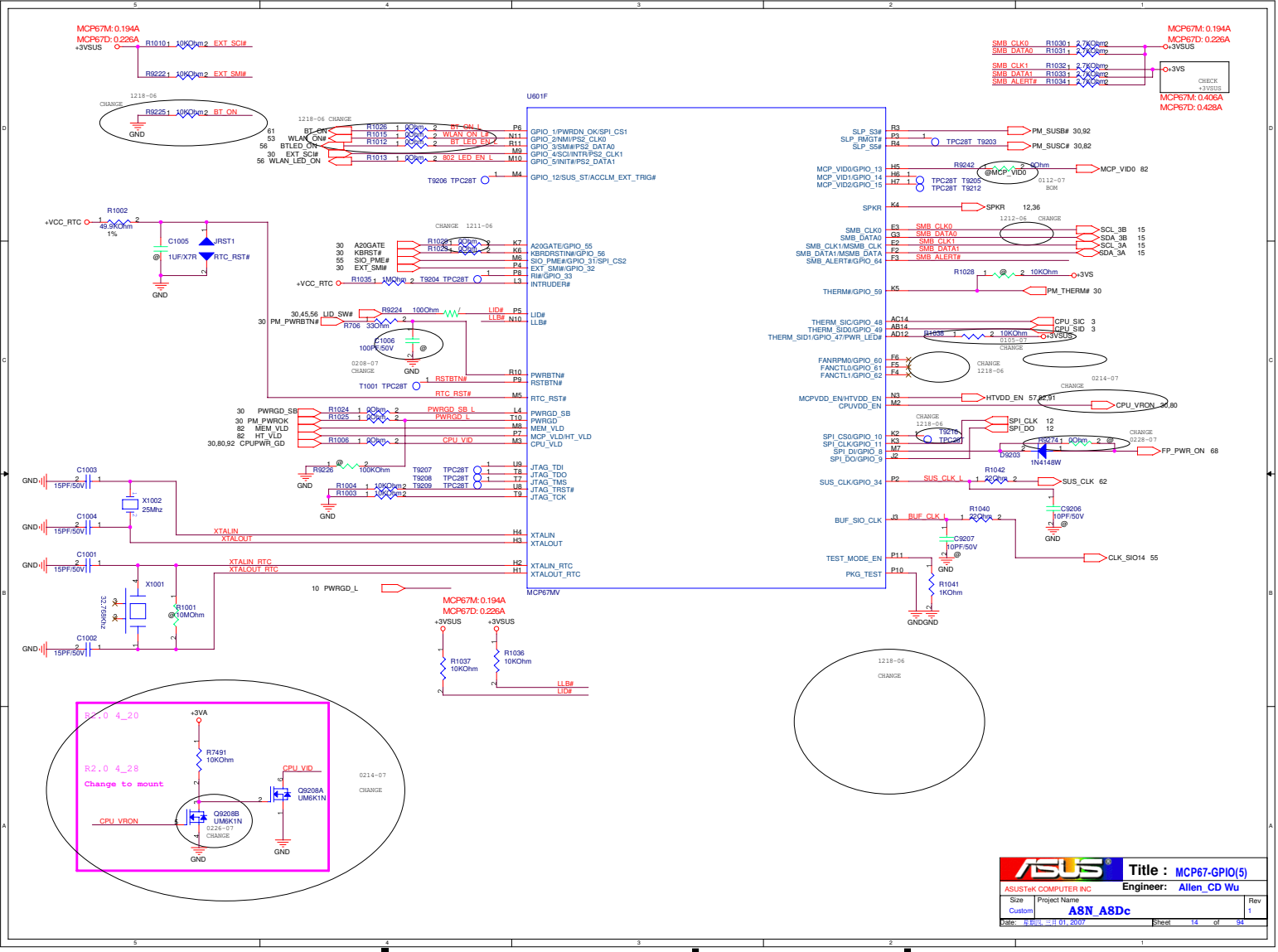
Title : MCP67-SATA,USB,HDA(3)

Engineer: Allen_CD Wu

Size: Custom | Project Name: A8N_A8Dc | Rev: 1

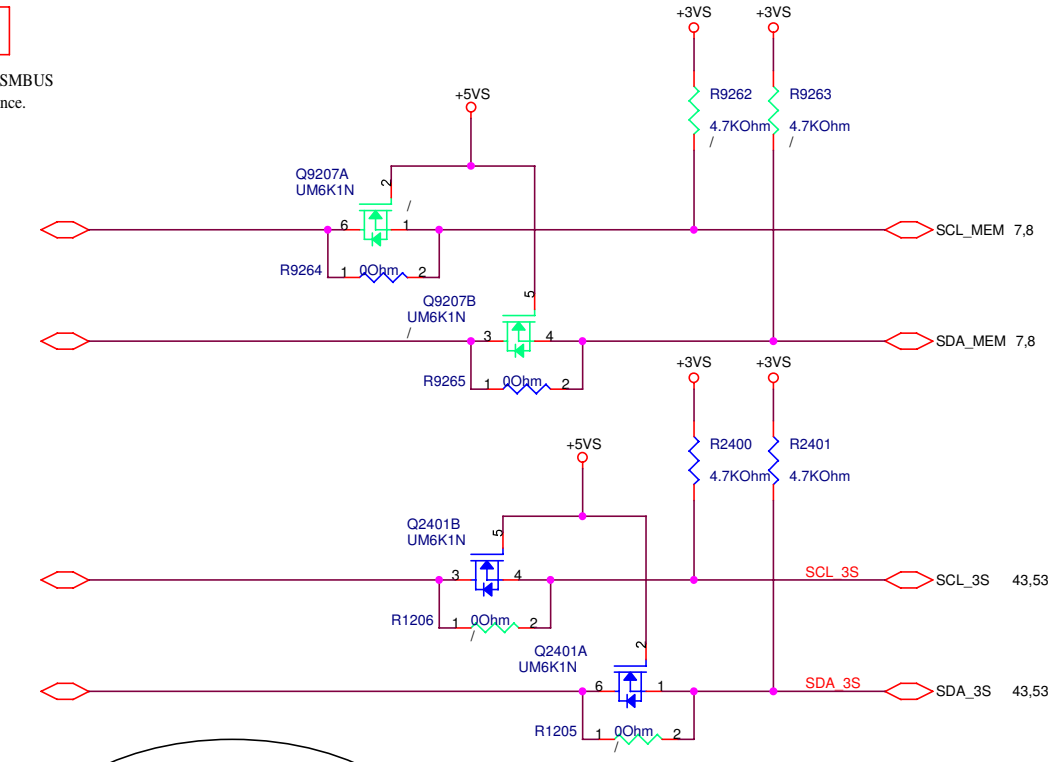
Date: 星期四, 三月 01, 2007 | Sheet 12 of 94

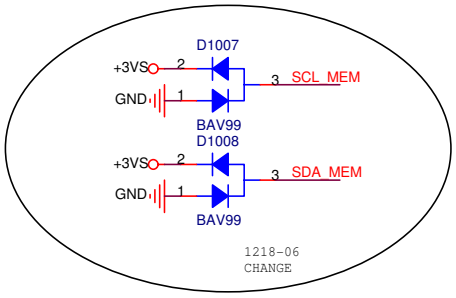




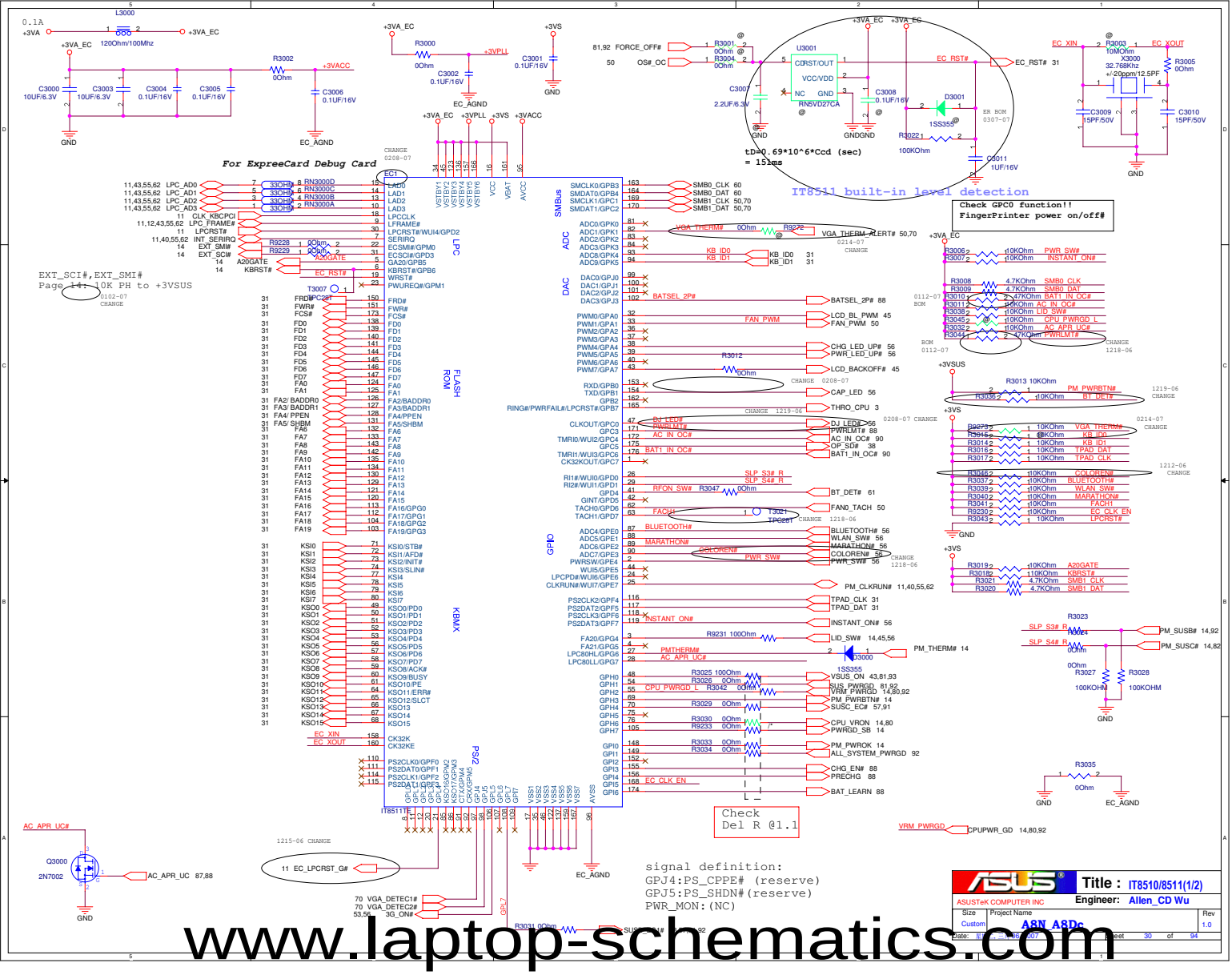
Check

Connect SMLINK and SMBUS
for SMBus 2.0 compliance.

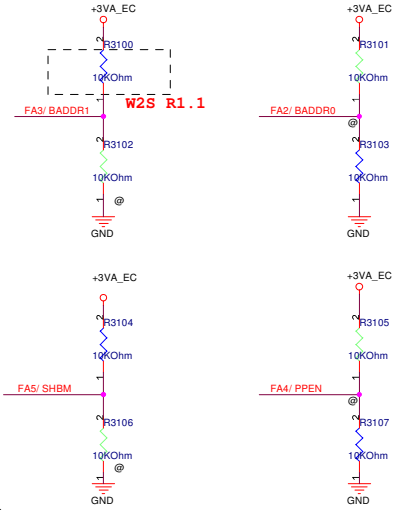




ASUSTeK COMPUTER INC	Title : LEVEL SHIFTER	
	Engineer: Allen_CD Wu	
Size: A	Project Name: A8N_A8Dc	Rev: 1.0
Date: 星期四, 三月 01, 2007	Sheet 15 of 94	



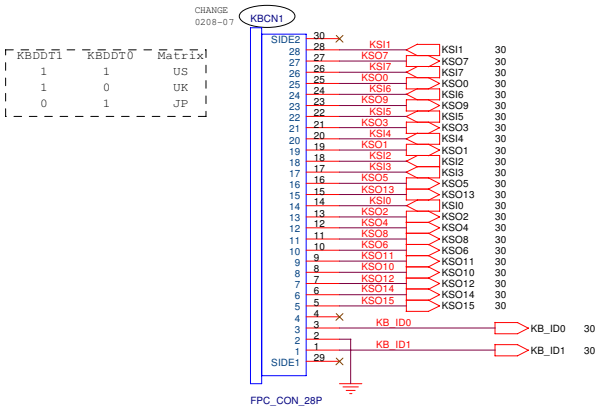
10:Determined by EC

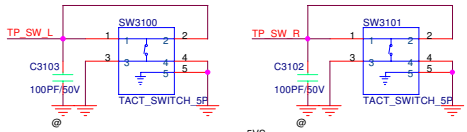


BADDR[1:0]
No pull up:
The register pair to access PNPCFG is 002Eh and 002Fh.
Ext 10K up on BADDR0:
The register pair to access PNPCFG is 004Eh and 004Fh.
Ext 10K up on BADDR1:
The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.

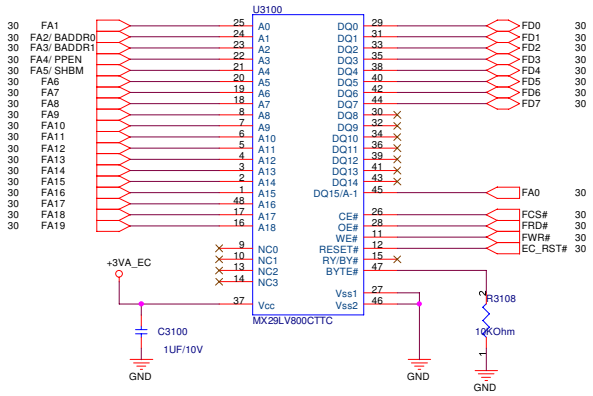
SHBM
No pull up:
disable shared memory with host BIOS
Ext 10K up:
enable shared memory with host BIOS

PPEN
No pull up:
Normal
Ext 10K up:
KBS interface pins are switched to parallel port interface for in-system programming.

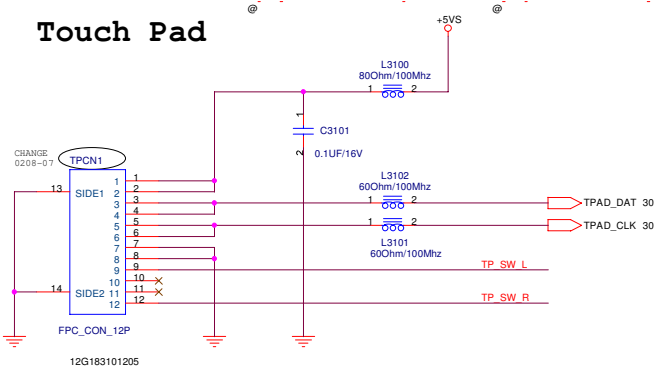




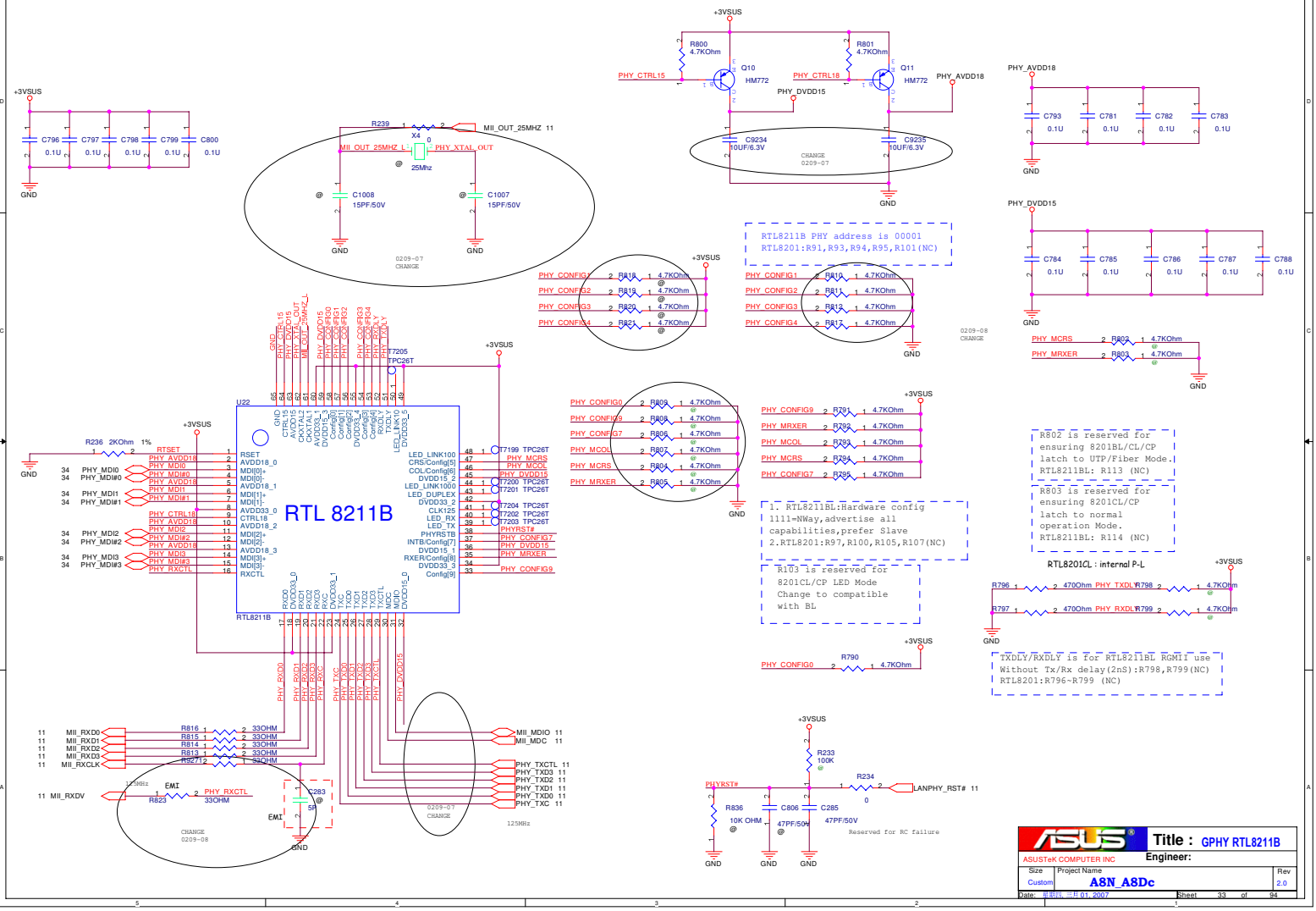
8M TSOP



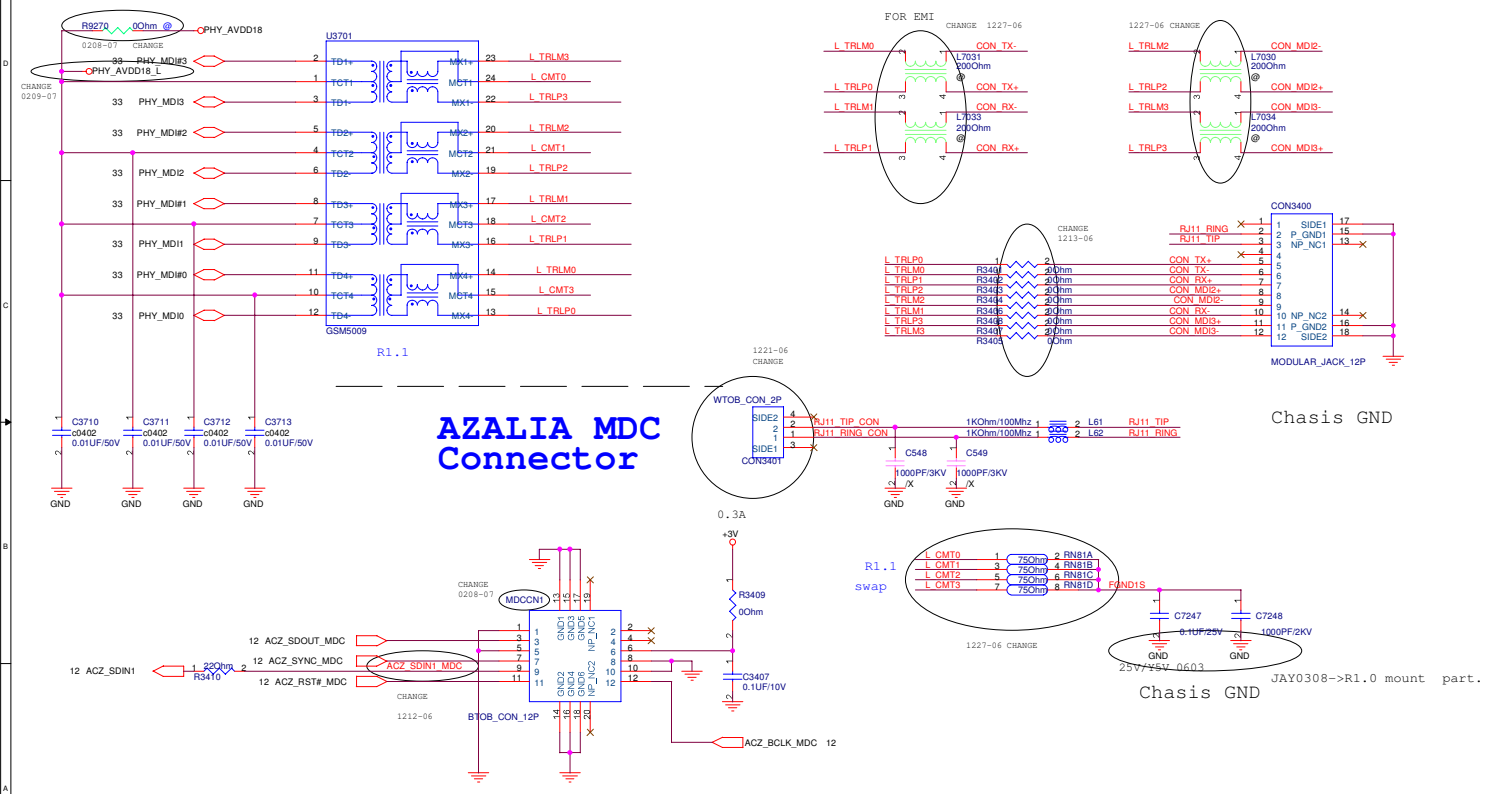
Touch Pad



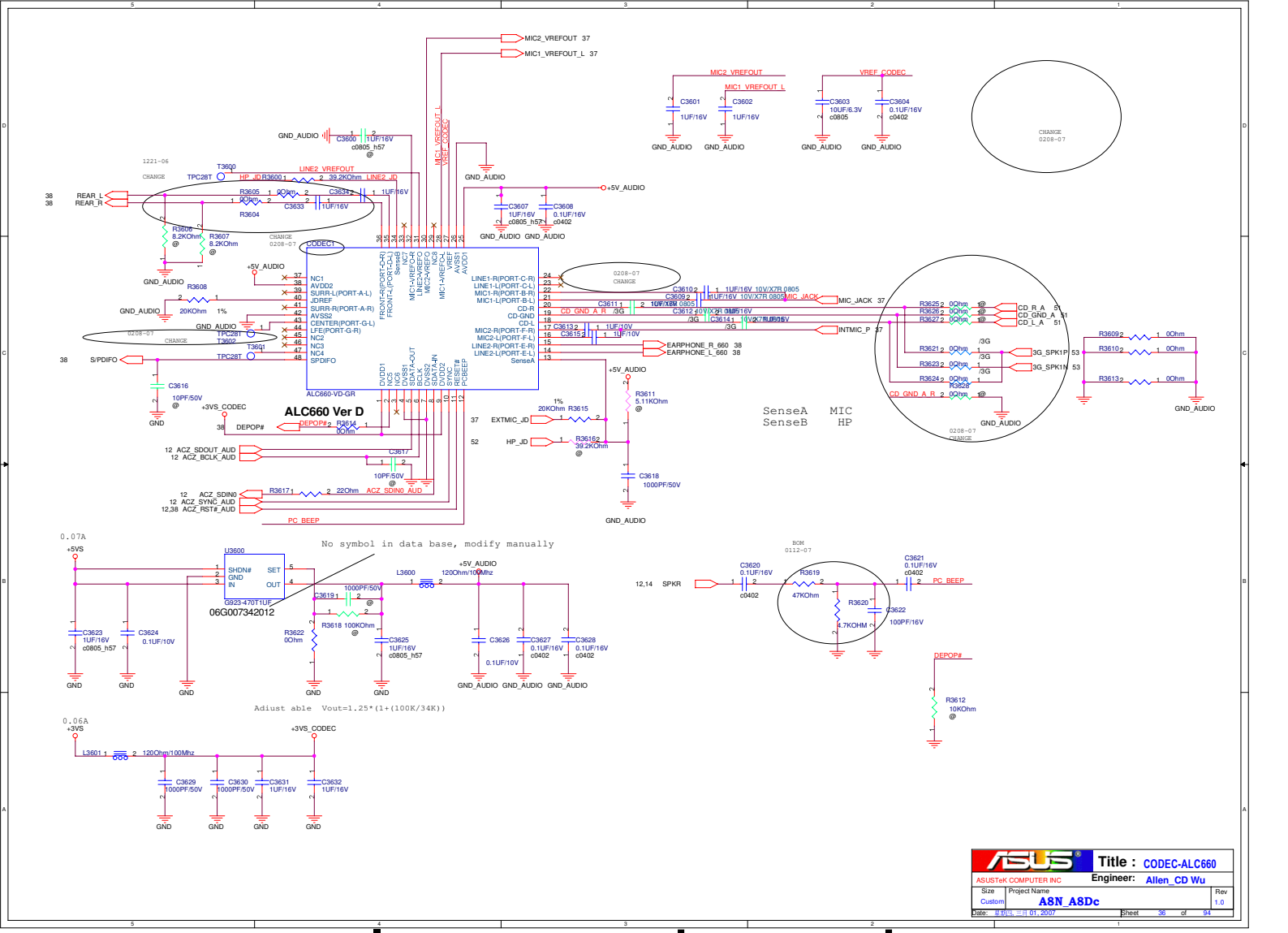
ASUSTeK COMPUTER INC	Title : IT8510/8511(2/2)	
	Engineer: Allen_CD Wu	
Size: Custom	Project Name: A8N_A8Dc	Rev: 1.0
Date: 星期四, 三月 01, 2007	Sheet 31 of 94	

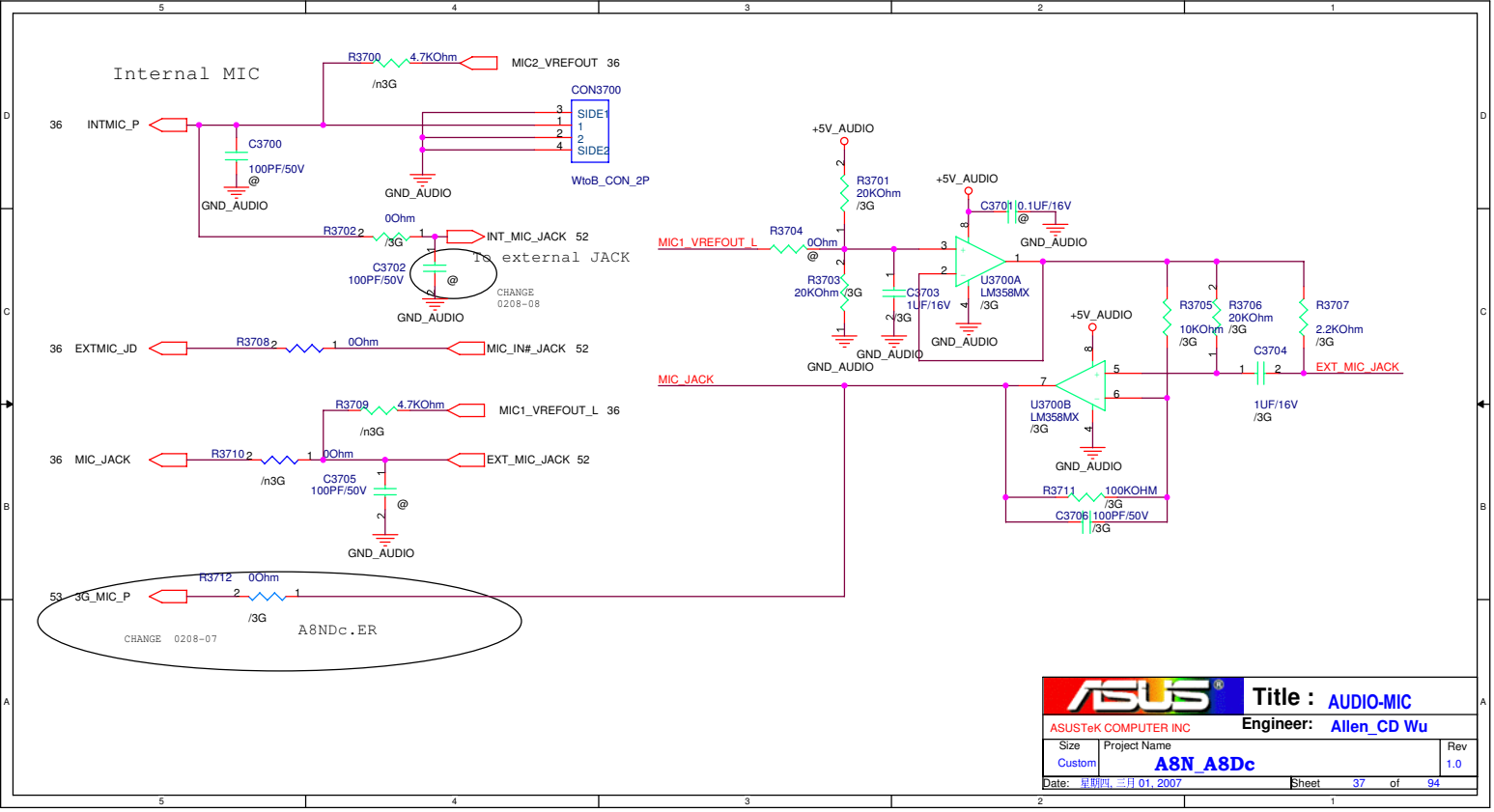


LAN PORT

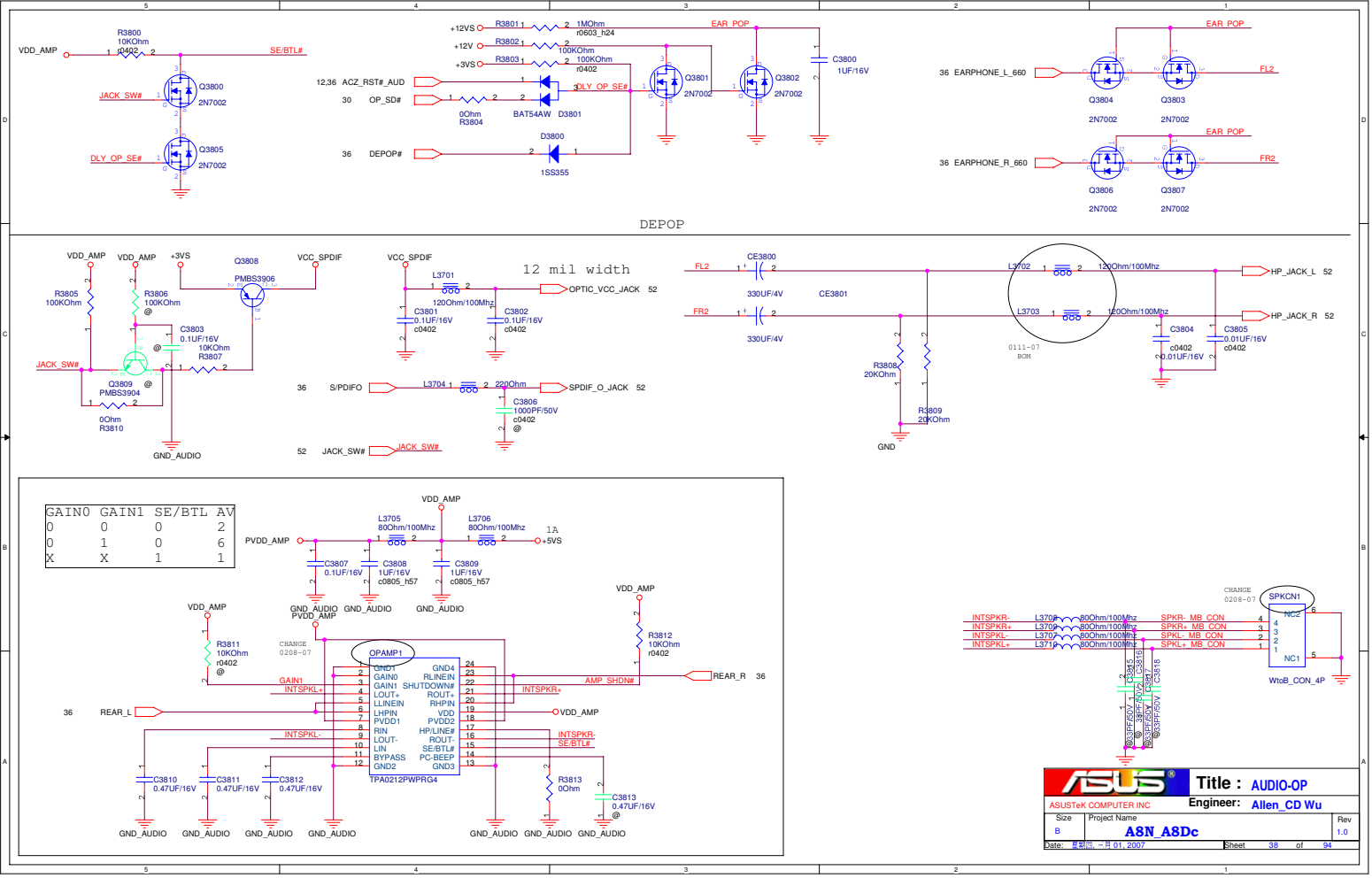


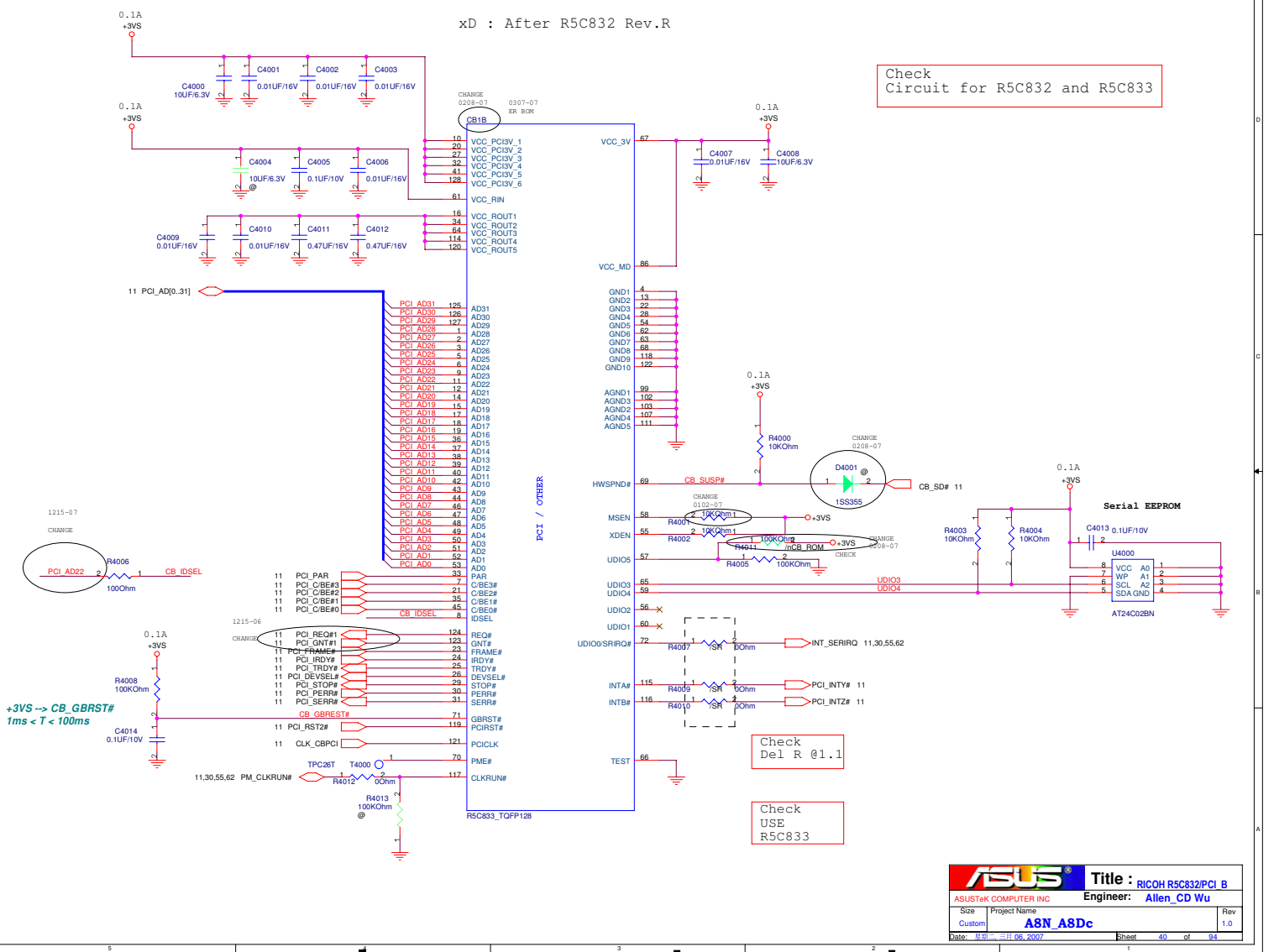
ASUSTeK COMPUTER INC	Title : RJ11+45 , MDC		
	Engineer: Allen_CD Wu		
Size: B	Project Name: A8N_A8Dc		Rev: 1.0
Date: 星期四, 一月 01, 2007	Sheet 34 of 94		

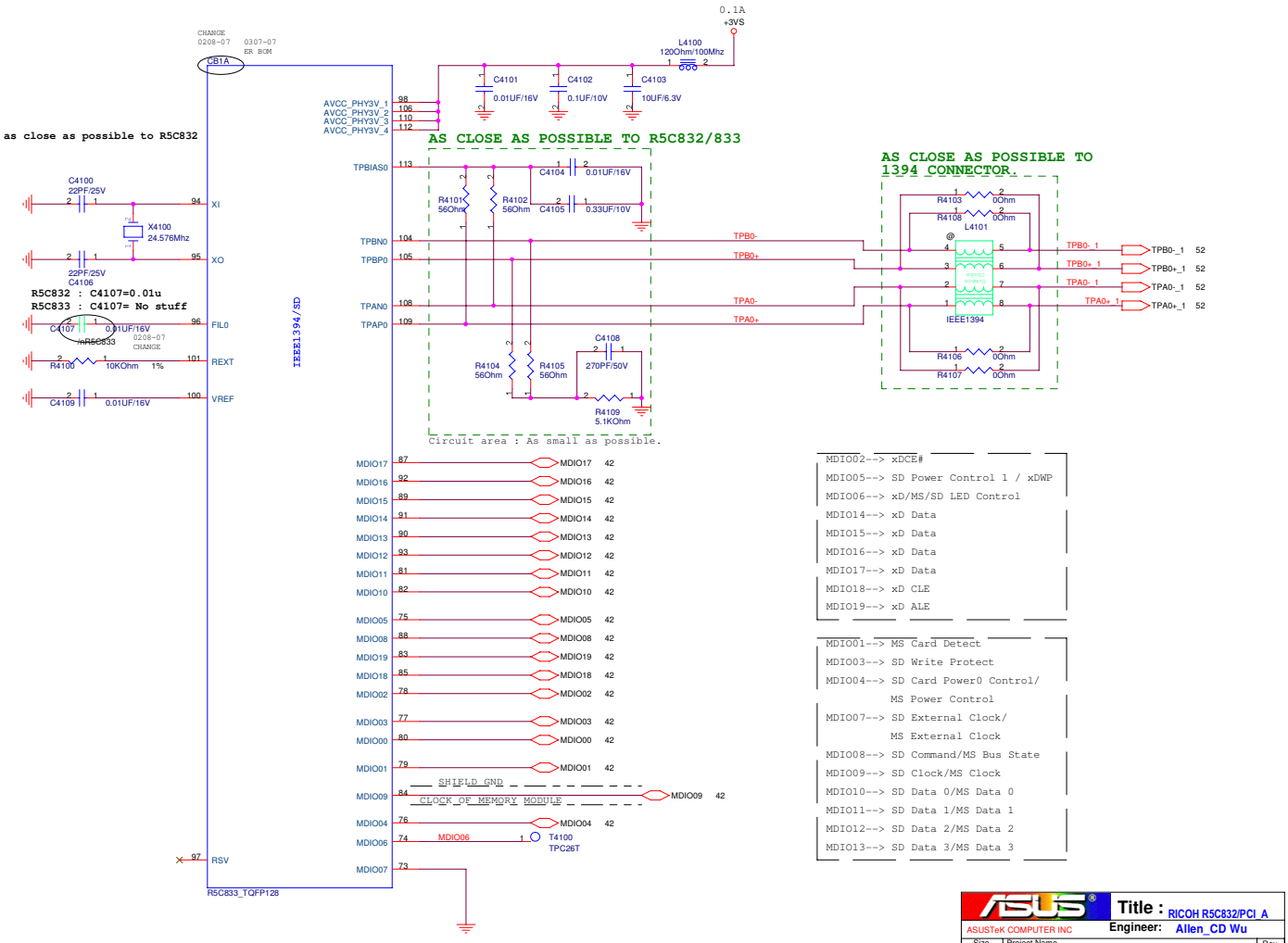


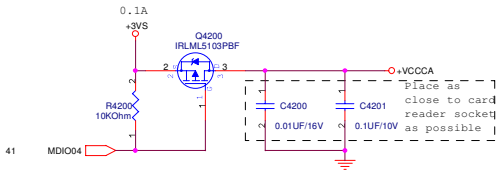


ASUSTeK COMPUTER INC	Title : AUDIO-MIC	
	Engineer: Allen_CD Wu	
Size: Custom	Project Name: A8N_A8Dc	Rev: 1.0
Date: 星期四, 三月 01, 2007	Sheet 37 of 94	

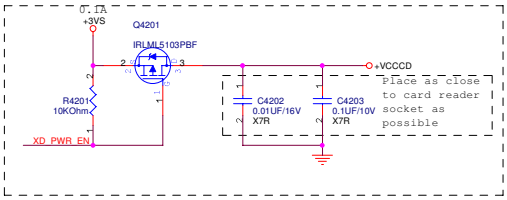




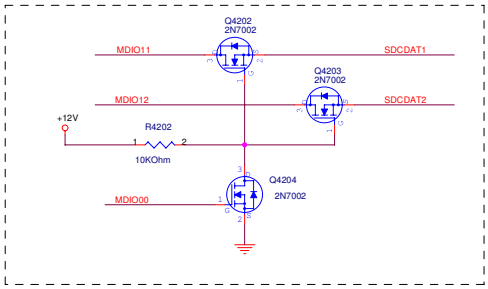




To correct the problem when MS Duo adaptor is in use.



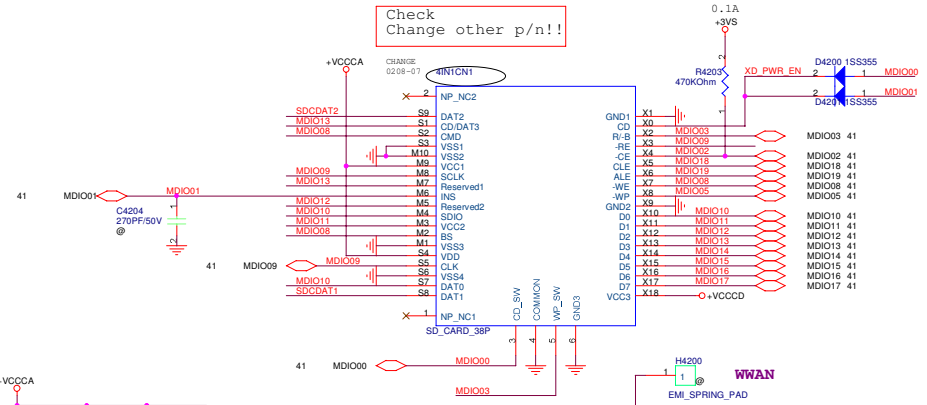
Solve MS Duo Adaptor short issue.

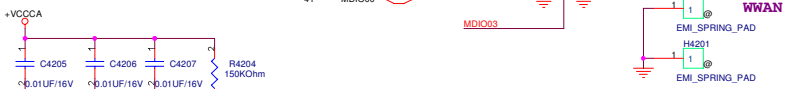


MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

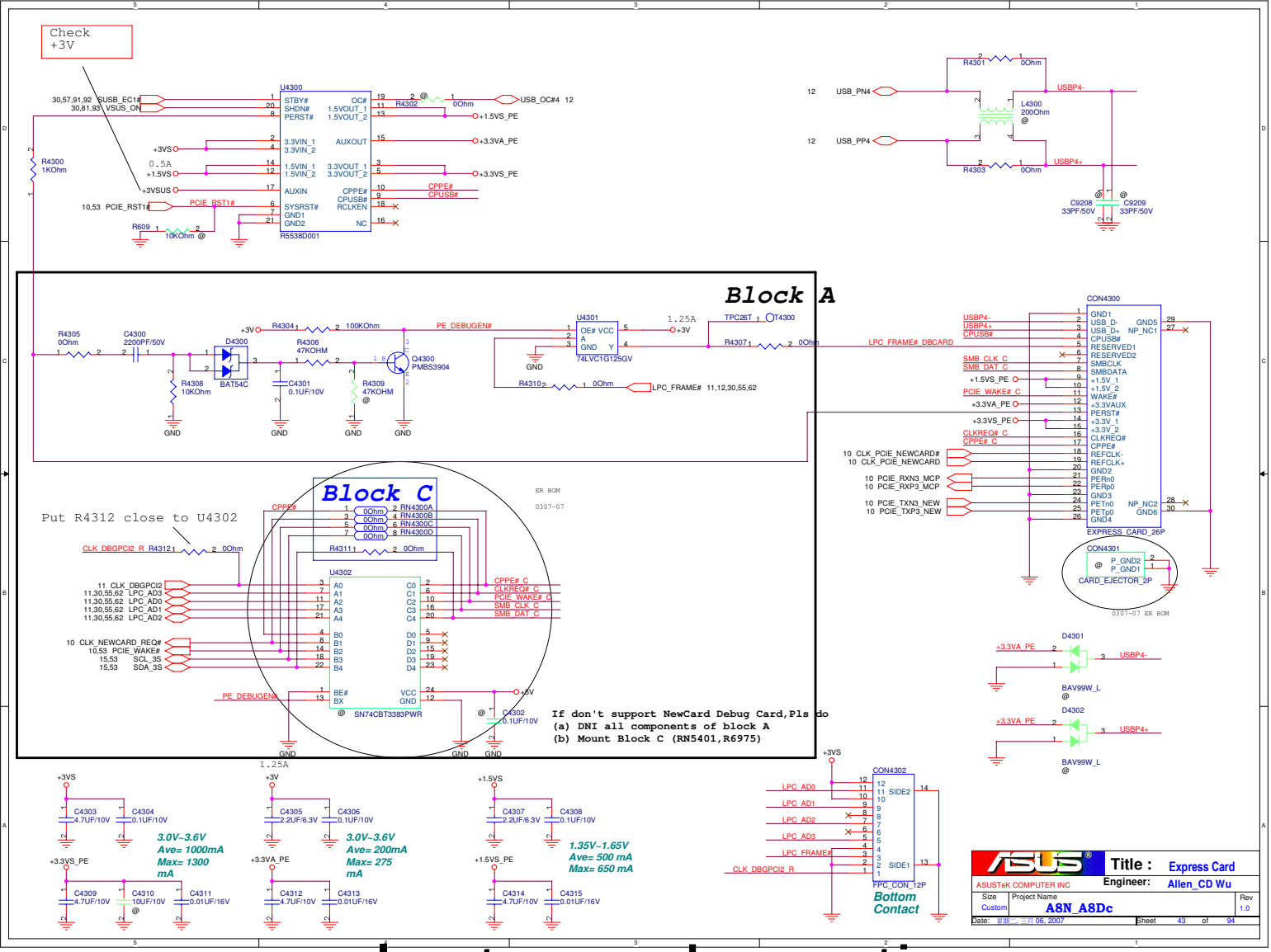
MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

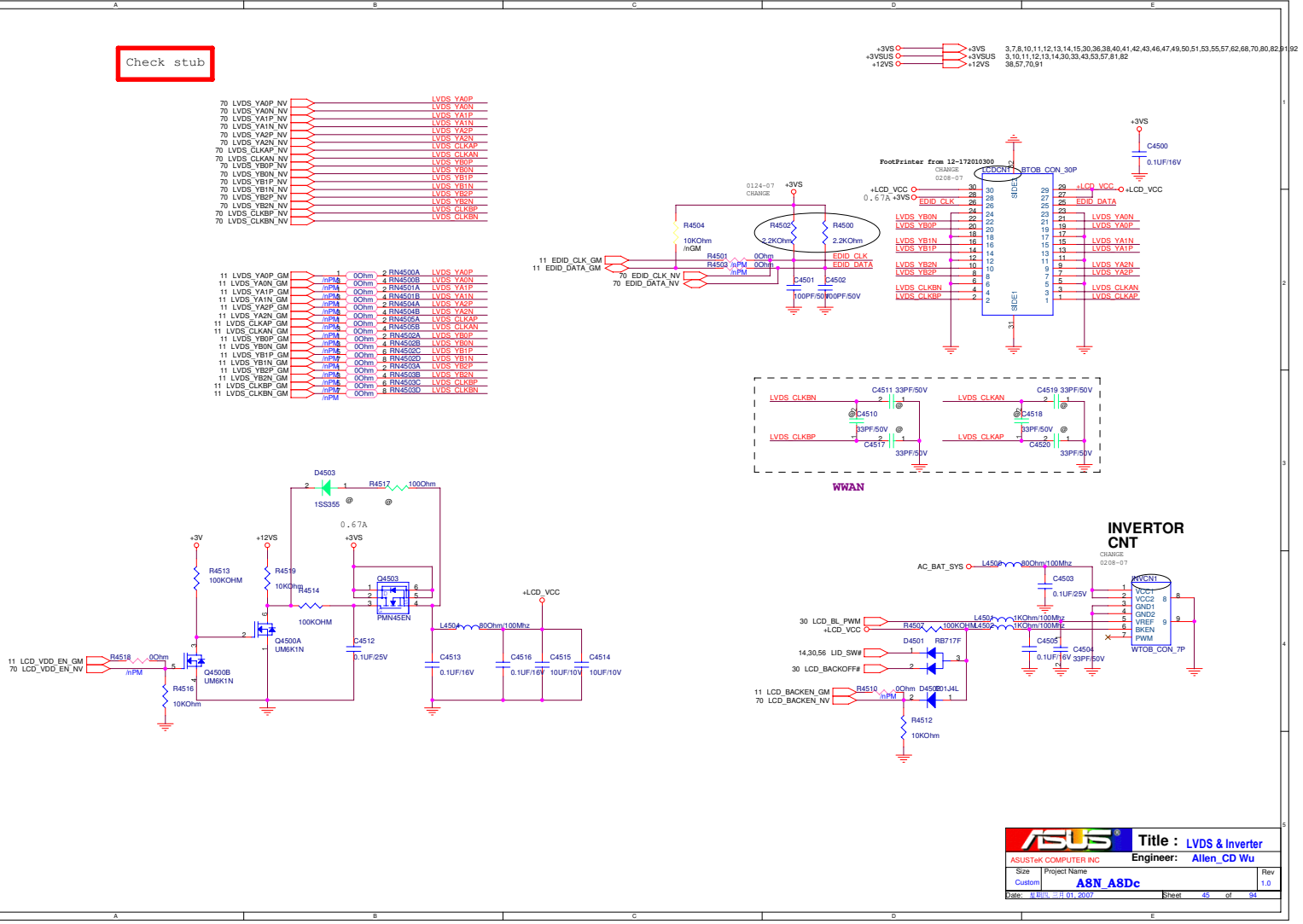
Check
Change other p/n!!

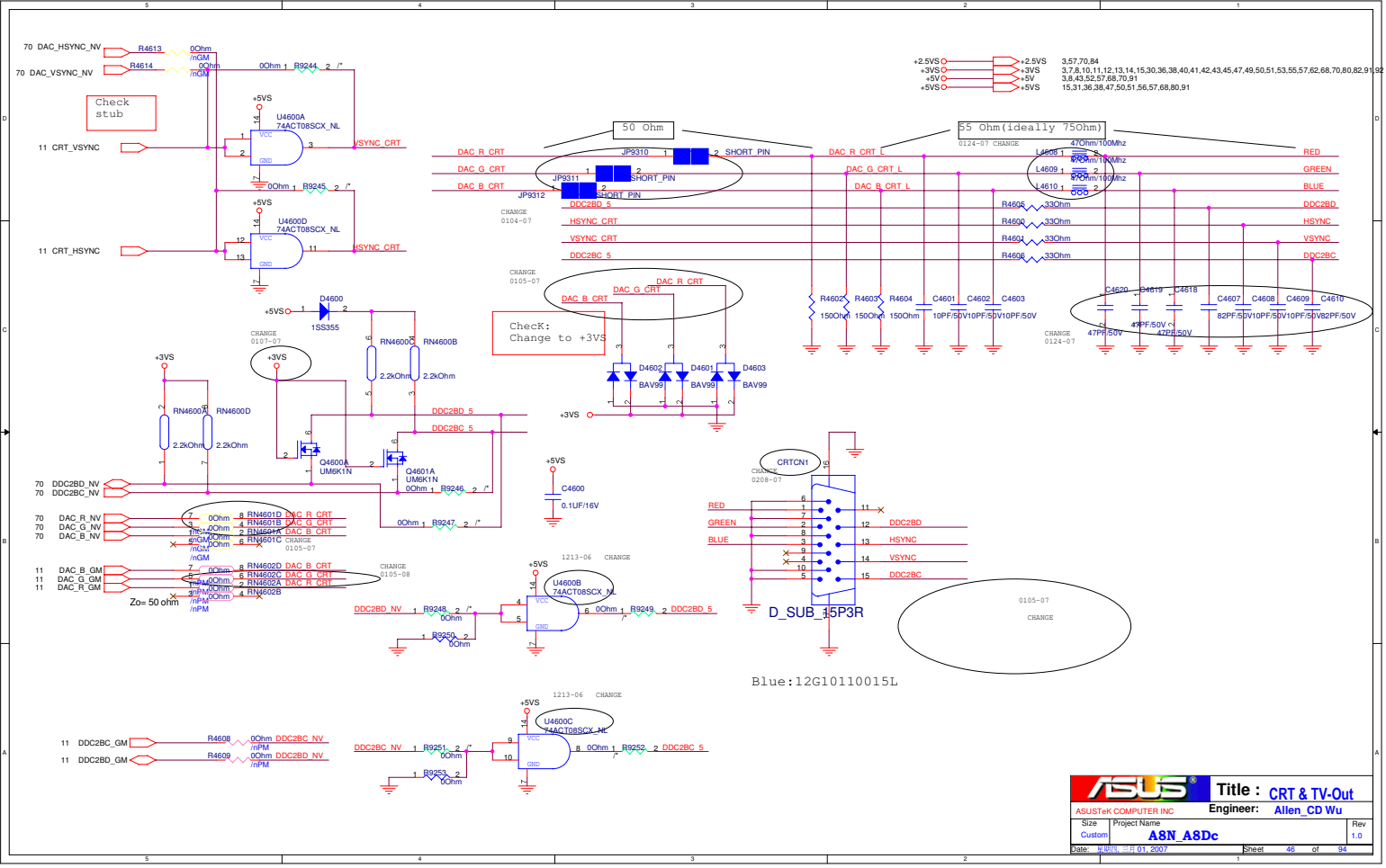


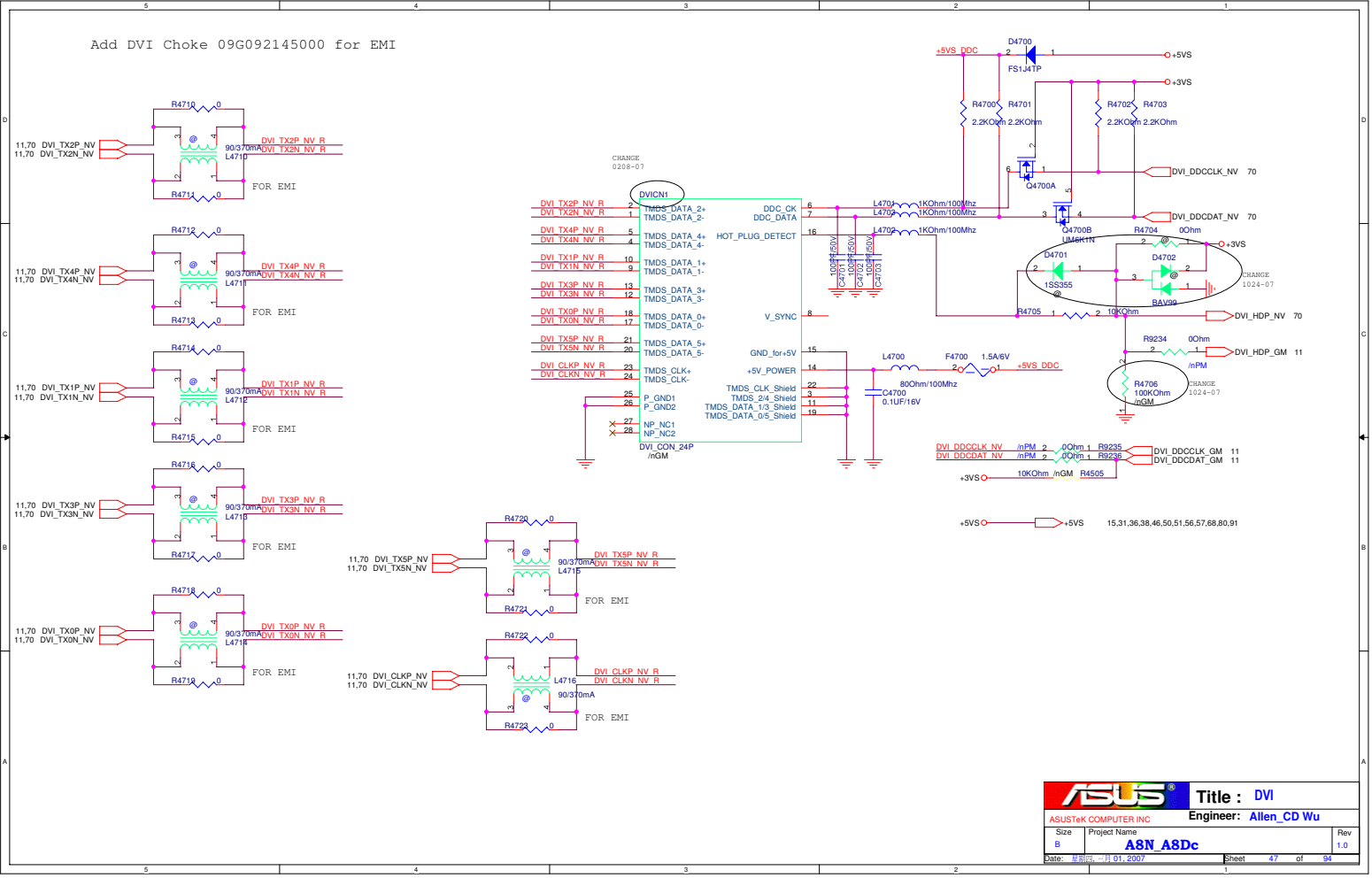


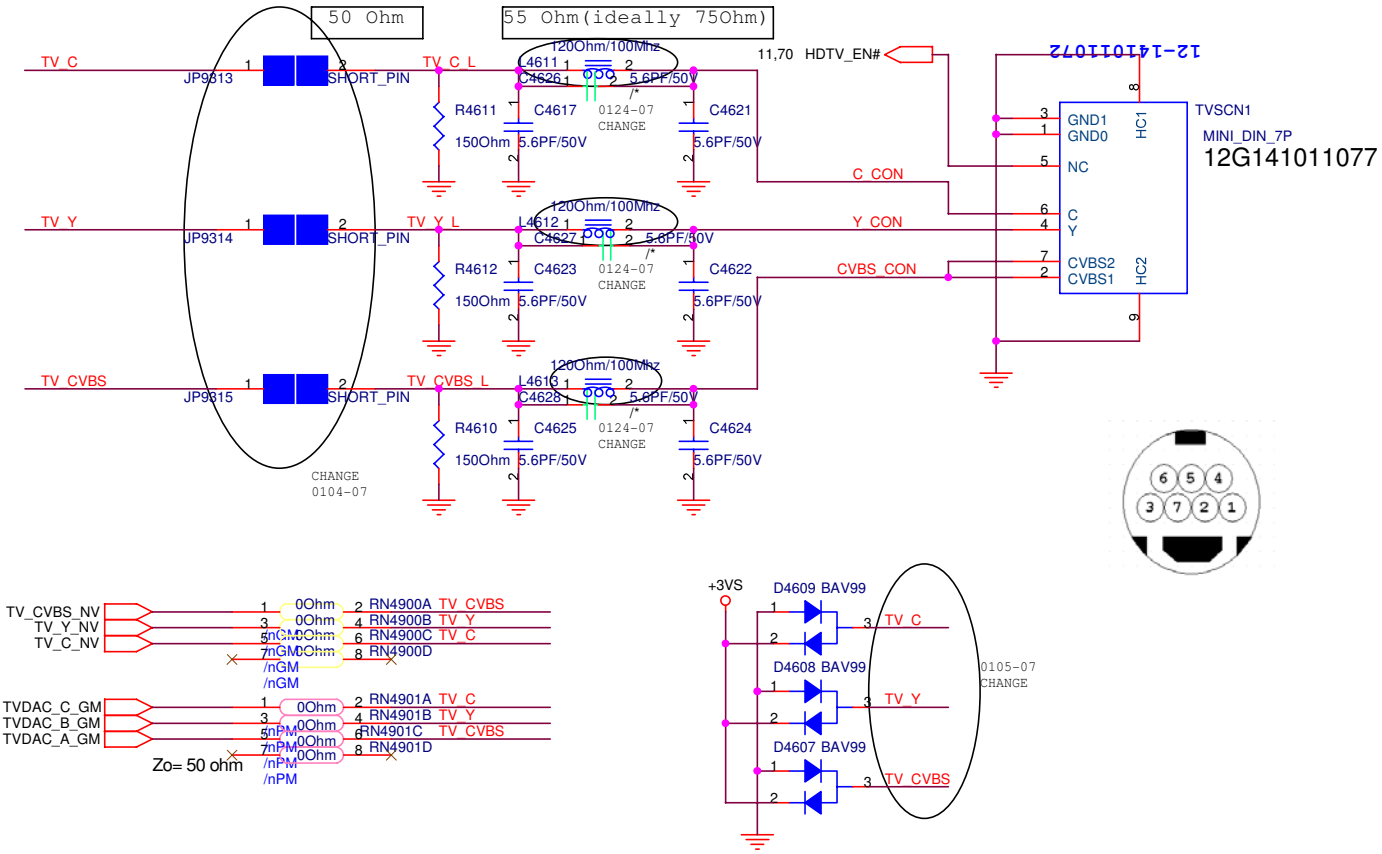
ASUSTeK COMPUTER INC	Title : CardReader	
	Engineer: Allen_CD Wu	
Size: Custom	Project Name: A8N_A8Dc	Rev: 1.0
Date: 星期四, 二月 01, 2007	Sheet 42 of 94	





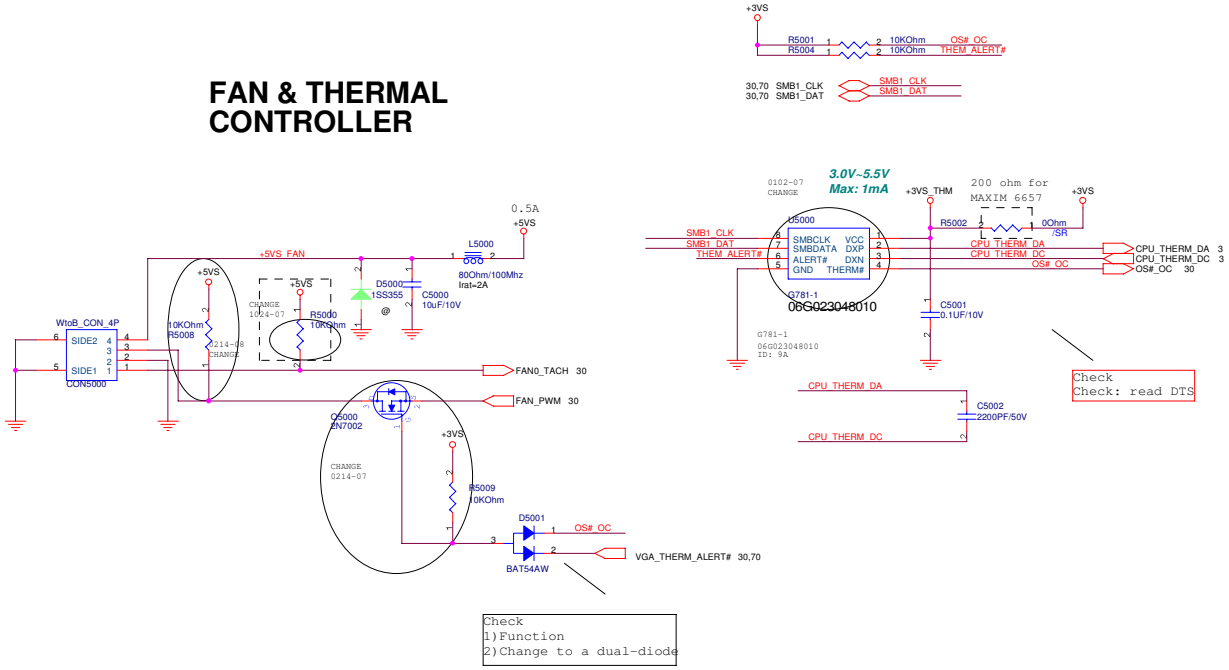




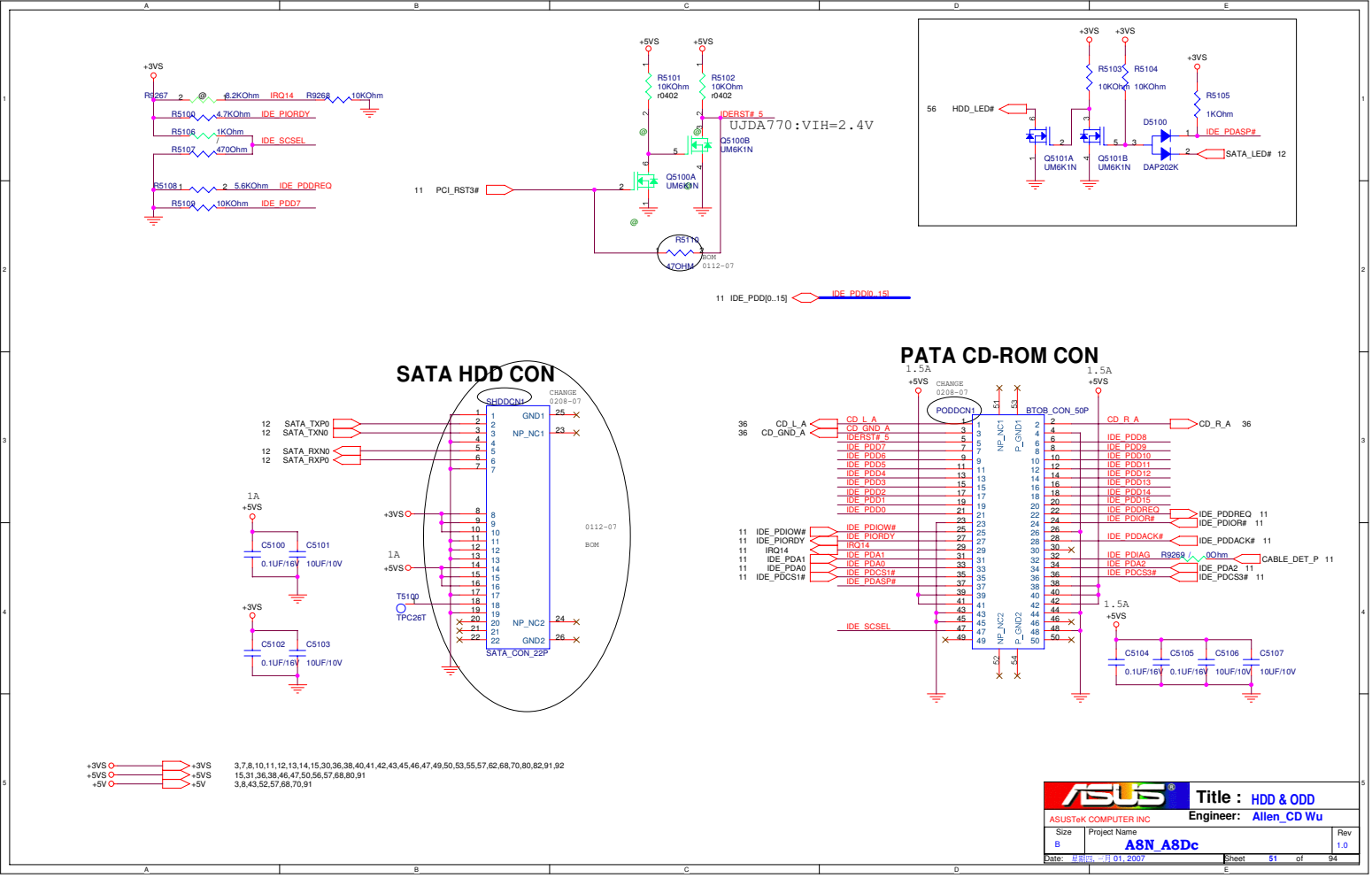


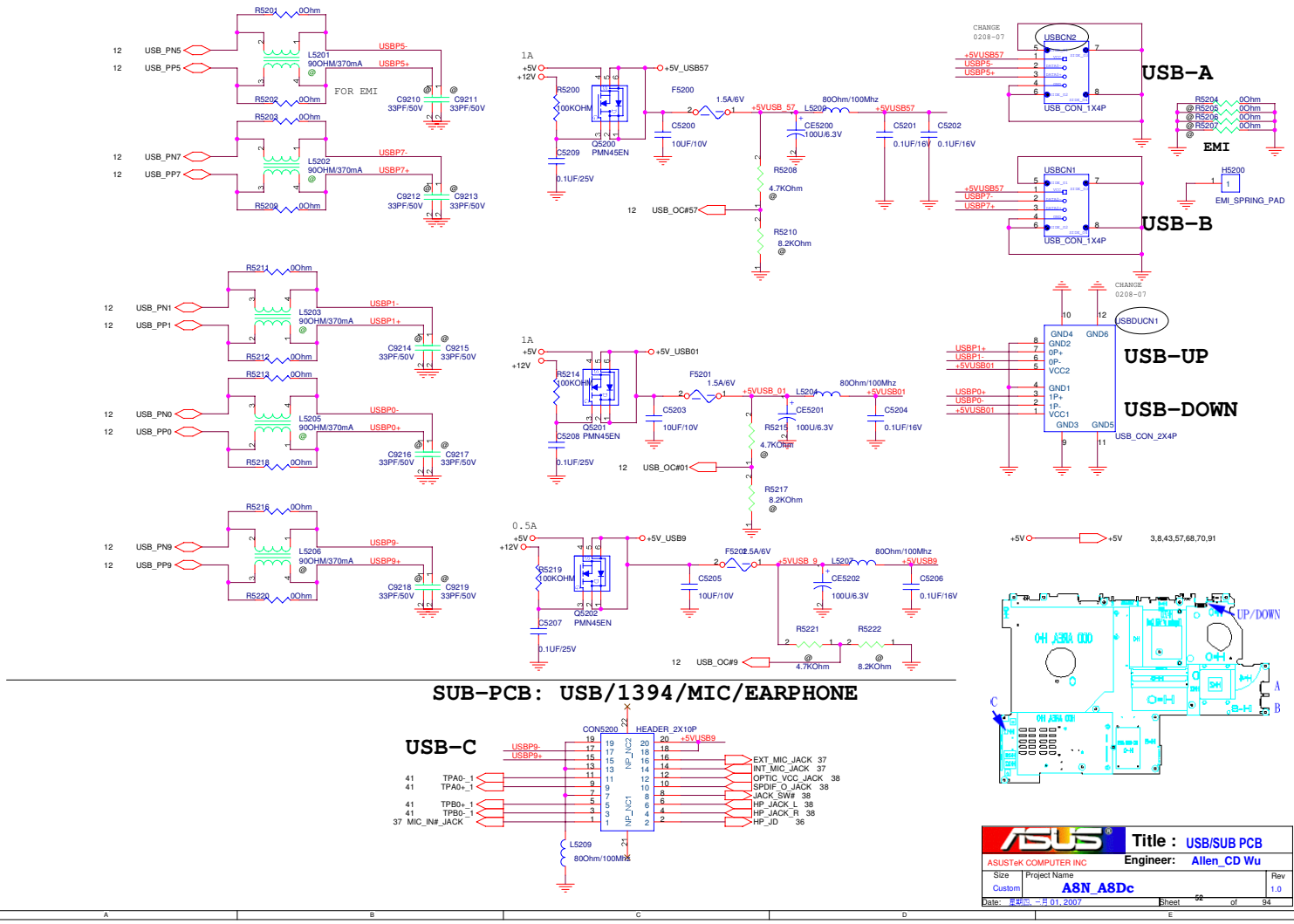
ASUSTeK COMPUTER INC	Title : TV	
	Engineer: Allen_CD Wu	
Size: A	Project Name: A8N_A8Dc	Rev: 1.0
Date: 星期四, 三月 01, 2007	Sheet 49 of 94	

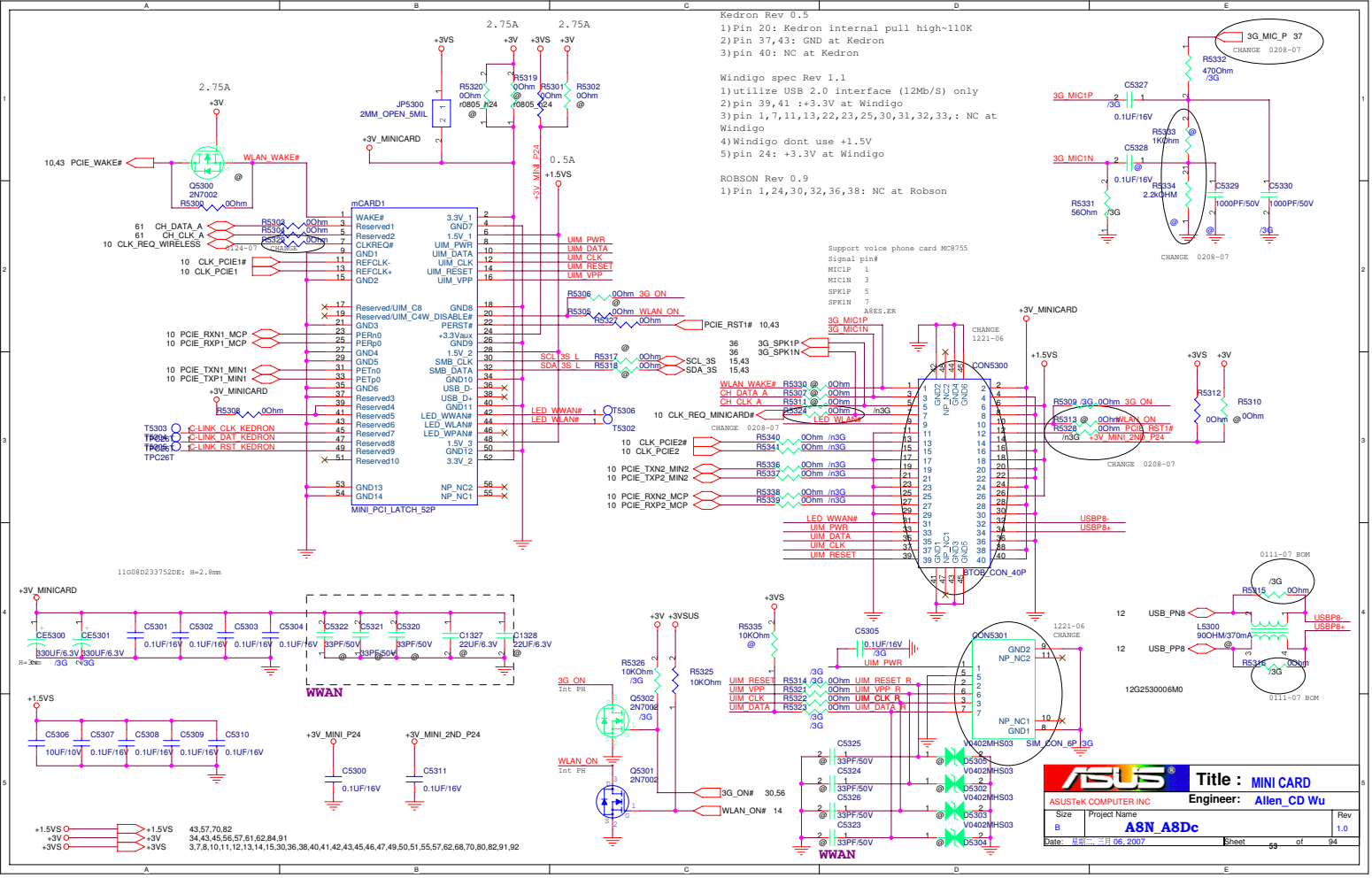
FAN & THERMAL CONTROLLER

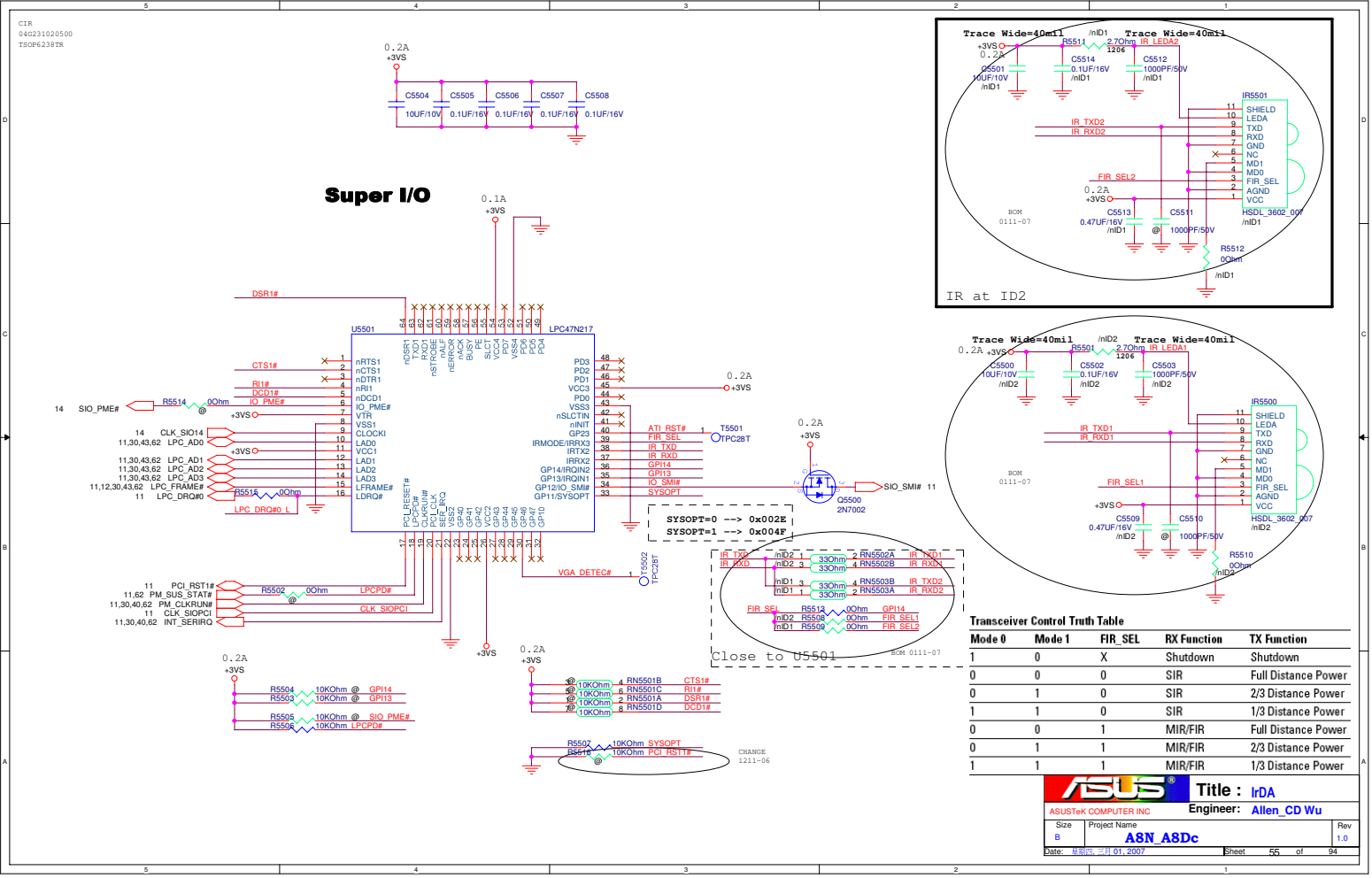


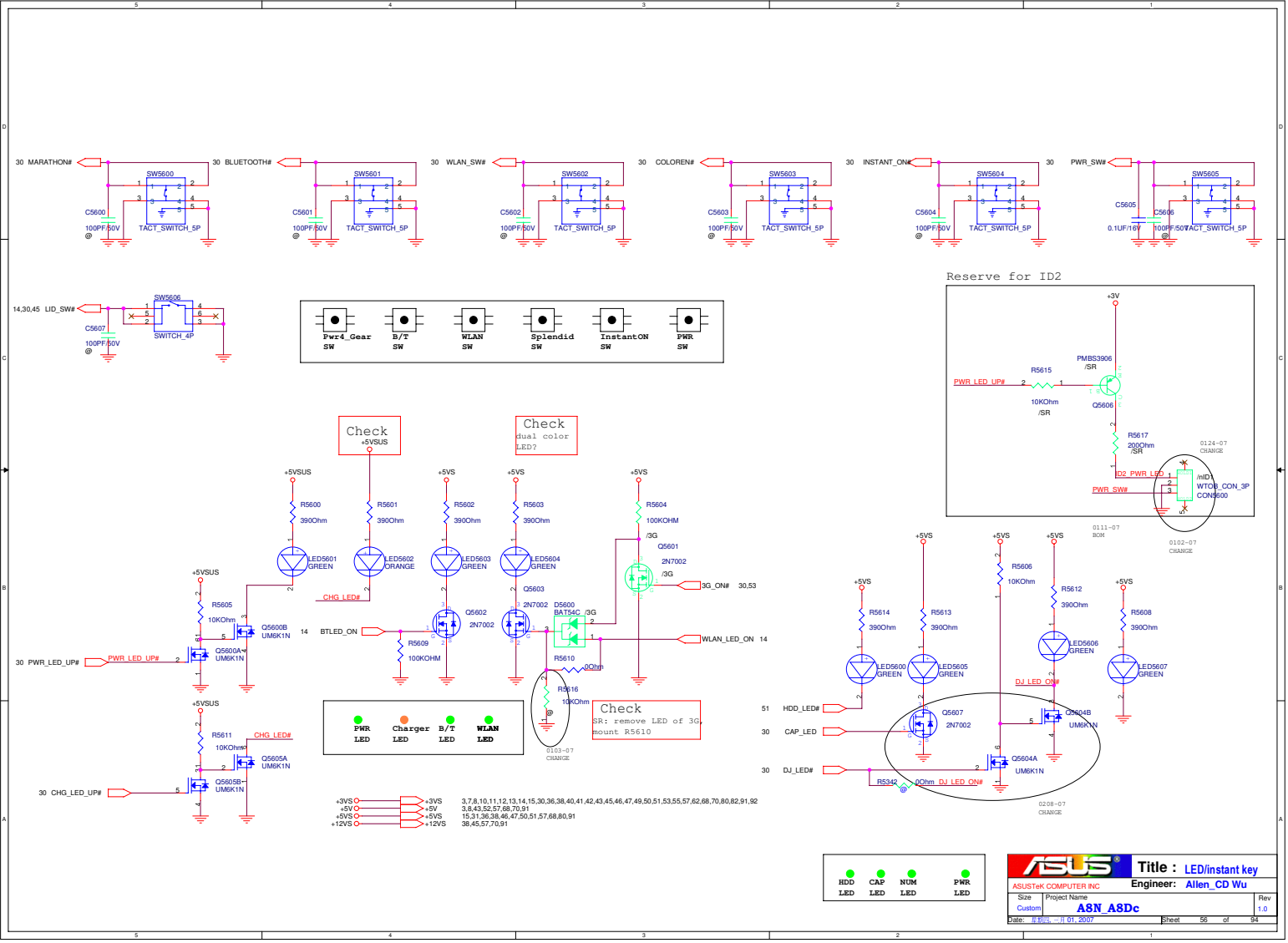
ASUSTeK COMPUTER INC	Title : FAN & THERMAL	
	Engineer: Allen_CD Wu	
Size: B	Project Name: A8N_A8Dc	Rev: 1.0
Date: 星期四, 一月 01, 2007	Sheet 50 of 94	

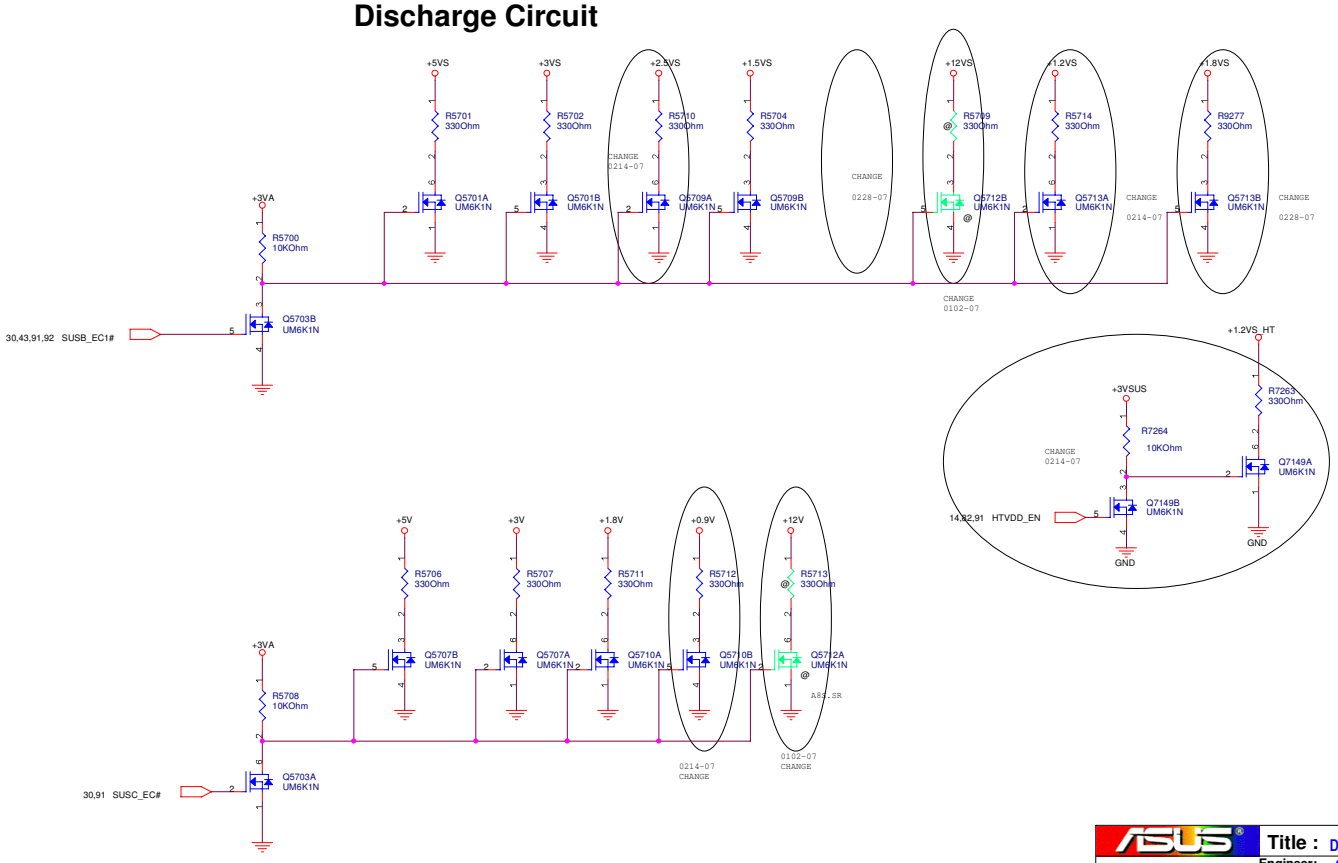


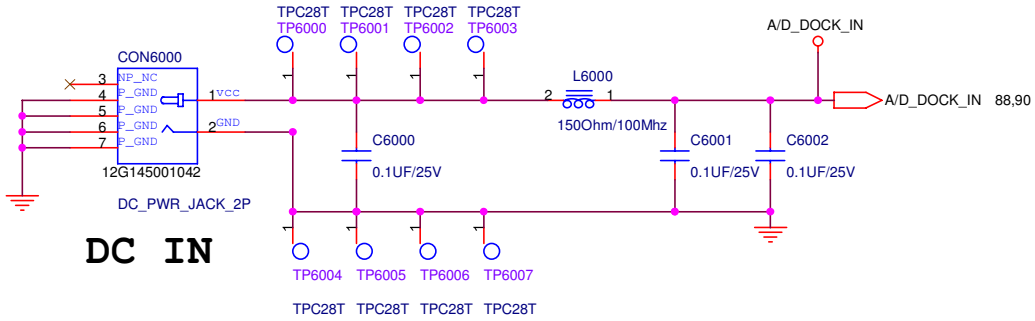




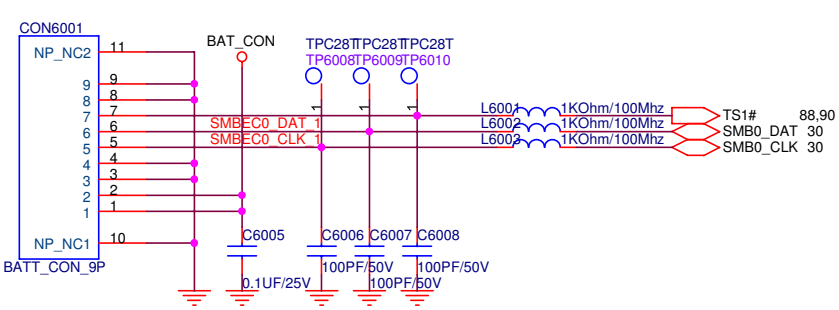


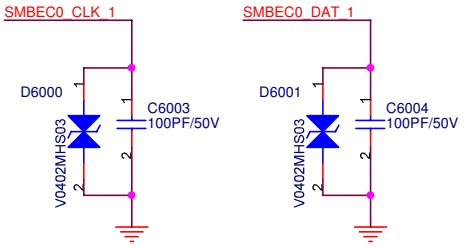






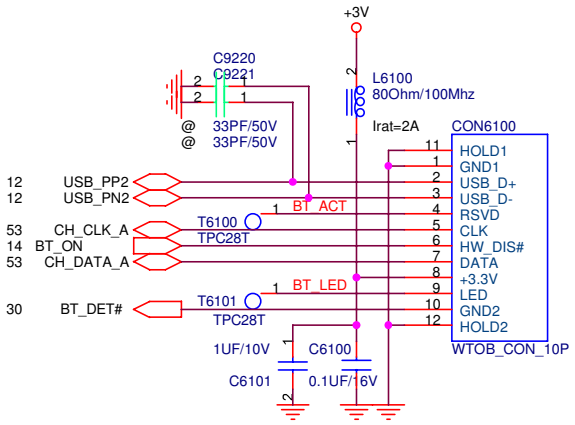
DC IN





Battery Connector

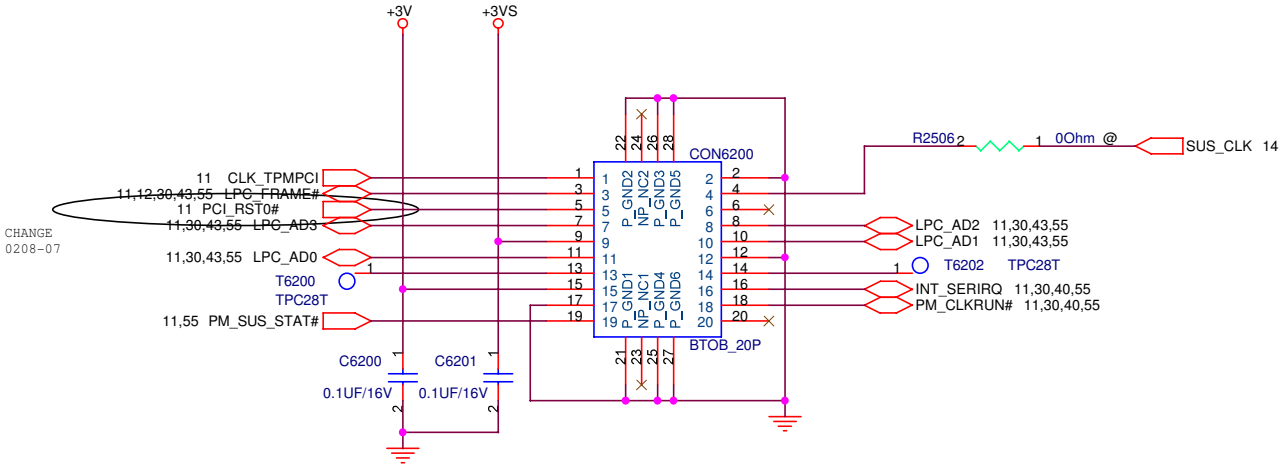
ASUSTeK COMPUTER INC	Title : DC IN / BAT	
	Engineer: Allen_CD Wu	
Size: A	Project Name: A8N_A8Dc	Rev: 1.0
Date: 星期四, 三月 01, 2007	Sheet 60 of 94	



Bluetooth Module CON

ASUSTeK COMPUTER INC	Title : BT/CAMERA	
	Engineer: Allen_CD Wu	
Size: A	Project Name: A8N_A8Dc	Rev: 1.0
Date: 星期四, 三月 01, 2007	Sheet 61 of 94	

TPM 1.2 Module



ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: Allen_CD Wu	
Size: A	Project Name: A8N_A8Dc	Rev: 1.0
Date: 星期四, 三月 01, 2007	Sheet 62 of 94	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARDBUS	AD22	1	Y, Z

CHANGE 1215-06

SM-Bus Device	SM-Bus Address
SO-DIMM 0 (low)	
SPD	A0
SO-DIMM 1(high)	
SPD	A4
G781-1	9A
G781(VGA board)	98

CHANGE 0102-07

Thermal Sensor (CPU)

SM-Bus Mapping 1001100

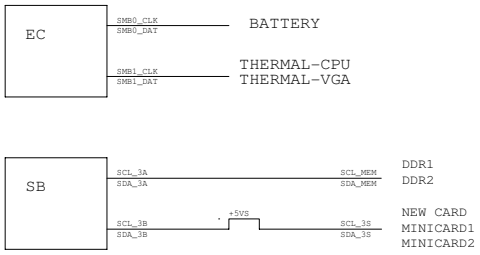
BOM option

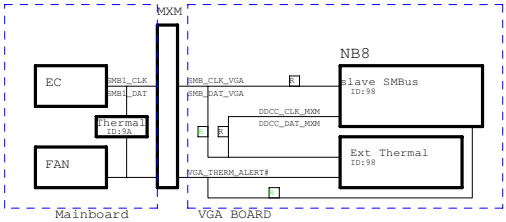
nGM:yellow
nPM:light red
==========
nGM :no stuff for A8N
nPM :no stuff for A8Dc
nGM1:no stuff for A8N, A8N/SR mount for debuging A8S in advance
3G :for Windigo, SR mount for debuging
SR :for SR debuging, should be removed or no stuff @ ER

Support ID2:

Support ID2:
page 68,Finger print
page 55,IR
Page 56,pwr switch and LED

Thermal block diagram





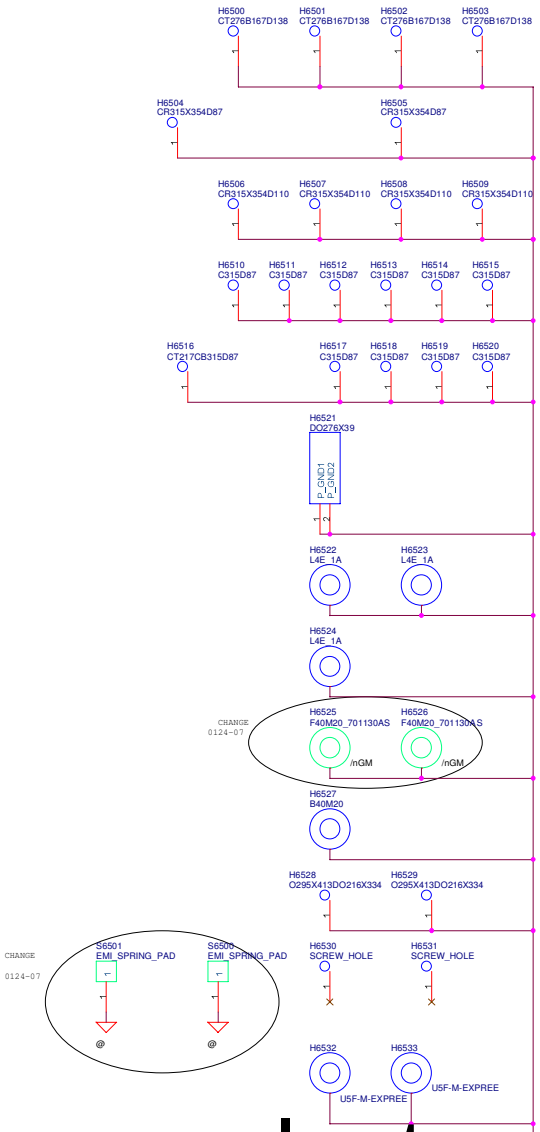
ASUSTeK COMPUTER INC

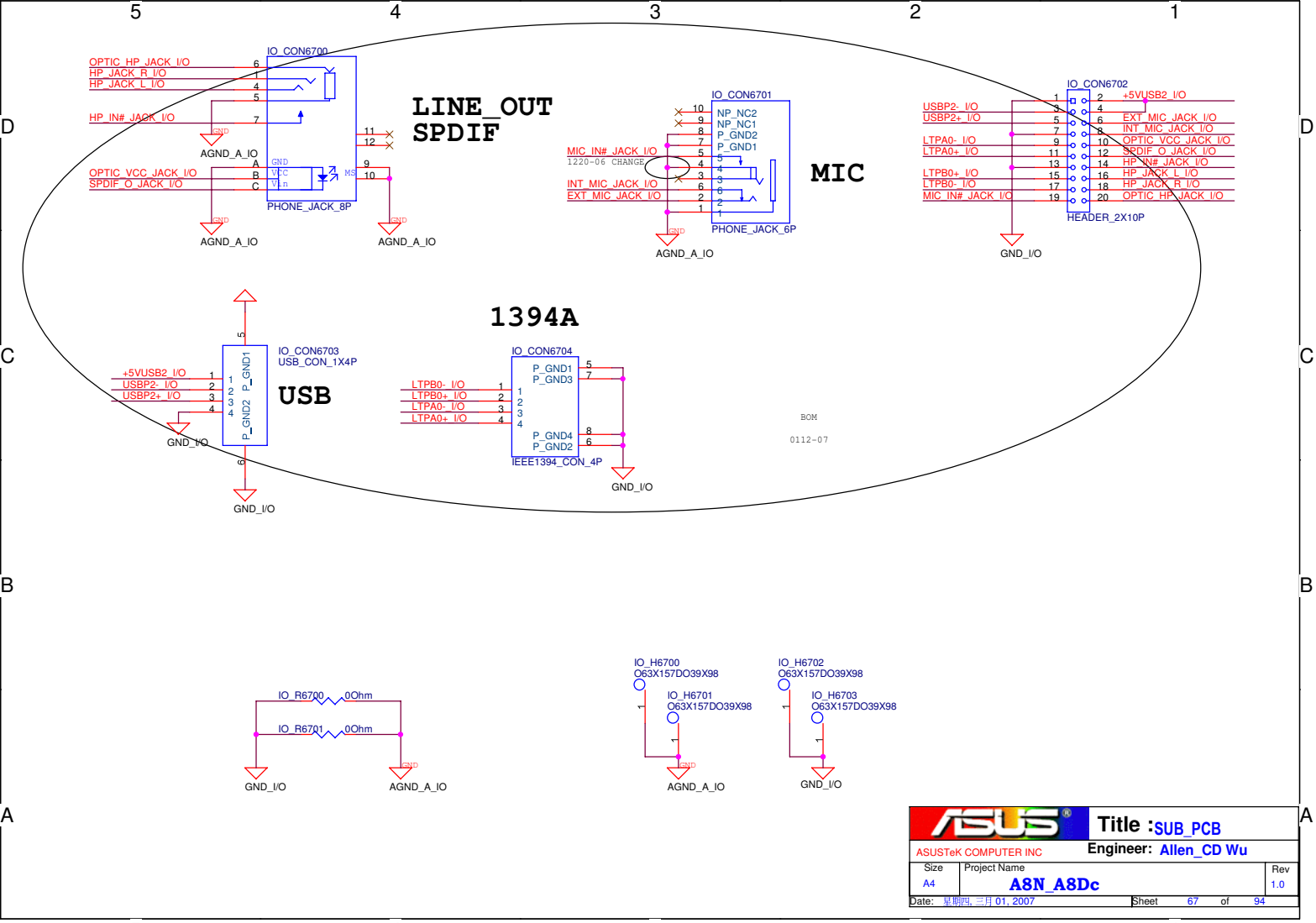
Title :

Engineer: Allen_CD Wu

Size	Project Name	Rev
B	A8N_A8Dc	1.0

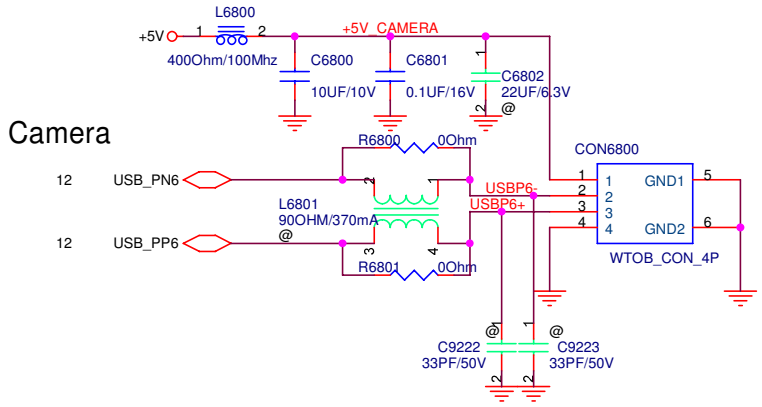
Date: 星期四, 一月 01, 2007 Sheet 64 of 94



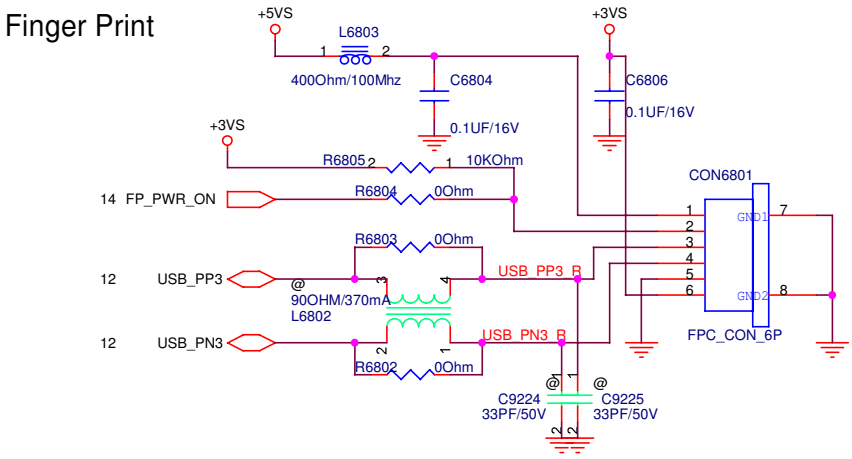


ASUSTeK COMPUTER INC	Title : SUB_PCB	
	Engineer: Allen_CD Wu	
Size: A4	Project Name: A8N_A8Dc	Rev: 1.0
Date: 星期四, 三月 01, 2007	Sheet 67 of 94	

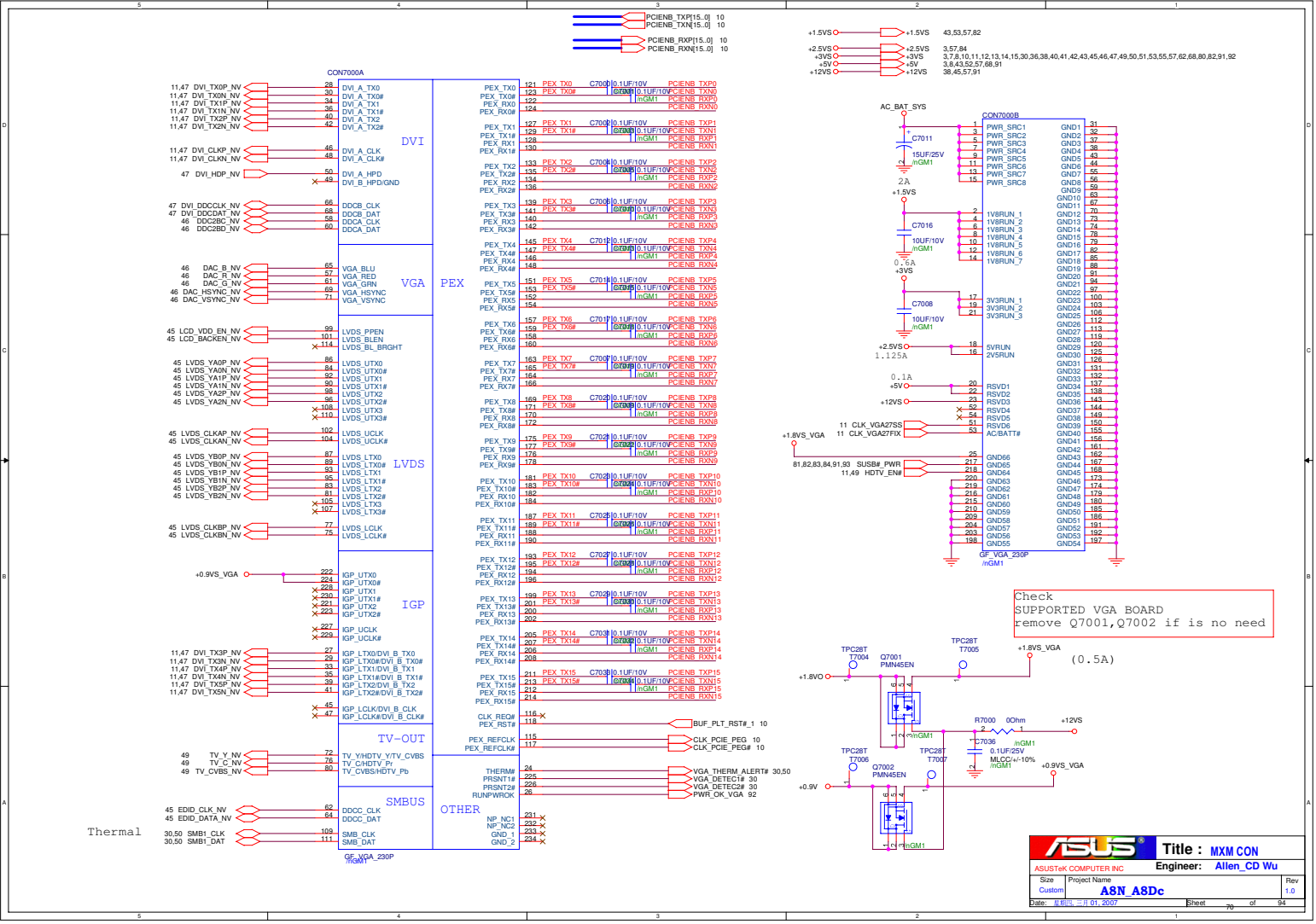
Camera



Finger Print



ASUSTeK COMPUTER INC	Title : CAMERA/FingerPrinter	
	Engineer: Allen_CD Wu	
Size: A	Project Name: A8N_A8Dc	Rev: 1.0
Date: 星期四, 三月 01, 2007	Sheet 68 of 94	



Change Note:

EE :

1. Reference name without 0 tail
2. Synchronize component size and type
3. Remove 0 ohm serial resistor
4.
5.
6.
7.
8.

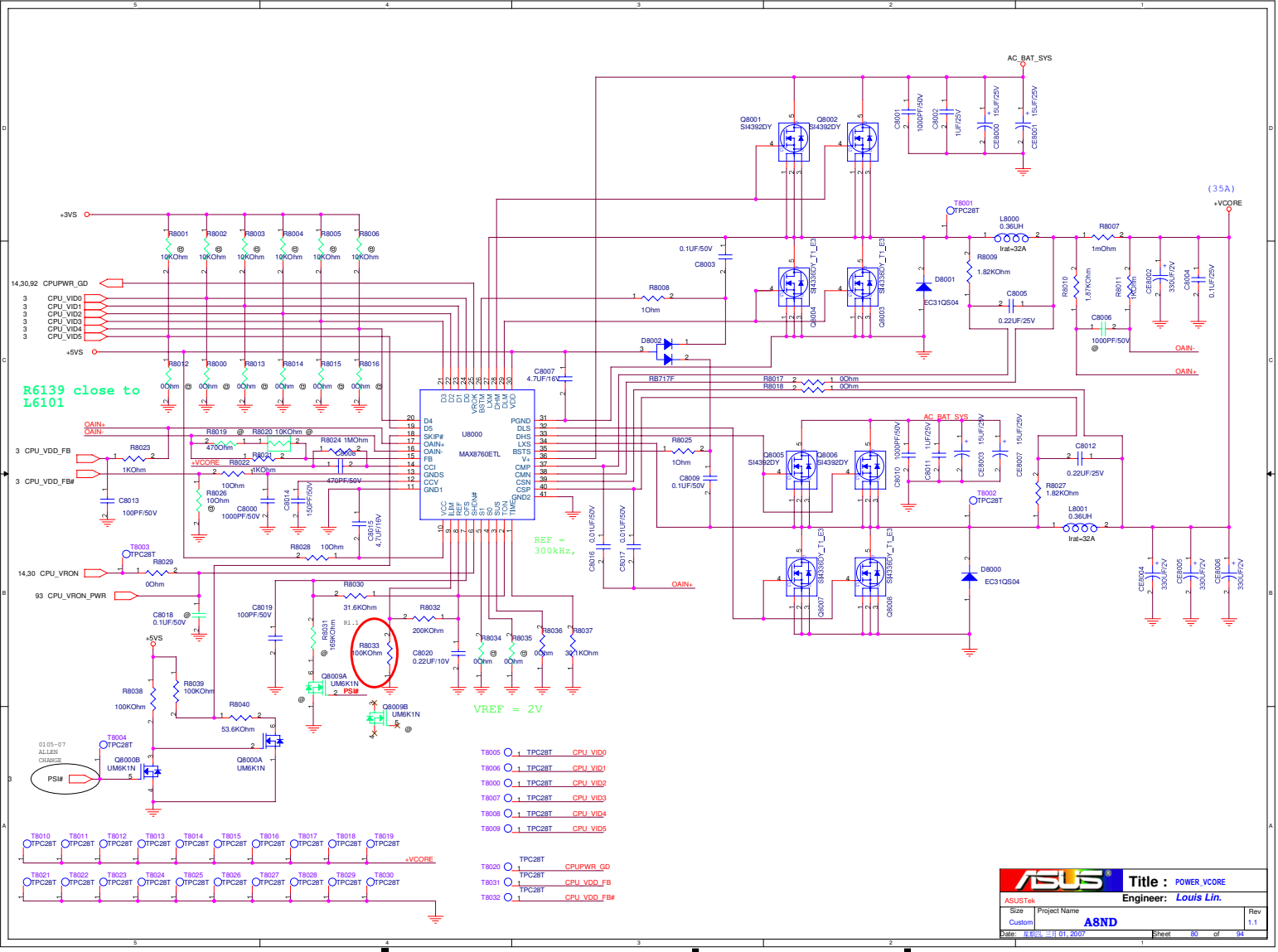
Layout :

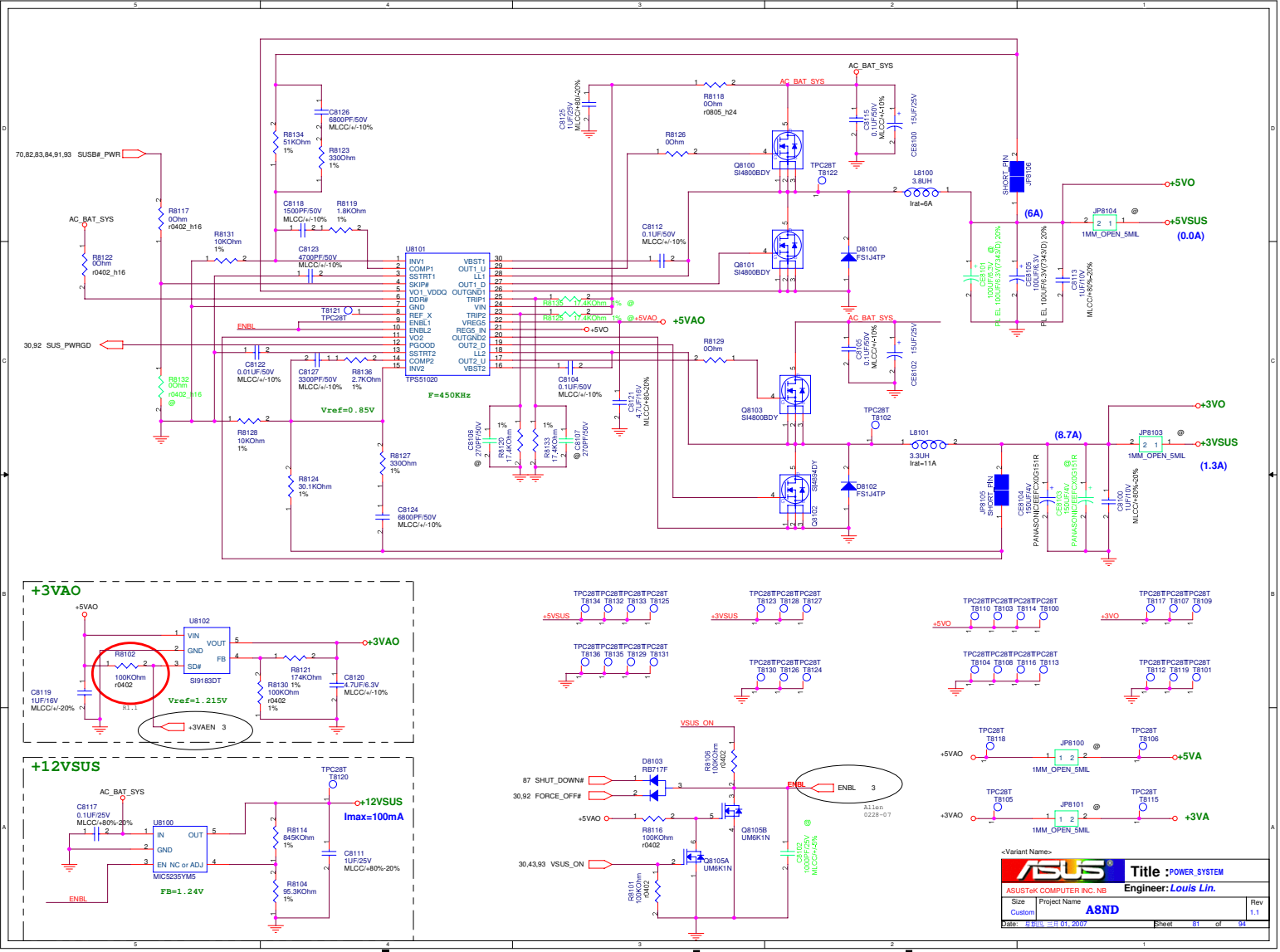
1. PCI MOAT
2. Equalize Crystal and PCI Clock Length
3. VGA Board
4. PCI-E Thread

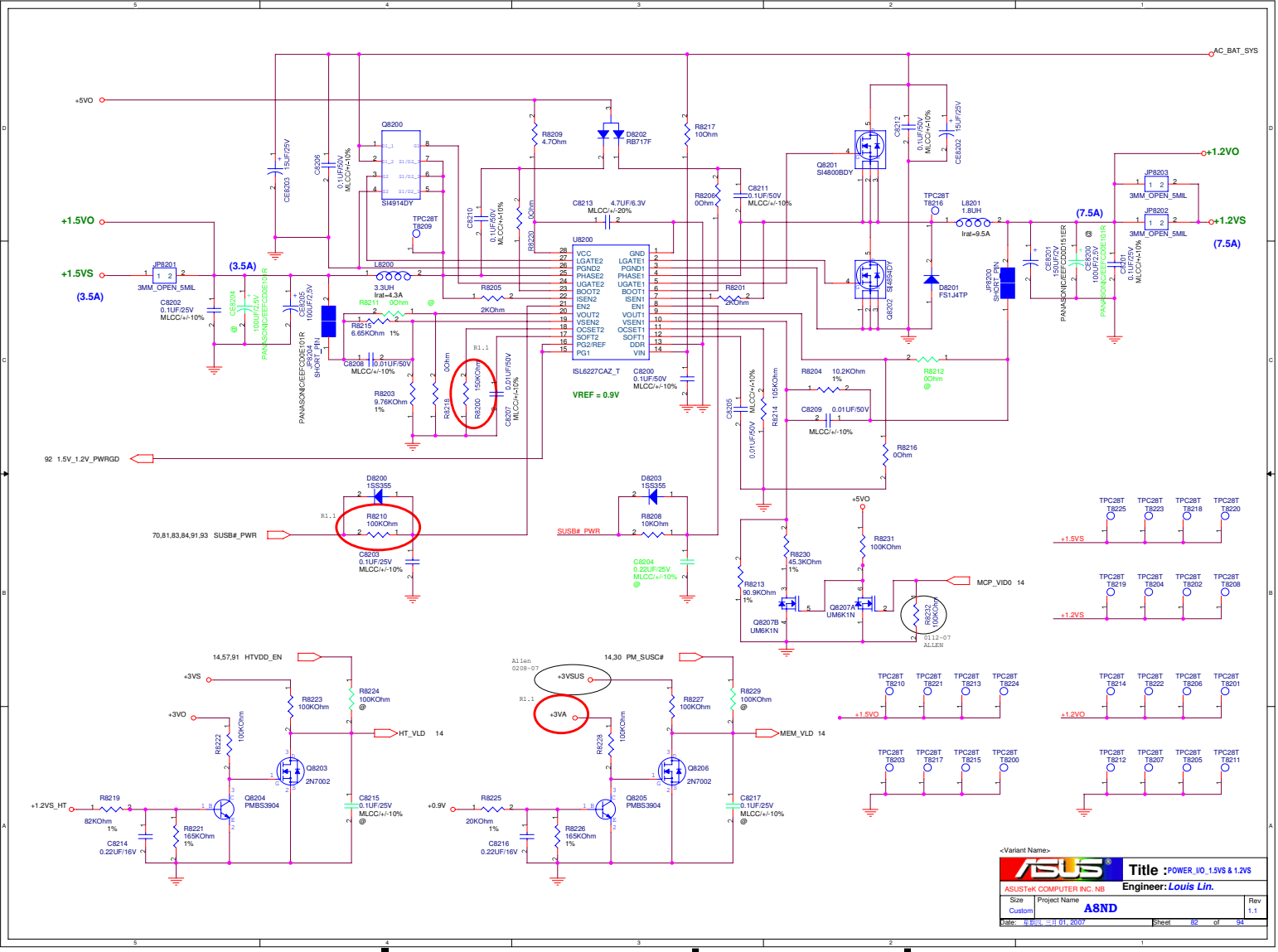
SMT :

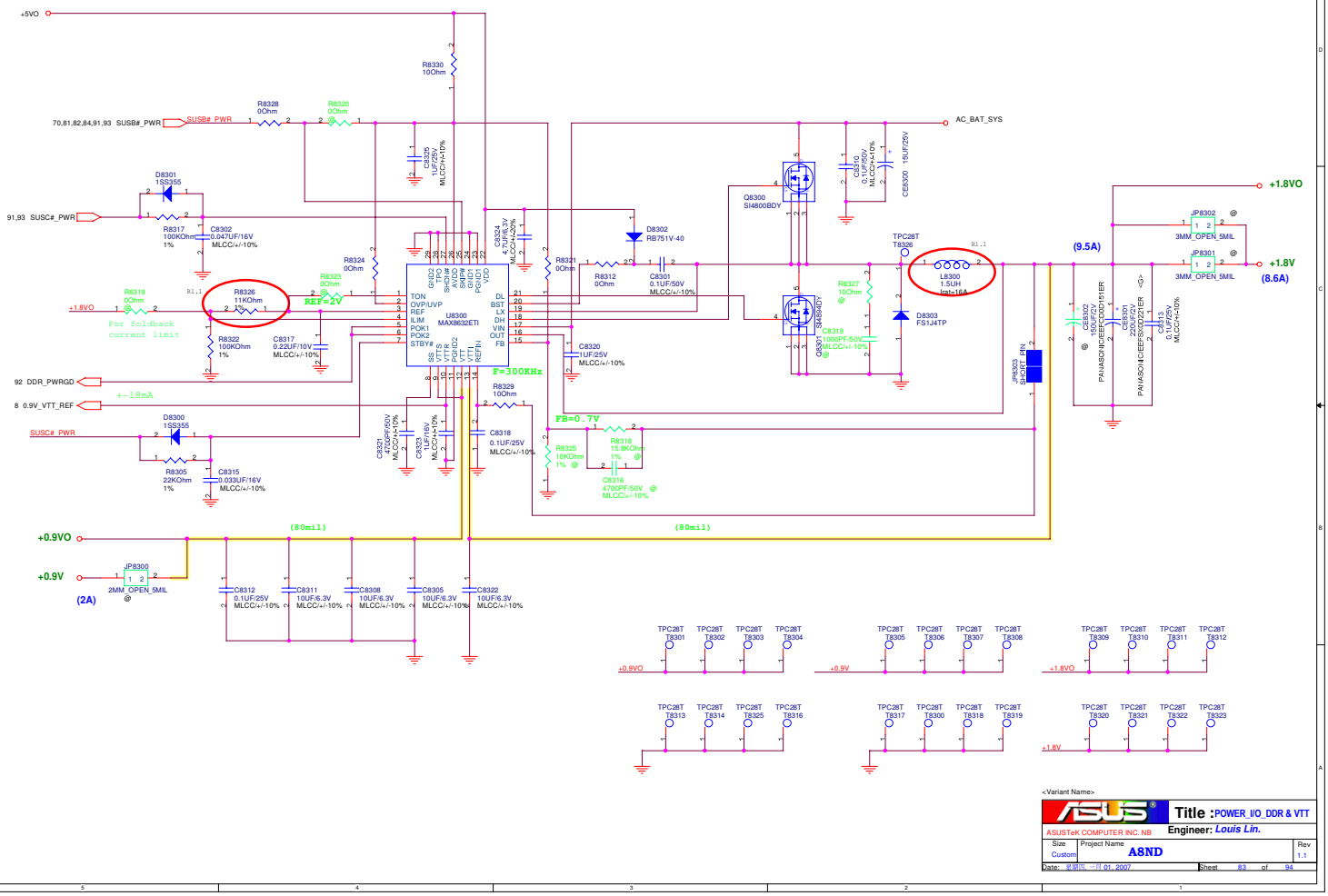
1.

ASUSTeK COMPUTER INC	Title : History	
	Engineer: Allen_CD Wu	
Size: Custom	Project Name: A8N_A8Dc	Rev: 1.0
Date: 星期四, 三月 01, 2007	Sheet 79 of 94	









<Variant Name>

ASUSTeK COMPUTER INC. NB

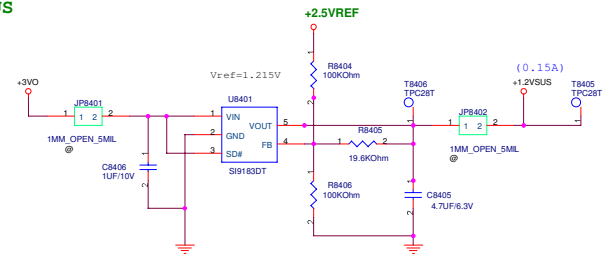
Title : POWER_I/O_DDR & VTT

Engineer: Louis Lin.

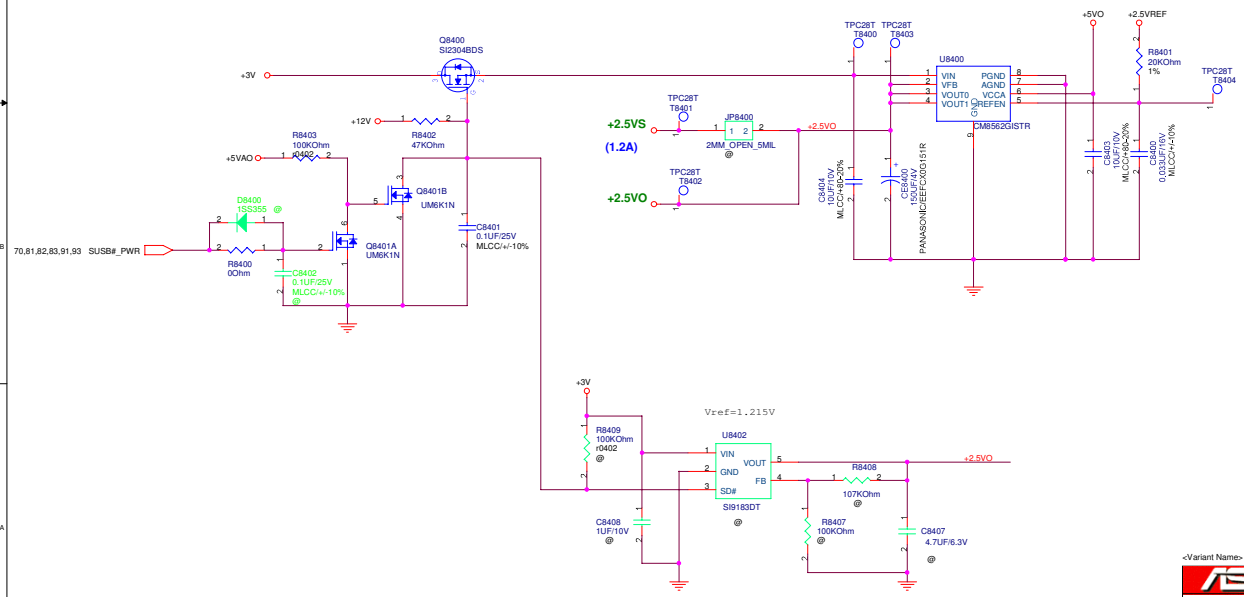
Size	Project Name	Rev
Custom	A8ND	1.1

Date: 日期四, 一月 01, 2007 Sheet 83 of 94

+1.2VSUS



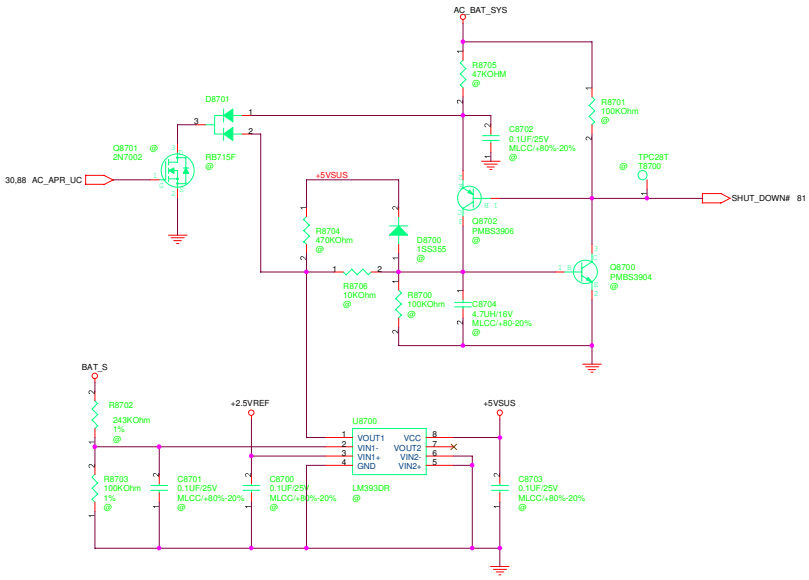
+2.5VS



<Variant Name>

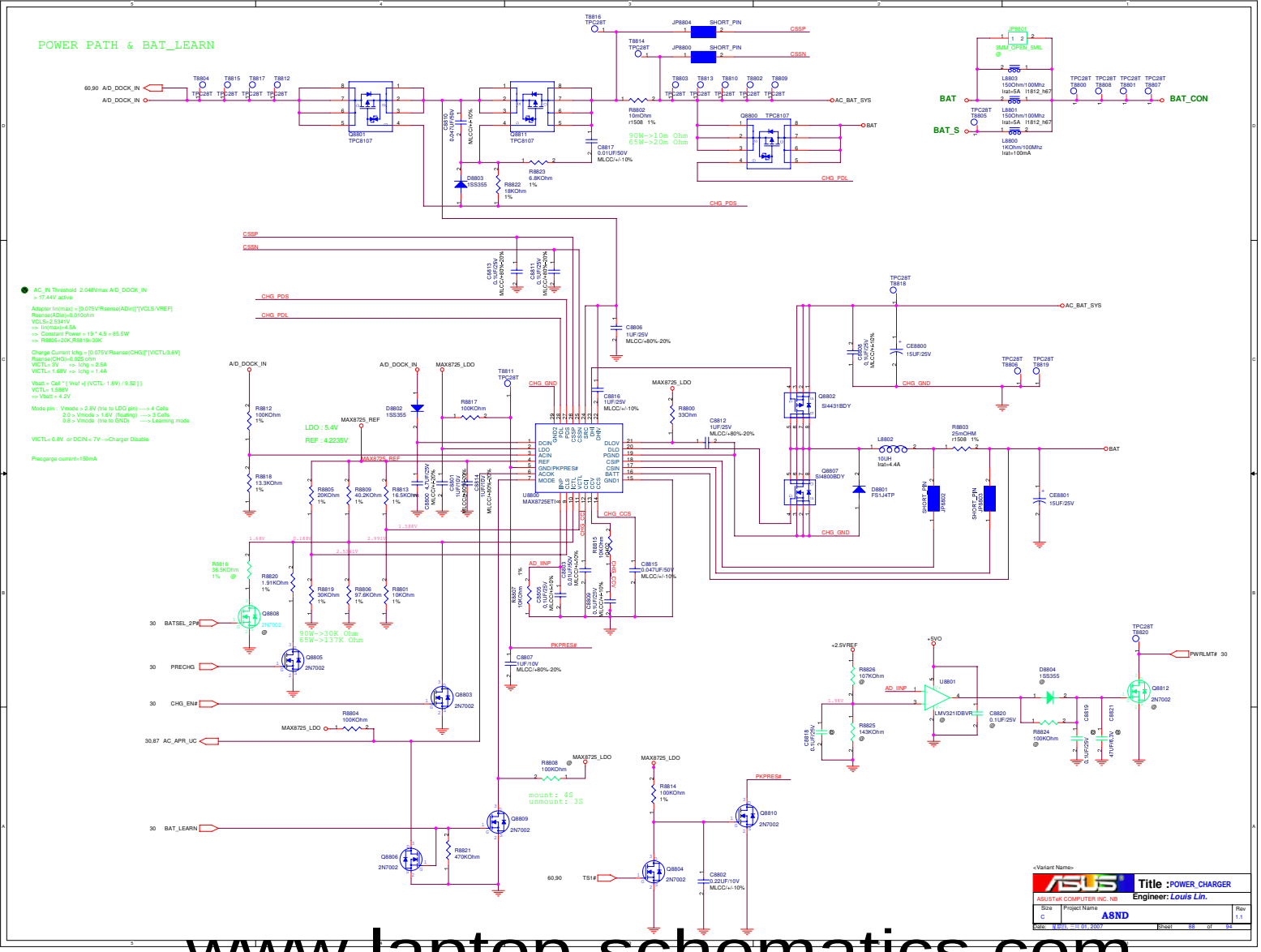
ASUS	Title : POWER_I/O_+1.2VSUS & +2.5V	
<OrgName>	Engineer: Louis Lin.	
Size: Custom	Project Name: A8ND	Rev: 1.1
Date: 星期四, 二月 01, 2007	Sheet 84 of 94	

PIC only

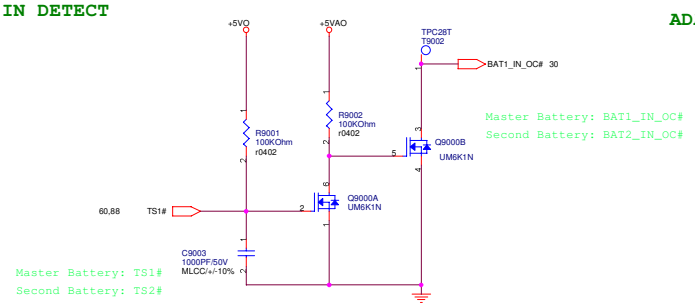


<Variant Name>

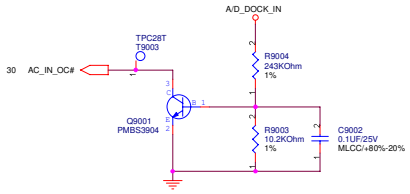
<OrgName>	Title : POWER_SHUTDOWN#	
	Engineer: Louis Lin.	
Size: Custom	Project Name: A8ND	Rev: 1.1
Date: 日期, 二月 01, 2007	Sheet 87 of 94	



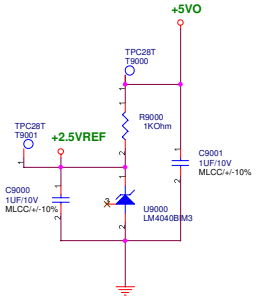
BATTERY IN DETECT



ADAPTER IN DETECT

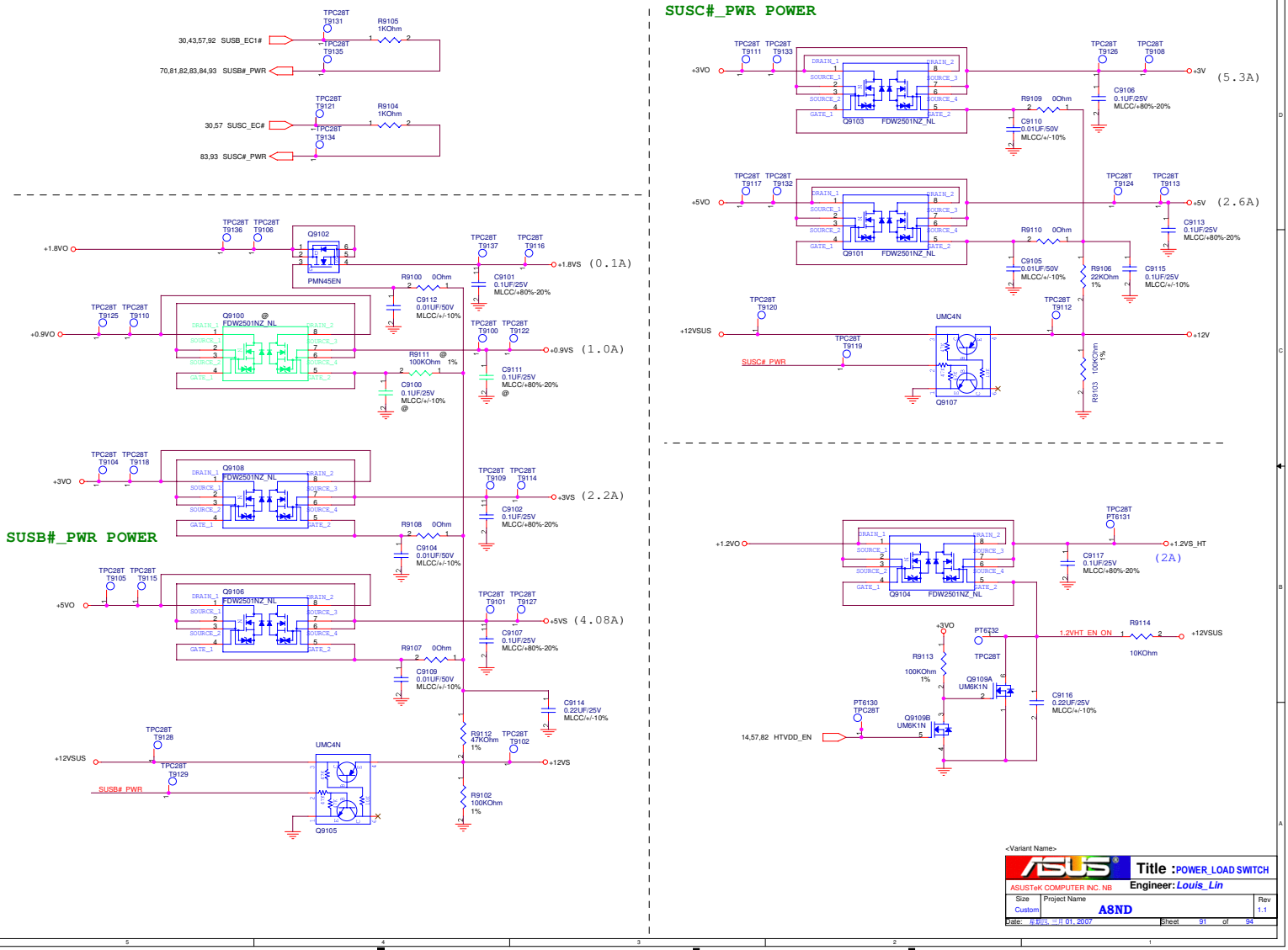


+2.5VREF

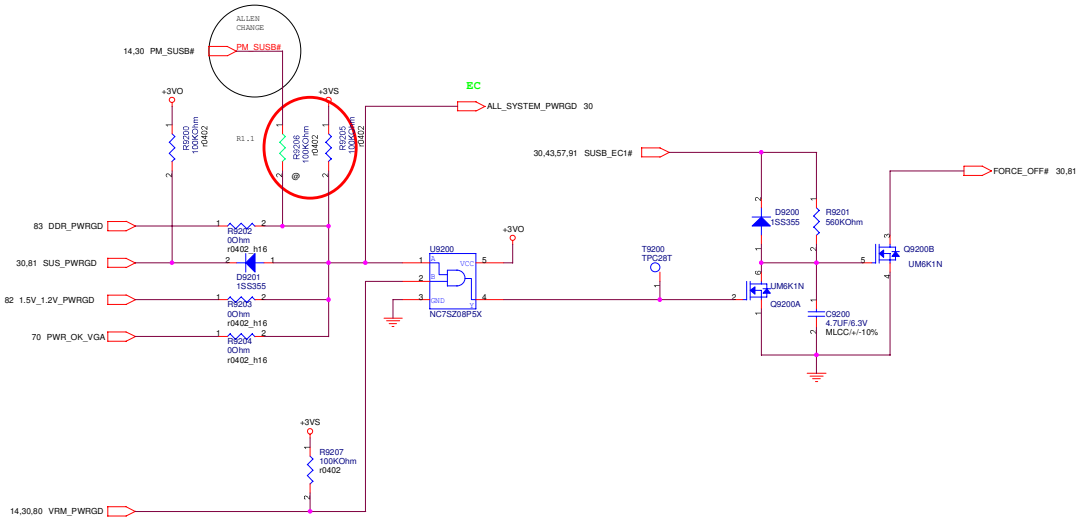


<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_DETECT	
	Engineer: Louis Lin.	
Size: Custom	Project Name: A8ND	Rev: 1.1
Date: 日期, 一月 01, 2007	Sheet 90 of 94	



POWER GOOD DETECTER



<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_PROTECT	
	Engineer: Louis Lin.	
Size: Custom	Project Name: A8ND	Rev: 1.1
Date: 日期, 二月 01, 2007	Sheet 92 of 94	

AC_BAT_SYS — AC_BAT_SYS 45,70,80,81,82,83,87,88

BAT — BAT 88

BAT_CON — BAT_CON 60,88

+2.5VREF — +2.5VREF 84,87,88,90

+3VA — +3VA 13,14,30,57,81,82

+5VAO — +5VAO 81,84,90

+5VO — +5VO 81,82,83,84,88,90,91

+5VSUS — +5VSUS 56,81,87

+5V — +5V 3,8,43,52,57,68,70,91

+5VS — +5VS 15,31,36,38,46,47,50,51,56,57,68,80,91

+3VO — +3VO 81,82,84,91,92

+3VSUS — +3VSUS 3,10,11,12,13,14,30,33,43,53,57,81,82

+3V — +3V 34,43,45,53,56,57,61,62,84,91

+3VS — +3VS 3,7,8,10,11,12,13,14,15,30,36,38,40,41,42,43,45,46,47,49,50,51,53,55,57,62,68,70,80,82,91,92

+12VSUS — +12VSUS 81,91

+12V — +12V 38,42,52,57,84,91

+12VS — +12VS 38,45,57,70,91

+1.8VO — +1.8VO 70,83,91

+1.8V — +1.8V 3,5,7,8,9,57,83

+1.8VS — +1.8VS 3,11,57,91

+0.9VS — +0.9VS 91

+0.9VO — +0.9VO 83,91

+1.5VO — +1.5VO 82

+1.5VS — +1.5VS 43,53,57,70,82

+2.5VO — +2.5VO 84

+2.5VS — +2.5VS 3,57,70,84

+VCORE — +VCORE 5,80

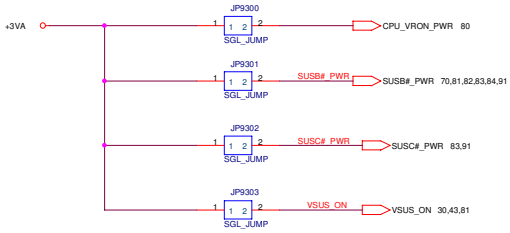
+1.25VS — +1.25VS

+1.2VSUS — +1.2VSUS 11,13,84

+1.2VS — +1.2VS 10,12,13,57,82

+1.2VO — +1.2VO 82,91

FOR POWER TEST



<Variant Name>

Title : POWER_SIGNAL

<OrgName> Engineer: Louis Lin.

Size	Project Name	Rev
Custom	A8ND	1.1

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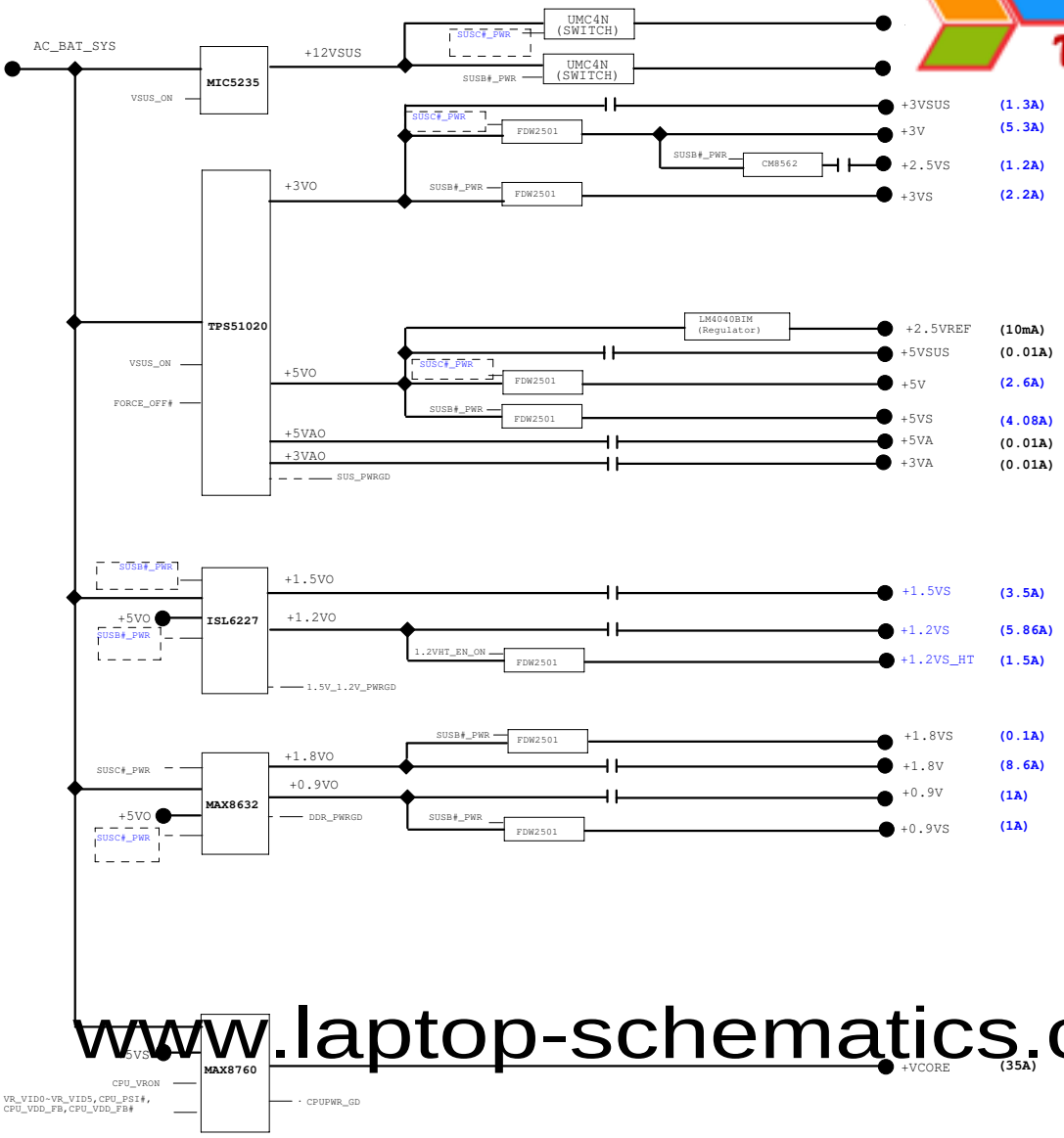

<Variant Name>
Title : POWER_FLOWCHART
ASUSTeK COMPUTER INC. NB
Engineer: Louis_Lin
Size: Custom | Project Name: A8ND | Rev: 1.1
Date: 日 四月 19 01 2007 | Sheet 94 of 94