F3Jr

GDDR2 16Mx16 x4 — Option

GDDR2 16Mx16 x4

CPU
YONAH 31W / MEROM 34W

CLOCK GEN
ICS 954310

THERMAL CONTROL

PSB 667MHz

LCD
CRT
TV-OUT
DVI

ATI M64-M or M76-M

PCI-E X16

NORTH BRIDGE
Intel 945PM

DDR2 — DDR2 SO-DIMM0

DDR2 — DDR2 SO-DIMM1

x4 DMI

Debug Conn.

TPM 1.2
INFINEON SLB9635

LPC

ISA ROM

EC
ITE IT8510E

Internal KB

Touch Pad

SOUTH BRIDGE
ICH7-M

PATA — PATA HDD

PATA — ODD

SATA — SATA HDD

AZALIA — AZALIA CODEC
Realtek ALC660

AUDIO AMP

EXT MIC

INT MIC

MDC

PCI

USB

PCIE x1 — MINICARD

PCIE x1 — NEWCARD

USB Port X4

Bluetooth

CMOS Camera

Finger Print

3 in 1 Card Reader

1394

Card Reader 1394
Ricoh R5C832/R5C841

PCMCIA

GIGALAN
Realtek RTL8111B

ASUSTek Computer INC. NB1

Title : Block Diagram

Engineer: Frank Xu

Size: Custom | Project Name: F3Jr | Rev: 2.0

Date: 十一月 11, 2006 | Sheet 1 of 94

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	/	
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	/	
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/0
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	/	
165	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	/	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	BUF_PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	RF_ON_SW#	I
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	GAIN_AMP#_K	O
87	ADC4/GPE0	COLOREN#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	
25	CLKRUN#/WUI7/GPE7	BT_ON#	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I/0
115	PS2DAT1/GPF3	/	I/0
116	PS2CLK2/GPF4	TP_CLK	
117	PS2DAT2/GPF5	TP_DAT	
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	INSTANTON#	I
113	FA16/GPG0	FA16\	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	
28	LPC80LL/GPG7	AC_APR_UC#	

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	/	O
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	BTLED_ON	O
AC18	GPIO07	WLAN_LED_EN	O
E21	GPIO08	EXTSMI#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	WLAN_ON#	O
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13	ICH_GPIO13	I
R4	GPIO14	TP_LEDON	I
E22	GPIO15	CB_SD#	I
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STP_PCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	ICH_GPIO19	I
AF21	GPIO20/STP_CPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	CPU_Select	I
A13	GPIO22/REQ4#	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	LPC_DRQ#1	I/O
R3	GPIO24	ICH_GPIO24	O
D20	GPIO25	ICH_GPIO25	O
A21	GPIO26/EL_RSVD	ICH_GPIO26	O
B21	GPIO27/EL_STATE0	PD_DET#	I
E23	GPIO28/EL_STATE1	ICH_GPIO28	O
C3	GPIO29/OC#5	USB_OC#5	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC#7	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O
AC19	GPIO33/AZ_DOCK_EN#	ICH_GPIO33	O
U2	GPIO34/AZ_DOCK_RST#	ICH_GPIO34	O
AD21	GPIO35	ICH_GPIO35	O
AH19	GPIO36/SATA2GP	ICH_GPIO36	I
AE19	GPIO37/SATA3GP	PCB_ID0	I
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER(832/841)	AD17/AD18	(0/1)	A
1394(832/841)	AD17/AD18	(0/1)	B
CARD BUD(/841)	AD18	1	C

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

ASUSTek Computer INC. NB1

Title : System Setting

Engineer: Frank Xu

Size: Custom | Project Name: F3Jr | Rev: 2.0

Date: 十月 11, 2006 | Sheet 2 of 94

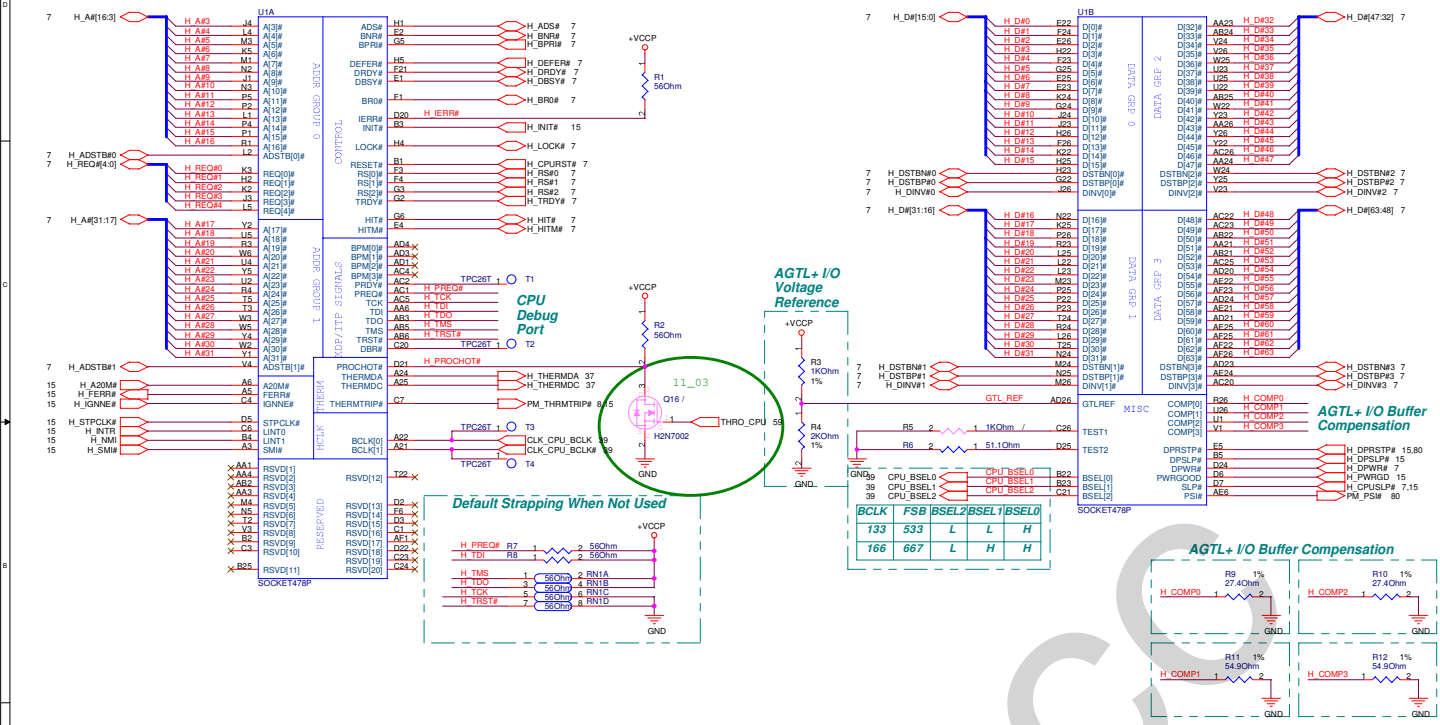
ASUSTeK COMPUTER INC

Title : Schematic page name

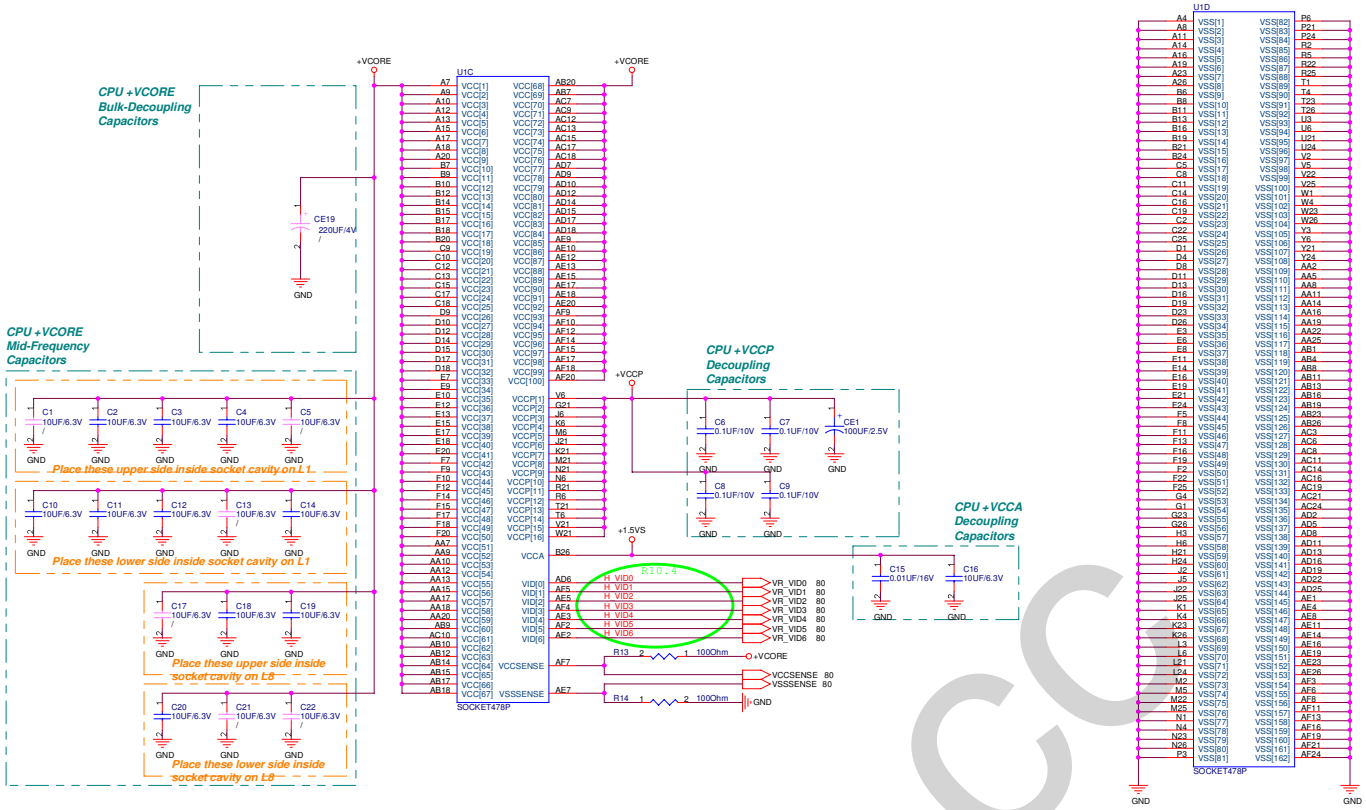
Engineer: Frank Xu

Size	Project Name	Rev
Custom	F3Jr	2.0

Date: 十二月 11, 2006 Sheet 3 of 94



ASUSTeK COMPUTER INC. NB1		Title : CPU-YONAH(HOST)			
		Engineer: Frank Xu			
Size	Project Name			Rev	
Custom	F3Jr			2.0	
Date: 星期一, 十二月 11, 2006		Sheet 4 of 94			



+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*R1F: 10UF *16*
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*R1F: 220UF *1, 0.1UF *4*

ASUSTeK COMPUTER INC. NB1

Title : CPU_YONAH(PWR)

Engineer: Frank Xu

Size	Project Name	Rev
Custom	F3Jr	2.0

Date: 十月 11, 2006 Sheet 5 of 94

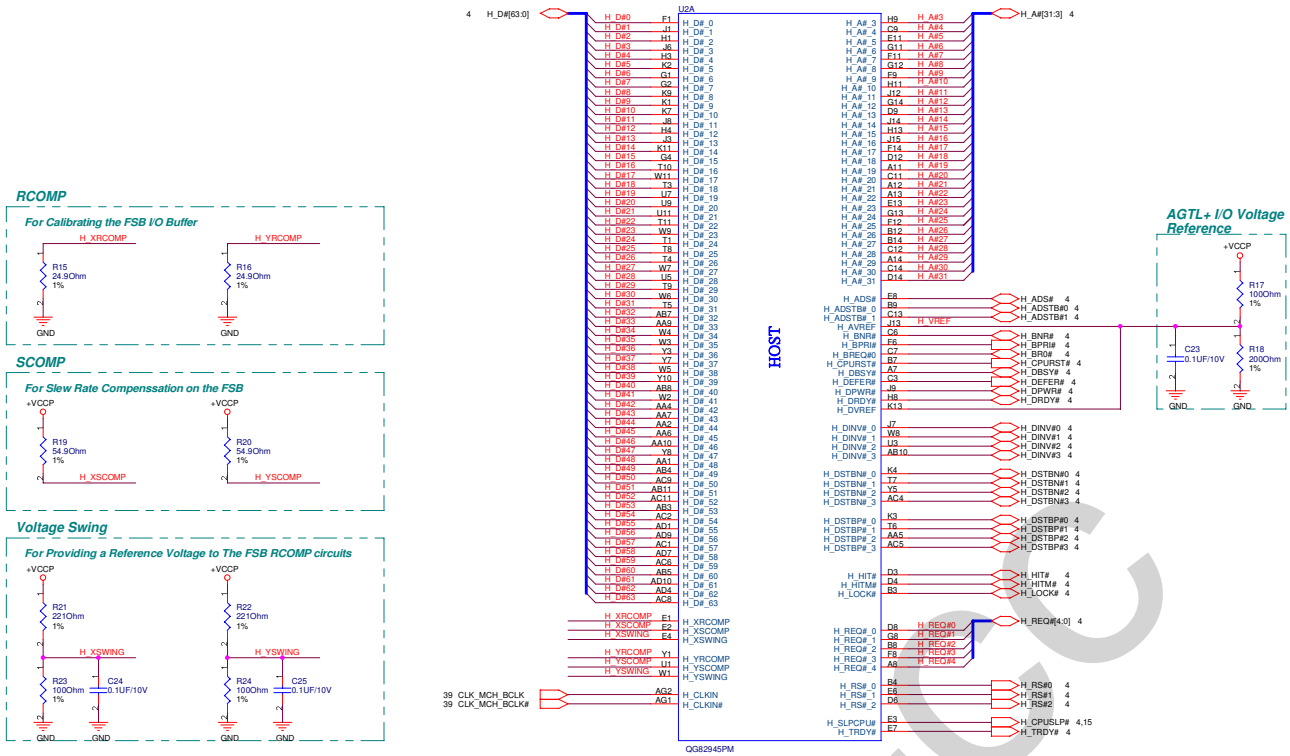
ASUSTeK COMPUTER INC

Title : Schematic page name

Engineer: Frank Xu

Size	Project Name	Rev
Custom	F3Jr	2.0

Date: 日曜一, 十二月 11, 2006 Sheet 6 of 94



ASUSTeK COMPUTER INC. NB1	Title : NB-945PM(HOST)		
	Engineer: Frank Xu		
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 五月 11, 2006	Sheet 7 of 94		

GMCH Strapping

CFG5 : DMI Strap
- 0 = DMI x2
- 1 = DMI x4 (D)

MCH_CFG_5 — R25 1KOhm — GND

CFG[13:12] : GMCH Test Mode
- 00= Partial CLK Gating Disable
- 01 = XOR Mode Enable
- 10 = All Z Mode Enable
- 11 = Normal Operation (D)

CFG7 : CPU Strap
- 0 = DT/Transpotable CPU
- 1 = Mobile CPU (D)

MCH_CFG_7 — R26 1KOhm — GND

CFG15 : ICH RESET Disable
- 0 = ICH Reset Disable
- 1 = Normal Operation (D)

MCH_CFG_15 — R27 1KOhm — GND

CFG9 : PCIE Graphic Lane
- 0 = Reverse Lane
- 1 = Normal Operation (D)

MCH_CFG_9 — R30 1KOhm — GND

CFG16 : FSB Dynamic ODT
- 0 = Dynamic ODT Disable
- 1 = Dynamic ODT Enable (D)

MCH_CFG_16 — R31 1KOhm — GND

CFG10 : HOST PLL VCO Select
- 0 = Reserved
- 1 = Mobility (D)

MCH_CFG_10 — R34 1KOhm — GND

CFG18 : VCC Select
- 0 = 1.05V (D)
- 1 = 1.5V

MCH_CFG_18 — R35 1KOhm — +2.5VS

CFG11 : PSB 4x CLK Enable
- 0 = 4x Enable
- 1 = 8x Enable (D)

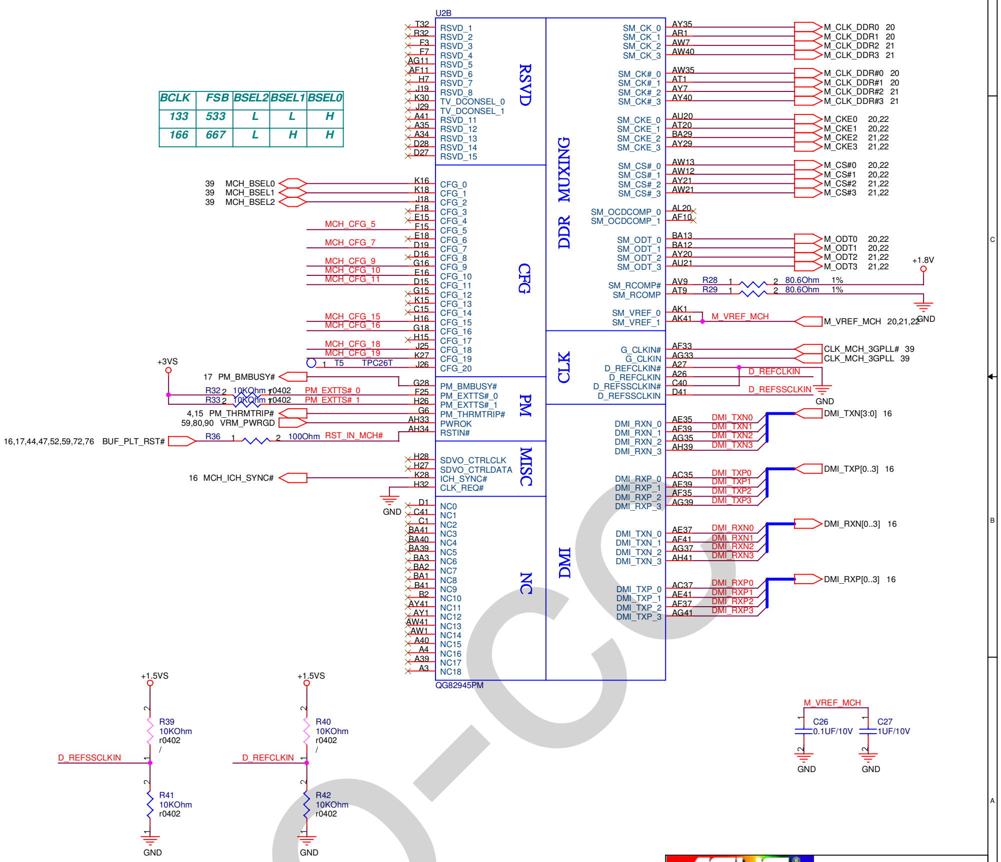
MCH_CFG_11 — R37 1KOhm — GND

CFG19 : DMI Lane Reversal
- 0 = Normal Operation (D)
- 1 = Lanes Reversed

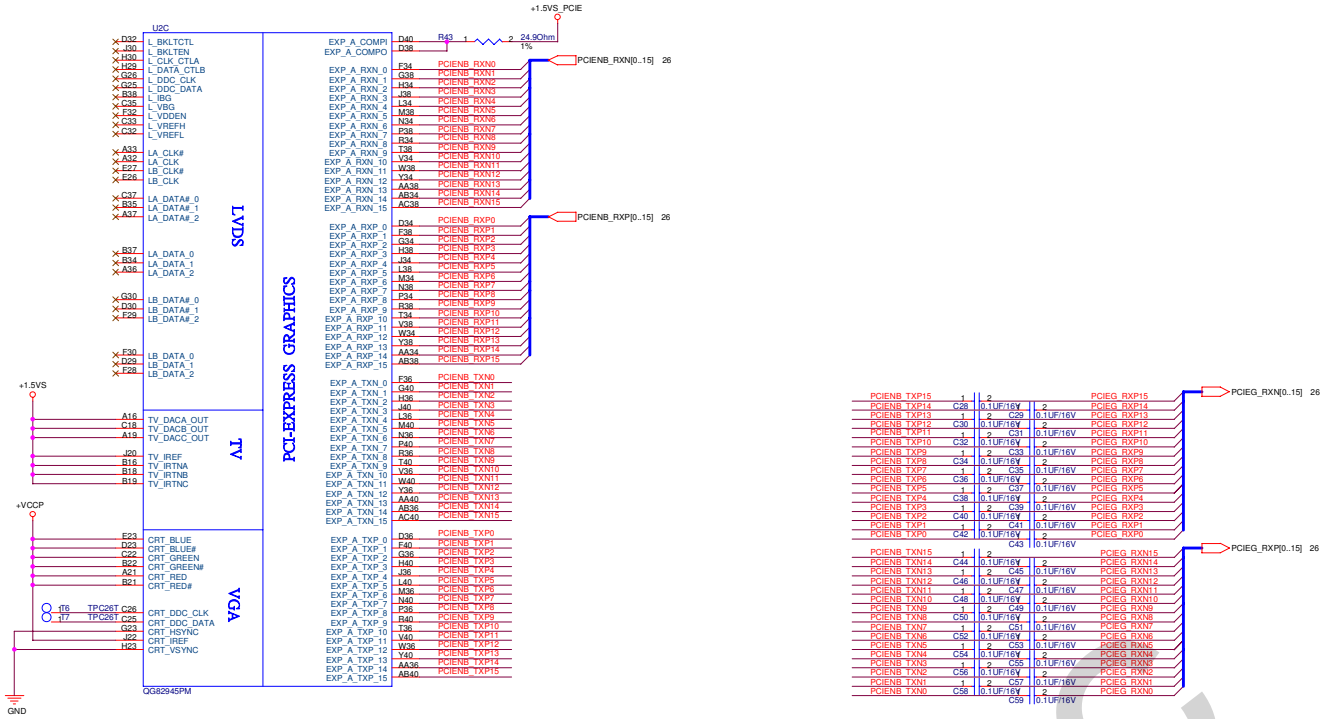
MCH_CFG_19 — R38 1KOhm — +2.5VS

Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

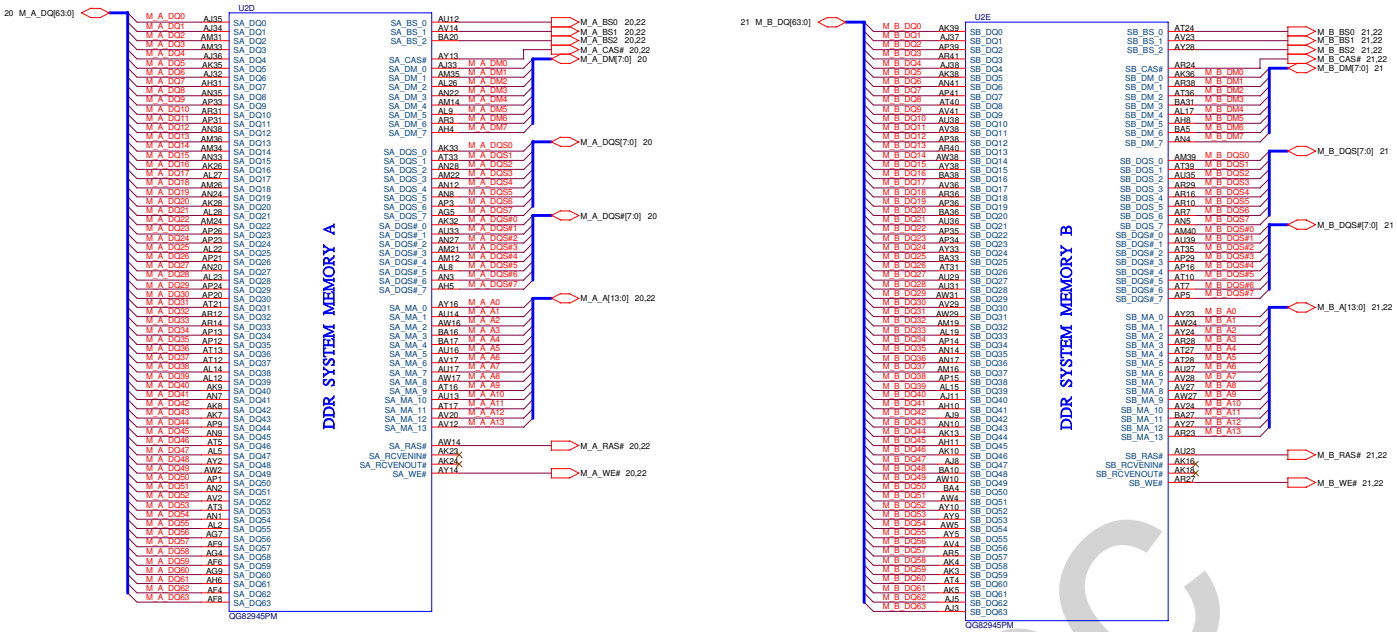
BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



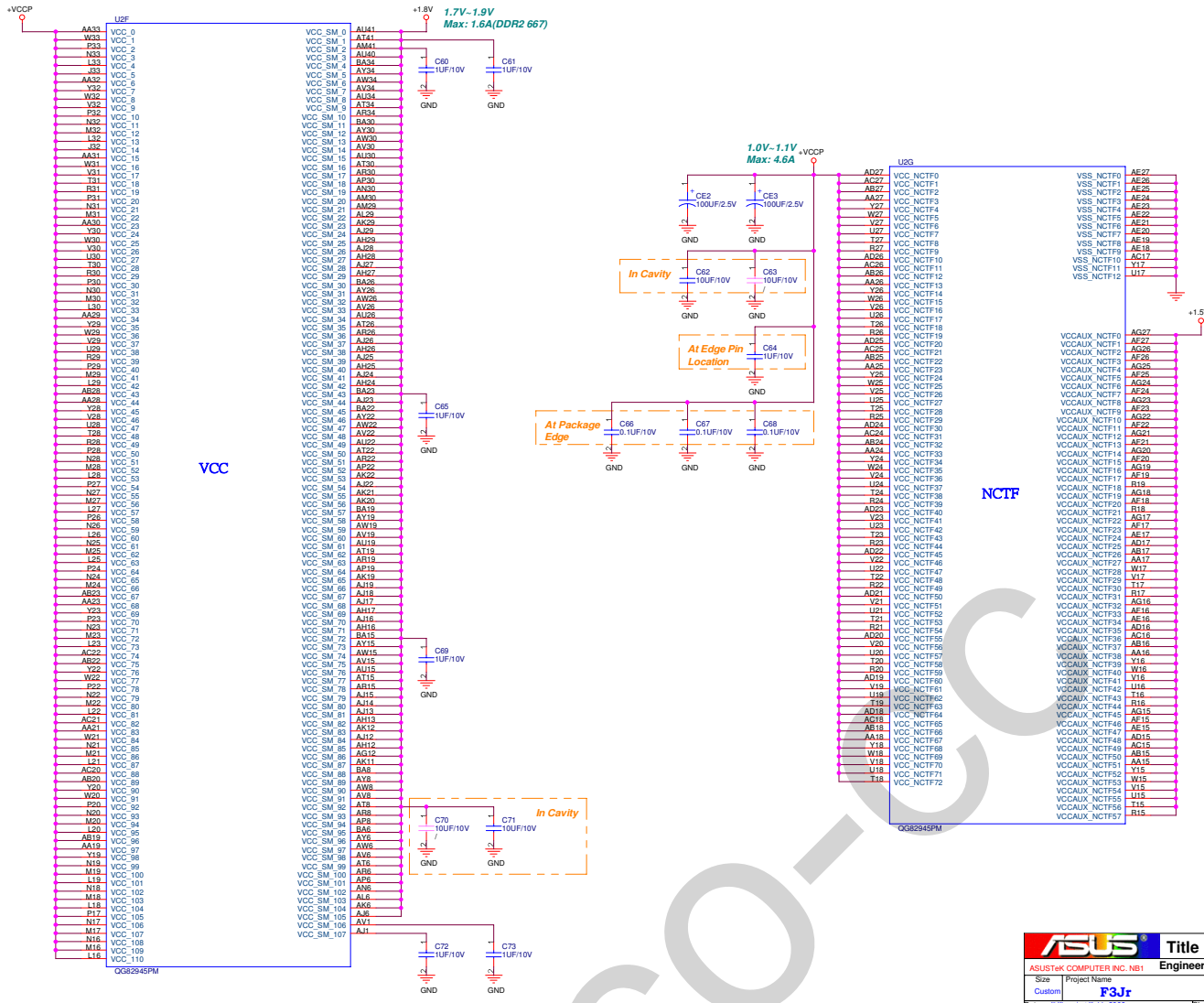
Title : NB-945PM(DMI & CFG)		
ASUSTeK COMPUTER INC. NB1	Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 星期一, 十二月 11, 2006	Sheet 8 of 94	



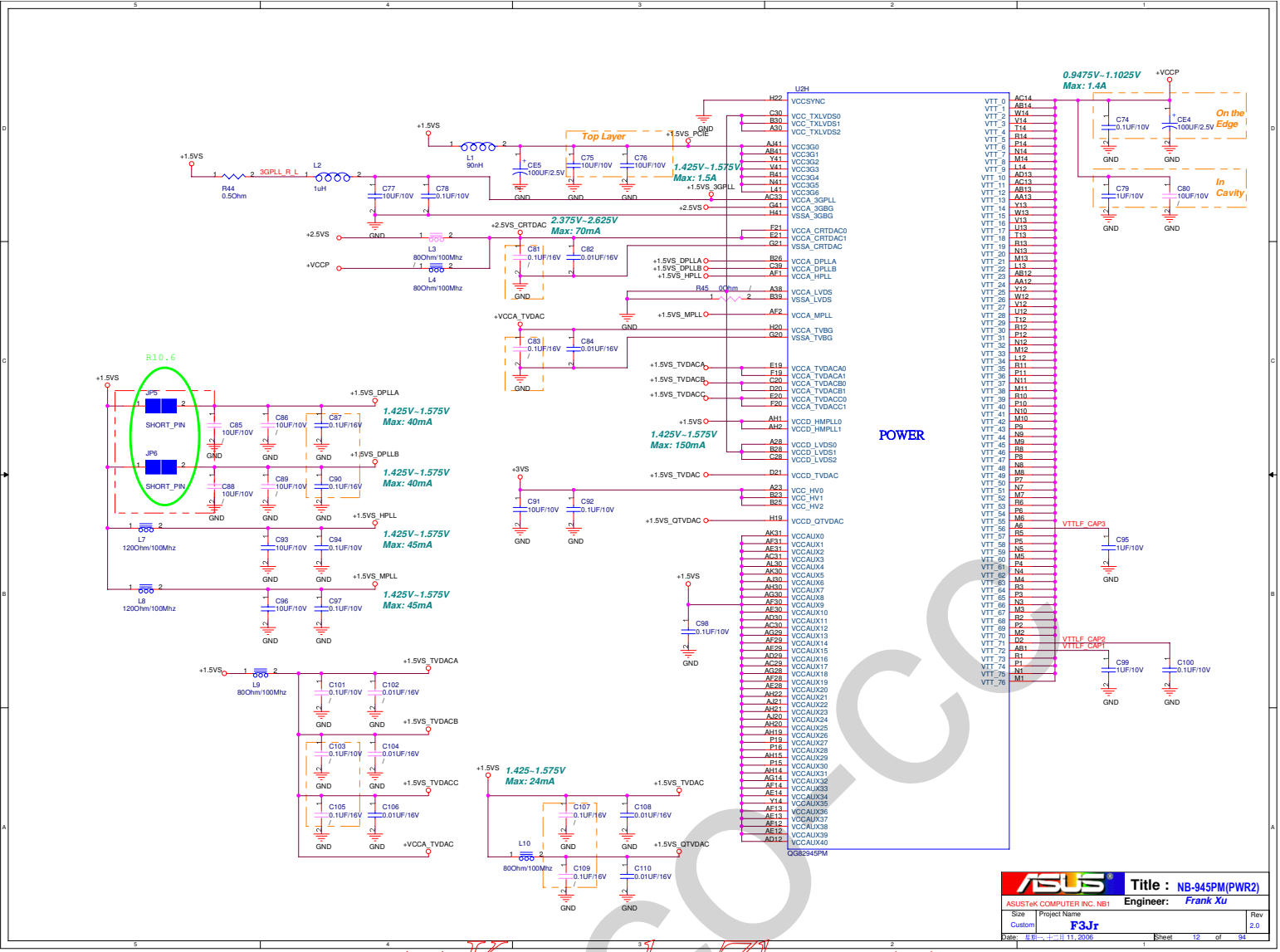
ASUSTeK COMPUTER INC. NB1	Title : NB_945PM(GRAPHIC)		
	Engineer: Frank Xu		
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 日期-, 十二月 11, 2006	Sheet 9 of 94		

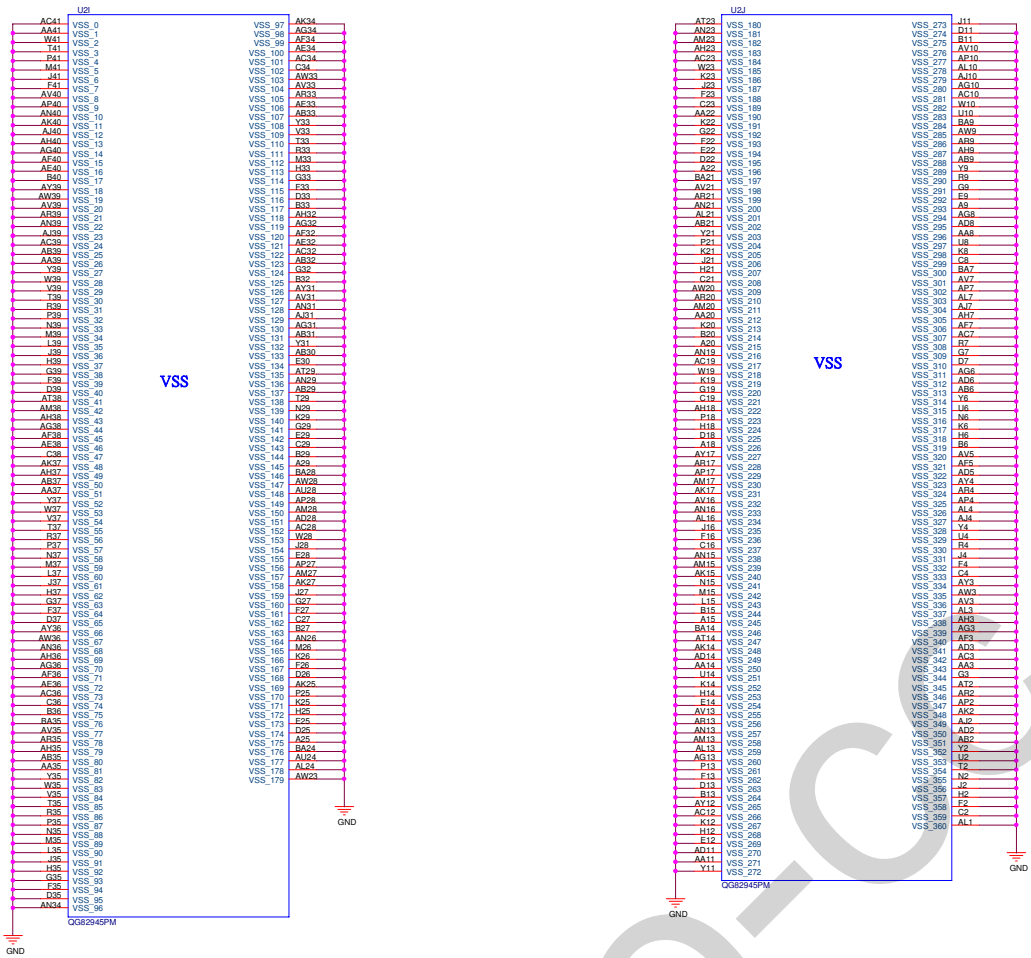


ASUSTeK COMPUTER INC. NB1	Title : NB-945PM(DDR2)	
	Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 日期-, 十二月 11, 2006	Sheet 10 of 94	



ASUSTeK COMPUTER INC. NB1	Title : NB-945PM(PWR)		
	Engineer: Frank Xu		
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 五月 11, 2006	Sheet 11 of 94		





ASUSTeK COMPUTER INC. NB1	Title : NB-945PM(GND)		
	Engineer: Frank Xu		
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 十月 11, 2006	Sheet 13 of 94		

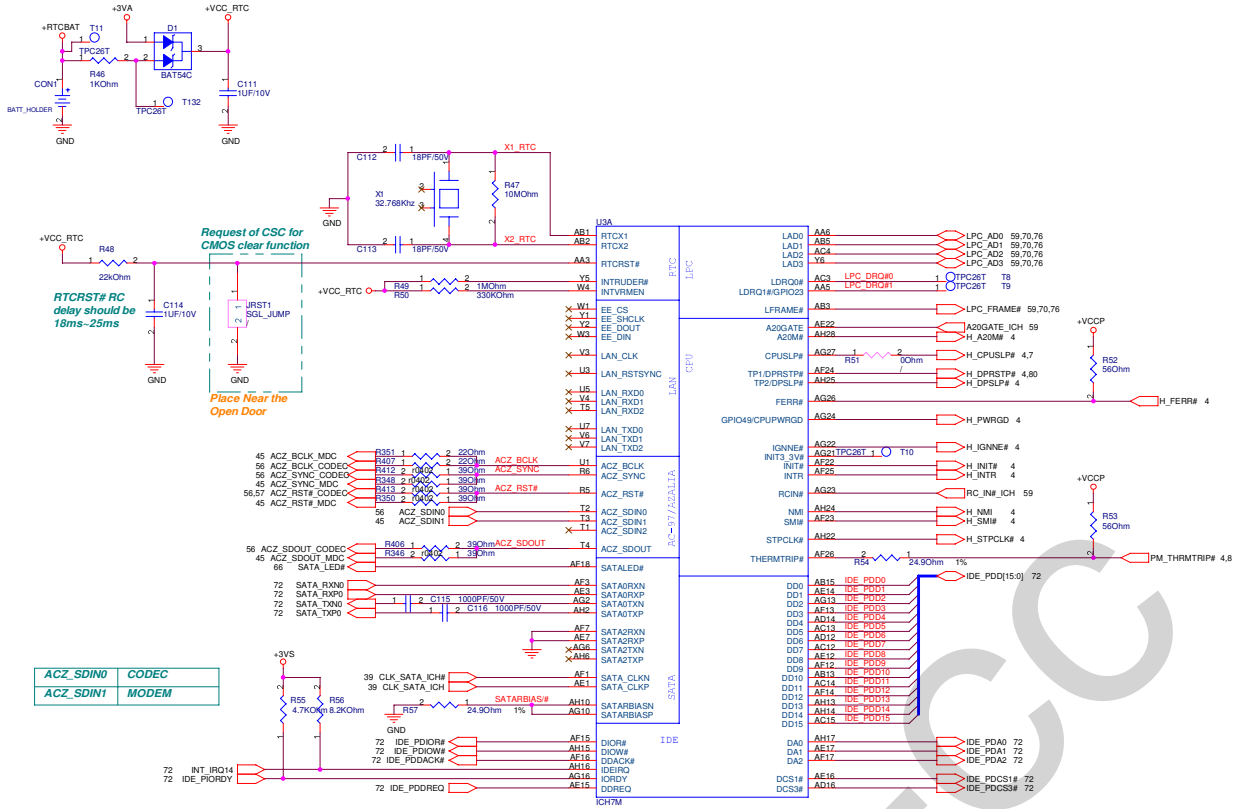
ASUSTeK COMPUTER INC

Title : Schematic page name

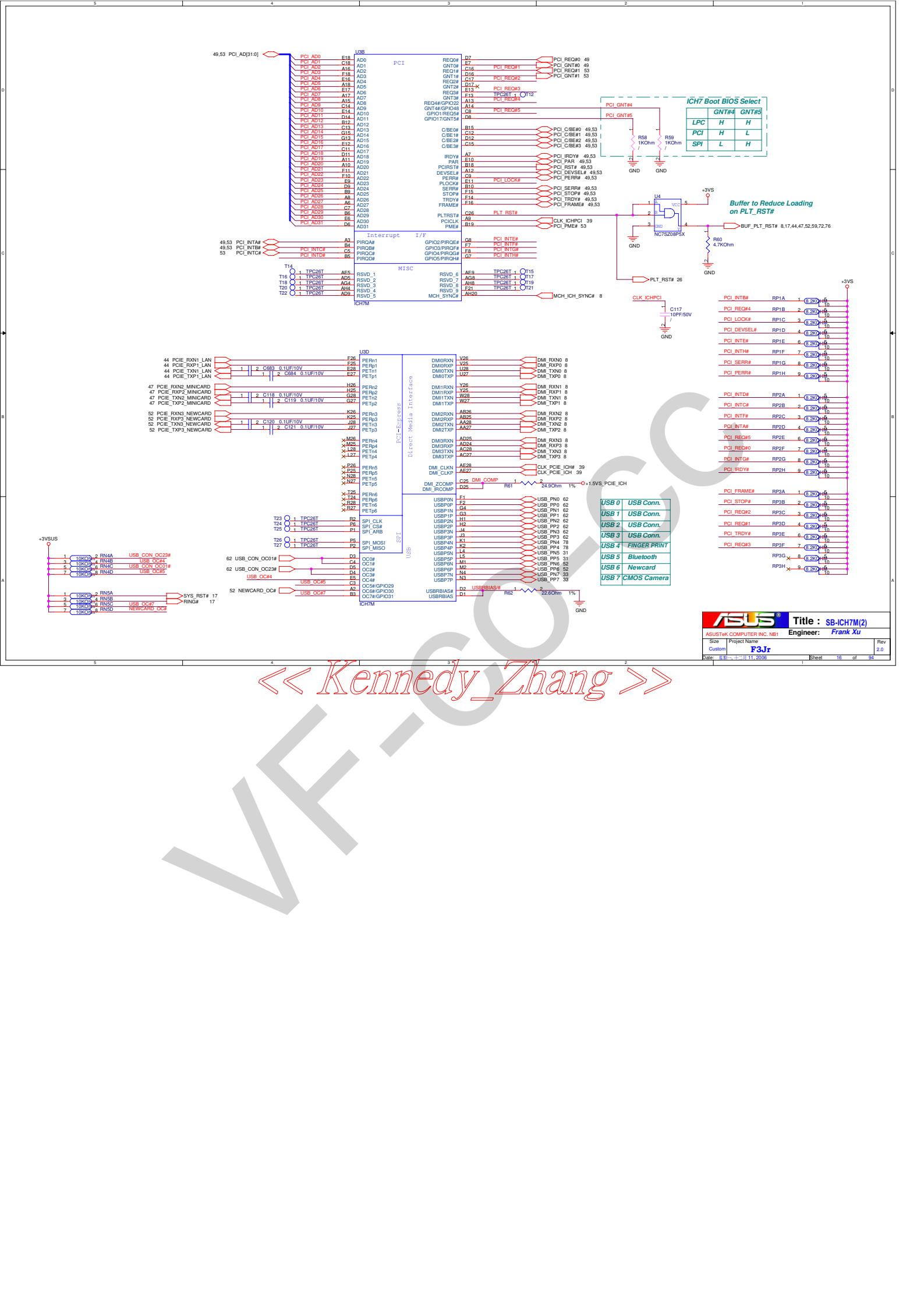
Engineer: Frank Xu

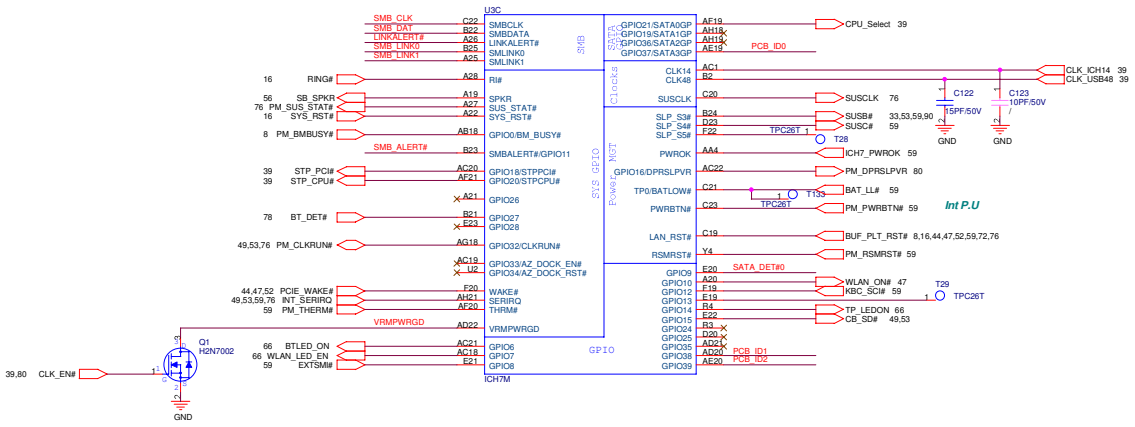
Size	Project Name	Rev
Custom	F3Jr	2.0

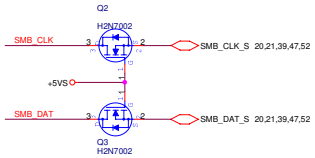
Date: 十月 11, 2006 Sheet 14 of 94

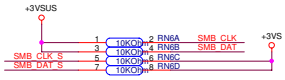


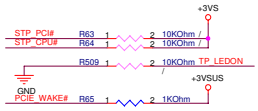
Title :	SB-ICH7-M(1)		
ASUSTeK COMPUTER INC. NB1	Engineer:	Frank Xu	
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 十月 11, 2006	Sheet 15 of 94		

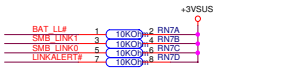

U3B
PCI
Interrupt I/F
MISC
ICH7M
ICH7 Boot BIOS Select
GNT#4
GNT#5
LPC H H
PCI H L
SPI L H
Buffer to Reduce Loading on PLT_RST#
U3D
PCI-Express
Direct Media Interface
USB
SPI
USB 0 USB Conn.
USB 1 USB Conn.
USB 2 USB Conn.
USB 3 USB Conn.
USB 4 FINGER PRINT
USB 5 Bluetooth
USB 6 Newcard
USB 7 CMOS Camera
Title : SB-ICH7M(2)
ASUSTeK COMPUTER INC. NB1
Engineer: Frank Xu
Project Name F3Jr
Rev 2.0
Sheet 16 of 94
<< Kennedy_Zhang >>
VF-CO-CC

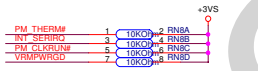


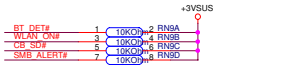


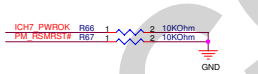


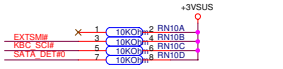


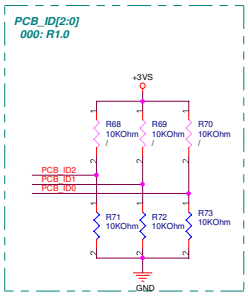










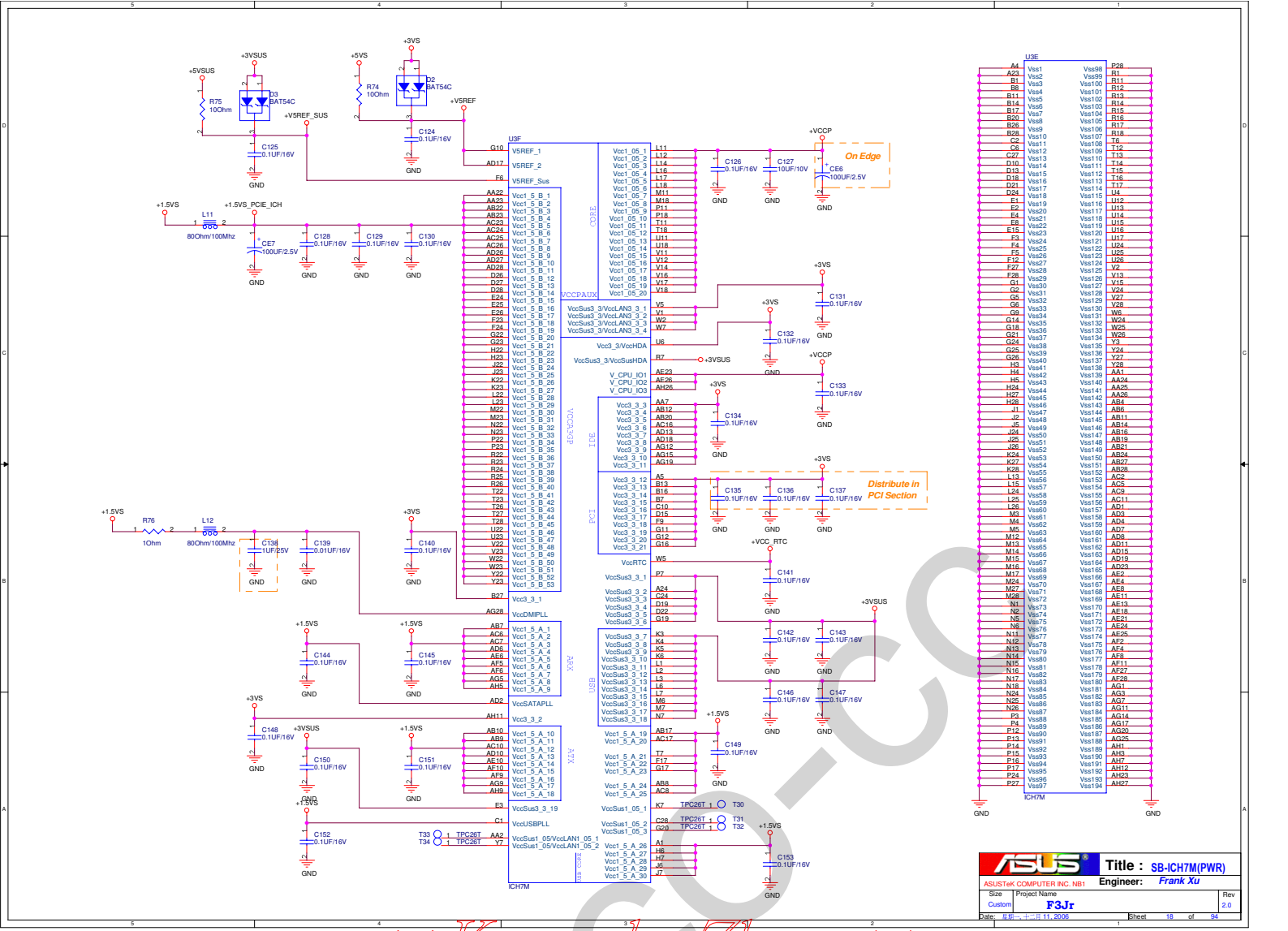


Title : SB-ICH7M(3)

ASUSTeK COMPUTER INC. NB1 Engineer: Frank Xu

Size	Project Name	Rev
Custom	F3Jr	2.0

Date: 五月 11, 2006 Sheet 17 of 94



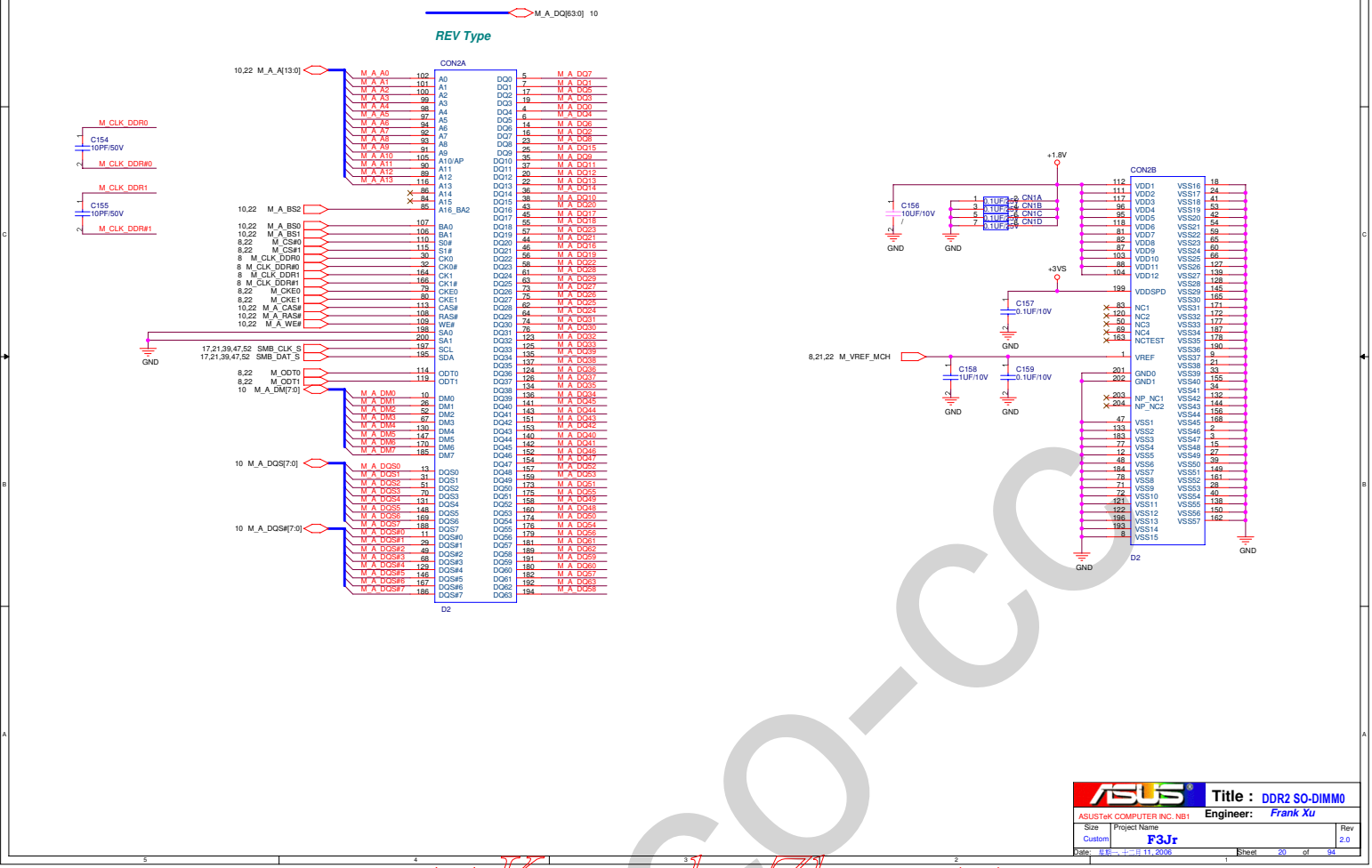
ASUSTeK COMPUTER INC

Title : Schematic page name

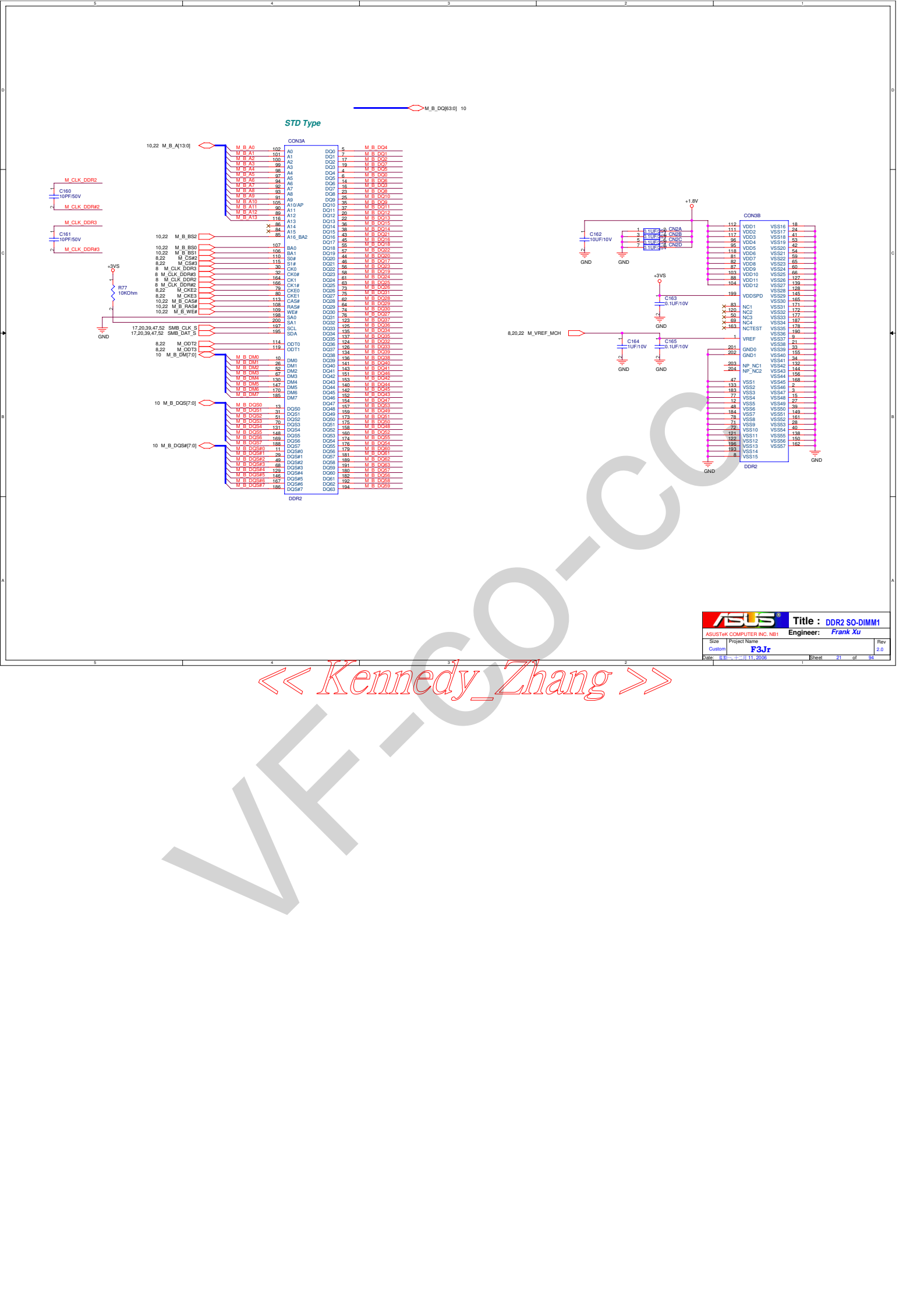
Engineer: Frank Xu

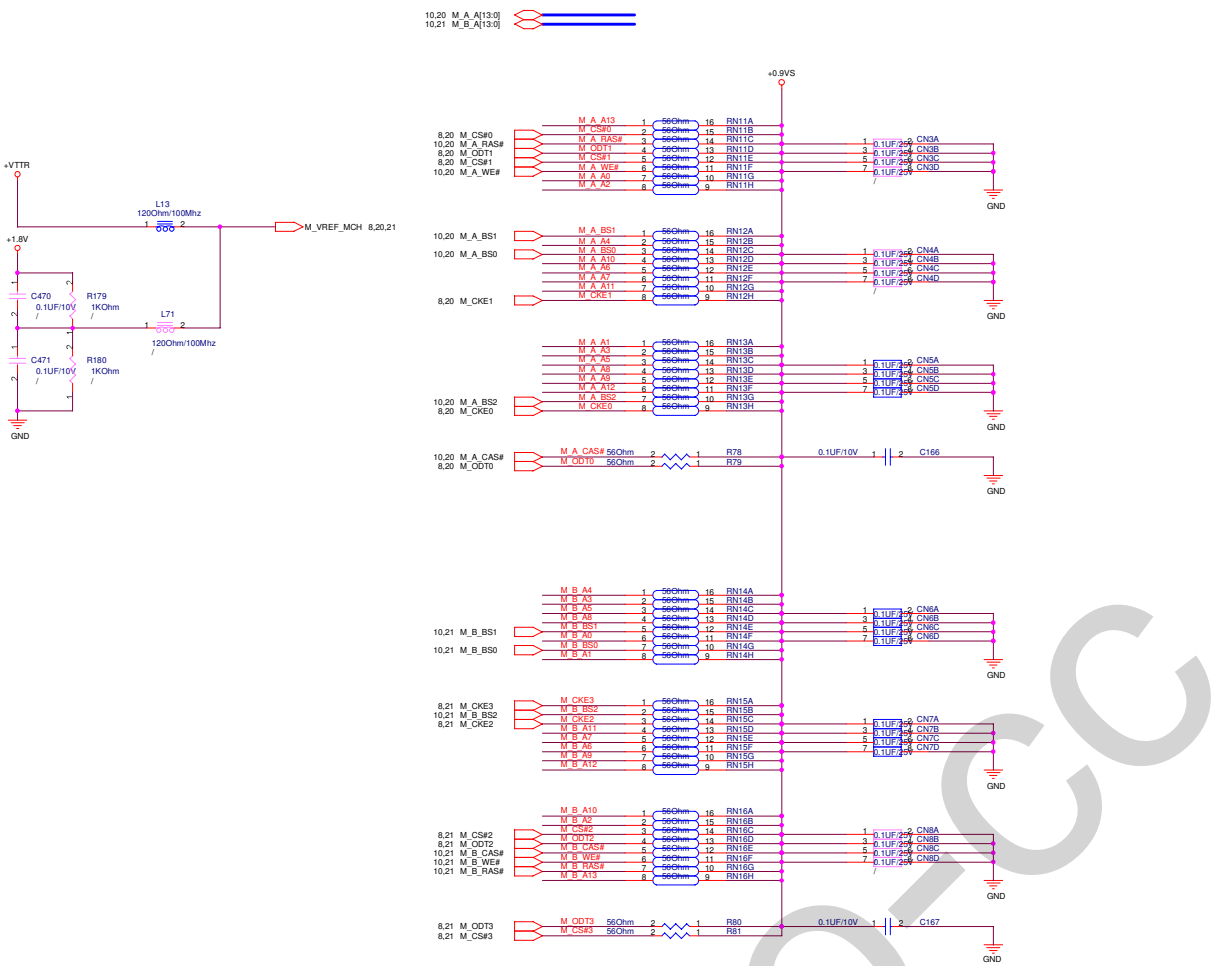
Size	Project Name	Rev
Custom	F3Jr	2.0

Date: 十二月 11, 2006 Sheet 19 of 94



ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM0	
	Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 日期-, 十二月 11, 2006	Sheet 20 of 94	





ASUSTeK COMPUTER INC. NB1

Title : DDR2 TERMINATION

Engineer: Frank Xu

Size	Project Name	Rev
Custom	F3Jr	2.0

Date: 十一月 11, 2006 Sheet 22 of 94

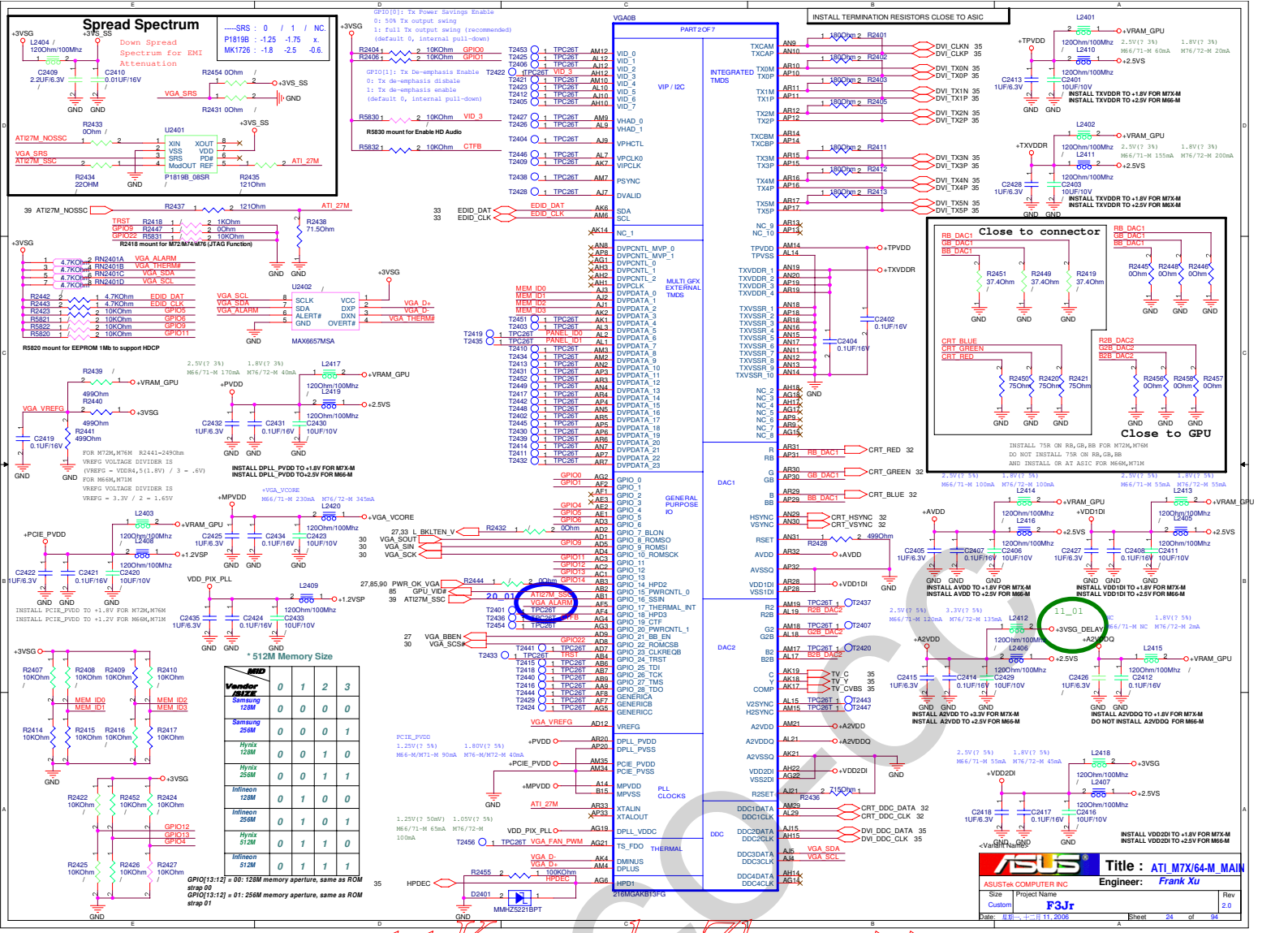
ASUSTeK COMPUTER INC

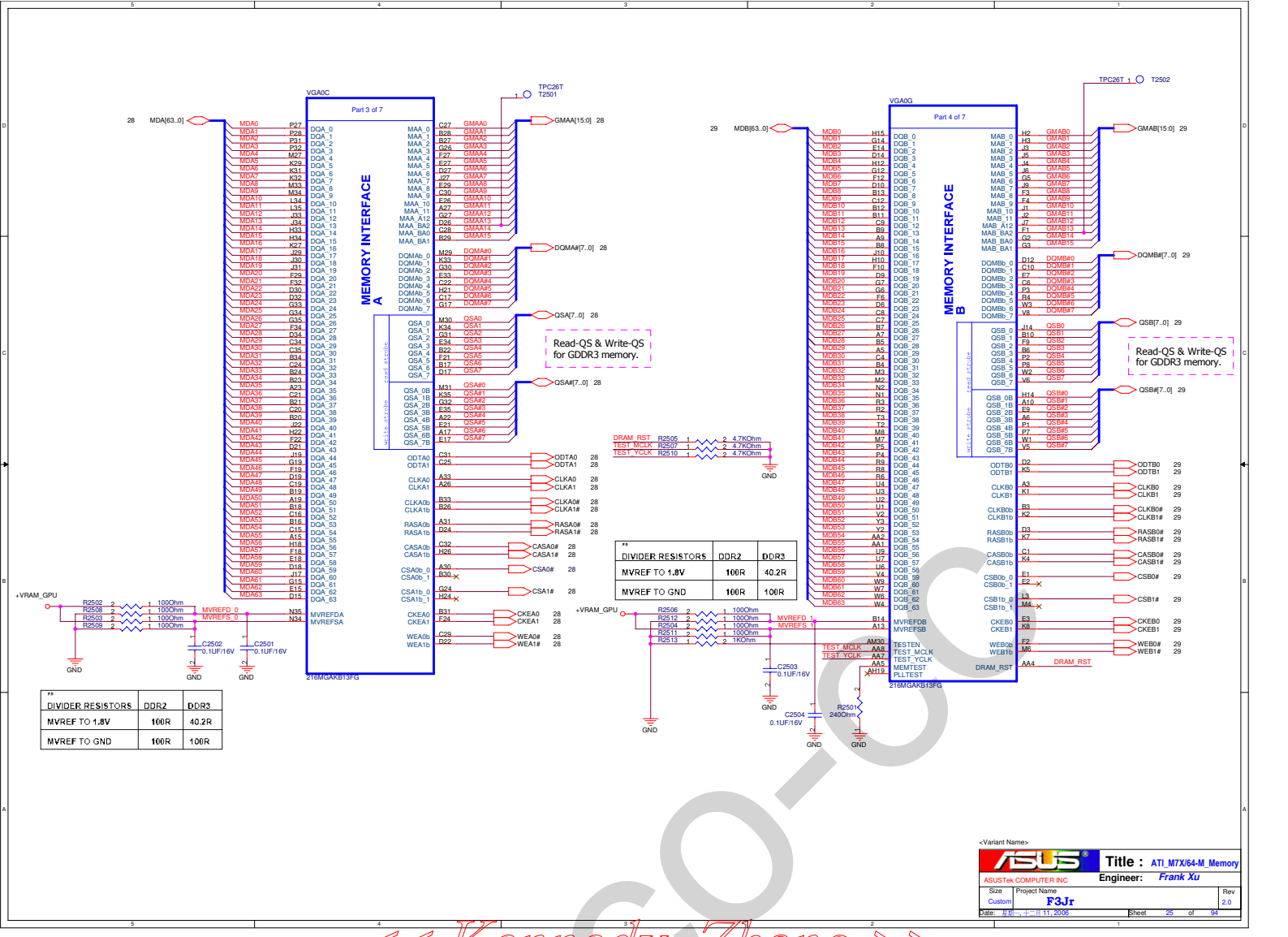
Title : Schematic page name

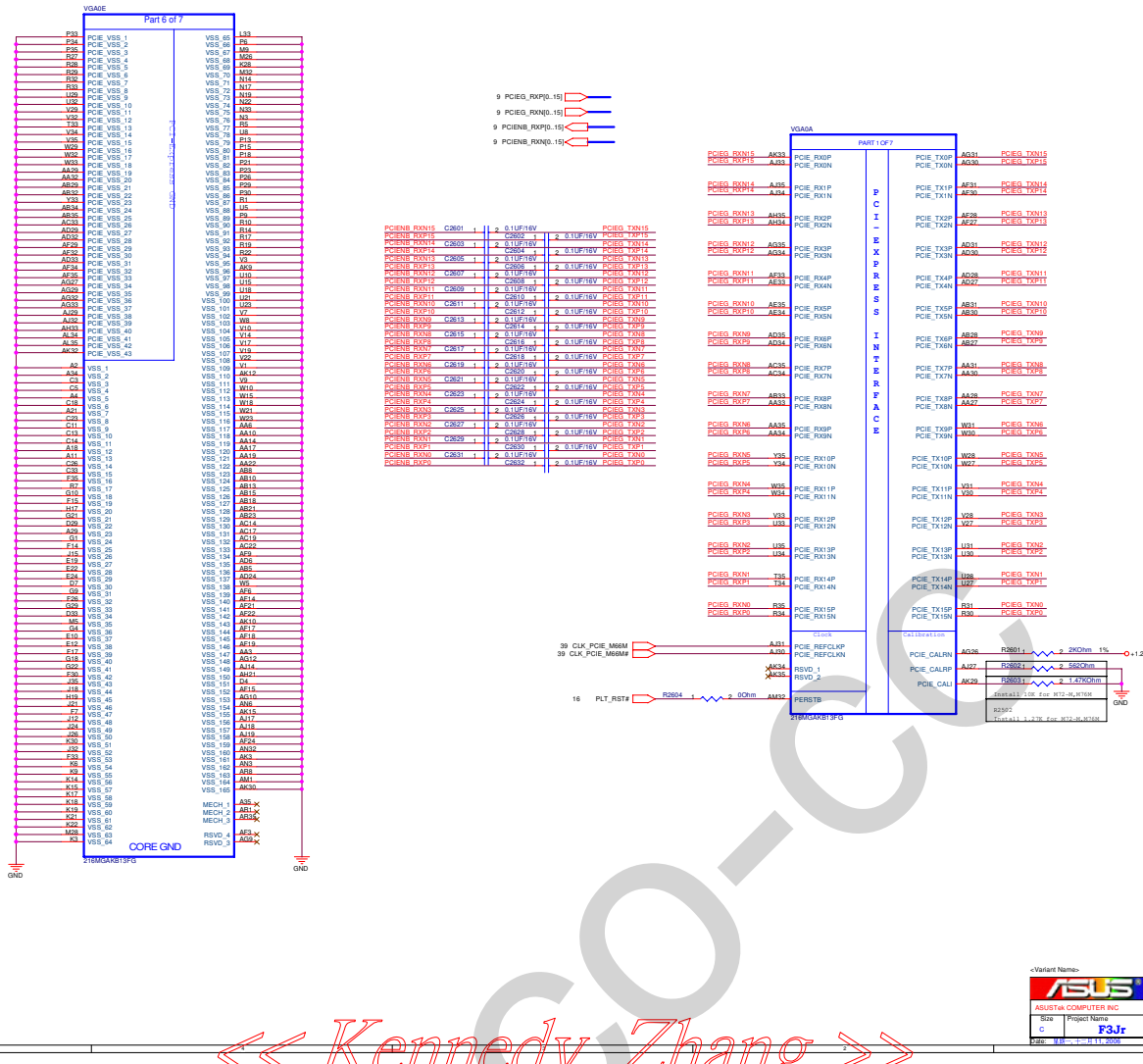
Engineer: Frank Xu

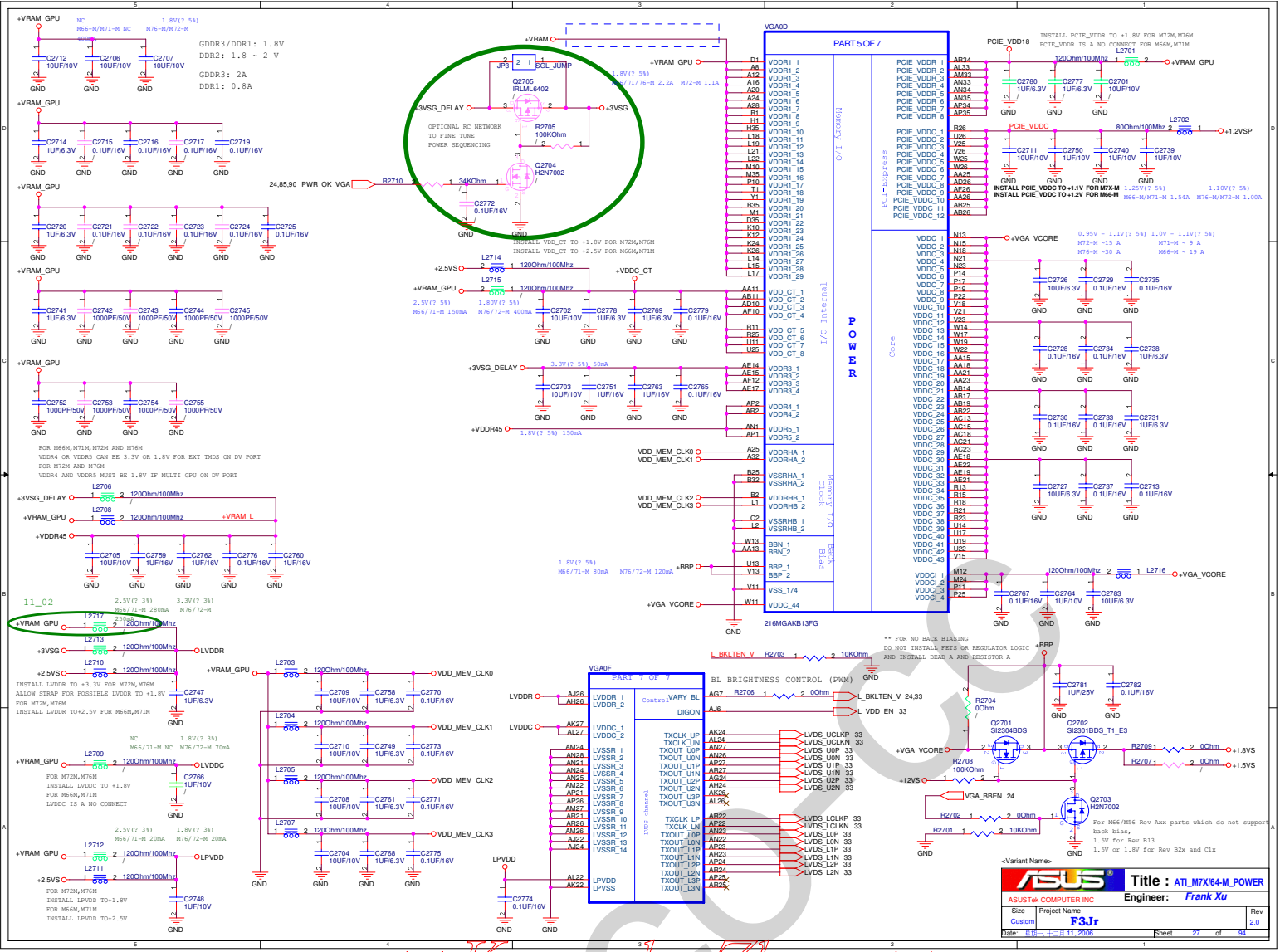
Size	Project Name	Rev
Custom	F3Jr	2.0

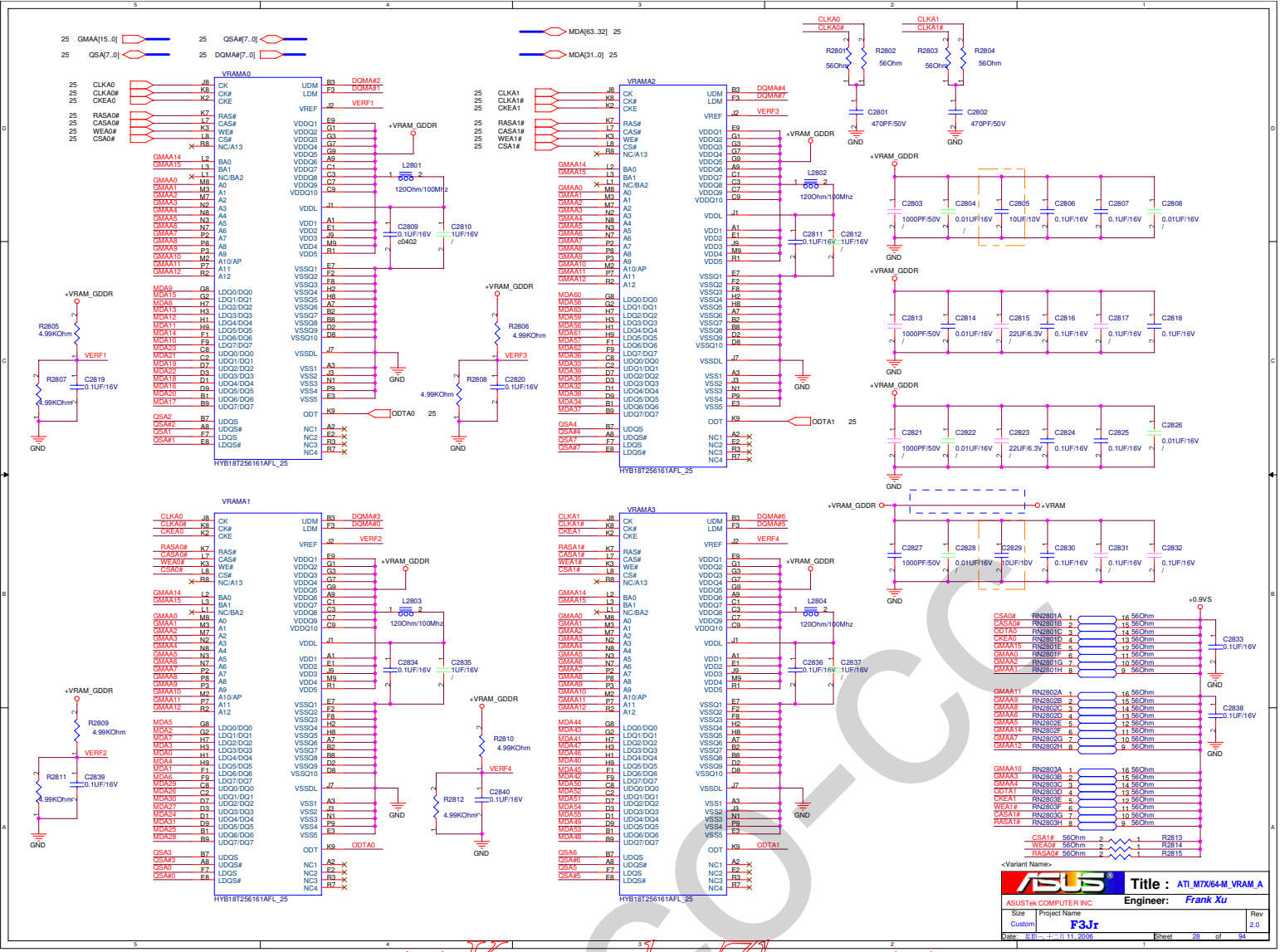
Date: 十月 11, 2006 Sheet 23 of 94

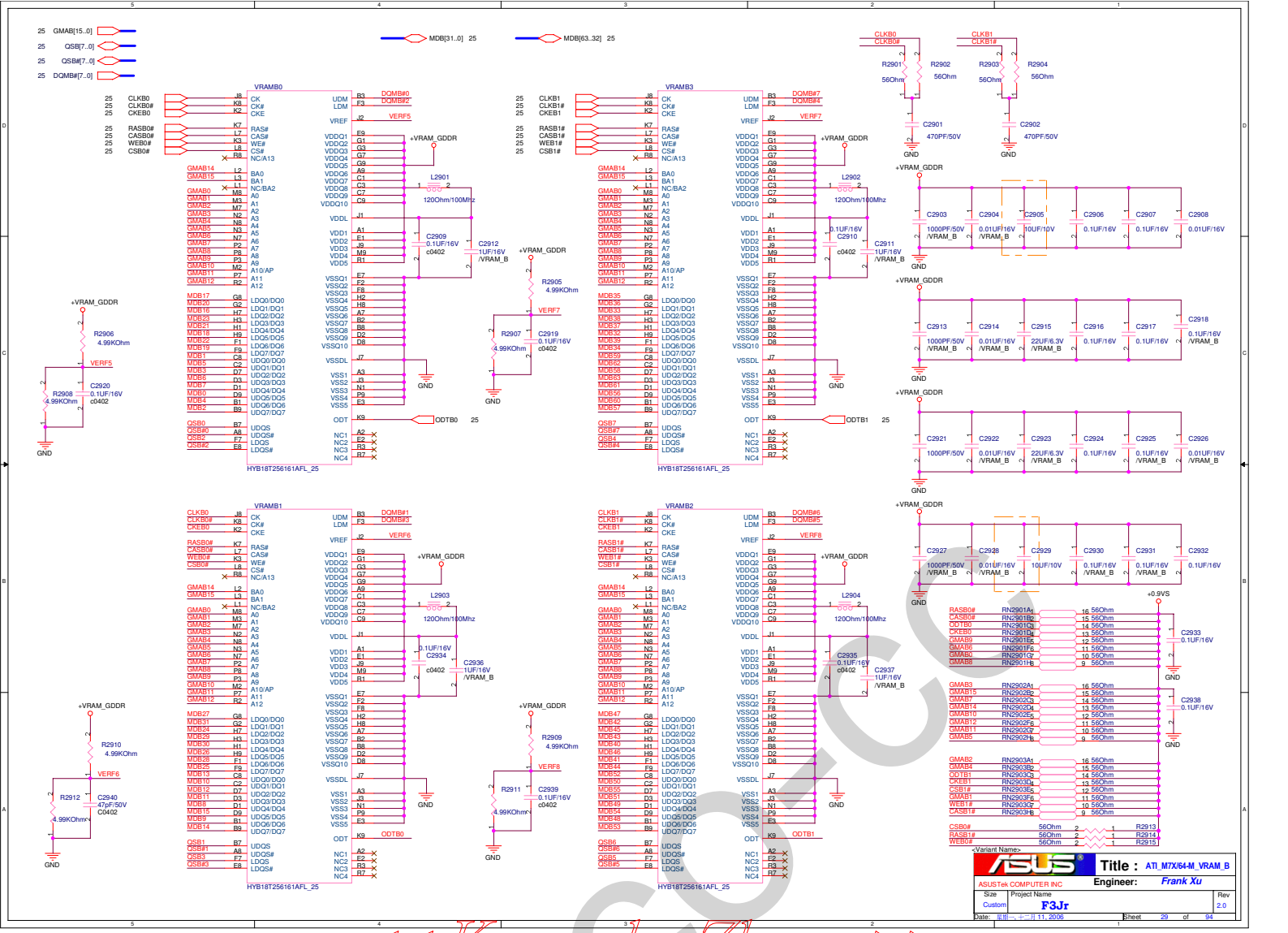


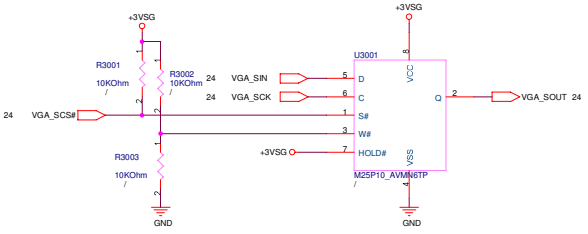












Support HDCP : pull low 10K ohm

<Variant Name>

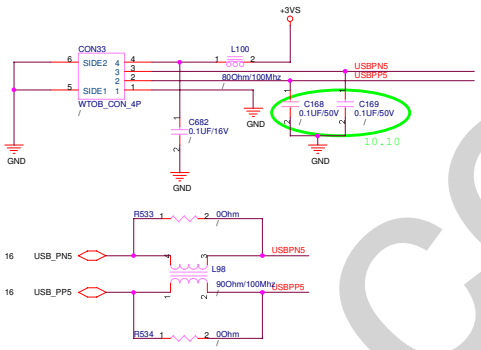
ASUSTeK COMPUTER INC

Title : VGA_SPI_ROM

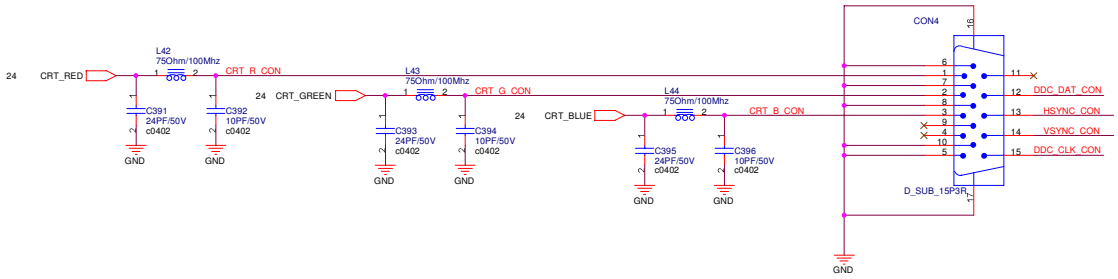
Engineer: Frank Xu

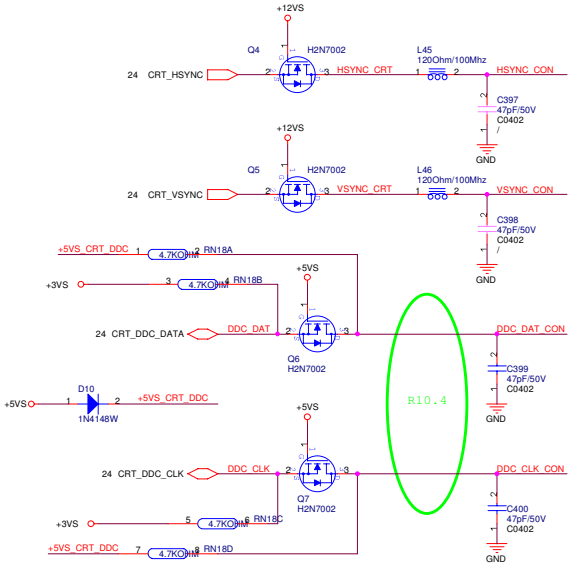
Size	Project Name	Rev
Custom	F3Jr	2.0

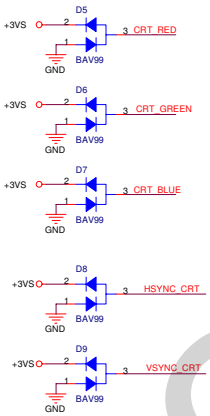
Date: 十月 11, 2006 Sheet 30 of 94



ASUSTeK COMPUTER INC	Title : FINGER PRINT		
	Engineer: Frank Xu		
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 十一月 11, 2006	Sheet 31 of 94		







PLACE ESD Diodes near VGA port

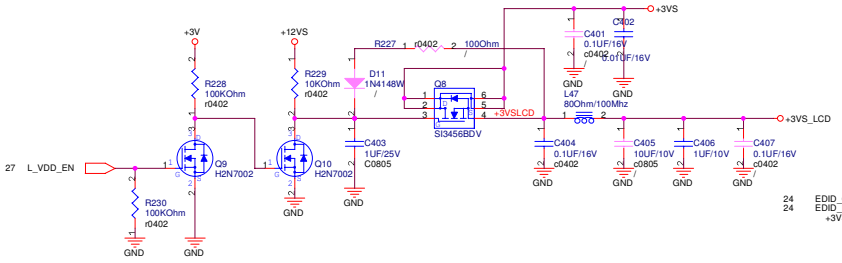
ASUSTeK COMPUTER INC	Title : CRT		
	Engineer: Frank Xu		
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 星期一, 十二月 11, 2006	Sheet 32 of 94		

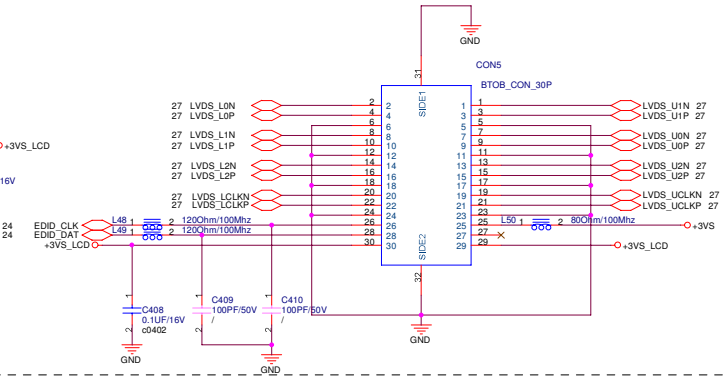
LCD Backlight Control

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD LVDS Interface

LCD Power

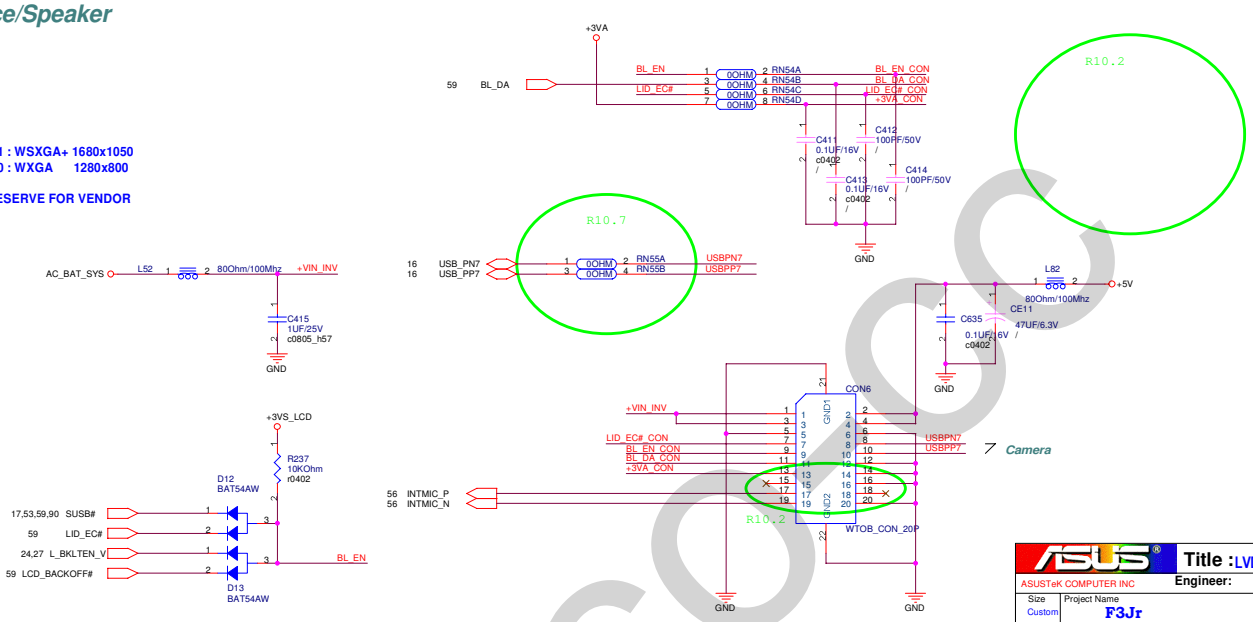




INVERTER Interface/Speaker CONN.

PANEL ID1 = 1 : WSXGA+ 1680x1050
PANEL ID1 = 0 : WXGA 1280x800

PANEL ID0 RESERVE FOR VENDOR



ASUSTeK COMPUTER INC	Title : LVDS & INVERTER		
	Engineer: Frank Xu		
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 星期一, 十二月 11, 2006	Sheet 33 of 94		

ASUSTeK COMPUTER INC

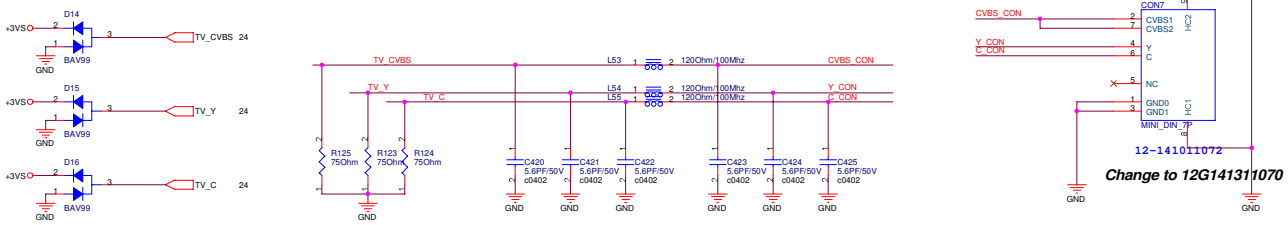
Title : Schematic page name

Engineer: Frank Xu

Size	Project Name	Rev
Custom	F3Jr	2.0

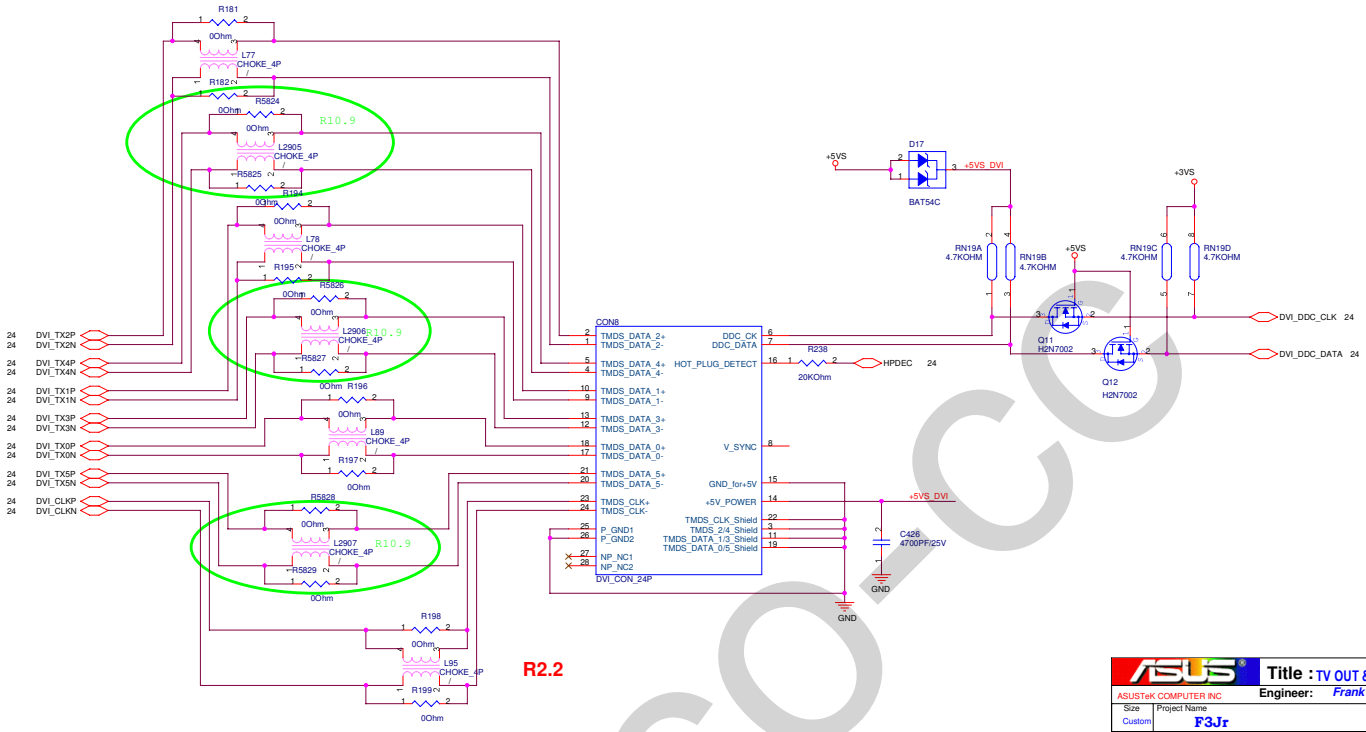
Date: 十月 11, 2006 Sheet 34 of 94

TV OUT



PLACE ESD
Diodes near
TV port

DVI



R2.2

ASUSTeK COMPUTER INC		Title : TV OUT & DVI CON.	
		Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 十一月 11, 2006		Sheet 35 of 94	

ASUSTeK COMPUTER INC

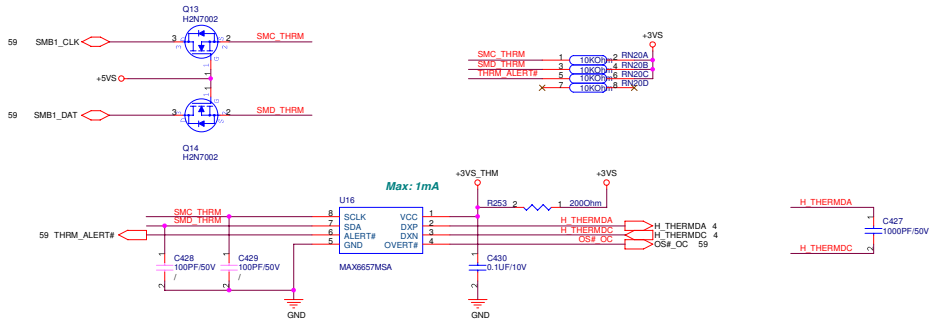
Title : Schematic page name

Engineer: Frank Xu

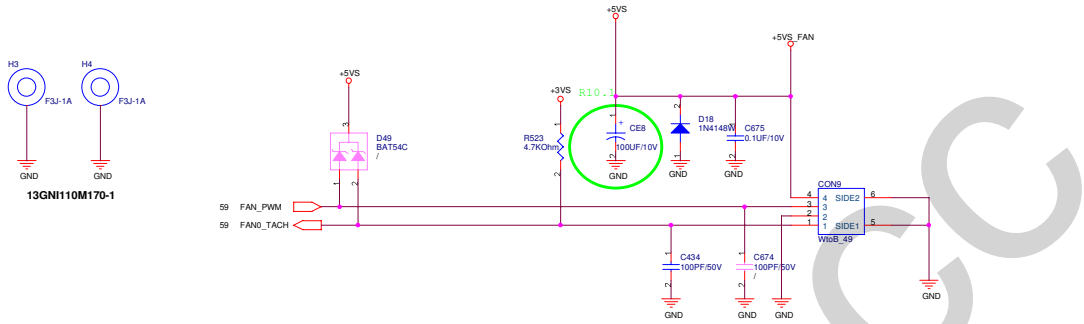
Size	Project Name	Rev
Custom	F3Jr	2.0

Date: 十月 11, 2006 Sheet 36 of 94

Thermal Sensor



DC FAN Control



ASUSTeK COMPUTER INC. NB1	Title : THER SENSOR & FAN	
	Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 十月 11, 2006	Sheet 37 of 94	

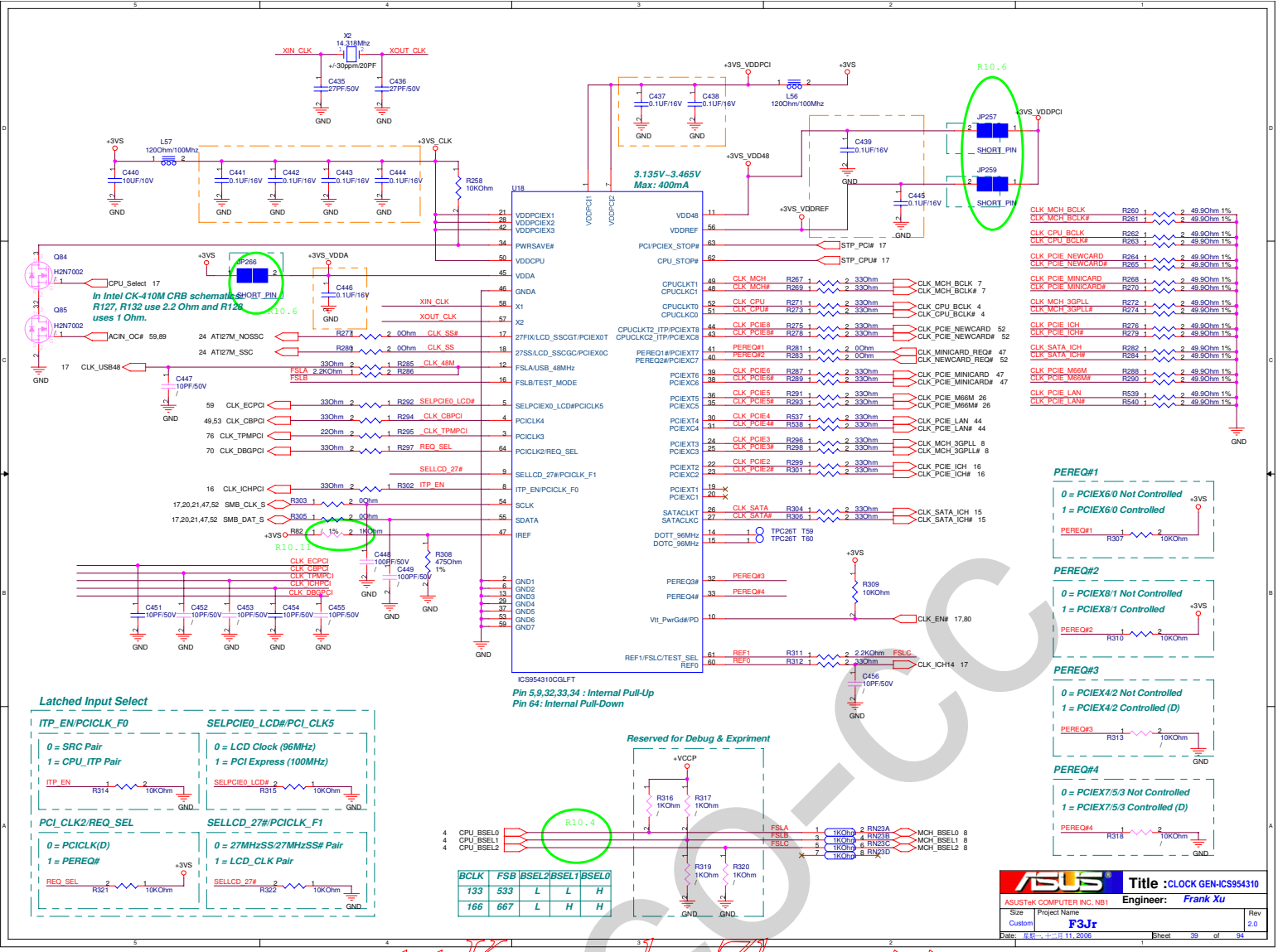
ASUSTeK COMPUTER INC

Title : Schematic page name

Engineer: Frank Xu

Size	Project Name	Rev
Custom	F3Jr	2.0

Date: 十月 11, 2006 Sheet 38 of 94



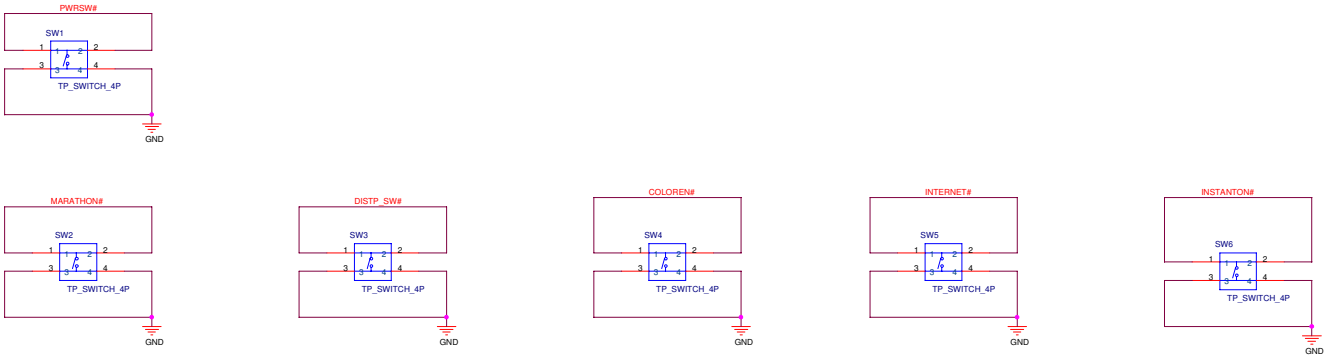
ASUSTeK COMPUTER INC

Title : Schematic page name

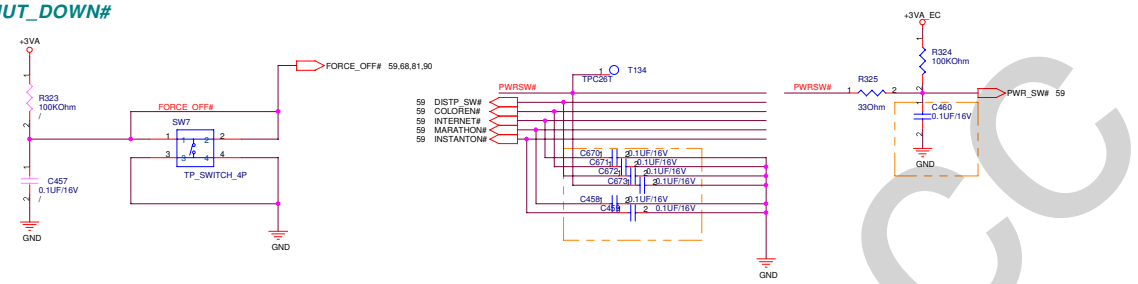
Engineer: Frank Xu

Size	Project Name	Rev
Custom	F3Jr	2.0

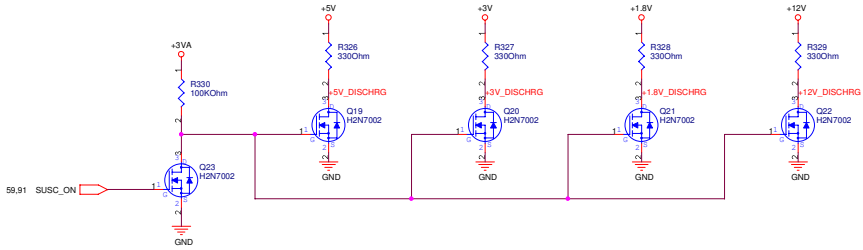
Date: 十月 11, 2006 Sheet 40 of 94

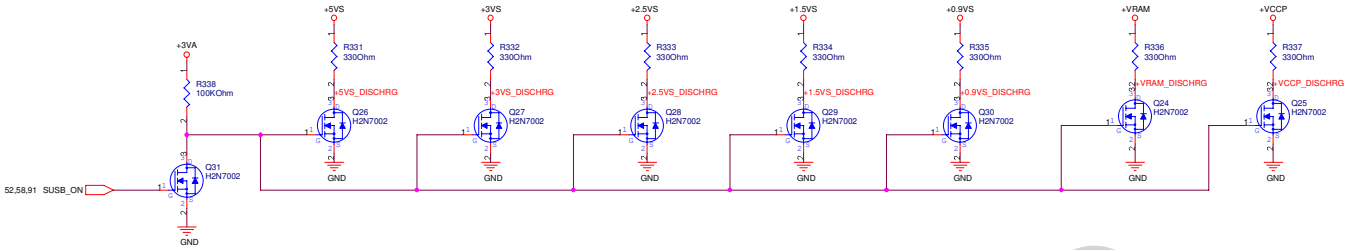


SHUT_DOWN#



ASUSTeK COMPUTER INC	Title : Power on & Res Freq	
	Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 十二月 11, 2006	Sheet 41 of 94	





ASUSTeK COMPUTER INC. NB1

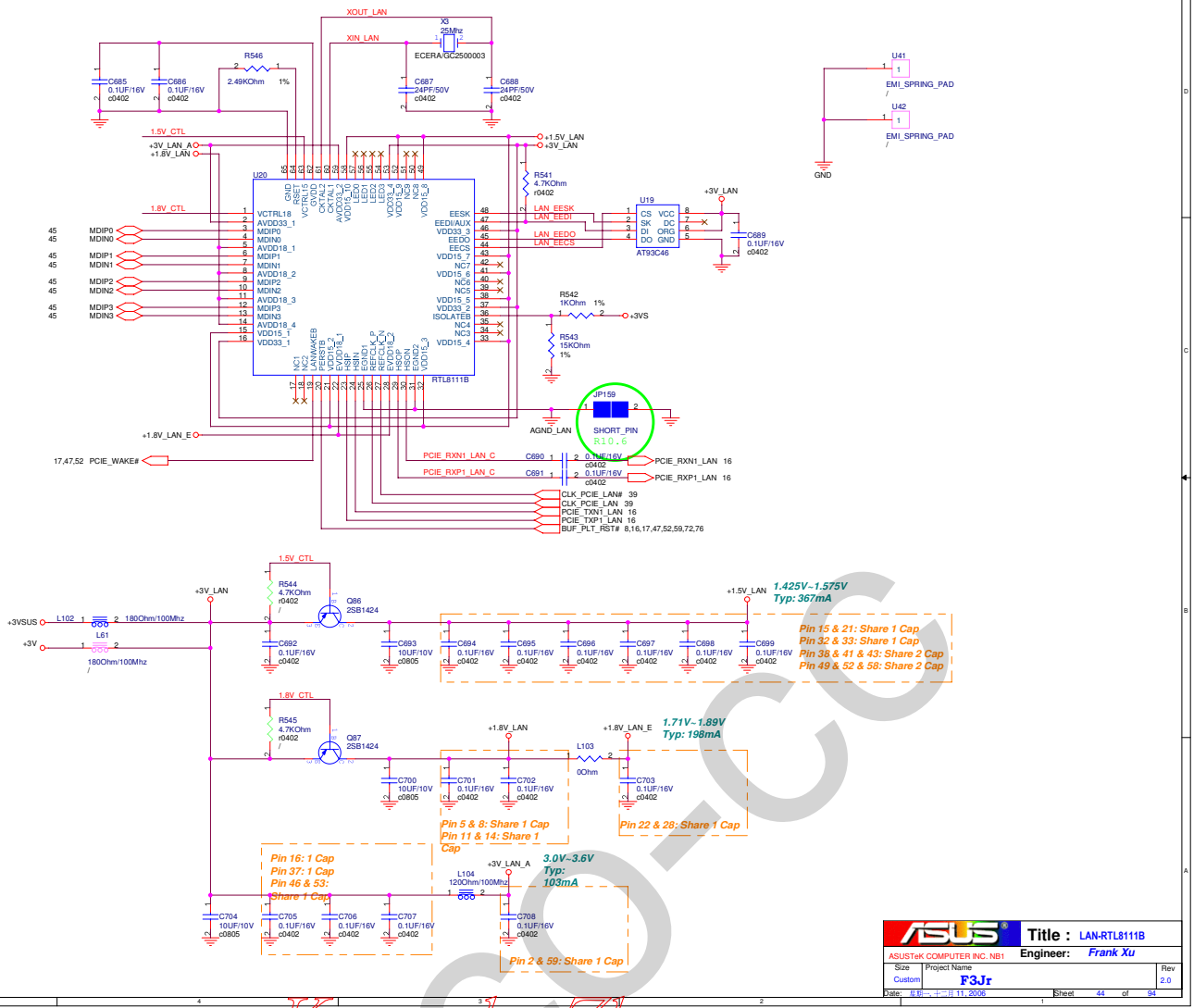
Title : DISCHARGE & EMI CAP

Engineer: Frank Xu

Size	Project Name	Rev
Custom	F3Jr	2.0

Date: 五月 11, 2006 Sheet 42 of 94

ASUSTeK COMPUTER INC	Title : Schematic page name		
	Engineer: Frank Xu		
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 十月 11, 2006	Sheet 43 of 94		



ASUSTeK COMPUTER INC. NB1

Title : LAN-RTL8111B

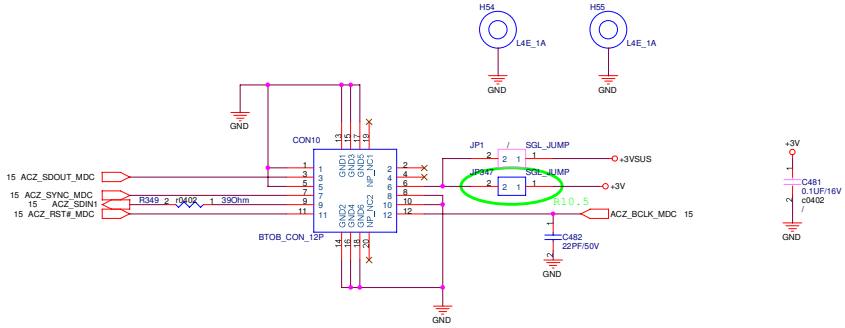
Engineer: Frank Xu

Size	Project Name	Rev
Custom	F3Jr	2.0

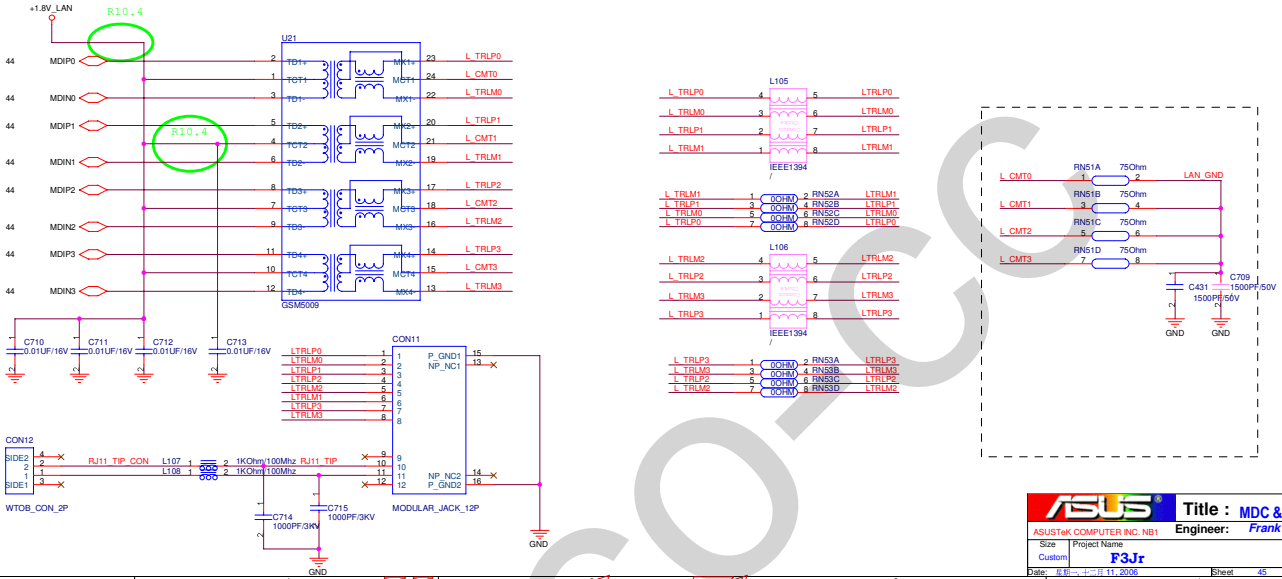
Date: 星期一, 十二月 11, 2006 Sheet 44 of 94

Change to
13GN7510M270

MDC CONN.

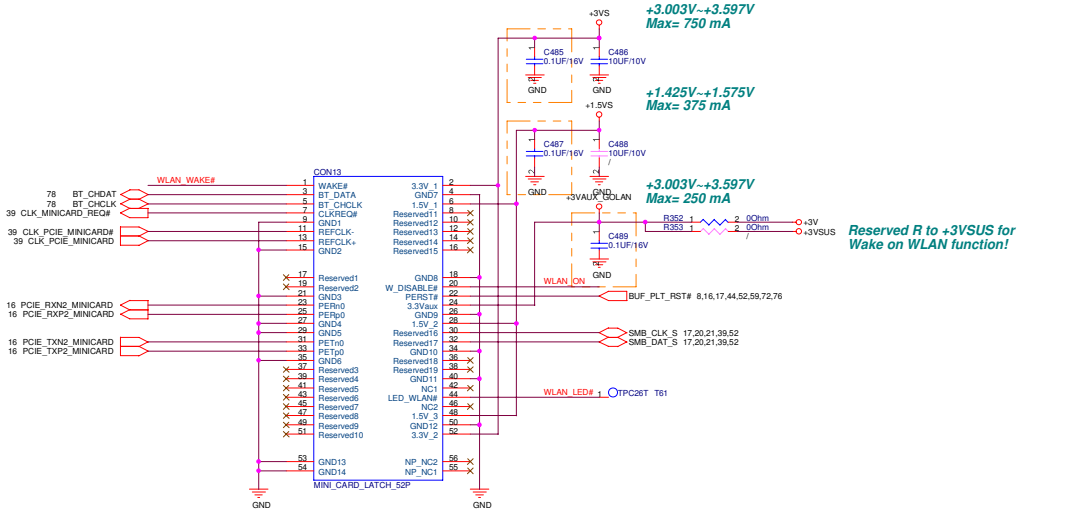


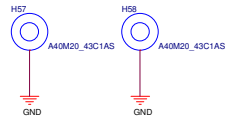
LAN CONN.



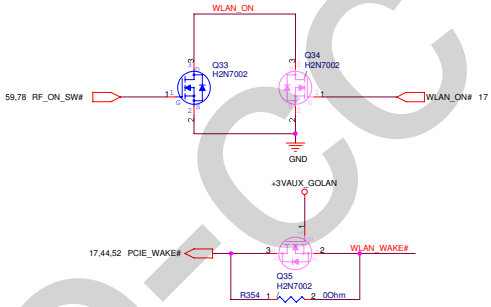
ASUSTeK COMPUTER INC. NB1	Title : MDC & RJ45+11	
	Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 十一月 11, 2006	Sheet 45 of 94	

ASUSTeK COMPUTER INC	Title : Schematic page name	
	Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 十二月 11, 2006	Sheet 46 of 94	





BOM change to 13G021043011



ASUSTeK COMPUTER INC. NB1	Title : MINICARD	
	Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 十一月 11, 2006	Sheet 47 of 94	

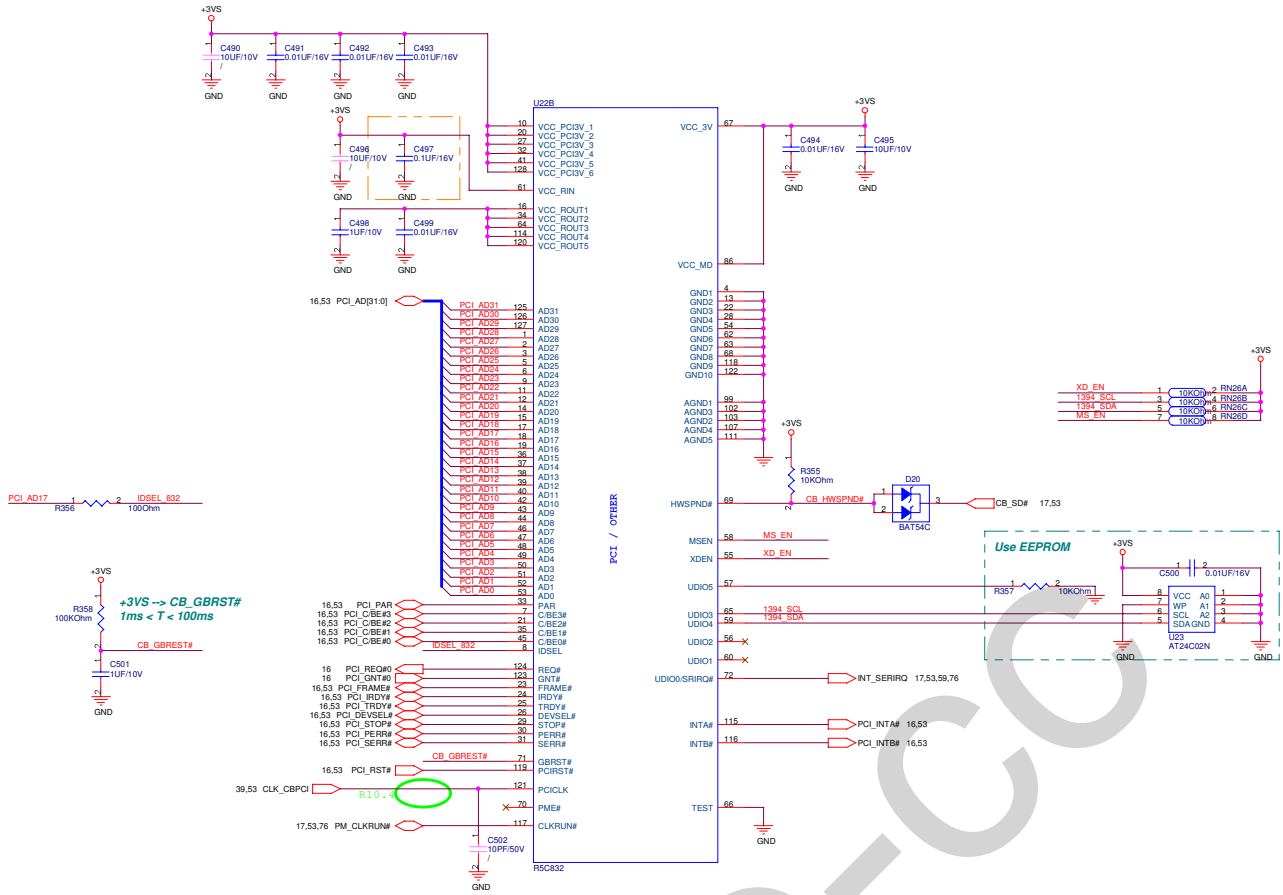
ASUSTeK COMPUTER INC

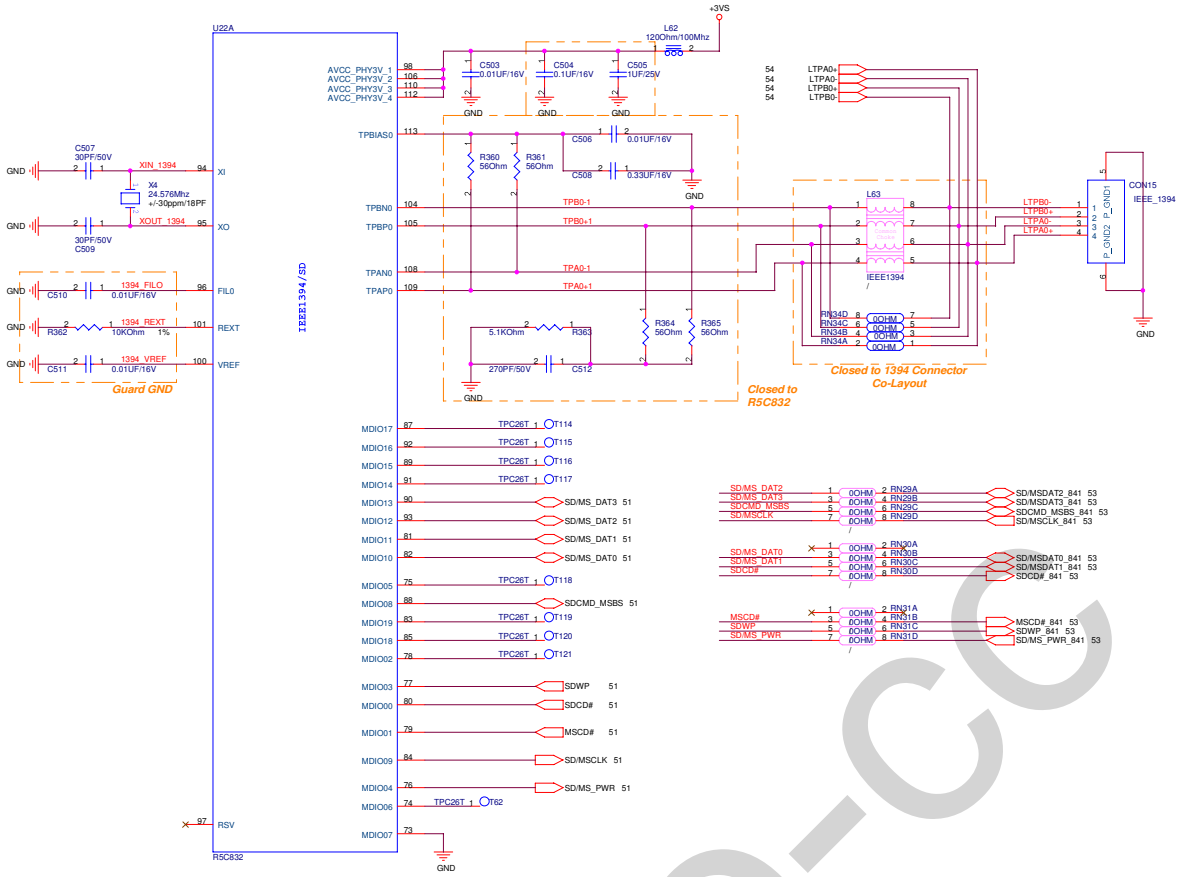
Title : Schematic page name

Engineer: Frank Xu

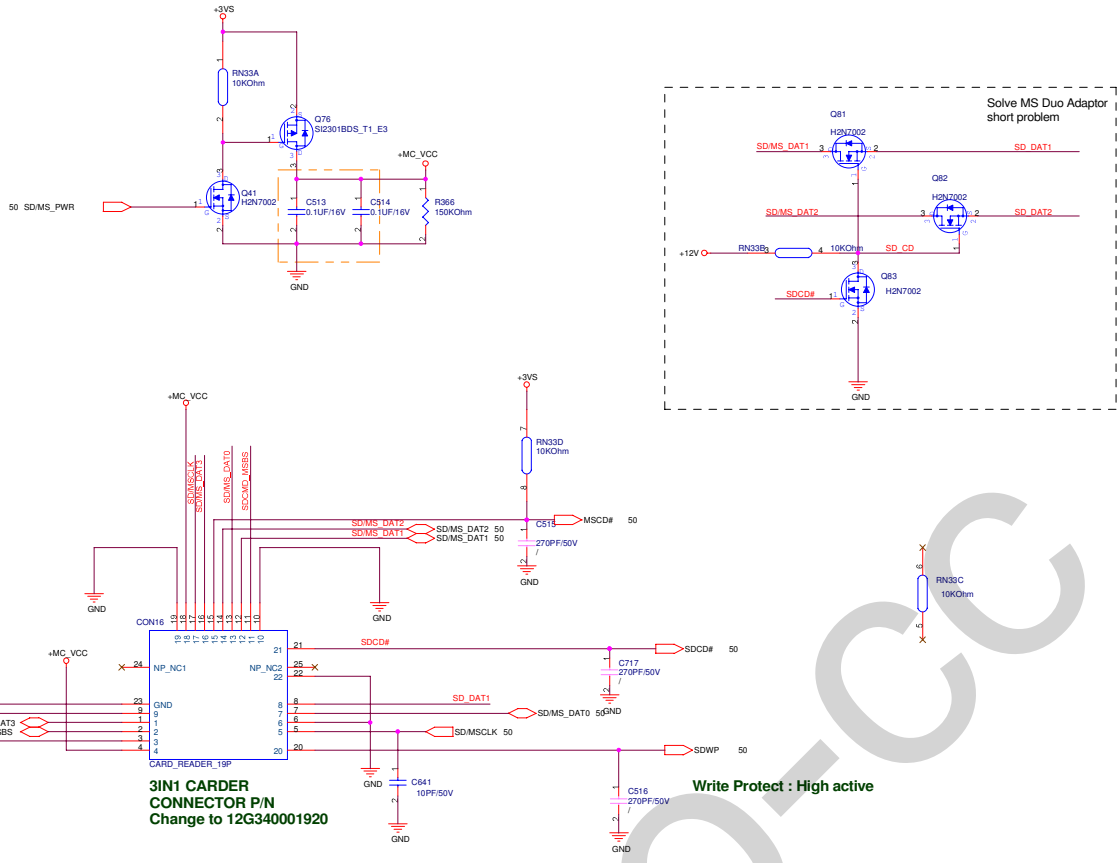
Size	Project Name	Rev
Custom	F3Jr	2.0

Date: 十月 11, 2006 Sheet 48 of 94

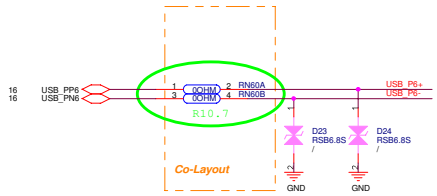


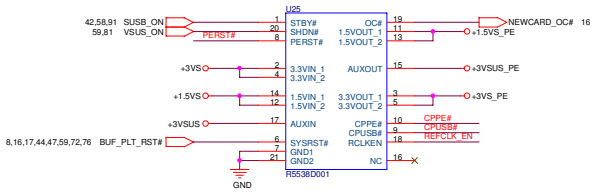


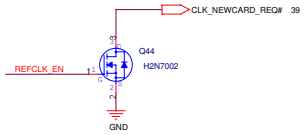
ASUSTeK COMPUTER INC. NB1	Title : CARD1394-R5C832(2)	
	Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 十一月 11, 2006	Sheet 50 of 94	



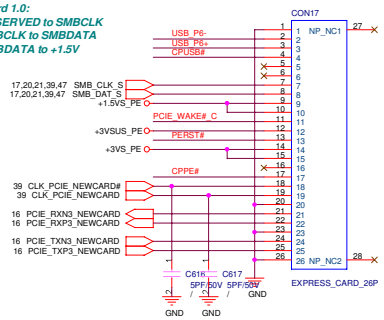
ASUSTeK COMPUTER INC	Title	3 in 1 CARD READER	
	Engineer:	Frank Xu	
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 十一月 11, 2006	Sheet 51 of 94		

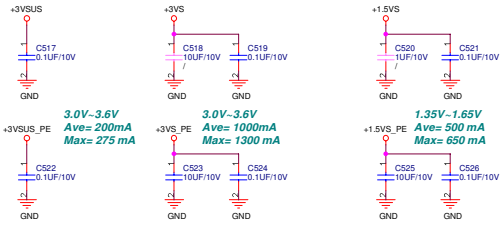


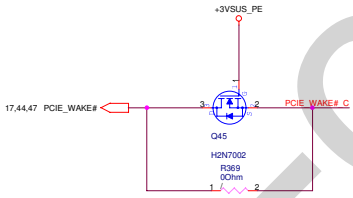




!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

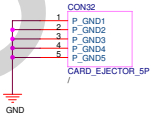




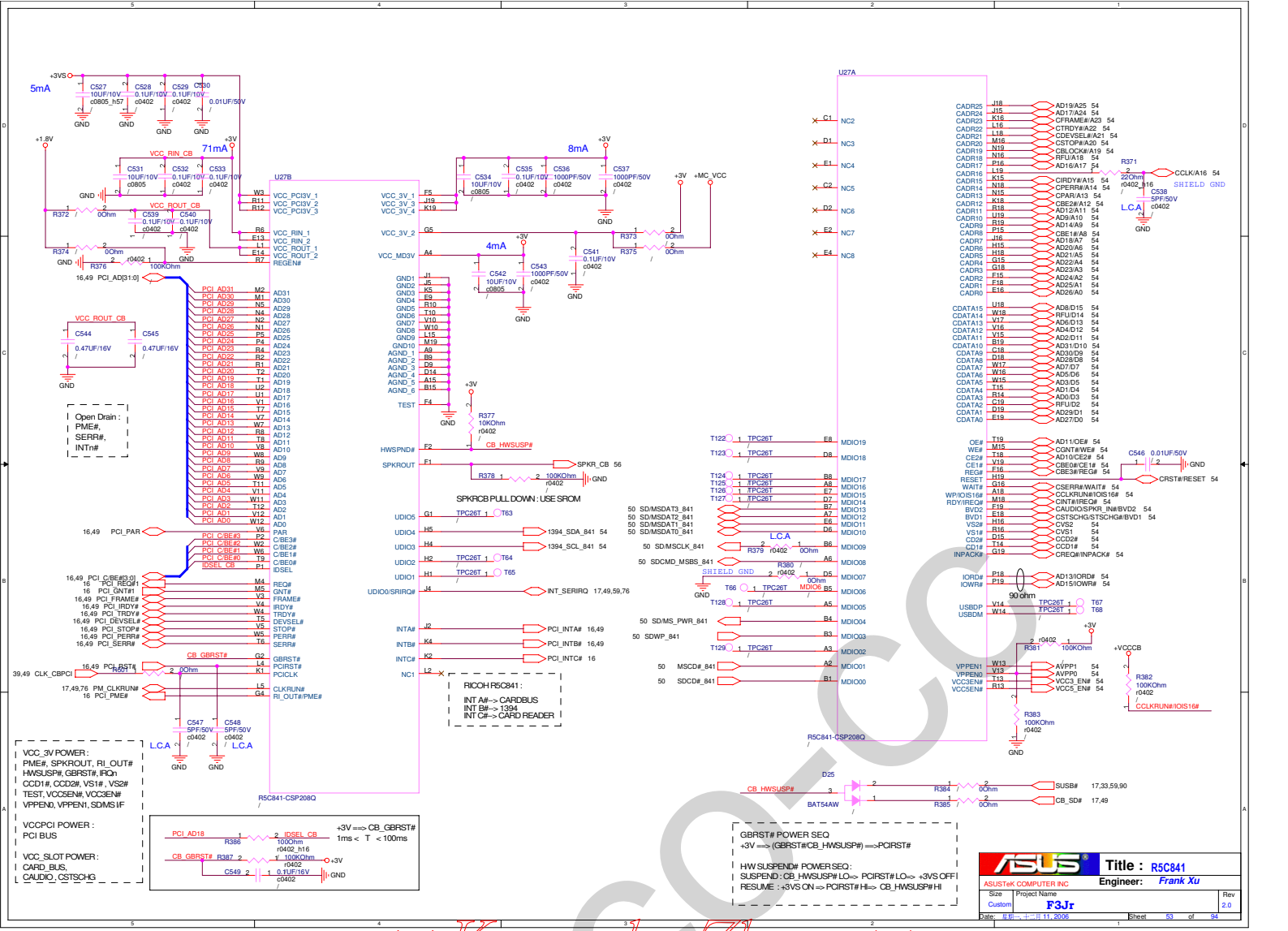


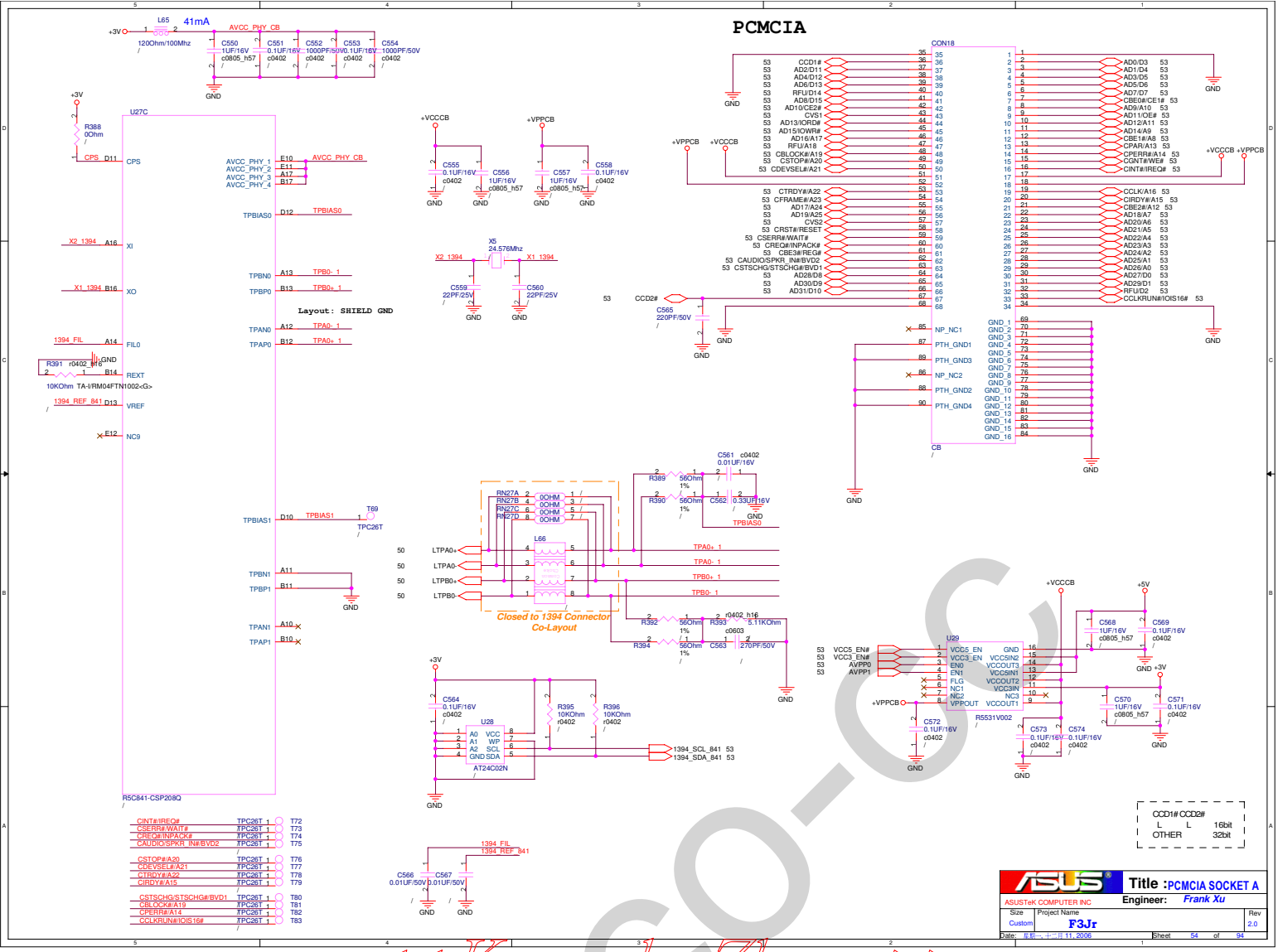
NewCard Header

NewCard Ejecter

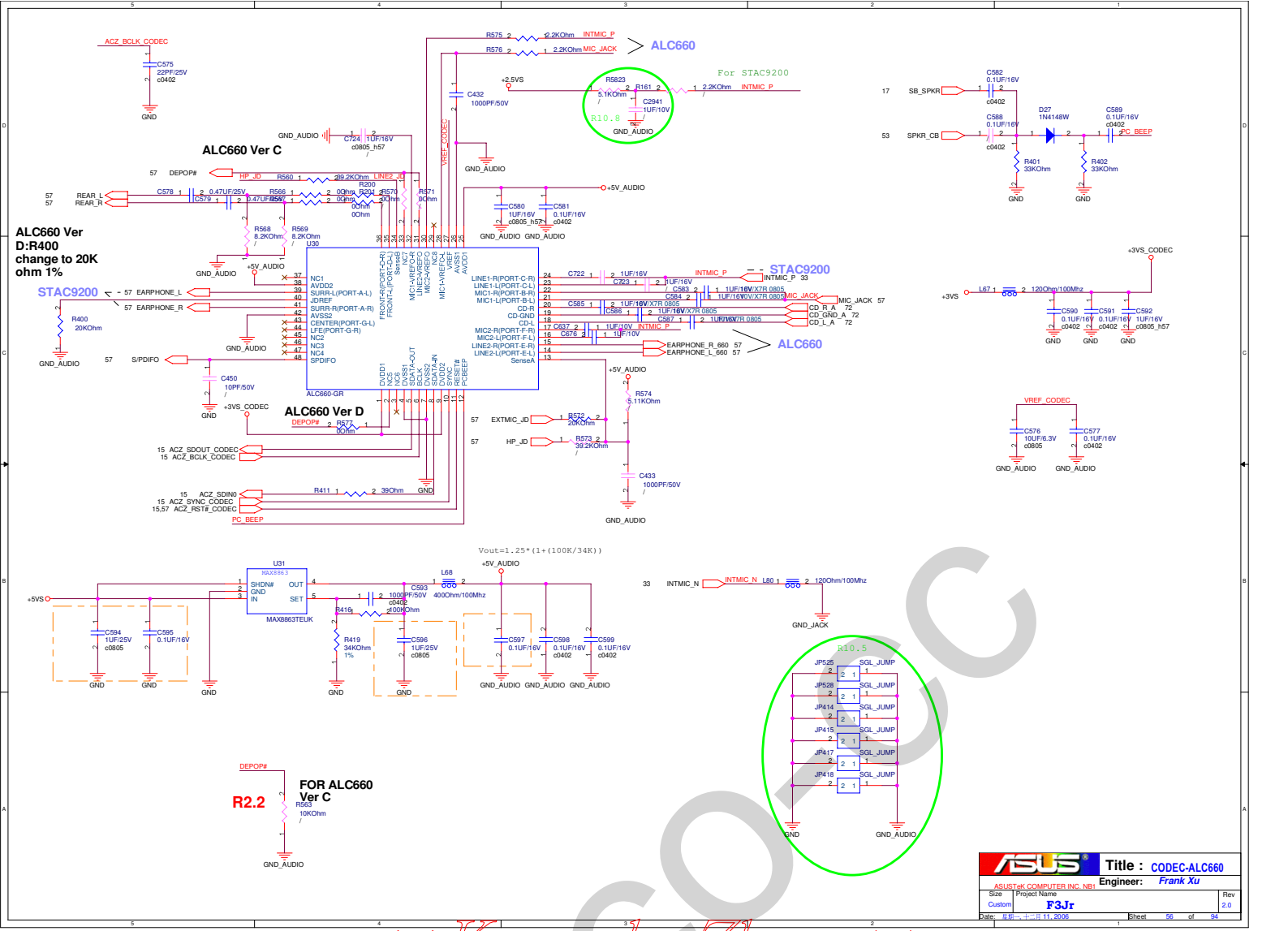


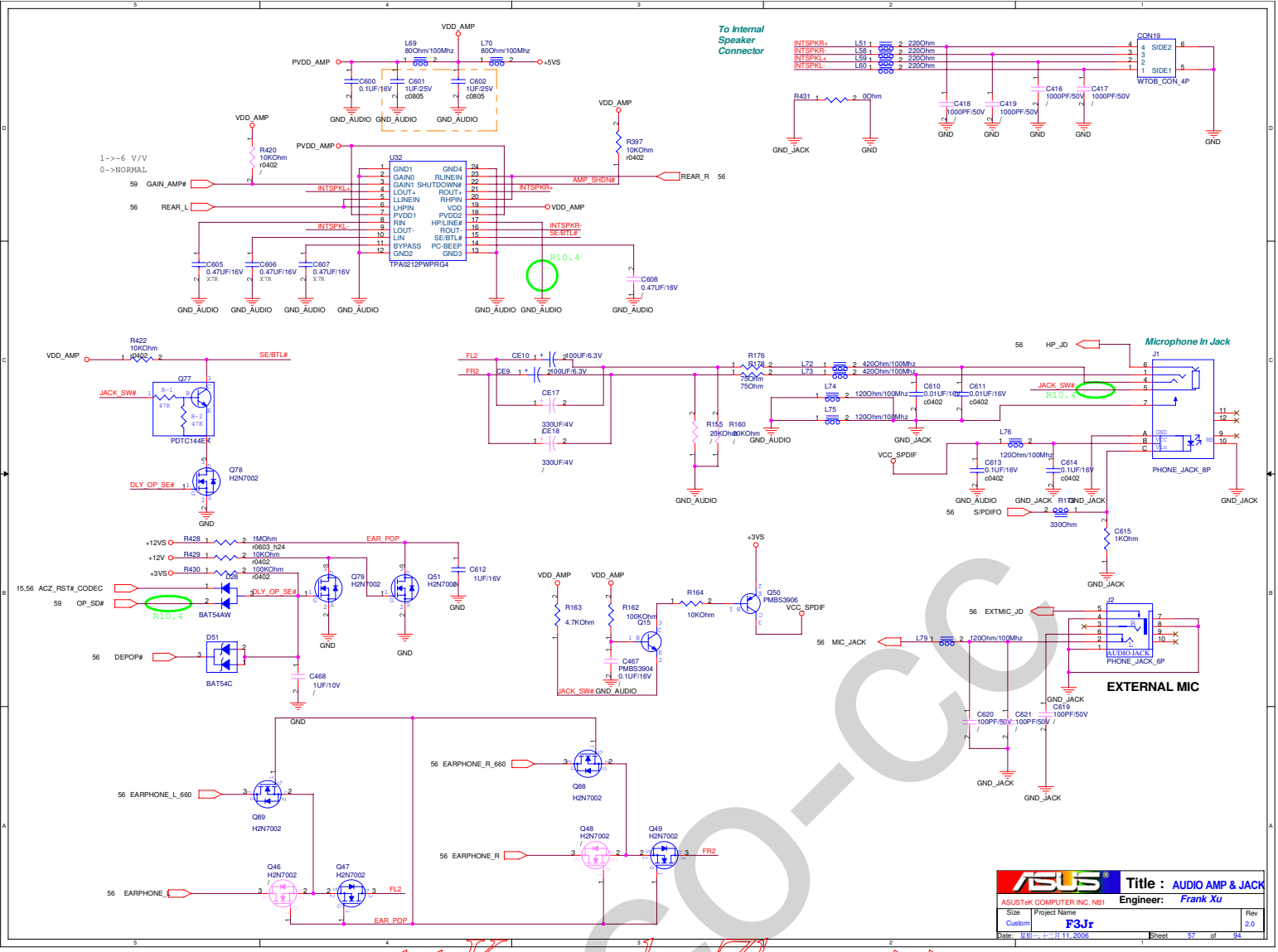
ASUSTeK COMPUTER INC. NB1		Title : NEWCARD	
		Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 日期-, 十二月 11, 2006		Sheet 52 of 94	

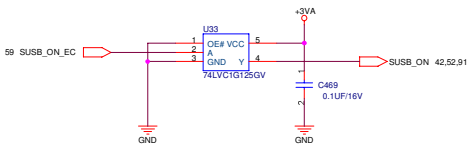




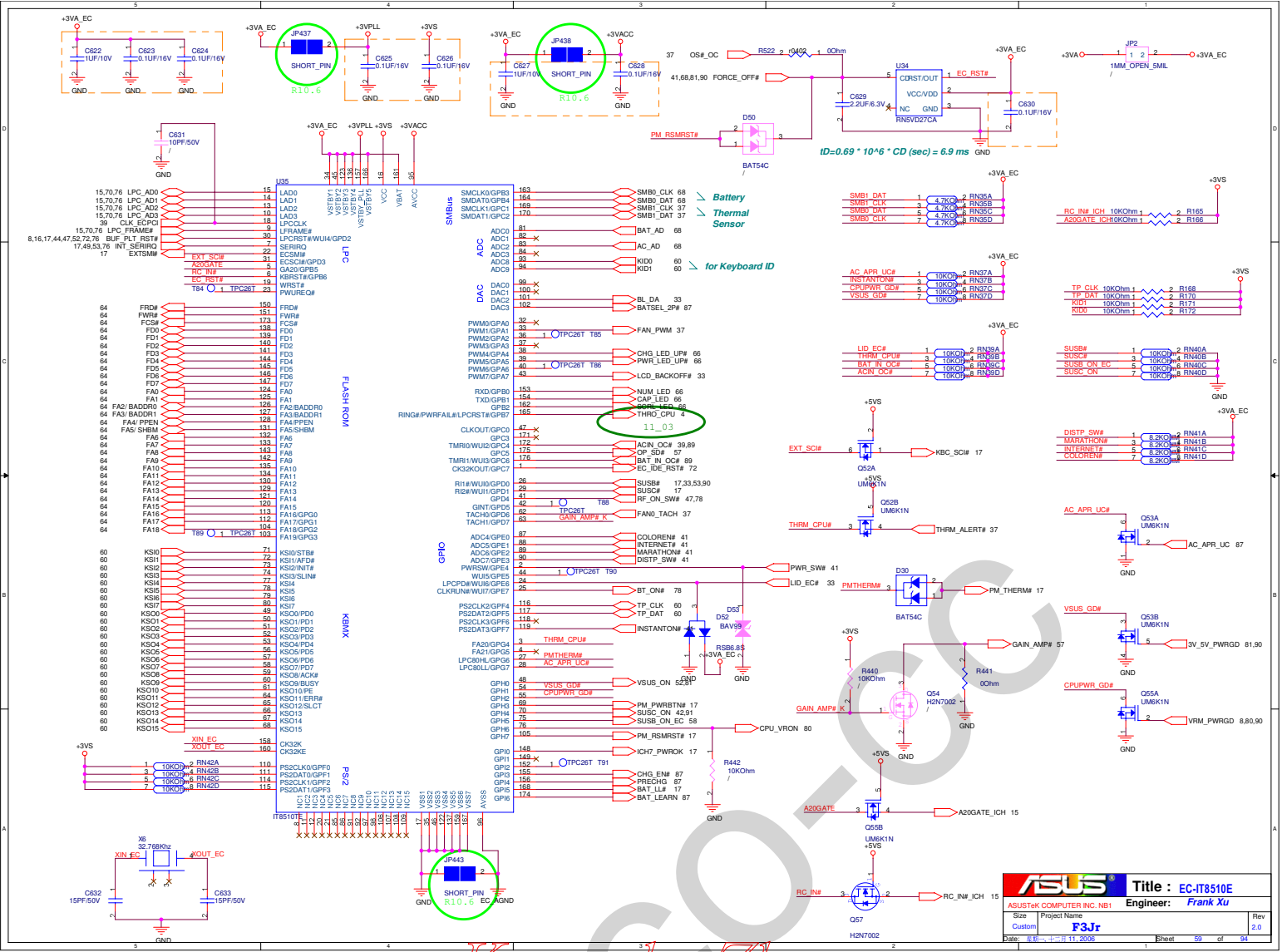
ASUSTeK COMPUTER INC	Title : F3J		
	Engineer: Frank Xu		
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 日期-, 十二月 11, 2006		Sheet 55 of 94	



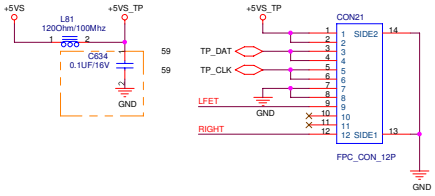


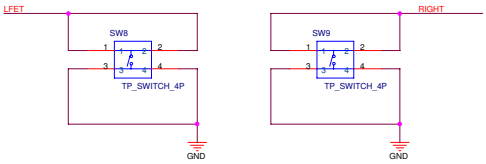


ASUSTeK COMPUTER INC	Title : ON1 & ON2	
	Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 十月 11, 2006	Sheet 58 of 94	

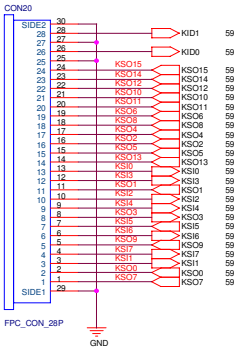


For Touch-Pad



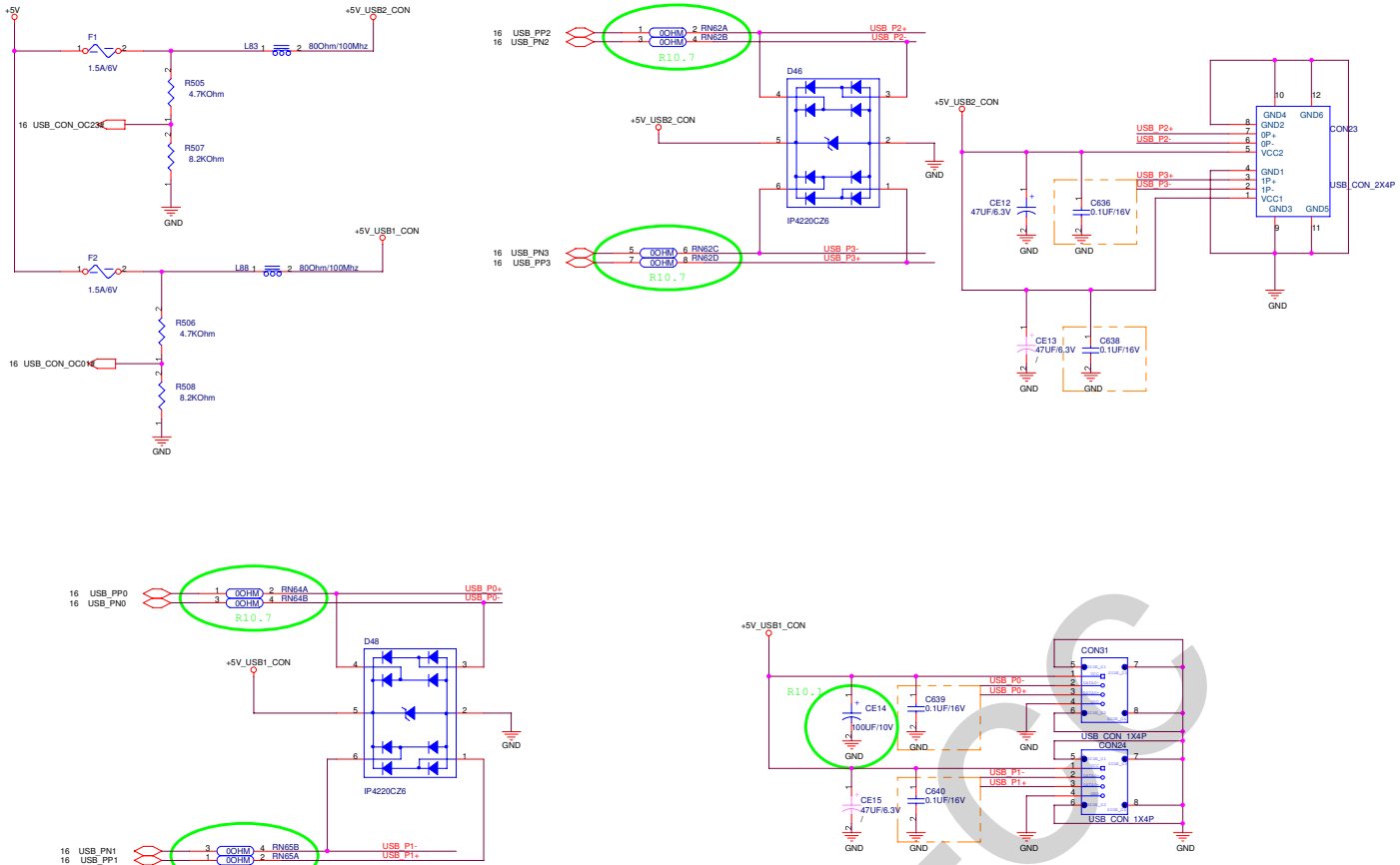


For Keyboard



ASUSTeK COMPUTER INC. NB1	Title : Touch Pad & KB		
	Engineer: Frank Xu		
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 十二月 11, 2006	Sheet 60 of 94		

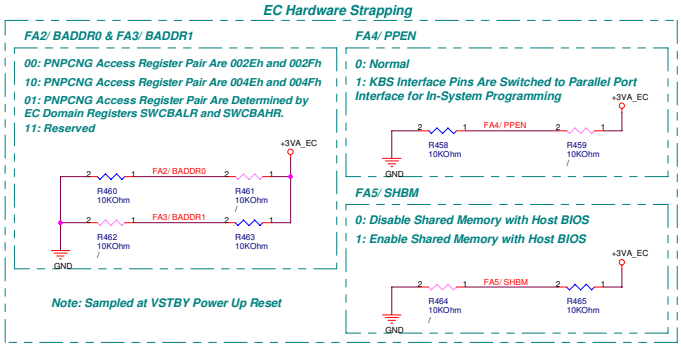
ASUSTeK COMPUTER INC		Title : Schematic page name		
		Engineer: Frank Xu		
Size: Custom	Project Name: F3Jr			Rev: 2.0
Date: 日曜一, 十二月 11, 2006		Sheet 61 of 94		

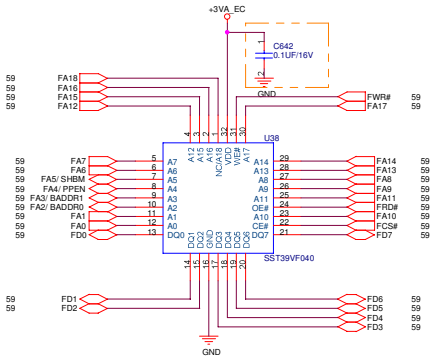


ASUSTeK COMPUTER INC	Title : USB CONN	
	Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 十一月 11, 2006	Sheet 62 of 94	

ASUSTeK COMPUTER INC			Title : Schematic page name	
			Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr			Rev: 2.0
Date: 十月 11, 2006		Sheet 63 of 94		

ISA ROM





ASUSTeK COMPUTER INC. NB1	Title : ISA ROM	
	Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 十一月 11, 2006	Sheet 64 of 94	

ASUSTeK COMPUTER INC

Title : Schematic page name

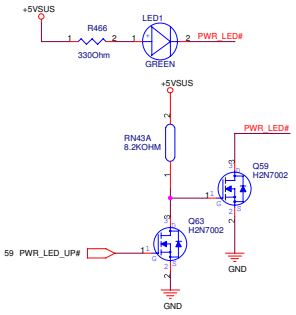
Engineer: Frank Xu

Size	Project Name	Rev
Custom	F3Jr	2.0

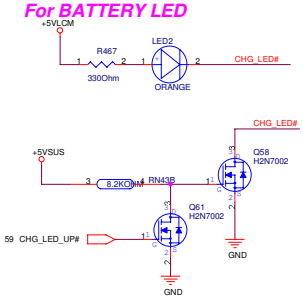
Date: 十二月 11, 2006 Sheet 65 of 94

For LED

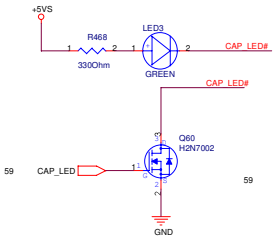
For POWER LED



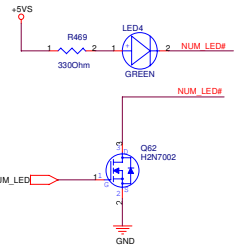
For BATTERY LED



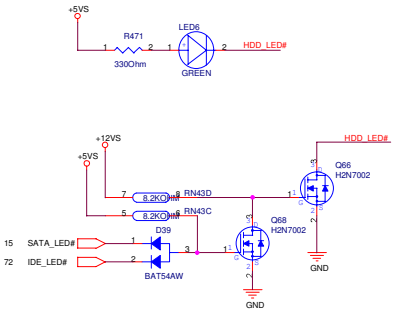
for Cap. Lock



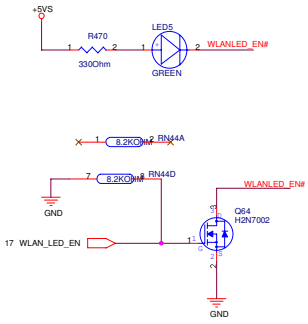
for Num Lock



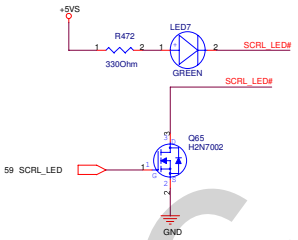
For SATA/IDE LED



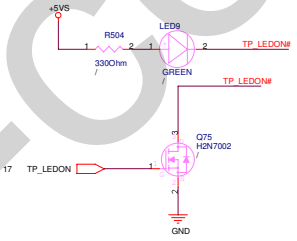
For WireLess LED



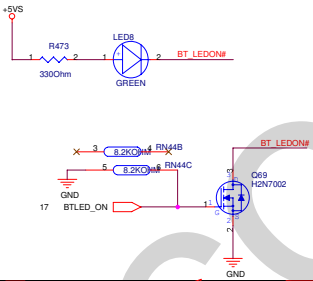
for Scroll Lock



for Touch Pad



For BT LED



ASUSTeK COMPUTER INC	Title : LED	
	Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 十一月 11, 2006	Sheet 66 of 94	

ASUSTeK COMPUTER INC

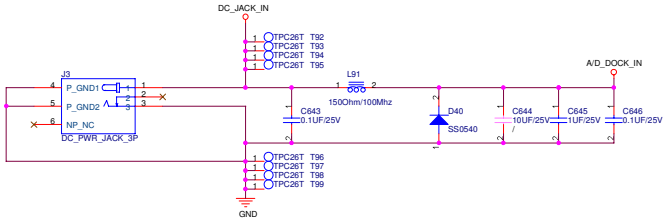
Title : Schematic page name

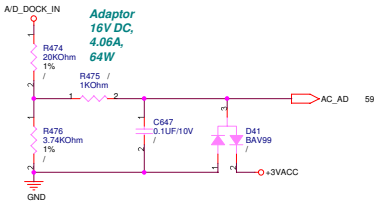
Engineer: Frank Xu

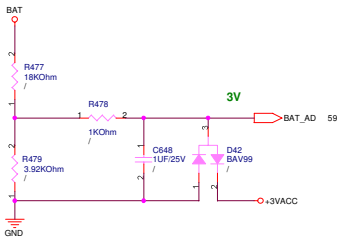
Size	Project Name	Rev
Custom	F3Jr	2.0

Date: 十二月 11, 2006 Sheet 67 of 94

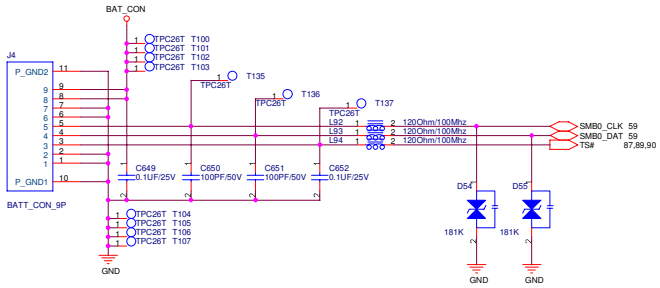
DC IN



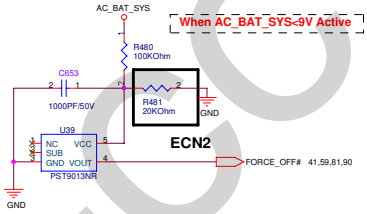




BAT IN



Without Battery & Pull out Adapter



ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN		
	Engineer: Frank Xu		
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 十一月 11, 2006	Sheet 68 of 94		

ASUSTeK COMPUTER INC

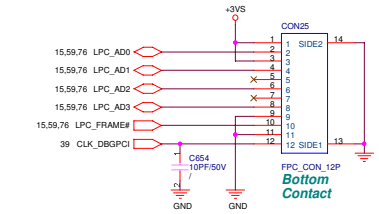
Title : Schematic page name

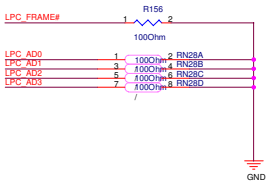
Engineer: Frank Xu

Size	Project Name	Rev
Custom	F3Jr	2.0

Date: 十月 11, 2006 Sheet 69 of 94

For Debug

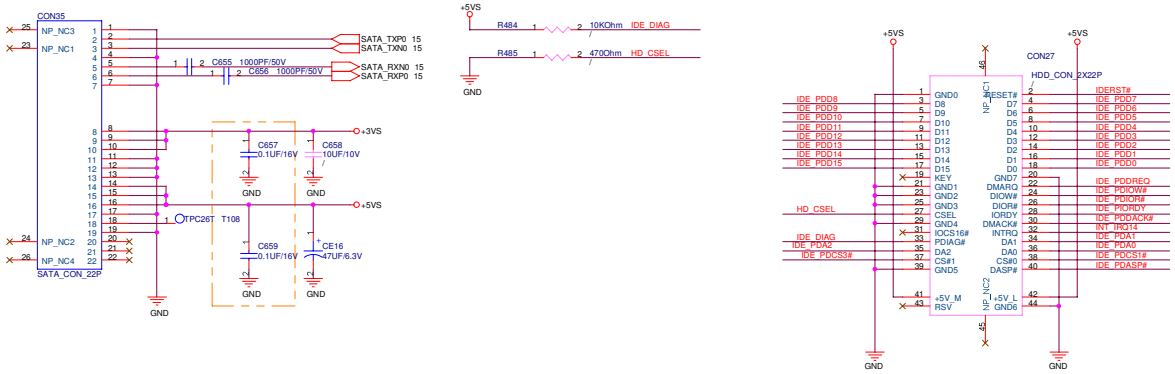




ASUSTeK COMPUTER INC	Title : Debug CONN.		
	Engineer: Frank Xu		
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 十月 11, 2006		Sheet 70 of 94	

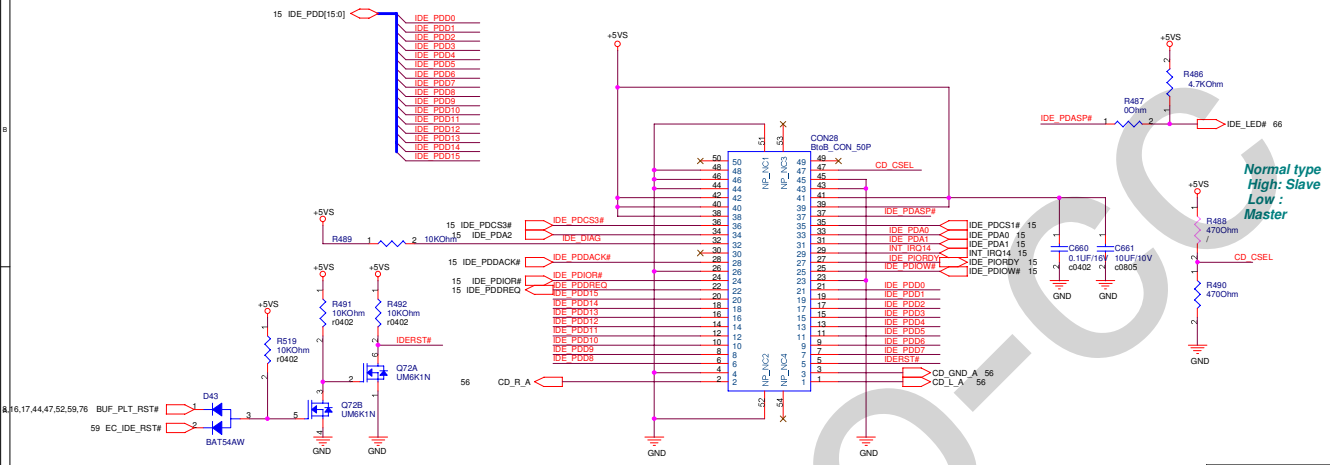
ASUSTeK COMPUTER INC			Title : Schematic page name	
			Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr			Rev: 2.0
Date: 日曜一, 十二月 11, 2006		Sheet 71 of 94		

HD_CSEL : Pull-Down, HDD as Master



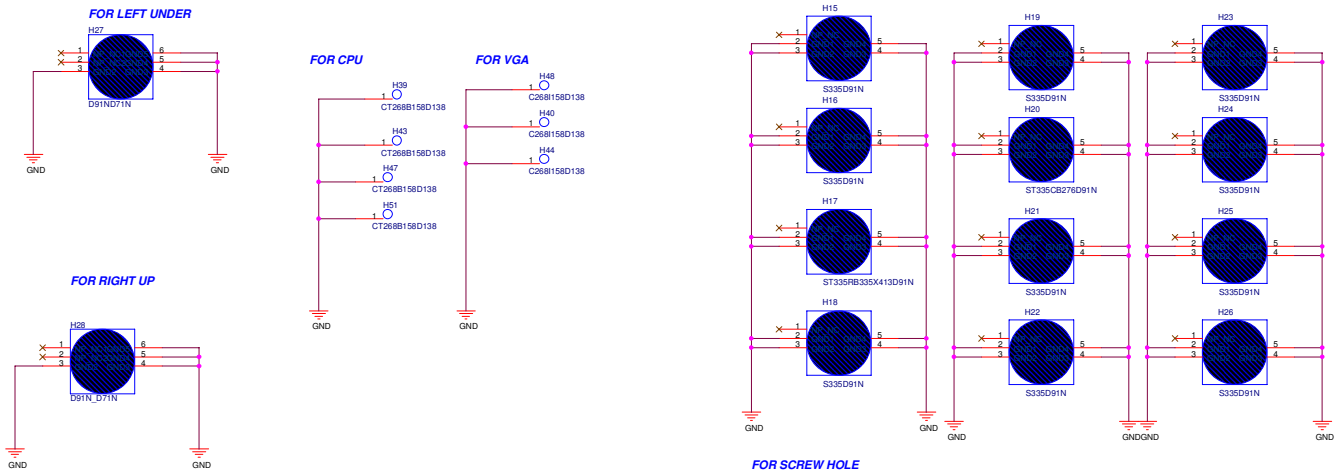
SATA HDD

ODD



ASUSTeK COMPUTER INC. NB1	Title : SATA-HDD & ODD		
	Engineer: Frank Xu		
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 十一月 11, 2006	Sheet 72 of 94		

ASUSTeK COMPUTER INC			Title : Schematic page name	
			Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr			Rev: 2.0
Date: 日期-, 十二月 11, 2006		Sheet 73 of 94		



ASUSTeK COMPUTER INC	Title : SREW HOLE		
	Engineer: Frank Xu		
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 十二月 11, 2006		Sheet 74 of 94	

ASUSTeK COMPUTER INC

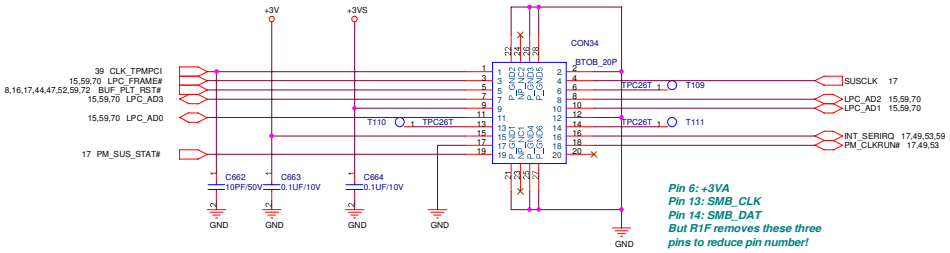
Title : Schematic page name

Engineer: Frank Xu

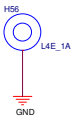
Size	Project Name	Rev
Custom	F3Jr	2.0

Date: 十月 11, 2006 Sheet 75 of 94

For TPM Module



Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

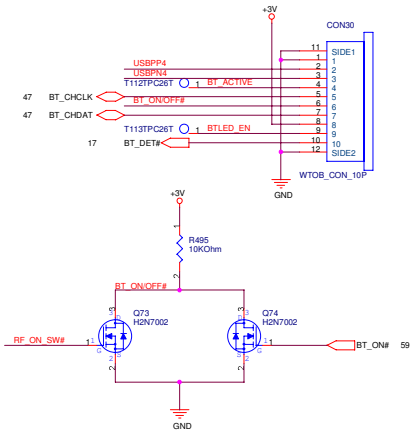


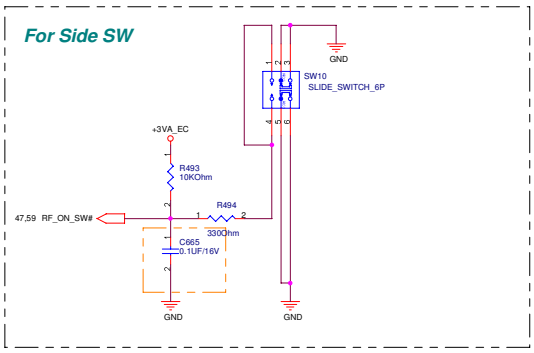
Change to 13GN7510M270-1

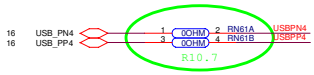
ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: Frank Xu	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 十一月 11, 2006	Sheet 76 of 94	

ASUSTeK COMPUTER INC	Title: Schematic page name		
	Engineer: Frank Xu		
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 日曜一, 十二月 11, 2006	Sheet 77 of 94		

For Bluetooth







ASUSTeK COMPUTER INC	Title : Blue Tooth		
	Engineer: Frank Xu		
Size: Custom	Project Name: F3Jr		Rev: 2.0
Date: 十一月 11, 2006	Sheet 78 of 94		

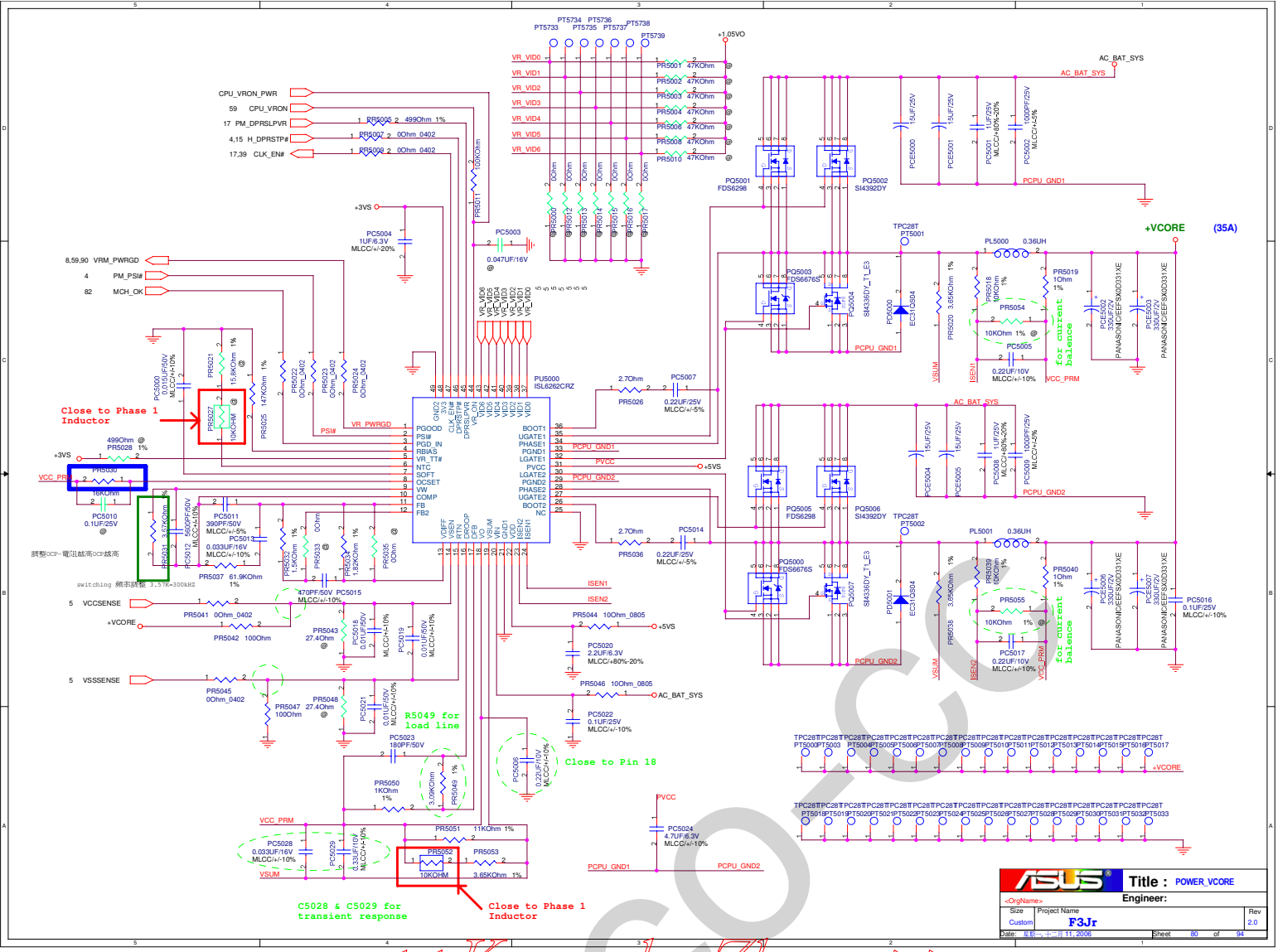
ASUSTeK COMPUTER INC

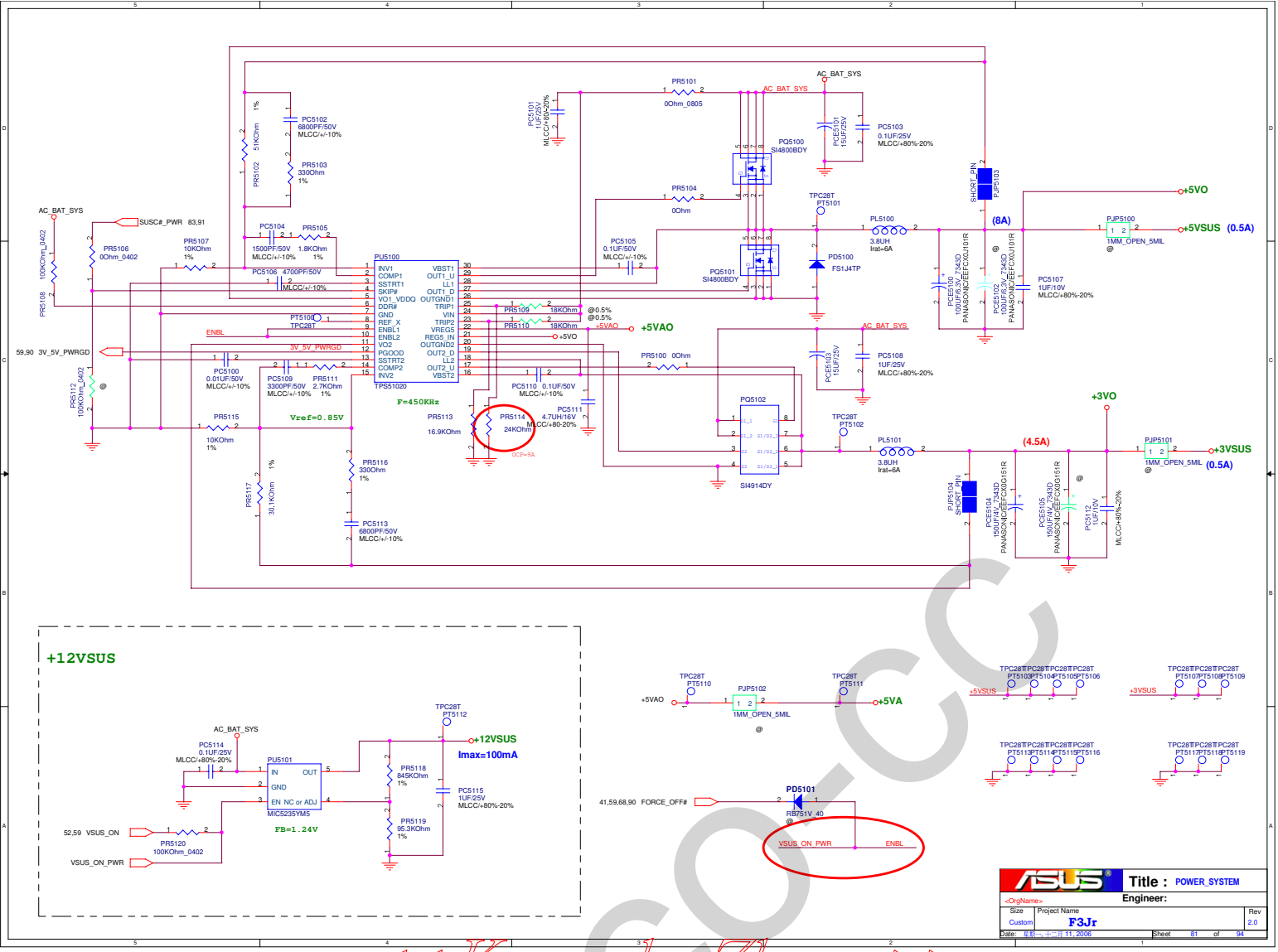
Title : Schematic page name

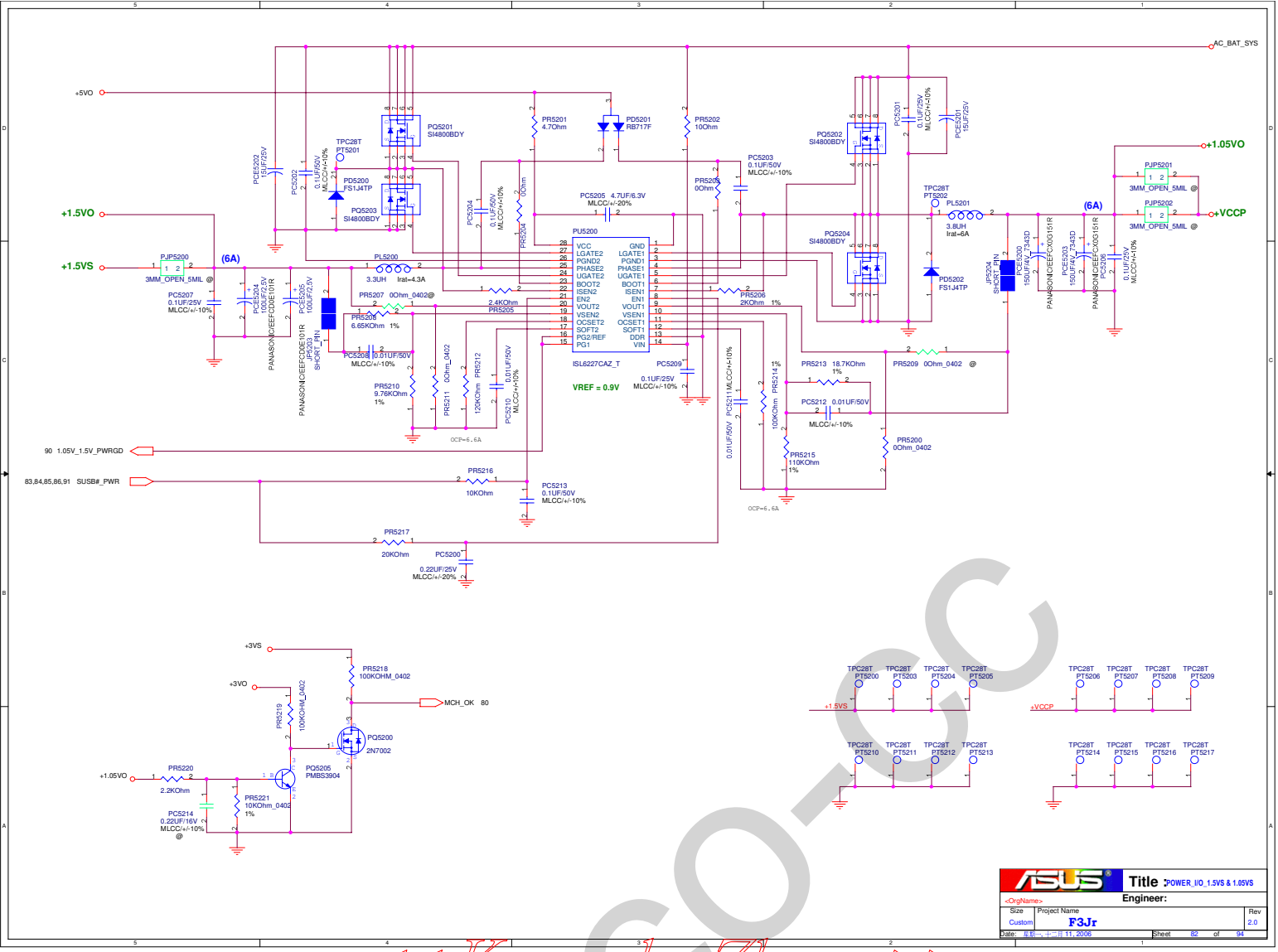
Engineer: Frank Xu

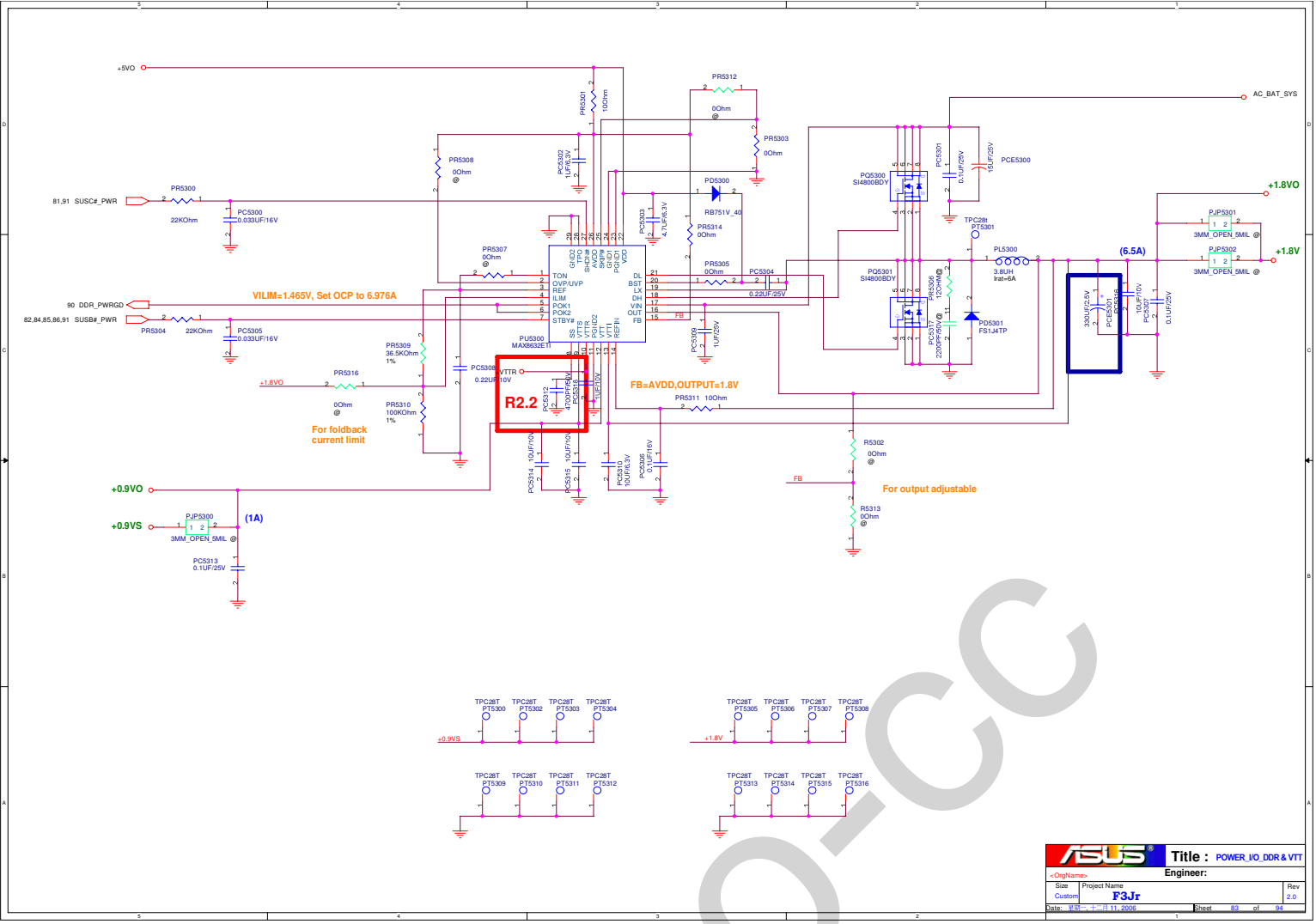
Size	Project Name	Rev
Custom	F3Jr	2.0

Date: 十二月 11, 2006 Sheet 79 of 94



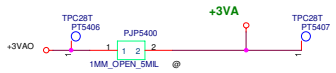


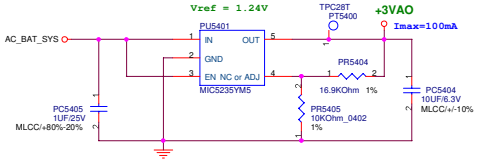




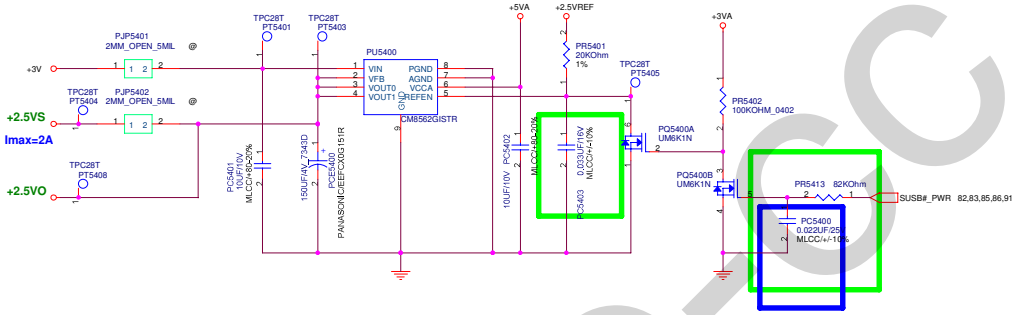
<< Kennedy_Zhang >>

+3VAO

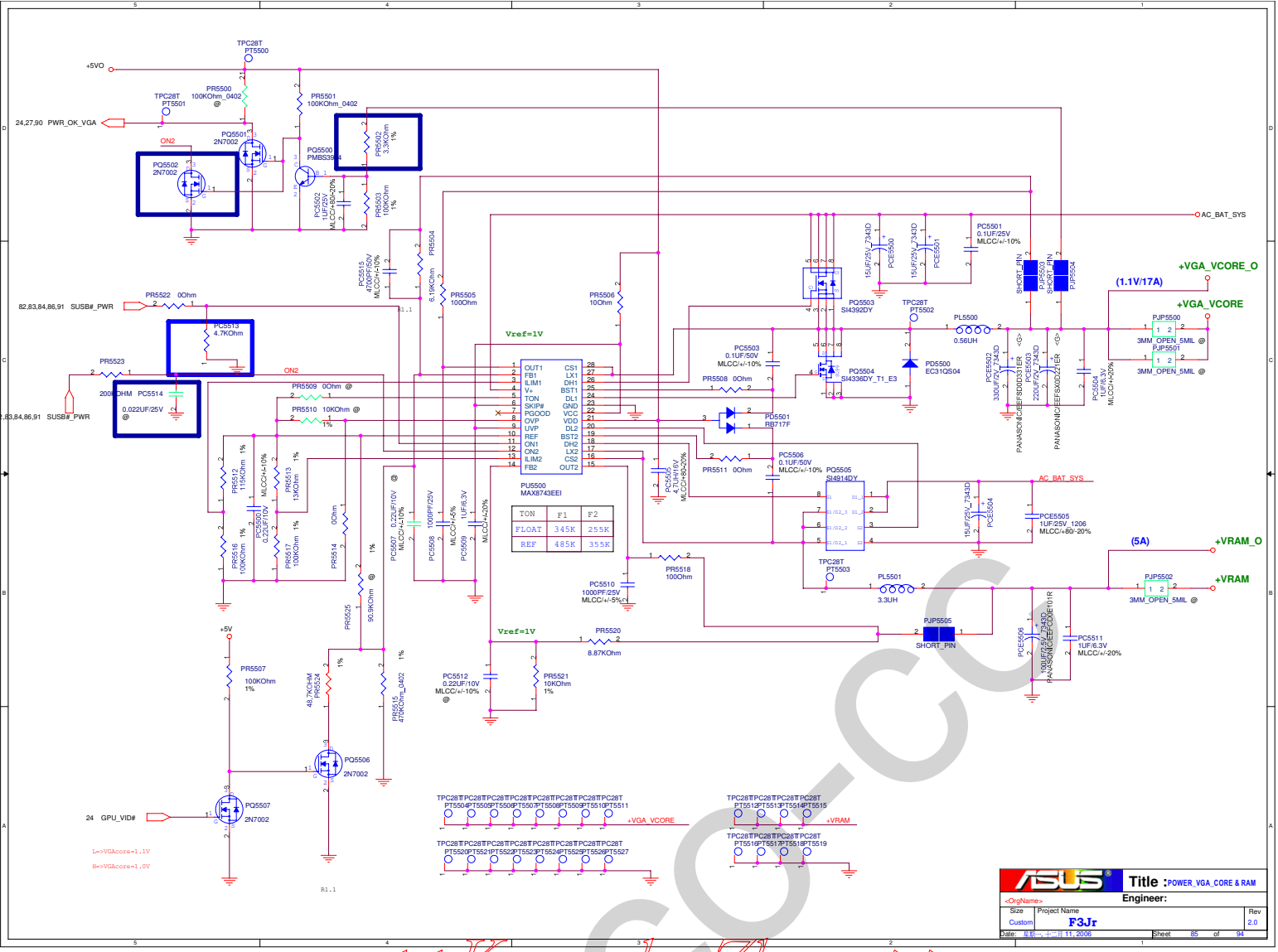




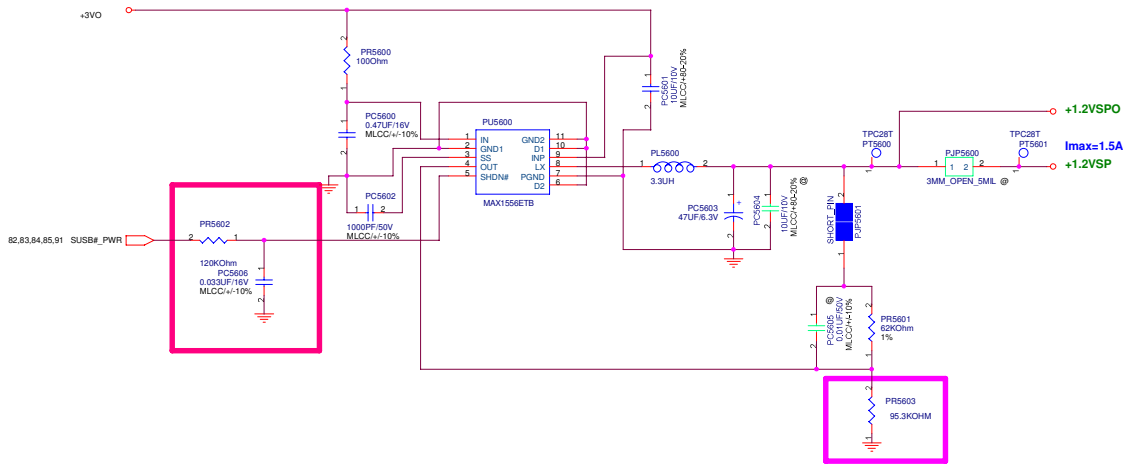
+2.5VS



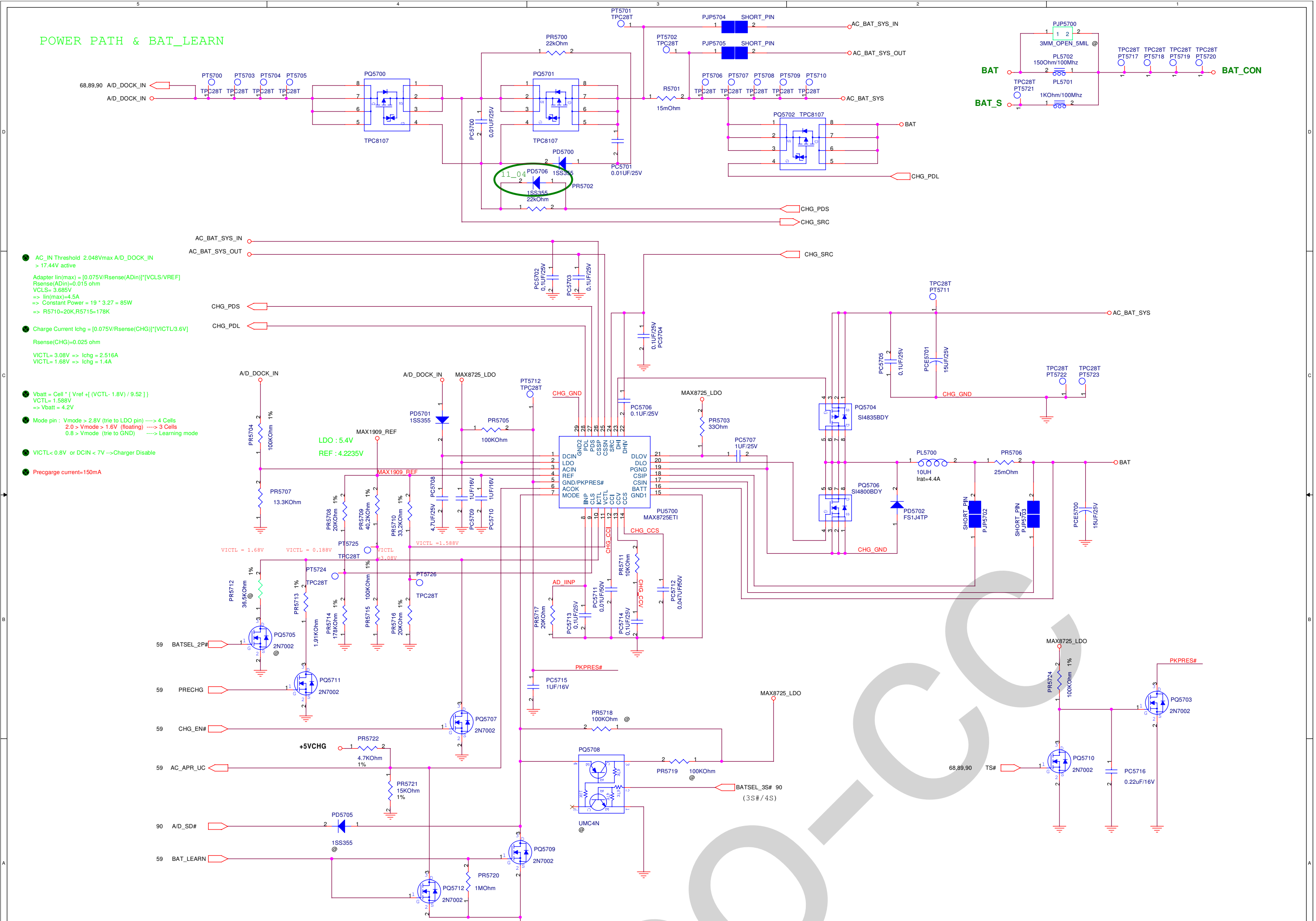
Title : POWER_I/O_+3VA & +2.5V		
<OrgName>	Engineer:	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 星期一, 十一月 11, 2006	Sheet 84 of 94	



+1.2VSP



Title : POWER_VGA_+1.2VSP		
<OrgName>	Engineer:	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 星期一, 十一月 11, 2006	Sheet 86 of 94	



Title : POWER_CHARGER

<OrgName>

Engineer:

Size	Project Name	Rev
C	F3Jr	2.0

Date: 星期一, 十二月 11, 2006 Sheet 87 of 94

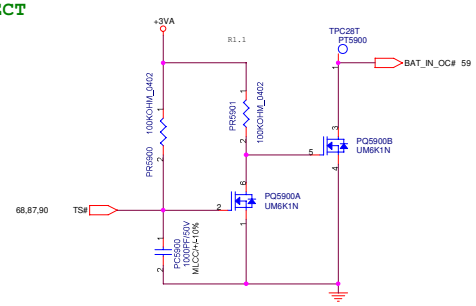
Title : POWER_PIC

<OrgName> Engineer:

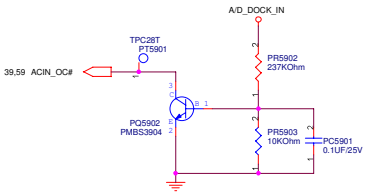
Size	Project Name	Rev
Custom	F3Jr	2.0

Date: 星期一, 十一月 11, 2006 Sheet 88 of 94

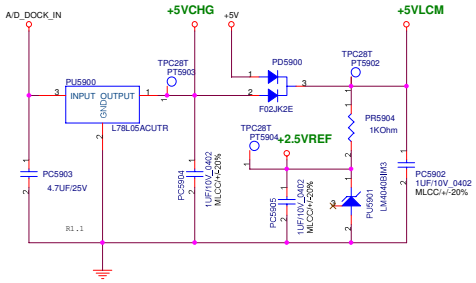
BATTERY IN DETECT



ADAPTER IN DETECT

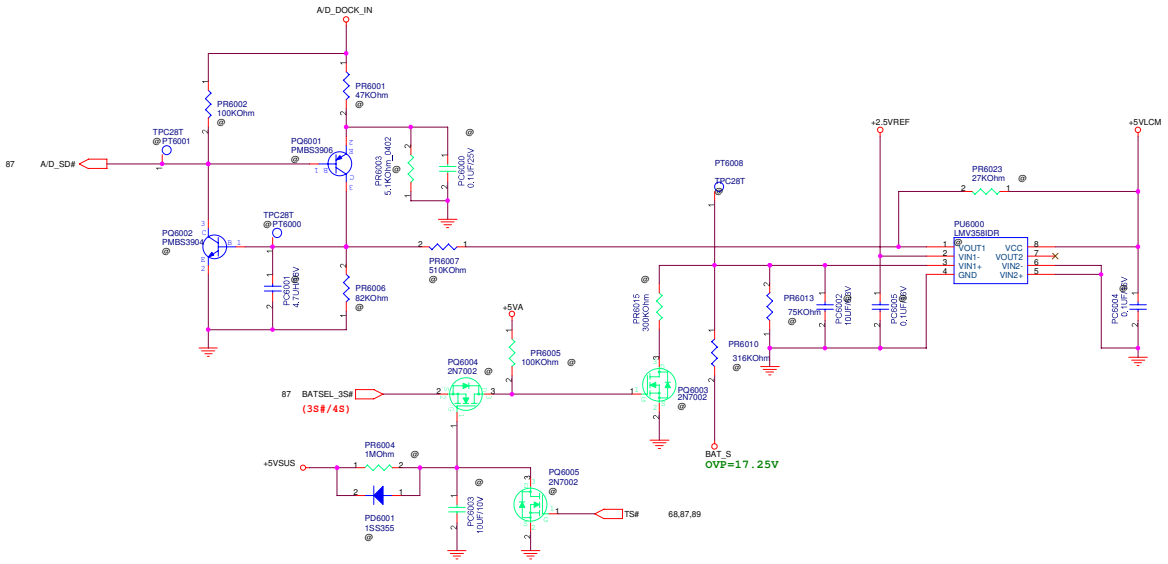


+5VLCM, +5VCHG & +2.5VREF

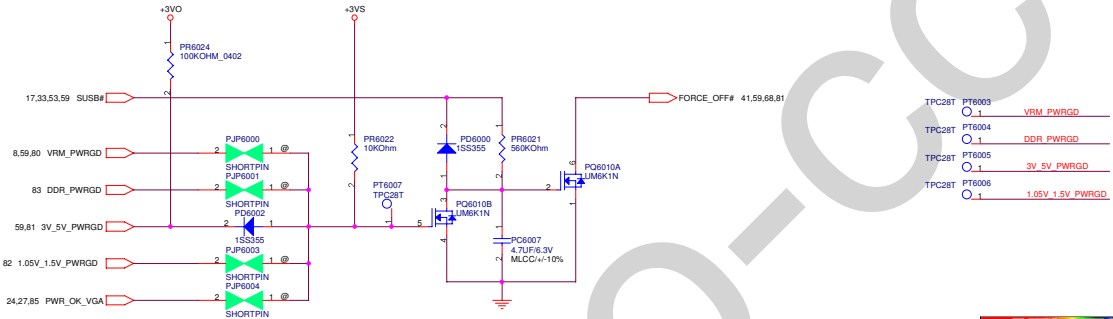


ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 星期一, 十一月 11, 2006	Sheet 89 of 94	

BATTERY A/D_SD# (OVP)

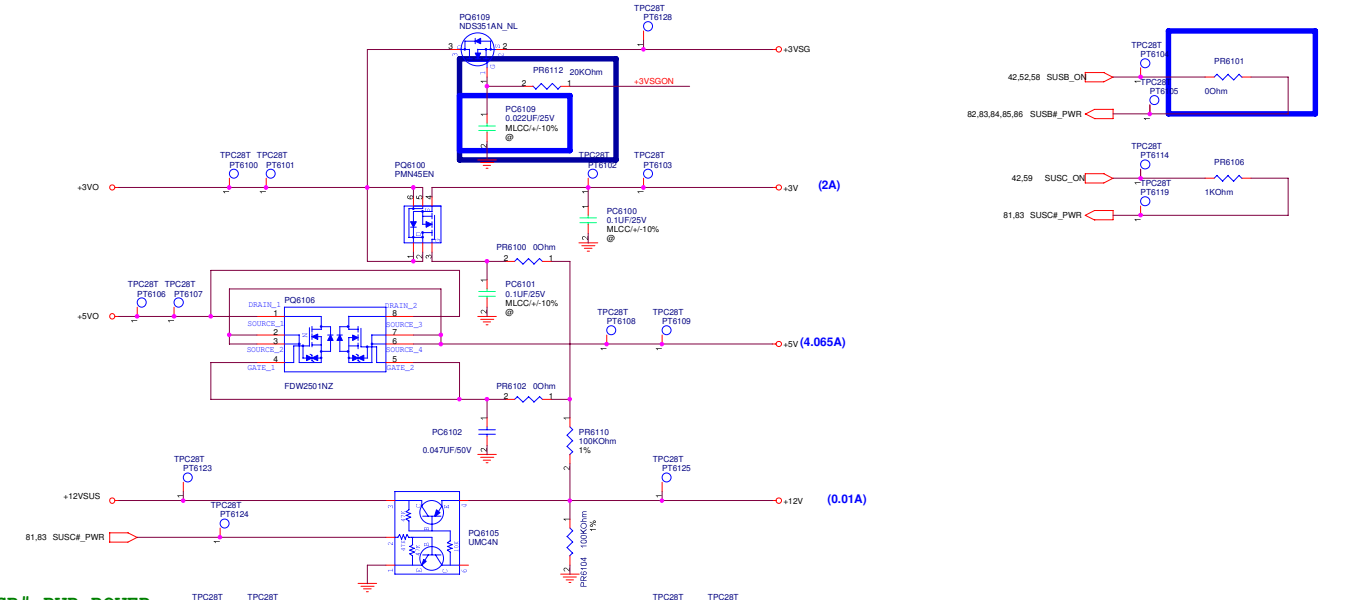


POWER GOOD DETECTER

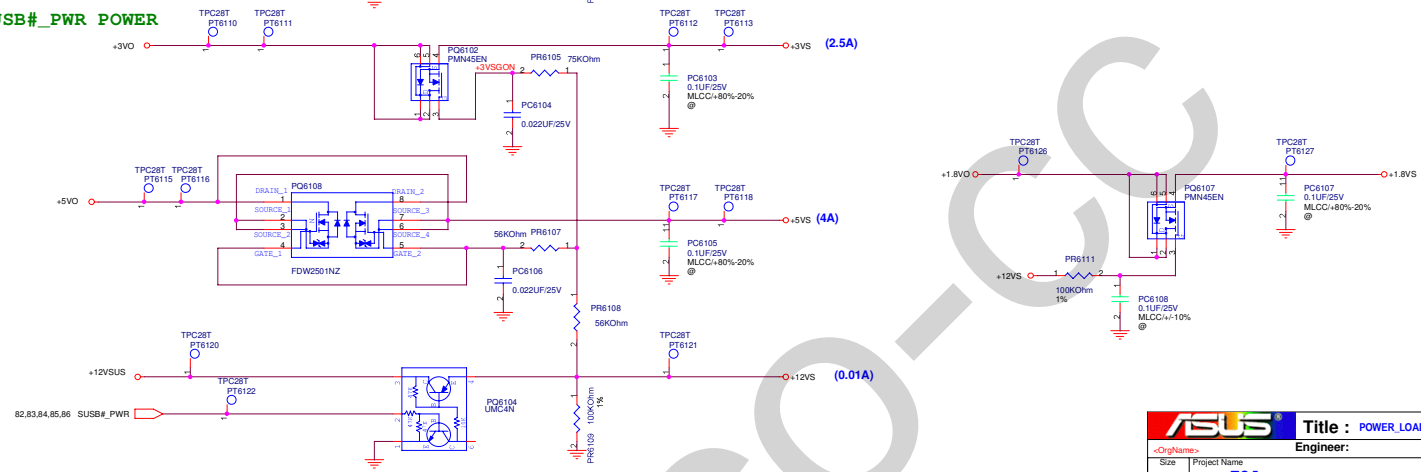


Title : POWER_PROTECT		
<OrgName>	Engineer:	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 星期一, 十一月 11, 2006	Sheet 90 of 94	

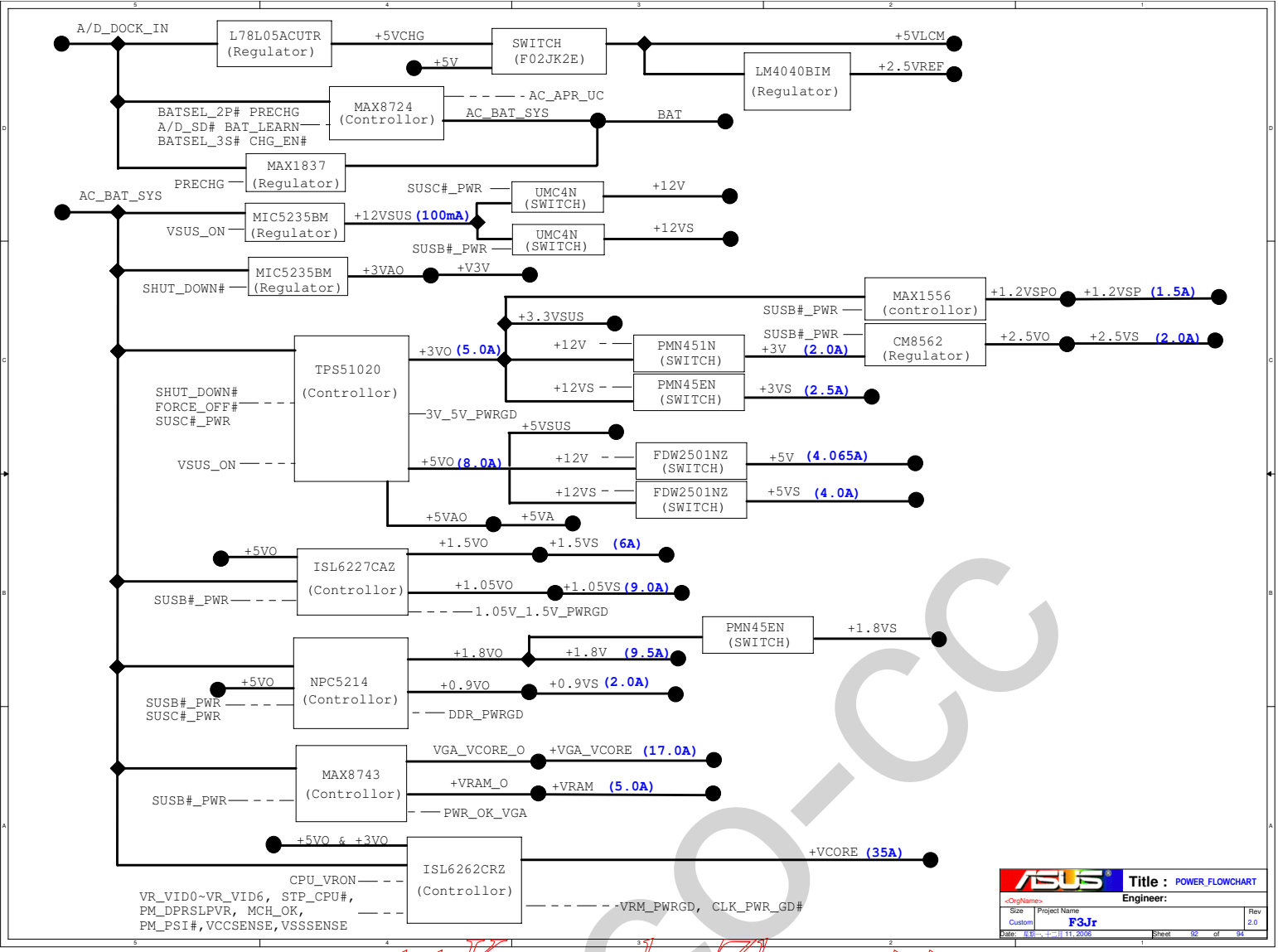
SUSC#_PWR POWER



SUSB#_PWR POWER



Title : POWER_LOAD SWITCH		
<OrgName>	Engineer:	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 星期一, 十一月 11, 2006	Sheet 91 of 94	



AC_BAT_SYS → AC_BAT_SYS 33,68,80,81,82,83,84,85,87

+3VA → +3VA 15,33,41,42,58,59,84,89

+5VA → +5VA 81,84,90

+5VO → +5VO 81,82,83,85,91

+3VO → +3VO 81,82,86,90,91

+3VSUS → +3VSUS 16,17,18,44,45,47,52,81

+5VSUS → +5VSUS 18,66,81,90

+3V → +3V 33,42,44,45,47,53,54,76,78,84,91

+3VS → +3VS 8,12,15,16,17,18,20,21,31,32,33,35,37,39,42,44,47,49,50,51,52,53,56,57,59,70,72,76,80,82,90,91

+12VSUS → +12VSUS 81,91

+12V → +12V 42,51,57,91

+12VS → +12VS 27,32,33,57,66,91

+5V → +5V 33,42,54,62,85,89,91

+5VS → +5VS 17,18,32,35,37,42,56,57,59,60,66,72,80,91

+2.5VO → +2.5VO 84

+2.5VS → +2.5VS 8,12,24,27,42,56,84

+1.8VO → +1.8VO 83,91

+1.8V → +1.8V 8,11,20,21,22,42,53,83

+1.8VS → +1.8VS 27,91

+VCCP → +VCCP 4,5,7,9,11,12,15,18,39,42,82

+0.9VS → +0.9VS 22,28,29,42,83

BAT → BAT 68,87

+5VCHG → +5VCHG 87,89

+5VLCM → +5VLCM 66,89,90

+2.5VREF → +2.5VREF 84,89,90

+VCORE → +VCORE 5,80

+VGA_VCORE → +VGA_VCORE 24,27,85

+VRAM → +VRAM 24,25,27,28,29,42,85

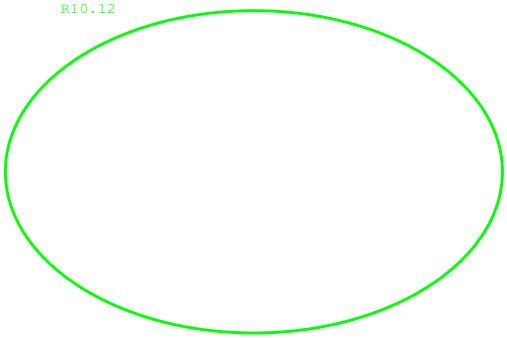
+1.2VSP → +1.2VSP 24,26,27,86

+3VSG → +3VSG 24,27,30,91

BAT_CON → BAT_CON 68,87

FOR POWER TEST

R10.12



ASUS	Title : POWER_SIGNAL	
<OrgName>	Engineer:	
Size: Custom	Project Name: F3Jr	Rev: 2.0
Date: 星期一, 十一月 11, 2006	Sheet 93 of 94	

Rev	Date	Description
1.0	10/12/06	1. Initial release.
1.1	11/03/06	1. Change L2412 Power from +3VSG to +3VSG_Delay and add JP3 default open. Page 24,27. 2. LVDDR power add L2717 connect to 1.8V for M8X. Page 27. 3. Add Q16 and THRO_CPU singal for batetry tempture protection. Page 4,59. 4. Add PD5706 for power request. Page 87.
2.0	12/05/06	1. Add VGA Thermal Sensor connect to VGA GPIO17.Page 24.

Rev	Date	Description
1.0	10/12/06 Change from F3Ja R2.2	1. Change CE8,CE14 from 47uF to 100uF CAP EL 5*5.4 for cost down. Page 37,62. 2. Remove R231,R530,R232,R529 for Pannel ID. Page 33. 3. Change PCB_ID [2:0] to 000. Page 17. 4. Remove RN2, RN3, RN22, R225, R226, R547, R548, R174, R421, R565, R500 for cost down. Page 5,39,32,45,57,49. 5. Change R347, R525, R528, R414, R415, R417, R418 to Short Pad and default Open. Page 45, 56. 6. Change R437, R438, L5, L6, R257, R259, R266, R443, R159 to Short Pad and default Short. Page 59,12,39,44. 7. Change R531, R532, L85, R367, R368, L64, R535, R536, L99, R444, R446, L84, R449, R450, L86, R451, R453, L87, R454, R457, L90 to RN55, RN60, RN61, RN62, RN64, RN65. Page 33,35,52,78,62. 8. Add R5823,C2941 for sigmatel internal MIC. pull up power. Page 56. 9. Add R5824, R5825, R5826, R5827, R5828, R5829, L2905, L2906, L2907 for DVI EMI. Page 35. 10. USB of Finger Print Add C168, C619 0603 Size for EMI Request. Page 31. 11. Add R82 for support Clock Gen. ICS9LPR363. Page 39. 12. Remove PJP6300,PJP6301,PJP6302,PJP6303. Page 93.

ASUSTek COMPUTER INC

Title : History

Engineer: Frank Xu

Size	Project Name	Rev
Custom	F3Jr	2.0

Date: 十一月 11, 2006 Sheet 94 of 94