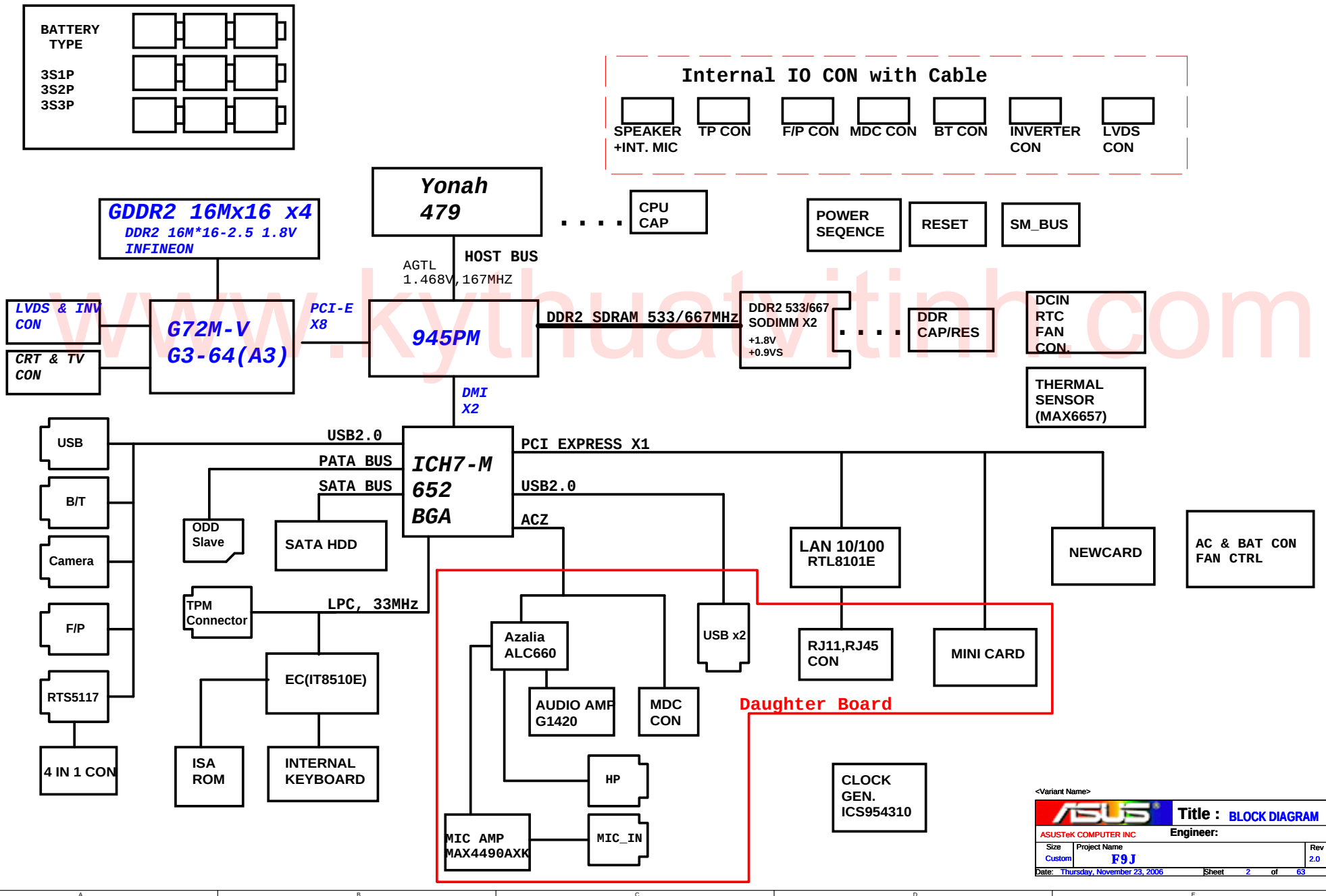


F9J SCHEMATIC Revision 2.0

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	SYSTEM PAGE REF.	47	DC & BAT IN
4	YONAH CPU (1)	48	History(1)
5	YONAH CPU (2)	49	History(2)
6	FAN CTRL&Thernal protection		
7	CLK GEN-ICS954310		
8	Calistoga--CPU		
9	Calistoga--PCIE		
10	Calistoga--DDR2		
11	Calistoga--POWER		
12	Calistoga--GND		
13	Calistoga--Strap		
14	DDR2 SO-DIMM_0		
15	DDR2 SO-DIMM_1		
16	DDR2 ADDRESS TERMINATION		
17	LVDS & INVERTER CONN		
18	CRT & TV OUT		
19	ICH7M--CPU, IDE, AUDIO		
20	ICH7M--GPIO		
21	ICH7M--PCI, PCI-E, USB		
22	ICH7M--VCC, GND		
23	HDD & CD-ROM CONN		
24	USB PORT		
25	B/T, F/P& TPM		
26	B TO B CONN(M)		
27	EMPTY		
28	EMPTY		
29	PCI-E--LAN_RTL8101E		
30	EMPTY		
31	EMPTY		
32	EMPTY		
33	NEWCARD		
34	EC-IT8510E		
35	ISA ROM & Touch Pad & KB& FP		
36	CARD READER_RST5117		
37	DISCHARGE		
38	Instant Key & Touch Pad		
39	LEDs		
40	G72M--PCIE (1)		
41	G72M--FB (2)		
42	G72M--VRAM (3)		
43	G72M--RGB/LCD/ROM/GPIO (4)		
44	G72M--MI0B/CRYSTAL/TMDS (5)		
45	G72M--VRAM_TERMINATOR (6)		
46	SREW HOLE		

F9J BLOCK DIAGRAM



EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	N/A	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	N/A	
37	PWM3/GPA3	N/A	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	N/A	O
163	SMCLK0/GPB3	SMB0_CLK	I/O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	N/A	I
47	CLKOUT/GPC0	N/A	O
169	SMCLK1/GPC1	SMB1_CLK	I/O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	N/A	
172	TMR10/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	PCI_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	N/A	
42	GINT/GPD5	N/A	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	N/A	
87	ADC4/GPE0	WLAN_SW#	I
88	ADC5/GPE1	BT_SW#	I
89	ADC6/GPE2	N/A	
90	ADC7/GPE3	N/A	
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	N/A	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	N/A	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	
115	PS2DAT1/GPF3	/	
116	PS2CLK2/GPF4	TP_CLK	I/O
117	PS2DAT2/GPF5	TP_DAT	I/O
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	N/A	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	N/A	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O
81	ADC0	BAT_AD	I
82	ADC1	ADP_ERR#	I
83	ADC2	AC_AD	I
84	ADC3	N/A	
93	ADC8	KID0	
94	ADC9	KID1	
99	DAC0	N/A	
100	DAC1	N/A	
101	DAC2	INVTER_DA	O
102	DAC3	BATSEL_2P#	O

ICH7M_PCI EXPRESS

PCI-E Device	PAIR
RTL8101E	1
GOLAN	2
NEWCARD	3

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A4)
Thermal Sensor(MAX6657)--CPU	1001100x (98)
Thermal Sensor(G781-1)--VGA	1001101x (9A)

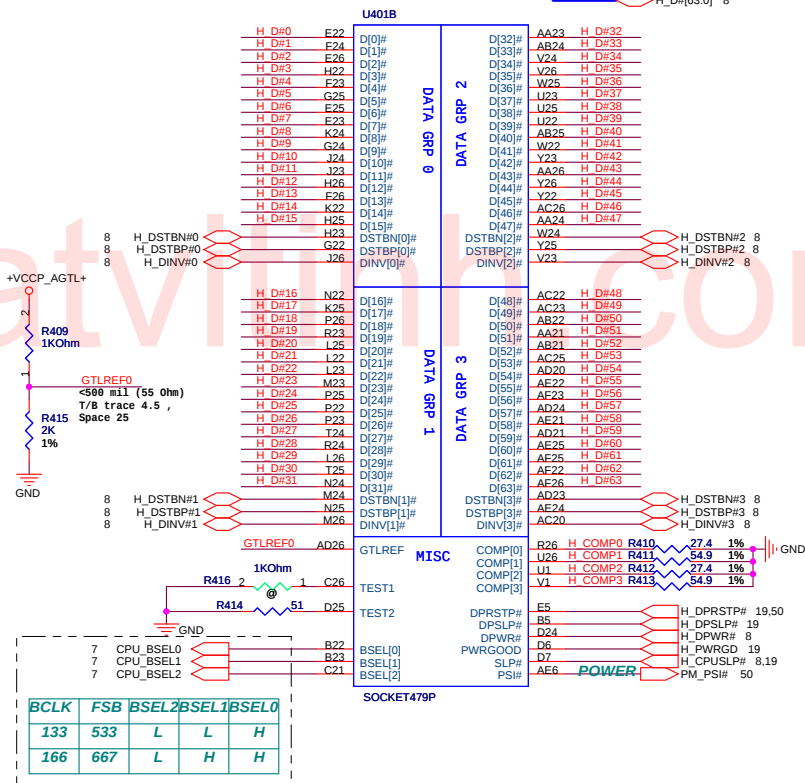
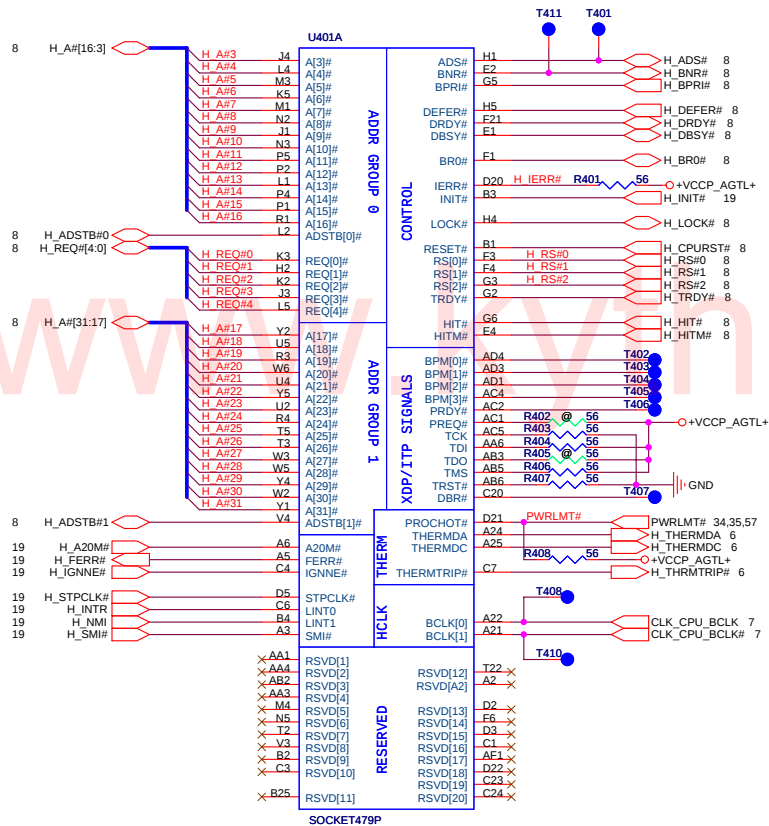
PCI Device	IDSEL#	REQ / GNT#	Interrupts

ICH7M_GPIO

Pin	Use As	Signal Name	Power
GPIO 00	i GPI	PM_BMBUSY#	+3VS
GPIO 01	i GPI	PCI_REQ#5	+3VS
GPIO [5:2]	i GPI	PCI_INT[E:H]#	+3VS
GPIO 06	i GPO	BT_LED_EN	+3VS
GPIO 07	i GPI	RF_ON_SW#	+3VS
GPIO 08	i GPI	EXTSMI#	+3VSUS
GPIO 09	i GPI	N/A	+3VSUS
GPIO 10	i GPI	N/A	+3VSUS
GPIO 11	i Native	SMB_ALERT#	+3VSUS
GPIO 12	i GPI	KBC_SCI#	+3VSUS
GPIO 13	i GPI	N/A	+3VSUS
GPIO 14	i GPI	N/A	+3VSUS
GPIO 15	i GPO	802_LED_EN	+3VSUS
GPIO 16	O 0 GPO	PM DPRSLPVR	+3VS
GPIO 17	O 1 GPO	PCI_GNT#5	+3VS
GPIO 18	O 1 GPO	STP_PCI#	+3VS
GPIO 19	i 1 GPI	N/A	+3VS
GPIO 20	O 1 GPO	STP_CPU#	+3VS
GPIO 21	i 1 GPO	N/A	+3VS
GPIO 22	i 1 Native	PCI_REQ#4	+3VS
GPIO 23	i 1 Native	N/A	+3VS
GPIO 24	O 0 GPO	MSK_PCIRST	+3VSUS
GPIO 25	O 1 GPO	N/A	+3VSUS
GPIO 26	O 0 GPO	BT_ON#	+3VSUS
GPIO 27	O 0 GPO	WLAN_ON#	+3VSUS
GPIO 28	O 0 GPO	N/A	+3VSUS
GPIO 29	i 0 Native	USB_OC#5	+3VSUS
GPIO 30	i 0 Native	USB_OC#6	+3VSUS
GPIO 31	i 0 Native	USB_OC#7	+3VSUS
GPIO 32	O 1 GPO	PM_CLKRUN#	+3VS
GPIO 33	O 1 GPO	N/A	+3VS
GPIO 34	O 0 GPO	N/A	+3VS
GPIO 35	O 0 GPO	N/A	+3VS
GPIO 36	i 0 GPO	N/A	+3VS
GPIO 37	i 0 GPI	PCB_ID0	+3VS
GPIO 38	i 0 GPI	PCB_ID1	+3VS
GPIO 39	i 0 GPI	PCB_ID2	+3VS
GPIO [40:47]	NA	NA	NA
GPIO 48	Native	PCI_GNT#4	+3VS
GPIO 49	Native	H_PWRGD	+VCORE

<Variant Name>

		Title : Schematic data	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9J		2.0
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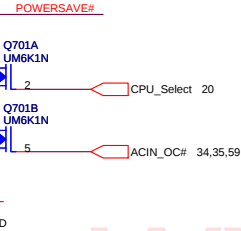


<Variant Name>

CPU_BSEL0 R701 1K MCH_BSEL0 9
CPU_BSEL1 R702 1K MCH_BSEL1 9
CPU_BSEL2 R705 1K MCH_BSEL2 9

FSLC FSLB FSLA

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



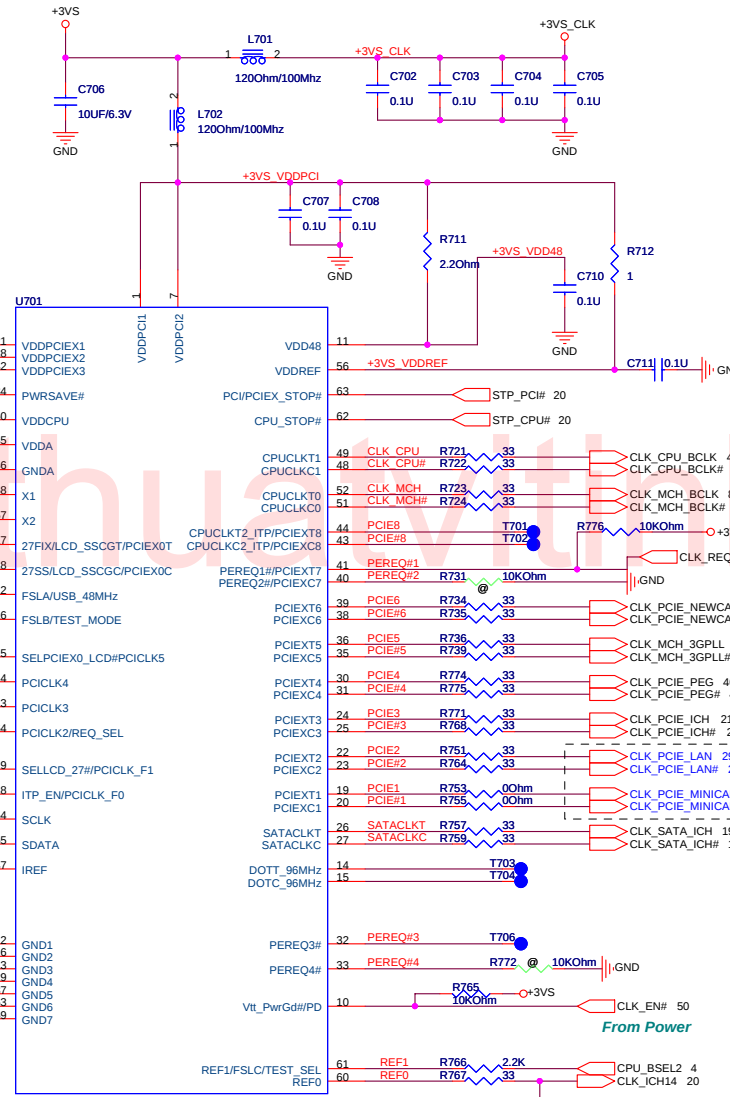
44 CLK_NV27
44 CLK_NV27SS
20 CLK_USB48

T705

35 CLK_DBGPCI
34 CLK_ECPCI
25 CLK_TPMPC
33 CLK_DEBUG2
21 CLK_IHPPCI
14,15,20,33 SCL_3S
14,15,20,33 SDA_3S

Latched Input Select

/	PIN9	PIN5	PIN17	PIN18
*	0	X	27FIX	27SS
	1	1	96MSS_T	96MSS_C
			PCIEX0_T	PCIEX0_C



ICS954310CGLT
Int. PU: PIN5, PIN9, PIN32, PIN33, PIN34
Int. PD: PIN64

PLACE termination close to source IC

CLK_CPU_BCLK R703 49.9 1%
CLK_CPU_BCLK# R704 49.9 1%
CLK_MCH_BCLK R706 49.9 1%
CLK_MCH_BCLK# R708 49.9 1%
CLK_MCH_3GPLL R709 49.9 1%
CLK_MCH_3GPLL# R710 49.9 1%
CLK_PCIE_NEWCARD R713 49.9 1%
CLK_PCIE_NEWCARD# R715 49.9 1%
CLK_PCIE_LAN R717 49.9 1%
CLK_PCIE_LAN# R718 49.9 1%
CLK_PCIE_MINICARD R763 49.9 1%
CLK_PCIE_MINICARD# R750 49.9 1%
CLK_PCIE_ICH R769 49.9 1%
CLK_PCIE_ICH# R770 49.9 1%
CLK_SATA_ICH R726 49.90hm
CLK_SATA_ICH# R728 49.90hm
CLK_PCIE_PEG R748 49.9 1%
CLK_PCIE_PEG# R773 49.9 1%

Layout SWAP(Different with F9F)

PEREQ#2 CLK_REQ_MINICARD# 26

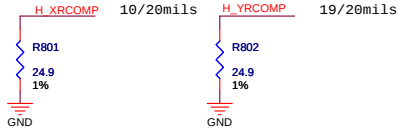
PEREQ#1: PCIE0, PCIE6
PEREQ#2: PCIE1, PCIE8
PEREQ#3: PCIE2, PCIE4
PEREQ#4: PCIE3, PCIE5, PCIE7

ITP_EN/PCICLK_F0 (PIN8)	0 = SRC Pair 1 = CPU ITP Pair
SELPICIE0_LCD#/PCI_CLK5 (PIN5)	0 = LCD Clock (96MHz) 1 = PCI Express (100MHz) (D)
PCI_CLK2/REQ_SEL (PIN64)	0 = PCICLK(D) 1 = PEREQ#
SELLCD_27#/PCICLK_F1 (PIN9 Variant Name)	0 = 27MHzSS/27MHzSS# Pair 1 = LCD_CLK Pair (D)

ASUS		Title : ICS954310	
ASUSTek COMPUTER INC		Engineer:	
Size Custom	Project Name F9J	Rev 2.0	
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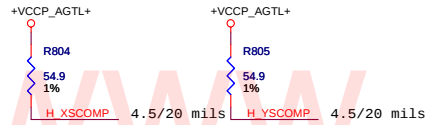
RCOMP

For Calibrating FSB I/O Buffer



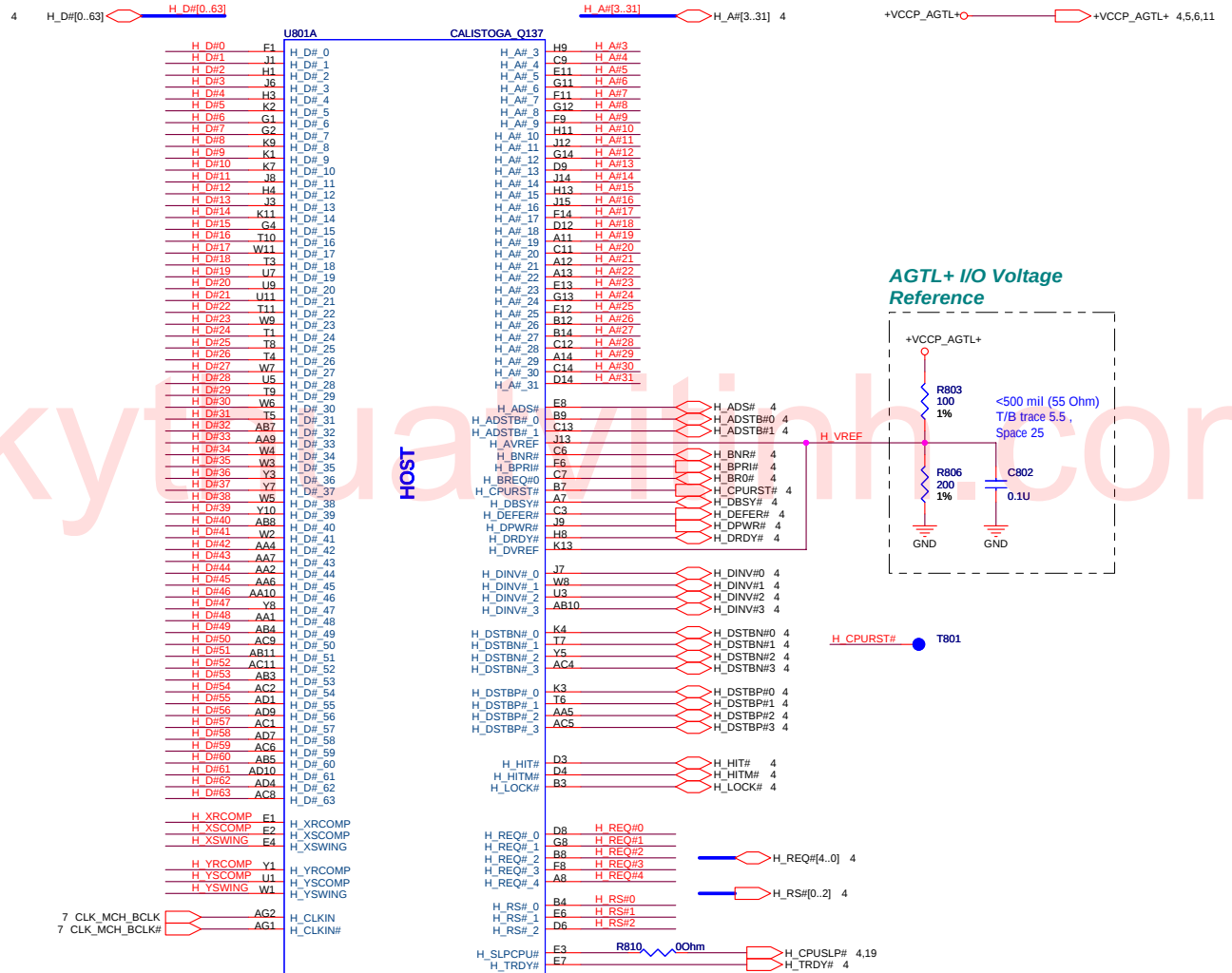
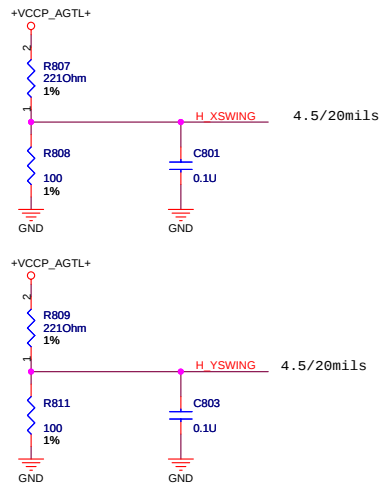
SCOMP

For Slow Rate Compensation on the FSB



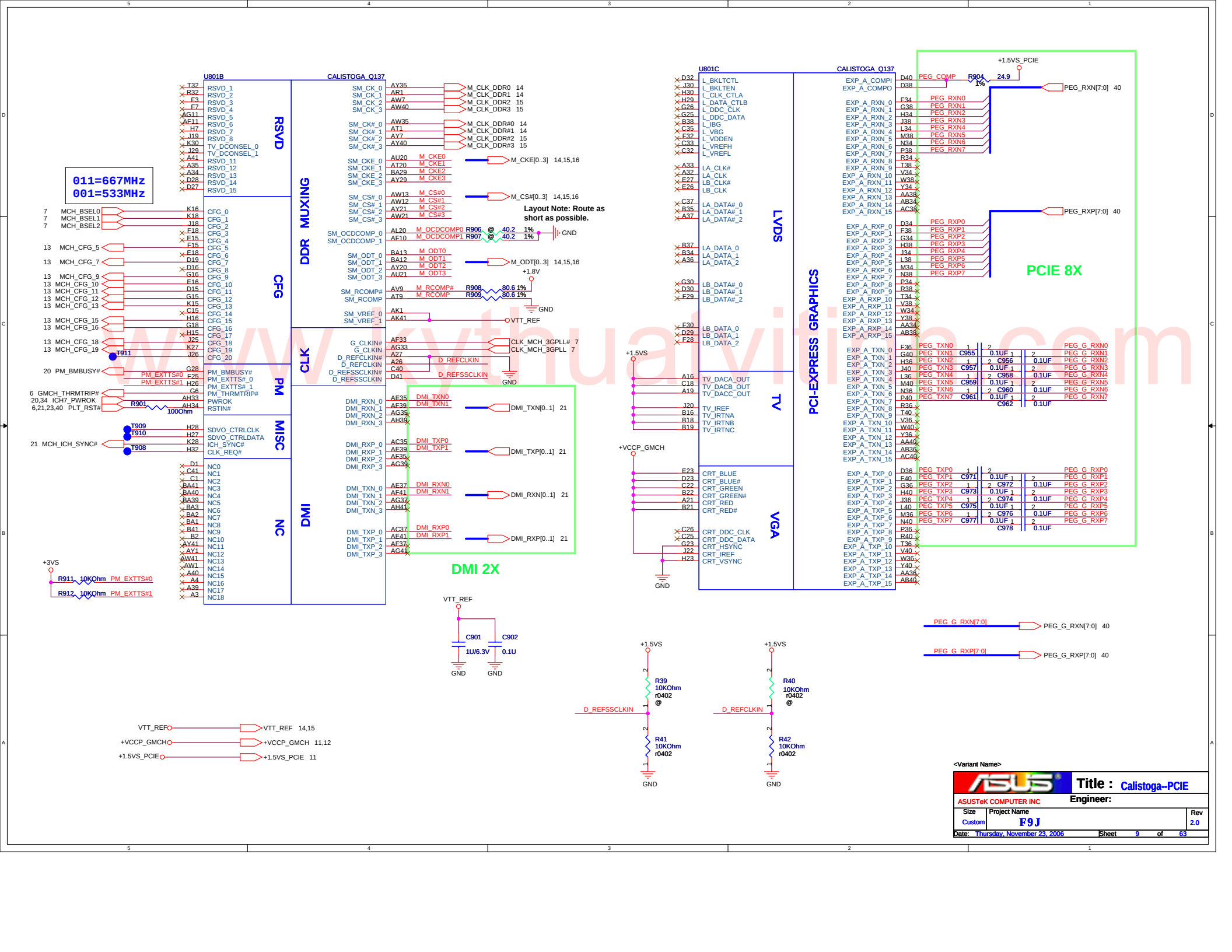
Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP Circuit



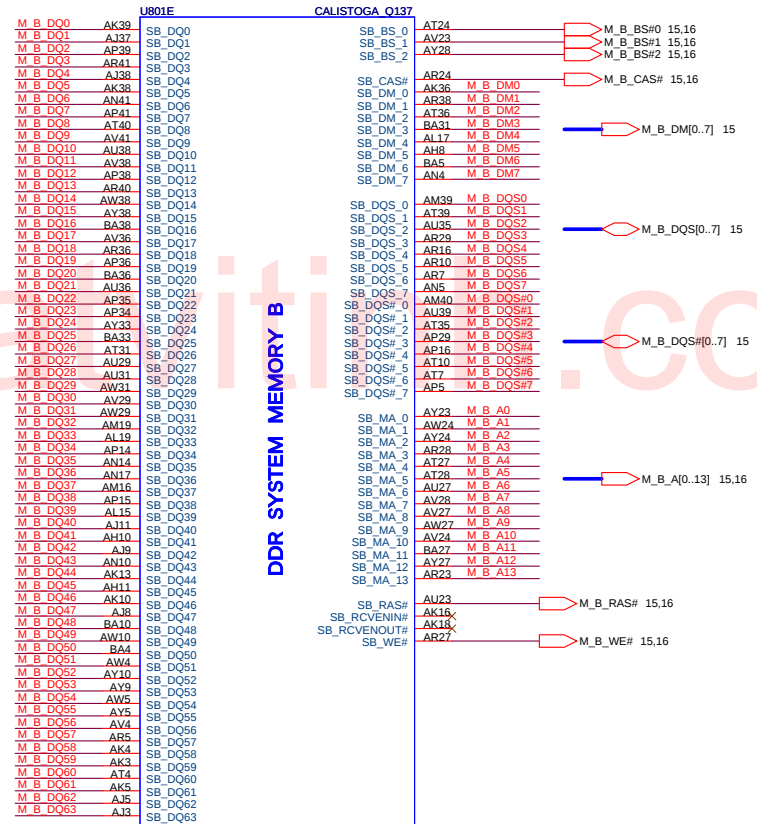
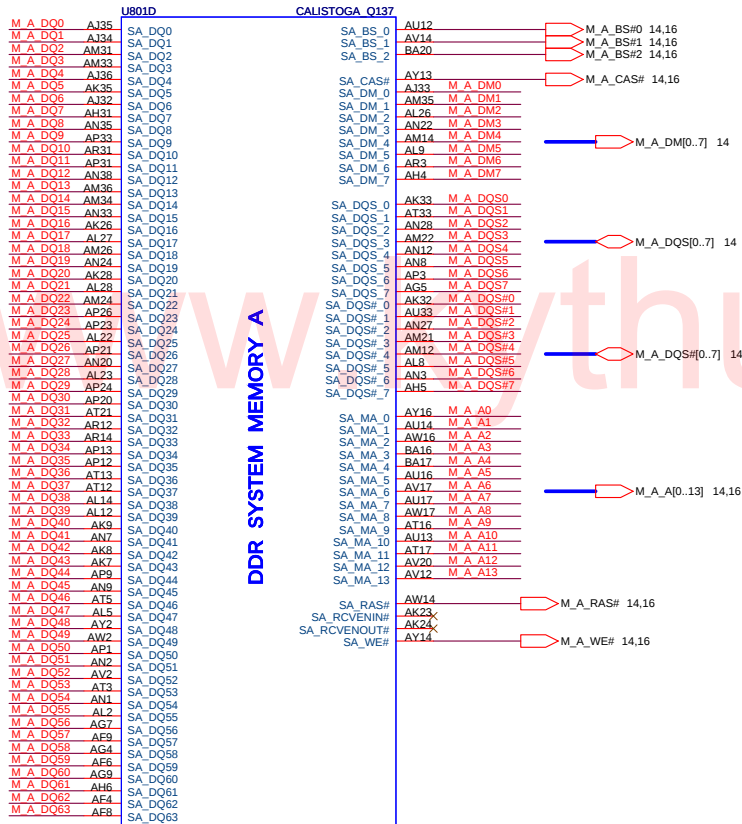
<Variant Name>

ASUS		Title : Calistoga-CPU	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F9J	2.0	
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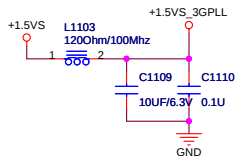
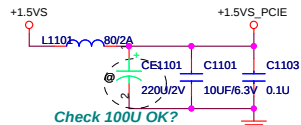
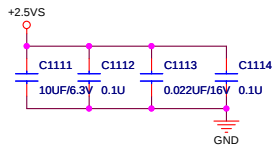
14 M_B_DQ[0..63]

15 M_B_DQ[0..63]

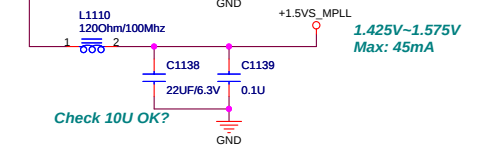
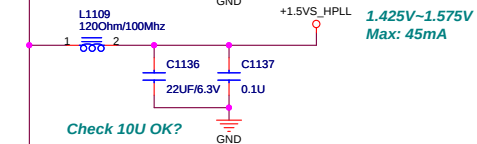
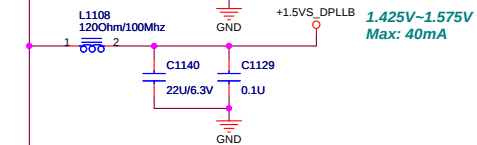
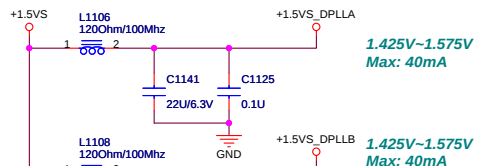


<Variant Name>

ASUS		Title : Calistoga-DDR2	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F9J	2.0	
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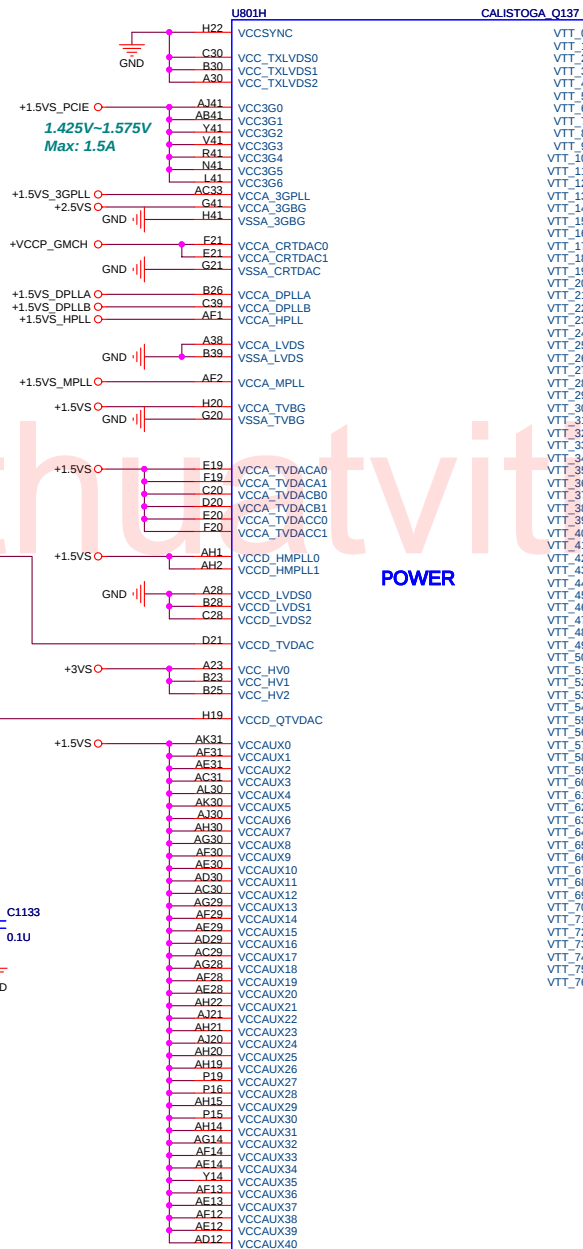


NOTE: 0.1uF caps in 1.5SxPLL need to be located as edge caps within 200 mils.

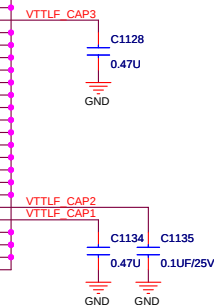
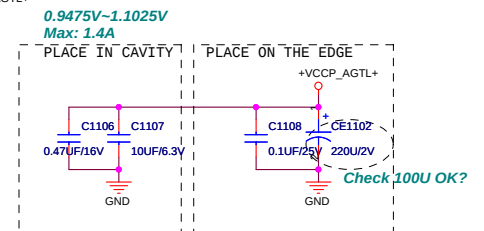


+1.5VS → +1.5VS 5,9,12,22,26,33,37,52,56
+2.5VS → +2.5VS 37,43,44,54
+3VS → +3VS 6,7,9,13,14,15,17,18,20,22,23,25,26,29,33,34,37,38,39,40,43,44,45,50,60,61
+VCCP_AGTL+ → +VCCP_AGTL+ 4,5,6,8

NOTE: 0.1uF CAPS USED IN +1.5VS, +3.3VS +2.5VS should be placed within 200 mils of edge.

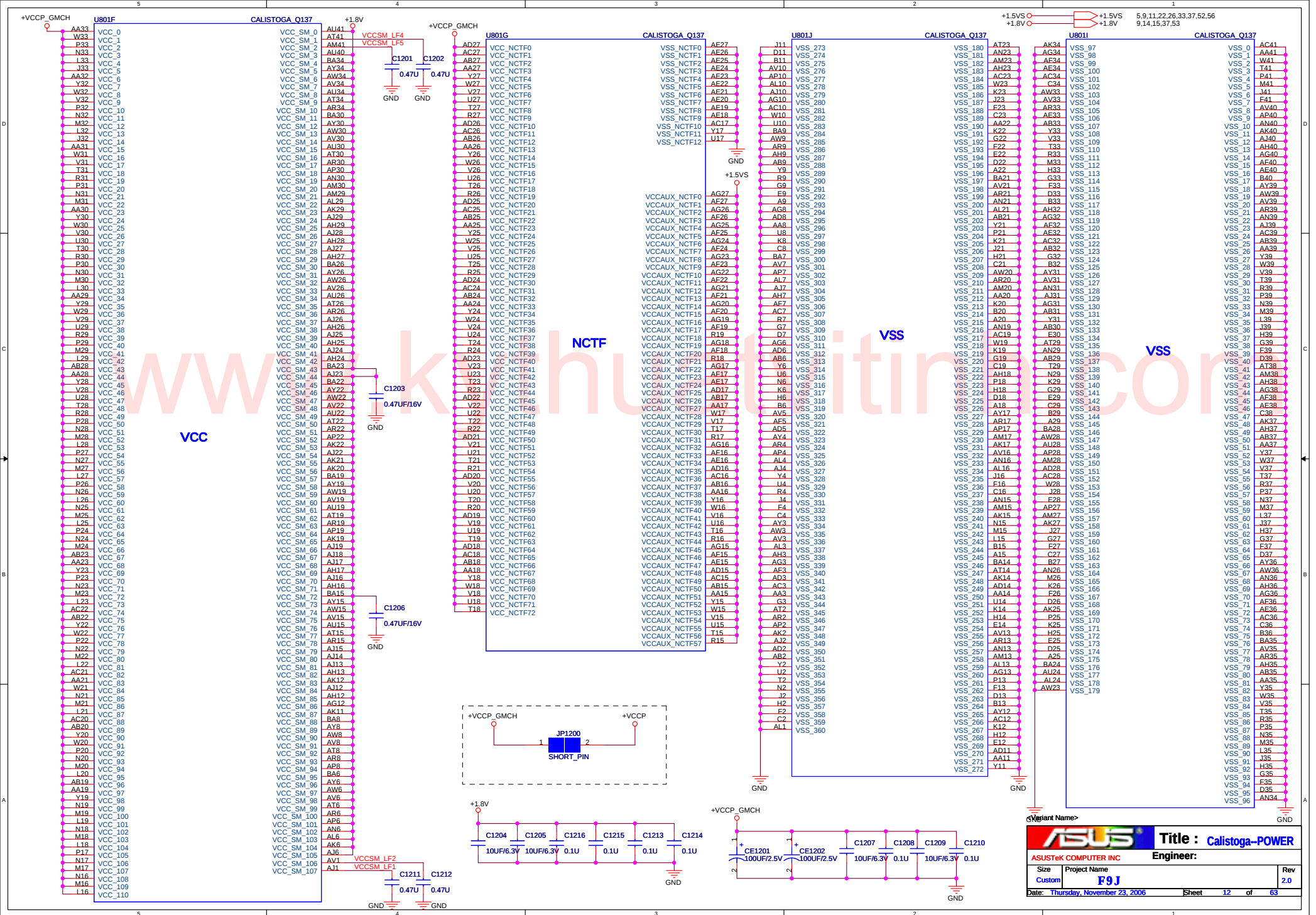


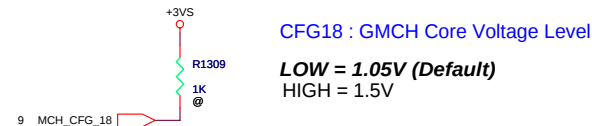
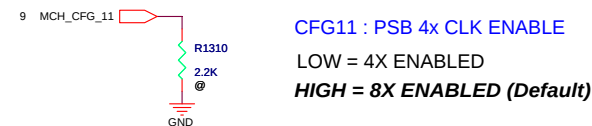
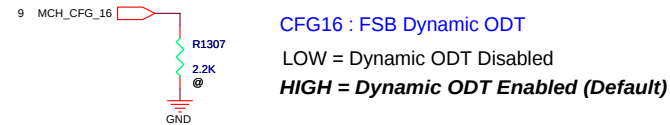
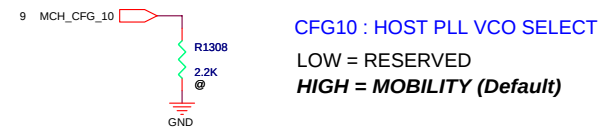
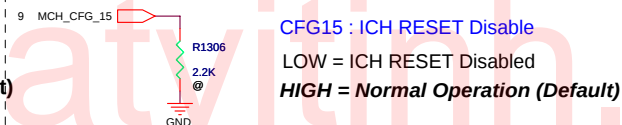
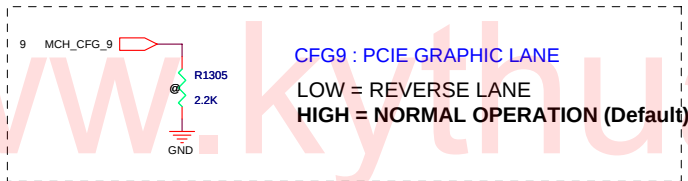
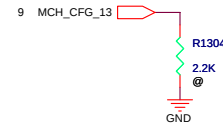
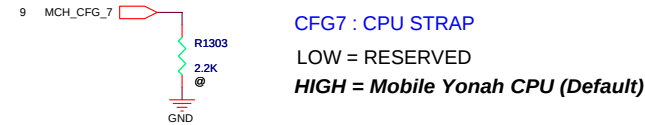
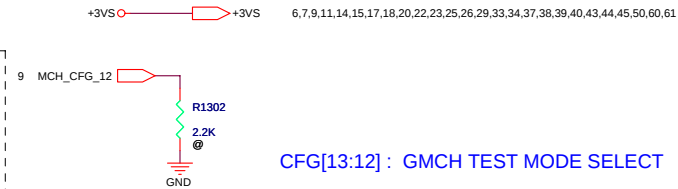
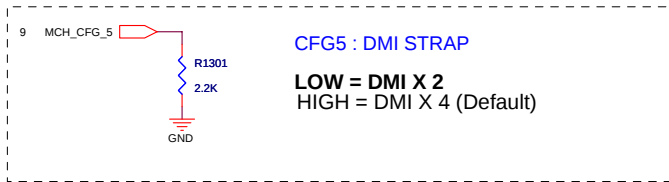
POWER



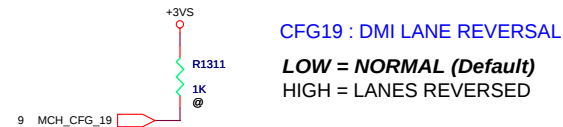
<Variant Name>

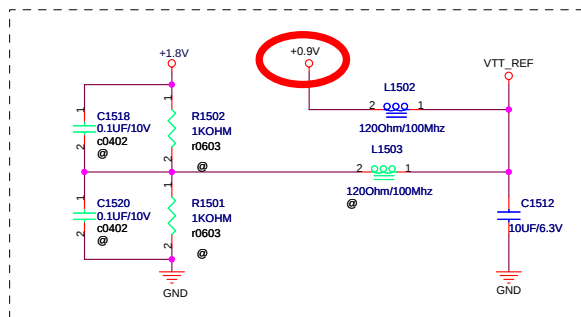
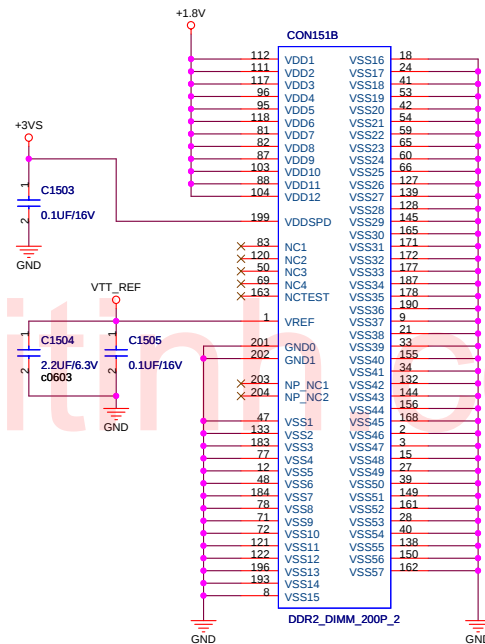
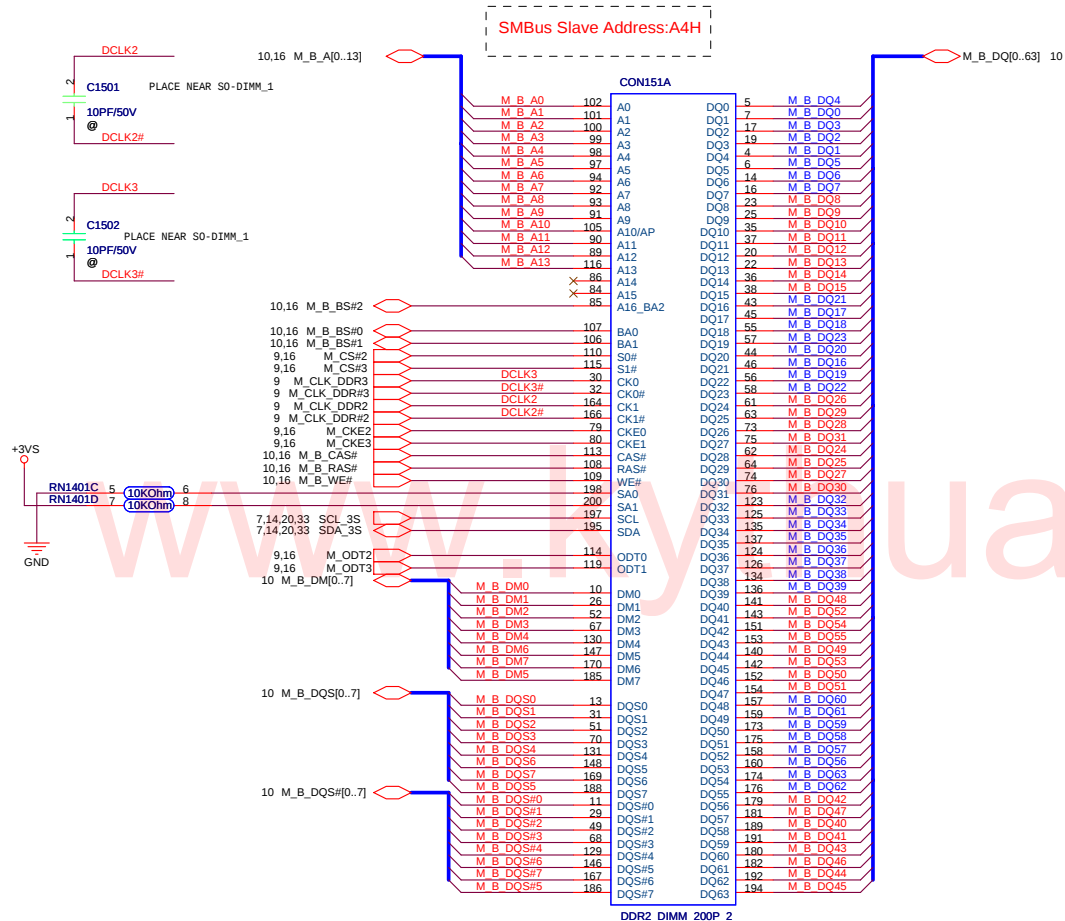
ASUS		Title : Calistoga-POWER	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F9J	2.0	
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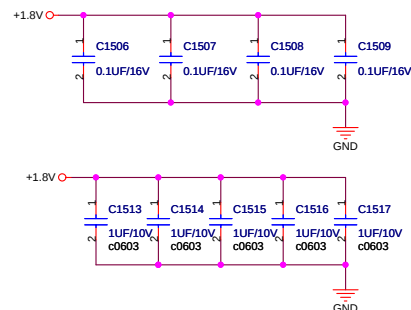


CFG[17..3] have internal pullup resistors.
 CFG[19..18] have internal pulldown resistors.
 SDVOCRTL_DATA has internal pulldown resistors.



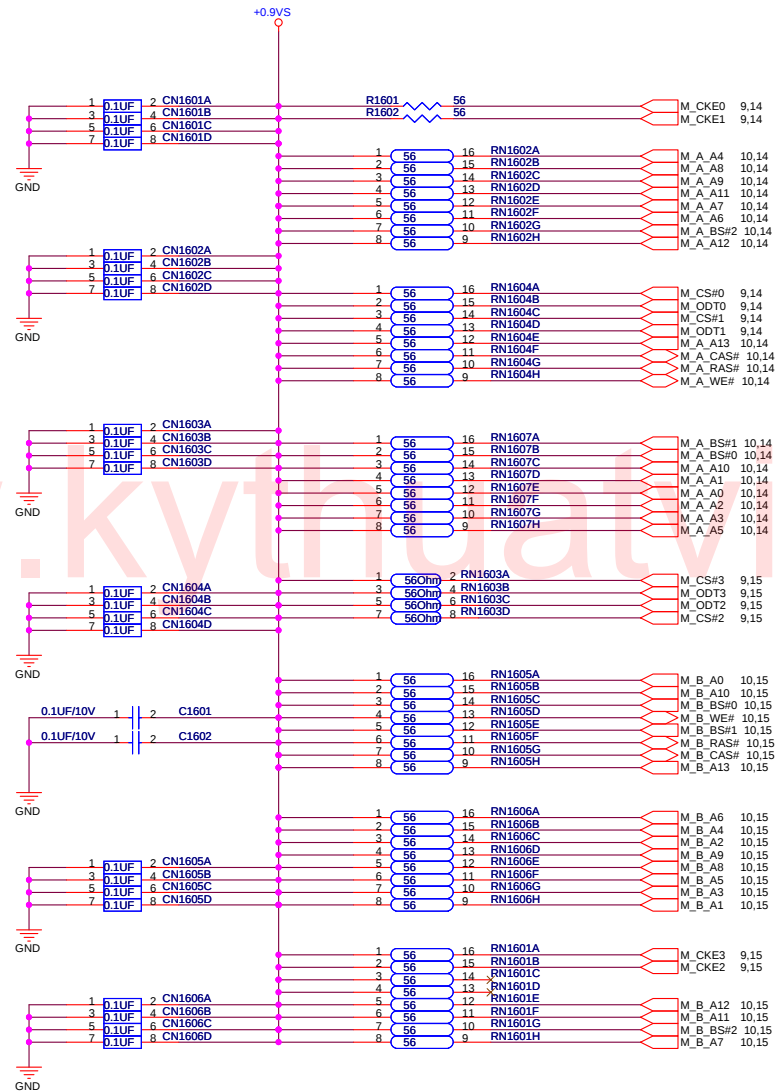


Layout Note: Place these Caps near SO DIMM 1



<Variant Name>

ASUS		Title : DDR2 SO-DIMM_1	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F9J	2.0	
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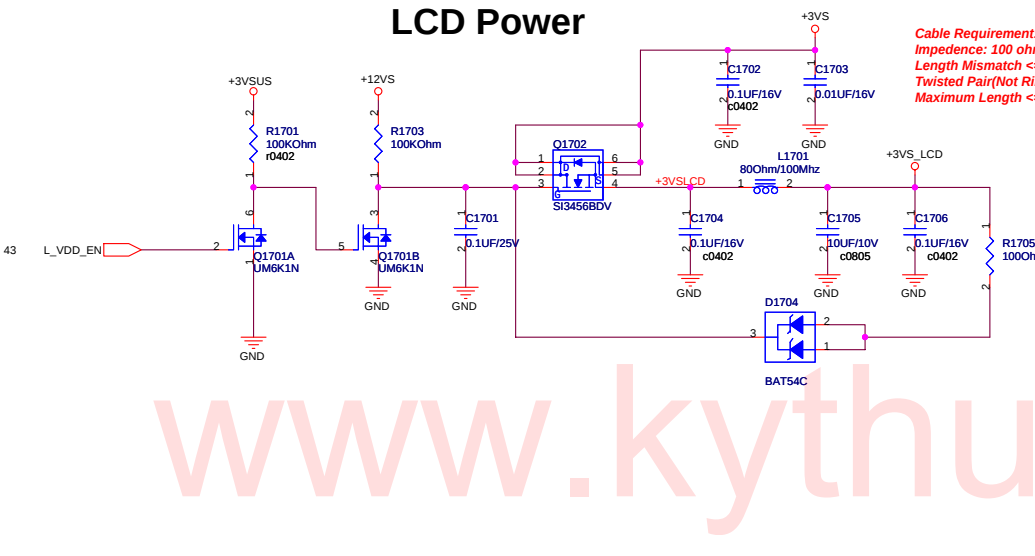


<Variant Name>

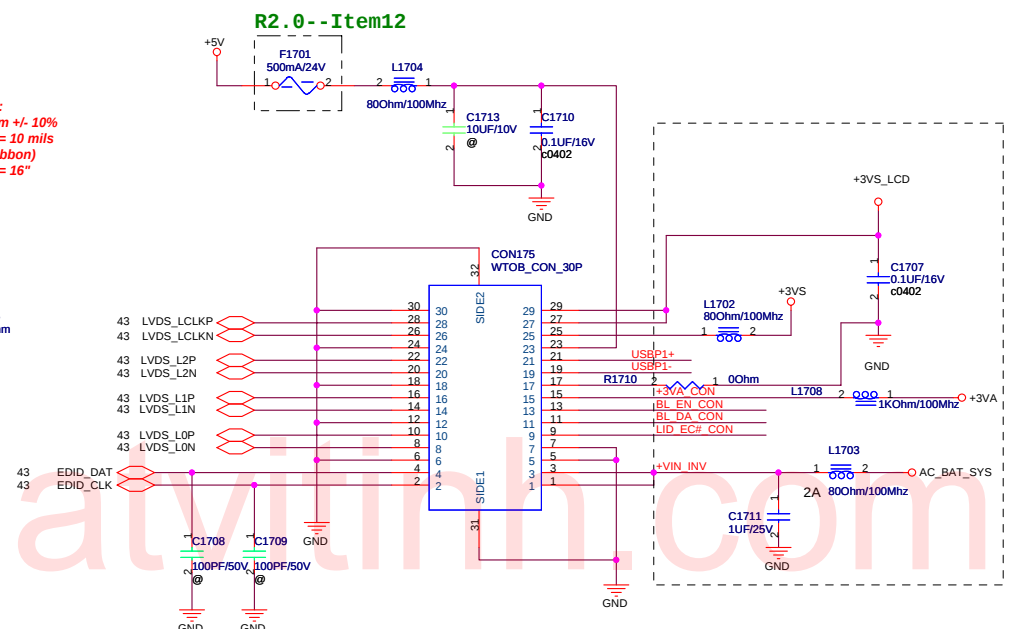
ASUS		Title :DDR2 TERMINATION	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F9J	2.0	
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LCD Backlight Control

LCD Power

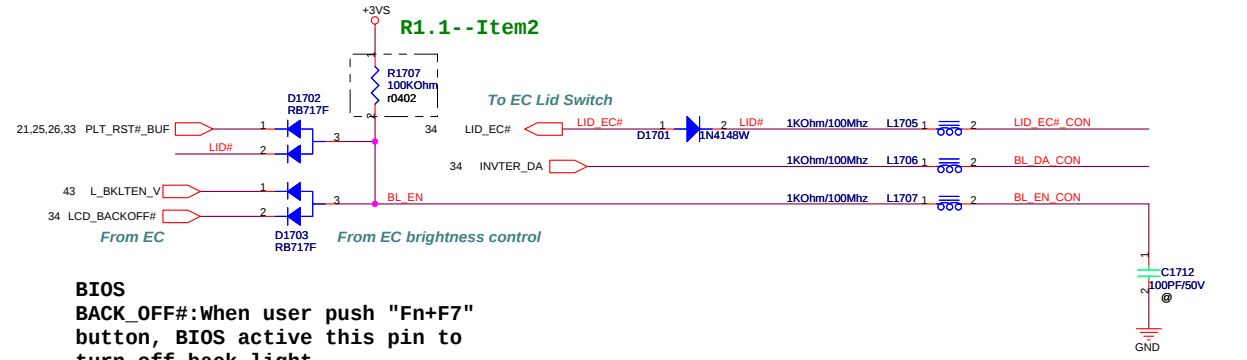
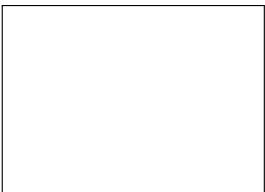


Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

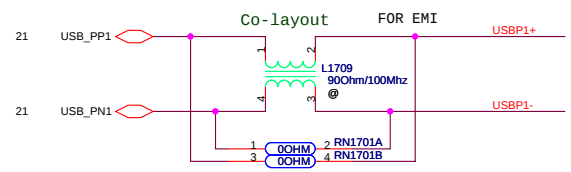


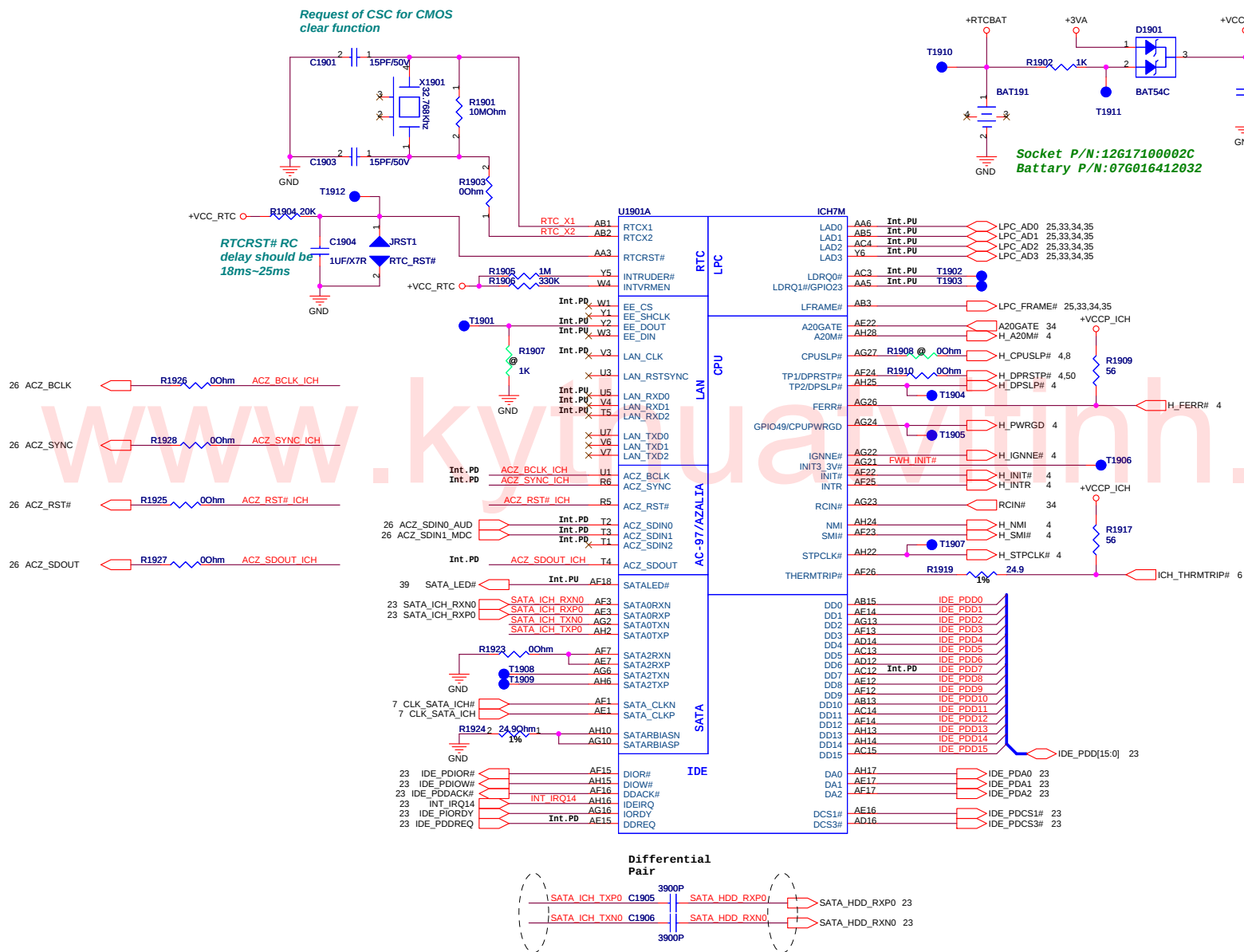
Use F3JA's inverter

CCD connector



BIOS
BACK_OFF#:When user push "Fn+F7"
button, BIOS active this pin to
turn off back light.

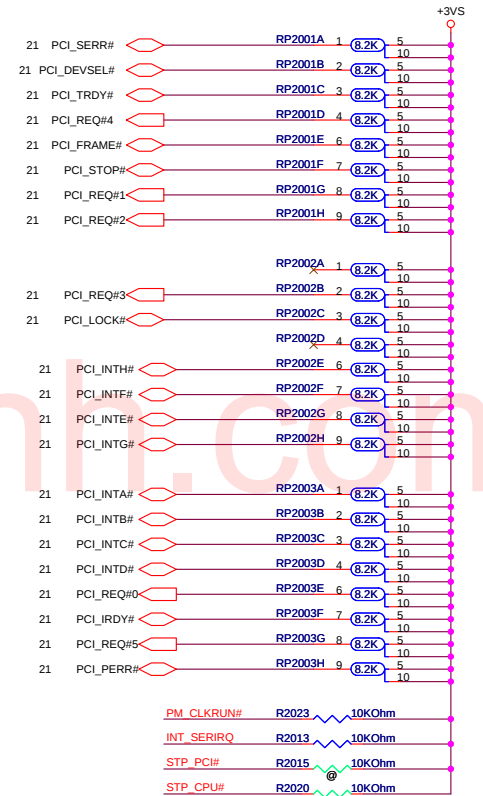
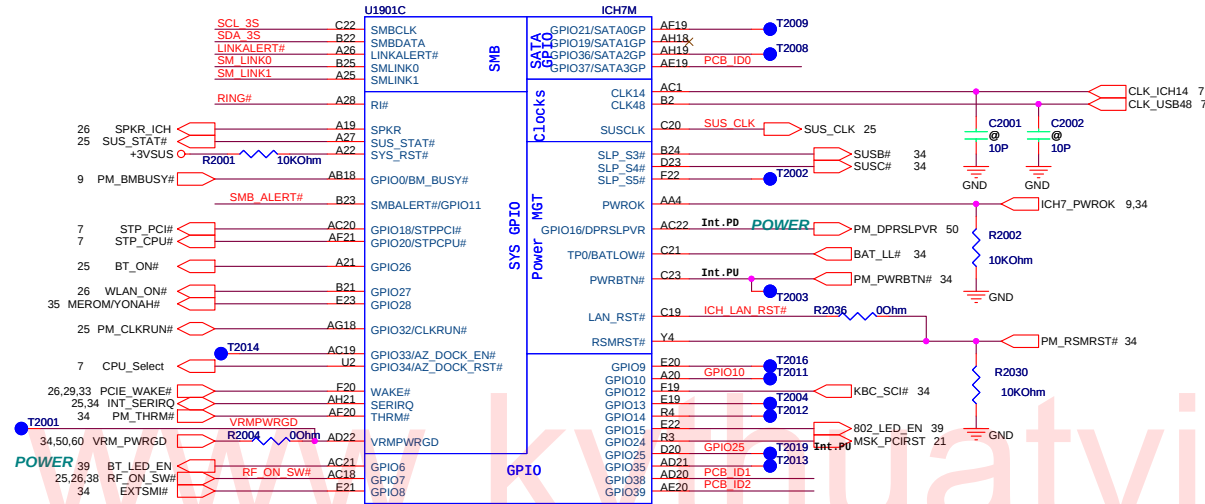




<Variant Name>

ASUS		Title : ICH7M (1)	
ASUSTek COMPUTER INC		Engineer:	
Size Custom	Project Name F9J	Rev 2.0	
Date: Thursday, November 23, 2006		Sheet 19 of 63	

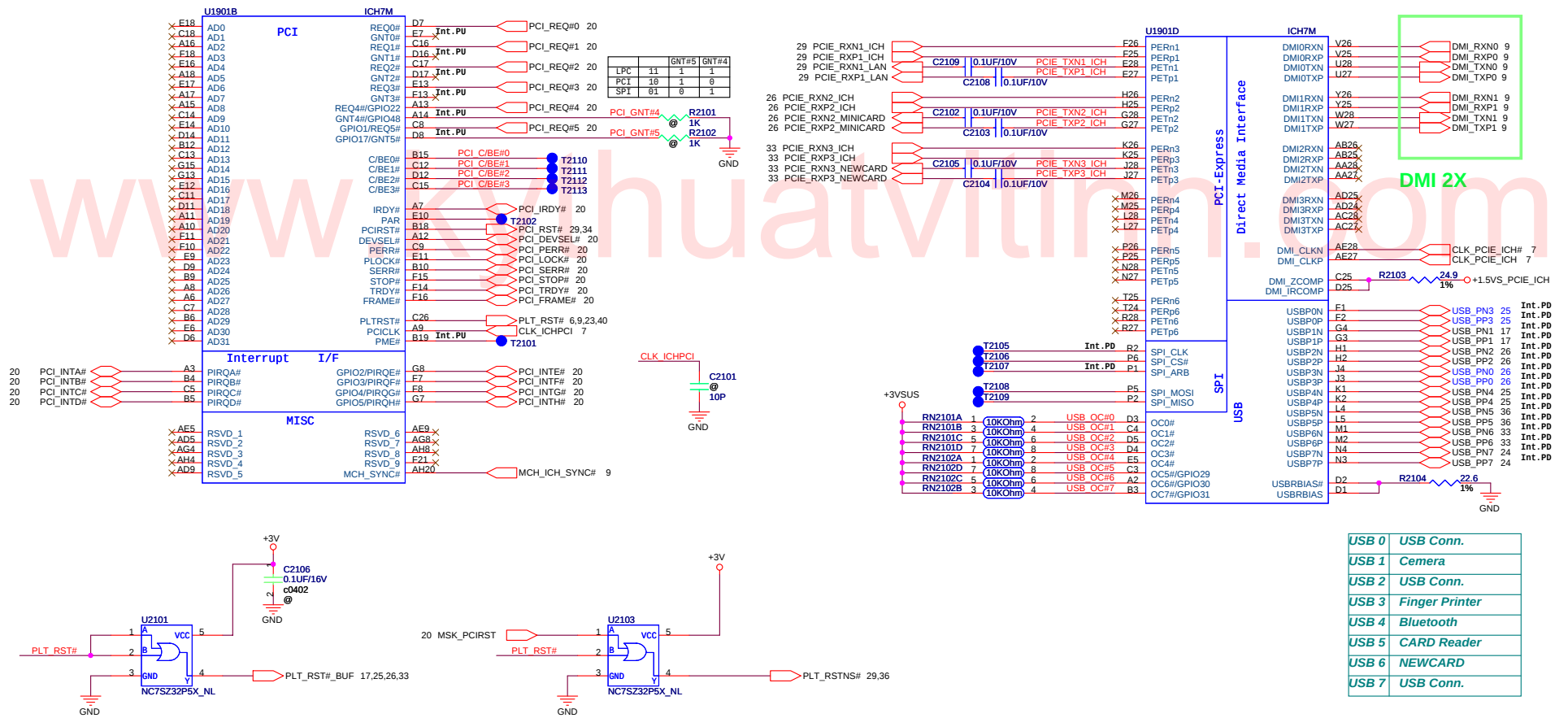
To new card check power plane



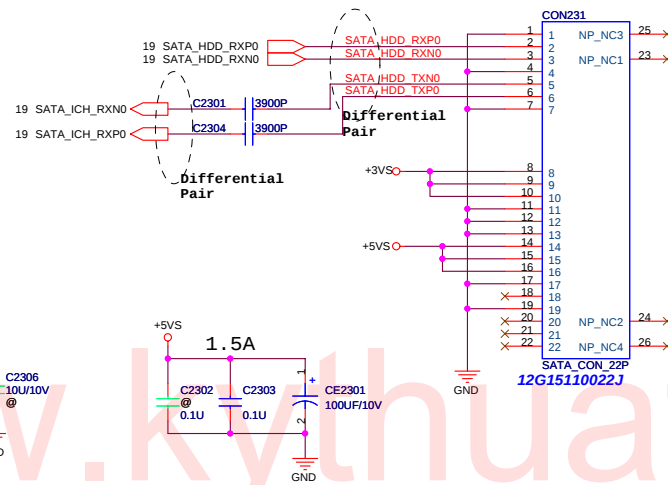
R1.1--Item8

<Variant Name>

ASUS		Title : ICH7M (2)	
ASUSTek COMPUTER INC		Engineer:	
Size Custom	Project Name F9J		Rev 2.0
Date: Thursday, November 23, 2006		Sheet	20 of 63

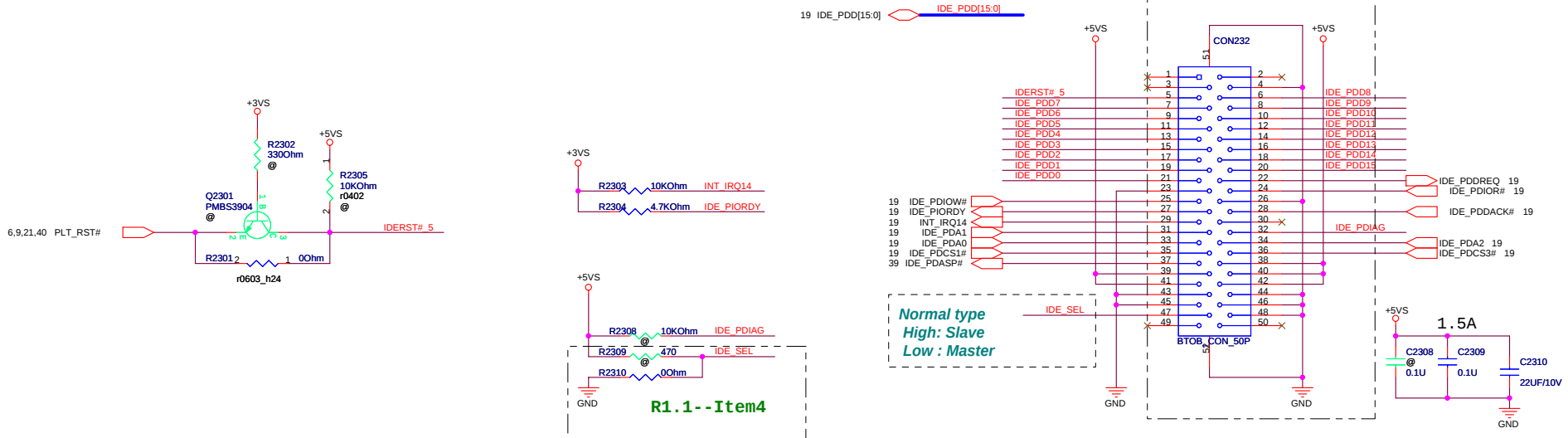


SATA HDD CON



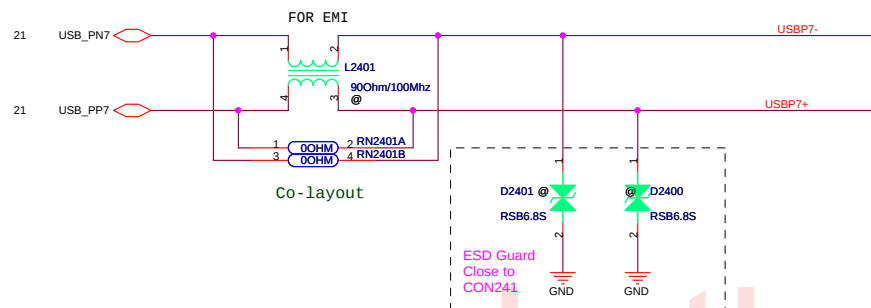
PATA CD-ROM CON

P/N:12G161240501

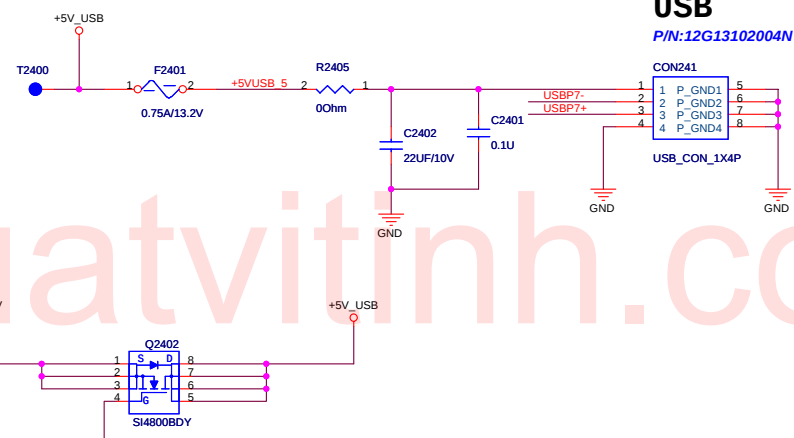


<Variant Name>

ASUS		Title : HDD & CDROM	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9J		2.0
Date: Thursday, November 23, 2006	Sheet	23	of 63



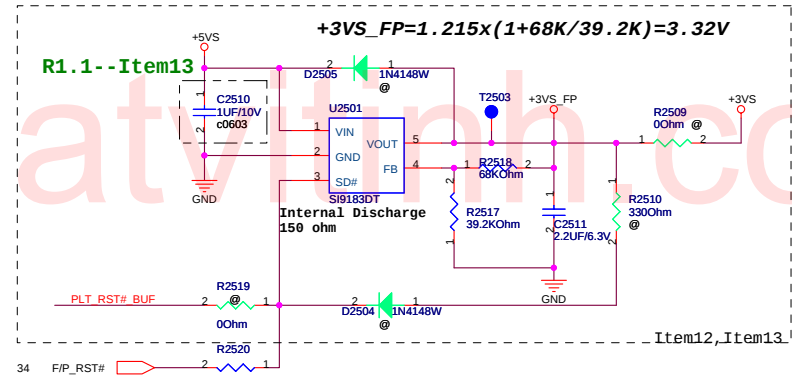
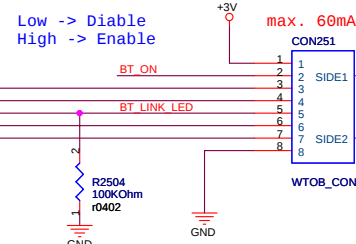
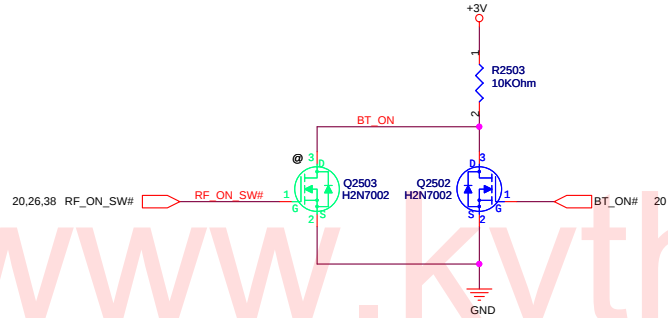
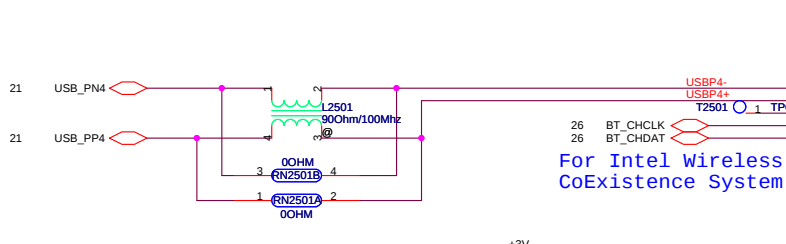
Change ESD package for layout placement.



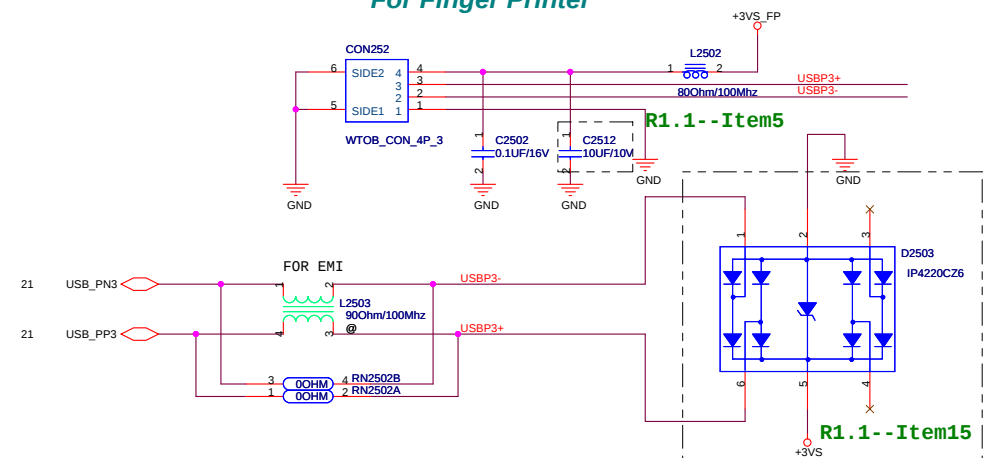
<Variant Name>

		Title : USB PORTS	
ASUSTek COMPUTER INC		Engineer:	
Size Custom	Project Name F9J		
Date: Thursday, November 23, 2006		Sheet	24 of 63

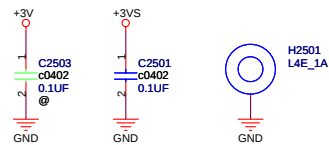
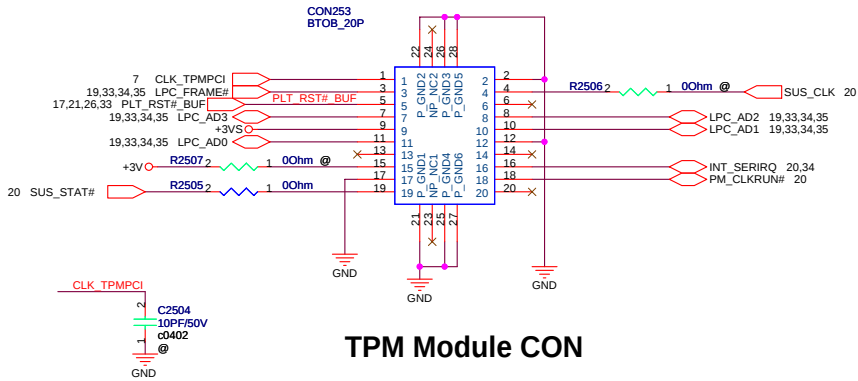
Co-layout FOR EMI



For Finger Printer



TPM Module CON



<Variant Name>

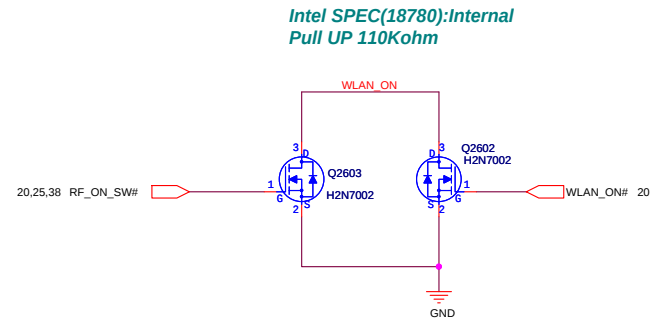
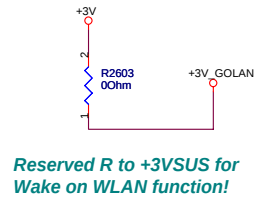
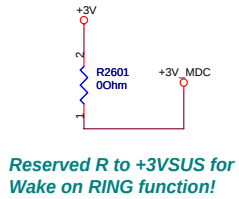
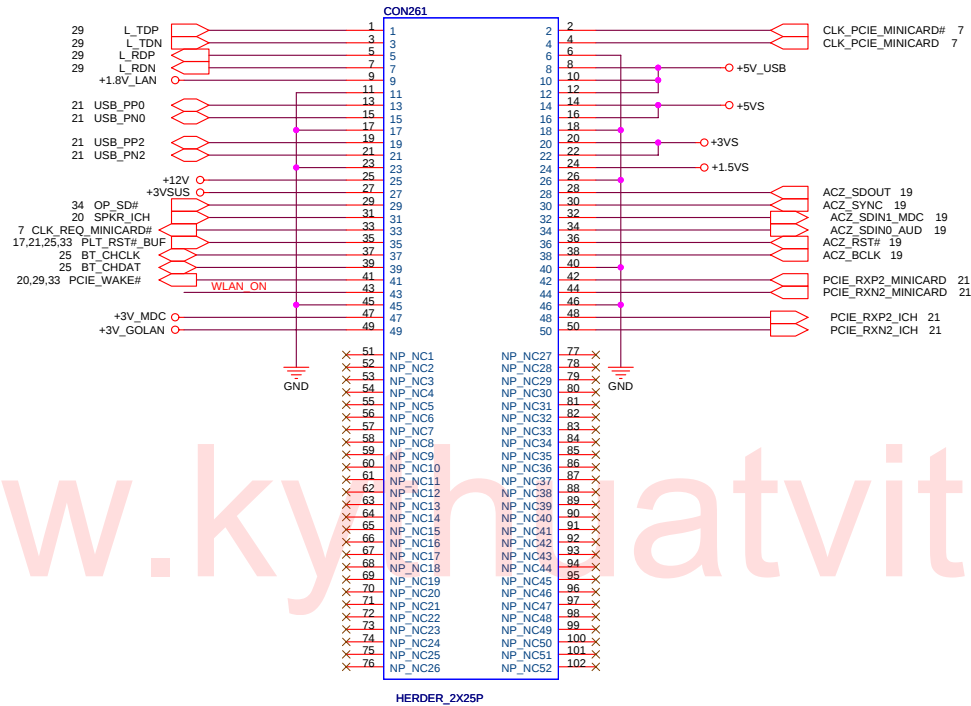
ASUS		Title : BIT,FIP& TPM	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F9J	2.0	
Date: Thursday, November 23, 2006	Sheet	25	of 63

POWER CONSUMPTION:
+3VS: +3.003V~+3.597V
Max= 750 mA

+1.5VS: +1.425V~+1.575V
Max= 375 mA

+3VAUX_GOLAN: +3.003V~+3.597V
Max= 250 mA

+3VAUX_MDC: +3.003V~+3.597V
Max= 300 mA



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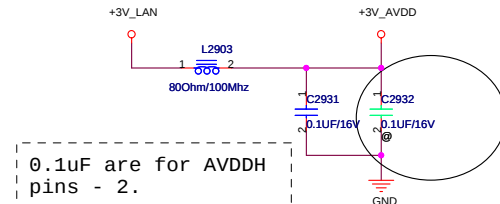
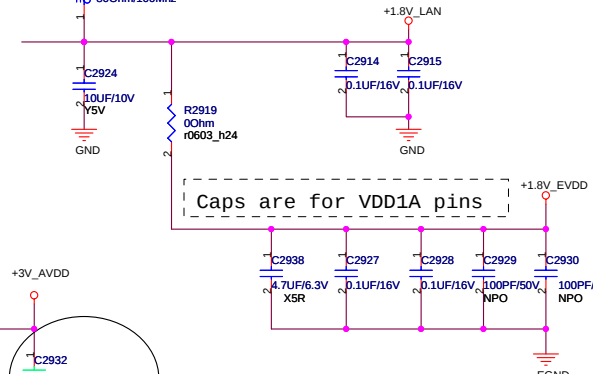
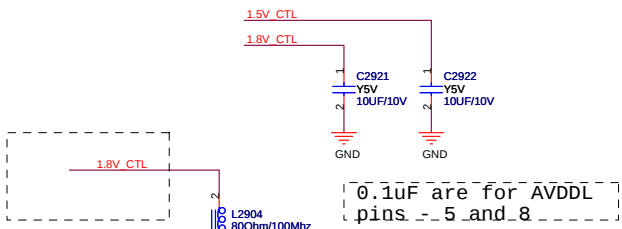
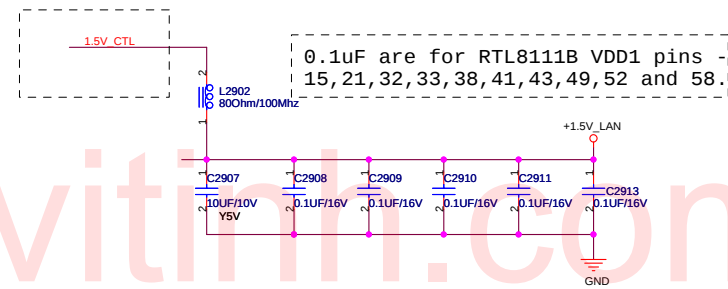
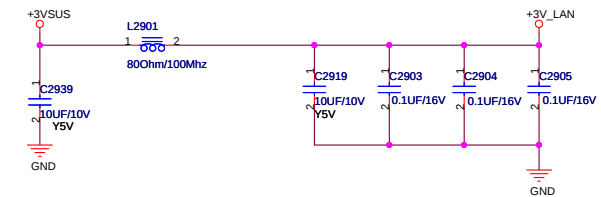
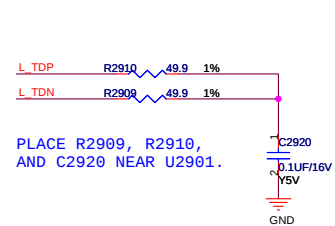
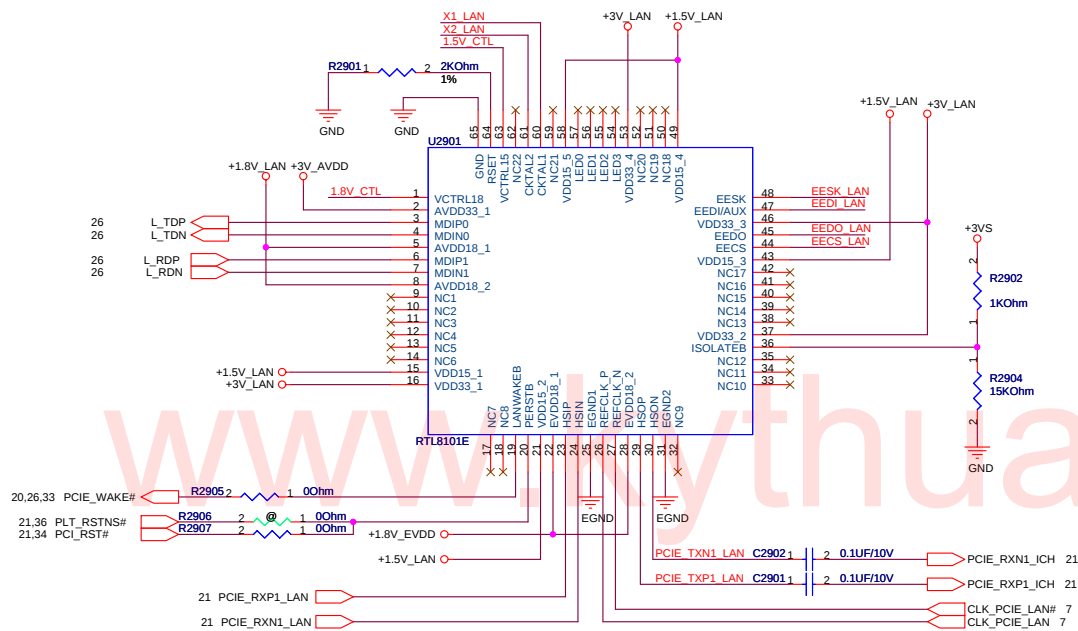
<Variant Name>

		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9F		2.0
Date: Thursday, November 23, 2006		Sheet	27 of 63

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<Variant Name>

		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9F		2.0
Date: Thursday, November 23, 2006		Sheet	28 of 63



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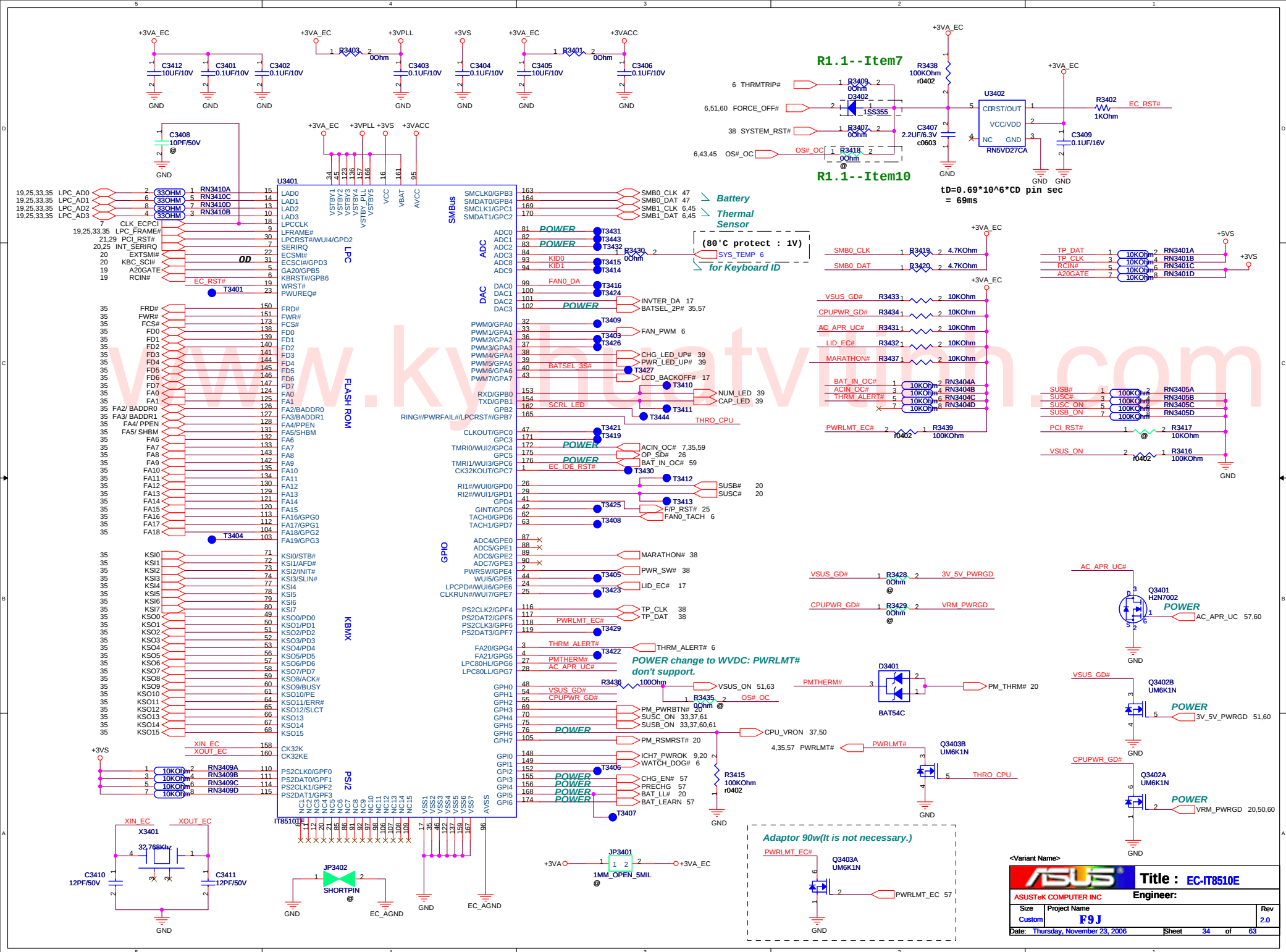
		Title : EMPTY	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9J		2.0
Date: Thursday, November 23, 2006		Sheet	30 of 63

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		Title : EMPTY	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9J		2.0
Date: Thursday, November 23, 2006		Sheet	31 of 63

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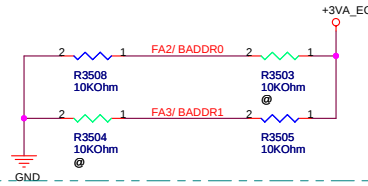
<Variant Name>		
		Title : EMPTY
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
Custom	F9J	2.0
Date: Thursday, November 23, 2006		Sheet 32 of 63



EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

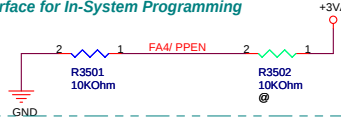
- 00: PNPCNG Access Register Pair Are 002Eh and 002Fh
 10: PNPCNG Access Register Pair Are 004Eh and 004Fh
 01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
 11: Reserved



Note: Sampled at VSTBY Power Up Reset

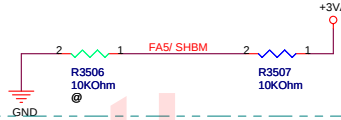
FA4/ PPEN

- 0: Normal
 1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

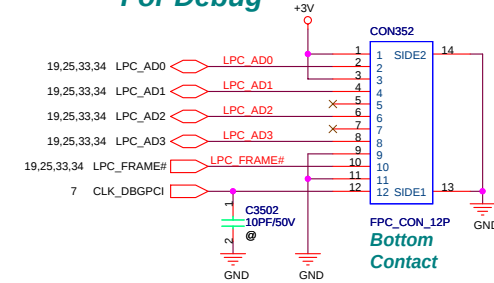


FA5/ SHBM

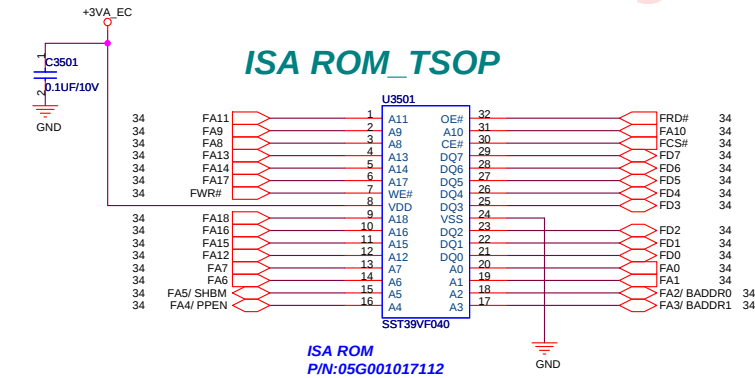
- 0: Disable Shared Memory with Host BIOS
 1: Enable Shared Memory with Host BIOS



For Debug

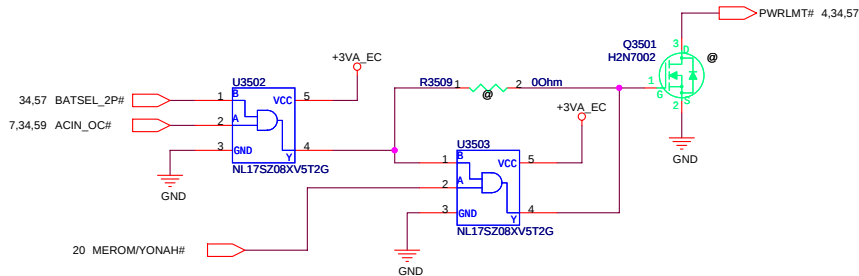
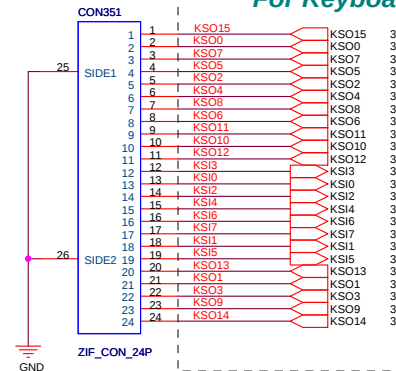


ISA ROM_TSOP



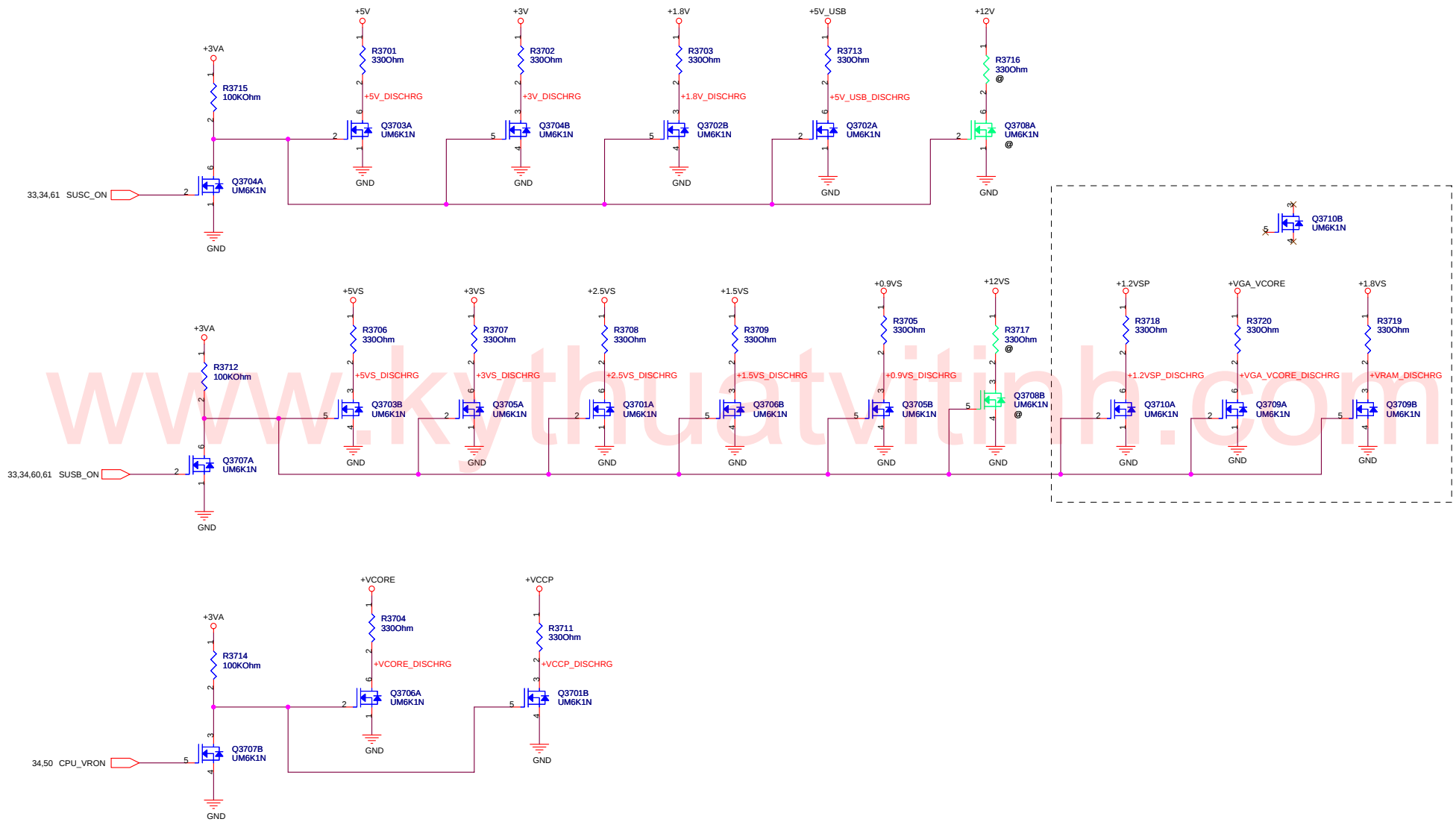
P/N:12G182402404

For Keyboard



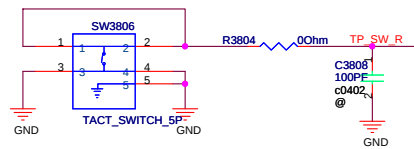
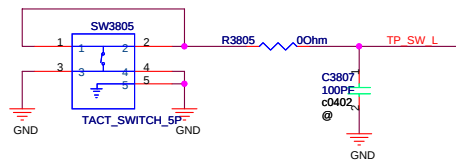
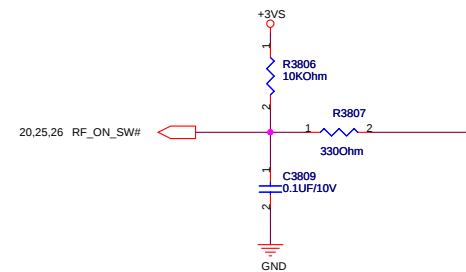
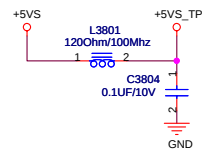
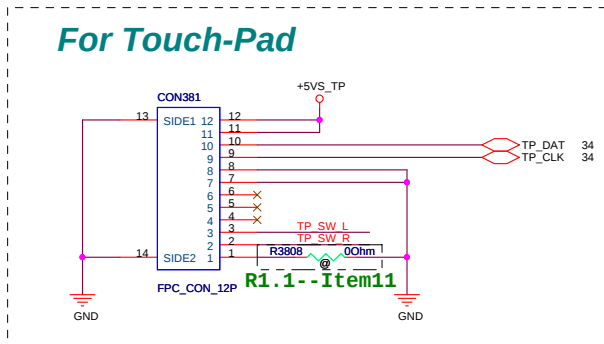
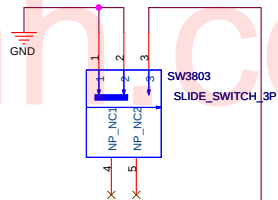
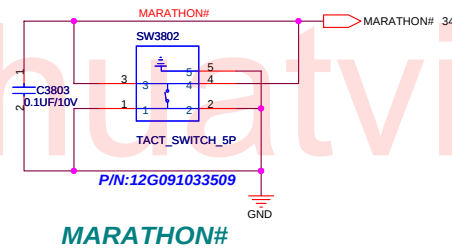
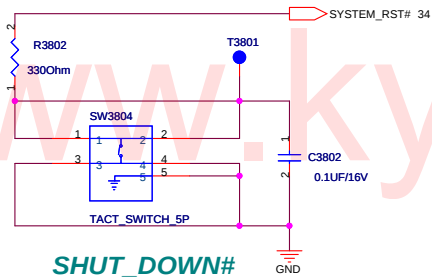
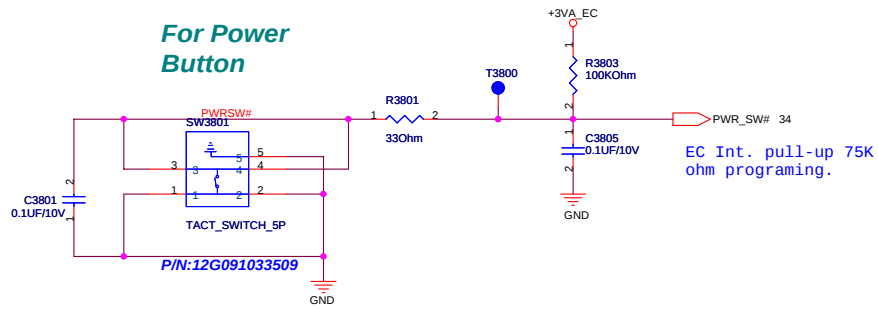
<Variant Name>

ASUS		Title : ISA_ROM&KB conn	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9J		2.0
Date: Thursday, November 23, 2006	Sheet	35	of 63



<Variant Name>

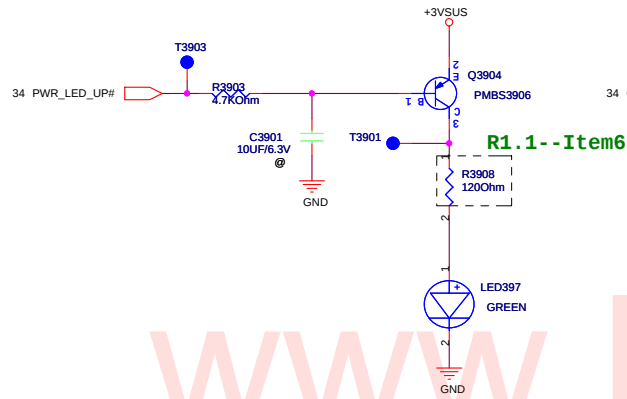
ASUS		Title : DISCHARGE	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9J		2.0
Date: Thursday, November 23, 2006		Sheet	37 of 63



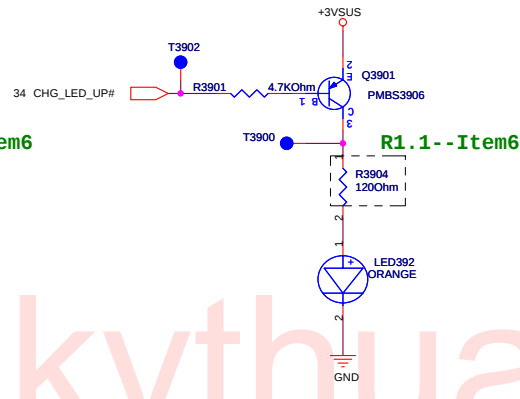
<Variant Name>

ASUS		Title : KEY & LED	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F9J	2.0	
Date:	Thursday, November 23, 2006	Sheet	38 of 63

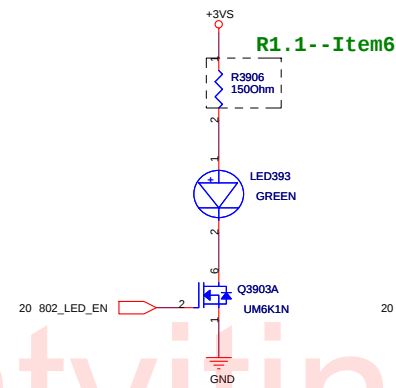
For PWR LED



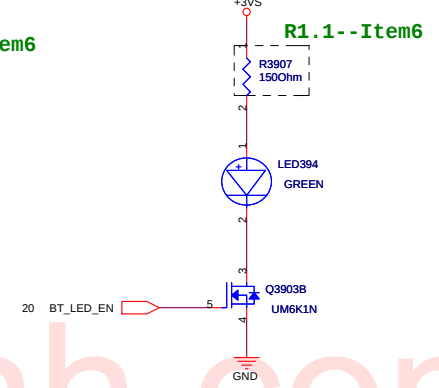
For BATTERY LED



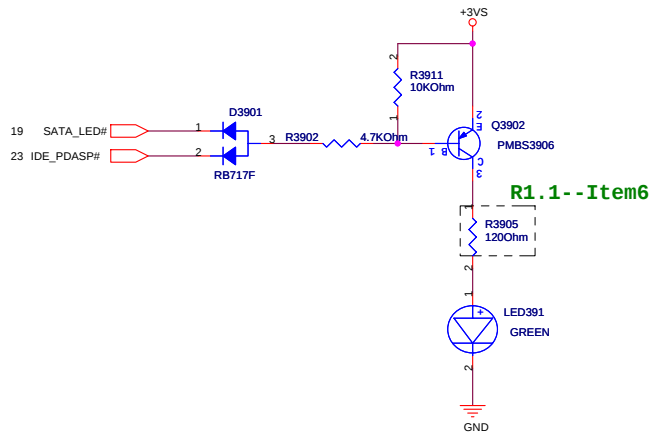
For WireLess LED



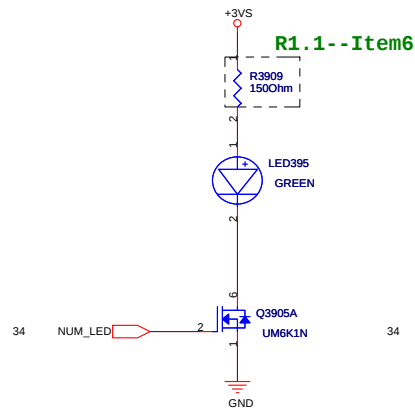
For BT LED



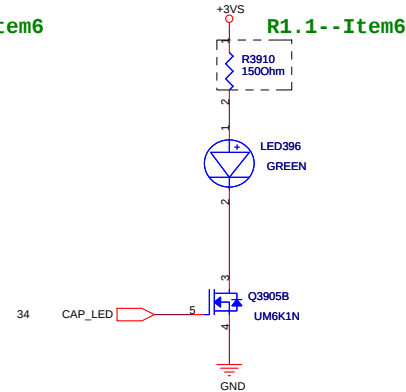
For SATA/IDE LED



For Num Lock

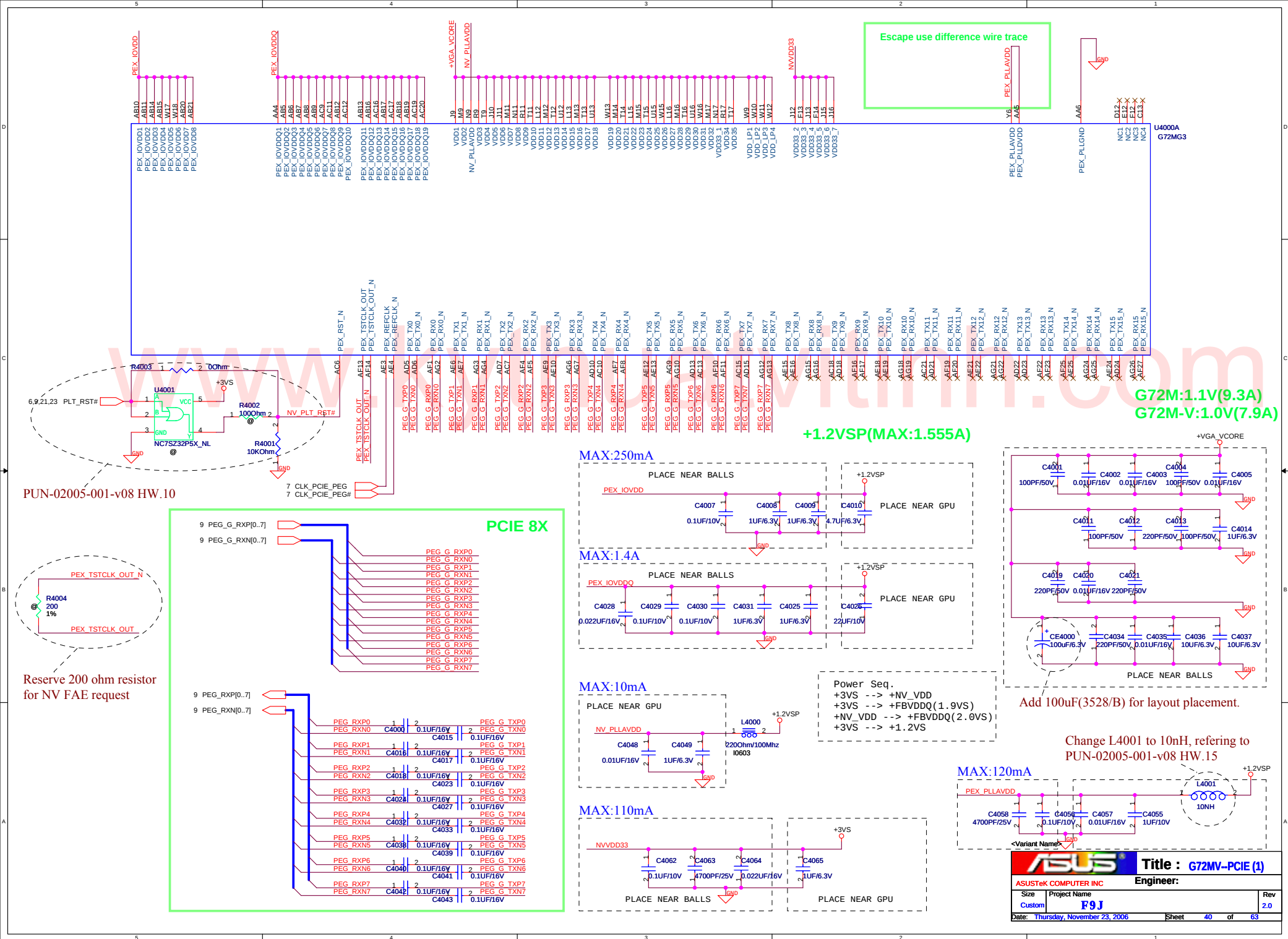


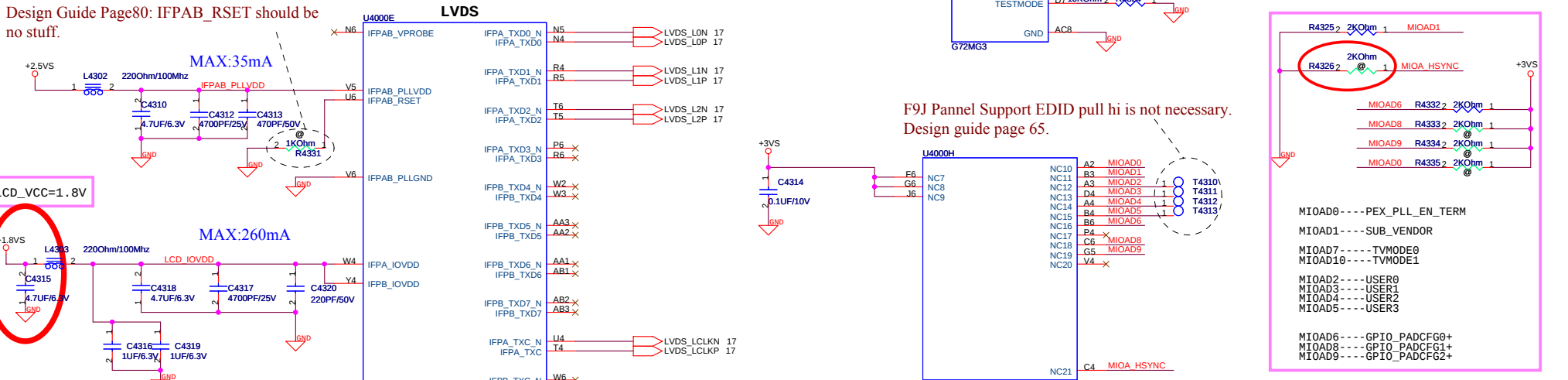
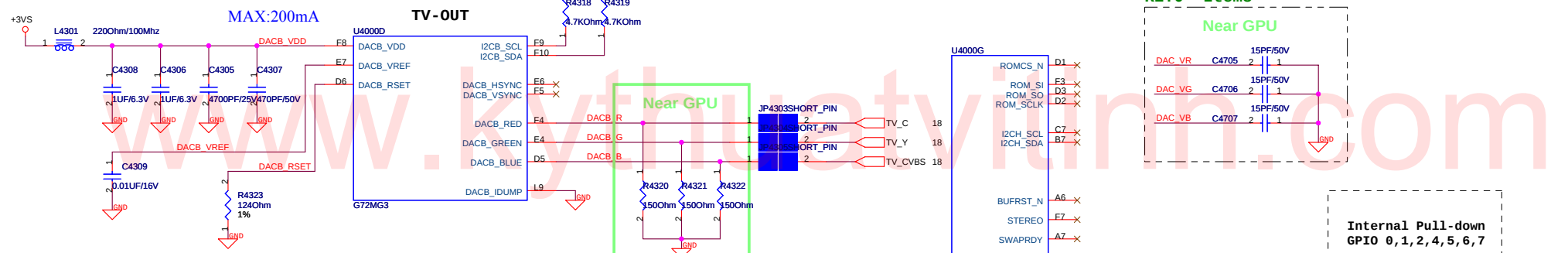
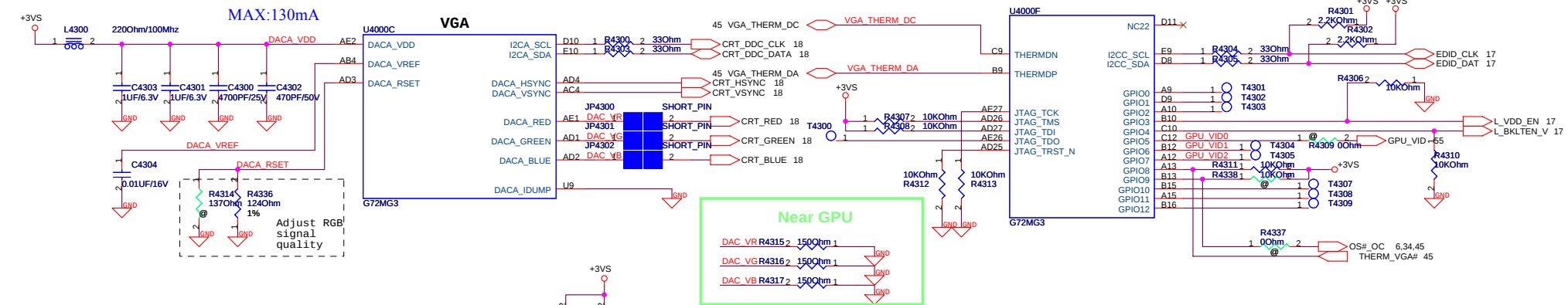
For Cap. Lock



<Variant Name>

ASUS		Title : LEDs	
ASUSTek COMPUTER INC		Engineer:	
Size Custom	Project Name F9J	Rev 2.0	
Date: Thursday, November 23, 2006		Sheet	39 of 63





Design Guide Page80: IFPAB_RSET should be no stuff.

+LCD_VCC=1.8V

F9J Pannel Support EDID pull hi is not necessary. Design guide page 65.

Internal Pull-down GPIO 0,1,2,4,5,6,7

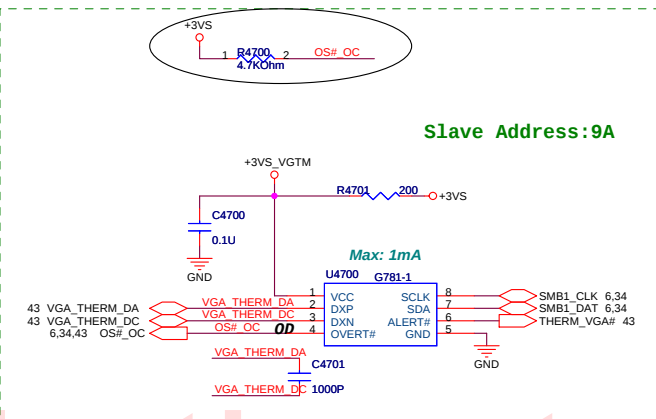
ASUS Title : G72MV-I/O (4)

ASUSTek COMPUTER INC Engineer:

Size Custom Project Name F9J Rev 2.0

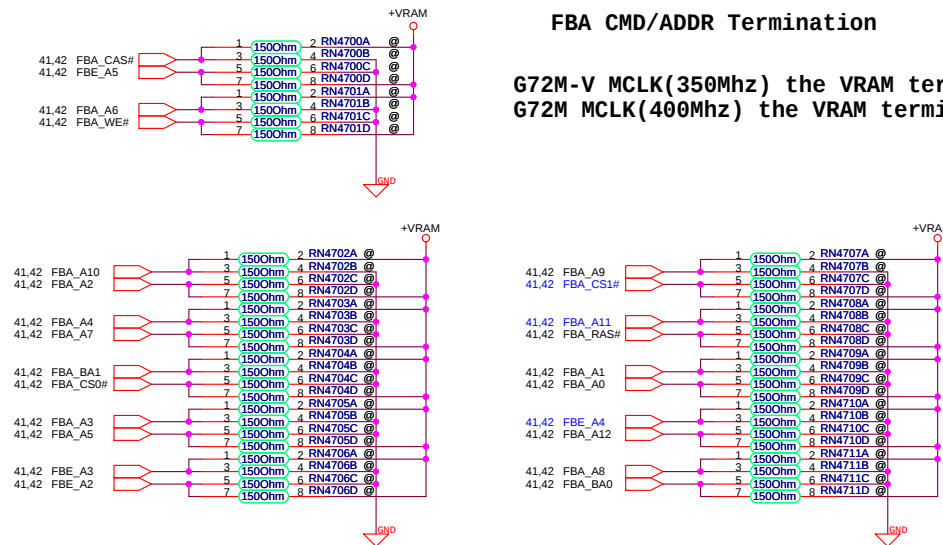
Date: Thursday, November 23, 2006 Sheet 43 of 63

OS#_OC connector to EC U3402(pin5) DNI R4700



FBA CMD/ADDR Termination

G72M-V MCLK(350Mhz) the VRAM termination is not necessary.
G72M MCLK(400Mhz) the VRAM termination is necessary.



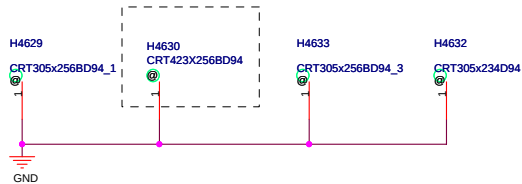
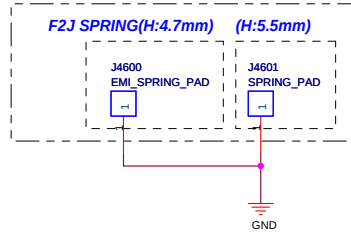
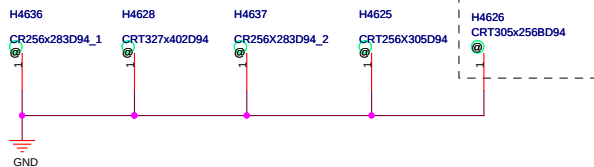
CMD/ADDR termination resistors 150ohm. Design Guide Page47

<Variant Name>

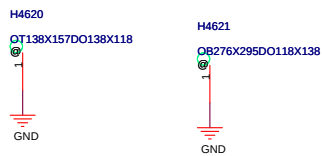
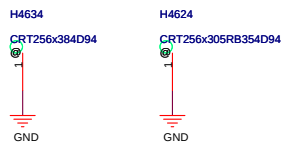
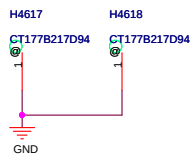
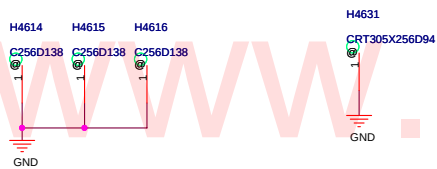
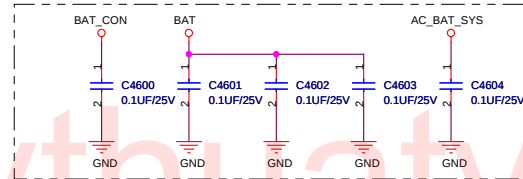
ASUS		Title G72MV-VRAM_TERM	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9J		2.0
Date: Thursday, November 23, 2006	Sheet	45	of 63

R1.1--Item12 EMI SPRING

F2J SPRING(H:4.7mm) (H:5.5mm)



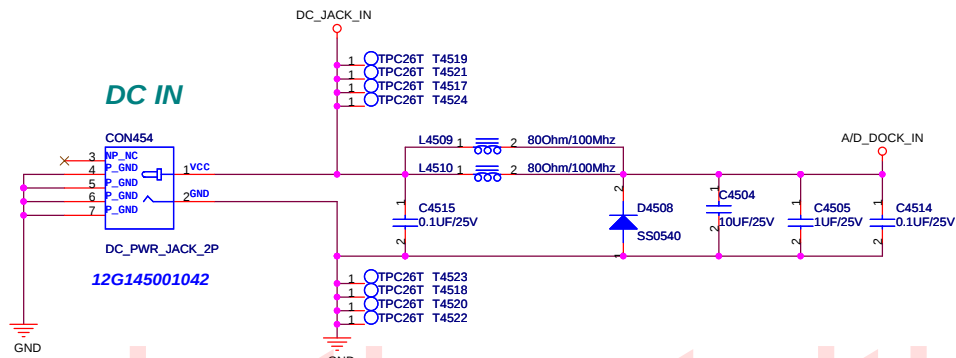
R1.1--Item13



<Variant Name>

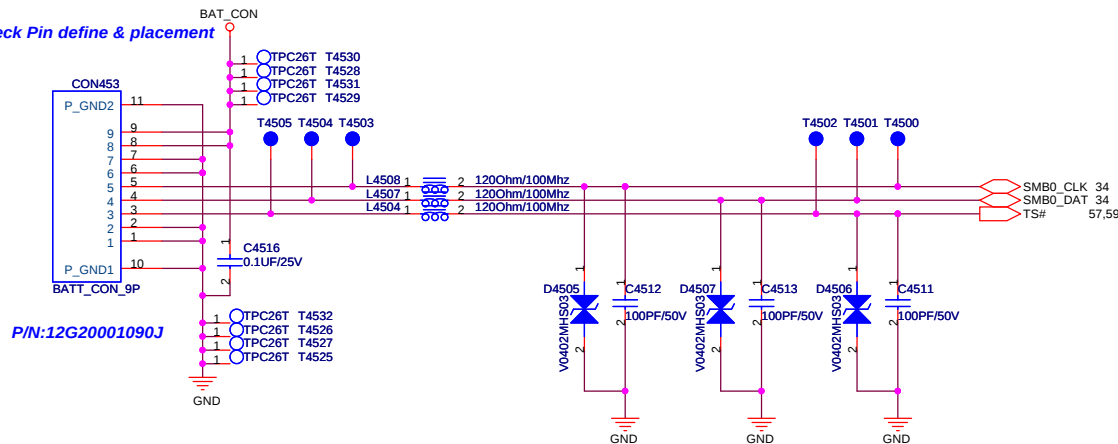
ASUS		Title : HDD & CDROM	
ASUSTeK COMPUTER INC.		Engineer:	
Size	Project Name	Rev	
Custom	F9J	2.0	
Date: Thursday, November 23, 2006	Sheet	46	of 63

DC IN



BAT IN

Check Pin define & placement



<Variant Name>

ASUS		Title : G72M-Terminator	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F9J	2.0	
Date: Thursday, November 23, 2006	Sheet	47	of 63

F9J SR_0928(R1.0---->R1.1)

- (1)Change the s-vedio CON(CON182) to 12G14101107K for SMT issue.---page18.
- (2)R1707 change from 10Kohm to 100Kohm to solve the LCD flash during warm boot.---Page17
- (3)CON361(4 in 1) change to 12G340003800 to solve the factory yield rate issue.---Page36
- (4)Add R2309 and R2310 for IDE select---Page 23
- (5)Add C2512(10UF/10V) for FP power---Page 25
- (6)Change R3904,R3905 and R3908 to 120 ohm, change R3906,R3907,R3909 and R2910 to 150 ohm to control LED current is about 10mA.---Page 39
- (7)Del R3418, R3408,R617 and Q605,and add D3402 and D3403 for the OS#_OC function.---Page6; Page 34
- (8)Reserved R2038 10K for GPIO10 pull high and R2039 10K for GPIO25 pull high.---Page 20
- (9)Add NPTH H3301 & H3302 for New Card EJECTOR CON for ME request.---Page33
- (10)Modify OS#_OC schematic: add R617 ; Q605 & reserved R3418.---Page6; Page34.
- (11)Reserved R3808 0 ohm to support ALPS TP.---Page38
- (12)Add J4600;J4601 EMI SPRING for EMI request.---Page46
- (13)Change C2510 from 0.1u to 1uF for FP power.---Page25
- (14)Reserved Change Cap C4600-C4604(0.1uF) for ESD issue of Buttom floating part ---Page46
- (15)Mount voltage protector on D2503 for ESD issue of Finger printer.---Page25
- (16)Mount 10uF capacitor on C534,C538,C533,C535,C536.---Page5
- (17)Mount 600 ohm Bead on L1814,L1815,L1816 and 100P capacitor on C1839 ~C1844 for EMI issue of S-terminal.---Page18
(ER double check signal quality).

F9J ER_1102(R1.1---->R2.0)

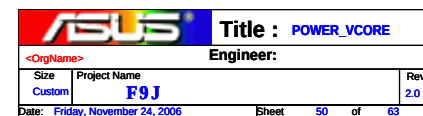
- (1) Update new CARD_EJECTOR_2P(CON332) footprint(add 2 npth hole) & remove 2 npth hole(H3301;H3302).---Page33
- (2) Change the ODD CON(CON232) from 12G16121050P to 12G161240501 for ME request.(Board lock hole:1.8mm; 3.0H)---Page23
- (3) Change the TV filter circuit. (Follow G72M design guide); this circuit can pass TV signal quality & EMI testing.---Page18
- (4) Change R1816 & R1817 from 0ohm to 33ohm; mount cap 22pf on C1837 & C1838 for VSYNC/HSYNC.---Page18
- (5) R753 & R755 change from 33ohm to 0ohm for CLK_PCIE_MINICARD#/CLK_PCIE_MINICARD signal quality.---Page7
- (6)CON361 change from 12G340003800 to 12G340003810 to improve the yield rate.---Page36
- (7)Add test point for factory request:
T1910(+RTCBAT);D1901 PIN2(T1911);+5V_USB(T2400);BAT_LL#(T3407);PWRSW#(R3801_2)(T3800);CHG_LED_UP(Q3901_3)(T3900);PWR_LED_UP(Q3904_3)(T3901).
- (8)For CRT signal quality & EMI issue change the filter components:
 - a.L1811-L1813 change to 0.082uH
 - b.C1831;C1833;C1835 change from 15pF to 22pF.
 - c.C1832;C1834;C1836 change from 22pF to 2pF.
 - d.Add C4705;C4706;C4707 15pF.
- (9)Change the card reader fuse(F3601) from 0.2A/30V to 0.5A/24V.(250mA_flash card + 77mA _ core logic)
- (10)R1806,R1807 change to L1806;L1807(120 ohm bead) to improve the noise from CRT port for EMI request.
- (11)C3658/C3655 change from 15pF to 18pF for card reader crystal adjustment.
- (12)CCD polyswitch(F1701) change to 07G014050102(RAYCHEM 500mA).

<Variant Name>

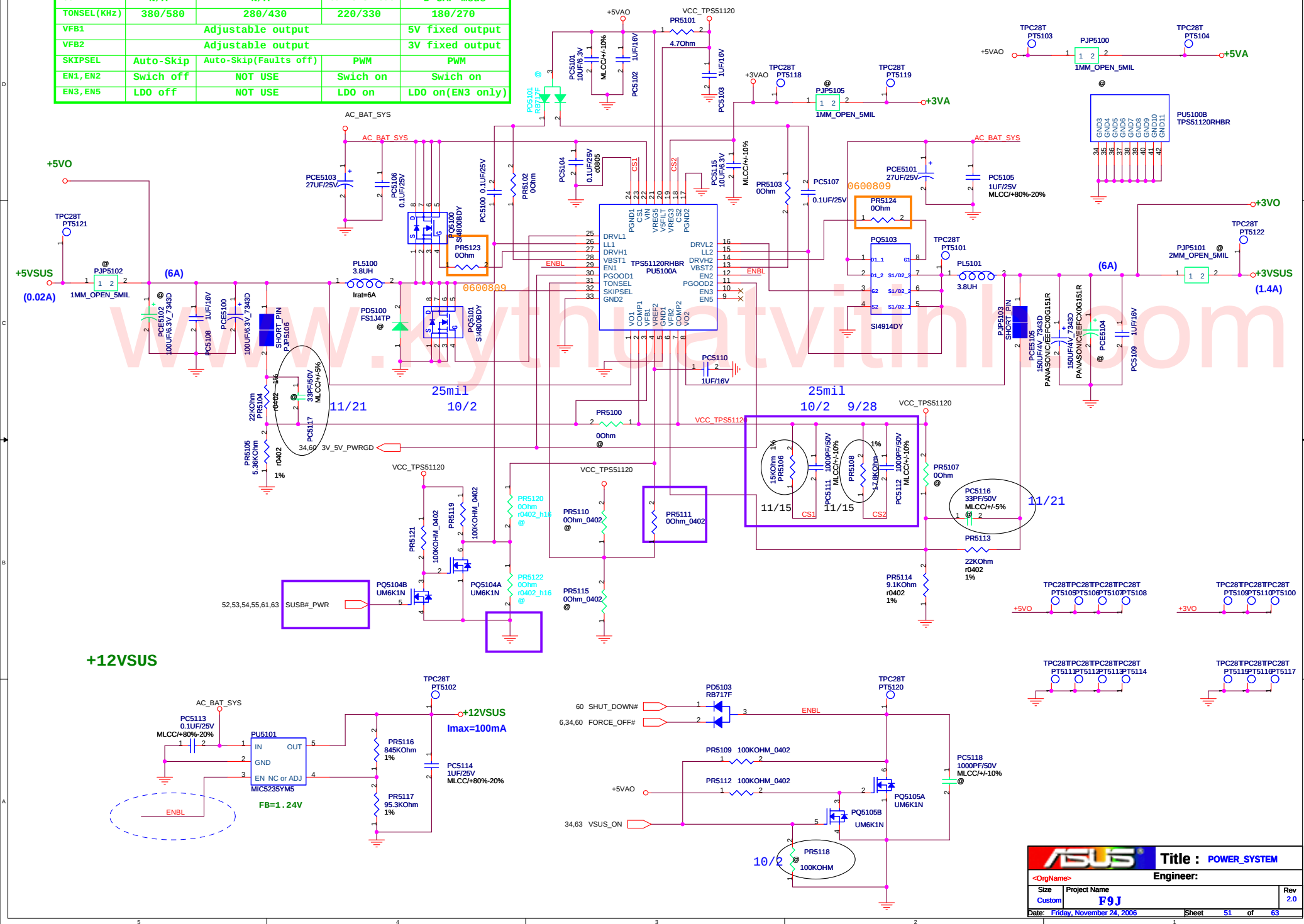
		Title : History(1)	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9J		2.0
Date:	Thursday, November 23, 2006	Sheet	48 of 63

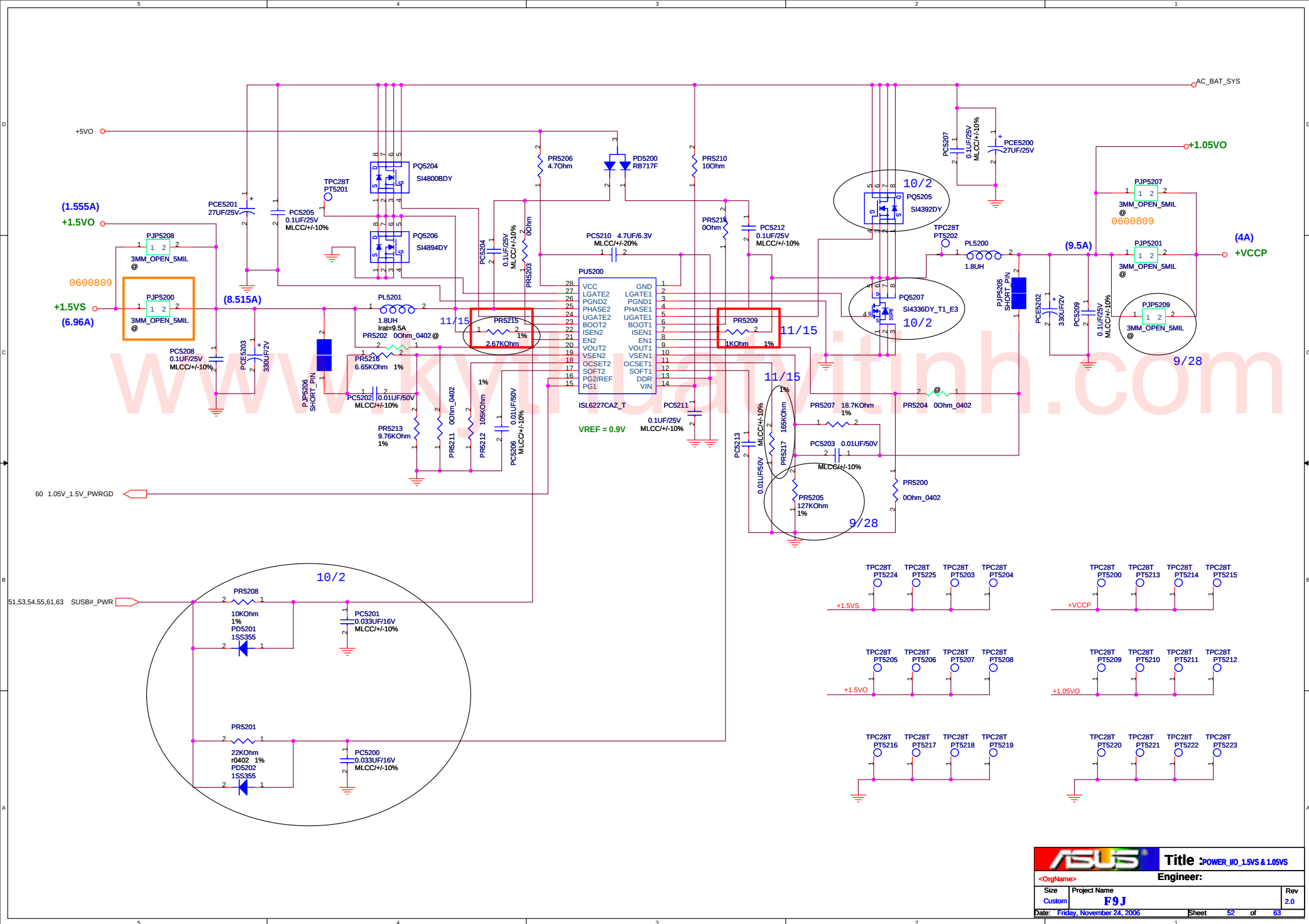
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<Variant Name>		
		Title : History(2)
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
Custom	F9J	2.0
Date: Thursday, November 23, 2006		Sheet 49 of 63



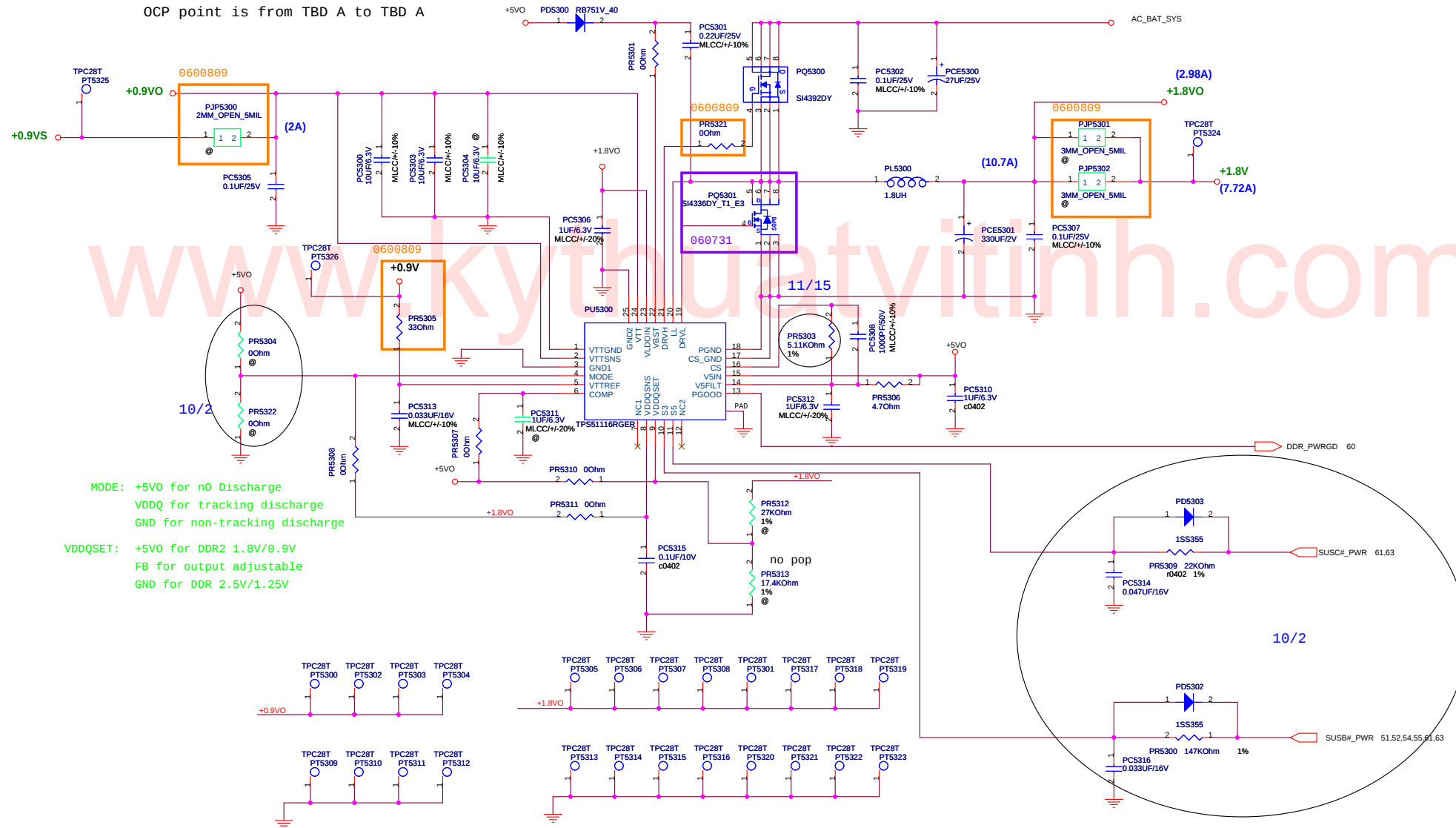
PIN	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current mode	D-CAP mode
TONSEL(KHz)	380/580	280/430	220/330	180/270
VFBI	Adjustable output		5V fixed output	
VFBI	Adjustable output		3V fixed output	
SKIPSEL	Auto-Skip	Auto-Skip(Faults off)	PWM	PWM
EN1,EN2	Swich off	NOT USE	Swich on	Swich on
EN3,EN5	LDO off	NOT USE	LDO on	LDO on(EN3 only)





.9 Volt +/-5% .9 Volt +/-5%
 Design Current:1.05A
 Maximum current:1.5A
 OCP point is from TBD A to TBD A

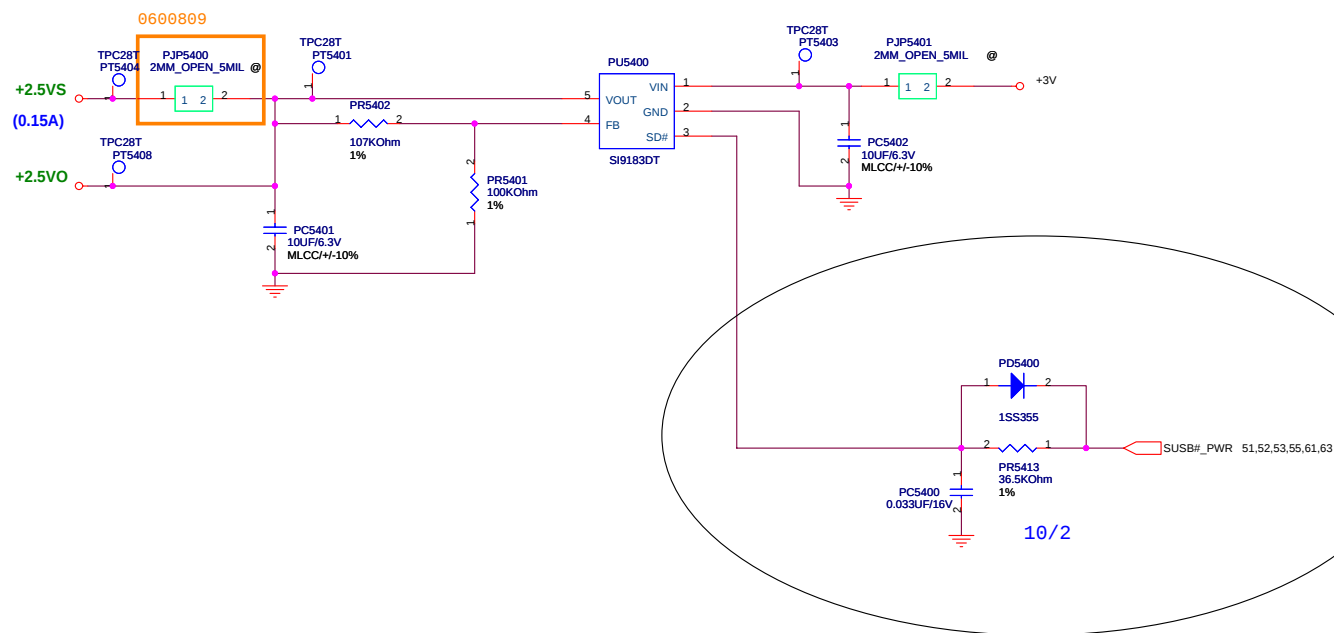
1.8Volt +/-5%
 Design Current:7.3A
 Maximum current:10.5A
 OCP point is from TBD A to TBD A

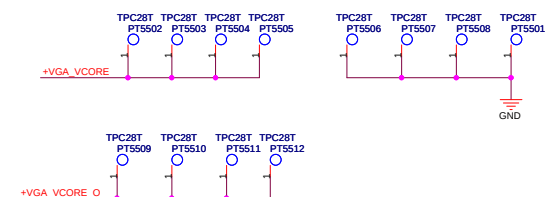
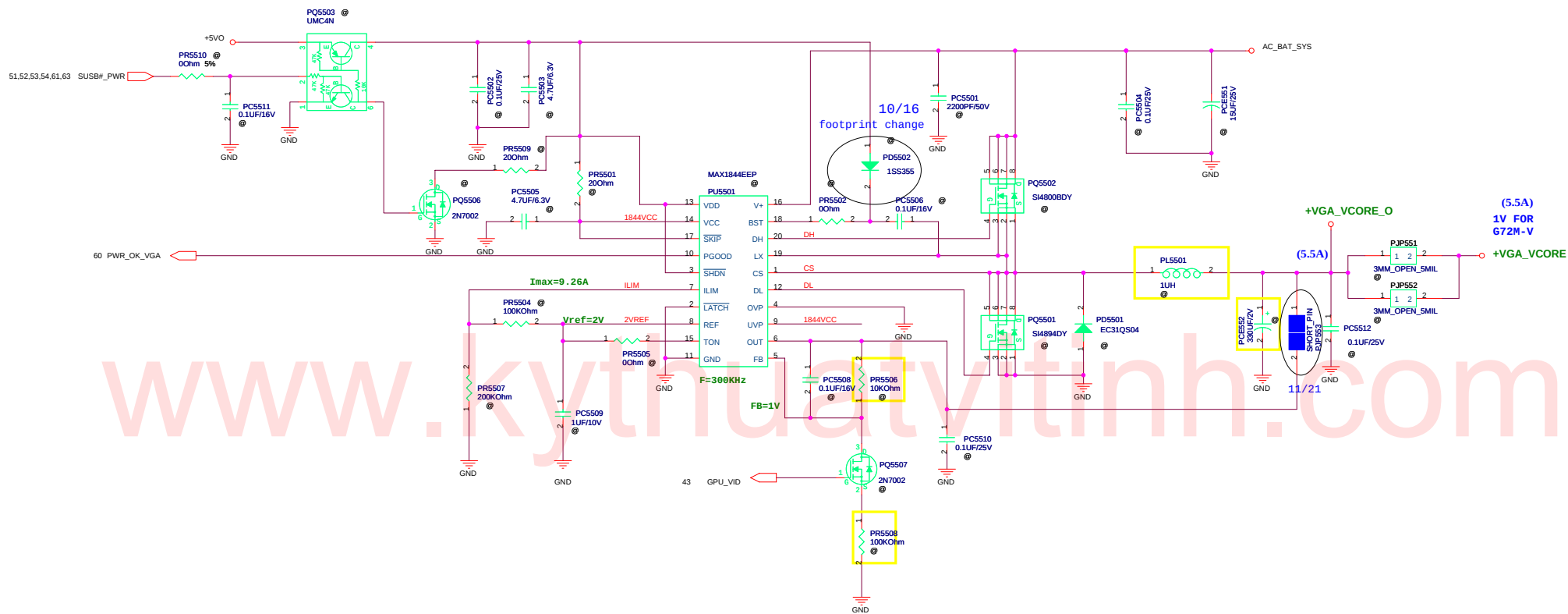


MODE: +5V0 for n0 Discharge
 VDDQ for tracking discharge
 GND for non-tracking discharge
 VDDQSET: +5V0 for DDR2 1.8V/0.9V
 FB for output adjustable
 GND for DDR 2.5V/1.25V

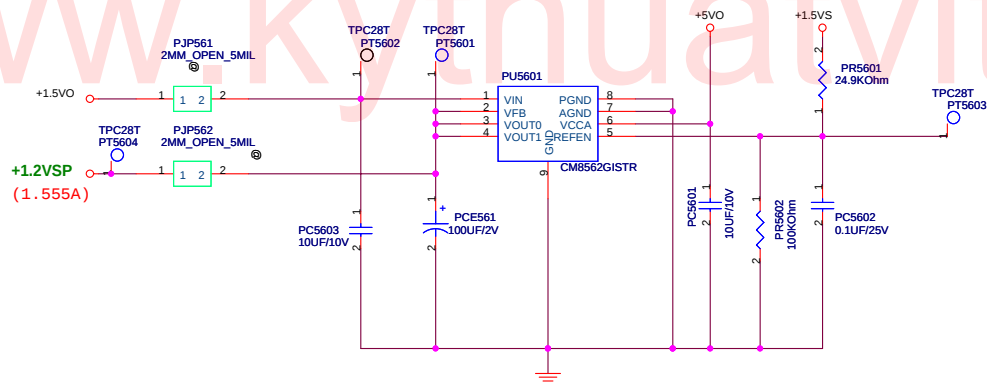
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+2.5VS

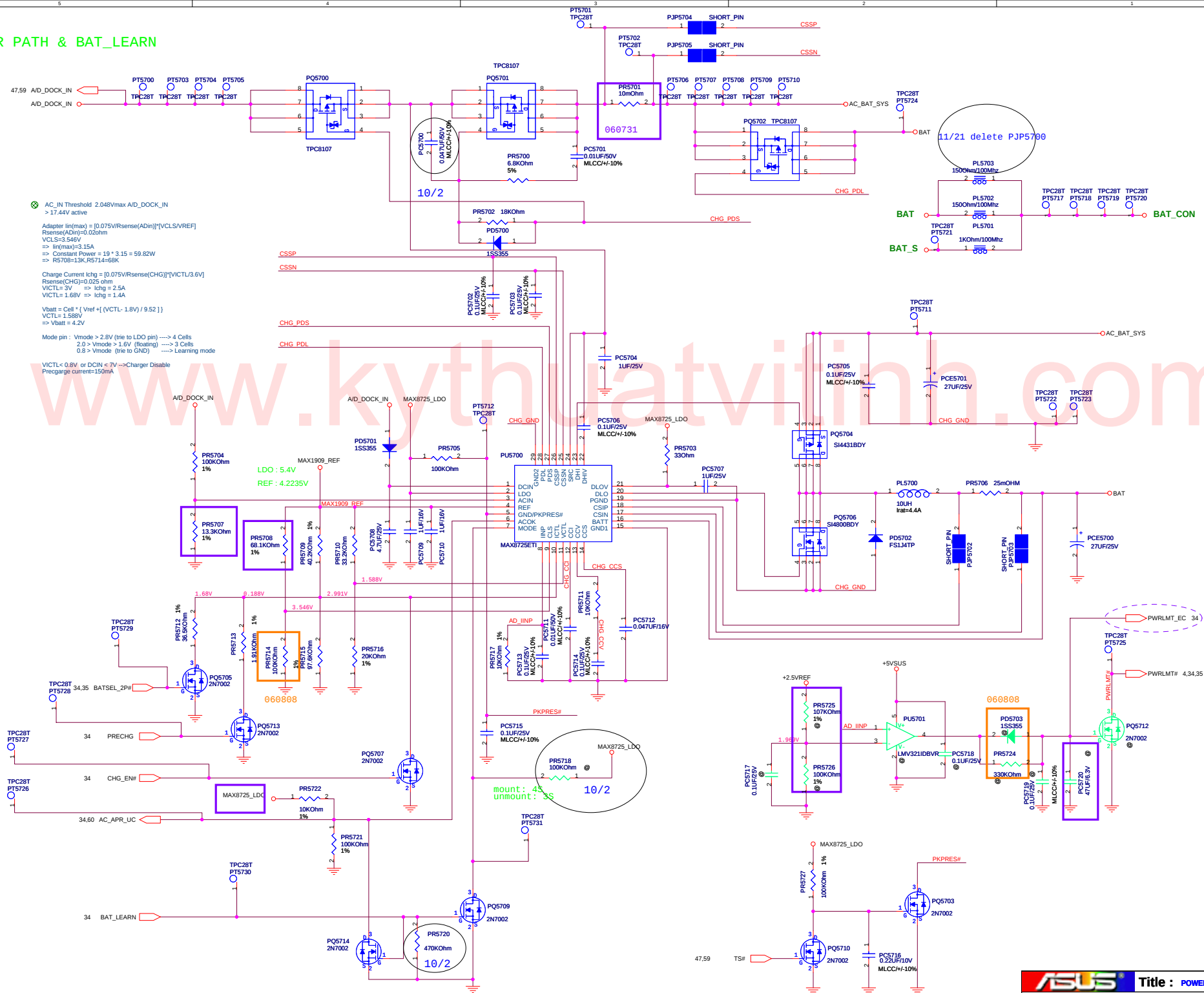




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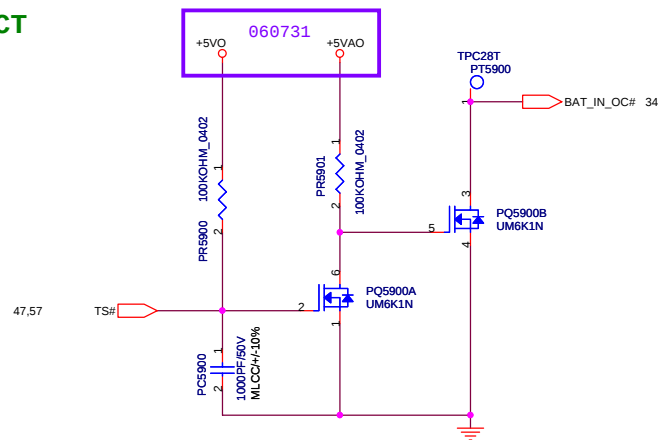
POWER PATH & BAT_LEARN



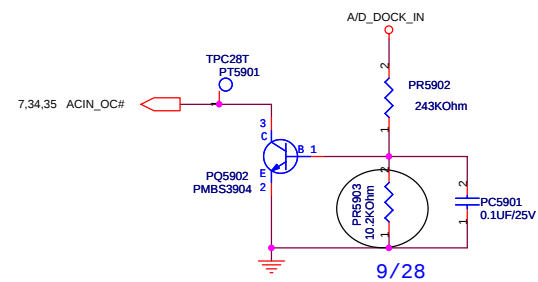
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		Title : POWER_PIC	
<OrgName>		Engineer:	
Size	Project Name		Rev
Custom	F9J		2.0
Date: Friday, November 24, 2006		Sheet	58 of 63

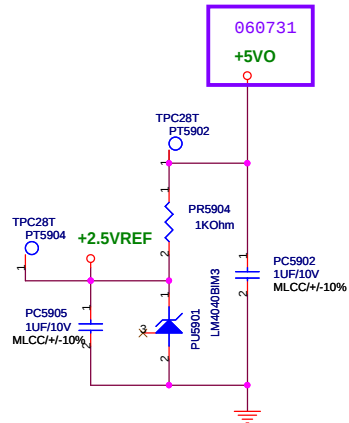
BATTERY IN DETECT

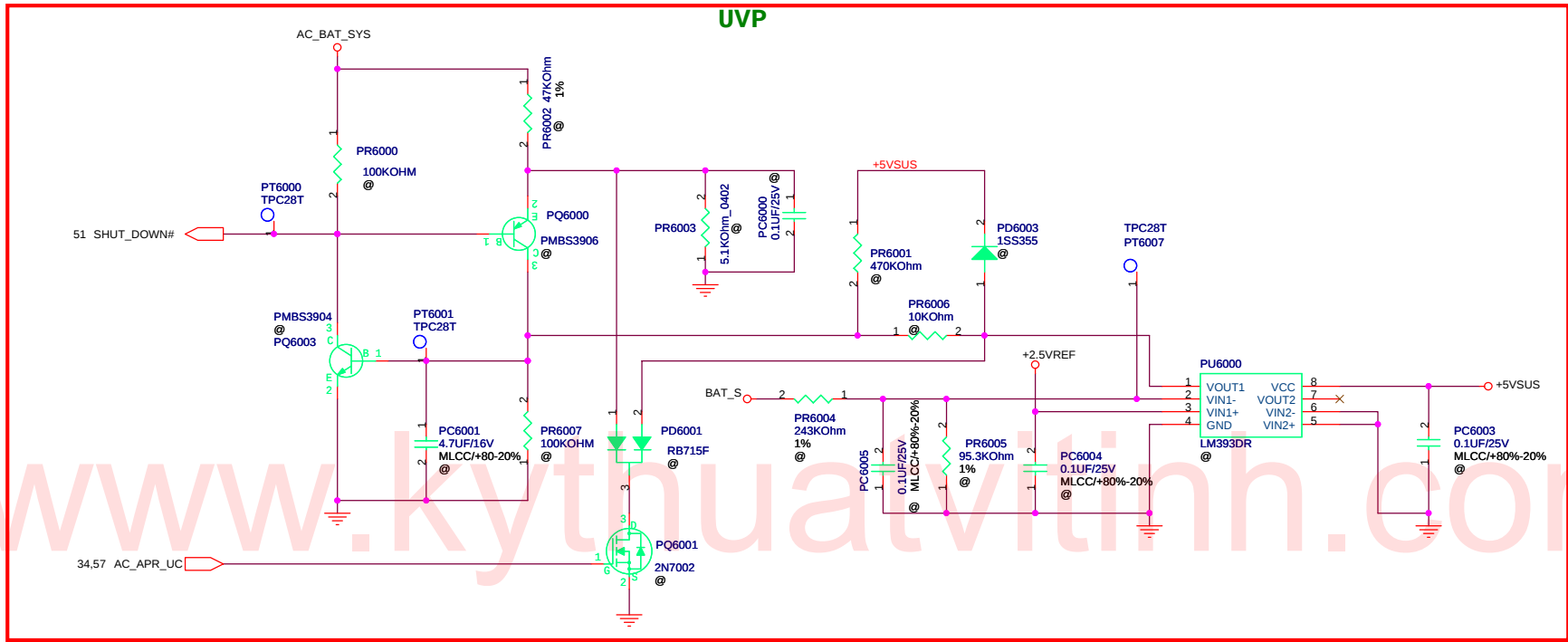


ADAPTER IN DETECT

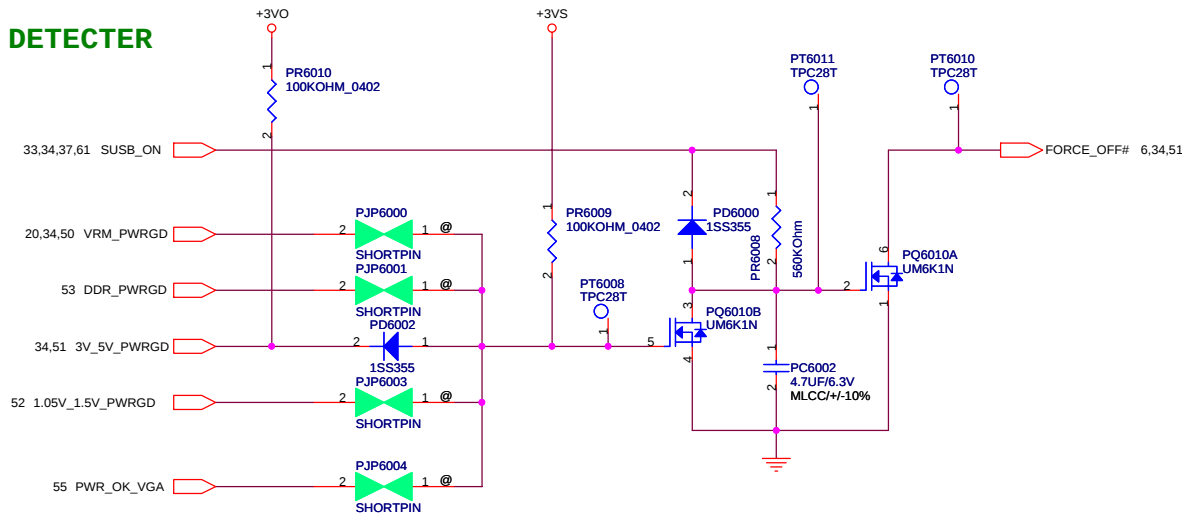


+5VLCM, +5VCHG & +2.5VREF





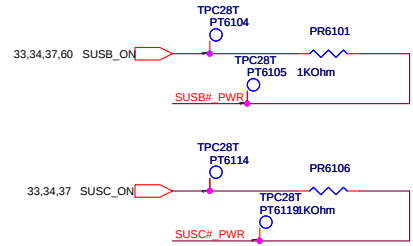
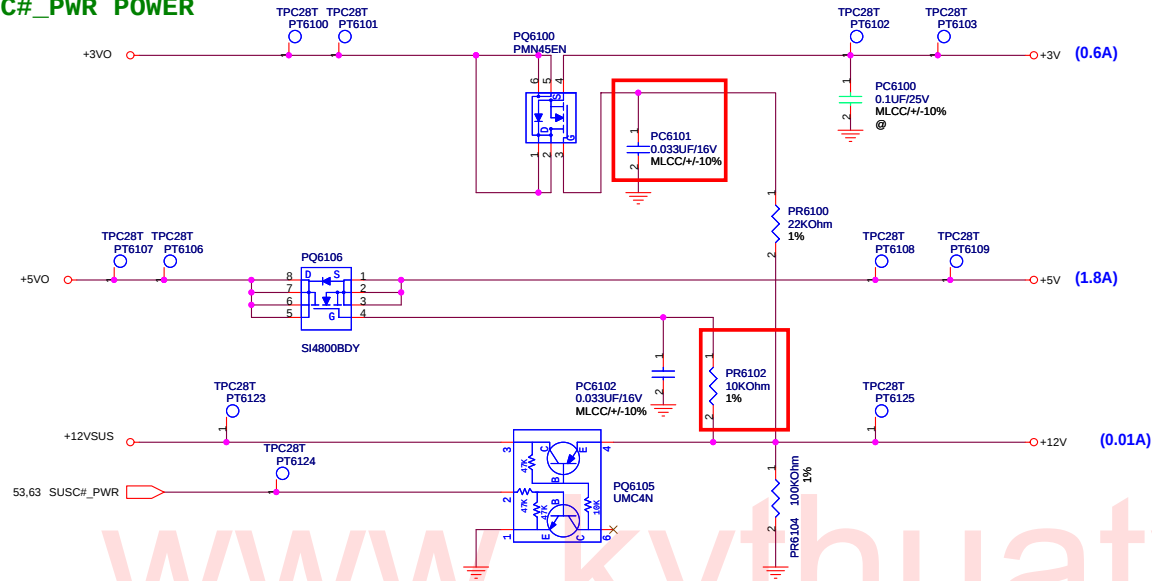
POWER GOOD DETECTOR



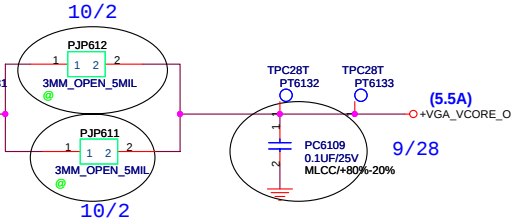
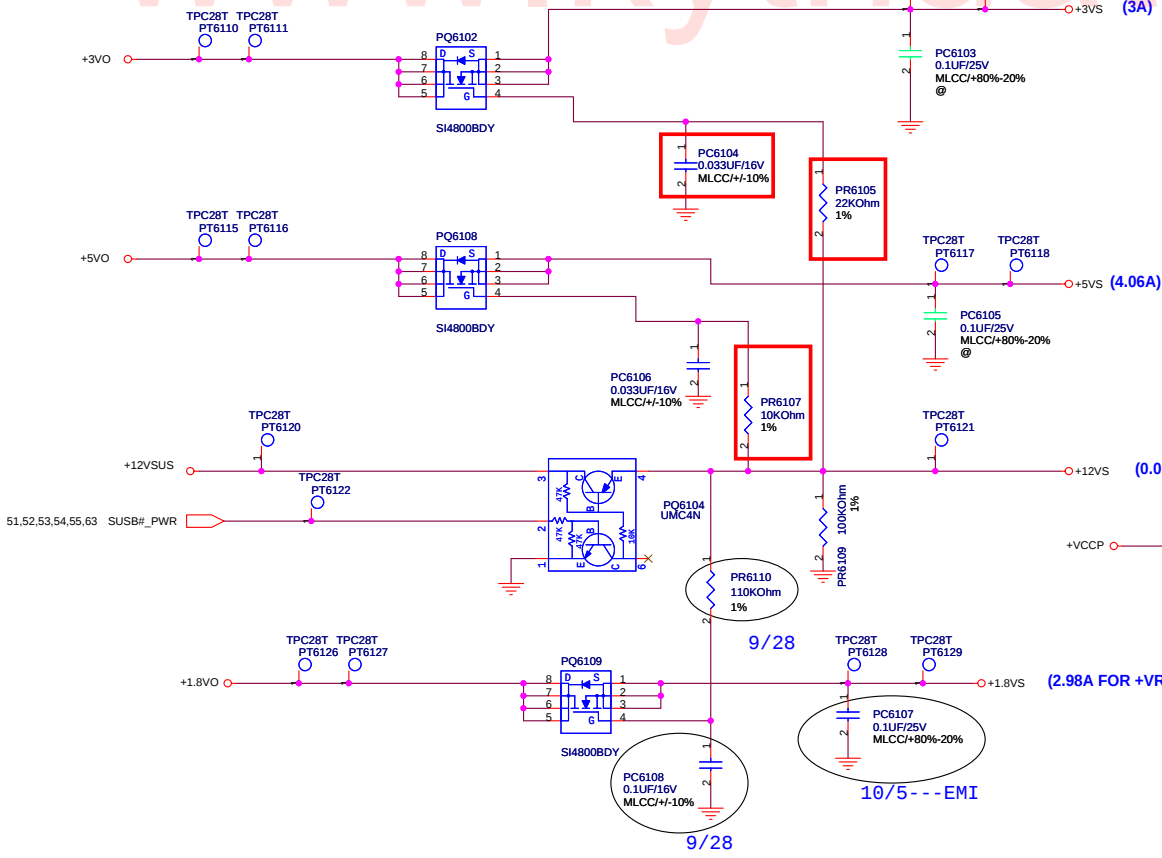
TPC28T	PT6003	VRM_PWRGD
TPC28T	PT6004	DDR_PWRGD
TPC28T	PT6005	3V_5V_PWRGD
TPC28T	PT6006	1.05V_1.5V_PWRGD
TPC28T	PT6009	PWR_OK_VGA

ASUS		Title : POWER_PROTECT	
<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom	F9J	2.0	
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SUSC#_PWR POWER



SUSB#_PWR POWER





FOR POWER TEST

