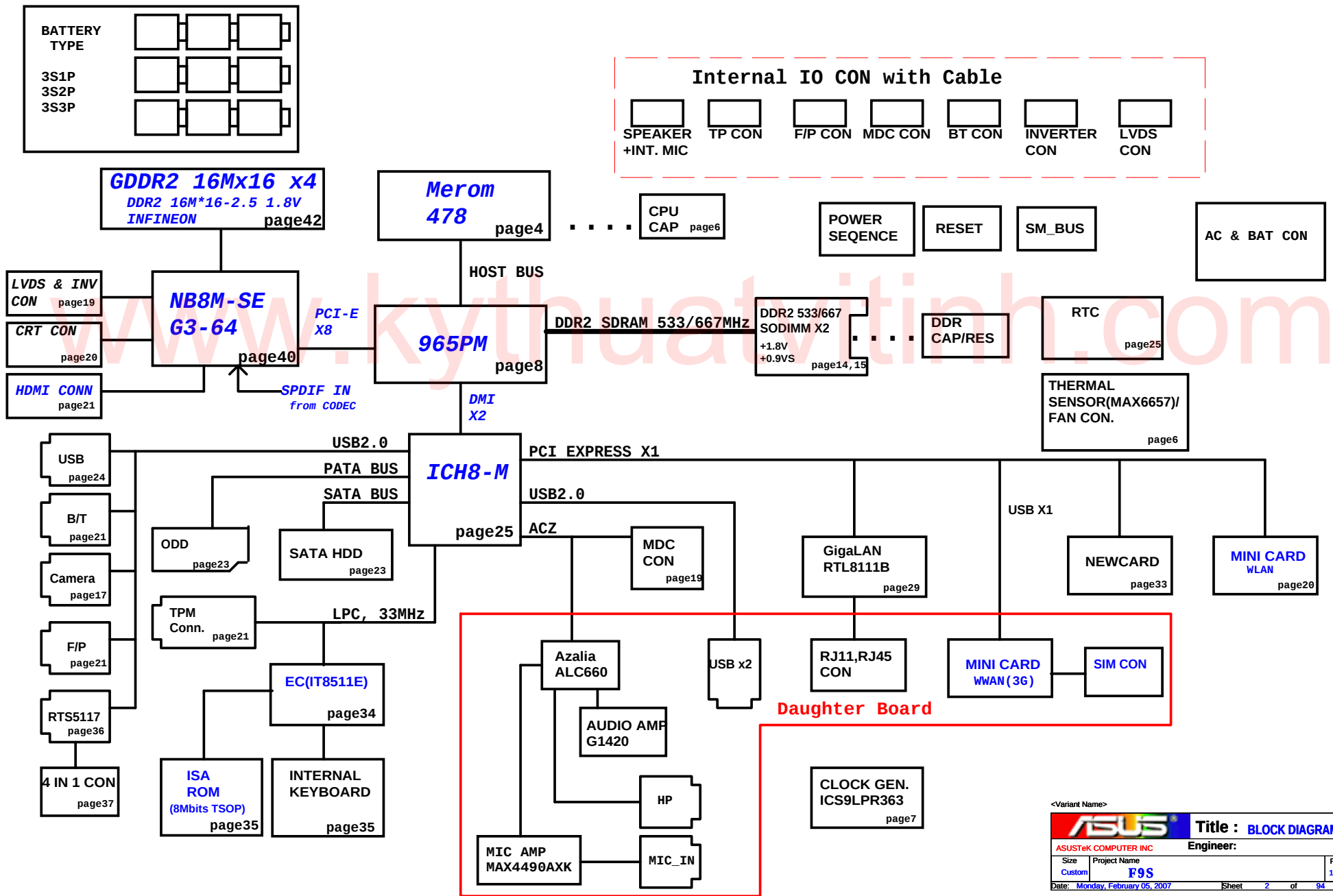


F9S SCHEMATIC Revision 1.3

[illegible]

F9S BLOCK DIAGRAM



EC-IT8511 GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	LCD_BL_PWM	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	BAT1_CNT1#	I
37	PWM3/GPA3	BAT2_CNT1#	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	O	
6	KBRST#/GPB6	RCIN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	N/A	
169	SMCLK1/GPC1	SMB1_CLK	O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	PWRLIMIT#	O
172	TMR10/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4/GPD2	BUF_PLT_RST#	O
31	ECSCI#/GPD3	EXT_SC#	I
41	GPD4	RF_ON_SW#	O
42	GIN7/GPD5	PM_SLP_M#	O
62	TACH0/GPD6	FAN0_TACH	
63	TACH1/GPD7	COLOREN#	I
87	ADC4/GPE0	BLUETOOTH#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	BAT2_IN_OC#	I
24	LPCPD#/WUI6/GPE6	WLAN_SW#	I
25	CLKRUN#/WUI7/GPE7	ME_ALERT#	O
110	PS2CLK0/GPF0	NC/PS2CLK0	O
111	PS2DAT0/GPF1	NC/PS2DAT0	I/O
114	PS2CLK1/GPF2	DVD/CD_ON#	I
115	PS2DAT1/GPF3	TV_ON#	I
116	PS2CLK2/GPF4	TP_CLK	O
117	PS2DAT2/GPF5	TP_DAT	I/O
118	PS2CLK3/GPF6	SLOT_ON# ??	I
119	PS2DAT3/GPF7	INSTANT_ON#	I
113	FA16/GPG0	FA16_SWAP	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	FA19 BAT2_IN_OC#	O
3	FA20/GPG4	LID_EC#	I
4	FA21/GPG5	BAT2_IN_OC#	I
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD	I
55	GPH2	CPUPWR_GD	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_EC#	O
75	GPH5	SUSB_EC0#	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPIO	ICH8_PWROK	O
149	GPIO1	ALL_SYS_PWRGD	I
152	GPIO2	BAT1_CNT2#	O
155	GPIO3	CHG_EN#	O
156	GPIO4	PRECHG	O
168	GPIO5	EC_CLK_EN	O
174	GPIO6	BAT_LEARN	O

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor(MAX6657)	1001100x (98)
VGA Thermal IC(G781-1)	1001101x (9A)

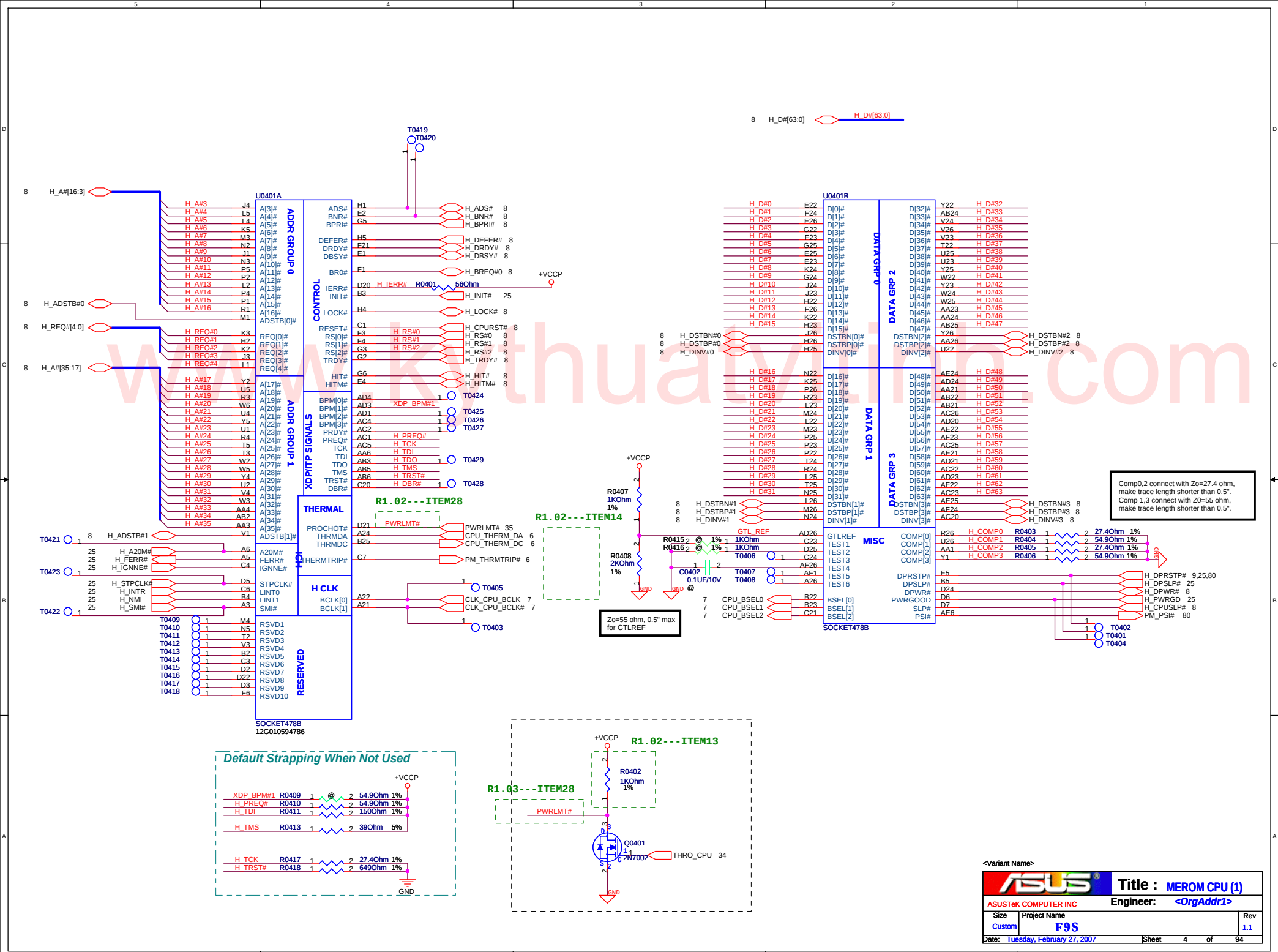
ICH8M_GPIO

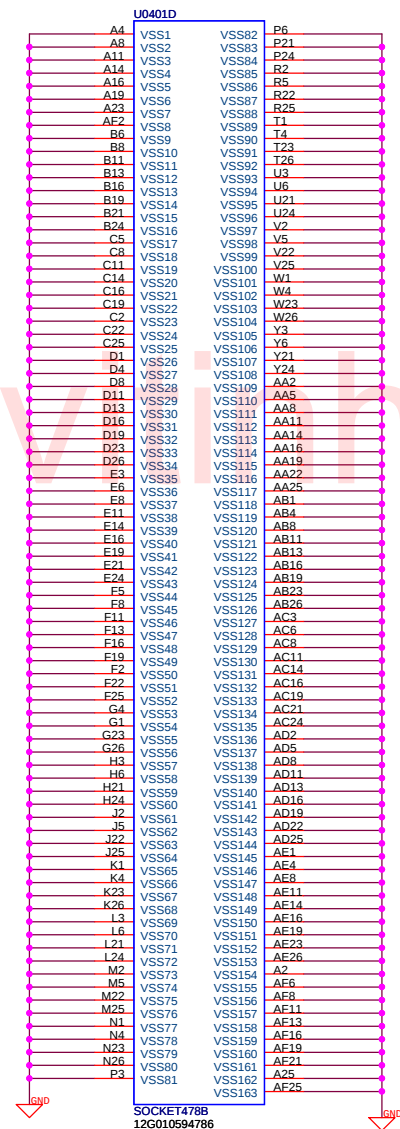
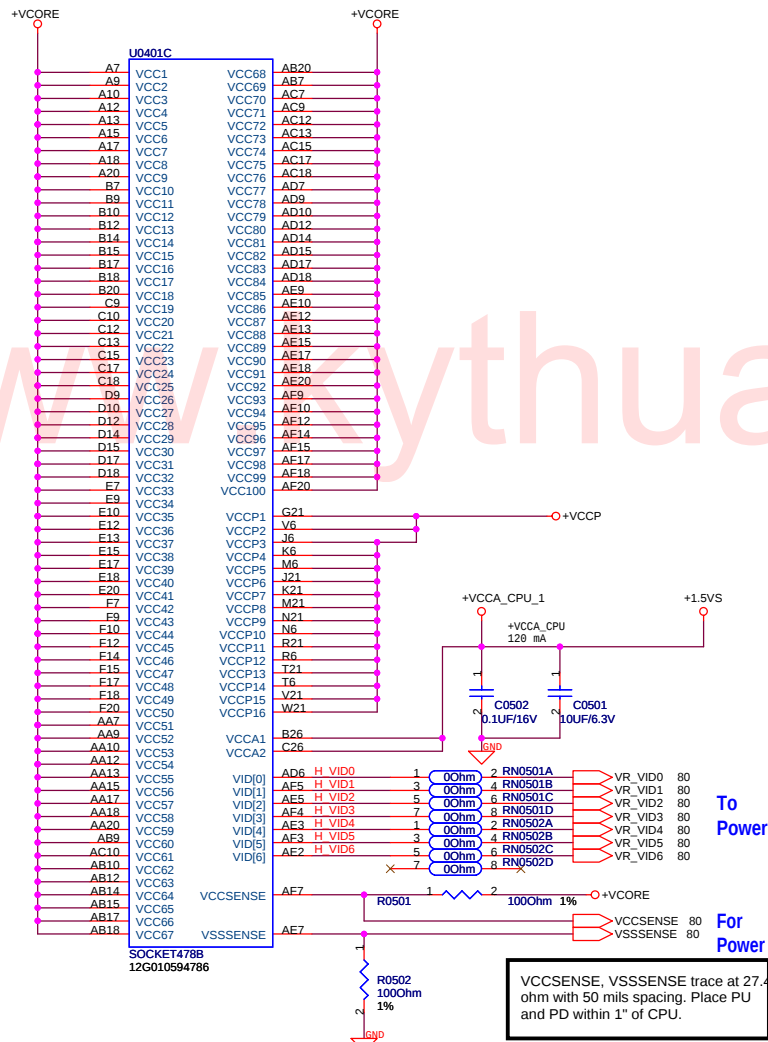
Pin.	Default	Use As	Signal Name	Power	Mux
GPIO 00	i	GPI	PM_BMBUSY#	+3VS	BM_BUSY#
GPIO 01	i	GPI	BT_DET#	+3VS	TACH1
GPIO [5:2]	i	GPI	PCI_INT[H:E]#	+3VS	PIRQ[H:E]#
GPIO 06	i	GPO	BIOS_REC_? (TP)	+3VS	TACH2
GPIO 07	i	GPO	802_LED_EN	+3VS	TACH3
GPIO 08	i	GPI	EXTSMI#	+3VSUS	N/A
GPIO 09	i	GPO	LAN_WOL_EN_? (TP)	+3VSUS	WOL_EN
GPIO 10	i	GPO	RST#_NEWCARD	+3VSUS	ALERT#
GPIO 11	Nat	Native	SMB_ALERT#	+3VSUS	SMBALERT#
GPIO 12	i	GPI	KBC_SCI#	+3VSUS	SLAN_DOCK#
GPIO 13	Nat	GPI	N/A	+3VSUS	ENERGY_DETECT
GPIO 14	i	GPI	N/A	+3VSUS	NETDETECT
GPIO 15	Nat	Native	STP_PCI#	+3VSUS	STP_PCI# , No-GPIO, in Mobile
GPIO 16	Nat	Native	PM DPRSLPVR	+3VS	DPRSLPVR
GPIO 17	i	GPO	WLAN_ON#	+3VS	TACH0
GPIO 18	O	GPO	N/A	+3VS	N/A
GPIO 19	i	GPO	CPU_SELECT	+3VS	SATA1GP
GPIO 20	O	GPO	BT_LED_EN	+3VS	N/A
GPIO 21	i	GPI	CPPE#_DET	+3VS	SATA0GP
GPIO 22	i	GPI	N/A	+3VS	SCLOCK
GPIO 23	Nat	Native	N/A	+3VS	LDRQ1#
GPIO 24	O	GPO	MSK_PCIRST	+3VSUS	CLGPIOQ(MEM_LED), Not Cleared by CF9h RST event.
GPIO 25	Nat	Native	STP_CPU#	+3VS	STP_CPU# , No-GPIO, in Mobile
GPIO 26	Nat	GPO	CPPE_EN	+3VSUS	S4_STATE#
GPIO 27	O	GPO	BT_ON#	+3VSUS	QRT_STATE0
GPIO 28	O	GPO	CB_SD#_? (TP)	+3VSUS	QRT_STATE1
GPIO 29	Nat	Native	USB_OC#5	+3VSUS	OC5#
GPIO 30	Nat	Native	USB_OC#6	+3VSUS	OC6#
GPIO 31	Nat	Native	USB_OC#7	+3VSUS	OC7#
GPIO 32	O	Native	PM_CLKRUN#	+3VS	CLKRUN# , No-GPIO, in Mobile
GPIO 33	O	GPO	N/A	+3VS	HDA_DOCK_EN#
GPIO 34	O	GPO	N/A	+3VS	HDA_DOCK_RST#
GPIO 35	O	GPO	SATACLKREQ#_? (TP)	+3VS	SATACLKREQ#
GPIO 36	i	GPO	EMAIL_LED#_? (TP)	+3VS	SATA2GP
GPIO 37	i	GPI	PCB_ID0	+3VS	SATA3GP
GPIO 38	i	GPI	PCB_ID1	+3VS	SLOAD

Pin	Default	Use As	Signal Name	Power	Mux
GPIO 39	i	GPI	PCB_ID2	+3VS	SDATAOUT0
GPIO [40:43]	Nat	Native	USB_OC[4:1]#	+3VSUS	OC[4:1]#
GPIO [47:44]	n/a	N/A	N/A	N/A	No implement
GPIO 48	i	Native		+3VS	SDATAOUT1
GPIO 49	Nat	Native	H_PWRGD	+VCORE	CPUPWRGD
GPIO 50	Nat	Native	PCI_REQ1#	+5VS	REQ1#
GPIO 51	Nat	Native	PCI_GNT1#	+3VS	GNT1#
GPIO 52	Nat	Native	PCI_REQ2#	+5VS	REQ2#
GPIO 53	Nat	Native	PCI_GNT2#	+3VS	GNT2#
GPIO 54	Nat	Native	PCI_REQ3#	+5VS	REQ3#
GPIO 55	Nat	Native	PCI_GNT3#	+3VS	GNT3#

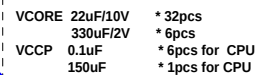
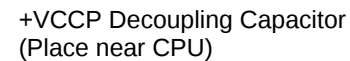
<Variant Name>

ASUS		Title : Schematic Info.	
ASUSTeK COMPUTER INC.		Engineer: <OrgAddr1>	
Size	Project Name		Rev
Custom	F9S		1.1
Date: Monday, February 05, 2007		Sheet	3 of 94

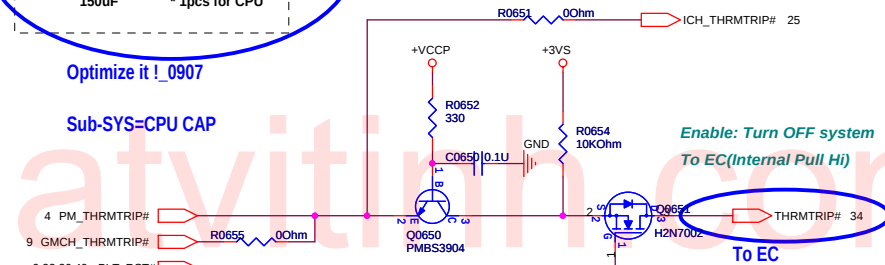




+VCCP		+VCCP	4,5,7,8,9,11,12,28,37,85
+VCORE		+VCORE	5,37,80
+3VS		+3VS	7,9,12,13,14,15,17,18,19,20,21,22,23,25,27,28,29,33,34,37,39,40,43,44,45,80,91,92
+5VA		+5VA	81



Sub-SYS=CPU CAP

[illegible]

PWM FAN Control

3V5

R0659 4.7kOhm

R0661 1.2kOhm

34 FAN0_TACH

1 2

34 FAN_PWM

1 2

R0671 150ohm

FAN_PWM_CON

FANSP

C0653 100PF/50V

C0654 100PF/50V

CE0602 47uF/6.3V

D0601 1N4148W

CON601

4 SIDE2 6

3

2

1 SIDE1 5

WtoB_CON_4P_1

P/N:12G1700004B

H/W Thermal Protect

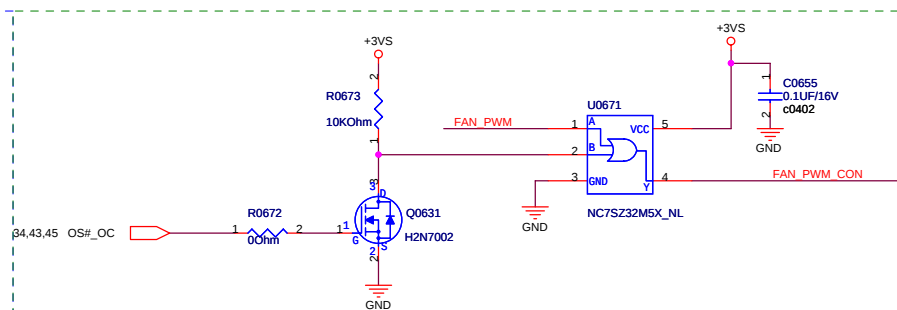
(94~98°C protect)

Components and connections:

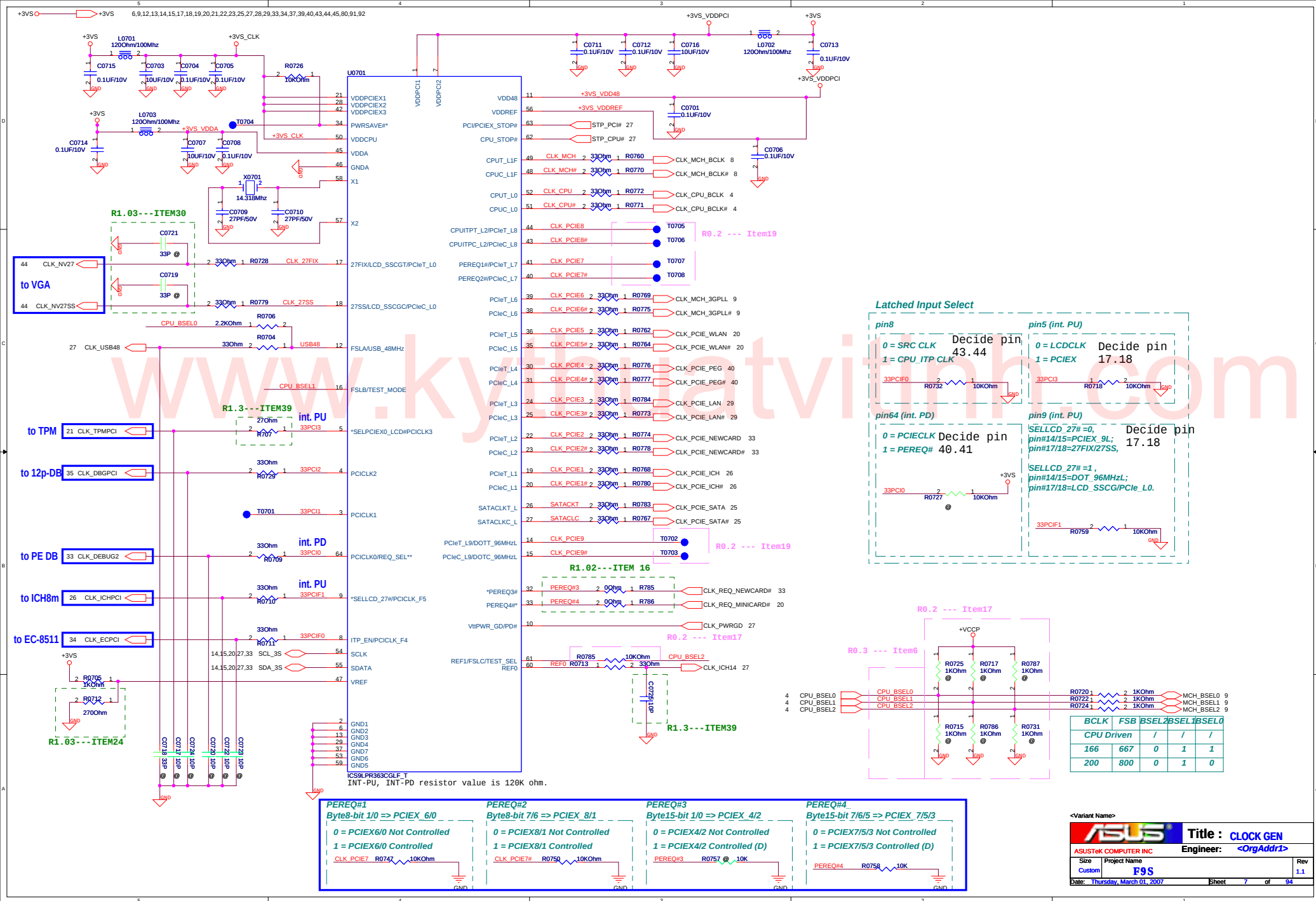
- +5V supply
- R0670: 22.1K 1%
- RT0671: 100K
- C0670: 0.1uF
- R0662: 4.7KOhm
- PST9013NR (PNP Transistor)
- VCC connected to +5V
- GND connected to ground
- VOUT connected to collector of R0662
- FORCE_OFF# output (34.81.92)

Enable: Turn OFF system

OPEN Collector



		Title : CPU CAP, Thermal,FAN_CTRL	
ASUSTeK COMPUTER INC		Engineer:	
Size Custom	Project Name F9S		Rev 1.1
Date: Tuesday, February 27, 2007		Sheet 6 of 94	



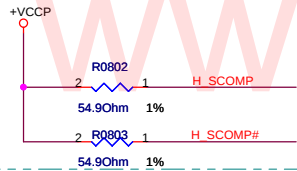
RCOMP

For Calibrating the FSB I/O Buffer



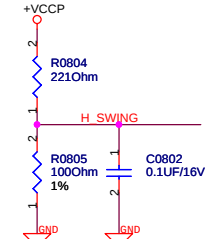
SCOMP

For Slew Rate Compensation on the FSB



Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits



4 H_D#[63:0] H_D#[63:0]

4 H_A#[35:3] H_A#[35:3]

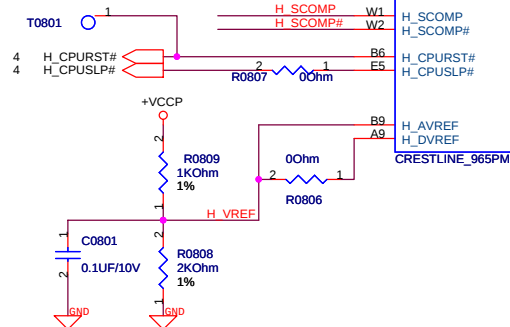
U0801A

H_D#0	E2	H_D#_0
H_D#1	G2	H_D#_1
H_D#2	G7	H_D#_2
H_D#3	M6	H_D#_3
H_D#4	H7	H_D#_4
H_D#5	M3	H_D#_5
H_D#6	G4	H_D#_6
H_D#7	F3	H_D#_7
H_D#8	N8	H_D#_8
H_D#9	H2	H_D#_9
H_D#10	M10	H_D#_10
H_D#11	N12	H_D#_11
H_D#12	N9	H_D#_12
H_D#13	H5	H_D#_13
H_D#14	P13	H_D#_14
H_D#15	K9	H_D#_15
H_D#16	M2	H_D#_16
H_D#17	W10	H_D#_17
H_D#18	Y8	H_D#_18
H_D#19	V4	H_D#_19
H_D#20	M3	H_D#_20
H_D#21	J1	H_D#_21
H_D#22	N5	H_D#_22
H_D#23	N3	H_D#_23
H_D#24	W6	H_D#_24
H_D#25	W9	H_D#_25
H_D#26	A2	H_D#_26
H_D#27	Y7	H_D#_27
H_D#28	Y9	H_D#_28
H_D#29	P4	H_D#_29
H_D#30	W3	H_D#_30
H_D#31	N1	H_D#_31
H_D#32	AD12	H_D#_32
H_D#33	AE3	H_D#_33
H_D#34	AD9	H_D#_34
H_D#35	AC9	H_D#_35
H_D#36	AC7	H_D#_36
H_D#37	AC14	H_D#_37
H_D#38	AD11	H_D#_38
H_D#39	AC11	H_D#_39
H_D#40	AB2	H_D#_40
H_D#41	AD7	H_D#_41
H_D#42	AB1	H_D#_42
H_D#43	Y3	H_D#_43
H_D#44	AC6	H_D#_44
H_D#45	AE2	H_D#_45
H_D#46	AC5	H_D#_46
H_D#47	AC3	H_D#_47
H_D#48	AJ9	H_D#_48
H_D#49	AH8	H_D#_49
H_D#50	AJ14	H_D#_50
H_D#51	AE9	H_D#_51
H_D#52	AE11	H_D#_52
H_D#53	AH12	H_D#_53
H_D#54	AJ5	H_D#_54
H_D#55	AH5	H_D#_55
H_D#56	AJ6	H_D#_56
H_D#57	AE7	H_D#_57
H_D#58	AJ7	H_D#_58
H_D#59	AJ2	H_D#_59
H_D#60	AE5	H_D#_60
H_D#61	AJ3	H_D#_61
H_D#62	AH2	H_D#_62
H_D#63	AH13	H_D#_63

HOST

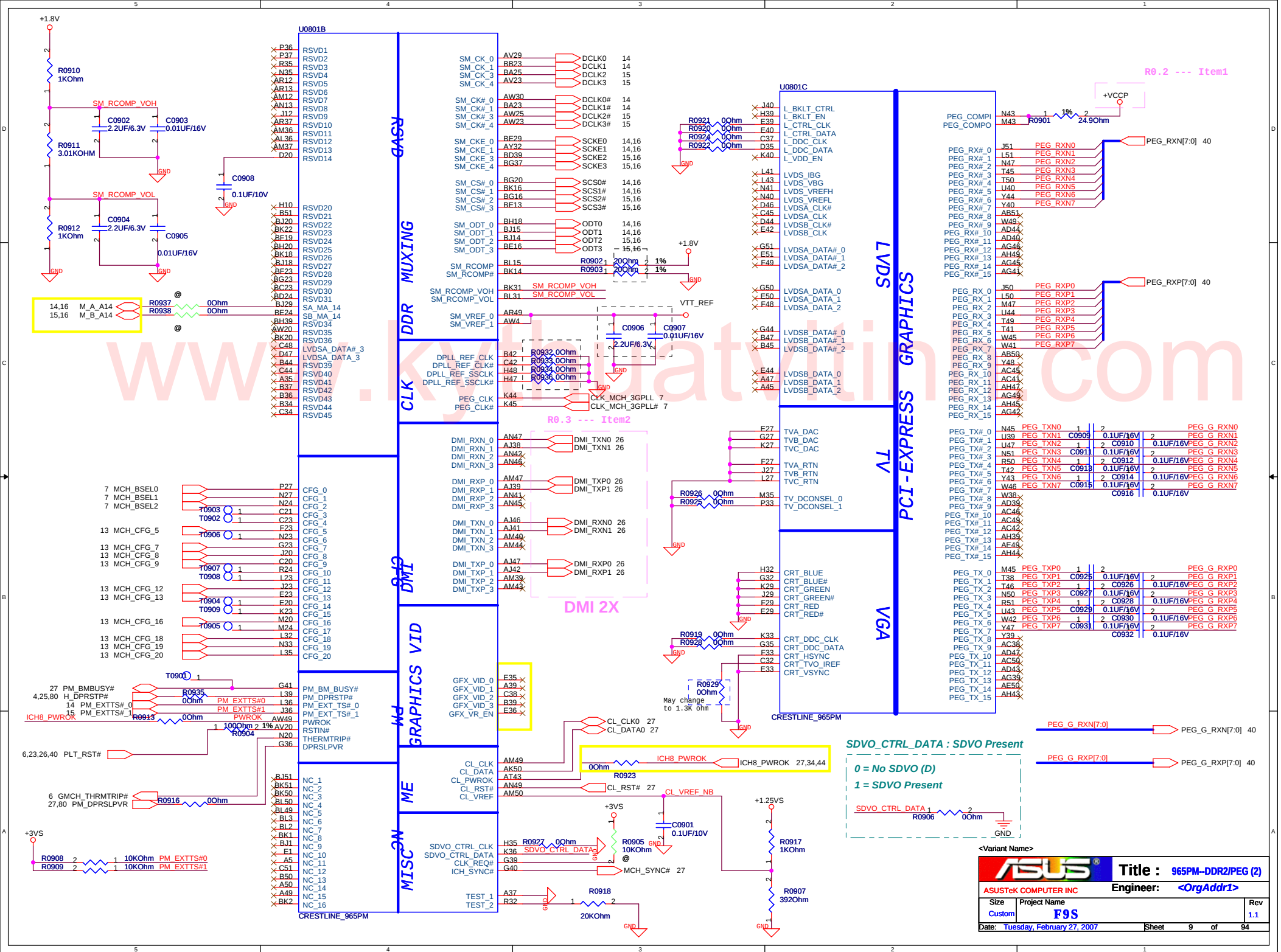
H_A#_3	J13	H_A#3
H_A#_4	B11	H_A#4
H_A#_5	C11	H_A#5
H_A#_6	M11	H_A#6
H_A#_7	C15	H_A#7
H_A#_8	F16	H_A#8
H_A#_9	L13	H_A#9
H_A#_10	G17	H_A#10
H_A#_11	C14	H_A#11
H_A#_12	K16	H_A#12
H_A#_13	B13	H_A#13
H_A#_14	L16	H_A#14
H_A#_15	J17	H_A#15
H_A#_16	B14	H_A#16
H_A#_17	K19	H_A#17
H_A#_18	P15	H_A#18
H_A#_19	R17	H_A#19
H_A#_20	B16	H_A#20
H_A#_21	H20	H_A#21
H_A#_22	L19	H_A#22
H_A#_23	D17	H_A#23
H_A#_24	M17	H_A#24
H_A#_25	N16	H_A#25
H_A#_26	J19	H_A#26
H_A#_27	B18	H_A#27
H_A#_28	E19	H_A#28
H_A#_29	B17	H_A#29
H_A#_30	B15	H_A#30
H_A#_31	E17	H_A#31
H_A#_32	C18	H_A#32
H_A#_33	A19	H_A#33
H_A#_34	B19	H_A#34
H_A#_35	N19	H_A#35
H_ADS#	G12	H_ADS#
H_ADSTB#_0	H17	H_ADSTB#0
H_ADSTB#_1	G20	H_ADSTB#1
H_BNR#	C8	H_BNR#
H_BPRI#	E8	H_BPRI#
H_BREQ#_0	F12	H_BREQ#0
H_DEFER#	D6	H_DEFER#
H_DBSY#	C10	H_DBSY#
H_DBSY#_4	AM5	H_DBSY#_4
HPLL_CLK#	AM7	HPLL_CLK#
H_DPWR#	H8	H_DPWR#
H_DRDY#	K7	H_DRDY#
H_HIT#	E4	H_HIT#
H_HITM#	C6	H_HITM#
H_LOCK#	G10	H_LOCK#
H_TRDY#	B7	H_TRDY#
H_DIN#_0	K5	H_DIN#0
H_DIN#_1	L2	H_DIN#1
H_DIN#_2	AD13	H_DIN#2
H_DIN#_3	AE13	H_DIN#3
H_DSTBN#_0	M7	H_DSTBN#0
H_DSTBN#_1	K3	H_DSTBN#1
H_DSTBN#_2	AD2	H_DSTBN#2
H_DSTBN#_3	AH11	H_DSTBN#3
H_DSTBP#_0	L7	H_DSTBP#0
H_DSTBP#_1	K2	H_DSTBP#1
H_DSTBP#_2	AC2	H_DSTBP#2
H_DSTBP#_3	AJ10	H_DSTBP#3
H_REQ#_0	M14	H_REQ#0
H_REQ#_1	E13	H_REQ#1
H_REQ#_2	A11	H_REQ#2
H_REQ#_3	H13	H_REQ#3
H_REQ#_4	B12	H_REQ#4
H_RS#_0	E12	H_RS#0
H_RS#_1	D7	H_RS#1
H_RS#_2	D8	H_RS#2

4 H_REQ#[4:0] H_REQ#[4:0]



<Variant Name>

ASUS		Title : 965PM -- CPU (1)	
ASUSTeK COMPUTER INC		Engineer: <OrgAddr1>	
Size	Project Name	Rev	
Custom	F9S	1.1	
Date: Tuesday, February 27, 2007		Sheet 8 of 94	

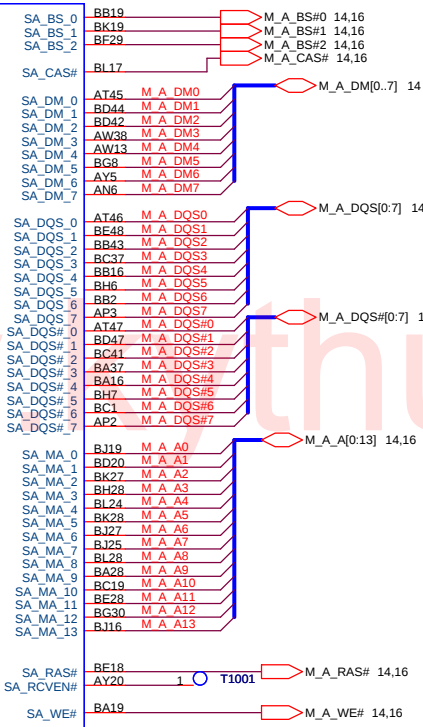


14 M_A_DQ[0:63]

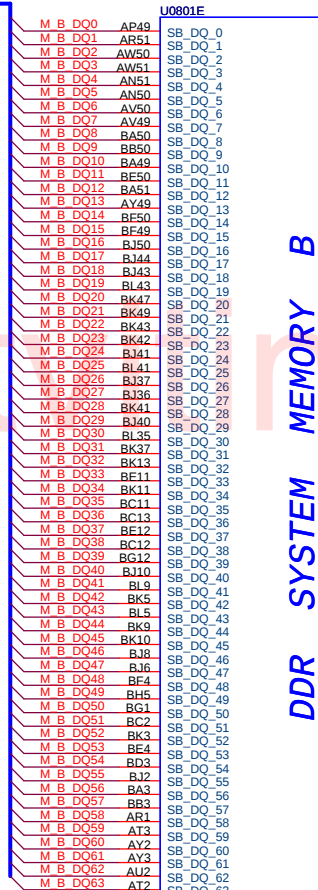


CRESTLINE_965PM

DDR SYSTEM MEMORY A

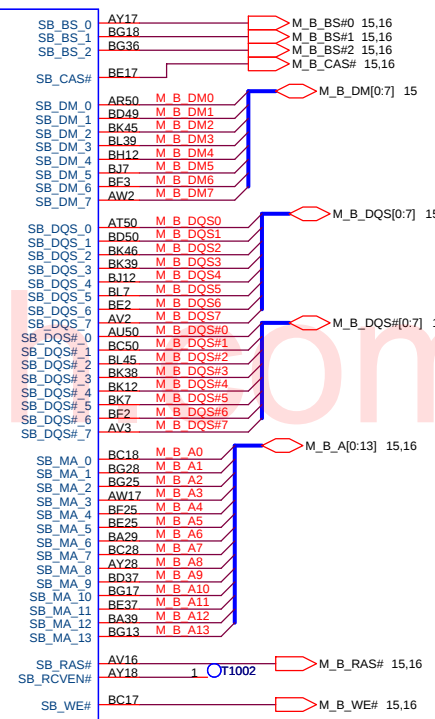


15 M_B_DQ[0:63]



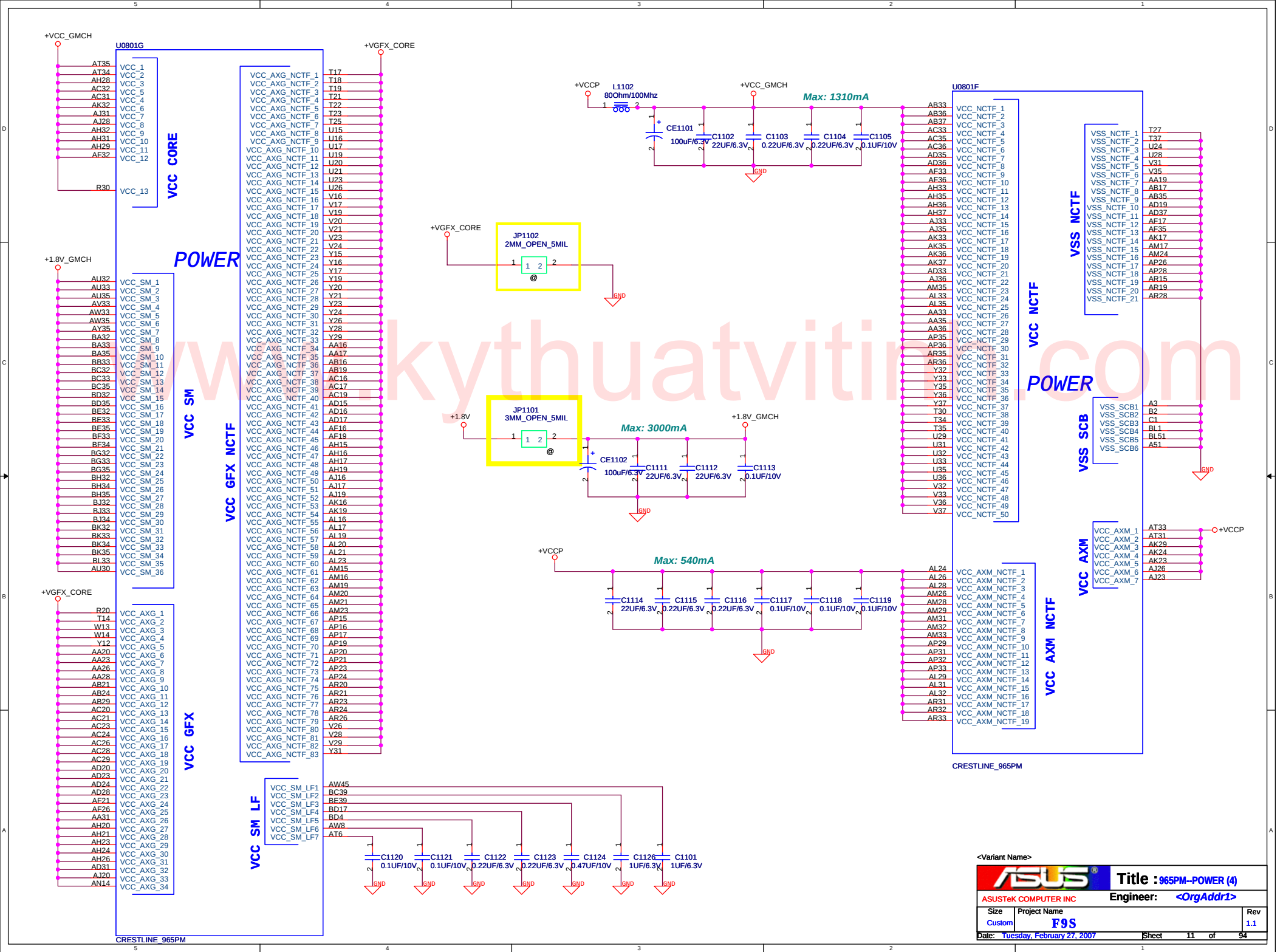
CRESTLINE_965PM

DDR SYSTEM MEMORY B



<Variant Name>

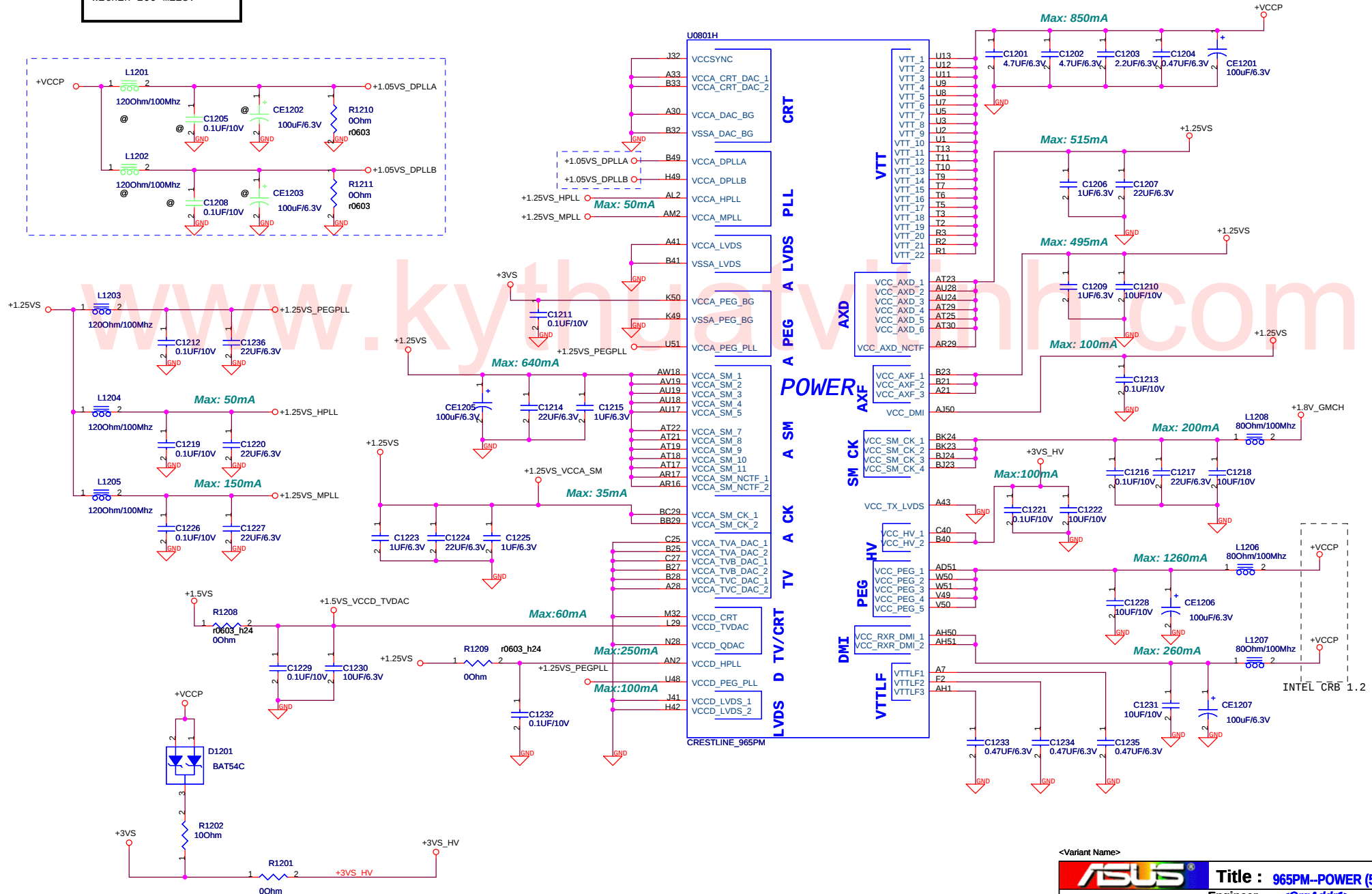
		Title : 965PM-DDR2 bus (3)	
ASUSTeK COMPUTER INC		Engineer: <OrgAddr1>	
Size Custom	Project Name F9S		Rev 1.1
Date: Tuesday, February 27, 2007		Sheet 10 of 94	



<Variant Name>

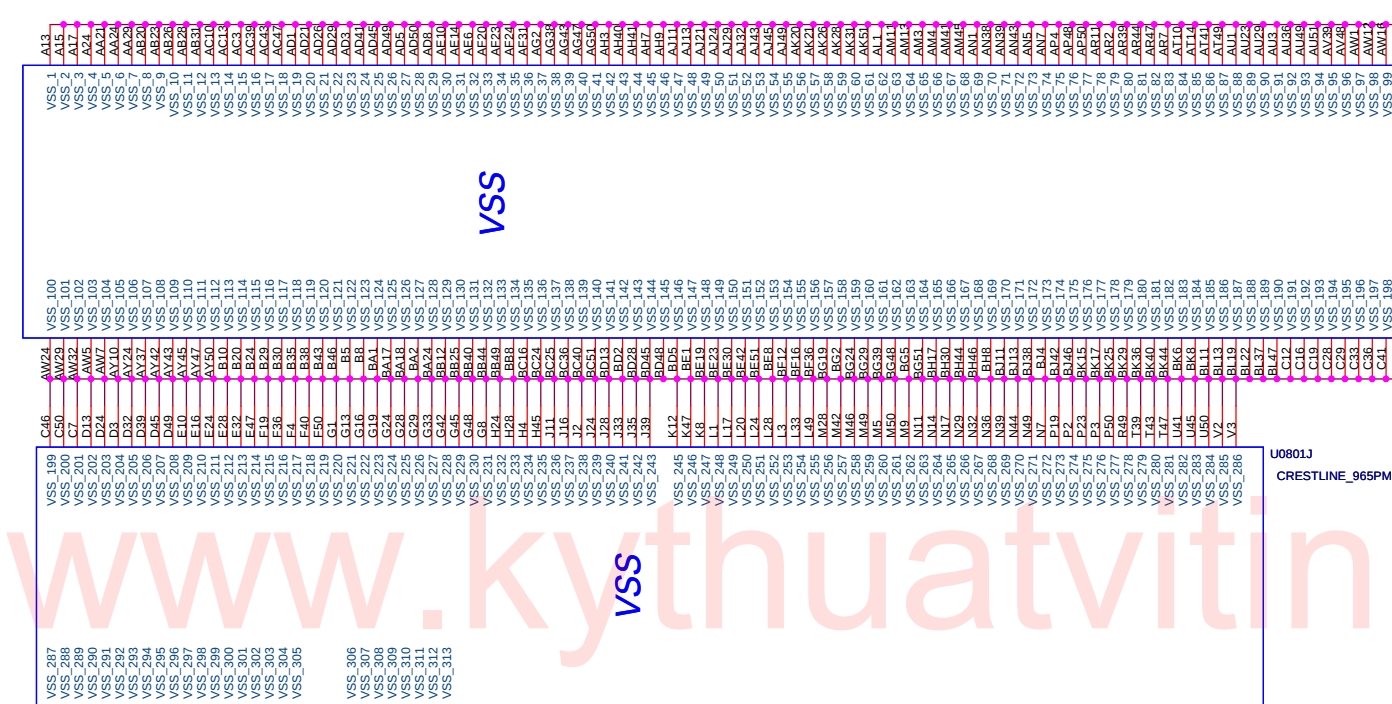
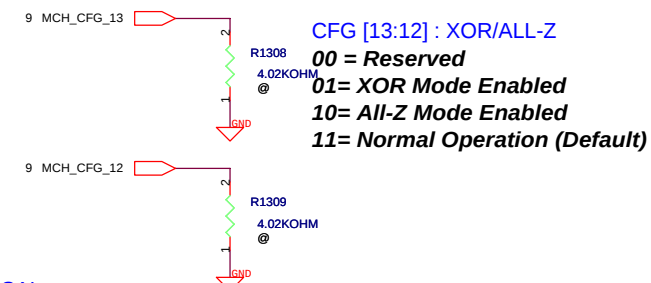
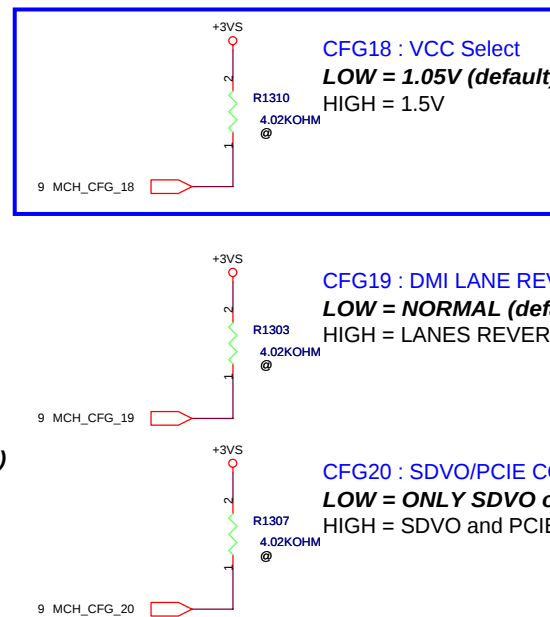
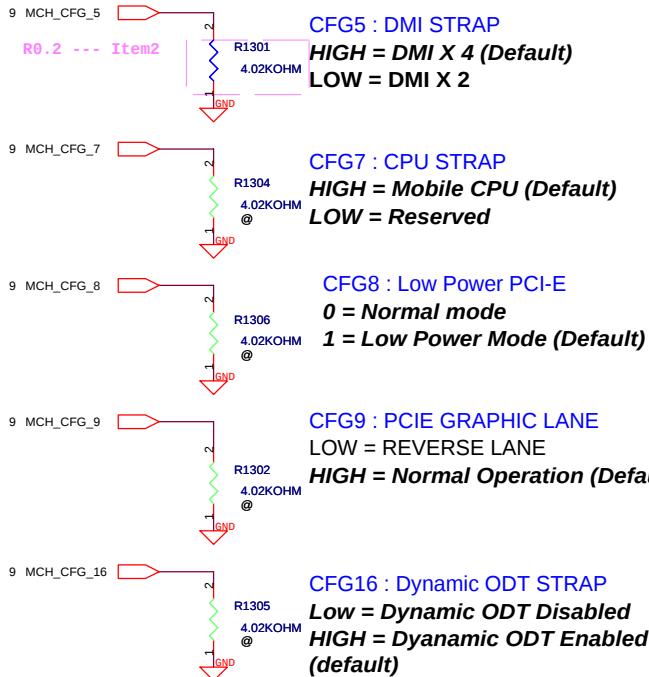
ASUS		Title : 965PM-POWER (4)	
ASUSTeK COMPUTER INC		Engineer: <OrgAddr>	
Size	Project Name	Rev	
Custom	F9S	1.1	
Date: Tuesday, February 27, 2007		Sheet	11 of 94

NOTE: 0.1uF caps in 1.5VS_XPLL need to be located as edge caps within 200 mils.

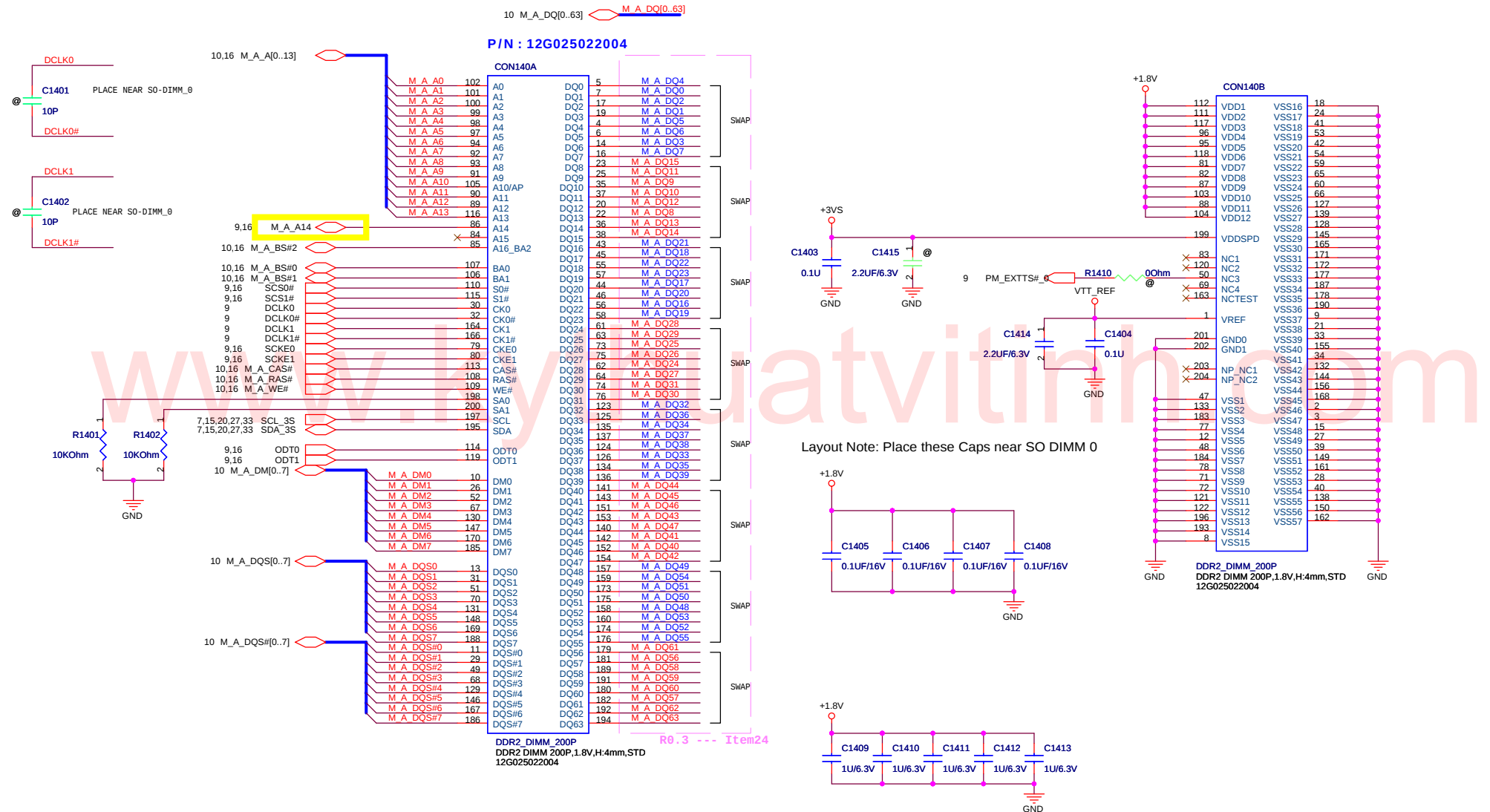


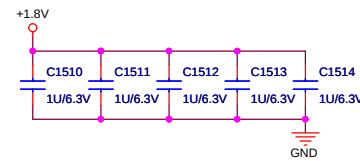
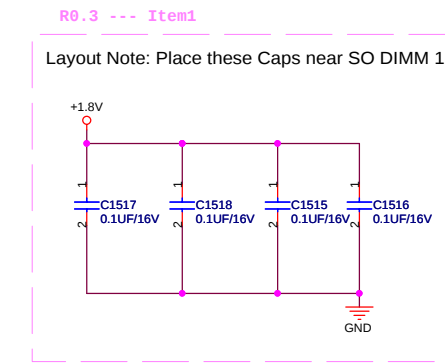
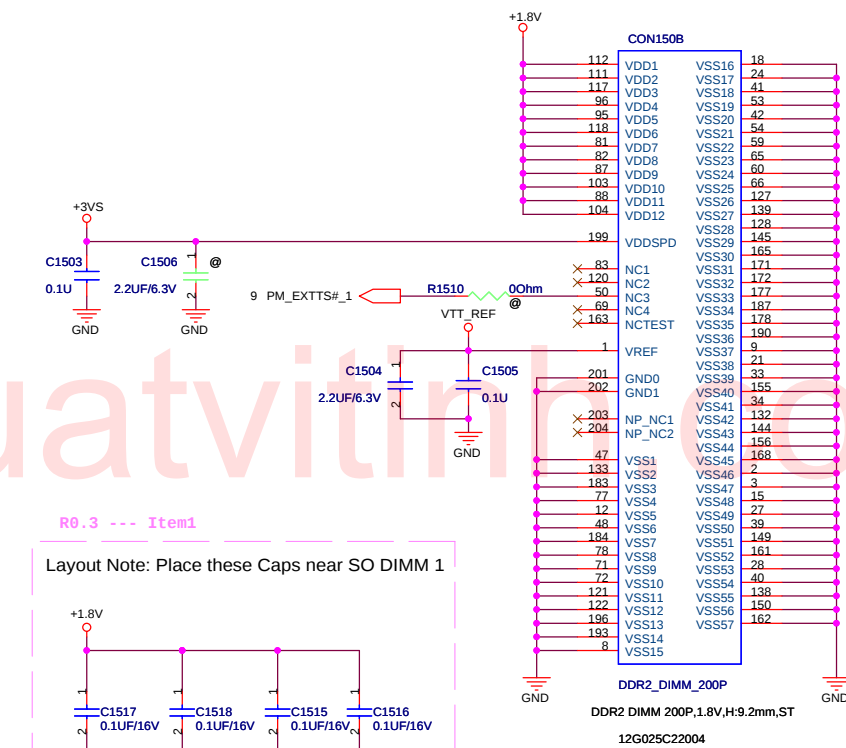
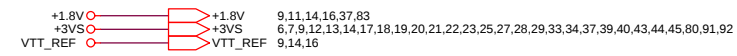
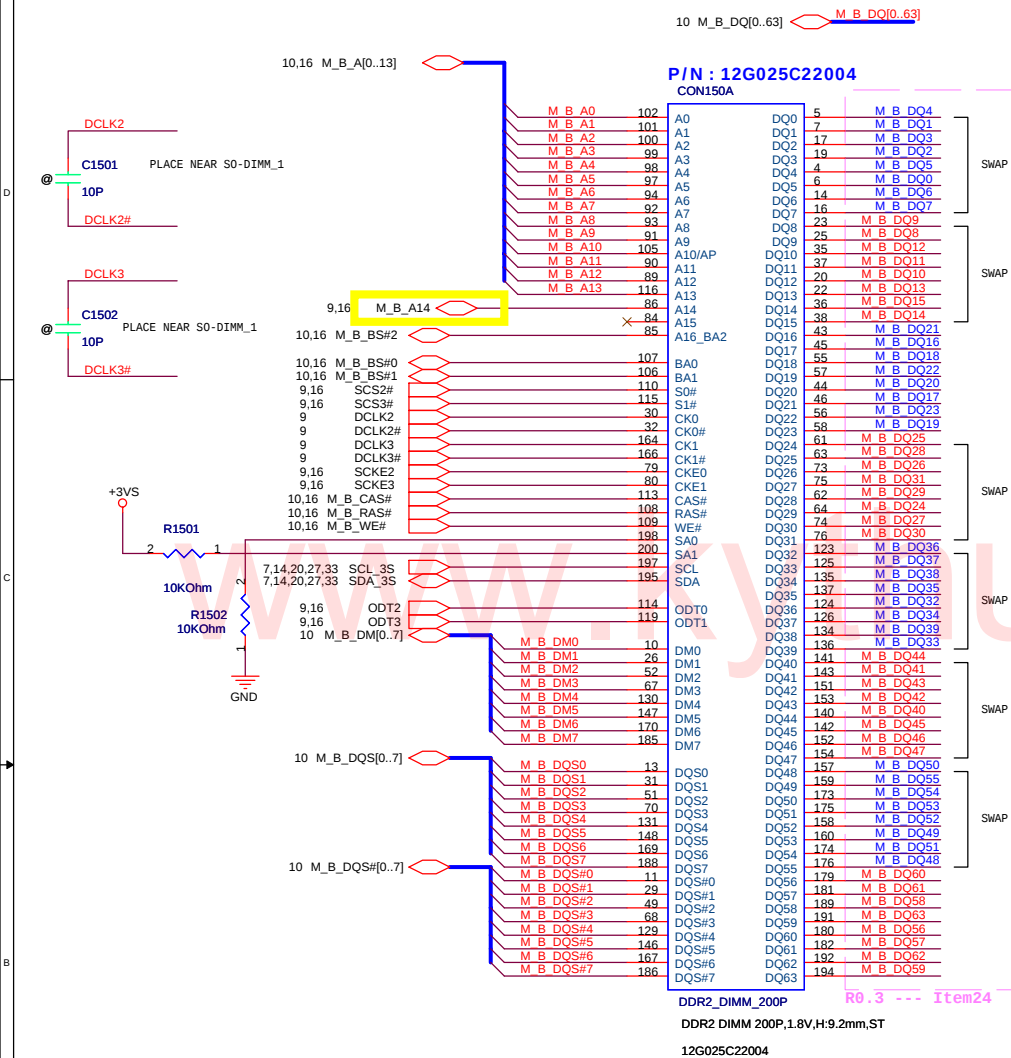
<Variant Name>

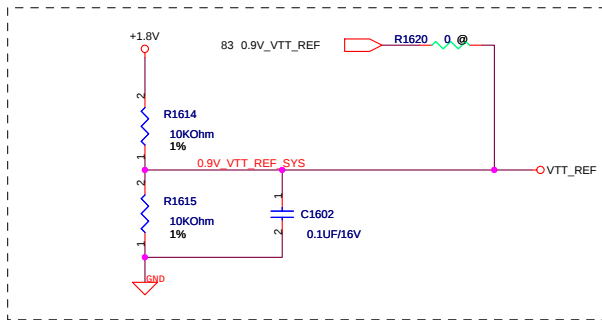
ASUS		Title : 965PM-Power (5)	
ASUSTeK COMPUTER INC		Engineer: <OrgAddr1>	
Size	Project Name	Rev	
Custom	F9S	1.1	
Date: Monday, February 05, 2007		Sheet	12 of 94



Standard Type

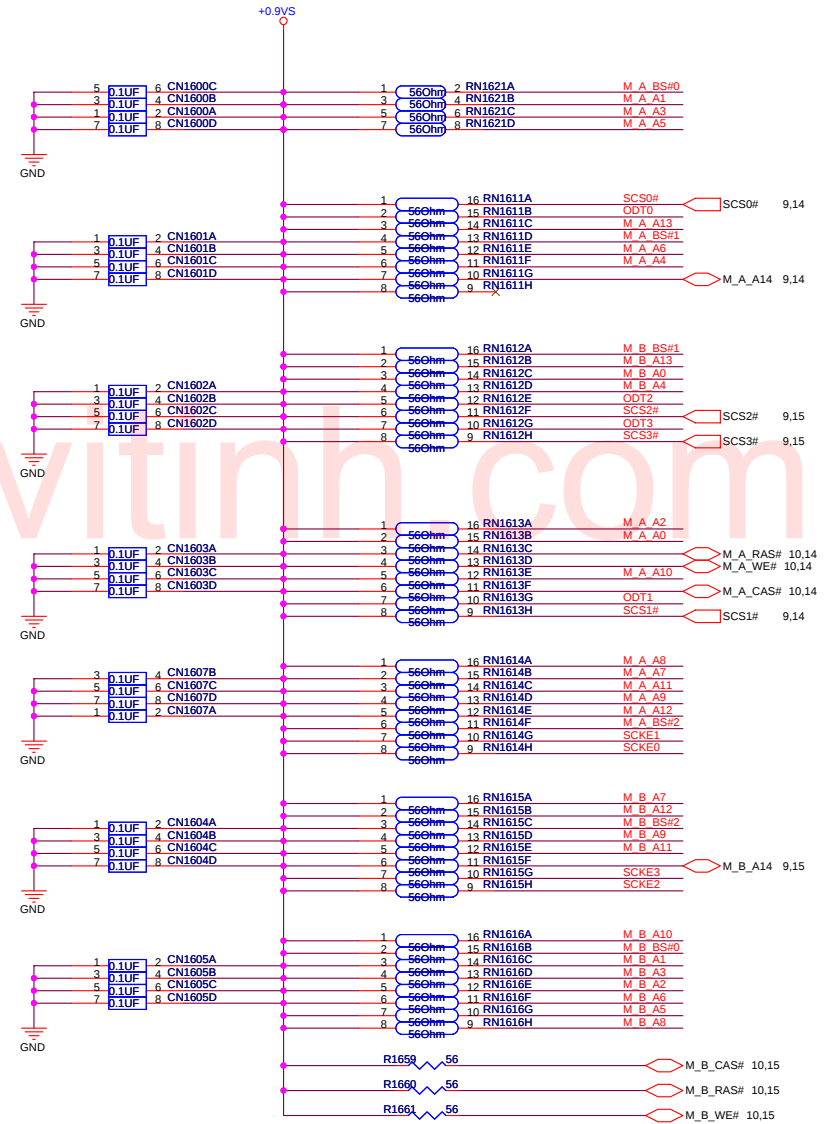






M_A_A[0..13] 10,14
 M_A_BS#[0..2] 10,14
 M_B_A[0..13] 10,15
 M_B_BS#[0..2] 10,15
 SCKE[0..3] 9,14,15
 ODT[0..3] 9,14,15

SWAPPED

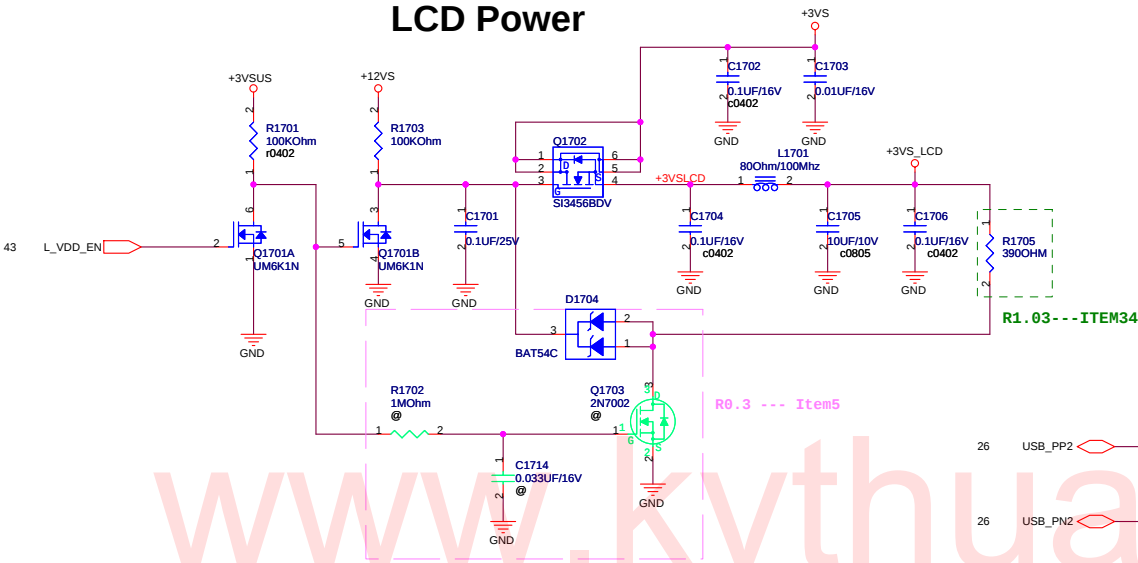


Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

<Variant Name>

ASUS		Title : DDR2 ADDR TERM	
ASUSTeK COMPUTER INC		Engineer: <OrgAddr1>	
Size	Project Name		Rev
Custom	F9S		1.1
Date: Tuesday, February 27, 2007		Sheet	16 of 94

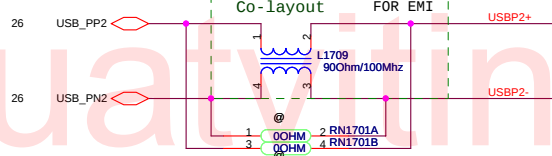
LCD Power



R1.2---ITEM36

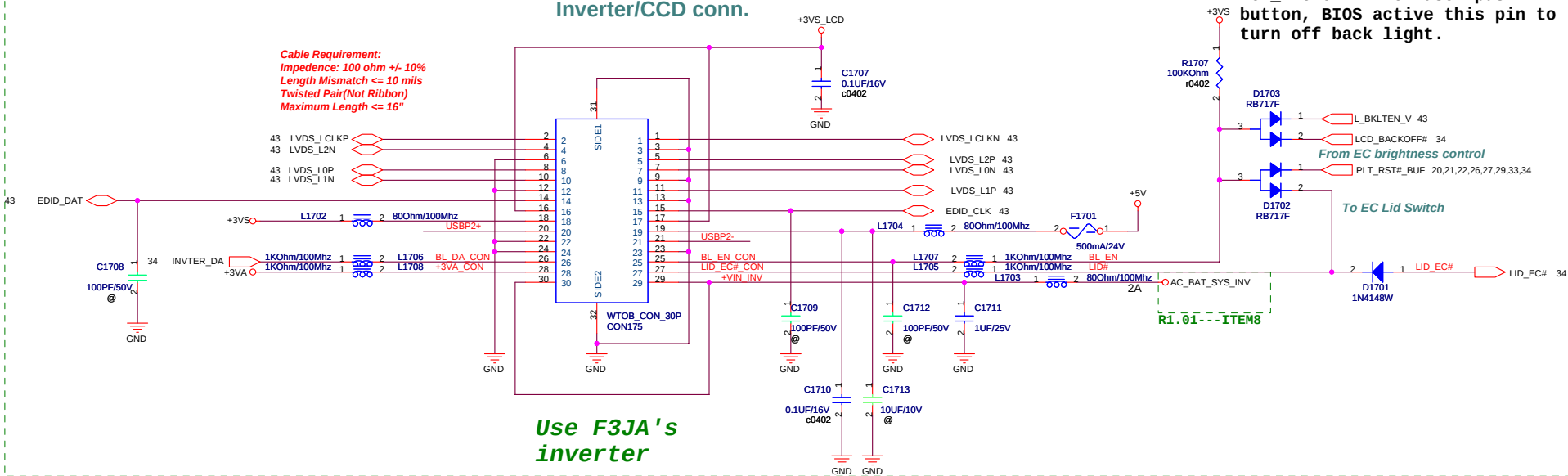
R1.03---ITEM31

Co-layout FOR EMI



Inverter/CCD conn.

Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"



Use F3JA's inverter

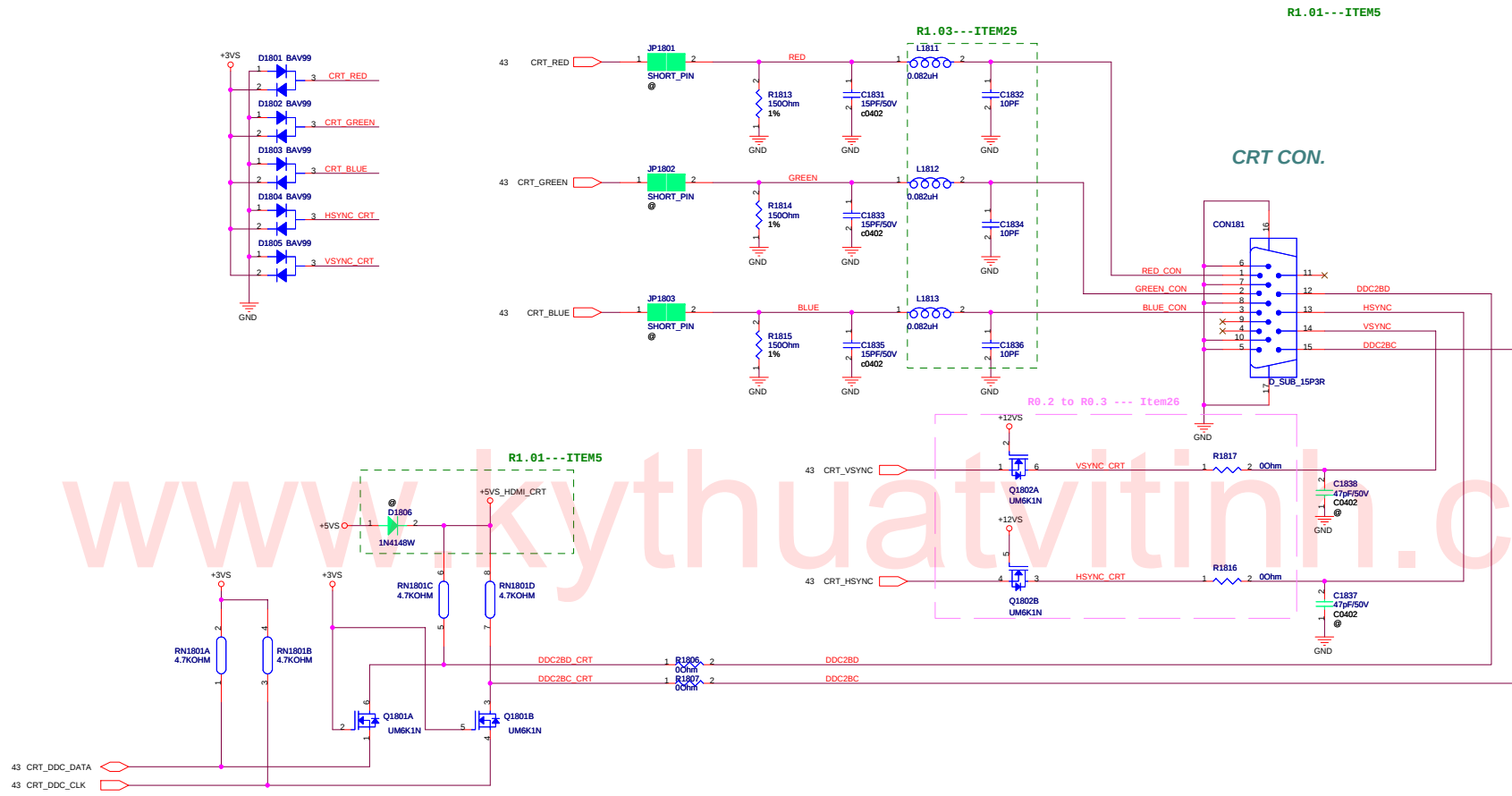
BIOS
LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

From EC brightness control
PLT_RST#_BUF 20,21,22,26,27,29,33,34

To EC Lid Switch

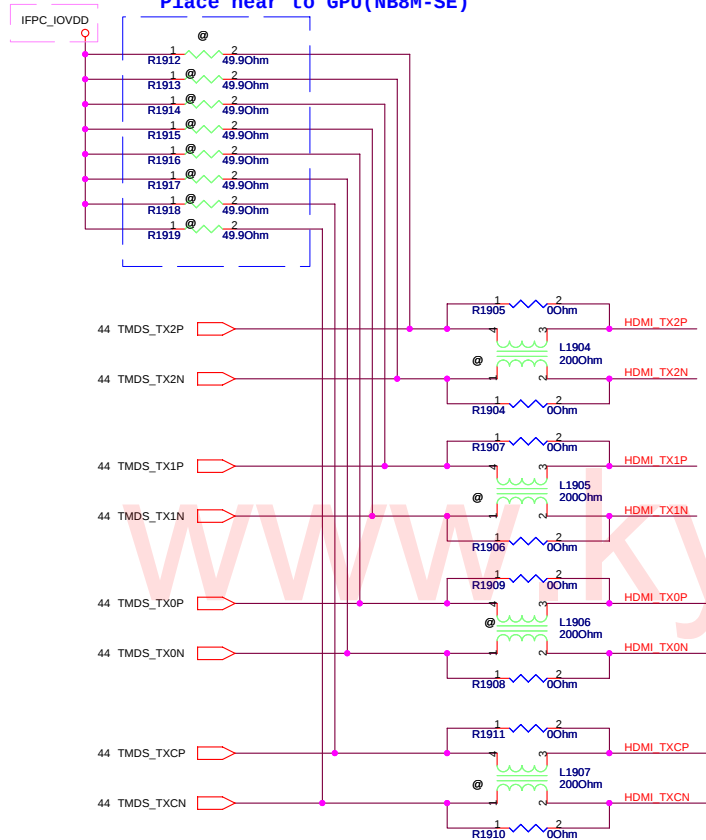
R1.01---ITEM8

ASUS		Title : LVDS & INVERTER	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F9S	1.1	
Date: Tuesday, February 27, 2007		Sheet 17 of 94	

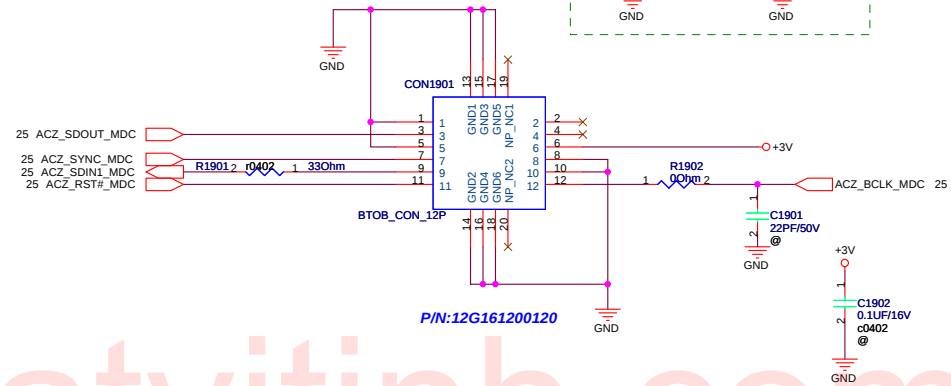
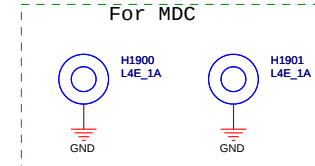


R0.2 --- Item5

Place near to GPU(NB8M-SE)

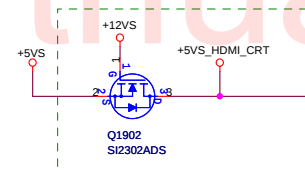


MDC CON.

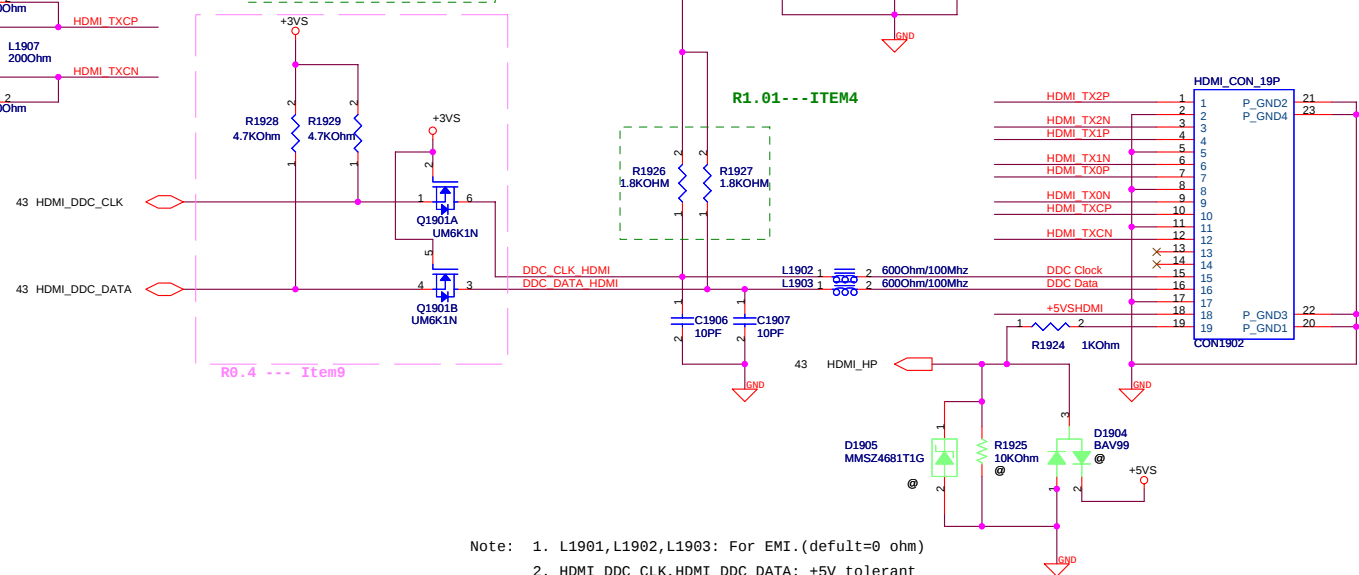


P/N:12G161200120

R1.01---ITEM4



HDMI CON.



R0.4 --- Item9

- Note: 1. L1901,L1902,L1903: For EMI.(default=0 ohm)
2. HDMI_DDC_CLK,HDMI_DDC_DATA: +5V tolerant

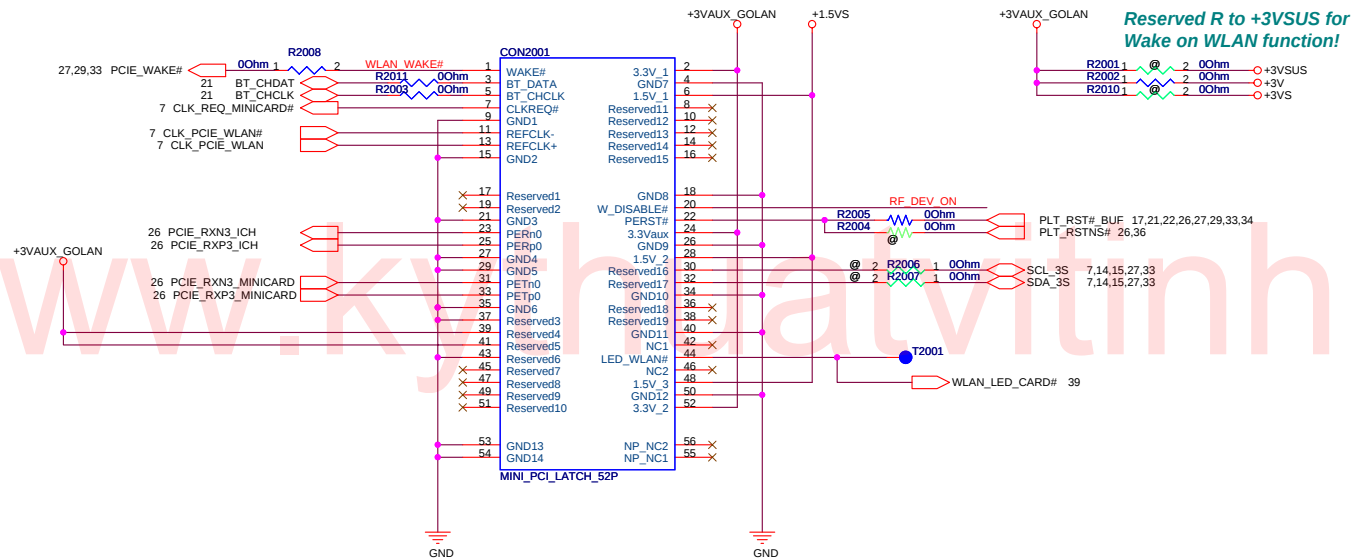
ASUSTek COMPUTER INC.
<DmAddr1> Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

MDC,HDMI CON		
Size	Document Number	Rev
Custom	F9S	1.1
Date:	Tuesday, February 27, 2007	Sheet 19 of 94

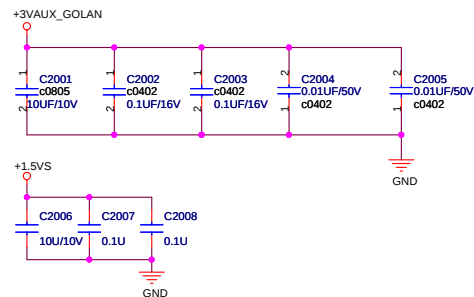
+3VAUX_GOLAN: +3.003V~+3.597V
Max= 1100 mA

+1.5VS: +1.425V~+1.575V
Max= 375 mA

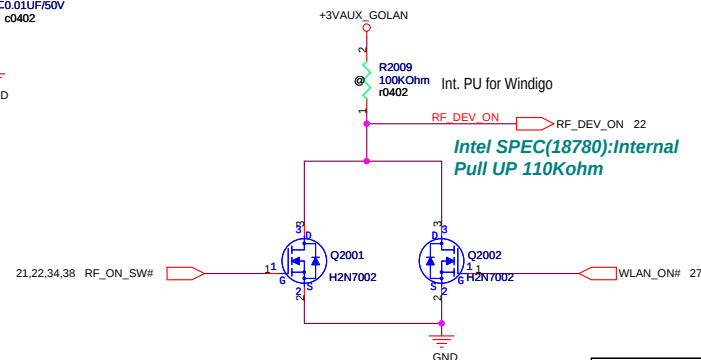
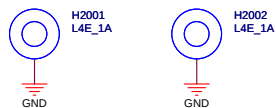
P/N : 12G030100525_2006/1024
WLAN



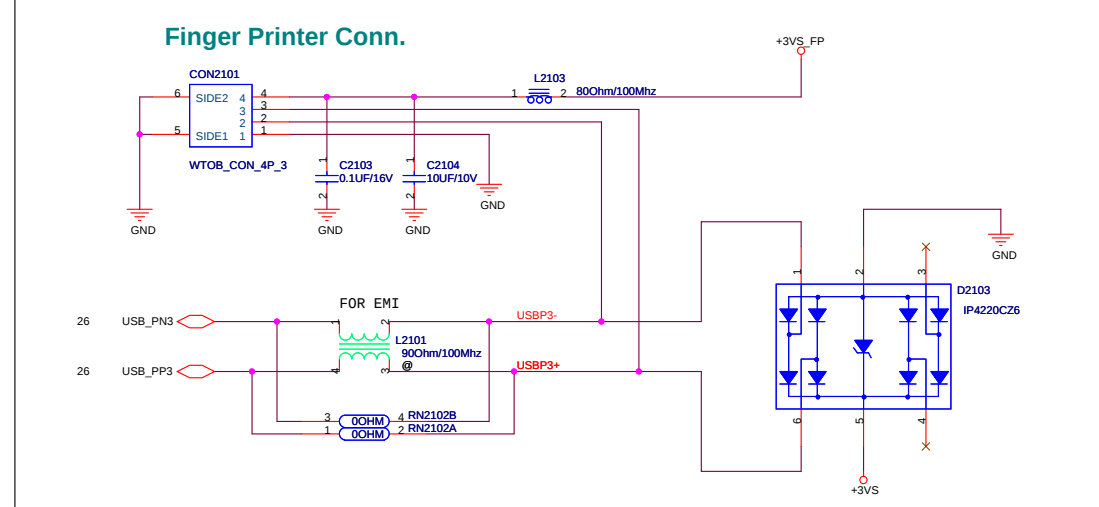
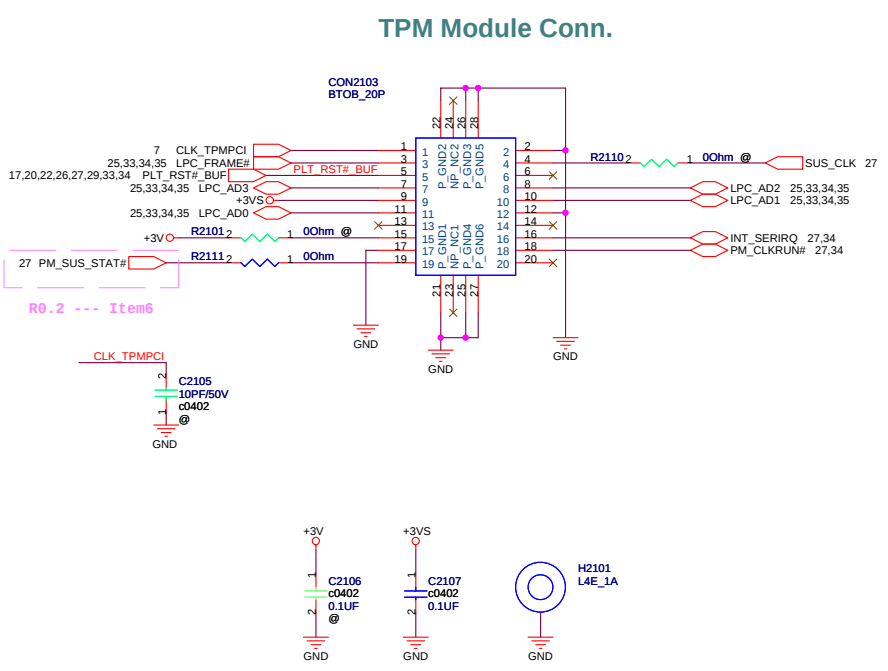
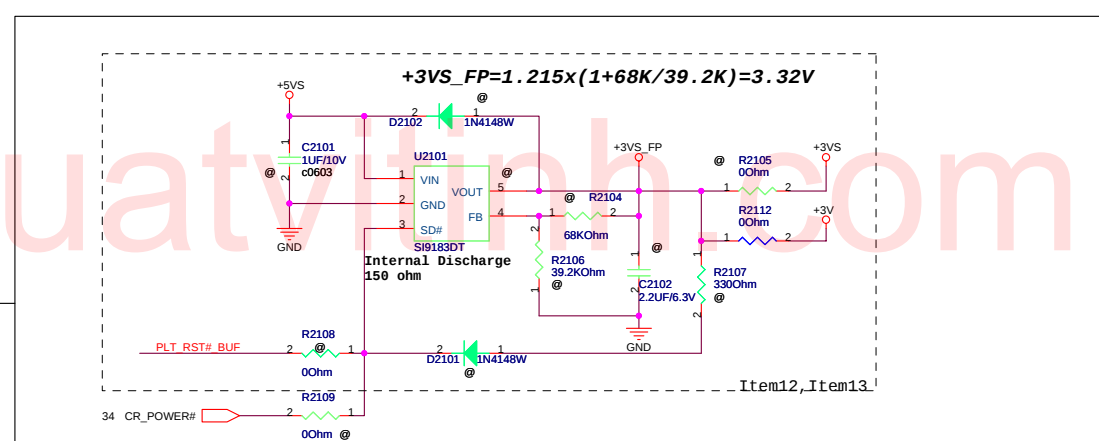
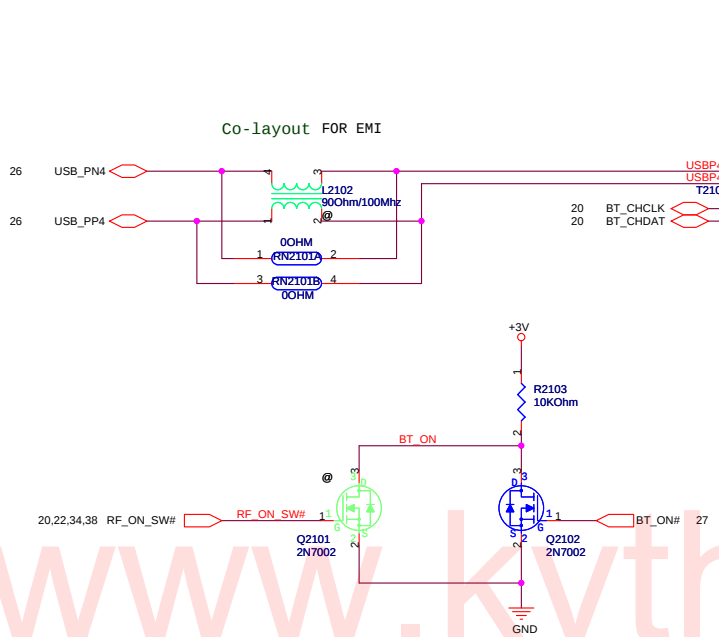
Reserved R to +3VSUS for Wake on WLAN function!

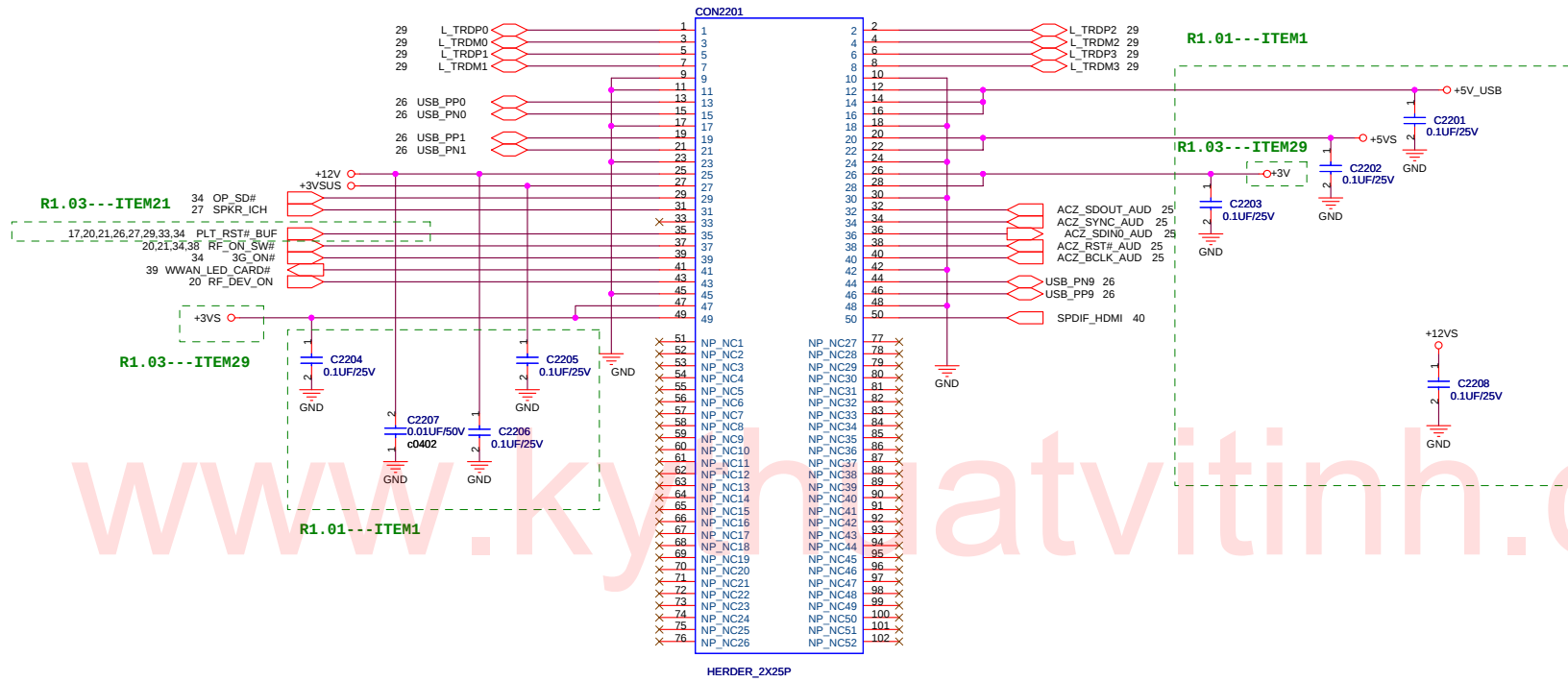


+1.5VS: 5,12,25,28,33,37,82
+3V: 19,21,22,26,33,35,37,91
+3VS: 6,7,9,12,13,14,15,17,18,19,21,22,23,25,27,28,29,33,34,37,39,40,43,44,45,80,91,92

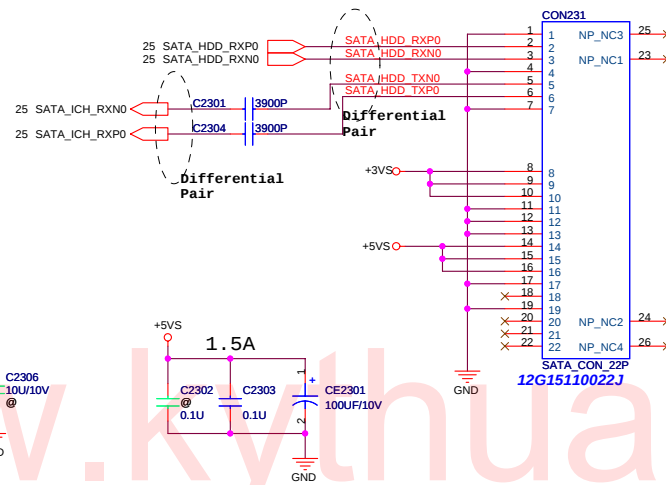


Intel SPEC(18780): Internal Pull UP 110Kohm

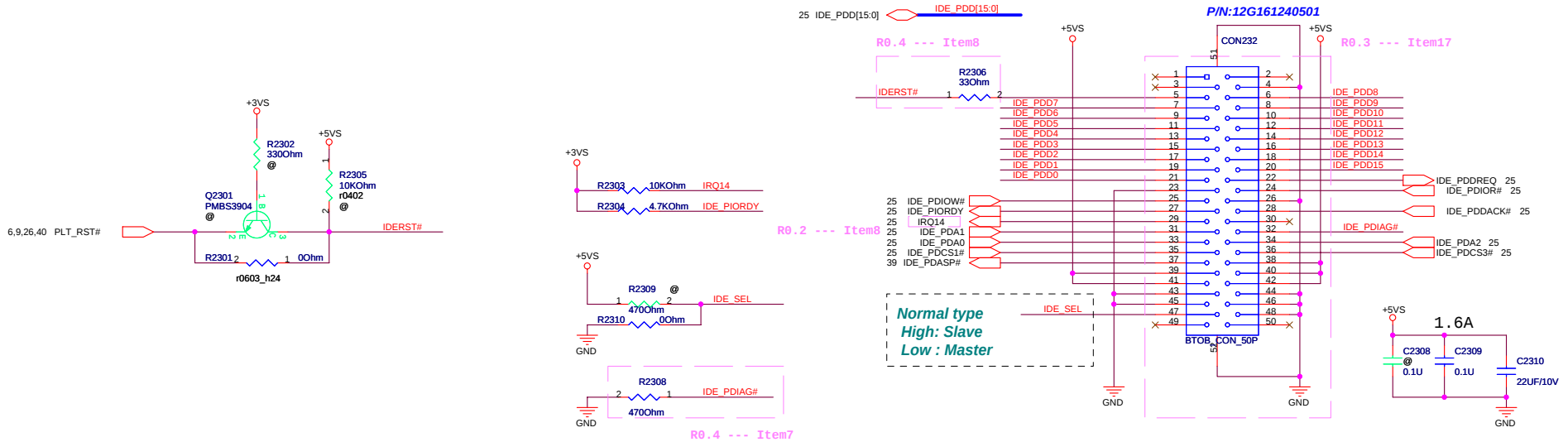




SATA HDD CON

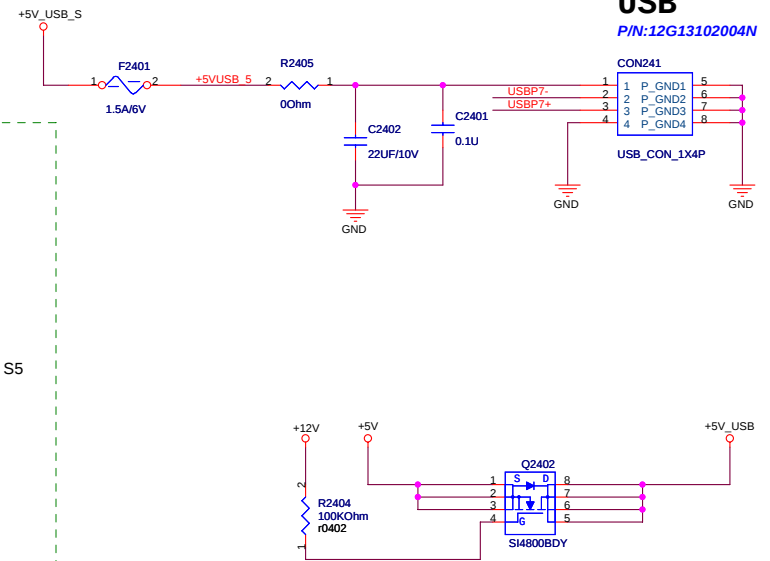
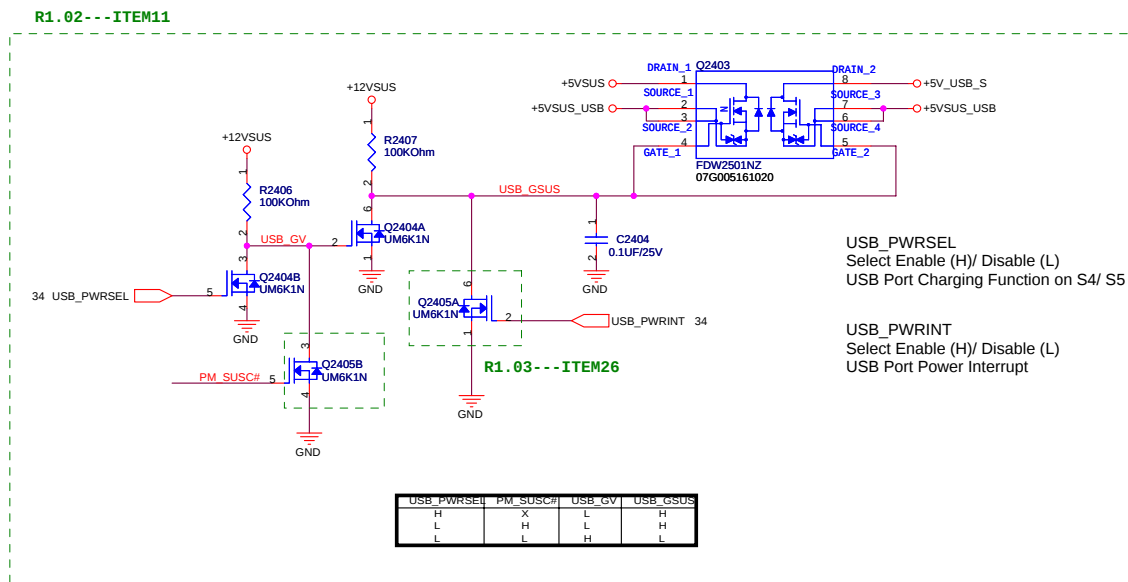
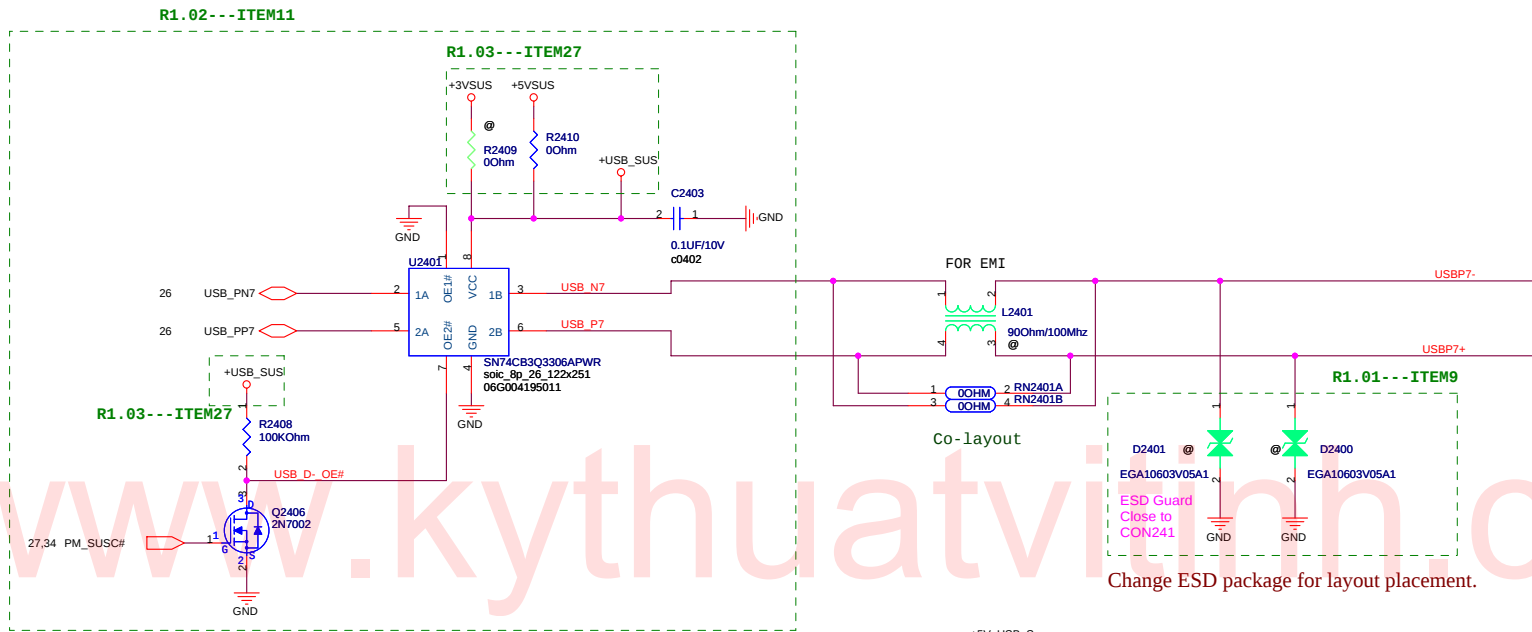


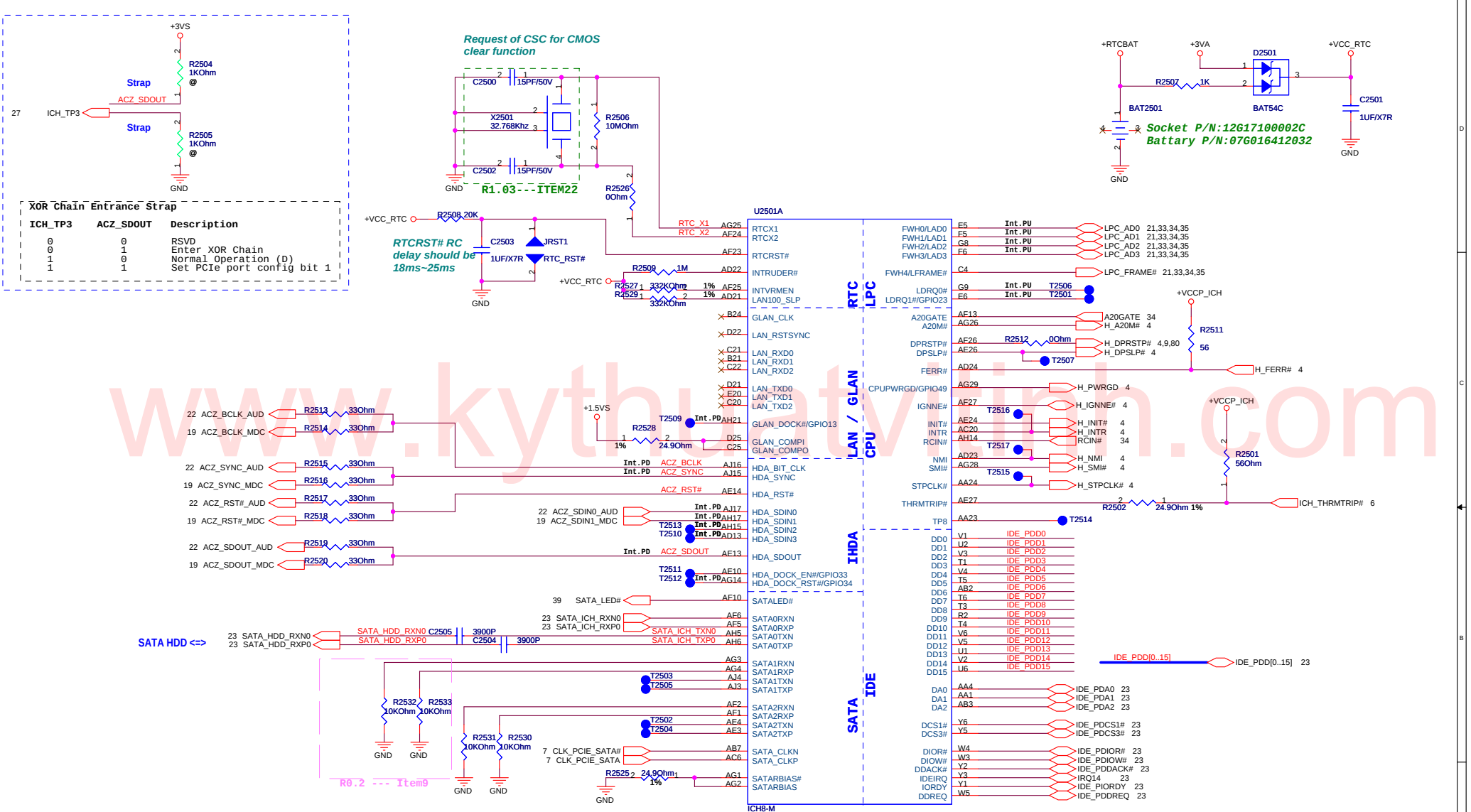
PATA CD-ROM CON

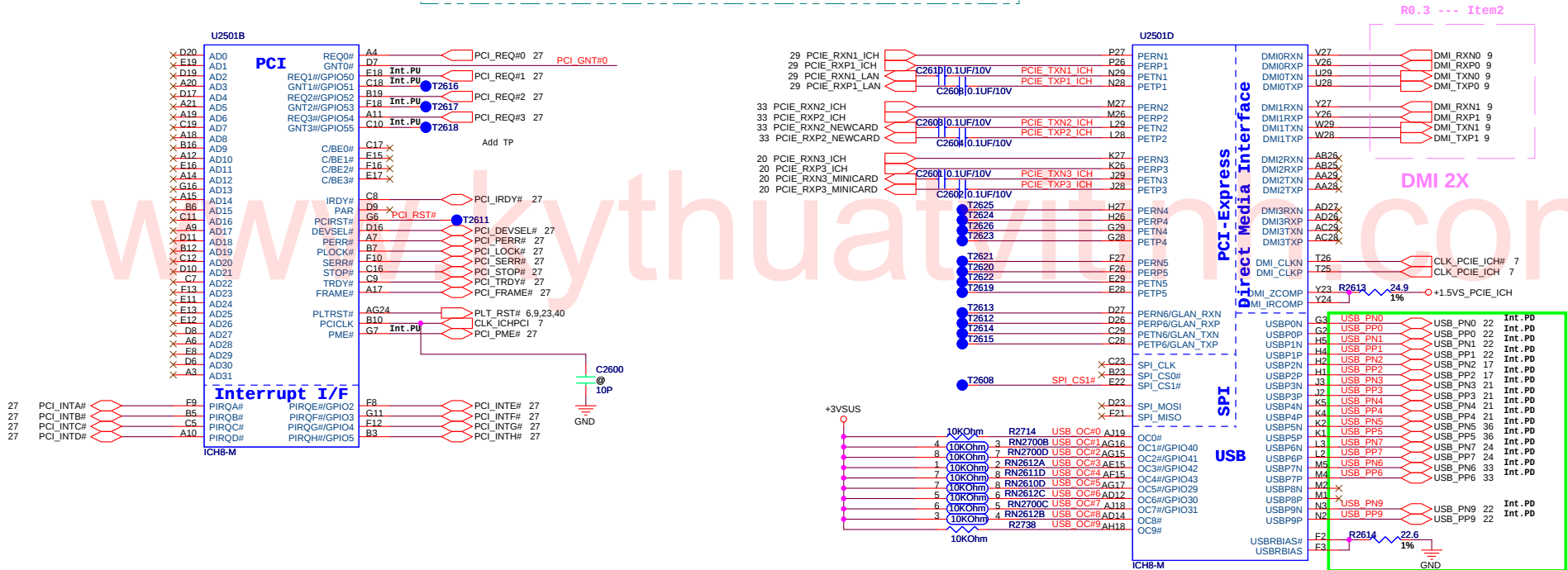
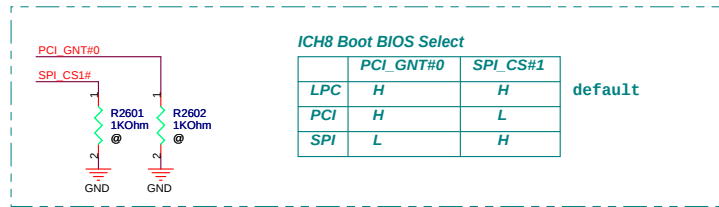


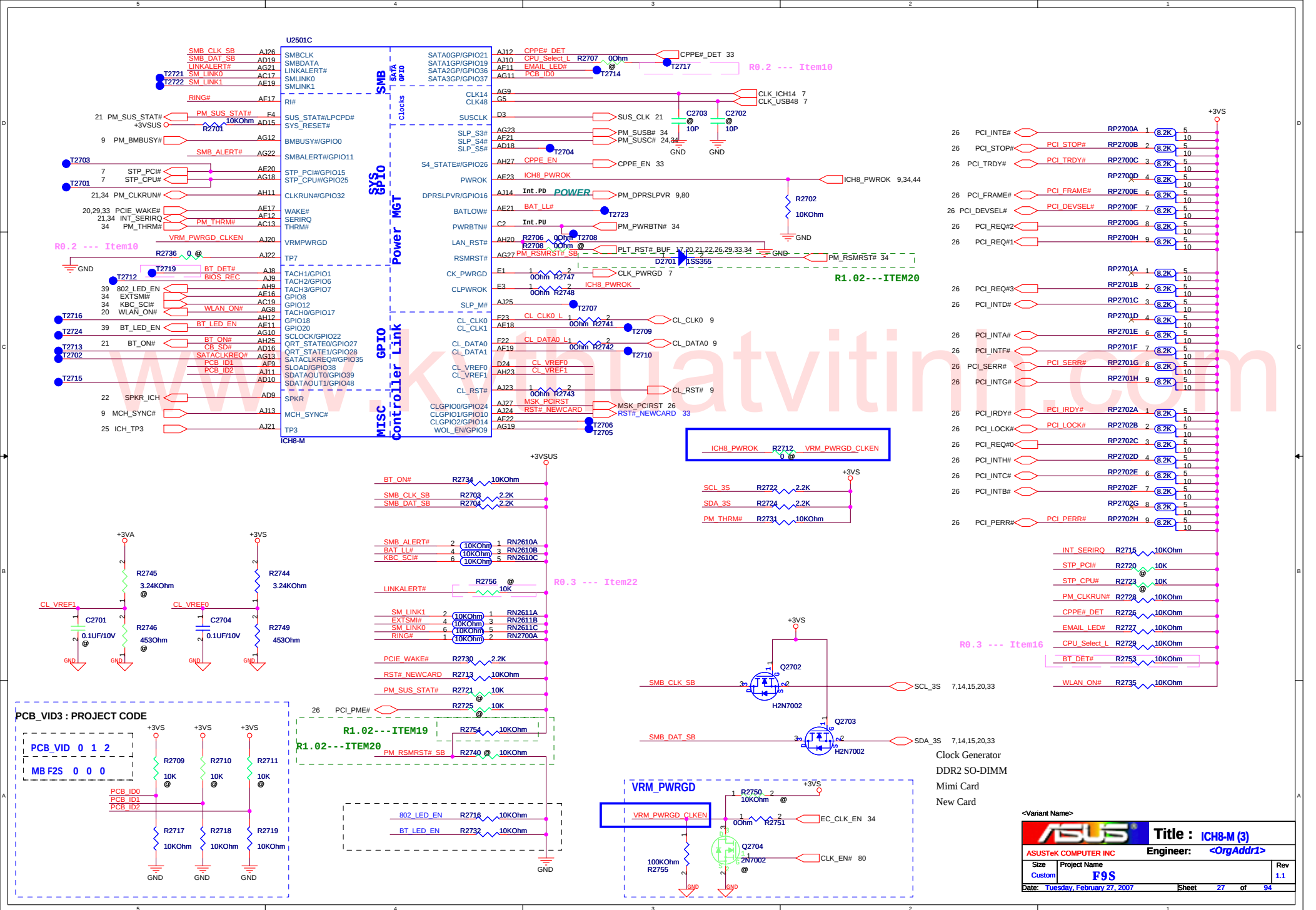
<Variant Name>

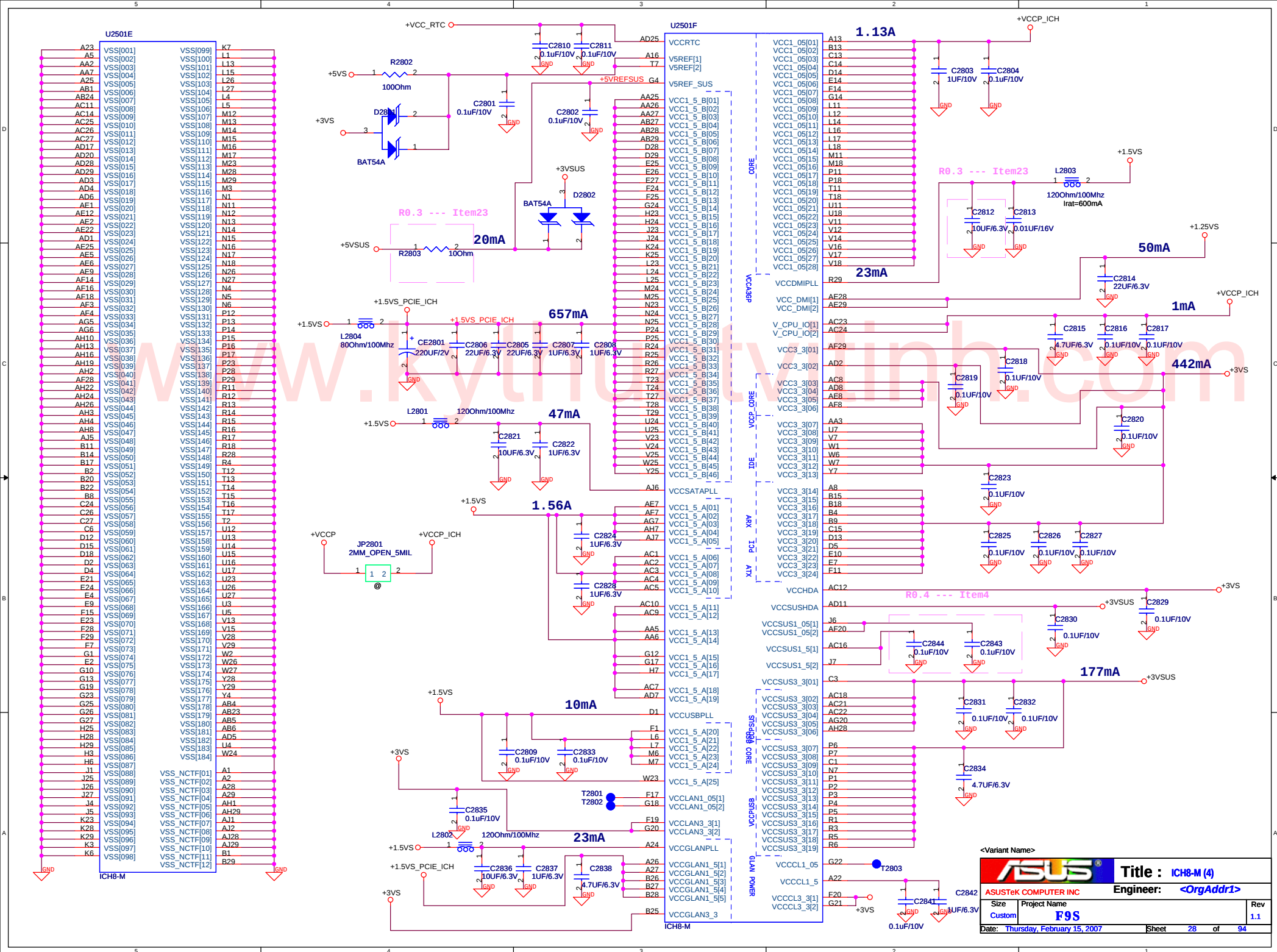
ASUS		Title : HDD & CDROM	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9S		1.1
Date: Tuesday, February 27, 2007		Sheet 23 of 94	



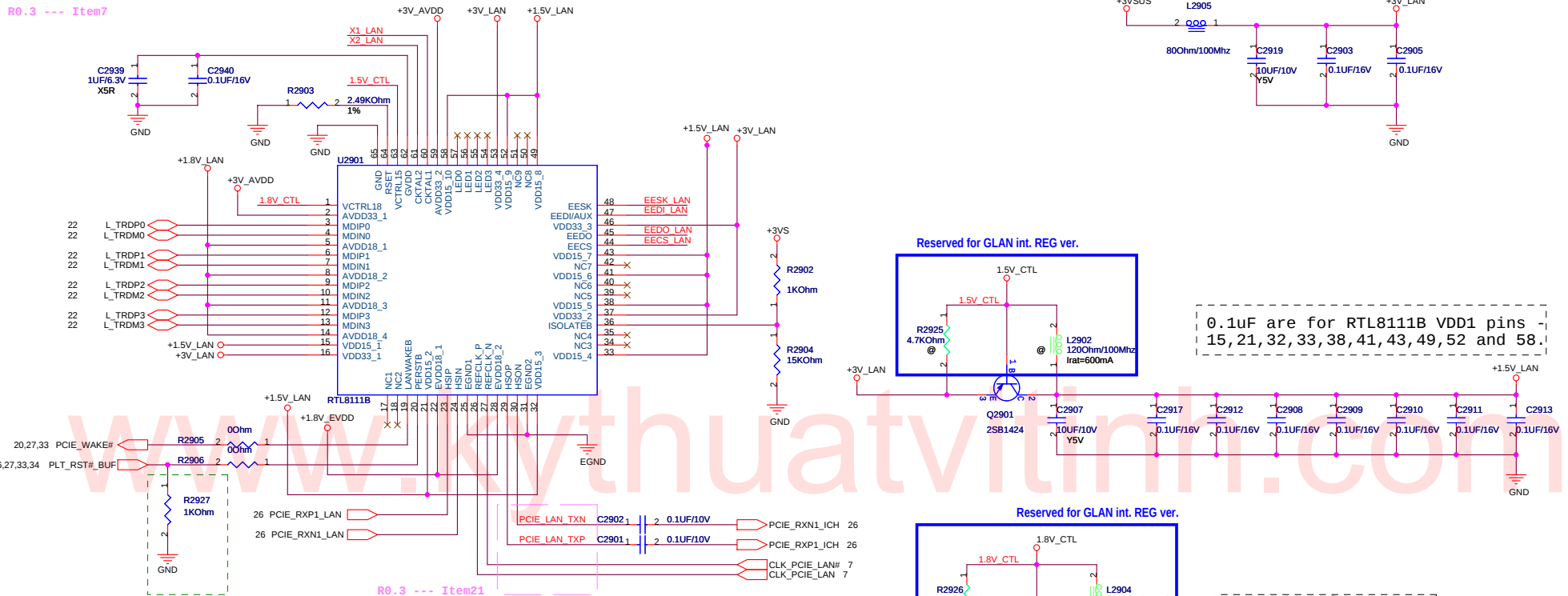




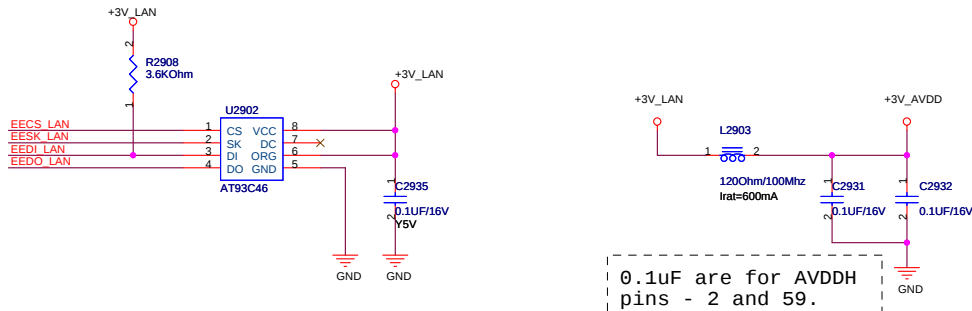




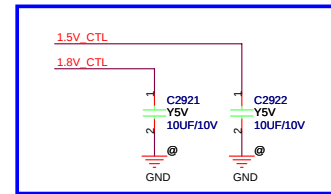
R0.3 --- Item7



Avoid current leakage from LAN when RST#



Reserved for GLAN int. REG ver.



<Variant Name>

ASUS		Title : LAN RTL8111B	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9S		1.1
Date: Tuesday, February 27, 2007		Sheet	29 of 94

www.kythuatvitinh.com

		Title :	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9S		1.1
Date: Thursday, February 08, 2007		Sheet	30 of 94

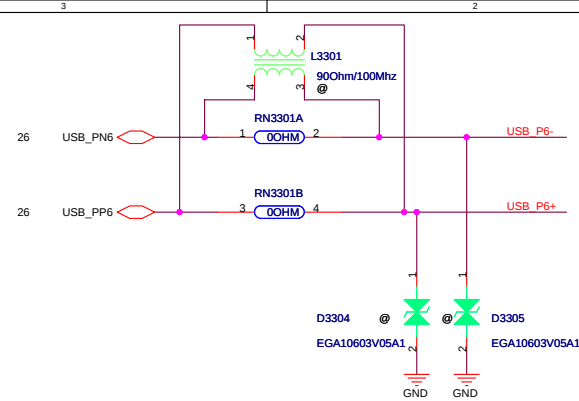
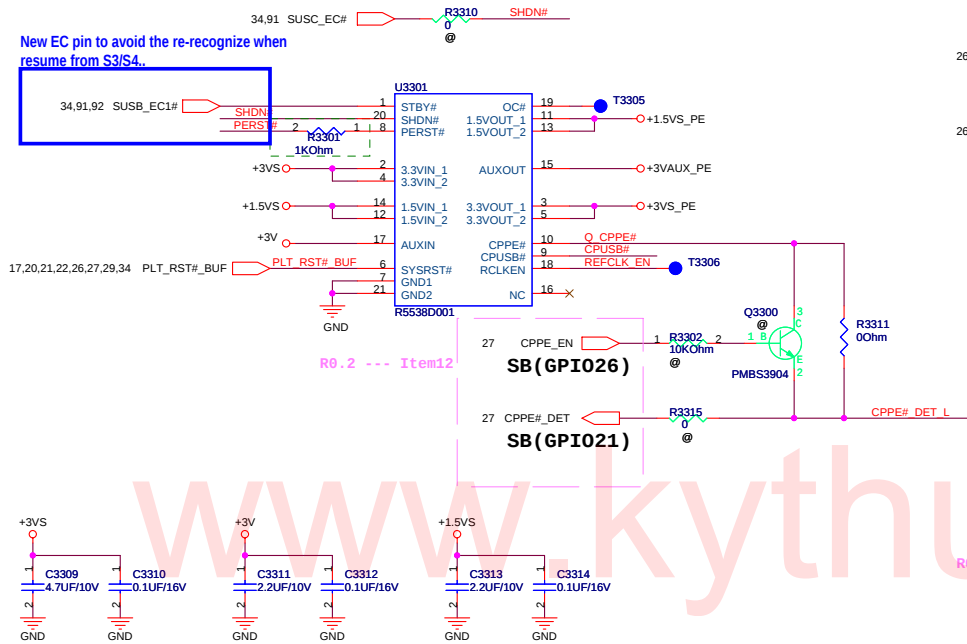
www.kythuatvitinh.com

		Title : EMPTY	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9S		1.1
Date: Monday, February 05, 2007		Sheet	31 of 94

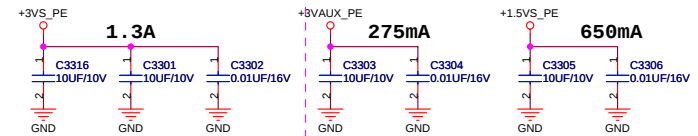
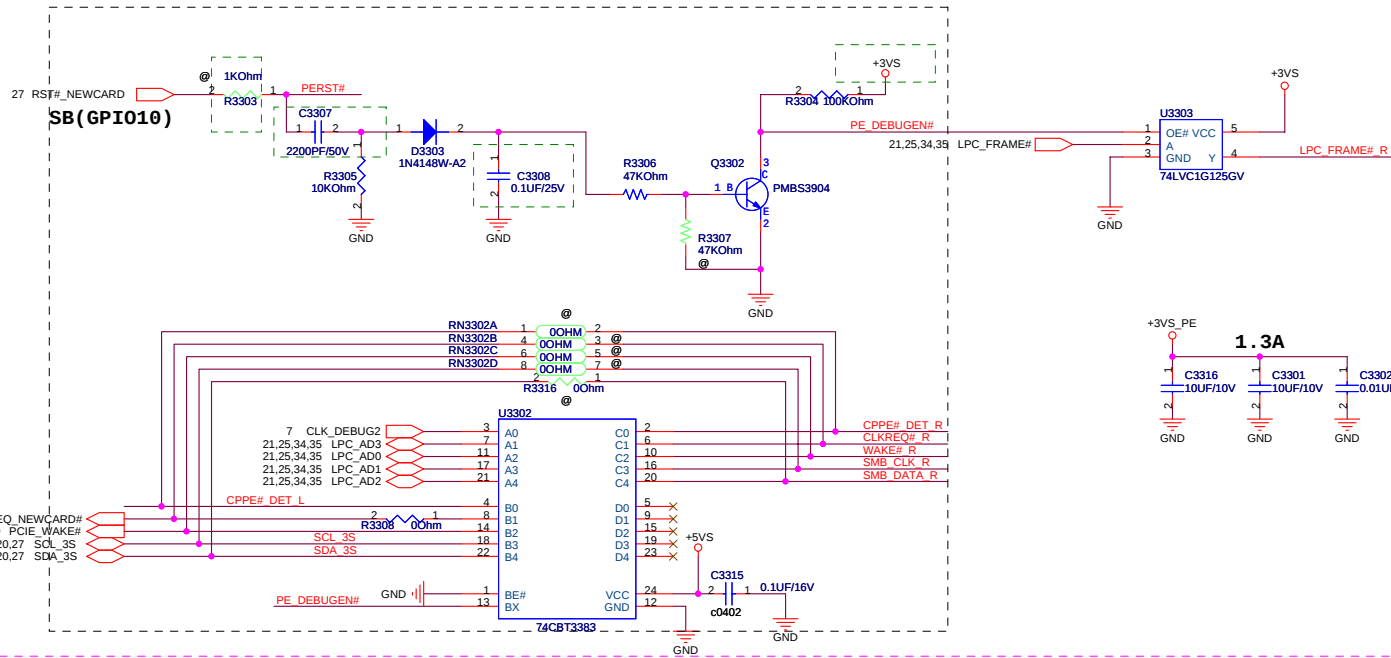
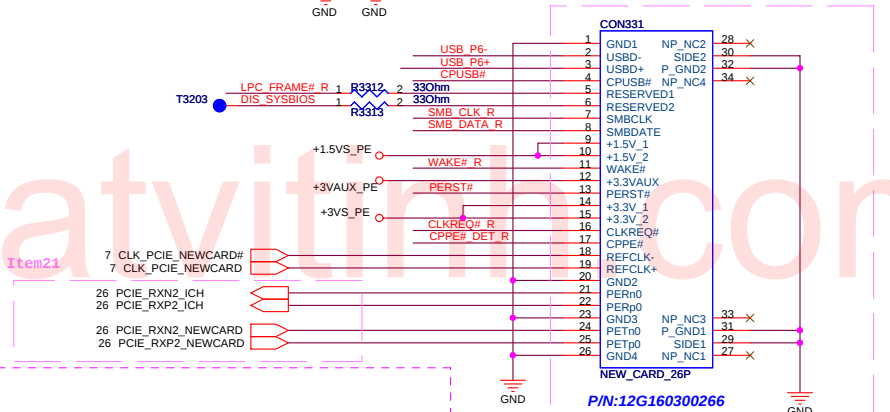
www.kythuatvitinh.com

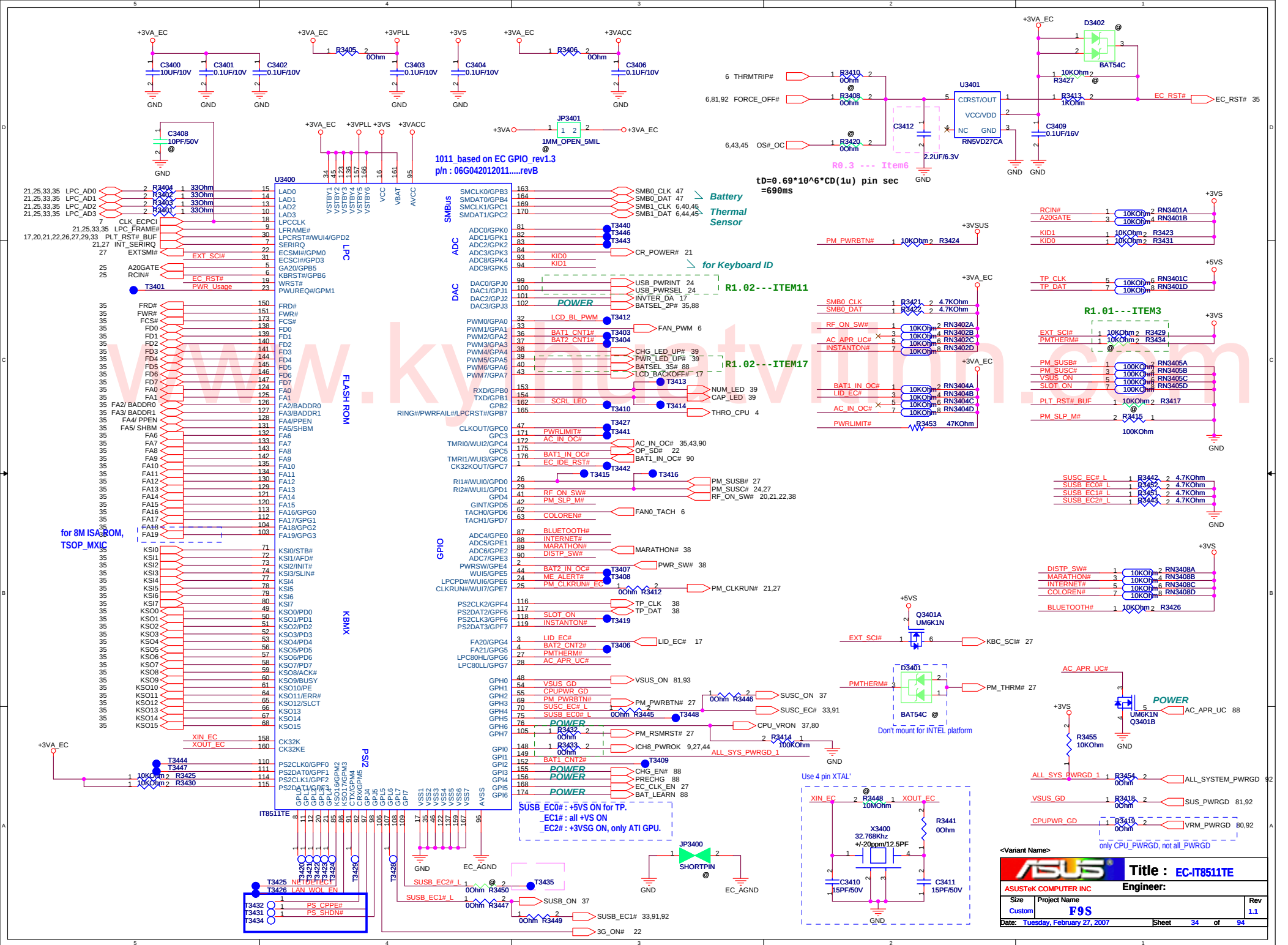
<Variant Name>		
		Title : EMPTY
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
Custom	F9S	1.1
Date: Monday, February 05, 2007		Sheet 32 of 94

New EC pin to avoid the re-recognize when resume from S3/S4..



NewCard Header



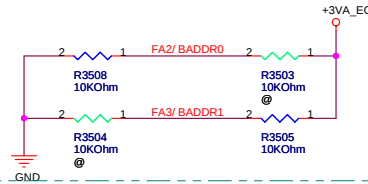


ISA ROM_TSOP

EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

00: PNPENG Access Register Pair Are 002Eh and 002Fh
10: PNPENG Access Register Pair Are 004Eh and 004Fh
01: PNPENG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
11: Reserved

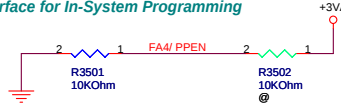


Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal

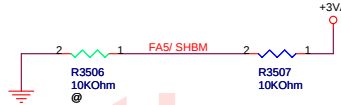
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



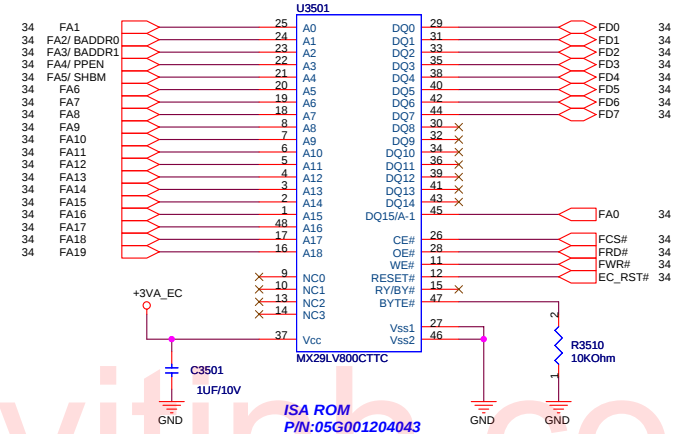
FA5/ SHBM

0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS

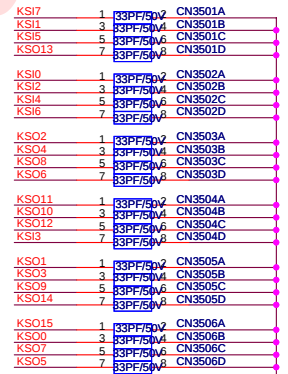


8M TSOP _ MXIC



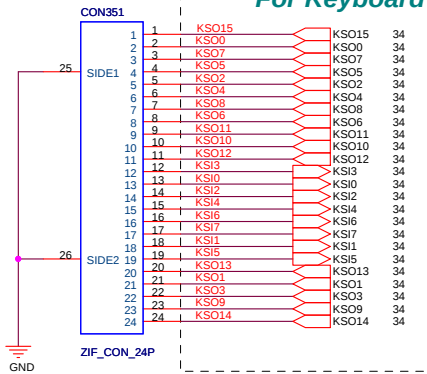
ISA ROM
P/N:05G001204043

R1.3 --- ITEM38

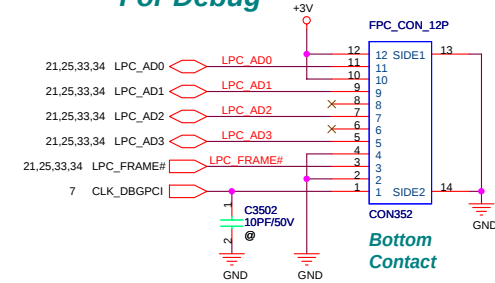


P/N:12G182402404

For Keyboard

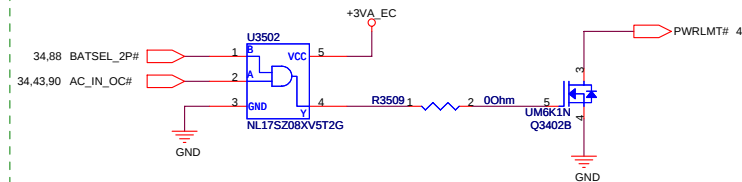


For Debug



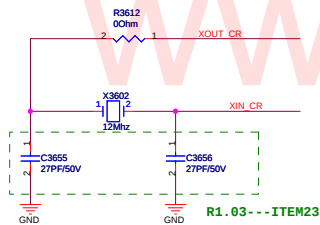
R1.03 --- ITEM28

PWRLMT Circuit: For Battery 1P

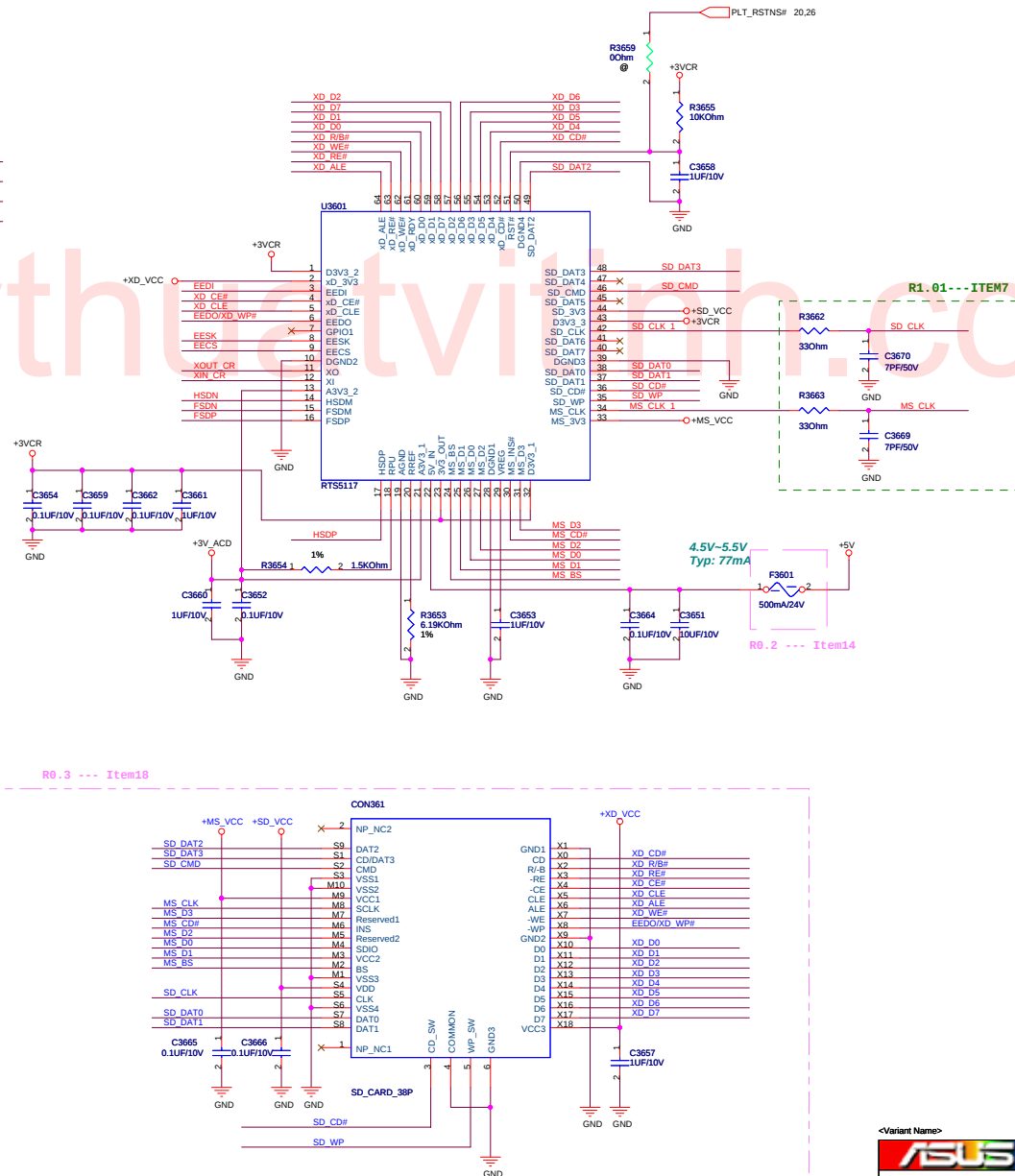
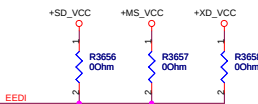
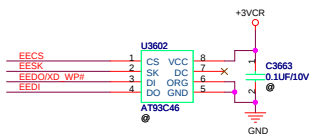


<Variant Name>

ASUS		Title : ISA_ROM&KB conn	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9S		1.1
Date: Tuesday, February 27, 2007		Sheet	35 of 94



R1.03---ITEM23

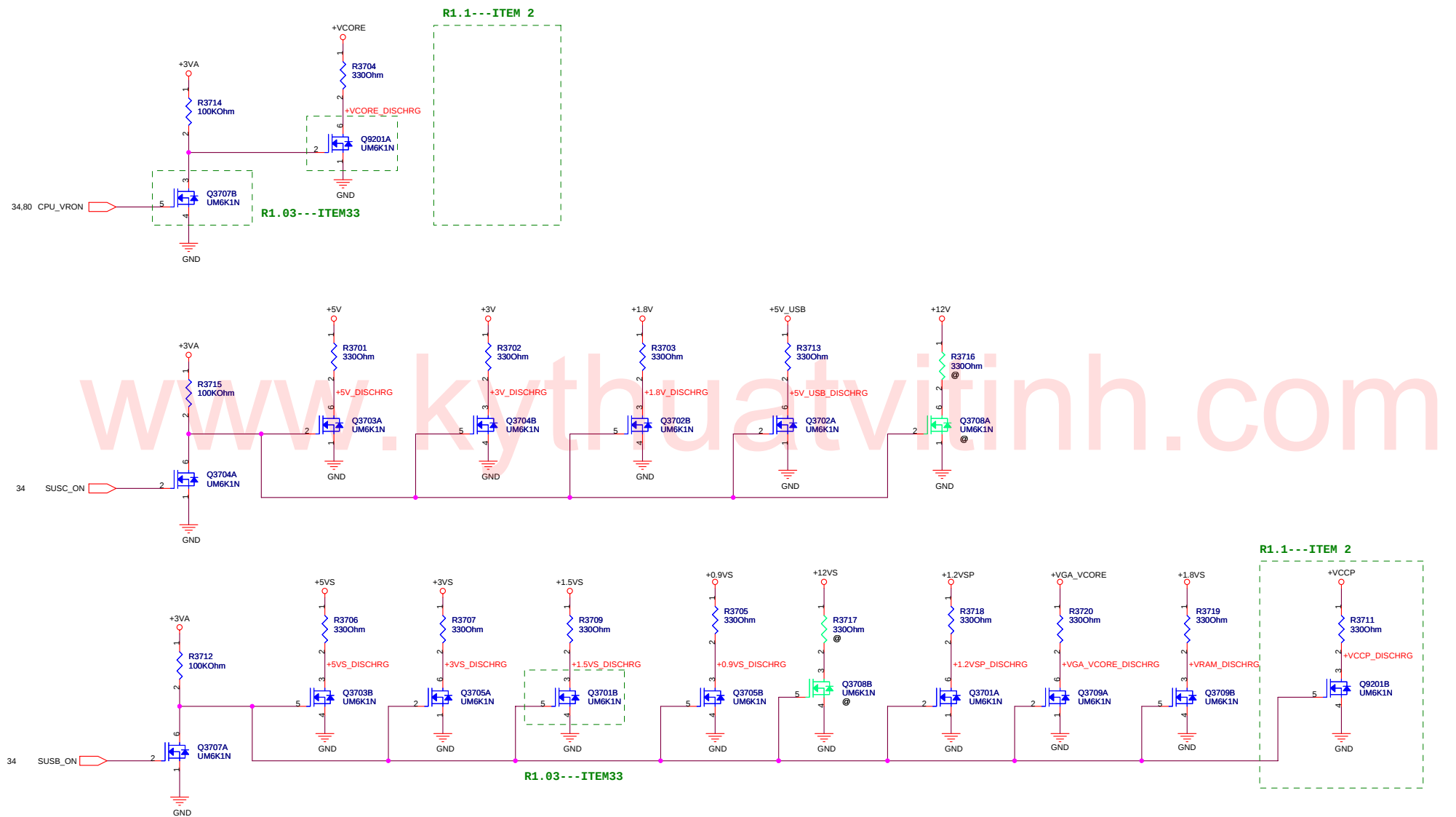


R1.01---ITEM7

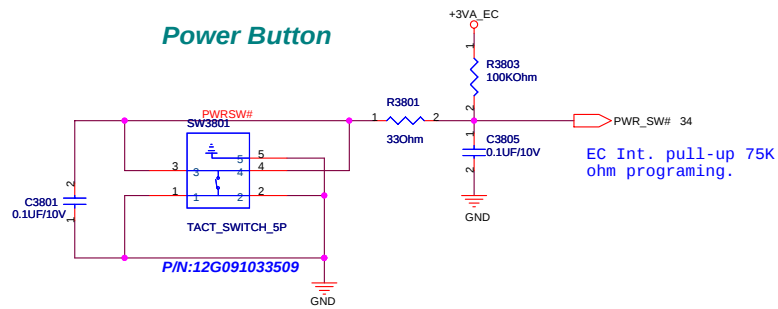
4.5V~5.5V
Typ: 77mA

R0.2 --- Item14

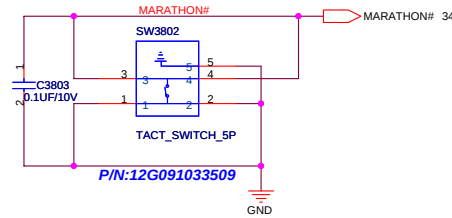
R0.3 --- Item18



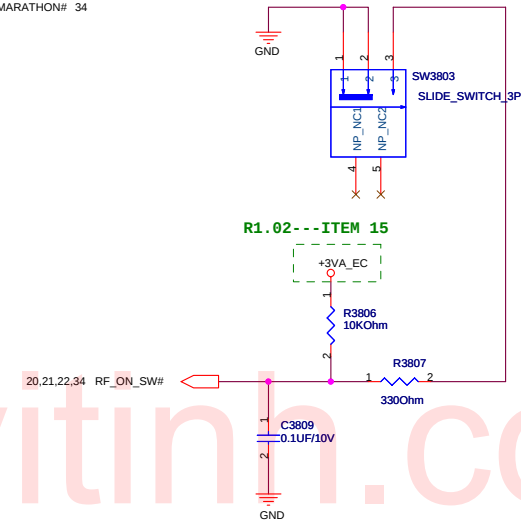
Power Button



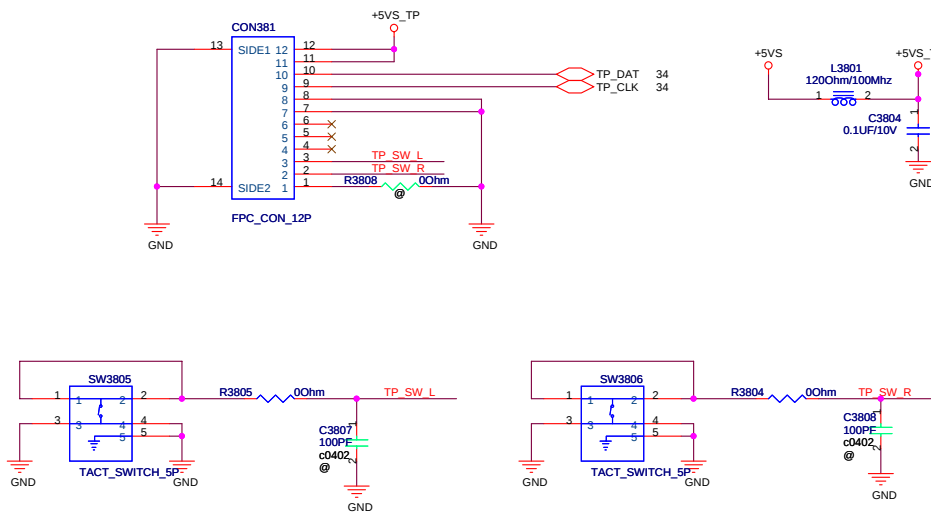
MARATHON#



BT/WLAN SW



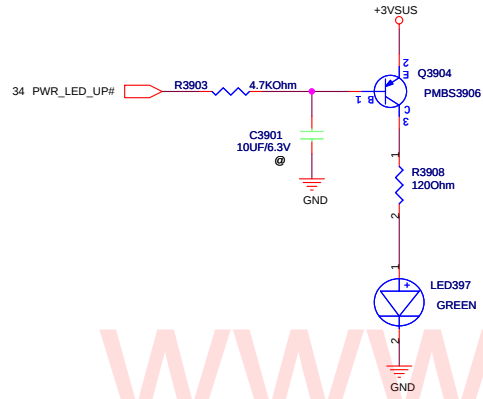
Touch-Pad



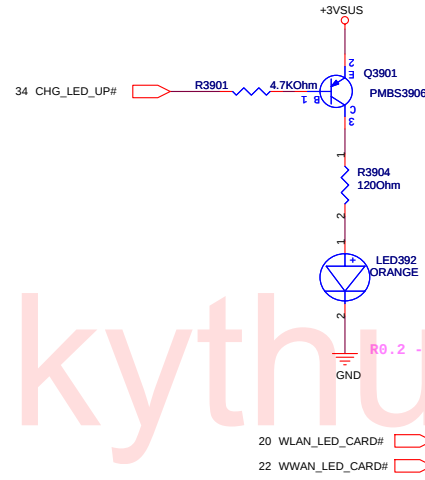
<Variant Name>

ASUS		Title : KEY & LED	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F9S	1.1	
Date:	Tuesday, February 27, 2007	Sheet	38 of 94

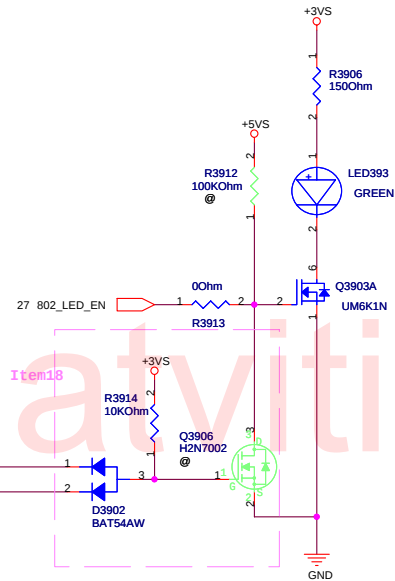
PWR LED



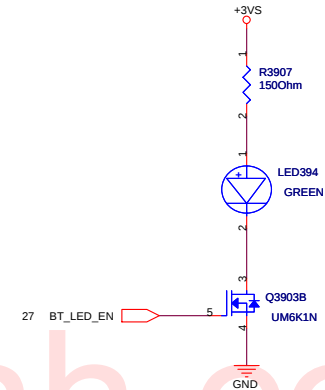
BATTERY LED



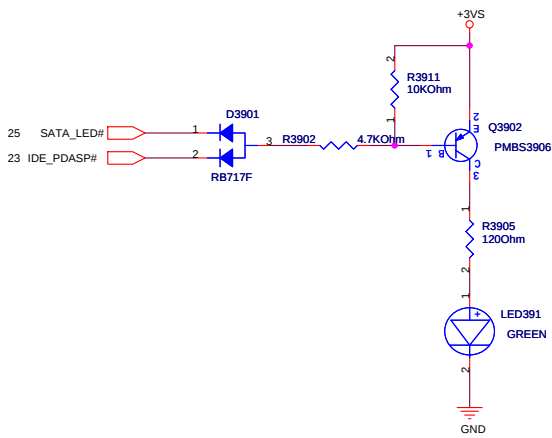
WireLess LED



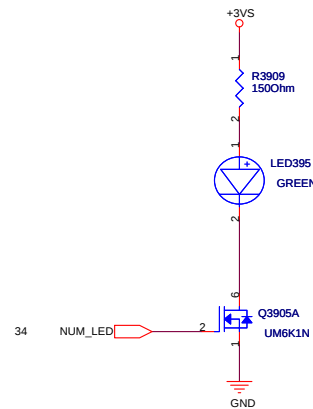
BT LED



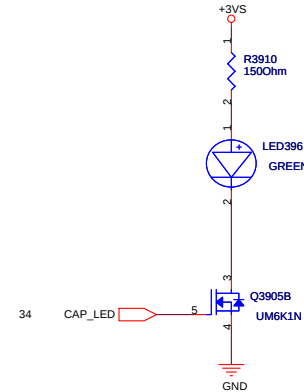
SATA/IDE LED



Num Lock

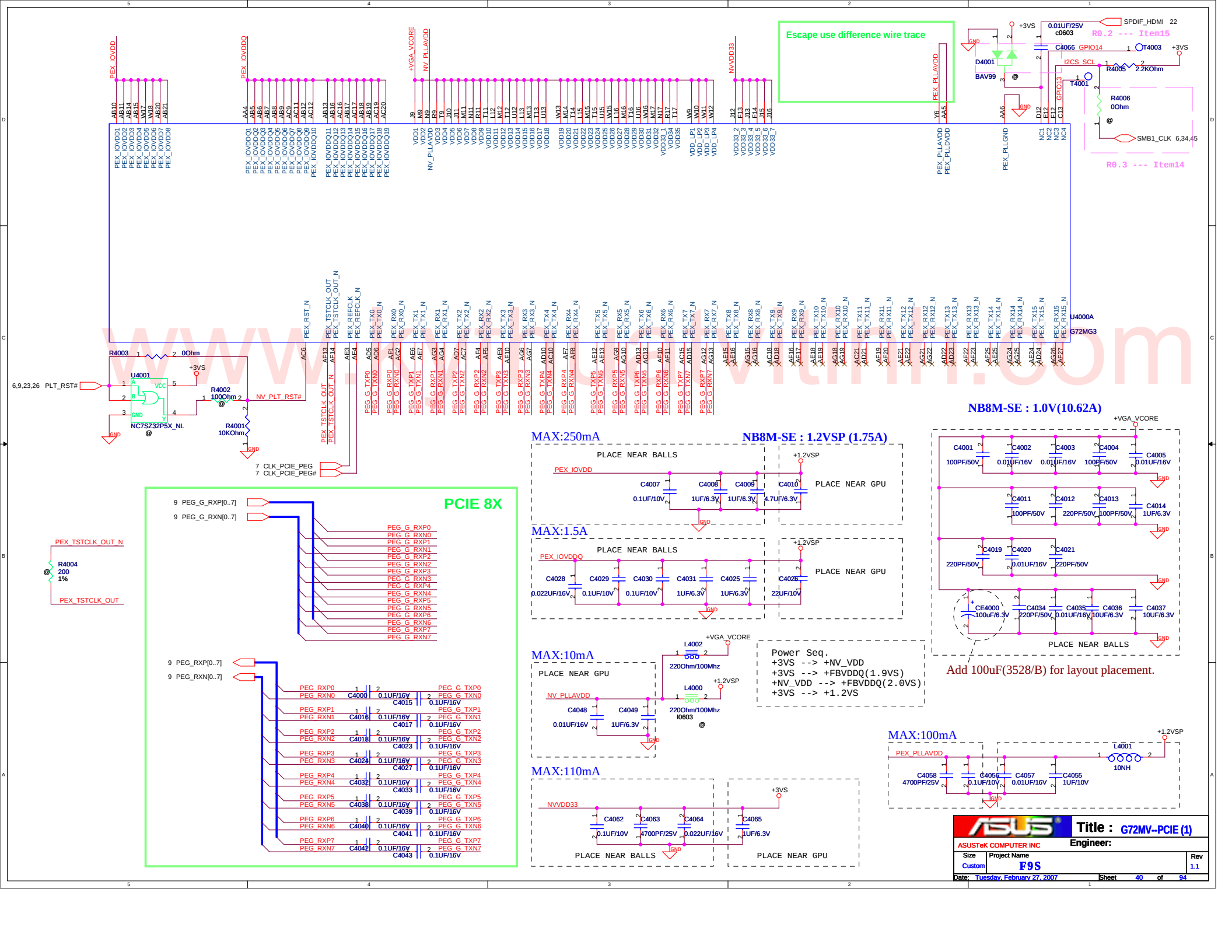


Cap. Lock



<Variant Name>

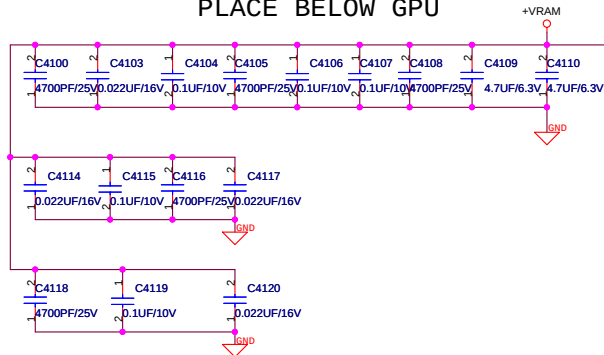
ASUS		Title : LEDs	
ASUSTek COMPUTER INC		Engineer:	
Size Custom	Project Name F9S	Rev 1.1	
Date: Tuesday, February 27, 2007		Sheet	39 of 94



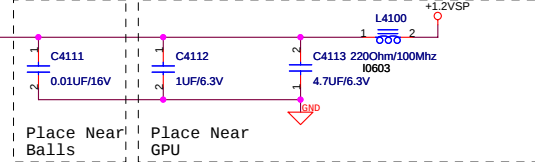
NB8M:MAX:2.47A
G72M:MAX:2.075A
G72M-V:MAX:1A

GDDR2 16x16 FBVDDQ 1.8V 84PIN

NVDD -> VRAM
PLACE BELOW GPU

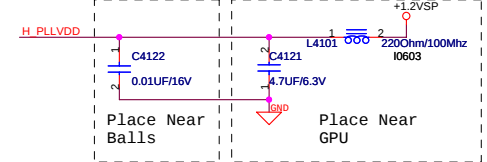


MAX:25mA



Place Near Balls
Place Near GPU

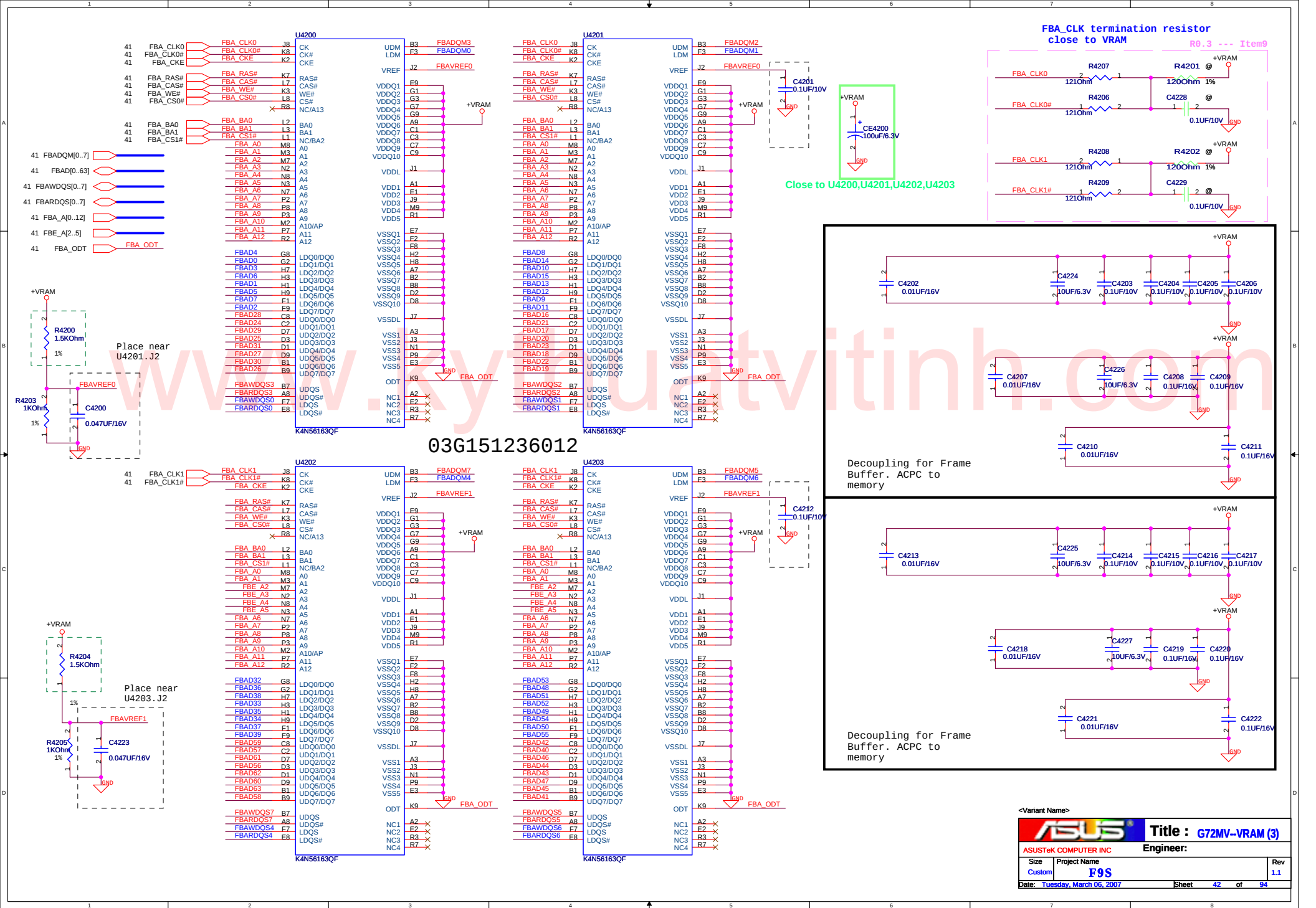
MAX:15mA

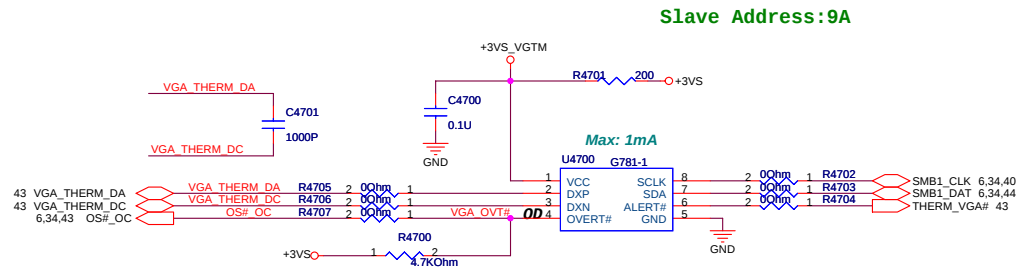


Place Near Balls
Place Near GPU

<Variant Name>

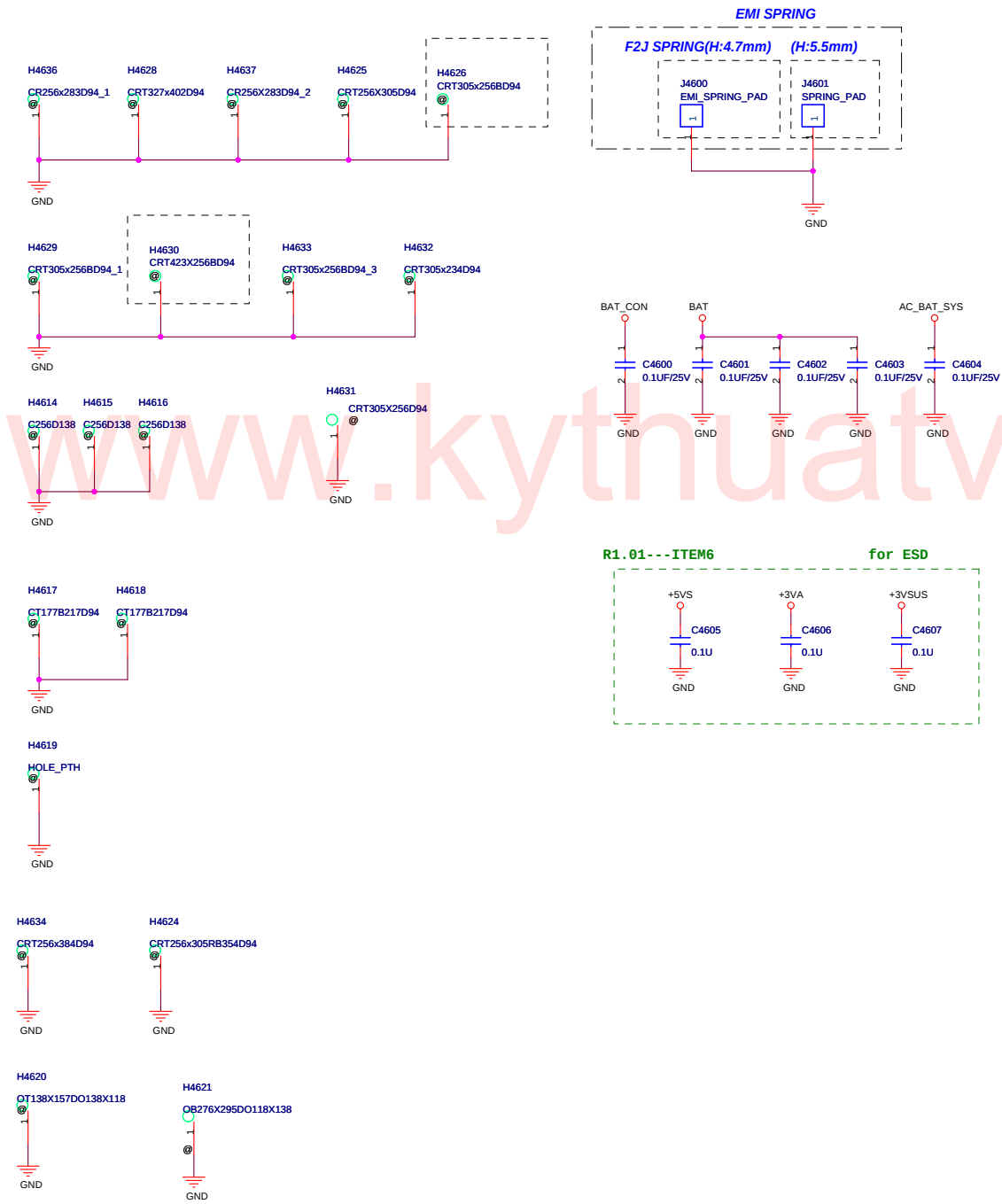
ASUS			Title : G72MV-FB (2)	
ASUSTek COMPUTER INC			Engineer:	
Size	Project Name			Rev
Custom	F9S			1.1
Date: Tuesday, February 27, 2007		Sheet 41 of 94		



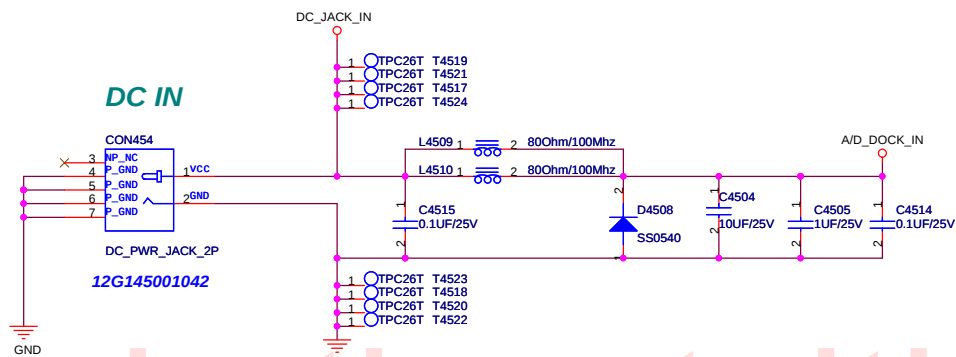


www.kythuativitinh.com

For frame buffer address/command lines those external pull up resistor can be removed for easy layout from Nvidia FAE

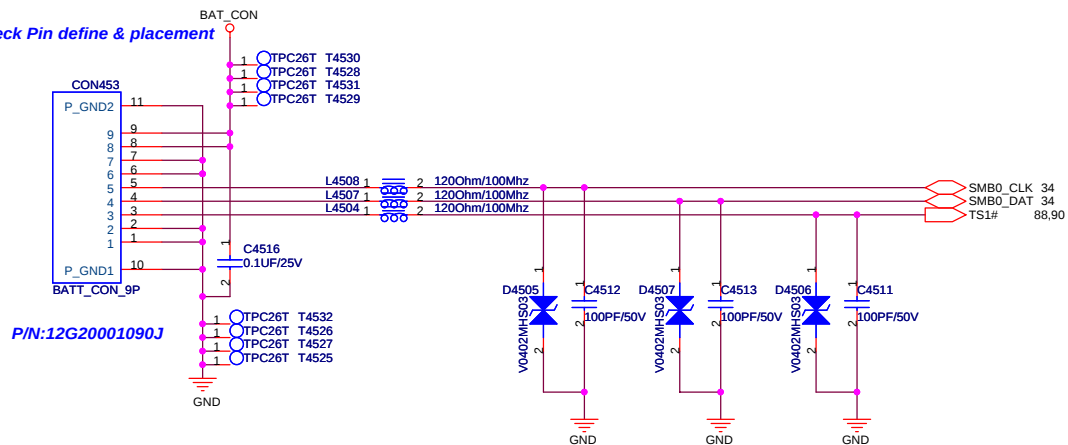


DC IN



BAT IN

Check Pin define & placement



<Variant Name>

ASUS		Title : G72M-Terminator	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F9S	1.1	
Date: Tuesday, February 27, 2007		Sheet	47 of 94

F9S SR_1128(R0.1---->R0.2)

- (1)Delete R0930,R0931 to follow Intel spec.---page9
- (2)Mount R1301 for DMI x2 ---page13
- (3)Modify netname USBP1 to USBP2 ---page17
- (4)Modify U1803,U1804 to N/A and R1817,R1818 connect to CRT_VSYNC,CRT_HSYNC ---page18
- (5)change TMDS pull high from +3VS to IFPC_IOVDD ---page19
- (6)Modify netname SUS_STAT# to PM_SUS_STAT# ---page21
- (7)Add signal for 1G LAN, ---page22
Delete R2201,R2202,Q2201,Q2202 and Modify netname ----- page22
- (8)Modify netname to IRQ14 ---page23
- (9)Delete E-SATA signal and add R2532,R2533 ---page25
- (10)Add test point T2717,T2719 ---page27
- (11)change 10/100 LAN to 10/100/1000 LAN(RTL811B) ---page29
- (12)Modify debug circuit ---page33
- (13)Modify single netname ---page34
- (14)Modify F3601 to 0.5A ---page36
- (15)Add C4066 ,D4001 for SPDIF_HDMI ---page40
- (16)Add R4434 to N/A ---page44
- (17)Add R0785,R0786,R0787 to follow Intel for CPU_BSEL ---page7
- (18)Add D3902,R3914,Q3906,R3912 for WLAN,WWAN LED(reserve) ---page39
- (19)Delete R0765,R0766,R0781,R0782,R0761,R0763 ---page7
- (20)Change CON2201 pin9 from +1.8V_LAN to GND---page22

F9S SR_1130(R0.2---->R0.3)

- (1)Delete CN1500 and add C1515~C1518---page15
- (2)DMI change to 2X---page9,26
- (3)Modify backdrive circuitry ---page44
- (4)Modify F1701 from 0.2A to 0.5A ---page17
- (5)Add R1702,C1714,Q1703 to reserve it for LCD power---page17
- (6)Delete R0719,R0721,R0723---page7
- (7)Modify L2902,L2903,L2904 size and add L2905,L2906 ---page29
- (8)R4105 change to 40ohm instead of 30ohm,and R4106 to N/A ---page41
- (9)Reserve FBA_CLKx clock terminator for NB8M-SE memory tuning---page42
- (10)Due to without TV function,C4309 and R4323 to N/A---page43
- (11)PCI_DEVICEID please set to "1000" for NB8M-SE---page44
- (12)For NB8M-SE ext. 27Mhz can connect directly without level shift,
R4422 use 0 ohm is ok---page44
- (13)For frame buffer address/command lines those external pull up resistor
can be removed for easy layout.---page45
- (14)I2CS_SCL and I2C_SDA to EC to access NB8M-SE internal thermal sensor---page40,44
- (15)Delete power limit circuit due to EC change to IT8511TE---page35
- (16)BT_DET# connect 3Vs to avoid the leakage-----Page27
- (17)Change the ODD CON(CON232) from 12G16121050P to 12G161240501 for ME request.
(Board lock hole:1.8mm; 3.0H)---Page23
- (18)CON361 change from 12G340003800 to 12G340003810 to improve the yield rate.--Page36
- (19)Add R1210,R1211 connect to GND for intel recommendation Rev1.5---page12
- (20)To modify duplicated netname from IFPC_IOVDD to IFPC_VDD ---page44
- (21)To modify duplicated netname of PCIE signal ---page29,33
- (22)Change RN2700 to 0402 size and no mount R2756 for Intel recommendation---page27
- (23)Change C2812,R2803 size from 0805 to 0603 for layout request.---page28
- (24)DDR SWAP for layout request---page14,15
- (25)Delete R3708,Q3710 due to +2.5VS power no use---page37
- (26)Add Q1802 to avoid current leakage from CRT device---page18

F9S SR_1130(R0.3---->R0.4 same as R1.0)

- (1)Change Newcard header H=3.2 and card ejector for F9S/E---page33
- (2)C3658/C3655 change from 15pF to 18pF for card reader crystal adjustment.---page36
- (3)No Mount R3806,to avoid +3VA_EC leakage to +3Vs---page38
- (4)Add C2843,C2844 connect to GND for intel recommendation---page28
- (5)Change C06XX from 10U to 22U for intel recommendation---page06
- (6)Change C3412 from 1U to 2.2U and delay EC_RST#---page34

- (7)R2308 reserve high change to pull low for intel recommendation. ---page23
- (8)Add R2306 33ohm for checklist ---page24
- (9)Add Q1901,R1928,R1929 to avoid leakage for HDMI DDC clk, and Data---page19
- (10)Add R3660,R3661,C3667,C3668(SD and MS CLK) for EMI request ---page36

F9S ER_0122(R1.0---->R1.01)

- (1)Add C2201 ~ C2208 for EMI request ---page22
- (2)Change +VCCP discharge by SUSB_ON for the correspondence with power enable ----page37
- (3)Change RES. 4R8P RN3403 to single RES R3429, R3434 for uncertain PMTHERM# leakag ---page34
- (4)Delete D1901 and add Q1902 and R1926,R1927 change to 1.8K ohm for HDMI spec. ---page19
- (5)+5VS_CRT change to +5VS_HDMI_CRT and D1806 to DNI ---page18
- (6)Add C4605,C4606,C4607 0.1uF cap. for ESD ---page46
- (7)R3660,R3661 mount 33 Ohm and C3667,C3668 mount 10p for EMI issue---page36
- (8)Power change to AC_BAT_SYS_INV for layout improve---page17
- (9)Change D2401 ,D2400 part from RSB6.8S to EGA10603V05A1---page24

F9S ER_0125(R1.01---->R1.02)

- (10)Add C2108 0.1uF cap. for ESD---page21
- (11)Add USB Port Charging Function on S4/ S5---page24
- (12))Add OS#_OC to FAN---page6
- (13)Change R0402 from 68 ohm to 1k ohm 1% because it can fixes the PROCHOT# failure when driven by thermal sensor on the CRB.----page4
- (14)Delete C0401 for intel recommend.---page4
- (15)Change WLAN SW pull up to +3VA_EC for leakage prevention.--page38
- (16)Del D0701,D0702 and add R785,R786 because there is no leakage at S3/S4 or card insertion.---page7
- (17)Power add BATSEL_3S# connect to EC.---page34
- (18)DNI useless U2603 and C2606.---page26
- (19)Reserve a RES R2754 to pull up PM_RSMRST# to +3VSUS.---page27
- (20)Change net name PM_RSMRST# to PM_RSMRST#_SB to pull up +3VSUS & add D2701 for leakage prevention.---page27

F9S ER_0126(R1.02---->R1.03 same as R1.1)

- (21)Add PLT_RST#_BUF for Sierra card modern reset signal MDL_RESET#----page22
- (22)Change C2500,C2502 from 22pF to 15pF to meet XTAL requirement---page25
- (23)C3656/C3655 change from 18pF to 27pF to meet XTAL requirement---page36
- (24)Change R0712 from 220 ohm to 270 ohm for clock signal quality improvement.--page07
- (25)Change L1811,L1812,L1813 from BEAD 120ohm to 82nH and C1832,C1834,C1836 from 22p to 10p for CRT signal quality---page18
- (26)Change Q2405,Q2407 2N7002 to UM6K1N ---page24
- (27)Add R2409,R2410 to reserve +5VSUS for SN74CBTD3306 5V power. ---page24
- (28)PWRLMT Circuit: For Battery 1P ---page35
- (29)SWAP +3V and +3VS power for 3G requirement ---page22
- (30)Add C0719,C0721 for 3G requirement ---page07
- (31)Mount L1709 common mode choke for 3G requirement---page17
- (32)Add C1715,C1716 for 3G requirement---page17
- (33)To combine UM6K1N for cost down :delete Q3706,Q9202,Q9203---page37
- (34)R1705 from 100 ohm change to 390 ohm for LCD power off sequence---page17
- (35)Mount Q4403 and remove Q4402,Q4401,R4432,R4433 for cost down---page44

F9S ER_0207(R1.1---->R1.2)

- (36)LVDS conn. pin modification for LVDS coaxial cable---page17

F9S ER_0215(R1.2---->R1.3)

- (37)Power Team modify +1.5VS power rating to 3.5A ---page82
- (38)Add CN3501~CN3506 for 3G requirement---page35
- (39)Change CLK_TPMPCI R0707 from 33 ohm to 27 ohm and mount C0725(10p) to meet edge rate spec---page36

		Title : History(1)	
ASUSTeK COMPUTER INC		Engineer:	
Size Custom	Project Name F9S		Rev 1.1
Date: Thursday, March 01, 2007		Sheet	48 of 94

F9S ER_0122(R1.0---->R1.01 same as R1.1)-----POWER

change list:

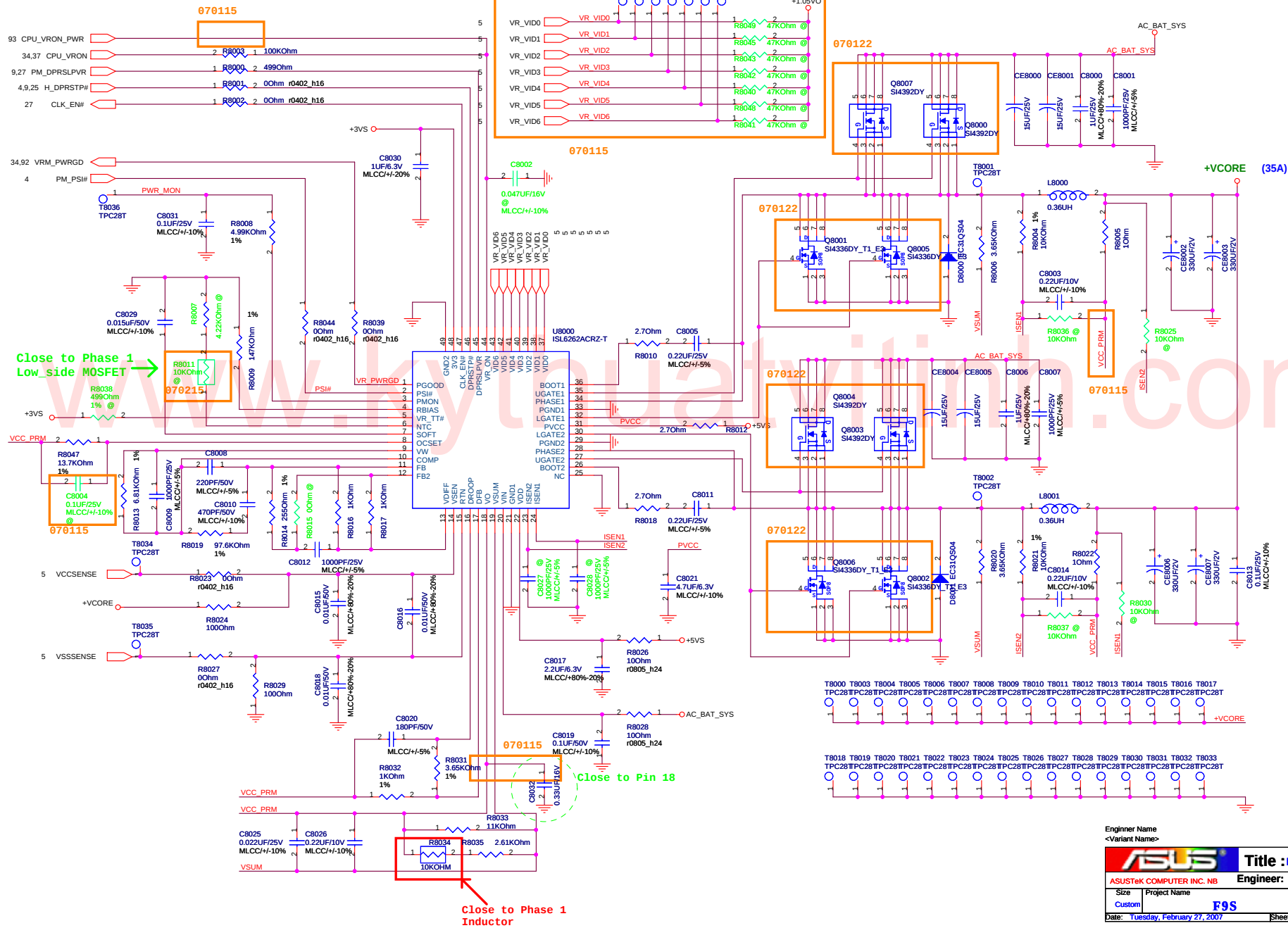
1. Delete R8046.
2. Change C8004(DNI) to U8000 pin8.
3. Change C8032 to U8000 pin18.
4. Add test point T8037~T8042.
5. For power sequency, change R8400 from 0 to 20K ohm.
6. For OCP adjust, change R8407 from 200K to 30K ohm.
7. For output voltage adjust, change R8406 from 20K to 4.22K, change R8409 from 100K to 20K ohm.
8. To Increase the saturation crrent of L8400, change L8400 from 09G02X103022 to 09G02X103U00.
9. DNI Q8404 and R8408.
10. Delete Q8505 and Q8501.
11. Change L8500 from 0.56uH to 1uH.
12. For OCP adjust, change R8508 from 100K to 51K.
13. For PWM oscillation issue, change output capacitor to 150uF/2V(ESR=18m ohm) *2.
14. For power sequency, change R8504 from 0 to 120K, change C8504 from DNI to 0.1uF, change C8515 from 0.033uF to 0.1uF.
15. Add JP8805 for layout improve.
16. Add 3S/4S selector circuit(DNI).
17. Add U9001 colay to U9000.
18. For power sequency, change R9108 and R9107 to 47K, change R9109 and R9110 to 22K, Delete R9106 and R9112.
19. Change Schematic_Part at Q8000,Q8001,Q8002,Q8003,Q8004 Q8005,Q8006,Q8007,Q8300,Q8301,Q8401,Q8403.
20. Change L8101 from 3.3uH/CYNTEC to 3.8uH/SUMIDA.
21. Change R8120 from 21K to 20K for OCP adjust.
22. For spec. change.Chagne Q8004 from SI4392 to SI4800, Change Q8006 from SI4336to SI4800, Change R8524 from 30K to 174K, Change L8500 from 1uH/18A to 1.8uH/9A. DNI CE8506, CE8504.

F9S ER_0215(R1.1 --> R1.3)-----POWER

23. Power team modify +1.5VS power rating to 3.5A ---page82

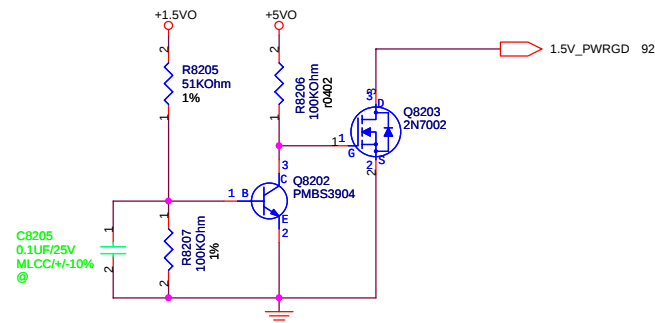
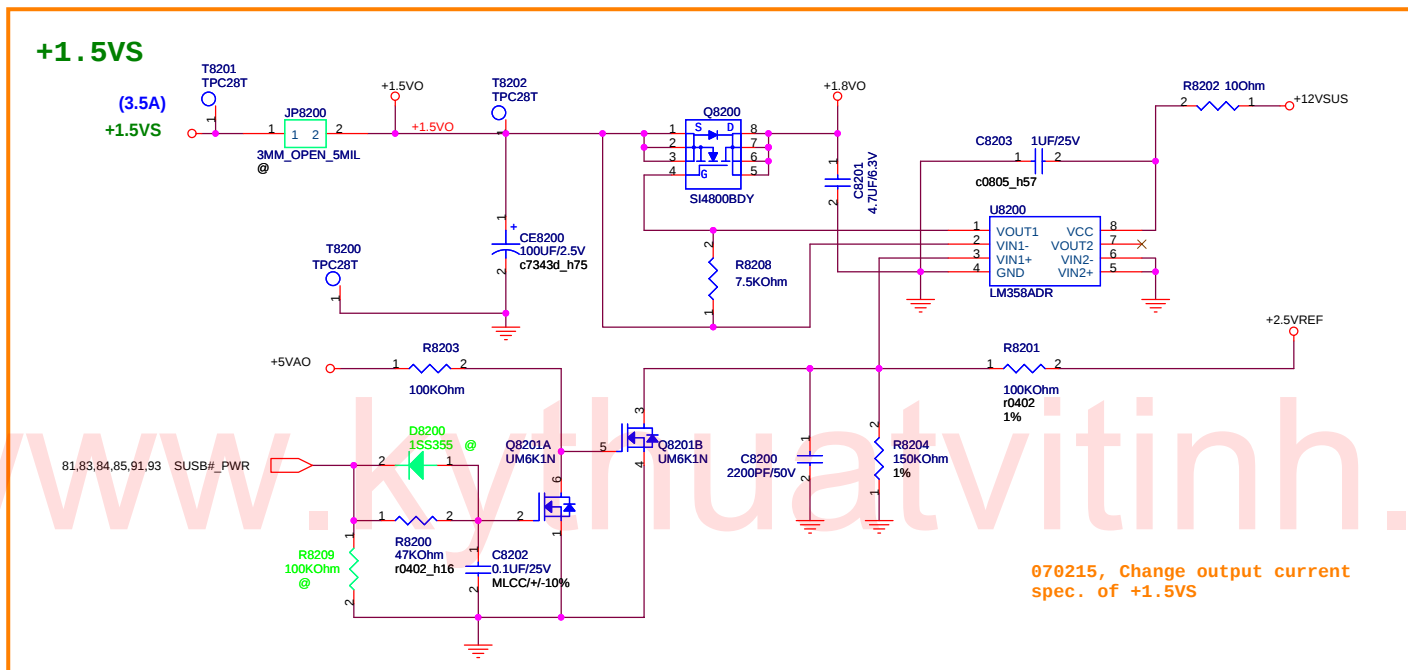
<Variant Name>

		Title : History(2)	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9S		1.1
Date: Thursday, February 15, 2007		Sheet	49 of 94



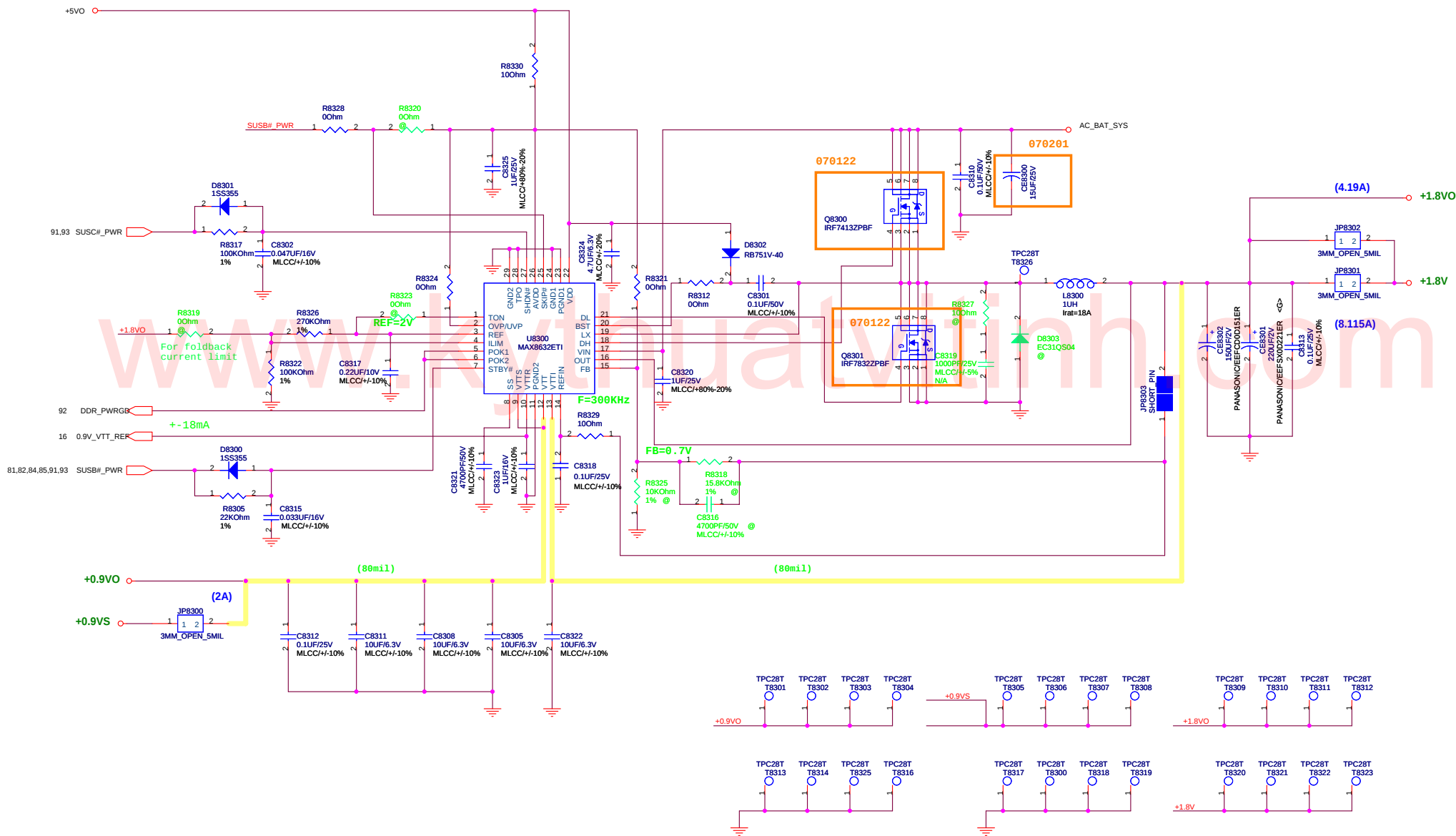
Engineer Name
<Variant Name>

		Title : POWER_VCORE	
ASUSTeK COMPUTER INC. NB		Engineer:	
Size	Project Name		
Custom			
		F9S	
Date: Tuesday, February 27, 2007		Sheet 80 of	



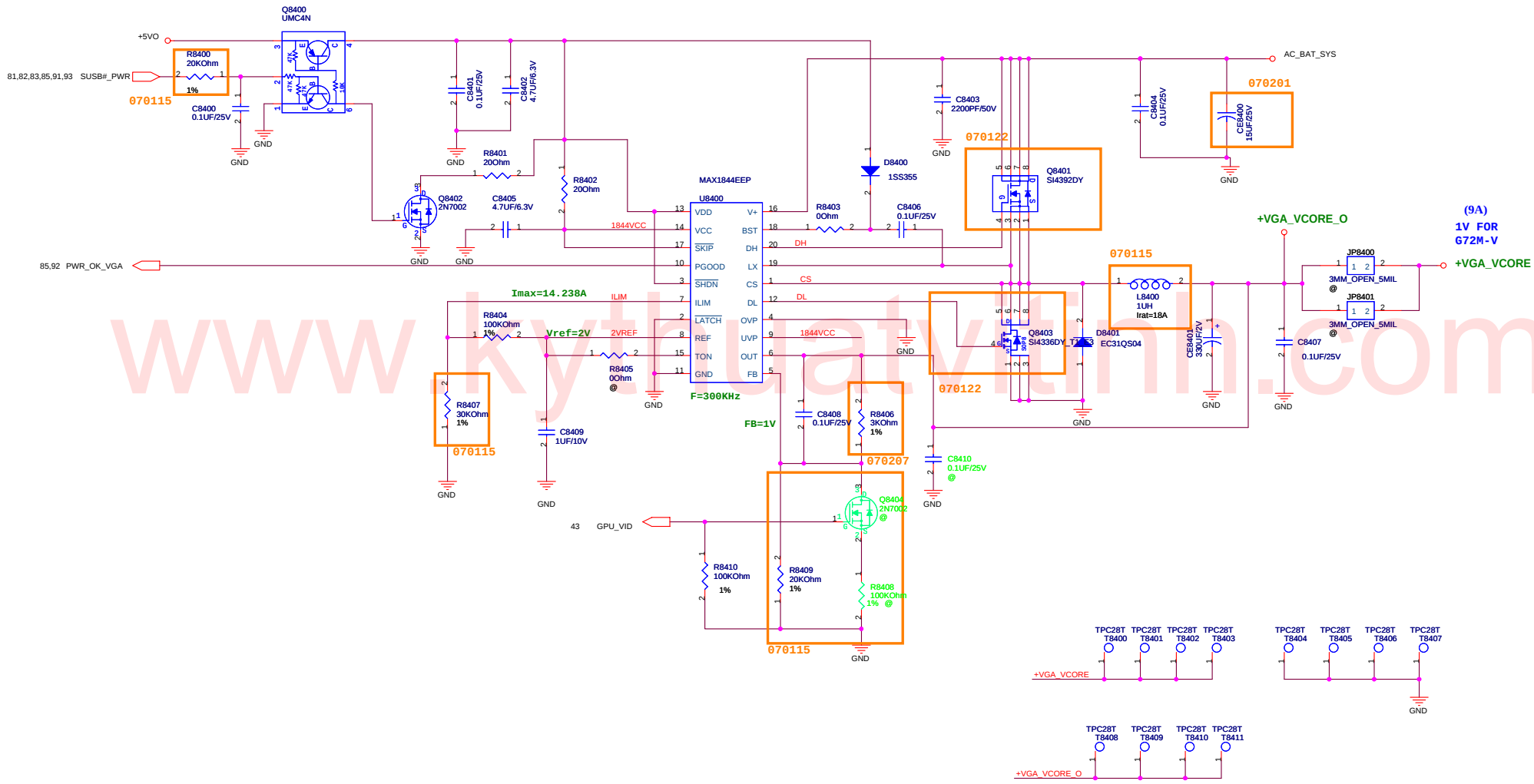
<Variant Name>

ASUS		Title : POWER_I/O_1.5VS & 1.05VS	
ASUSTeK COMPUTER INC. NB		Engineer: Ehong-Ping	
Size B	Project Name F9S		Rev 1.0
Date: Tuesday, February 27, 2007		Sheet	82 of 94



<Variant Name>

ASUS		Title : POWER_I/O_DDR & VTT	
ASUSTeK COMPUTER INC. NB		Engineer: Ehong-Ping	
Size	Project Name	Rev	
Custom	F9S	1.0	
Date: Tuesday, February 27, 2007		Sheet	83 of 94



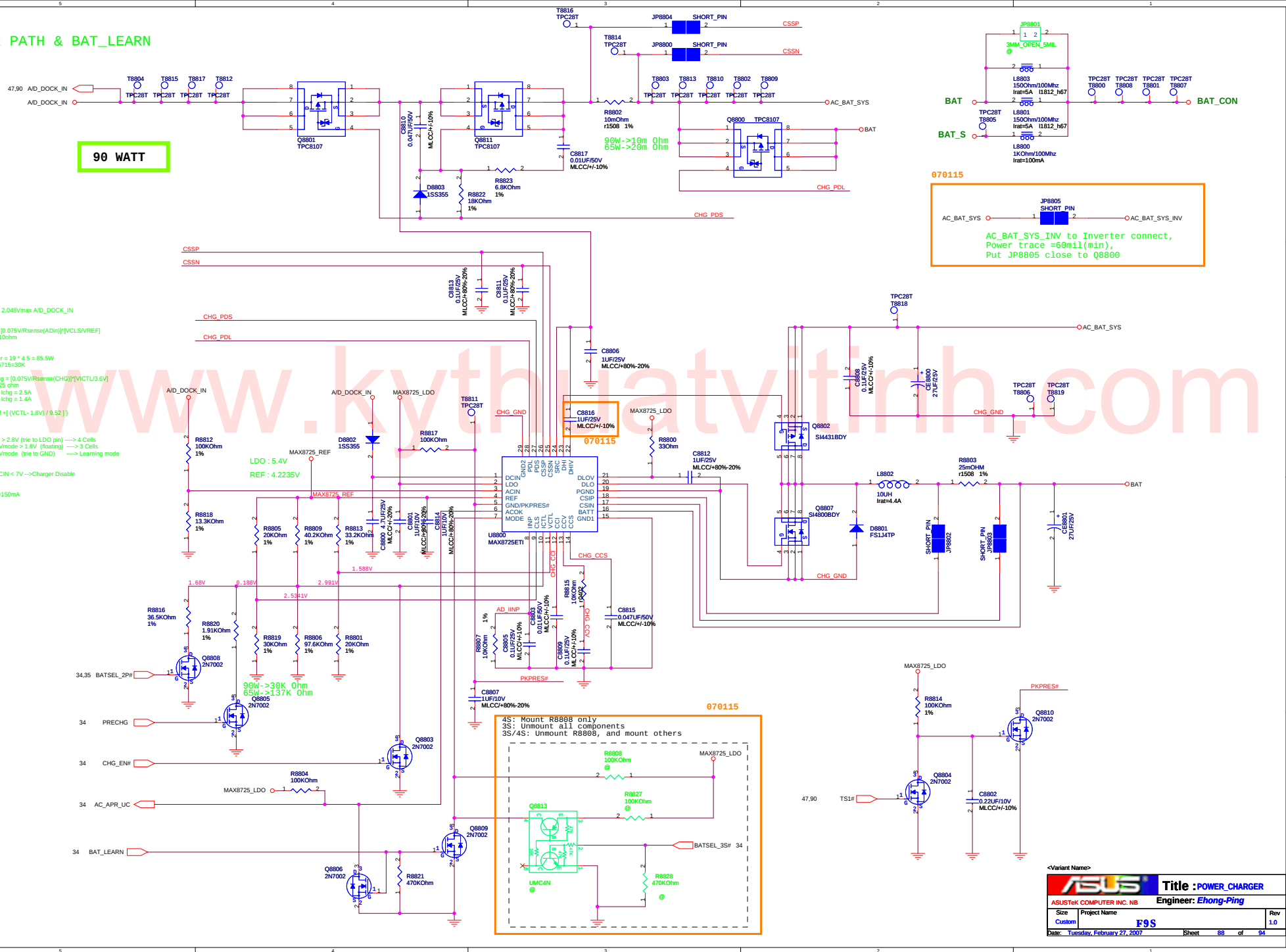
www.kythuatvitinh.com

<Variant Name>		
		Title : <i>N/A</i>
ASUSTeK COMPUTER INC. NB		Engineer: <i>Ehong-Ping</i>
Size B	Project Name F9S	Rev 1.0
Date: <i>Thursday, February 15, 2007</i>		Sheet <i>86</i> of <i>94</i>

www.kythuatvitinh.com

<Variant Name>		
		Title :POWER_SHUTDOWN#
ASUSTeK COMPUTER INC. NB		Engineer: Ehong-Ping
Size	Project Name	Rev
Custom	F9S	1.0
Date: Thursday, February 15, 2007		Sheet 87 of 94

POWER PATH & BAT_LEARN

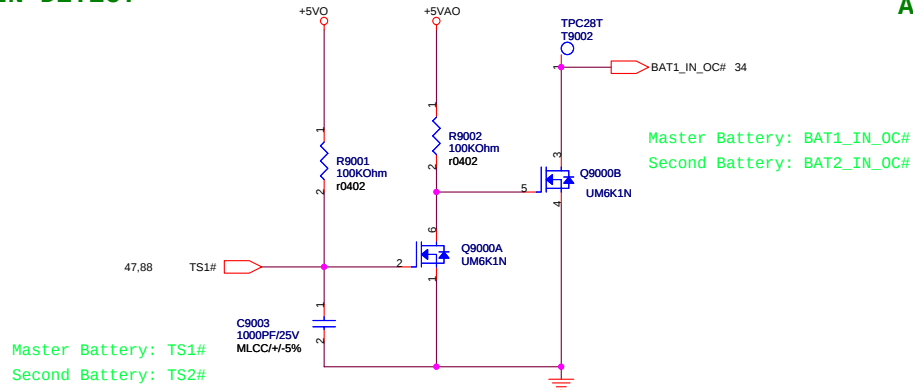


<Variant Name>	
	Title : POWER_CHARGER
ASUSTeK COMPUTER INC. NB	Engineer: Ehong-Ping
Size Custom	Project Name F9S
Date: Tuesday, February 27, 2007	Sheet 88 of 94 Rev 1.0

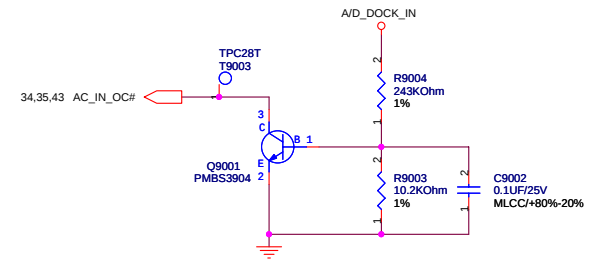
www.kythuatvitinh.com

<Variant Name>			
		Title : NIA	
ASUSTeK COMPUTER INC. NB		Engineer: Ehong-Ping	
Size	Project Name		Rev
Custom		F9S	1.0
Date: Thursday, February 15, 2007		Sheet	89 of 94

BATTERY IN DETECT

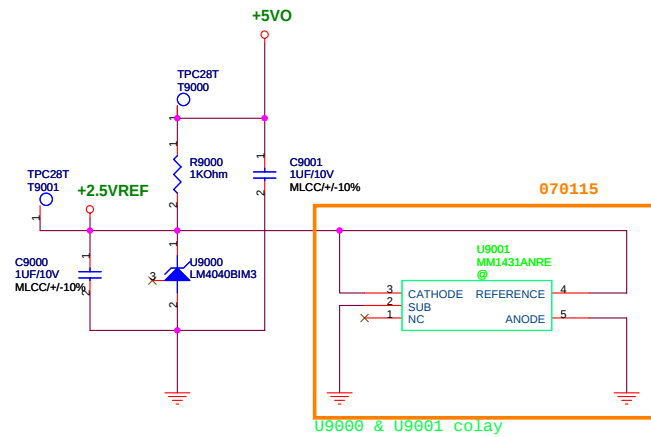


ADAPTER IN DETECT



www.kythuatvitinh.com

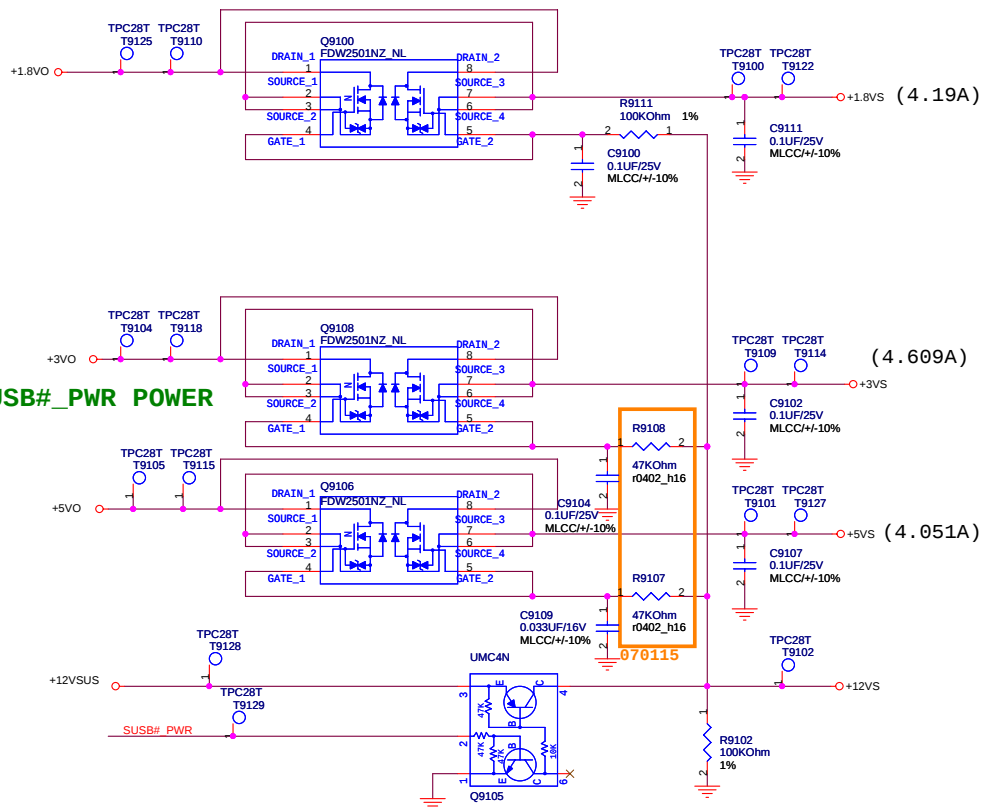
+2.5VREF



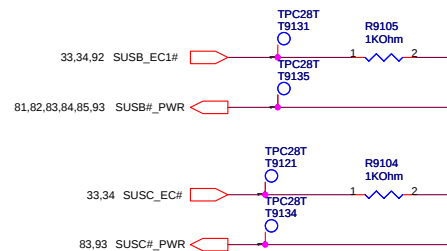
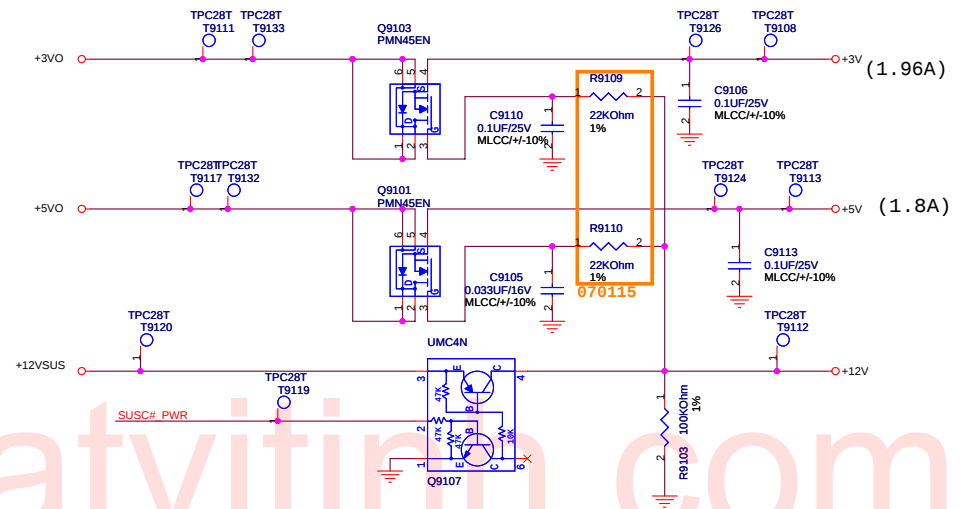
<Variant Name>

ASUS		Title :POWER_DETECT	
ASUSTeK COMPUTER INC. NB		Engineer: Ehong-Ping	
Size	Project Name		Rev
Custom	F9S		1.0
Date: Tuesday, February 27, 2007	Sheet	90	of 94

www.kythuativitinh.com

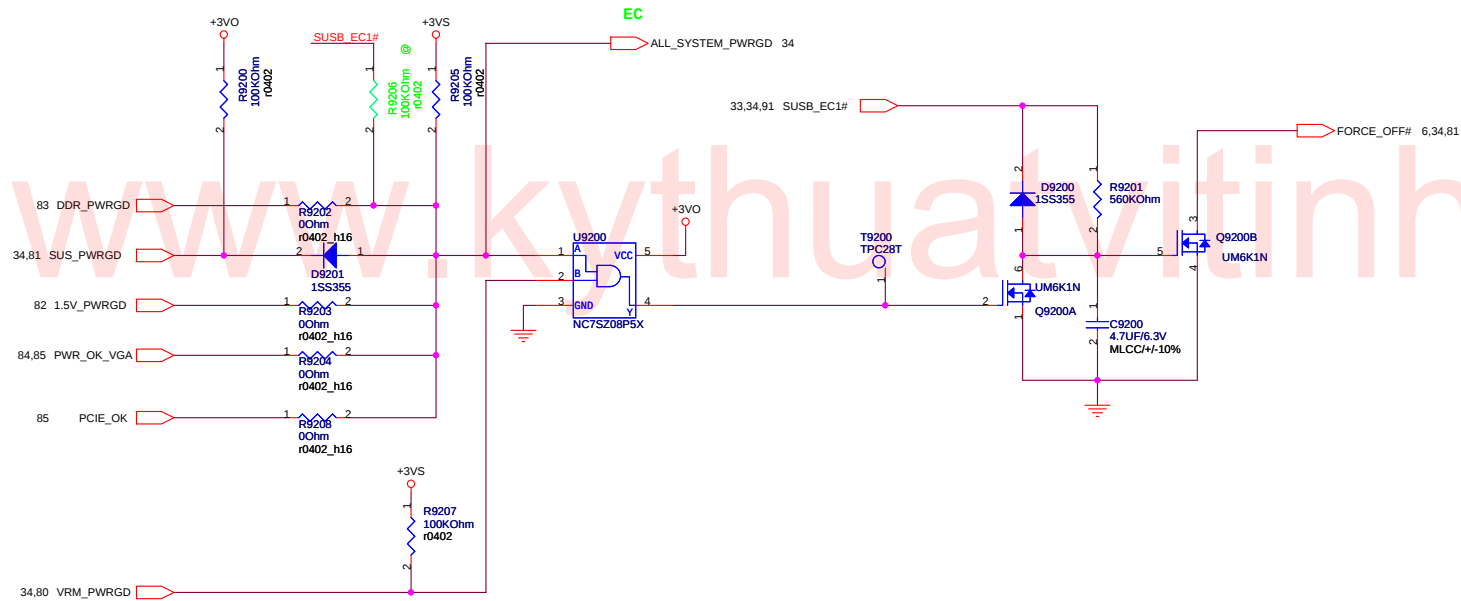


SUSC#_PWR POWER



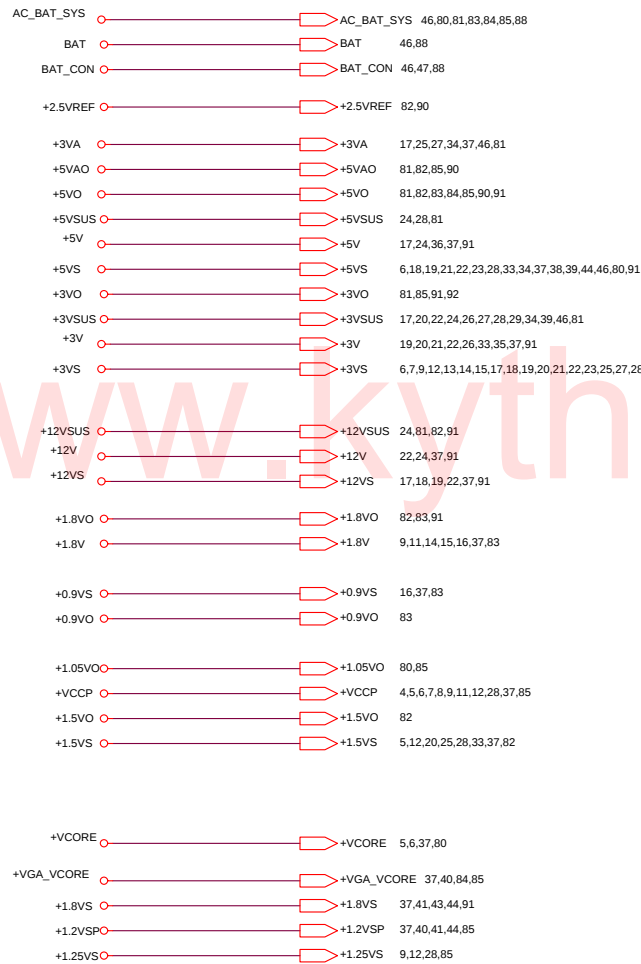
ASUS		Title : POWER_LOAD SWITCH	
ASUSTek COMPUTER INC. NB		Engineer: Engong-Ping	
Size	Project Name	F9S	Rev
Custom			1.0
Date: Tuesday, February 27, 2007		Sheet	91 of 94

POWER GOOD DETECTOR

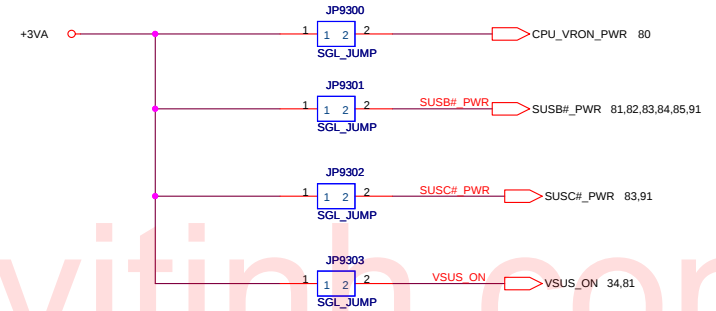


<Variant Name>

ASUS		Title :POWER_PROTECT	
ASUSTeK COMPUTER INC. NB		Engineer: Ehong-Ping	
Size	Project Name		Rev
Custom	F9S		1.0
Date: Tuesday, February 27, 2007		Sheet	92 of 94



FOR POWER TEST



<Variant Name>

ASUS		Title :POWER_SIGNAL	
ASUSTeK COMPUTER INC. NB		Engineer: Ehong-Ping	
Size	Project Name		Rev
Custom	F9S		1.0
Date: Tuesday, February 27, 2007		Sheet	93 of 94

AC_BAT_SYS

VSUS_ON

VSUS_ON

FORCE_OFF#

SUSB#_PWR

+5V0

SUSB#_PWR

DNI when use +1.05V

GVR_VR_EN

GVR_VID

+5V0

SUSB_PWR

PWR_CNTL_*

+5V0

SUSB#_PWR

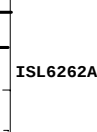
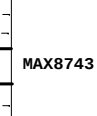
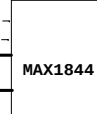
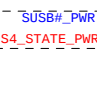
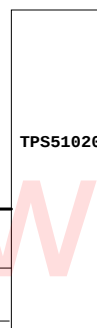
SLP_M_PWR

+5VS

CPU_VRON

VR_VID0~VR_VID6, H_DPRSTP#,
MCH_OK, PM_DPRSLPVR, PM_PSI#,
VCCSENSE, VSSSENSE, STP_CPU#,
PWR_MON

VRM_PWRGD, CLK_EN#



+12VSUS

+3V0

+5V0

+5VA0

+3VA0

+1.5V0

+1.8V0

+0.9V0

+VCCFX_CORE

GFX_PWRGD

+1.05V0

+1.25V0

PWR_OK_VGA

+VCORE

SUSC#_PWR

S4_STATE_PWR

SUSB#_PWR

SUSC#_PWR

S4_STATE_PWR

SUSB#_PWR

SUSC#_PWR

S4_STATE_PWR

SUSB#_PWR

SUSB#_PWR

SUSB#_PWR

DDR_PWRGD



<Variant Name>

ASUS			Title : POWER_FLOWCHART	
ASUSTek COMPUTER INC. NB			Engineer: Ehong-Ping	
Size	Project Name	Rev		
Custom		1.0		
Date: Thursday, February 15, 2007			Sheet 64 of 94	

F9S
Non-IAMT

Design rating

+12V

+12VS

+3VSUS

+3V

+3VS

+2.5VREF

+5VSUS

+5V

+5VS

+5VA

+3VA

+1.5VS

+1.8VS

+1.8V

+0.9VS

+VGA_VCORE

+VCCP

+1.25VS

+1.2VSP

+VCORE

(10mA)

(10mA)

(0.856A)

(1.96A)

(4.779A)

(10mA)

(0.01A)

(1.8A)

(4.051A)

(0.01A)

(0.01A)

(1.32A)

(4.19A)

(8.115A)

(1A)

(10.62A)

(9.85A)

(2.49A)

(1.75A)

(44A)

(7.55A)

(6A)

(1.5A)

(12.3A)

(2A)

(20.5A)

(5A)

(44A)