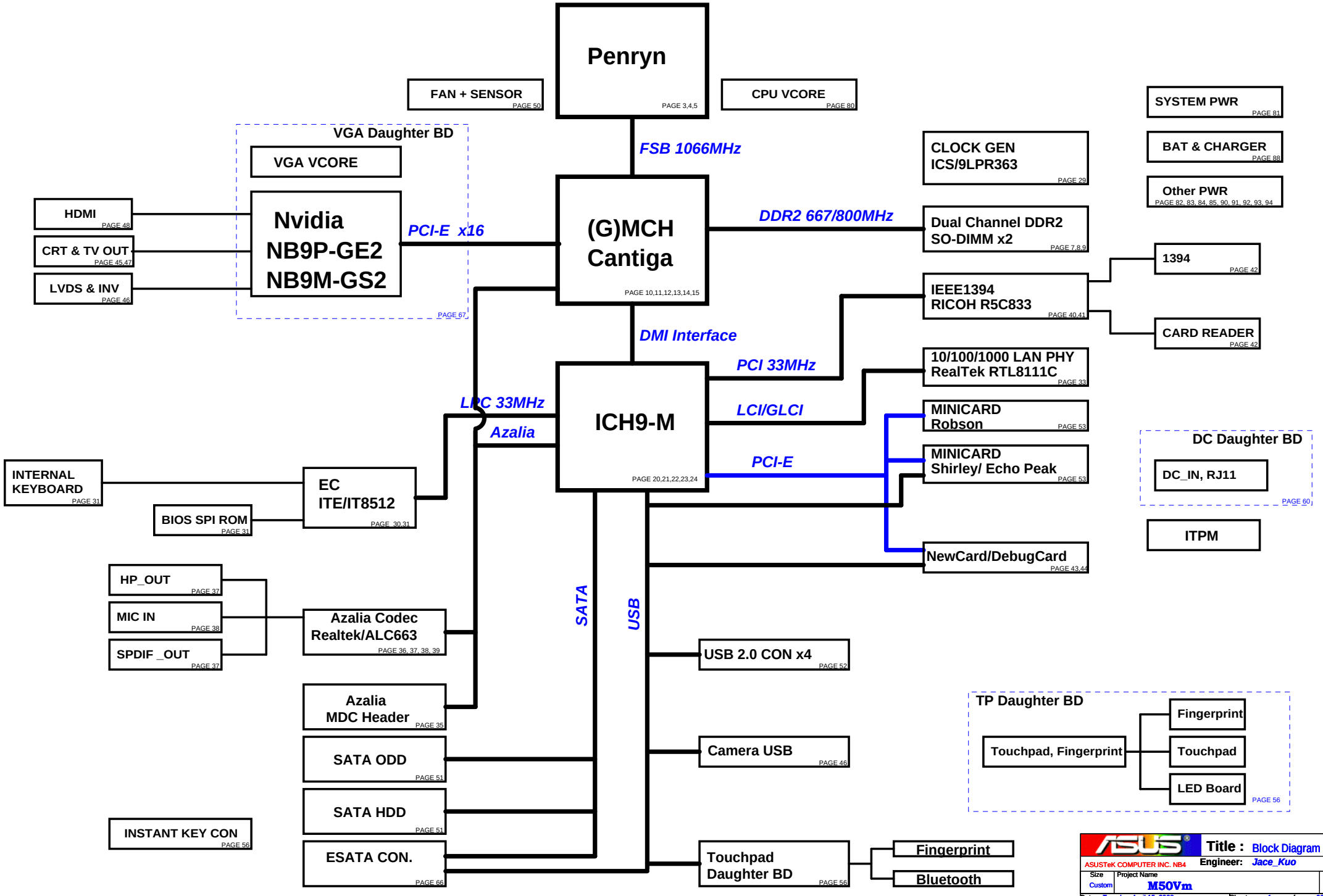
M50Vm Montevina Block Diagram



ASUSTeK COMPUTER INC. NB4	Title : Block Diagram		
	Engineer: Jace_Kuo		
Size: Custom	Project Name: M50Vm		Rev: 1.0
Date: Tuesday, April 15, 2008	Sheet 1 of 96		

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81	POWER_SYSTEM
82	POWER_I/O_1.5V & 1.05VM
83	POWER_I/O_DDR & VTT
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90	POWER_DETECT
91	POWER_LOAD SWITCH
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93	POWER_SIGNAL
94	POWER_FLOWCHART

ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PM_SYNC#	+3VS
GPIO 01	GPI	-	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	+3VS
GPIO 06	GPI	SIO_SMI#	+3VS
GPIO 07	GPI	WLAN_LED_ON	+3VS
GPIO 08	GPI	EXT_SMI#	+3VSUS
GPIO 09	GPI	LAN_WOL_EN	+3VSUS
GPIO 10	GPI	SUSPWR_ACK	+3VSUS
GPIO 11	GPI	EXT_SCI#	+3VSUS
GPIO 12	GPO		+3VSUS
GPIO 13	GPI		+3VSUS
GPIO 14	GPI	AC_PRESENT	+3VSUS
GPIO 15	Native	STP_PCI#	+3VSUS
GPIO 16	Native	PM_DPRSLPVR	+3VS
GPIO 17	GPI	WLAN_ON#	+3VS
GPIO 18	GPO	PD_RST#	+3VS
GPIO 19	GPI	-	+3VS
GPIO 20	GPO	-	+3VS
GPIO 21	GPI	-	+3VS
GPIO 22	GPI	-	+3VS
GPIO 23	Native	LPC_DRQ1#	+3VS
GPIO 24	GPO	PD_EN	+3VSUS
GPIO 25	Native	STP_CPU#	+3VSUS
GPIO 26	Native	PM_S4_STATE#	+3VSUS
GPIO 27	GPO	BT_ON	+3VSUS
GPIO 28	GPO	CB_SD#	+3VSUS
GPIO 29	Native	USB_OC#5	+3VSUS
GPIO 30	Native	USB_OC#6	+3VSUS
GPIO 31	Native	USB_OC#7	+3VSUS
GPIO 32	GPO	PM_CLKRUN#	+3VS
GPIO 33	GPO	-	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	-	+3VS
GPIO 36	GPI	EMAIL_LED#	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC#1	+3VSUS
GPIO 41	Native	USB_OC#2	+3VSUS
GPIO 42	Native	USB_OC#3	+3VSUS
GPIO 43	Native	USB_OC#4	+3VSUS
GPIO 44	Native	USB_OC8#	N/A
GPIO 45	Native	USB_OC9#	N/A
GPIO 46	Native	USB_OC10#	N/A
GPIO 47	Native	USB_OC11#	N/A
GPIO 48	GPI	-	+3VS
GPIO 49	GPO	HDTV_EN#	**+3VS**
GPIO 50	Native	PCI_REQ#1	+3VS
GPIO 51	Native		+3VS
GPIO 52	Native	PCI_REQ#2	+3VS
GPIO 53	Native		+3VS
GPIO 54	Native	PCI_REQ#3	+3VS
GPIO 55	Native		+3VS
GPIO 56			+3VSUS
GPIO 57	GPI		+3VSUS
GPIO 58	GPI	SPI_CS#1	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	Native		+3VSUS

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED_UP#	
GPA1	GPO	CHG_LED_UP#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	-	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FAN0_PWM	
GPA6	GPO	BAT1_CNT1#	
GPA7	GPO	BAT2_CNT1#	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	GPI	DISTP#	
GPB3	ALT	SMB0_CLK	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	GPI	MARATHON#	
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	ALT	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	GPO	3G_ON#	
GPD0	GPI	PWRLIMIT#	
GPD1	ALT	PM_S4_STATE#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	ALT	FAN0_TACH	
GPD7	GPI	COLOREN#	
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC1#	
GPE3	GPO	CPU_VRON	
GPE4	ALT	PWR_SW#	
GPE5	ALT	BAT2_IN_OC#	
GPE6	GPI	LID_SW#	
GPE7	GPO	PM_THERM#	
GPF0	GPI	BLUETOOTH#	
GPF1	GPI	WIRELESS#	
GPF2	ALT	PS2_CLK_5S_PD	
GPF3	ALT	PS2_DATA_5S_PD	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	PS_SHDN#	
GPG0	GPI	INSTANT_ON#	
GPG1	ALT	PM_SUSB#	
GPG2	GPO	BAT1_CNT2#	
-	-	-	
-	-	-	

EC GPIO	Use As	Signal Name	Power
-	-	-	
GPG6	GPO	BAT2_CNT2#	
-	-	-	
GPH0	OD	PM_CLKRUN#	
GPH1	ALT	-	
GPH2	ALT	-	
GPH3	GPO	BAT_LEARN	
GPH4	GPO	-	
GPH5	GPO	NUM_LED	
GPH6	GPO	CAP_LED	
-	-	-	
GPI0	GPI	-	
GPI1	GPI	SUS_PWRGD	
GPI2	GPI	ALL_SYSTEM_PWRGD	
GPI3	GPI	VRM_PWRGD	
GPI4	GPI	PWR_MON	
GPI5	GPI	PD_DET#	
GPI6	GPI	KB_ID0	
GPI7	GPI	KB_ID1	
GPJ0	GPO	EC_CLK_EN	
GPJ1	GPO	PM_PWROK	
GPJ2	GPI	UNDOCK#_PD	
GPJ3	-	-	
GPJ4	GPO	BL_DA	
GPJ5	GPO	FAN_DA	
GPK0	GPI	PM_SLP_M#	
GPK1	GPI	SUSPWR_ACK	
GPK2	GPI	PM_SUSC#	
GPK3	GPI	+3VM_PG	
GPK4	GPI	+1.05VM_+3VMCLK_PG	
GPK5	GPI	LAN_WOL_EN	
GPL0	GPI	AC_APR_UC#	
GPL1	GPI	-	
GPL2	GPO	-	
GPL3	GPO	LAN_RST#	
GPL4	GPO	CL_PWROK	
GPL5	GPO	EC_WLAN_PWR	
GPL6	GPO	SLP_M_ON	
GPL7	GPO	S4_STATE_ON	
GPK6	GPO	AC_PRESENT	
GPK7	GPI	PS_CPPE#	

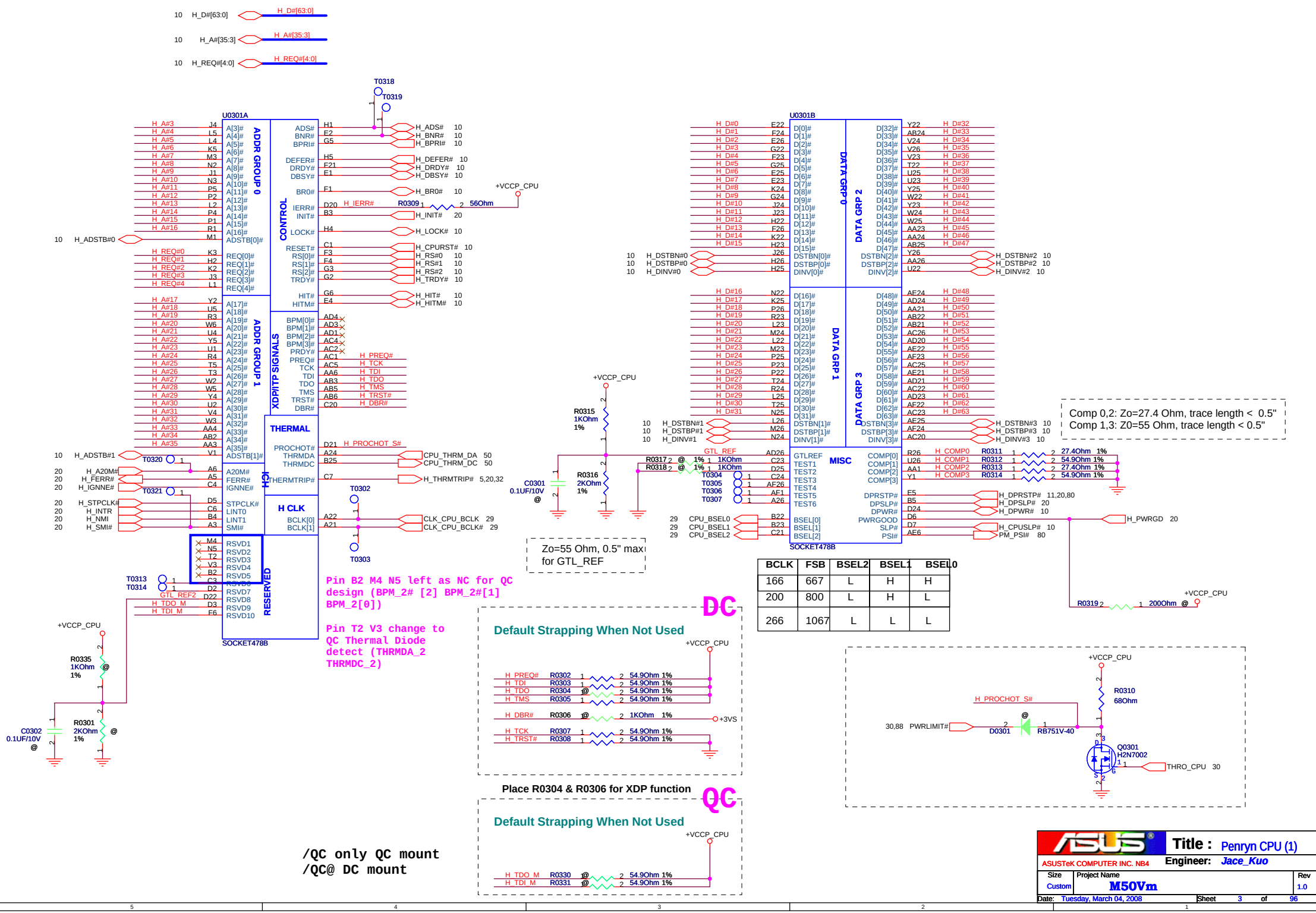
ASUSTeK COMPUTER INC. NB6

Title : Schematic Information

Engineer: Raphael_Chen

Size	Project Name	Rev
Custom	M50Vm	1.1

Date: Wednesday, February 13, 2008 Sheet 2 of 96



BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L

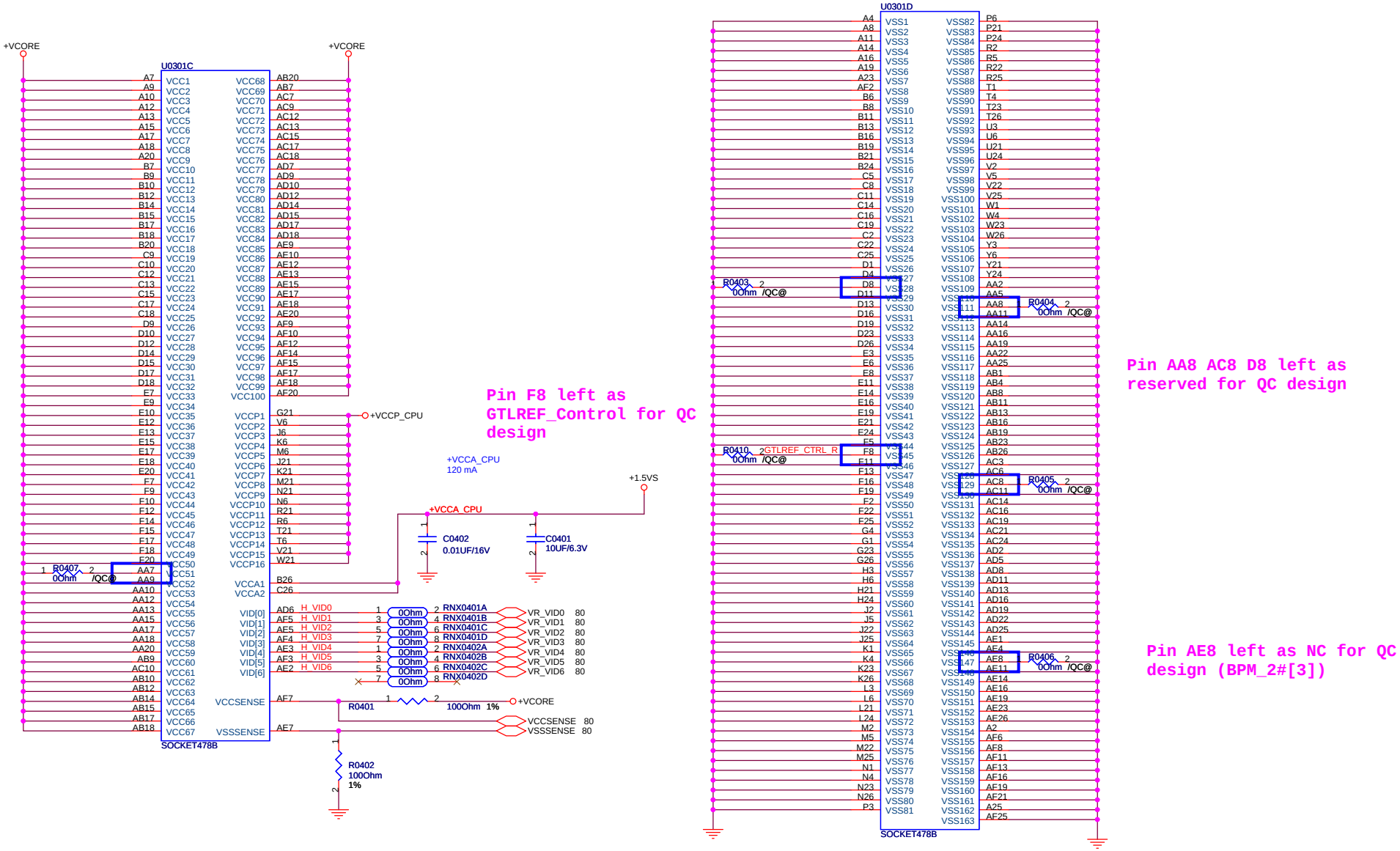
ASUSTeK COMPUTER INC. NB4

Title : Penryn CPU (1)

Engineer: Jace_Kuo

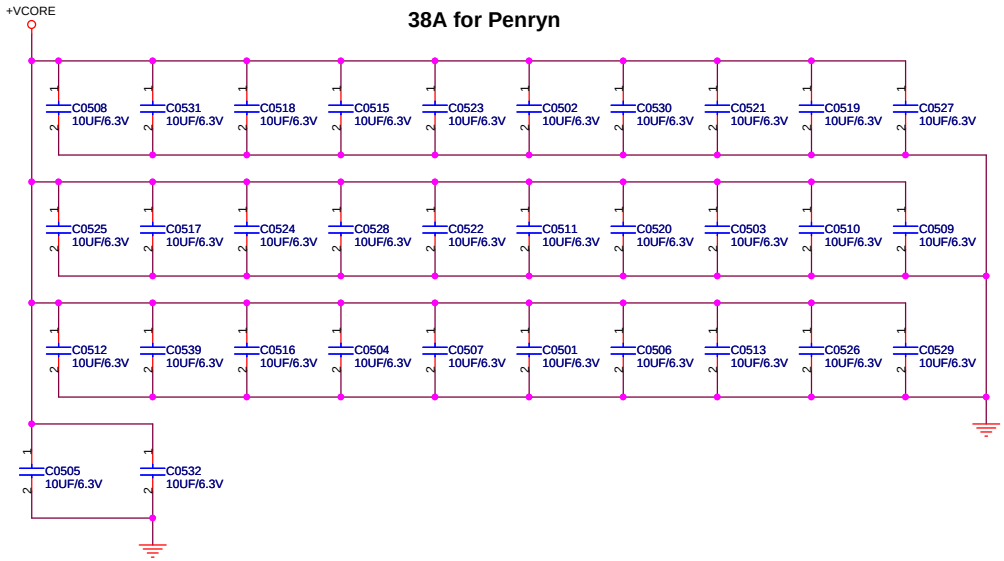
Size	Project Name	Rev
Custom	M50Vm	1.0

Date: Tuesday, March 04, 2008 Sheet 3 of 96

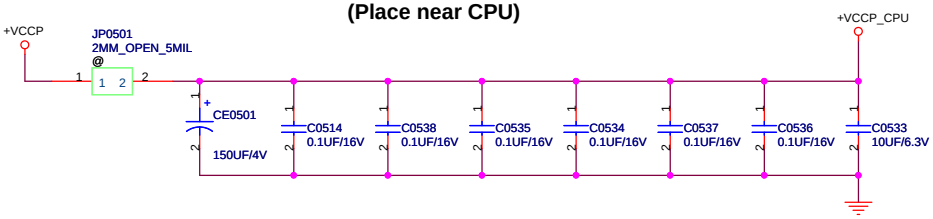


ASUSTeK COMPUTER INC. NB4	Title : Penryn CPU (2)	
	Engineer: Jace_Kuo	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 4 of 96	

38A for Penryn



+VCCP Decoupling Capacitor (Place near CPU)

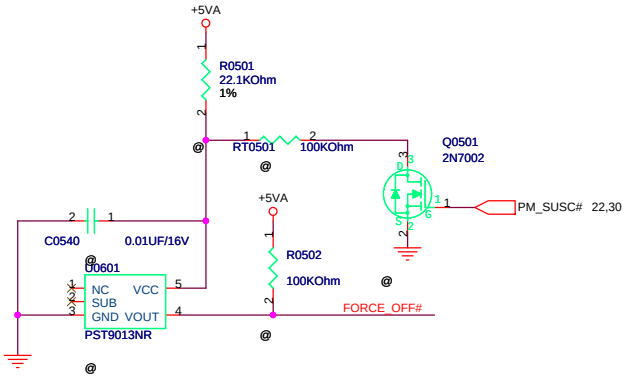


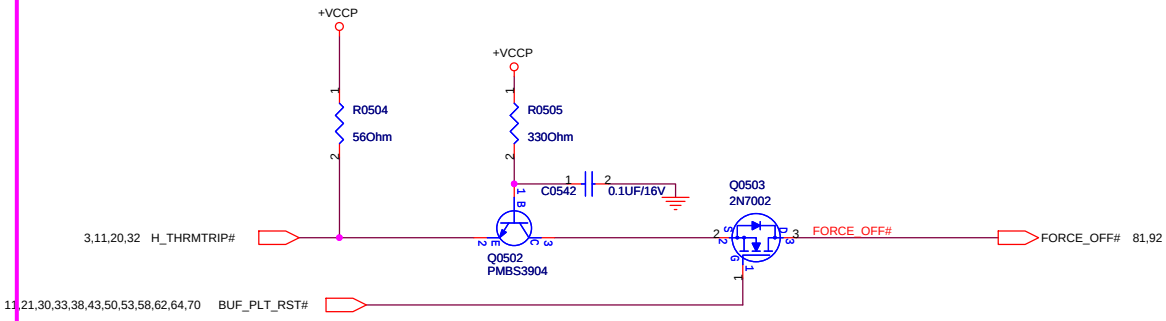
Decoupling guide from Intel

VCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*F3S: 10UF *16*
*A7S: 10UF *10 ....11/17*
V1V: ?
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*F3S: 100UF *1, 0.1UF *4*
V1V: ?

? DEGREE C
THERMAL PROTECTION
PLACE UNDER CPU

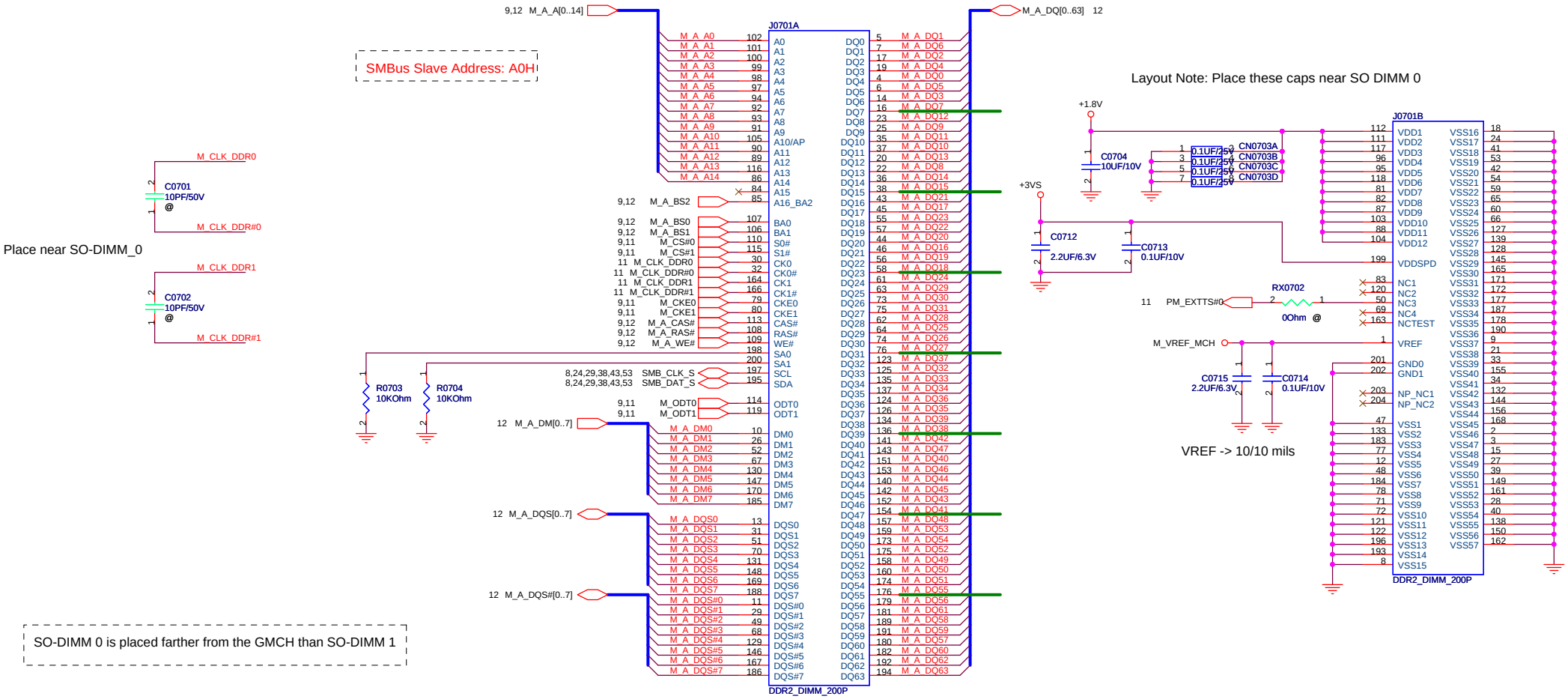




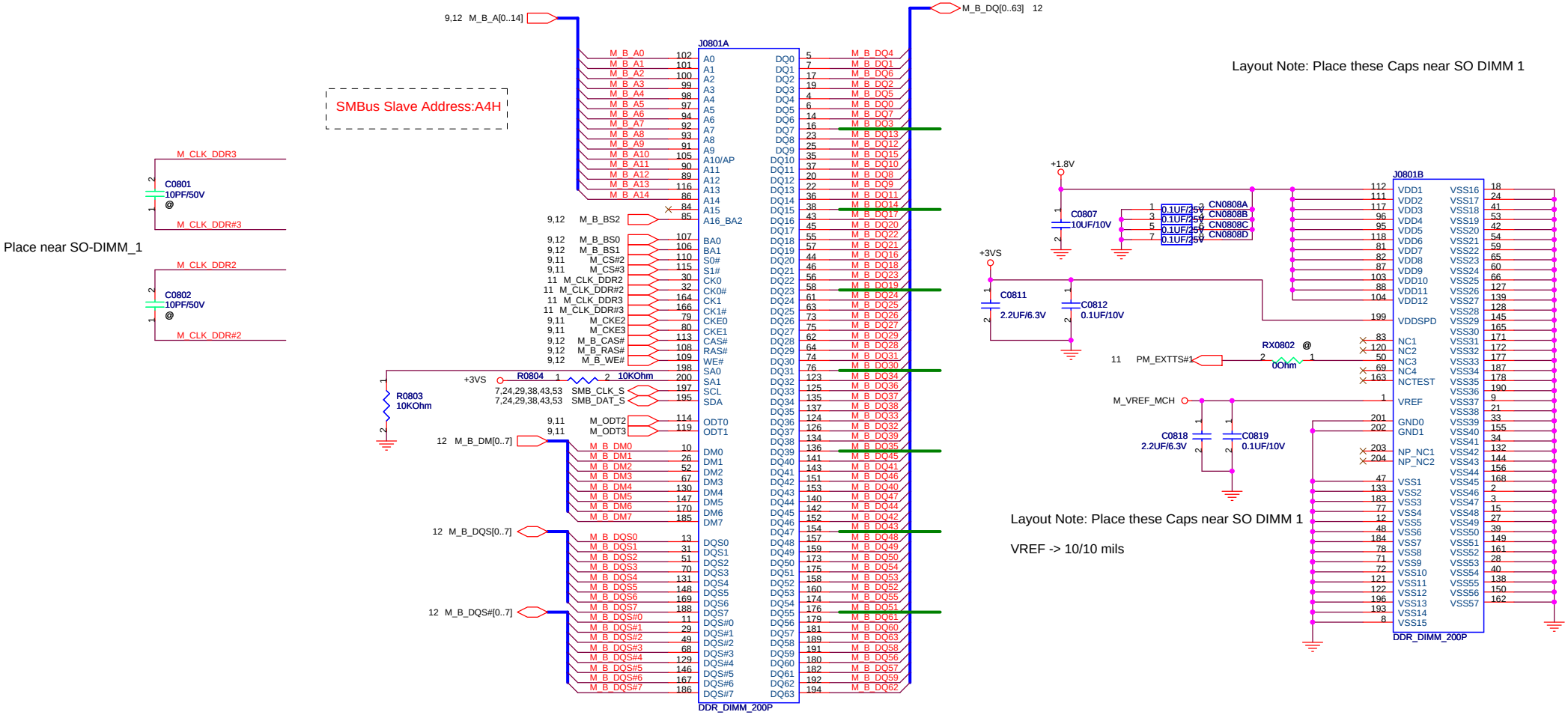
Thermal Trip signal (From CPU to ICH-9M and sequence)

ASUSTeK COMPUTER INC. NB4	Title : CPU CAPS		
	Engineer: Jace_Kuo		
Size: Custom	Project Name: M50Vm		Rev: 1.0
Date: Friday, March 07, 2008	Sheet 5 of 96		

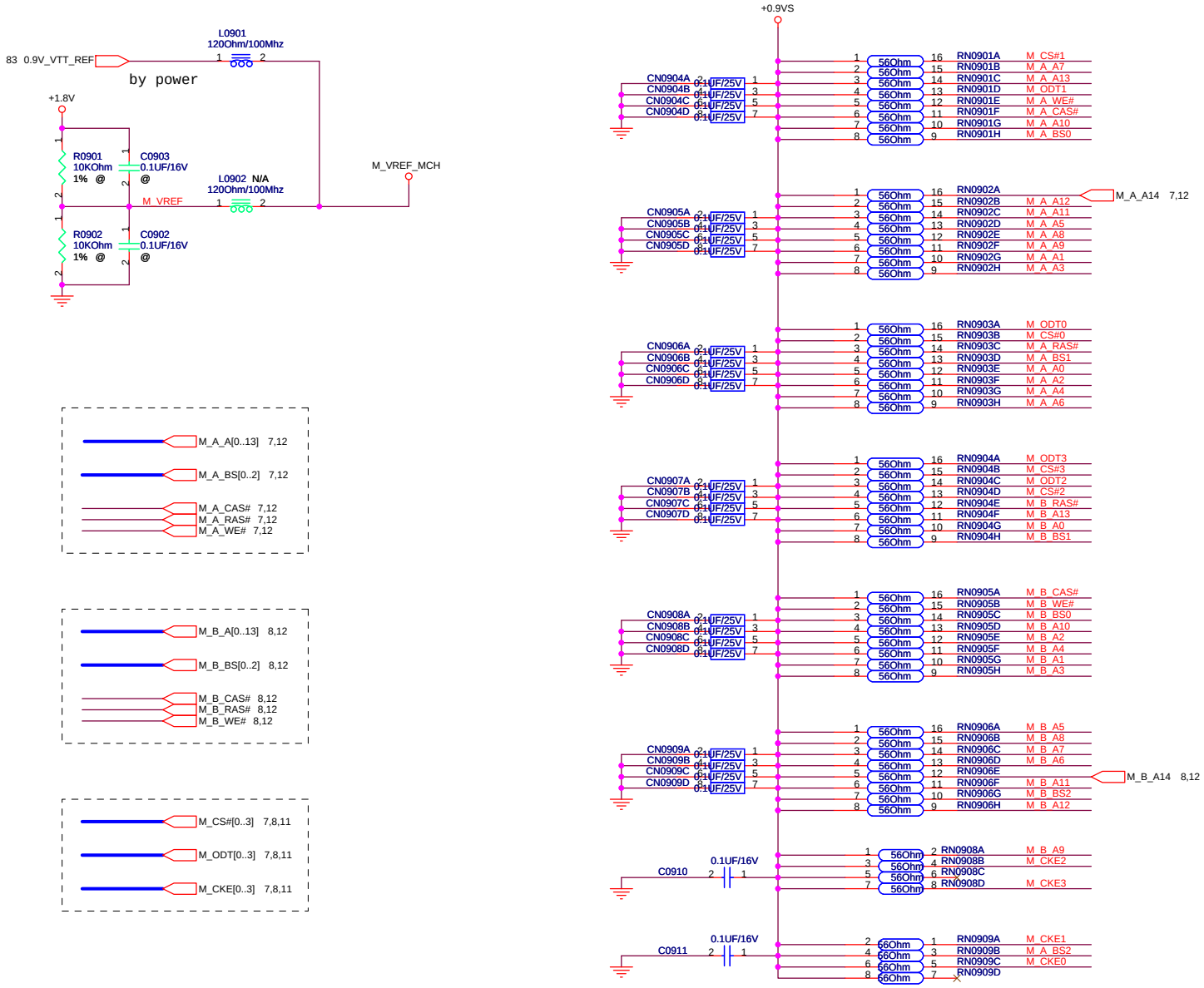
ASUSTeK COMPUTER INC. NB6	Title : Engineer:	
Size: A	Project Name	Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 6 of 96	



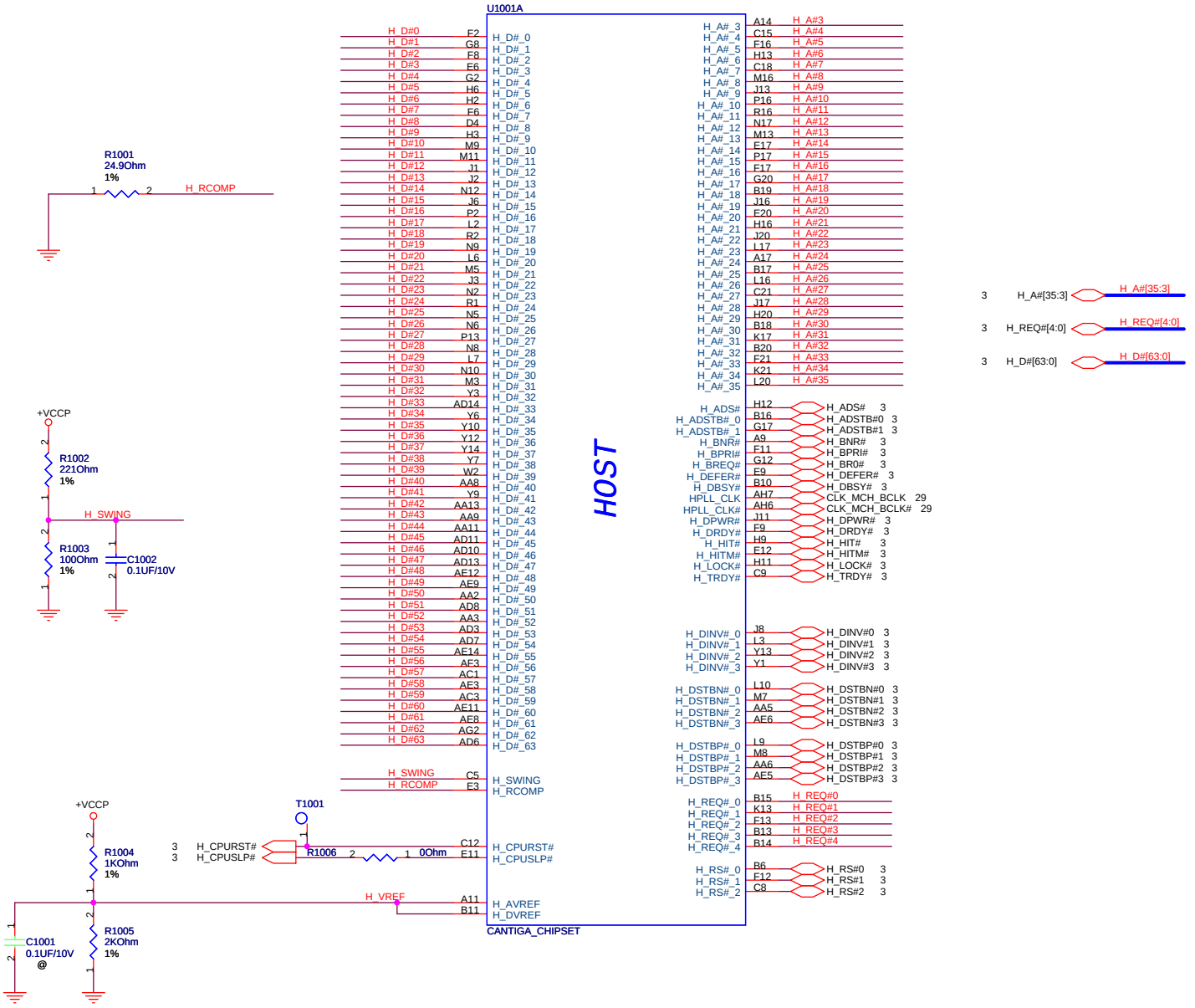
ASUSTeK COMPUTER INC. NB4	Title : DDR2 SO-DIMM_0	
	Engineer: Jace_Kuo	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 7 of 96	



ASUSTeK COMPUTER INC. NB4	Title : DDR2 SO-DIMM_1	
	Engineer: Jace_Kuo	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 8 of 96	



ASUSTeK COMPUTER INC. NB4	Title : DDR2 termination	
	Engineer: Jace_Kuo	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Tuesday, March 04, 2008	Sheet 9 of 96	



Cap 0.1uF within 500 mils from GMCH

ASUSTeK COMPUTER INC. NB4	Title : Cantiga - CPU (1)	
	Engineer: Michael_Wang	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 10 of 96	

LVDS signals
PM:NC
CRT signals
PM:GND
OTH Hsync and Vsync NC

U1001B

U1001C

R1.1 SWAP LVDS Chanel A B

change CRT part-number to 0 Ohm
10G212000004010
R1112

R1112: 0 ohm for PM

change CRT part-number to 0 Ohm 10G212000004010 R1109 R1120 R1111

FOLLOW INTEL Design

To EC(THERM.)

PM_NC_AUD_side

PM: 0Ohm R1111 150Ohm R1109 150Ohm
GM disable: 0Ohm
GM: 150Ohm
R1120 150Ohm

CANTIGA_CHIPSET

CANTIGA_CHIPSET

Title : Cantiga-DDR2/PEG(2)
ASUSTeK COMPUTER INC. NB4
Engineer: Michael_Wang
Size: Custom
Project Name: M50Vm
Rev: 1.0
Date: Friday, March 07, 2008
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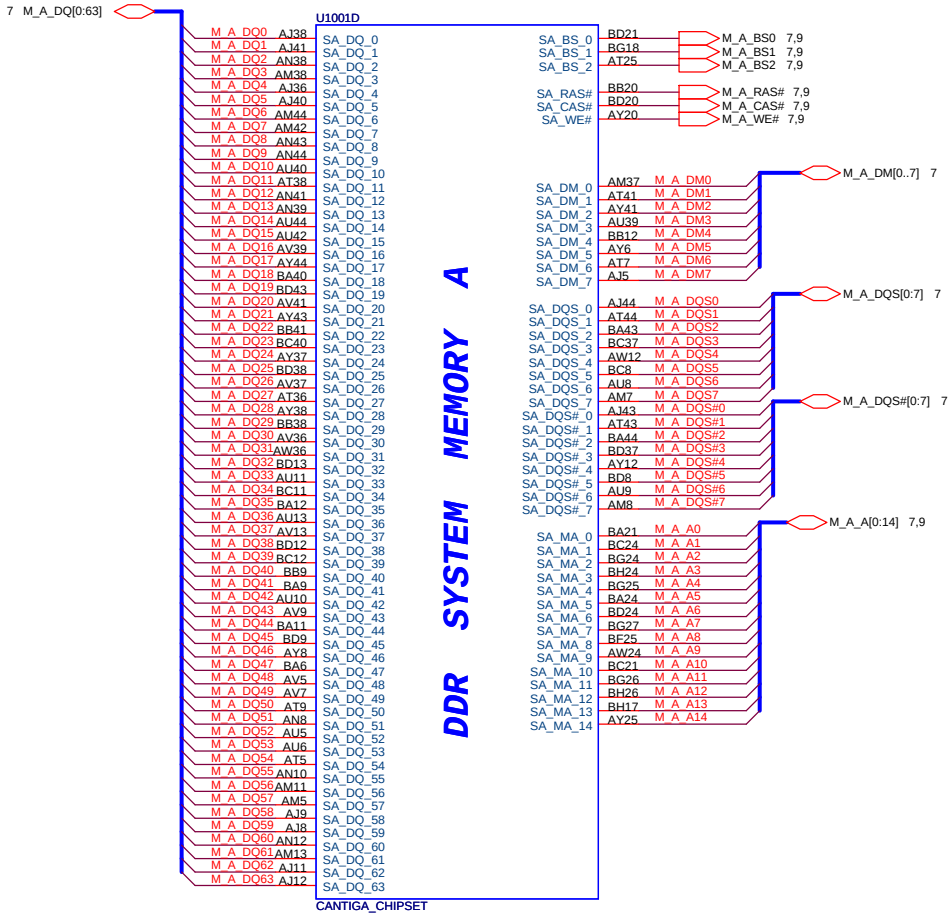
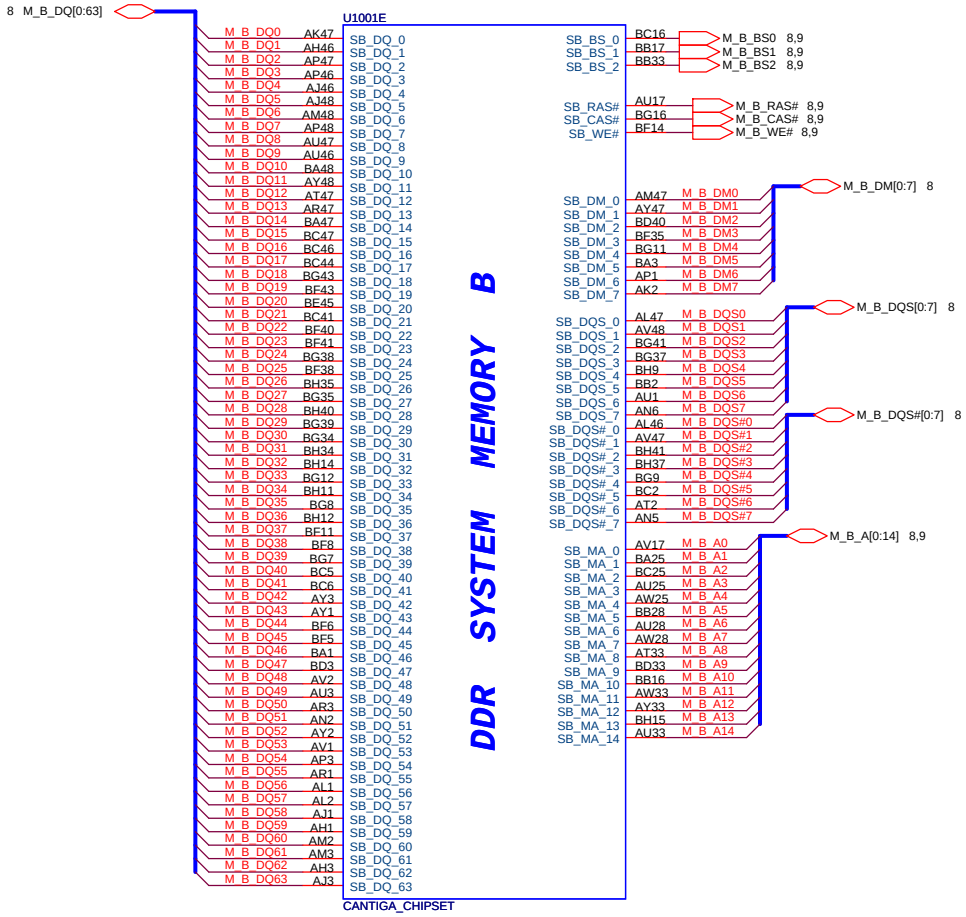
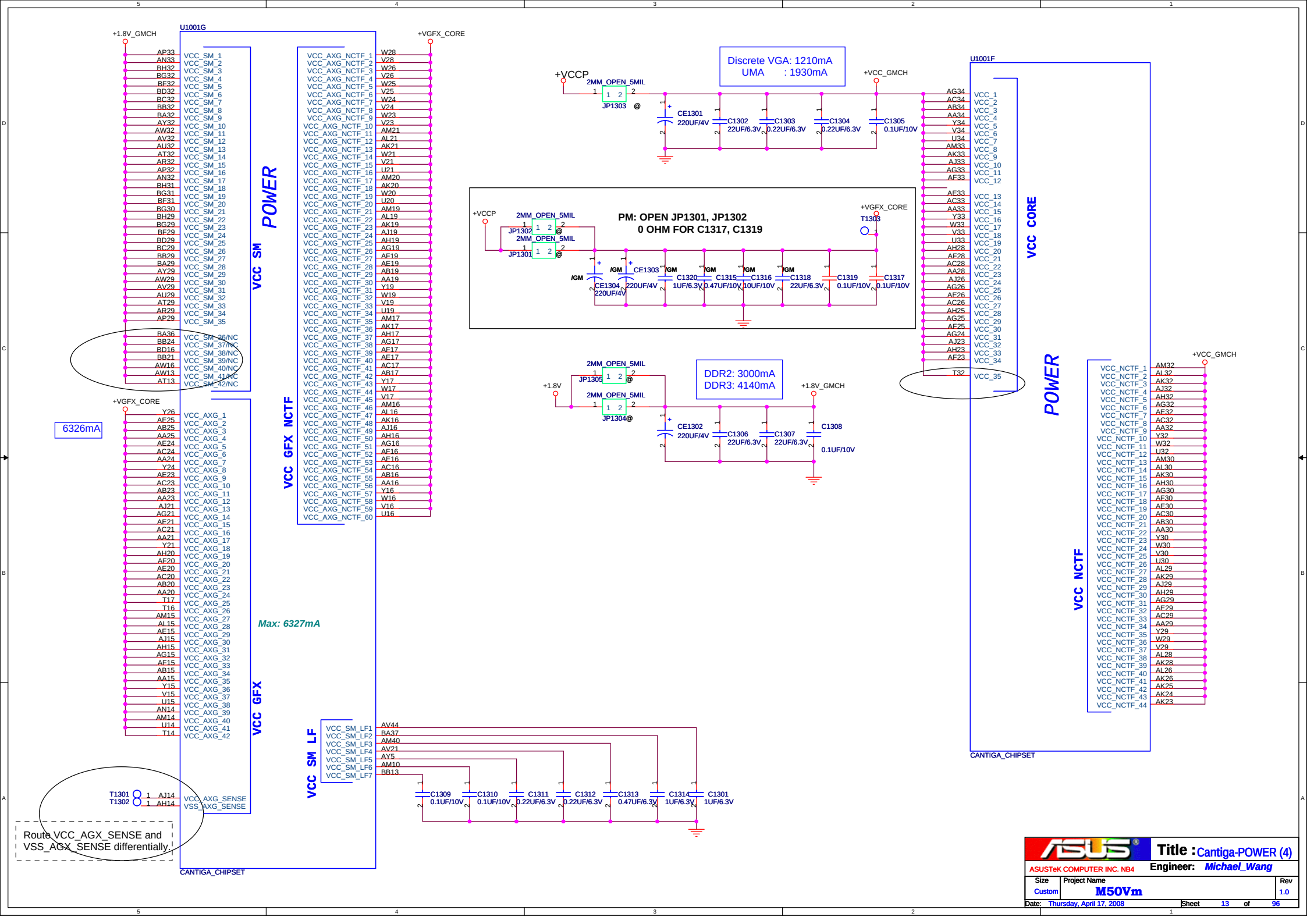
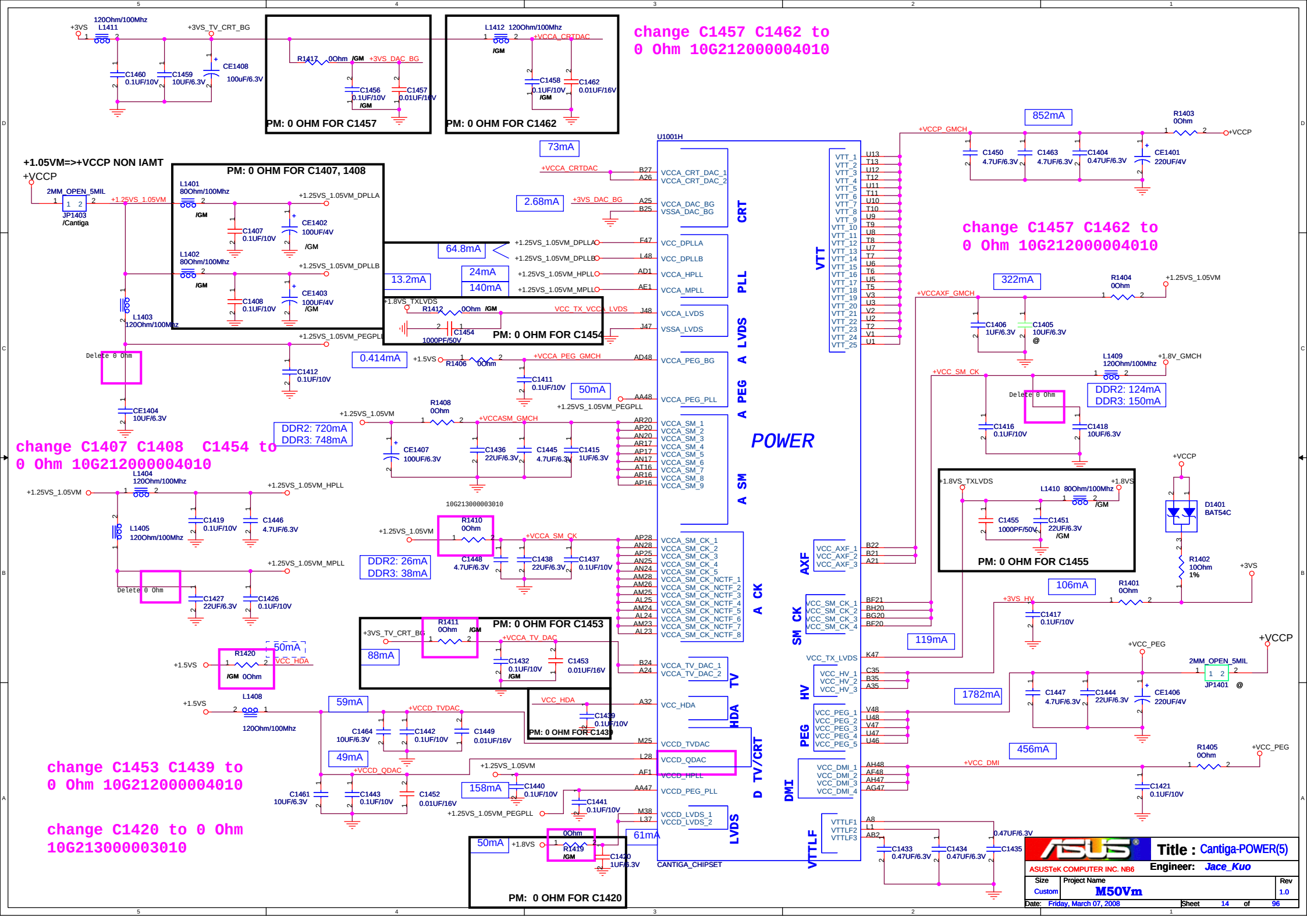




ASUSTeK COMPUTER INC. NB4	Title : Cantiga-DDR2 bus (3)	
	Engineer: Michael_Wang	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 12 of 96	



ASUSTeK COMPUTER INC. NB4	Title : Cantiga-POWER (4)	
	Engineer: Michael_Wang	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Thursday, April 17, 2008	Sheet 13 of 96	


change C1457 C1462 to
0 Ohm 10G212000004010
PM: 0 OHM FOR C1457
PM: 0 OHM FOR C1462
+1.05VM=>+VCCP NON IAMT
+VCCP
PM: 0 OHM FOR C1407, 1408
PM: 0 OHM FOR C1454
change C1407 C1408 C1454 to
0 Ohm 10G212000004010
PM: 0 OHM FOR C1453
PM: 0 OHM FOR C1439
change C1453 C1439 to
0 Ohm 10G212000004010
change C1420 to 0 Ohm
10G213000003010
PM: 0 OHM FOR C1420
U1001H
CANTIGA_CHIPSET
POWER
CRT
PLL
LVDS
PEG
SM
CK
TV
HDA
D TV/CRT
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
852mA
322mA
change C1457 C1462 to
0 Ohm 10G212000004010
DDR2: 124mA
DDR3: 150mA
PM: 0 OHM FOR C1455
106mA
119mA
1782mA
456mA
73mA
2.68mA
64.8mA
13.2mA
24mA
140mA
0.414mA
50mA
DDR2: 720mA
DDR3: 748mA
DDR2: 26mA
DDR3: 38mA
88mA
59mA
49mA
158mA
61mA
50mA
Title : Cantiga-POWER(5)
ASUSTeK COMPUTER INC. NB6
Engineer: Jace_Kuo
Size: Custom
Project Name: M50Vm
Rev: 1.0
Date: Friday, March 07, 2008
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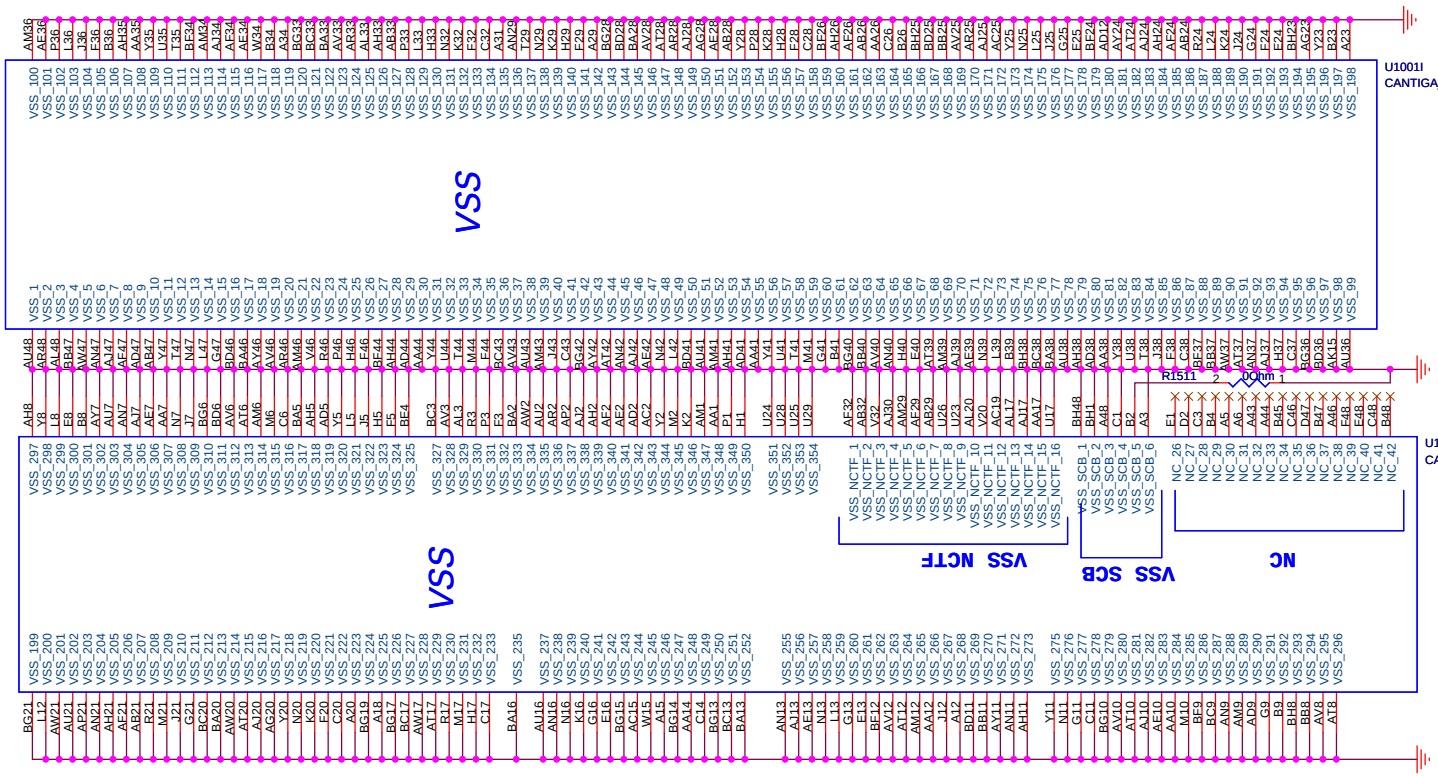


11 MCH_CFG_5

R1505
2.21KOhm
@

CFG5 : DMI STRAP

HIGH = DMI X 4 (Default)

LOW = DMI X 2

11 MCH_CFG_6

R1510
2.21KOhm
@

CFG6 : Integrated TPM Host Interface

HIGH = iTPM disable (Default)

LOW = iTPM enable

11 MCH_CFG_7

R1507
2.21KOhm
@

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite

HIGH = With confidentiality (Default)

LOW = Without confidentiality

11 MCH_CFG_9

R1508
2.21KOhm
@

CFG9 : PCIE GRAPHIC LANE

HIGH = Normal Operation (Default)

LOW = Reverse Lanes

11 MCH_CFG_16

R1503
2.21KOhm
@

CFG16 : FSB Dynamic ODT

HIGH = Ensable (Default)

LOW = Disable

11 MCH_CFG_10

R1504
2.21KOhm
@

CFG10 : PCIe Loopback

HIGH = Disable (Default)

LOW = Enable

11 MCH_CFG_12

R1509
2.21KOhm
@

CFG [13:12] : XOR/ALL-Z

00 = Reserved

01= XOR Mode Enabled

10= All-Z Mode Enabled

11= Normal Operation (Default)

11 MCH_CFG_13

R1506
2.21KOhm
@

+3VS

R1501
4.02KOHM
@

11 MCH_CFG_19

CFG19 : DMI Lane Reversal

LOW = NORMAL (default)

HIGH = Reverse Lanes

+3VS

R1502
4.02KOHM
@

11 MCH_CFG_20

CFG20 : SDVO/PCIE CONCURRENT MODE

LOW = ONLY SDVO or PCIE is Operational (Default)

HIGH = SDVO and PCIE are operating simultaneously via the PEG port

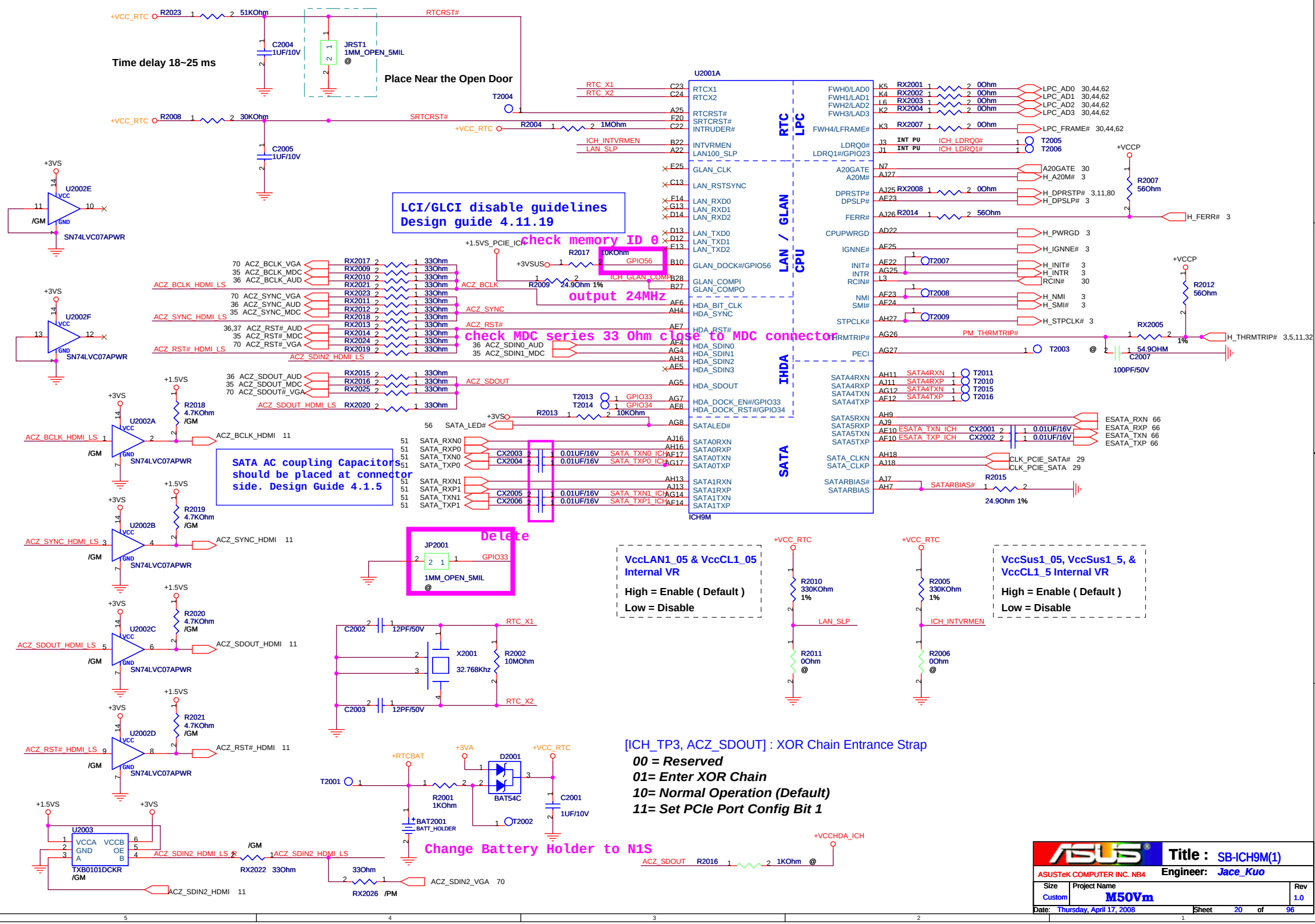
ASUSTeK COMPUTER INC. NB4	Title : Cantiga-GND	
	Engineer: Michael_Wang	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Tuesday, March 04, 2008	Sheet 15 of 96	

Title :	
Engineer:	
Size: A	Project Name:
Rev: 1.0	
Date: Wednesday, February 13, 2008	Sheet 16 of 96

ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 17 of 96	

Title :	
Engineer:	
Size: A	Project Name
Rev: 1.0	
Date: Wednesday, February 13, 2008	Sheet 18 of 96

Title :	
Engineer:	
Size: A	Project Name
Rev: 1.0	
Date: Wednesday, February 13, 2008	Sheet 19 of 96


Time delay 18~25 ms
Place Near the Open Door
JRST1
1MM_OPEN_5MIL
@
LCI/GLCI disable guidelines
Design guide 4.11.19
check memory ID 0
output 24MHz
check MDC series 33 Ohm close to MDC connector
SATA AC coupling Capacitors should be placed at connector side. Design Guide 4.1.5
Delete
JP2001
1MM_OPEN_5MIL
VccLAN1_05 & VccCL1_05 Internal VR
High = Enable (Default)
Low = Disable
VccSus1_05, VccSus1_5, & VccCL1_5 Internal VR
High = Enable (Default)
Low = Disable
[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1
Change Battery Holder to N1S
U2001A
ICH9M
RTC
LPC
GLAN
LAN / GLAN
CPU
IHDA
SATA
SN74LVC07APWR
TXB0101DCKR
BAT54C
Title : SB-ICH9M(1)
ASUSTeK COMPUTER INC. NB4
Engineer: Jace_Kuo
Size: Custom
Project Name: M50Vm
Rev: 1.0
Date: Thursday, April 17, 2008
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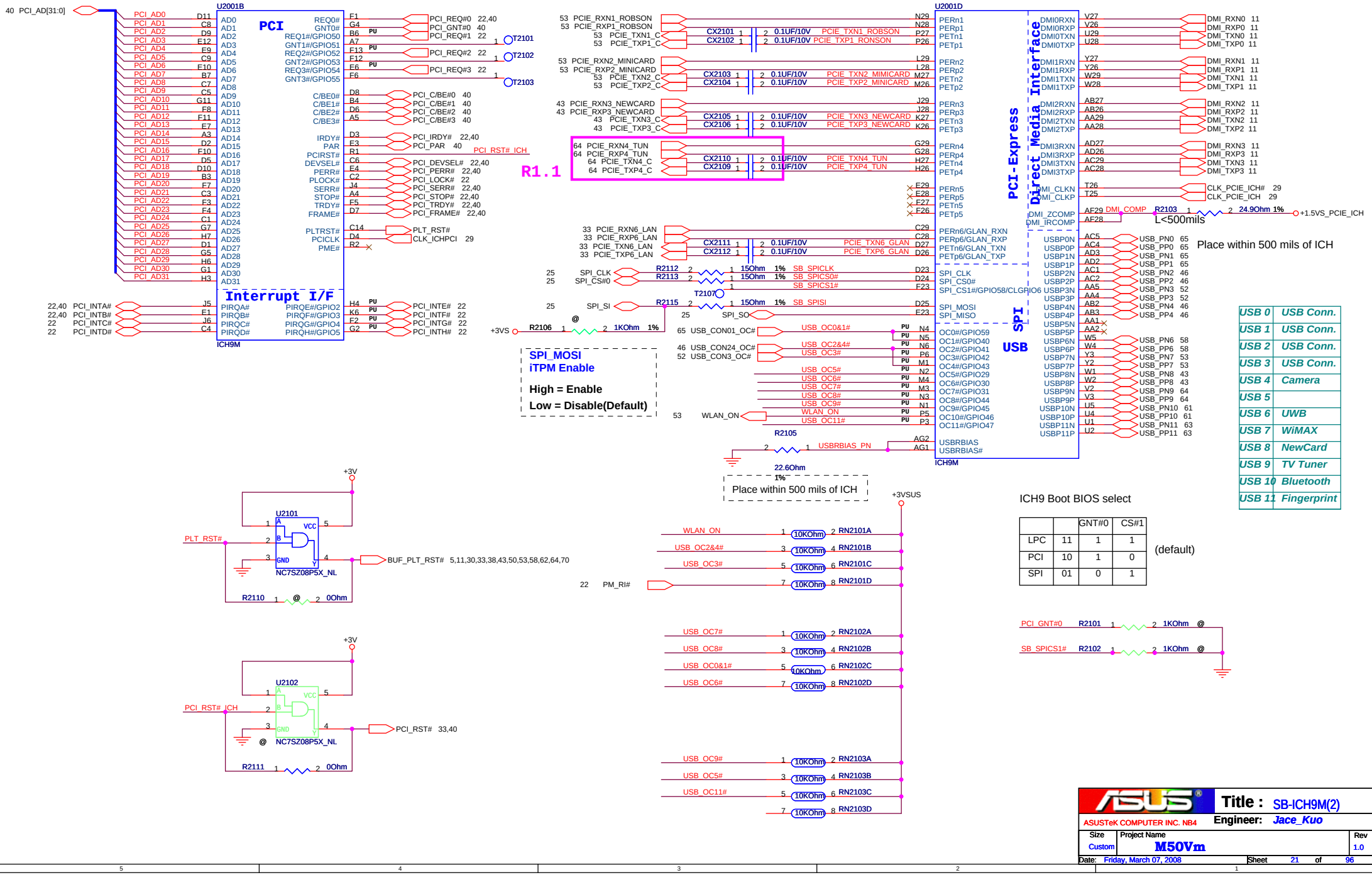
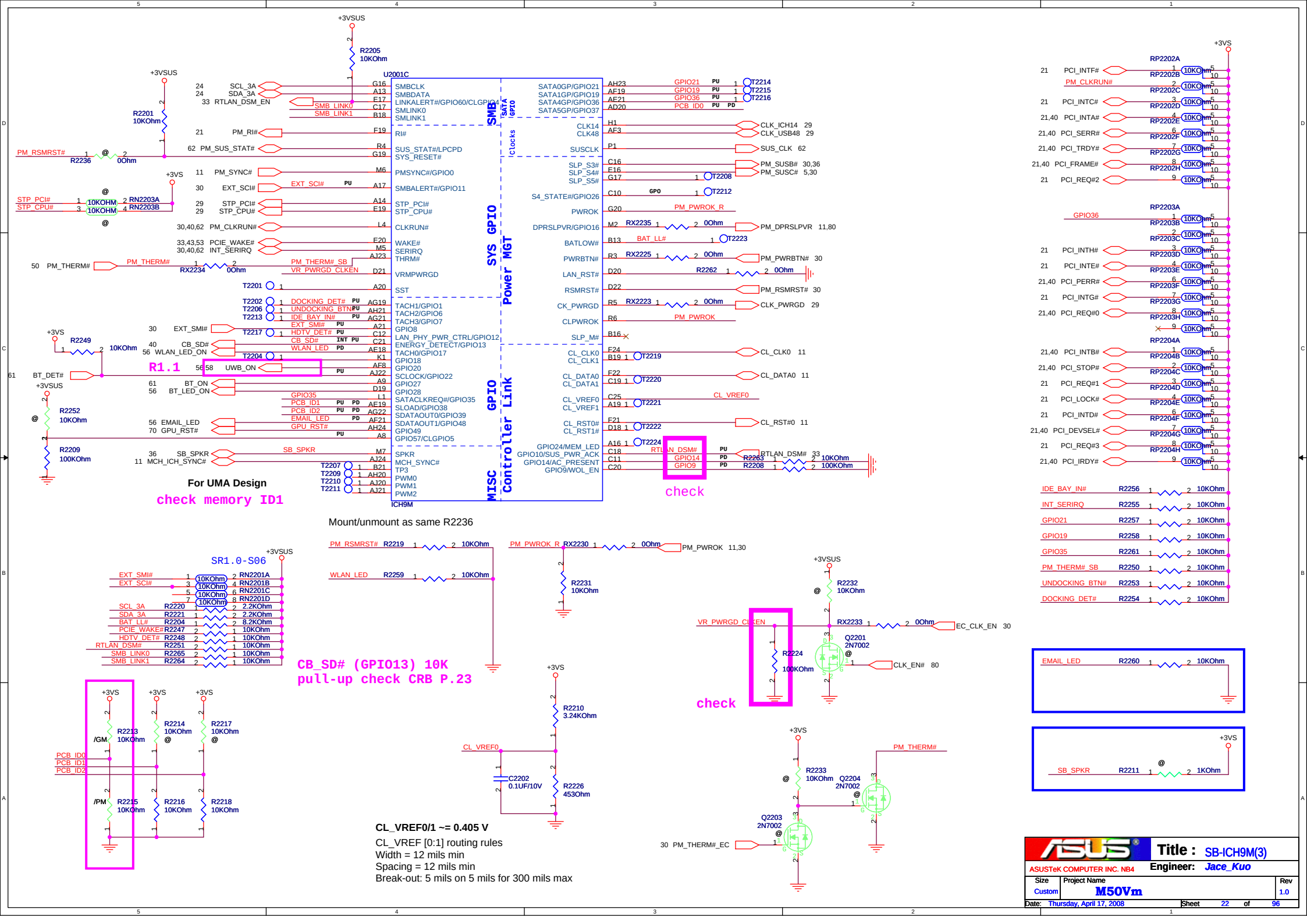


USB 0	USB Conn.
USB 1	USB Conn.
USB 2	USB Conn.
USB 3	USB Conn.
USB 4	Camera
USB 5	
USB 6	UWB
USB 7	WiMAX
USB 8	NewCard
USB 9	TV Tuner
USB 10	Bluetooth
USB 11	Fingerprint

		GNT#0	CS#1
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1


U2001C
ICH9M
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SATA GPIO
Clocks
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
SST
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
R1.1
For UMA Design
check memory ID1
Mount/unmount as same R2236
check
SR1.0-S06
CB_SD# (GPIO13) 10K
pull-up check CRB P.23
check
CL_VREF0/1 ~= 0.405 V
CL_VREF [0:1] routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out: 5 mils on 5 mils for 300 mils max
Title : SB-ICH9M(3)
ASUSTeK COMPUTER INC. NB4
Engineer: Jace_Kuo
Size: Custom
Project Name: M50Vm
Rev: 1.0
Date: Thursday, April 17, 2008
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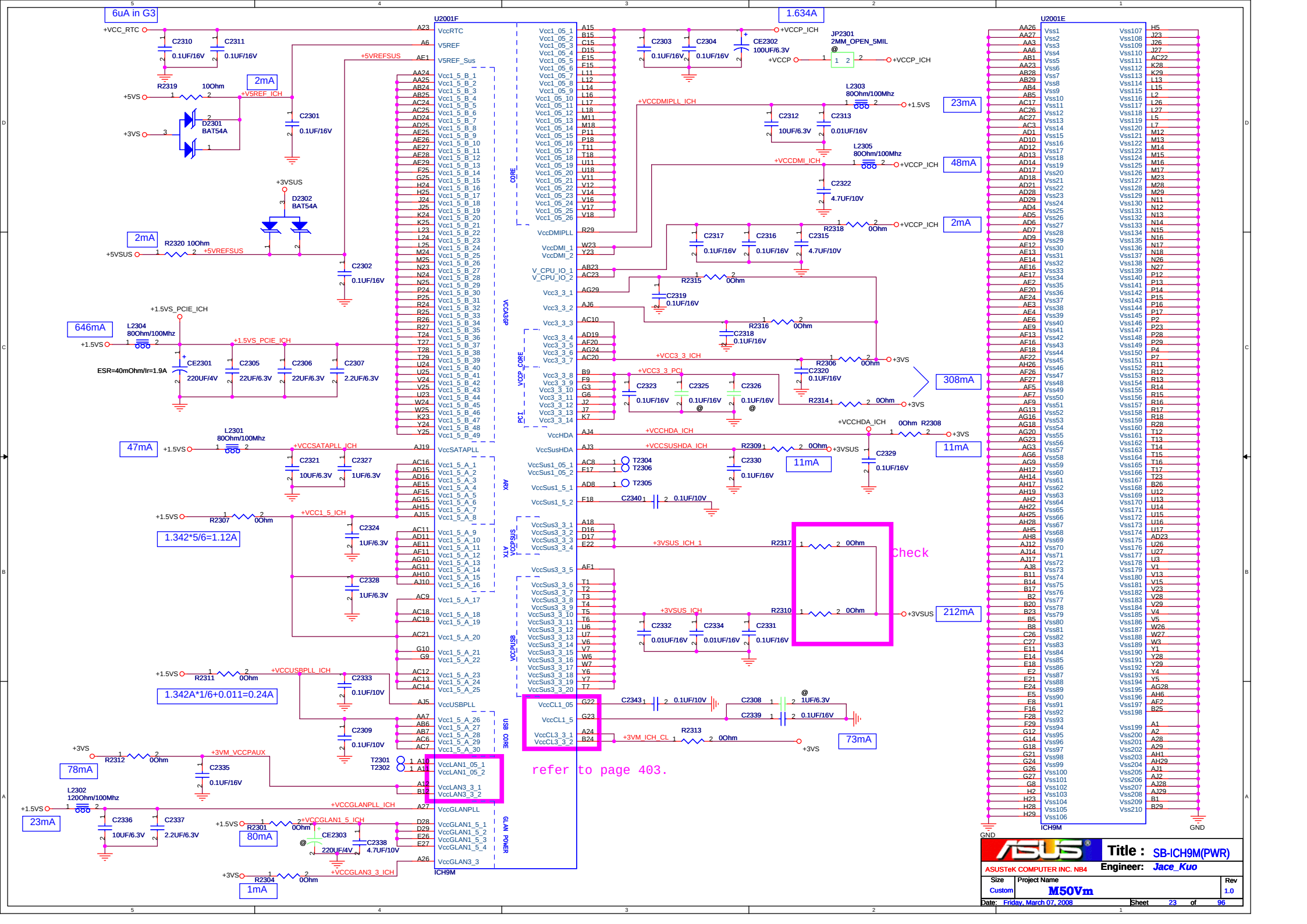
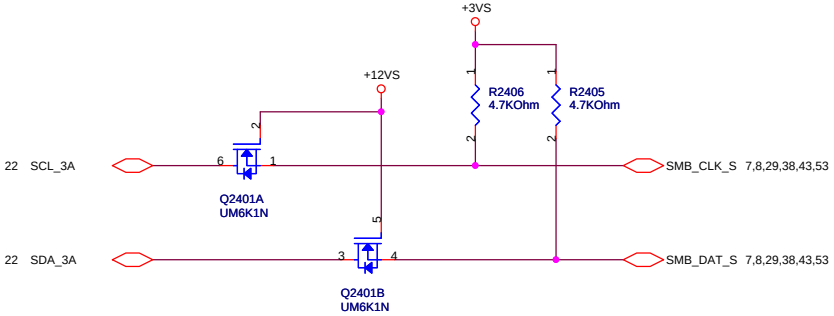


Title : SB-ICH9M(PWR)			
ASUSTeK COMPUTER INC. NB4	Engineer: Jace_Kuo		
Size: Custom	Project Name: M50Vm		Rev: 1.0
Date: Friday, March 07, 2008	Sheet 23 of 96		

ICH9-M



7 SO-DIMM0
8 SO-DIMM1
29 CLK-GEN
39 AUD-DSP
43 NEWCARD
53 WLAN

EC-IT8752

Master	Slave
SCL_3A SDA_3A (ICH9M)	A. SMB_CLK_S SMB_DAT_S → SO-DIMM0; SO-DIMM1; Debug; WLAN Card B. SMB_CLK_M SMB_DAT_M → CLK Generator
SMB0_CLK SMB0_DAT (EC)	BATTERY
SMB1_CLK SMB1_DAT (EC)	Thermal Sensor

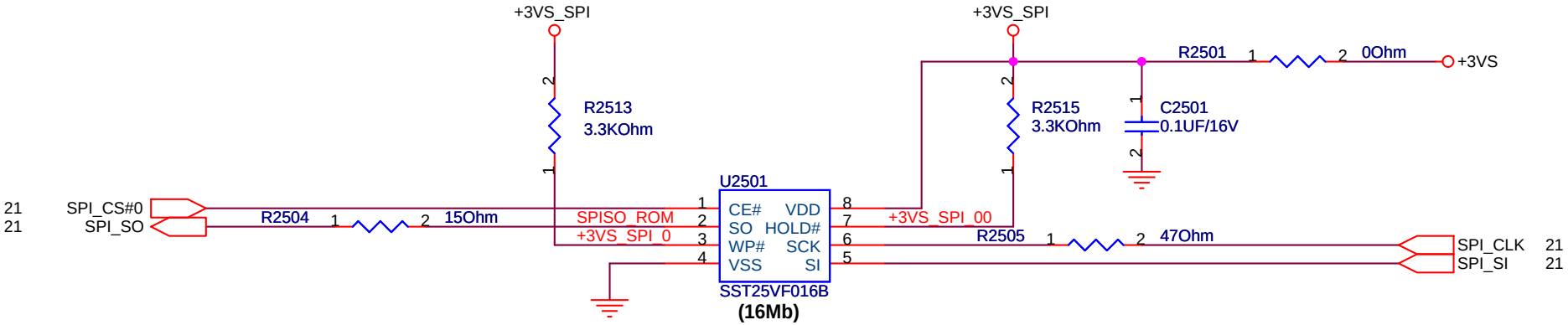
ASUSTeK COMPUTER INC. NB4

Title : ICH9M-Other

Engineer: Jace_Kuo

Size	Project Name	Rev
Custom	M50Vm	1.0

Date: Friday, March 07, 2008 Sheet 24 of 96



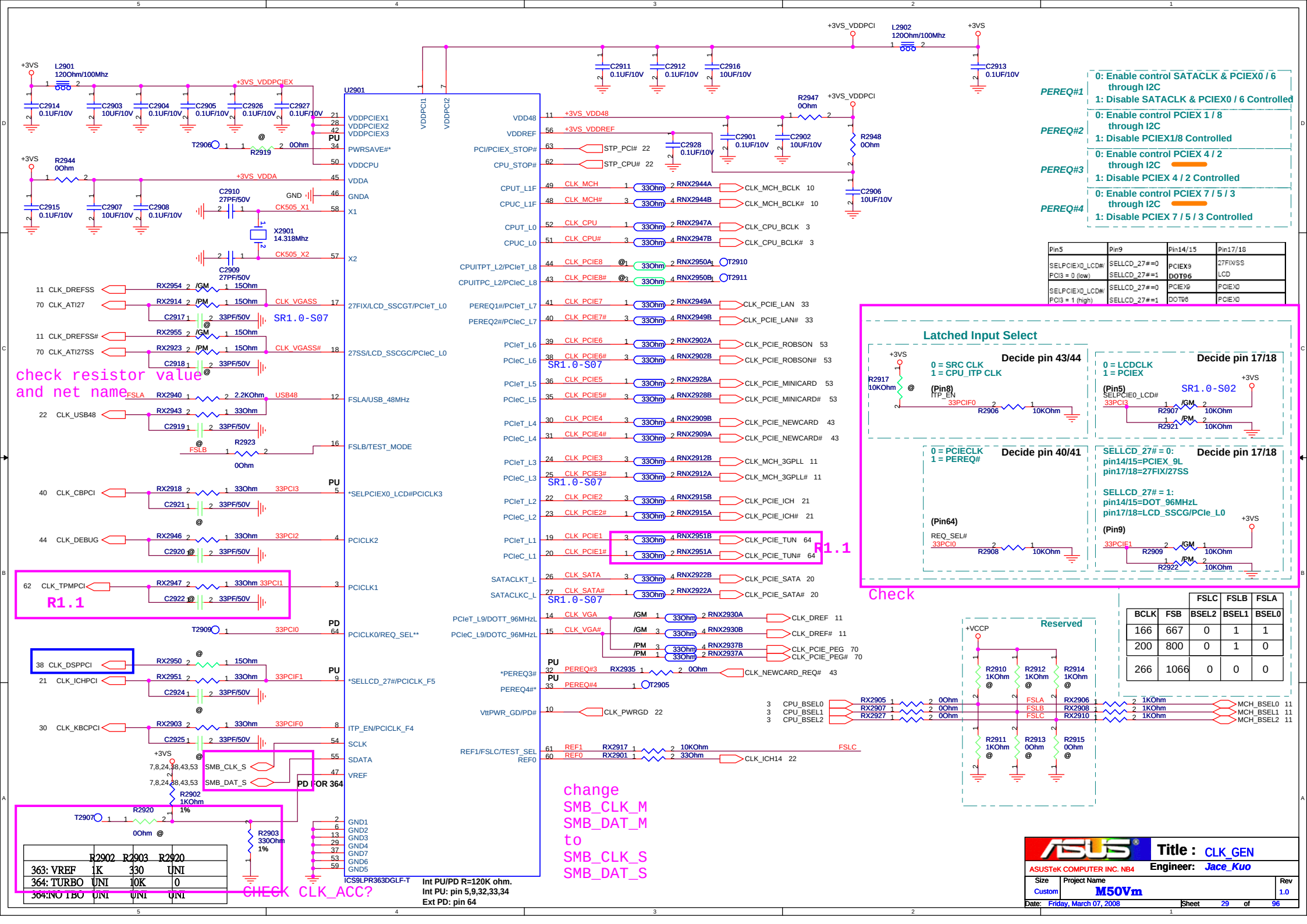
FOR iTPM

ASUSTeK COMPUTER INC. NB4	Title : SPI ROM	
	Engineer: Jace_Kuo	
Size: A	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 25 of 96	

Title :	
Engineer:	
Size: A	Project Name
Rev: 1.0	
Date: Wednesday, February 13, 2008	Sheet 26 of 96

Title :	
ASUSTeK COMPUTER INC. NB6	Engineer: Raphael_Chen
Size: A	Project Name: M50Vm
Rev: 1.0	
Date: Wednesday, February 13, 2008	Sheet 27 of 96

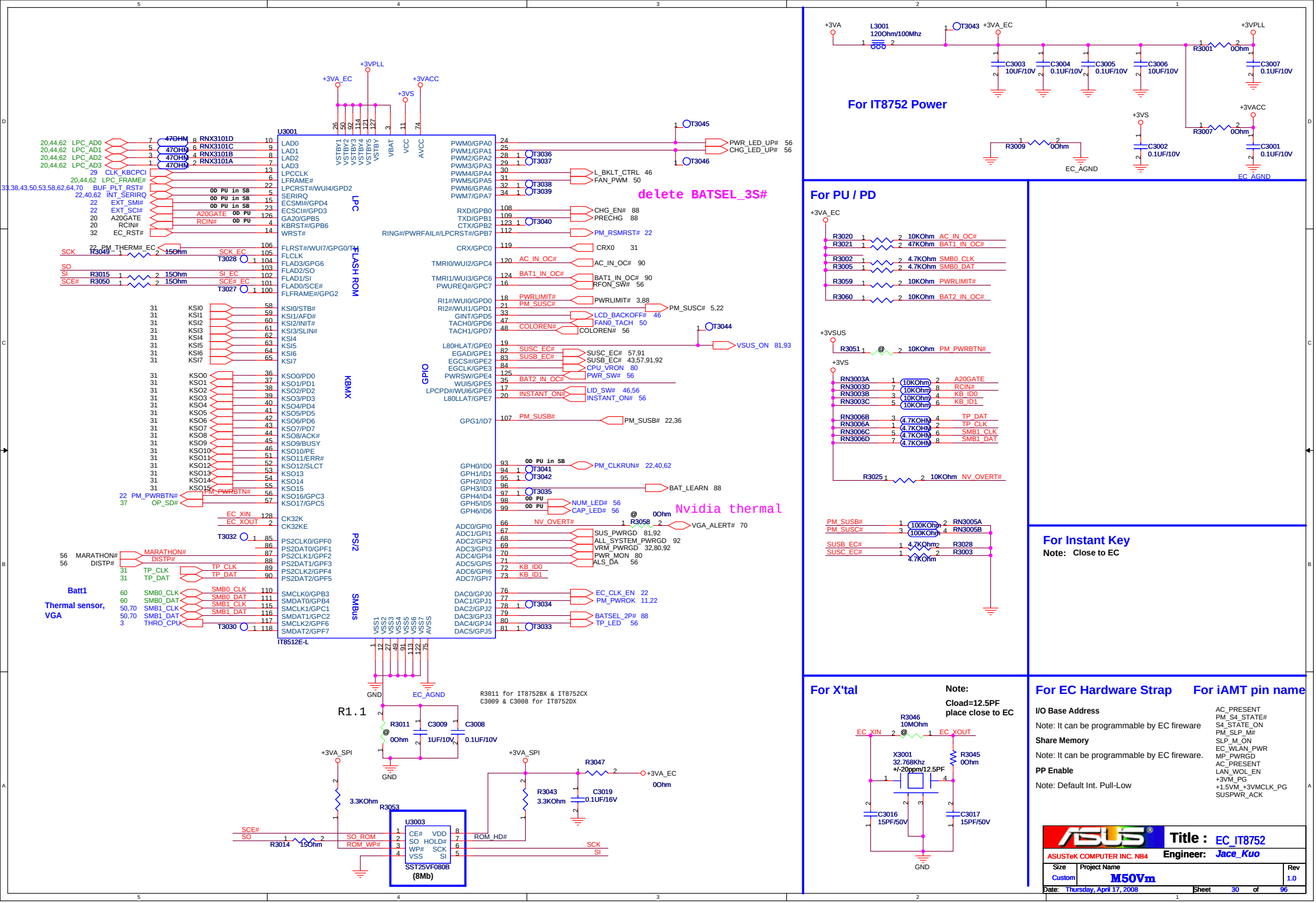
Title :	
ASUSTeK COMPUTER INC. NB6	Engineer: Raphael_Chen
Size: A	Project Name: M50Vm
Rev: 1.0	
Date: Wednesday, February 13, 2008	Sheet 28 of 96



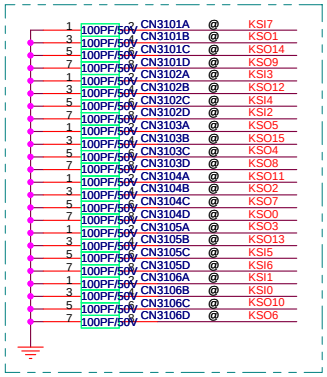
	R2902	R2903	R2920
363: VREF	1K	330	UNI
364: TURBO	UNI	10K	0
364:NO TBO	UNI	UNI	UNI

Pin5	Pin9	Pin14/15	Pin17/18
SELPCIEX0_LCD#/ PCI3 = 0 (low)	SELLCD_27#=0	PCIEX9 DOT96	27FIXSS LCD
	SELLCD_27#=1		
SELPCIEX0_LCD#/ PCI3 = 1 (high)	SELLCD_27#=0	PCIEX9	PCIEX0
	SELLCD_27#=1	DOT96	PCIEX0

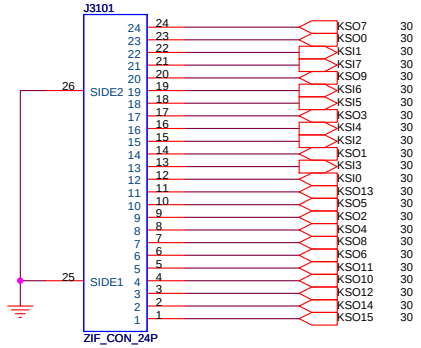
BCLK	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0


U3001
IT8512E-L
LPC
FLASH ROM
KBMX
PS/2
SMBus
GPIO
delete BATSEL_3S#
Nvidia thermal
Batt1
Thermal sensor, VGA
R1.1
R3011 for IT8752BX & IT8752CX
C3009 & C3008 for IT8752DX
U3003
SST25VF080B
(8Mb)
For IT8752 Power
For PU / PD
For Instant Key
Note: Close to EC
For X'tal
Note:
Cload=12.5PF
place close to EC
For EC Hardware Strap
I/O Base Address
Note: It can be programmable by EC fireware
Share Memory
Note: It can be programmable by EC fireware.
PP Enable
Note: Default Int. Pull-Low
For iAMT pin name
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK
Title : EC_IT8752
ASUSTeK COMPUTER INC. NB4
Engineer: Jace_Kuo
Size: Custom
Project Name: M50Vm
Rev: 1.0
Date: Thursday, April 17, 2008
Sheet 30 of 96

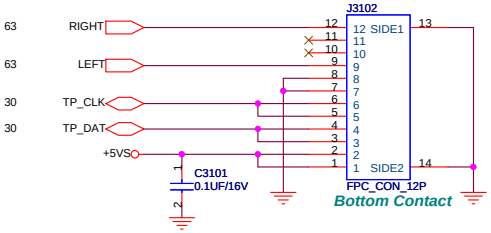
EMI



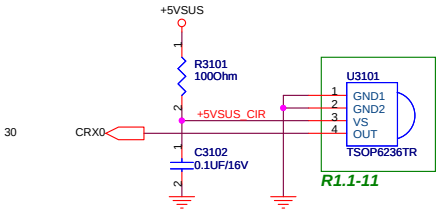
Keyboard



Touchpad



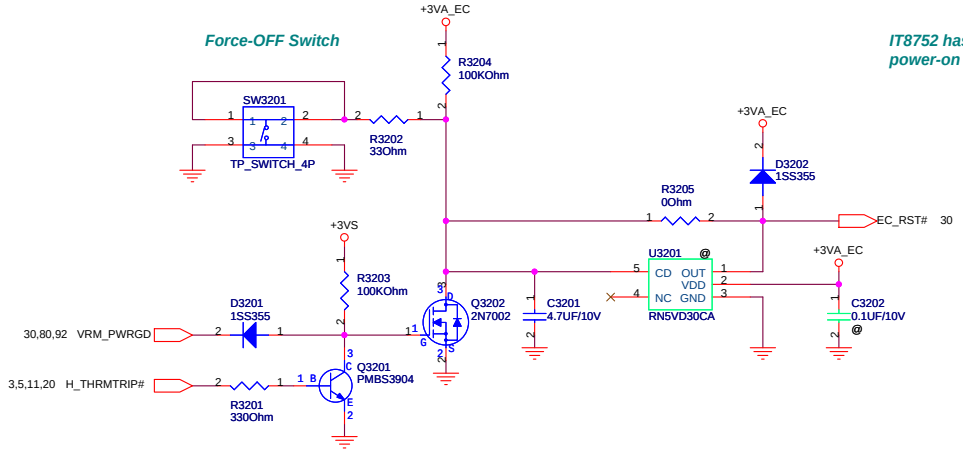
CIR



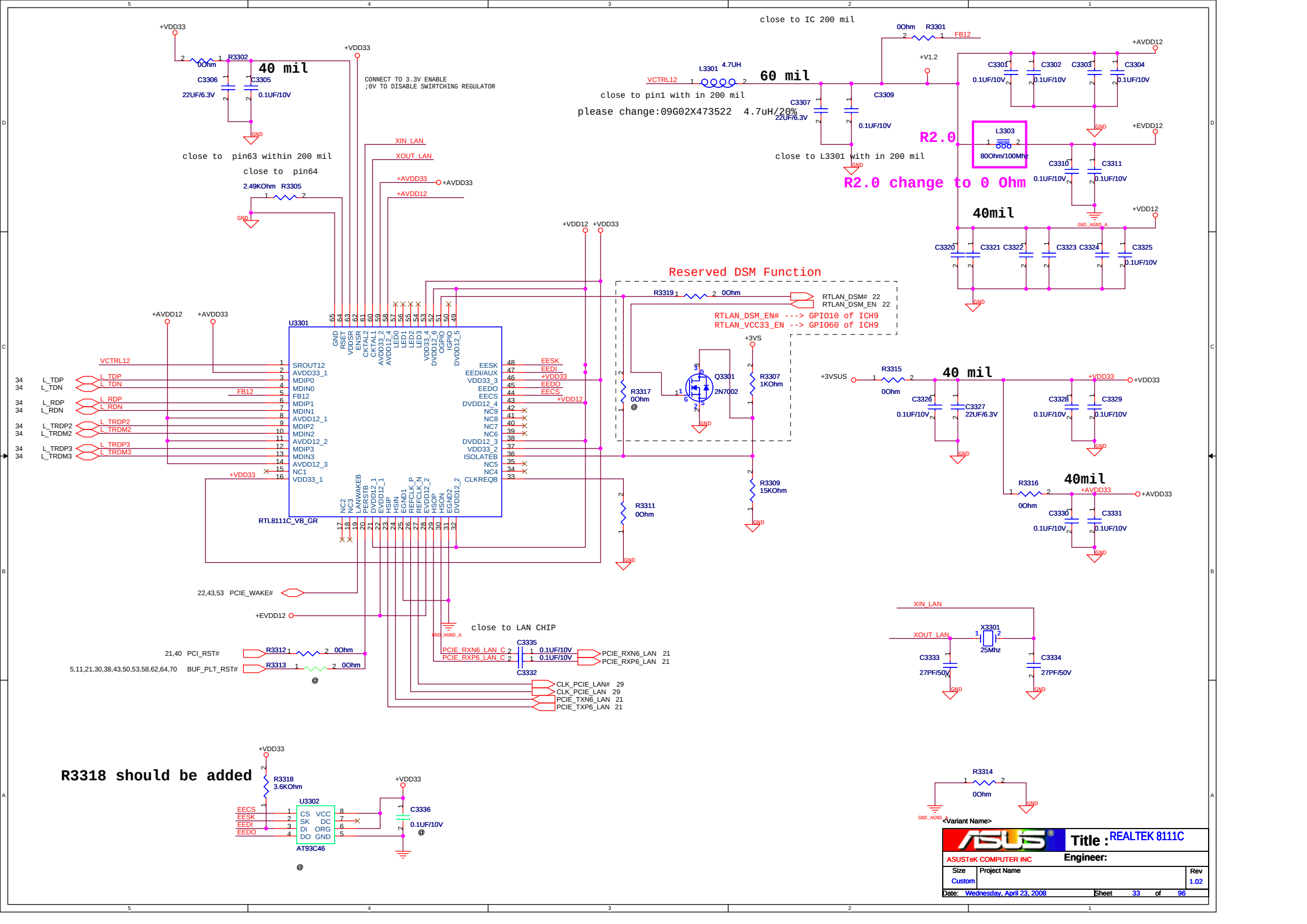
ASUSTeK COMPUTER INC. NB1	Title : KBC_KB, TP & CIR	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 31 of 96	

Force-OFF Switch

IT8752 has built-in level detection for power-on reset circuit



ASUSTeK COMPUTER INC. NB1	Title : RST_Reset Circuit	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 32 of 96	


close to IC 200 mil
0Ohm R3301
FB12
+AVDD12
+V1.2
L3301 4.7UH
VCTRL12
60 mil
close to pin1 with in 200 mil
please change:09G02X473522 4.7uH/20%
C3307 22UF/6.3V
C3309
0.1UF/10V
close to L3301 with in 200 mil
C3301 C3302 C3303 C3304 0.1UF/10V
+EVDD12
L3303 80Ohm/100Mhz
R2.0
R2.0 change to 0 Ohm
C3310 C3311 0.1UF/10V
40mil
+VDD12
GND_AGND_A
C3320 C3321 C3322 C3323 C3324 C3325 0.1UF/10V
+VDD33
+VDD12 +VDD33
Reserved DSM Function
R3319 0Ohm
RTLAN_DSM# 22
RTLAN_DSM_EN 22
RTLAN_DSM_EN# ---> GPIO10 of ICH9
RTLAN_VCC33_EN --> GPIO60 of ICH9
+3VS
Q3301 2N7002
R3317 0Ohm @
R3307 1KOhm
R3309 15KOhm
R3311 0Ohm
+3VSUS
R3315 0Ohm
40 mil
C3326 0.1UF/10V
C3327 22UF/6.3V
C3328 C3329 0.1UF/10V
R3316 0Ohm
40mil
C3330 C3331 0.1UF/10V
+AVDD33
+AVDD12 +AVDD33
U3301
RTL8111C_VB_GR
VCTRL12
L_TDP L_TDN
L_RDP L_RDN
L_TRDP2 L_TRDM2
L_TRDP3 L_TRDM3
FB12
+VDD33
EESK EEDI +VDD33 EEDO EECS +VDD12
22,43,53 PCIE_WAKE#
+EVDD12
close to LAN CHIP
21,40 PCI_RST#
5,11,21,30,38,43,50,53,58,62,64,70 BUF_PLT_RST#
R3312 0Ohm
R3313 0Ohm @
C3335 C3332 0.1UF/10V
PCIE_RXN6_LAN_C
PCIE_RXP6_LAN_C
PCIE_RXN6_LAN 21
PCIE_RXP6_LAN 21
CLK_PCIE_LAN# 29
CLK_PCIE_LAN 29
PCIE_TXN6_LAN 21
PCIE_TXP6_LAN 21
XIN_LAN
XOUT_LAN
X3301 25Mhz
C3333 C3334 27PF/50V
R3314 0Ohm
GND_AGND_A
+VDD33
R3302 0Ohm
40 mil
C3306 22UF/6.3V
C3305 0.1UF/10V
CONNECT TO 3.3V ENABLE
;0V TO DISABLE SWIRTCHING REGULATOR
close to pin63 within 200 mil
close to pin64
XIN_LAN
XOUT_LAN
+AVDD33
+AVDD12
2.49KOhm R3305
R3318 should be added
R3318 3.6KOhm
U3302
AT93C46
EECS EESK EEDI EEDO
C3336 0.1UF/10V @
@
<Variant Name>
Title : REALTEK 8111C
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name
Rev 1.02
Date: Wednesday, April 23, 2008
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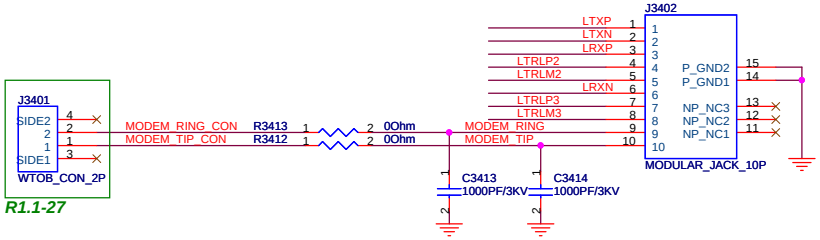
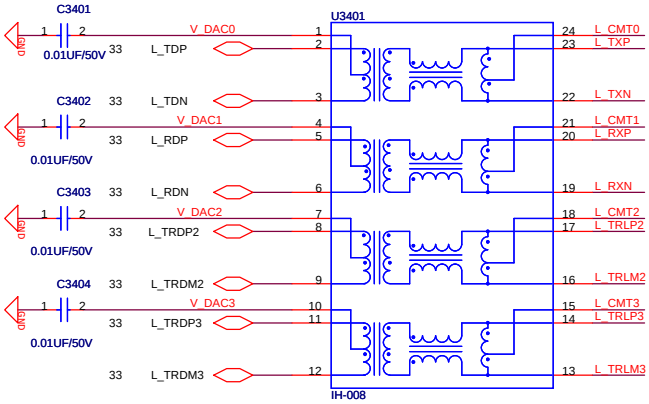
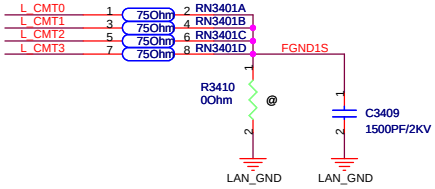
N1S Check connector to follow N1S or not

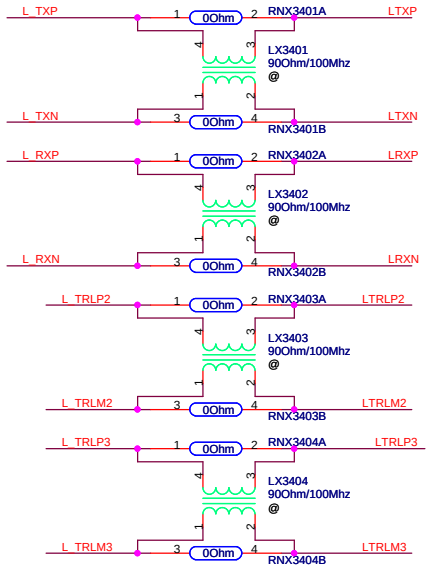


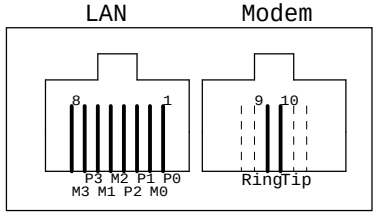
R1.1-27

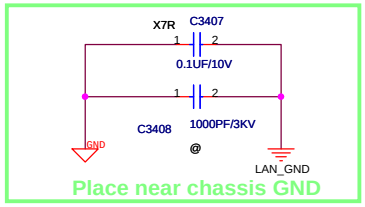


Transformer close CN3402









<Variant Name>

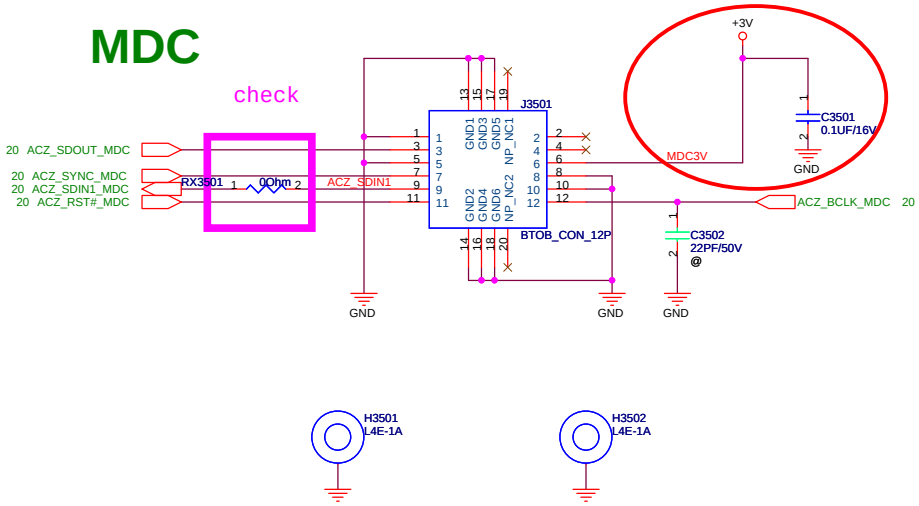
Title : IO

ASUSTeK COMPUTER INC Engineer:

Size	Project Name	Rev
Custom		1.01

Date: Wednesday, April 16, 2008 Sheet 34 of 96

MDC



ASUSTeK COMPUTER INC	Title : MDC	
	Engineer: Borland_Huang	
Size: Custom	Project Name: M50Vm	Rev: 1.01
Date: Friday, March 07, 2008	Sheet 35 of 96	

change codec part-number to ALC663 02G611005200

R3608 5.1K_663/39.2K_660
change Sense B Resistor R3608
partnumber to 39.2KOhm for 662

1. HP1 with S/PDIF
2. HP2
3. MIC1(Jack)
4. MIC2 (Digital INT MIC)

change AC HP1 Capacitor C3625
C3626 partnumber to 0 Ohm

change MIC Capacitor C3635 C3637
C3630 C3631 from Y5V to X5R

Input impedence:64K ohm(Typical)

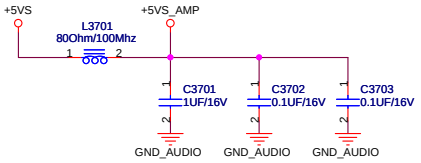
Audio Power

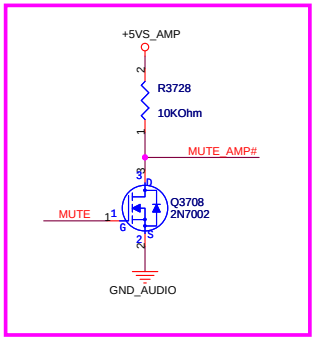
FOR ADJUST MODE:
Vo=1.25*(1+R3706/R3705)
= 1.25*(1+ 100K/34.8K) = 4.84

Try 0 ohm

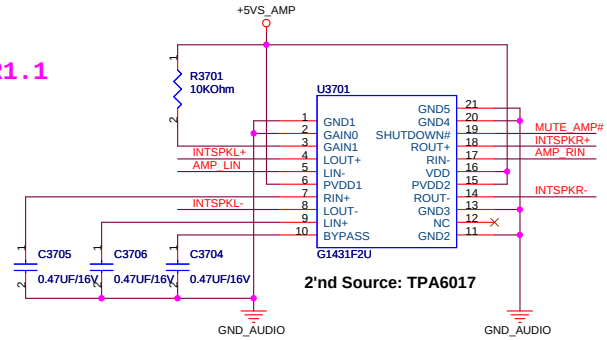
PC BEEP

Title : CODEC ALC663			
Engineer:			
Size: Custom	Project Name		Rev: 1.1
Date: Thursday, April 17, 2008		Sheet 36 of 96	





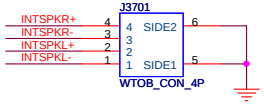
R1.1



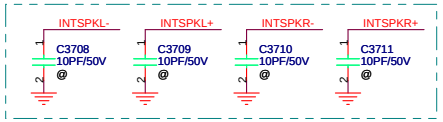
2'nd Source: TPA6017

GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

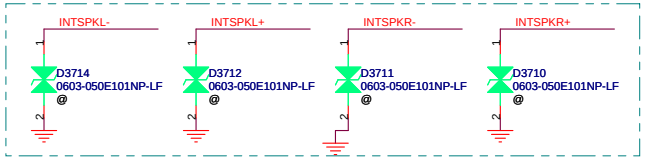
Internal Speaker Conn.

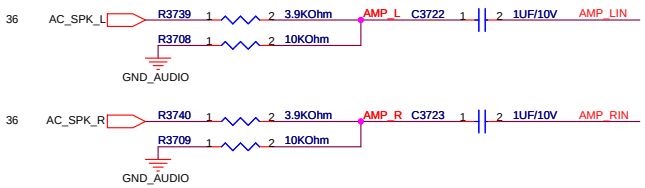


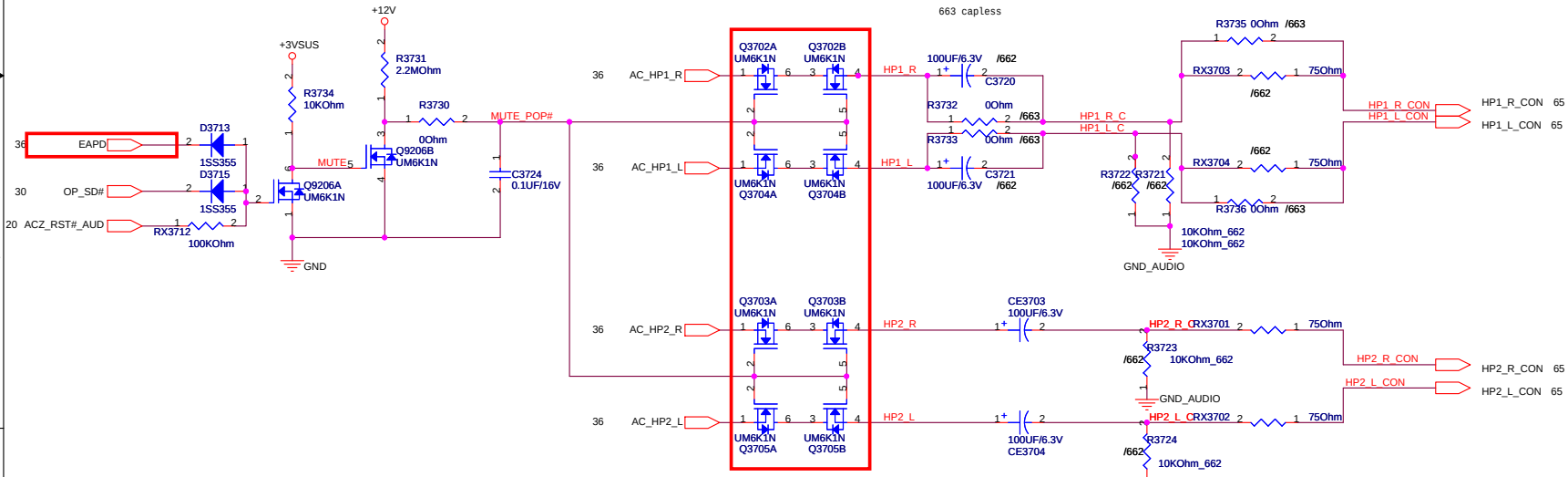
Reserved for 3G



Reserved for EMI

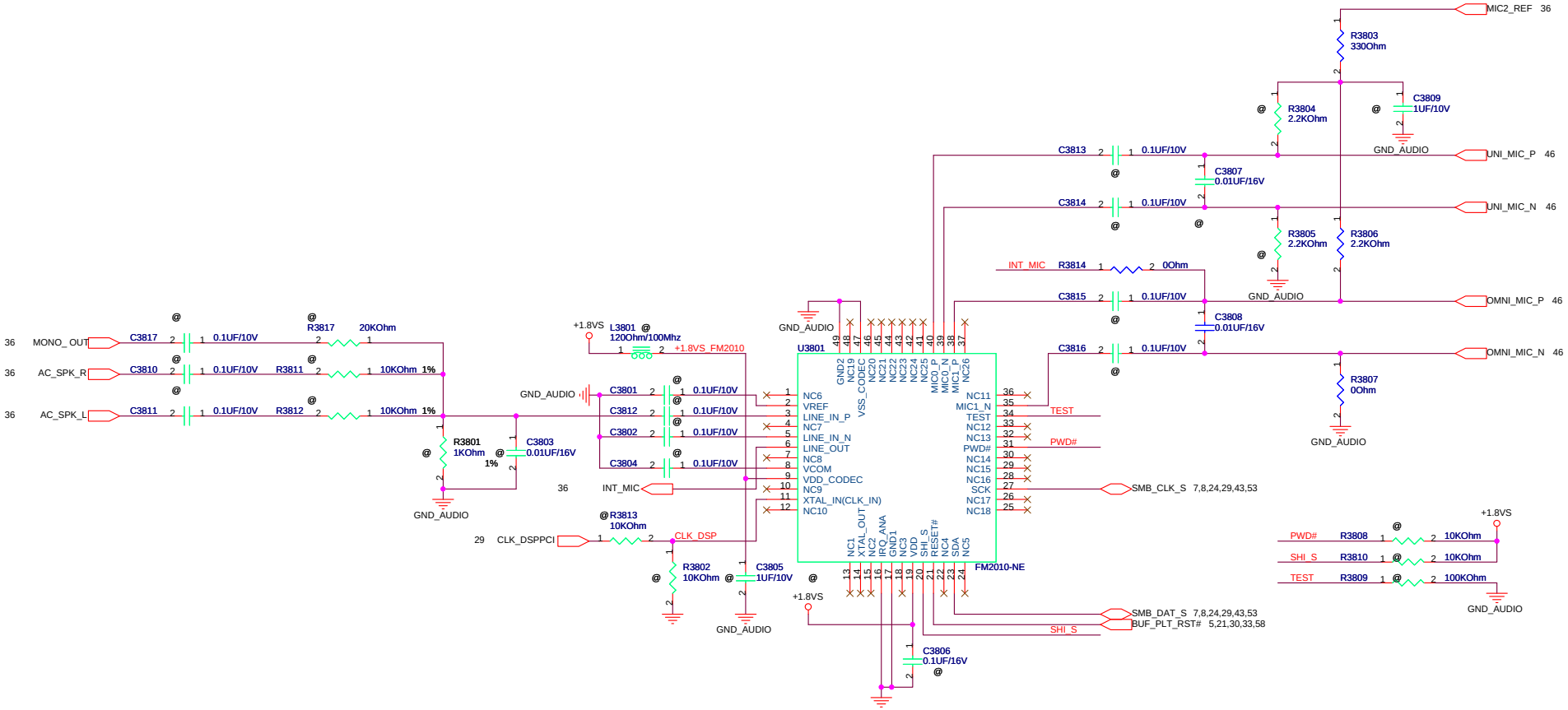






ASUS	Title : AUD_Amp & Jack		
	Engineer:		
Size: Custom	Project Name		Rev: 1.0
Date: Friday, March 07, 2008	Sheet 37 of 96		

Main Board



ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer:	
Size: Custom	Project Name	Rev: 1.0
Date: Tuesday, April 15, 2008	Sheet 38 of 96	

Main Board

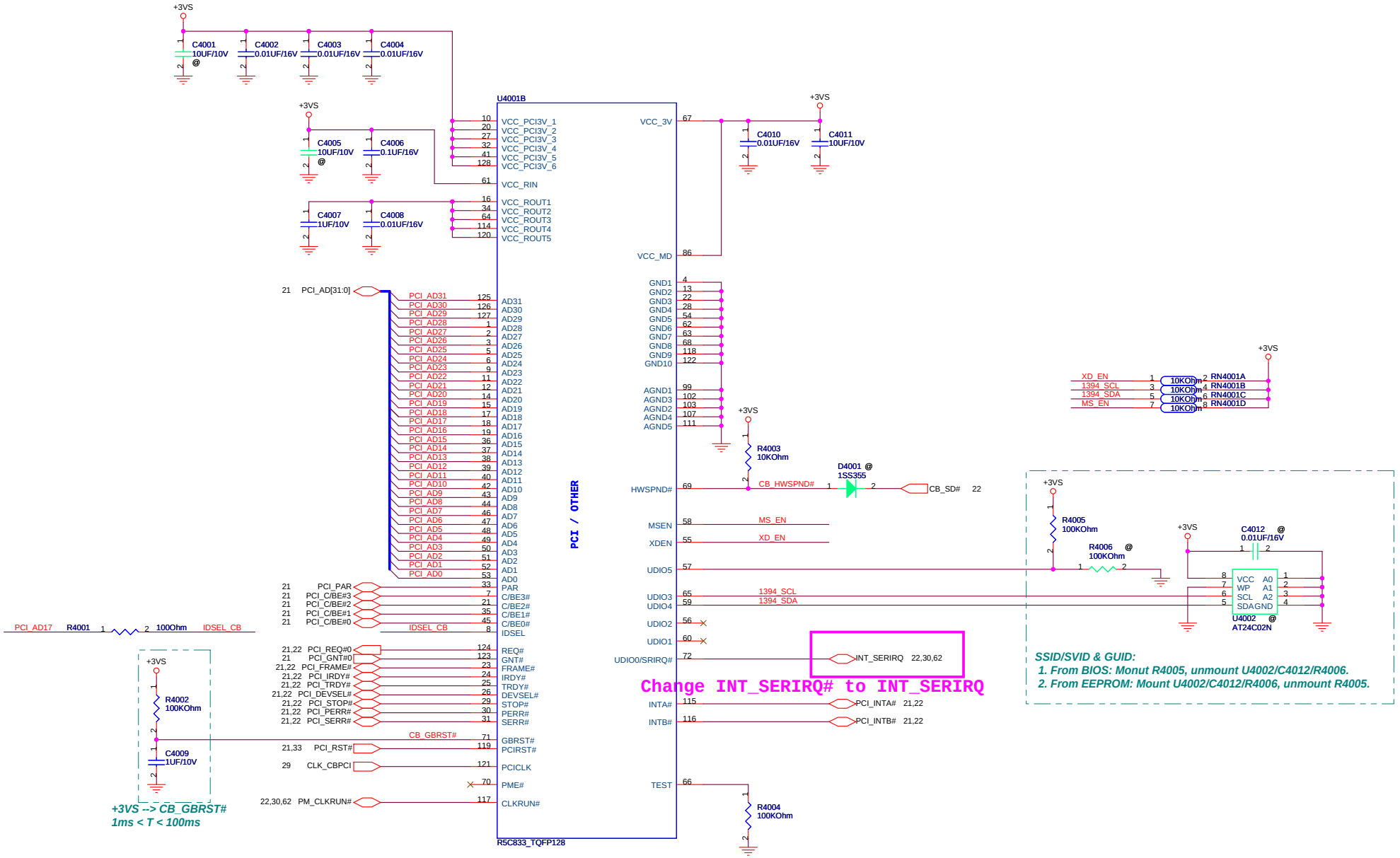
ASUSTeK COMPUTER INC. NB1

Title : AUD_****

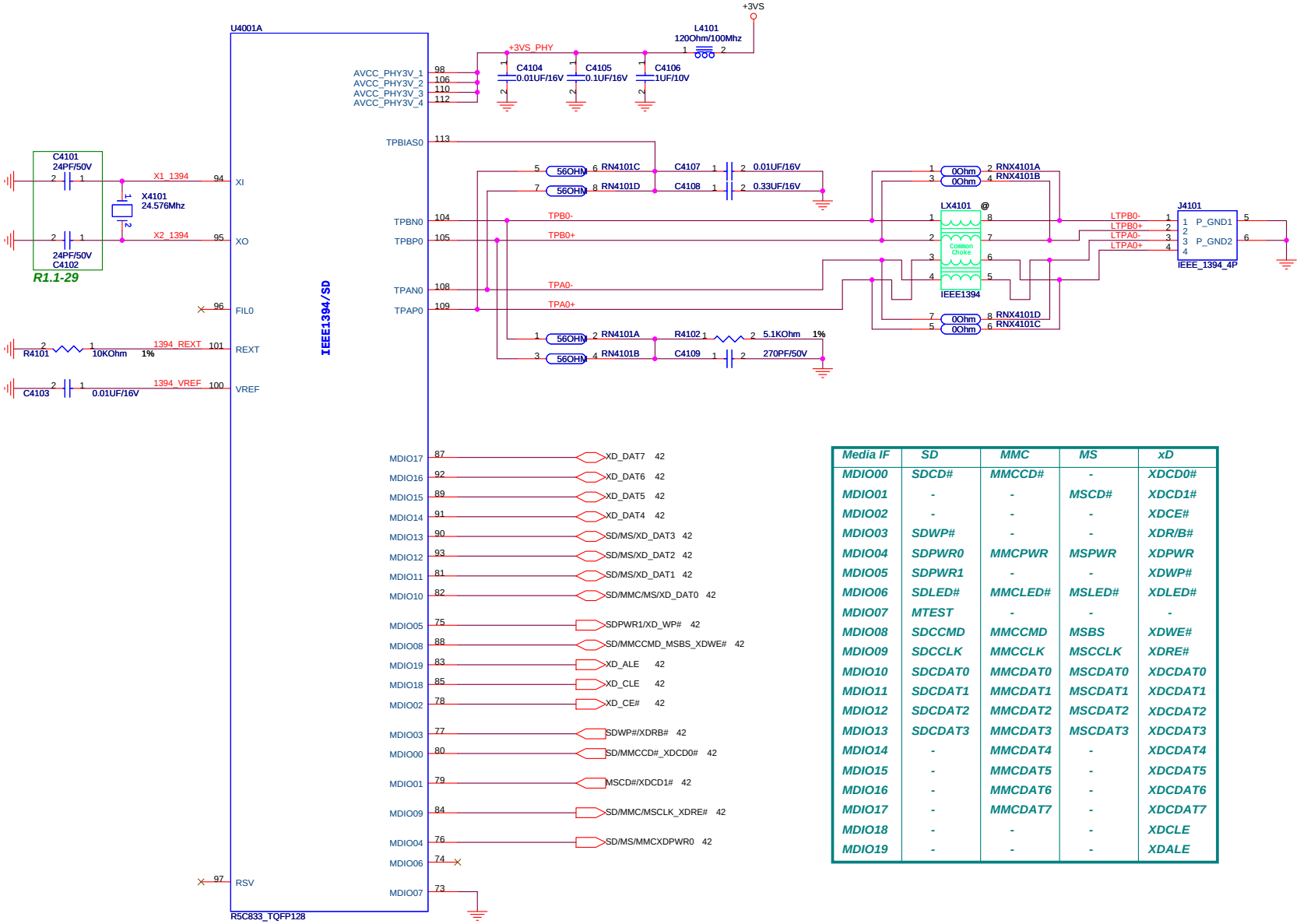
Engineer: John Hung

Size	Project Name	Rev
Custom	M50Vm	1.0

Date: Wednesday, February 13, 2008 Sheet 39 of 96



ASUSTeK COMPUTER INC. NB1	Title : CB_R5C833	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 40 of 96	



Media IF	SD	MMC	MS	xD
MDIO00	SDCD#	MMCCD#	-	XDCD0#
MDIO01	-	-	MSCD#	XDCD1#
MDIO02	-	-	-	XDCE#
MDIO03	SDWP#	-	-	XDR/B#
MDIO04	SDPWR0	MMCPWR	MSPWR	XDPWR
MDIO05	SDPWR1	-	-	XDWP#
MDIO06	SDLED#	MMCLED#	MSLED#	XDLED#
MDIO07	MTEST	-	-	-
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCCLK	MMCCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT0	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1	MMCDAT1	MSCDAT1	XDCDAT1
MDIO12	SDCDAT2	MMCDAT2	MSCDAT2	XDCDAT2
MDIO13	SDCDAT3	MMCDAT3	MSCDAT3	XDCDAT3
MDIO14	-	MMCDAT4	-	XDCDAT4
MDIO15	-	MMCDAT5	-	XDCDAT5
MDIO16	-	MMCDAT6	-	XDCDAT6
MDIO17	-	MMCDAT7	-	XDCDAT7
MDIO18	-	-	-	XDCLE
MDIO19	-	-	-	XDALE

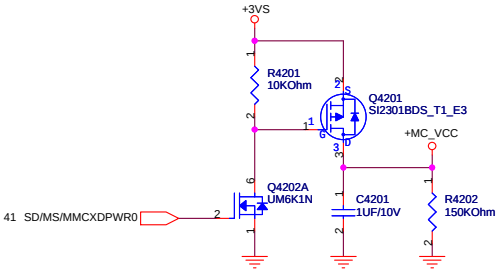
ASUSTeK COMPUTER INC. NB1

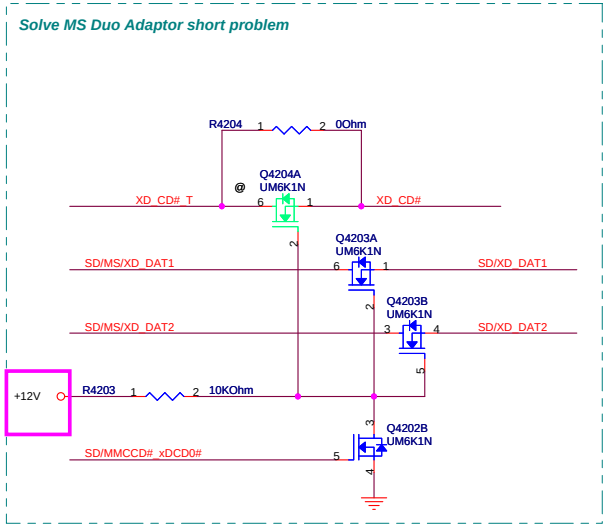
Title : CB_R5C833

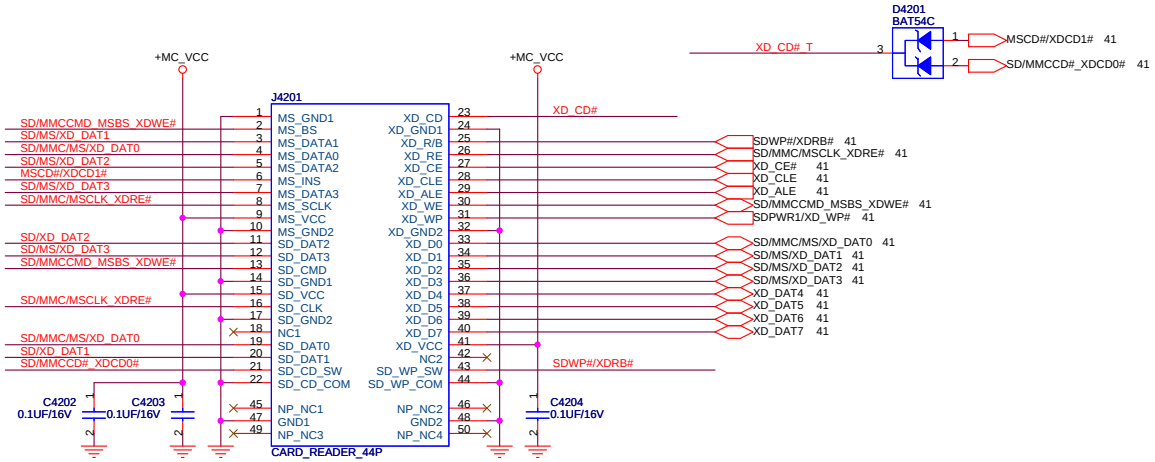
Engineer: John Hung

Size	Project Name	Rev
Custom	M50Vm	1.0

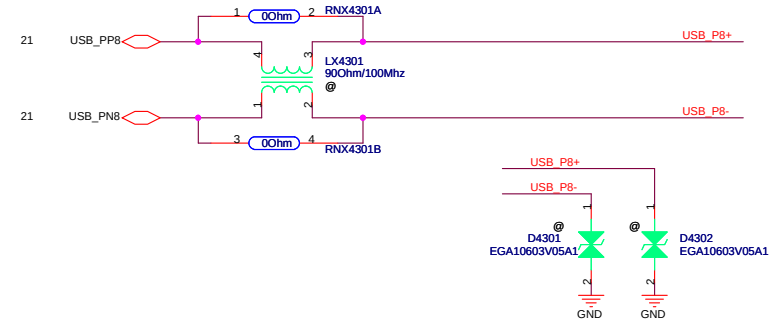
Date: Friday, March 07, 2008 Sheet 41 of 96



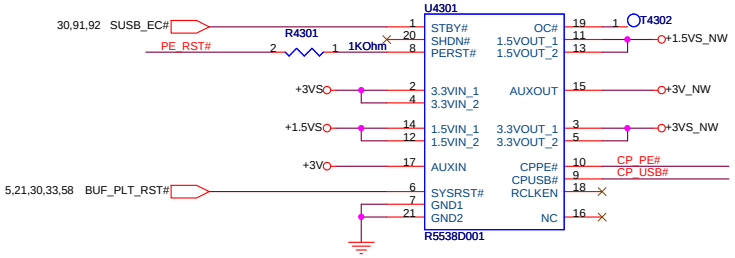




ASUSTeK COMPUTER INC. NB1	Title : CB_4in1 CardReader	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 42 of 96	

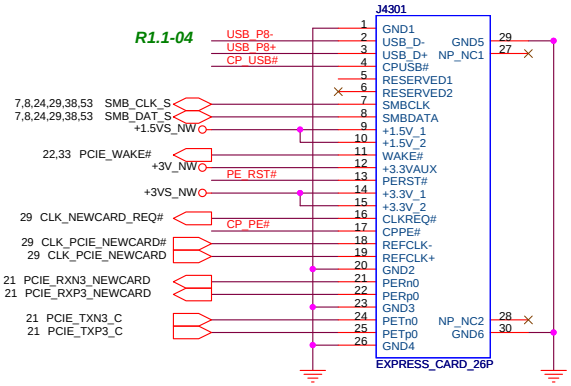


R1.1-04

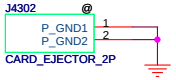


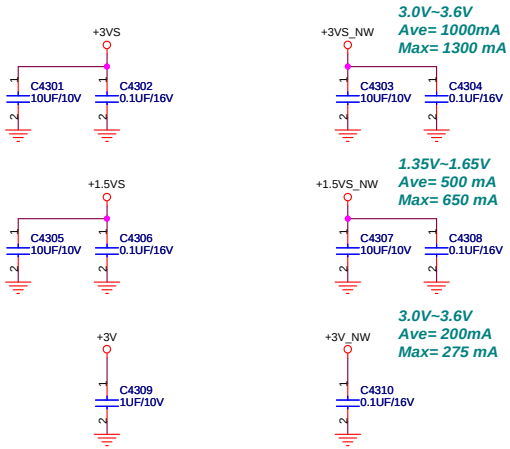
NewCard Header

R1.1-04



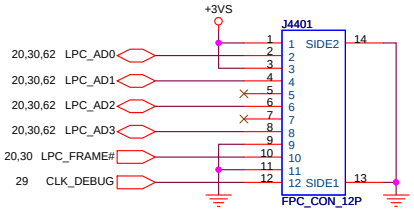
NewCard Ejecter





ASUSTeK COMPUTER INC. NB1	Title : CB_NewCard	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 43 of 96	

LPC Debug Port



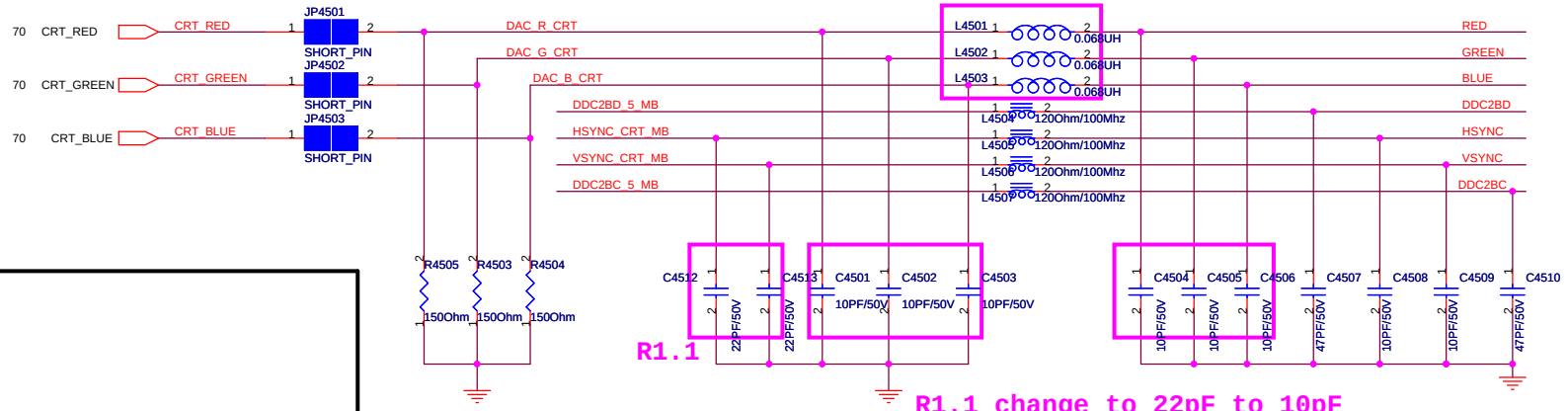
Bottom Contact

For NewCard Debug Card

Delete

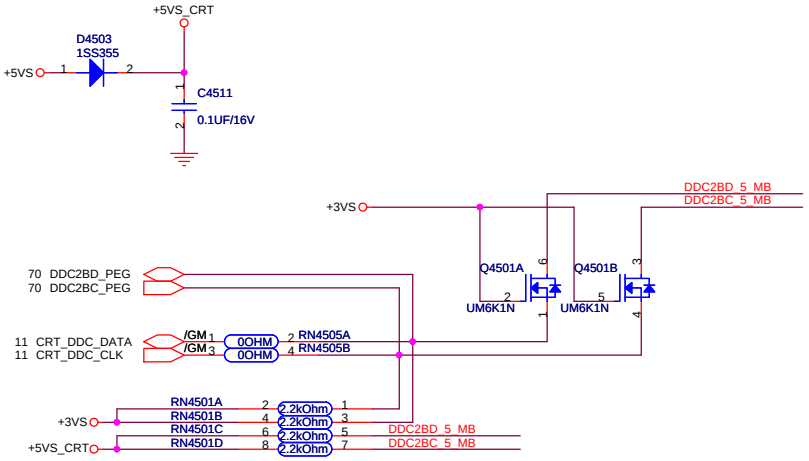
ASUSTeK COMPUTER INC. NB1	Title : BUG_LPC Debug	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 44 of 96	

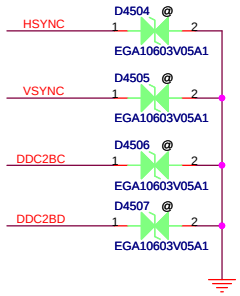
R1.1 change to 0.068uH



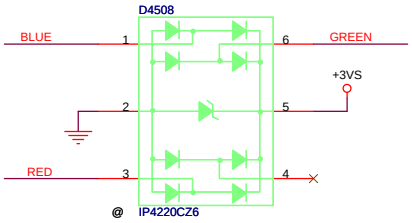
R1.1 change to 22pF to 10pF

MXM CONNECTOR SIDE

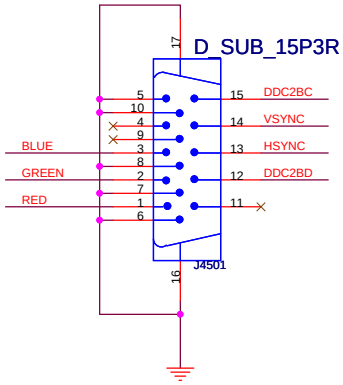


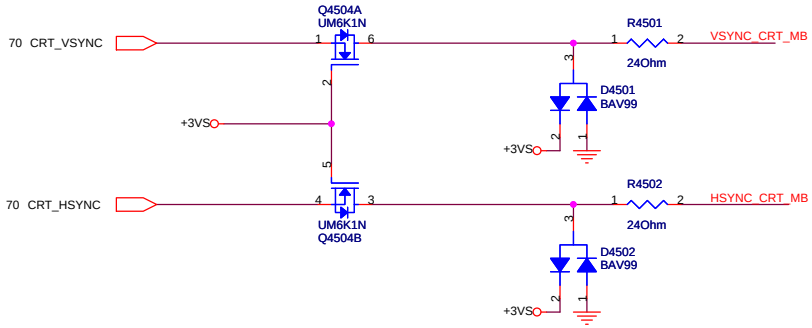


PLACE ESD Diodes near VGA port

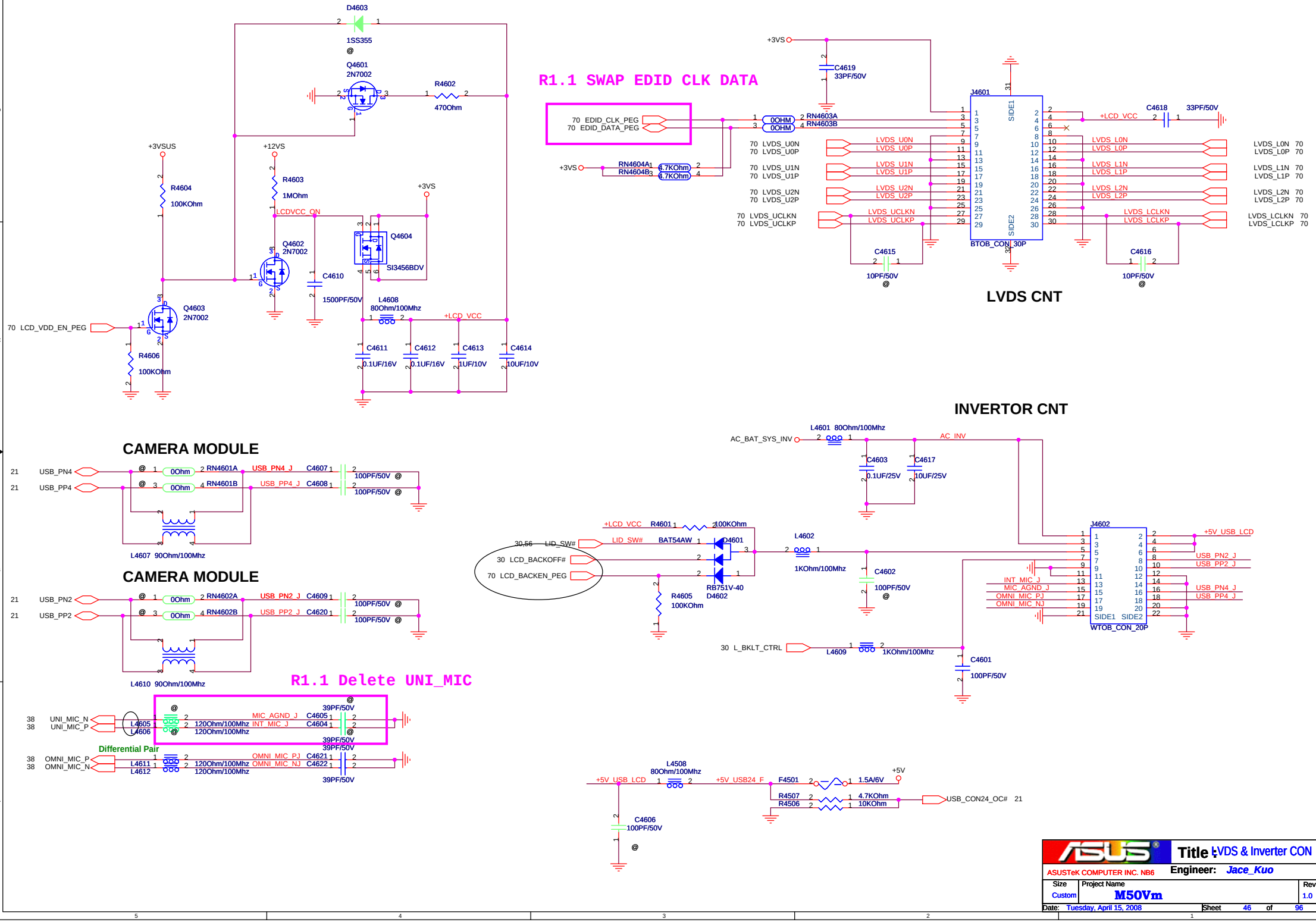


12G101102155





ASUSTeK COMPUTER INC. NB6	Title : CRT	
	Engineer: Jace_Kuo	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 45 of 96	


D4603
1SS355
Q4601
2N7002
R4602
470Ohm
+3VSUS
+12VS
R4604
100KOhm
R4603
1MOhm
LCDVCC_ON
+3VS
Q4604
SI3456BDV
Q4602
2N7002
C4610
1500PF/50V
L4608
80Ohm/100Mhz
+LCD_VCC
70 LCD_VDD_EN_PEG
Q4603
2N7002
R4606
100KOhm
C4611
0.1UF/16V
C4612
0.1UF/16V
C4613
1UF/10V
C4614
10UF/10V
R1.1 SWAP EDID CLK DATA
70 EDID_CLK_PEG
70 EDID_DATA_PEG
C4619
33PF/50V
J4601
RN4603A
RN4603B
0OHM
RN4604A
RN4604B
4.7KOhm
70 LVDS_U0N
70 LVDS_U0P
70 LVDS_U1N
70 LVDS_U1P
70 LVDS_U2N
70 LVDS_U2P
70 LVDS_UCLKN
70 LVDS_UCLKP
LVDS_U0N
LVDS_U0P
LVDS_U1N
LVDS_U1P
LVDS_U2N
LVDS_U2P
LVDS_UCLKN
LVDS_UCLKP
C4615
10PF/50V
C4616
10PF/50V
C4618
33PF/50V
+LCD_VCC
LVDS_L0N
LVDS_L0P
LVDS_L1N
LVDS_L1P
LVDS_L2N
LVDS_L2P
LVDS_LCLKN
LVDS_LCLKP
BTOB_CON_30P
LVDS CNT
CAMERA MODULE
21 USB_PN4
21 USB_PP4
RN4601A
RN4601B
USB_PN4_J
USB_PP4_J
C4607
C4608
100PF/50V
L4607 90Ohm/100Mhz
CAMERA MODULE
21 USB_PN2
21 USB_PP2
RN4602A
RN4602B
USB_PN2_J
USB_PP2_J
C4609
C4620
100PF/50V
L4610 90Ohm/100Mhz
R1.1 Delete UNI_MIC
38 UNI_MIC_N
38 UNI_MIC_P
L4605
L4606
120Ohm/100Mhz
MIC_AGND_J
INT_MIC_J
C4605
C4604
39PF/50V
Differential Pair
38 OMNI_MIC_P
38 OMNI_MIC_N
L4611
L4612
OMNI_MIC_PJ
OMNI_MIC_NJ
C4621
C4622
INVERTOR CNT
AC_BAT_SYS_INV
L4601 80Ohm/100Mhz
AC_INV
C4603
0.1UF/25V
C4617
10UF/25V
+LCD_VCC
R4601
100KOhm
30,56 LID_SW#
LID_SW#
BAT54AW
D4601
30 LCD_BACKOFF#
70 LCD_BACKEN_PEG
RB751V-40
D4602
R4605
100KOhm
L4602
1KOhm/100Mhz
C4602
100PF/50V
J4602
INT_MIC_J
MIC_AGND_J
OMNI_MIC_PJ
OMNI_MIC_NJ
+5V_USB_LCD
USB_PN2_J
USB_PP2_J
USB_PN4_J
USB_PP4_J
WTOB_CON_20P
30 L_BKLT_CTRL
L4609
1KOhm/100Mhz
C4601
100PF/50V
L4508
80Ohm/100Mhz
+5V_USB_LCD
+5V_USB24_F
F4501
1.5A/6V
+5V
R4507
4.7KOhm
R4506
10KOhm
USB_CON24_OC#
C4606
100PF/50V
ASUSTeK COMPUTER INC. NB6
Title: LVDS & Inverter CON
Engineer: Jace_Kuo
Size: Custom
Project Name: M50Vm
Rev: 1.0
Date: Tuesday, April 15, 2008
Sheet 46 of 96

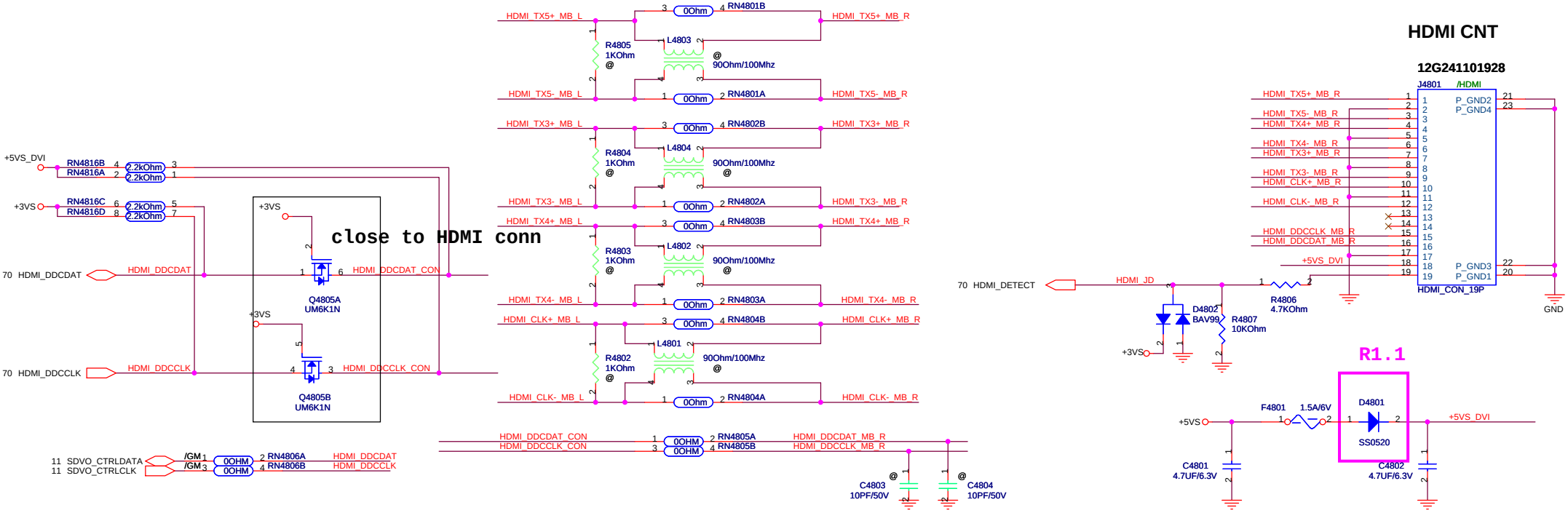
Title : TV_OUT CON

ASUSTeK COMPUTER INC. NB6

Engineer: Jace_Kuo

Size	Project Name	Rev
Custom	M50Vm	1.0

Date: Wednesday, February 13, 2008 Sheet 47 of 96



HDMI CNT

12G241101928

R1.1

Delete HDMI UMA

HDMI_TX3-_MB_L
HDMI_TX3+_MB_L
HDMI_TX4-_MB_L
HDMI_TX4+_MB_L
HDMI_TX5-_MB_L
HDMI_TX5+_MB_L
HDMI_CLK-_MB_L
HDMI_CLK+_MB_L

VGA_HDMI_TX3- 70
VGA_HDMI_TX3+ 70
VGA_HDMI_TX4- 70
VGA_HDMI_TX4+ 70
VGA_HDMI_TX5- 70
VGA_HDMI_TX5+ 70
VGA_HDMI_CLKB- 70
VGA_HDMI_CLKB+ 70

ASUSTeK COMPUTER INC. NB6

Title: LVDS & Inverter CON

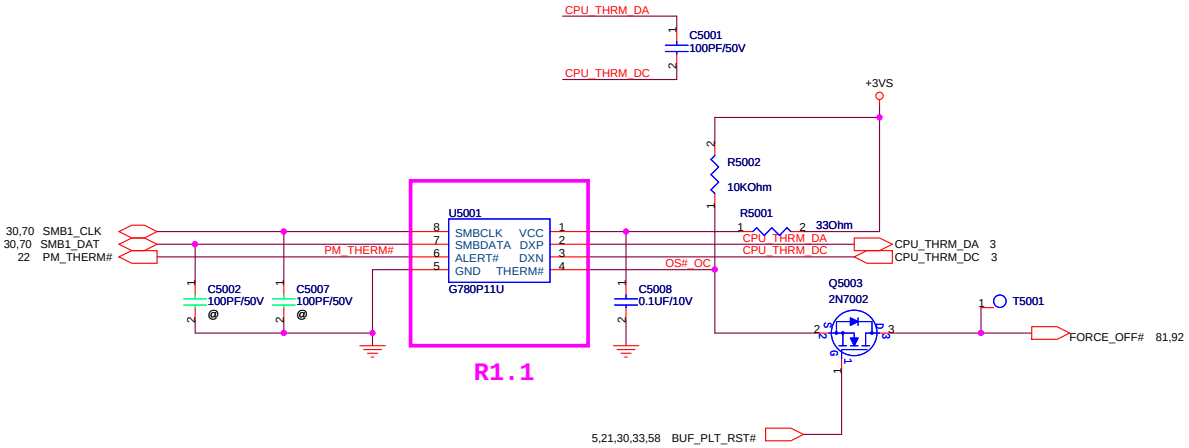
Engineer: Jace_Kuo

Size	Project Name	Rev
Custom	M50Vm	1.0

Date: Friday, March 07, 2008 Sheet 48 of 96

Title :	
ASUSTeK COMPUTER INC. NB6	Engineer: Jace_Kuo
Size: Custom	Project Name: M50Vm
Rev: 1.0	
Date: Wednesday, February 13, 2008	Sheet 49 of 96

Thermal Sensor

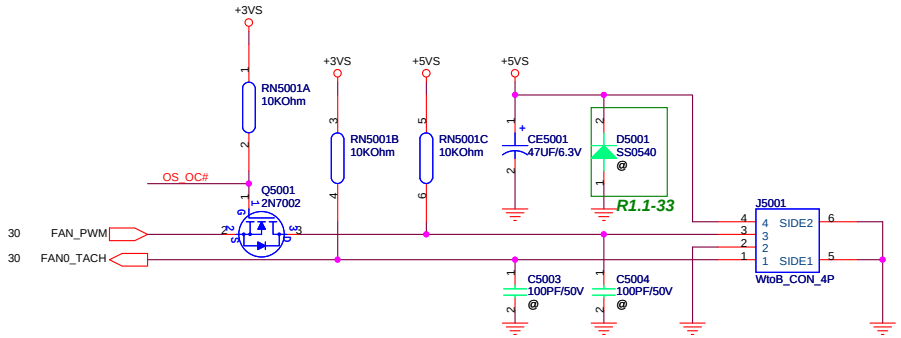


R1.1

SM Bus Address fix at:
1001 100x (98, 99),
Resolution : +/- 1
degree

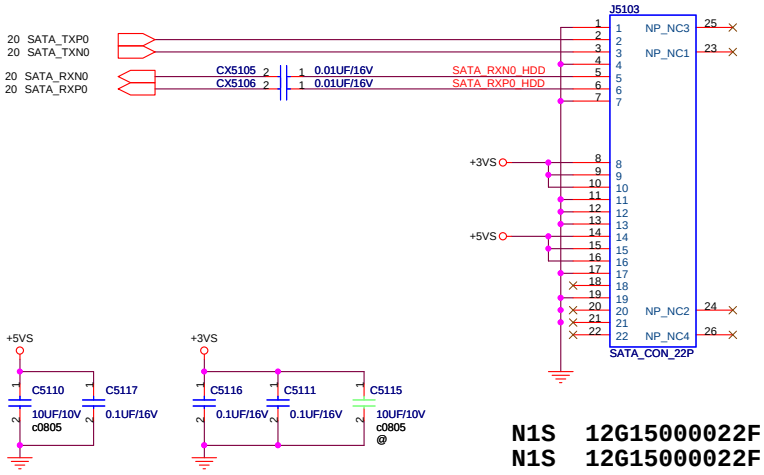
SM Bus Address fix at:
1001 100x (98, 99),
Resolution : +/- 1
degree

PWM Fan



ASUSTeK COMPUTER INC. NB1	Title : FAN_Fan & Sensor	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Thursday, April 17, 2008	Sheet 50 of 96	

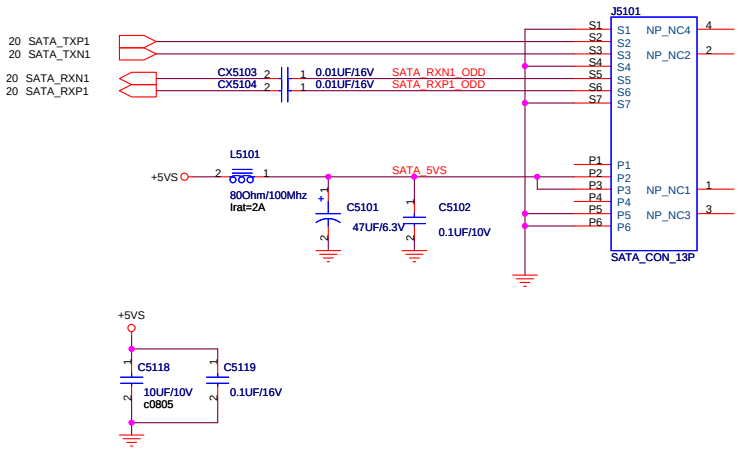
SATA0 HDD CON



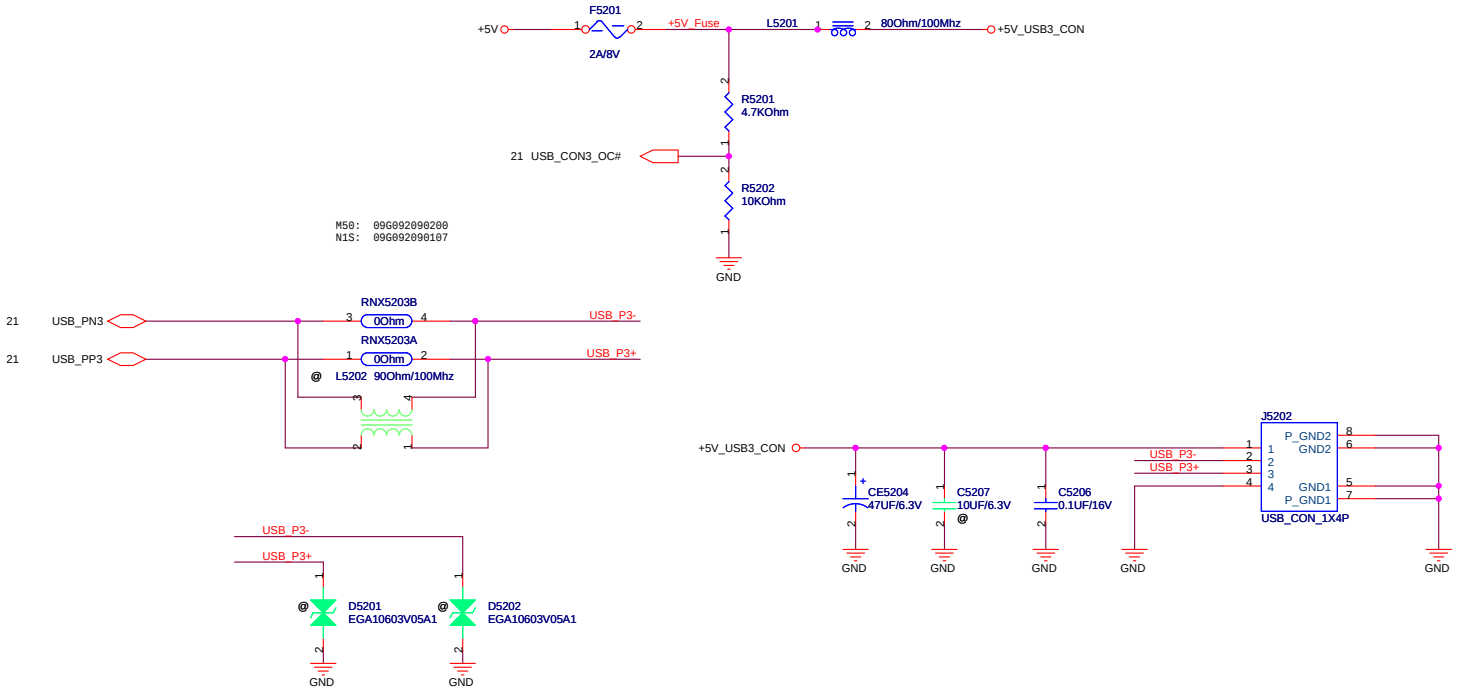
N1S 12G15000022F
N1S 12G15000022F

LAYOUT NOTE:
Two Strobes : Matched within 100 mils of each other
D[0:15] : Matched within +/- 450 mils of two strobes

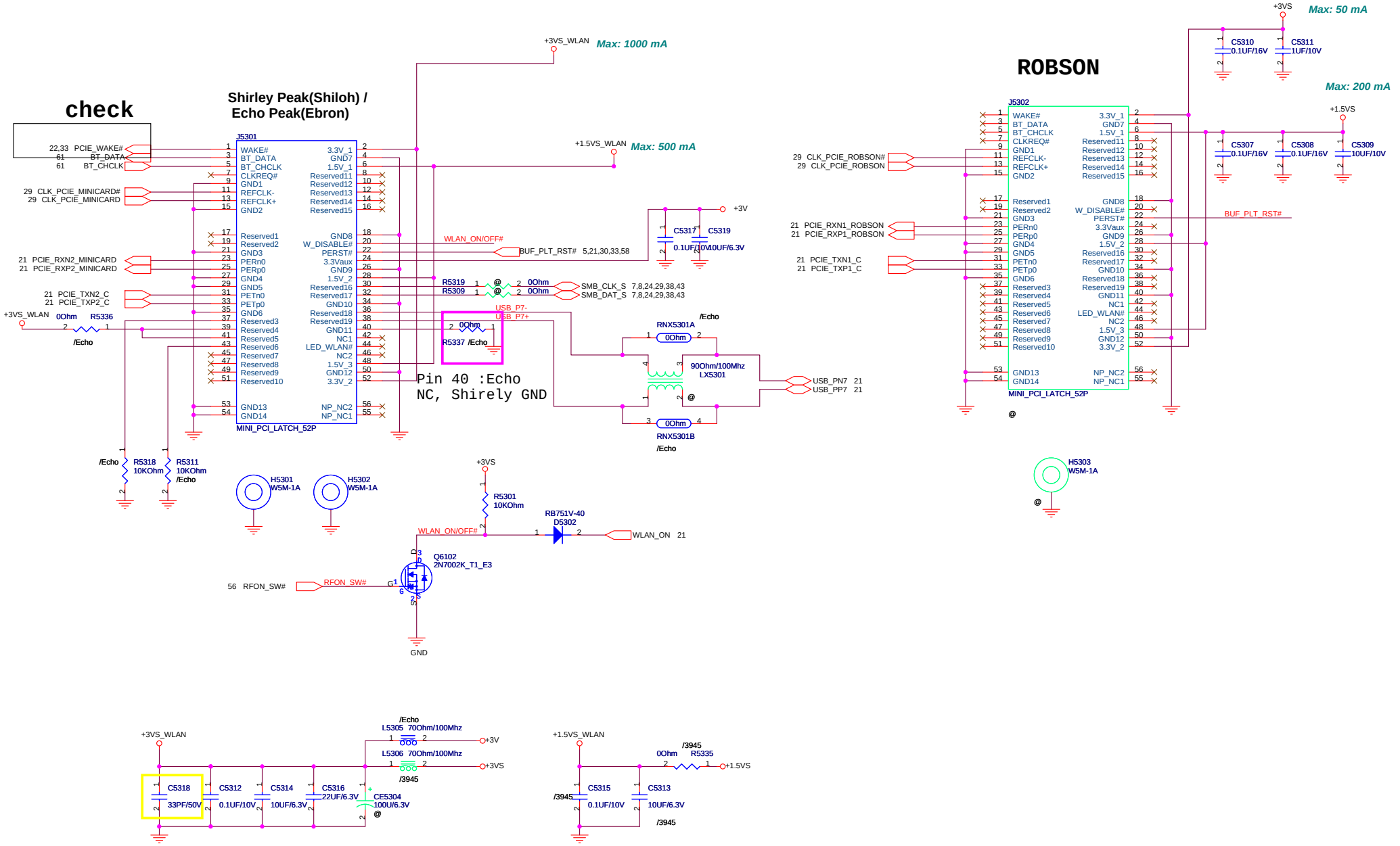
ODD CNT



ASUS	Title : HDD & ODD CONN.	
Engineer:		
Size: Custom	Project Name	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 51 of 96	



ASUSTeK COMPUTER INC. NB1	Title : USB_USB Ports	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Tuesday, April 15, 2008	Sheet 52 of 96	



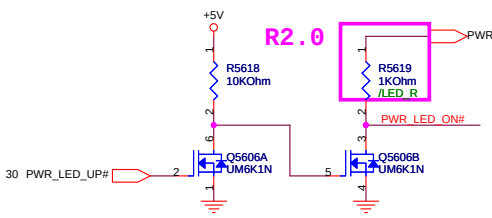
Title : PCI_WLAN		
ASUSTeK COMPUTER INC. NB1	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 53 of 96	

Title :	
Engineer:	
Size: A	Project Name:
Rev: 1.0	
Date: Wednesday, February 13, 2008	Sheet 54 of 96

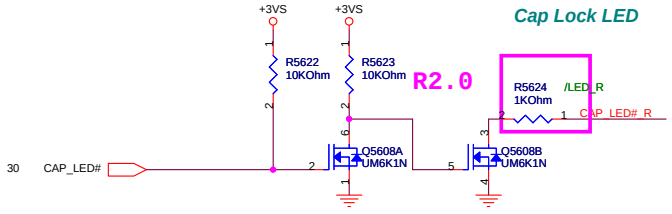
Title :	
Engineer:	
Size: A	Project Name:
Rev: 1.0	
Date: Wednesday, February 13, 2008	Sheet 55 of 96

Rear

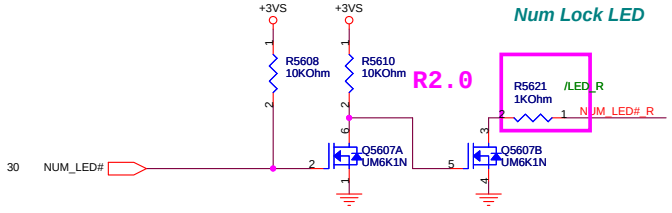
Power LED



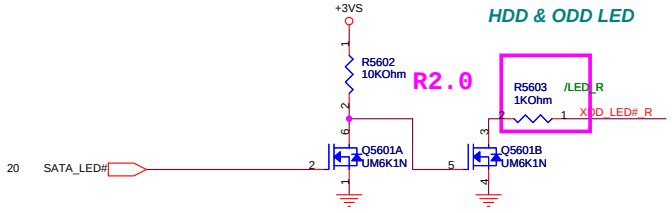
Cap Lock LED



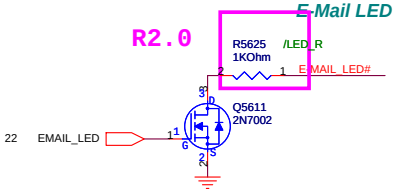
Num Lock LED



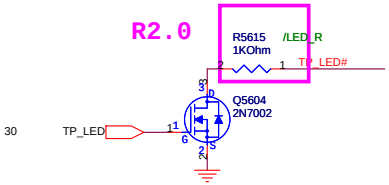
HDD & ODD LED

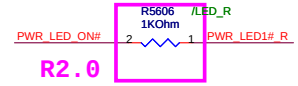


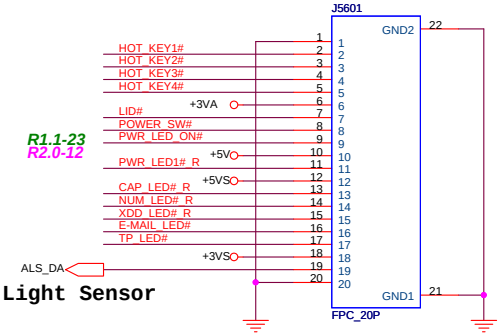
E-Mail LED

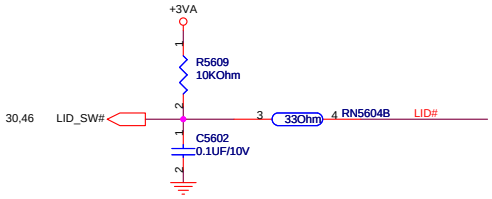


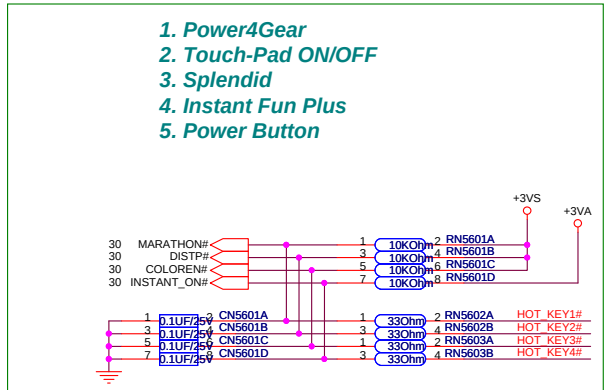
Touch-pad Lock LED



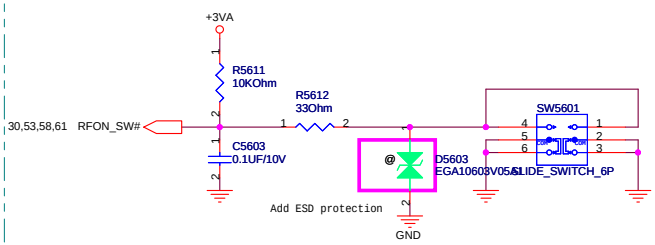




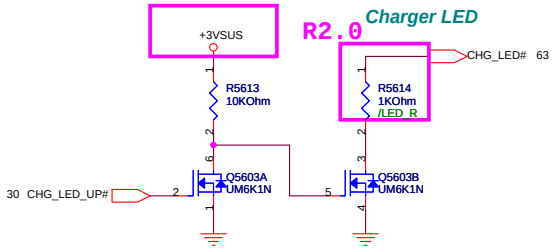




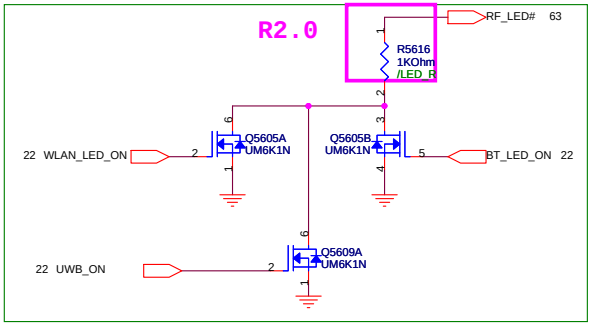
Main Board



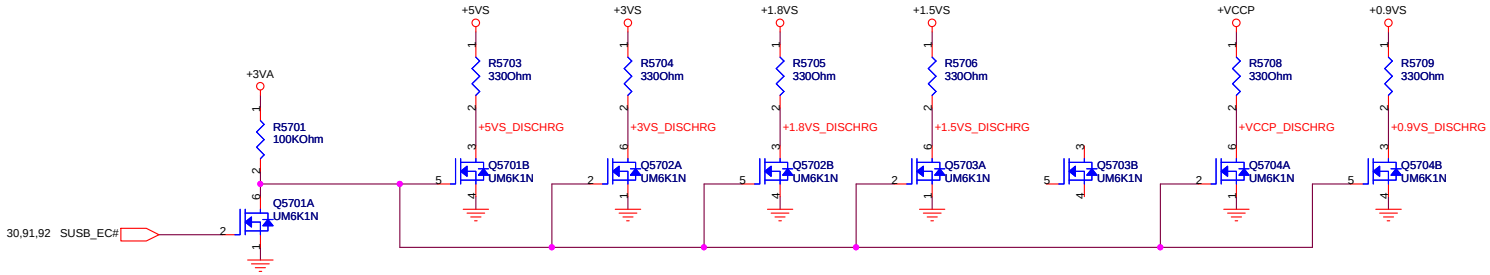
Charger LED

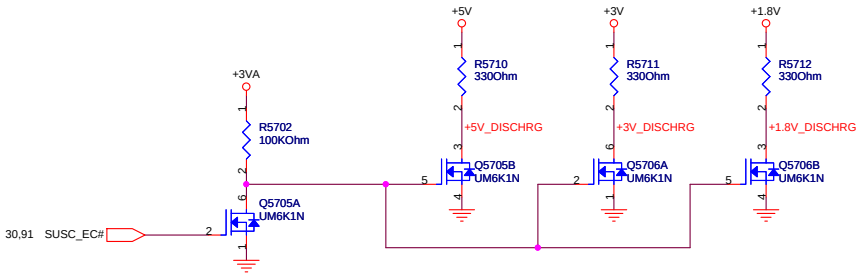


WLAN LED

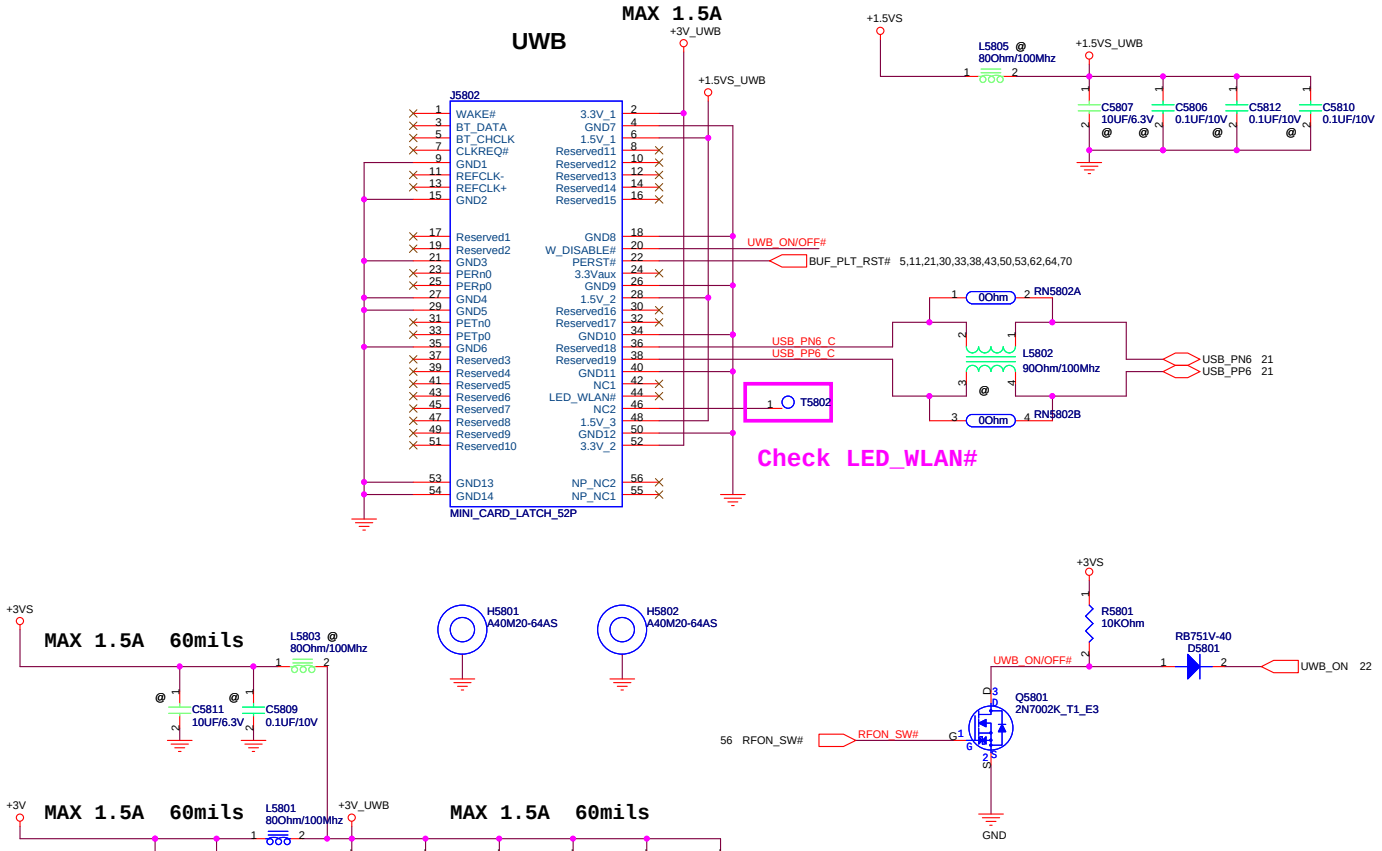


ASUSTeK COMPUTER INC. NB1	Title : LED_Indicator	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 2.0
Date: Wednesday, April 23, 2008	Sheet 56 of 96	





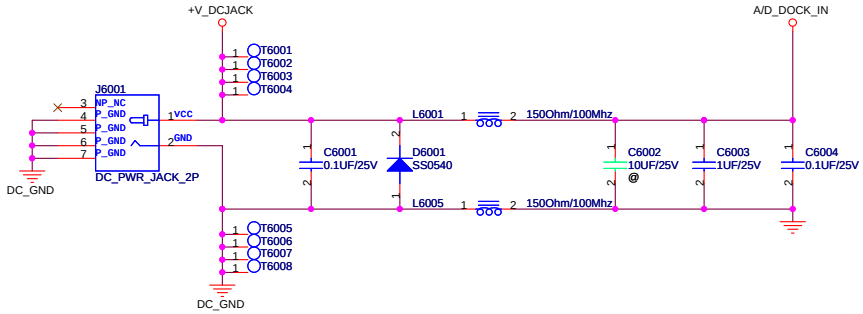
ASUSTeK COMPUTER INC. NB1	Title : DSG_Discharge	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 57 of 96	



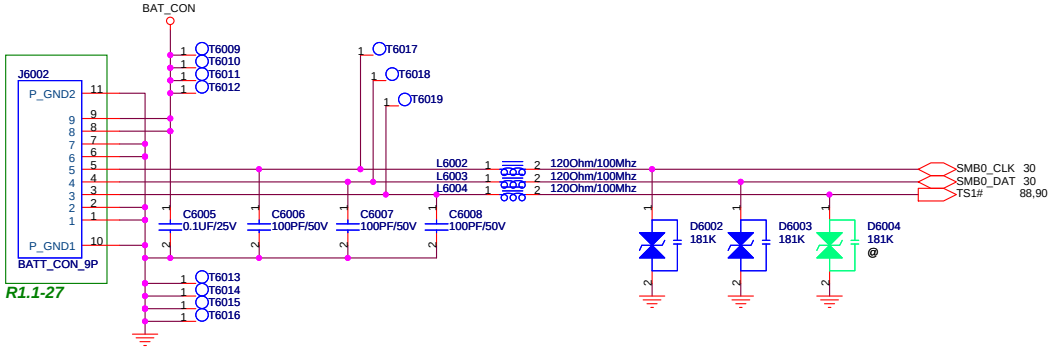
ASUSTeK COMPUTER INC. NB6	Title : UWB Minicard card	
	Engineer: Raphael_Chen	
Size: Custom	Project Name: V1V	Rev: 1.1
Date: Friday, March 07, 2008	Sheet 58 of 94	

ASUSTeK COMPUTER INC. NB6	Title : Engineer:	
Size: A	Project Name	Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 59 of 96	

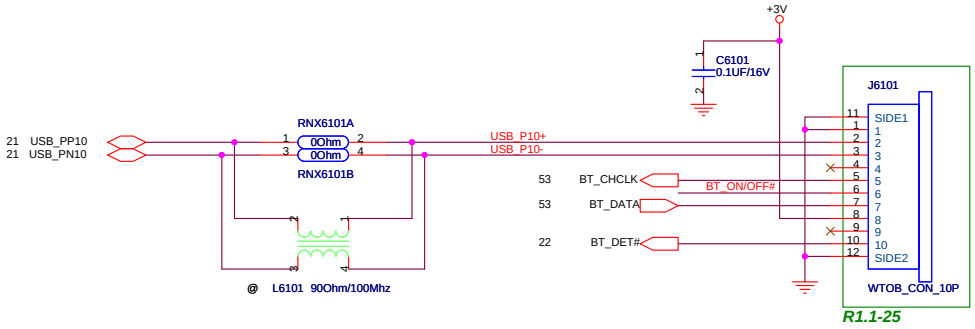
DC Jack



Battery Connector

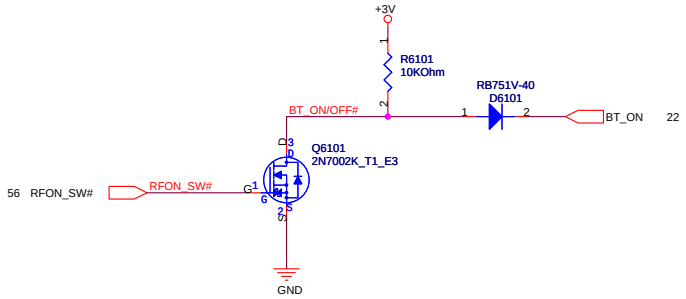


ASUSTeK COMPUTER INC. NB1	Title : DC_DC & BAT Conn.	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Thursday, April 17, 2008	Sheet 60 of 96	

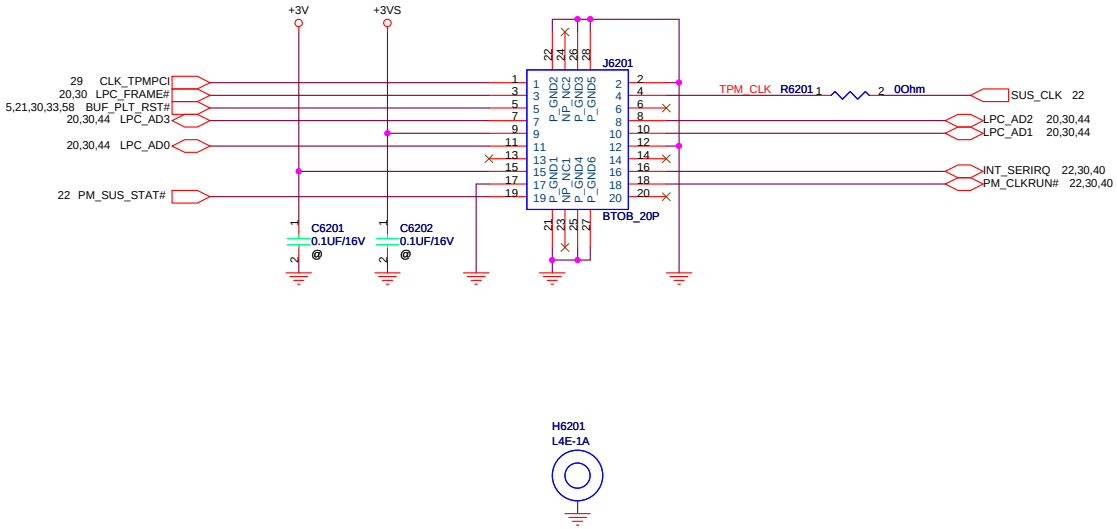


R1.1-25

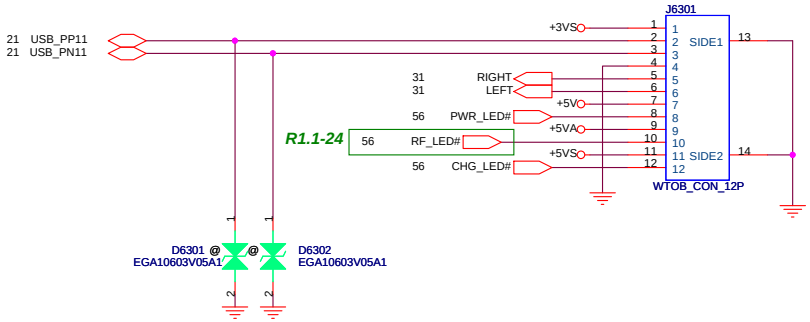
BT change from 2.0 to 2.1



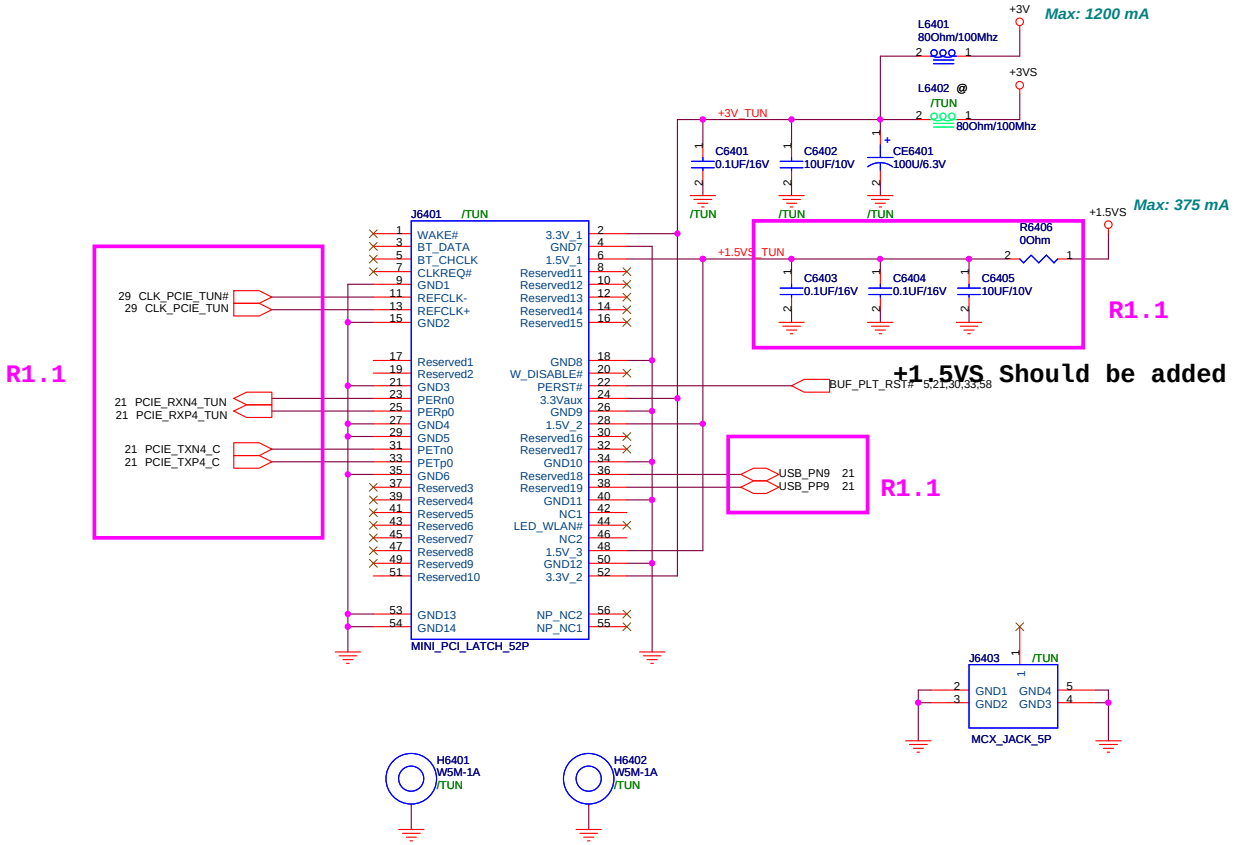
ASUSTeK COMPUTER INC. NB1	Title : BT_Bluetooth	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 61 of 96	



ASUSTeK COMPUTER INC. NB1	Title : TPM_TPM 1.2	
	Engineer:	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 62 of 96	

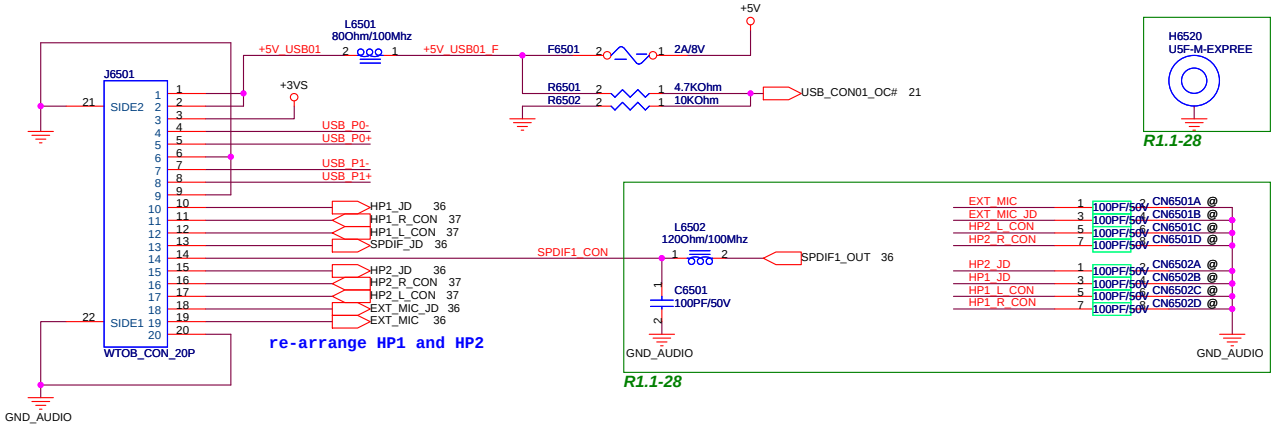


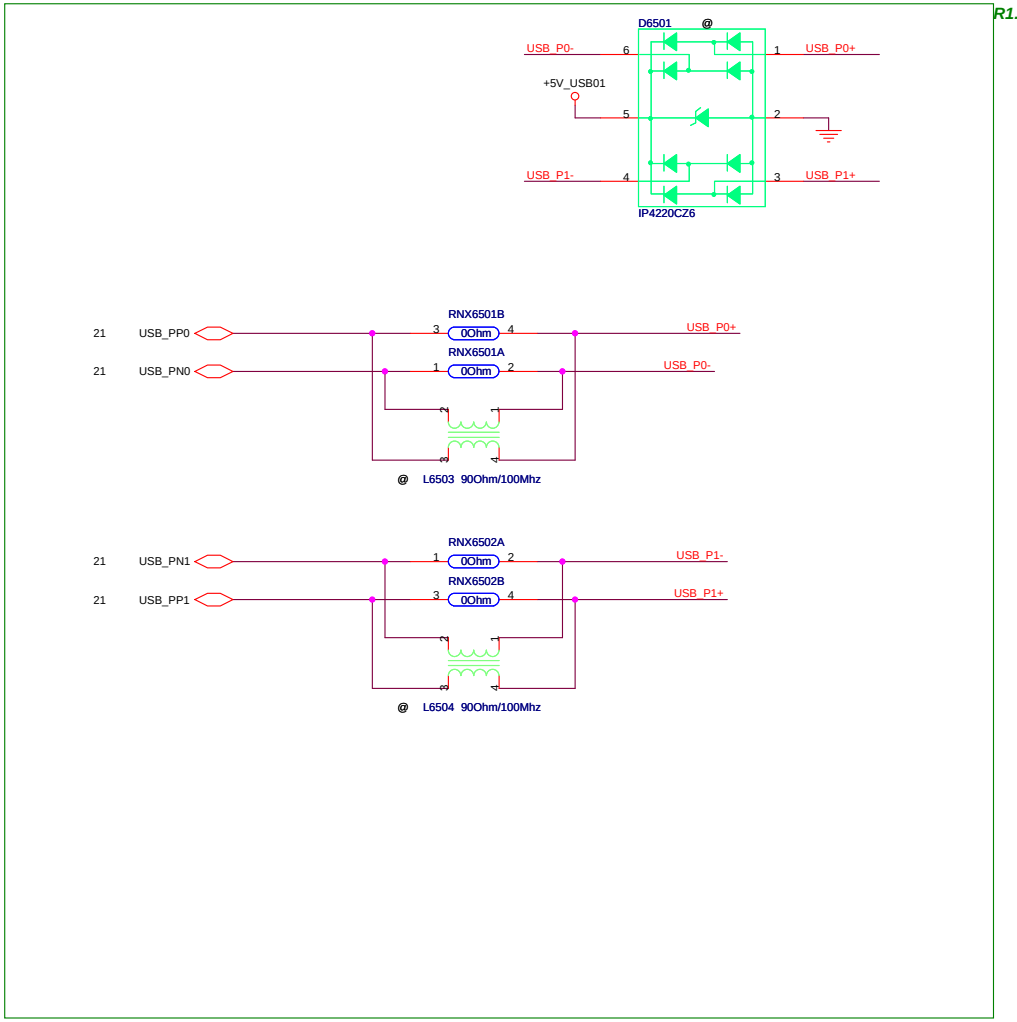
ASUSTeK COMPUTER INC. NB1	Title : FP_Fingerprint Conn.	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 63 of 96	



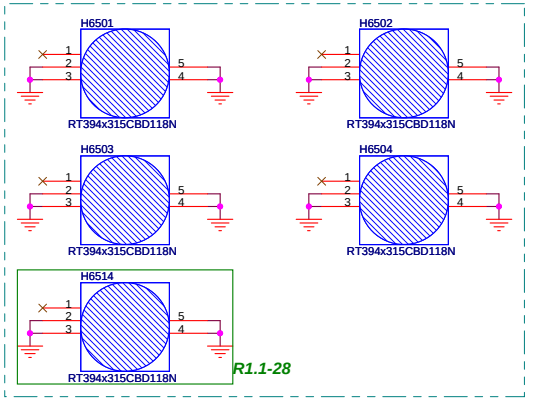
ASUSTeK COMPUTER INC. NB1	Title : TUN_TV Tuner	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 64 of 96	

Main Board

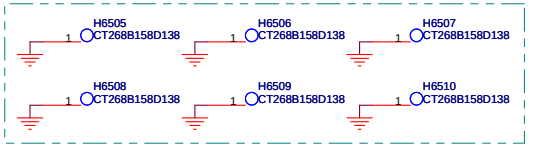




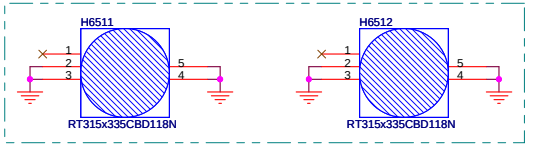
Screw Hole A



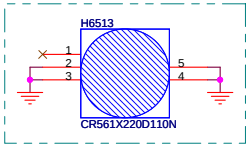
Screw Hole B



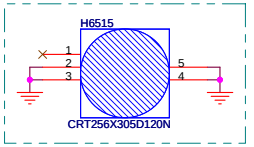
Screw Hole C



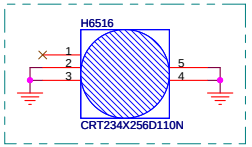
Screw Hole F



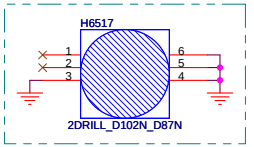
Screw Hole H



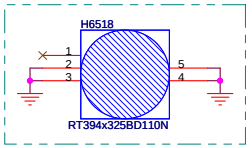
Screw Hole I



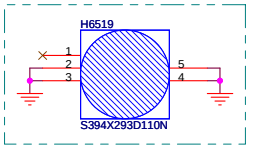
Screw Hole J



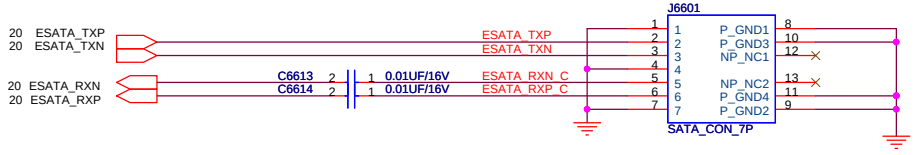
Screw Hole K



Screw Hole L



ASUSTeK COMPUTER INC. NB1	Title : ME_Conn & Screw Holes	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Tuesday, April 15, 2008	Sheet 65 of 96	



ASUS	Title : E-SATA	
	Engineer:	
Size: Custom	Project Name	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 66 of 96	

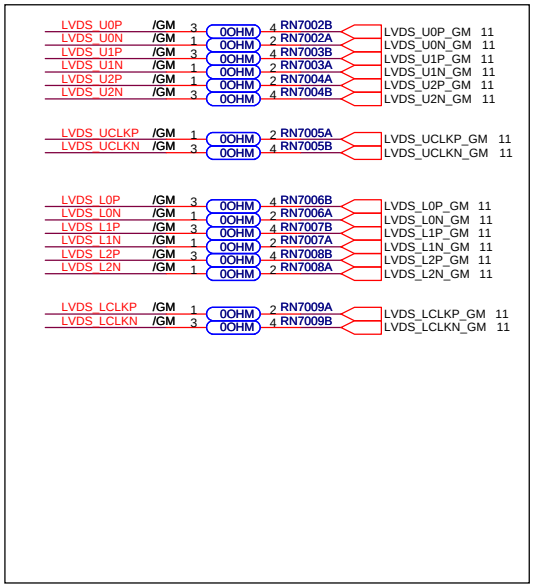
Main Board

ASUSTeK COMPUTER INC. NB1	Title : PCI_WWAN		
	Engineer: John Hung		
Size: Custom	Project Name: M50Vm		Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 67 of 96		

Title :	
Engineer:	
Size: A	Project Name:
Rev: 1.0	
Date: Wednesday, February 13, 2008	Sheet 68 of 96

Title :	
Engineer:	
Size: A	Project Name
Rev: 1.0	
Date: Wednesday, February 13, 2008	Sheet 69 of 96

RESISTERS CLOSE TO MXM



CON7001A

DVI
- DVI_A_TX0 / DVI_A_TX0#
- DVI_A_TX1 / DVI_A_TX1#
- DVI_A_TX2 / DVI_A_TX2#
- DVI_A_CLK / DVI_A_CLK#
- DVI_A_HPD / DVI_B_HPD/GND — 48 HDMI_DETECT
- DDCB_CLK / DDCB_DAT — 45 DDC2BC_PEG
- DDCA_CLK / DDCA_DAT — 45 DDC2BD_PEG

CRT DDC

VGA
- VGA_BLU — 45 CRT_BLUE
- VGA_RED — 45 CRT_RED
- VGA_GRN — 45 CRT_GREEN
- VGA_HSYNC — 45 CRT_HSYNC
- VGA_VSYNC — 45 CRT_VSYNC

LVDS
- LVDS_PPEN — 46 LCD_VDD_EN_PEG
- LVDS_BLEN — 46 LCD_BACKEN_PEG
- LVDS_BL_BRGHT
- LVDS_UTX0 / LVDS_UTX0# — 46 LVDS_L0P / 46 LVDS_L0N
- LVDS_UTX1 / LVDS_UTX1# — 46 LVDS_L1P / 46 LVDS_L1N
- LVDS_UTX2 / LVDS_UTX2# — 46 LVDS_L2P / 46 LVDS_L2N
- LVDS_UTX3 / LVDS_UTX3#
- LVDS_UCLK / LVDS_UCLK# — 46 LVDS_LCLKP / 46 LVDS_LCLKN
- LVDS_LTX0 / LVDS_LTX0# — 46 LVDS_U0P / 46 LVDS_U0N
- LVDS_LTX1 / LVDS_LTX1# — 46 LVDS_U1P / 46 LVDS_U1N
- LVDS_LTX2 / LVDS_LTX2# — 46 LVDS_U2P / 46 LVDS_U2N
- LVDS_LTX3 / LVDS_LTX3#
- LVDS_LCLK / LVDS_LCLK# — 46 LVDS_UCLKP / 46 LVDS_UCLKN

R1.1 SWAP LVDS Channel A B

Reserve to GDDR3 sequence

IGP
- +0.9VS
- IGP_UTX0 / IGP_UTX0#
- IGP_UTX1 / IGP_UTX1#
- IGP_UTX2 / IGP_UTX2# — 36 SPDIF2_OUT; 20 ACZ_RST#_VGA; 20 ACZ_SDOUT#_VGA; 20 ACZ_SDIN2_VGA
- IGP_UCLK / IGP_UCLK# — 20 ACZ_SYNC_VGA; 20 ACZ_BCLK_VGA

HDMI
- IGP_LTX0/DVI_B_TX0 / IGP_LTX0#/DVI_B_TX0# — 48 VGA_HDMI_TX3+ / 48 VGA_HDMI_TX3-
- IGP_LTX1/DVI_B_TX1 / IGP_LTX1#/DVI_B_TX1# — 48 VGA_HDMI_TX4+ / 48 VGA_HDMI_TX4-
- IGP_LTX2/DVI_B_TX2 / IGP_LTX2#/DVI_B_TX2# — 48 VGA_HDMI_TX5+ / 48 VGA_HDMI_TX5-
- IGP_LCLK/DVI_B_CLK / IGP_LCLK#/DVI_B_CLK# — 48 VGA_HDMI_CLKB+ / 48 VGA_HDMI_CLKB-

TV-OUT
- TV_Y/HDTV_Y/TV_CVBS
- TV_C/HDTV_Pr
- TV_CVBS/HDTV_Pb

LVDS DDC

SMBUS
- DDCC_CLK / DDCC_DAT — 46 EDID_CLK_PEG / 46 EDID_DATA_PEG
- SMB_CLK / SMB_DAT — 30,50 SMB1_CLK / 30,50 SMB1_DAT

RN7001A 0OHM; RN7001B 0OHM

thermal

MXM_230P

B TO B : Height = 7mm

PEX
- PEX_TX0 / PEX_TX0# — PCIEG_RXP0 / PCIEG_RXN0 — PCIENB_RXP0 / PCIENB_RXN0
- PEX_TX1 / PEX_TX1# — PCIEG_RXP1 / PCIEG_RXN1 — PCIENB_RXP1 / PCIENB_RXN1
- PEX_TX2 / PEX_TX2# — PCIEG_RXP2 / PCIEG_RXN2 — PCIENB_RXP2 / PCIENB_RXN2
- PEX_TX3 / PEX_TX3# — PCIEG_RXP3 / PCIEG_RXN3 — PCIENB_RXP3 / PCIENB_RXN3
- PEX_TX4 / PEX_TX4# — PCIEG_RXP4 / PCIEG_RXN4 — PCIENB_RXP4 / PCIENB_RXN4
- PEX_TX5 / PEX_TX5# — PCIEG_RXP5 / PCIEG_RXN5 — PCIENB_RXP5 / PCIENB_RXN5
- PEX_TX6 / PEX_TX6# — PCIEG_RXP6 / PCIEG_RXN6 — PCIENB_RXP6 / PCIENB_RXN6
- PEX_TX7 / PEX_TX7# — PCIEG_RXP7 / PCIEG_RXN7 — PCIENB_RXP7 / PCIENB_RXN7
- PEX_TX8 / PEX_TX8# — PCIEG_RXP8 / PCIEG_RXN8 — PCIENB_RXP8 / PCIENB_RXN8
- PEX_TX9 / PEX_TX9# — PCIEG_RXP9 / PCIEG_RXN9 — PCIENB_RXP9 / PCIENB_RXN9
- PEX_TX10 / PEX_TX10# — PCIEG_RXP10 / PCIEG_RXN10 — PCIENB_RXP10 / PCIENB_RXN10
- PEX_TX11 / PEX_TX11# — PCIEG_RXP11 / PCIEG_RXN11 — PCIENB_RXP11 / PCIENB_RXN11
- PEX_TX12 / PEX_TX12# — PCIEG_RXP12 / PCIEG_RXN12 — PCIENB_RXP12 / PCIENB_RXN12
- PEX_TX13 / PEX_TX13# — PCIEG_RXP13 / PCIEG_RXN13 — PCIENB_RXP13 / PCIENB_RXN13
- PEX_TX14 / PEX_TX14# — PCIEG_RXP14 / PCIEG_RXN14 — PCIENB_RXP14 / PCIENB_RXN14
- PEX_TX15 / PEX_TX15# — PCIEG_RXP15 / PCIEG_RXN15 — PCIENB_RXP15 / PCIENB_RXN15
- PEX_RX0 / PEX_RX0# — PCIENB_RXP0 / PCIENB_RXN0
- PEX_RX1 / PEX_RX1# — PCIENB_RXP1 / PCIENB_RXN1
- PEX_RX2 / PEX_RX2# — PCIENB_RXP2 / PCIENB_RXN2
- PEX_RX3 / PEX_RX3# — PCIENB_RXP3 / PCIENB_RXN3
- PEX_RX4 / PEX_RX4# — PCIENB_RXP4 / PCIENB_RXN4
- PEX_RX5 / PEX_RX5# — PCIENB_RXP5 / PCIENB_RXN5
- PEX_RX6 / PEX_RX6# — PCIENB_RXP6 / PCIENB_RXN6
- PEX_RX7 / PEX_RX7# — PCIENB_RXP7 / PCIENB_RXN7
- PEX_RX8 / PEX_RX8# — PCIENB_RXP8 / PCIENB_RXN8
- PEX_RX9 / PEX_RX9# — PCIENB_RXP9 / PCIENB_RXN9
- PEX_RX10 / PEX_RX10# — PCIENB_RXP10 / PCIENB_RXN10
- PEX_RX11 / PEX_RX11# — PCIENB_RXP11 / PCIENB_RXN11
- PEX_RX12 / PEX_RX12# — PCIENB_RXP12 / PCIENB_RXN12
- PEX_RX13 / PEX_RX13# — PCIENB_RXP13 / PCIENB_RXN13
- PEX_RX14 / PEX_RX14# — PCIENB_RXP14 / PCIENB_RXN14
- PEX_RX15 / PEX_RX15# — PCIENB_RXP15 / PCIENB_RXN15
- CLK_REQ# / PEX_RST# — R7014 @ 0Ohm; R7015 @ 0Ohm — GPU_RST# 22; BUF_PLT_RST# 5,21,30,33,58
- PEX_REFCLK — CLK_PCIE_PEG# 29
- PEX_REFCLK# — CLK_PCIE_PEG 29

OTHER
- THERM#
- PRSNT1# — PRSNT2#
- PRSNT2# — PWR_OK_VGA 92
- RUNPWROK — BUF_PLT_RST#
- NP_NC1
- NP_NC2
- GND_1
- GND_2

VGA_OVT# — Q7002 2N7002@ — R7001 @ 0Ohm — FORCE_OFF# 81,92; VGA_ALERT# 30

LCD_VDD_EN_PEG 0Ohm /GM R7005 — L_VDDEN 11
LCD_BACKEN_PEG 0Ohm /GM R7006 — L_BKLTEN 11
EDID_DATA_PEG 0Ohm /GM R7008 — EDID_DAT 11
EDID_CLK_PEG 0Ohm /GM R7009 — EDID_CLK 11

MXM Heatsink Stand-Off
- H7001 /PM CT217B67D47
- H7002 /PM CT217B67D47
- H7003 /PM U5F-M-EXPREE
- H7004 /PM U5F-M-EXPREE

CON7001B

- AC_BAT_SYS — max 3A?
- +1.5VS — 3.15A — max 3.5A — PWR_SRC1 / PWR_SRC2 / PWR_SRC3 / PWR_SRC4 / PWR_SRC5 / PWR_SRC6 / PWR_SRC7 / PWR_SRC8
- 1V8RUN_1 / 1V8RUN_2 / 1V8RUN_3 / 1V8RUN_4 / 1V8RUN_5 / 1V8RUN_6 / 1V8RUN_7
- +3VS — 850mA — max 1.5A
- 3V3RUN_1 / 3V3RUN_2 / 3V3RUN_3
- 5VRUN / 2V5RUN
- +5V / +12VS — RSVD1 / RSVD2 / RSVD3 / RSVD4 / RSVD5 / RSVD6 / AC/BATT#
- +1.8VS — SUSB# PWR VGA
- GND1 … GND66

MXM_230P

HDMI DDC
- 48 HDMI_DDCCLK
- 48 HDMI_DDCDAT
- 29 CLK_ATI27SS
- 29 CLK_ATI27

+3VSUS
- R7002 100KOhm
- U7001 NC7SZ14P5_NL (NC, A, GND, Vcc, Y) — SUSB# PWR VGA
- R7003 10KOhm — 81,82,83,91,93 SUSB#_PWR
- Q7001 PMBS3904
- +12VSUS — R7004 100KOhm — PRSNT2# — ATI : Low / NV : High
- Q7003 2N7002
- C7001 0.1UF/16V

ASUSTeK COMPUTER INC. NB6	Title : VGA CON	
	Engineer: Raphael_Chen	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 70 of 96	

Title :	
Engineer:	
Size: A	Project Name
Rev: 1.1	
Date: Wednesday, February 13, 2008	Sheet 71 of 96

Title :	
Engineer:	
Size: A	Project Name
Rev: 1.1	
Date: Wednesday, February 13, 2008	Sheet 72 of 96

ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.1
Date: Wednesday, February 13, 2008	Sheet 73 of 96	

Title :	
Engineer:	
Size: A	Project Name
Rev: 1.1	
Date: Wednesday, February 13, 2008	Sheet 74 of 96

Title :	
Engineer:	
Size: A	Project Name
Rev: 1.1	
Date: Wednesday, February 13, 2008	Sheet 75 of 96

Title :	
Engineer:	
Size: A	Project Name
Rev: 1.1	
Date: Wednesday, February 13, 2008	Sheet 76 of 96

Title :	
Engineer:	
Size: A	Project Name
Rev: 1.1	
Date: Wednesday, February 13, 2008	Sheet 77 of 96

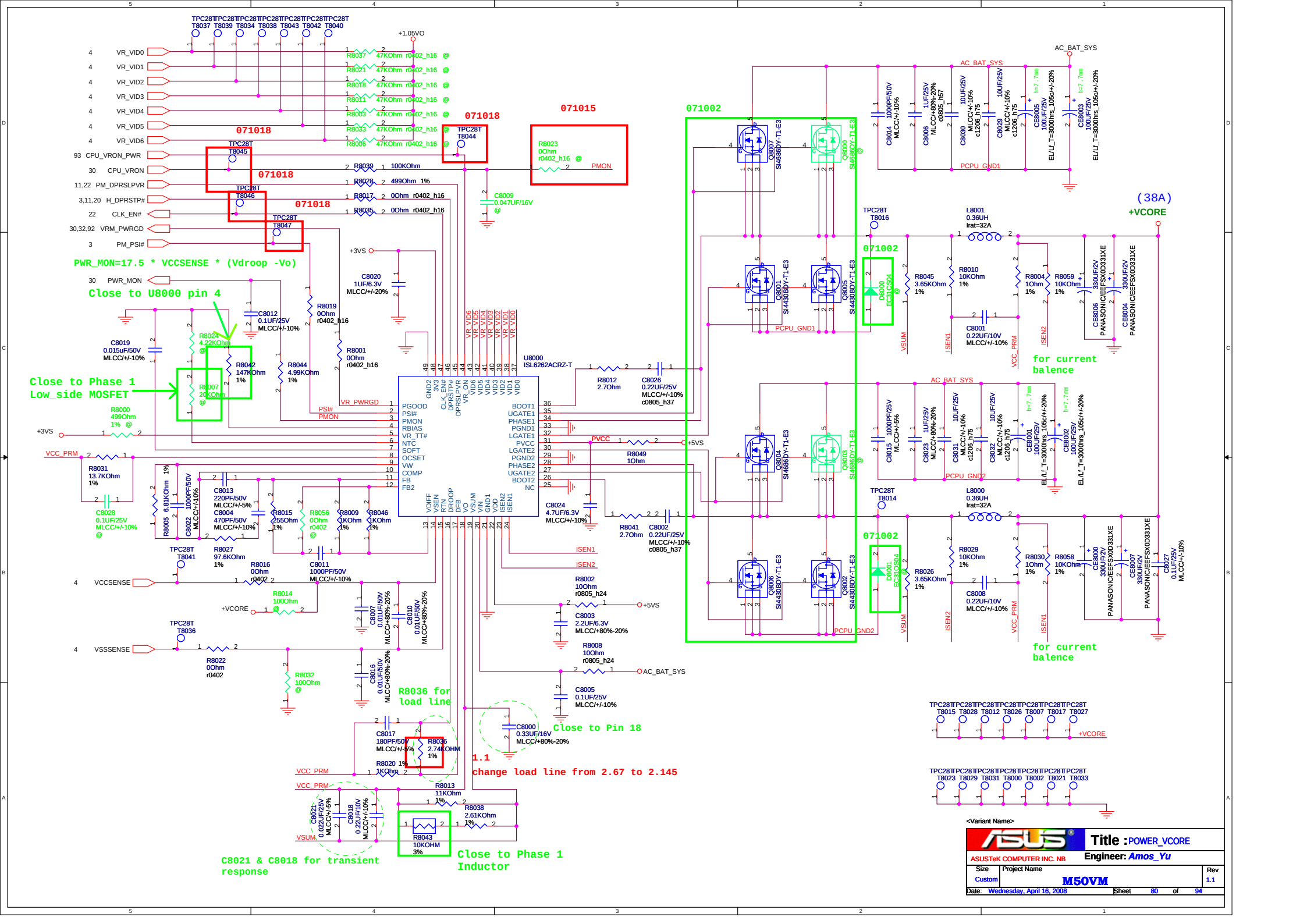
Title :	
Engineer:	
Size: A	Project Name
Rev: 1.1	
Date: Wednesday, February 13, 2008	Sheet 78 of 96

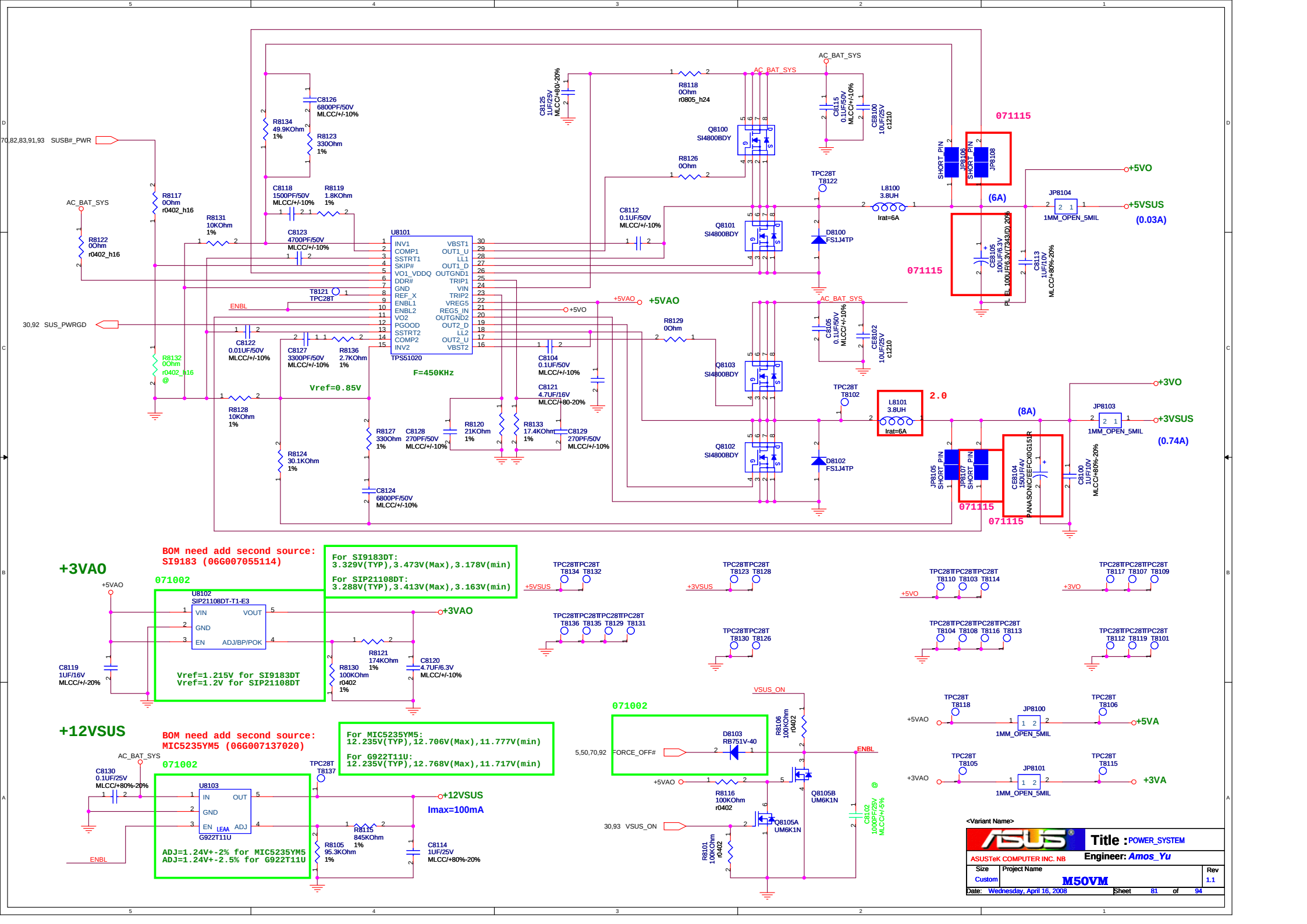
History

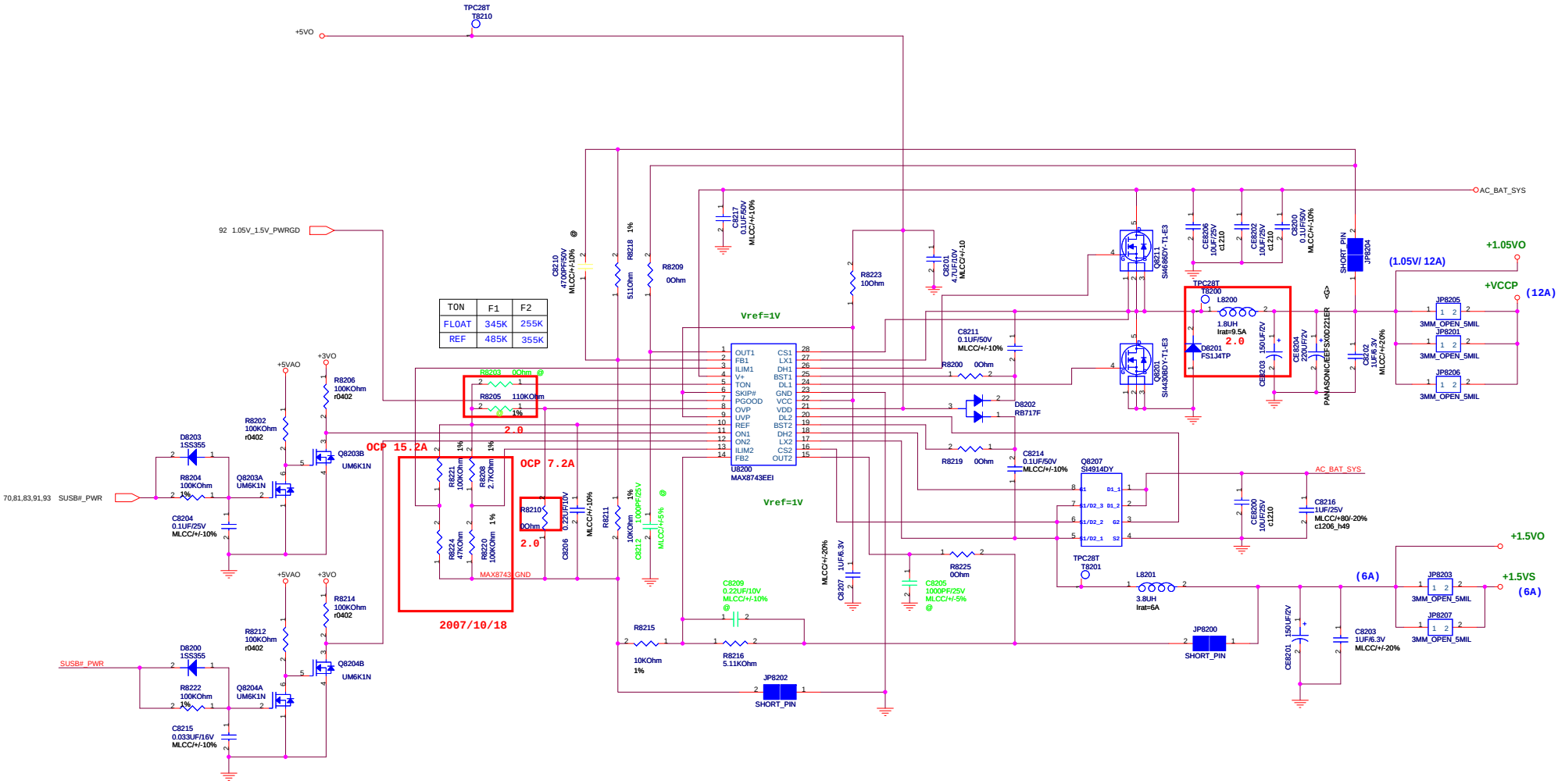
20070820 R1.01:

1. RTL8111C first release.
2. Remove RTL8111B co-lay circuit.
3. Change the L3404 part-name for the same part reference.

ASUSTeK COMPUTER INC	Title : History	
	Engineer:	
Size: Custom	Project Name	Rev: 1.01
Date: Wednesday, February 13, 2008	Sheet 79 of 96	


PWR_MON=17.5 * VCCSENSE * (Vdroop -Vo)
Close to U8000 pin 4
Close to Phase 1 Low_side MOSFET
U8000 ISL6262ACRZ-T
for current balence
for current balence
R8036 for load line
Close to Pin 18
1.1
change load line from 2.67 to 2.145
C8021 & C8018 for transient response
Close to Phase 1 Inductor
(38A)
+VCORE
Title : POWER_VCORE
ASUSTeK COMPUTER INC. NB
Engineer: Amos_Yu
M50VM
Date: Wednesday, April 16, 2008
Sheet 80 of 94


70,82,83,91,93 SUSB#_PWR
30,92 SUS_PWRGD
AC_BAT_SYS
ENBL
U8101
TPS51020
F=450KHz
Vref=0.85V
+5VAO
+5VO
+5VAO
+3VO
+3VSUS
(0.03A)
(0.74A)
(6A)
(8A)
2.0
071115
+3VAO
BOM need add second source:
SI9183 (06G007055114)
071002
U8102
SIP21108DT-T1-E3
For SI9183DT:
3.329V(TYP),3.473V(Max),3.178V(min)
For SIP21108DT:
3.288V(TYP),3.413V(Max),3.163V(min)
Vref=1.215V for SI9183DT
Vref=1.2V for SIP21108DT
+12VSUS
BOM need add second source:
MIC5235YM5 (06G007137020)
U8103
G922T11U
For MIC5235YM5:
12.235V(TYP),12.706V(Max),11.777V(min)
For G922T11U:
12.235V(TYP),12.768V(Max),11.717V(min)
Imax=100mA
ADJ=1.24V+-2% for MIC5235YM5
ADJ=1.24V+-2.5% for G922T11U
VSUS_ON
5,50,70,92 FORCE_OFF#
30,93 VSUS_ON
+5VA
1MM_OPEN_5MIL
M50VM
ASUSTeK COMPUTER INC. NB
Engineer: Amos_Yu
Project Name
Rev
1.1
Date: Wednesday, April 16, 2008
Sheet 81 of 94



<Variant Name>

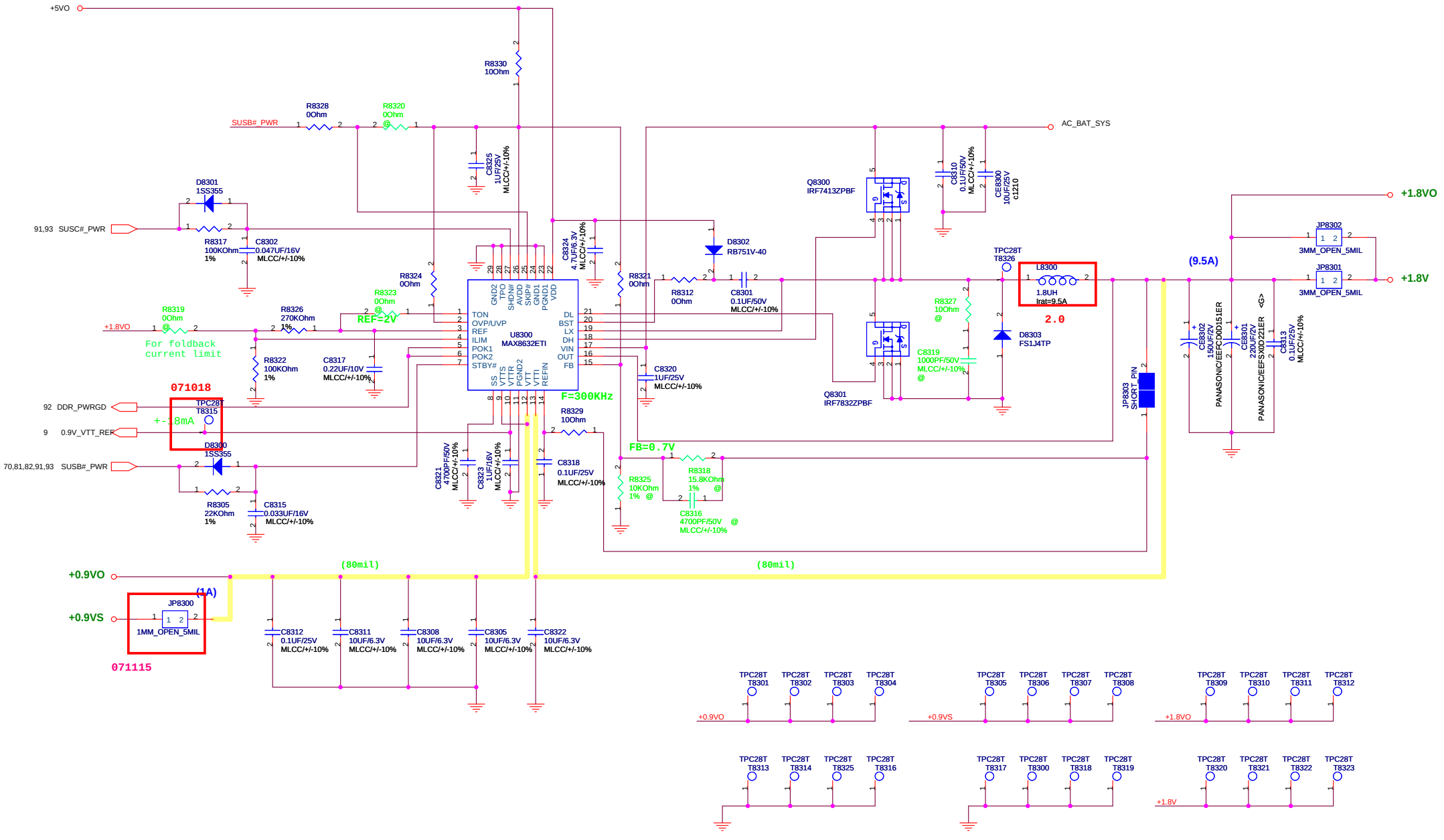
ASUSTeK COMPUTER INC. NB

Title : POWER_VGA_CORE & RAM

Engineer: Amos_Yu

Size	Project Name	Rev
C	M50VM	1.1

Date: Wednesday, April 16, 2008 Sheet 82 of 94



<Variant Name>

Title : POWER_I/O_DDR & VTT

ASUSTeK COMPUTER INC. NB

Engineer: Amos_Yu

Size	Project Name	Rev
Custom	M50VM	1.1

Date: Wednesday, April 16, 2008 Sheet 83 of 94

071002

<Variant Name>

Title : POWER_I/O_ +2.5VS

ASUSTeK COMPUTER INC. NB

Engineer: Amos_Yu

Size	Project Name	Rev
Custom	M50VM	1.0

Date: Wednesday, April 16, 2008 Sheet 84 of 94

071002

<Variant Name>

Title : POWER_I/O_1.5VS & 1.05VS

ASUSTeK COMPUTER INC. NB

Engineer: Amos_Yu

Size	Project Name	Rev
Custom	M50VM	1.0

Date: Wednesday, April 16, 2008 Sheet 85 of 94

071002

<Variant Name>

Title : N/A

ASUSTeK COMPUTER INC. NB

Engineer: Amos_Yu

Size	Project Name	Rev
B	M50VM	1.0

Date: Wednesday, April 16, 2008 Sheet 86 of 94

071002

<Variant Name>

071002

ASUSTeK COMPUTER INC. NB

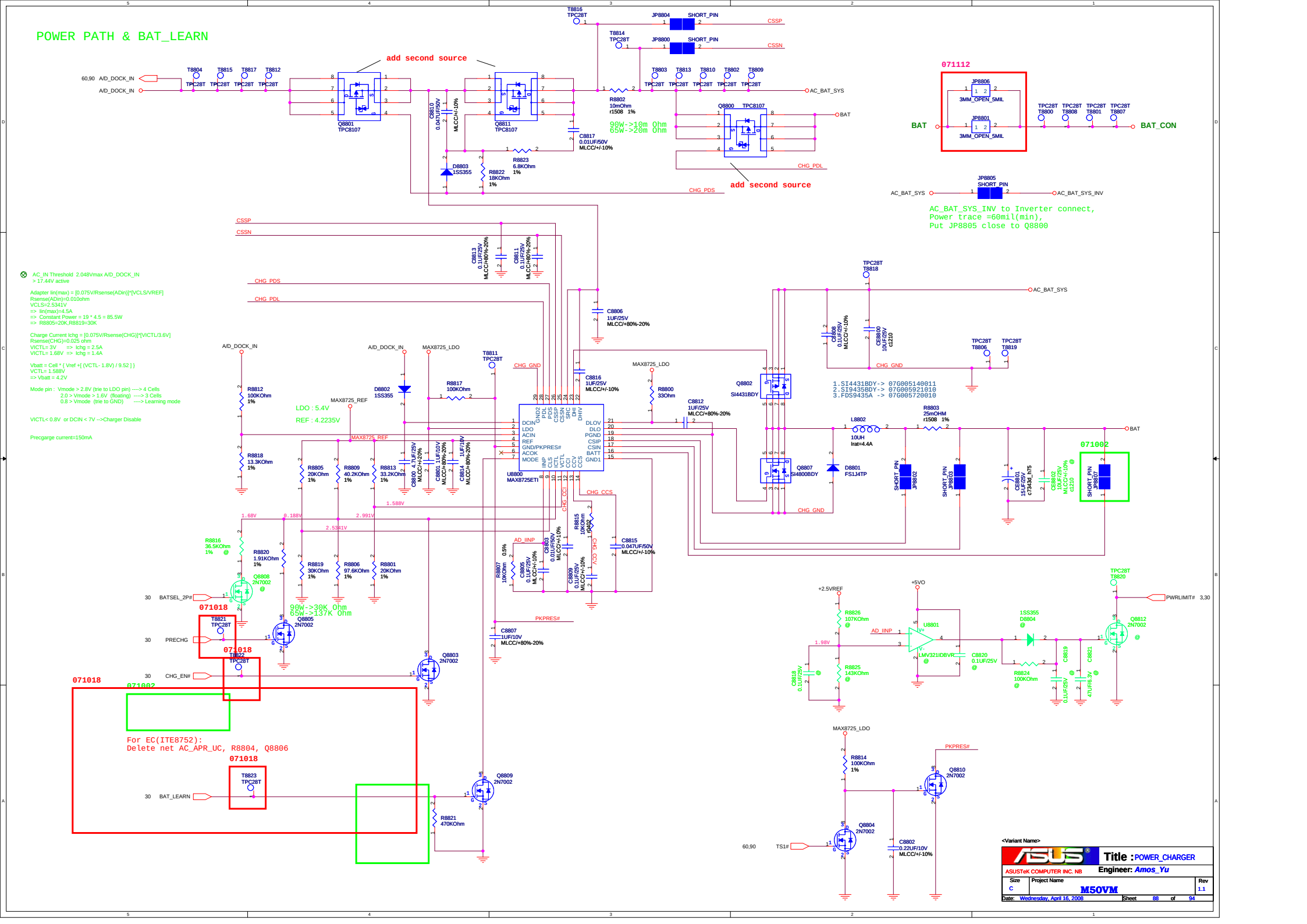
Title : POWER_SHUTDOWN#

Engineer: Amos_Yu

Size	Project Name	Rev
Custom	M50VM	1.0

Date: Wednesday, April 16, 2008 Sheet 87 of 94

POWER PATH & BAT_LEARN



<variant_name>

ASUSTeK COMPUTER INC. NB	Title : POWER_CHARGER	
	Engineer: Amos_Yu	
Size: C	Project Name: M50VM	Rev: 1.1
Date: Wednesday, April 16, 2008	Sheet 88 of 94	

071002

<Variant Name>

Title : N/A

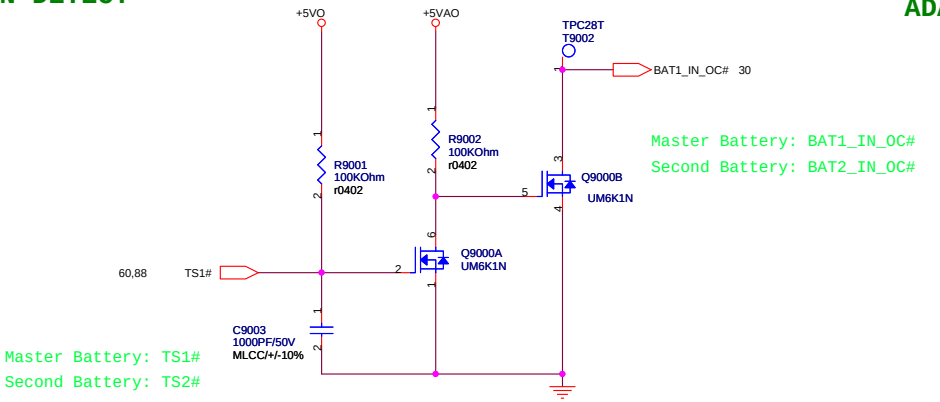
ASUSTeK COMPUTER INC. NB

Engineer: Amos_Yu

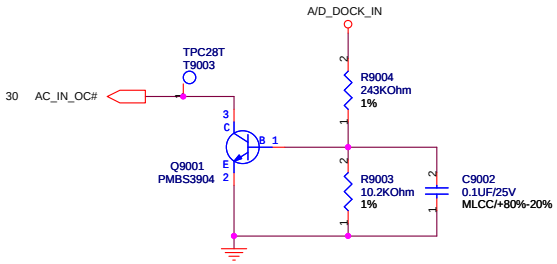
Size	Project Name	Rev
Custom	M50VM	1.0

Date: Wednesday, April 16, 2008 Sheet 89 of 94

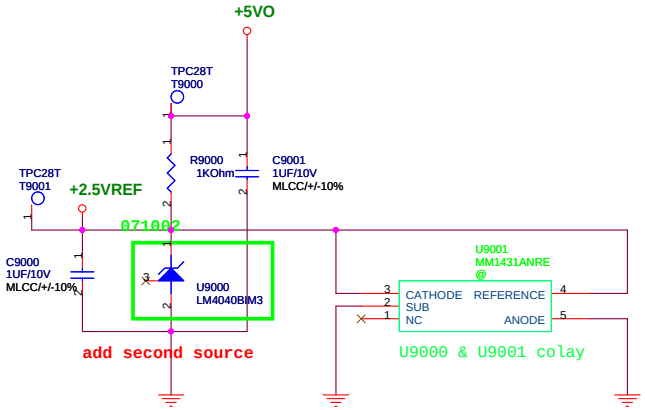
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF



U9000 06G006002412 (tolerence:0.2%) add second source 06G006002610 (tolerence:1%) and 06G006002414(tolerence:1%)

<Variant Name>

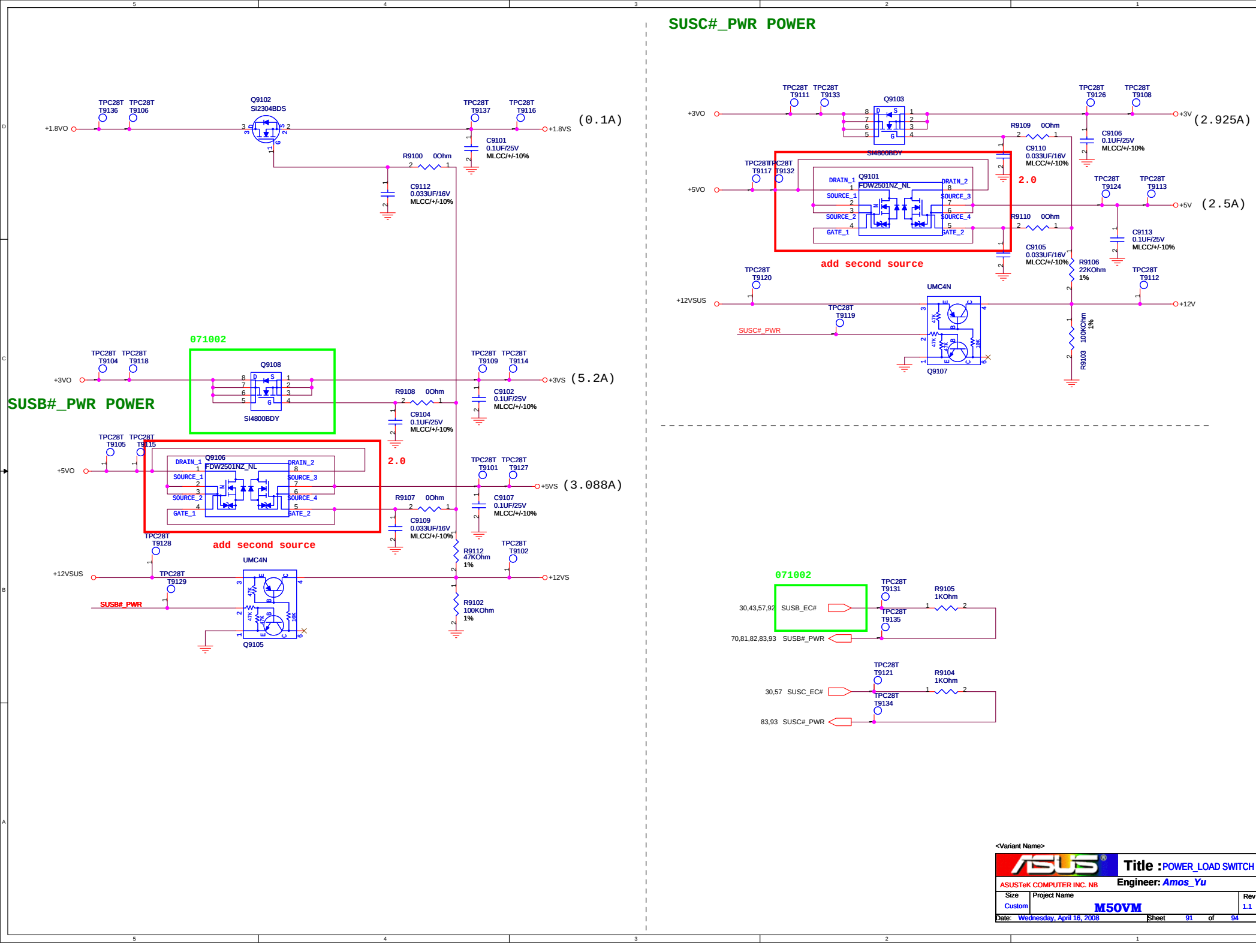
Title : POWER_DETECT

ASUSTeK COMPUTER INC. NB

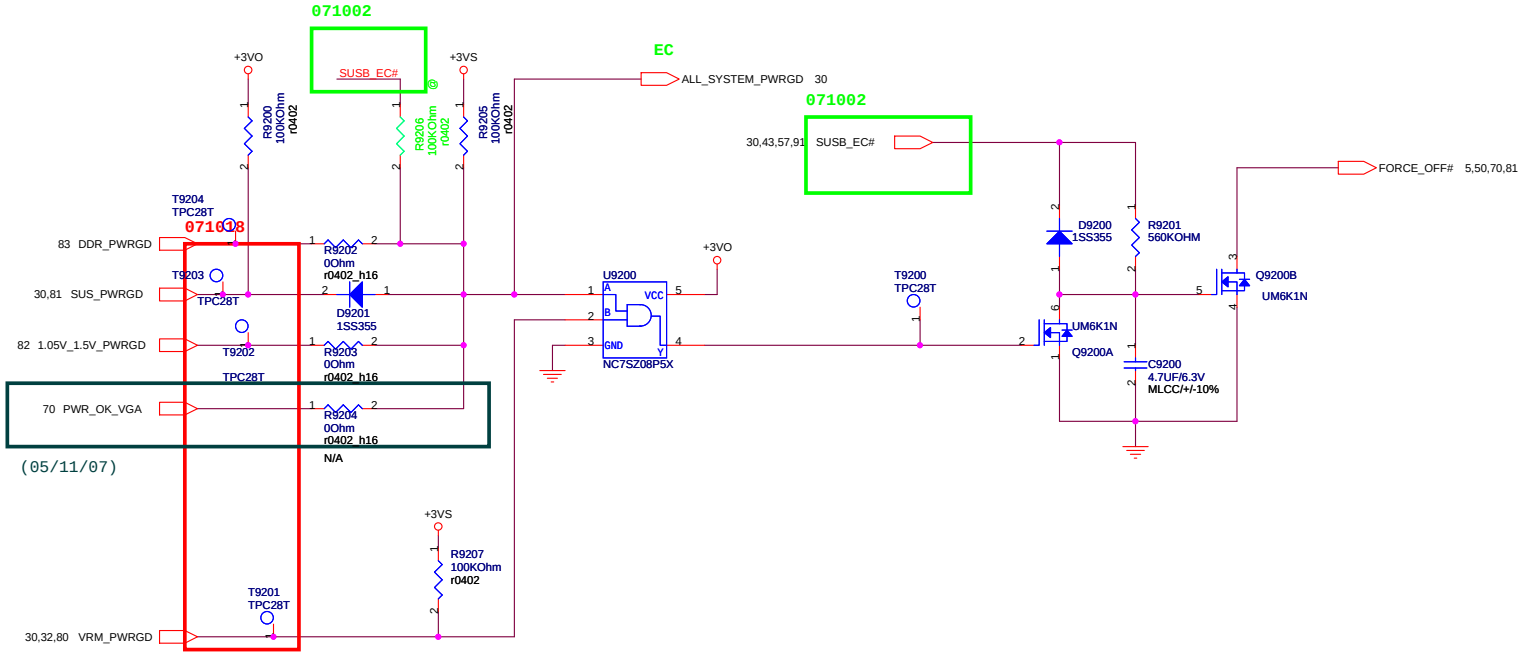
Engineer: Amos_Yu

Size	Project Name	Rev
Custom	M50VM	1.1

Date: Wednesday, April 16, 2008 Sheet 90 of 94


SUSB#_PWR POWER
SUSC#_PWR POWER
071002
add second source
Q9102
SI2304BDS
Q9108
SI4800BDY
Q9106
FDW2501NZ_NL
Q9105
Q9103
Q9101
Q9107
UMC4N
+1.8VO
+1.8VS
(0.1A)
+3VO
+3VS
(5.2A)
+5VO
+5VS
(3.088A)
+3V
(2.925A)
+5V
(2.5A)
+12VSUS
+12VS
+12V
SUSB# PWR
SUSC# PWR
2.0
R9100 0Ohm
R9108 0Ohm
R9107 0Ohm
R9109 0Ohm
R9110 0Ohm
R9112 47KOhm 1%
R9102 100KOhm 1%
R9103 100KOhm 1%
R9106 22KOhm 1%
C9101 0.1UF/25V MLCC/+/-10%
C9112 0.033UF/16V MLCC/+/-10%
C9104 0.1UF/25V MLCC/+/-10%
C9102 0.1UF/25V MLCC/+/-10%
C9109 0.033UF/16V MLCC/+/-10%
C9107 0.1UF/25V MLCC/+/-10%
C9110 0.033UF/16V MLCC/+/-10%
C9106 0.1UF/25V MLCC/+/-10%
C9105 0.033UF/16V MLCC/+/-10%
C9113 0.1UF/25V MLCC/+/-10%
30,43,57,92 SUSB_EC#
70,81,82,83,93 SUSB#_PWR
30,57 SUSC_EC#
83,93 SUSC#_PWR
R9105 1KOhm
R9104 1KOhm
<Variant Name>
Title : POWER_LOAD SWITCH
ASUSTeK COMPUTER INC. NB
Engineer: Amos_Yu
Size Custom
Project Name M50VM
Rev 1.1
Date: Wednesday, April 16, 2008
Sheet 91 of 94

POWER GOOD DETECTER



<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_PROTECT

Engineer: Amos_Yu

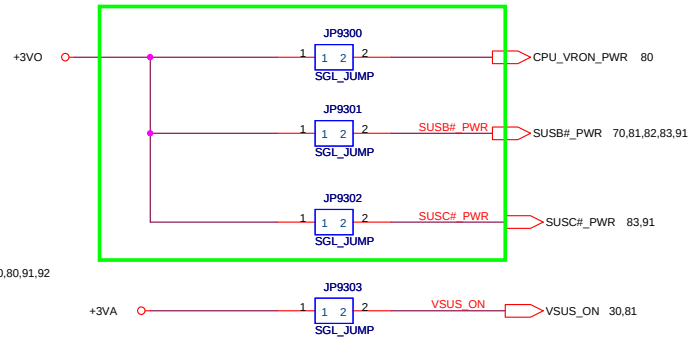
Size	Project Name	Rev
Custom	M50VM	1.1

Date: Wednesday, April 16, 2008 Sheet 92 of 94

AC_BAT_SYS	AC_BAT_SYS	70,80,81,82,83,88
BAT	BAT	88
BAT_CON	BAT_CON	60,88
+2.5VREF	+2.5VREF	88,90
+3VA	+3VA	20,30,56,57,81
+5VAO	+5VAO	81,82,90
+5VO	+5VO	81,82,83,88,90,91
+5VSUS	+5VSUS	23,31,81
+5V	+5V	36,46,52,56,57,63,65,70,91
+5VS	+5VS	23,31,37,45,48,50,51,56,57,63,80,91
+3VO	+3VO	81,82,91,92
+3VSUS	+3VSUS	20,21,22,23,30,33,37,46,56,70,81
+3V	+3V	21,35,43,53,57,61,64,91
+3VS	+3VS	3,7,8,11,14,15,20,21,22,23,24,25,29,30,32,33,36,37,40,41,42,43,44,45,46,48,50,51,53,56,57,63,64,65,70,80,91,92
+12VSUS	+12VSUS	70,81,91
+12V	+12V	37,91
+12VS	+12VS	24,42,46,70,91
+1.8VO	+1.8VO	83,91
+1.8V	+1.8V	7,8,9,11,13,57,83
+1.8VS	+1.8VS	14,20,38,57,70,91
+0.9VS	+0.9VS	9,57,70,83
+0.9VO	+0.9VO	83
+1.05VO	+1.05VO	80,82
+VCCP	+VCCP	5,10,11,13,14,20,23,29,57,82
+1.5VO	+1.5VO	82
+1.5VS	+1.5VS	4,14,20,23,43,53,57,64,70,82
+VCORE	+VCORE	4,5,80

FOR POWER TEST

1017



<Variant Name>

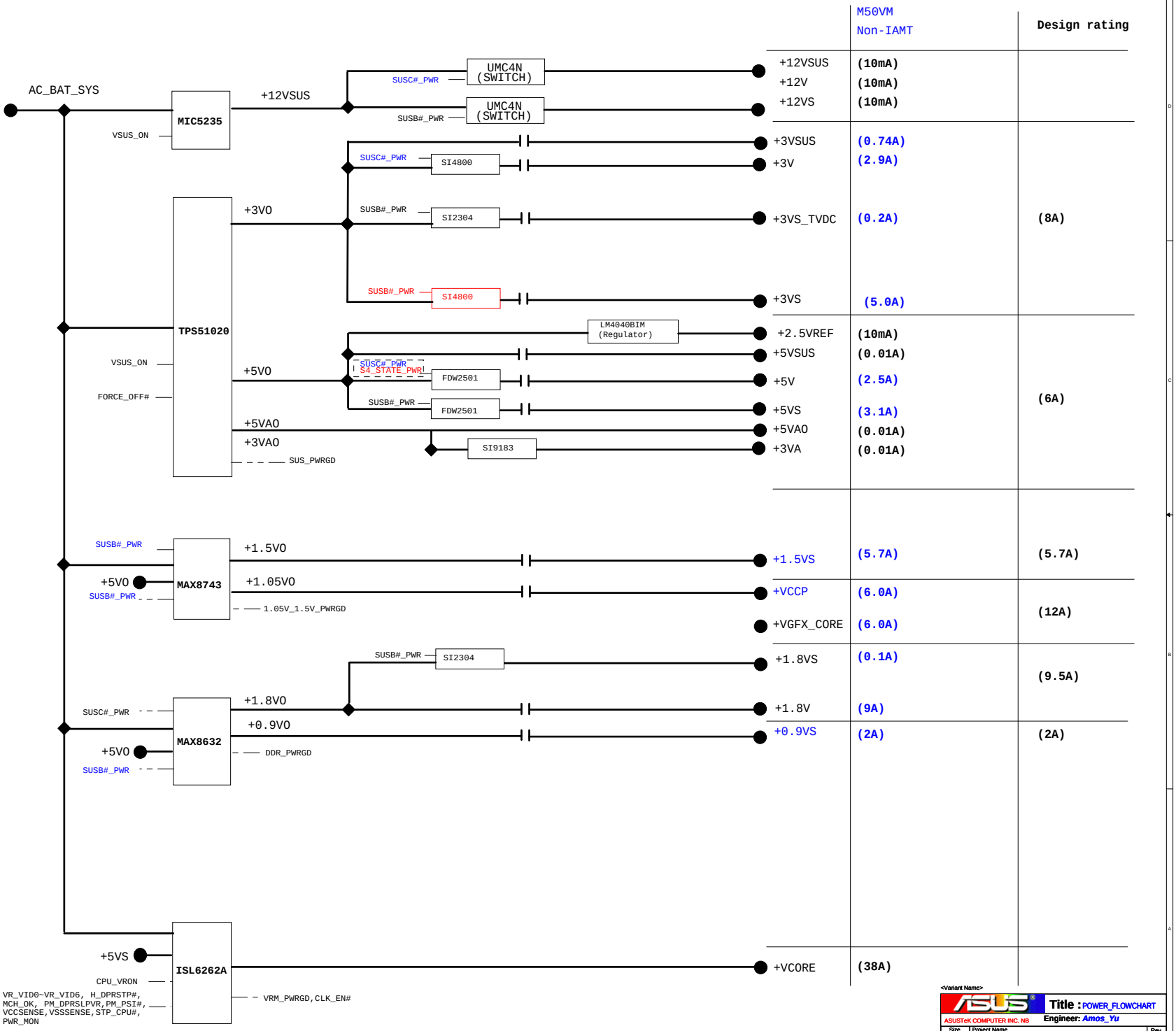
ASUSTeK COMPUTER INC. NB

Title : POWER_SIGNAL

Engineer: Amos_Yu

Size	Project Name	Rev
Custom	M50VM	1.1

Date: Wednesday, April 16, 2008 Sheet 93 of 94



	M50VM Non-IAMT	Design rating
+12VSUS	(10mA)	
+12V	(10mA)	
+12VS	(10mA)	
+3VSUS	(0.74A)	
+3V	(2.9A)	
+3VS_TVDC	(0.2A)	(8A)
+3VS	(5.0A)	
+2.5VREF	(10mA)	
+5VSUS	(0.01A)	
+5V	(2.5A)	
+5VS	(3.1A)	(6A)
+5VA0	(0.01A)	
+3VA	(0.01A)	
+1.5VS	(5.7A)	(5.7A)
+VCCP	(6.0A)	
+VGFX_CORE	(6.0A)	(12A)
+1.8VS	(0.1A)	
+1.8V	(9A)	(9.5A)
+0.9VS	(2A)	(2A)
+VCORE	(38A)	

<Variant Name>

ASUSTeK COMPUTER INC. NB

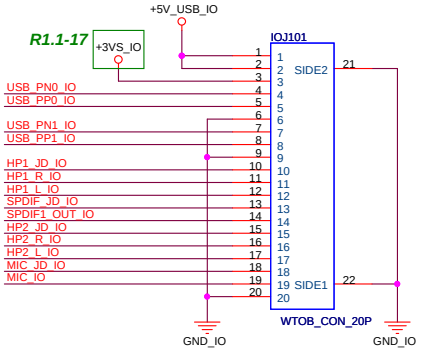
Title : POWER_FLOWCHART

Engineer: Amos_Yu

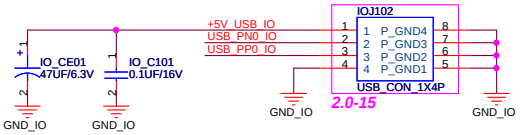
Size	Project Name	Rev
Custom	M50VM	1.1

Date: Wednesday, April 16, 2008 Sheet 94 of 94

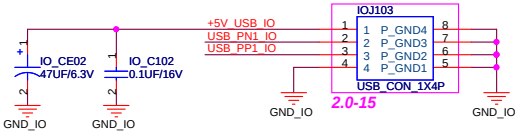
I/O Board

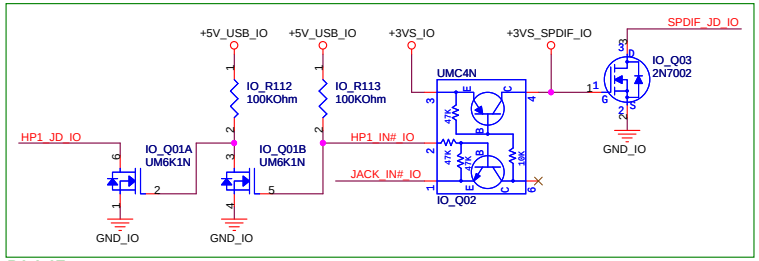


USB Port 0

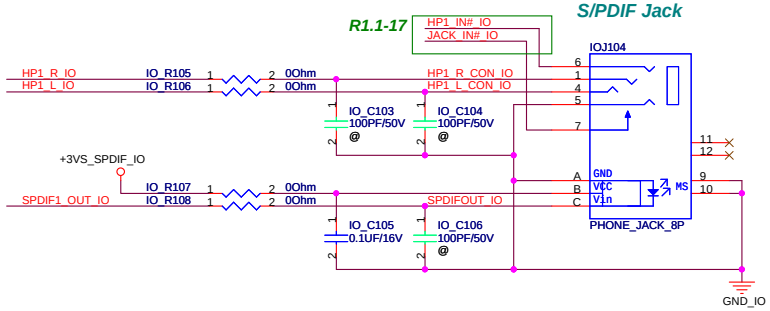


USB Port 1

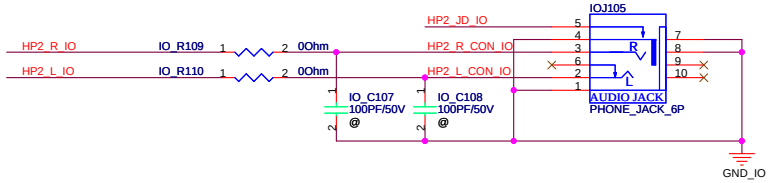




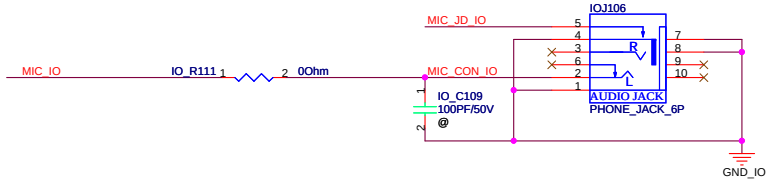
Headphone & S/PDIF Jack



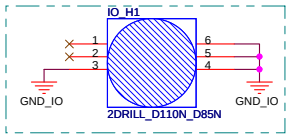
Headphone Jack



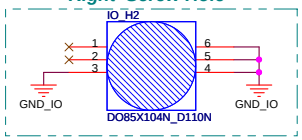
MIC In Jack



Left Screw Hole



Right Screw Hole



ASUSTeK COMPUTER INC. NB1	Title : USB & Audio Jack	
	Engineer: Wenchi_Shen	
Size: Custom	Project Name: M50Vm	Rev: 2.0
Date: Tuesday, April 15, 2008	Sheet 95 of 96	

Rev	Date	Description
R1.0		First Release!
R1.1 Green Block		** Merge IO board into main board PCB. Page 95. 01.Remove VR_VID[6:0] testing series 0 0hm. Page 4. 02.Change 6pcs +VCORE capacitors to No-Stuff for cost down. Page 5. 03.Change 3pcs +0.9VS capacitors to No-Stuff for cost down. Page 9. 04.Change N1Sv USB port to follow N2Sv, and modify USB_OC#. Page 21,43,45. 05.PM Request: Change Bluetooth LED tp E-Mail LED. Page 22,56. 06.Follow Intel to change C2304 to 1uF/16V(XR). Page 23. 07.Follow R1E to change R2904 to 270ohm. Page 29. 08.Follow IT8752/8512 EC Common Hardware Pin Assignment v0.005, change GPE7 to INSTANT_ON# and GPG0 to PM_THERM#. Page 30. 09.PM REquest: Remove USB port charger function. Page 30,65. 10.PM change WWAN LED to touch-pad lock LED. Page 30,56. 11.Change IR to 36KHz to meet Vista remote control Min. range requirement. Page 31. 12.Remove testing 2nd CIR design. Page 31. 13.Change X3301 to 49S type for cost down. Page 33. 14.LAN chip version change. Page 33. 15.Audio codec chip change version. Page 36. 16.N1Sv/X55 will not supprot 3G function. Page 36,67. 17.Add S/PDIF & HDMI jack detect by Realtek sugesstion. Page 36,65,70,95. 18.Modify audio de-pop circuit. Page 36,37. 19.Modify LVDS power sequence failed bug. Page 45. 20.Modify LCD abnormal display bug due to LVDS pair mismatch. Page 45,70. 21.Remove HDTV support function. Page 47,70. 22.Remove HDMI EMI filter design. Page 48. 23.X55 need two pwer LEDs. Page 56. 24.PM change WLAN LED to RF LED. Page 56,63. 25.Bluetooth pin define error. Page 61. 26.Remove co-layout sequence logic control circuit. Page 68. 27.ME change parts: J3401,J5102,J6002,J6501. Page 34,51,60,65. 28.EMI modification. Page 34,36,65. 29.Crystal accuracy fine-tune. Page 30.USB droop test fail. Page 65. 31.Remove IO board USB common choke design. Page 95. 32.Speaker fine-tune. Page 37. 33.Cost down for 4-wire PWM fan. Page 50. 34.Cost down: Change RB717F to BAT54AW. Page 37,45,48,56.
R2.0 Pink Block		01.Change +1.25VS_MPLL, +1.25VS_PEGPLL & +1.8V_SM_CK PLL design. Page 15. 02.Add CMOS crack protection circuit. Page 22. 03.Reserve C2337 (10UF/16V) for +5VREF_ICH. Page 23. 04.With EMI RD's confirmation, remove reserved LAN common choke circuit. Page 34. 05.With EMI RD's confirmation, change R3612, R3614, R3615, R3616, R3622, R3624,R3626 to short-pad. Page 36. 06.With EMI RD's confirmation, remove reserved 1394 common choke circuit. Page 41. 07.With EMI RD's confirmation, remove reserved NewCard USB common choke circuit. Page 43. 08.Add NewCard debug card co-layout circuit. Page 44. 09.EMI modification: change reserved common choke circuit from USB port to internal camera port. Page 45. 10.HDMI jack detection modification. Page 48,70. 11.Change FAN capacitors to 10UF. Page 50. 12.Modify X55 power LED design. Page 56.

Rev	Date	Description
		13.With EMI RD's confirmation, remove reserved e-SATA/USB combo port USB common choke circuit. Page 41. 14.Reserve R8023 for shortage issue of ISL6262A. Page 80. 15.QTR USB plug test failed, change USB connector. Page 95.

ASUSTeK COMPUTER INC. NB1

Title : Revision History

Engineer: John Hung

Size	Project Name	Rev
Custom	M50Vm	1.0

Date: Wednesday, February 13, 2008 Sheet 96 of 96