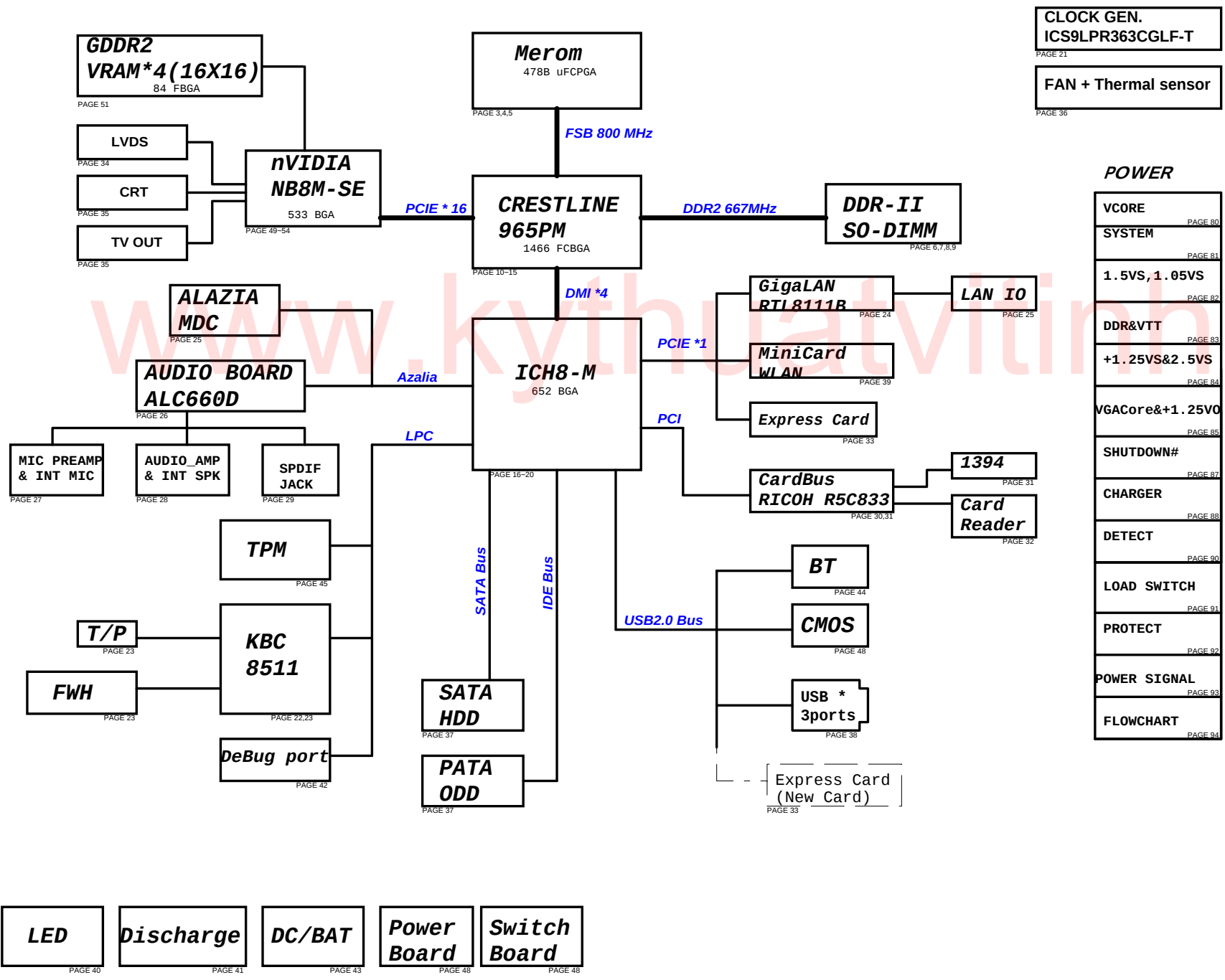


T76S: MEROM/965-PM/ICH8-M/NB8M-SE BLOCK DIAGRAM

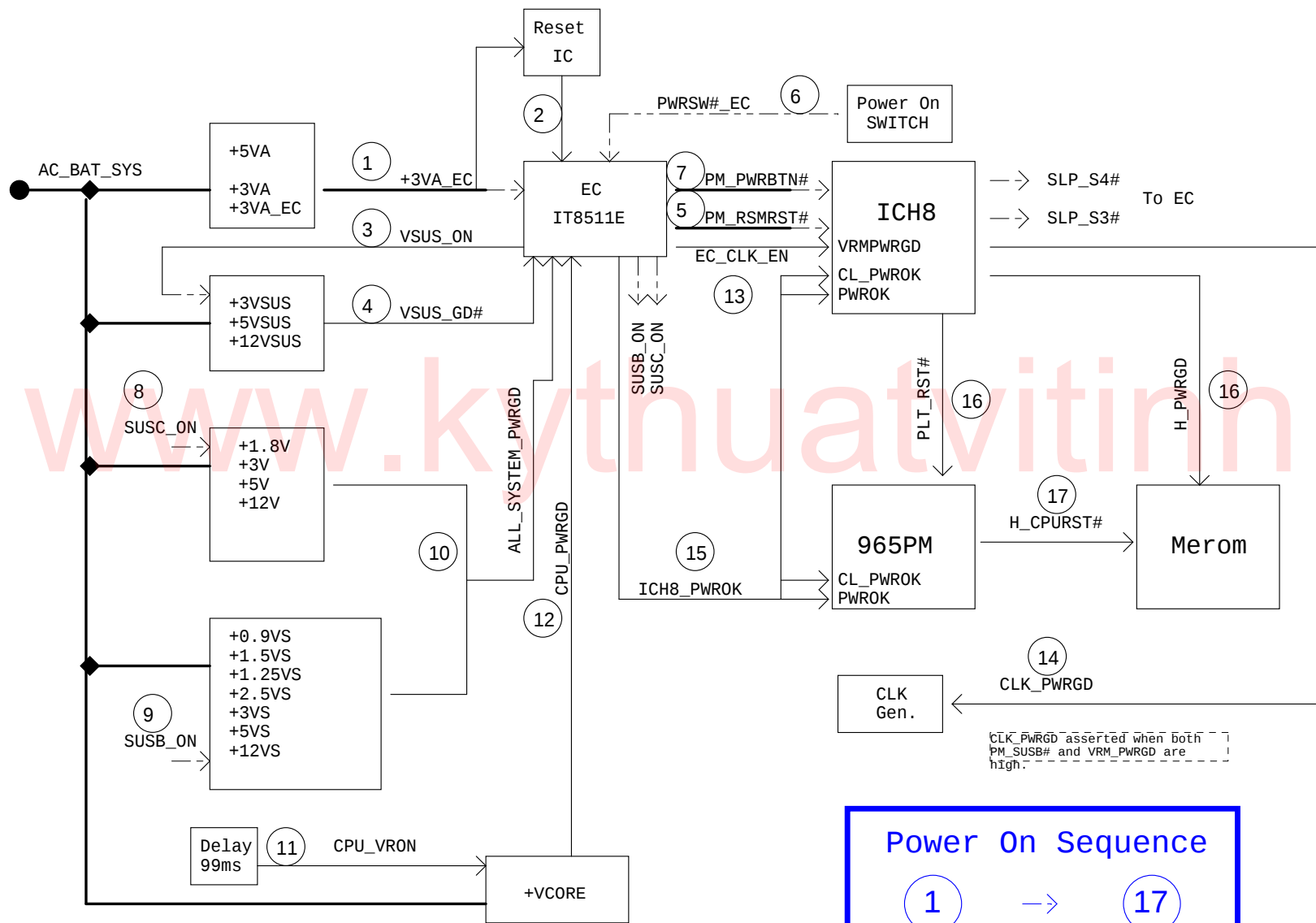


CLOCK GEN.
ICS9LPR363CGLF-T
PAGE 21

FAN + Thermal sensor
PAGE 36

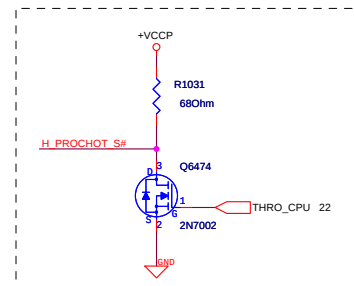
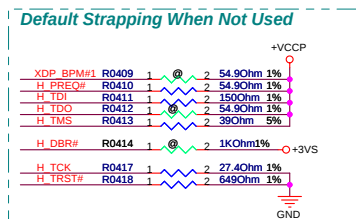
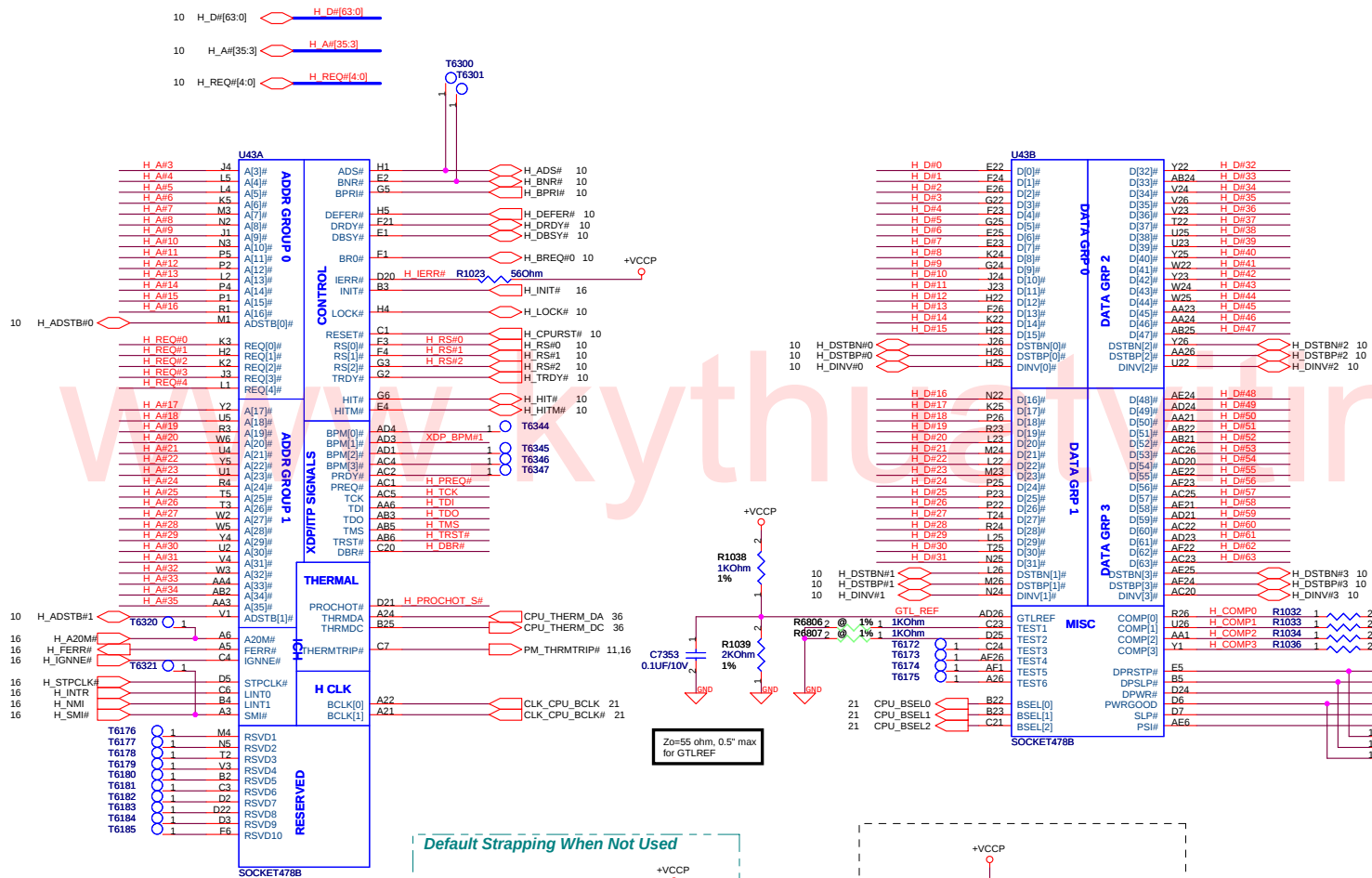
POWER

VCORE	PAGE 80
SYSTEM	PAGE 81
1.5VS, 1.05VS	PAGE 82
DDR&VTT	PAGE 83
+1.25VS&2.5VS	PAGE 84
VGACore&+1.25V0	PAGE 85
SHUTDOWN#	PAGE 87
CHARGER	PAGE 88
DETECT	PAGE 90
LOAD SWITCH	PAGE 91
PROTECT	PAGE 92
POWER SIGNAL	PAGE 93
FLOWCHART	PAGE 94



Power On Sequence

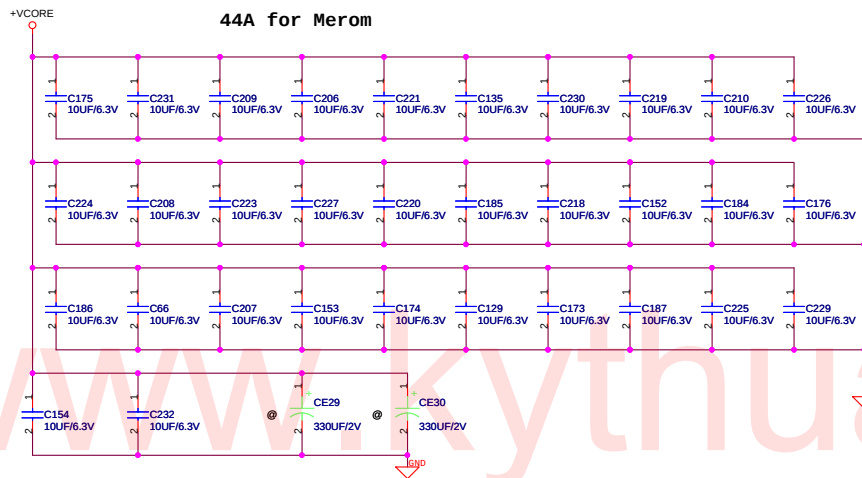




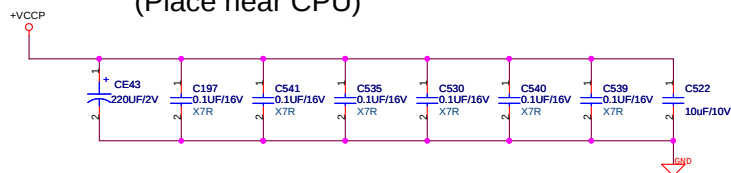
Comp0.2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp 1.3 connect with Zo=55 ohm, make trace length shorter than 0.5".

	MEROM	FSB800	Vcore
VCCP	Min 1.0V	Typ 1.05V	Max 1.1V
ICCP	Min	Typ	Max 2.5A





+VCCP Decoupling Capacitor (Place near CPU)



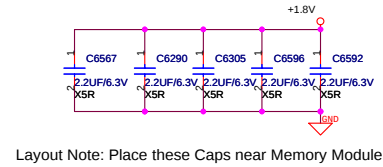
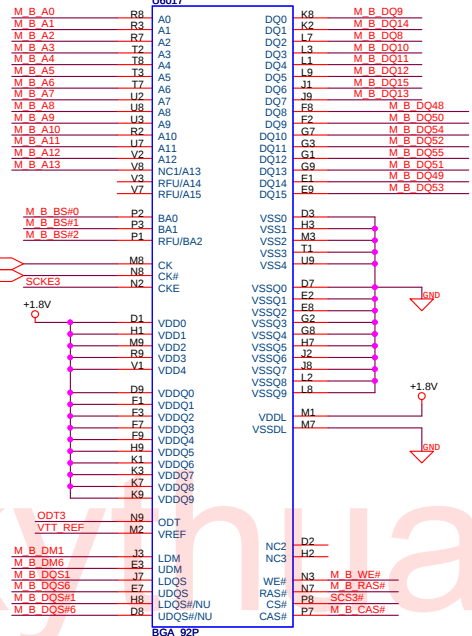
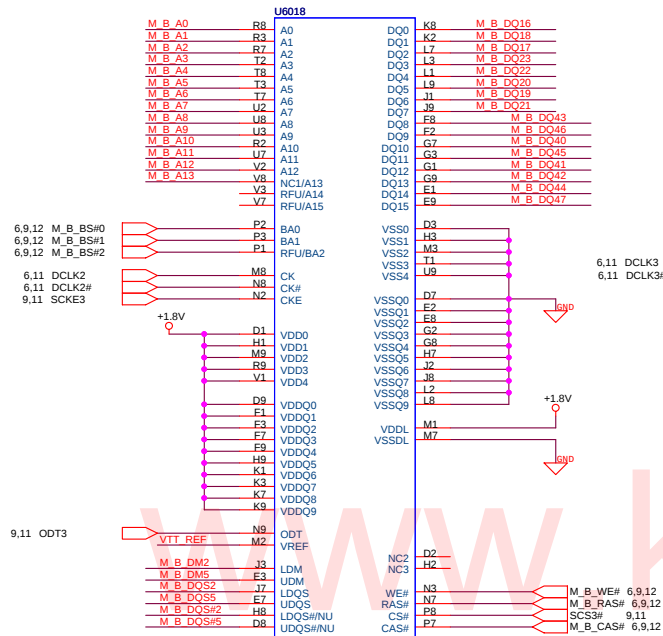
Decoupling guide from INTEL

VCCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	270uF	* 1pcs for CPU

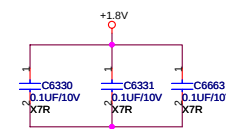
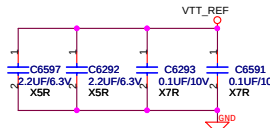
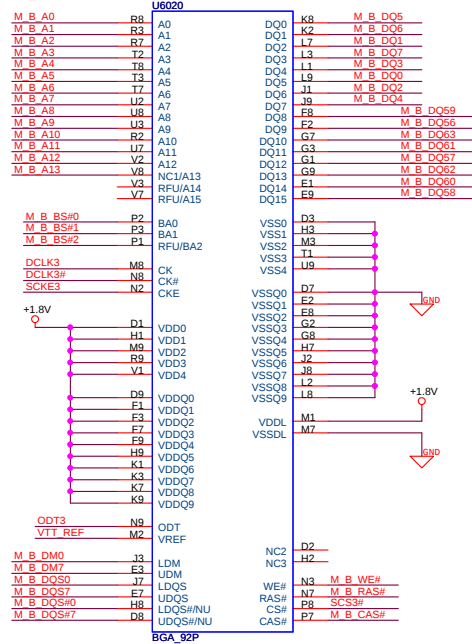
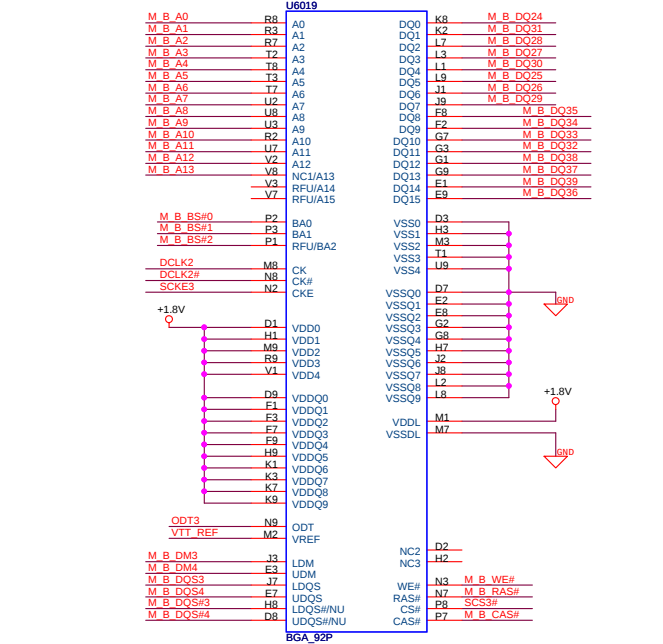
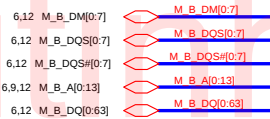
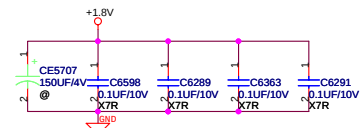
Decoupling for W7S

VCCORE	10uF/6.3V	* 32pcs
	330uF/2V	* 2pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

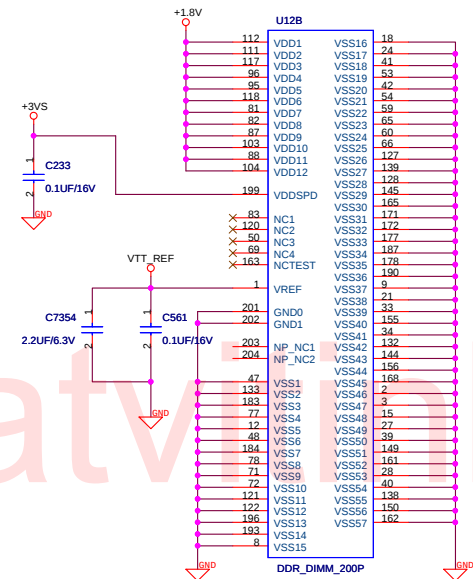




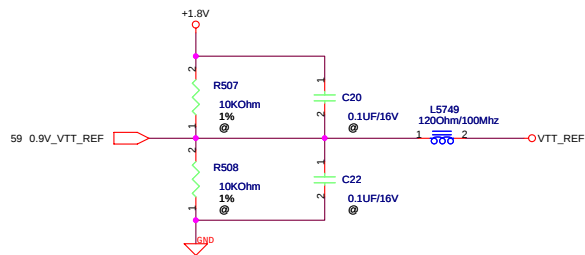
Layout Note: Place these Caps near Memory Module



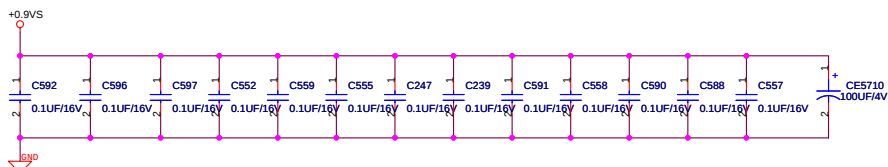
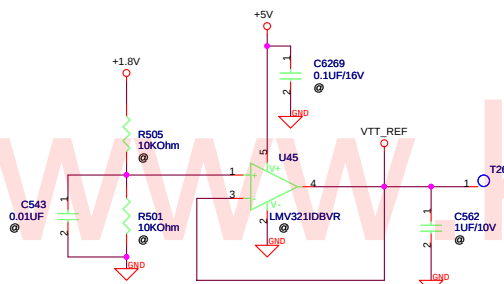
BOTTOM SIDE:
Channel B



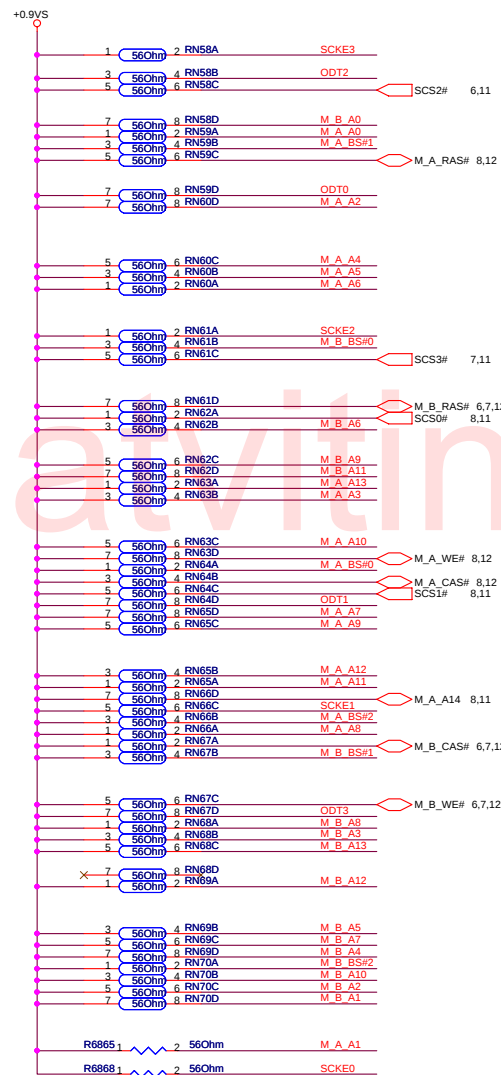
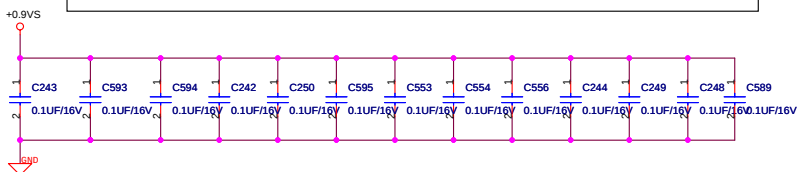
		Title : <u>DDR SO-DIMM</u>	
ASUSTek COMPUTER INC		Engineer: <u>Lorentz_Chang</u>	
Size Custom	Project Name T76S	Rev 2.0	
Date: <u>Tuesday, August 21, 2007</u>		Sheet <u>8</u> of <u>70</u>	

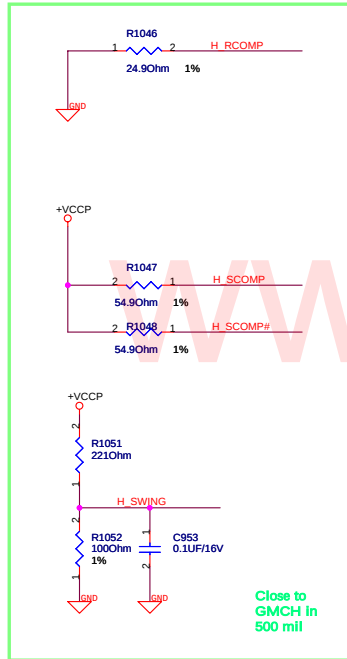


- M_A_A[0..13] 8,12
- M_A_BS#[0..2] 8,12
- M_B_A[0..13] 6,7,12
- M_B_BS#[0..2] 6,7,12
- SCKE[0..3] 6,7,8,11
- ODT[0..3] 6,7,8,11

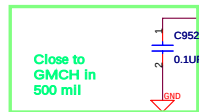


Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

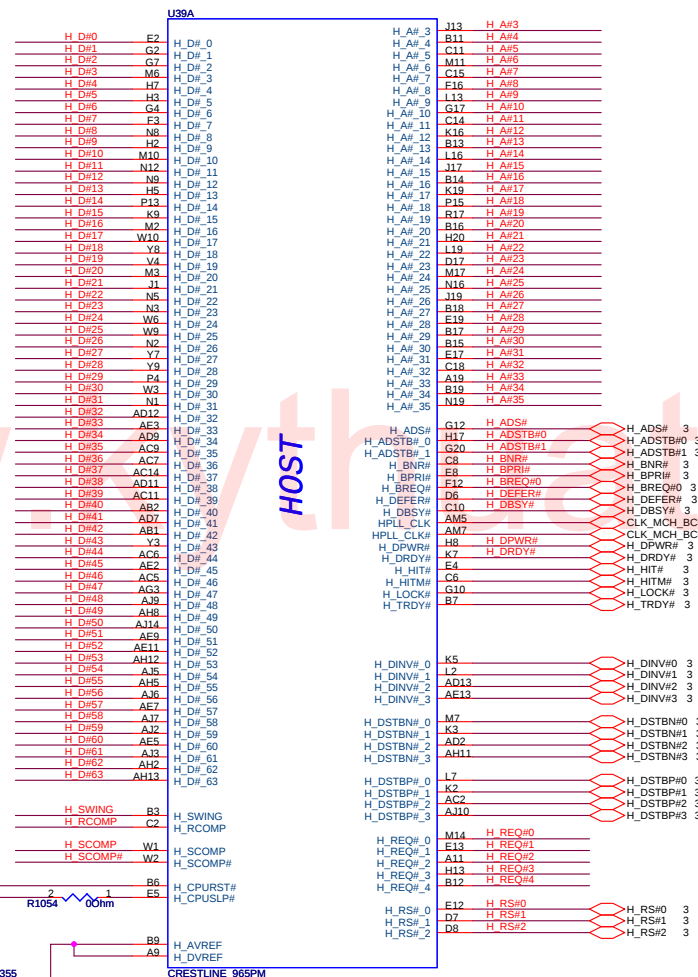
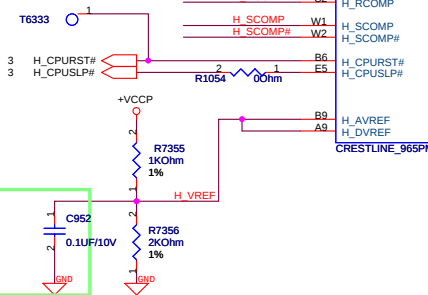




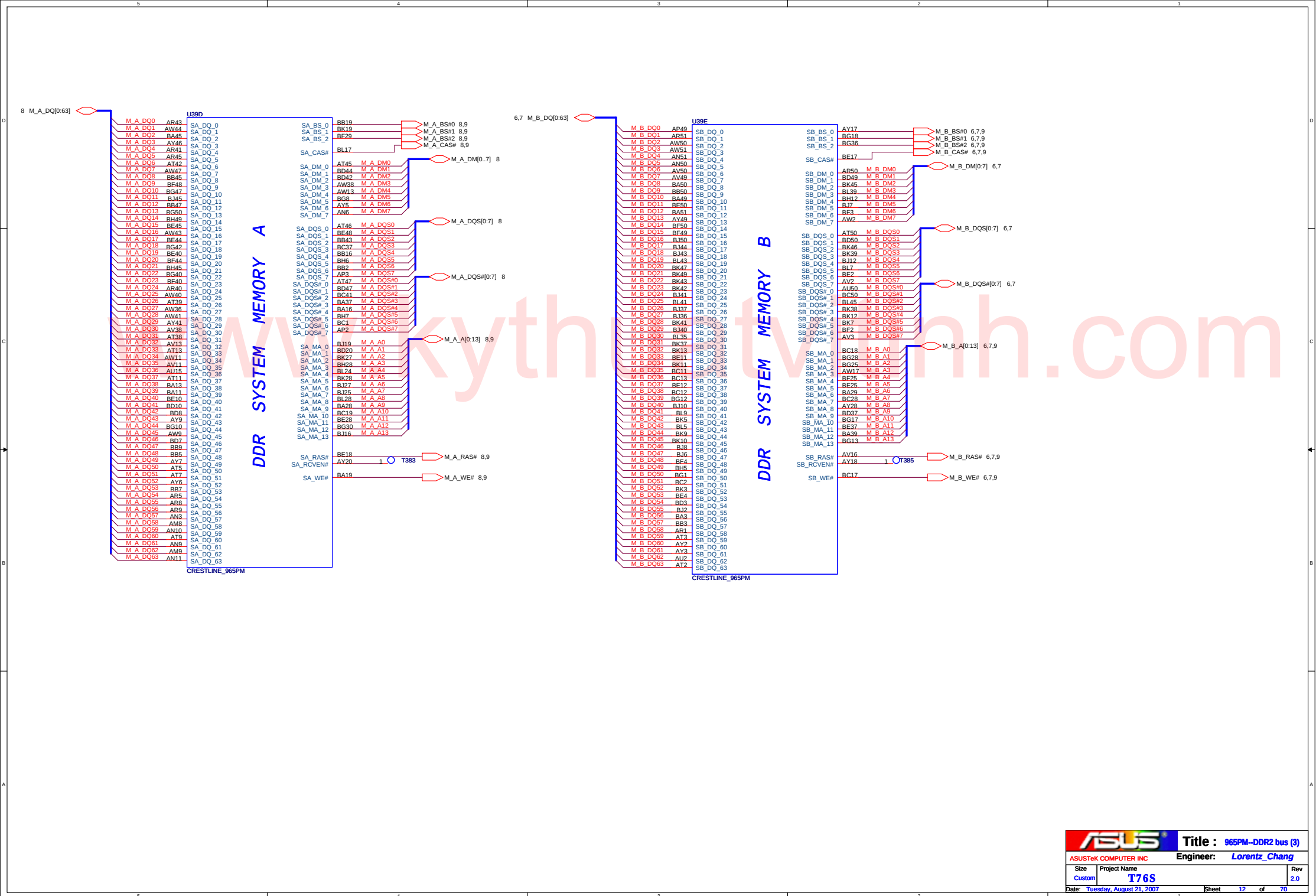
Close to GMCH in 500 mil



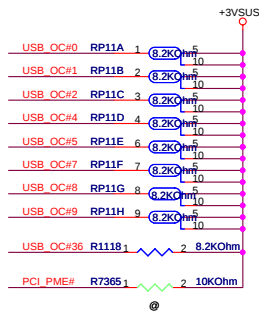
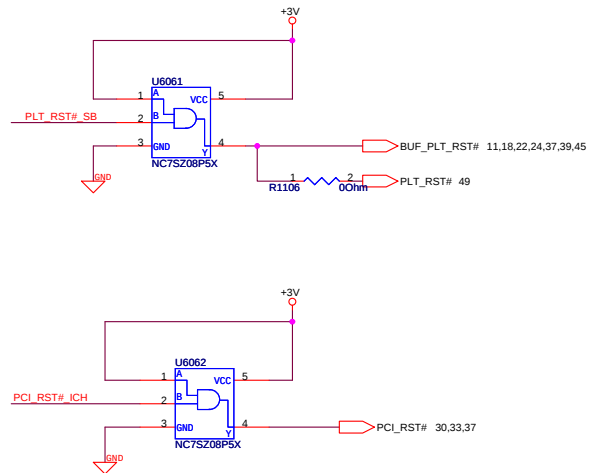
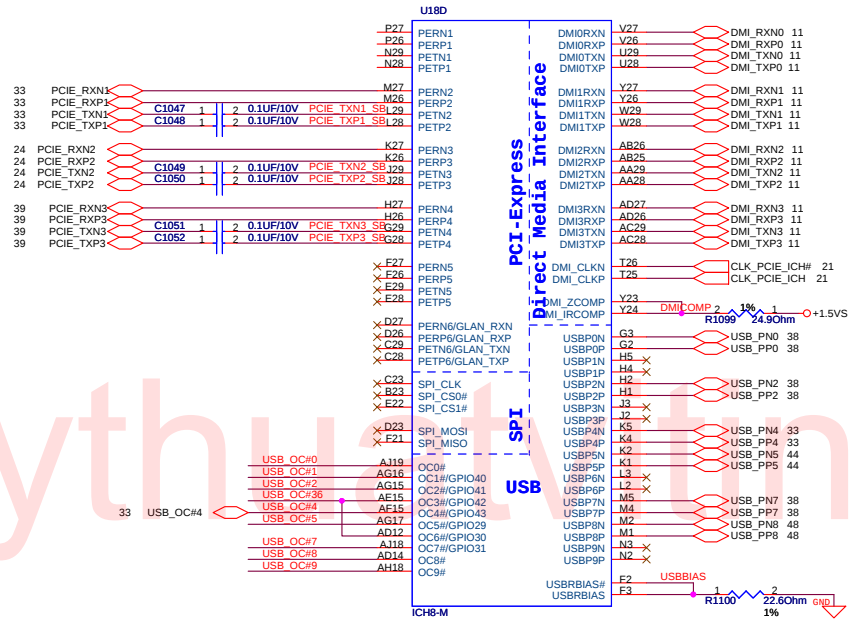
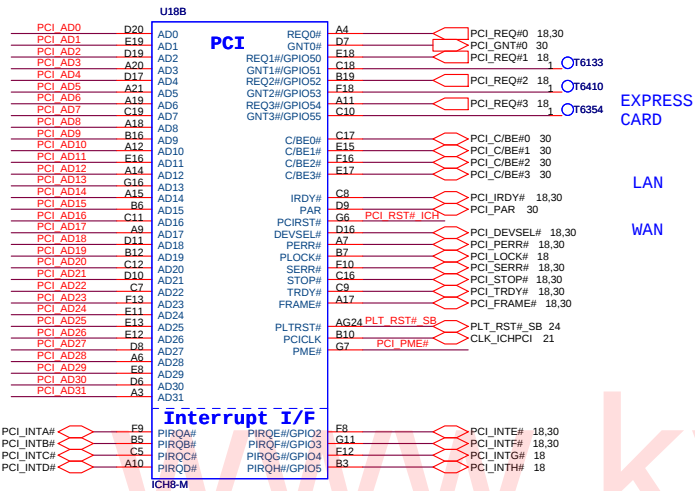
Close to GMCH in 500 mil





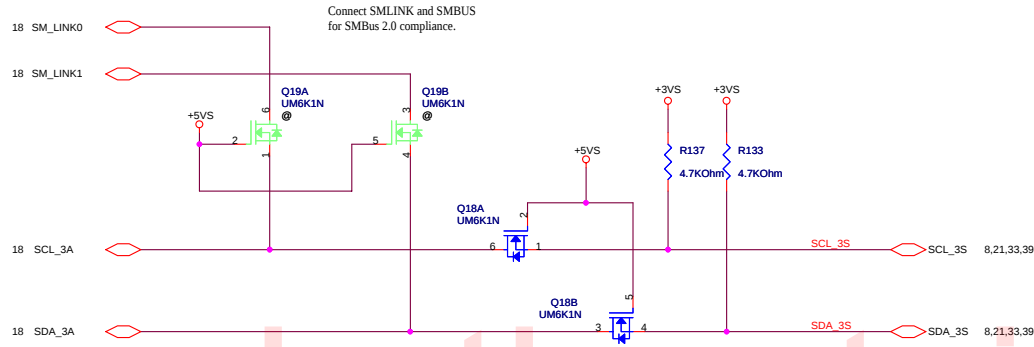


30 PCI_AD[0..31] PCI_AD[0..31]

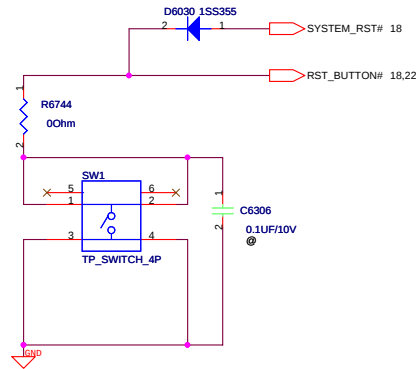


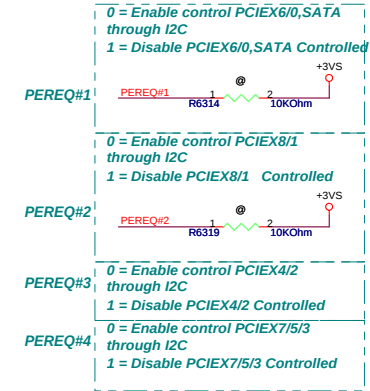
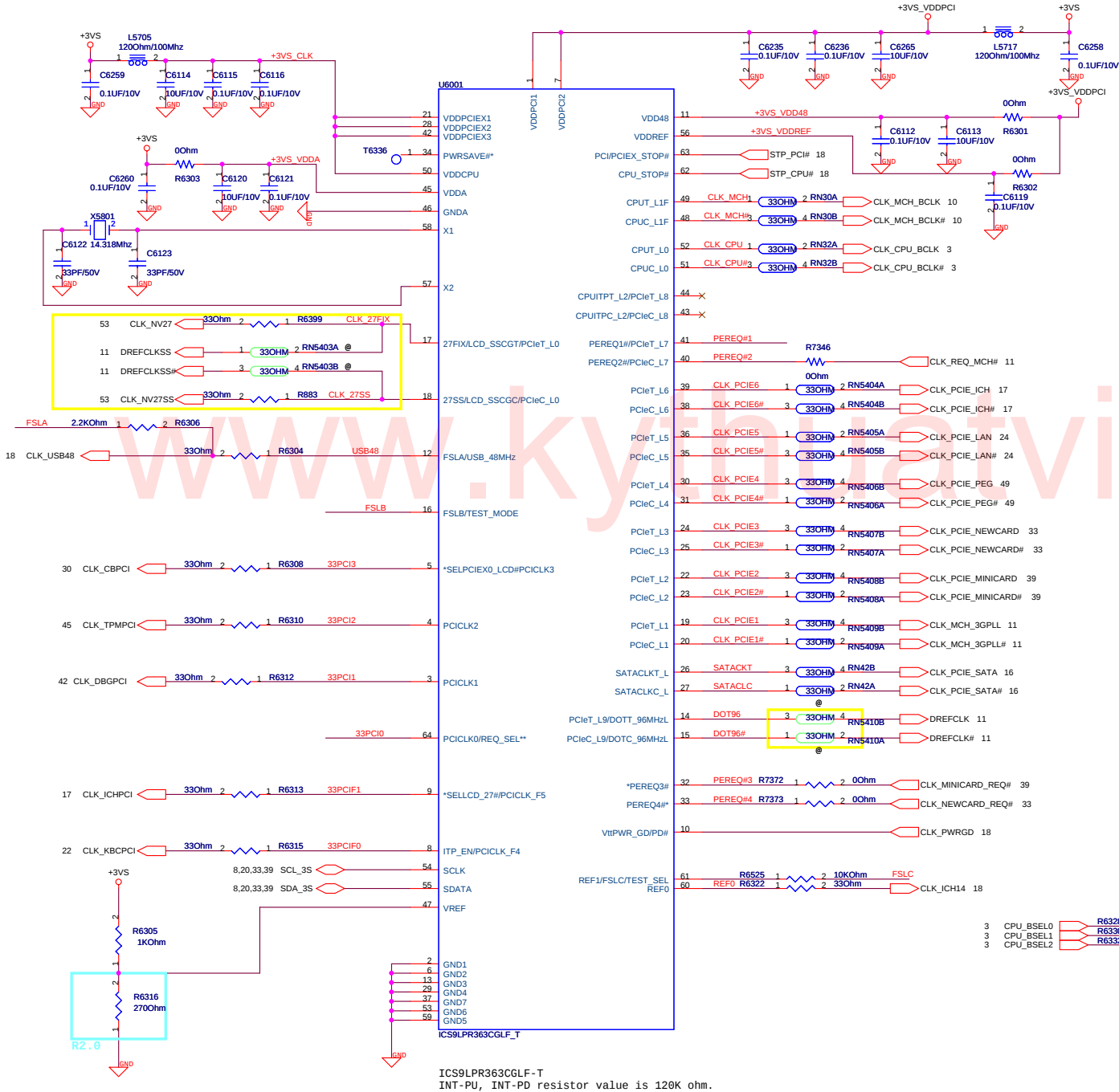


ICH8-M

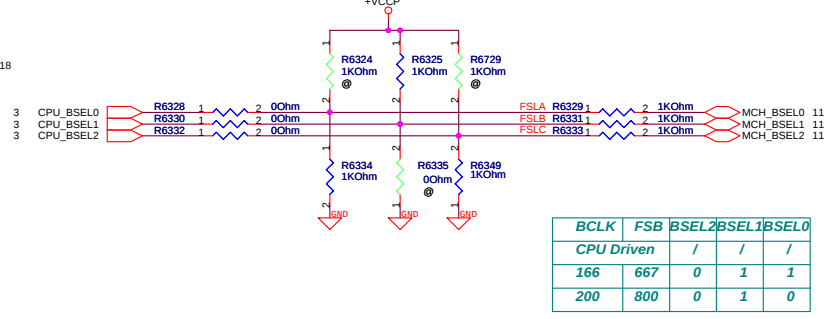
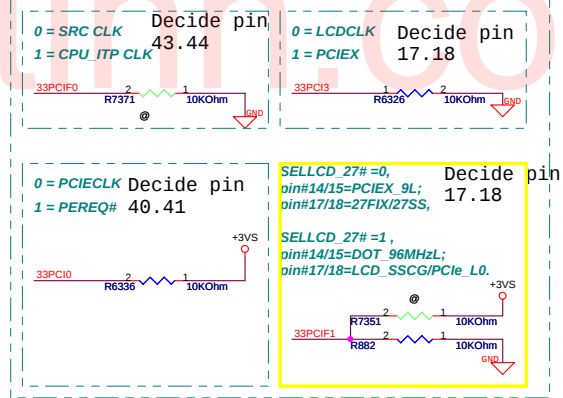


ICH8-M



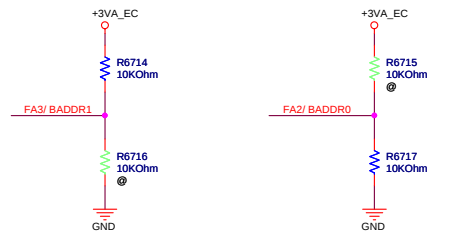


Latched Input Select



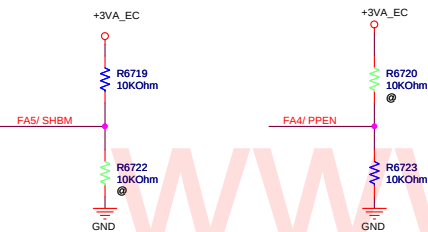
BCLK	FSB	BSEL2	BSEL1	BSEL0
CPU Driven	/	/	/	/
166	667	0	1	1
200	800	0	1	0

10:Determined by EC



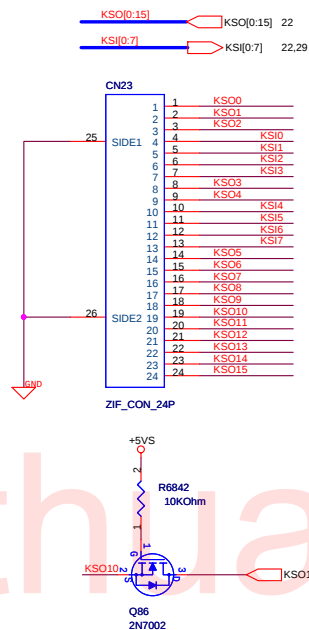
FA3/ BADDR1:seect LPC
address: 4E/4F

FA2/ BADDR0 :seect LPC
address:2E/2F

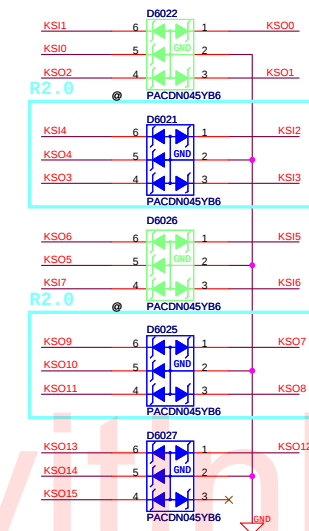


FA5/ SHBM:share BIOS
mode enable.

FA4/ PPEN:enable in-system
program via parallel port
interface.(KBS down)

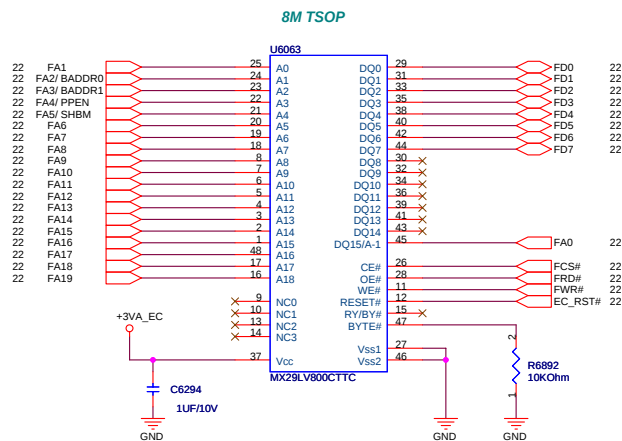


EMI recommendation. To protect KBC destroy by ESD.
Need put between KB connector and KBC, and close to
the connector as possible.

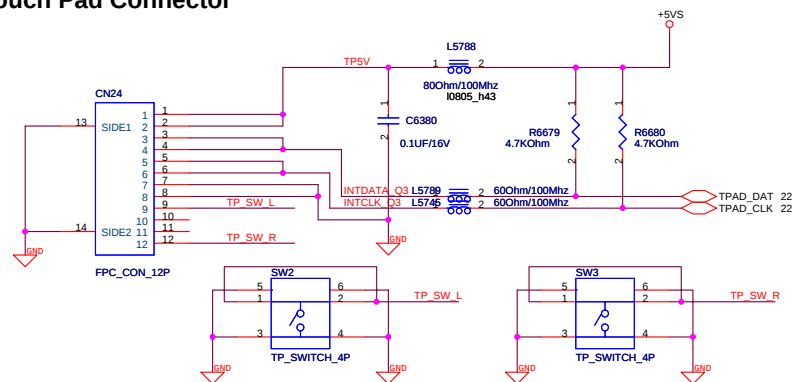


Each IC needs 2 vias to ground.

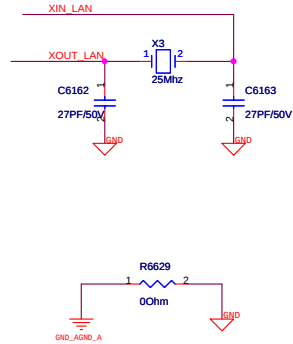
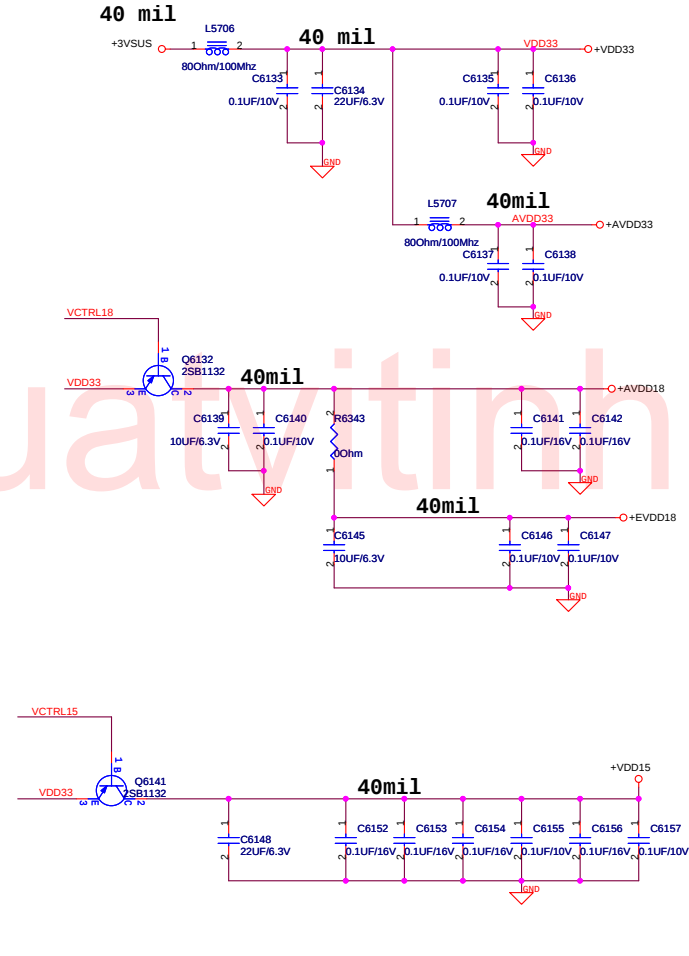
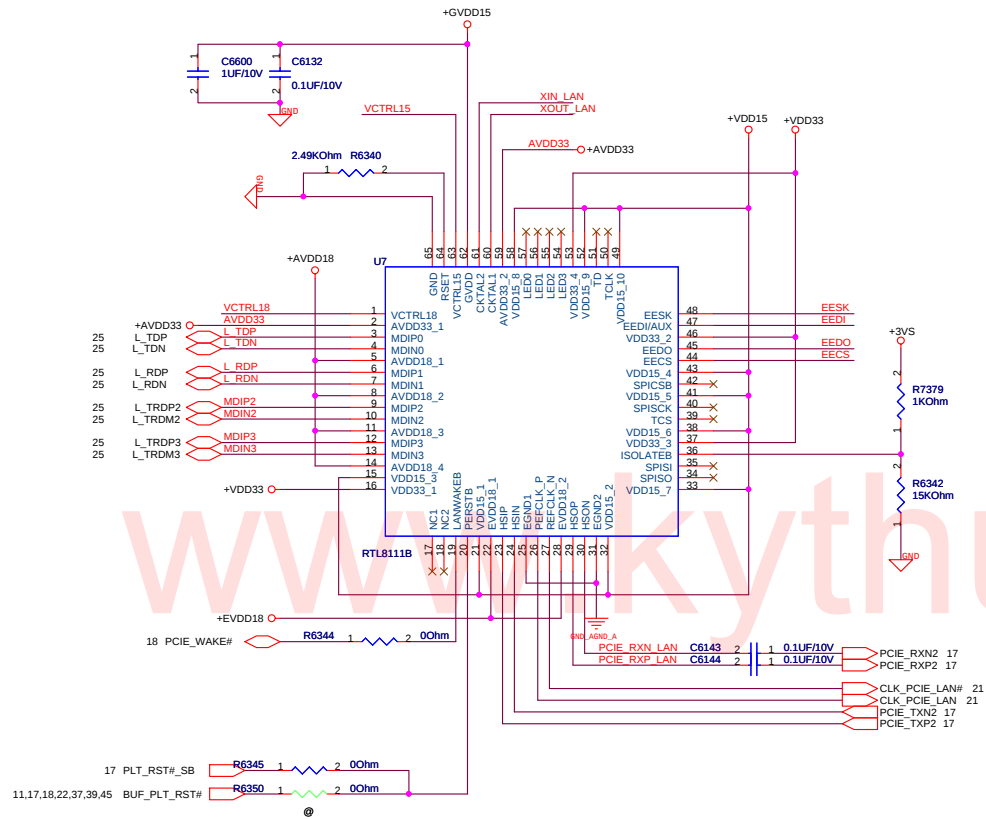
8M-ROM

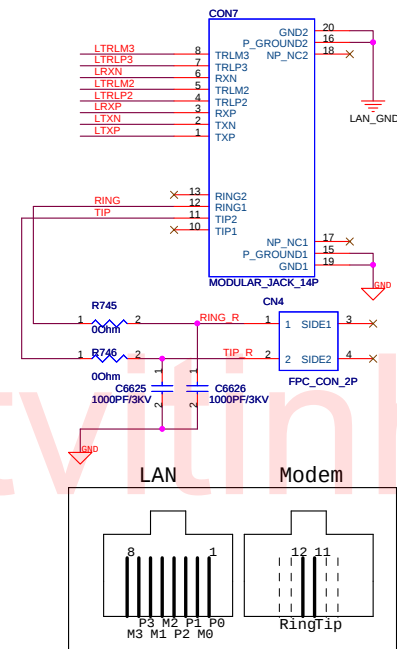
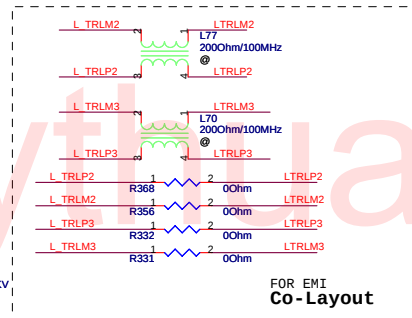
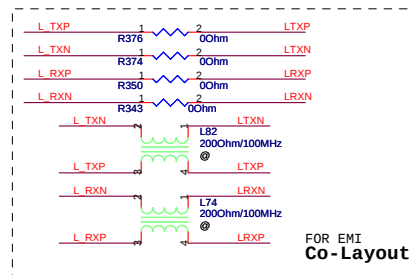
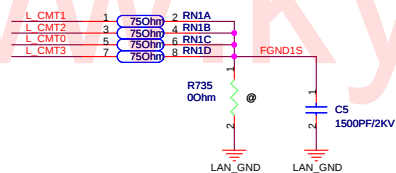
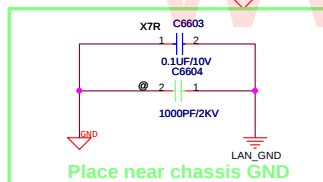
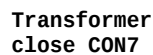


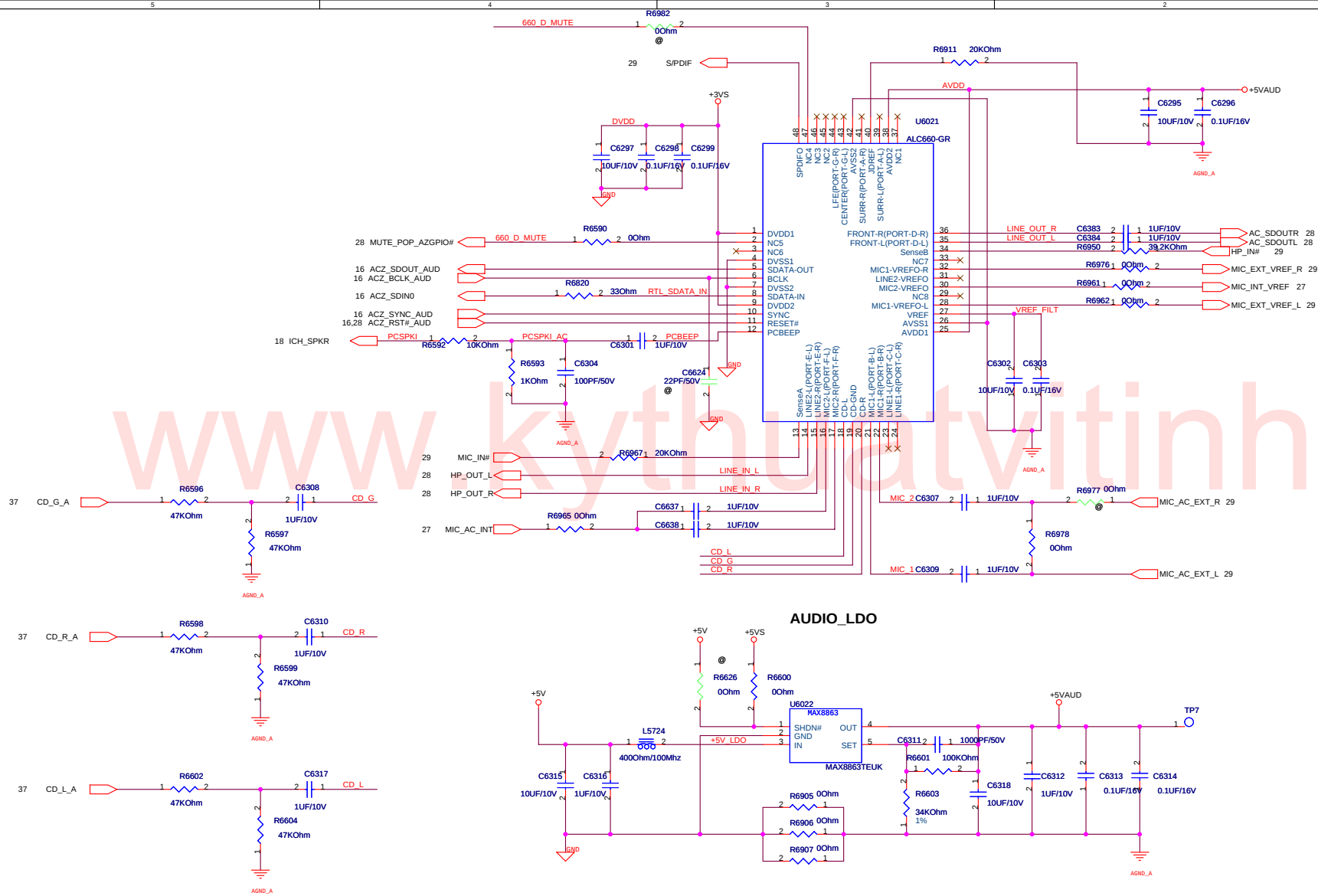
Touch Pad Connector



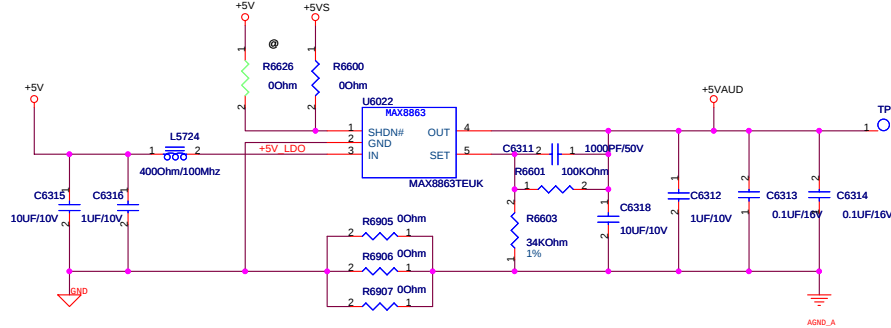
Average supply current
VDD33 103mA
AVDD18+EVDD18 198mA
VDD15 367mA



[illegible]



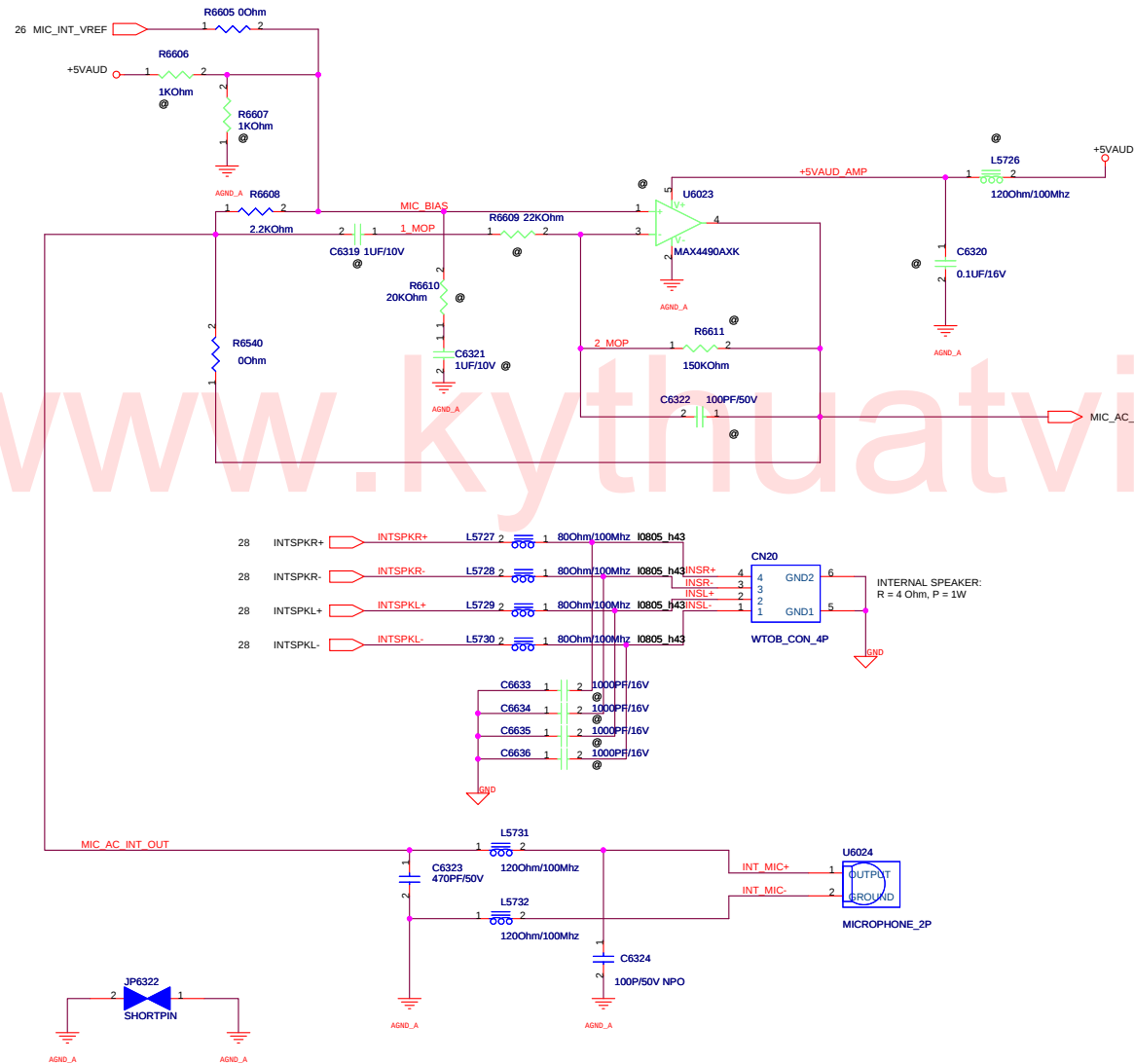
AUDIO_LDO



<Variant Name>

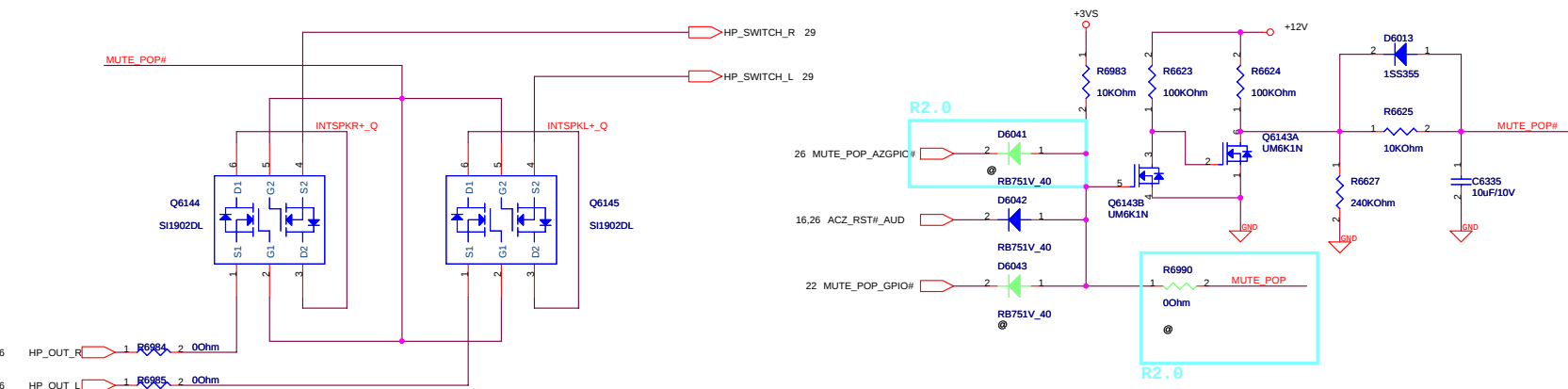
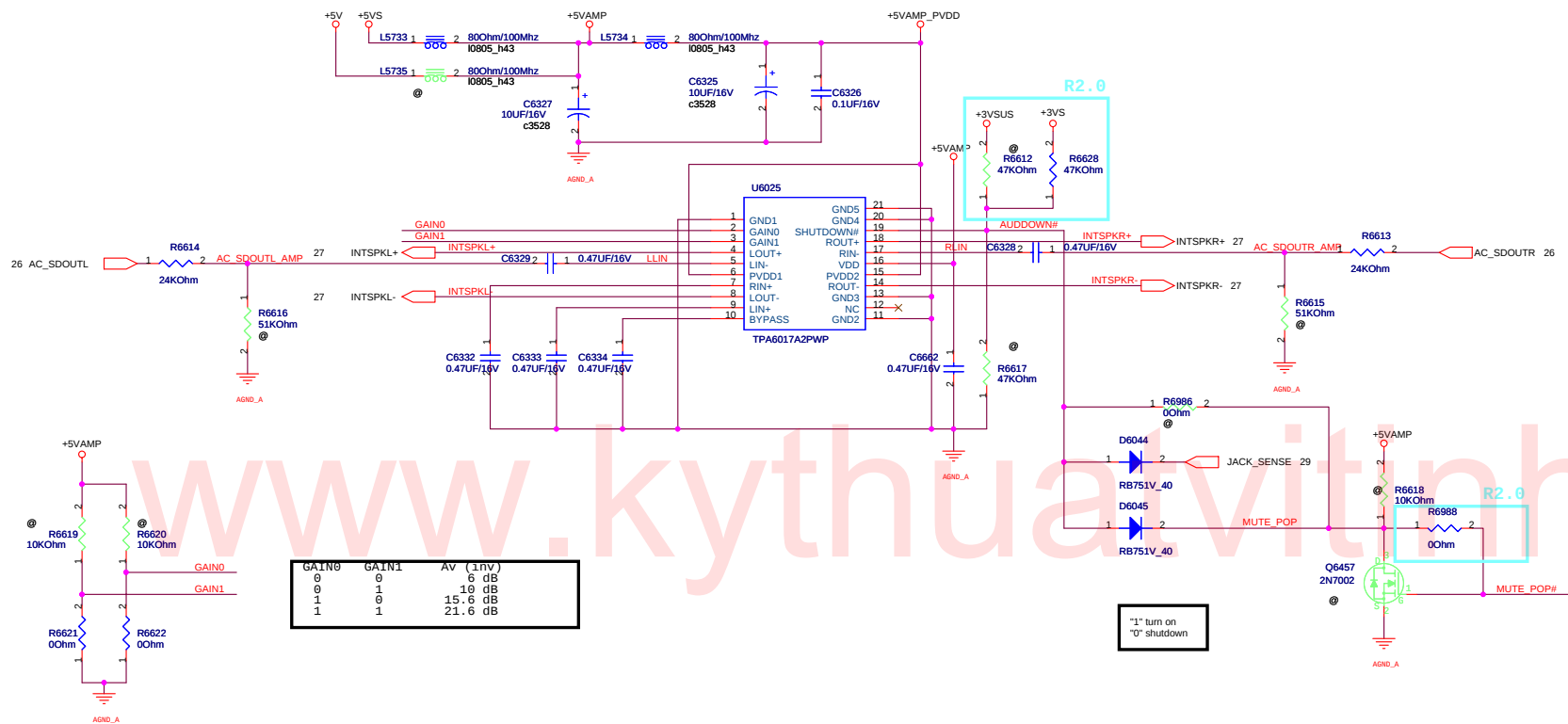
ASUS		Title : AZALIA_ALC660	
ASUSTek COMPUTER INC		Engineer:	
Size Custom	Project Name T76S	Rev 2.0	
Date: Tuesday, August 21, 2007		Sheet 26 of 70	

MIC PreAmp & Mic Jack



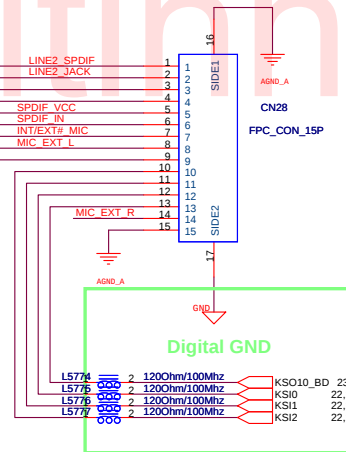
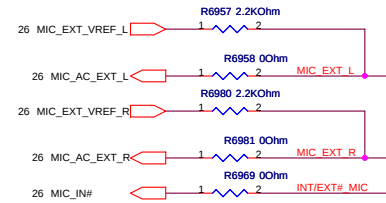
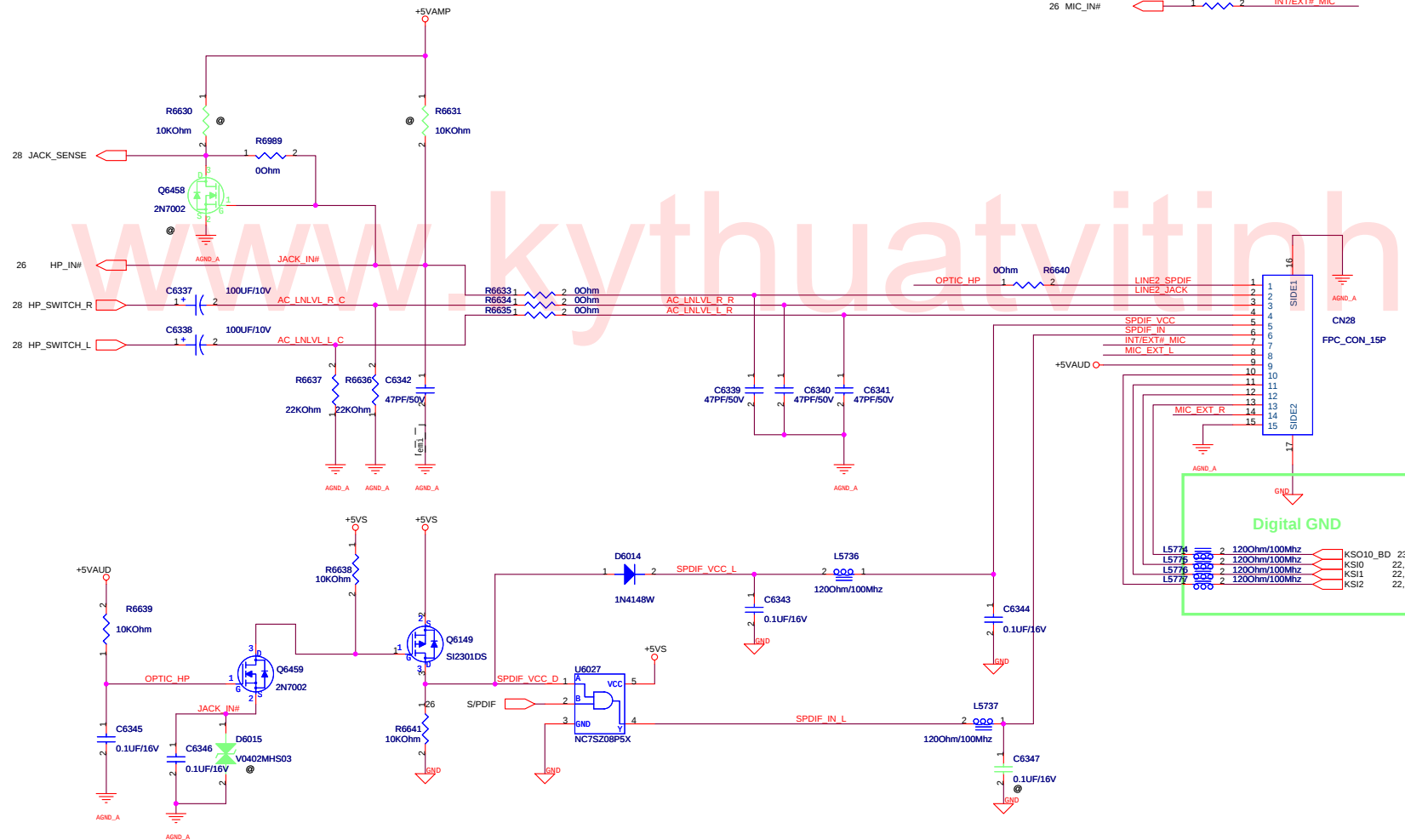
<Variant Name>

ASUS		Title : MIC PREAMP & INT MIC	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	T76S	2.0	
Date: Tuesday, August 21, 2007		Sheet 27 of 70	



<Variant Name>

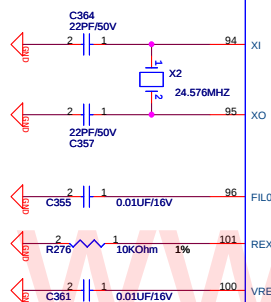
JACK_IN#	OPTIC_HP	SPDIF
L	H	LINE OUT
L	L	LINE OUT
H	H	NO CONNECT



<Variant Name>

ASUS		Title : SPDIF JACK	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	T76S	2.0	
Date: Tuesday, August 21, 2007		Sheet 29 of 70	

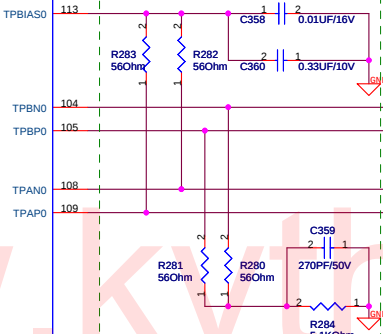
as close as possible to R5C832



IEEE1394/SD

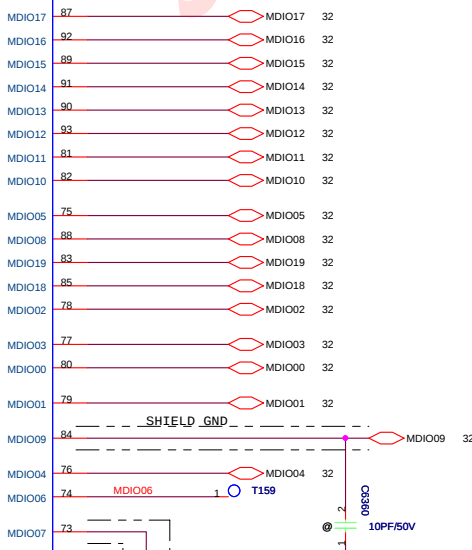
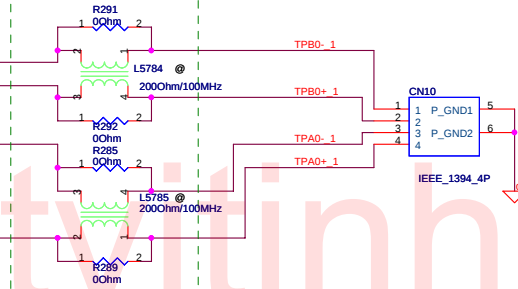
AVCC_PHY3V_1
AVCC_PHY3V_2
AVCC_PHY3V_3
AVCC_PHY3V_4

AS CLOSE AS POSSIBLE TO R5C832



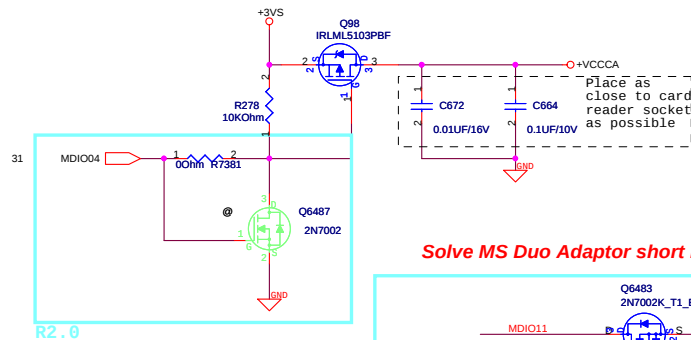
Circuit area : As small as possible.

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR

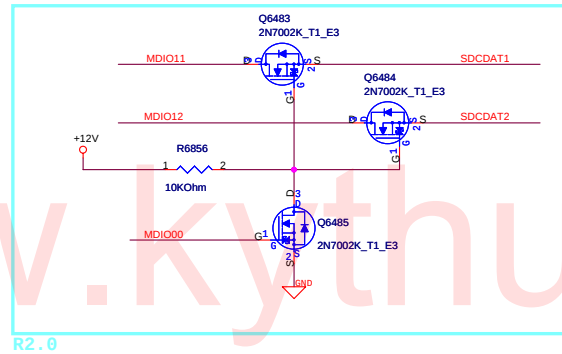


MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

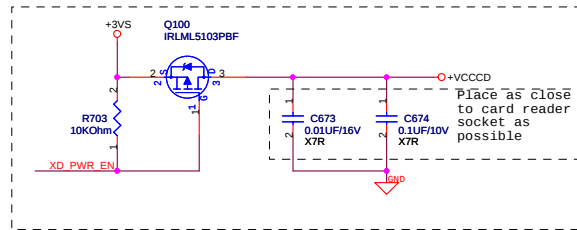
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO07--> SD External Clock/
MS External Clock
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3



Solve MS Duo Adaptor short issue.

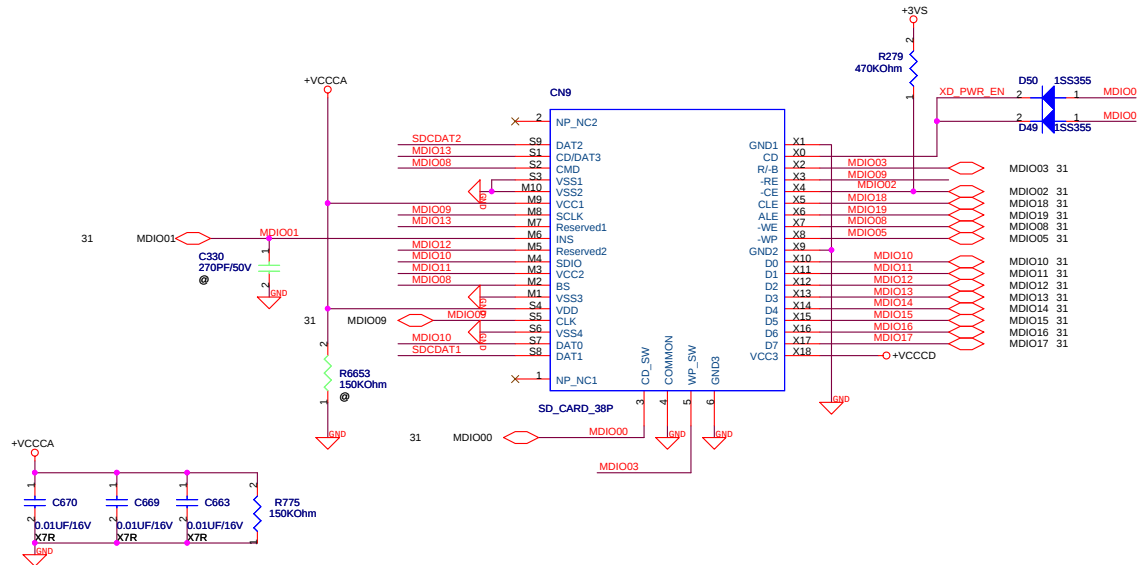


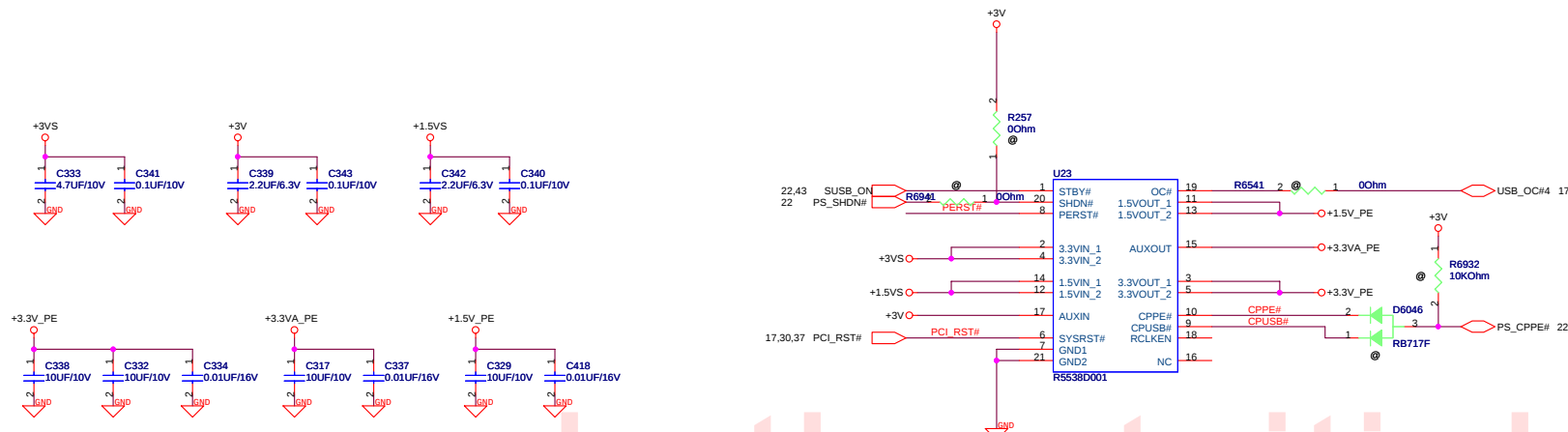
To correct the problem when MS Duo adaptor is in use.



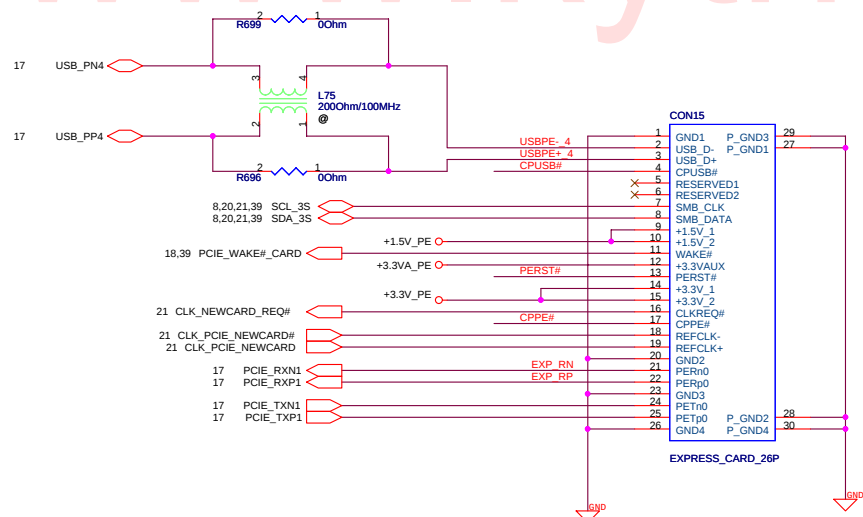
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE





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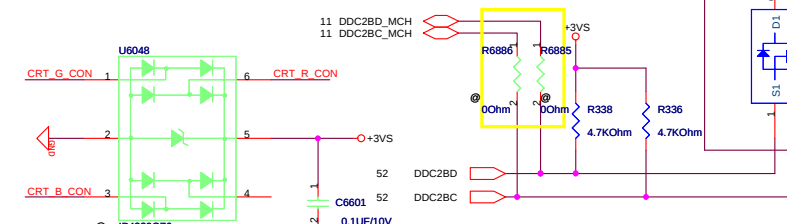
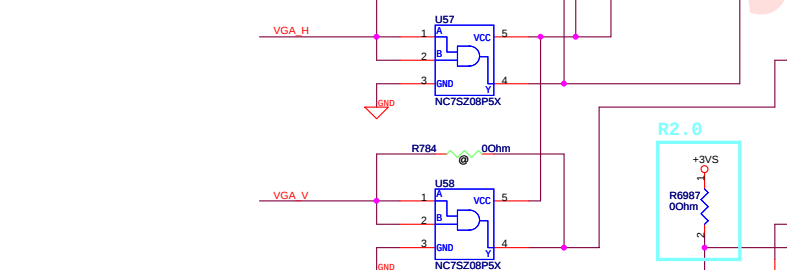
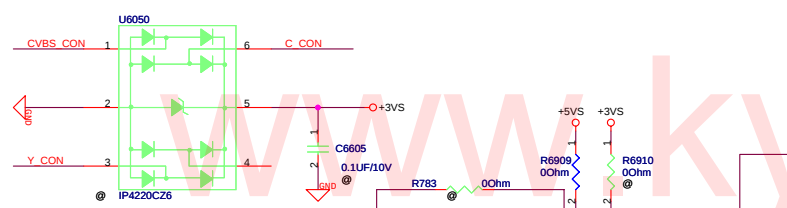
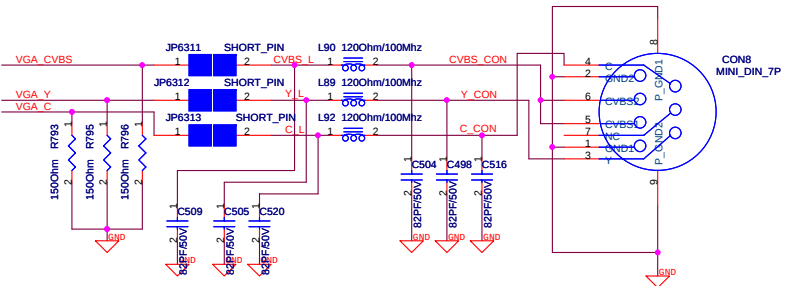
As short as possible



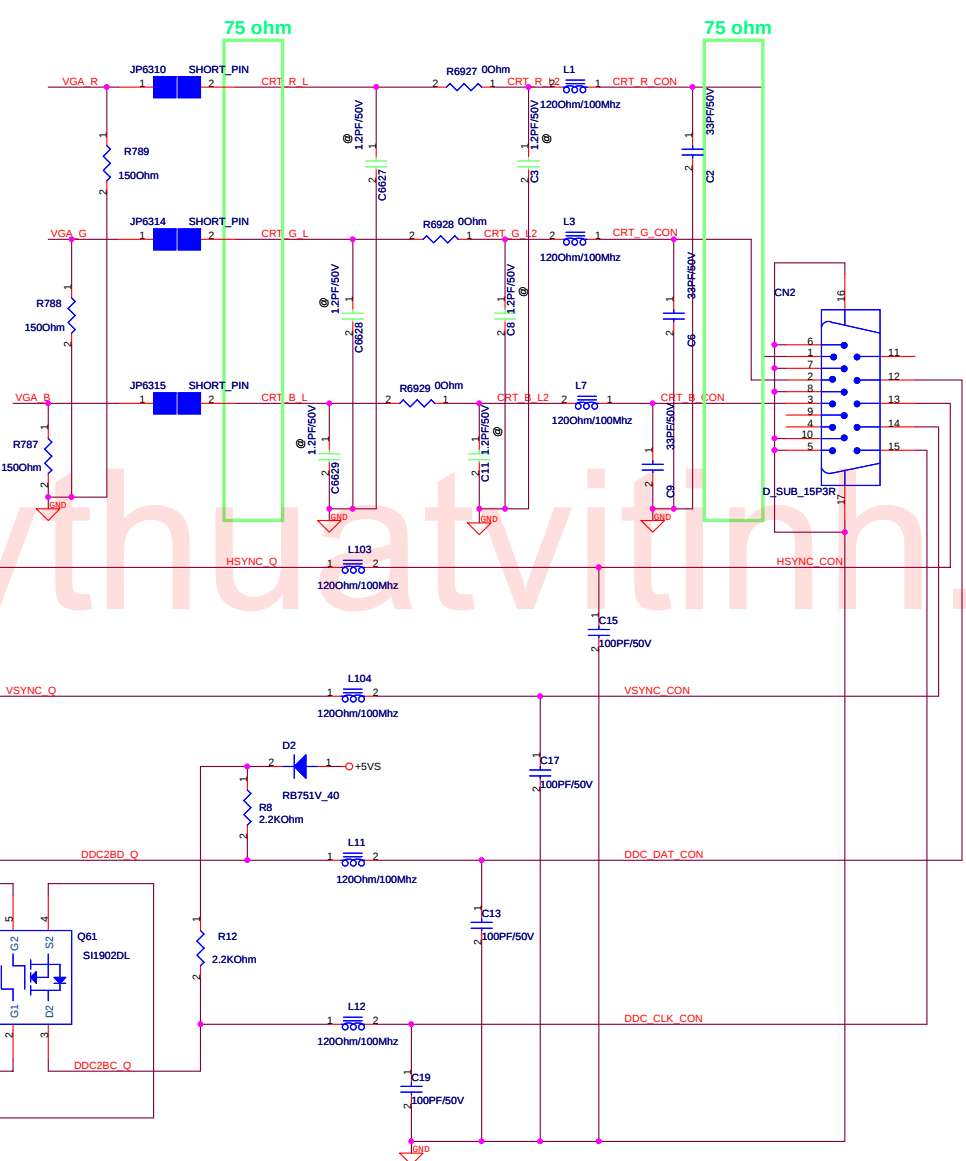
WTOB CON 20P

52	TV_COMP_B_PB	2	1	VGA CVBS	2	1	CVBS_MCH	11
52	TV_Y_G	2	1	VGA Y	2	1	Y_MCH	11
52	TV_C_R_PR	2	1	VGA C	2	1	C_MCH	11

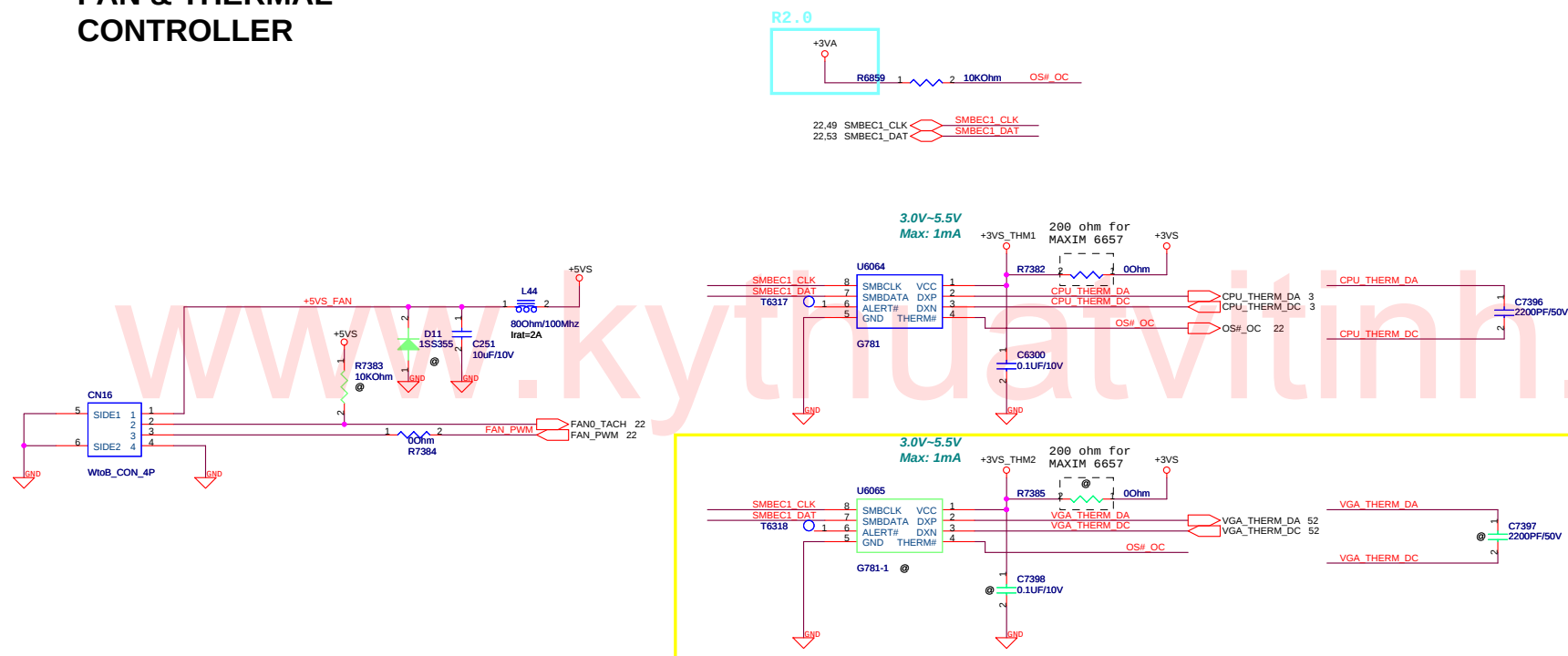
TV OUT

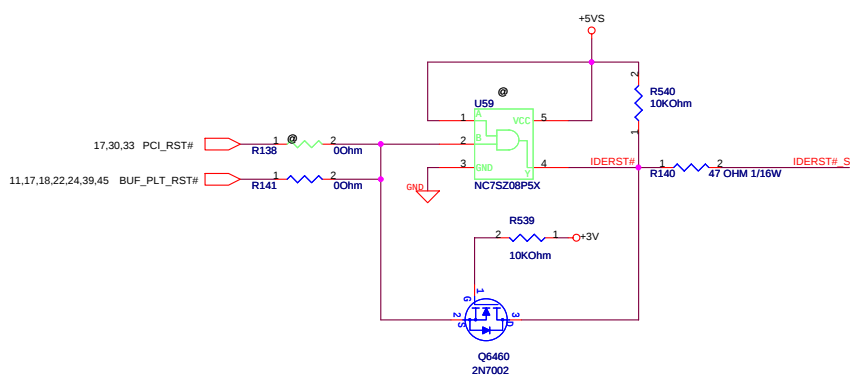
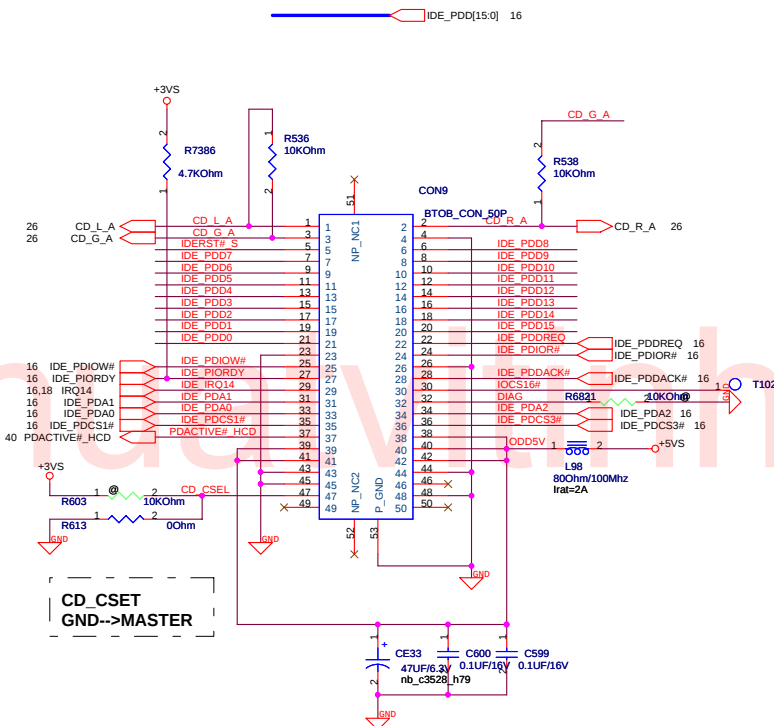
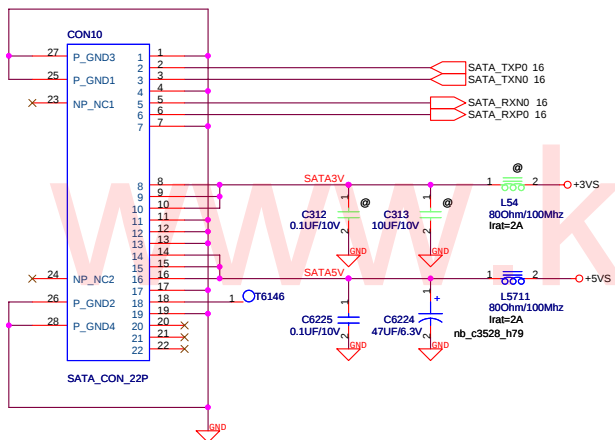


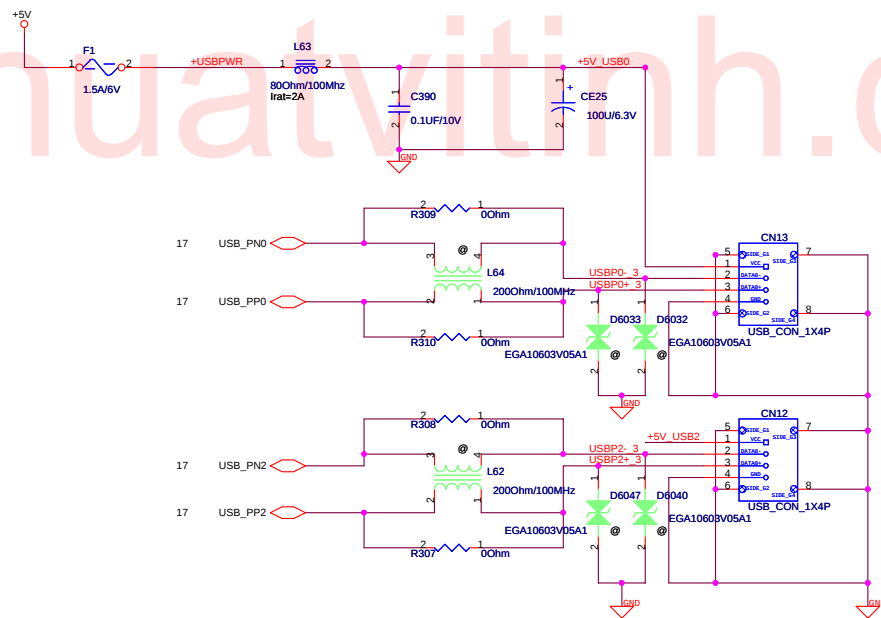
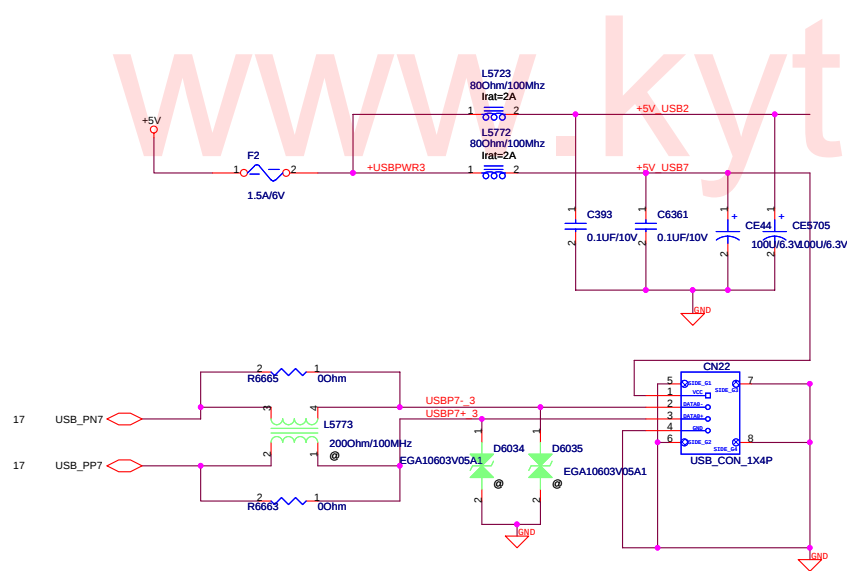
52	DAC_R	2	1	VGA R	2	1	R_MCH	11
52	DAC_G	2	1	VGA G	2	1	G_MCH	11
52	DAC_B	2	1	VGA B	2	1	B_MCH	11
52	DAC_HSYNC	2	1	VGA H	2	1	HSYNC_MCH	11
52	DAC_VSYNC	2	1	VGA V	2	1	VSYNC_MCH	11



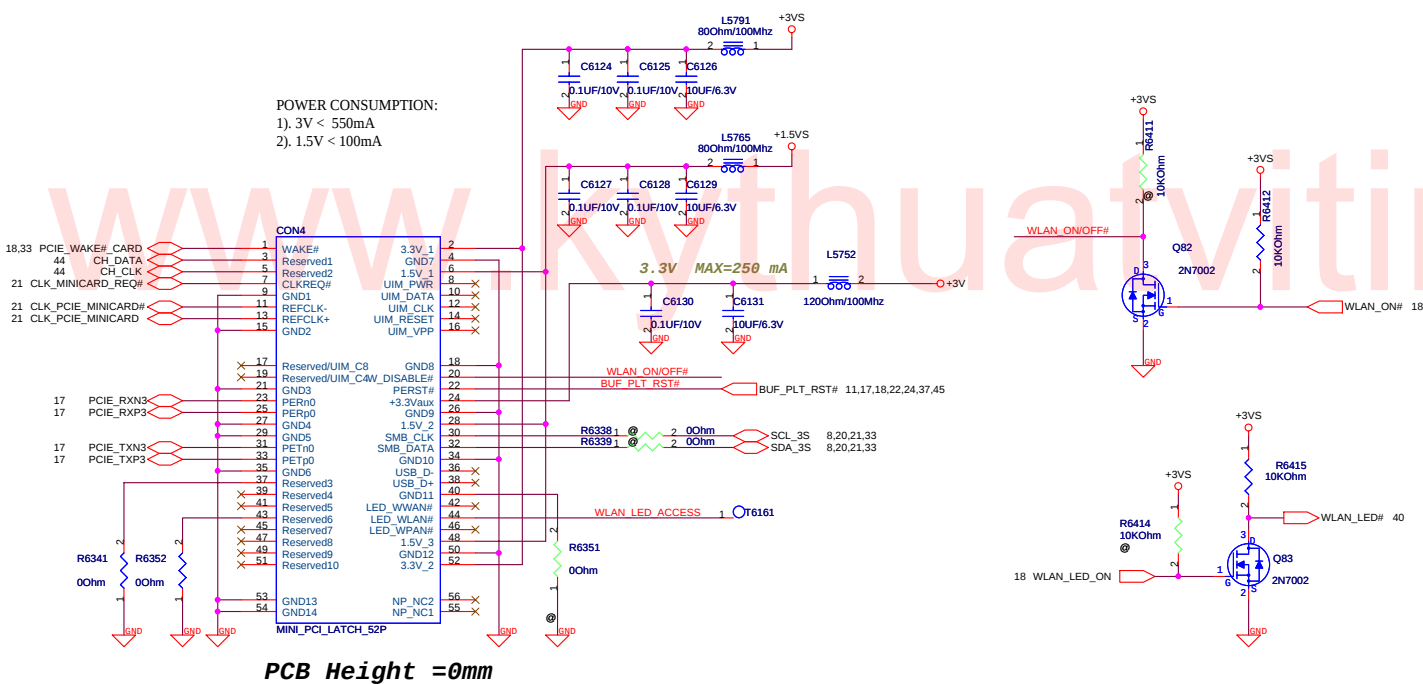
FAN & THERMAL CONTROLLER



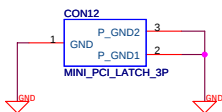




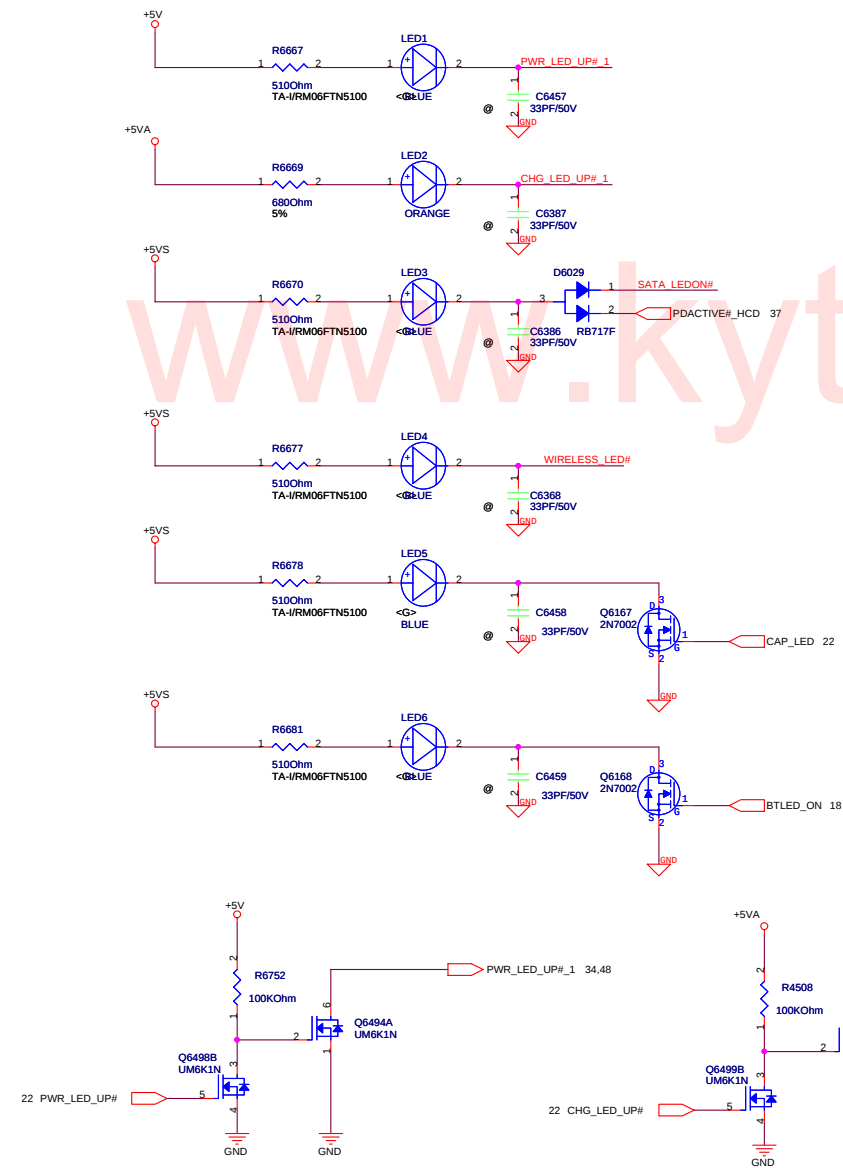
WLAN CON



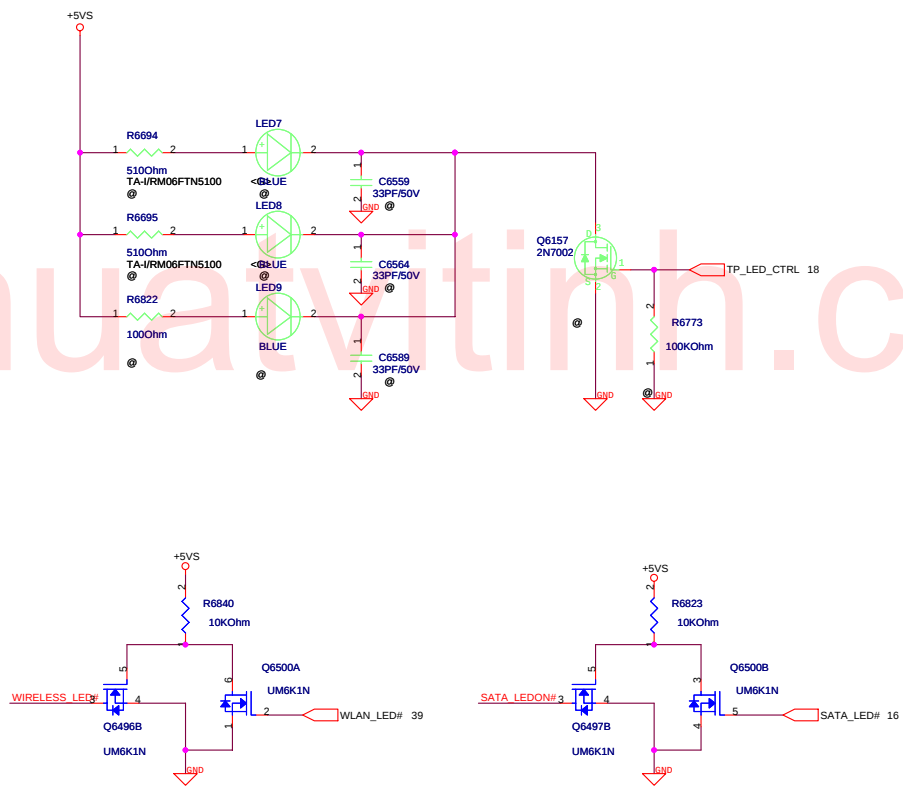
Mini Card Latch



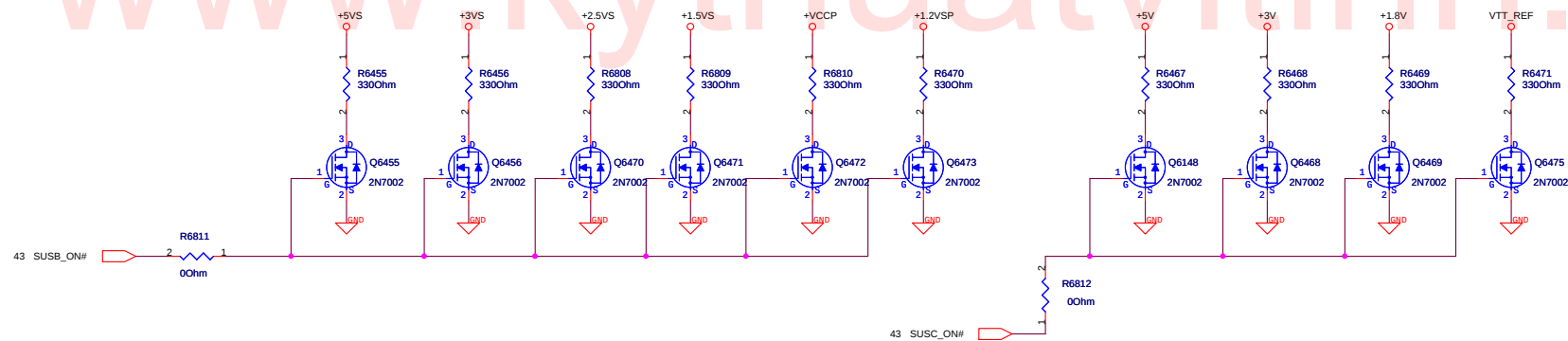
MB/LEDs



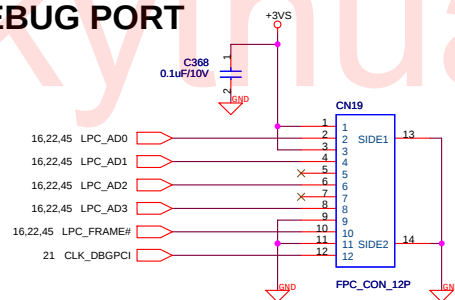
Touch Pad LED



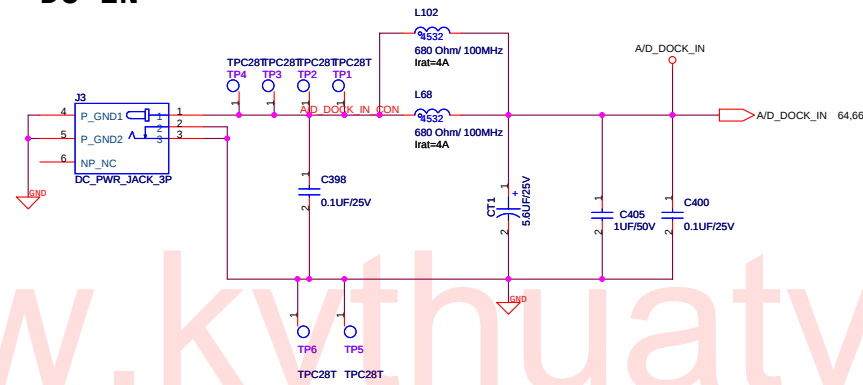
Discharge Circuit



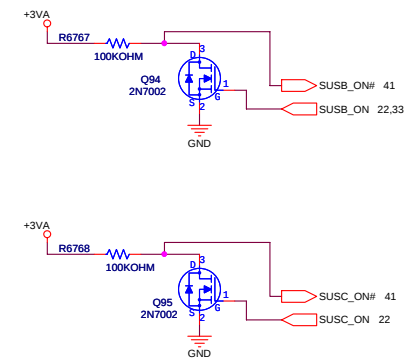
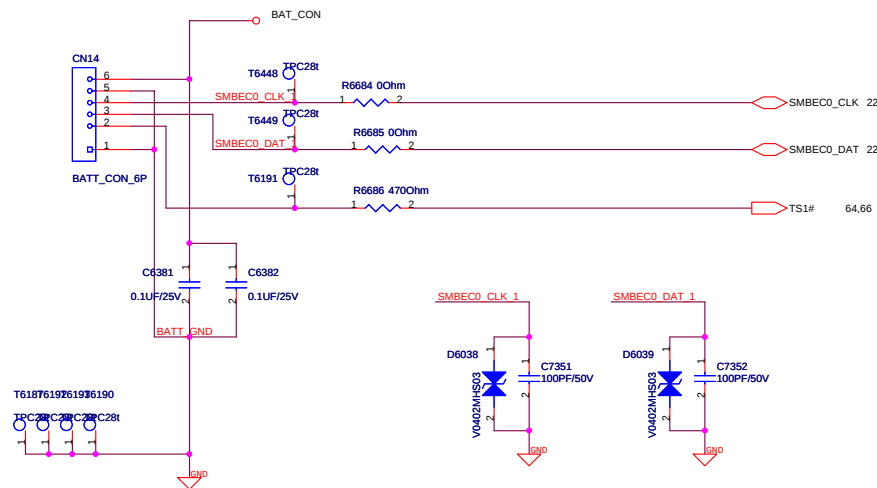
LPC DEBUG PORT

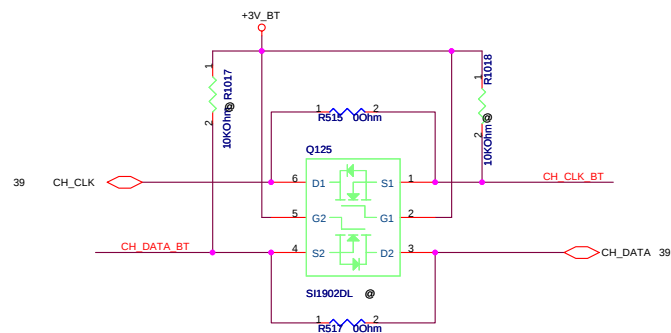


DC-IN



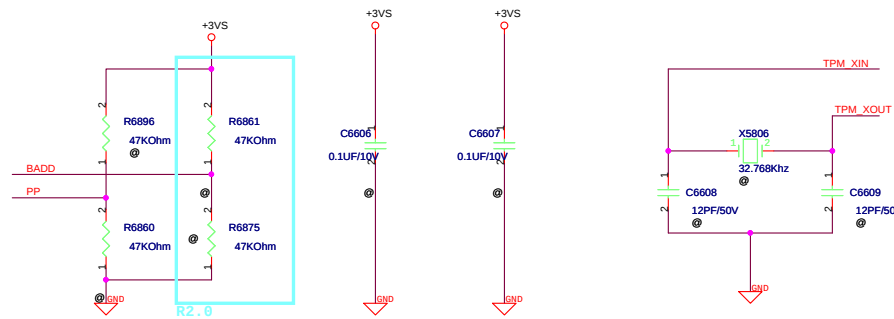
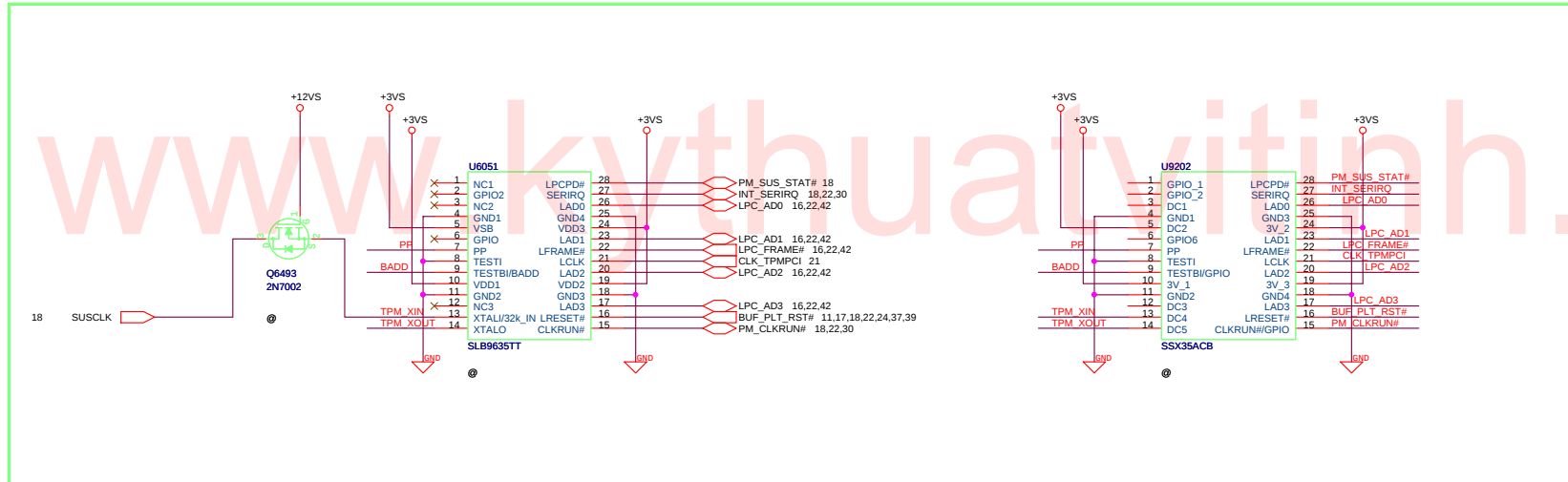
Battery Connector



[illegible]

CO - LAYOUT

TESTBI/BADD PIN LPC ADDRESS SELETE High 4E h, LOW 2E h.
 TEST PIN For normal operation, connect TEST1 to GND.
 PP PIN is connected to VDD, some special commands are enabled.



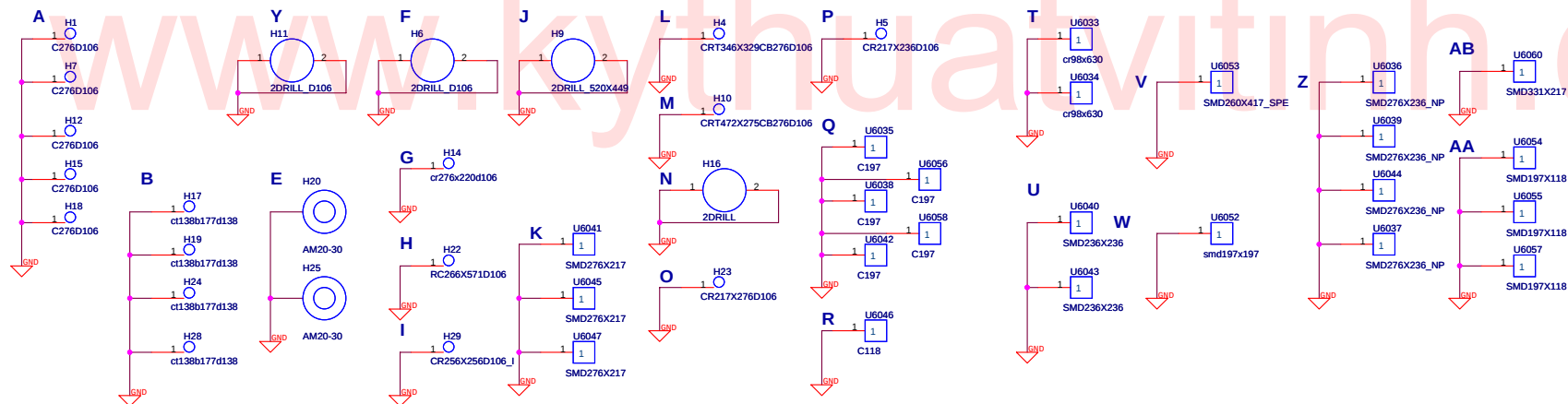
PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 (Internal)		
VGA	AD16		A
LAN	AD16	0	B
CARD READER	AD17	1	B
CARDBUS	AD19	1	C
1394	AD17	1	D
MINIPCI 2 (802.11)	AD17	3	D,C

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
Thermal Sensor (CPU)	1001100x (98)
Thermal Sensor (VGA)	1001101x (9A)

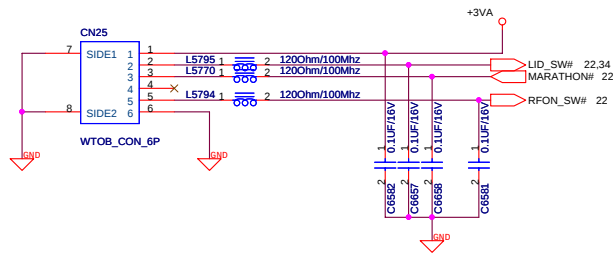
ICH8-M GPIO	W7S
GPIO 0	PM_BMBUSY#
GPIO 2	PCI_INTE#
GPIO 3	PCI_INTF#
GPIO 4	PCI_INTG#
GPIO 5	PCI_INTH#
GPIO 7	WLAN_LED_ON
GPIO 8	EXT_SMI#
GPIO 11	SMBALERT#
GPIO 12	EXT_SCI_SB#
GPIO 15	STP_PCI#
GPIO 16	DPRSLPVR
GPIO 17	WLAN_ON#
GPIO 19	MEM_ID1
GPIO 20	BTLED_ON
GPIO 21	MEM_ID0
GPIO 22	MEMCLK_SET
GPIO 25	STP_CPU#
GPIO 27	BT_ON/OFF#
GPIO 29	USB_OC#5
GPIO 31	USB_OC#7
GPIO 32	CLKRUN#
GPIO 36	MEM_ID2
GPIO 37	PCB_ID0
GPIO 38	PCB_ID1
GPIO 39	PCB_ID2
GPIO 40	USB_OC#1
GPIO 41	USB_OC#2
GPIO 43	USB_OC#4
GPIO 49	CPUPWRGD
GPIO 50	PCI_REQ#1
GPIO 52	PCI_REQ#2
GPIO 54	PCI_REQ#3

ITE8511 GPIO	W7S
GPA0	LCD_BL_PWM
GPA1	FAN_PWN
GPA4	CHG_LED_UP#
GPA5	PWR_LED_UP#
GPA7	LCD_BACKOFF#
GPB1	CAP_LED
GPB2	TP_LED_CTRL
GPB3	SMBEC0_CLK
GPB4	SMBEC0_DAT
GPB5	A20GATE
GPB6	RC_IN#
GPB7	THRO_CPU
GPC1	SMBEC1_CLK
GPC2	SMBEC1_DAT
GPC4	ACIN_OC#
GPC5	MUTE_POP_GPIO#
GPC6	BAT_IN_OC#
GPD0	SLP_S3#_R
GPD1	SLP_S4#_R
GPD2	BUF_PLT_RST#
GPD3	EXT_SCI#
GPD4	RFON_SW#
GPD6	FAN0_TACH
GPE2	MARATHON#
GPE4	PWR_ON#
GPE7	PM_CLKRUN#
GPF4	TPAD_CLK
GPF5	TPAD_DAT
GPG0	FA16
GPG1	FA17
GPG2	FA18
GPG3	FA19
GPG4	LID_SW#
GPG7	AC_APR_UC#
GPH0	VSUS_ON
GPH1	SUS_PWRGD
GPH2	CPU_PWRGD
GPH3	PM_PWRBTN#
GPH4	SUSC_ON
GPH5	SUSB_ON
GPH6	CPU_VRON
GPH7	PM_RSMRST#
GP10	ICH8_PWROK
GP11	ALL_SYSTEM_PWRGD
GP13	CHG_EN#
GP14	PRECHG
GP15	EC_CLK_EN
GP16	BAT_LEARN
GPJ4	PS_CPPE#
GPJ5	PS_SHDN#
GPM0	EXT_SMI#

SCREW HOLE



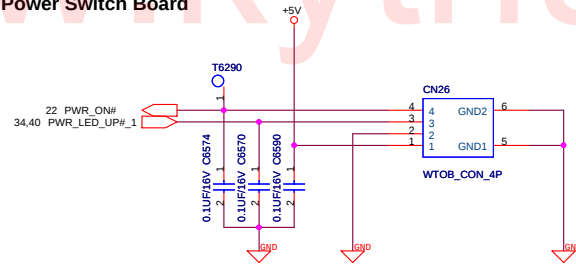
LID_SW_Board



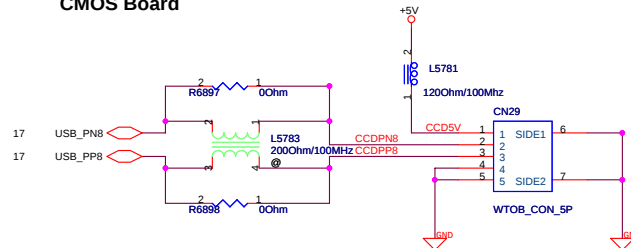
RFON_SW#(RF OFF)

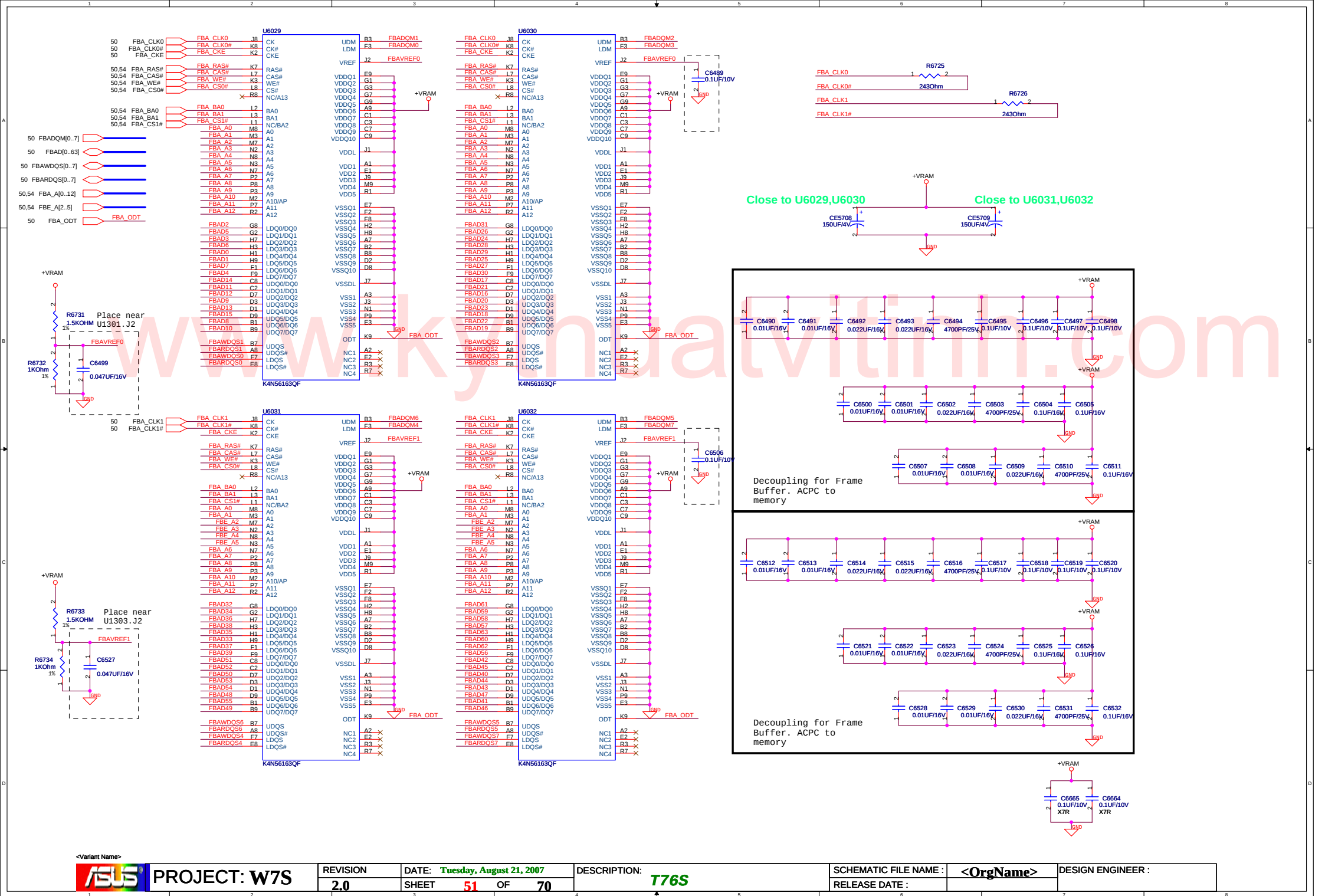
 right off ---> high
 left on ---> low

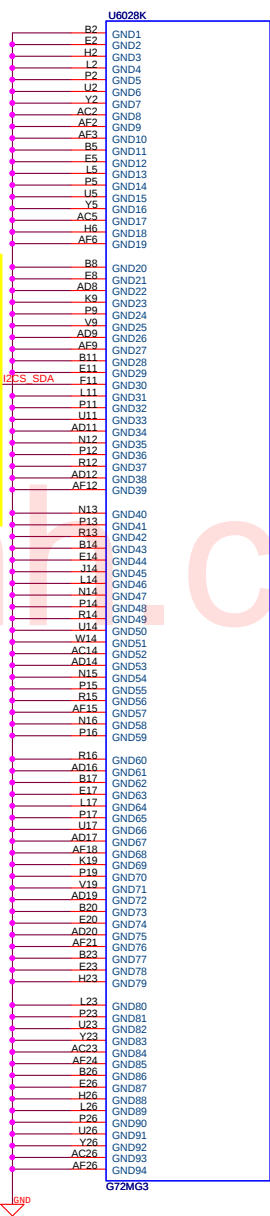
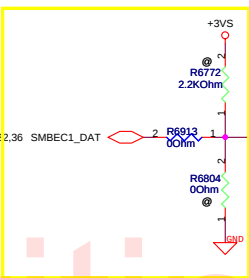
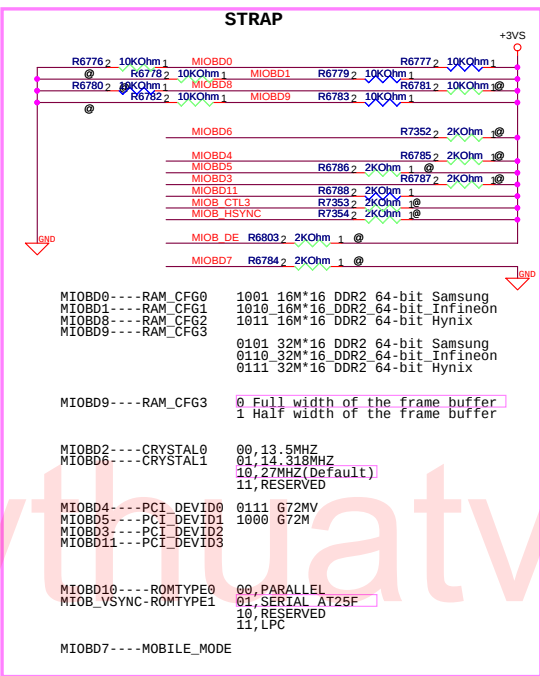
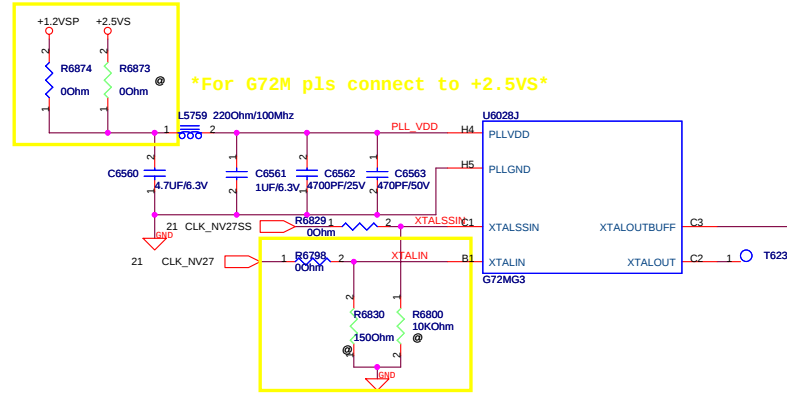
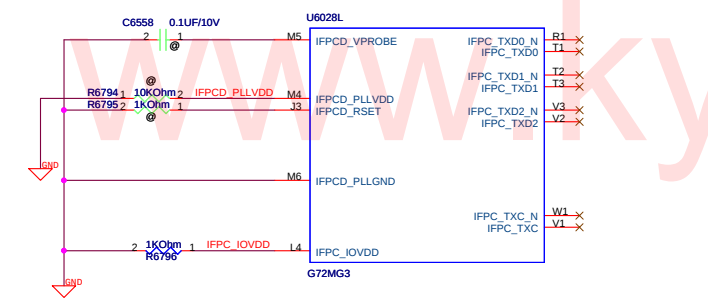
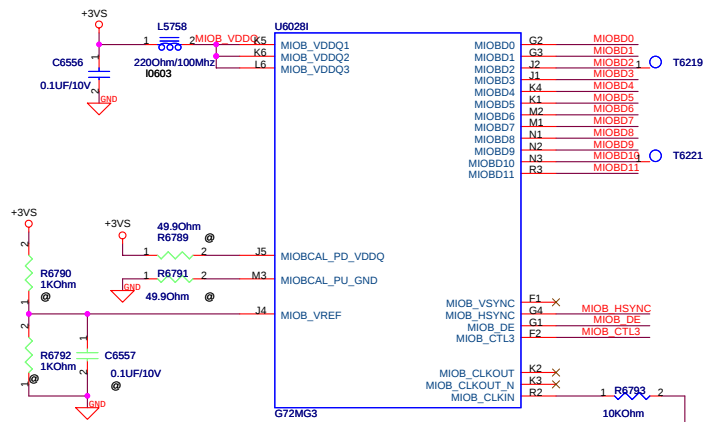
Power Switch Board



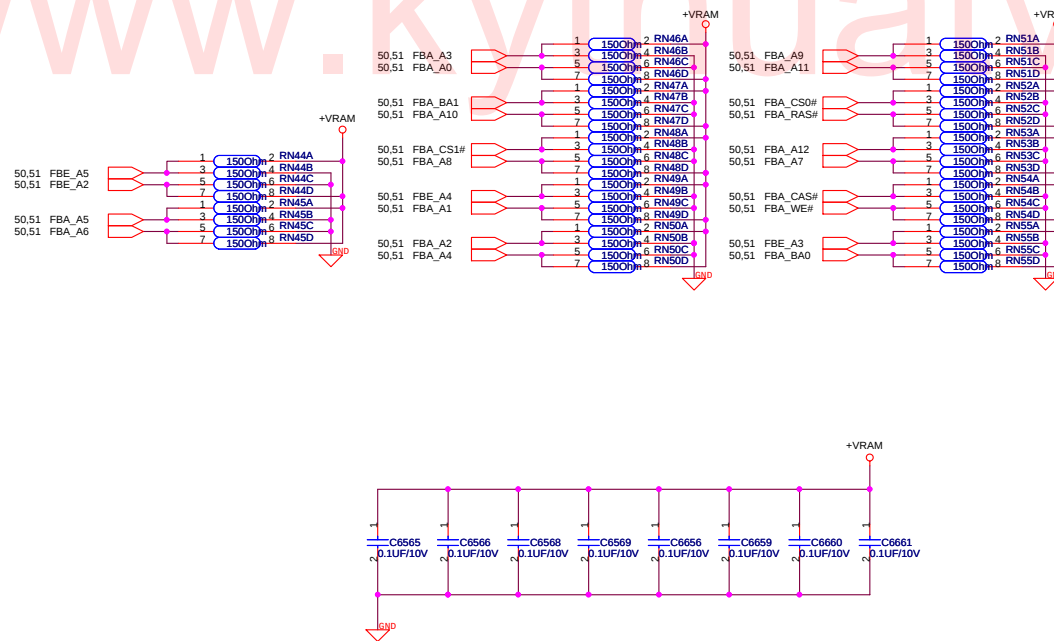
CMOS Board







FBA CMD/ADDR Termination

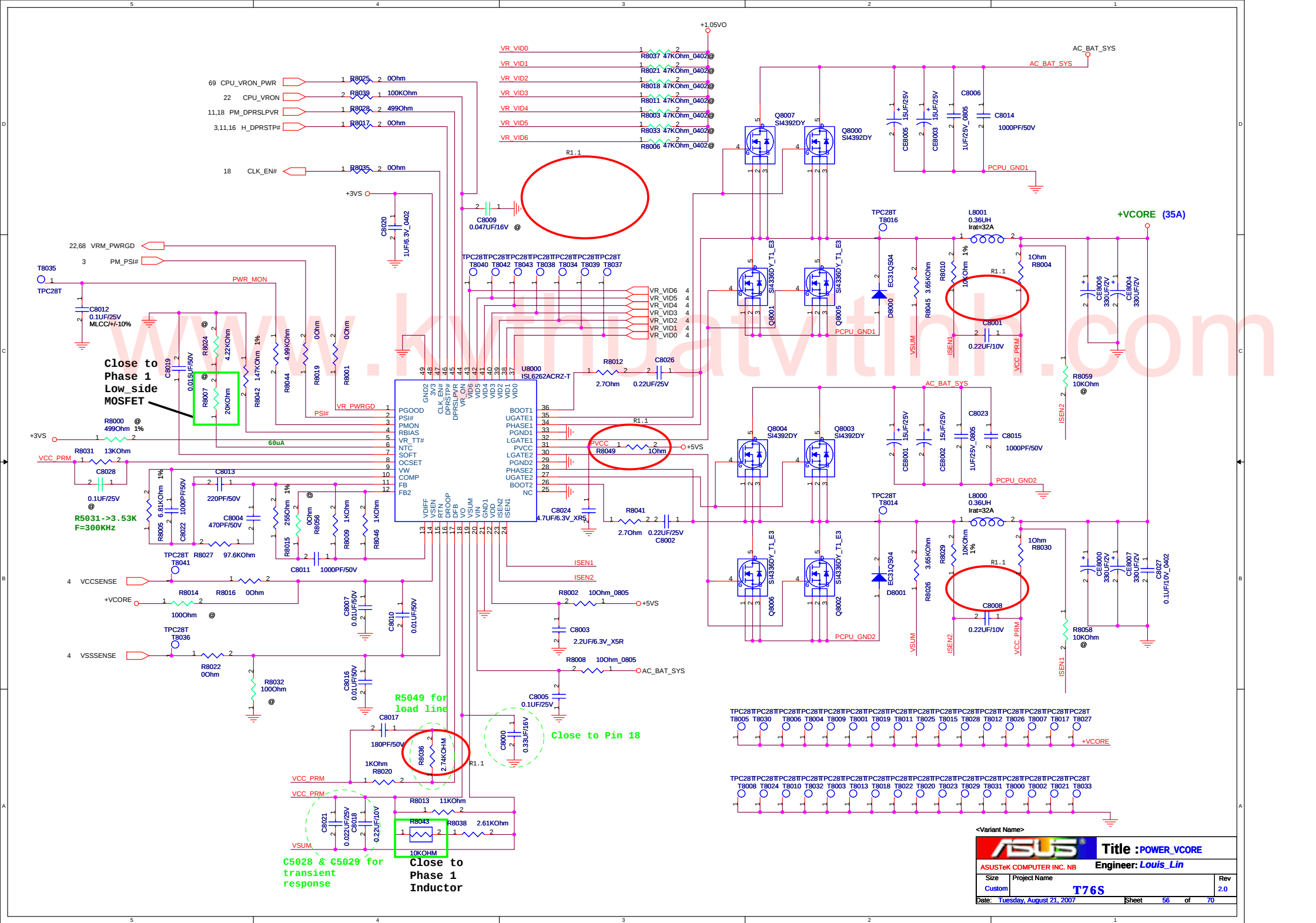


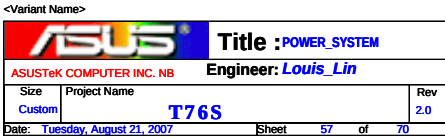
<Variant Name>

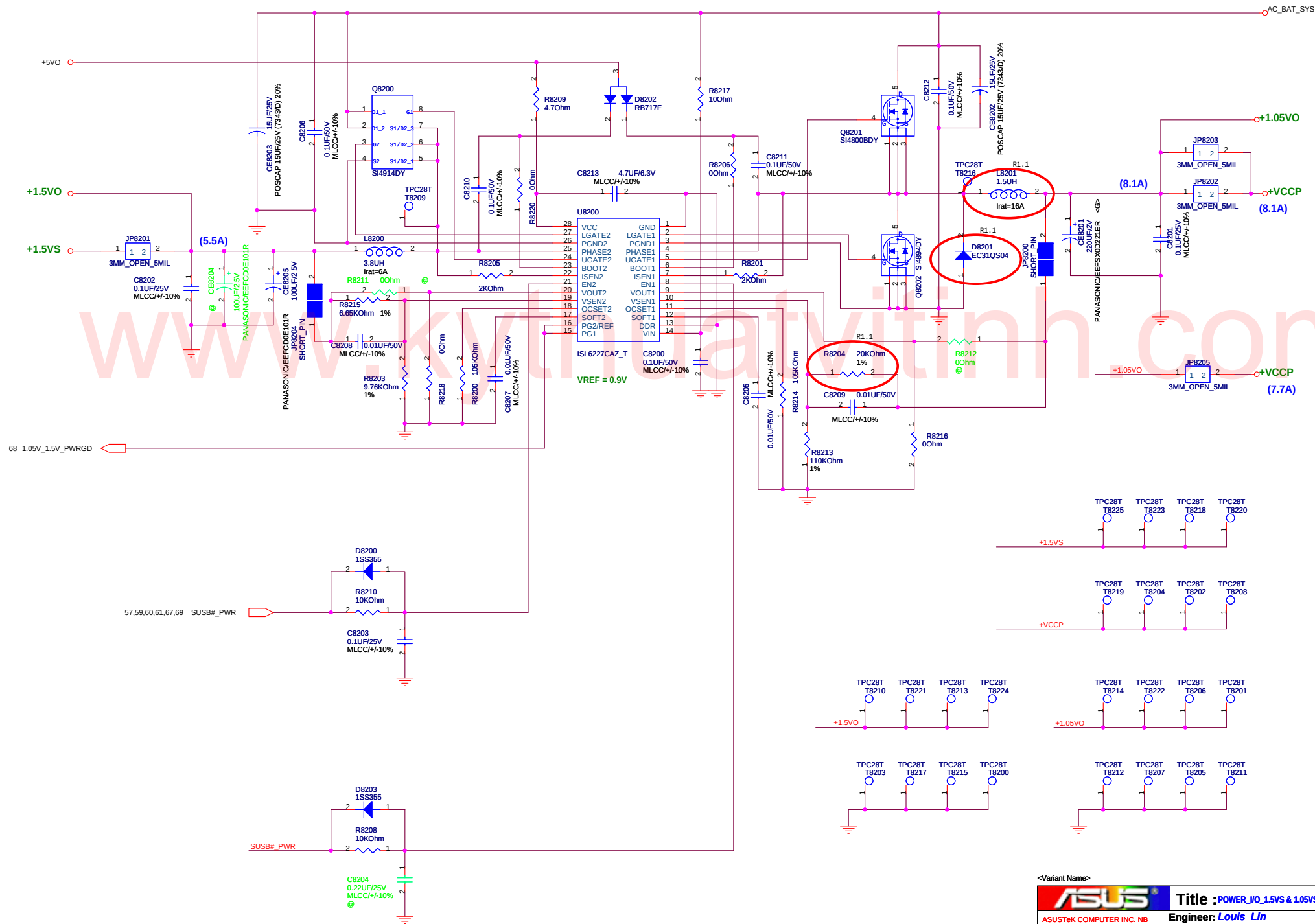
ASUS		Title VGA-Terminator	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	T76S	2.0	
Date: Tuesday, August 21, 2007		Sheet	54 of 70

Rev	Date	Description
R1.0	2006/10/25	1. Initial release.
R1.1	2007/01/12	1. Change R6316 to 390 ohm page.21 2. Add R6662 and NET NV_OVERT# page.22 3. Del R6026 Add D6044,D6045,R6988 and R6990 page.28 4. Add R6989 page.29 5. Add R691 page.30 6. Add R6415 page.39 7. Add R6471 and Q6475 page.41 8. Add R6912 page.49 9. Change R6731,R6733 to 1.5Kohm and R6725, R6726 to 243ohm page.51 10. Add R6916 page.52 11. Add R6913 page.53
R2.0	2007/03/14	1. Add R6805 page.18 2. Change R6316 to 270 ohm page.21 3. Add R6628 page.28 4. Add R7381,Q6487 page.32 5. Change Q6483,Q6484,Q6485 to ESD protect device page.32 6. Change R6987 to 0 ohm page.35 7. Change R6859 pull high to +3VA page.36 8. Del C6595 page.49

Rev	Date	Description



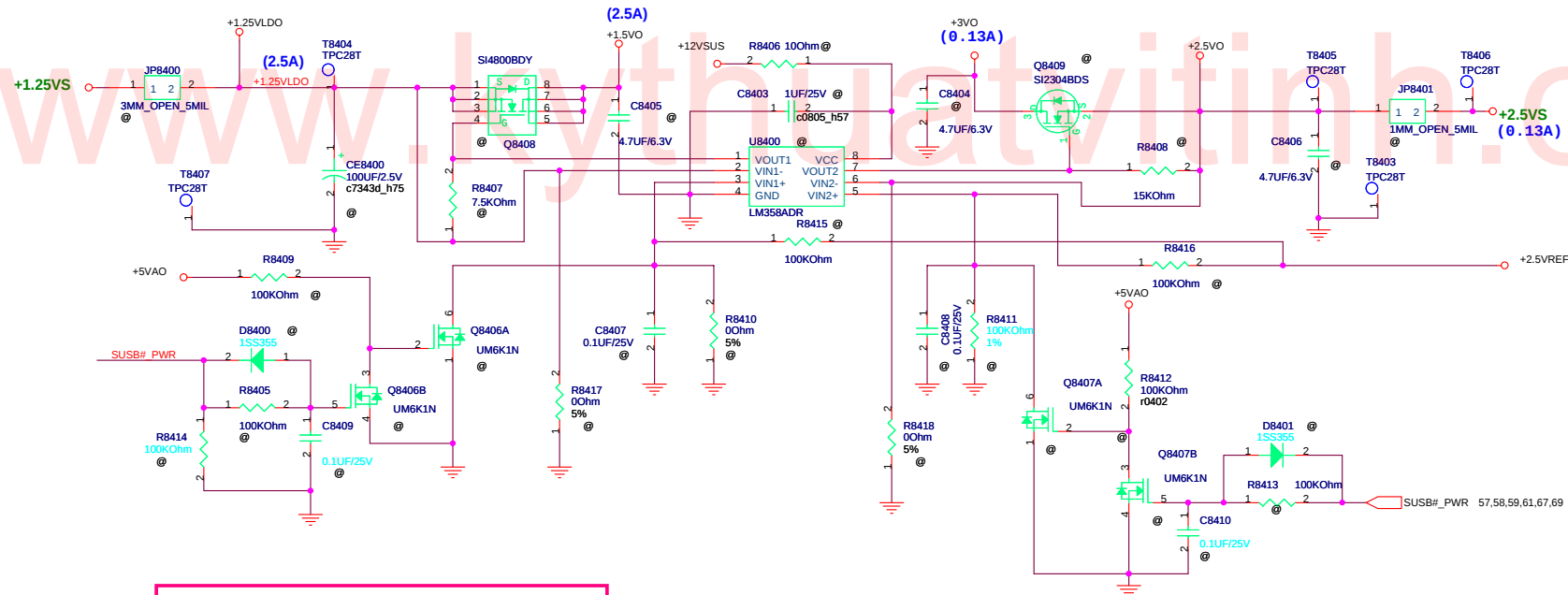




<Variant Name>

ASUS		Title : POWER_W0_1.5VS & 1.05VS	
ASUSTeK COMPUTER INC. NB		Engineer: Louis_Lin	
Size	Project Name	T76S	Rev 2.0
Custom			
Date: Tuesday, August 21, 2007		Sheet	58 of 70

+1.25VS & +2.5VS



UMA Enable +1.25VS
R8417 UNMOUNT, R8410 100K 10G212100314010

Discrete V6A Disable +1.25VS
R8417 MOUNT, R8410 0 ohm 10G212000004030
And other UNMOUNT.

R8414, D8400, C8409 Always Keep UNMOUNT

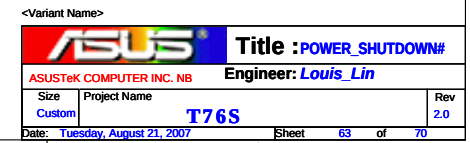
<Variant Name>

ASUS		Title : POWER_I/O_+1.25VS&+2.5VS	
ASUSTeK COMPUTER INC. NB		Engineer: Louis_Lin	
Size	Project Name		
Custom		Rev 2.0	
Date: Tuesday, August 21, 2007		Sheet 60	of 70

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<Variant Name>

		Title : N/A	
ASUSTeK COMPUTER INC. NB		Engineer: Louis_Lin	
Size B	Project Name T76S		Rev 2.0
Date: Tuesday, August 21, 2007		Sheet 62 of 70	

[illegible]

POWER PATH & BAT_LEARN

AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active

1011

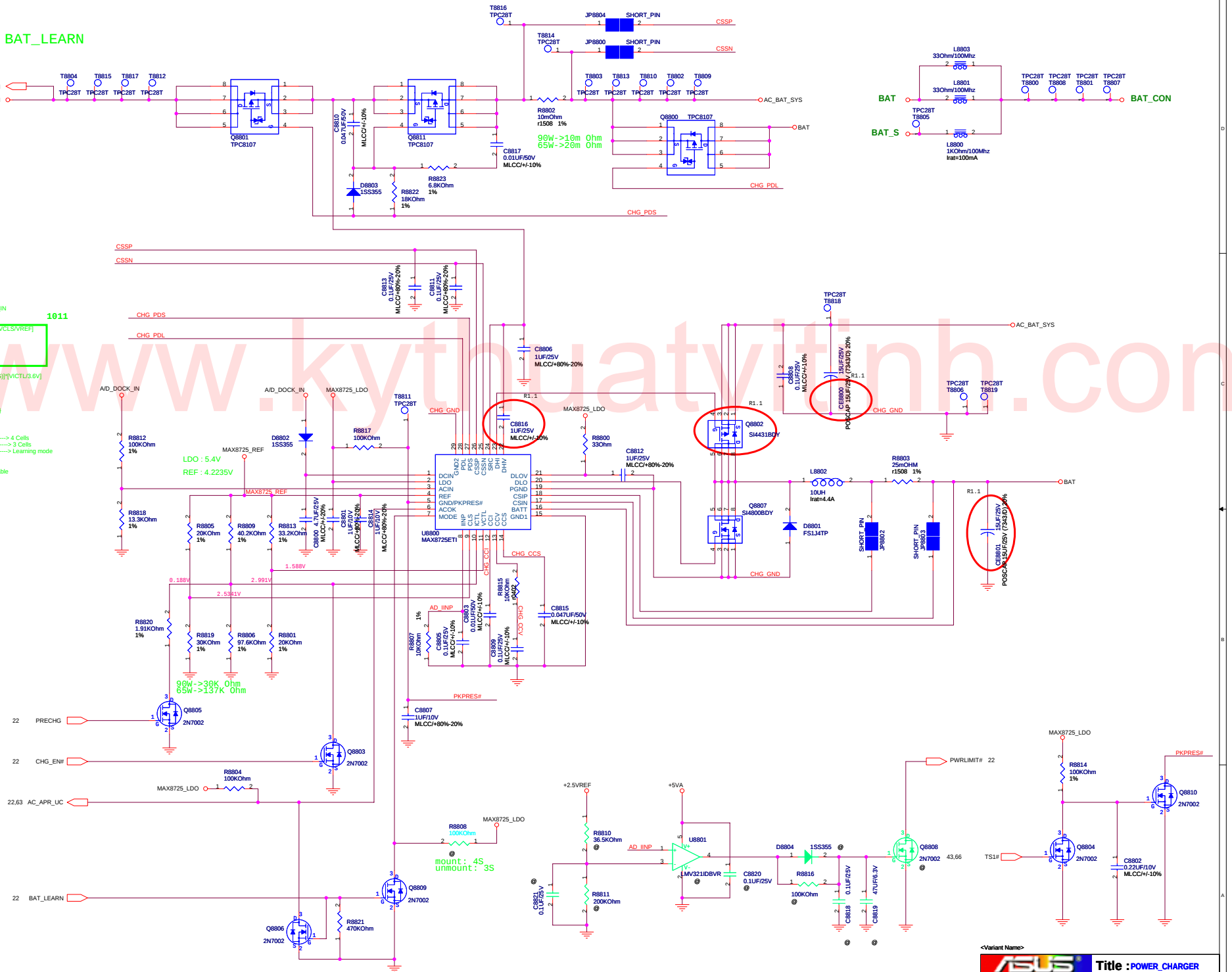
Adapter Im(max) = [0.075V/Rsense(Adm)] * [VCLSVREF]
Rsense(Adm) = 0.010ohm
VCLSV = 2.5341V
=> Im(max) = 4.5A
=> Constant Power = 19 * 4.5 = 85.5W
=> R8805 = 20K R8819 = 30K

Charge Current Ichg = [0.075V/Rsense(CHG)] * [VICTL3.6V]
Rsense(CHG) = 0.025 ohm
VICTL = 3V => Ichg = 2.5A
VICTL = 1.08V => Ichg = 1.4A
Vbatt = Cell * Vref - [(VCTL - 1.8V) / 9.52]
VCTL = 1.588V
=> Vbatt = 4.2V

Mode pin : Vmode > 2.8V (tie to LDO pin) -> 4 Cells
2.0 > Vmode > 1.6V (floating) -> 3 Cells
0.8 > Vmode (tie to GND) -> Learning mode

VICTL < 0.8V or DCIN < 7V -> Charger Disable

Precgare current = 150mA



<Variant Name>

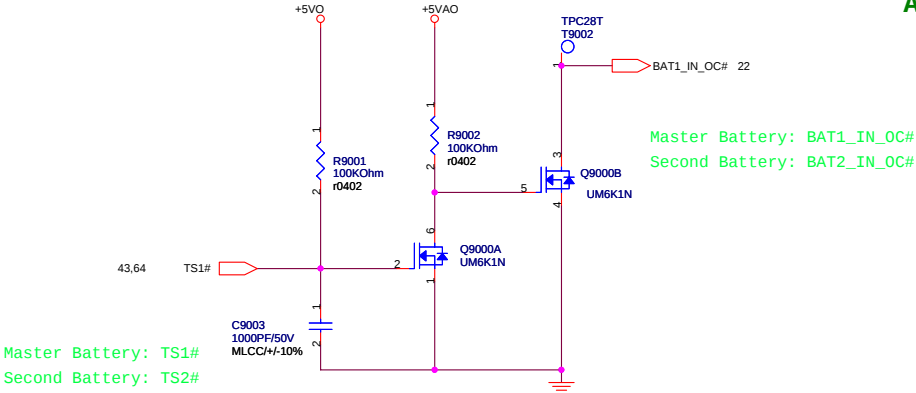
ASUS		Title : POWER_CHARGER	
ASUSTeK COMPUTER INC. NB		Engineer: Louis Lin	
Size	Project Name	Rev	
C	T76S	2.0	
Date: Tuesday, August 21, 2007	Sheet	64	of 70

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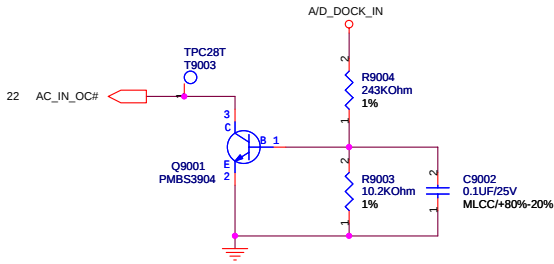
<Variant Name>

		Title : N/A	
ASUSTeK COMPUTER INC. NB		Engineer: Louis_Lin	
Size	Project Name	Rev	
Custom	T76S	2.0	
Date: Tuesday, August 21, 2007		Sheet	65 of 70

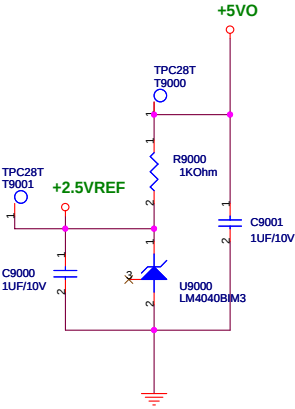
BATTERY IN DETECT



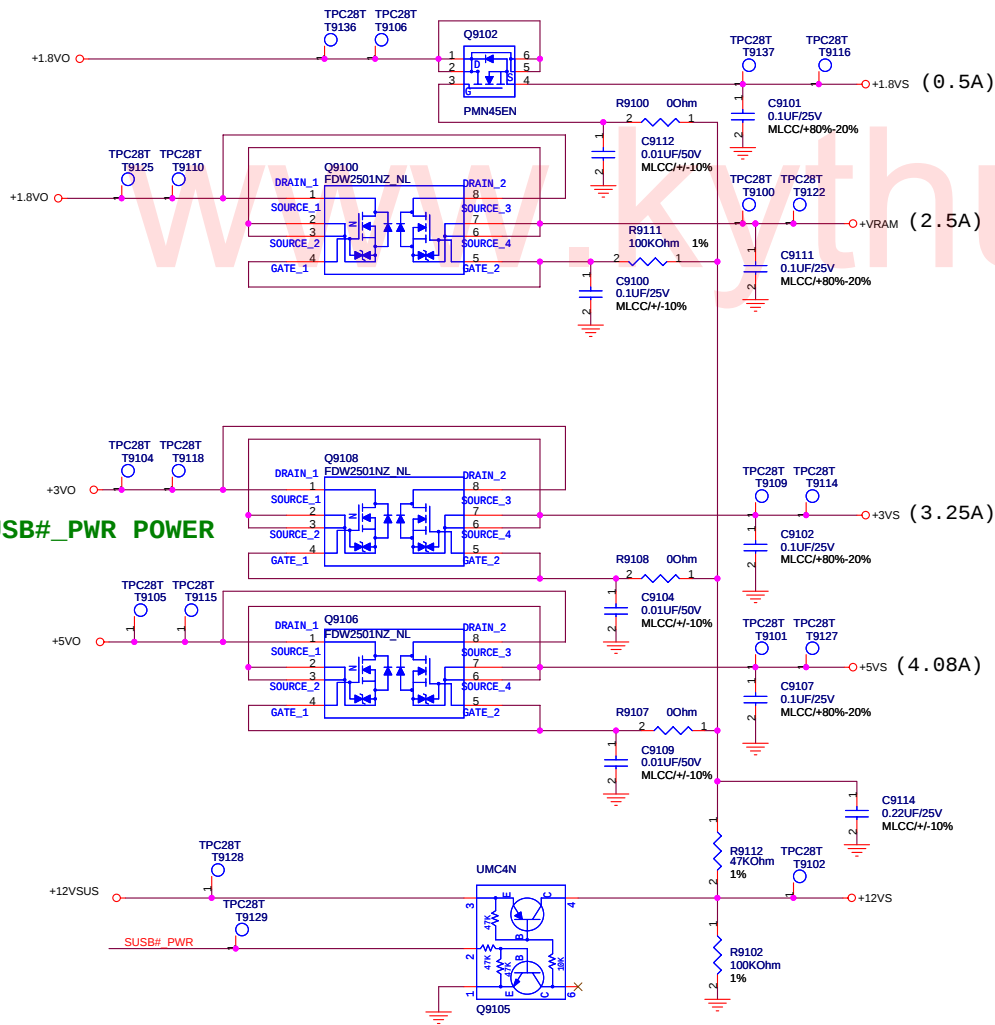
ADAPTER IN DETECT



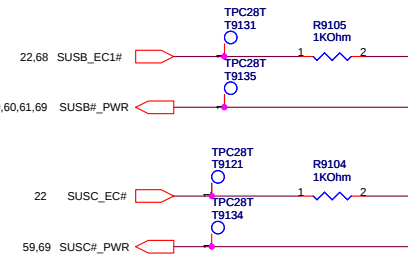
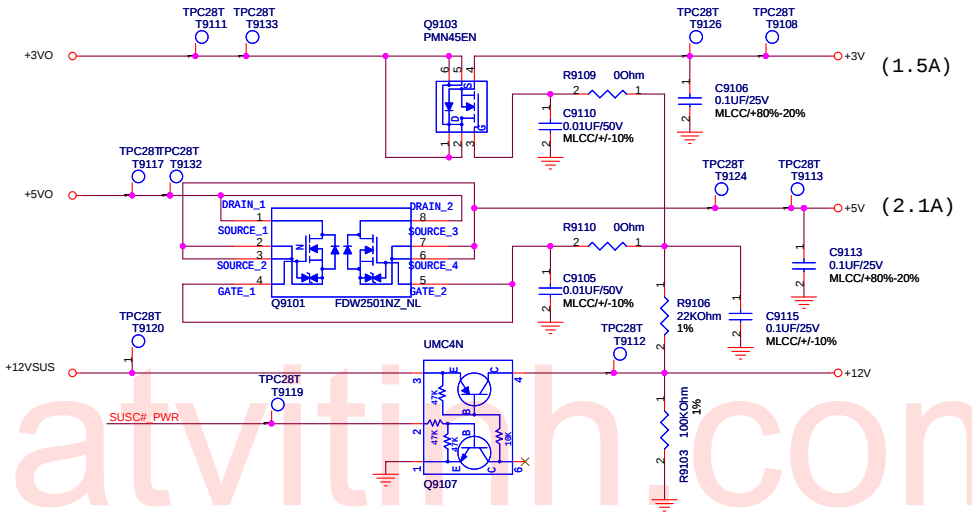
+2.5VREF



SUSB#_PWR POWER



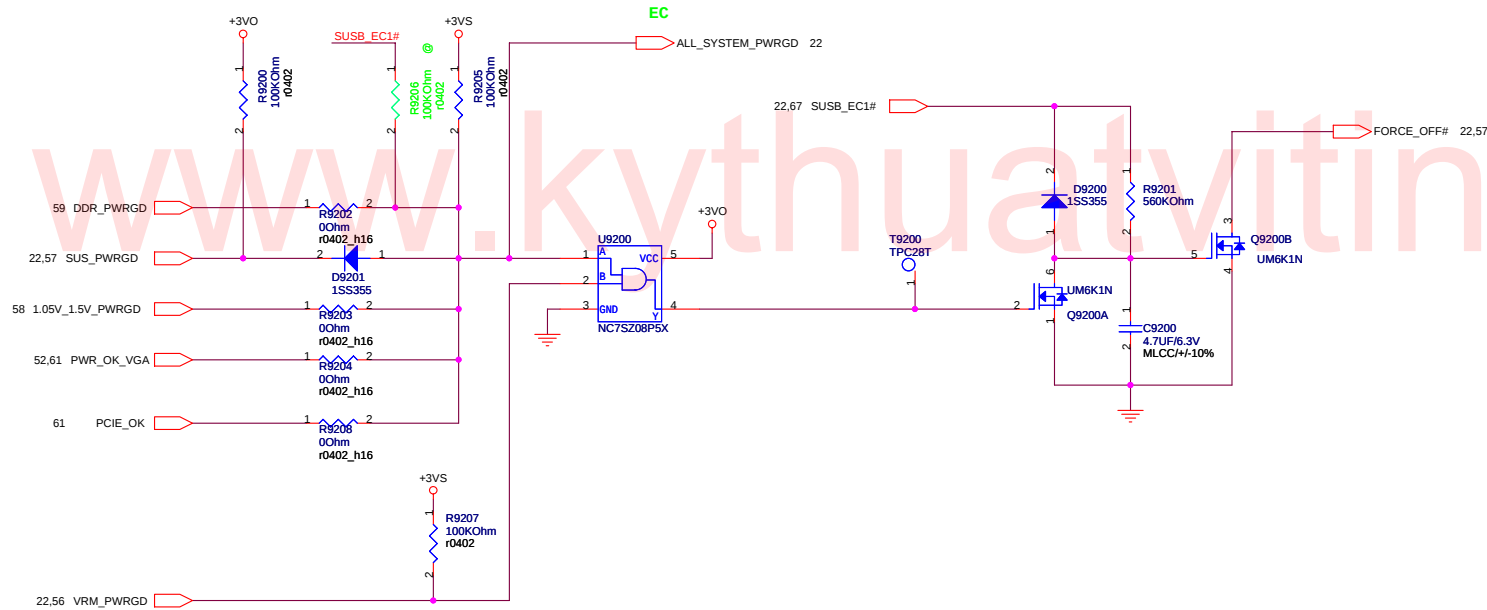
SUSC#_PWR POWER



<Variant Name>

ASUS		Title :POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC. NB		Engineer: <u>Louis_Lin</u>	
Size Custom	Project Name T76S		Rev 2.0
Date: Tuesday, August 21, 2007		Sheet	67 of 70

POWER GOOD DETECTOR

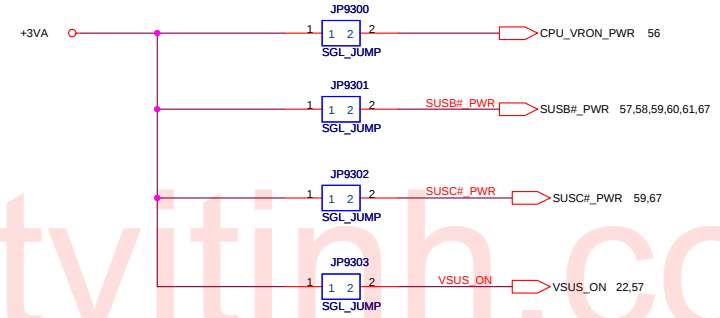


<Variant Name>

ASUS		Title :POWER_PROTECT	
ASUSTeK COMPUTER INC. NB		Engineer: Louis_Lin	
Size Custom	Project Name T76S	Rev 2.0	
Date: Tuesday, August 21, 2007		Sheet	68 of 70

AC_BAT_SYS	AC_BAT_SYS	34,56,57,58,59,61,63,64
BAT	BAT	64
BAT_CON	BAT_CON	43,64
+2.5VREF	+2.5VREF	60,63,64,66
+3VA	+3VA	16,22,43,48,57
+5VAO	+5VAO	57,60,61,66
+5VO	+5VO	57,58,59,61,66,67
+5VSUS	+5VSUS	19,57,63
+5V	+5V	9,26,28,38,40,41,48,67
+5VS	+5VS	19,20,23,26,28,29,35,36,37,40,41,56,67
+3VO	+3VO	57,60,61,67,68
+3VSUS	+3VSUS	17,18,19,22,24,28,57
+3V	+3V	17,25,33,37,39,41,44,67
+3VS	+3VS	3,8,11,14,15,16,18,19,20,21,22,24,26,28,30,31,32,33,34,35,36,37,39,41,42,45,49,52,53,56,67,68
+12VSUS	+12VSUS	57,60,67
+12V	+12V	18,28,32,67
+12VS	+12VS	45,67
+1.8VO	+1.8VO	59,67
+1.8V	+1.8V	6,7,8,9,11,13,14,41,59
+1.8VS	+1.8VS	52,67
+0.9VS	+0.9VS	9,59
+0.9VO	+0.9VO	59
+1.05VO	+1.05VO	56,58
+VCCP	+VCCP	3,4,5,10,11,13,14,16,19,21,41,58
+1.5VO	+1.5VO	58,60
+1.5VS	+1.5VS	4,14,16,17,19,33,39,41,58
+2.5VO	+2.5VO	60
+2.5VS	+2.5VS	41,52,53,60
+VCORE	+VCORE	4,5,56
+VGA_VCORE	+VGA_VCORE	49,61
+VRAM	+VRAM	50,51,54,67
+1.2VSP	+1.2VSP	41,49,50,53,61
+1.25VS	+1.25VS	11,14,19,60,61

FOR POWER TEST



<Variant Name>

ASUS		Title :POWER_SIGNAL	
ASUSTeK COMPUTER INC. NB		Engineer: <u>Louis_Lin</u>	
Size Custom	Project Name T76S		Rev 2.0
Date: <u>Tuesday, August 21, 2007</u>		Sheet <u>69</u> of <u>70</u>	

Non - IAMT

