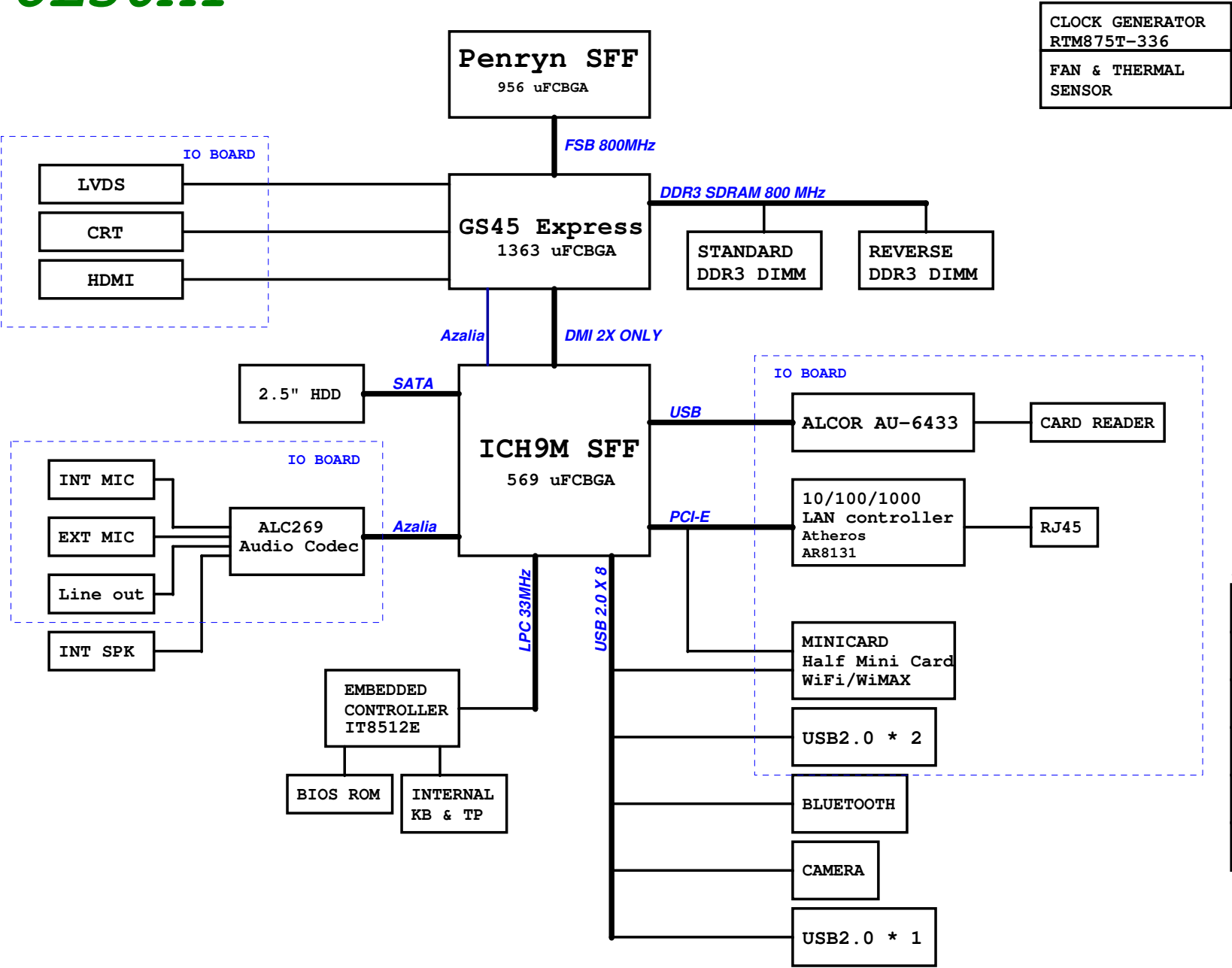


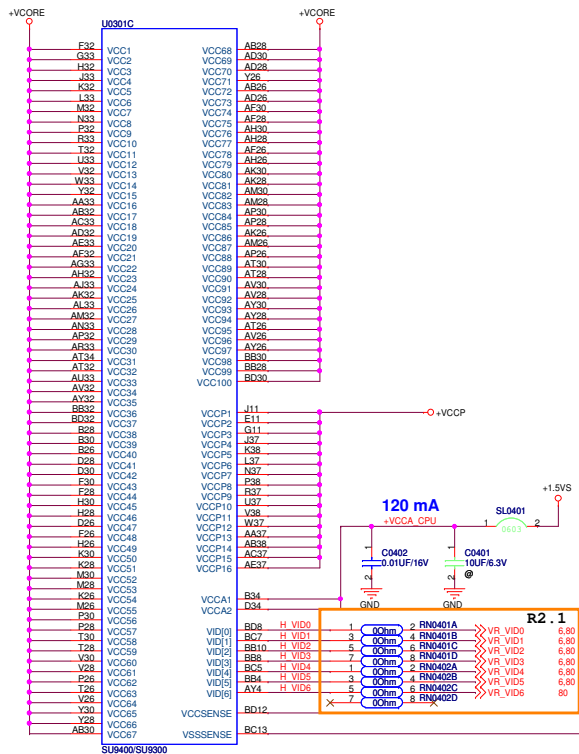
UL50AT



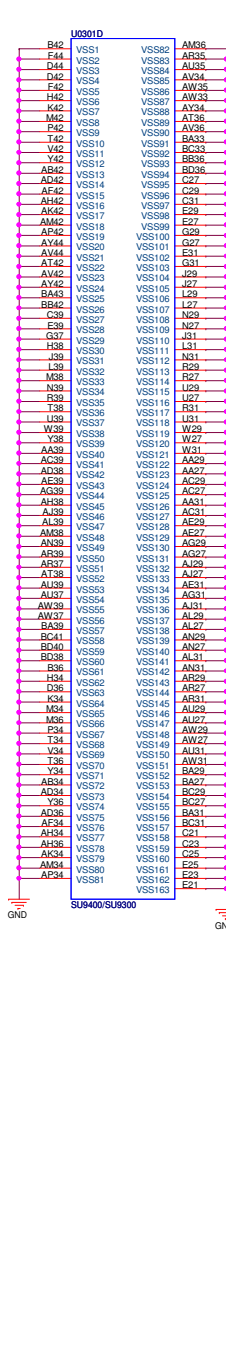
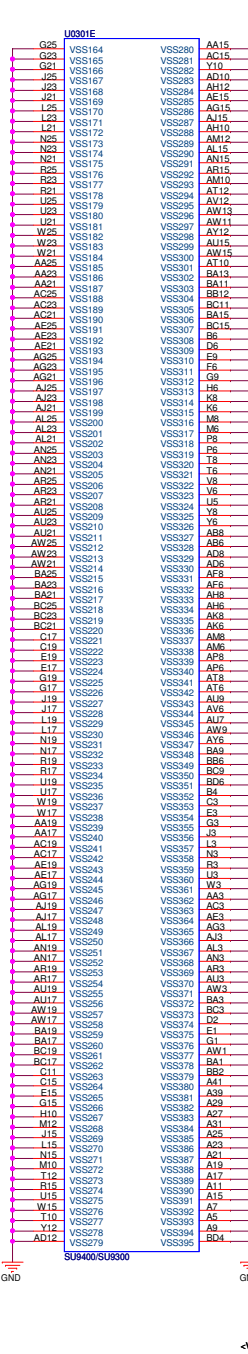
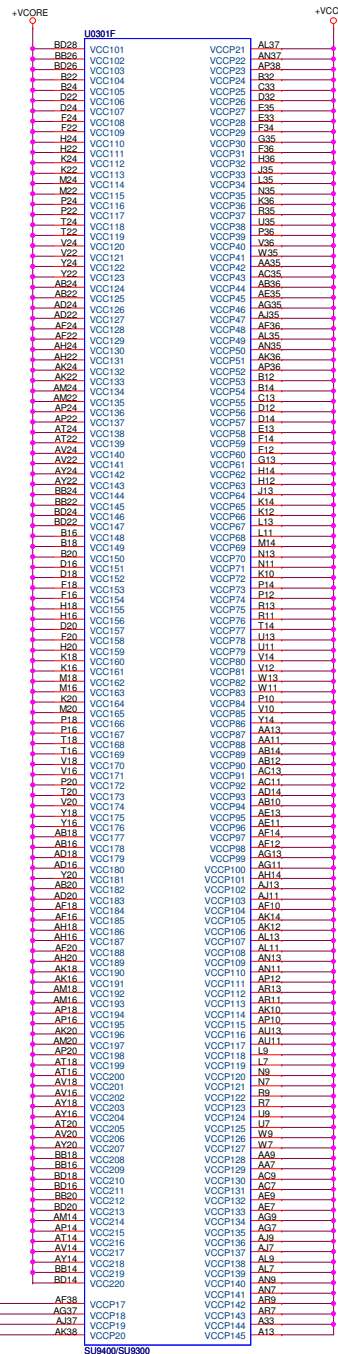
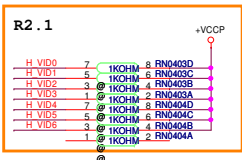
POWER

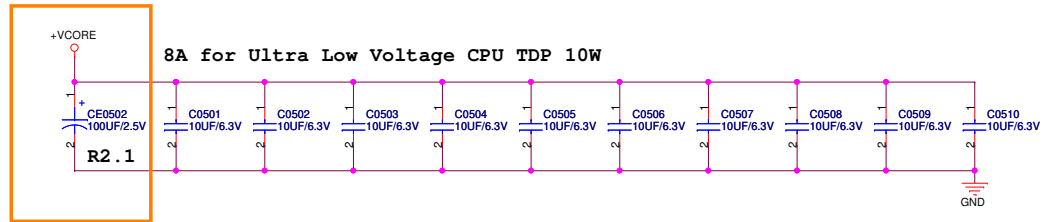
VCORE
SYSTEM
I/O_1.05VS
I/O_DDR & VTT
I/O_+1.8VS
CHARGER

[illegible][illegible]



VCCSENSE, VSSSENSE trace at 27.4 ohm with 7 mils spacing. Place PU and PD within 1" of CPU.

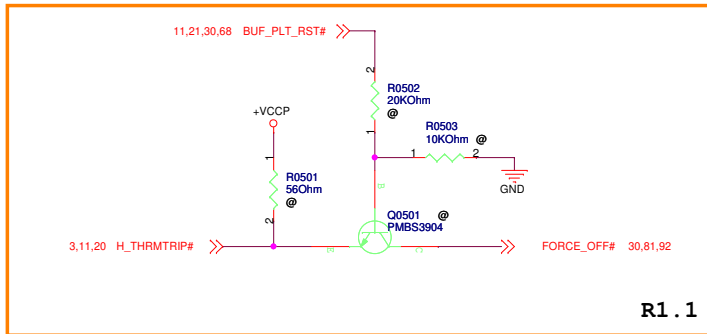
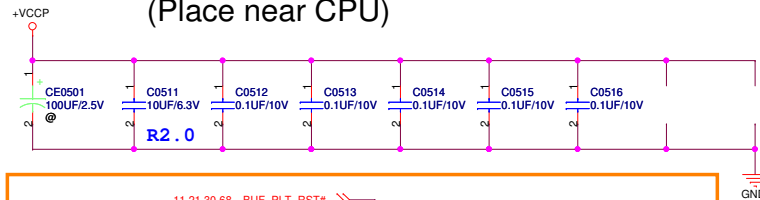




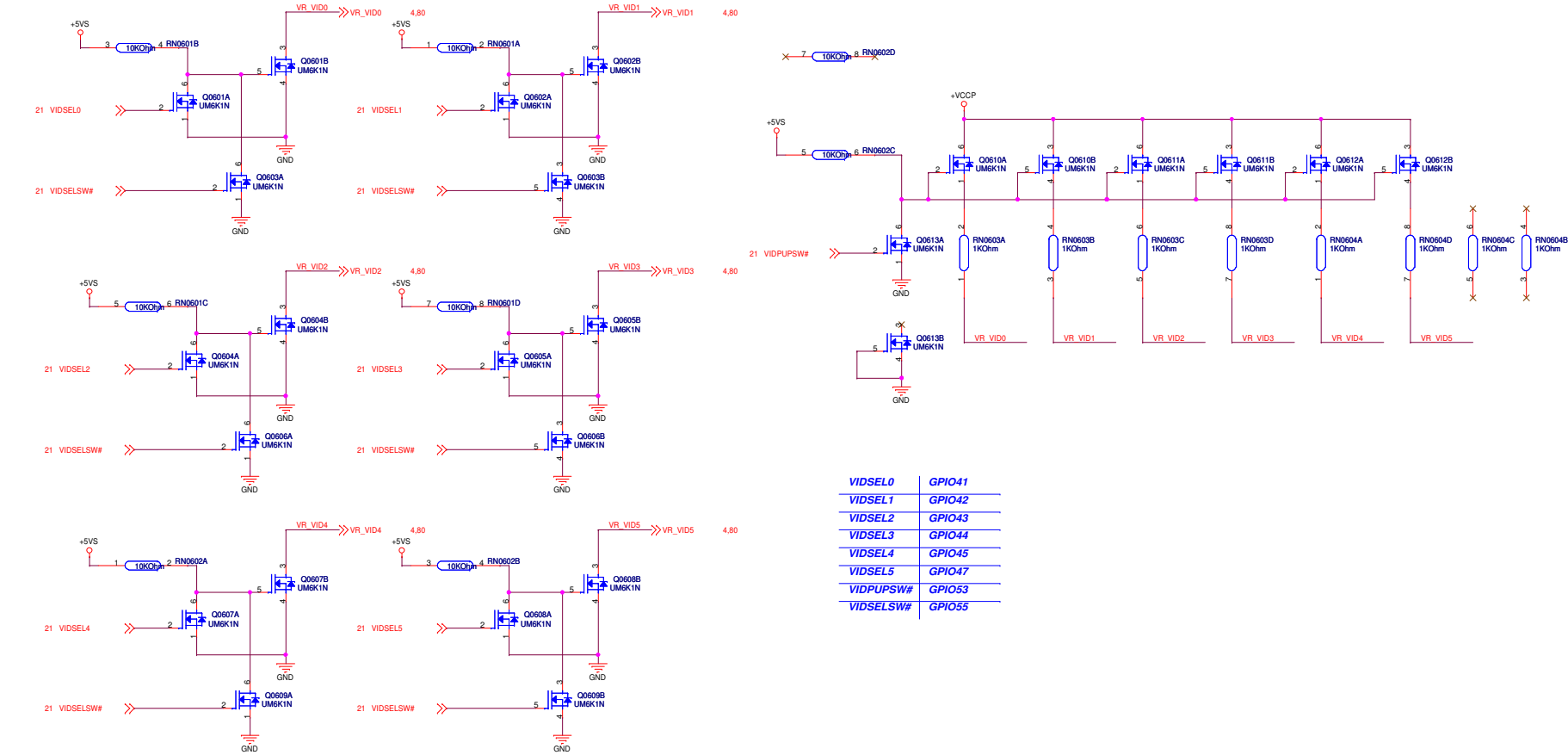
Decoupling guide from Intel

VCCORE	10uF	mount	*4pcs
	0.1uF	mount	*5pcs
VCCP	1uF		* 12pcs
	270uF		* 1pcs
VCCA	0.01uF		* 1 pcs
	10uF		* 1 pcs

+VCCP Decoupling Capacitor (Place near CPU)

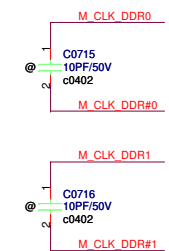


<Variant Name>



VIDSEL0	GPIO41
VIDSEL1	GPIO42
VIDSEL2	GPIO43
VIDSEL3	GPIO44
VIDSEL4	GPIO45
VIDSEL5	GPIO47
VIDPUPSW#	GPIO53
VIDSELW#	GPIO55

Place near SO-DIMM_0



13 M_A_DQS[7:0] << M_A_DQS[7:0]
13 M_A_DQS# [7:0] << M_A_DQS# [7:0]

13 M_A_DM[7:0] << M_A_DM[7:0]

8,22,24,29 SMB_CLK_S
8,22,24,29 SMB_DAT_S

11 M_CLK_DDR1
11 M_CLK_DDR#1
11 M_CLK_DDR0
11 M_CLK_DDR#0
11 M_CS#1
11 M_CS#0
11 M_ODT1
11 M_ODT0
13 M_A_WE#
13 M_A_RAS#
13 M_A_CAS#
13 M_A_BS2
13 M_A_BS1
13 M_A_BS0
11 M_CKE1
11 M_CKE0

GND

SA1

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

SA0

13 M_A_DQ[0..63] << M_A_DQ[0..63]

U0701A
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A10/AP
A12/BC#
A13
A14
A15

CK1
CK1#
CK0
CK0#
S1#
S0#

ODT1
ODT0
WE#
CAS#
BA2
BA1
BA0

CKE1
CKE0
SA1
SA0

M_A_DQS7
M_A_DQS#7
M_A_DQS6
M_A_DQS#6
M_A_DQS5
M_A_DQS#5
M_A_DQS4
M_A_DQS#4
M_A_DQS3
M_A_DQS#3
M_A_DQS2
M_A_DQS#2
M_A_DQS1
M_A_DQS#1
M_A_DQS0
M_A_DQS#0

M_A_DM7
M_A_DM6
M_A_DM5
M_A_DM4
M_A_DM3
M_A_DM2
M_A_DM1
M_A_DM0

SCL
SDA

RESET#

M_DRAMRST#

DDR3_DIMM_204P

12G02553204W

DDR3 DIMM 204P,1.5V,5.2H,REV

SWAP

SWAP

SWAP

SWAP

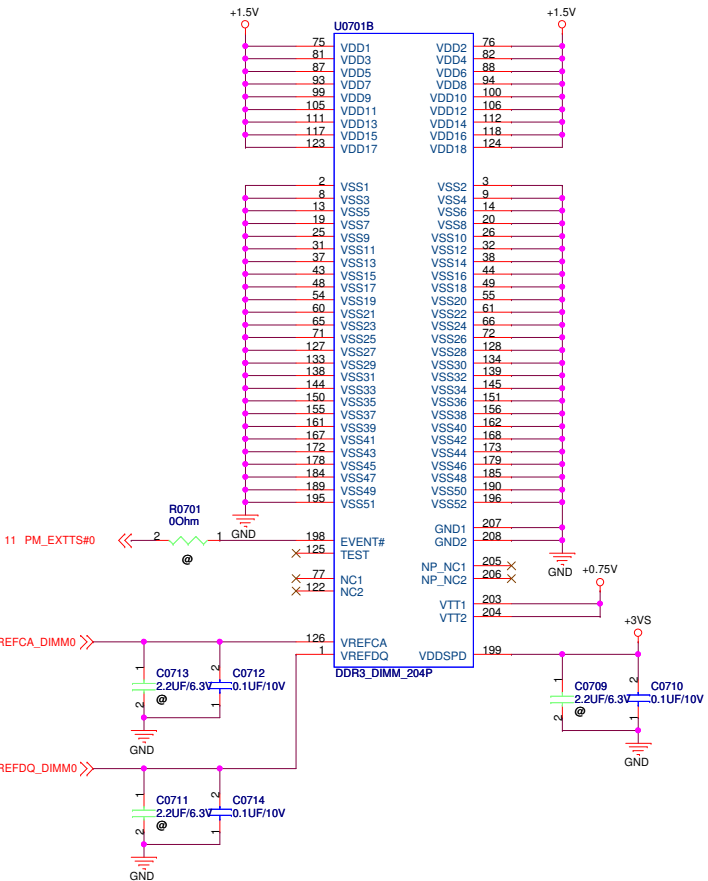
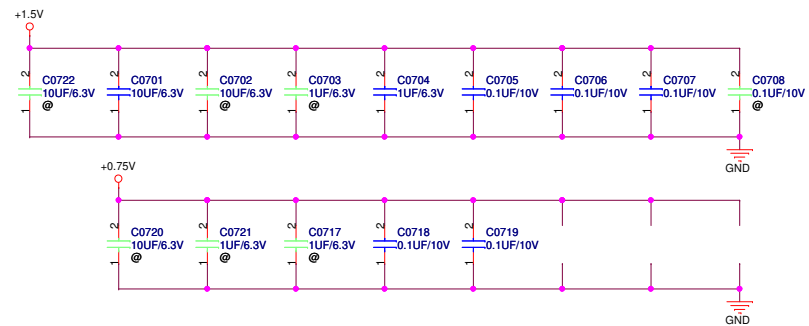
SWAP

SWAP

SWAP

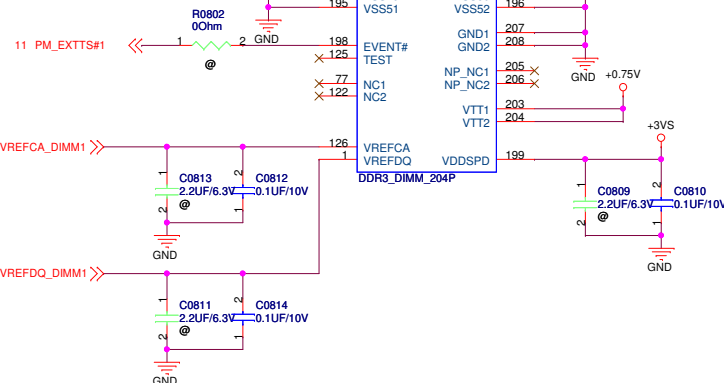
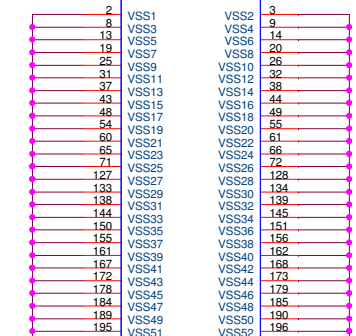
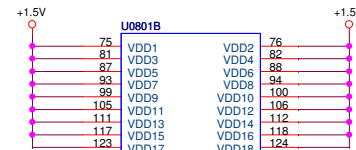
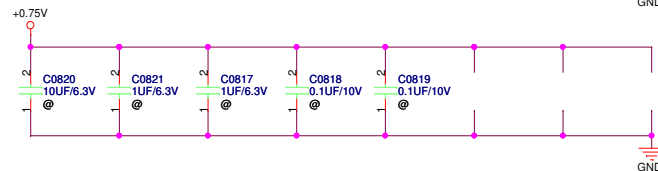
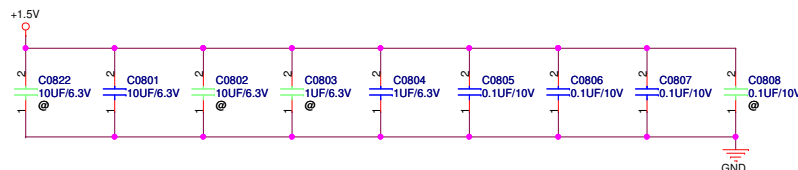
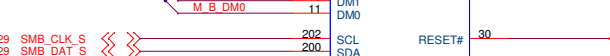
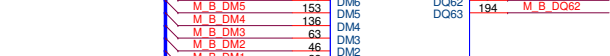
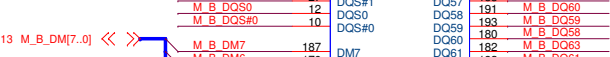
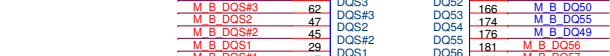
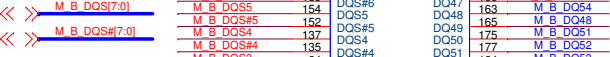
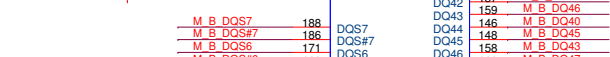
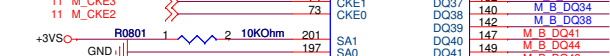
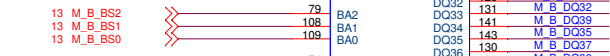
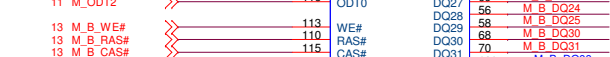
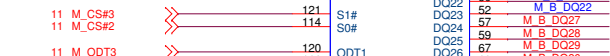
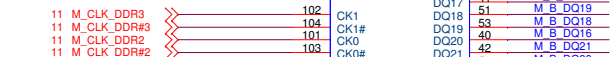
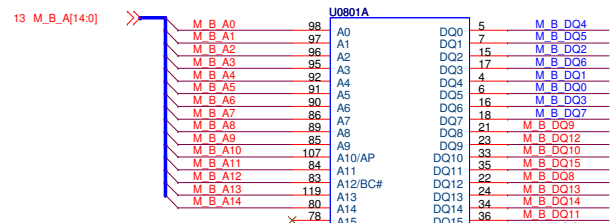
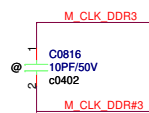
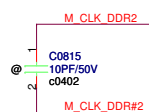
SWAP

SWAP



<Variant Name>

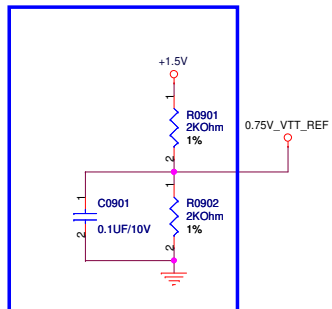
Place near SO-DIMM_1



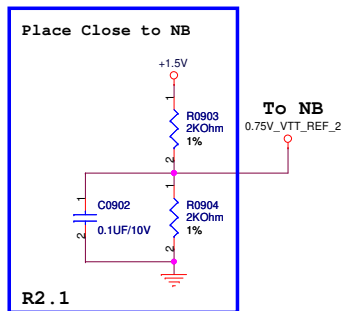
DDR3 DIMM_204P
12G02553204K
DDR3 DIMM 204P,1.5V,5.2H,STD

<Variant Name>

R2.1

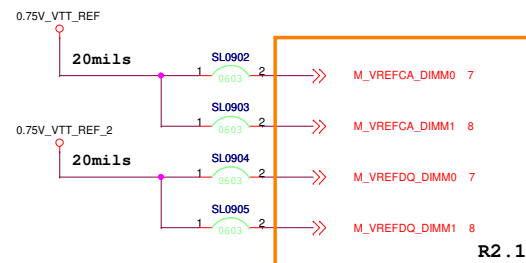
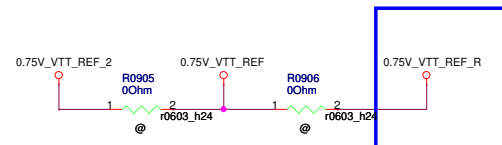


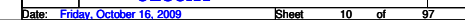
Place Close to NB

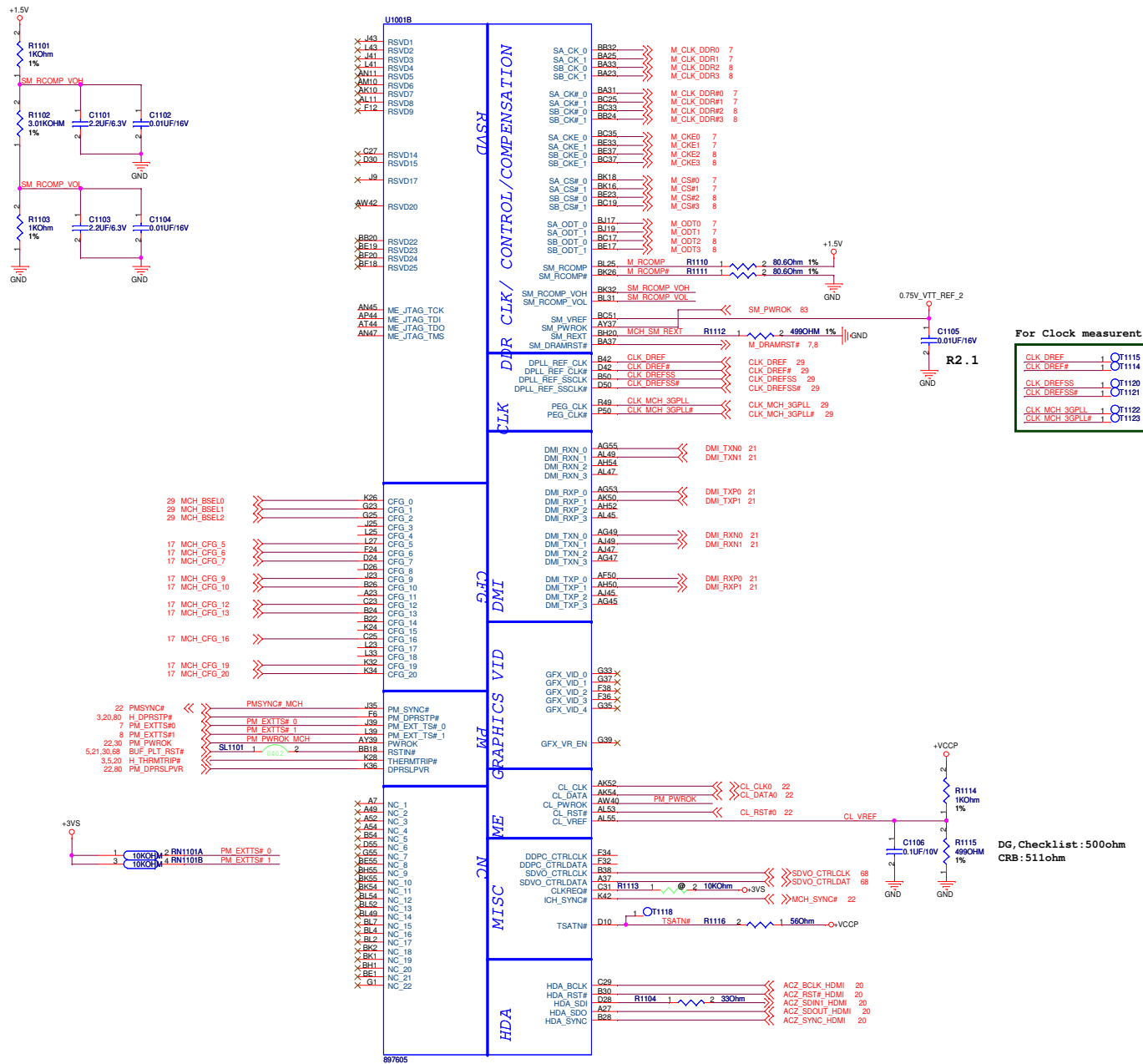


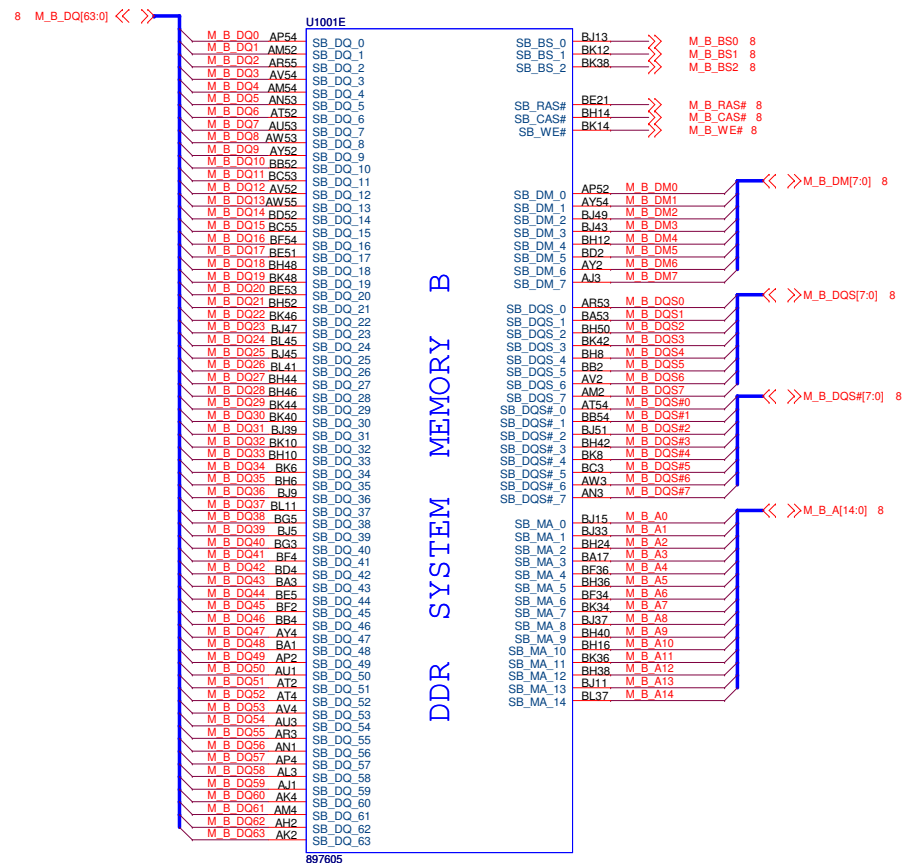
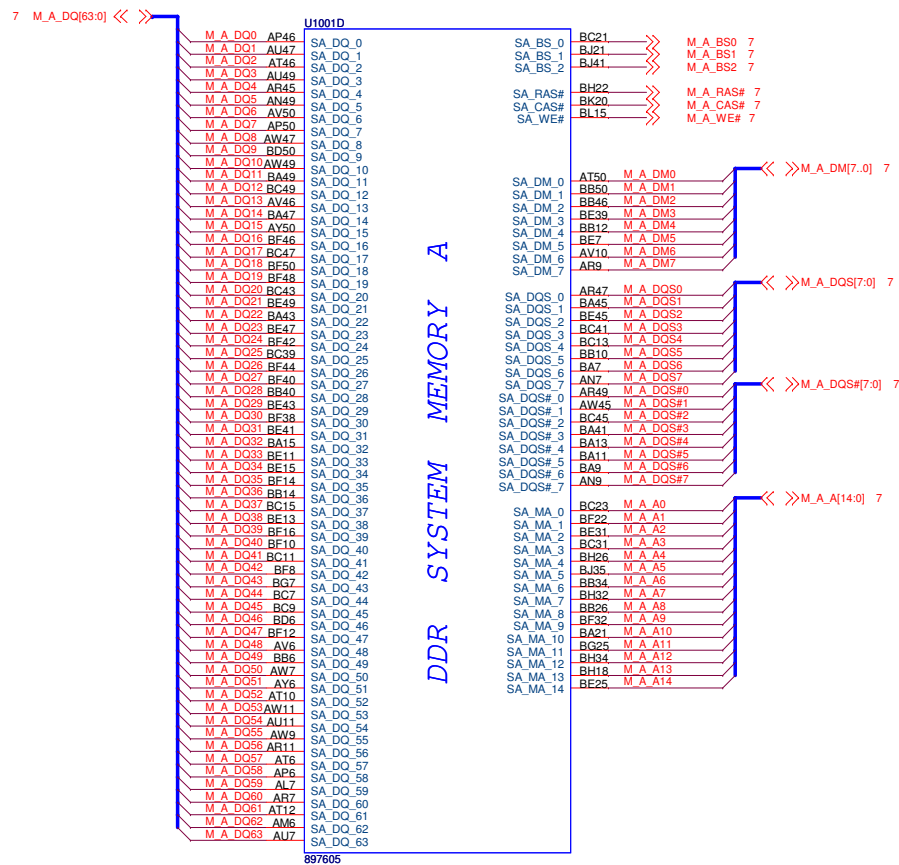
R2.1

From DDR/VTT Power Circuit









+1.5V_GMCH

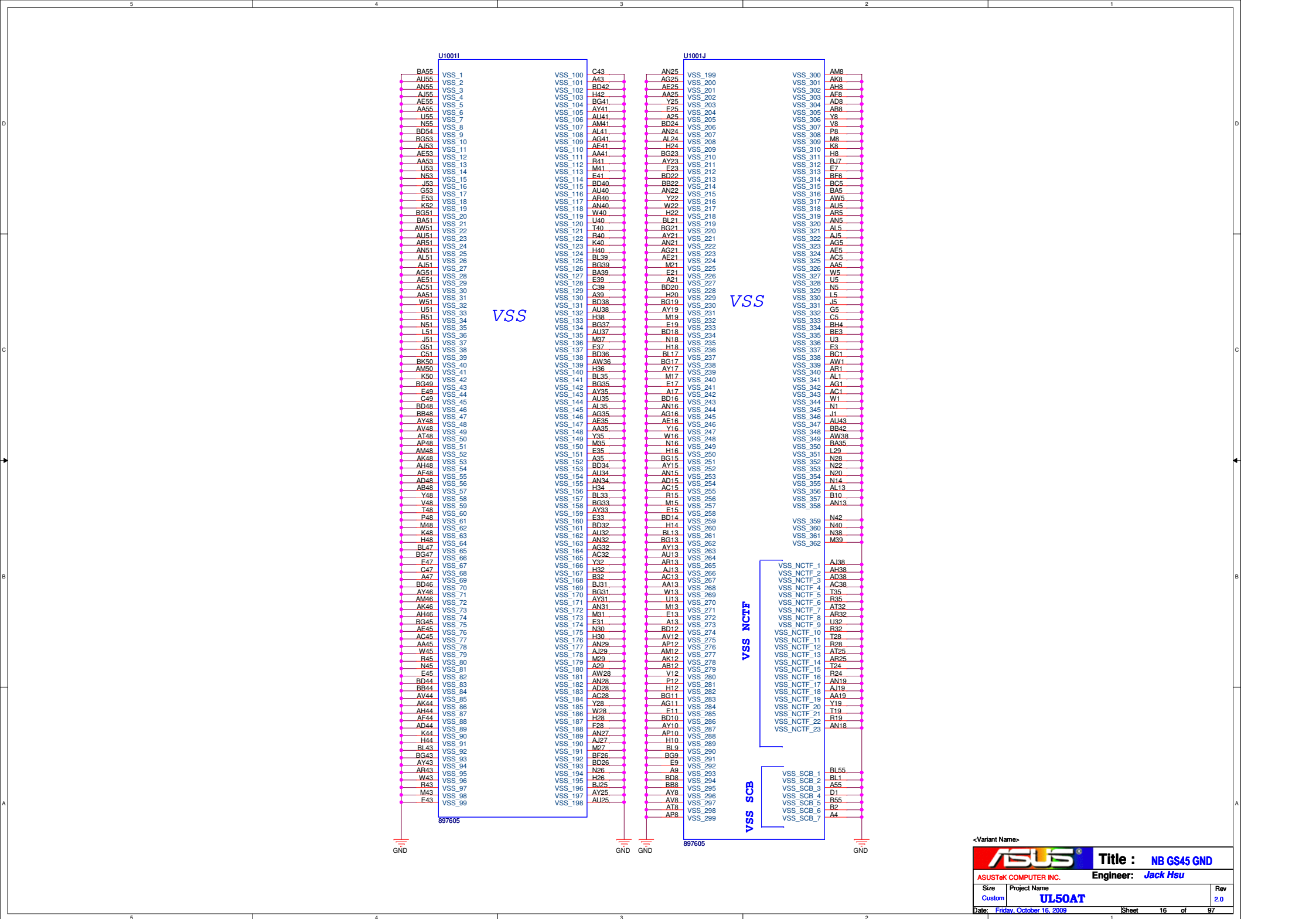
+VGFX_CORE

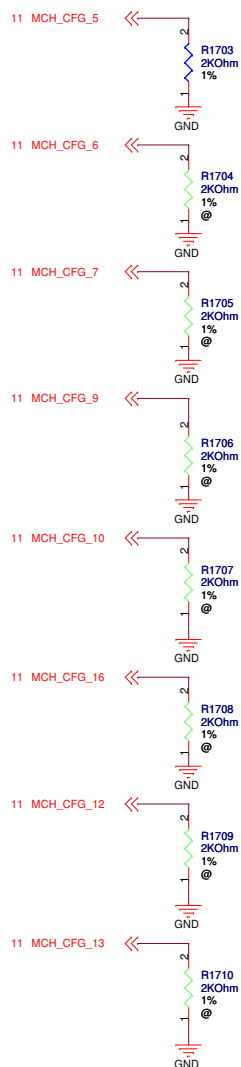
+VGFX_CORE

3060mA
+VCC_GMCH

+VCC_GMCH

Route VCC_AGX_SENSE and VSS_AGX_SENSE differentially.





CFG5 : DMI STRAP

H = DMI X 4 (Default)
L = DMI X 2

CFG6 : ITPM Host Interface (Relate to SPI_MOSI)

H = ITPM Disable (Default)
L = ITPM enable(Can disable by SW)

CFG7 : Intel ME Crypto Strap

H = With confidentiality (Default)
L = Without confidentiality

CFG9 : PCIE Graphic Lane Reverse

H = Normal (Default)
L = Lanes Reverse

CFG10 : PCIE Loopback

H = Disable (Default)
L = Enable

CFG16 : FSB Dynamic ODT

H =Enable (Default)
L = Disable

CFG12 : ALL-Z Mode

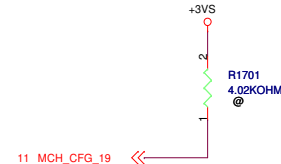
H =Disable (Default)
L = Enable

CFG13 : XOR Mode

H = Disable (Default)
L = Enable

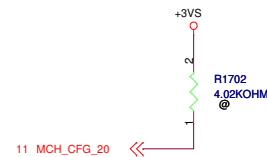
CFG [13:12] : XOR/ALL-Z

00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)



CFG19 : DMI Lane Reversal

H =DMI Lane Reversal
L = Normal (Default)



CFG20 : SDVO/PCIE CONCURRENT MODE

L = Only Digital display port or PCIE is
Operational (Default)

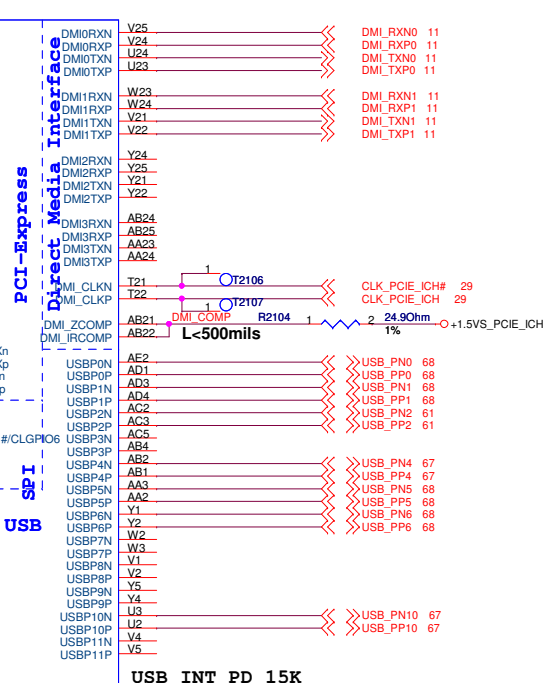
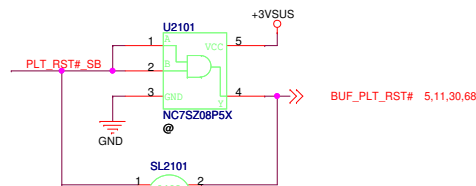
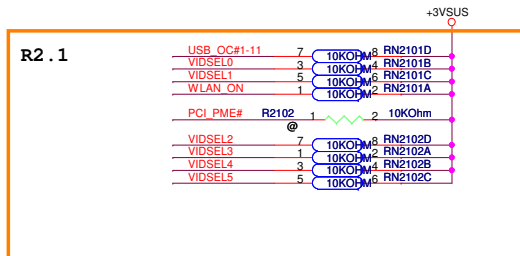
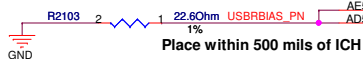
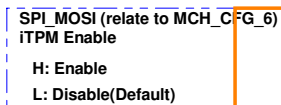
H = Digital display port and PCIE are operating
simultaneously via the PEG port

<Variant Name>

ASUS		Title : NB GS45 STRAPPING	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name		Rev
Custom	UL50AT		2.0
Date: Friday, October 16, 2009		Sheet	17 of 97



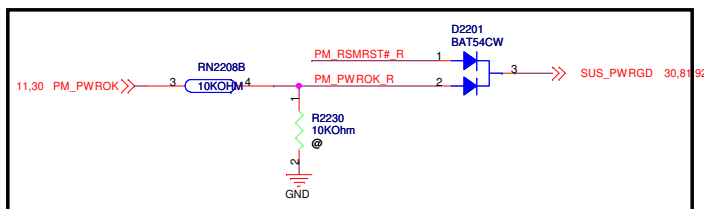
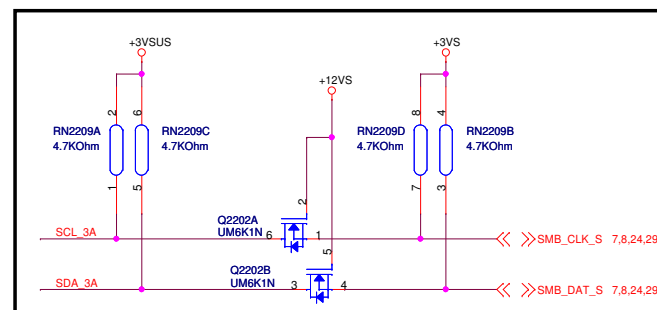
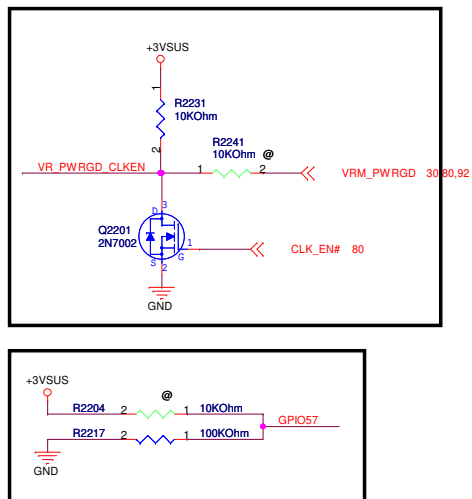
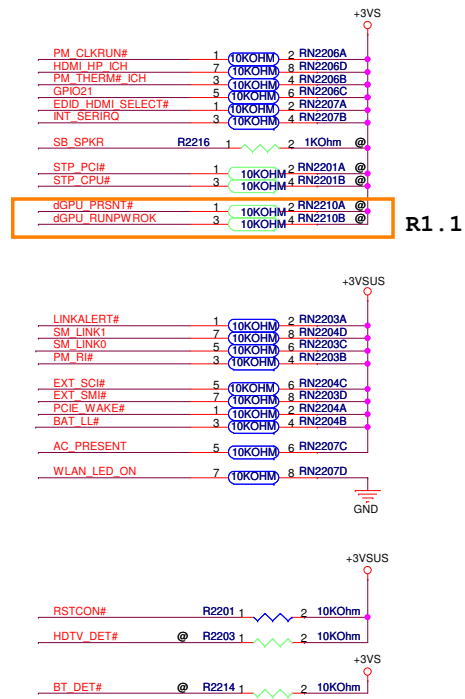
PCIE 1	
PCIE 2	WLAN
PCIE 3	
PCIE 4	
PCIE 5	
PCIE 6	GLAN

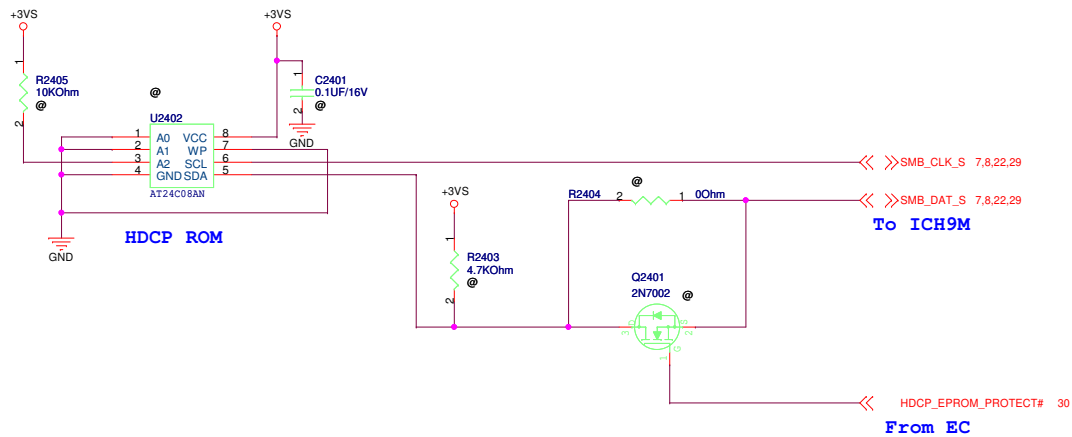


		GNT#0	SPICS#1
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

(default)

USB 0	USB Conn.
USB 1	USB Conn.
USB 2	Bluetooth
USB 3	
USB 4	CMOS Camera
USB 5	Card Reader
USB 6	WiMax
USB 7	
USB 8	
USB 9	
USB 10	USB Conn.
USB 11	





<Variant Name>

ASUS		Title : SB ICH9M (5)	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name		Rev
Custom	UL50AT		2.0
Date: Friday, October 16, 2009		Sheet	24 of 97

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

<Variant Name>		Title :	
		Engineer: <i>Jack Hsu</i>	
Size	Project Name		Rev
C	UL50AT		2.0
Date: <u>Friday, October 16, 2009</u>		Sheet	26 of 97

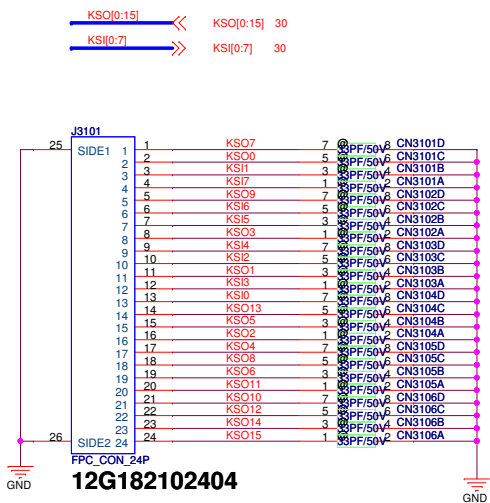
	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

<Variant Name>		Title :	
		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	26 of 97

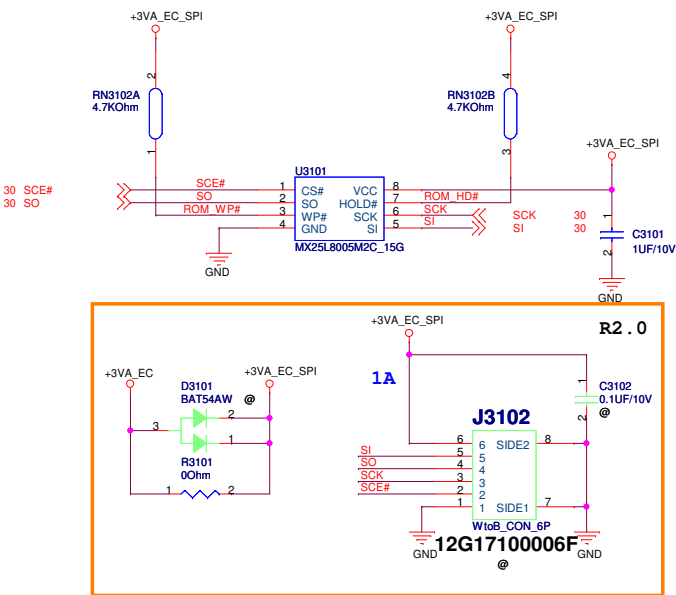
	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

<Variant Name>		Title :	
		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	28 of 97

Internal Keyboard



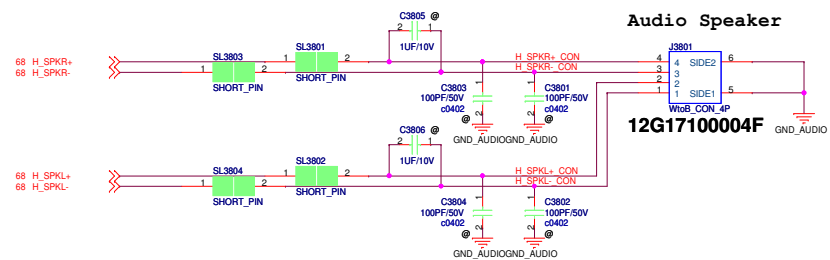
SPI Flash ROM (8Mb)





	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

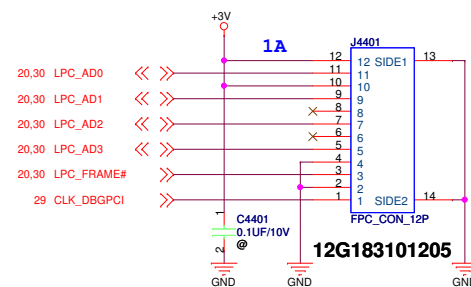
<Variant Name>		Title :<Title>	
		Engineer: Jack Hsu	
Size	Project Name		Rev
C	UL50AT		2.0
Date: Friday, October 16, 2009		Sheet	35 of 97



	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

<Variant Name>		Title :<Title>	
		Engineer: Jack Hsu	
Size	Project Name		Rev
C	UL50AT		2.0
Date: Friday, October 16, 2009		Sheet	39 of 97

LPC DEBUG PORT



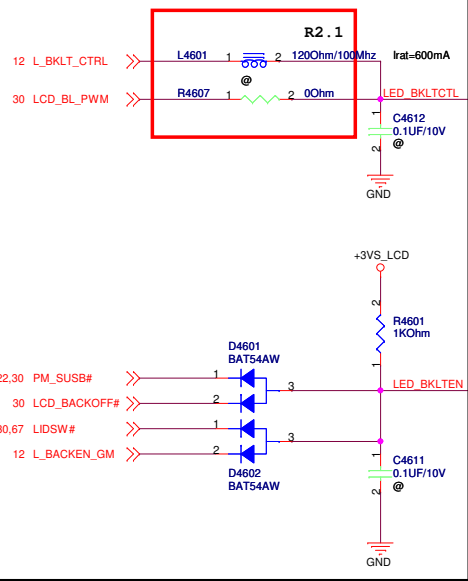
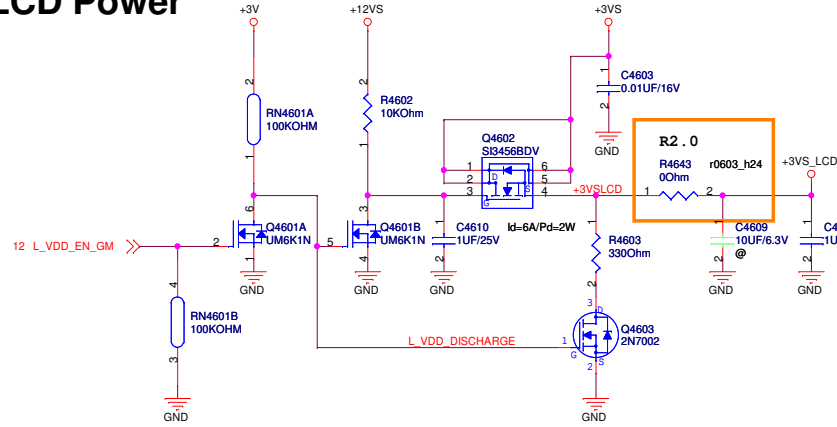
<Variant Name>

		Title : DEBUG PORT	
ASUSTeK COMPUTER INC.		Engineer: <i>Jack Hsu</i>	
Size Custom	Project Name UL50AT		Rev 2.0
Date: Friday, October 16, 2009		Sheet 44 of	97

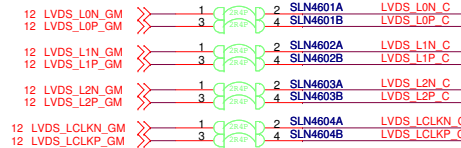
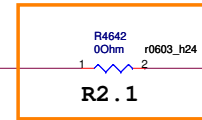
	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

<Variant Name>		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name		Rev
C	UL50AT		2.0
Date: Friday, October 16, 2009		Sheet	45 of 97

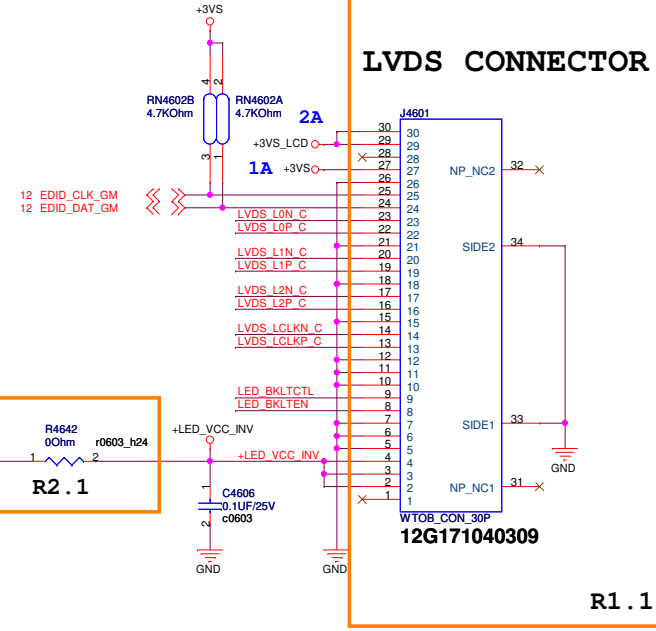
LCD Power



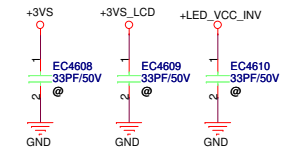
AC_BAT_SYS



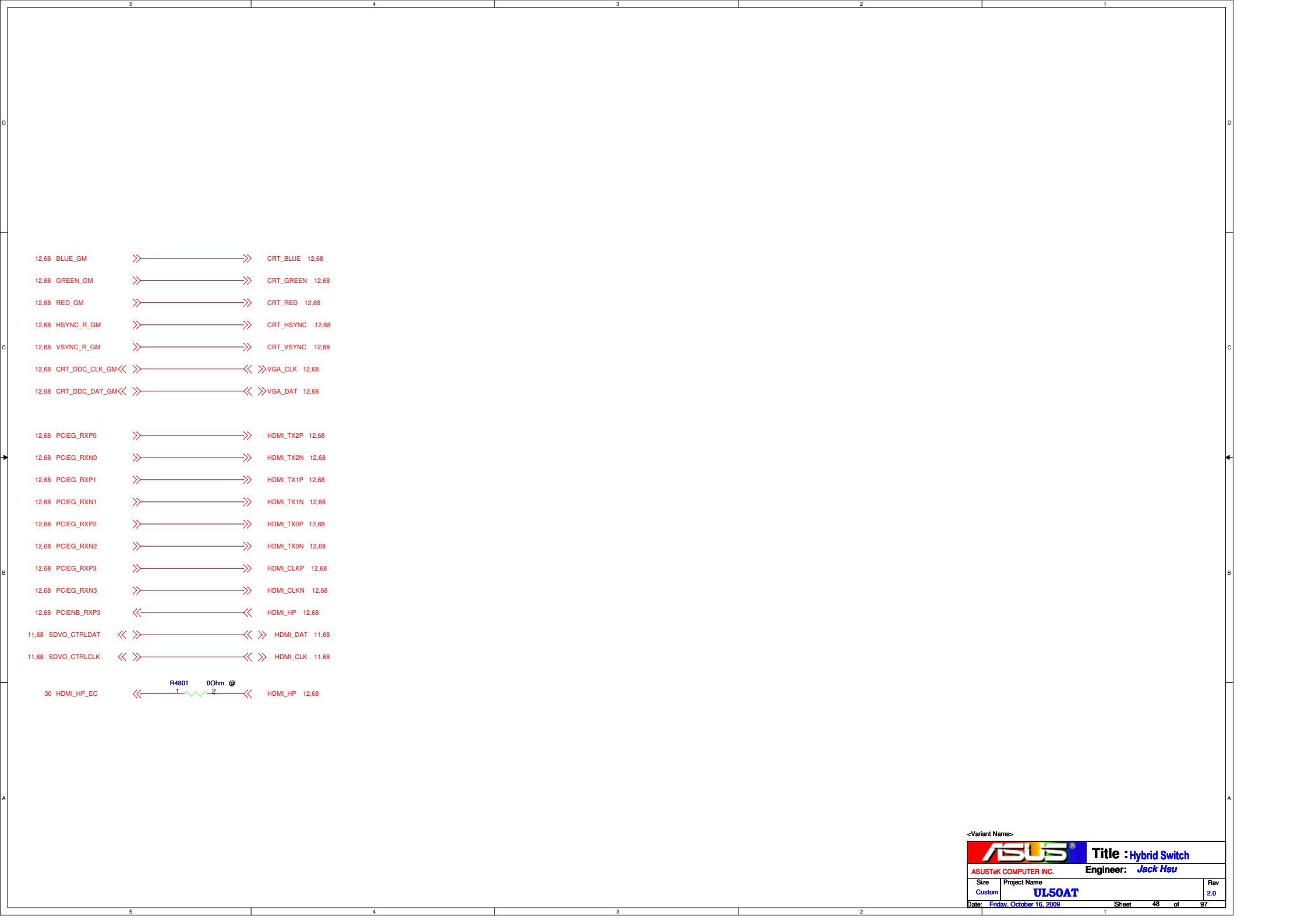
LVDS CONNECTOR



R1.1



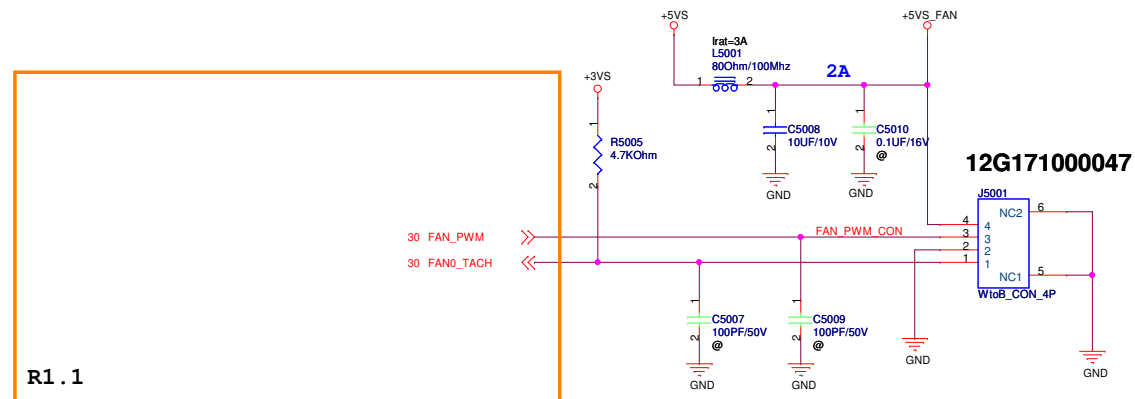
<Variant Name>



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D					
C					
B					
A					
	5	4	3	2	1

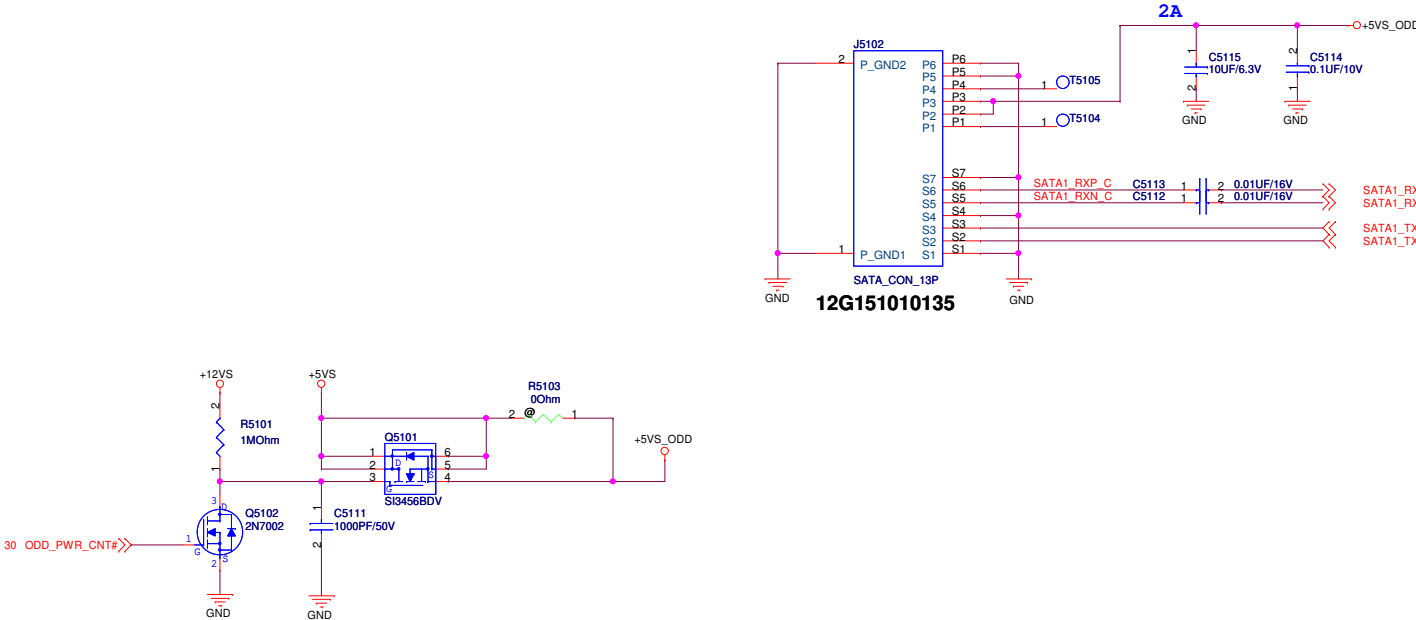
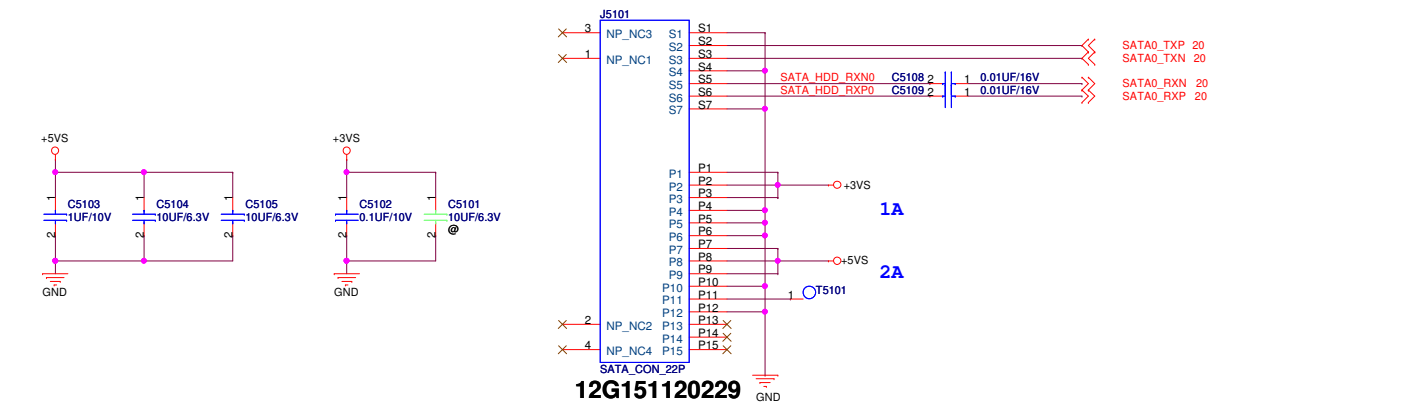
Route CPU_THRM_DA , CPU_THRM_DC and MEM_THERM_DA , MEM_THERM_DC on the same layer

Avoid FSB,Power

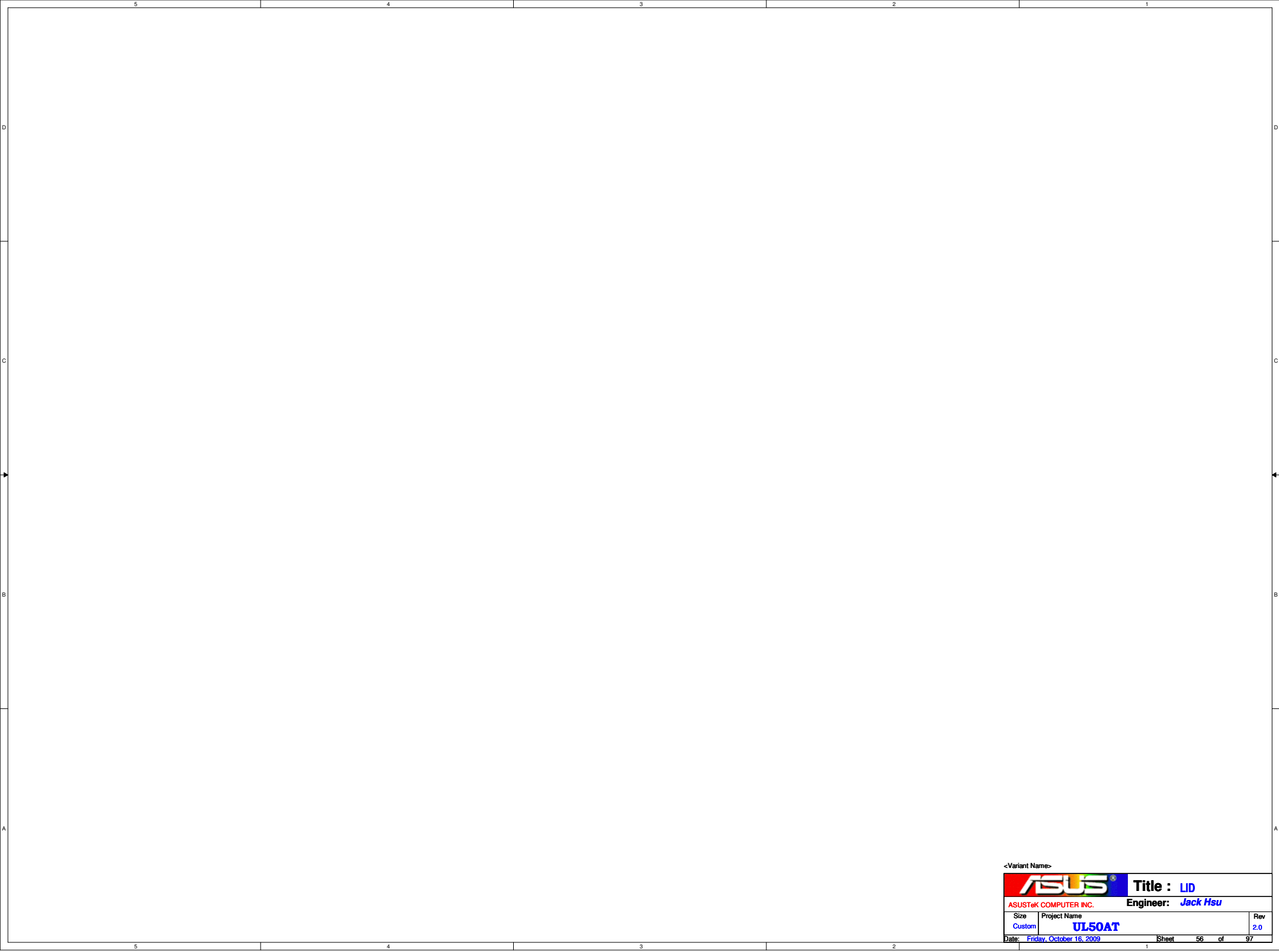
[illegible]

SATA HDD

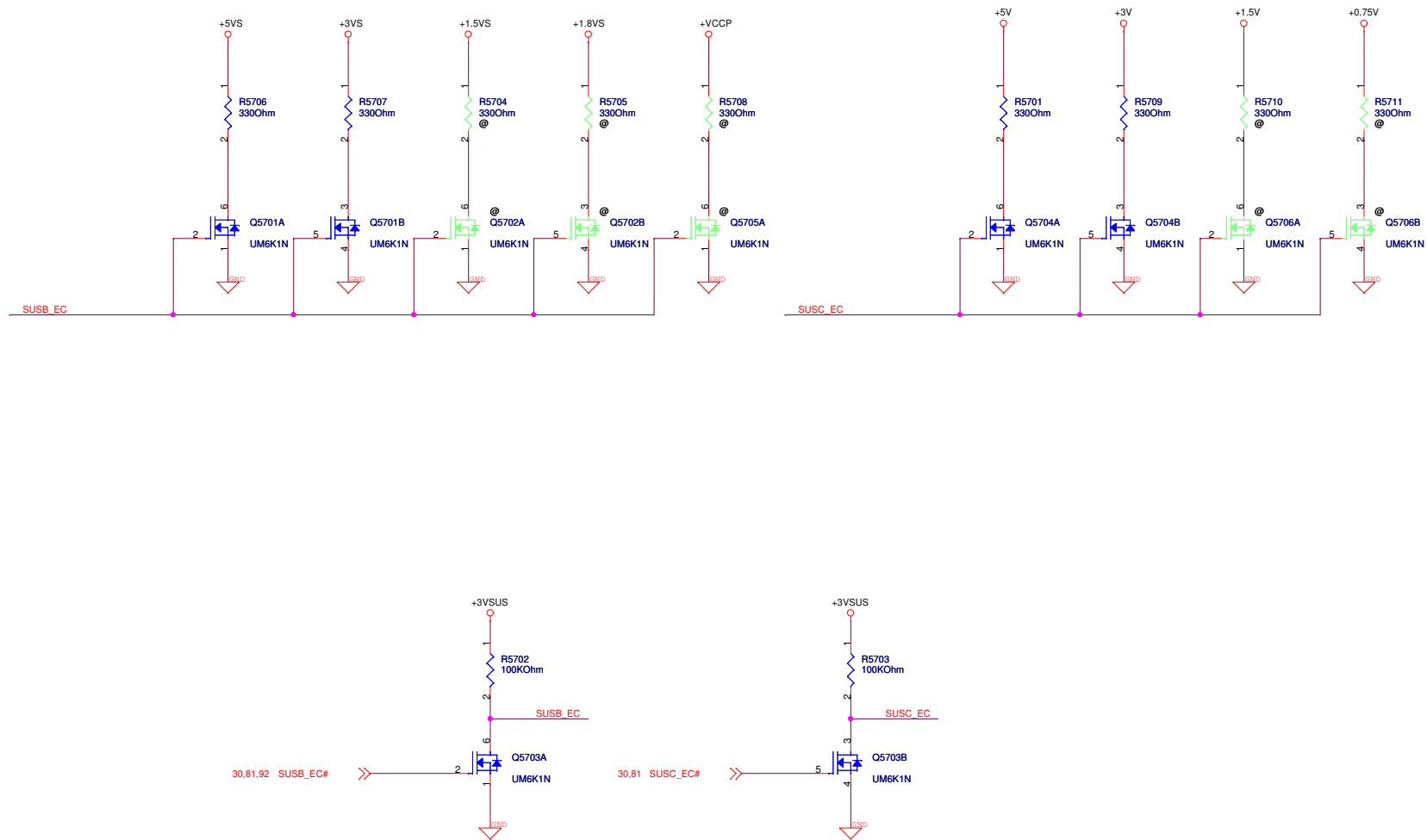
SATA ODD



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D											
C											
B											
A											
<Variant Name>  Title : <Title> ASUSTeK COMPUTER INC. Engineer: Jack Hsu <table><tr><td>Size</td><td>Project Name</td><td>Rev</td></tr><tr><td>C</td><td>UL50AT</td><td>2.0</td></tr></table> Date: Friday, October 16, 2009Sheet 53 of 97						Size	Project Name	Rev	C	UL50AT	2.0
Size	Project Name	Rev									
C	UL50AT	2.0									
	5	4	3	2	1						



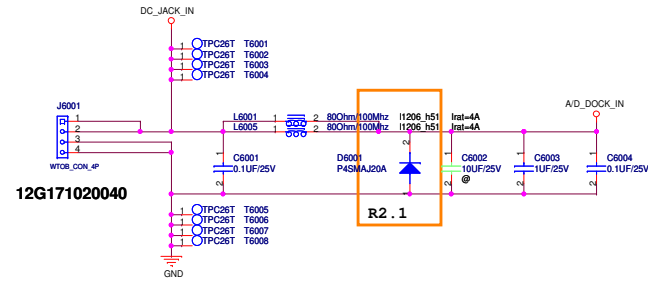
Discharge Circuit



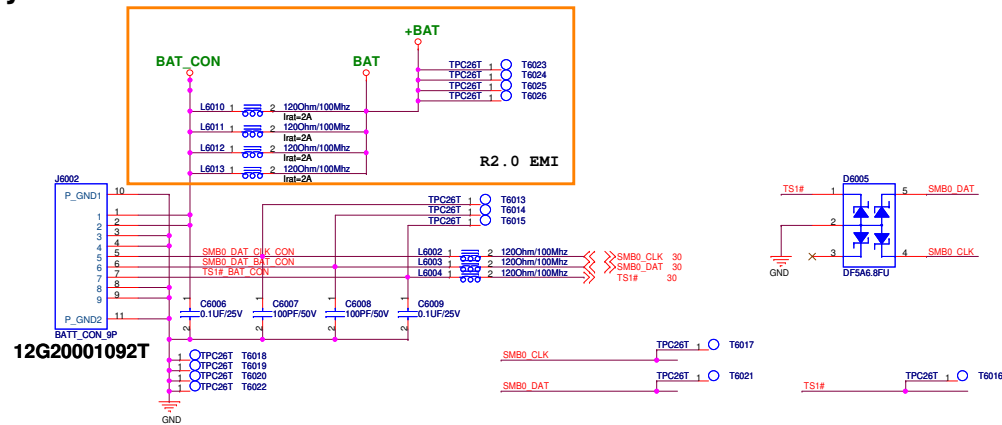
<Variant Name>

ASUS		Title DISCHARGE CIRCUIT	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	57 of 97

DC-IN



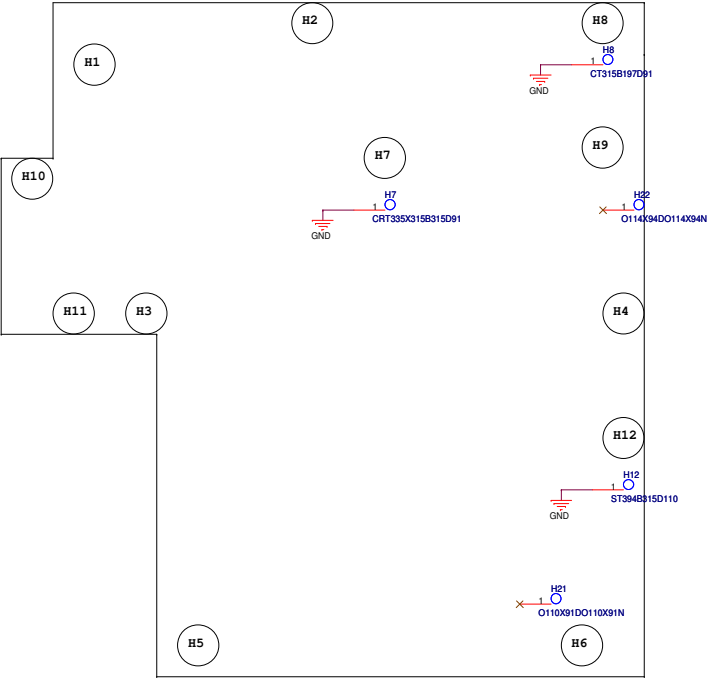
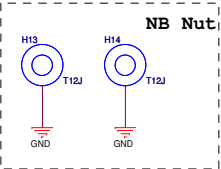
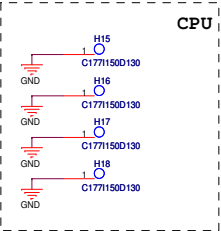
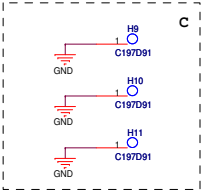
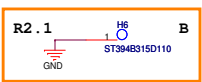
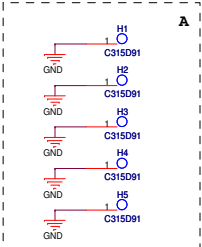
Battery Connector



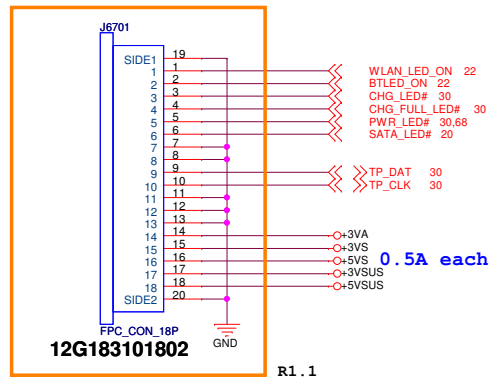


<Variant Name>			
		Title : <i>BlueTooth</i>	
ASUSTeK COMPUTER INC.		Engineer: <i>Jack Hsu</i>	
Size C	Project Name UL50AT	Rev 2.0	
Date: <i>Friday, October 16, 2009</i>		Sheet	61 of 97

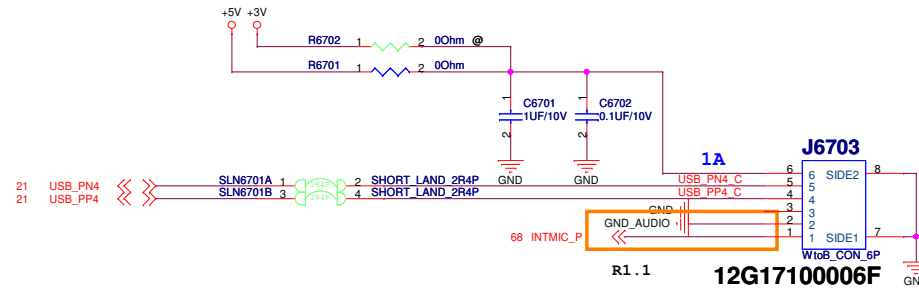
Screw Hole & SMT Nut



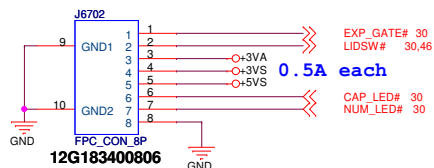
Touch Pad / LED Board



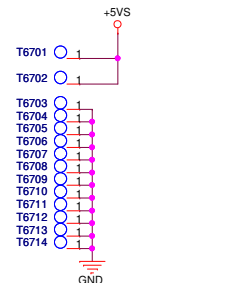
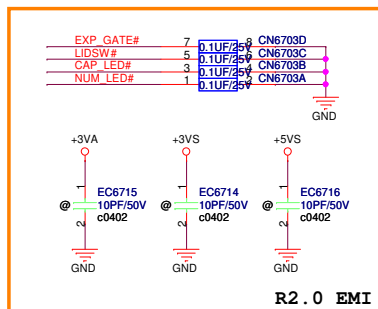
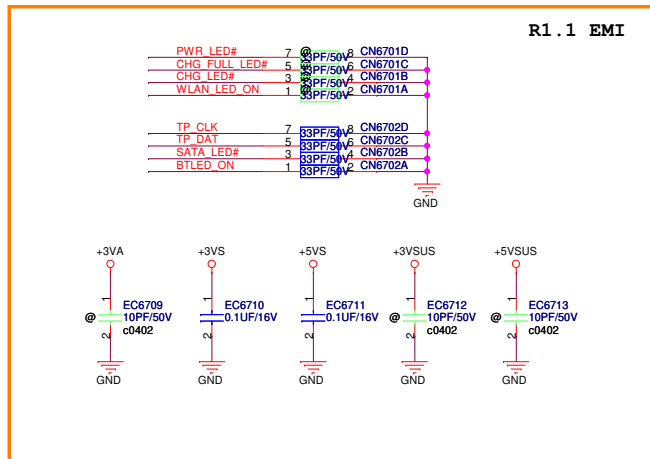
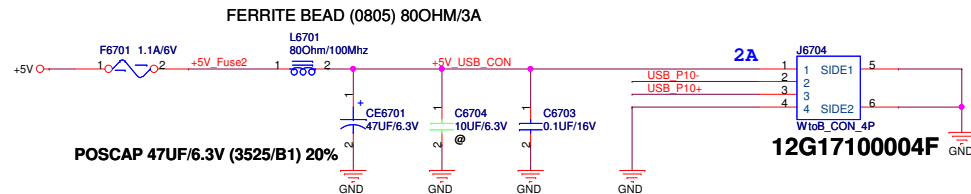
Camera Module



Function Board



FLY USB Cable

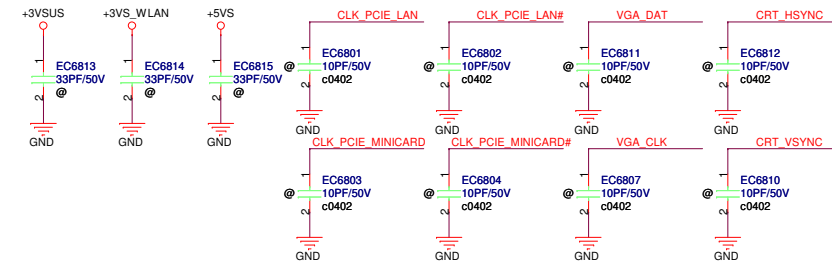
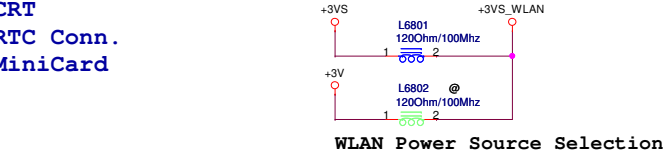


<Variant Name>

ASUS		Title : SUB BOARD	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	UL50AT	Rev 2.0
Custom			
Date: Friday, October 16, 2009		Sheet 67	of 97

IO BOARD - 02

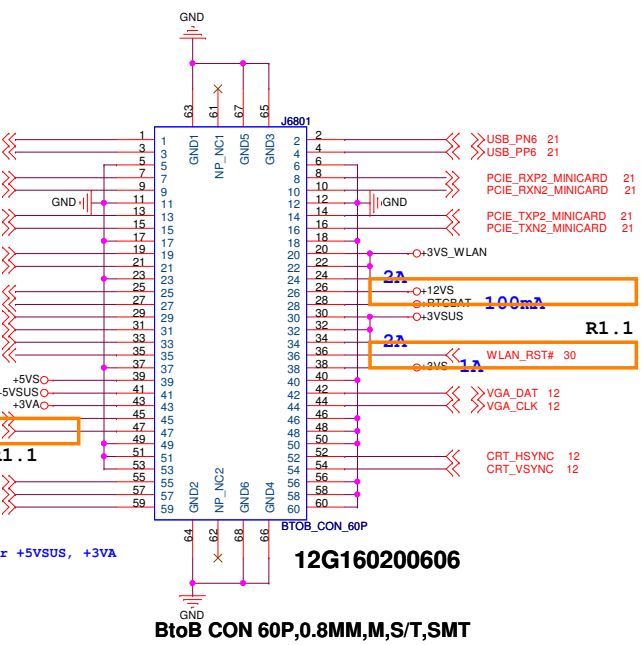
LAN IC
RJ45
CRT
RTC Conn.
MiniCard



- 21 PCIE_RXP6_LAN
- 21 PCIE_RXN6_LAN
- 21 PCIE_TXP6_LAN
- 21 PCIE_TXN6_LAN
- 29 CLK_PCIE_LAN
- 29 CLK_PCIE_LAN#
- 29 CLK_PCIE_MINICARD
- 29 CLK_PCIE_MINICARD#
- 29 CLK_REQ_LAN#
- 29 CLK_REQ_WLAN#
- 21 WLAN_ON
- 22 PCIE_WAKE#
- 30 PWR_SW#

12 CRT_BLUE
12 CRT_GREEN
12 CRT_RED

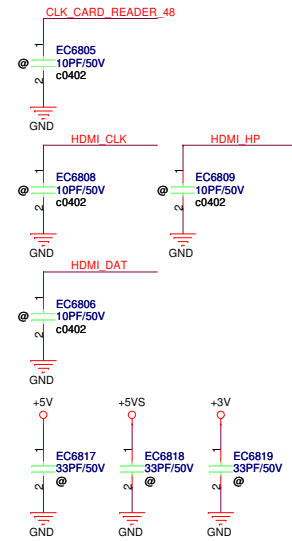
1A for +5VS, 100mA for +5VSUS, +3VA



USB 0	USB Conn.
USB 1	USB Conn.
USB 2	Bluetooth
USB 3	
USB 4	CMOS Camera
USB 5	Card Reader
USB 6	WiMax
USB 7	
USB 8	
USB 9	
USB 10	USB Conn.
USB 11	

IO BOARD - 01

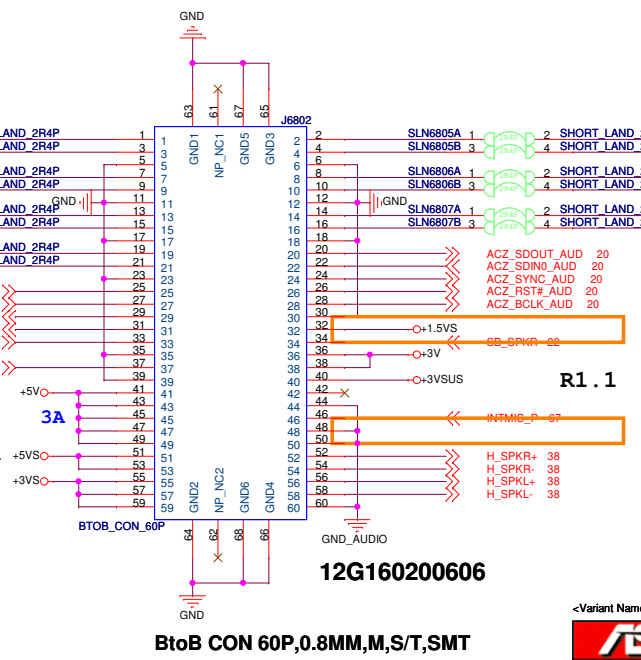
HDMI Conn.
USB Conn.x2
MIC-IN Conn.
Head Phone Conn.
Audio IC
Card Reader IC
Card Reader Conn.



- 12 HDMI_CLKN
- 12 HDMI_CLKP
- 12 HDMI_TX0N
- 12 HDMI_TX0P
- 12 HDMI_TX1N
- 12 HDMI_TX1P
- 12 HDMI_TX2N
- 12 HDMI_TX2P

- 11 HDMI_CLK
- 11 HDMI_DAT
- 12,48 HDMI_HP
- 30 SD_CD#_EC
- 30 OP_SD#
- 29 CLK_CARD_READER_48

1.5A
2A



- SLN6801A 1
- SLN6801B 3
- SLN6802A 1
- SLN6802B 3
- SLN6803A 1
- SLN6803B 3
- SLN6804A 1
- SLN6804B 3

- 2 SHORT LAND 2R4P
- 4 SHORT LAND 2R4P
- 2 SHORT LAND 2R4P
- 4 SHORT LAND 2R4P
- 2 SHORT LAND 2R4P
- 4 SHORT LAND 2R4P
- 2 SHORT LAND 2R4P
- 4 SHORT LAND 2R4P

- ACZ_SDOUT_AUD 20
- ACZ_SDIN0_AUD 20
- ACZ_SYNC_AUD 20
- ACZ_RST#_AUD 20
- ACZ_BCLK_AUD 20

- H_SPKR+ 38
- H_SPKR- 38
- H_SPKL+ 38
- H_SPKL- 38





		Title : M10M-GE1 (4)	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name		Rev
C	UL50AT		2.0
Date: Friday, October 16, 2009		Sheet	78 of 97



		Title : M10M-GE1 (5)	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name		Rev
C	UL50AT		2.0
Date: Friday, October 16, 2009		Sheet	74 of 97

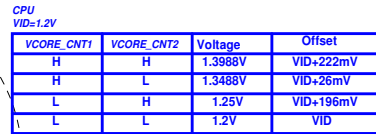




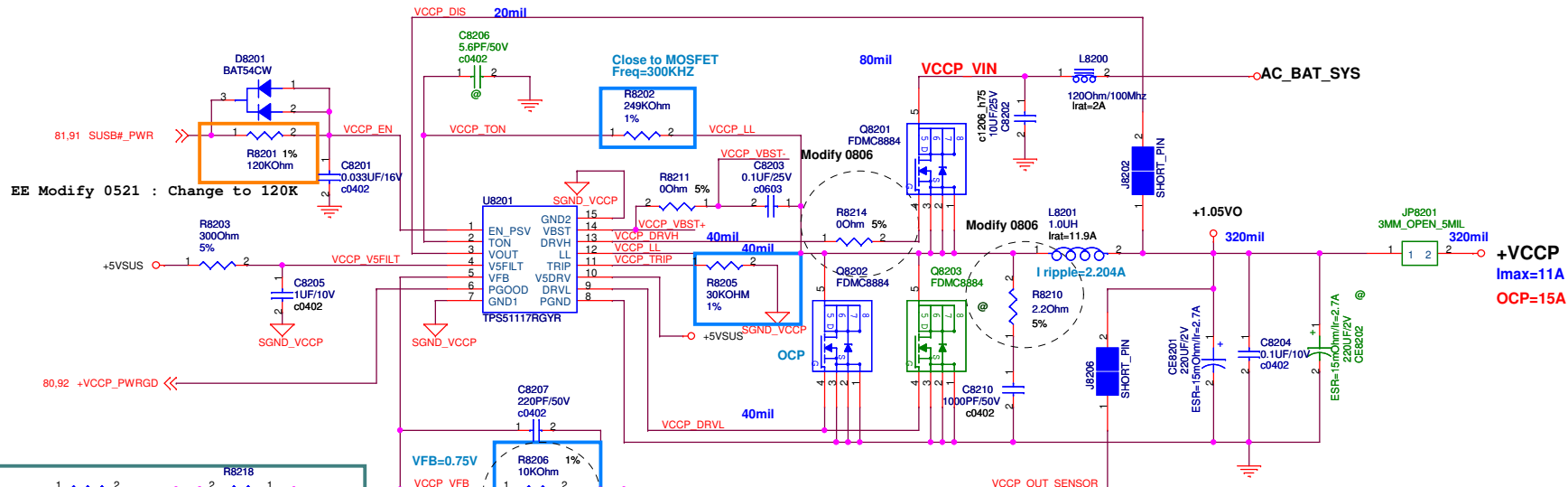
		Title: <i>Title></i>	
ASUSTeK COMPUTER INC.		Engineer: <i>Alan Chen</i>	
Size	Project Name		Rev
C	UL50AT		2.0
Date: <i>Friday, October 16, 2009</i>		Sheet	78 of 97

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

		Title: <i>Title></i>	
ASUSTeK COMPUTER INC.		Engineer: <i>Alan Chen</i>	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: <i>Friday, October 16, 2009</i>		Sheet	79 of 97





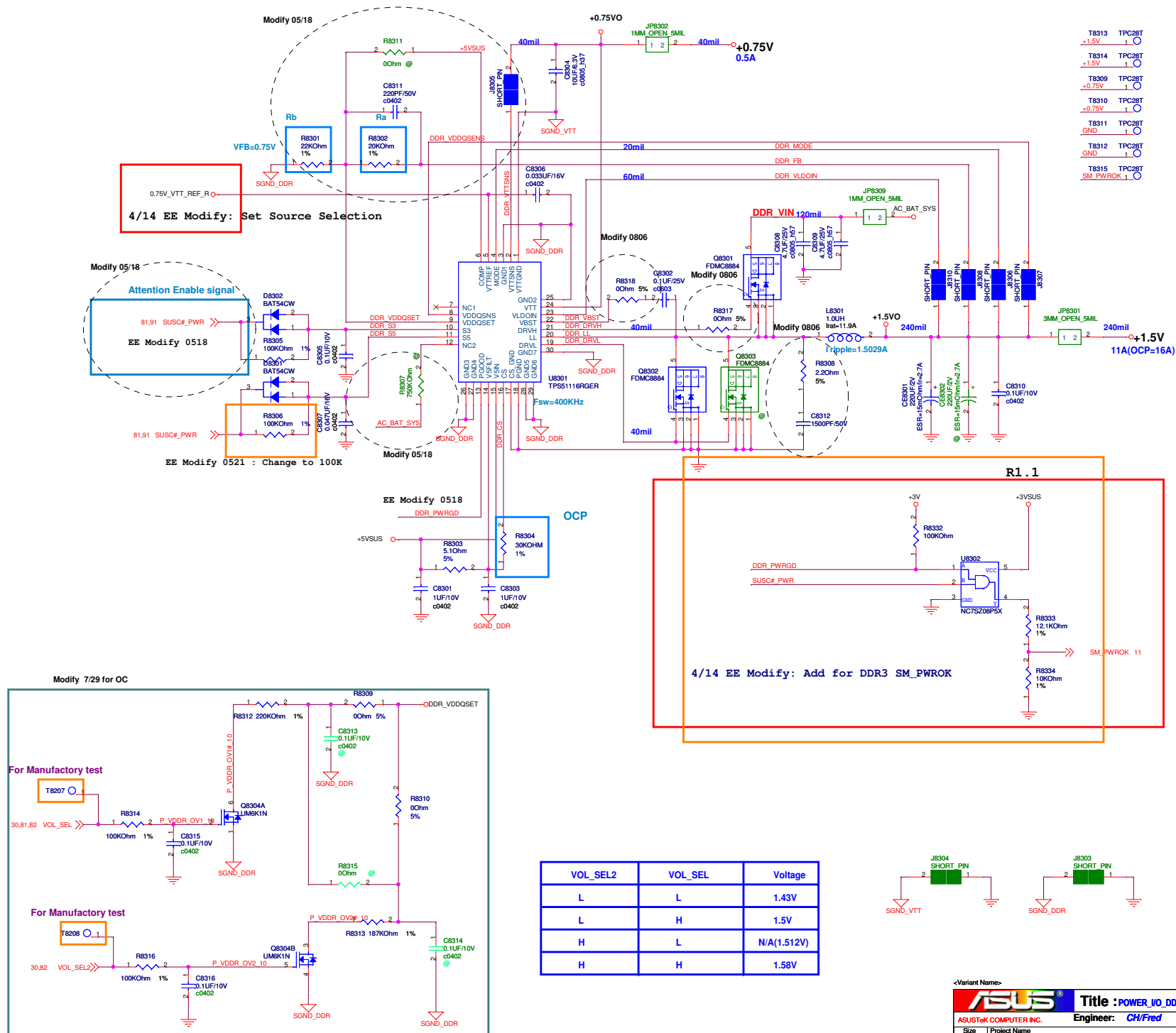


T8201 TPC28T
+1.05VO 1
T8202 TPC28T
+VCCP 1
T8203 TPC28T
GND 1
T8204 TPC28T
GND 1

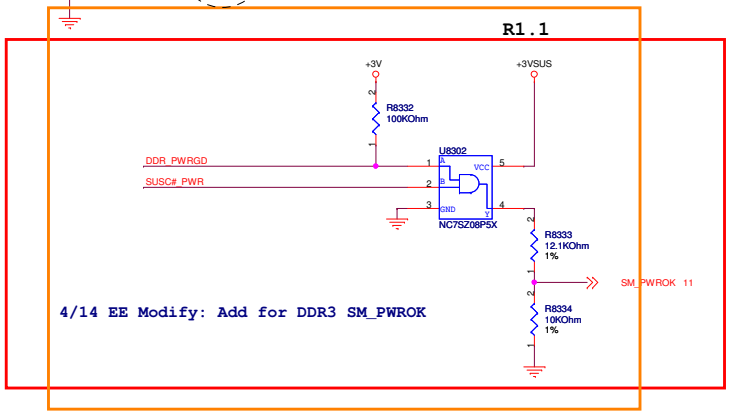
VOL_SEL2	VOL_SEL	Voltage
L	L	1V
L	H	1.05V
H	L	N/A(1.079V)
H	H	1.129V

<Variant Name>

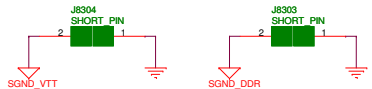
ASUS		Title : POWER_IO +VCCP	
ASUSTek COMPUTER INC.		Engineer:	
Size Custom	Project Name UL50AT	Rev 2.0	
Date: Friday, October 16, 2009	Sheet 82 of 97		



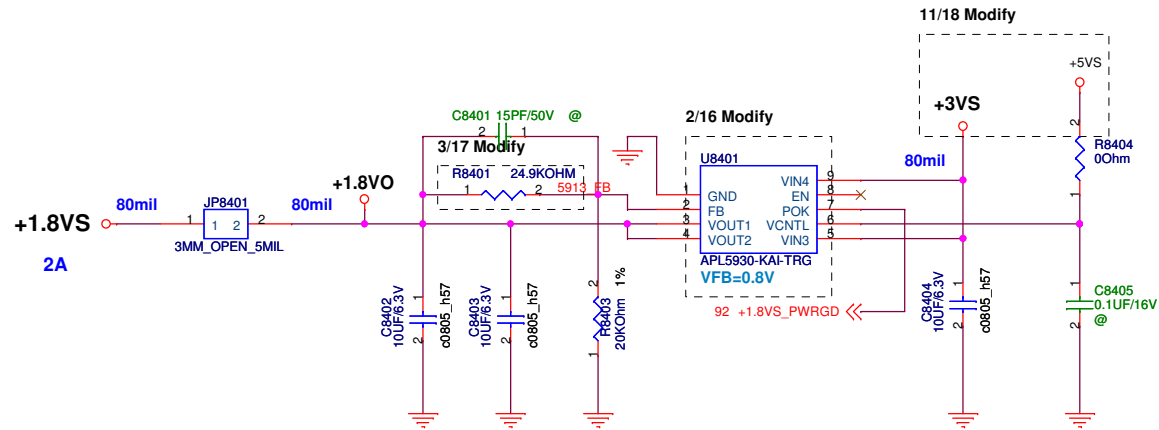
- T8313 TPC28T
- T8314 TPC28T
- T8309 TPC28T
- T8310 TPC28T
- T8311 TPC28T
- T8312 TPC28T
- T8315 TPC28T
- SM_PWR0K 1



VOL_SEL2	VOL_SEL	Voltage
L	L	1.43V
L	H	1.5V
H	L	N/A(1.512V)
H	H	1.58V



+1.8VS



T8401	TPC28T
+1.8VO	1
T8402	TPC28T
+1.8VS	1
T8403	TPC28T
GND	1
T8404	TPC28T
GND	1

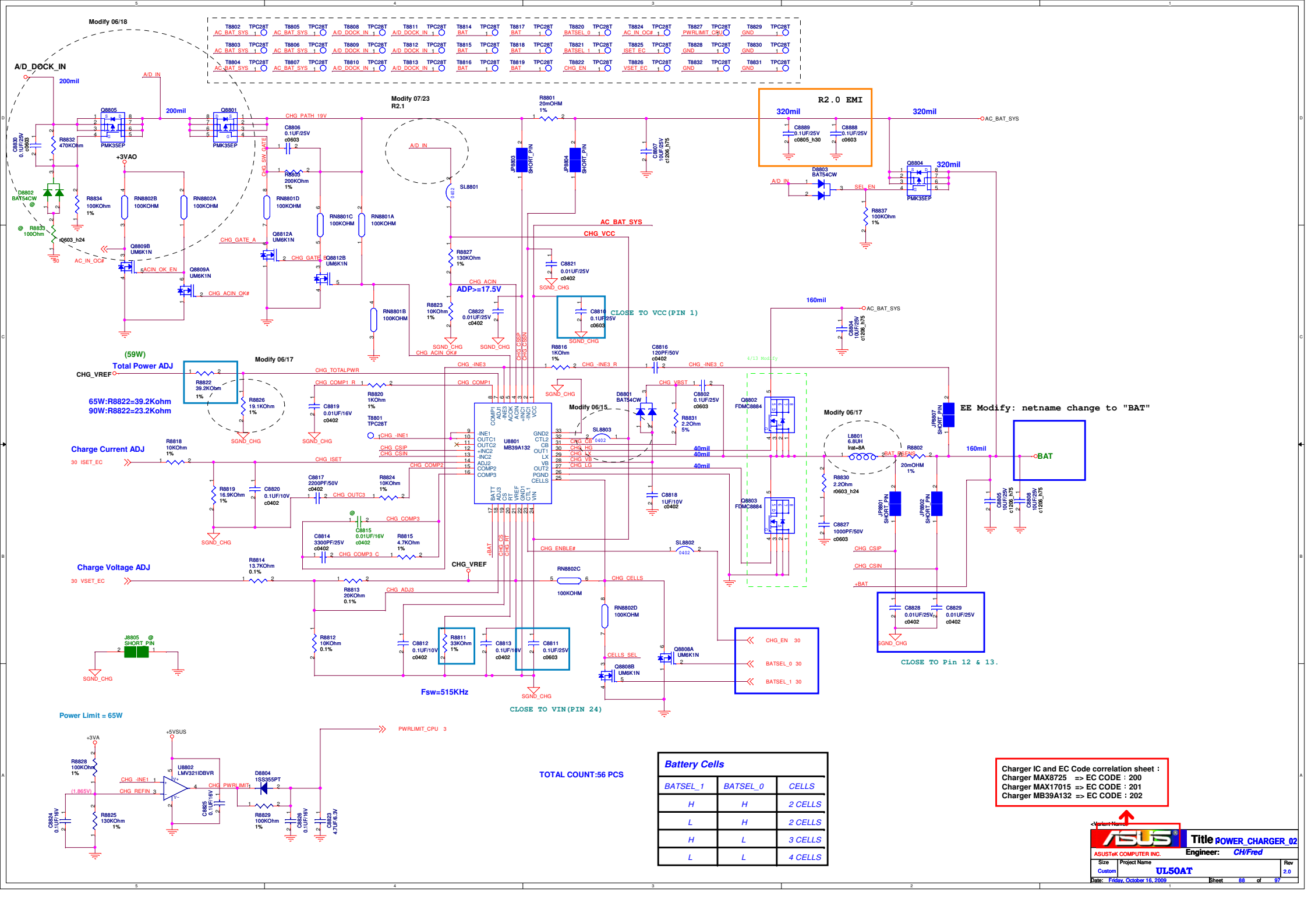
<Variant Name>

ASUS		Title : POWER_IO_+1.8VS	
ASUSTeK COMPUTER INC.		Engineer: CH/Fred	
Size	Project Name		Rev
Custom	UL50AT		2.0
Date: Friday, October 16, 2009		Sheet	84 of 97

	5	4	3	2	1
D					D
C					C
B					B
A					A
	5	4	3	2	1

<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: CH/Fred	
Size A	Project Name UL50AT		Rev 2.0
Date: Friday, October 16, 2009		Sheet 87	of 97



T8802	TPC28T	T8805	TPC28T	T8808	TPC28T	T8811	TPC28T	T8814	TPC28T	T8817	TPC28T	T8820	TPC28T	T8824	TPC28T	T8827	TPC28T	T8829	TPC28T
AC_BAT_SYS	1	AC_BAT_SYS	1	A/D_DOCK_IN	1	A/D_DOCK_IN	1	BAT	1	BAT	1	BATSEL_0	1	AC_IN_OCF	1	PWRLIMIT_CHG	1	GND	1
T8803	TPC28T	T8806	TPC28T	T8809	TPC28T	T8812	TPC28T	T8815	TPC28T	T8818	TPC28T	T8821	TPC28T	T8825	TPC28T	T8828	TPC28T	T8830	TPC28T
AC_BAT_SYS	1	AC_BAT_SYS	1	A/D_DOCK_IN	1	A/D_DOCK_IN	1	BAT	1	BAT	1	BATSEL_1	1	ISET_EC	1	GND	1	GND	1
T8804	TPC28T	T8807	TPC28T	T8810	TPC28T	T8813	TPC28T	T8816	TPC28T	T8819	TPC28T	T8822	TPC28T	T8826	TPC28T	T8832	TPC28T	T8831	TPC28T
AC_BAT_SYS	1	AC_BAT_SYS	1	A/D_DOCK_IN	1	A/D_DOCK_IN	1	BAT	1	BAT	1	CHG_EN	1	VSET_EC	1	GND	1	GND	1

Battery Cells		
BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS

Charger IC and EC Code correlation sheet :
Charger MAX8725 => EC CODE : 200
Charger MAX17015 => EC CODE : 201
Charger MB39A132 => EC CODE : 202

D

C

B

A

<Variant Name>



Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: *CH/Fred*

Size

A

Project Name

UL50AT

Rev

2.0

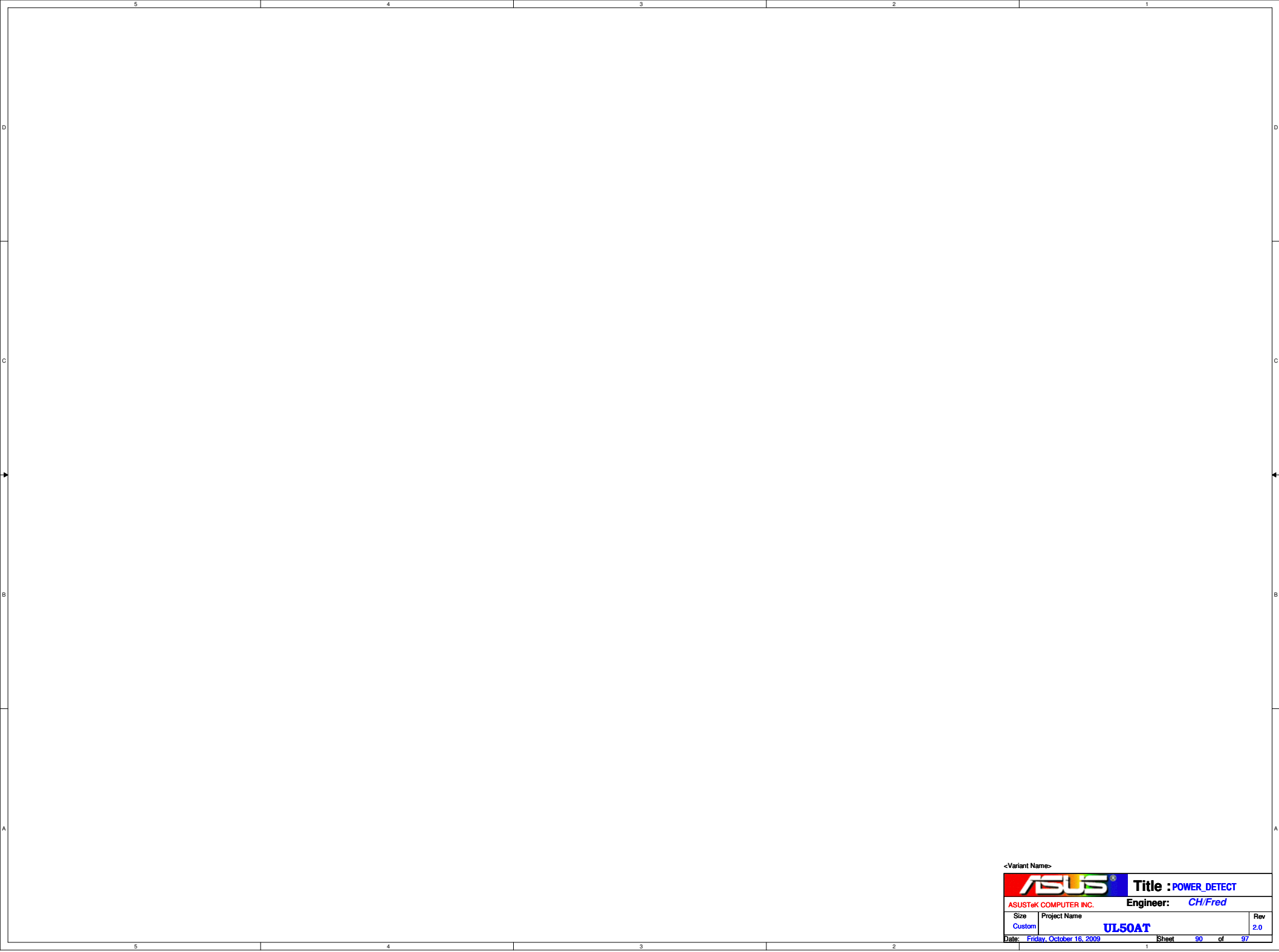
Date: Friday, October 16, 2009

Sheet

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of

97



<Variant Name>



Title :POWER_DETECT

ASUSTeK COMPUTER INC.

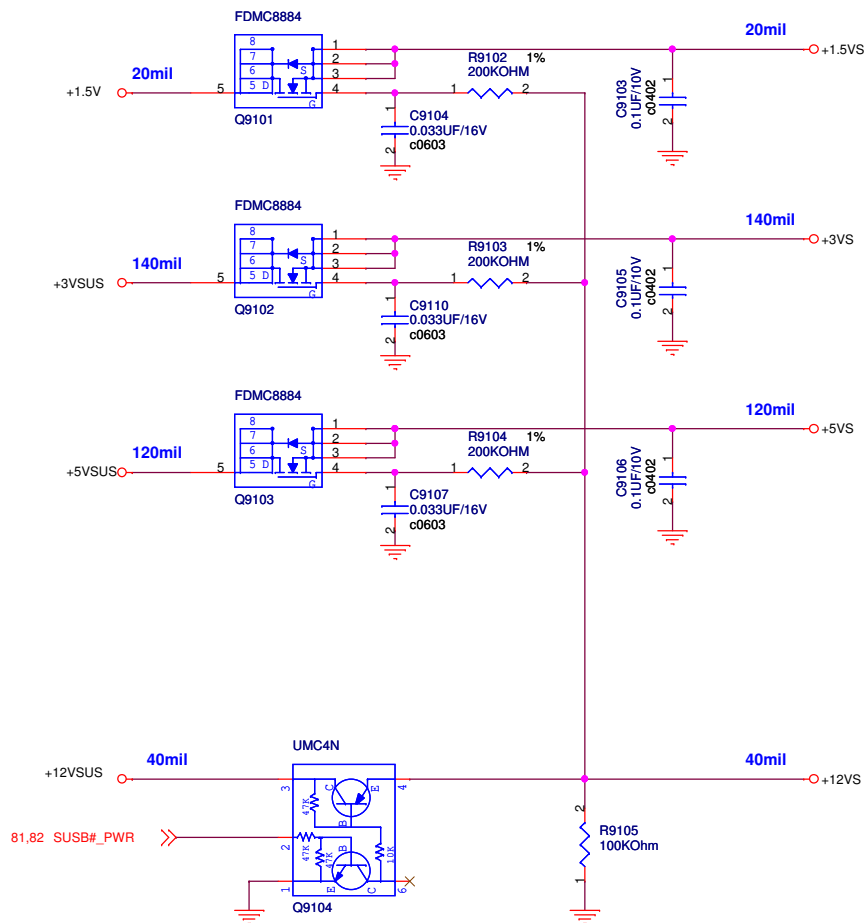
Engineer: CH/Fred

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009

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SUSB#_PWR POWER



Total count: 19 pcs

SUSC#_PWR POWER

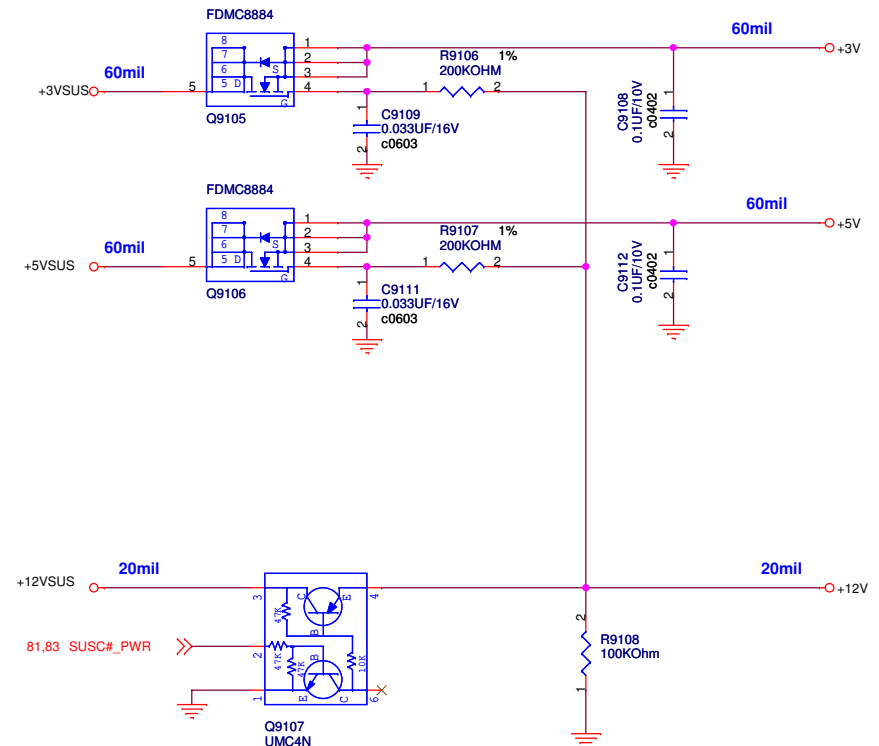
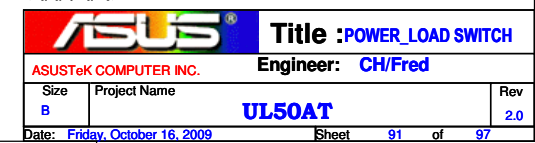
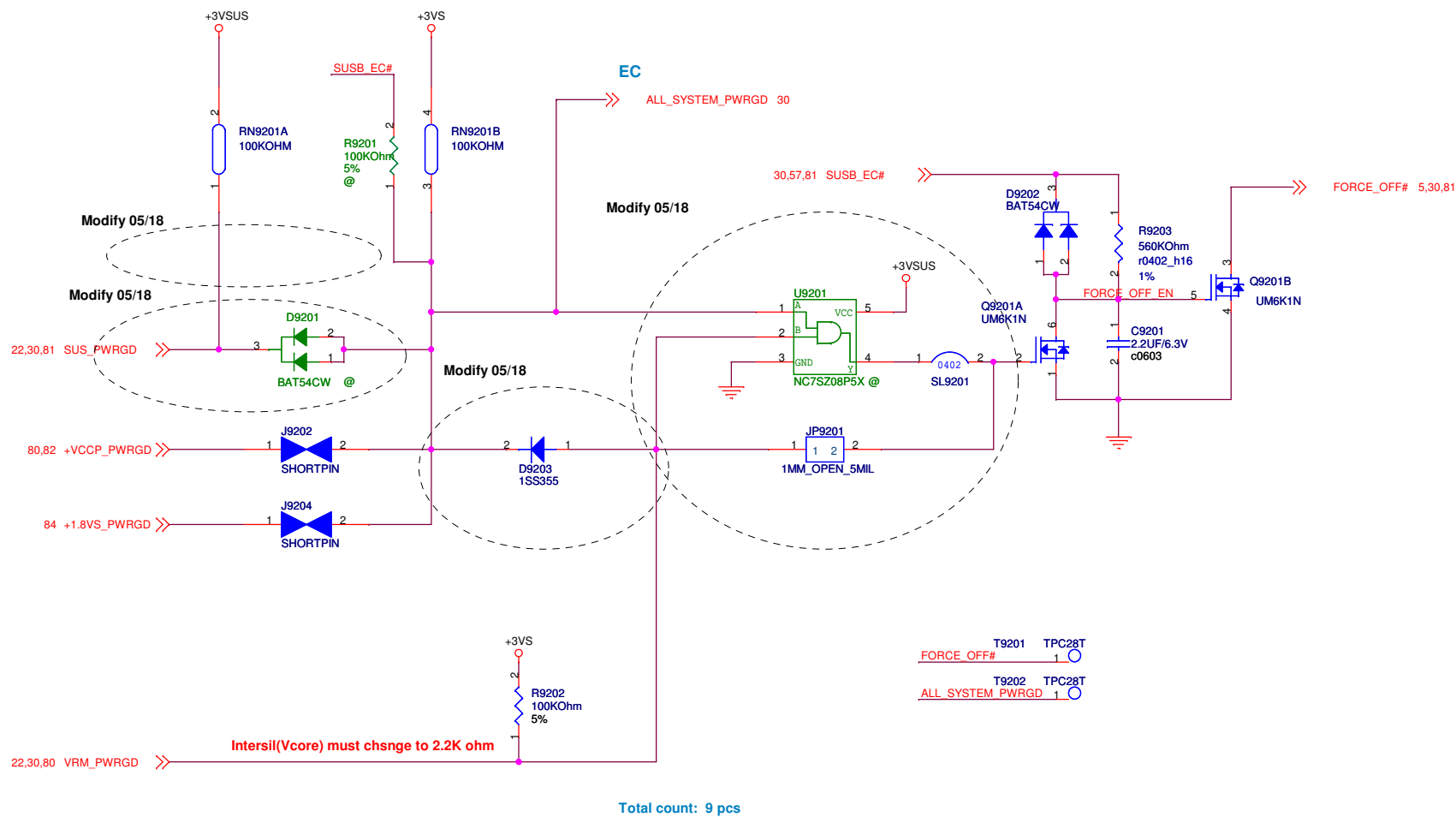


Figure 1: Schematic representation of the TPC28T and TPC28TΔSUSC# PWR1 mouse strains. The diagram shows the genomic organization of the Tpc28t gene on chromosome 10, with exons represented by boxes and introns by lines. The TPC28T strain has a wild-type allele with 11 exons. The TPC28TΔSUSC# PWR1 strain has a deletion of exons 10 and 11, indicated by a red line and a blue circle. The TPC28TΔSUSC# PWR1 strain also has a deletion of exons 10 and 11, indicated by a red line and a blue circle. The TPC28TΔSUSC# PWR1 strain also has a deletion of exons 10 and 11, indicated by a red line and a blue circle.

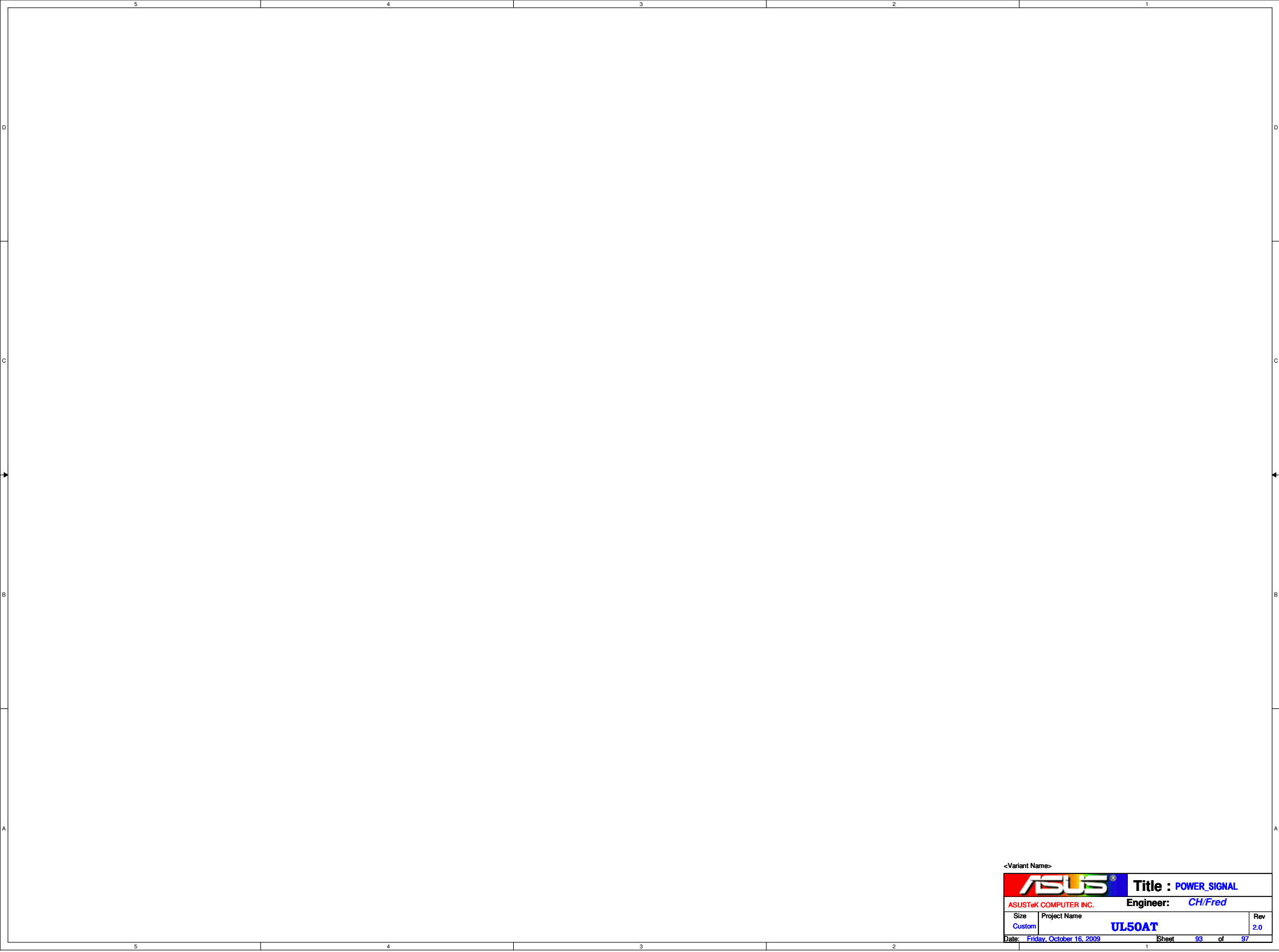
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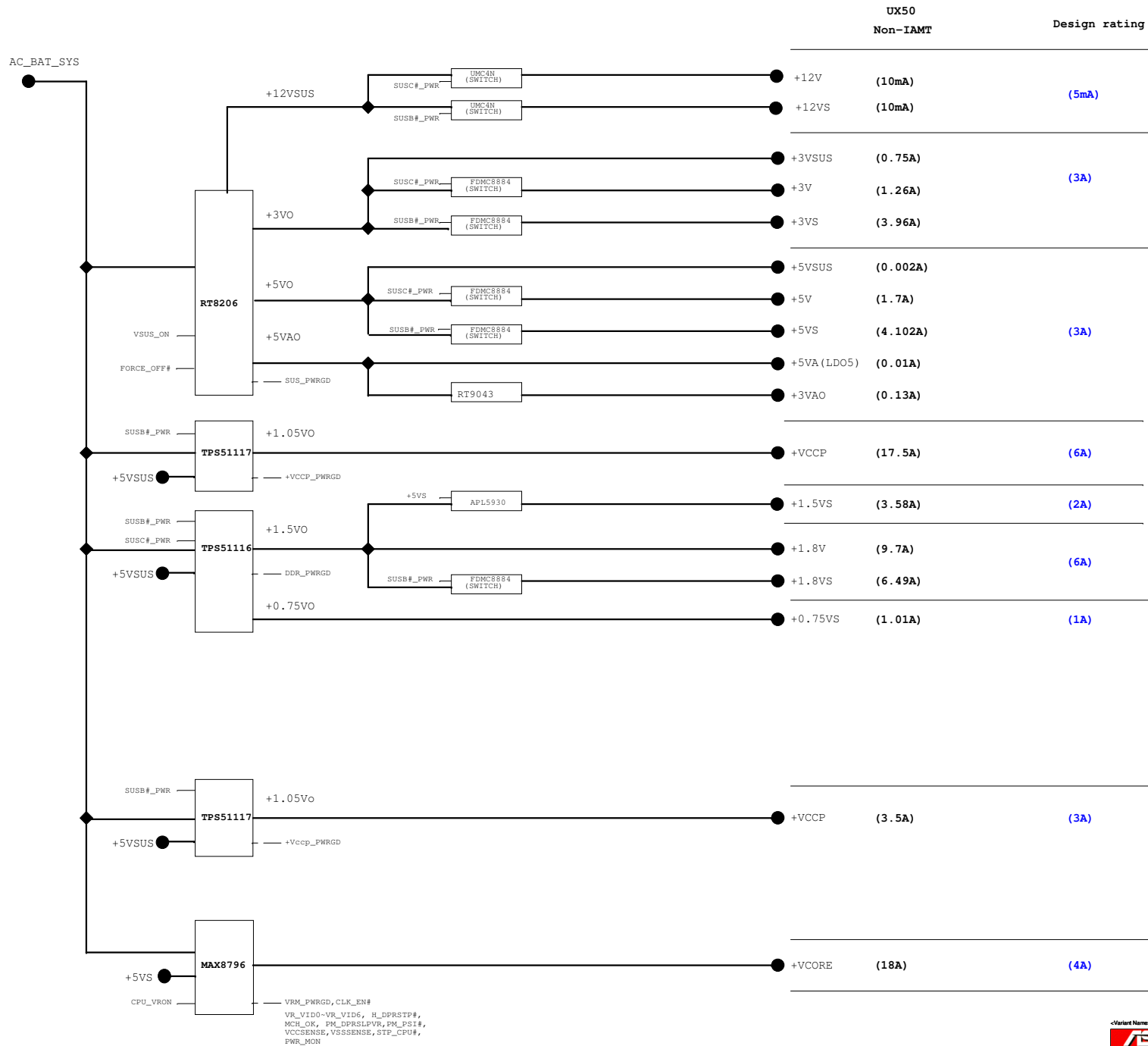


POWER GOOD DETECTOR



<Variant Name>		Title :POWER_PROTECT	
ASUSTeK COMPUTER INC.		Engineer: CH/Fred	
Size B	Project Name UL50AT	Rev 2.0	
Date: Friday, October 16, 2009		Sheet	92 of 97





D

D

C

C

B

B

A

A

<Variant Name>



Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: *CH/Fred*

Size

A

Project Name

UL50AT

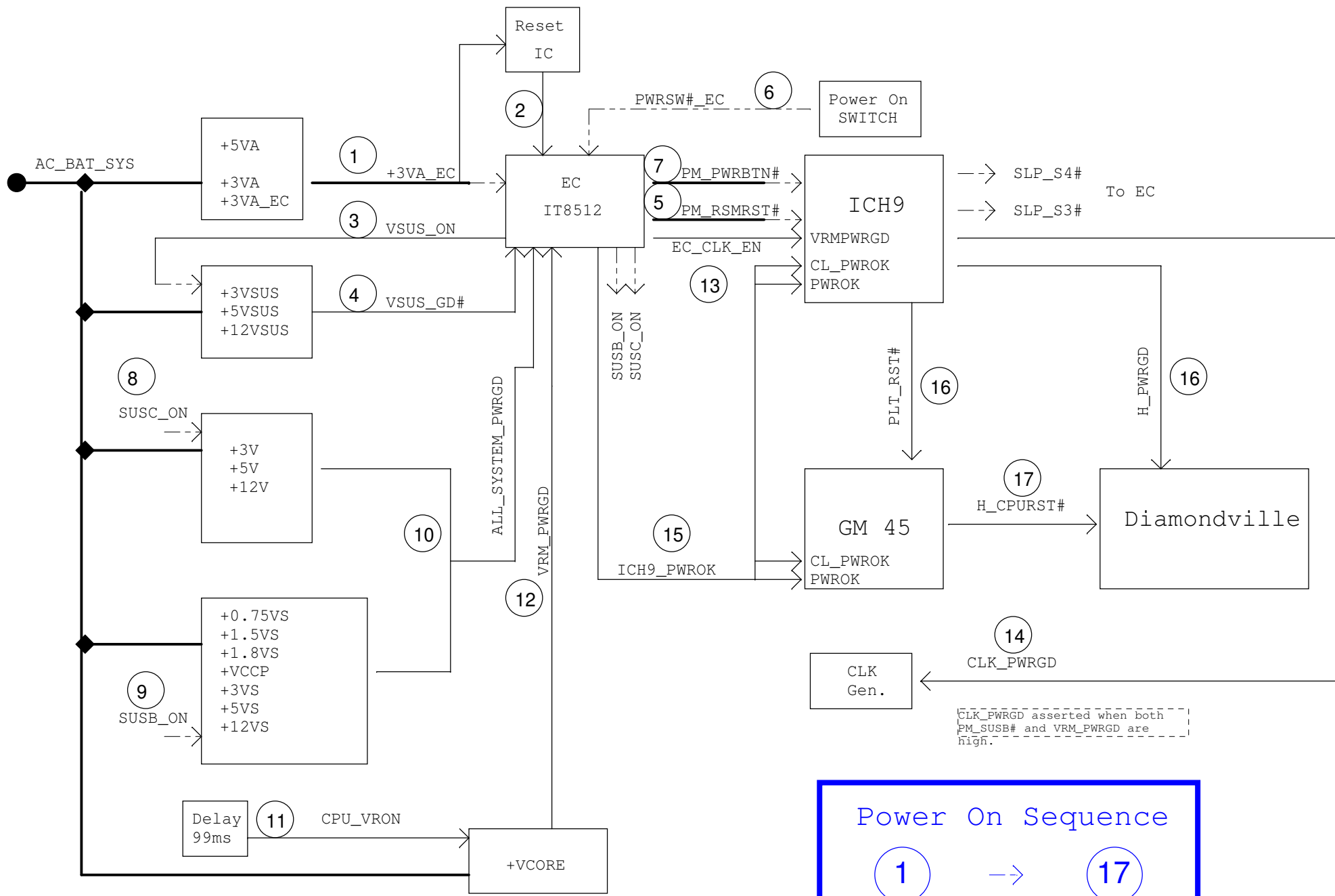
Rev

2.0

Date: Friday, October 16, 2009

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Rev	Date	Description
1.00		First Release!
1.10		
2.00		



<Variant Name>