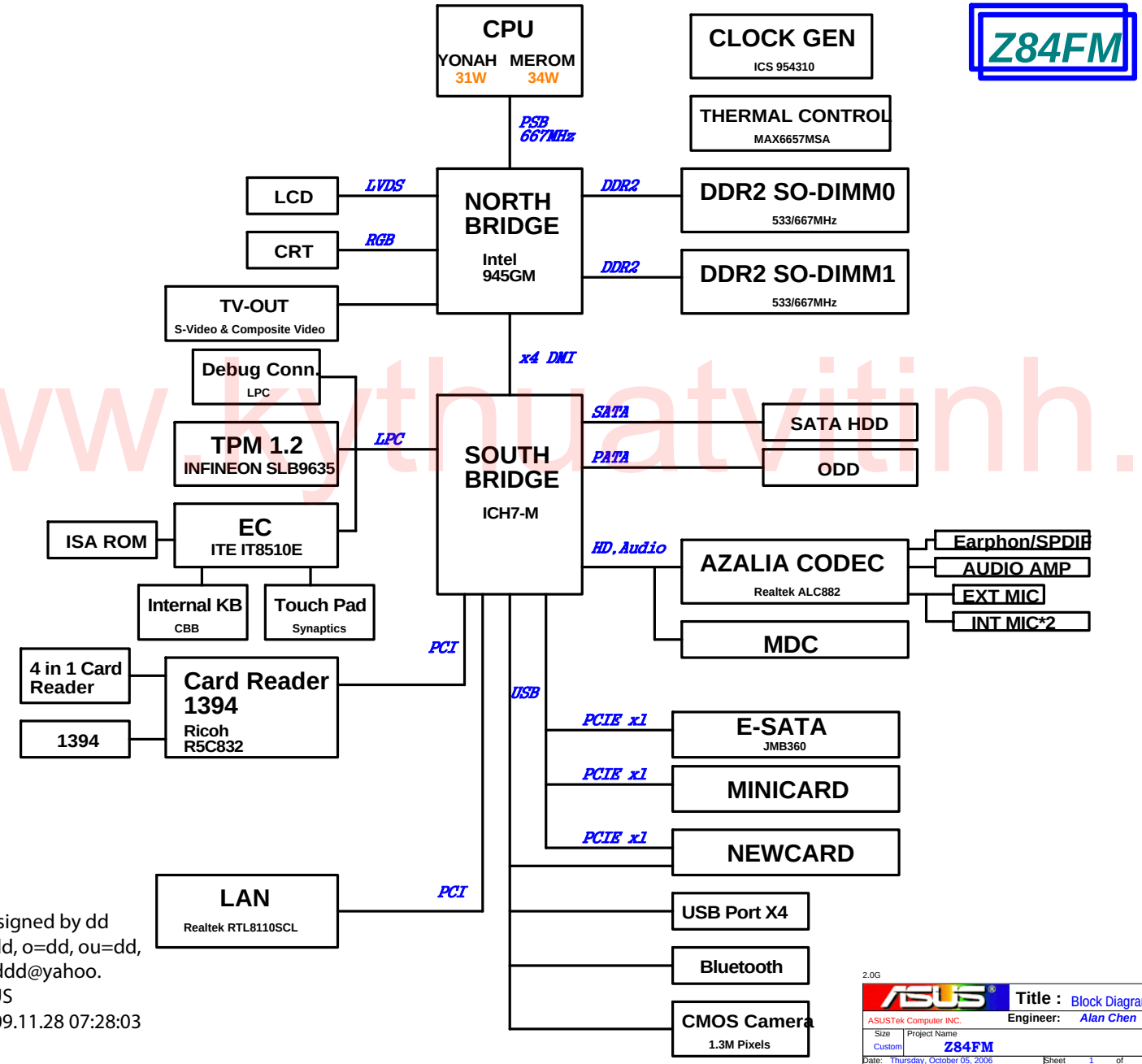


2.0G

ASUSTek Computer INC.

Title : Block Diagram

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 1 of 57

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BL_PWM_DA	O
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	CLK_PWRSAVE#	O
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/0
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	/	
47	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	Mail_LED	O
172	TMRI0/WUI2/GPC4	AC_OK#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	/	
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	/	
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	/	
87	ADC4/GPE0	EMAIL_SW#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	PWR4G_SW#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	/	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I
115	PS2DAT1/GPF3	/	I
116	PS2CLK2/GPF4	TP_CLK	I/0
117	PS2DAT2/GPF5	TP_DAT	I/0
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	/	
113	FA16/GPG0	FA16	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	CPUPWR_GD#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	/	
152	GPI2	MCHOK	I
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCI_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCI_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCI_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCI_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCI_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	I	Core(To:3.3V)	GPI
E21	GPIO08	EXTSMI#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SCI#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16	PM_DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCI_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PCI#	STP_PCI#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCI_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCI_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	I	V_CPU_IO	Native

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	INTB-->INTB
1394	AD17	0	INTA-->INTA
LAN	AD16	2	INTA-->INTD

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

2.0G

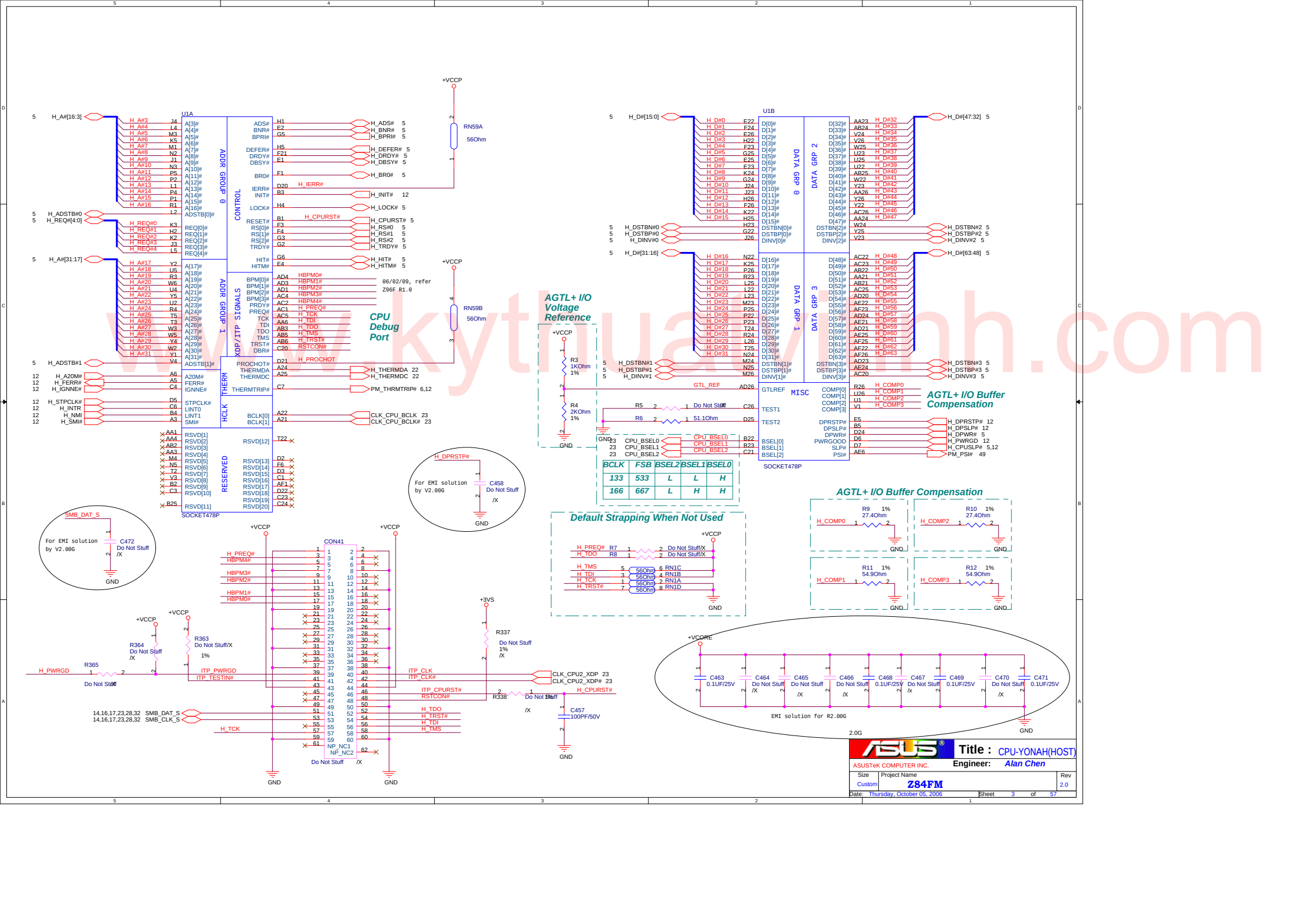
ASUSTek Computer INC.

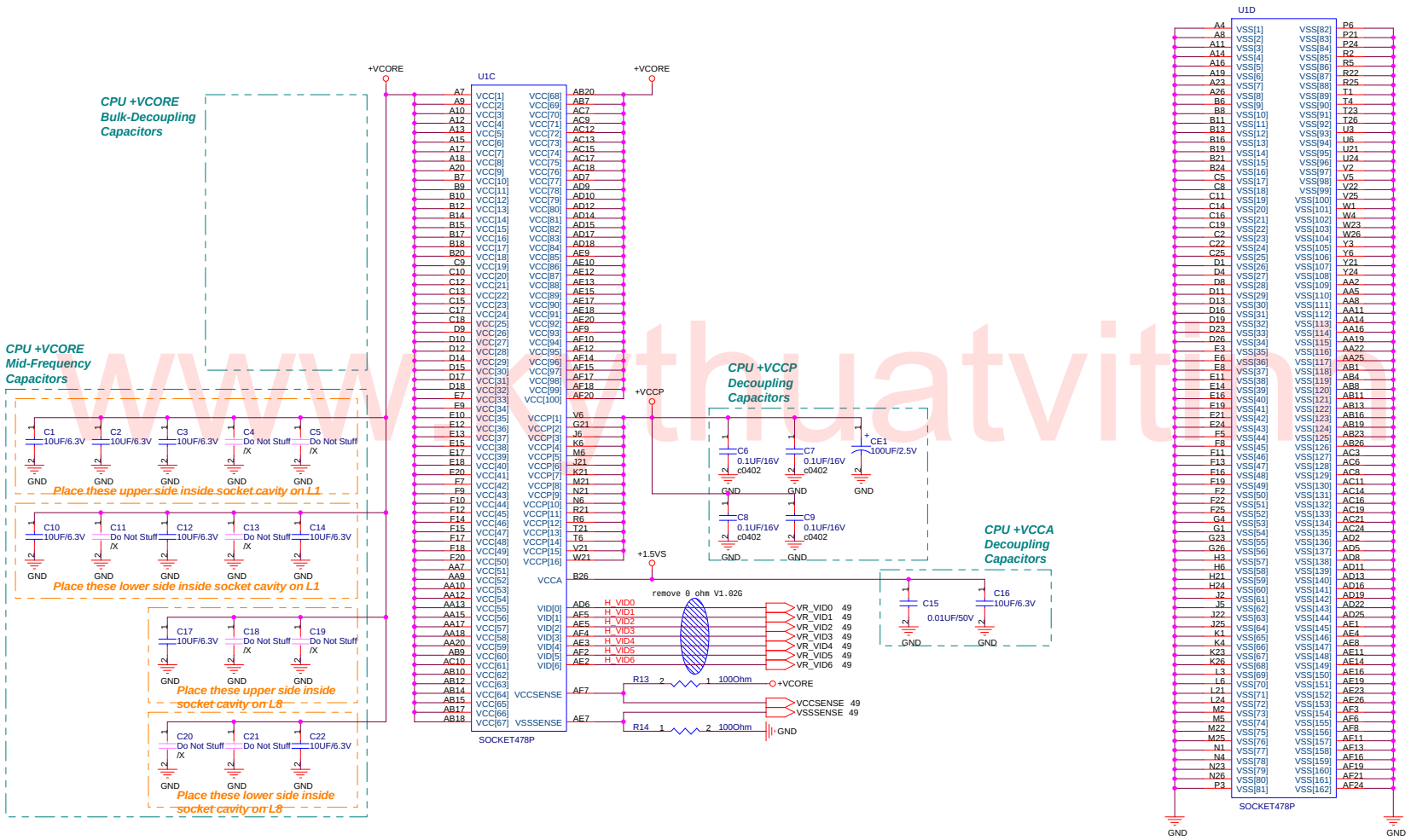
Title : <Title>

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 2 of 57





+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*R1F: 10UF *16*
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*R1F: 220UF *1, 0.1UF *4*

2.0G

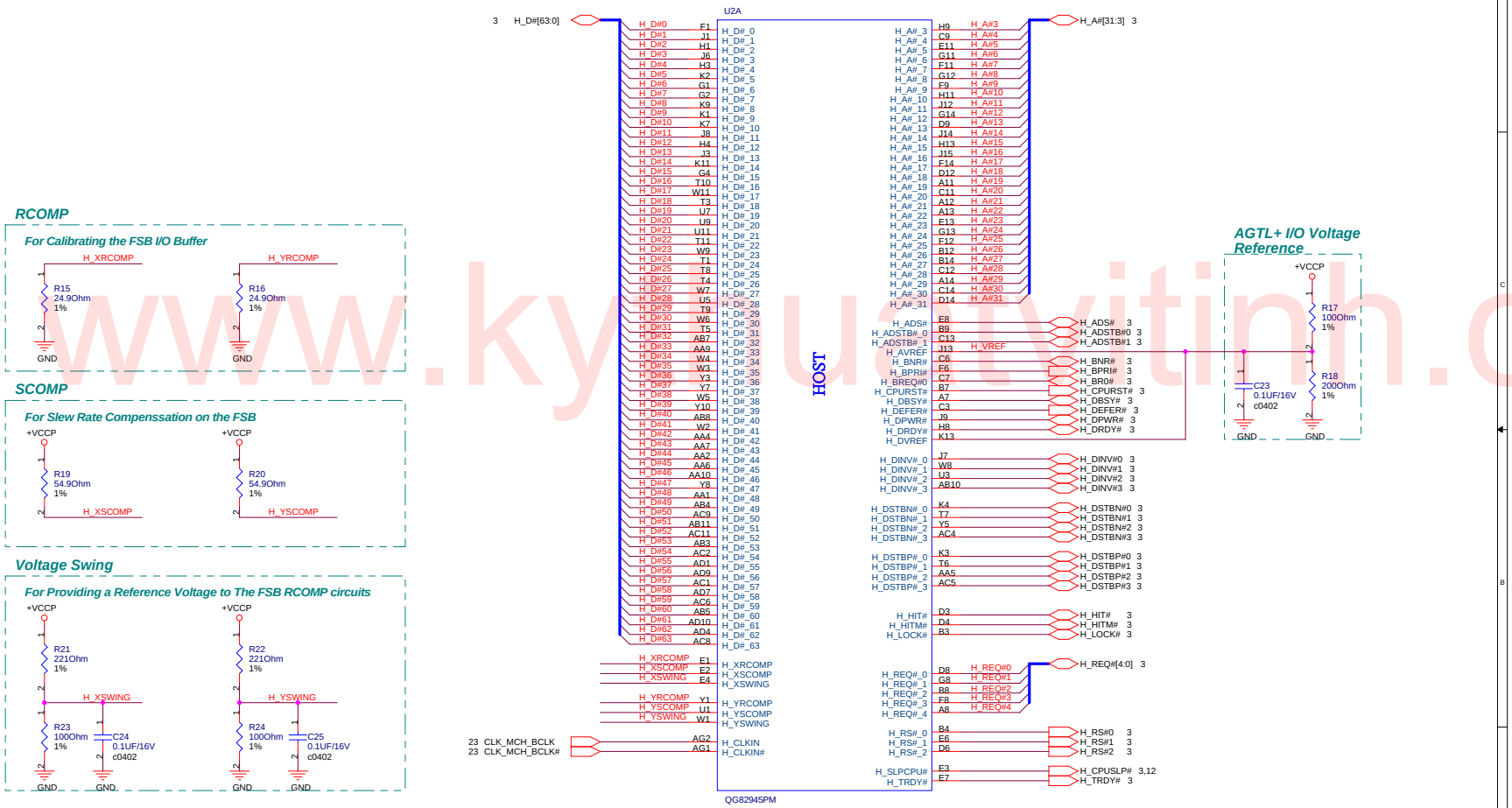
ASUSTeK COMPUTER INC. NB1

Title : CPU_YONAH(PWR)

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 4 of 57



2.0G

ASUSTeK COMPUTER INC.

Title : NB-945GM(HOST)

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 5 of 57

GMCH Strapping

CFG5 : DMI Strap

0 = DMI x2

1 = DMI x4 (D)

MCH_CFG_5 — R25 /X — Do Not Stuff — GND

CFG[13:12] : GMCH Test Mode

00= Partial CLK Gating Disable

01 = XOR Mode Enable

10 = All Z Mode Enable

11 = Normal Operation (D)

CFG7 : CPU Strap

0 = DT/Transpotable CPU

1 = Mobile CPU (D)

MCH_CFG_7 — R26 /X — Do Not Stuff — GND

CFG15 : ICH RESET Disable

0 = ICH Reset Disable

1 = Normal Operation (D)

MCH_CFG_15 — R27 /X — Do Not Stuff — GND

CFG9 : PCIE Graphic Lane

0 = Reverse Lane

1 = Normal Operation (D)

MCH_CFG_9 — R30 — 1KOhm — GND

CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable

1 = Dynamic ODT Enable (D)

MCH_CFG_16 — R31 /X — Do Not Stuff — GND

CFG10 : HOST PLL VCO Select

0 = Reserved

1 = Mobility (D)

MCH_CFG_10 — R34 /X — Do Not Stuff — GND

CFG18 : VCC Select

0 = 1.05V (D)

1 = 1.5V

+2.5VS — MCH_CFG_18 — R35 /X — Do Not Stuff

CFG11 : PSB 4x CLK Enable

0 = 4x Enable

1 = 8x Enable (D)

MCH_CFG_11 — R37 /X — Do Not Stuff — GND

CFG19 : DMI Lane Reversal

0 = Normal Operation (D)

1 = Lanes Reversed

+2.5VS — MCH_CFG_19 — R38 /X — Do Not Stuff

Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

U2B

RSVD: RSVD_1 T32, RSVD_2 R32, RSVD_3 E3, RSVD_4 F7, RSVD_5 AG11, RSVD_6 AF11, RSVD_7 H7, RSVD_8 J19, TV_DCONSEL_0 K30, TV_DCONSEL_1 J29, RSVD_11 A41, RSVD_12 A35, RSVD_13 A34, RSVD_14 D28, RSVD_15 D27

CFG: 23 MCH_BSEL0 → CFG_0 K16; 23 MCH_BSEL1 → CFG_1 K18; 23 MCH_BSEL2 → CFG_2 J18; CFG_3 F18; CFG_4 E15; MCH_CFG_5 → CFG_5 F15; CFG_6 E18; MCH_CFG_7 → CFG_7 D19; CFG_8 D16; MCH_CFG_9 → CFG_9 G16; MCH_CFG_10 → CFG_10 E16; MCH_CFG_11 → CFG_11 D15; CFG_12 G15; CFG_13 K15; CFG_14 C15; MCH_CFG_15 → CFG_15 H16; MCH_CFG_16 → CFG_16 G18; CFG_17 H15; MCH_CFG_18 → CFG_18 J25; MCH_CFG_19 → CFG_19 K27; CFG_20 J26

PM: PM_BMBUSY# G28, PM_EXTTS#_0 F25, PM_EXTTS#_1 H26, PM_THRMTRIP# G6, PWROK AH33, RSTIN# AH34

MISC: SDVO_CTRLCLK H28, SDVO_CTRLDATA H27, ICH_SYNC# K28, CLK_REQ# H32

NC: NC0 D1, NC1 C41, NC2 C1, NC3 BA41, NC4 BA40, NC5 BA39, NC6 BA3, NC7 BA2, NC8 BA1, NC9 B41, NC10 B2, NC11 AY41, NC12 AY1, NC13 AW41, NC14 AW1, NC15 A40, NC16 A4, NC17 A39, NC18 A3

QG82945PM

+3VS — 14 PM_BMBUSY# — R32 10KOhm 0402 PM_EXTTS#_0 — R33 10KOhm 0402 PM_EXTTS#_1

3,12 PM_THRMTRIP# — 14,35,49,54 VRM_PWRGD — R36 100Ohm RST_IN_MCH# — 13,14,28,32 BUF_PLT_RST#

13 MCH_ICH_SYNC#

T3 Do Not Stuff — GND

DDR MUXING: SM_CK_0 AY35, SM_CK_1 AR1, SM_CK_2 AW7, SM_CK_3 AW40 → M_CLK_DDR0 16, M_CLK_DDR1 16, M_CLK_DDR2 17, M_CLK_DDR3 17

SM_CK#_0 AW35, SM_CK#_1 AT1, SM_CK#_2 AY7, SM_CK#_3 AY40 → M_CLK_DDR#0 16, M_CLK_DDR#1 16, M_CLK_DDR#2 17, M_CLK_DDR#3 17

SM_CKE_0 AU20, SM_CKE_1 AT20, SM_CKE_2 BA29, SM_CKE_3 AY29 → M_CKE0 16,18, M_CKE1 16,18, M_CKE2 17,18, M_CKE3 17,18

SM_CS#_0 AW13, SM_CS#_1 AW12, SM_CS#_2 AY21, SM_CS#_3 AW21 → M_CS#0 16,18, M_CS#1 16,18, M_CS#2 17,18, M_CS#3 17,18

SM_OCDCOMP_0 AL20, SM_OCDCOMP_1 AF10

SM_ODT_0 BA13, SM_ODT_1 BA12, SM_ODT_2 AY20, SM_ODT_3 AU21 → M_ODT0 16,18, M_ODT1 16,18, M_ODT2 17,18, M_ODT3 17,18

SM_RCOMP# AV9 — R28 80.6Ohm 1% — +1.8V; SM_RCOMP AT9 — R29 80.6Ohm 1%

SM_VREF_0 AK1, SM_VREF_1 AK41 — M_VREF_MCH — M_VREF_MCH 16,17,18

CLK: G_CLKIN# AF33, G_CLKIN AG33, D_REFCLKIN# A27, D_REFCLKIN A26, D_REFSSCLKIN# C40, D_REFSSCLKIN D41 → CLK_MCH_3GPLL# 23, CLK_MCH_3GPLL 23, CLK_UMA_96M# 23, CLK_UMA_96M 23, CLK_LCD_SSCG# 23, CLK_LCD_SSCG 23

DMI: DMI_RXN_0 AE35, DMI_RXN_1 AF39, DMI_RXN_2 AG35, DMI_RXN_3 AH39 → DMI_TXN0, DMI_TXN1, DMI_TXN2, DMI_TXN3 → DMI_TXN[3:0] 13

DMI_RXP_0 AC35, DMI_RXP_1 AE39, DMI_RXP_2 AF35, DMI_RXP_3 AG39 → DMI_TXP0, DMI_TXP1, DMI_TXP2, DMI_TXP3 → DMI_TXP[0..3] 13

DMI_TXN_0 AE37, DMI_TXN_1 AF41, DMI_TXN_2 AG37, DMI_TXN_3 AH41 → DMI_RXN0, DMI_RXN1, DMI_RXN2, DMI_RXN3 → DMI_RXN[0..3] 13

DMI_TXP_0 AC37, DMI_TXP_1 AE41, DMI_TXP_2 AF37, DMI_TXP_3 AG41 → DMI_RXP0, DMI_RXP1, DMI_RXP2, DMI_RXP3 → DMI_RXP[0..3] 13

M_VREF_MCH — C26 0.1UF/16V c0402 — GND; C27 1UF/10V — GND

2.0G

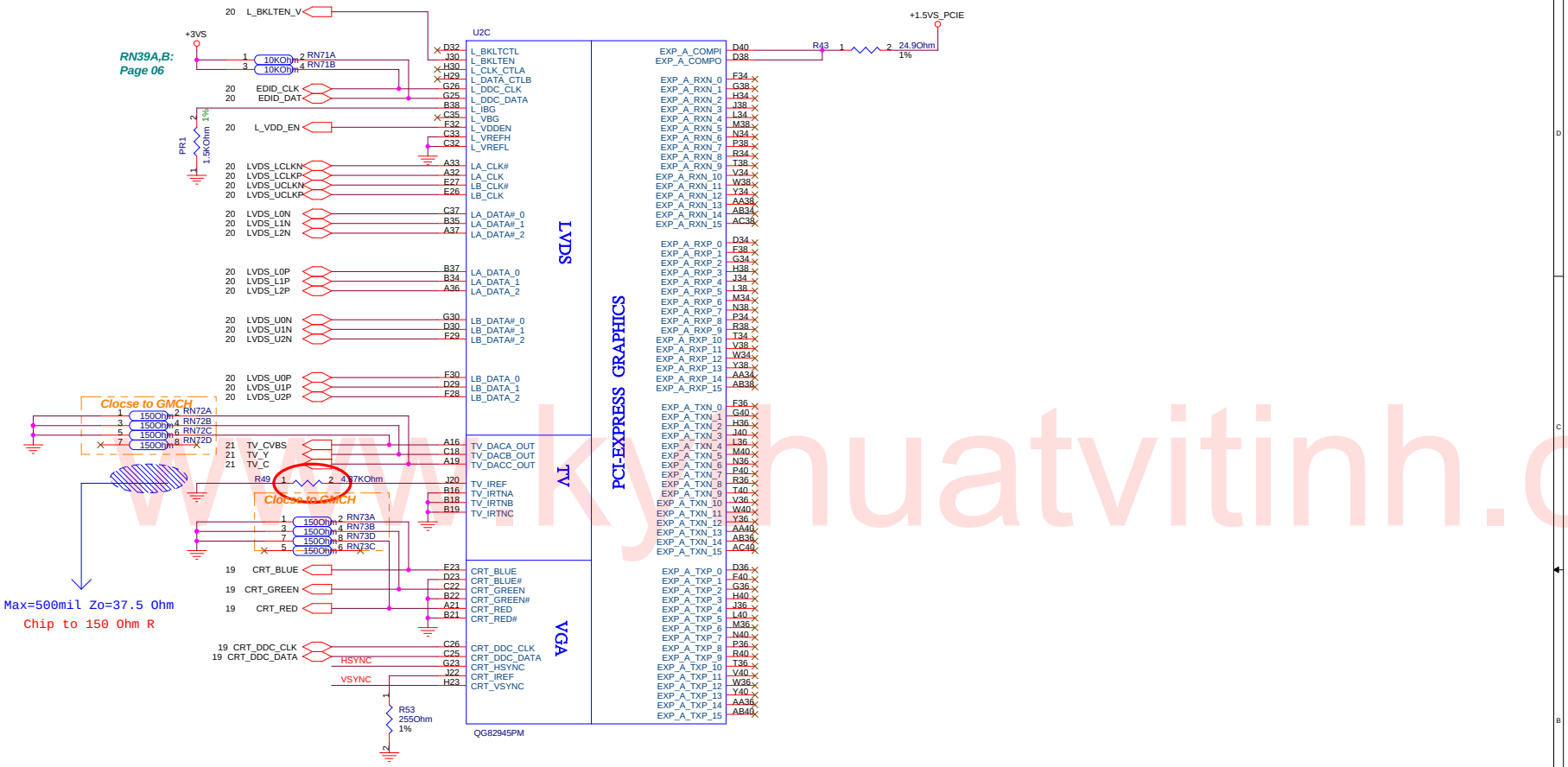
ASUSTeK COMPUTER INC.

Title : NB-945GM(DMI & CFG)

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 6 of 57



2.0G

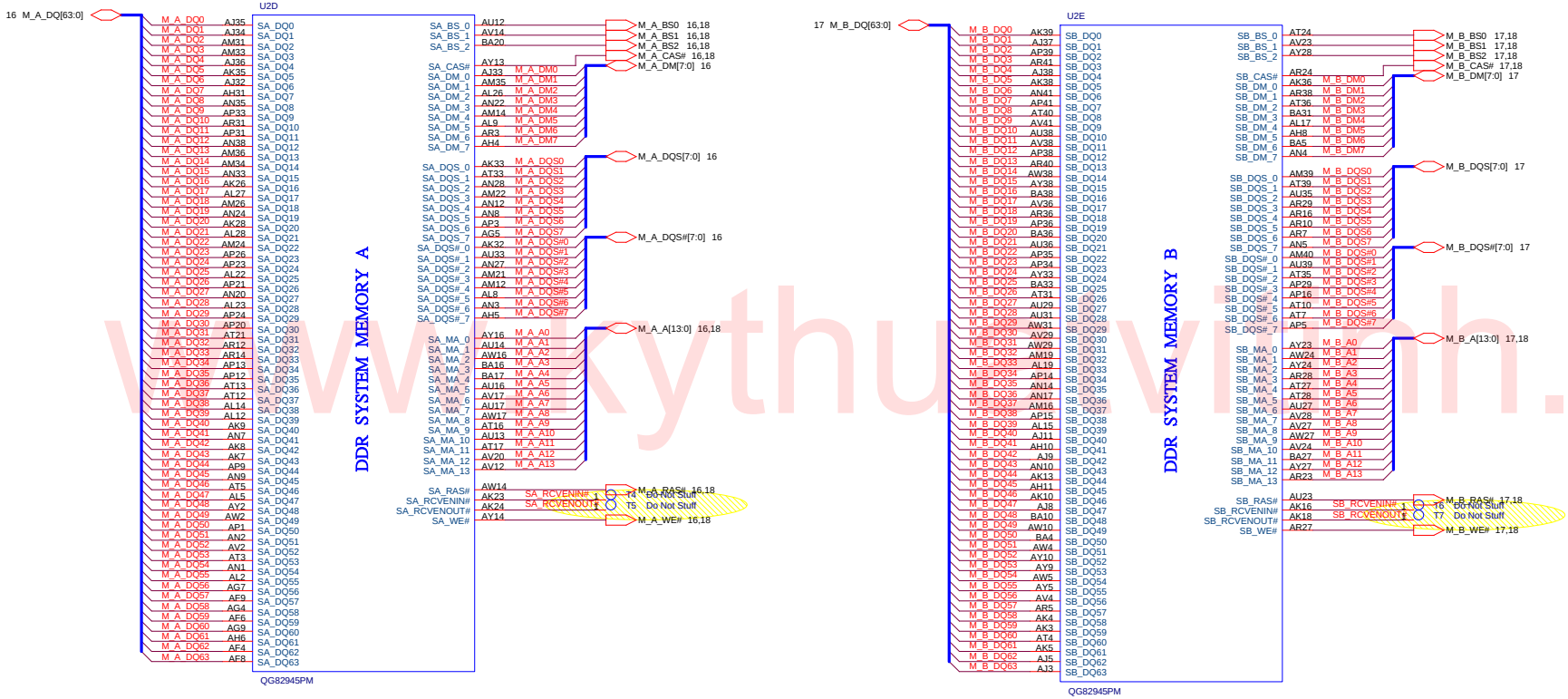
ASUSTeK COMPUTER INC.

Title : NB_945GM(GRAPHIC)

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 7 of 57



2.0G

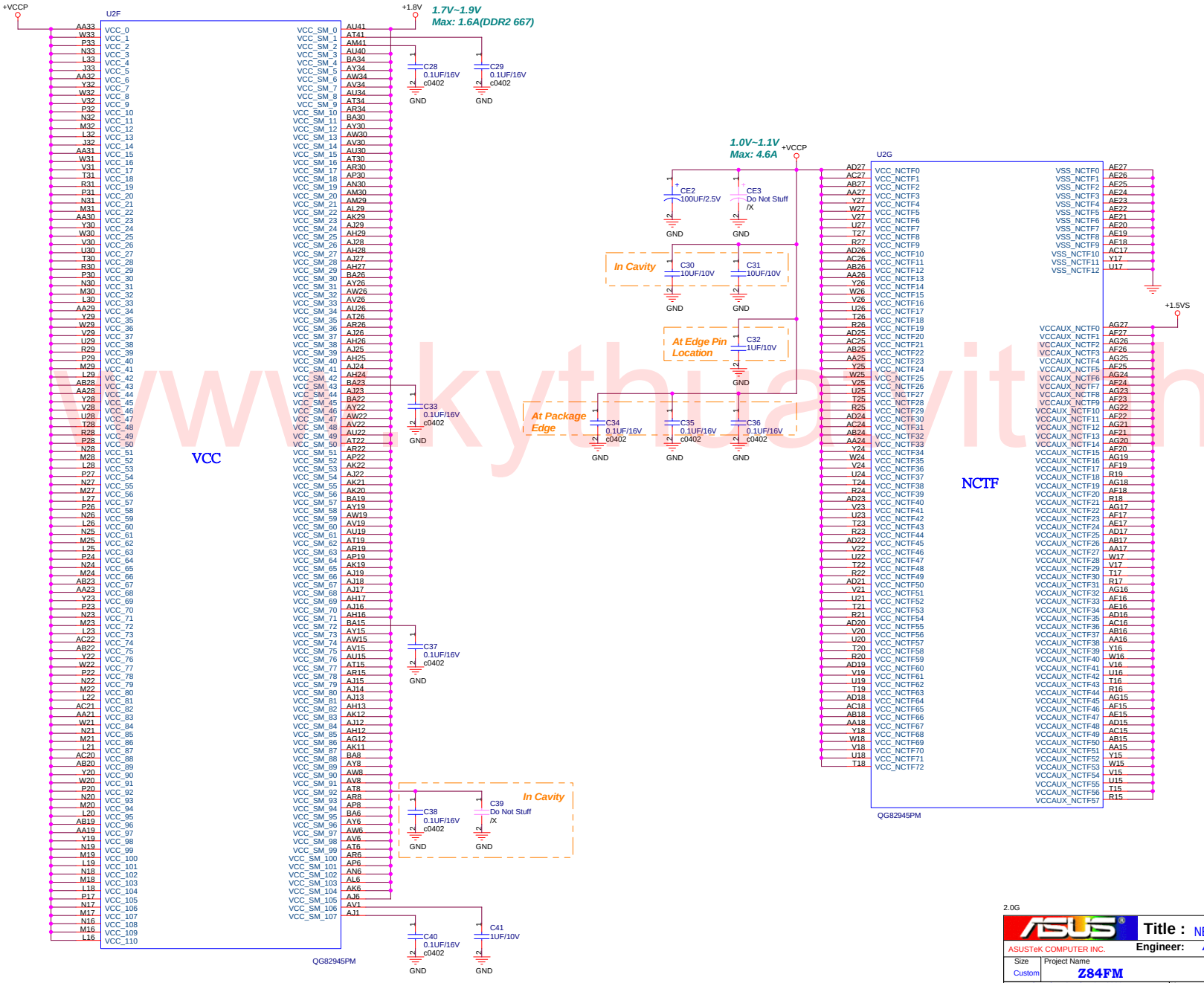
ASUSTeK COMPUTER INC.

Title : NB-945GM(DDR2)

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 8 of 57



2.0G

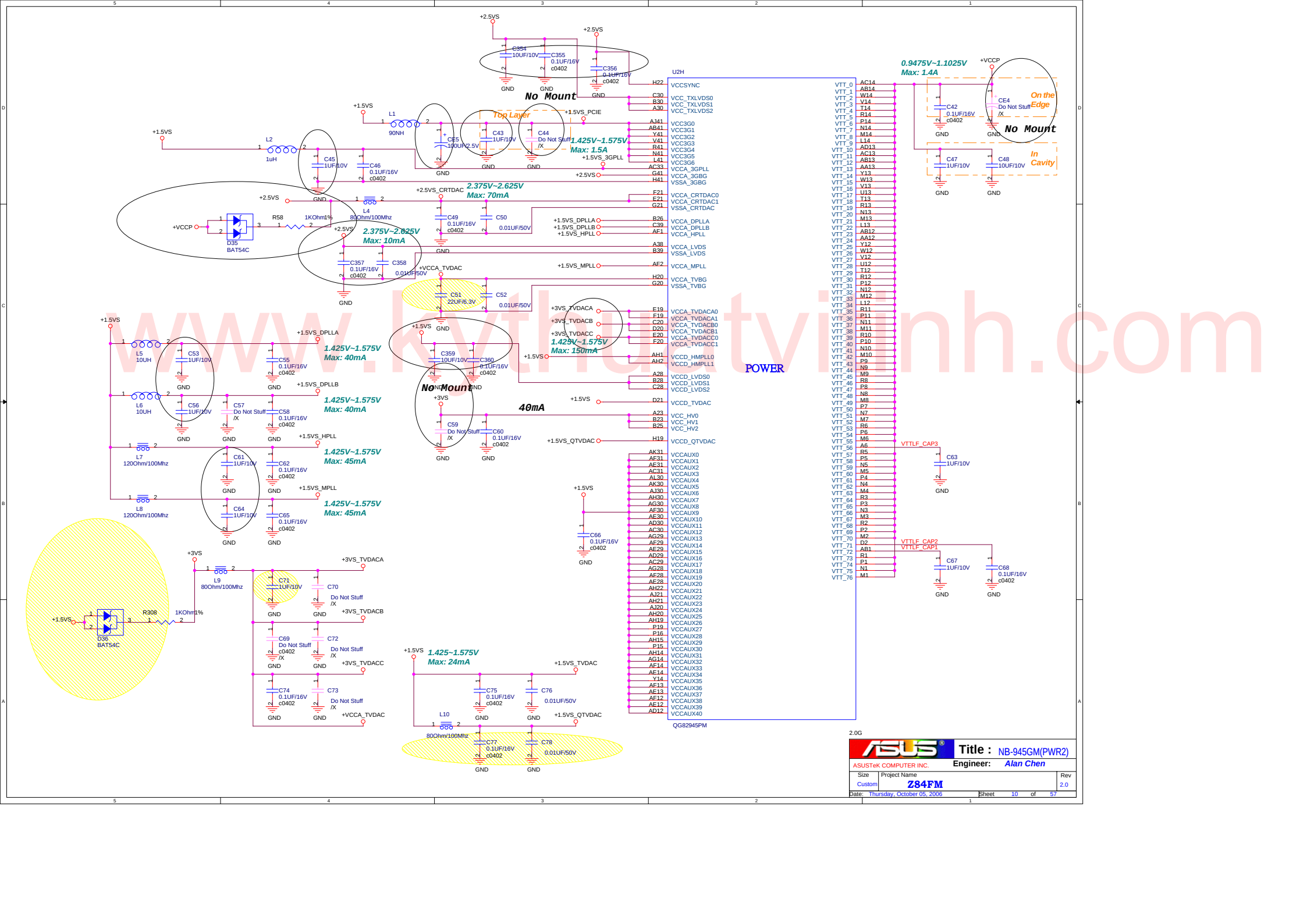
ASUSTeK COMPUTER INC.

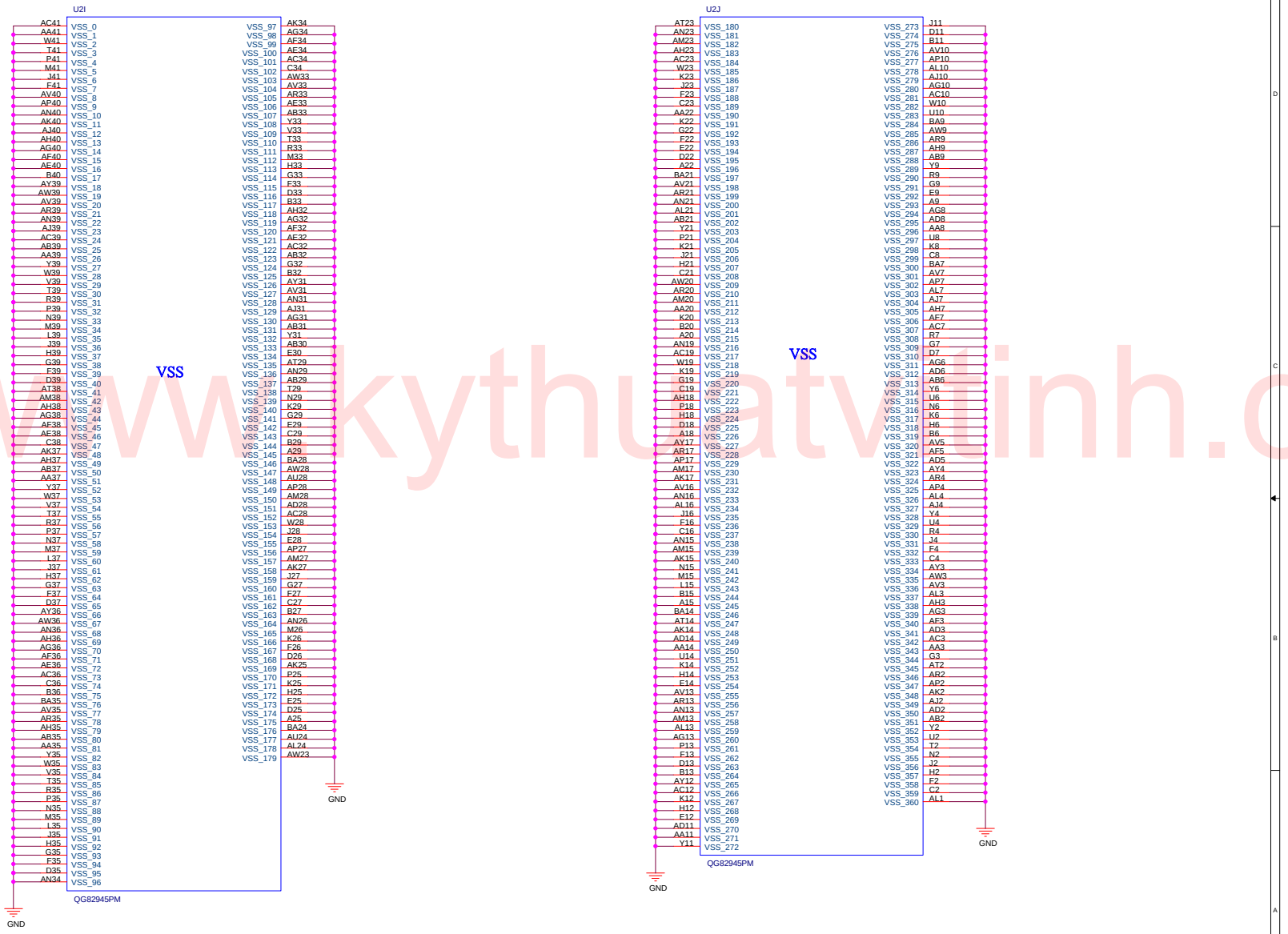
Title : NB-945GM(PWR)

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 9 of 57





2.0G

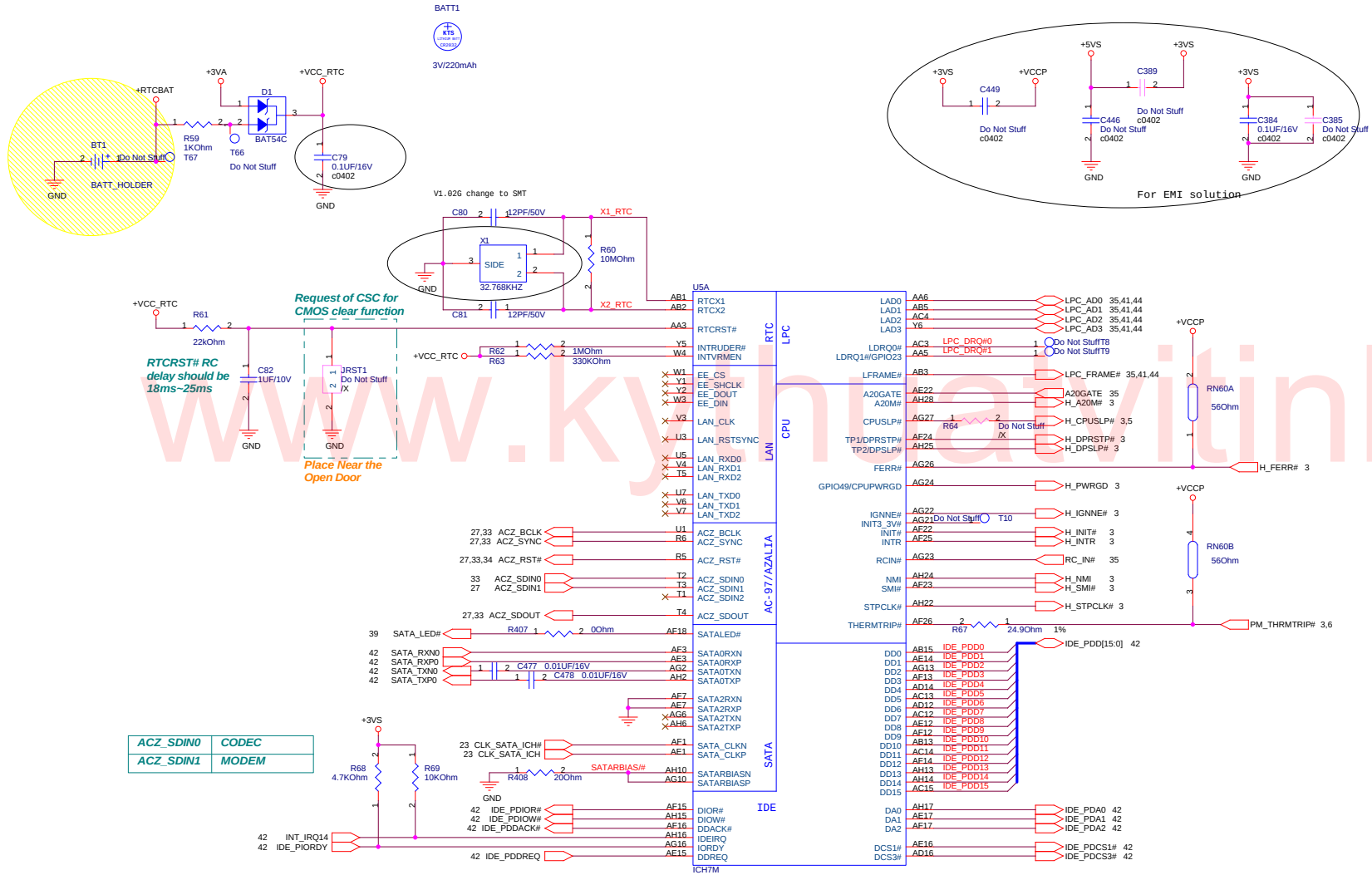
ASUSTeK COMPUTER INC.

Title : NB-945PM(GND)

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 11 of 57



ACZ_SDIN0	CODEC
ACZ_SDIN1	MODEM

2.0G

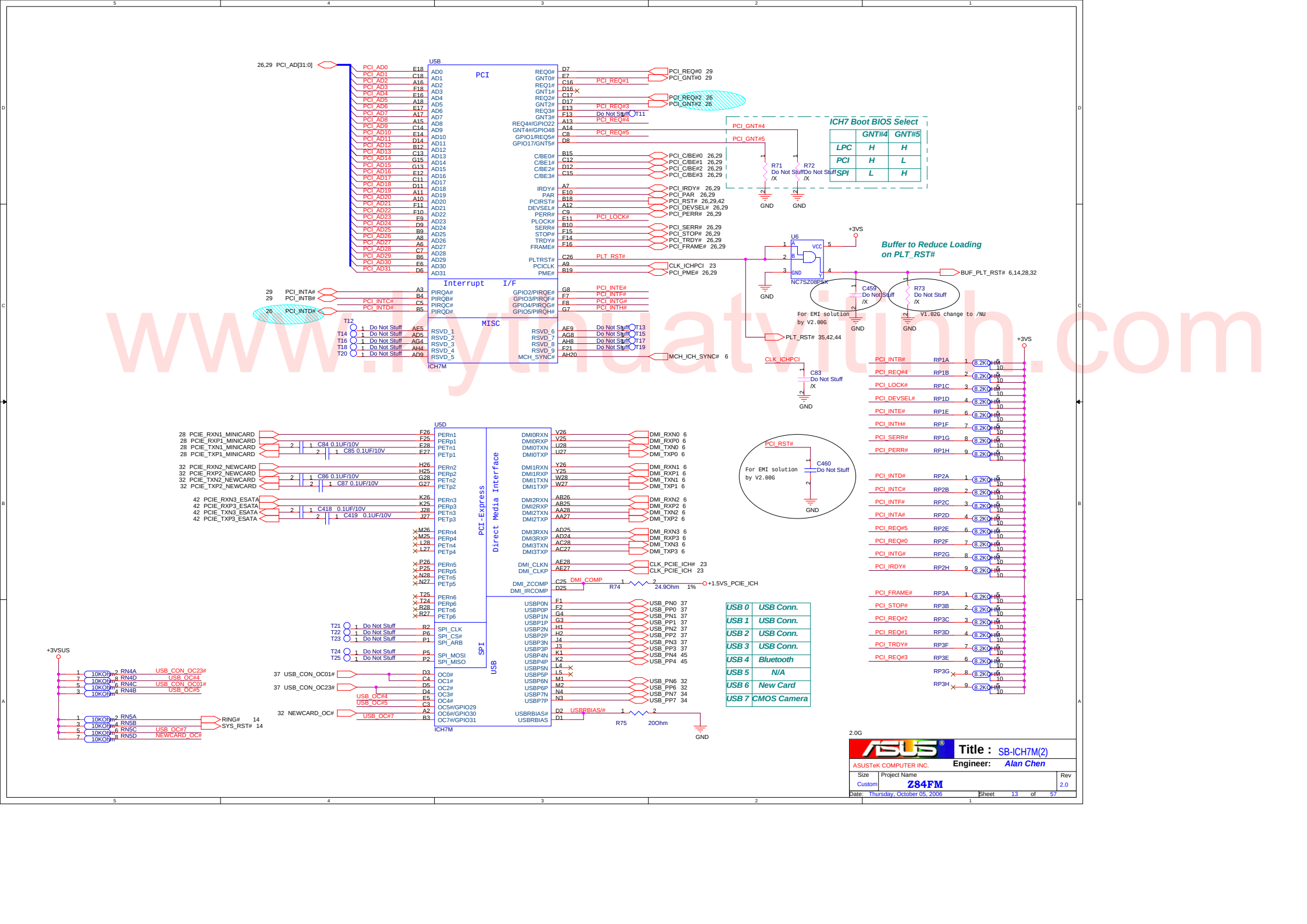
ASUSTeK COMPUTER INC.

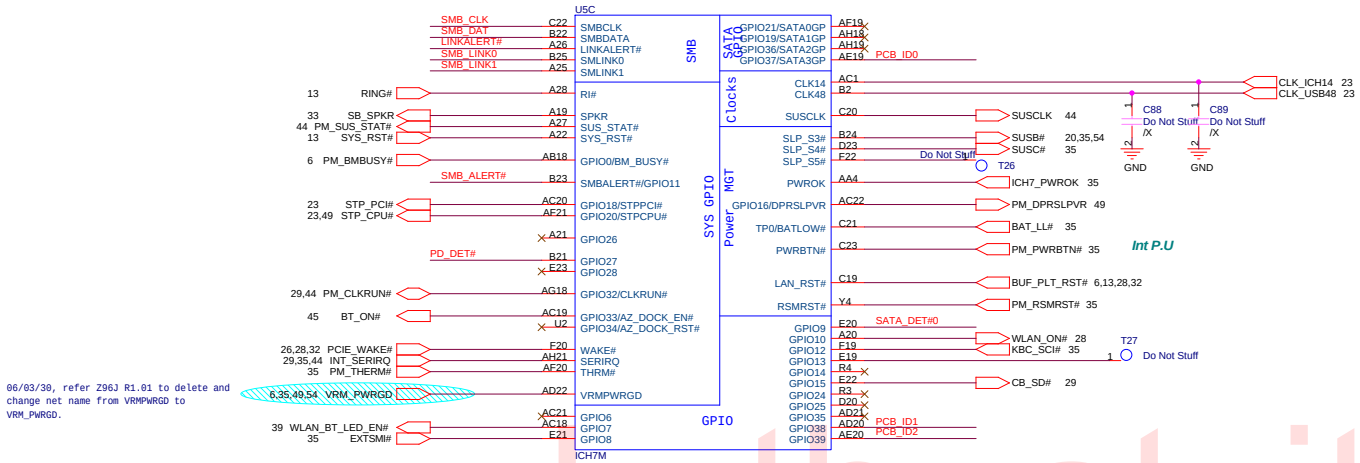
Title : SB-ICH7-M(1)

Engineer: Alan Chen

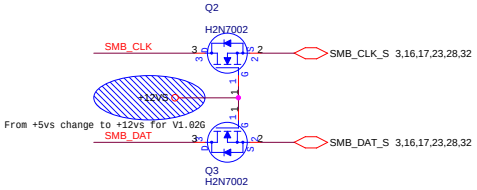
Size	Project Name	Rev
Custom	Z84FM	2.0

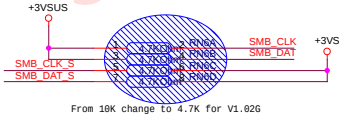
Date: Thursday, October 05, 2006 Sheet 12 of 57

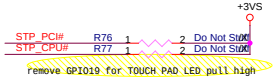


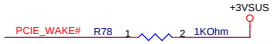


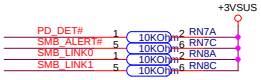
06/03/30, refer Z96J R1.01 to delete and change net name from VRMPWRGD to VRM_PWRGD.

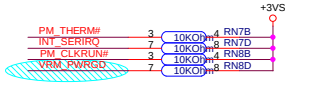


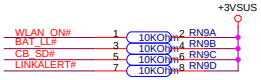


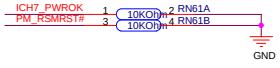


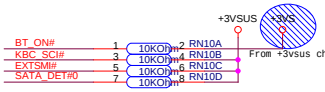


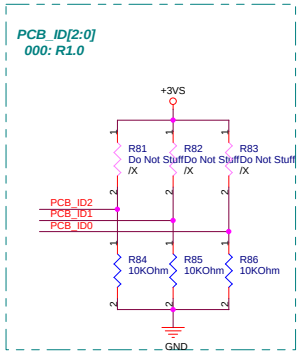












2.0G

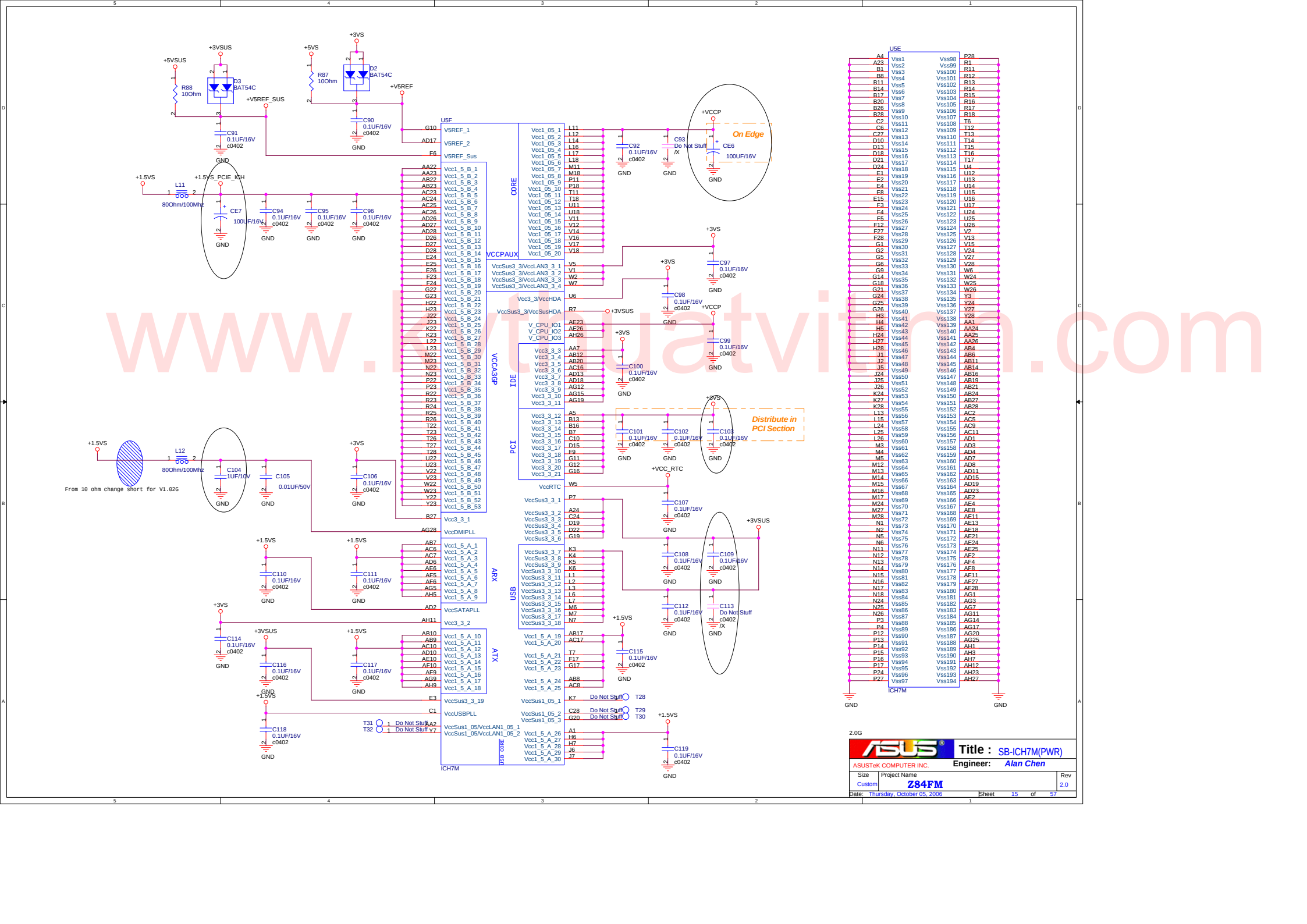
ASUSTeK COMPUTER INC

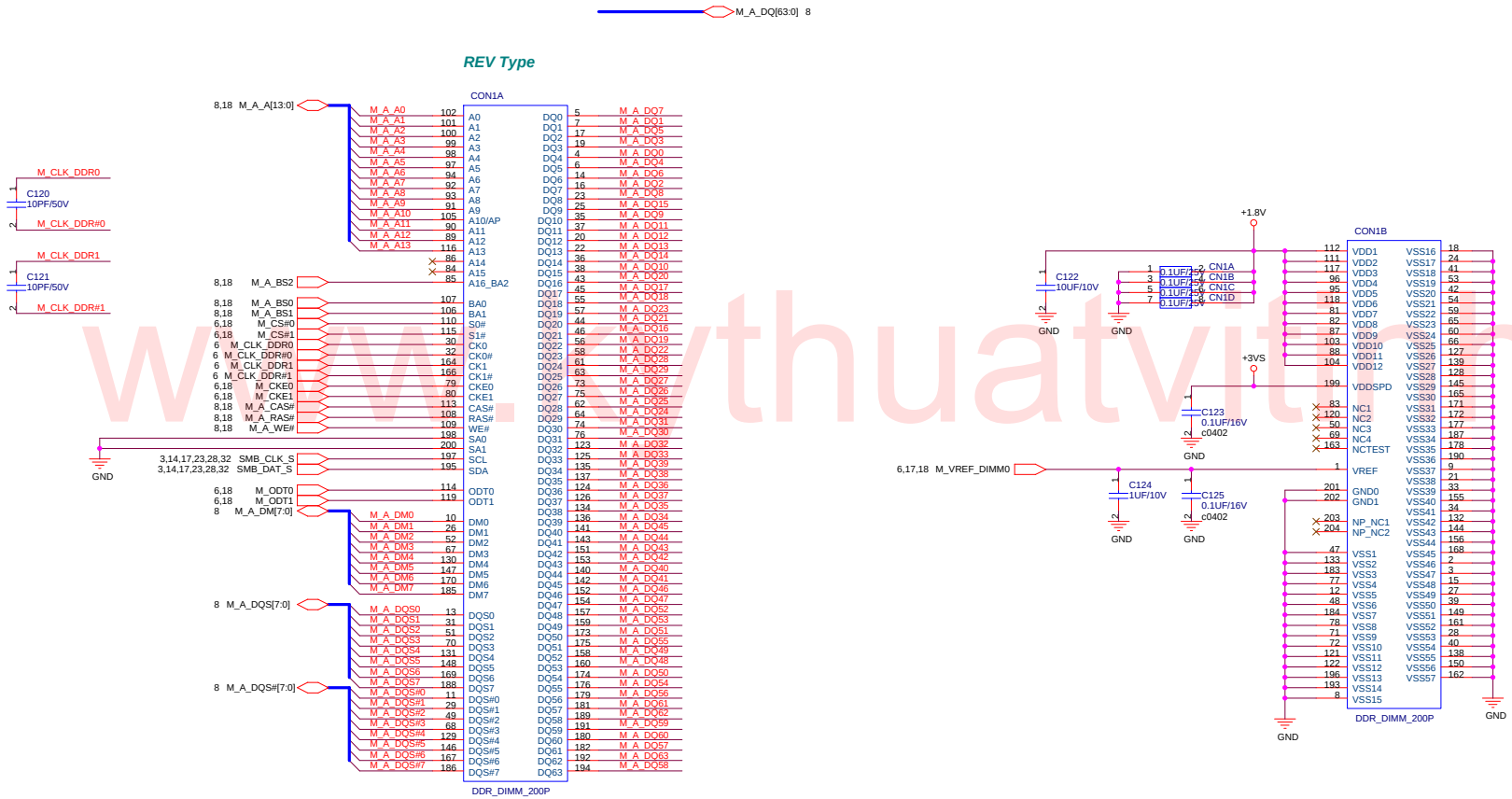
Title : SB-ICH7M(3)

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 14 of 57


+3VSUS
+5VSUS
R88
10Ohm
D3
BAT54C
+5V
R87
10Ohm
D2
BAT54C
+3VS
+V5REF
+V5REF_SUS
C90
0.1UF/16V
c0402
C91
0.1UF/16V
c0402
GND
U5F
V5REF_1
V5REF_2
V5REF_Sus
CORE
VCCPAUX
IDE
PCI
USB
ARX
ATX
VCCA3GP
VccSus3_3/VccLAN3_3_1
VccSus3_3/VccLAN3_3_2
VccSus3_3/VccLAN3_3_3
VccSus3_3/VccLAN3_3_4
Vcc3_3/VccHDA
VccSus3_3/VccSusHDA
V_CPU_IO1
V_CPU_IO2
V_CPU_IO3
VccRTC
VccSATAPLL
VccDMIPLL
VccUSBPLL
VccSus1_05/VccLAN1_05_1
VccSus1_05/VccLAN1_05_2
ICH7M
+1.5VS
+1.5VS_PCIE_IGH
L11
80Ohm/100Mhz
CE7
100UF/16V
C94
0.1UF/16V
C95
0.1UF/16V
C96
0.1UF/16V
L12
C104
1UF/10V
C105
0.01UF/50V
From 10 ohm change short for V1.02G
C106
0.1UF/16V
C110
0.1UF/16V
C111
0.1UF/16V
C114
0.1UF/16V
C116
0.1UF/16V
C117
0.1UF/16V
C118
0.1UF/16V
T31
T32
Do Not Stuff
C92
0.1UF/16V
C93
Do Not Stuff
/X
+VCCP
On Edge
CE6
100UF/16V
C97
0.1UF/16V
C98
0.1UF/16V
C99
0.1UF/16V
C100
0.1UF/16V
R7
C101
0.1UF/16V
C102
0.1UF/16V
C103
0.1UF/16V
Distribute in
PCI Section
+VCC_RTC
C107
0.1UF/16V
C108
0.1UF/16V
C109
0.1UF/16V
C112
0.1UF/16V
C113
Do Not Stuff
/X
C115
0.1UF/16V
C119
0.1UF/16V
T28
T29
T30
U5E
ICH7M
2.0G
ASUSTeK COMPUTER INC.
Title : SB-ICH7M(PWR)
Engineer: Alan Chen
Size
Custom
Project Name
Z84FM
Rev
2.0
Date: Thursday, October 05, 2006
Sheet 15 of 57



2.0G

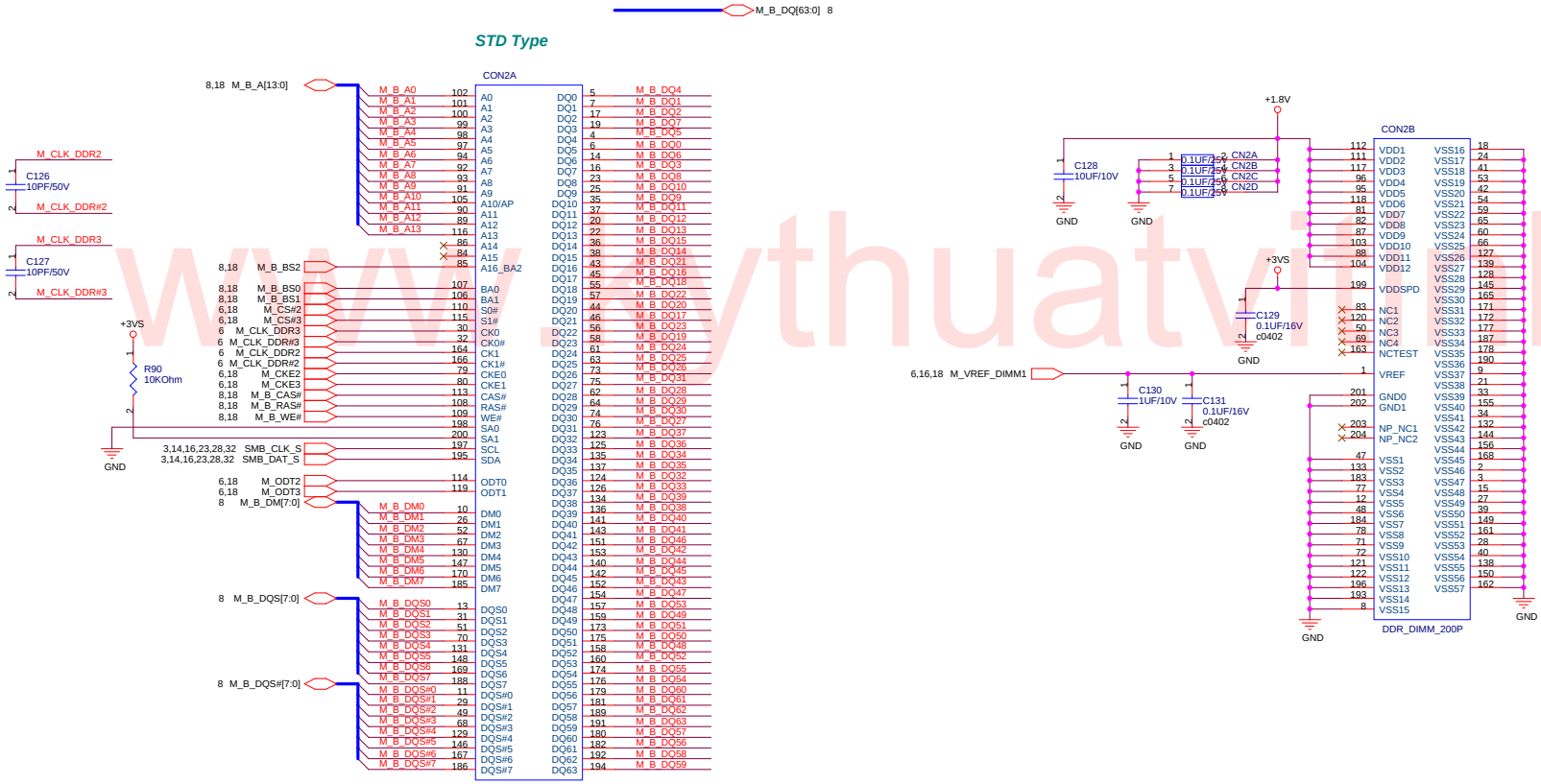
ASUSTeK COMPUTER INC.

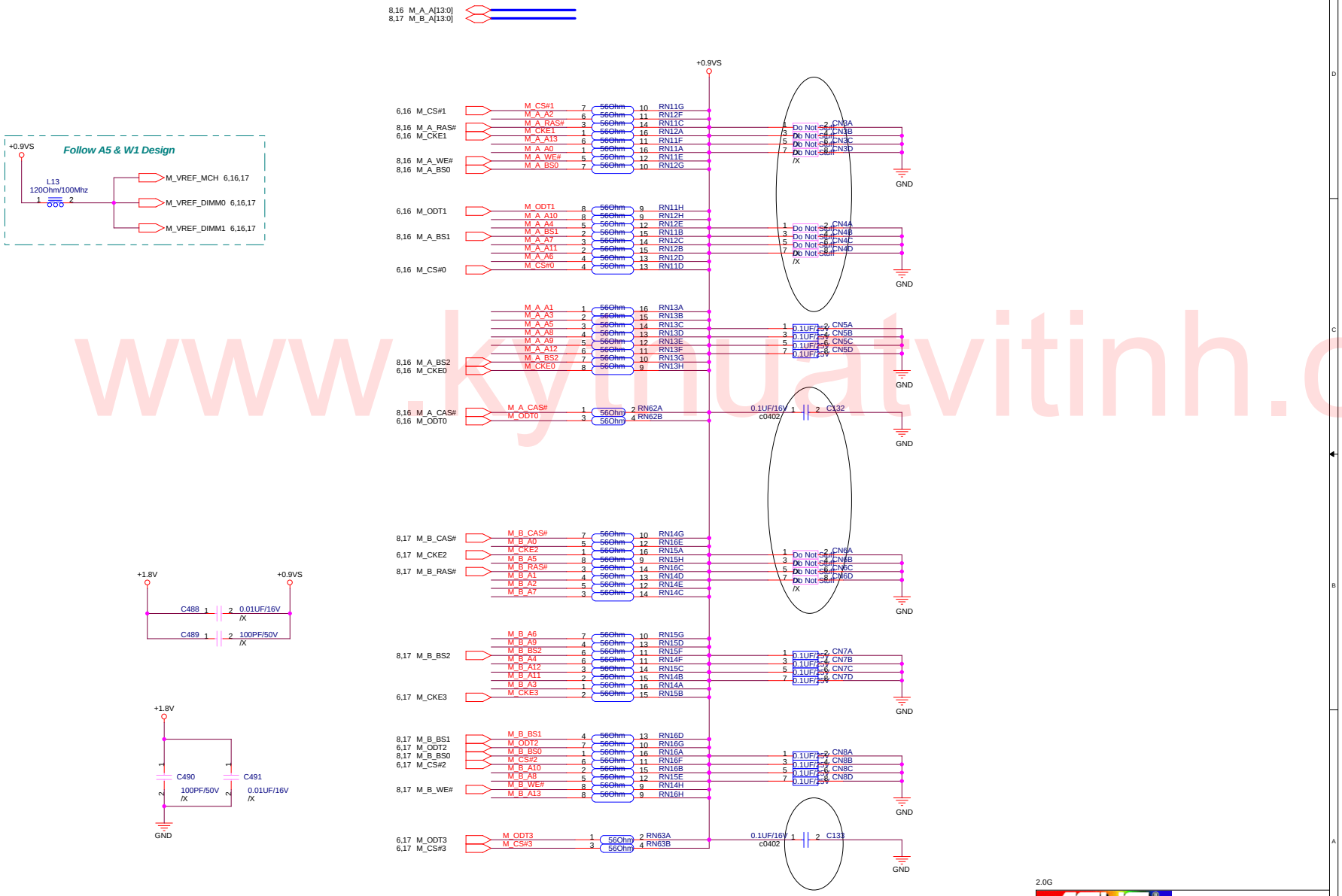
Title : DDR2 SO-DIMM0

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 16 of 57





2.0G

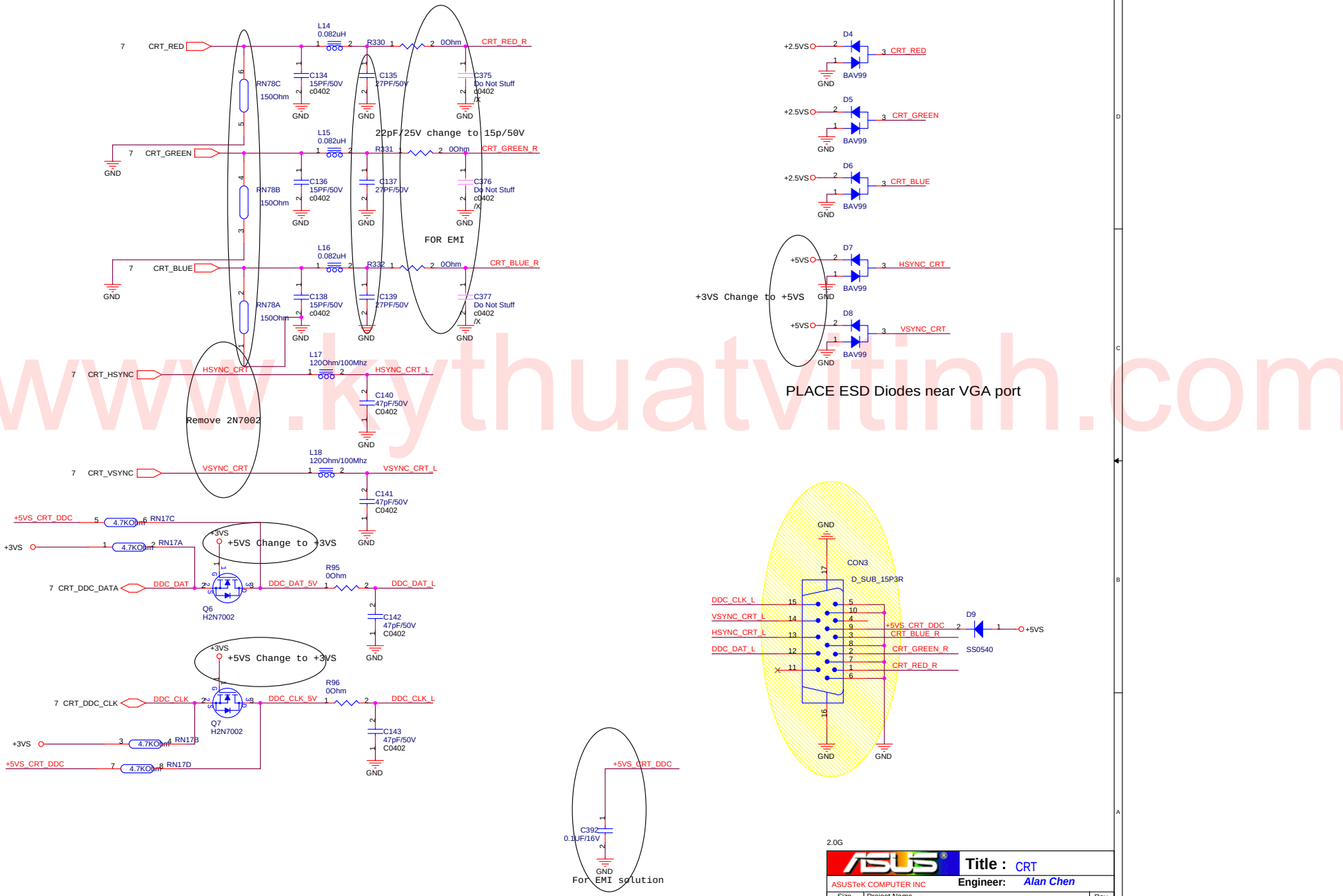
ASUSTeK COMPUTER INC. NB1

Title : DDR2 TERMINATION

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 18 of 57



2.0G

Title : CRT

ASUSTeK COMPUTER INC

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 19 of 57

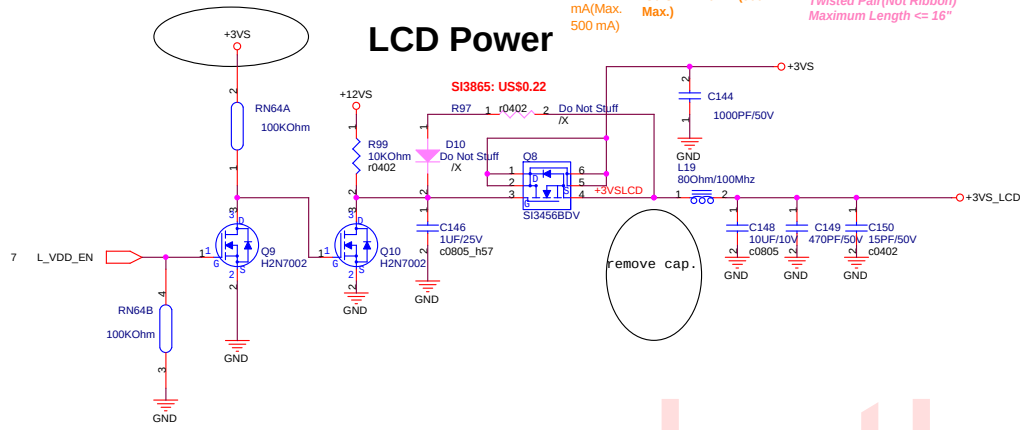
LCD Backlight Control

3V-3.6V Full Active: 410 mA(Max. 500 mA)

3-3.6V S0-S1M:410 mA(500 mA Max.)

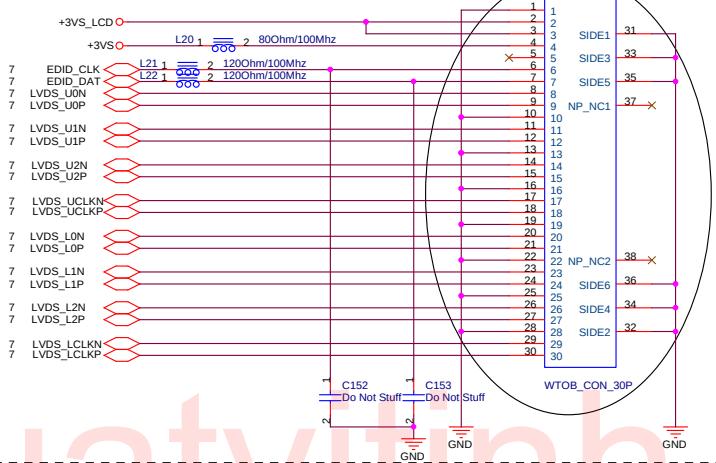
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD Power



LCD LVDS Interface

Updata pin define

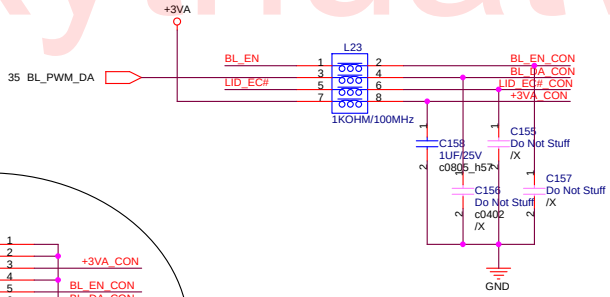


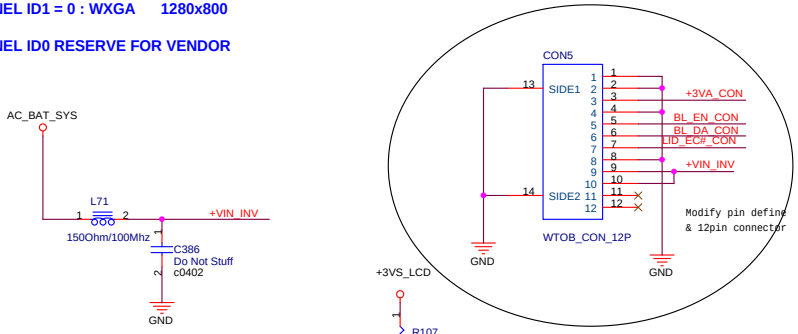
INVERTER Interface/Speaker CONN.

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

PANEL ID1 = 1 : WSXGA+ 1680x1050
PANEL ID1 = 0 : WXGA 1280x800

PANEL ID0 RESERVE FOR VENDOR

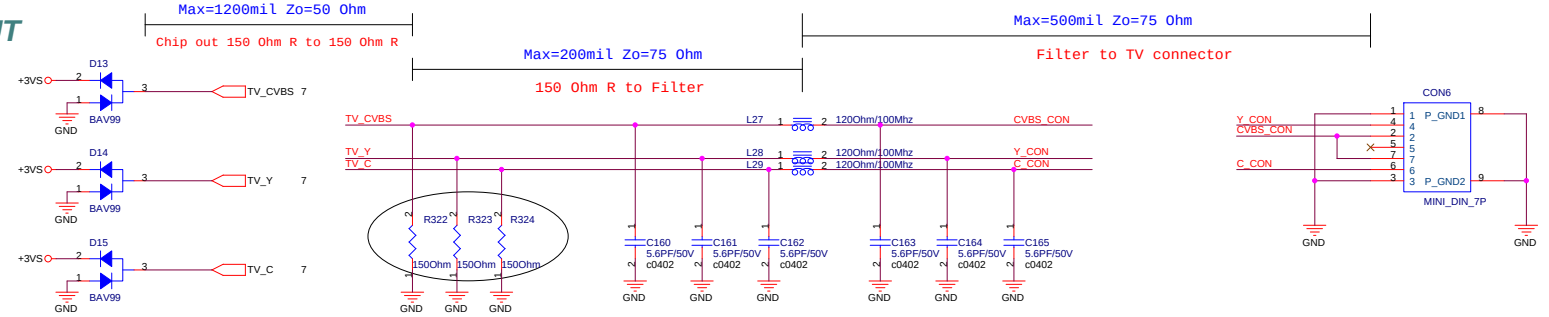




2.0G

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Thursday, October 05, 2006	Sheet 20 of 57	

TV OUT



PLACE ESD
Diodes near
TV port

2.0G

ASUSTeK COMPUTER INC

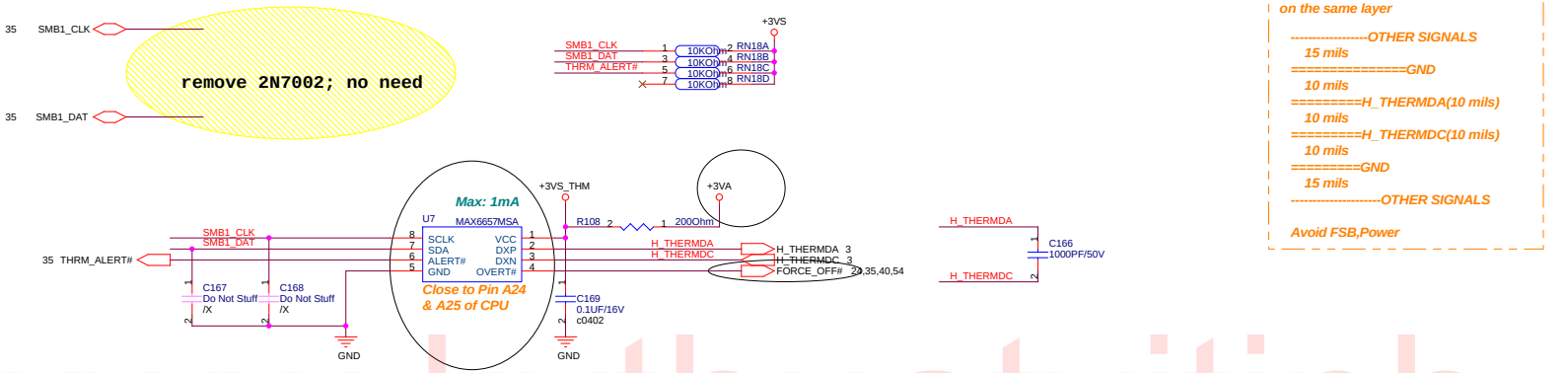
Title : TV OUT & DVI CON.

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 21 of 57

Thermal Sensor

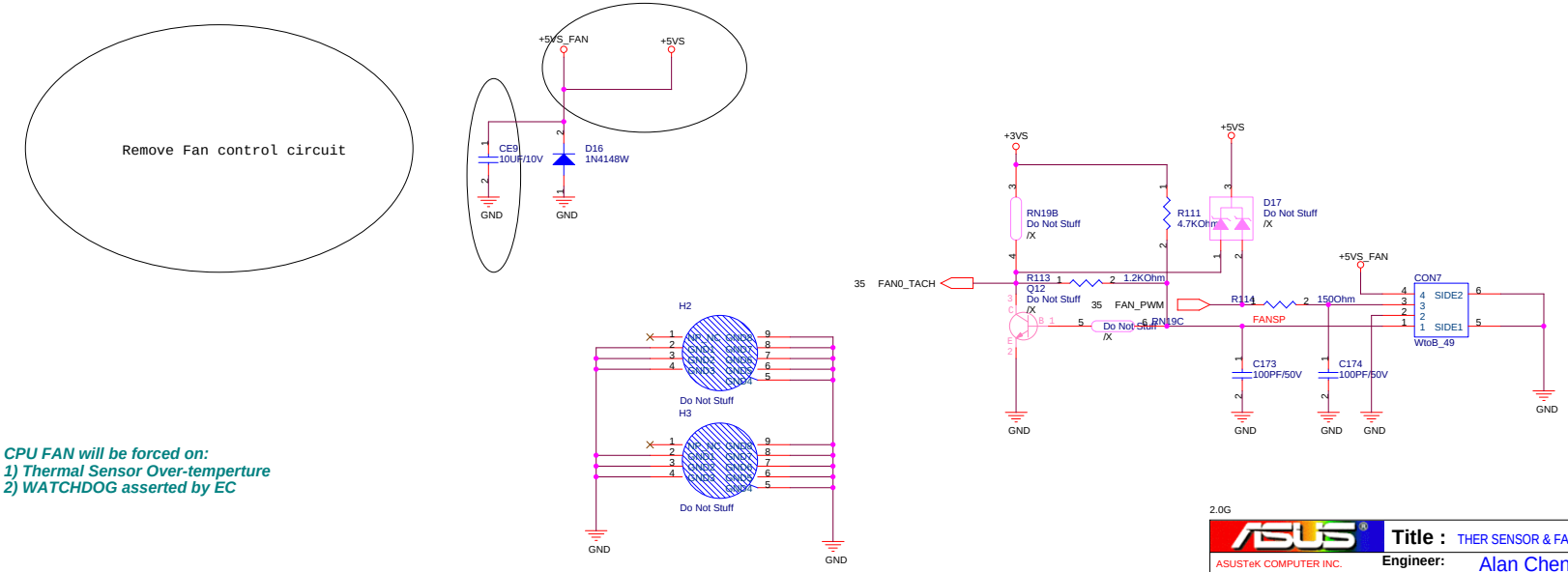


Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power

DC FAN Control



CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC

2.0G

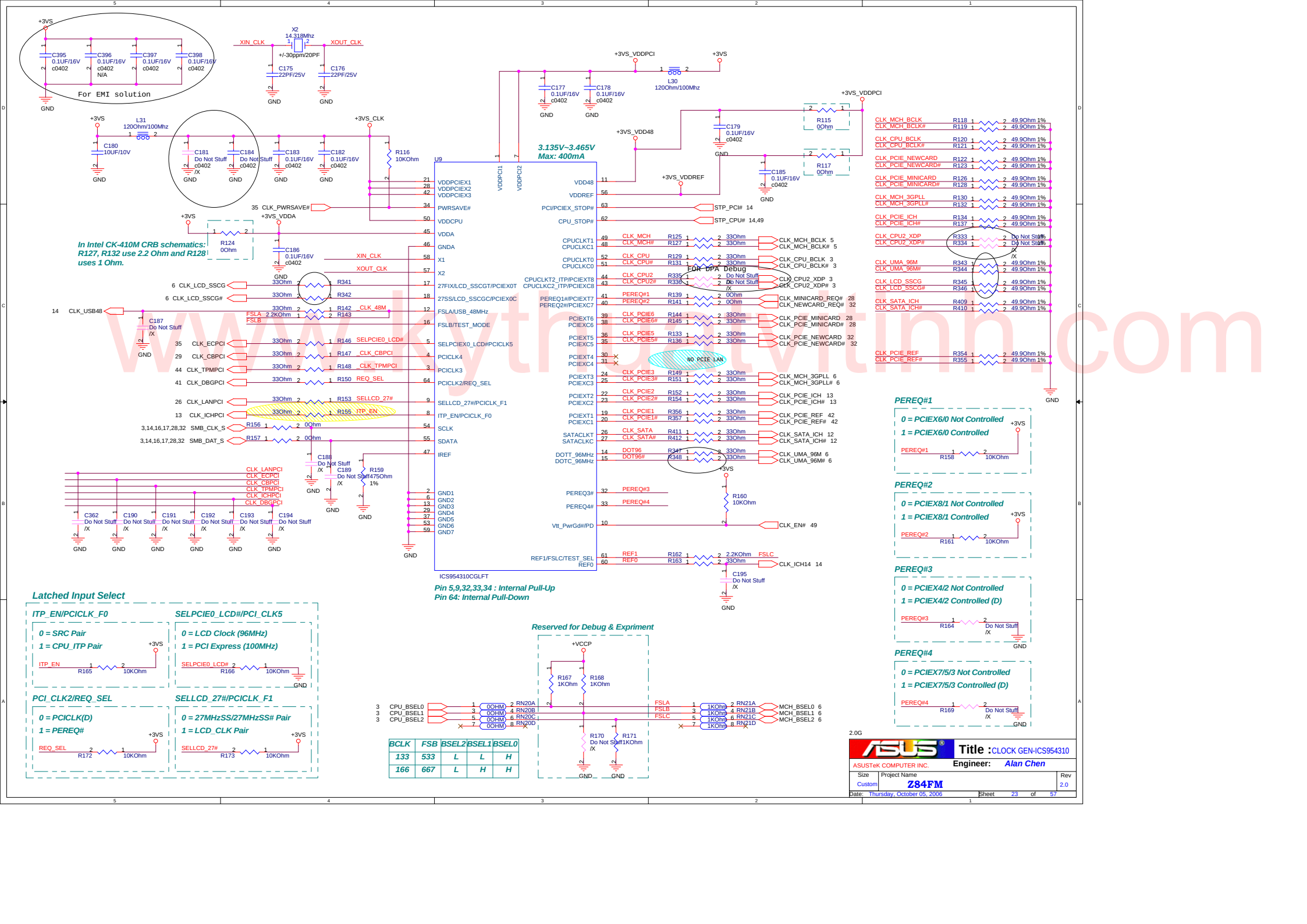
ASUSTeK COMPUTER INC.

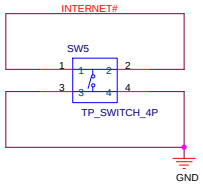
Title : THER SENSOR & FAN

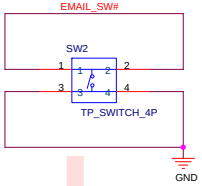
Engineer: Alan Chen

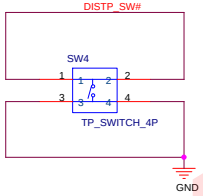
Size	Project Name	Rev
Custom	Z84FM	2.0

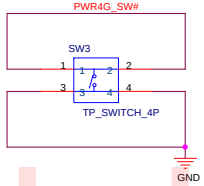
Date: Thursday, October 05, 2006 Sheet 22 of 57

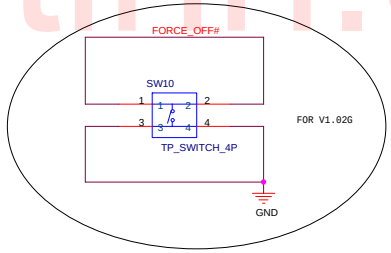




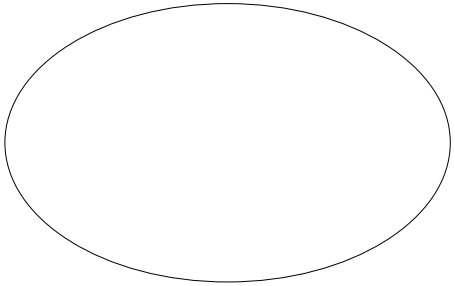


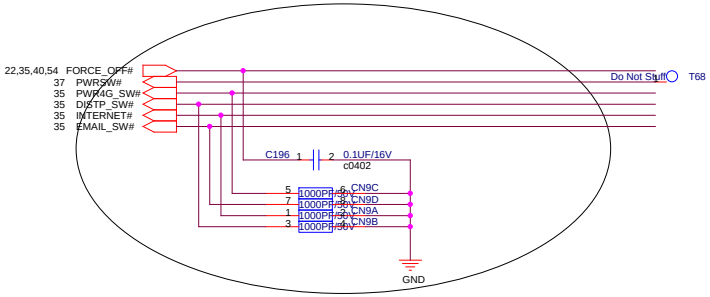


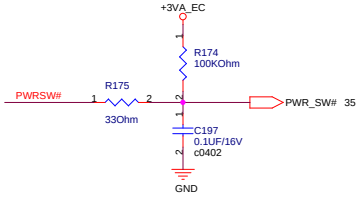




SHUT_DOWN#







2.0G

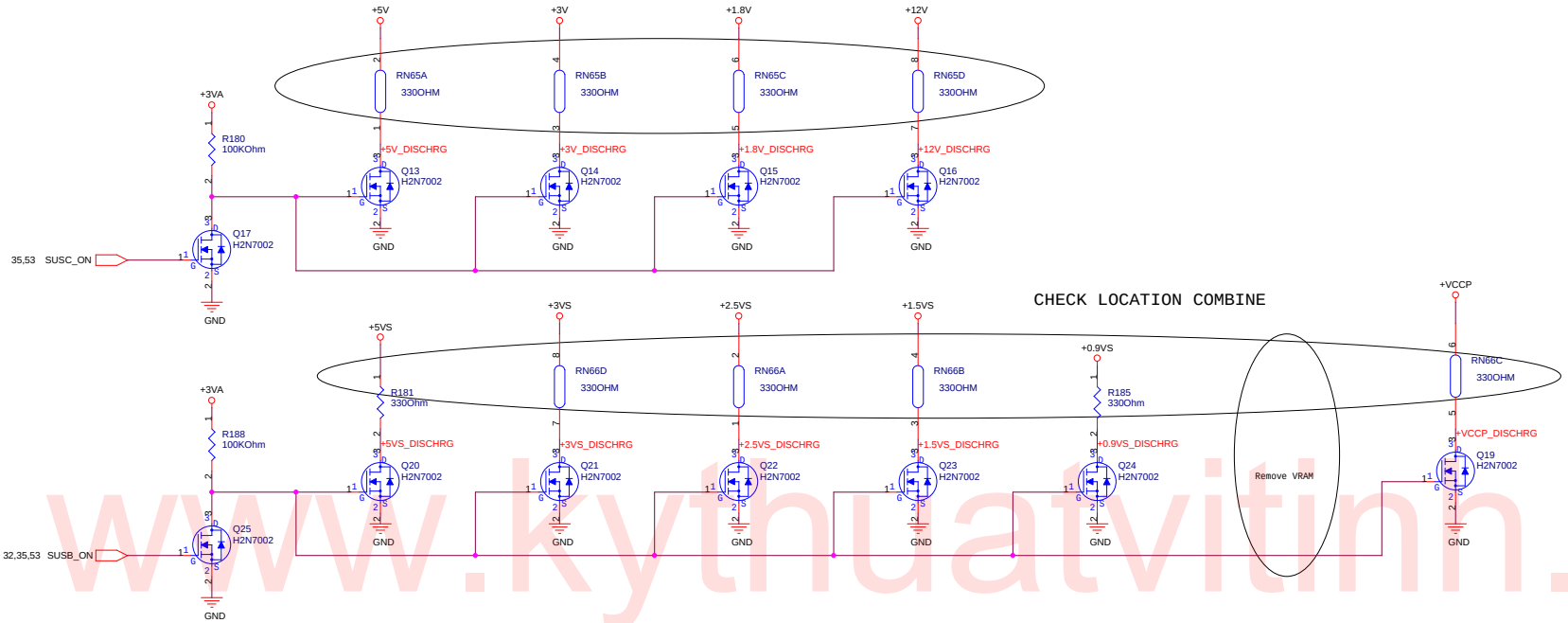
ASUSTeK COMPUTER INC

Title : Power on & Res Freq

Engineer: Alan Chen

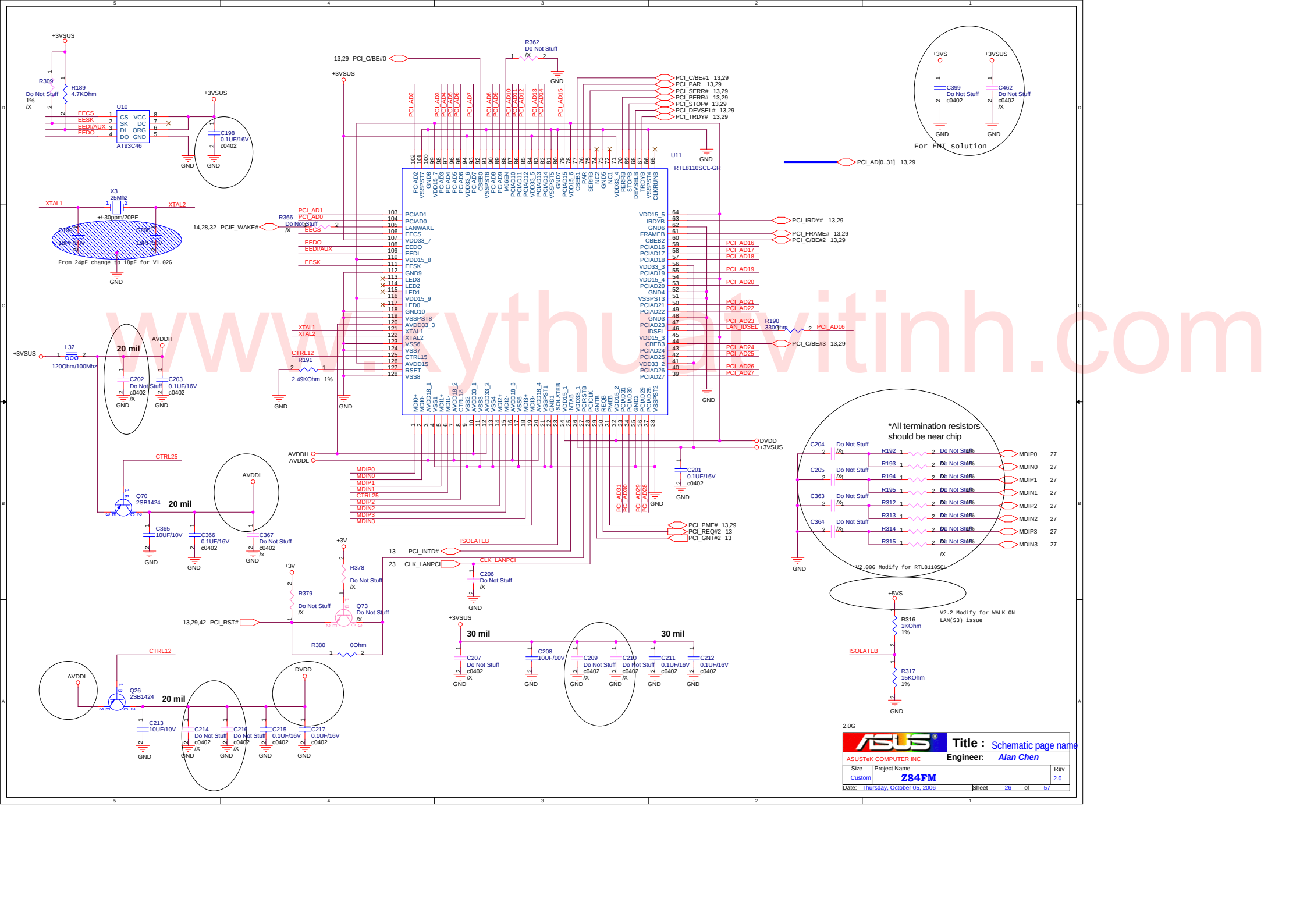
Size	Project Name	Rev
Custom	Z84FM	2.0

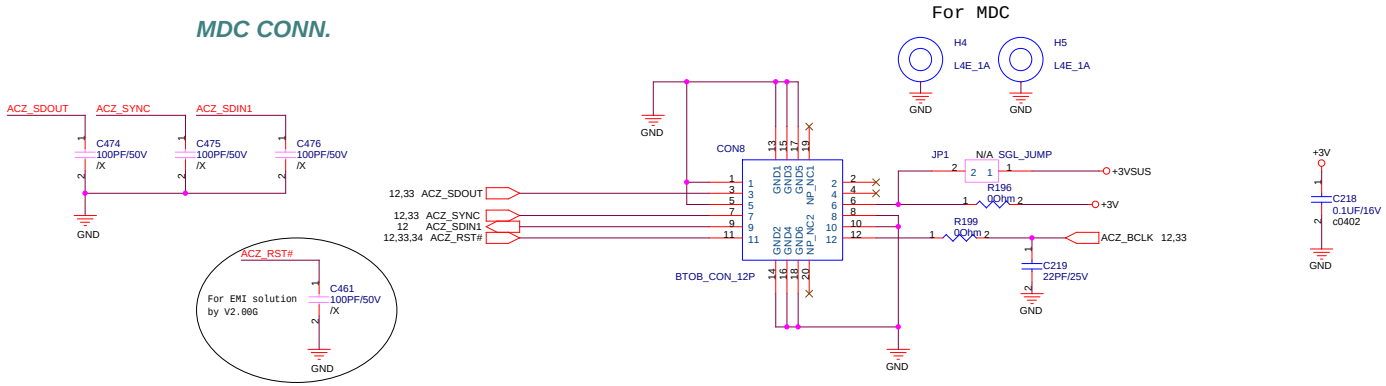
Date: Thursday, October 05, 2006 Sheet 24 of 57

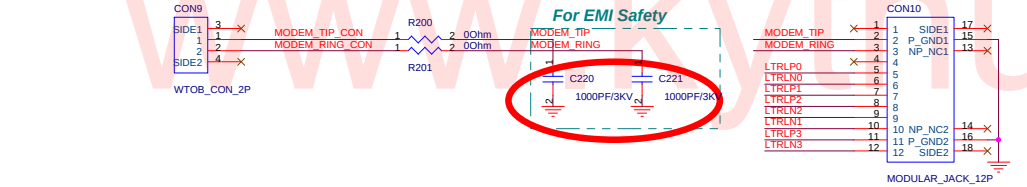


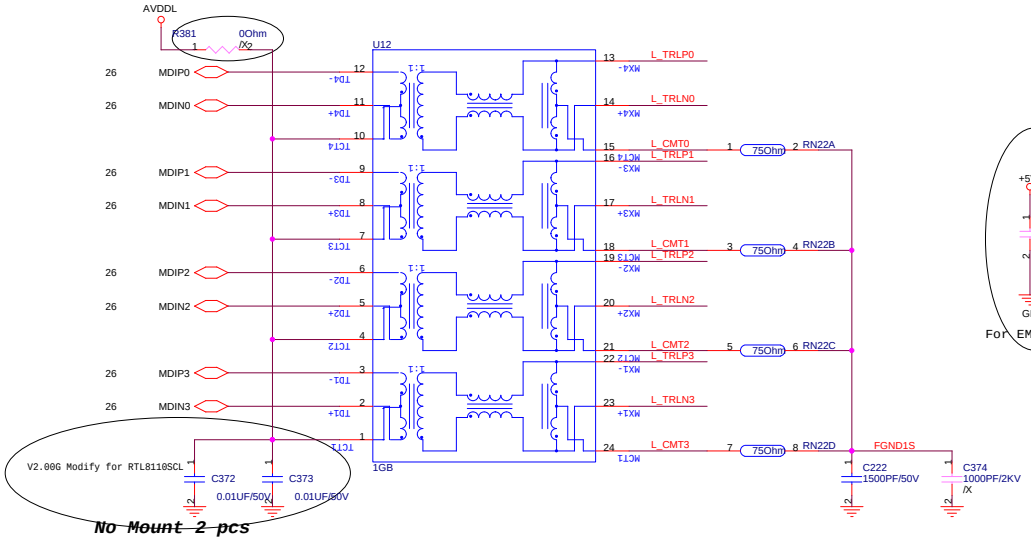
2.0G

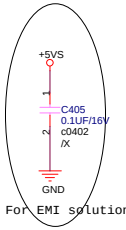
ASUSTeK COMPUTER INC. NB1	Title : DISCHARGE & EMI CAP	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Thursday, October 05, 2006	Sheet 25 of 57	

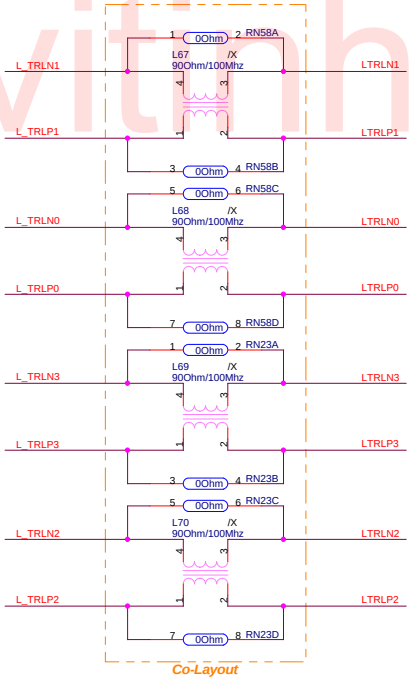












2.0G

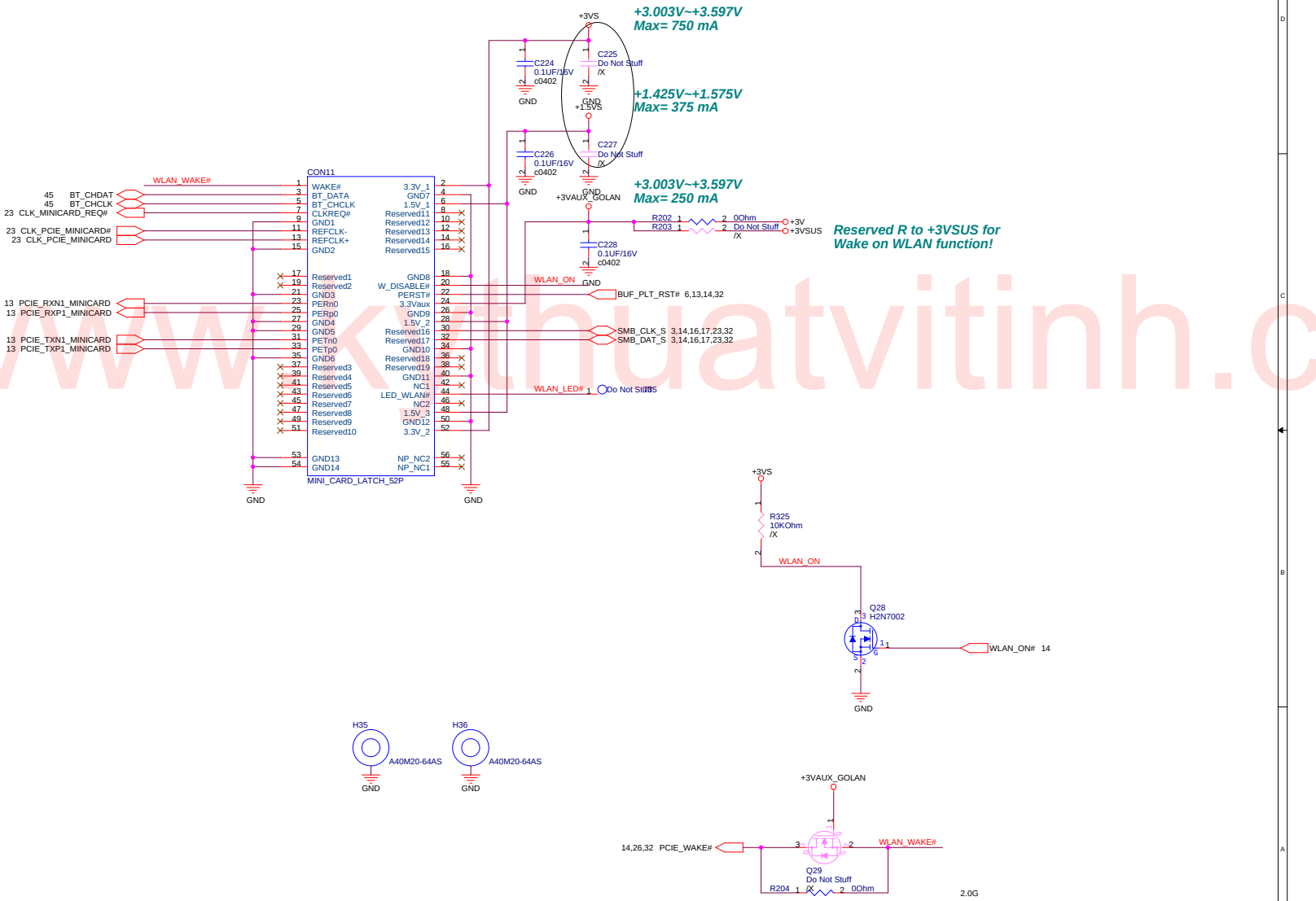
ASUSTeK COMPUTER INC.

Title : RJ45&RJ11

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 27 of 57



2.0G

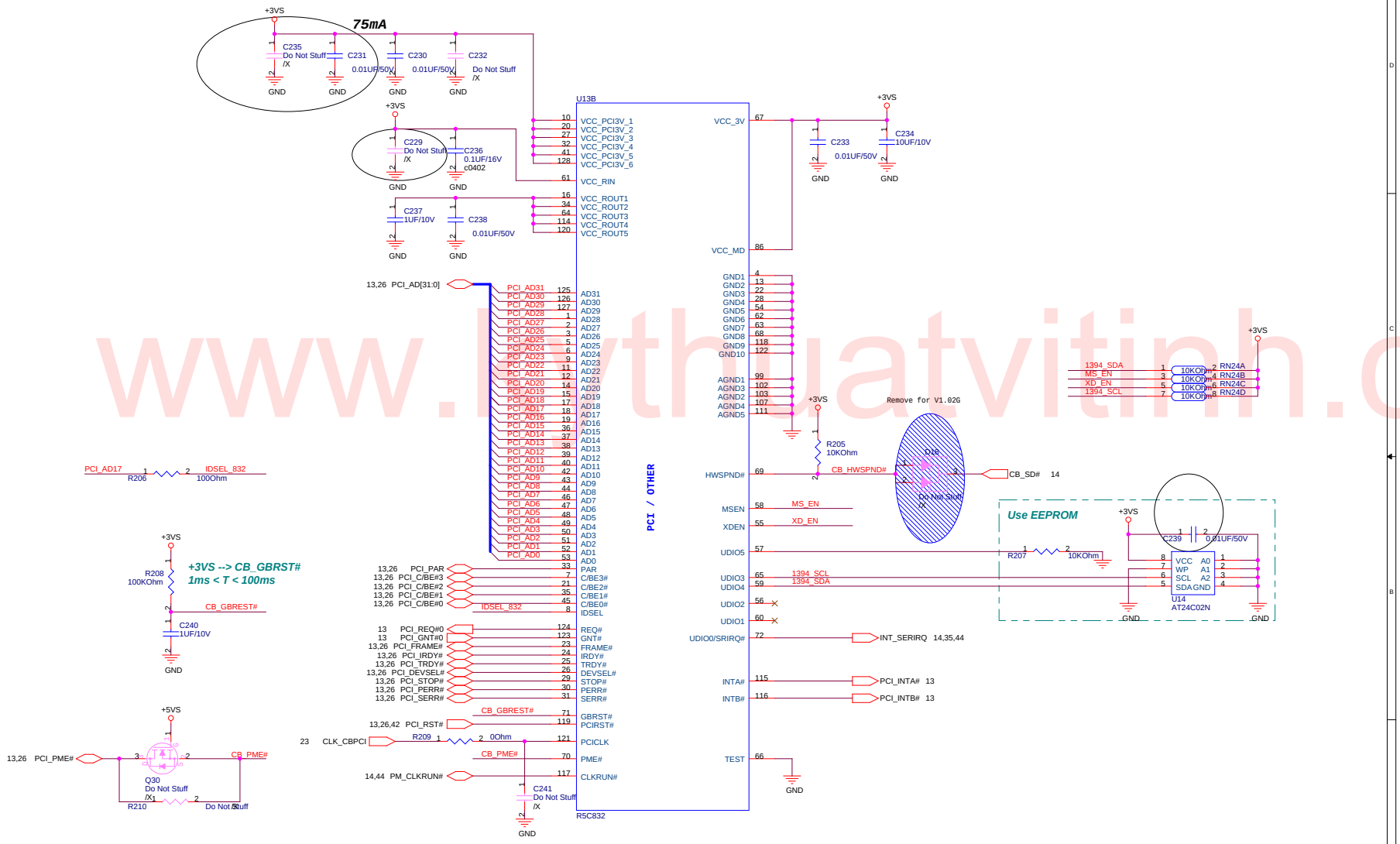
ASUSTeK COMPUTER INC.

Title : MINICARD

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 28 of 57



2.0G

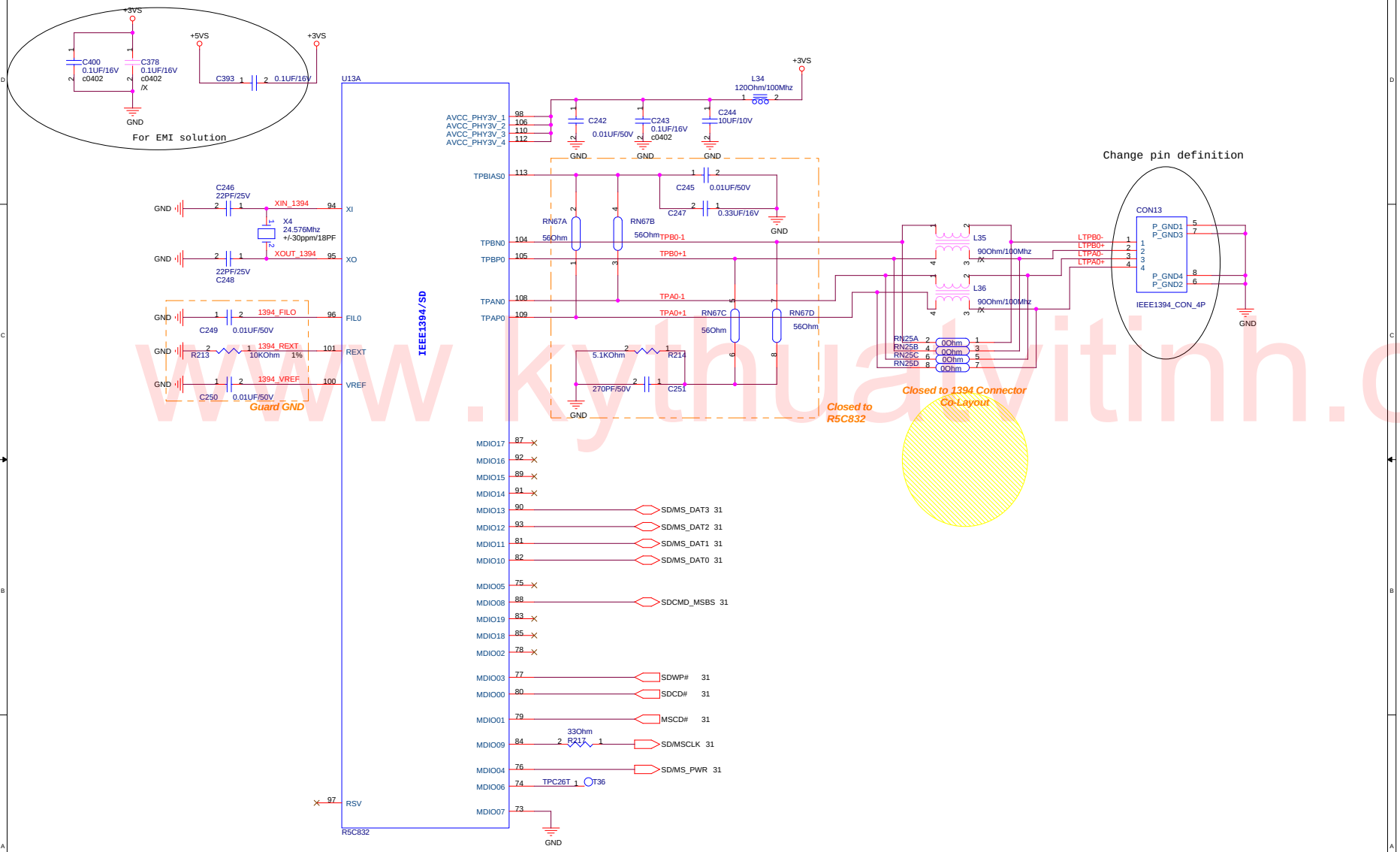
ASUSTeK COMPUTER INC. MB6

Title : CARD1394-R5C832(1)

Engineer: ALAN Chen

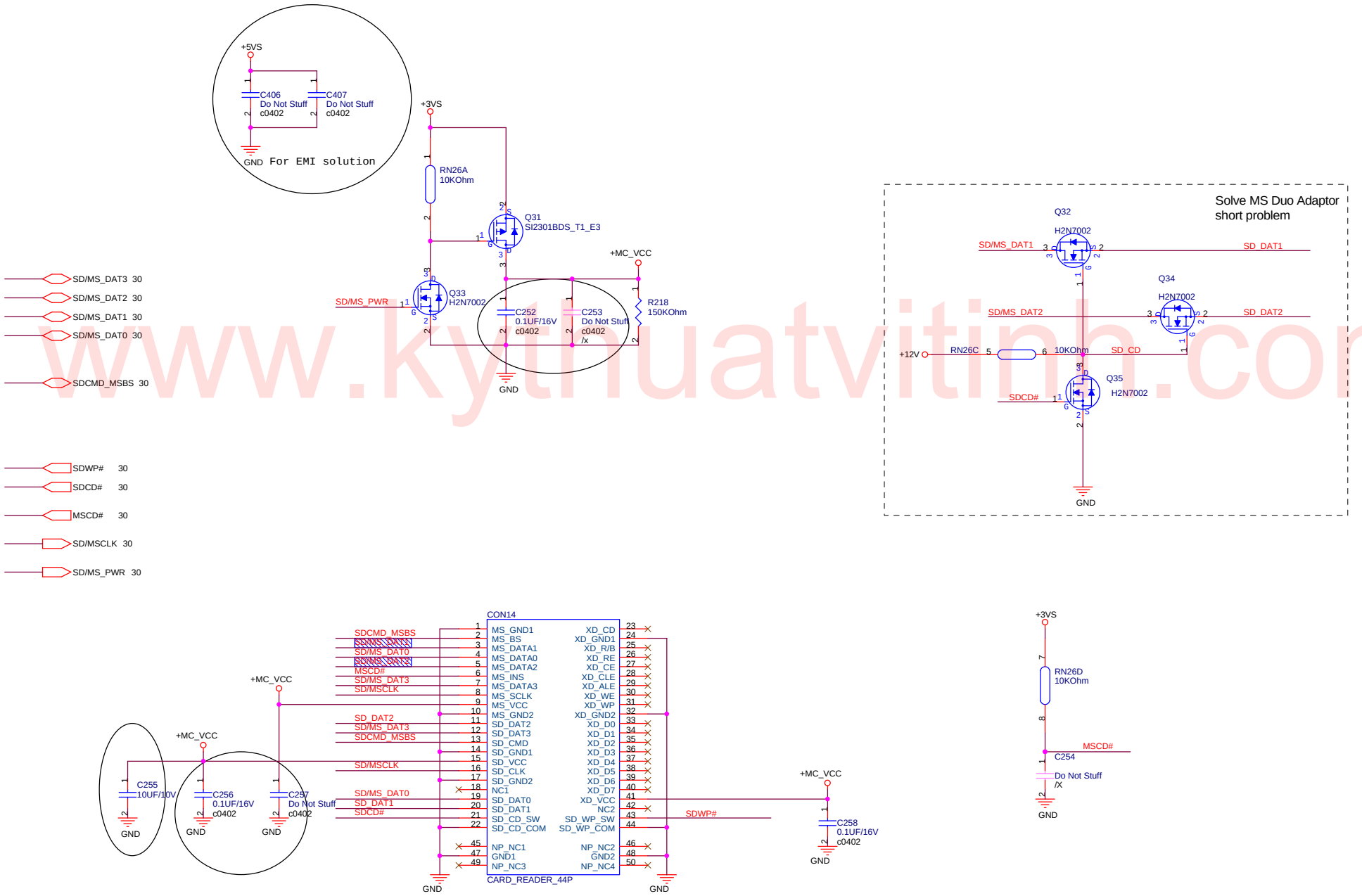
Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 29 of 57



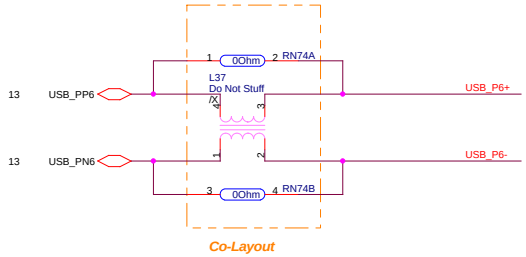
2.0G

ASUSTeK COMPUTER INC. MB6	Title : CARD1394-R5C832(2)	
	Engineer: ALAN Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Thursday, October 05, 2006	Sheet 30 of 57	

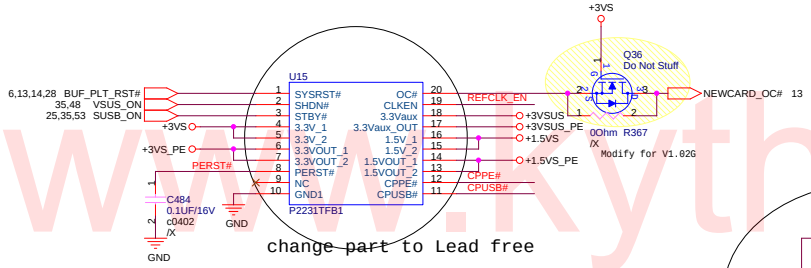


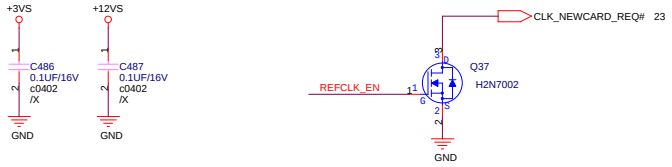
2.0G

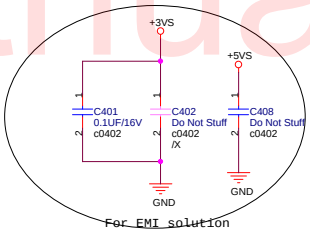
ASUSTeK COMPUTER INC	Title : 4 in 1 CARD READER	
	Engineer: ALAN CHEN	
Size: A3	Project Name: Z84FM	Rev: 2.0
Date: Thursday, October 05, 2006	Sheet 31 of 57	



Co-Layout

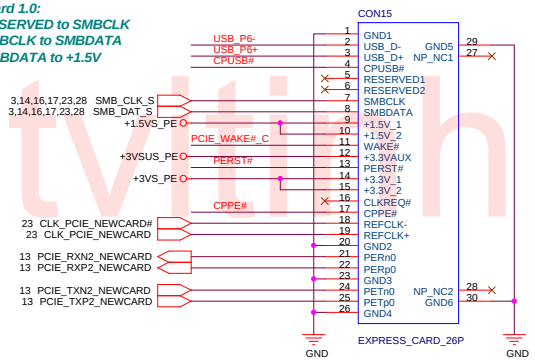




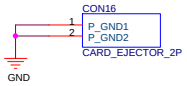


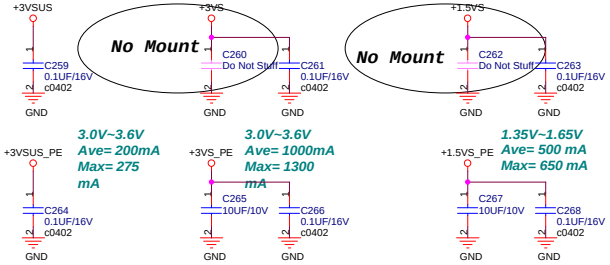
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

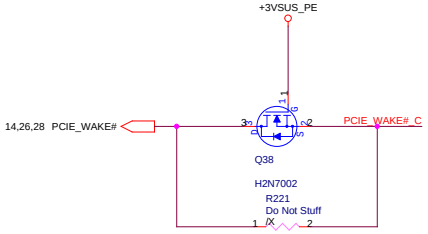
NewCard Header



NewCard Ejecter







2.0G

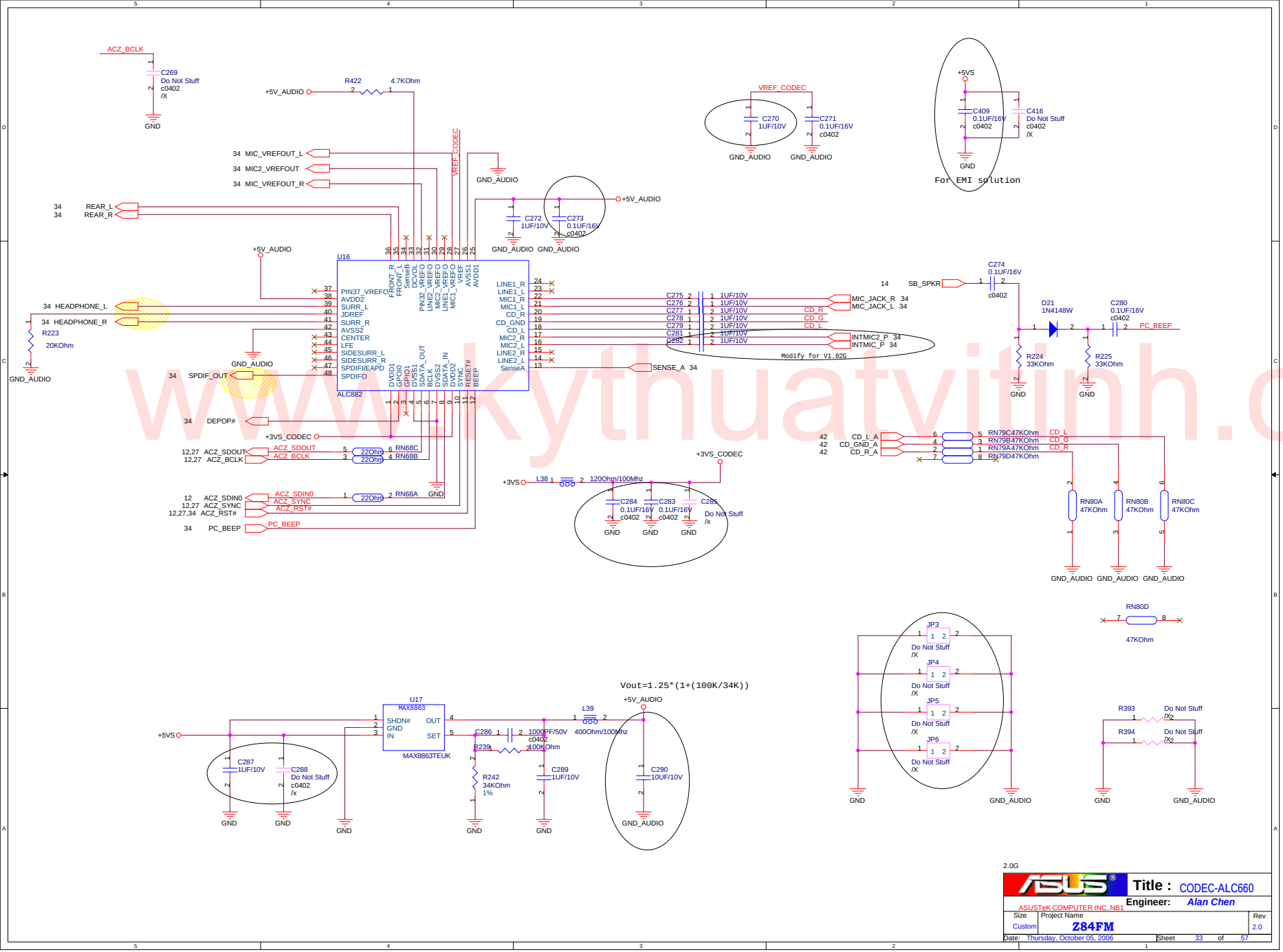
ASUSTeK COMPUTER INC. NB1

Title : NEWCARD

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 32 of 57



2.0G

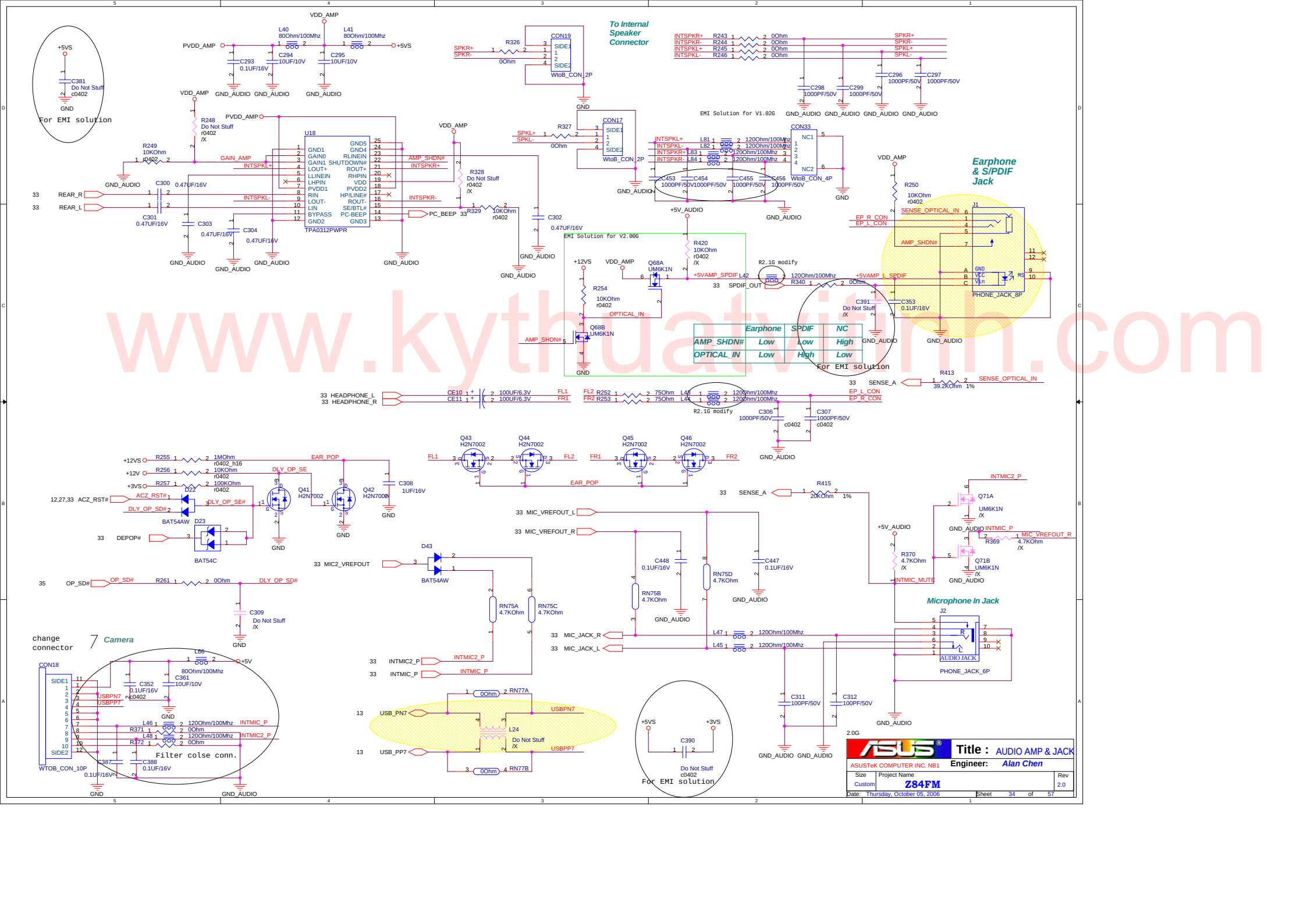
ASUSTeK COMPUTER INC. NB1

Title : CODEC-ALC660

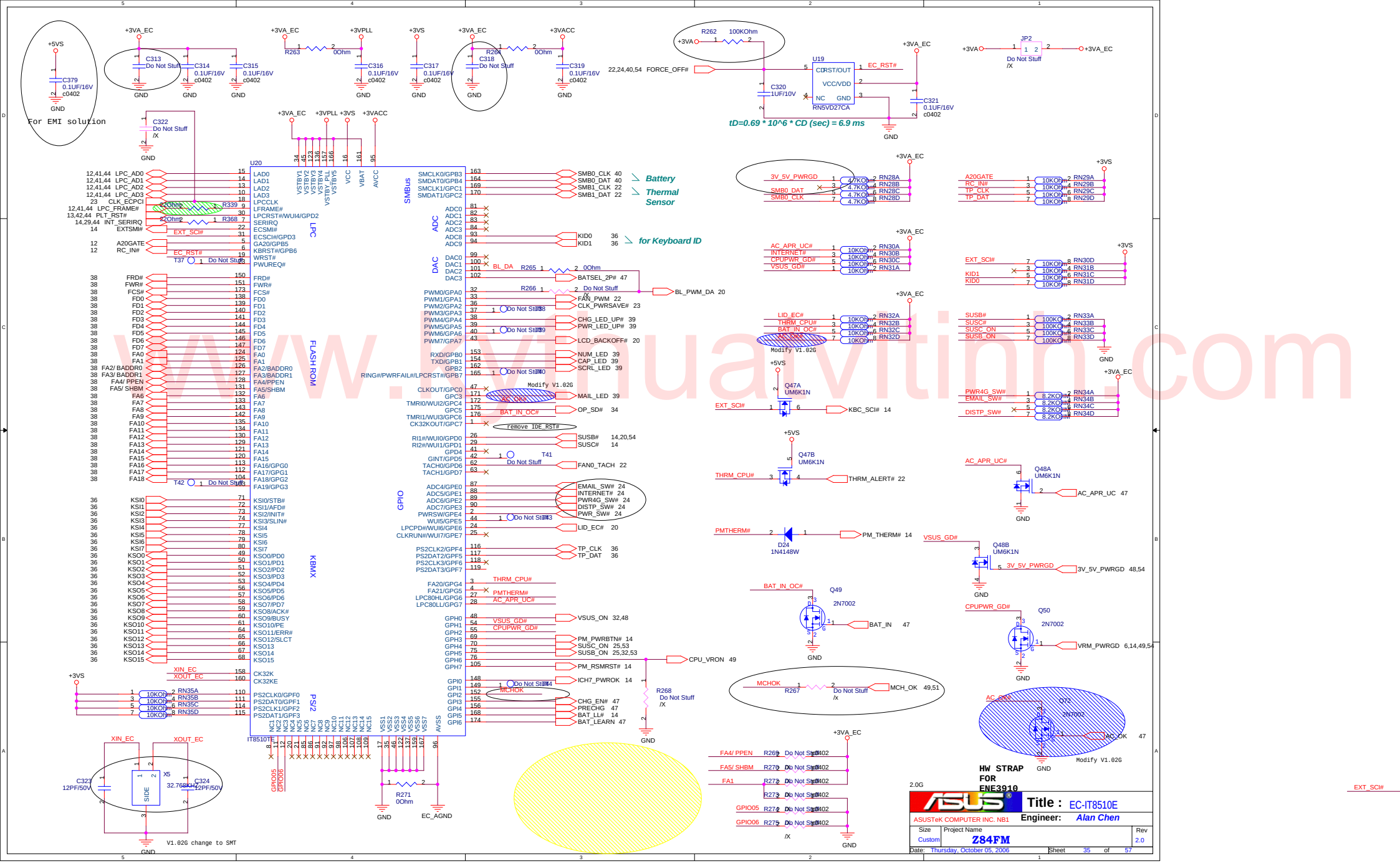
Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

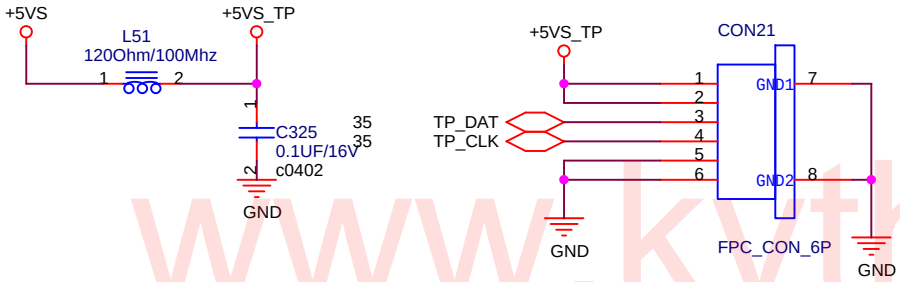
Date: Thursday, October 05, 2006 Sheet 33 of 57



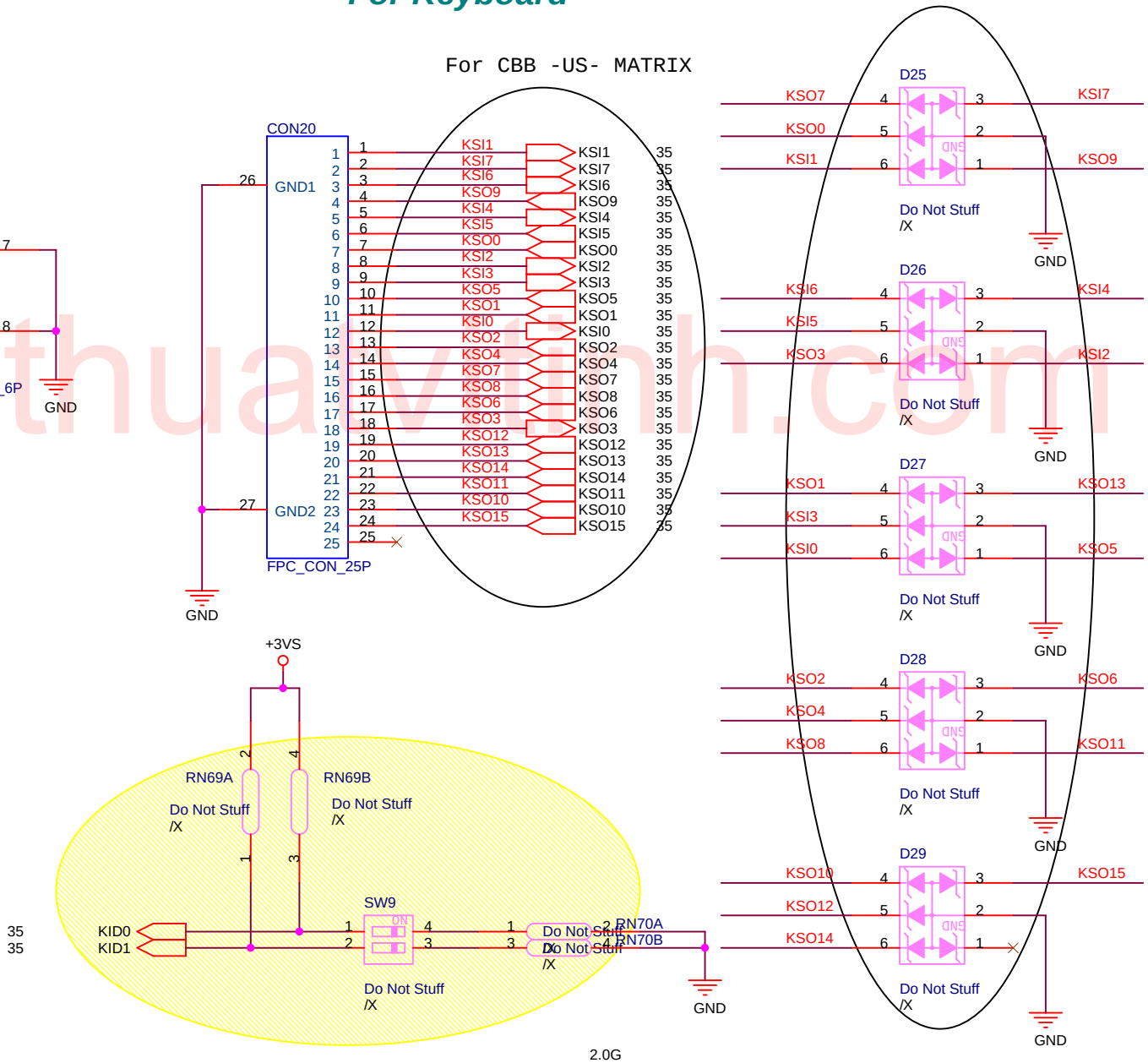
	Earphone	SPDIF	NC
AMP_SHDN#	Low	Low	High
OPTICAL_IN	Low	High	Low



For Touch-Pad

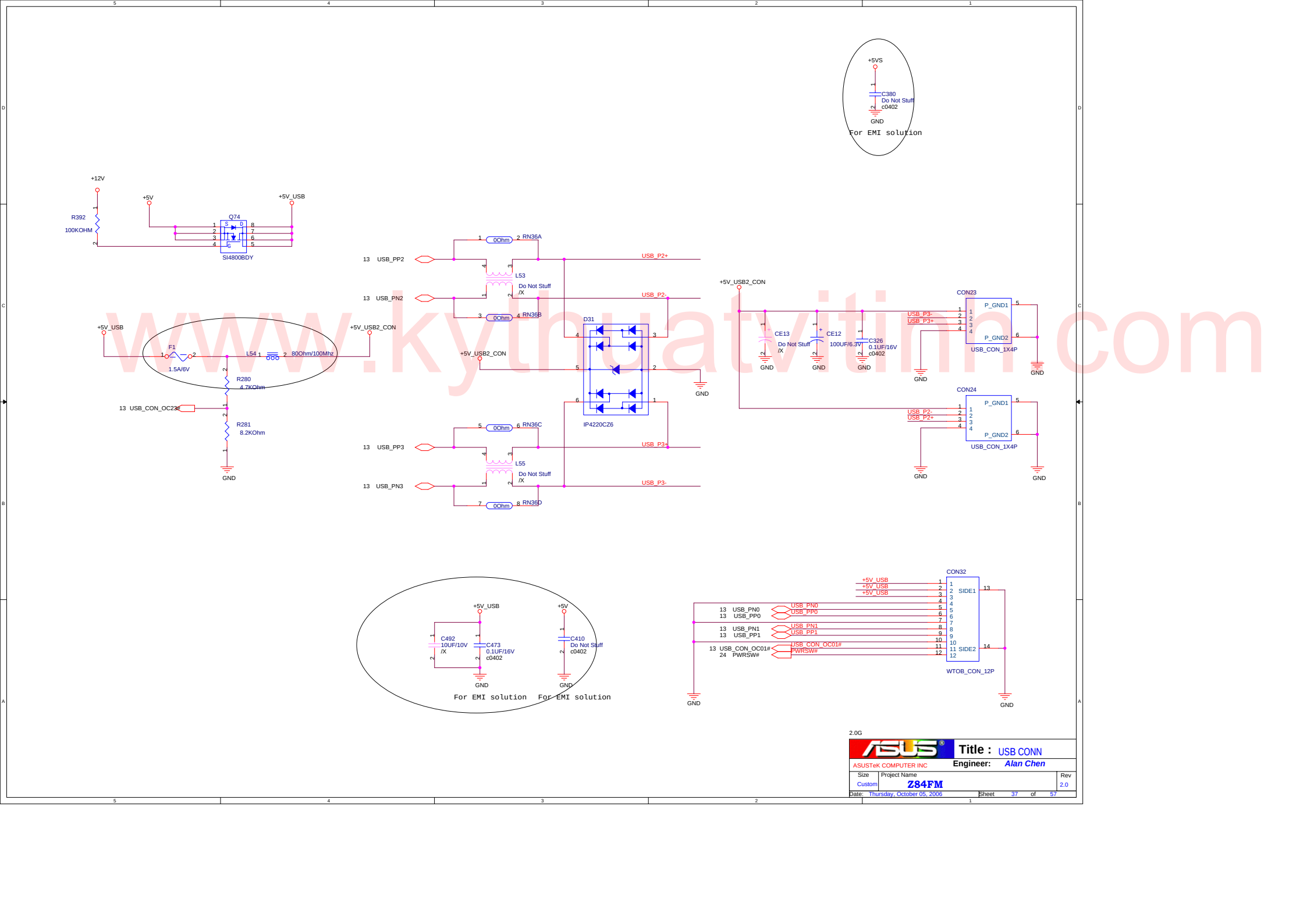


For Keyboard



2.0G

ASUSTeK COMPUTER INC. MB6	Title : Touch Pad & KB	
	Engineer: ALAN CHEN	
Size: A4	Project Name: Z84FM	Rev: 2.0
Date: Thursday, October 05, 2006	Sheet 36 of 57	



2.0G

ASUSTeK COMPUTER INC

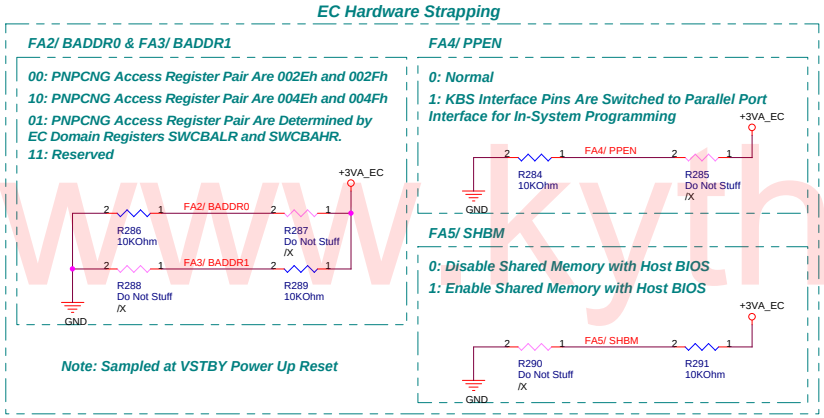
Title : USB CONN

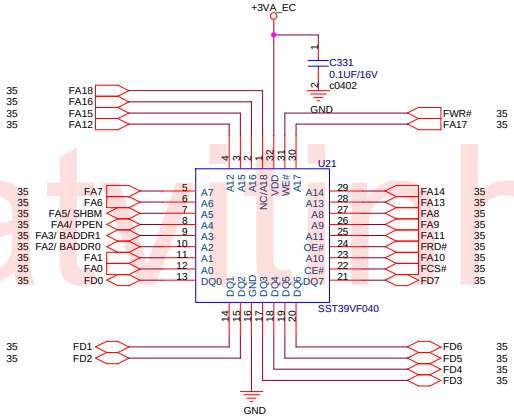
Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 37 of 57

ISA ROM





2.0G

ASUSTeK COMPUTER INC. NB1

Title : ISA ROM

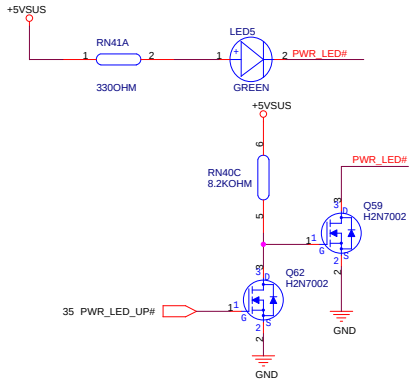
Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

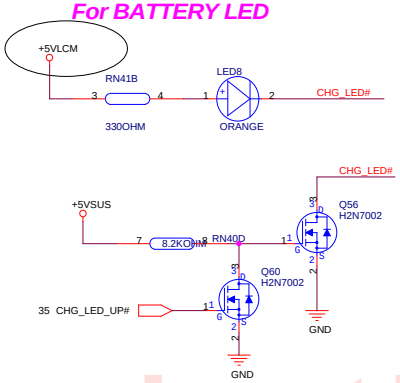
Date: Thursday, October 05, 2006 Sheet 38 of 57

For LED

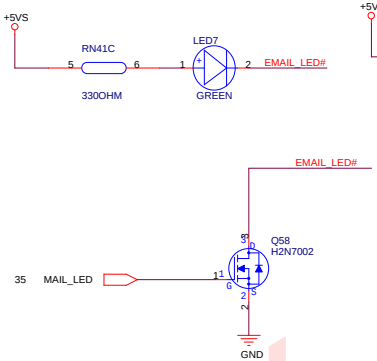
For POWER LED



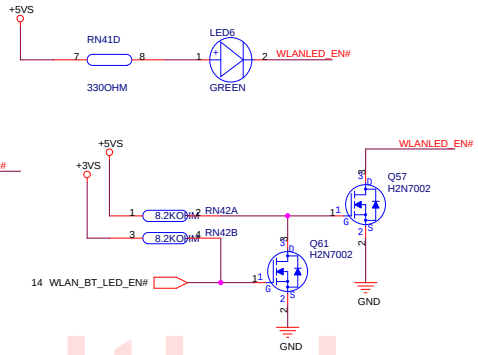
For BATTERY LED



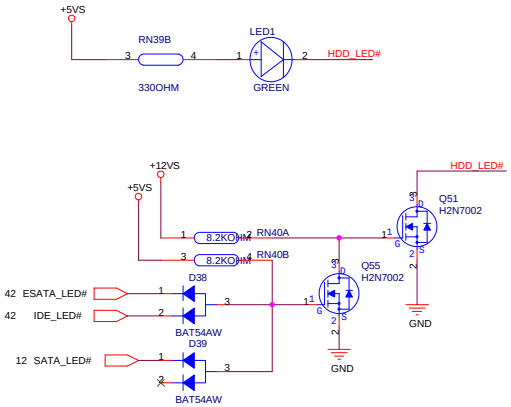
for EMIAL LED



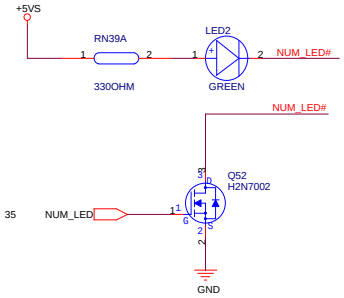
For WireLess LED



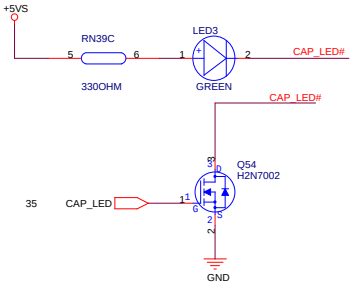
For ESATA/IDE LED



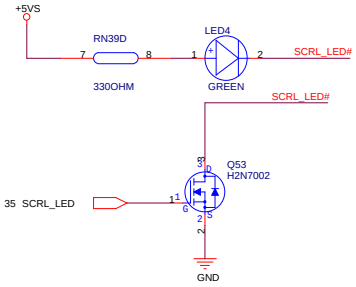
for Num Lock

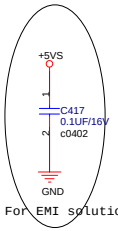


for Cap. Lock



for Scroll Lock



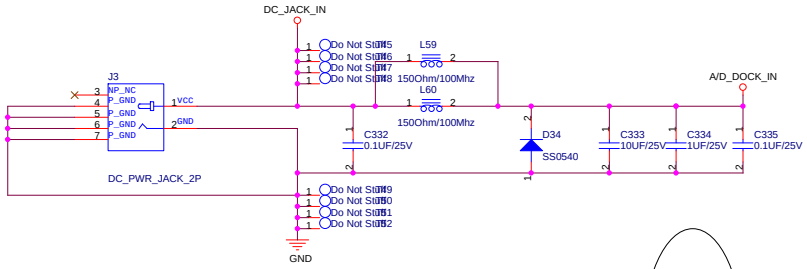


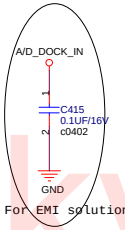
For EMI solution

2.0G

ASUSTeK COMPUTER INC	Title : LED	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Thursday, October 05, 2006	Sheet 39 of 57	

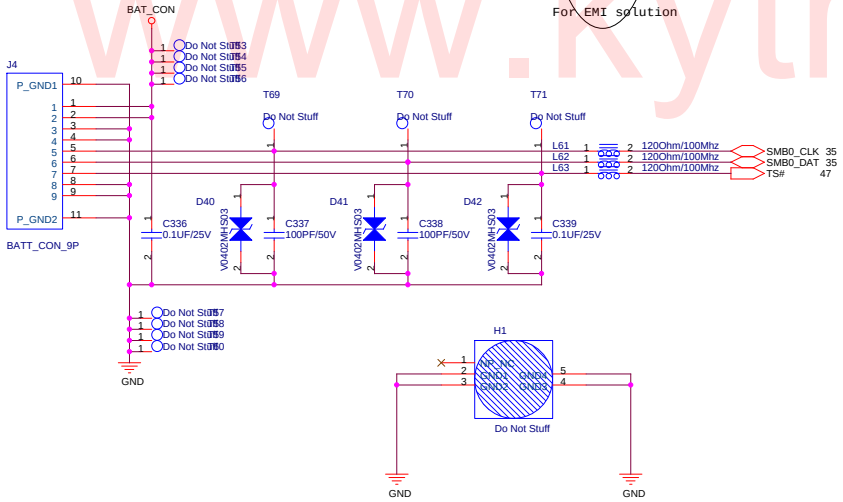
DC IN



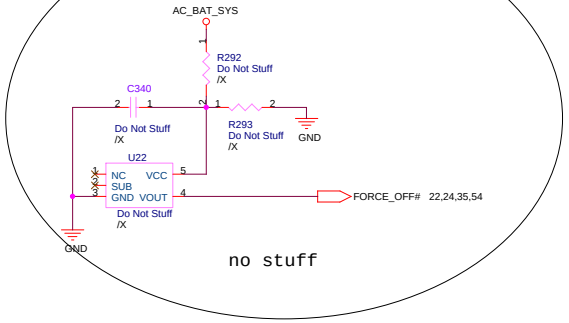


remove AC DC detect; no need

BAT IN



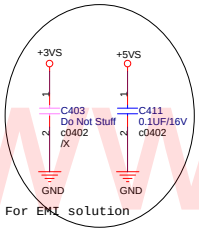
Without Battery & Pull out Adapter



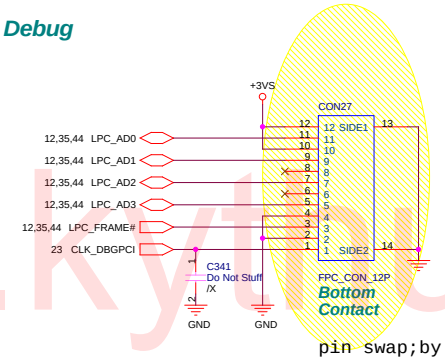
no stuff

2.0G

ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Thursday, October 05, 2006	Sheet 40 of 57	



For Debug



pin swap;by F3J

2.0G

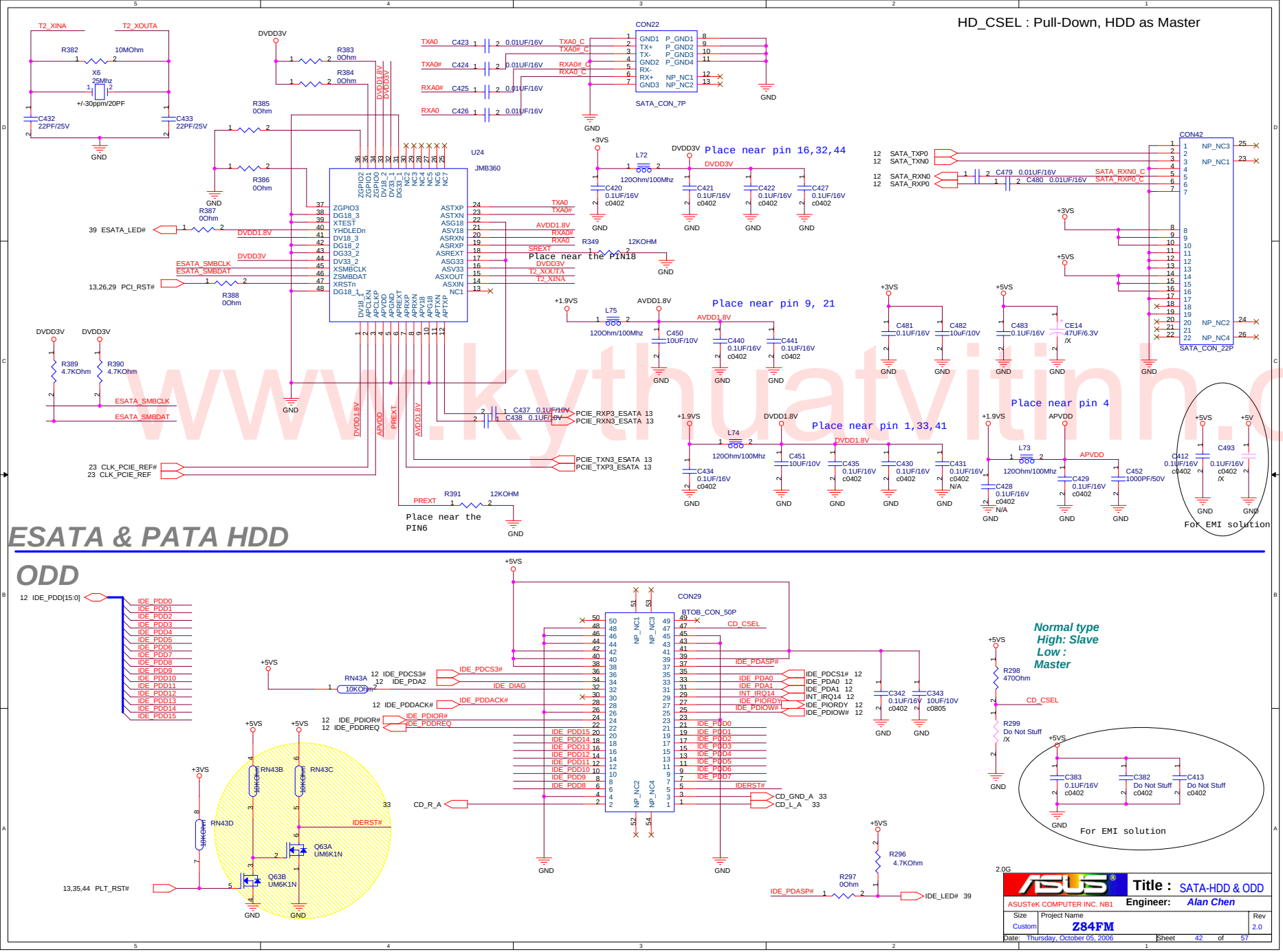
ASUSTeK COMPUTER INC

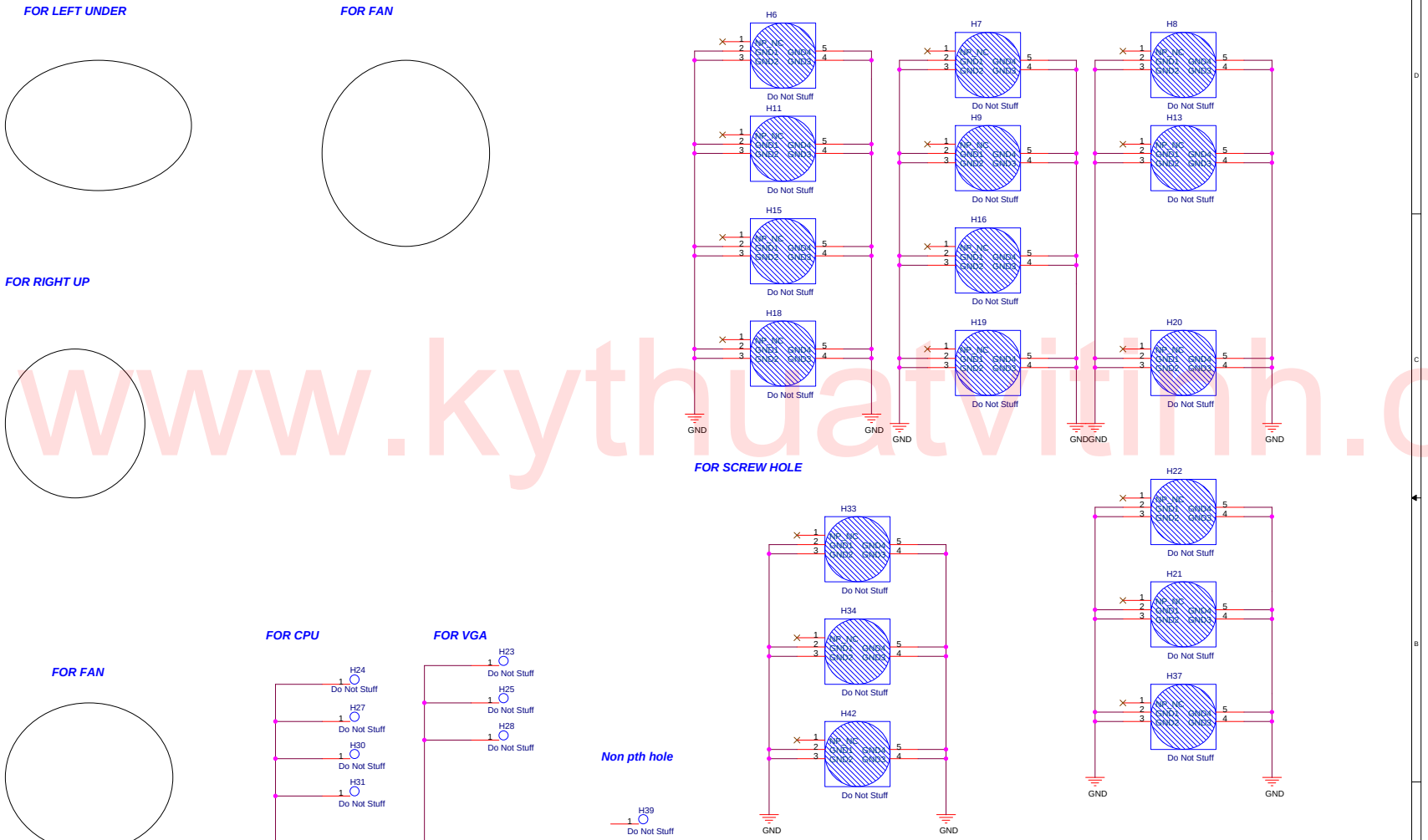
Title : Debug CONN.

Engineer: *Alan Chen*

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 41 of 57





2.0G

ASUSTeK COMPUTER INC

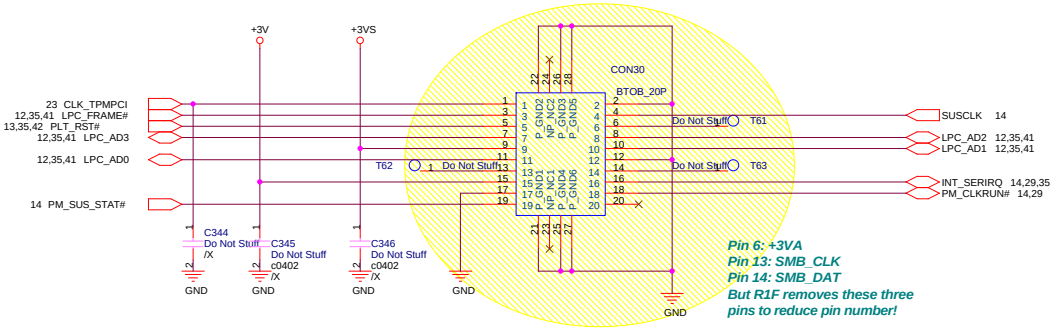
Title : SREW HOLE

Engineer: ALan Chen

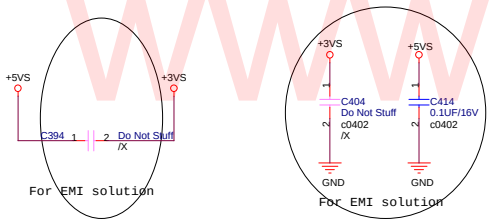
Size	Project Name	Rev
Custom	Z84FM	2.0

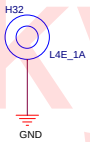
Date: Thursday, October 05, 2006 Sheet 43 of 57

For TPM Module



Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

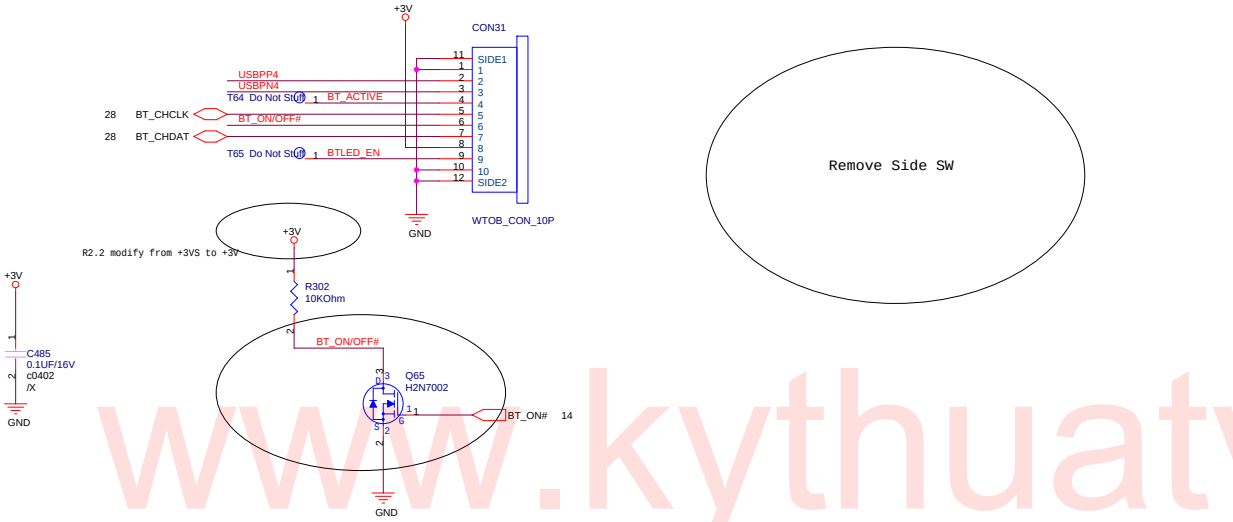




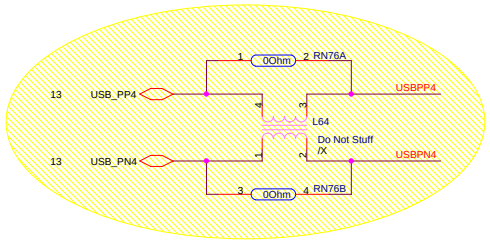
2.0G

ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: *Alan Chen*	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Thursday, October 05, 2006	Sheet 44 of 57	

For Bluetooth

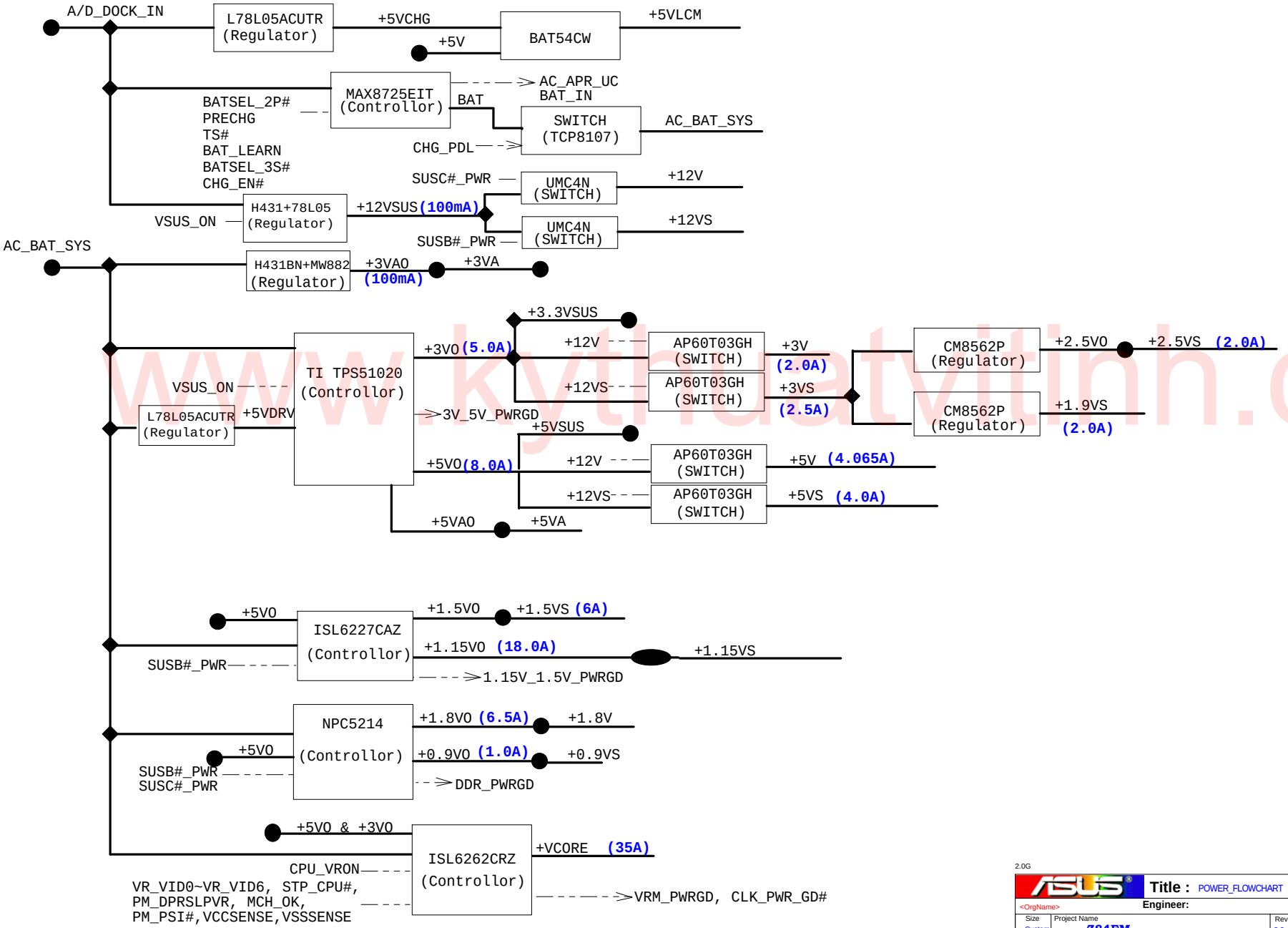


Remove Side SW



2.0G

ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Thursday, October 05, 2006	Sheet 45 of 57	



2.0G

Title : POWER_FLOWCHART

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 46 of 57

AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active

Setting the Adapter Input Current Limit

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]

VCLS= 2.865V

Adaptor Max. Current :

PR5718=20K PR5714 = 178K; Ilimit = 4.5A; 90W

PR5718=27K PR5714 = 47K; Ilimit = 3.175A; 60W

Setting the Charge Voltage

Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }

VCTL= 1.588V => Vbatt = 4.2V

Setting the Charge Current

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]

Rsense(CHG)= 15m Ohm

Pre-Charging Mode :

Precharging current = 148 ~ 152mA

VictI = 0.107V ~ 0.109V

Battery Cell Selection :

BATSEL_2P# = 1, 3 Cells; VictI = 2.084V

=> Icharge = 1.6933A

BATSEL_2P# = 0, 6 or 9 Cells; VictI = 2.111V

=> Icharge = 2.9329A

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells

2.0 > Vmode > 1.6V (floating) ----> 3 Cells

0.8 > Vmode (trie to GND) ----> Learning mode

VICTL< 0.8V or DCIN < 7V -->Charger Disable

MAX8725_REF : 4.2235V

MAX8725_LDO : 5.4V

POWER PATH & BAT_LEARN

Battery Voltage

Rev2.0 power update

Rev1.2 power update

Rev1.1 power update

AC_IN = 1, Adaptor is present

AC_IN = 0, Adaptor is absent

BATSEL_2P# = 1, 3 Cells

BATSEL_2P# = 0, 6 or 9 Cells

PRECHG = 1, Pre-Charging Mode

Charging Current = 156mA

CHG_EN# = 1, Charger Disabled

CHG_EN# = 0, Charger Enabled

AC_OK = 1, Adaptor is present

AC_OK = 0, Adaptor is absent

BAT_LEARN = 1, Battery discharges

BAT_LEARN = 0, charging voltage with 3 time VCTL (3 Cells)

AC_APR_UC = 1, Adaptor is present

AC_APR_UC = 0, Adaptor is absent

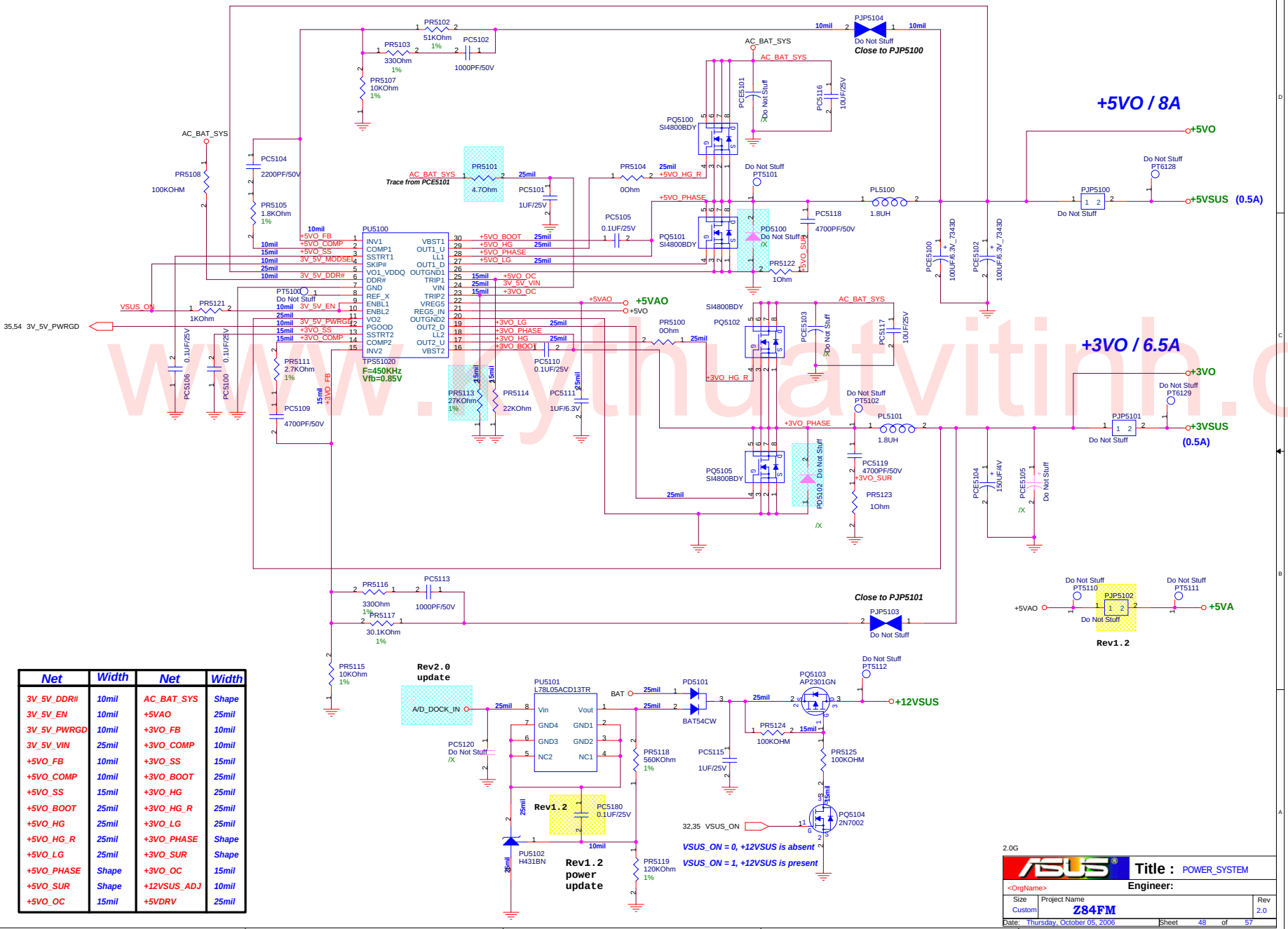
BAT_IN_OC# = 1; Battery absence

BAT_IN_OC# = 0; Battery Plug-in

TS# = 1; Battery absence

TS# = 0; Battery Plug-in

Title : POWER_CHARGER		
<OrgName>	Engineer:	
Size: C	Project Name: Z84FM	Rev: 2.0
Date: Thursday, October 05, 2006	Sheet 47 of 57	



Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5VO_FB	10mil	+3VO_SS	15mil
+5VO_COMP	10mil	+3VO_BOOT	25mil
+5VO_SS	15mil	+3VO_HG	25mil
+5VO_BOOT	25mil	+3VO_HG_R	25mil
+5VO_HG	25mil	+3VO_LG	25mil
+5VO_HG_R	25mil	+3VO_PHASE	Shape
+5VO_LG	25mil	+3VO_OC	Shape
+5VO_PHASE	Shape	+3VO_SUR	15mil
+5VO_SUR	Shape	+12VSUS_ADJ	10mil
+5VO_OC	15mil	+5VDRV	25mil

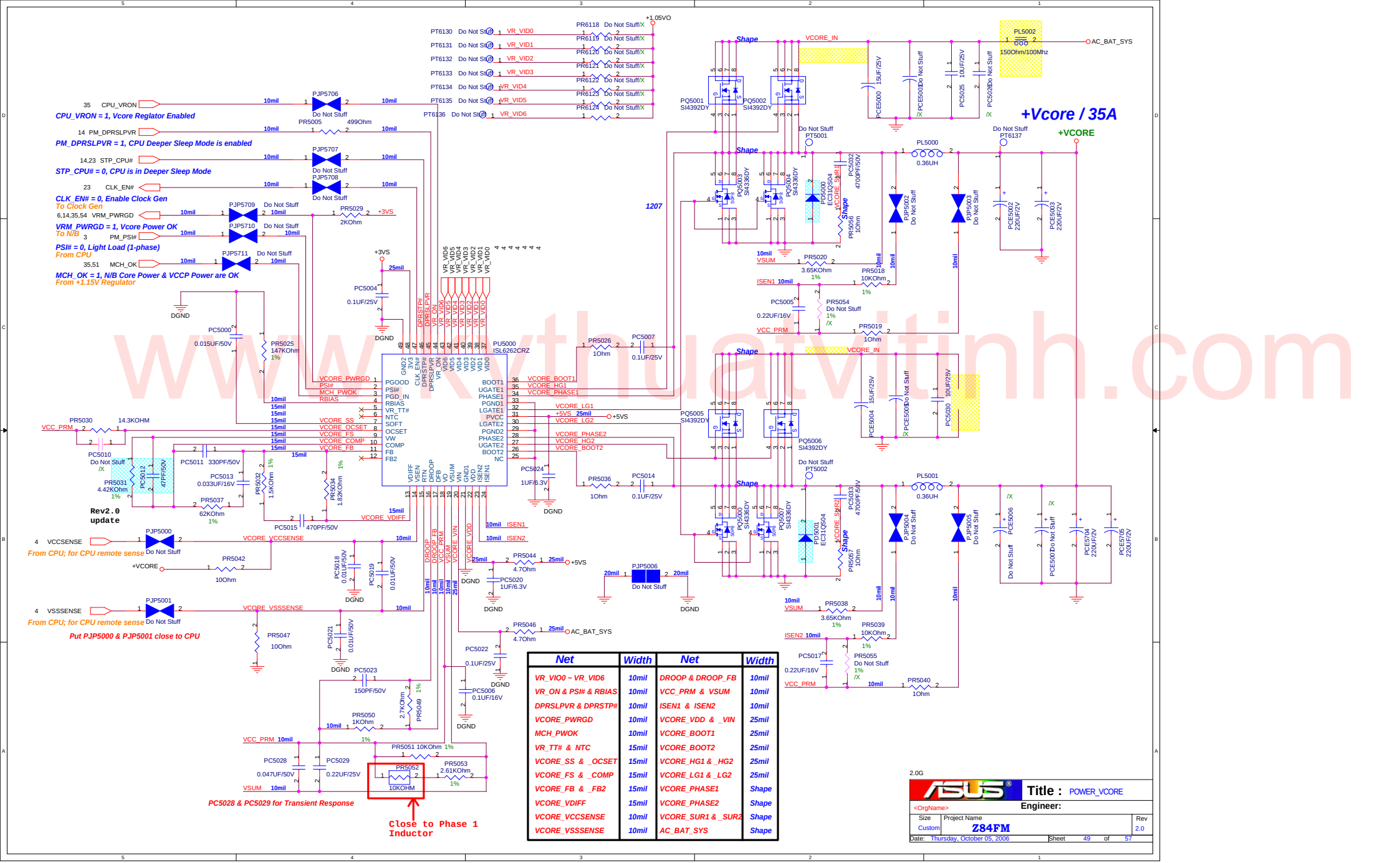
2.0G

Title : POWER_SYSTEM

<OrgName> Engineer:

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 48 of 57



Net	Width	Net	Width
VR_VID0 ~ VR_VID6	10mil	DROOP & DROOP_FB	10mil
VR_ON & PSI# & RBIAS	10mil	VCC_PRM & VSUM	10mil
DPRSLPVR & DPRSTP#	10mil	ISEN1 & ISEN2	10mil
VCORE_PWRGD	10mil	VCORE_VDD & _VIN	25mil
MCH_PWOK	10mil	VCORE_BOOT1	25mil
VR_TT# & NTC	15mil	VCORE_BOOT2	25mil
VCORE_SS & _OCSET	15mil	VCORE_HG1 & _HG2	25mil
VCORE_FS & _COMP	15mil	VCORE_LG1 & _LG2	25mil
VCORE_FB & _FB2	15mil	VCORE_PHASE1	Shape
VCORE_VDIFF	15mil	VCORE_PHASE2	Shape
VCORE_VCCSENSE	10mil	VCORE_SUR1 & _SUR2	Shape
VCORE_VSSSENSE	10mil	AC_BAT_SYS	Shape

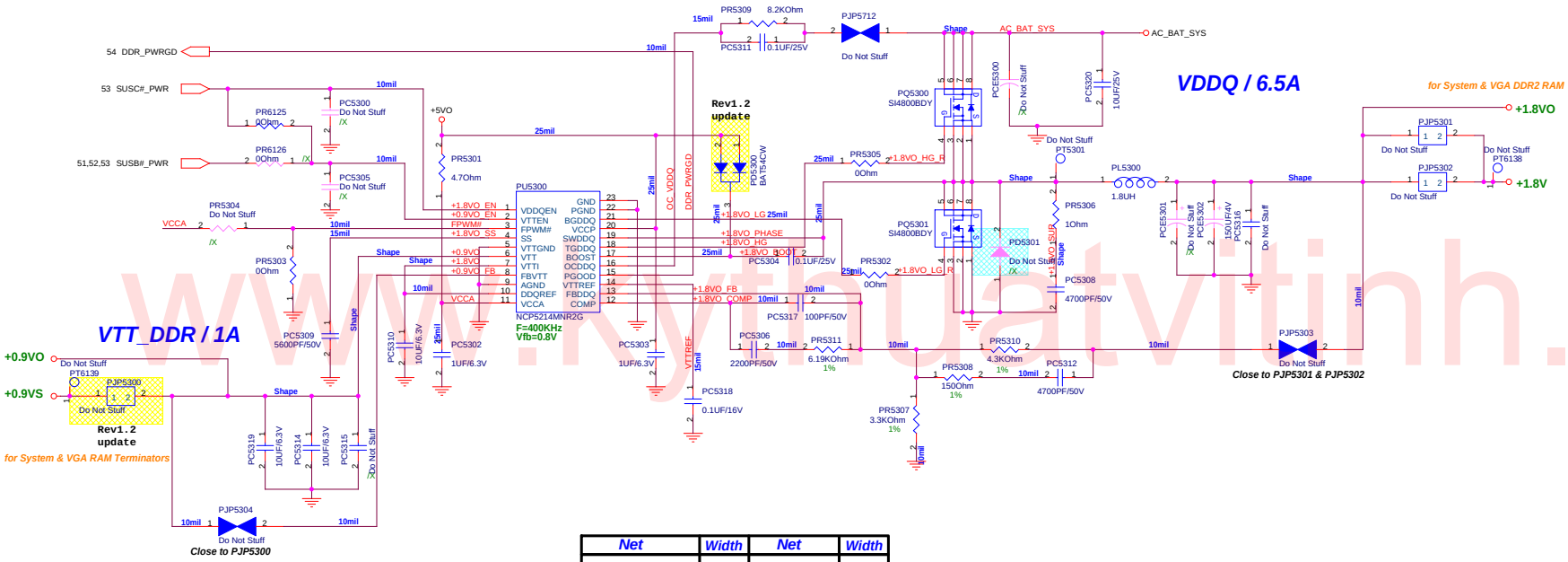
Title : POWER_VCORE

Engineer:

<OrgName>

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Thursday, October 05, 2006 Sheet 49 of 57



Net	Width	Net	Width
+1.8VO_EN	10mil	+1.8VO_BOOT	25mil
+1.8VO	Shape	+1.8VO_COMP	10mil
+0.9VO_EN	10mil	+1.8VO_HG_R	25mil
+0.9VO	Shape	+1.8VO_LG_R	25mil
+0.9VO_FB	10mil	+1.8VO_HG	25mil
+1.8VO --> DDQREF	10mil	+1.8VO_LG	25mil
VTTREF	15mil	+1.8VO_PHASE	Shape
FPWM#	10mil	+1.8VO_SUR	Shape
VCCA	10mil	+1.8VO_FB	10mil
DDR_PWRGD	10mil	+1.8VO_SS	15mil
OC_VDDQ	15mil	AC_BAT_SYS	Shape

2.0G

Title : POWER_I/O_DDR & VTT

<OrgName> Engineer:

Size	Project Name	Rev
Custom	Z84FM	2.0

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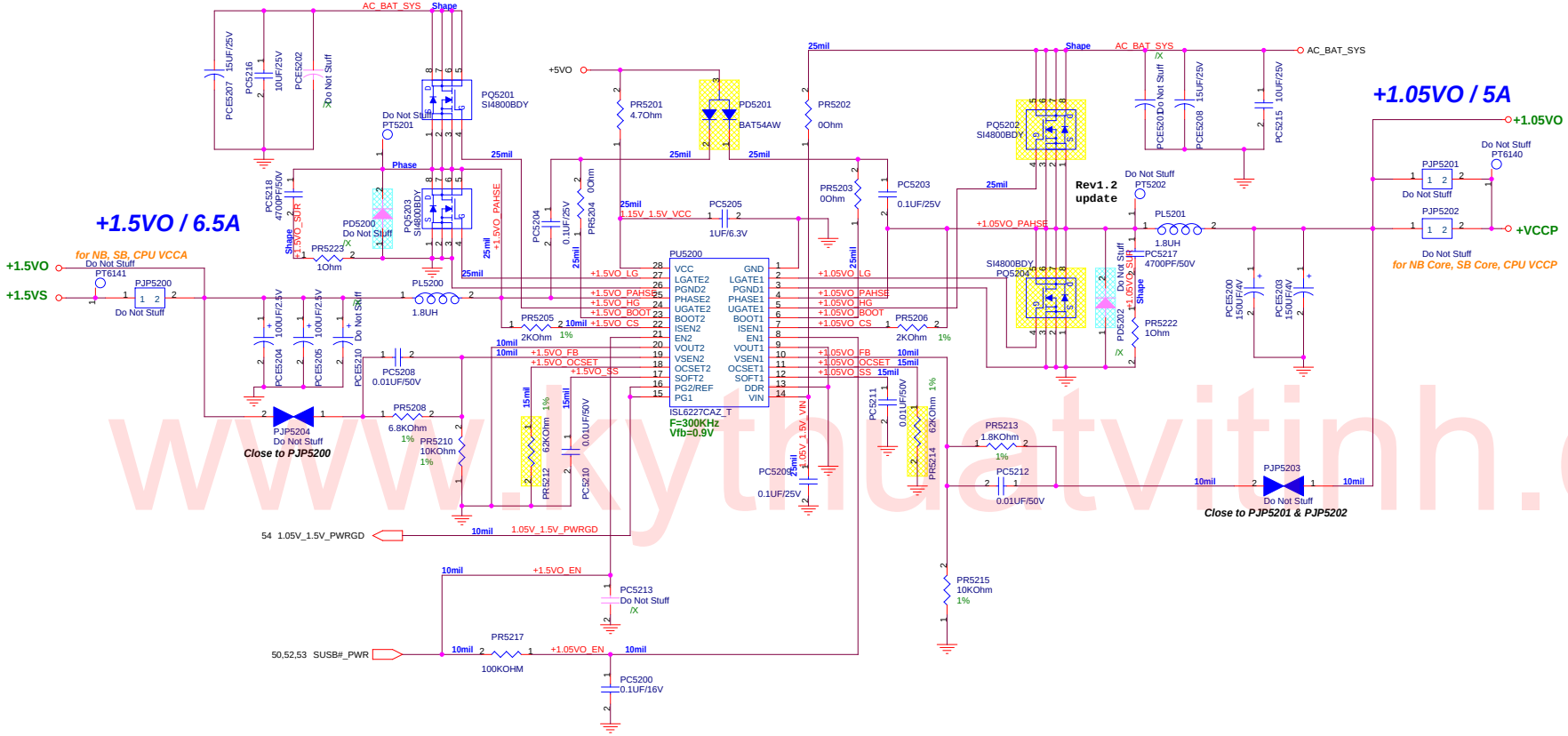

Net	Width	Net	Width
1.15V_1.5V_VCC	25mil	+1.5VO_SS	15mil
1.15V_1.5V_PWRGD	10mil	AC_BAT_SYS	Shape
1.15V_1.5V_VIN	25mil	+1.15VO_EN	10mil
+1.5VO_EN	10mil	+1.15VO_LG	25mil
+1.5VO_LG	25mil	+1.15VO_HG	25mil
+1.5VO_HG	25mil	+1.15VO_PHASE	Shape
+1.5VO_PHASE	Shape	+1.15VO_BOOT	25mil
+1.5VO_BOOT	25mil	+1.15VO_MODSEL	10mil
+1.5VO_MODSEL	10mil	+1.15VO_CS	10mil
+1.5VO_CS	10mil	+1.15VO_FB	10mil
+1.5VO_FB	10mil	+1.15VO_OCSET	25mil
+1.5VO_OCSET	15mil	+1.15VO_SS	15mil
+1.5VO_SUR	Shape	+1.15VO_SUR	Shape

2.0G

ASUS

Title : POWER_I/O_1.5VS & 1.05VS

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	Z84FM	2.0

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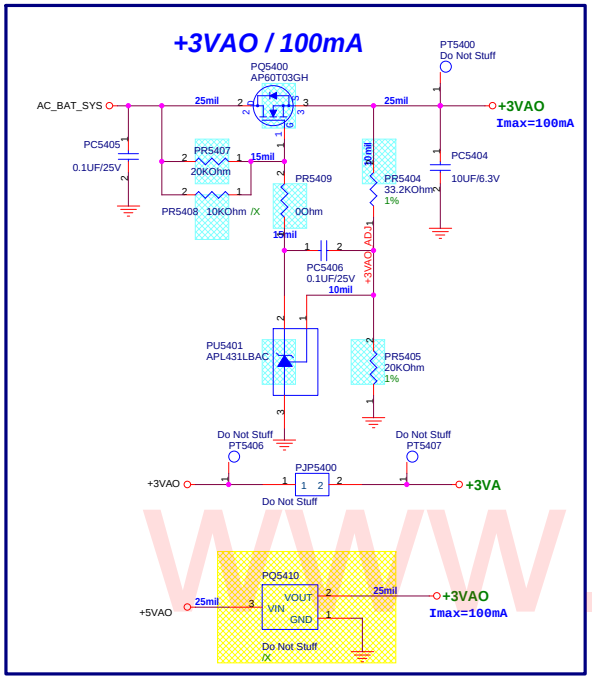

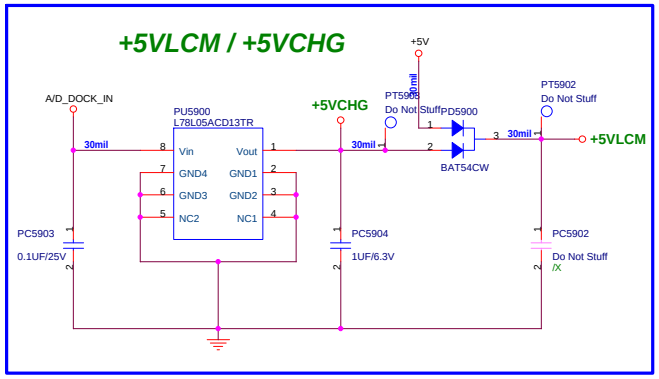

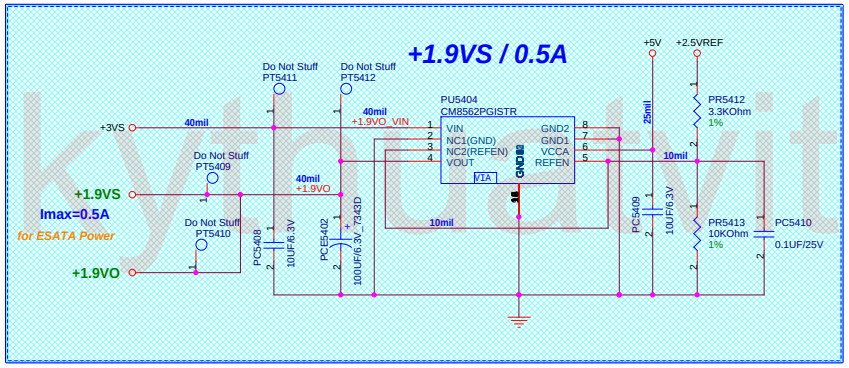

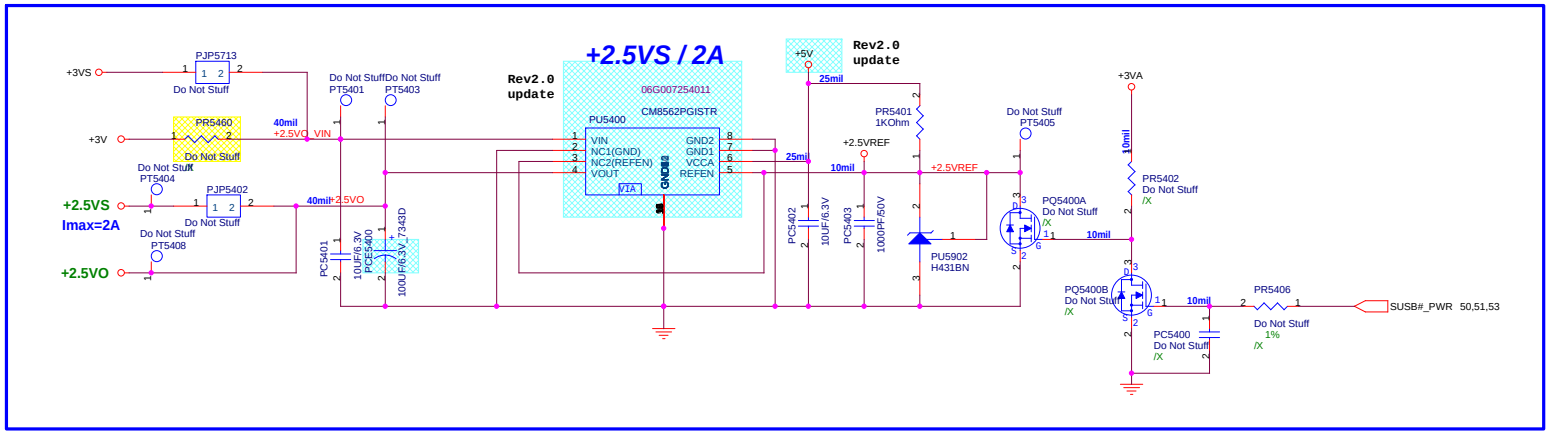

2.0G

ASUS

Title : POWER_I/O_+3VA & +2.5V

<OrgName>

Engineer:

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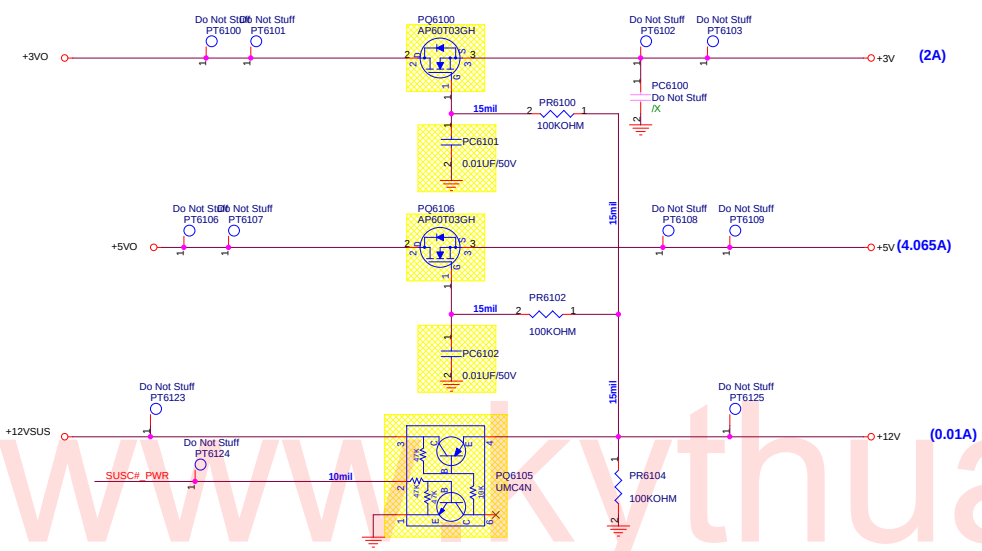
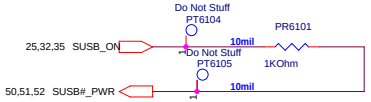
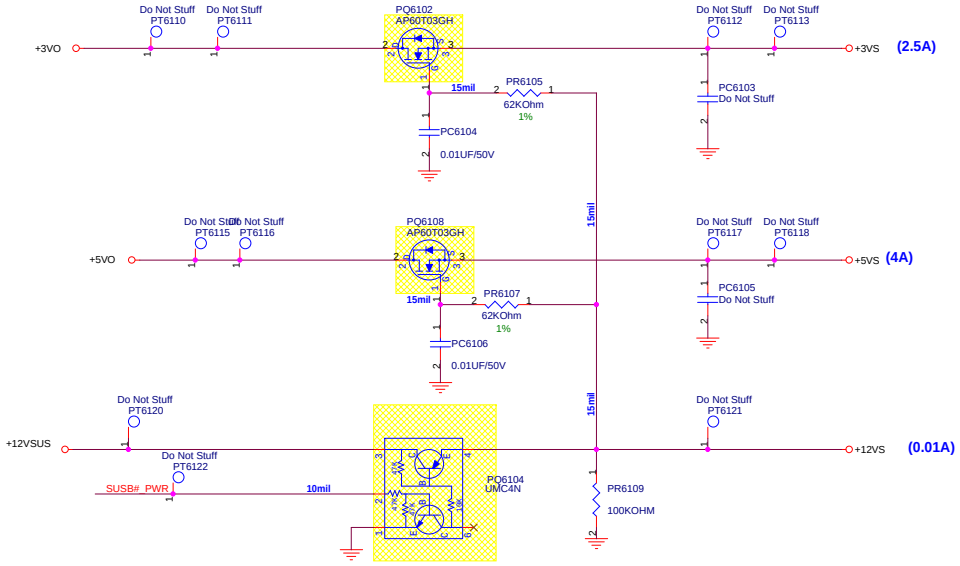
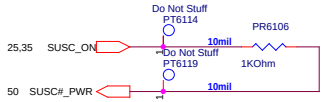
SUSC#_PWR POWER





SUSB#_PWR POWER





2.0G

ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: Z84FM	Rev: 2.0
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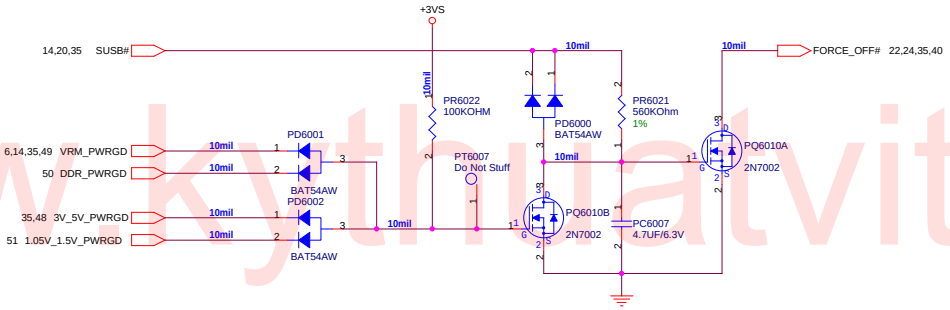
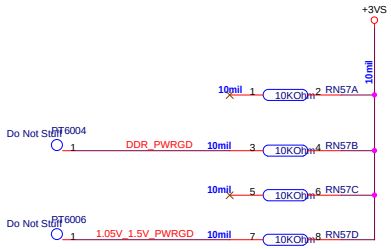
Power Good Detecter





2.0G

Title : POWER_PROTECT

<OrgName> Engineer:

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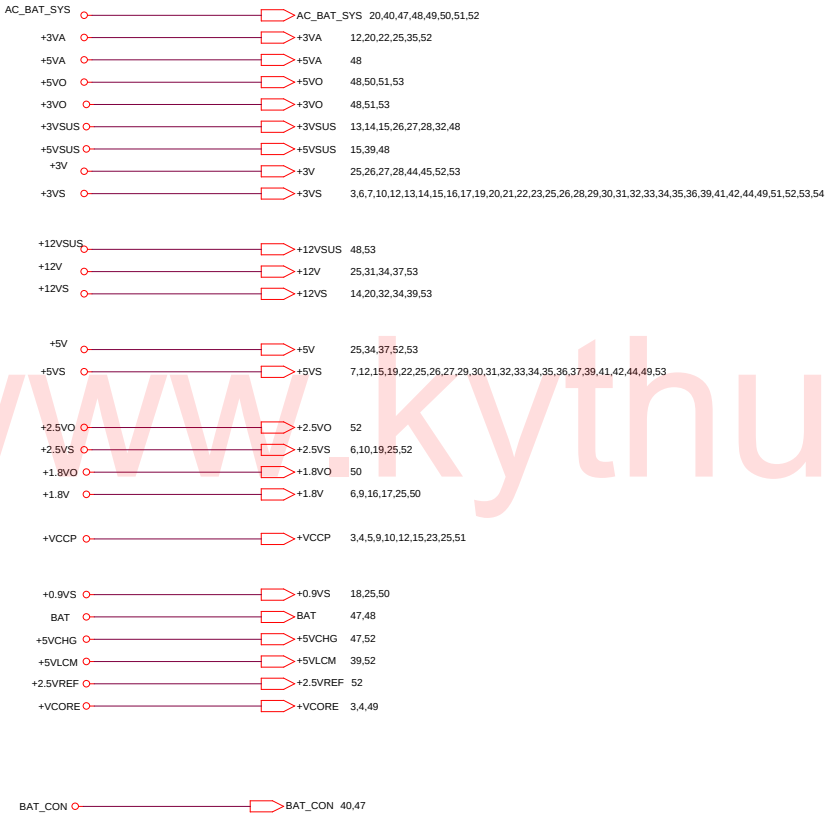

2.0G

Title : POWER_SIGNAL

<OrgName>

Engineer:

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Custom	Z84FM	2.0

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Rev	Date	Description
1.0	08/04/06	Refer Z84F R2.2G
1.0	08/04/06	1. Change PATA to SATA<p42>
1.0	08/08/06	2.Modify Audio circuit for Jack-sense<P33 & P34>
1.0	08/08/06	3.Add D40,D41,D42 for Battery varistor<P40>
1.0	08/08/06	4.Modify inverter connector pin define<P20>
1.0	08/08/06	5.Change CON5 Connector from 10pin to 12pin <p20>
1.0	08/10/06	6.ADD PR6125,PR6126 for DDR&VTT on S3 issue<P50>
1.0	08/10/06	7.Change CON21 touch pad connector type<P36>
1.0	08/10/06	8.Change J2 connector type for Azalia <P34>
1.0	08/10/06	9.Add C484,C485,C486,C487 for EMI Solution<P32>
2.0	08/16/06	1.Change R49 from 4.99K to 4.87K for Macro Vision issue <P7>
2.0	08/16/06	2.Add D43 and Del R422 for MIC2_VREFOUT issue<P33&P34>
2.0	09/11/06	3.R408 from 24.9 ohm change to 20 ohm for SATA eye-patten issue<P12>
2.0	09/12/06	4.PC5005, PC5017 from 0.1uF change to 0.22uF for Power solution<p49>
2.0	09/13/06	5.Add C488,C489,C490,C491,C492 and C493 for EMI solution<P42>
2.0	09/13/06	6.C481, C482 and C483 from /N change to load for EMI solution<P42>

Rev	Date	Description

2.0G

ASUSTek COMPUTER INC

Title : History

Engineer: Alan Chu

Size	Project Name	Rev
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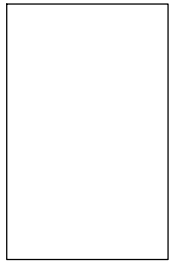
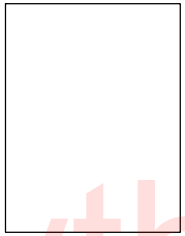
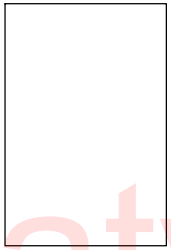
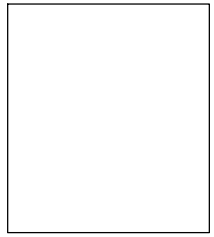
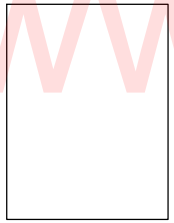
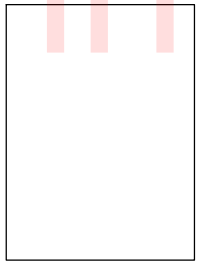

2.0G

Title : <Title>

ASUSTeK COMPUTER INC

Engineer: Alan Chu

Size	Project Name	Rev
A3	Z84FM	2.0

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