DQDN15 AMD QUEEN M12
Muxless /UMA Schematics Document

AMD LIANO APU FS1
AMD GPU Seymour XT

FCH HUDSON M3
PCB 10246-1
2011-05-28
REV : A00

DY :None Installed
UMA_PX:UMA and Muxless platform installed
DIS_PX:DIS and Muxless platform installed
PX:Muxless platform installed
FCH_UMA_PX:UMA_PX CRT FCH output
Whistler: For 8 X Vram
DN15: For DN15

DQ15 AMD DIS SAMSUNG TI

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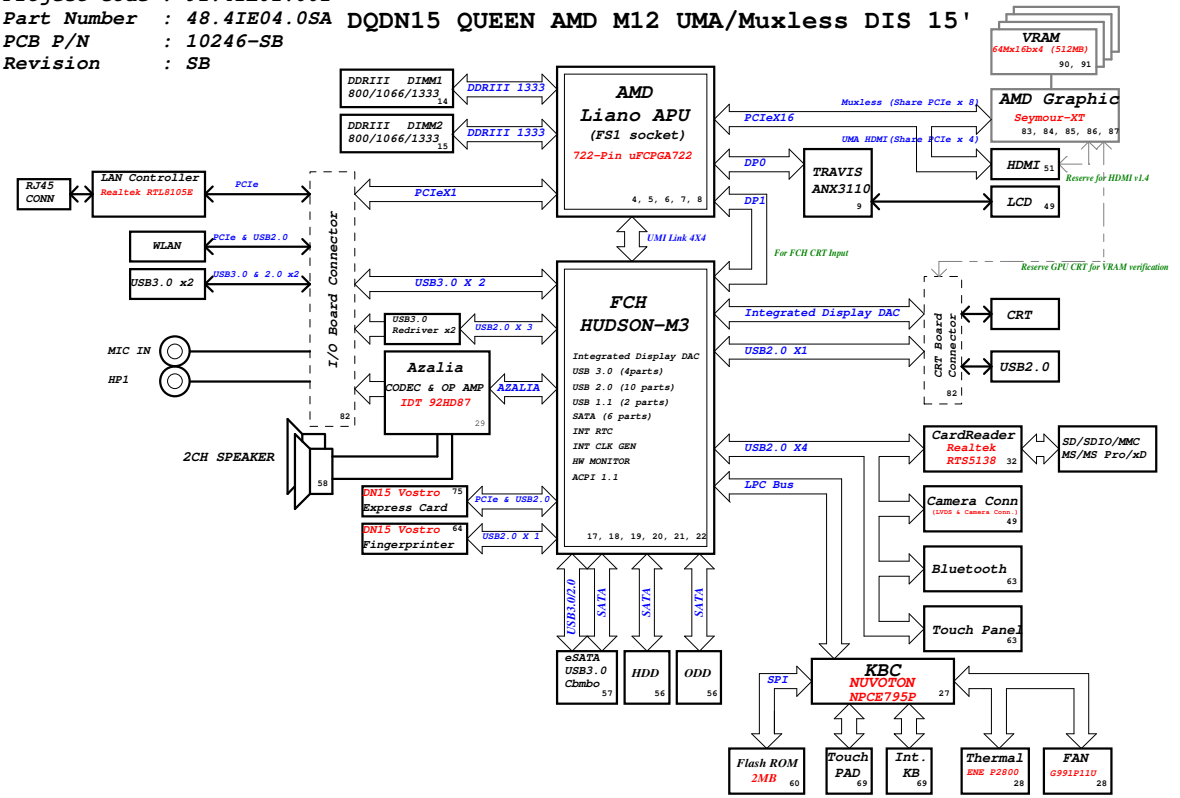
Project code : 91.4IE01.001
Part Number : 48.4IE04.0SA
PCB P/N : 10246-SB
Revision : SB

DQDN15 QUEEN AMD M12 UMA/Muxless DIS 15'



CHARGER	
BQ24745	40
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC	
TPS51123	41
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5

APU Core/NB Power	
ISL6267HRTZ-T	42, 43
INPUTS	OUTPUTS
DCBATOUT	APU_VDD APU_VDDNB

DDRIII SUS	
TPS51116RGER	44
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

DDRIII VTT	
TPS51116RGER	44
INPUTS	OUTPUTS
DCBATOUT	0D75V_S0

APU VDDR/VDDP	
RT8209	46
INPUTS	OUTPUTS
DCBATOUT	1D2V_S0

AMD FCH CORE Power	
RT8209	46
INPUTS	OUTPUTS
DCBATOUT	1D1V_S5

AMD GPU CORE	
RT8208B	92
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_PWR

PCB LAYER
L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

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Strapping

No Fusion Config, Strap Not needed, but reserve

REQUIRED SYSTEM STRAPS

	EC_PWM2 PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM DEFAULT	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

USB Table

USB	
Pair	Device
0	USB Debug Port / CRT USB 2.0
1	Mini Card (WLAN)
2	Fingerprint
3	~~WWAN~~
4	Bluetooth
5	Touch Panel
6	~~eSATA/USB Charger~~
7	CCD Camera
8	~~New Card~~
9	CardReader
10	USB 3.0 port 1
11	USB 3.0 port 2
12	USB 3.0 port 3
13	USB 3.0 port 4

PCIe Routing

	APU
LANE0	LAN
LANE1	~~WWAN~~
LANE2	WLAN
LANE3	~~CardReader~~

	FCH
LANE0	
LANE1	~~Express Card~~
LANE2	
LANE3	

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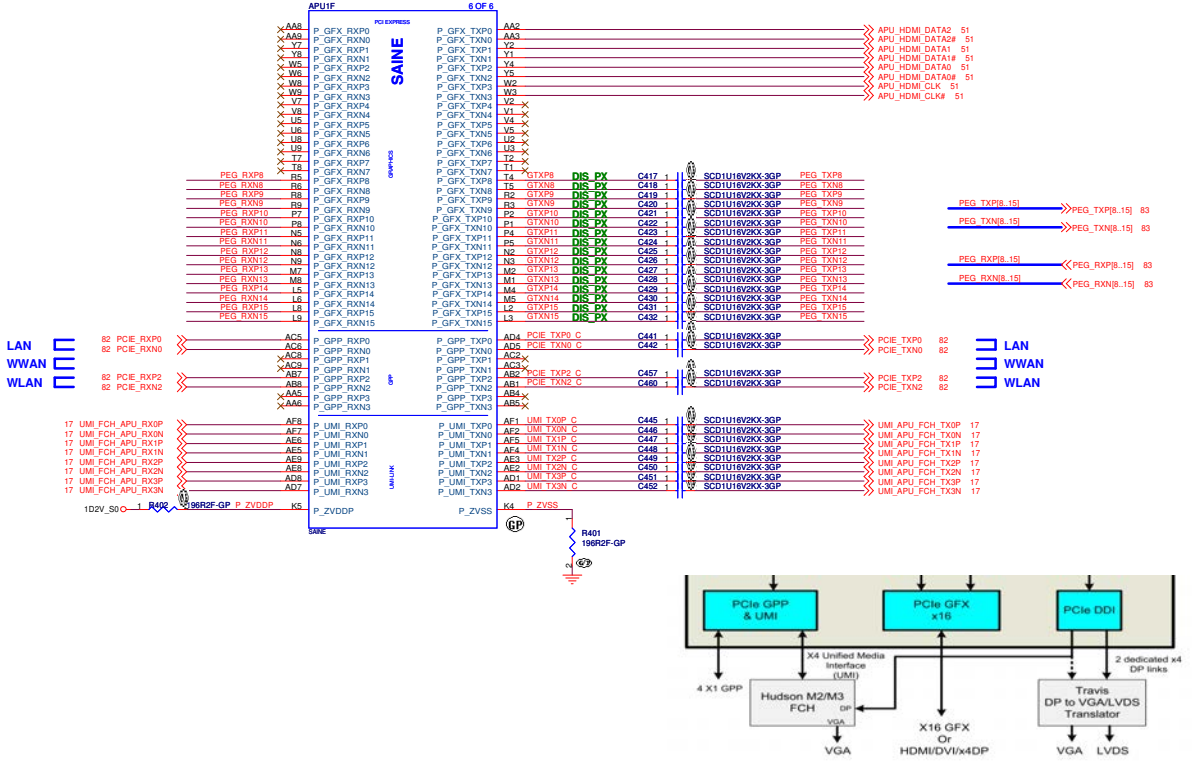

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Title: **APU_PCIE(1/5)**

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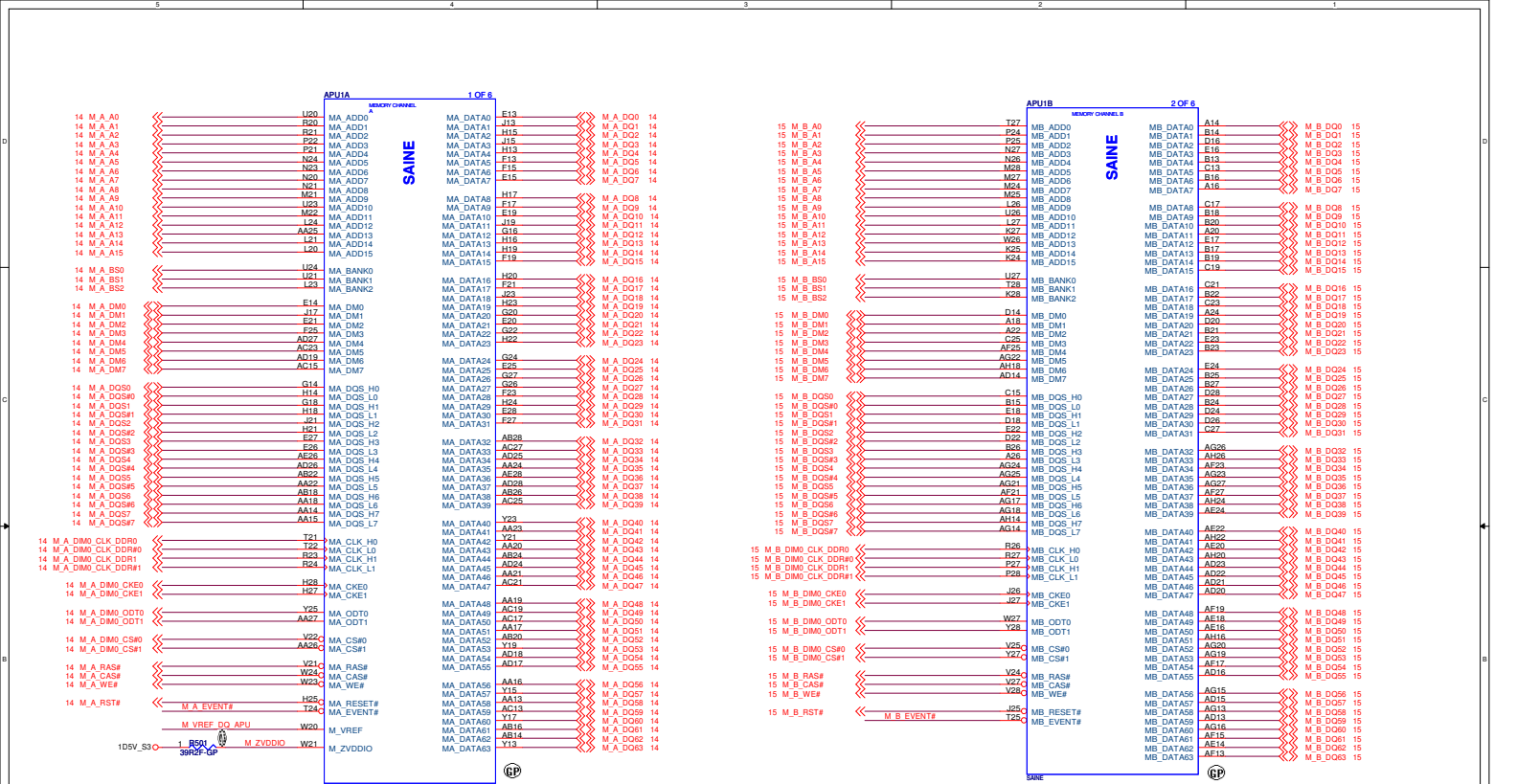
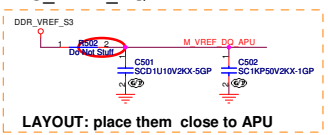
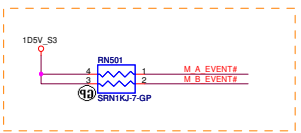


APU_VREF_DQ





1207: Change To 4 Pin Array Resistor

AMD Confirm: PU Needed even if not used

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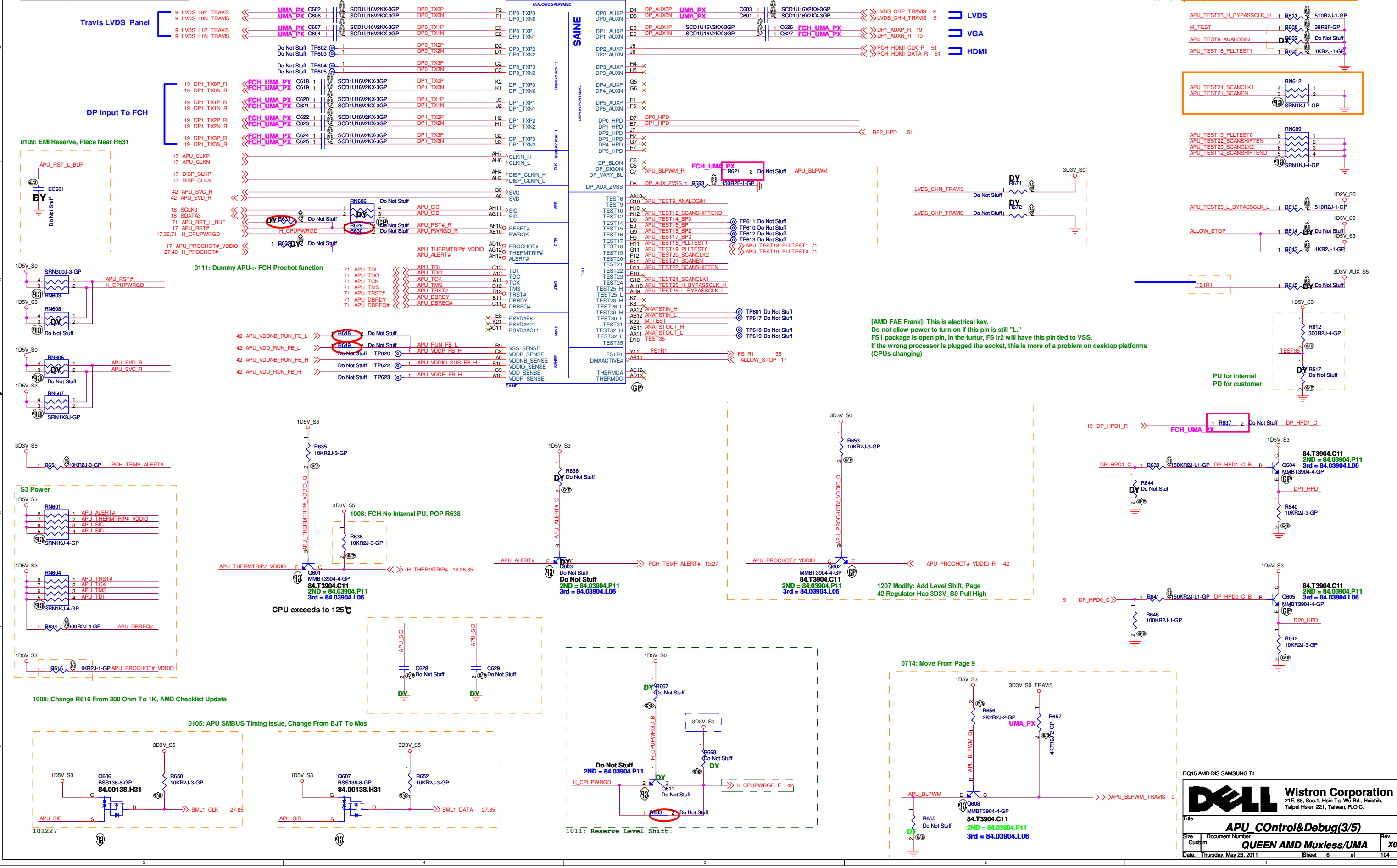
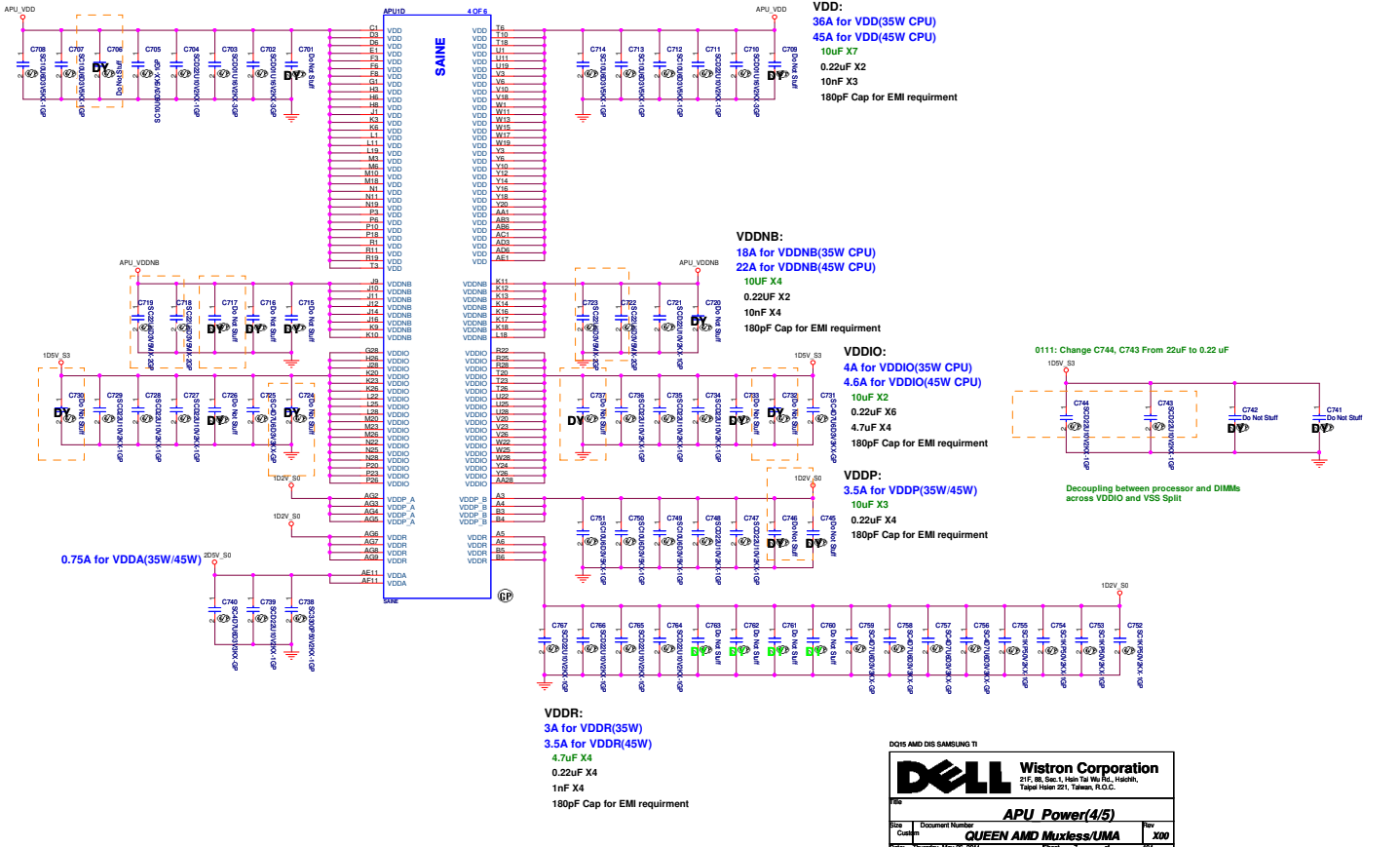
SVC	SVD	Boot Voltage (VCC/GND)	Boot Voltage (open)
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.1
1	1	0.8	0.9




APU_VDD
APU1D
4 OF 6
SAINE
VDD:
36A for VDD(35W CPU)
45A for VDD(45W CPU)
10uF X7
0.22uF X2
10nF X3
180pF Cap for EMI requirment
APU_VDDNB
VDDNB:
18A for VDDNB(35W CPU)
22A for VDDNB(45W CPU)
10UF X4
0.22UF X2
10nF X4
180pF Cap for EMI requirment
1D5V_S3
VDDIO:
4A for VDDIO(35W CPU)
4.6A for VDDIO(45W CPU)
10uF X2
0.22uF X6
4.7uF X4
180pF Cap for EMI requirment
0111: Change C744, C743 From 22uF to 0.22 uF
Decoupling between processor and DIMMs across VDDIO and VSS Split
1D2V_S0
VDDP:
3.5A for VDDP(35W/45W)
10uF X3
0.22uF X4
180pF Cap for EMI requirment
0.75A for VDDA(35W/45W)
2D5V_S0
VDDR:
3A for VDDR(35W)
3.5A for VDDR(45W)
4.7uF X4
0.22uF X4
1nF X4
180pF Cap for EMI requirment
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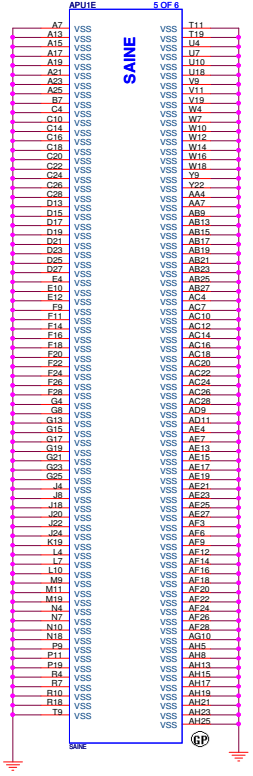

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1207: Use PLT_RST# to replace
3D3V_S0_TRAVIS for APU_PCIE_RST#_R.

0628: Change Tolerance to 5 %

TRAVIS Rev 1.01 suggest
to stuff 1M-ohm

1231: New Spec Changed Pin 30 To IN and Connect P,
From Vendor Feedback. Mail Confirm

0105: Vendor Suggestion To Add Pair of Cap In Near Travis Also

if use single channel,
have to use L Group

No Need

0112: Vendor Suggestion To Add PU For AUXP, PL for AUXN

1231: Change To 10K PU

1231:Reserve 10K, Vendor Suggest

Vendor Confirm: C912 100p

Figure 3-2: AUX CH Differential Pair

0504 -Sabine David
Annie and Rosa team soluton co-layout

MOS spec VGS:20V
Rosa:RUN_Enable 15V
Annie:RUN Enable 9V

0714: Add to Avoid System Run Power Being Pull Low

Do Not Stuff
2ND = 84.2N702.031

Reserved for tuning sequence of 3.3V and 1.2V

MOS spec VGS:20V
Rosa:RUN_Enable 15V
Annie:RUN Enable 9V

ANX9834 power on delay time

For ANX3100 ALSO

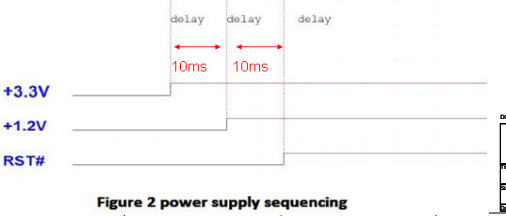

Figure 2 power supply sequencing

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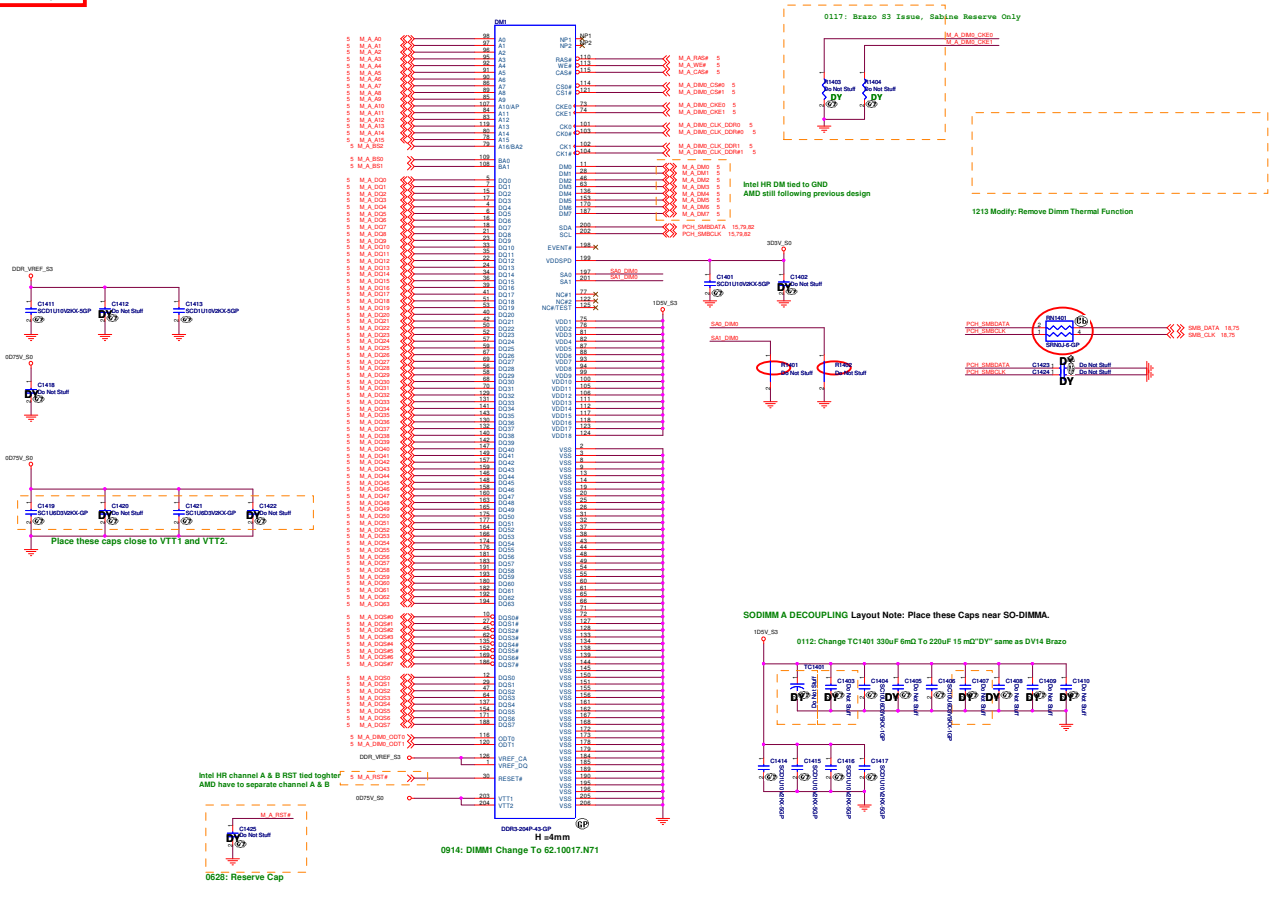
SSID = MEMORY



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SSID = MEMORY

SO-DIMMB is placed farther from the Processor than SO-DIMMA

0117: Brazo S3 Issue, Sabine Reserve Only

Intel HR DM tied to GND
AMD still following previous design

Intel HR B channel address is 01
AMD B channel address is 10

SODIMM B DECOUPLING

Layout Note: Place these Caps near SO-DIMMB.

Place these caps close to VTT1 and VTT2.

Intel HR channel A & B RST tied togther
AMD have to separate channel A & B

0628: Reserve Cap

0914: DIMM2 Change To 62.10017.N91

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Title: DDR3-SODIMM2

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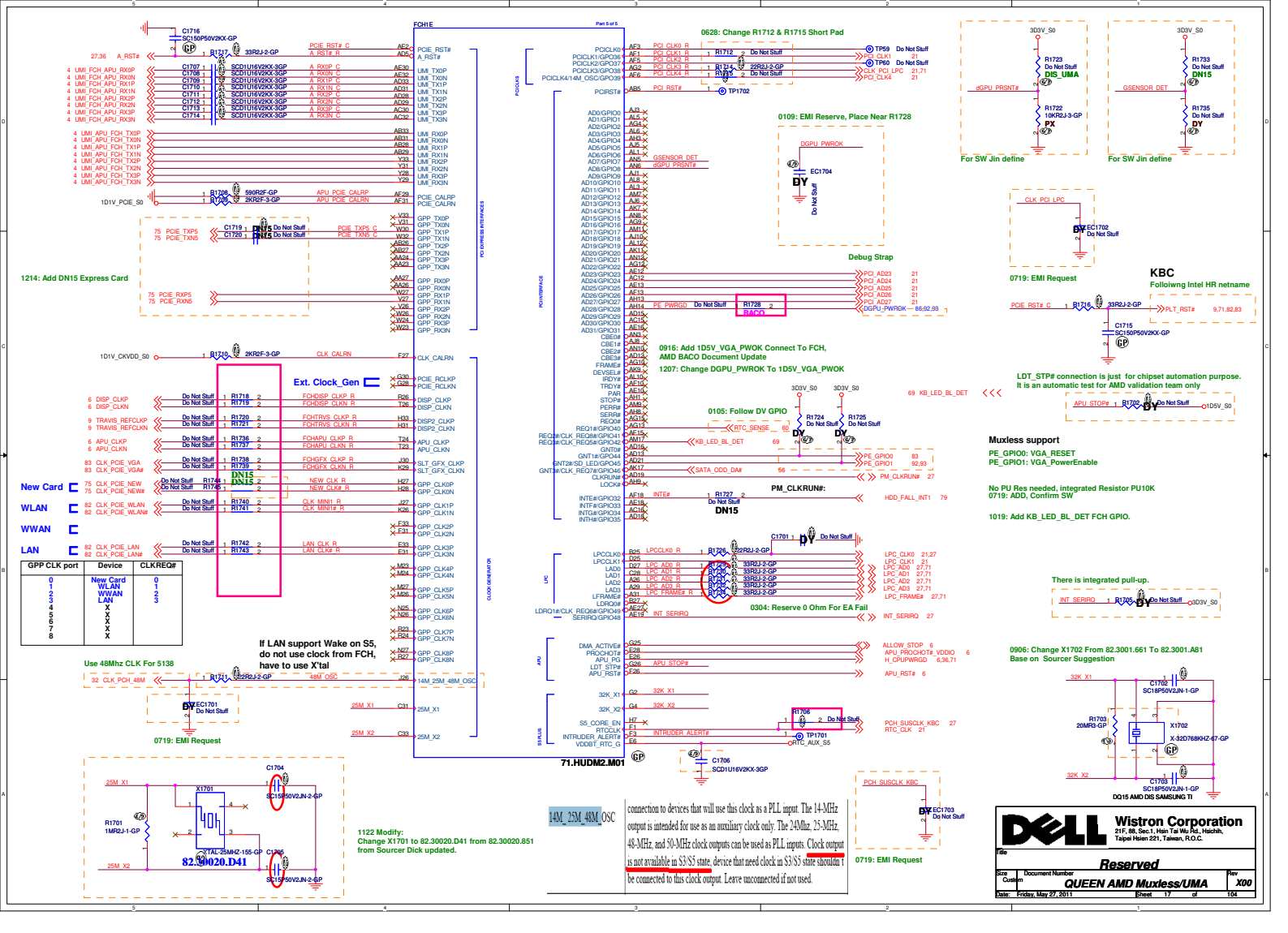

GPP CLK port	Device	CLKREQ#
0	New Card	0
1	WLAN	1
2	WWAN	2
3	LAN	3
4	X	
5	X	
6	X	
7	X	
8	X	

0909: Modify
Pop R1843 For UMA Config
Pop R1844 For Muxless Config

0109: EMI Reserve, Place Near R1810

Remove PCIE2_RST, Did Not Use FCH GPP

1213 Modify: Remove Dimm Thermal Function
1214 Add PCIE2_RST For EXPRESS CARD FCH GPP

Confirm with SW, RSMRST# from KBC is push-pull.
It can be drived high by SW.

0716: From KBC

0719: ADD

* Travis_EN#: Base on AMD suggestion, use the GPIO66 same the CRB first.
If it work normally, ask BIOS to re-program to GPIO55 to double verify.

0719: Change From 2.2K and POP

There are integrated pull-up.

0721: Reserve PM_PWRBTN# If KBC Change To OD

Modify Zero Power ODD circuit by
Annie team suggestion.

Checklist suggestion: Don't stuff for default

0719: Modify

Integrated PU is not
supported when the pin is
configured for USB over
current function.

0909: Un-Stuff (DY) For Leakage Issue, Follow DQ15 Intel

1214: Add Express Card For DN15

1214: Add FP For DN15

0914: Remove DBC_EN & COLOR_ENGINE

0719: If not used SMBUS or GPIO, PD 10k.

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Pari	USB Device
0	USB Debug port
1	Mini Card1 (WLAN)
2	Fingerprint
3	Mini Card2 (WWAN)
4	Bluetooth
5	Touch Panel / 3G SIM Card
6	E-SATA / USB CHARGER
7	CCD
8	New Card
9	Card Reader
10	USB 2.0 & 3.0 Ext. port 1
11	USB 2.0 & 3.0 Ext. port 2
12	USB 2.0 & 3.0 Ext. port 3
13	USB 2.0 & 3.0 Ext. port 4

Function	Net Name	Integrated Resistor	External Resistor
GA20IN	H_A20GATE	8.2k Pull-up	10k PU 3.3_S0 [DY]
KBRST#	H_RCIN#	8.2k Pull-up	10k PU 3.3_S0 [DY]
PME#	EC_SCI#	10kPull-up	10k PU 3.3_S5 [DY]
THRIPTRIP#	H_THERMTRIP#	10kPull-up	10k PU 3.3_S5 [DY]
PCIE_RST2#	PCH_PCIE_RST#	10kPull-up	
Gevent5	MEM_Hot#	10kPull-up	
Gevent6	EC_SWI#	10kPull-up	10k PU 3.3_S5 [DY]
WAKE#	PCIE_WAKE#	10kPull-up	10k PU 3.3_S5 [DY]
USB_OC0#	USB_OC0#	10kPull-up	
USB_OC1#	USB_OC1#	10kPull-up	
USB_OC2#	USB_OC2#	10kPull-up	
Gevent15#	SATA_ODD_PRSNT#	10kPull-up	
Gevent16#	ODD_DA	10kPull-up	
USB_OC5#	USB_OC5#	10kPull-up	
Gevent17#	EC_SWI#	10kPull-up	10k PU 3.3_S0 [DY]
USB_OC7#	USB_OC7#	10kPull-up	
LPC_SMI#	EC_SMI#	8.2k Pull-up	10k PU 3.3_S5 [DY]
GPIO35	SATA_ODD_DA#	8.2k Pull-up	
SERIRQ	INT_SERIRQ	8.2k Pull-up	10k PU 3.3_S0 [DY]
CLK_REQ0	CLK_PCIE_NEW_REQ#	8.2k Pull-up	
CLK_REQ1	CLK_PCIE_WLAN_REQ#	8.2k Pull-up	
CLK_REQ2	CLK_PCIE_WWAN_REQ#	8.2k Pull-up	
CLK_REQ3	PCIE_CLK_LAN_RQ1#	8.2k Pull-up	
CLK_REQG	PEG_CLKREQ#	8.2k Pull-up	

71.HUDM2.M01

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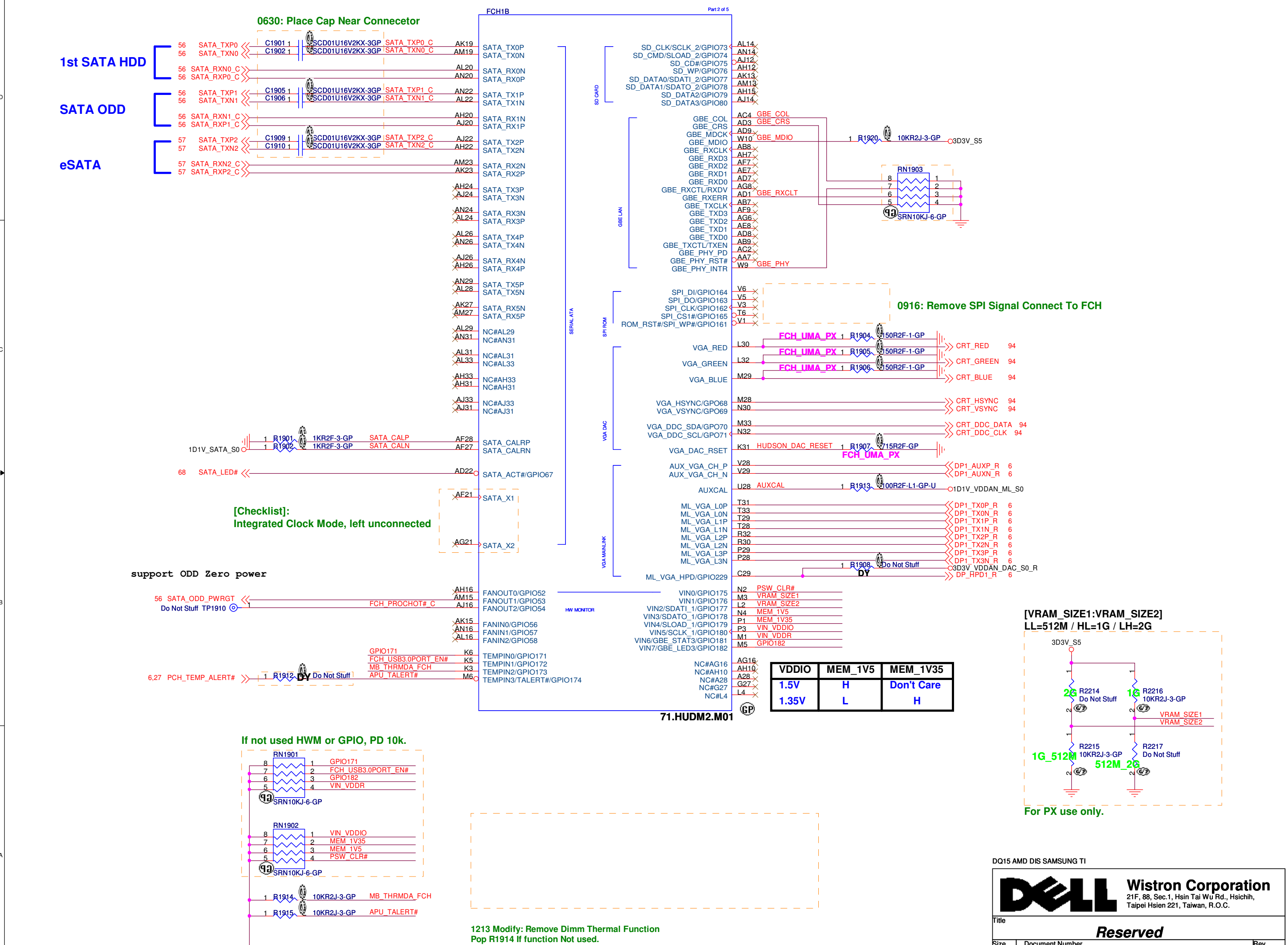

FCH1B
Part 2 of 5
0630: Place Cap Near Connector
1st SATA HDD
SATA ODD
eSATA
SATA_TXP0
SATA_TXN0
SATA_RXN0_C
SATA_RXP0_C
SATA_TXP1
SATA_TXN1
SATA_RXN1_C
SATA_RXP1_C
SATA_TXP2
SATA_TXN2
SATA_RXN2_C
SATA_RXP2_C
C1901
C1902
C1905
C1906
C1909
C1910
SCD01U16V2KX-3GP
SERIAL ATA
SD CARD
GBE LAN
SPI ROM
VGA DAC
VGA MAINLINK
HW MONITOR
SATA_CALP
SATA_CALN
1D1V_SATA_S0
R1901
R1902
1KR2F-3-GP
SATA_LED#
SATA_ACT#/GPIO67
[Checklist]:
Integrated Clock Mode, left unconnected
SATA_X1
SATA_X2
support ODD Zero power
SATA_ODD_PWRGT
Do Not Stuff TP1910
FCH_PROCHOT#_C
FANOUT0/GPIO52
FANOUT1/GPIO53
FANOUT2/GPIO54
FANIN0/GPIO56
FANIN1/GPIO57
FANIN2/GPIO58
GPIO171
FCH_USB3.0PORT_EN#
MB_THRMDA_FCH
APU_TALERT#
TEMPIN0/GPIO171
TEMPIN1/GPIO172
TEMPIN2/GPIO173
TEMPIN3/TALERT#/GPIO174
PCH_TEMP_ALERT#
R1912
DY
Do Not Stuff
GBE_COL
GBE_CRS
GBE_MDIO
GBE_RXCLT
GBE_PHY
R1920
10KR2J-3-GP
3D3V_S5
RN1903
SRN10KJ-6-GP
0916: Remove SPI Signal Connect To FCH
SPI_DI/GPIO164
SPI_DO/GPIO163
SPI_CLK/GPIO162
SPI_CS1#/GPIO165
ROM_RST#/SPI_WP#/GPIO161
FCH_UMA_PX
R1904
R1905
R1906
150R2F-1-GP
VGA_RED
VGA_GREEN
VGA_BLUE
CRT_RED
CRT_GREEN
CRT_BLUE
CRT_HSYNC
CRT_VSYNC
CRT_DDC_DATA
CRT_DDC_CLK
VGA_DAC_RSET
HUDSON_DAC_RESET
R1907
715R2F-GP
AUXCAL
R1913
100R2F-L1-GP-U
1D1V_VDDAN_ML_S0
DP1_AUXP_R
DP1_AUXN_R
DP1_TX0P_R
DP1_TX0N_R
DP1_TX1P_R
DP1_TX1N_R
DP1_TX2P_R
DP1_TX2N_R
DP1_TX3P_R
DP1_TX3N_R
R1908
3D3V_VDDAN_DAC_S0_R
DP_HPD1_R
ML_VGA_HPD/GPIO229
PSW_CLR#
VRAM_SIZE1
VRAM_SIZE2
MEM_1V5
MEM_1V35
VIN_VDDIO
VIN_VDDR
GPIO182
71.HUDM2.M01
[VRAM_SIZE1:VRAM_SIZE2]
LL=512M / HL=1G / LH=2G
R2214
R2216
R2215
R2217
10KR2J-3-GP
2G
1G
1G_512M
512M_2G
For PX use only.
If not used HWM or GPIO, PD 10k.
RN1901
RN1902
R1914
R1915
1213 Modify: Remove Dimm Thermal Function
Pop R1914 If function Not used.

VDDIO	MEM_1V5	MEM_1V35
1.5V	H	Don't Care
1.35V	L	H

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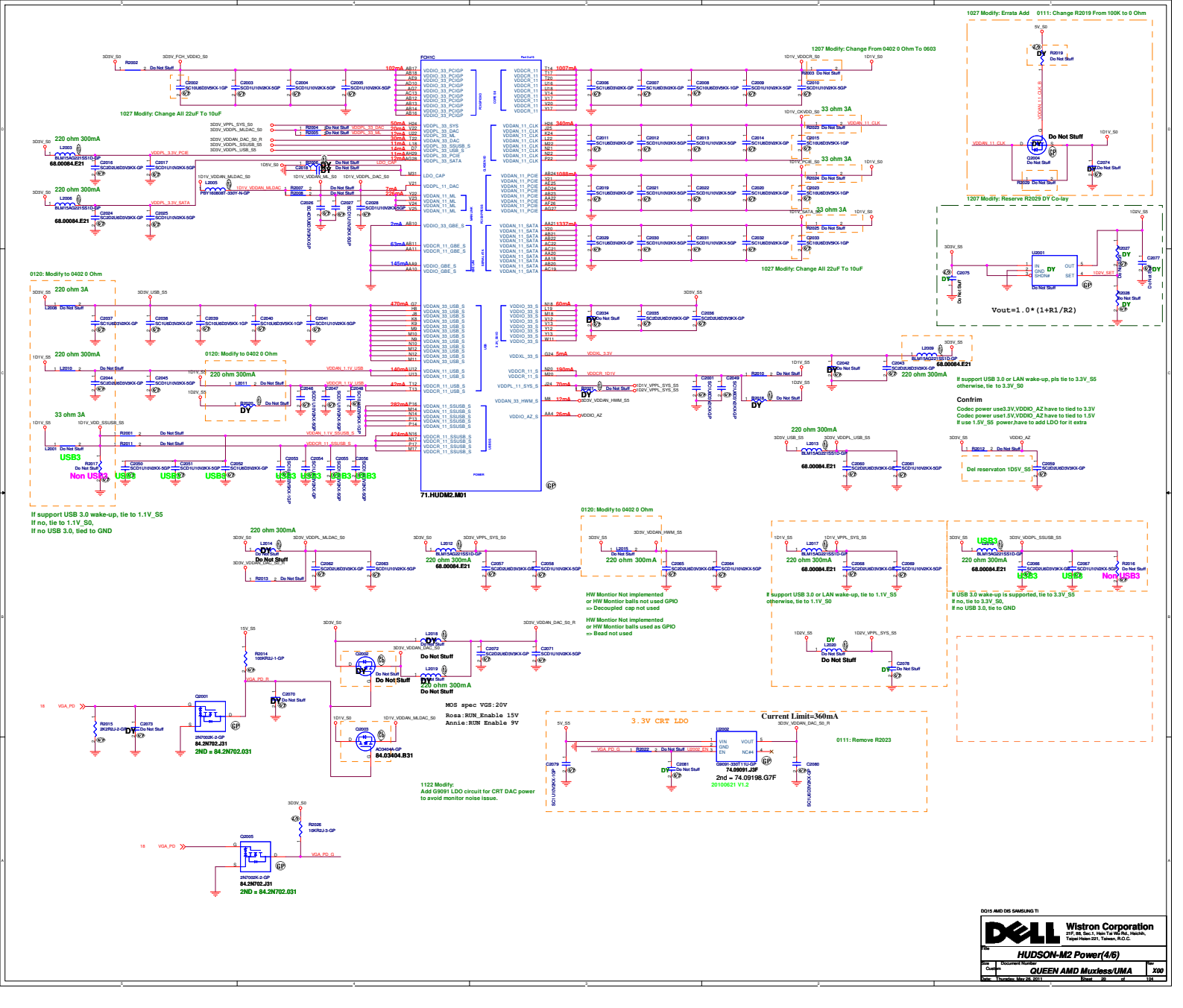
1027 Modify: Errata Add 0111: Change R2019 From 100K to 0 Ohm
1207 Modify: Change From 0402 0 Ohm To 0603
1027 Modify: Change All 22uF To 10uF
1207 Modify: Reserve R2029 DY Co-lay
0120: Modify to 0402 0 Ohm
220 ohm 300mA
220 ohm 3A
33 ohm 3A
Do Not Stuff
68.00084.E21
FCH1C
71.HUDM2.M01
If support USB 3.0 wake-up, pls tie to 3.3V_S5 otherwise, tie to 3.3V_S0
Confirm
Codec power use3.3V,VDDIO_AZ have to tied to 3.3V
Codec power use1.5V,VDDIO_AZ have to tied to 1.5V
If use 1.5V_S5 power,have to add LDO for it extra
Del reservaton 1D5V_S5
If support USB 3.0 wake-up, tie to 1.1V_S5
If no, tie to 1.1V_S0,
If no USB 3.0, tied to GND
If support USB 3.0 or LAN wake-up, tie to 1.1V_S5 otherwise, tie to 1.1V_S0
HW Montior Not implemented or HW Montior balls not used GPIO => Decoupled cap not used
HW Montior Not implemented or HW Montior balls used as GPIO => Bead not used
If USB 3.0 wake-up is supported, tie to 3.3V_S5 If no, tie to 3.3V_S0 If no USB 3.0, tie to GND
MOS spec VGS:20V
Rosa:RUN_Enable 15V
Annie:RUN Enable 9V
1122 Modify: Add G9091 LDO circuit for CRT DAC power to avoid monitor noise issue.
3.3V CRT LDO
Current Limit=360mA
0111: Remove R2023
Vout=1.0*(1+R1/R2)
2nd = 74.09198.G7F
20100621 V1.2
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
AO3404A-GP
84.03404.B31
USB3
USB2
Non USB3
Non USB2
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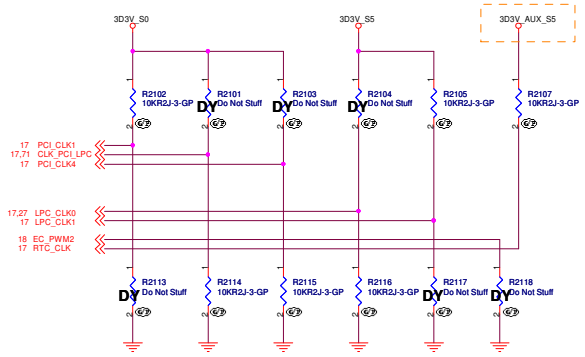
HUDSON-M2 Power(4/6)
QUEEN AMD Muxless/UMA
X00
Thursday, May 26, 2011

SSID = S.B

REQUIRED STRAPS

CRB: PU to 3.3V_AUX_S5
Checklist: PU to 3.3V_S5
Confirm with AMD, follow CRB suggestion



REQUIRED SYSTEM STRAPS

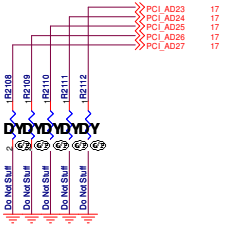
Use this pin to determine INT/EXT CLK

	EC_PWM2 PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

No Fusion Config, Strap Not needed, but reserve

Ball Name	Strap Function	Description
EC_PWM2	ROM Type	SPI ROM: 2.2-KΩ 5% pull-down LPC ROM: Pull-up to 3.3V_S5. External pull-up resistor is not required as FCH has integrated 10-KΩ pull-up to 3.3V_S5.

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: FCH has 15K internal PU FOR PCI_AD[27:23]

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Title: SB820M_STRAPPING_(5/5)

Size: A3 | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

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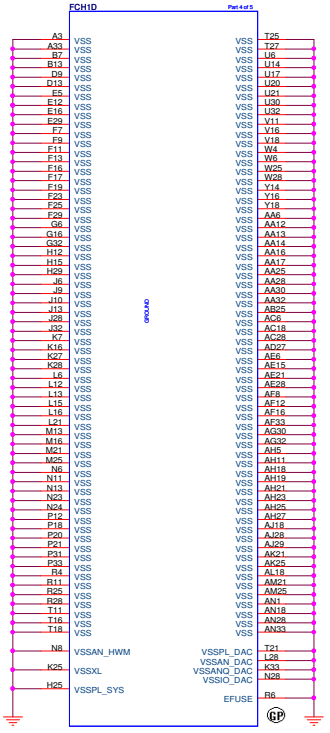

71.HUDM2.M01

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A3	QUEEN AMD Muxless/UMA	A00

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Title

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Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	00

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A3	*QUEEN AMD Muxless/UMA*	*X00*

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A3	*QUEEN AMD Muxless/UMA*	*00*

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Title

Reserved

Size	Document Number	Rev
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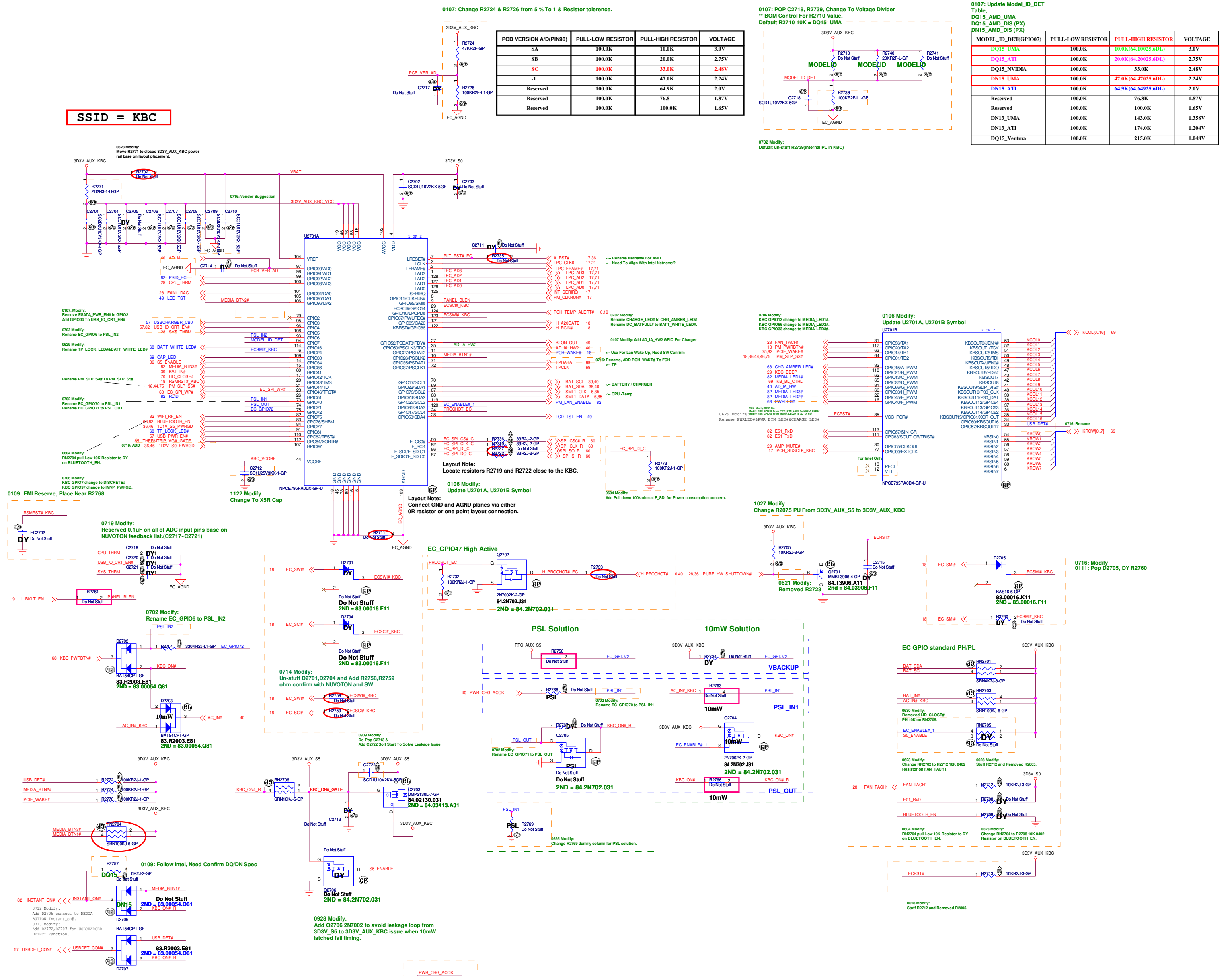
SSID = KBC

0107: Change R2724 & R2726 from 5 % To 1 & Resistor tolerence.

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V

0107: Update Model_ID_DET Table,
DQ15_AMD_UMA
DQ15_AMD_DIS (PX)
DN15_AMD_DIS (PX)

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DQ15_UMA	100.0K	10.0K(64.10025.6DL)	3.0V
DQ15_ATI	100.0K	20.0K(64.20025.6DL)	2.75V
DQ15_NVIDIA	100.0K	33.0K	2.48V
DN15_UMA	100.0K	47.0K(64.47025.6DL)	2.24V
DN15_ATI	100.0K	64.9K(64.64925.6DL)	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V
DN13_UMA	100.0K	143.0K	1.358V
DN13_ATI	100.0K	174.0K	1.204V
DQ15_Ventura	100.0K	215.0K	1.048V



0107: POP C2718, R2739, Change To Voltage Divider
** BOM Control For R2710 Value.
Default R2710 10K = DQ15_UMA
0702 Modify:
Default un-stuff R2739(internal PL in KBC)
0628 Modify:
Move R2771 to closed 3D3V_AUX_KBC power rail base on layout placement.
U2701A
NPCE795PA0DX-GP-U
U2701B
0106 Modify:
Update U2701A, U2701B Symbol
Layout Note:
Locate resistors R2719 and R2722 close to the KBC.
Layout Note:
Connect GND and AGND planes via either 0R resistor or one point layout connection.
1122 Modify:
Change To X5R Cap
0109: EMI Reserve, Place Near R2768
0719 Modify:
Reserved 0.1uF on all of ADC input pins base on NUVOTON feedback list.(C2717~C2721)
0702 Modify:
Rename EC_GPIO6 to PSL_IN2
EC_GPIO47 High Active
0714 Modify:
Un-stuff D2701,D2704 and Add R2758,R2759 ohm confirm with NUVOTON and SW.
1027 Modify:
Change R2075 PU From 3D3V_AUX_S5 to 3D3V_AUX_KBC
0621 Modify:
Removed R2723
0716: Modify
0111: Pop D2705, DY R2760
PSL Solution
10mW Solution
EC GPIO standard PH/PL
0109: Follow Intel, Need Confirm DQ/DN Spec
0928 Modify:
Add Q2706 2N7002 to avoid leakage loop from 3D3V_S5 to 3D3V_AUX_KBC issue when 10mW latched fail timing.
0109: EMI Reserve, Place Near R2768

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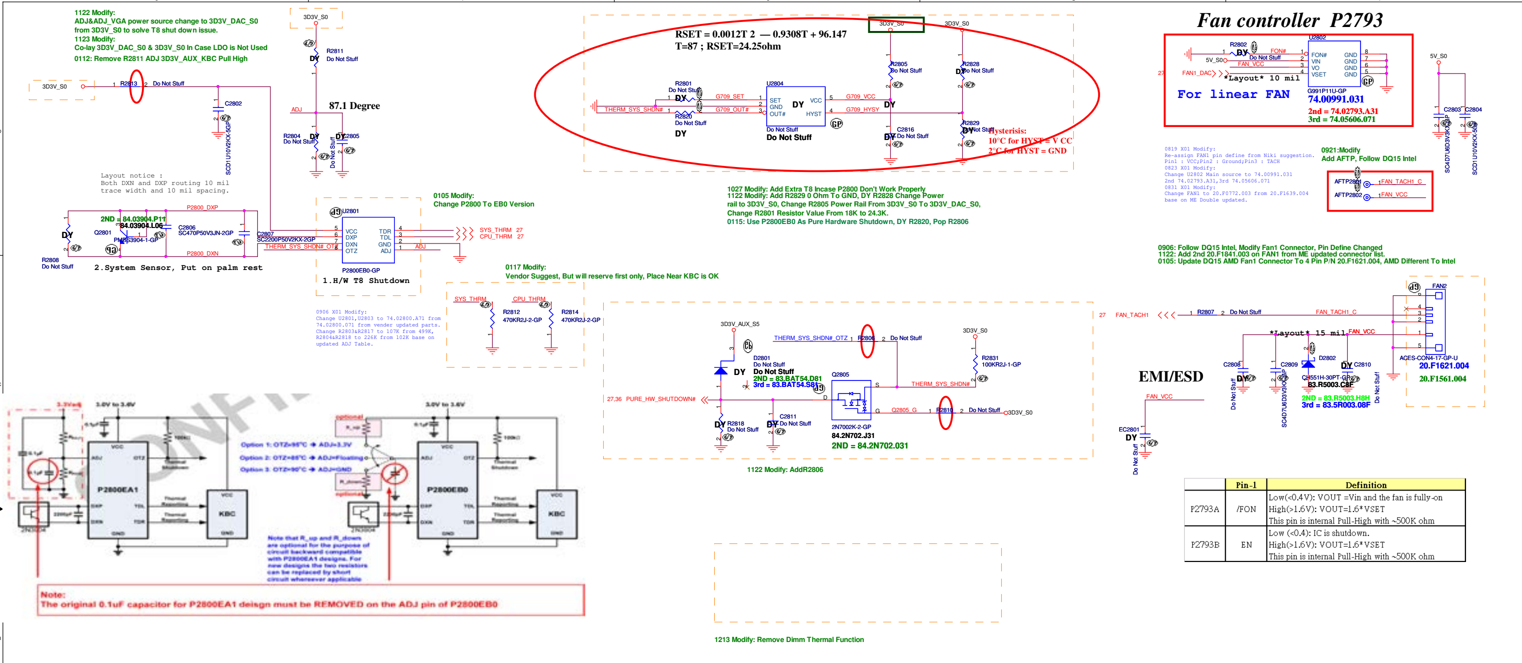
Title	KBC Nuvoton NPCE795	
Size: Custom	Document Number: QUEEN AMD Muxless/UMA	Rev: X00
Date: Thursday, May 26, 2011	Sheet 27 of 104	


1122 Modify:
ADJ&ADJ_VGA power source change to 3D3V_DAC_S0 from 3D3V_S0 to solve T8 shut down issue.
1123 Modify:
Co-lay 3D3V_DAC_S0 & 3D3V_S0 In Case LDO is Not Used
0112: Remove R2811 ADJ 3D3V_AUX_KBC Pull High
87.1 Degree
Layout notice :
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.
2.System Sensor, Put on palm rest
1.H/W T8 Shutdown
0105 Modify:
Change P2800 To EB0 Version
RSET = 0.0012T 2 — 0.9308T + 96.147
T=87 ; RSET=24.25ohm
Hysterisis:
10°C for HYST = V CC
2°C for HYST = GND
1027 Modify: Add Extra T8 Incase P2800 Don't Work Properly
1122 Modify: Add R2829 0 Ohm To GND, DY R2828 Change Power rail to 3D3V_S0, Change R2805 Power Rail From 3D3V_S0 To 3D3V_DAC_S0, Change R2801 Resistor Value From 18K to 24.3K.
0115: Use P2800EB0 As Pure Hardware Shutdown, DY R2820, Pop R2806
0117 Modify:
Vendor Suggest, But will reserve first only, Place Near KBC is OK
Fan controller P2793
For linear FAN
Layout 10 mil
74.00991.031
2nd = 74.02793.A31
3rd = 74.05606.071
0921:Modify
Add AFTP, Follow DQ15 Intel
0906: Follow DQ15 Intel, Modify Fan1 Connector, Pin Define Changed
1122: Add 2nd 20.F1841.003 on FAN1 from ME updated connector list.
0105: Update DQ15 AMD Fan1 Connector To 4 Pin P/N 20.F1621.004, AMD Different To Intel
Layout 15 mil
20.F1621.004
20.F1561.004
EMI/ESD
1122 Modify: AddR2806
Option 1: OTZ=95°C → ADJ=3.3V
Option 2: OTZ=85°C → ADJ=Floating
Option 3: OTZ=90°C → ADJ=GND
P2800EA1
P2800EB0
KBC
Note that R_up and R_down are optional for the purpose of circuit backward compatible with P2800EA1 designs. For new designs the two resistors can be replaced by short circuit whenever applicable
Note:
The original 0.1uF capacitor for P2800EA1 deisgn must be REMOVED on the ADJ pin of P2800EB0
1213 Modify: Remove Dimm Thermal Function
0107: Remove VGA P2800, SW Does Not Use

	Pin-1	Definition
P2793A	/FON	Low(<0.4V): VOUT =Vin and the fan is fully-on High(>1.6V): VOUT=1.6*VSET This pin is internal Pull-High with ~500K ohm
P2793B	EN	Low(<0.4): IC is shutdown. High(>1.6V): VOUT=1.6*VSET This pin is internal Pull-High with ~500K ohm

ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (v)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

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Title: Thermal/Fan Controllor EMC2102

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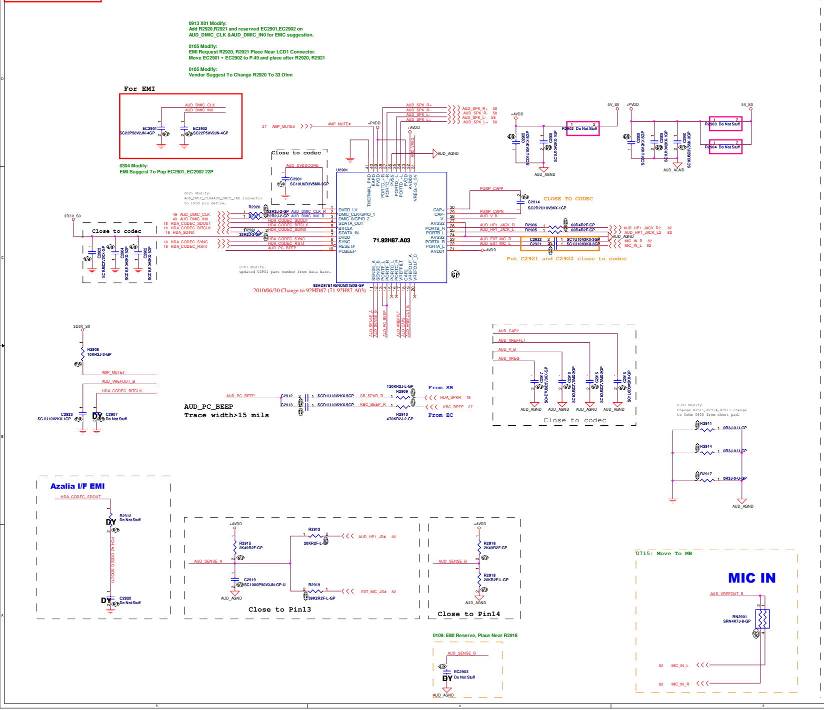
SSID = AUDIO

ANNIE Audio solution



Remove Annie Audio

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Title: Audio Codec 92HD79B1

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AUDIO OP AMPLIFIER

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Title: AMP

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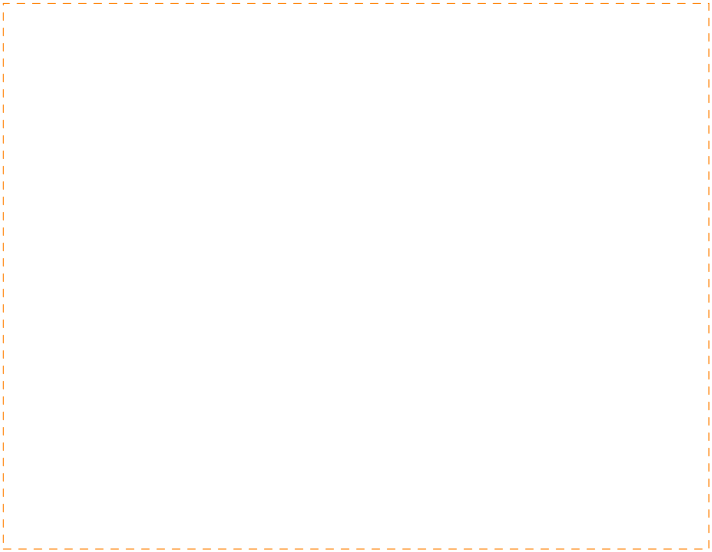
DG15 M12 In Daughter BD



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Title: LOM

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

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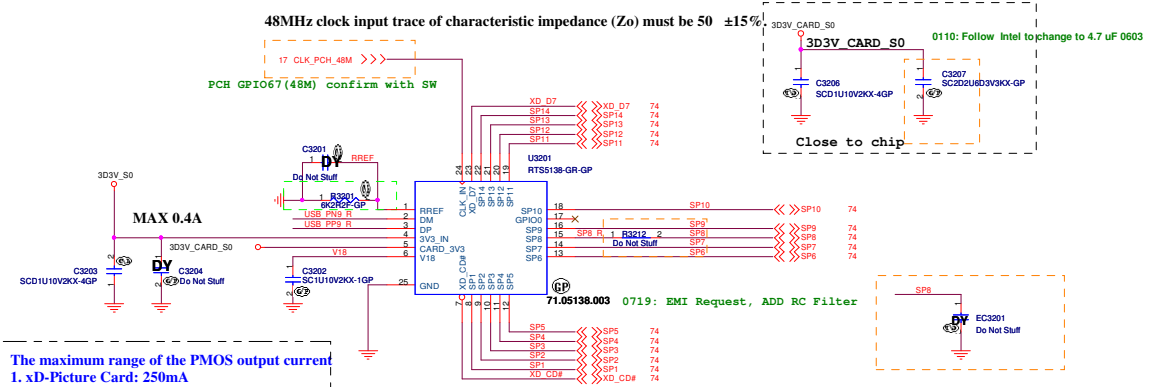
SSID = SDIO

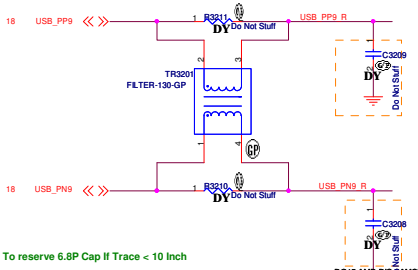
48MHz clock input trace of characteristic impedance (Zo) must be 50 ±15%



The maximum range of the PMOS output current
1. xD-Picture Card: 250mA
2. SD/MMC Card: 250mA
3. MS/MSPRO/Duo-HG: 250mA

The pin2 / pin3 (DM/DP) of RTS5138 chip trace layout with differential characteristic impedance (Zdiff) is 90Ω± 10%

POWER TRACE
1.RTS5138: pin 4 (3V3_IN) trace fixed width is 30 mils (minimum).
2.RTS5138: pin 5 (CARD_3V3) trace fixed width is 30 mils (minimum).
3.RTS5138: pin 6 (V18) trace fixed width is 12 mils (minimum).
Keep the trace routing lengths as short as possible.
4.RTS5138: pin 1(RREF) trace fixed width is 12 mils (minimum).
5.RTS5138: pin 1(RREF) trace must far away 48MHz clock trace.
6.De-coupling and Bulk capacitor should place near to RT5138 chip and Combo Socket.
7.It is recommended that use of ferrites bead on power trace.
8.Via size: Pad>=32 mils, Finished hole>=16 mils.



0103 Modify:
AMD Spec Update To reserve 6.8P Cap If Trace < 10 Inch
0118 Modify:
Change TR3201 To 69.10118.001 due to layout limitation

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Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

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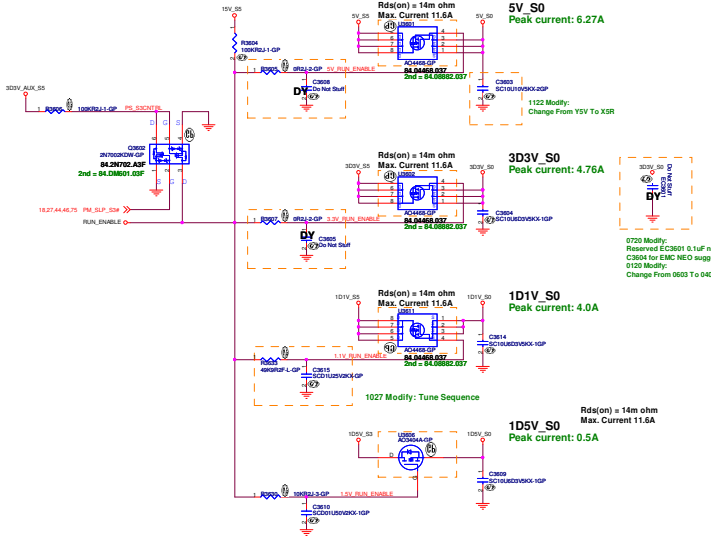
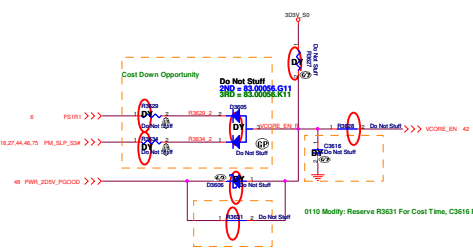
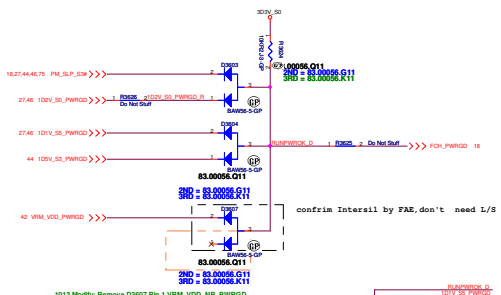
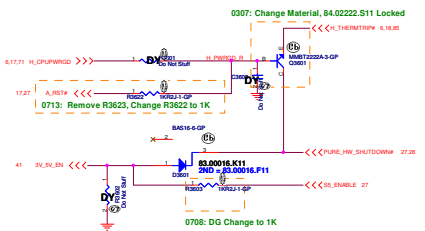
ROSA Run Power



Power Sequence







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Title: Power On Logic		
Size: Custom	Document Number: QUEEN AMD Muxless/UMA	Rev: X00
Date: Thursday, May 26, 2011	Sheet 36 of 104	

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Title

Power Plane Enable

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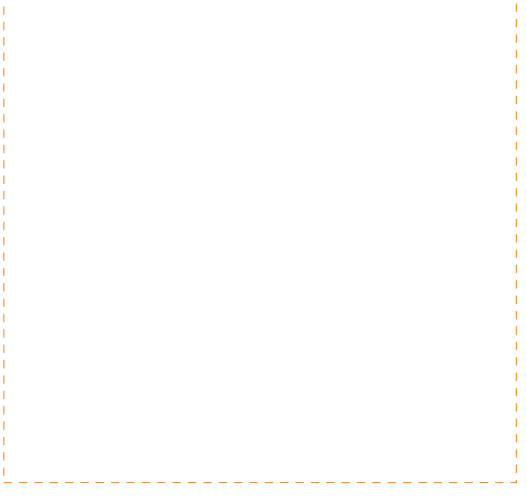
Move To CRT BD



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Title: DCIN_JACK

Size: Custom | Document Number: QUEEN AMD Muxless/UMA | Rev: 1.00

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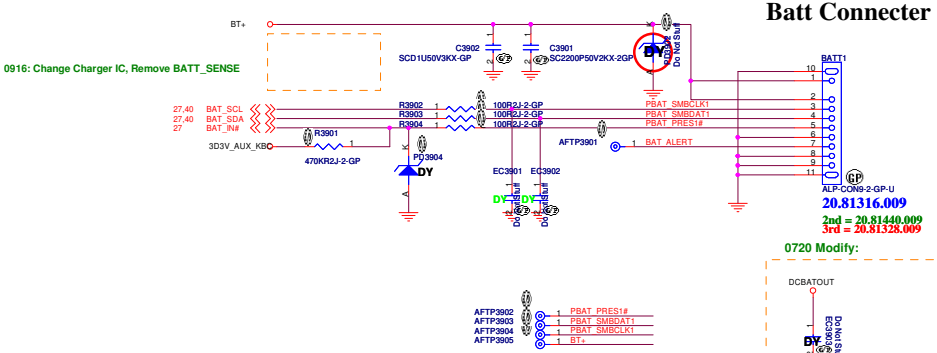
SSID = BATT CONN

Batt Connecter

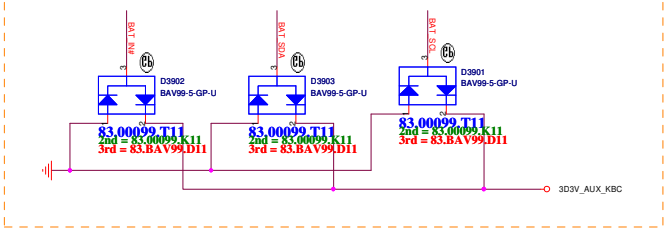


0720 Modify:

0719 Modify:
Reserved EC3903 0.1uF near EC3901 for EMC NEO suggestion.

For actual location, need to be swap all pin

Close to Batt Connector



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Title: BATT CONN

Size: A3 | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

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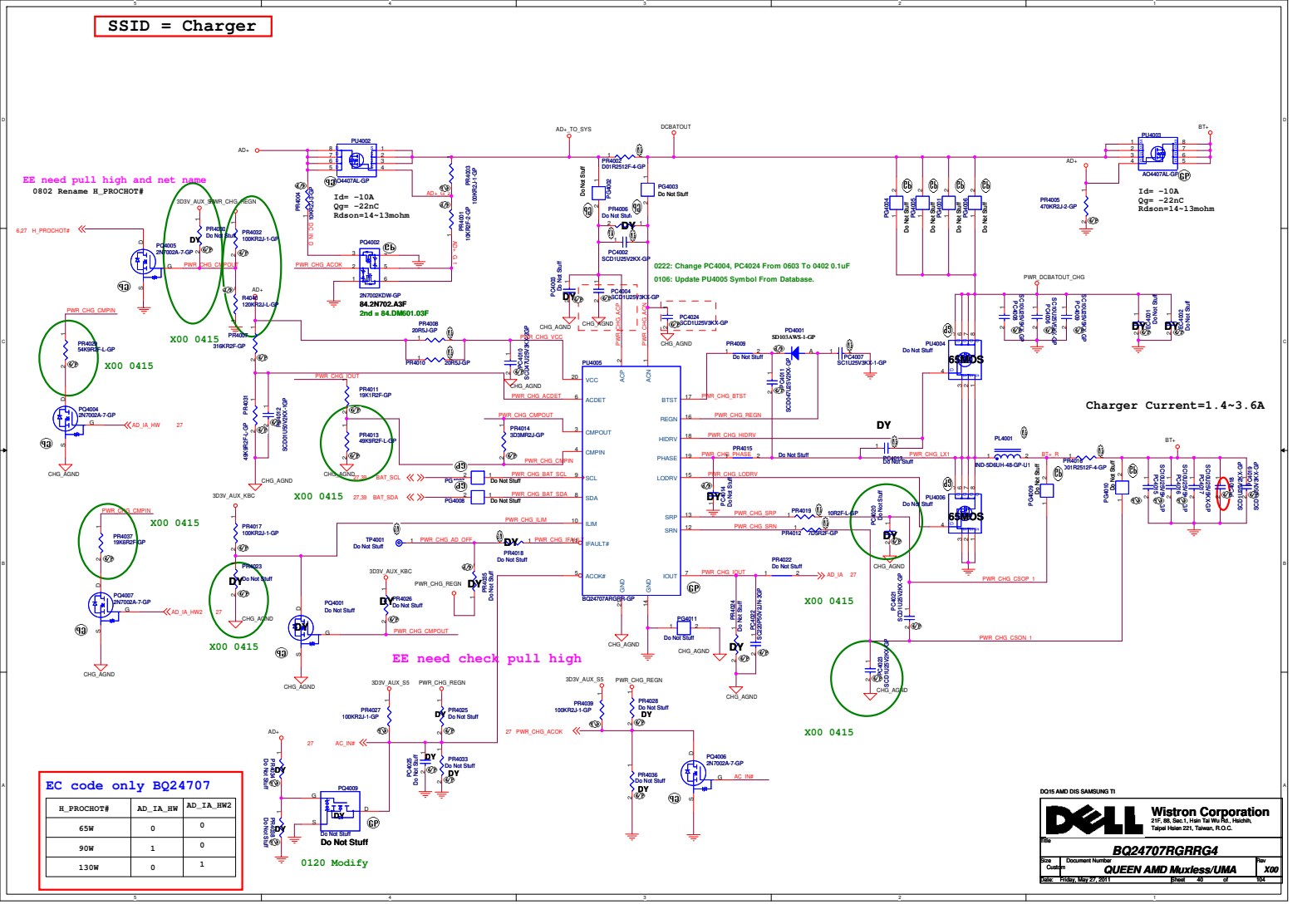
SSID = Charger
EE need pull high and net name
0802 Rename H_PROCHOT#
Id= -10A
Qg= -22nC
Rdson=14~13mohm
84.2N702.A3F
2nd = 84.DM601.03F
0222: Change PC4004, PC4024 From 0603 To 0402 0.1uF
0106: Update PU4005 Symbol From Database.
Charger Current=1.4~3.6A
X00 0415
EE need check pull high
EC code only BQ24707
H_PROCHOT# AD_IA_HW AD_IA_HW2
65W 0 0
90W 1 0
130W 0 1
0120 Modify
Do Not Stuff
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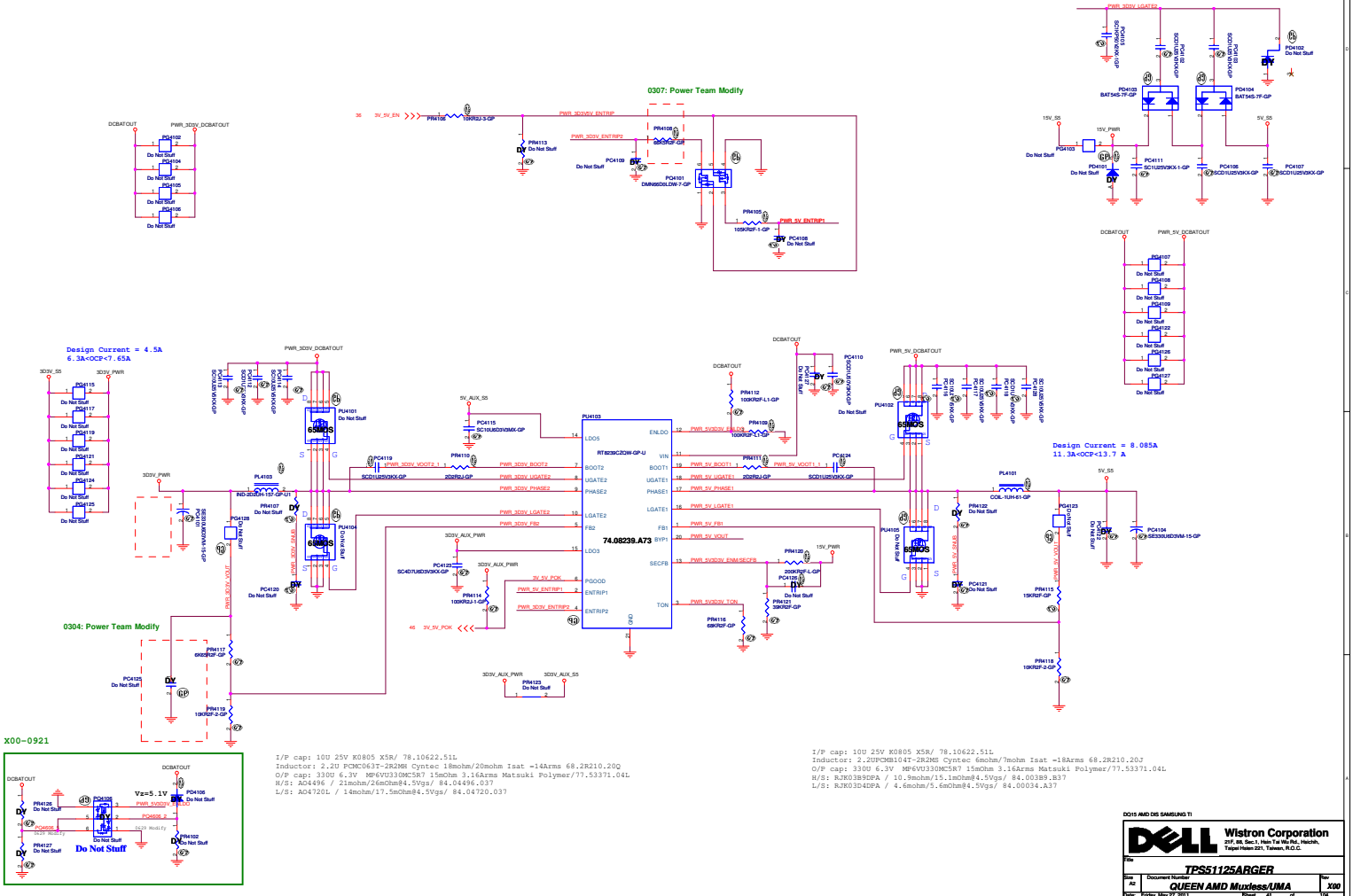
BQ24707RGRRG4
QUEEN AMD Muxless/UMA
X00
Friday, May 27, 2011

SSID = PWR.Plane.Regulator_3p3v5v



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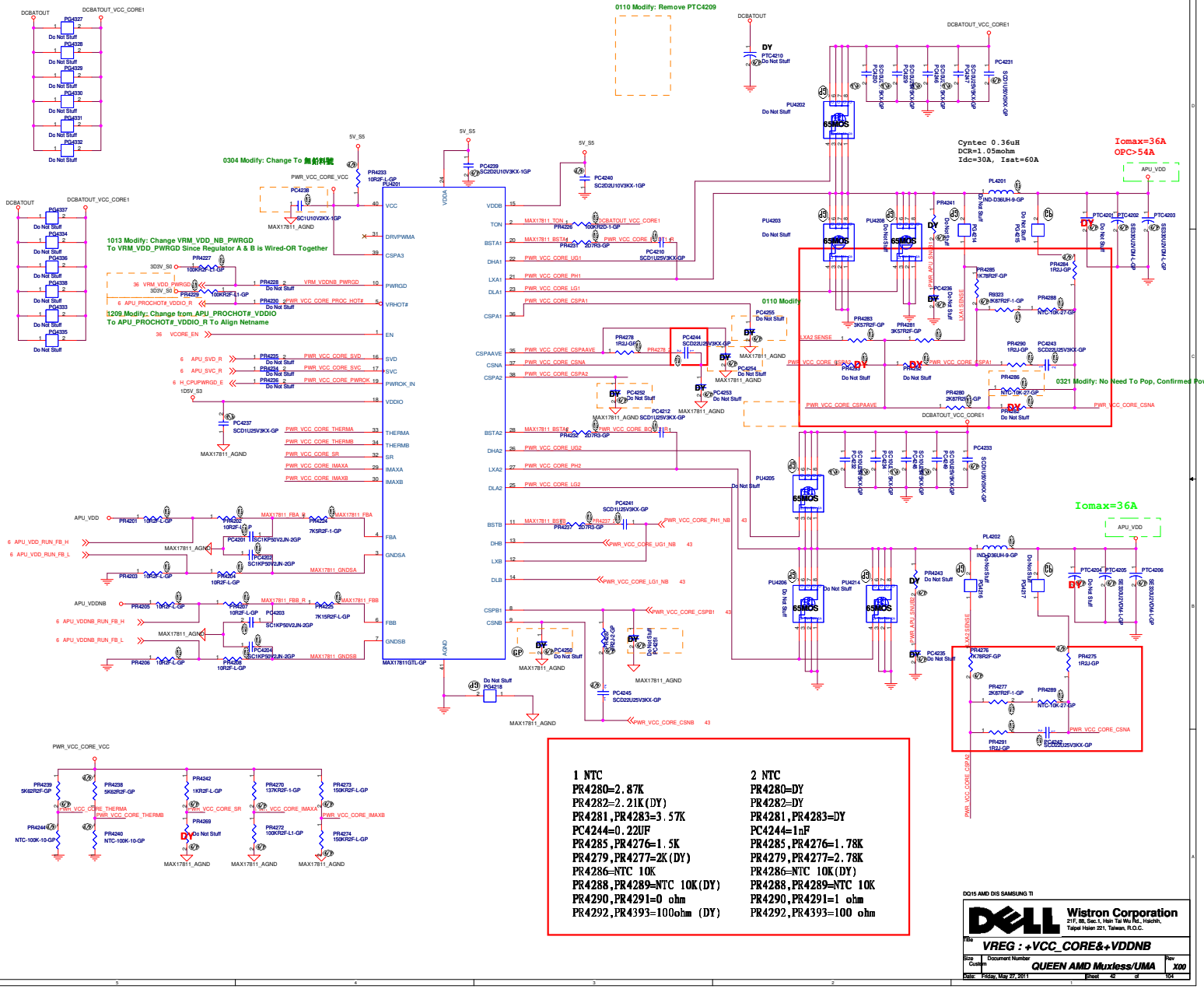
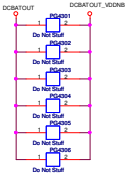
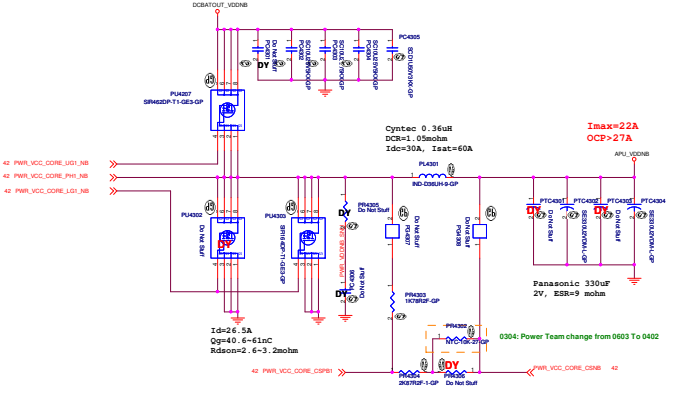
File: TPS51125ARGER

Size	Document Number	Rev
A0	QUEEN AMD Muxless/UMA	X00
Date: Friday, May 27, 2011	Sheet 43 of 56	


0110 Modify: Remove PTC4209
0304 Modify: Change To 無鉛料號
1013 Modify: Change VRM_VDD_NB_PWRGD
To VRM_VDD_PWRGD Since Regulator A & B is Wired-OR Together
1209 Modify: Change from APU_PROCHOT# VDDIO
To APU_PROCHOT# VDDIO_R To Align Netname
0110 Modify
0321 Modify: No Need To Pop, Confirmed Power
Cyntec 0.36uH
DCR=1.05mohm
Idc=30A, Isat=60A
Iomax=36A
OPC>54A
Iomax=36A
MAX17811GTL-GP
1 NTC
PR4280=2.87K
PR4282=2.21K(DY)
PR4281,PR4283=3.57K
PC4244=0.22UF
PR4285,PR4276=1.5K
PR4279,PR4277=2K(DY)
PR4286=NTC 10K
PR4288,PR4289=NTC 10K(DY)
PR4290,PR4291=0 ohm
PR4292,PR4393=100ohm (DY)
2 NTC
PR4280=DY
PR4282=DY
PR4281,PR4283=DY
PR4244=1nF
PR4285,PR4276=1.78K
PR4279,PR4277=2.78K
PR4286=NTC 10K(DY)
PR4288,PR4289=NTC 10K
PR4290,PR4291=1 ohm
PR4292,PR4393=100 ohm
DQ15 AMD DIS SAMSUNG TI
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
VREG : +VCC_CORE&+VDDNB
QUEEN AMD Muxless/UMA
X00
Friday, May 27, 2011
42
104





DC15 AMD DIS SAMSUNG TI

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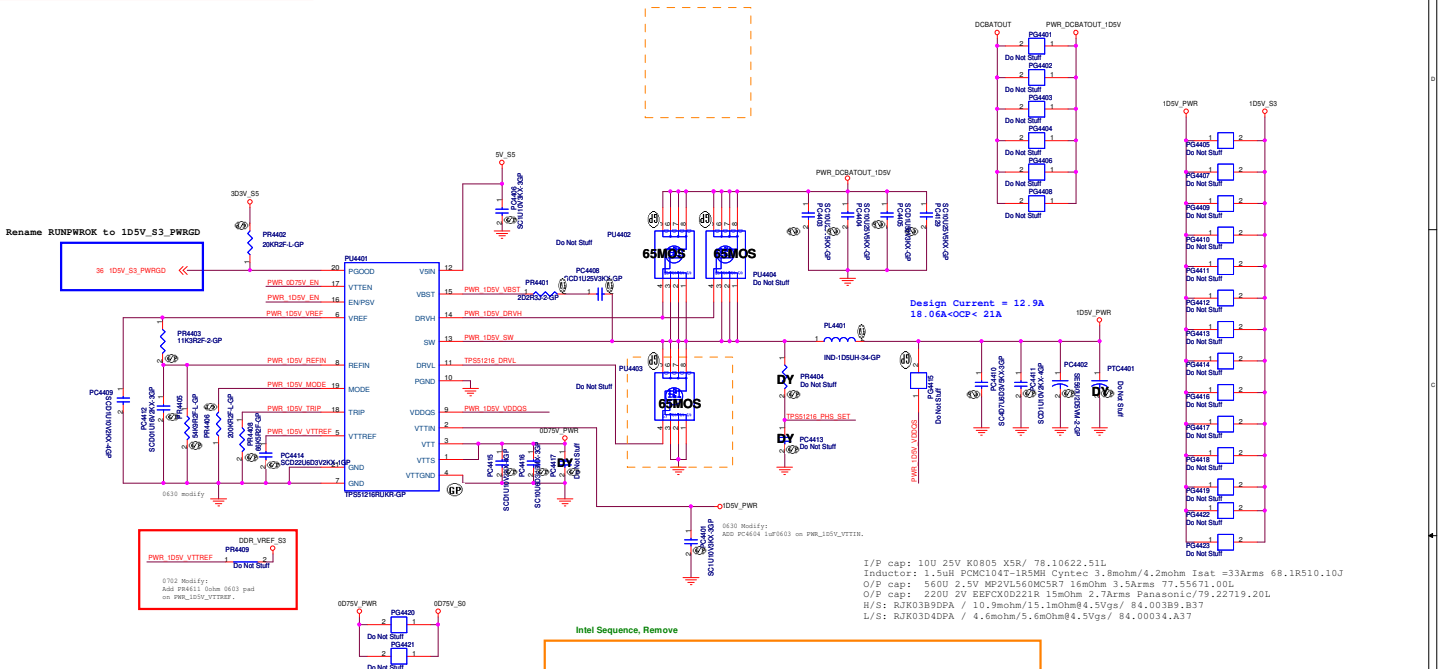
Taipei Hsien 221, Taiwan, R.O.C.

File: VDDNB

Size	Document Number	Rev
A0	QUEEN AMD Muxless/UMA	X00
Date: Thursday, May 26, 2011	Sheet 43 of 55	

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4406	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

DQ15 AMD DIS SAMSUNG TI

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Title: TPS51216 1D5V S3

Size: Custom | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Friday, May 27, 2011 | Sheet 44 of 104

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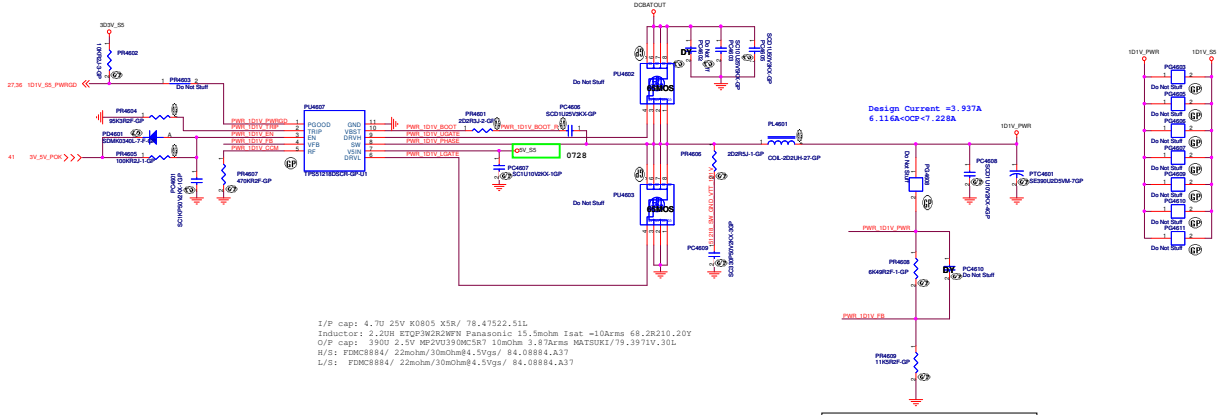
File

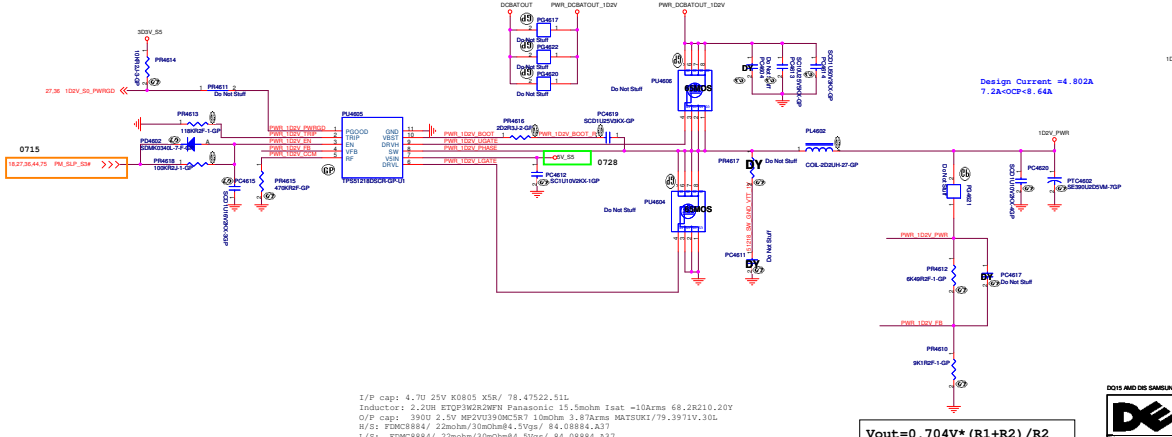
VDDR & VDDP

Size	Document Number	Rev
A0		QUEEN AMD Muxless/UMA X00

Date: Thursday, May 26, 2011 Sheet 45 of 105

SSID = PWR.Plane.Regulator_1D1V_S5





DQ15 AMD DIS SAMSUNG TI

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File: VDDR & VDDP

Size	Document Number	Rev
A0	QUEEN AMD Muxless/UMA X00	

Date: Friday, May 27, 2011 Sheet 46 of 105

DC15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

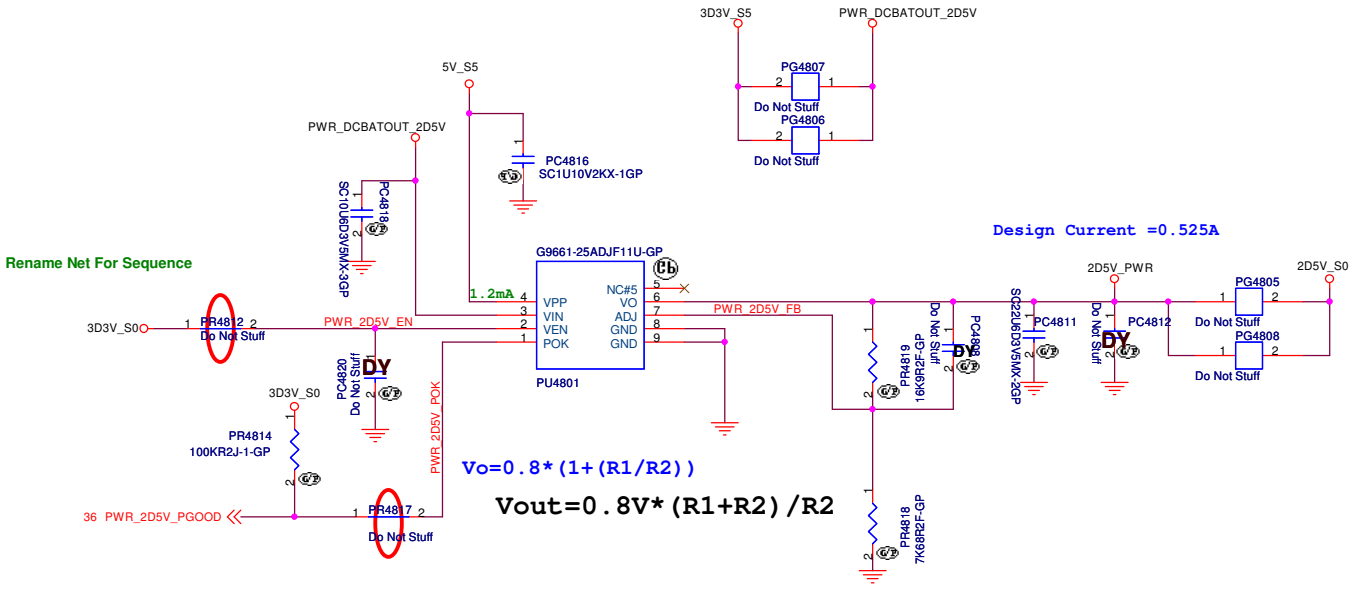
Reserved

Size	Document Number	Rev
A2	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 47 of 124

SSID = PWR.Plane.Regulator_2p5v VGA 1V

G9661 for 2D5V_S0



DQ15 AMD DIS SAMSUNG TI

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 2D5V_S0		
Size: A4	Document Number: QUEEN AMD Muxless/UMA	Rev: X00
Date: Thursday, May 26, 2011	Sheet 48 of 104	

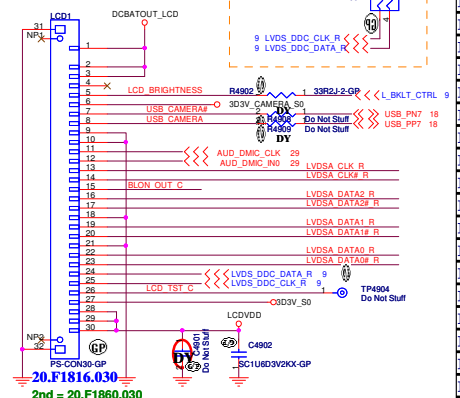
SSID = VIDEO

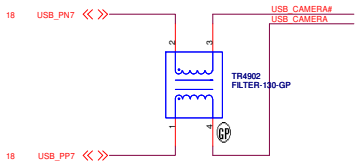
0909 X01 Modify:
Change LCD1 to 20.F1816.030 for 30pin
Re-assign LCD1 pin define base on Roy updated cable pin define list.

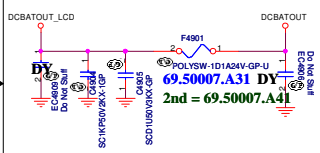
0921Modify:
Change BLON_OUT_C to pin 15 and pin 4 to NC on LCD1.

0914 Modify:
Change PU From Page 82 To Page 49

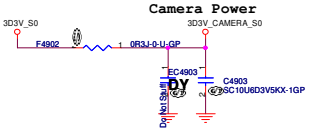
LVDS CONNECTOR





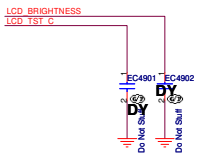


Camera Power



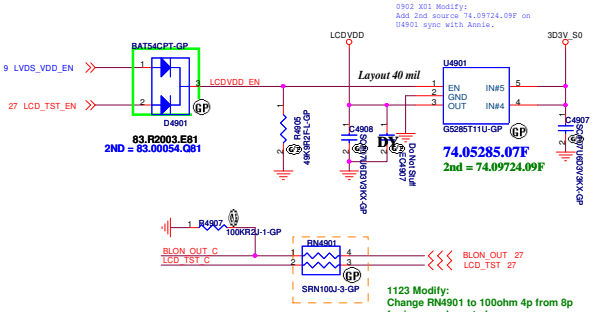
(MB Pin Define)	
MB CONN. (WIRE)	
Pin 1	DCBATOUT_LCD
Pin 2	DCBATOUT_LCD
Pin 3	DCBATOUT_LCD
Pin 4	BLON_OUT_C
Pin 5	LCD_BRIGHTNESS
Pin 6	3D3V_CAMERA_S0
Pin 7	USB_CAMERA#
Pin 8	USB_CAMERA
Pin 9	GND
Pin 10	GND
Pin 11	AUD_DMIC_CLK
Pin 12	AUD_DMIC_IN0
Pin 13	LVDSA_CLK
Pin 14	LVDSA_CLK#
Pin 15	LCD_DET_G
Pin 16	LVDSA_DATA2
Pin 17	LVDSA_DATA2#
Pin 18	GND
Pin 19	LVDSA_DATA1
Pin 20	LVDSA_DATA1#
Pin 21	GND
Pin 22	LVDSA_DATA0
Pin 23	LVDSA_DATA0#
Pin 24	LVDS_DDC_DATA_R
Pin 25	LVDS_DDC_CLK_R
Pin 26	LCD_TST_C
Pin 27	3D3V_S0
Pin 28	LCDVDD
Pin 29	LCDVDD
Pin 30	LCDVDD

For EMI request
Close to LVDS connector

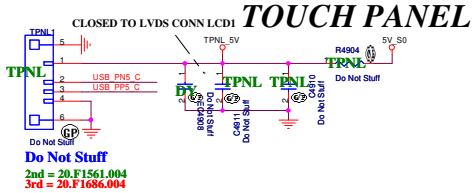


SSID = VIDEO

LCD POWER for ROSA

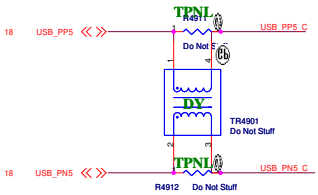


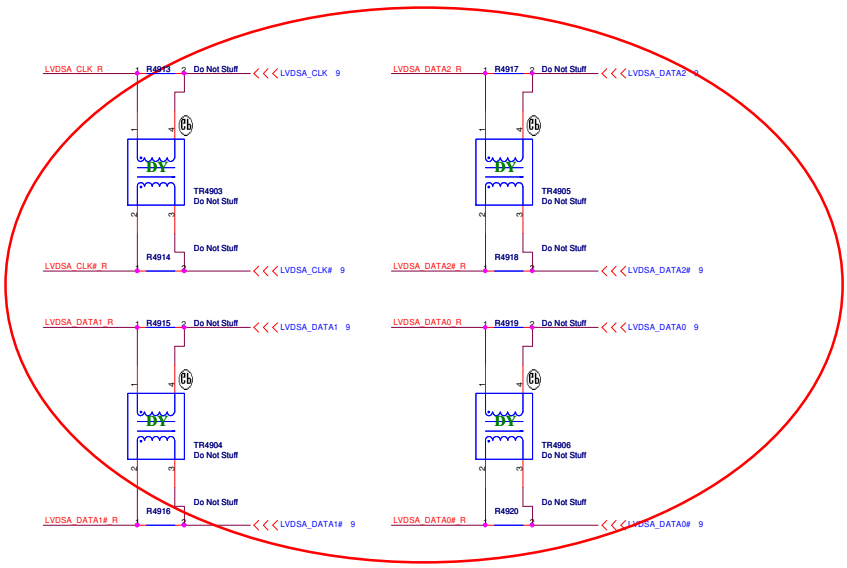
TOUCH PANEL



0909 Modify:
Add TPNL1 for touch panel solution 4pin connector.

0928 Modify:
Change To 20.F1621.004 on TPNL1 from updated connector list.





DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

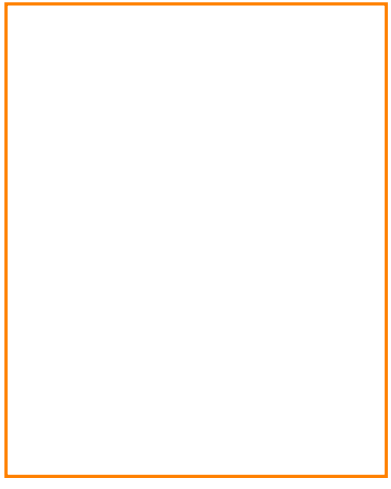
Size: Custom | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Thursday, April 21, 2011 | Sheet 49 of 104

Remove For M12 Spec & Put In Daughter BD

Remove For M12 Spec & Put In Daughter BD

Remove For M12 Spec & Put In Daughter BD



DQ15 AMD DIS SAMSUNG TI

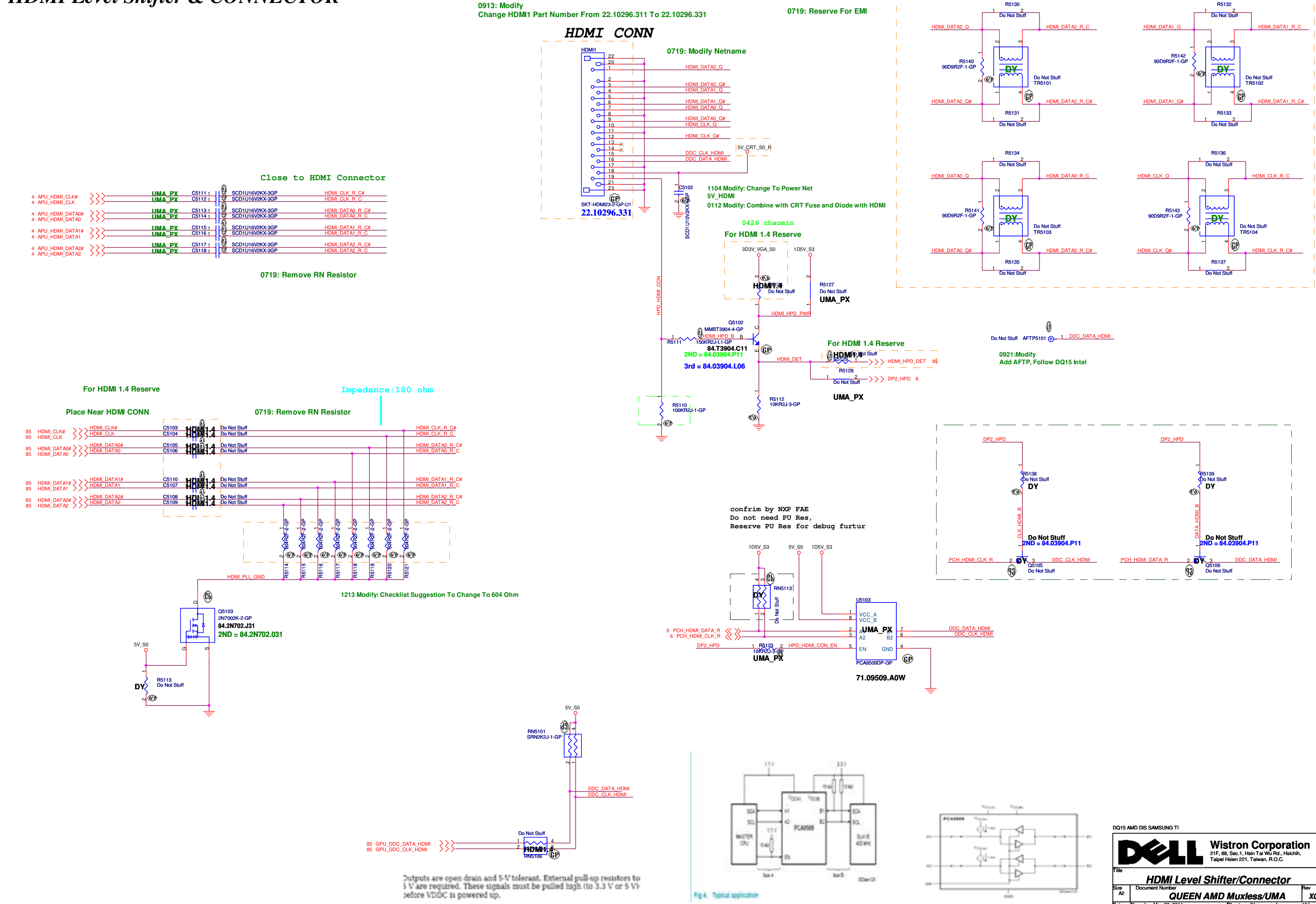
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Board Connector

Size: Custom | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Thursday, May 26, 2011 | Sheet 50 of 104

HDMI Level Shifter & CONNECTOR



DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	HDMI Level Shifter/Connector
Size	A2
Document Number	QUEEN AMD Muxless/UMA
Rev	X00
Date:	Thursday, May 26, 2011
Sheet	51 of 104

Remove EDP

LCD POWER CIRCUIT

Remove EDP

Rosa team

Remove EDP

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: eDP		
Size: Custom	Document Number: QUEEN AMD Muxless/UMA	Rev: 1.00
Date: Thursday, May 26, 2011	Sheet 52 of 104	

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	*QUEEN AMD Muxless/UMA*	00

Date: Thursday, May 26, 2011 Sheet 53 of 104

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

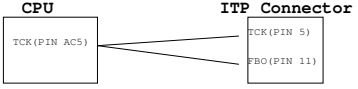
Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	A00

Date: Thursday, May 26, 2011 Sheet 54 of 104

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



DQ15 AMD DIS SAMSUNG TI

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

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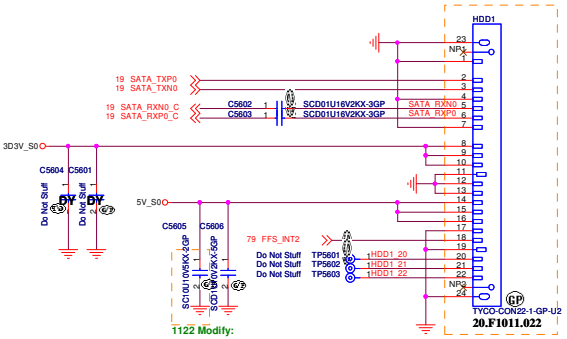
SSID = SATA

SATA HDD Connector



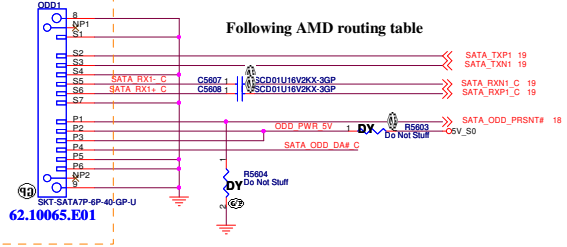
1122 Modify:
Change From Y5V To X5R

0614 Modify:
Change HDD1 connector part number to
20.F1011.022 base on ME EMN and DXF.

ODD Connector

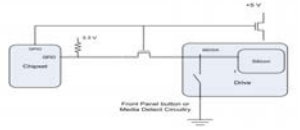
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

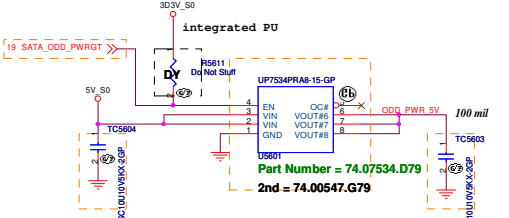
SUPPORT ZERO SATA ODD



0914 Modify:
Change ODD Part number From 22.10300.421 To 62.10065.E01

When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

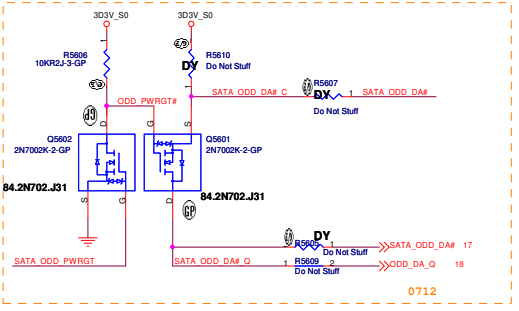




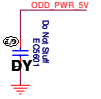
Current limit
Active High
typ =>2.5A

1122 Modify:
Change From Y5V To X5R

0719: Modify Zero ODD Circuit



0109: EMI Request.



DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

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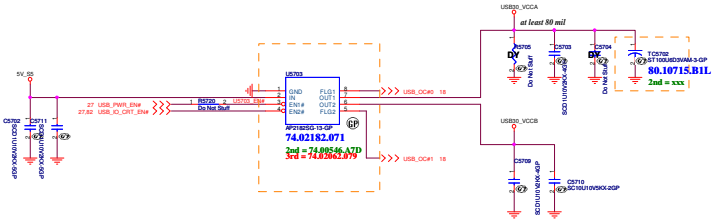
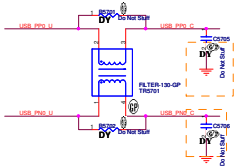
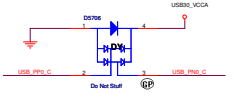
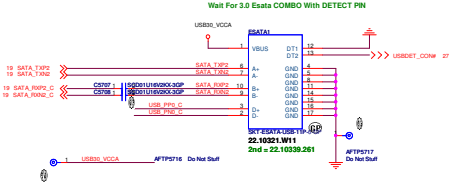


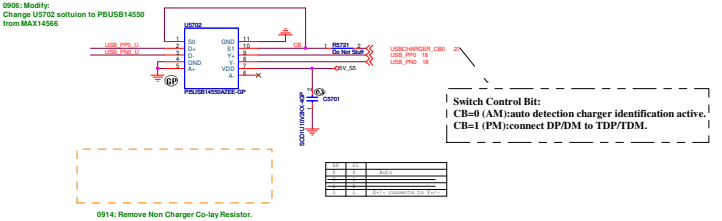
0101: Change ESATA1 To 22.10290.271







USB CHARGER



DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ESATA/USB Charger

Size	Document Number	Rev
A0	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 28, 2009 Sheet 57 of 104

SSID = AUDIO

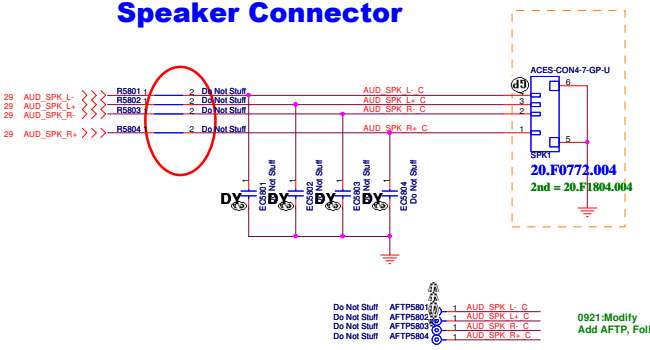
0715 Modify:
Change EC5801~EC5804 to 100p 0402
and default un-stuff.
Add R5801~R5804 between SPK signal and connector
for EMC NEO suggest.

0914 Modify:
Change SPK1 to 20.F0772.004 from
20.F1647.004 from Double updated.

0921 Modify:
Modify Pin Define Base On DQ15 Intel

1110 X02 Modify:
Add 2nd 20.F1804.004 on SPK1 from
ME updated connector list.

Speaker Connector



MB CONN. (WIRE)	
Pin 4	AUD_SPK_L-C
Pin 3	AUD_SPK_L+C
Pin 2	AUD_SPK_R-C
Pin 1	AUD_SPK_R+C

0921:Modify
Add AFTP, Follow DQ15 Intel

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 58 of 104

LAN CONN In Daugthter BD

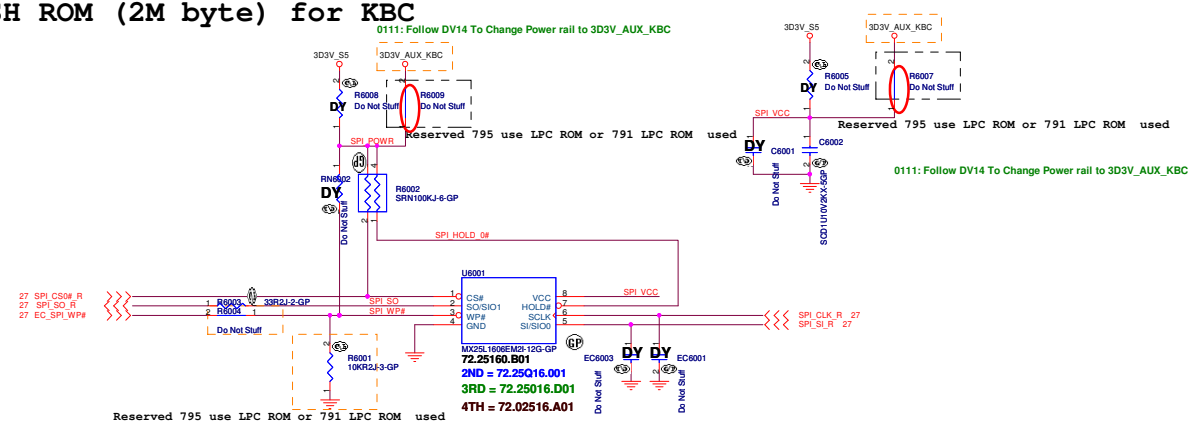
DQ15 AMD DIS SAMSUNG TI

DELL	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LAN CONN	
Size A3	Document Number QUEEN AMD Muxless/UMA	Rev 1.00
Date: Thursday, May 26, 2011	Sheet 59 of 104	

SSID = Flash.ROM

SPI FLASH ROM (2M byte) for KBC

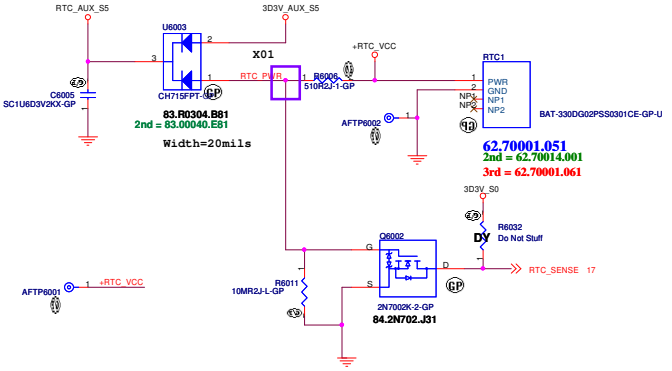
0111: Follow DV14 To Change Power rail to 3D3V_AUX_KBC



Reserved 795 use LPC ROM or 791 LPC ROM used

0111: Follow DV14 To Change Power rail to 3D3V_AUX_KBC

SSID = RBATT



0105 Modify:
updated RTC1 symbol and footprint from data base.
1122 Modify:
Add Q6002, R6010, R6011 for FACTORY RTC detect function.

0111: Change RTC Schematic As DV14 Brazo, SW Suggest.

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 60 of 104

SSID = USB

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

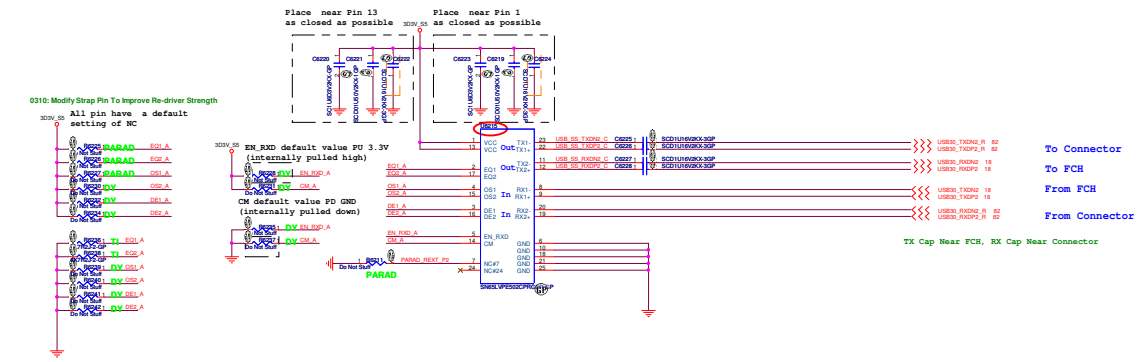
Title: USB Power SW

Size | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Thursday, May 26, 2011 | Sheet 61 of 104

1222 Modify:
C6222,C6224, C6231, C6234 Change Y5V To X7R

0916: Move From IO Board To Main Board

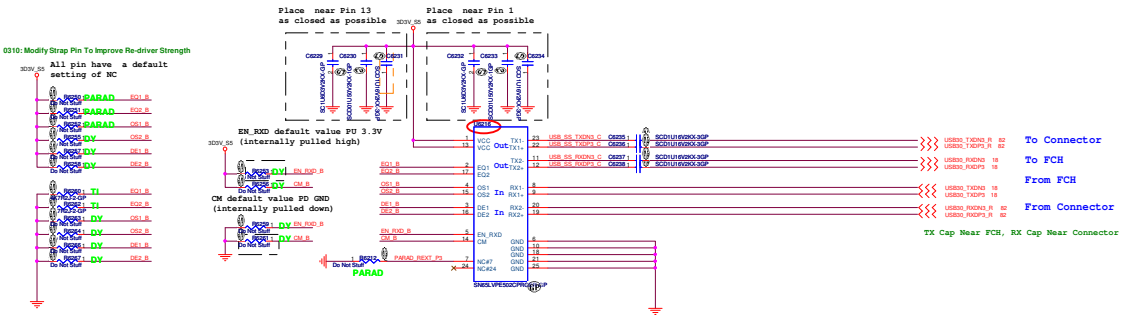


DUMMY NAME CONFIGURATION
TI = TI 502R Need Pop
PARAD_ALL = For Both PARAD I2C Mode & Normal MODE
PARAD_I2C = Parad I2C Mode
TI_PARAD= Both TI & PARAD Normal Mode

Pin5 EN_RX_A = Parade = DUMMY
Pin14 CM_A = Parade = Default DUMMY (PU)
Pin2 EQ1 = Parad B_EQ0 = Default DUMMY (PU)
Pin17 EQ2 = Parad A_EQ0 = Default DUMMY (PU)
Pin4 OS1 = Parad B_EQ1 = Default DUMMY (PU)
Pin15 OS2 = Parad A_EQ1 = Default DUMMY (PU)
Pin3 DE1 = Parad B_DE0 = Default Pull High
PIN16 DE2 = Parad A_DE0 = Default Pull High
GND6 = Parad B_DE1 = Default Pull High
GND18= Parad A_DE1 = Default Pull High

Parad I2C Mode:
PIN3 DE1 = Parad I2C_ADDR0 = Default DUMMY (PU)
PIN4 OS1 = Parad I2C_ADDR1 = Default DUMMY (PU)

Parad I2C Mode:
PIN15 OS2 = Parad I2C = SDA_CTL (DATA)
PIN16 DE = Parad I2C = SCL_CTL (CLK)



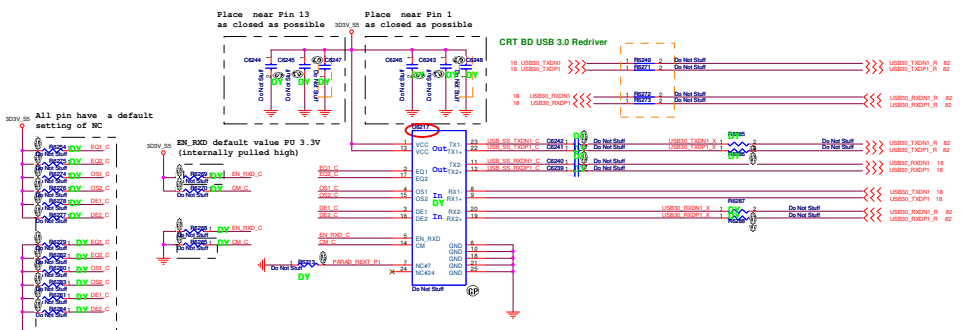
DUMMY NAME CONFIGURATION
TI = TI 502R Need Pop
PARAD_ALL = For Both PARAD I2C Mode & Normal MODE
PARAD_I2C = Parad I2C Mode
TI_PARAD= Both TI & PARAD Normal Mode

Pin5 EN_RX_A = Parade = DUMMY
Pin14 CM_A = Parade = Default DUMMY (PU)
Pin2 EQ1 = Parad B_EQ0 = Default DUMMY (PU)
Pin17 EQ2 = Parad A_EQ0 = Default DUMMY (PU)
Pin4 OS1 = Parad B_EQ1 = Default DUMMY (PU)
Pin15 OS2 = Parad A_EQ1 = Default DUMMY (PU)
Pin3 DE1 = Parad B_DE0 = Default Pull High
PIN16 DE2 = Parad A_DE0 = Default Pull High
GND6 = Parad B_DE1 = Default Pull High
GND18= Parad A_DE1 = Default Pull High

Parad I2C Mode:
PIN15 OS2 = Parad I2C = SDA_CTL (DATA)
PIN16 DE = Parad I2C = SCL_CTL (CLK)

Parad I2C Mode:
PIN3 DE1 = Parad I2C_ADDR0 = Default DUMMY (PU)
PIN4 OS1 = Parad I2C_ADDR1 = Default DUMMY (PU)

0113: CRT BD Redriver



Eng stuff 20.K0216.024 Pin1 -> left side
PD change to 20.K0276.024 Pin1 -> left side
so do not swap net

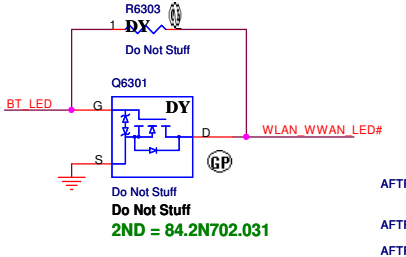
DC15 AMD DIS SAMSUNG TI

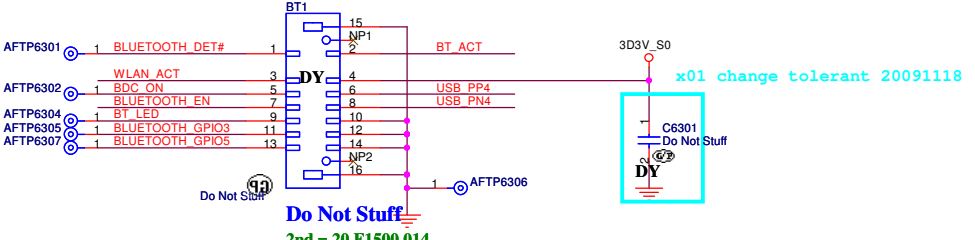
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

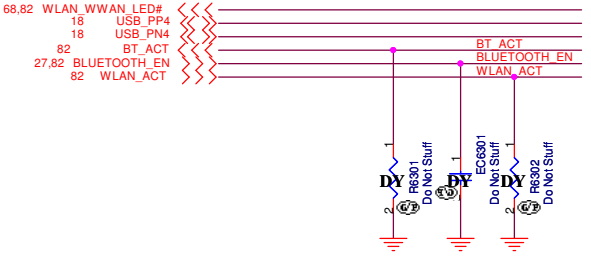
Title: USB 3.0
Size: Custom
Document Number: QUEEN AMD Muxless/UMA
Rev: X00
Date: Friday, May 27, 2011
Sheet 50 of 58

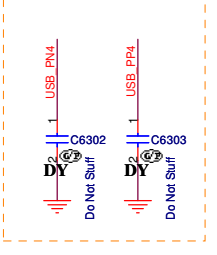
SSID = User.Interface

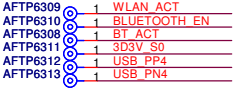
Bluetooth Module conn.











0906 Modify:
Dell Peter already confirmed DQ15 and DN15 will not support Bluetooth BT365, only support combo Wirless+BT. Please DUMMY Bluetooth connector(BT1) and stand off (HBT1) and related components.

0103 Modify:
AMD Spec Update To reserve 6.8P Cap If Trace < 10 Inch

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
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Title: Bluetooth

Size: A4 | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

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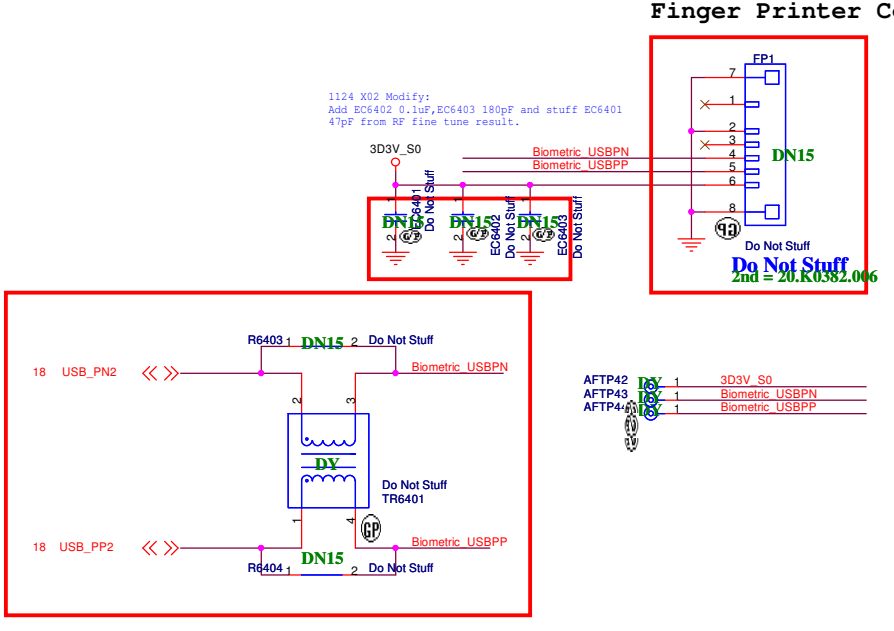
Finger Printer Connector



MB CONN.(FFC)	
Pin1	NC
Pin2	GND
Pin3	NC
Pin4	Biometric_USBPN
Pin5	Biometric_USBPP
Pin6	3D3V_S0

DQ15 AMD DIS SAMSUNG TI

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Title: F/P

Size: A4 | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Thursday, May 26, 2011 | Sheet 64 of 104

WLAN CONN In Daugthter BD

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Title: WLAN

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	00

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Remove For DG12 M12 SPEC

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Title: WWAN

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 66 of 104

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DQ15 AMD DIS SAMSUNG TI

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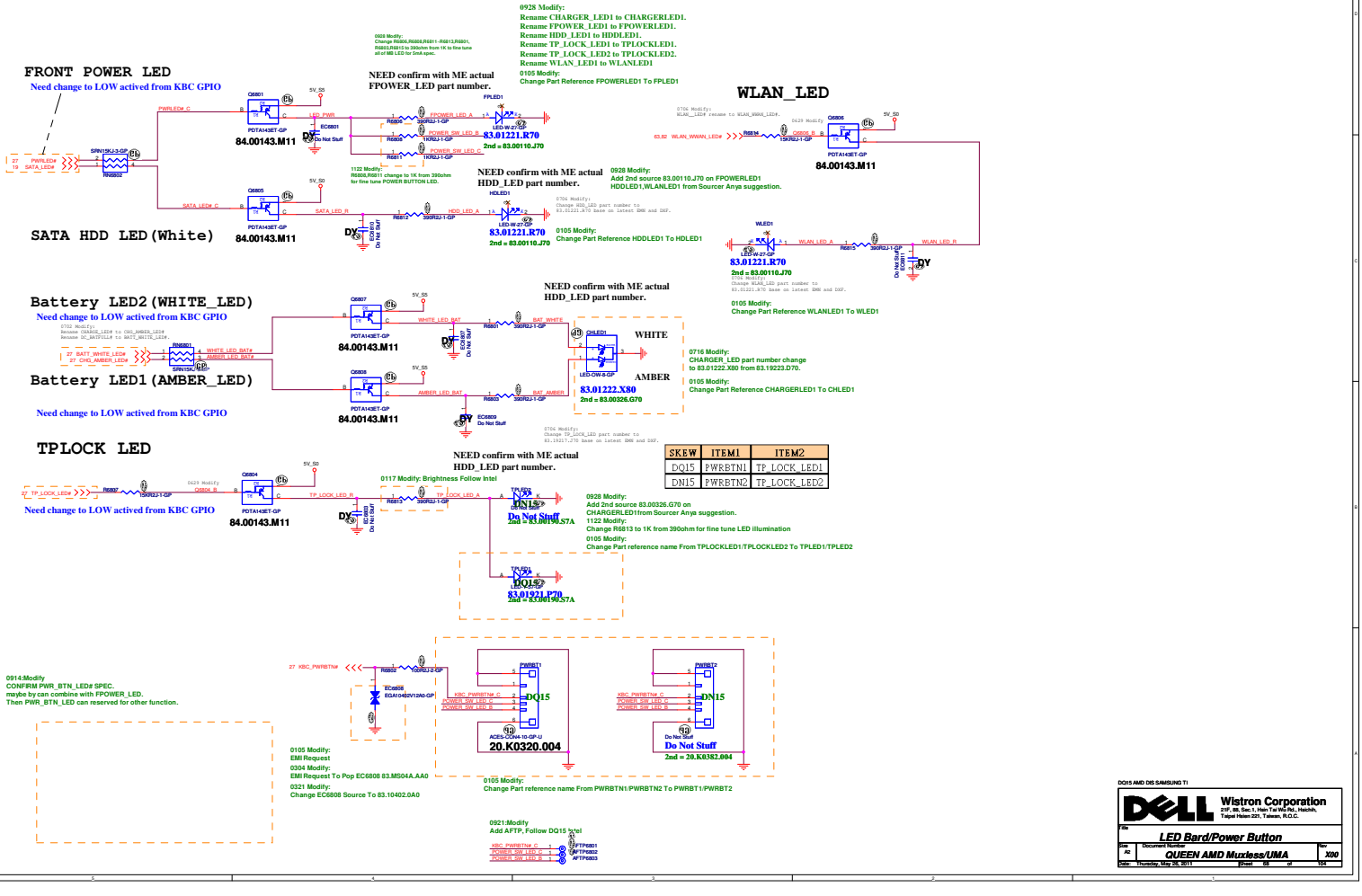
Title: *Reserved*

Size	Document Number	Rev
A3	*QUEEN AMD Muxless/UMA*	*X00*

Date: Thursday, May 26, 2011 Sheet 67 of 104

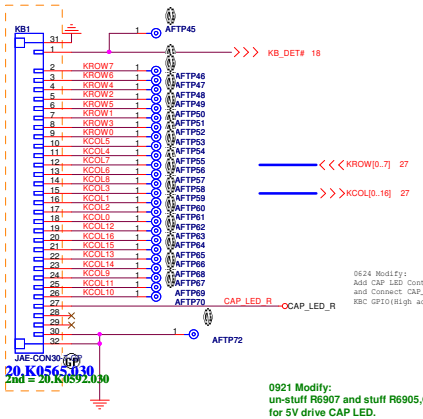
SSID = User.Interface



1122 Modify:
Add 2nd 20.K0592.030 on KB1 from ME
updated connector list.

Internal KeyBoard Connector

0630 Modify:
Change KB1 part number to 20.K0565.030
base on ME updated EMN and DXF.



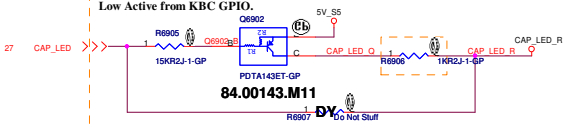
20.K0565.030
2nd = 20.K0592.030

0624 Modify:
Add CAP LED Control circuit(Q6902,R6906,R6907)
and Connect CAP_LED_R control to KB1 pin27 from
KBC GPIO(High active).

0921 Modify:
un-stuff R6907 and stuff R6905,Q6902,R6906
for 5V drive CAP LED.
0109 Modify: CAP_LED Change To Low Active From KBC GPIO
0109 Modify: R6906 Change To 1K

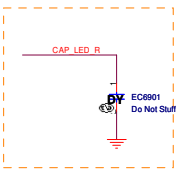
CAP LED CONTROL

Low Active from KBC GPIO.



84.00143.M11

0719: EMI Request



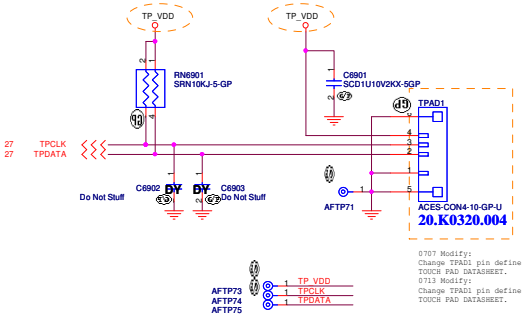
SSID = Touch.Pad

0624 Modify:
Removed TP_LOCKED CONTROL combin
with KEYBOARD Function KEY.

0713 Modify:
Change TPAD1 power source to 3D3V_S0 from
5V_S0 base on DELL latest spec A02.

TouchPad Connector

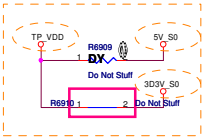
0630 Modify:
Change TPAD1 part number to 20.K0320.006
base on ME updated EMN&DXF.
0712 Modify:
Change TPAD1 part number to 20.K0320.004
from 20.K0320.006.



MB CONN.	(FFC)
Pin 4	TP_VDD
Pin 3	TPCLK
Pin 2	TPDATA
Pin 1	GND

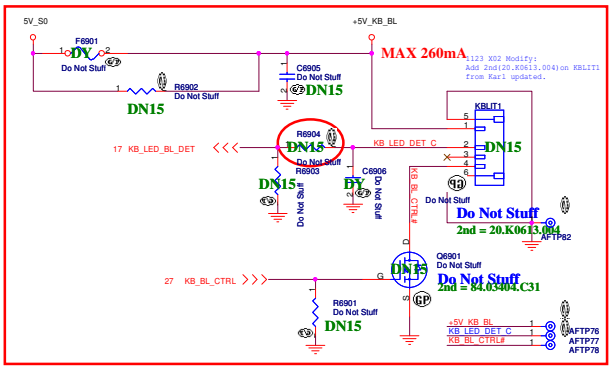
0707 Modify:
Change TPAD1 pin define to follow
TOUCH PAD DATASHEET.
0713 Modify:
Change TPAD1 pin define to follow
TOUCH PAD DATASHEET.

0715 Modify:
Add R6908,R6909 for TPAD1 co-lay power option.
0109 Modify:
Change TP_VDD To 3D3V_S0, Follow Intel



MB CONN. (FFC)	
Pin 1	+5V_KB_BL
Pin2	KB_LED_DET_C
Pin3	NC
Pin4	KB_BL_CTRL#

KB Backlight Connector



DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

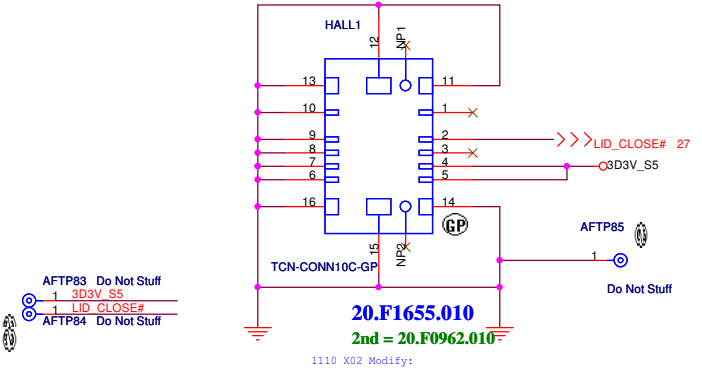
Size	Document Number	Rev
Custom	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 69 of 104

SSID = Hall.Sensor

0906 Modify:
HALL SENSOR move to small board at X01 stage,so Removed HALLSW1 related circuit and add HALL1 connector.

1122 Modify:
Add 2nd 20.F0962.010 on HALL1 from ME updated connector list.



DQ15 AMD DIS SAMSUNG TI

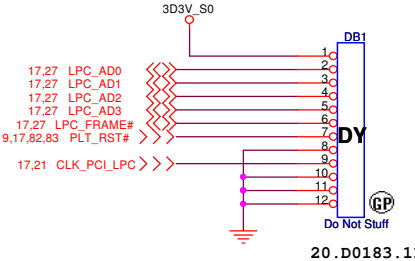
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Hall Effect Sensor

Size	Document Number	Rev
A4	QUEEN AMD Muxless/UMA	X00

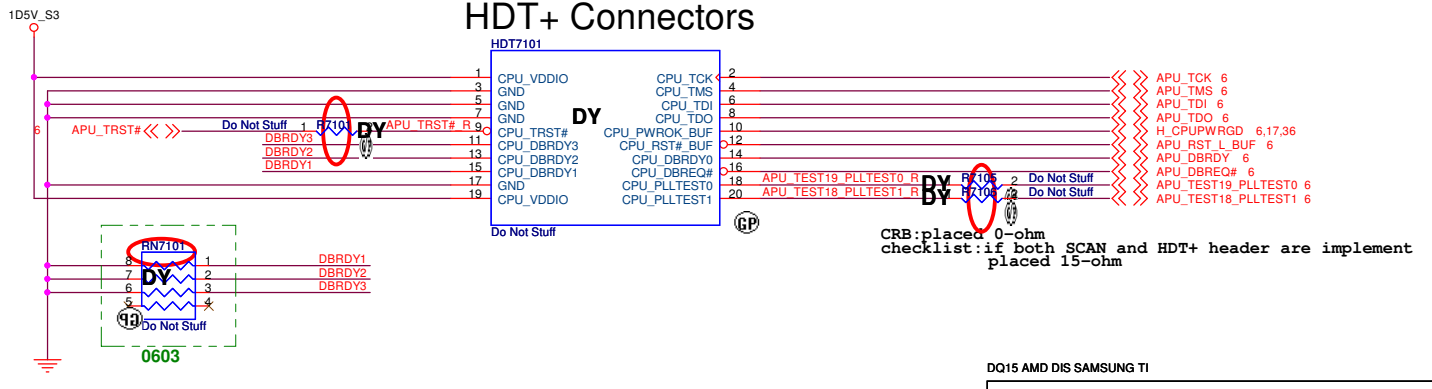
Date: Thursday, May 26, 2011 Sheet 70 of 104

SSID = Debug



20.D0183.110

HDT+ Connectors



CRB:placed 0-ohm
checklist:if both SCAN and HDT+ header are implement
placed 15-ohm

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Title: Dubug connector

Size	Document Number	Rev
A4	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 71 of 104

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DQ15 AMD DIS SAMSUNG TI

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Title: RESERVED

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 72 of 104

DQ15 AMD DIS SAMSUNG TI

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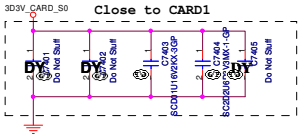
Title

Reserved

Size	Document Number	Rev
A3	*QUEEN AMD Muxless/UMA*	*X00*

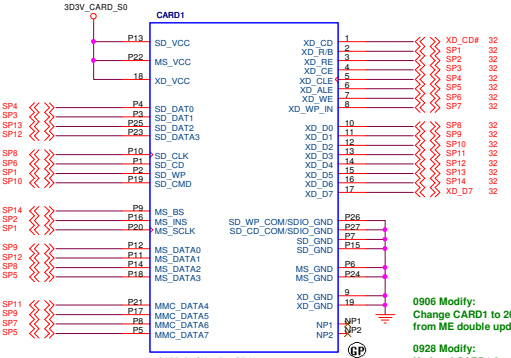
Date: Thursday, May 26, 2011 Sheet 73 of 104

SSID = SDIO



SD/XD/MS/MMC+ Card Reader

	WP	CD	GND
WITHOUT CARD			
CARD INSERTED WP-SW:LOCK			
CARD INSERTED WP-SW:UNLOCK			



20.I0129.001

2nd = 20.I0135.001

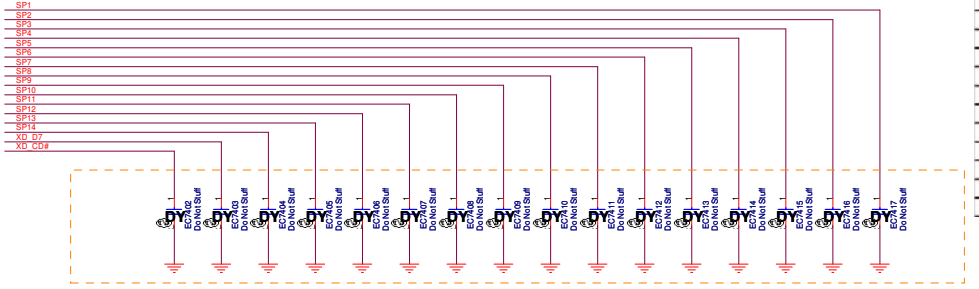
PCB Footprint = R013-P12-HM-1

0906 Modify:
Change CARD1 to 20.I0129.001 from 62.10051.931 from ME double updated latest DXF&EMN on X01.

0928 Modify:
Updated CARD1 footprint to R013-P12-HM-1 from data base updated footprint.

1122 Modify:
Add 2nd 20.I0135.001 on CARD1 from ME updated latest connector list.

For EMI Reserved



0913: Schematic Score Card Suggest Cap Less Than 10P

20.I0129.001			
PIN	TYPE	FUNCTION	RTS5138 NET
P1	SD	SD-CD	SP6
P2	SD	SD-WP	SP1
P3	SD	SD-DAT1	SP3
P4	SD	SD-DAT0	SP4
P5	MMC_PLUS	MMC-DATA7	SP5
P6	MemoryStick	MS-GND	GND
P7	SD	SD-GND	GND
P8	MMC_PLUS	MMC-DATA6	SP7
P9	MemoryStick	MS-BS	SP14
P10	SD	SD-CLK	SP8
P11	MemoryStick	MS-DATA1	SP12
P12	MemoryStick	MS-DATA0	SP9
P13	SD	SD-VCC	3D3V_CARD_S0
P14	MemoryStick	MS-DATA2	SP8
P15	SD	SD-GND	GND
P16	MemoryStick	MS-INS	SP2
P17	MMC_PLUS	MMC-DATA5	SP9
P18	MemoryStick	MS-DATA3	SP5
P19	SD	SD-CMD	SP10
P20	MemoryStick	MS-SCLK	SP1
P21	MMC_PLUS	MMC-DATA4	SP11
P22	MemoryStick	MS-VCC	3D3V_CARD_S0
P23	SD	SD-DATA3	SP12
P24	MemoryStick	MS-GND	GND
P25	SD	SD-DAT2	SP13
P26	SD	SD-WP COM /SDIO GND	GND
P27	SD	SD-CD COM /SDIO GND	GND
#1	XD	XD-CD	XD_CD#
#2	XD	XD-R/B	SP1
#3	XD	XD-RE	SP2
#4	XD	XD-CE	SP3
#5	XD	XD-CLE	SP4
#6	XD	XD-ALE	SP5
#7	XD	XD-WE	SP6
#8	XD	XD-WP-IN	SP7
#9	XD	XD-GND	GND
#10	XD	XD-D0	SP8
#11	XD	XD-D1	SP9
#12	XD	XD-D2	SP10
#13	XD	XD-D3	SP11
#14	XD	XD-D4	SP12
#15	XD	XD-D5	SP13
#16	XD	XD-D6	SP14
#17	XD	XD-D7	XD-D7
#18	XD	XD-VCC	3D3V_CARD_S0
#19	XD	XD-GND	GND

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

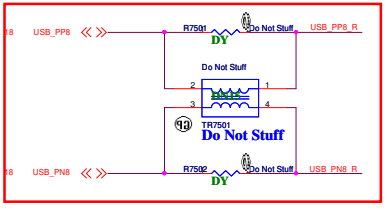
Size: A3 | Document Number: **QUEEN AMD Muxless/UMA** | Rev: X00

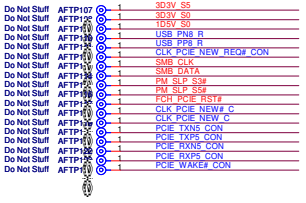
Date: Thursday, May 26, 2011 | Sheet 74 of 104

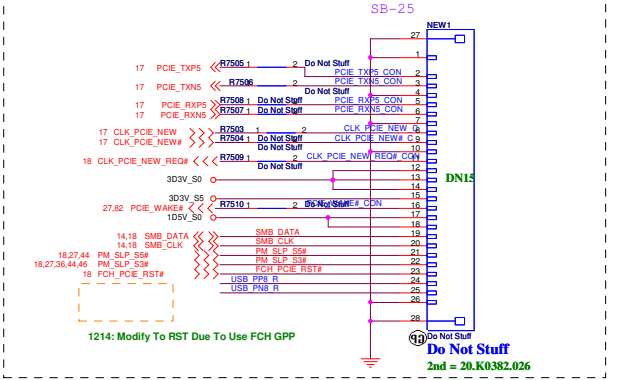
SSID = ExpressCard

1D5V_S0_CARD Max. 650mA, Average 500mA.
3D3V_S0_CARD Max. 1300mA, Average 1000mA
3D3V_S5_CARDAUX Max. 275mA

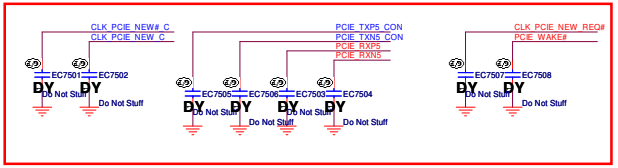
1122 X02 Modify:
Change TR7501 CM choke to 69.10103.041
and un-stuff R7501,R7502 from EMC Neo Suggestion.
Change R7501,R7502 to 0603 from 0402.
1123 X02 Modify:
SWAP TR7501 pin1&4 and pin2&3 each other
base on Connie swap report.







For EMI



DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Express Card

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 75 of 104

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DQ15 AMD DIS SAMSUNG TI

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Title: *Reserved*

Size	Document Number	Rev
A4	*QUEEN AMD Muxless/UMA*	X00

Date: Thursday, May 26, 2011 Sheet 76 of 104

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DQ15 AMD DIS SAMSUNG TI

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Title: *Reserved*

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 77 of 104

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DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

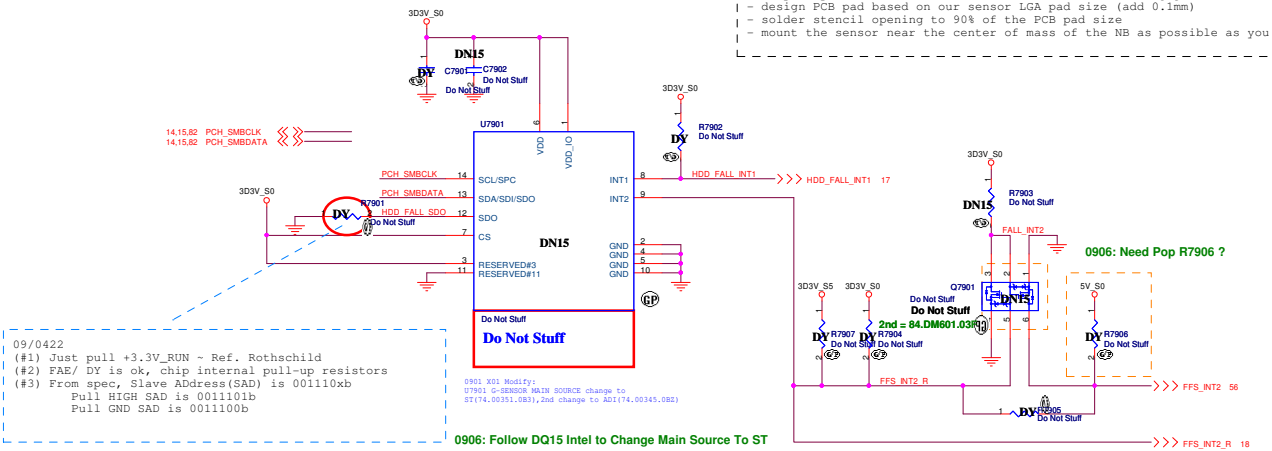
Size: A4 | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Thursday, May 26, 2011 | Sheet 78 of 104

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

DQ15 AMD DIS SAMSUNG TI

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Free Fall Sensor

Size: A3 | Document Number: QUEEN AMD Muxless/UMA | Rev: 1A00

Date: Thursday, May 26, 2011 | Sheet 79 of 104

(Blanking)

DQ15 AMD DIS SAMSUNG TI

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Title

Reserved

Size	Document Number	Rev
A	*QUEEN AMD Muxless/UMA*	X00

Date: Thursday, May 26, 2011 Sheet 80 of 104

(Blanking)

DQ15 AMD DIS SAMSUNG TI

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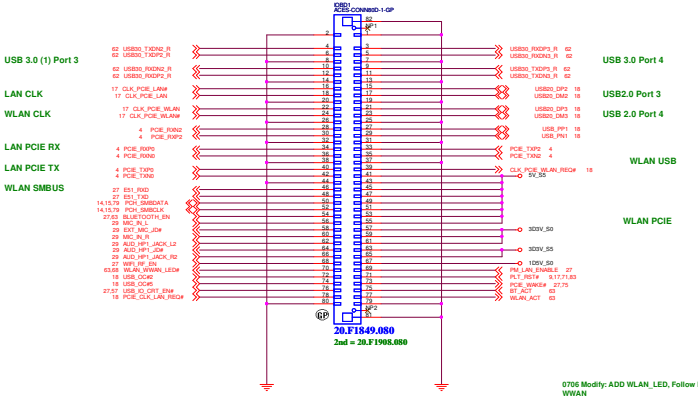
Title
UNUSED PARTS/EMI Capacitors

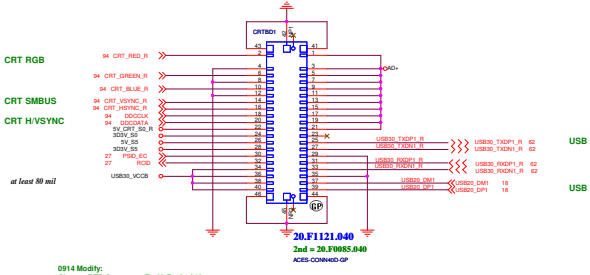
Size	Document Number	Rev
A4	QUEEN AMD Muxless/UMA	X00

IO Board CONN 80 pin

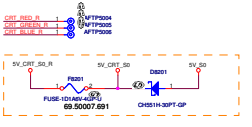


0706 Modify: ADD WLAN_LED, Follow Intel, AMD Dont have WWAN

1123 Modify: Change Main Source To 20.F1849.080 & Add 2nd 20.F1908.080 on IOBD1 from ME updated latest connector list & Modify Pin Define So 4 corner pin are GND.

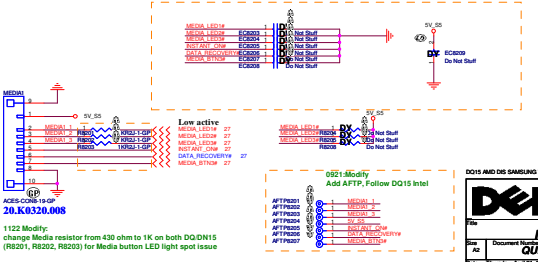


0914 Modify:
Change BTB Connector To 20.F121.040
Follow ME Connector List
1228 Modify:
Remove USB 3.0 Signal and Re-arrange Pin-Define For Better Layout Routing
1118 Modify:
Modify Pin Define



0906 Modify:
Change Part Number 20.K0422.010 To20.K0320.008
Base On ME Connector List
0914 Modify:
Change R8201~R8203 to 470 ohm from 33ohm
for fine tune MEDIA LED 5mA current.
0928 Modify:
Change R8201~R8203 to 430 ohm from 470 ohm
for fine tune MEDIA LED 5mA current.

0105:Modify
EMI Neo Suggest To Reserve, Close To Media Buttom Board



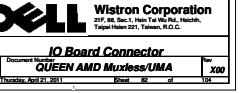
0902 XS1 Modify:
Add PR201,R8201 sync with DQ15-WV.
Rename CNTRS1 pin24 power to 5V_CRT_SS_R.

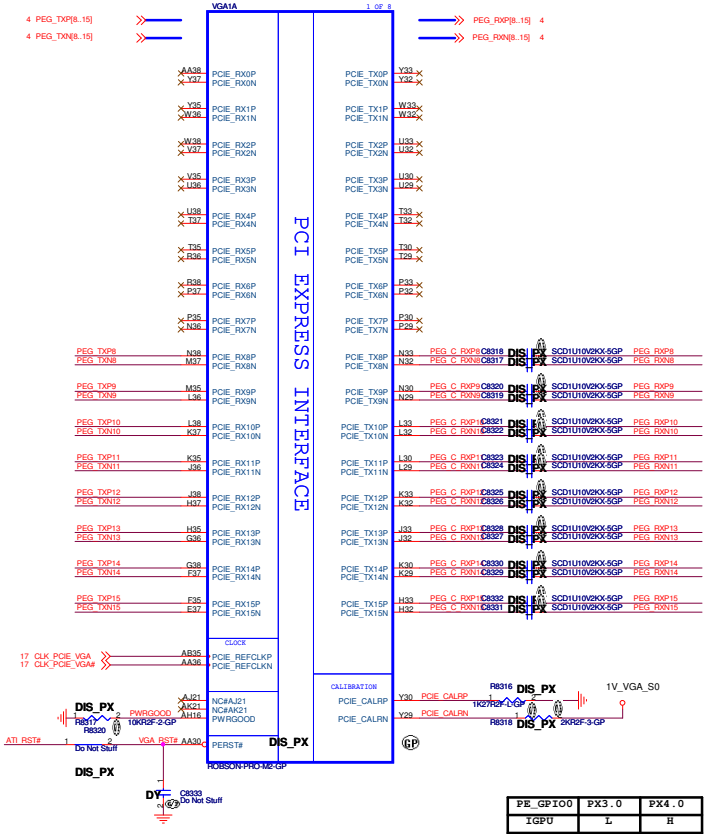
0914 XS1 Modify:
Change R8201~R8203 to 430ohm from 100ohm.
Add R8204,R8205,R8208 PH 5V_S5 on MEDIA_LED1~3# for PWM OD mode.

1122 Modify:
change Media resistor from 430 ohm to 1K on both DQ/DN15
(R8201, R8202, R8203) for Media button LED light spot issue

0921:Modify
Add AFTP, Follow DQ15 Intel

DQ15 AMD DIS SAMSUNG T1



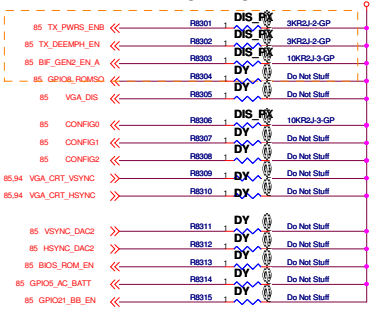


CONFIGURATION STRAPS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 3K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE	
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	1
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

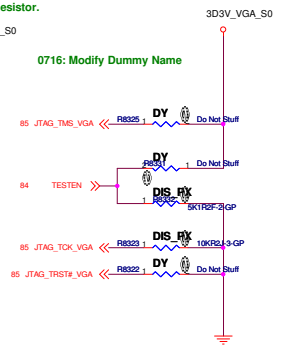
Full Tx output swing. Must be pulled to 3.3 V at reset using ~3-K (5%) resistor.

DG DY, CHECK

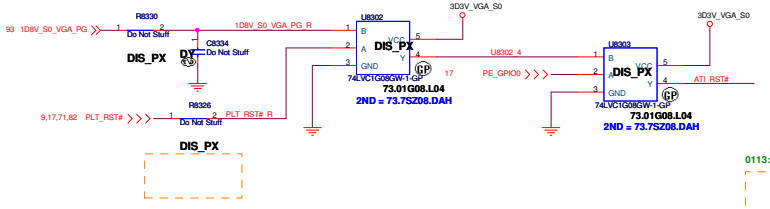
PIN STRAPS



0716: Modify Dummy Name



PE_GPIO0	PX3.0	PX4.0
IGPU	L	H
DGPU	H	H



0113: Remove APU_RST# Colay

JTAG SIGNAL OPTION – for option2

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

0113: Remove APU_RST# Level Shift

1008: Add Level Shift For APU_RST# To 3.3V

DQ15 AMD DIS SAMSUNG TI

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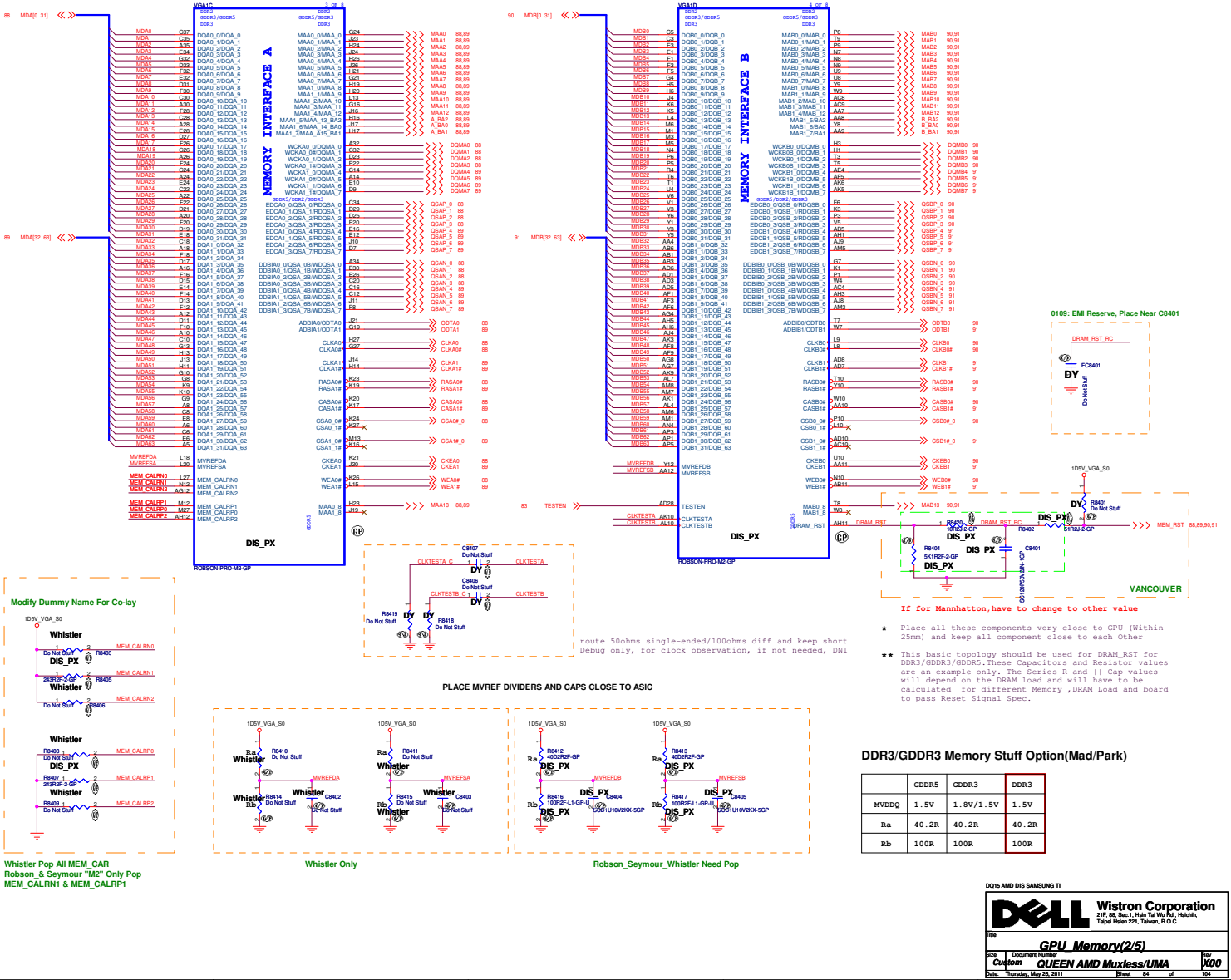
Title: GPU_PCIE/STRAPPING(1/5)

Size: Custom | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Thursday, May 26, 2011 | Sheet 83 of 104



DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

DO15 AMD DIS SAMSUNG TI

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Title: GPU_Memory(2/5)

Size: Custom | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Thursday, May 26, 2011 | Sheet 84 of 104

1228: Modify Table

Default 1G + Hynix Vram, 0011 72.52G63.A0U

MEMORY ID Table

DVPDATA[3:0]	Description	PN
0001	DDR3 Hynix-H5TQ2G63BFR-11C (900MHz) 128M*16	72.52G63.A0U
0011	DDR3 Hynix-H5TQ1G63DFR-11C (900MHz) 64M*16	72.51G63.H0U
0010	DDR3 SAMSUNG-K4W2G1646C-HC11 (900MHz) 128M*16	72.42164.D0U
0000	DDR3 SAMSUNG-K4W1G1646G-BC11 (900MHz) 64M*16	72.41646.Q0U

0914: Change R8518 Part Reference To HYNIX
For Hynix + Vram 1G, Pop R8518, Pop R8519
For Hynix + Vram 512M, Pop R8518, De-pop R8519
For Samsung+Vram1G, De-pop R8518, Pop R8519
For Samsung+Vram512M, De-pop R8518, De-POP R8519

0708: Need To Pick GPIO
0708: Add Thermal Shutdown Circuit
0107: SW Will Not Use This Function, DY For Reserve Only

I2C Bus for LVDS

For new version no 27M

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

DDC1/DDC2/DDC6 have 5V-tolerant

DDC1 channel for CRT

DDC2 channel for HDMI

AUXP PD 100K
AUXN PU 100K
Draw on EDP circuit page

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

0107 Modify: Removed P2800 Circuit , So does C8523.

1027 Modify: Use VGA Smbus Instead of use another P2800

DQ15 AMD DIS SAMSUNG TI

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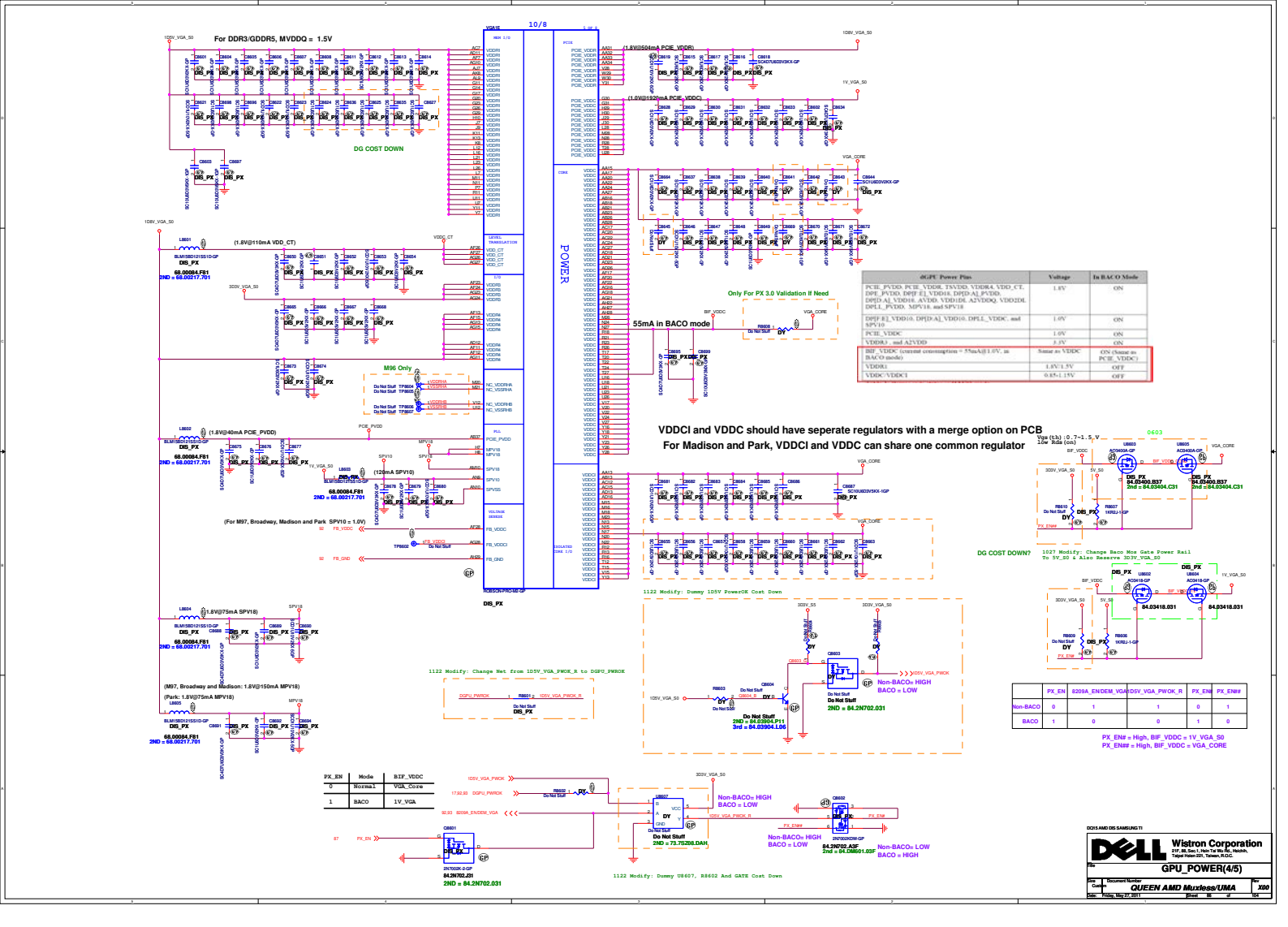
Taipei Hsien 221, Taiwan, R.O.C.

GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A0 | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Thursday, May 26, 2011 | Sheet 16 of 56

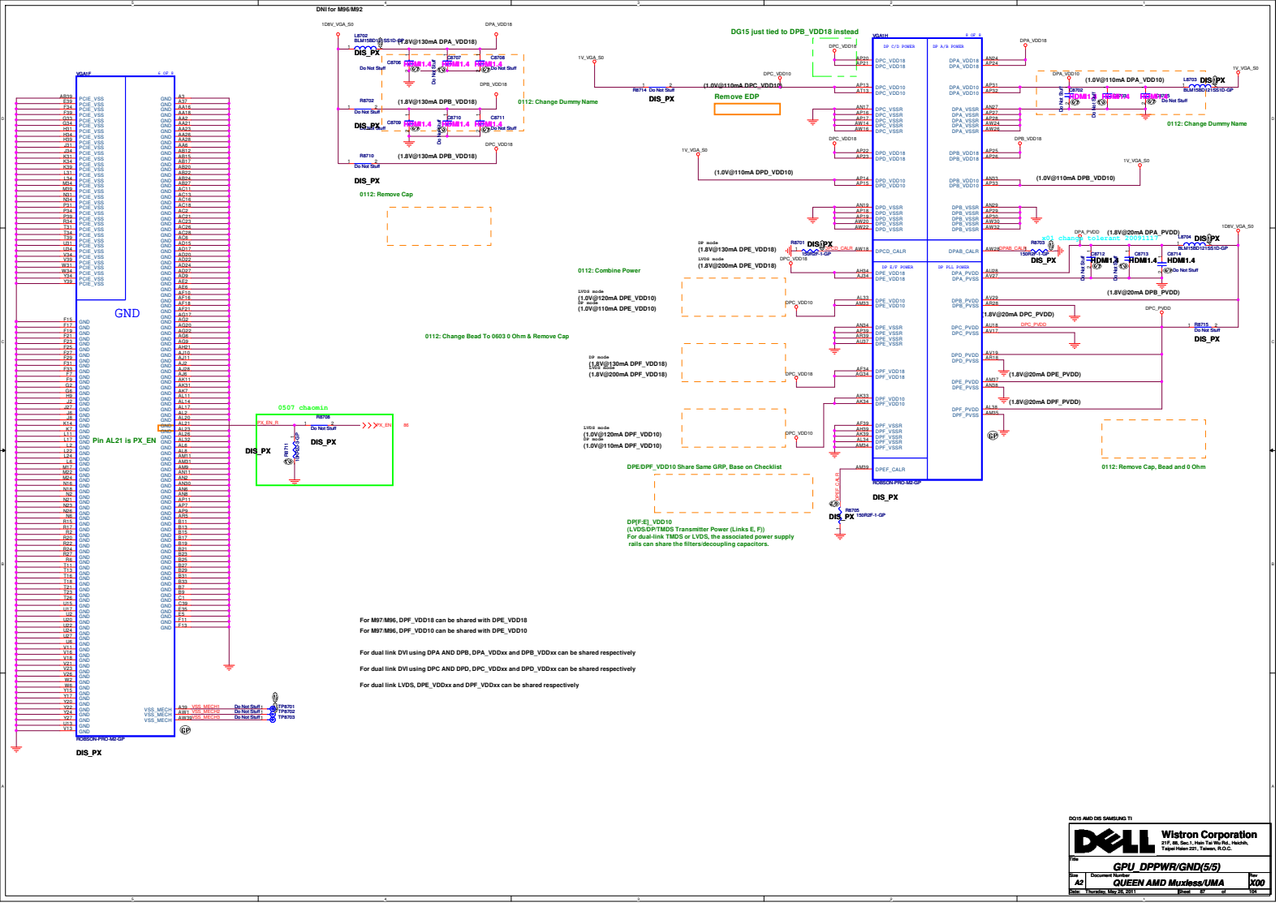


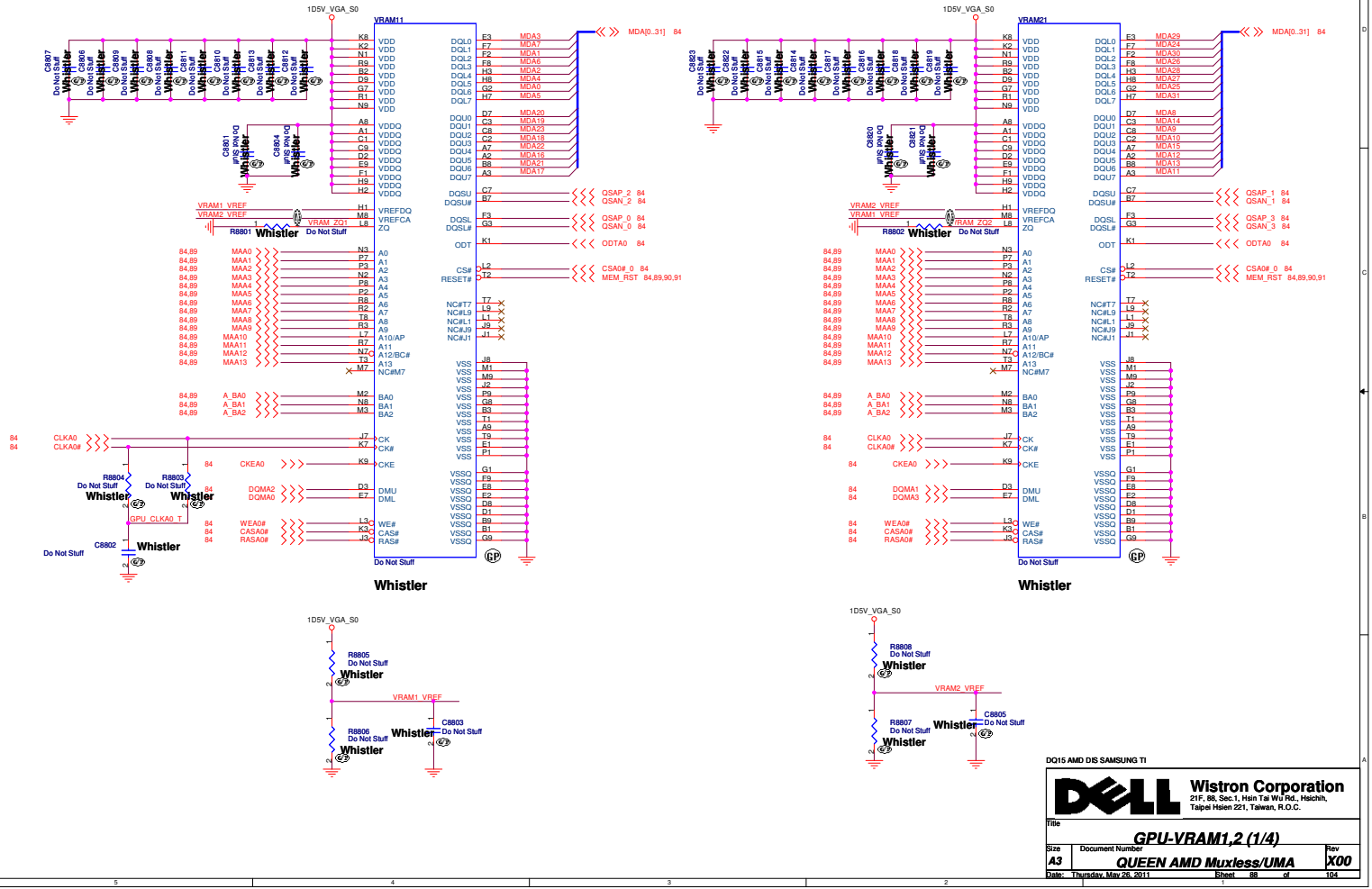
dGPU Power Pins	Voltage	In BACO Mode
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDRA, VDD_CT, DPE_PVDD, DPIF_E1_VDD10, DP[E:A]_PVDD, DP[D:A]_VDD10, AVDD, VDD10DE, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	ON
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	ON
PCIE_VDDC	1.0V	ON
VDDR3, and A2VDD	3.3V	ON
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	ON (Same as PCIE_VDDC)
VDDCI	1.8V/1.5V	OFF
VDDC-VDDCI	0.85~1.15V	OFF

PX_EN	Mode	BIF_VDDC
0	Normal	VGA_Core
1	BACO	1V_VGA

	PX_EN	8209A_EN/DEM_VGA	1D5V_VGA_PWOK_R	PX_EN	PX_EN##
Non-BACO	0	1	1	0	1
BACO	1	0	0	1	0

PX_EN# = High, BIF_VDDC = 1V_VGA_S0
PX_EN## = High, BIF_VDDC = VGA_CORE


DNI for M96/M92
DG15 just tied to DPB_VDD18 instead
Remove EDP
0112: Change Dummy Name
0112: Remove Cap
0112: Combine Power
0112: Change Bead To 0603 0 Ohm & Remove Cap
0112: Remove Cap, Bead and 0 Ohm
0507 chaomin
Pin AL21 is PX_EN
DPE/DPF_VDD10 Share Same GRP, Base on Checklist
DPF[F,E]_VDD10
(LVDS/DP/TMDS Transmitter Power (Links E, F))
For dual-link TMDS or LVDS, the associated power supply
rails can share the filters/decoupling capacitors.
For M97/M96, DPF_VDD18 can be shared with DPE_VDD18
For M97/M96, DPF_VDD10 can be shared with DPE_VDD10
For dual link DVI using DPA AND DPB, DPA_VDDxx and DPB_VDDxx can be shared respectively
For dual link DVI using DPC AND DPD, DPC_VDDxx and DPD_VDDxx can be shared respectively
For dual link LVDS, DPE_VDDxx and DPF_VDDxx can be shared respectively
DIS_PX
GND
VGAIF
ROBSON-PHO-M2-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
GPU_DPPWR/GND(5/5)
QUEEN AMD Muxless/UMA
X00
Thursday, May 28, 2009



DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

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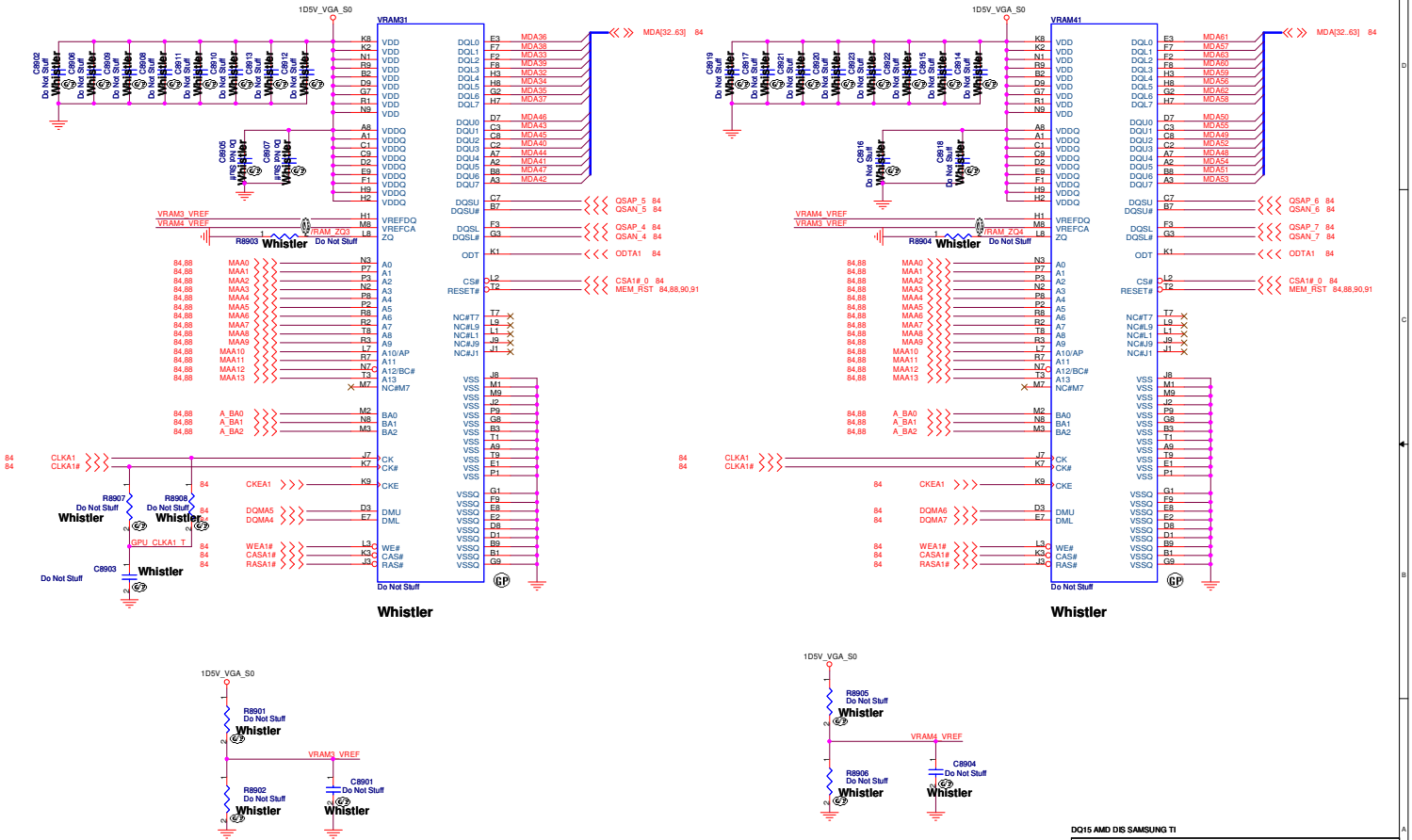

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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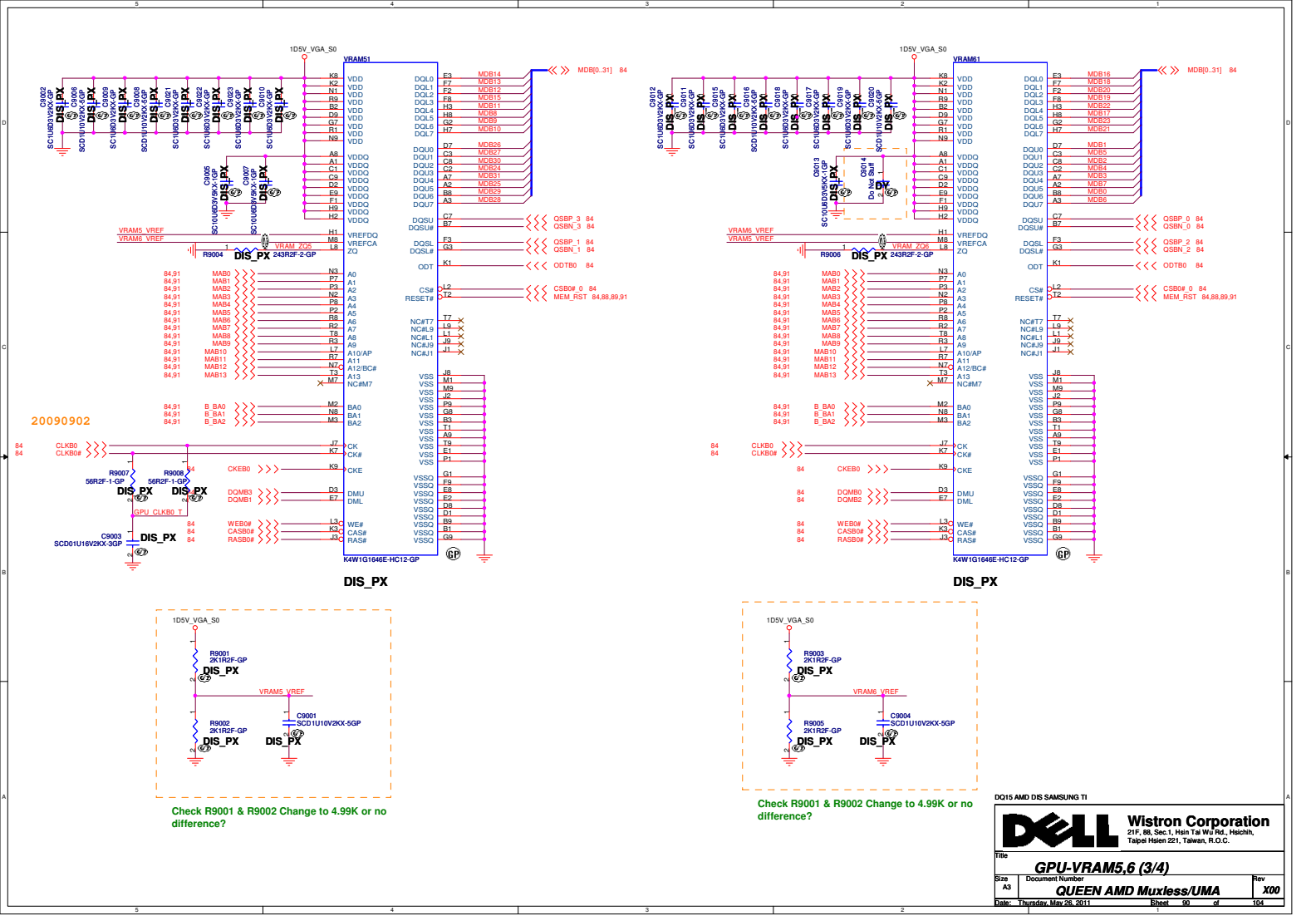
Title: GPU-VRAM3,4 (2/4)

Size: A3 | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Thursday, May 26, 2011 | Sheet 89 of 104



DQ15 AMD DIS SAMSUNG TI

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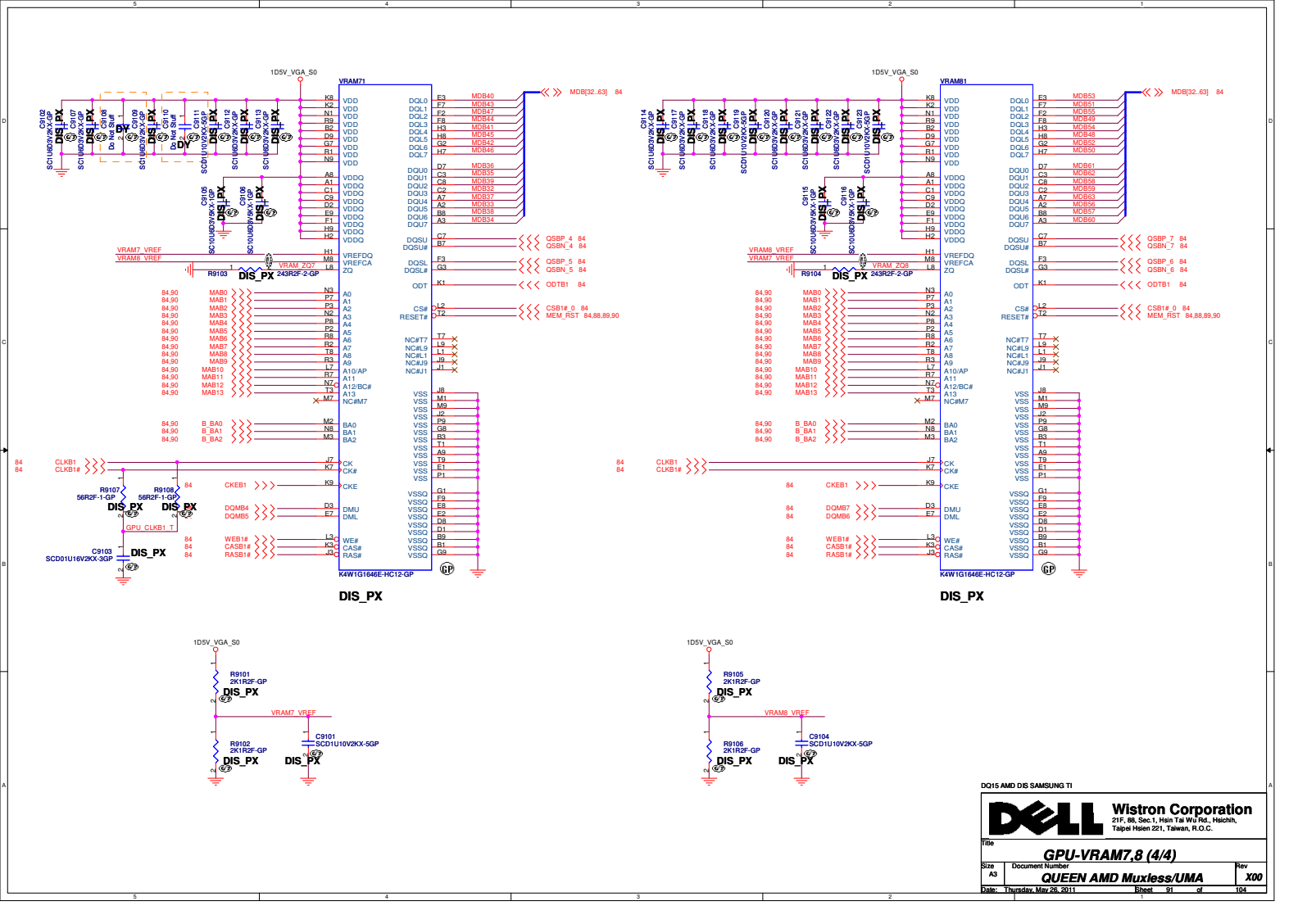
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM5,6 (3/4)**

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 90 of 104



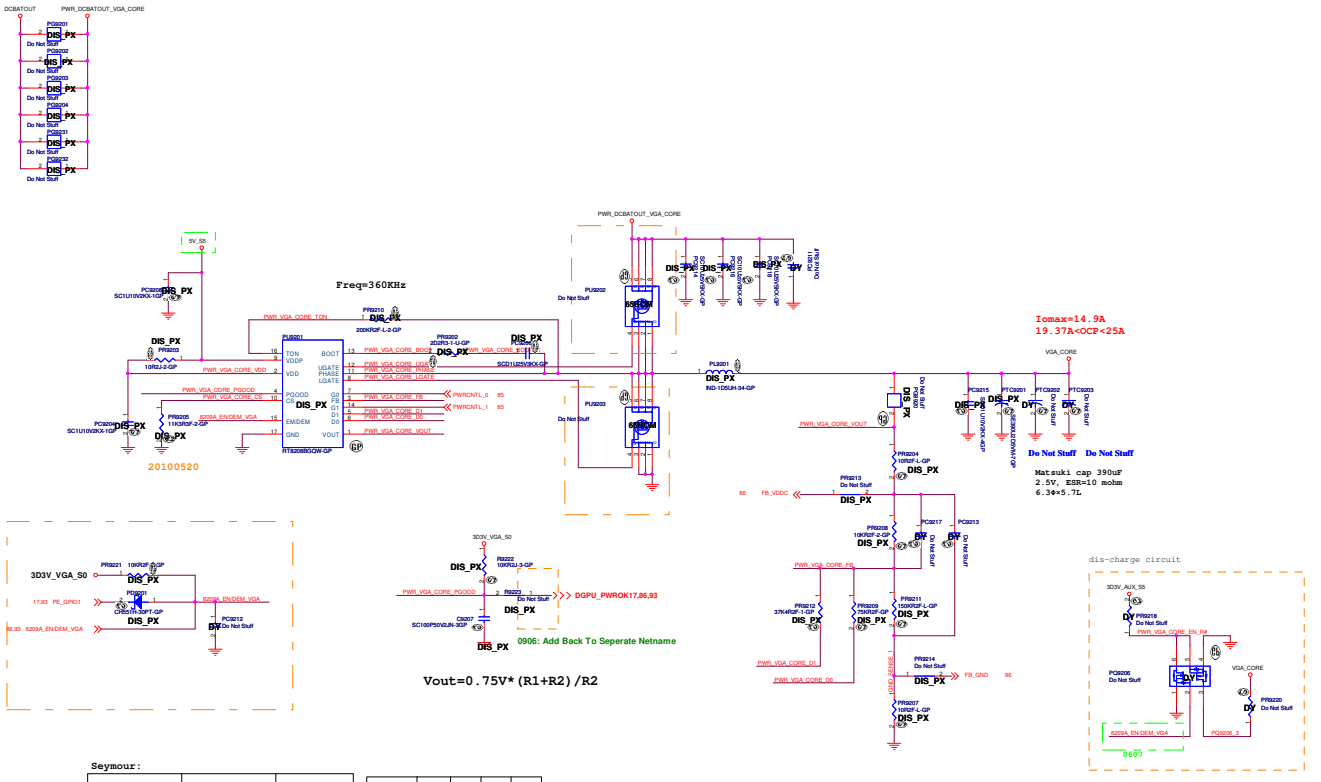
DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM7,8 (4/4)**

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 91 of 104



Seymour:

PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
L	L	1.1V
L	H	1.0V
H	L	0.9V
H	H	X

	PR9208	PR9211	PR9209	PR9212
Seymour	10R2F	150R	75R	37R4
Whistler	10R2F	75R	150R	150R

Whistler :

PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
L	L	1.0V
L	H	X
H	L	0.9V
H	H	X

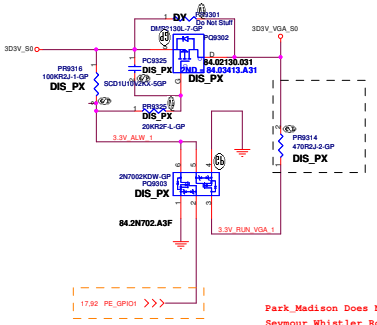
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.5uH PCMC104T-1R5MH Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 560U 2.5V MPZVL560M7SR7 16mOhm 3.5Arms 77.55671.00L
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms Panasonic/79.22719.20L
H/S: RJK03B9DPA / 10.9mohm/15.1mOhm@4.5Vgs/ 84.003B9.B37
L/S: RJK03D4DPA / 4.6mohm/5.6mOhm@4.5Vgs/ 84.00034.A37

DCIS AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title:	RT8208B +VGA_CORE	
Size: A0	Document Number: QUEEN AMD Muxless/UMA	Rev: X00
Date: Friday, May 27, 2011	Sheet 86 of 103	

+3VS to 3.3V_DELAY Transfer



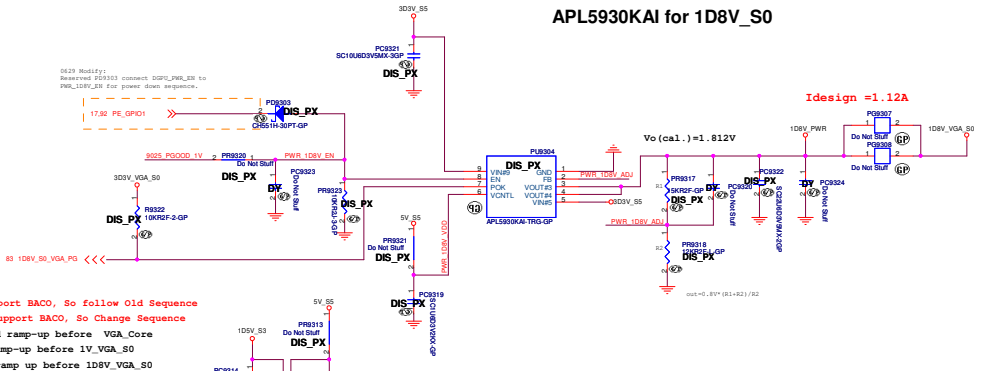
Different To Intel, AMD Is High Active

PE_GPIO1	PX3.0	PX4.0
IGPU	L	H
DGPU	H	H

2nd = 84.DM601.03F

APL5930KAI for 1D8V_S0

Idesign =1.12A

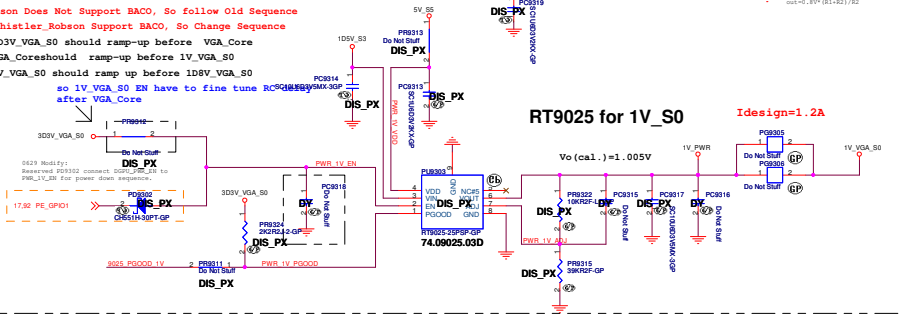


Park_Madison Does Not Support BACO, So follow Old Sequence
Seymour_Whistler_Robson Support BACO, So Change Sequence
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Coreshould ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

RT9025 for 1V_S0

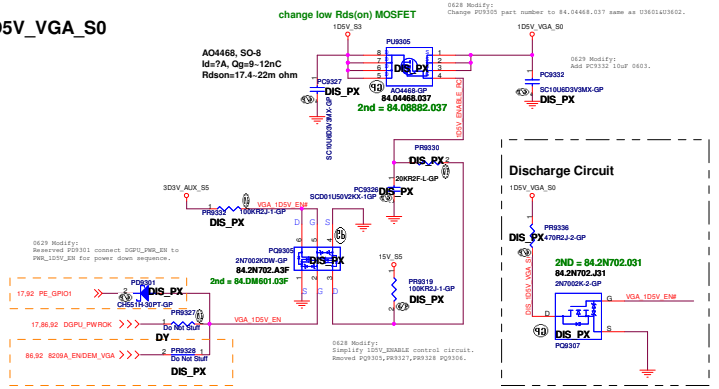
Idesign=1.2A



1D5V_VGA_S0

change low Rds(on) MOSFET

AO4468, SO-8
Id=7A, Qg=9~12nC
Rdson=17.4~22m ohm



Discharge Circuit

DQ15 AMD DIS SAMSUNG TI

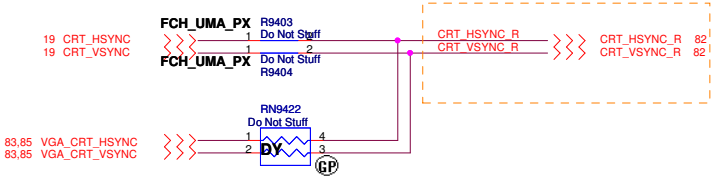
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

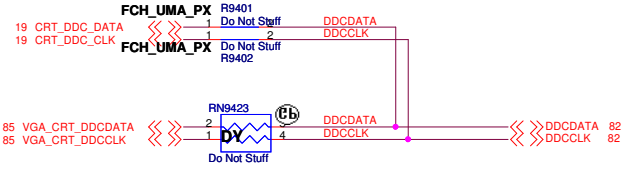
Title: DISCRETE VGA POWER

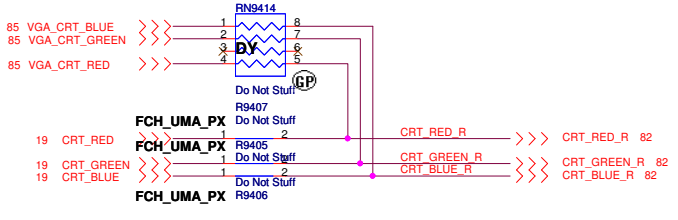
Size	Document Number	Rev
Custom	QUEEN AMD Muxless/UMA	X00

Date: Friday, May 27, 2011 Sheet 93 of 104

SSID = VIDEO







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Title: *LVDS_VGA_Switch*

Size | Document Number: *QUEEN AMD Muxless/UMA* | Rev: *X00*

Date: Thursday, May 26, 2011 | Sheet 94 of 104

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Title

Reserved

Size	Document Number	Rev
A	***QUEEN AMD Muxless/UMA***	X00

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TOUCH PANEL connector

0707: Move To Page 49, Touch Panel Combine With LVDS

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Title: Touch Panel

Size	Document Number	Rev
A	QUEEN AMD Muxless/UMA	X00

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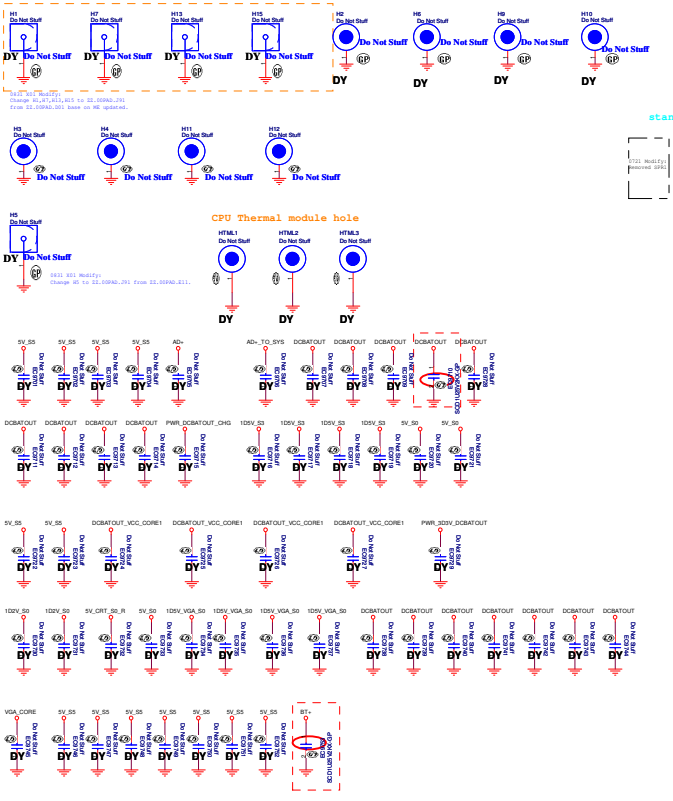

Check test point

0624 Modify:
Removed AFTP1,AFTP7~AFTP13.

0109: EMI Reserve EC9701~EC9704 Place: (970 , 7875) Top near C5702 Bottom near PTC9203 Bottom near H15 Bottom

0109: EMI Reserve EC9705 Place: near PU4002 Top

0109: EMI Reserve EC9706 Place: near PR4002 Top

0109: EMI Reserve EC9707~EC9714,EC9728 Place: near LCD1 Top (4090, 7615) Top (6275 7295) Top near PU4003 Top near PC4016 Top near F6901 Top (7600 6015) Top near PC4117 Top near PC4301 Top

0109: EMI Reserve EC9715 Place: near PR4002 Top

0109: EMI Reserve EC9716~EC9719 Place: (3785 3415) Top (5785 2050) Top

0109: EMI Reserve EC9716~EC9719 Place: (3785 3415) Top (5785 2050) Top

0109: EMI Reserve EC9720~EC9721 Place: near C5604 Top near D3604 Top

0109: EMI Reserve EC9722~EC9723 Place: near C5604 Top near D3604 Top

0109: EMI Reserve EC9724~EC9727 Place: near PC4248 Top near PC4246 Top (4300 3985) Bottom (4300 3985) Bottom

0109: EMI Reserve EC9729 Place: near PC4114 Top

0109: EMI Reserve EC9730~EC9731 Place: near C765 Top near PTC4203 Top

0105: Add SPR1~9
0115: EMI Agree To Remove Spring7 & 10
0117: Add back SPR7
0118: Remove SPR6
0127: Change SPR9 P/N To 34.4B312.002, Old P/N No Stock

0817 X01 Modify:
Dell Peter already confirmed DQ15 and DN15 will not support Bluetooth BT365, only support combo Wirless+BT. Please DUMMY Bluetooth connector(BT1) and stand off (HBT1) and related components.

1122 Modify:
Change HHD1,HDD4,HGPU1,HGPU2 2nd to 34.4CK01.401 from 34.4CK01.201 from ME updated connector list.

0321 Modify:
Add HGPU1,HGPU2 Dummy Name DIS_PX, So UMA Wont Pop

DC15 AMD DIS SAMSUNG TI

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Title: UNUSED PARTS/CAP

Size: A2 | Document Number: QUEEN AMD Muxless/UMA X00 | Rev:

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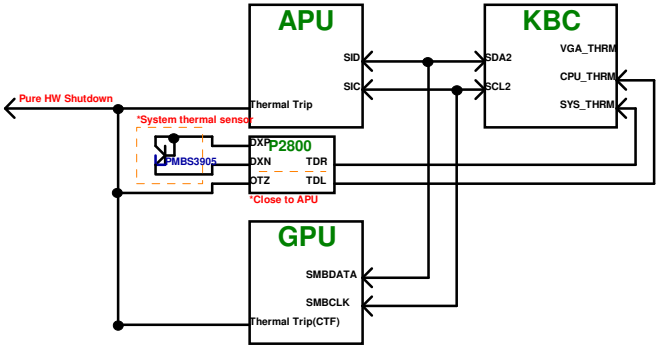
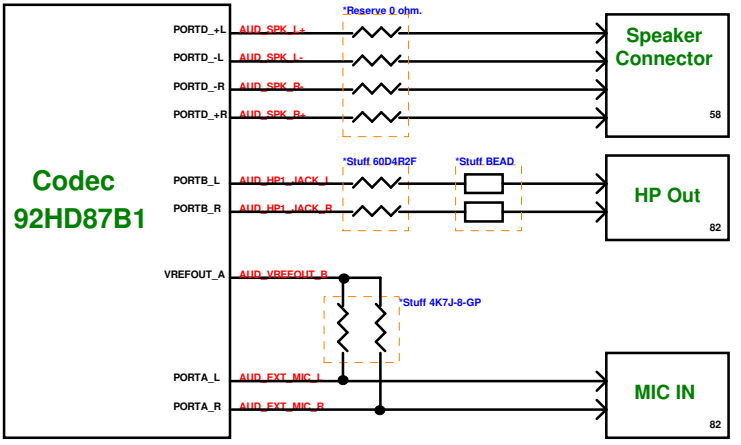
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

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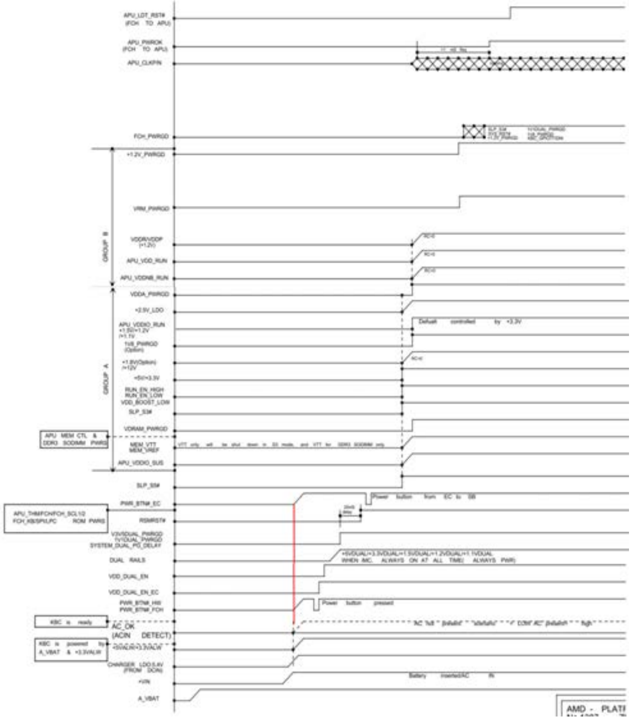
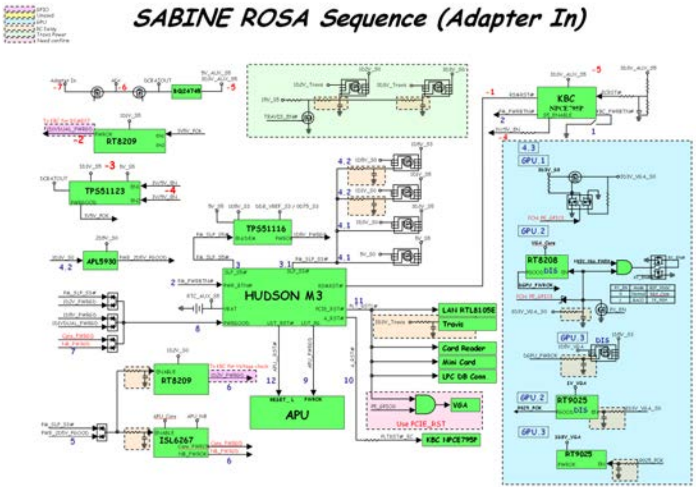
POWER SEQUENCE





DO15 AMD DIS SAMSUNG TI

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Title	POWER SEQUENCE	
Size: Custom	Document Number: QUEEN AMD Muxless/UMA	Rev: X00
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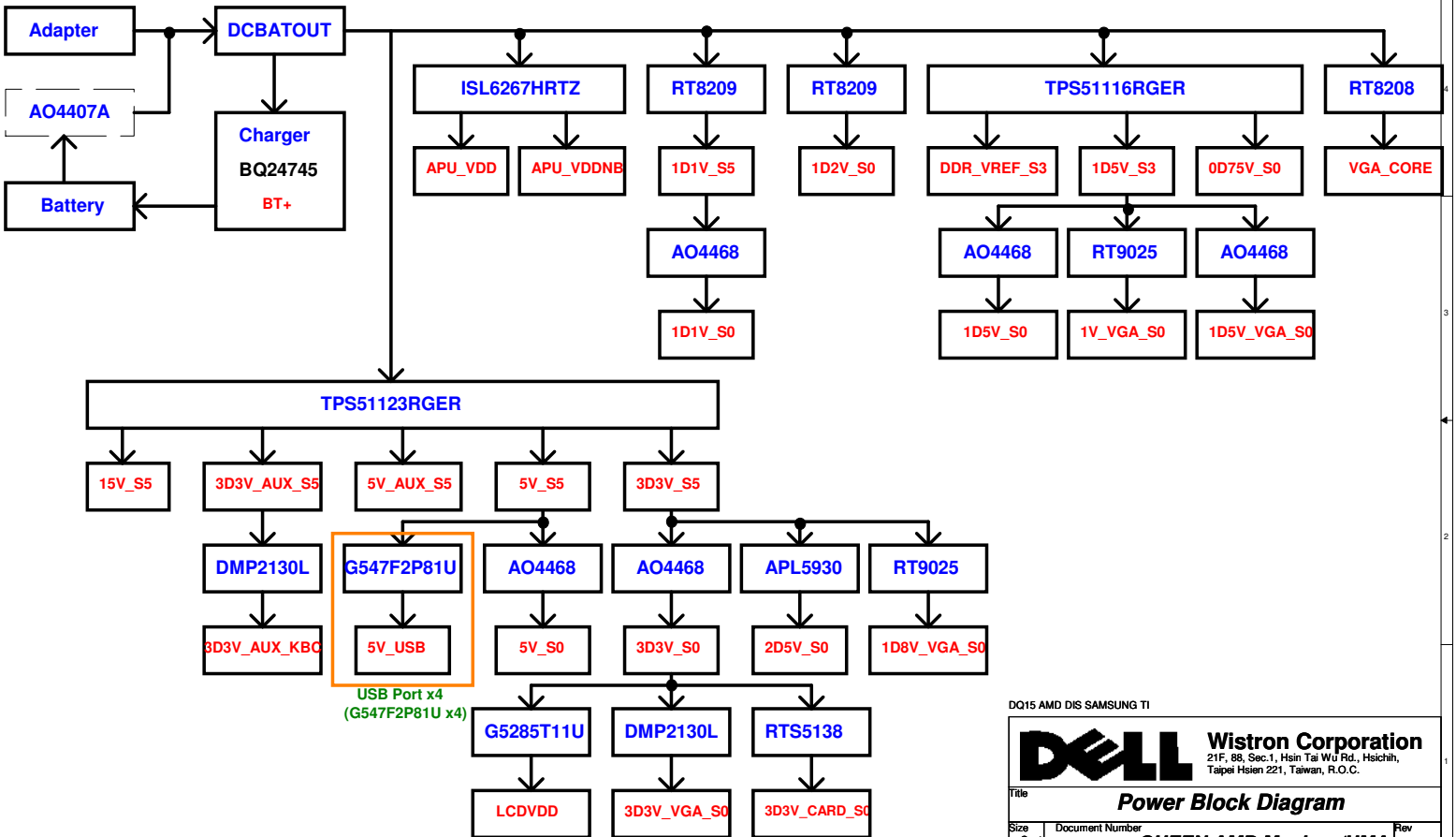

DQ15 AMD DIS SAMSUNG TI

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Title: **Power Block Diagram**

Size: Custom | Document Number: **QUEEN AMD Muxless/UMA** | Rev: X00

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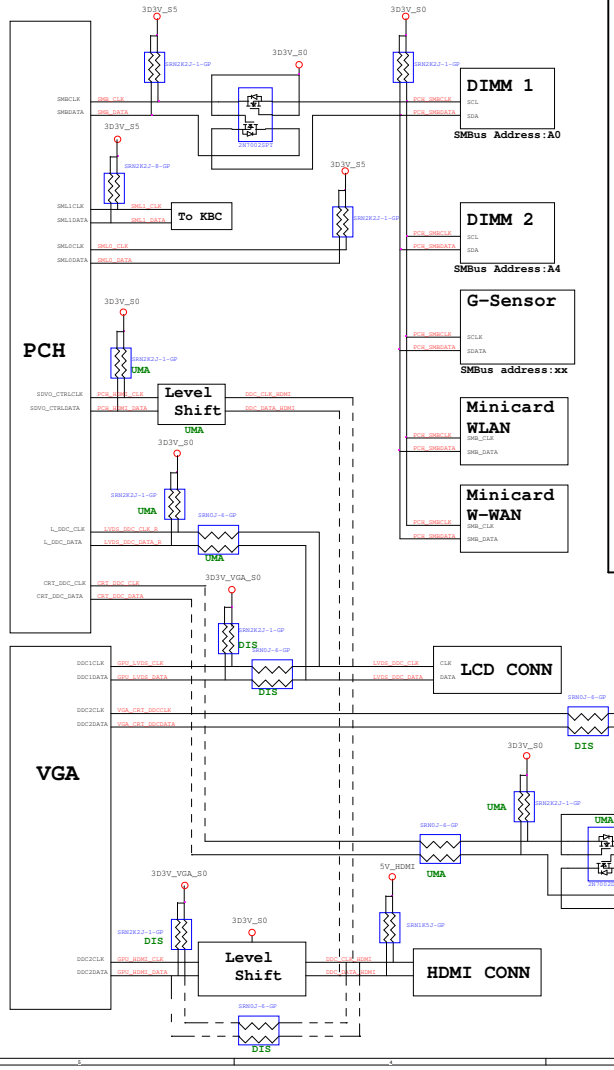
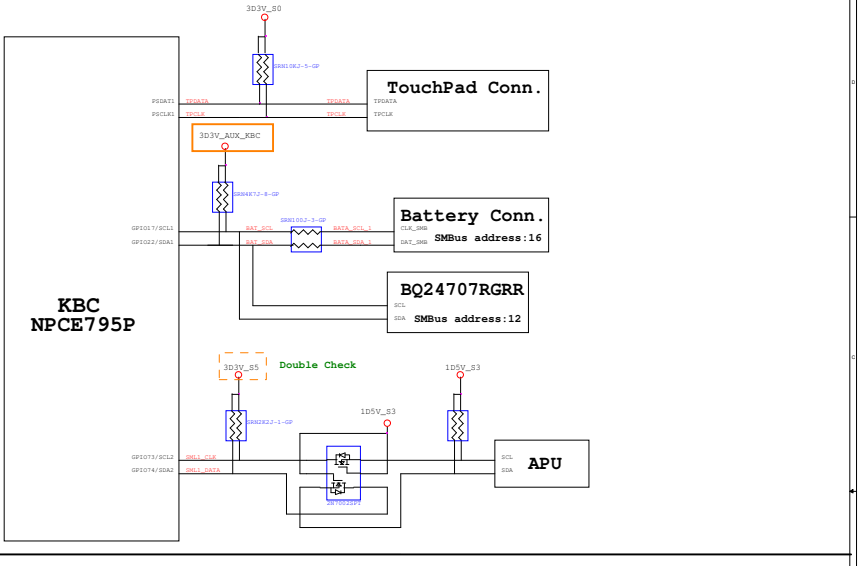
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title	SMBUS BLOCK DIAGRAM		
Size	Document Number	QUEEN AMD Muxless/UMA	Rev
A0			X00
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Change notes –

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Title: *Change notes*

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

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Change notes – Page 4

VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
X02	01/08	3	18,19	Add C1825,C1922.	Reduce V_REF ripple by EA team result.	EE
		4	37	Reserve C3721,C3722.	Prevent signal cross talk.	EE
		5	ALL	Change capacitors value and add C3723.	Ensure signal quality.	EE
	01/11	1	68	Change KB1 P/N.	According ME request.	ME
		2	66	Change R6601,R6602,R6604,R6606 to 1KR, R6603 to 470R.	Decrease LED brightness.	EE
	01/12	1	37	Add C3724, R3757.	To set accurate current detection in EC.	EE
		2	10	Add R1041 0R.	Add 0R for level shift off.	EE
	01/13	1	21,37	Add C3725, C2105.	Reserve for singal quality.	EE
	01/14	1	Power	Modify power team componets.	Request by Power Team.	Power
		2	7	Change RN712 to 22R.	Fine tuned damping resistor value.	EE
A00	02/08	1	66	Reserve R6609, R6610 1KR.	Add for future LED brightness balance.	EE
		2	68	Add keyboard back light circuit, remove R5403.	Add for keyboard with back light module.	EE
		3	69	Change HALLSW1 footprint for co-layout.	Change for co-layout different kind of HALLSW1.	EE
		4	77	Add AFTP7701, AFTP7702, AFTP7703.	Add AFTP test point for factory test.	EE
	02/10	1	Power	Update Obsolete parts.	Update obsolete parts due to policy.	Power
		2	79	Change HBT1 part number.	Change HBT1 part number to match ME EMN file.	ME
		3	47	Add PTC4710.	Add to solve board accoustic issue.	EE
	02/22	1	54	Remove co-layout pad.	As factory requst.	EE
		2	42	Add C4217, C4401, C4402.	Ensure signal quality.	EE
		3	48	Delete Power Gap.	Request by Power Team.	Power
	02/23	1	ALL	Change to short pad.	Change most of 0-ohm resistors to short pad.	EE
	02/24	1	7,68,79	Reserve C724, C725, C6806, C6807, EC7928-EC7932.	As EMC team request.	EMC
	02/25	1	13	Add TP1309.	As factory requset to add.	Factory
		2	7,68	Rename EMC capacitor to EC704,EC705,EC6801,EC6802.	Meet schematic standardization.	EE
		3	49,89	Change PR4913 to 3.9R, PR8905 to 6.98KR.	PR4913 for snubber, PR8905 for OCP.	Power
		4	21	Change R2133 to 0R.	Set GPIO input level from 0.5V to 0V.	EE
		5	79	Remove EC7928.	Layout space limitation.	EE
	02/26	1	39,42	Empty R3906 and Change R4202 from 0R to 1KR.	It is for solving T8 shutdown issue.	EE
	03/03	1	60	Change SPK1 part number.	Request by ME.	ME
	03/05	1	20,24,37	Empty R2029,R2404,R3751.	Saving unused components.	EE

0303-1

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Title	Change notes	
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