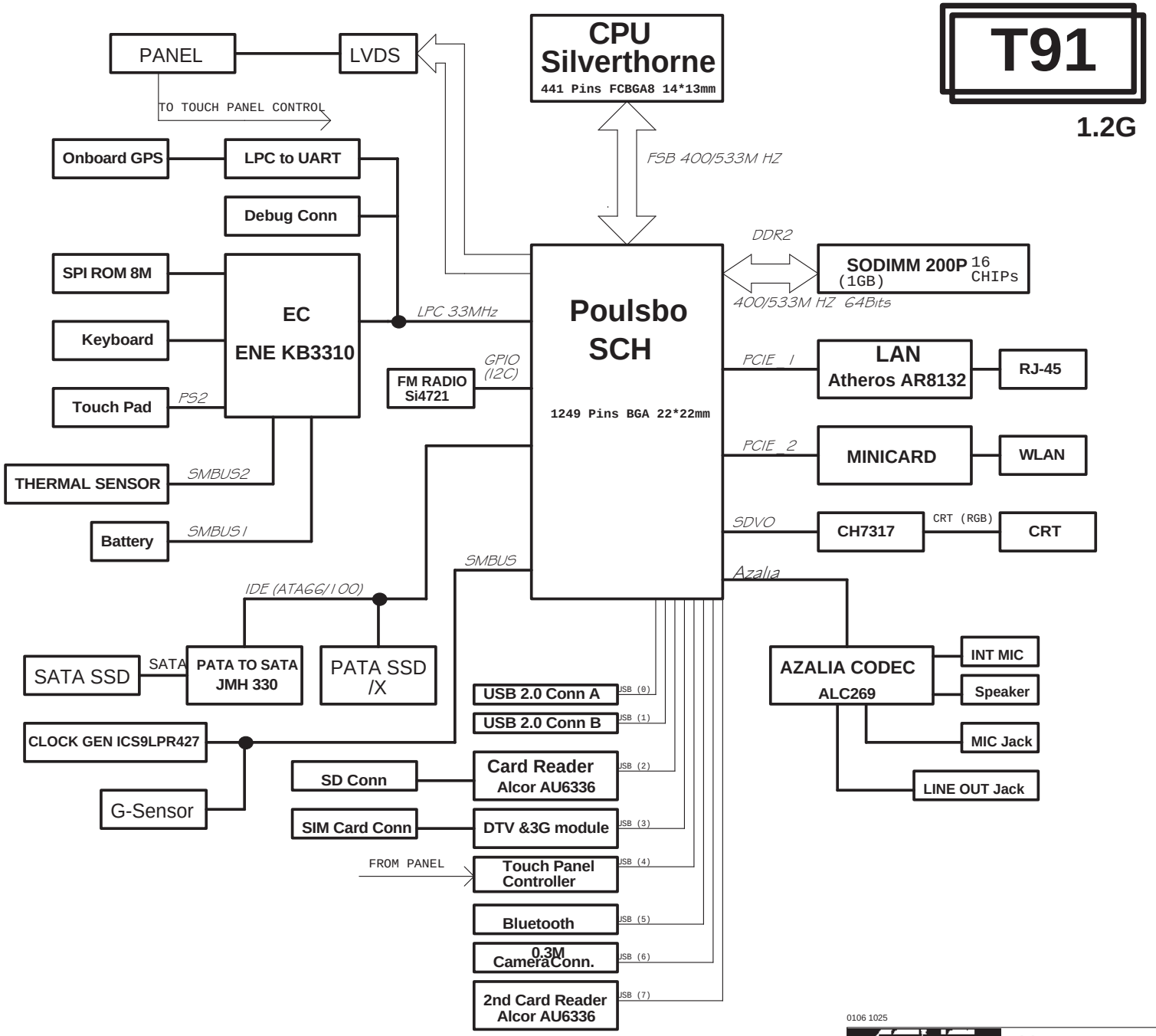

0106 1025

ASUSTeK COMPUTER INC

Title : Block Diagram

Engineer: Jerry Liu

Size	Project Name	Rev
Custom	T91	1.2G

Date: Tuesday, January 06, 2009 Sheet 1 of 57

SCH GPIO SETTING

Pin	Pin Name	Connect to	Type	Power Well	S3	S4/ S5	Input/Output Set
U41	GPIOSUS0	PM_LEVELDOWN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Output
N43	GPIOSUS1	CPU_LEVELDOWN	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
N45	GPIOSUS2	PM_PWRBTN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
R41	GPIOSUS3/ USBCC	Test Point	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
G29	GPIO0	Strap CMC/ BT_Disable	I/O CMOS3.3	Core	OFF	OFF	Input
K30	GPIO1	PCB ID	I/O CMOS3.3	Core	OFF	OFF	Input
F34	GPIO2	GPS_EN	I/O CMOS3.3	Core	OFF	OFF	Output
G33	GPIO3	Strap CMC	I/O CMOS3.3	Core	OFF	OFF	Input
K36	GPIO4	3GLAN_OFF	I/O CMOS3.3	Core	OFF	OFF	Output
H36	GPIO5	MINICARD_EN#	I/O CMOS3.3	Core	OFF	OFF	Output
F36	GPIO6	DDR_MEM_CONFIG	I/O CMOS3.3	Core	OFF	OFF	Input
J31	GPIO7/ SLPIOVR#	SLPIOVR#	I/O CMOS3.3	Core	OFF	OFF	Output
H34	GPIO8/ PROCHOT#	CAMERA_EN	I/O CMOS3.3/ OD	Core	OFF	OFF	Output
K28	GPIO9/ EXTTS1#	WLAN_LED	I/O CMOS3.3	Core	OFF	OFF	Output

0106 1025

ASUSTek Computer INC.

Title : SCH GPIO Setting

Engineer: Jerry Liu

Size	Project Name	Rev
A3	T91	1.2G

Date: Tuesday, January 06, 2009 Sheet 2 of 57

EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	HOTKEY_SW0#	I	Internal pull high
13	GPIO05/PCIRST#	BUF_RST#	I	
14	GPIO07	HOTKEY_SW1#	I	Battery over temperature
15	GPIO08	EXT_SMI#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	Reserved for GPIO extender
18	GPIO0C/ESB_DAT	NC	O	Reserved for GPIO extender
19	GPIO0D	LID_EC_R#	I	Internal pull high
20	GPIO0E/SCI#	KBC_SCI#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BATSEL#	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	PS-ON	O	latch power
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	LPC_CLKRUN#	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_A	I	
64	GPI39/AD1	BAT_B	I	
65	GPIO3A/AD2	BAT_C	I	
66	GPIO3B/AD3	BAT_D	I	
68	GPO3C/DA0	CHG_EN#	O	battery charger enabled

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	THRO_CPU_VOLT#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	Batt1 (Small/Internal): 1-present, 0-absent
76	GPI43	BAT2_IN	I	Batt2 (Small/Internal): 1-present, 0-absent
77	GPIO44/SCL1	SMB0_CLK	I/OD	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/OD	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/OD	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/OD	10K pull high to +3V
81	GPIO48/KSO16	KB_ID0	I	for KB type detection
82	GPIO49/KSO17	KB_ID1	I	for KB type detection
83	GPIO4A/PSCLK1	N.C.	O	
84	GPIO4B/PSDAT1	N.C.	O	
85	GPIO4C/PSCLK2	N.C.	O	
86	GPIO4D/PSDAT2	GS2_INT2	O	
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/OD	10K pull high to +3V
89	GPIO50/SELIO#	CHG_LED_GREEN#	O	Green charger LED
90	GPIO52/E51_CS#	CHG_LED_UP#	O	Orange charger LED
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCRL_LED#	O	
95	GPIO56	GS1_INT1	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	CNT1_CHG#	O	batt1 (Big/External) charging enabled. Batt1 is discharging priority in AC mode.
103	GPXOA06	CNT1_DIS#	O	batt1 discharging enabled
104	GPXOA07	CNT2_CHG#	O	batt2 (Small/Internal) charging enabled. Batt2 is charging priority in AC mode.
105	GPXOA08	CNT2_CHG#	O	batt2 discharging enabled
106	GPXOA09	SPI_WP#	O	
107	GPX0A10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	PM_PWROK	O	Battery parallel, H:1P, L:2P~3P
110	GPXID1	RST#	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	PM_SLPRDY#	I	SLPRDY#,100K pull down to GND
115	GPXID4	SLPMODE	I	SUSC#,100K pull down to GND
116	GPXID5	VRM_PWRGD	I	Pull high to +3V
117	GPXID6	PM_RSTRDY#	I	
118	GPXID7	RSTWARN	O	
121	GPIO57	GS1_INT2	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	GS2_INT1	O	

EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA	P	
24	GND	GND	P	
33	VCC	+3VA	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VA_AEC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA	P	
111	VCC	+3VA	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
122	XCLKI	K_XCLKI	I	
123	XCLKO	K_XCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA	P	
128	SPICS#/SELMEM#	SPI_CS#	O	

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ASUSTek Computer INC.

Title : EC Pin Define

Engineer: Jerry Liu

Size	Project Name	Rev
A3	T91	1.2G

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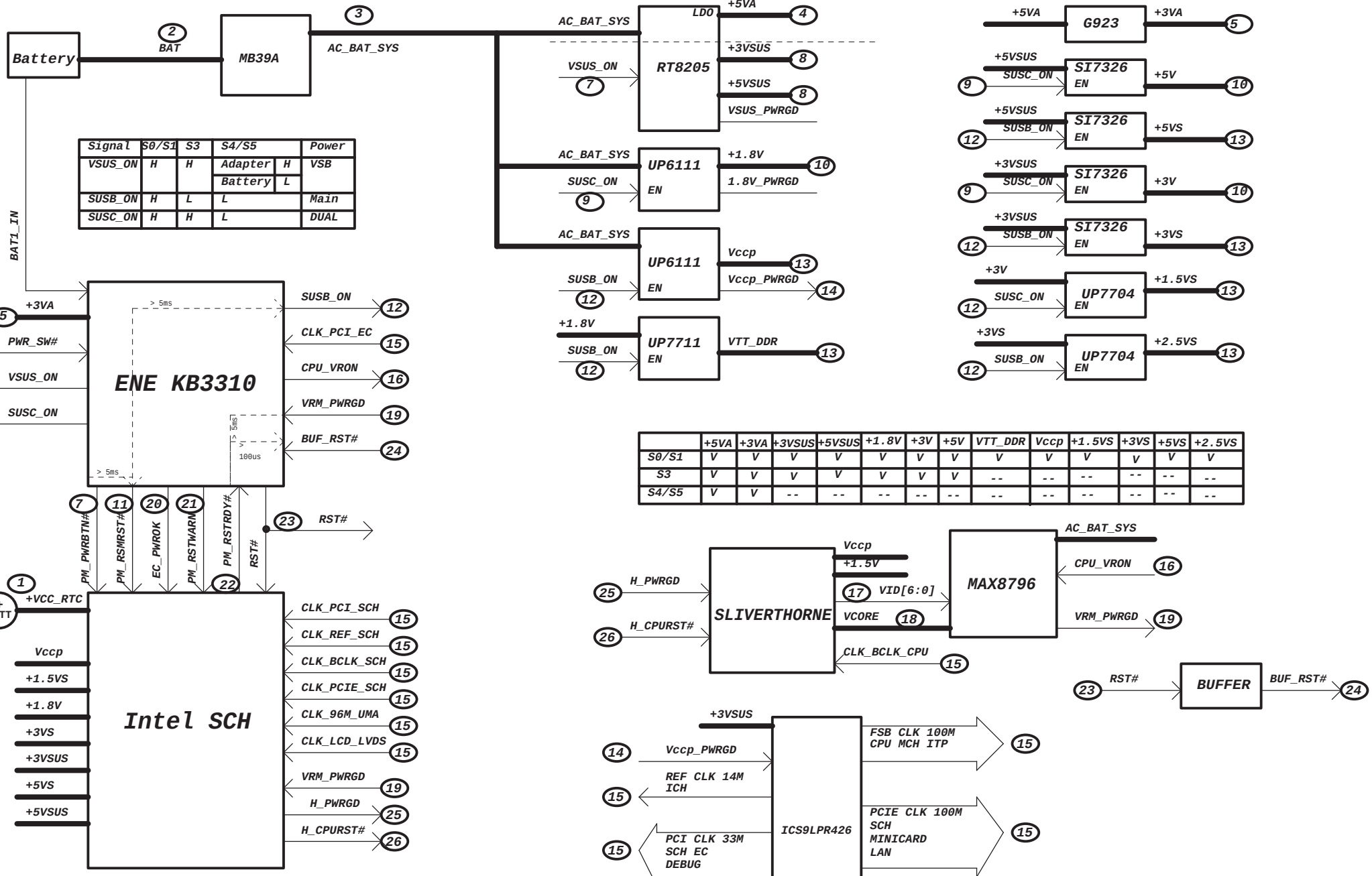


Signal	S0/S1	S3	S4/S5		Power
VSUS_ON	H	H	Adapter	H	VSB
			Battery	L	
SUSB_ON	H	L	L		Main
SUSC_ON	H	H	L		DUAL

	+5VA	+3VA	+3VSUS	+5VSUS	+1.8V	+3V	+5V	VTT_DDR	Vccp	+1.5VS	+3VS	+5VS	+2.5VS
S0/S1	V	V	V	V	V	V	V	V	V	V	V	V	V
S3	V	V	V	V	V	V	V	--	--	--	--	--	--
S4/S5	V	V	--	--	--	--	--	--	--	--	--	--	--

0106 1025

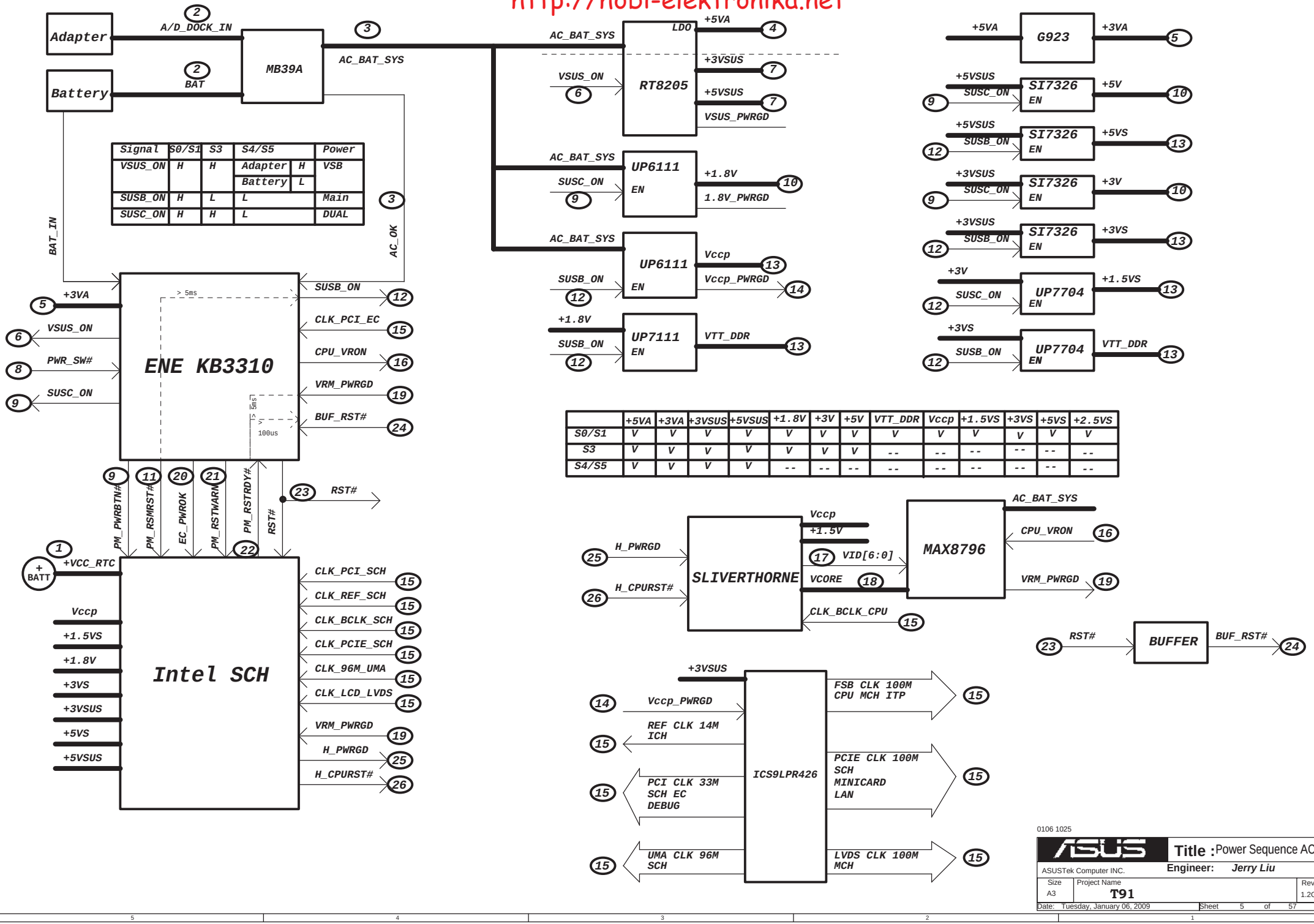
ASUSTek Computer INC.

Title : Power Sequence DC

Engineer: Jerry Liu

Size	Project Name	Rev
A3	T91	1.2G

Date: Tuesday, January 06, 2009 Sheet 4 of 57



0106 1025

ASUSTek Computer INC.	Title : Power Sequence AC
	Engineer: Jerry Liu
Size: A3	Project Name: T91
Rev: 1.2G	
Date: Tuesday, January 06, 2009	Sheet 5 of 57

S4/S5 to S0(Adapter Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS_ON=0, SUSB_ON=0, SUSC_ON=0, A20GA=X, KBRST=X, CPU_VRON=0, ICH_PWROK=0, RSTWARN=0, and PM_RSMRST#=0, RESET#=0.

1.Waiting for AC_OK until adaptor power is good, then

2.At least 5mS after AC_OK is asserted, EC asserts VSUS_ON to enable VSUS power.

3.At least 20mS after VSUS power is stable, waiting for PWR_SW# until user is pressed. (Or waiting for SCH deasserted SLPRDY#, too?)

4.EC asserts RSTWARN.

5.SUSC_ON is asserted at least 20mS (de-bounce) after receiving PWR_SW#.

6.PM_RSMRST# is deasserted at least 5mS after SUSC power is stable.

7.At least 5mS after PM_RSMRST# is deasserted, SUSB_ON is enabled.

8.CPU_VRON is deasserted at least 100mS after SUSB power is stable.

9.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.

10.At least 10mS after receiving CPUPWR_GD, PM_PWROK is asserted, and then deasserts RSTWARN.

11.Waiting for RSTRDY# until deasserted by SCH.

12.RESET# can be deasserted at lease 100uS after PM_PWROK is asserted.

S4/S5 to S0(Battery Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS_ON=0, SUSB_ON=0, SUSC_ON=0, A20GA=X, KBRST=X, CPU_VRON=0, ICH_PWROK=0, RSTWARN=0, and PM_RSMRST#=0, RESET#=0.

1.Waiting for BAT_IN until battery power is good, then

2.Waiting for PWR_SW# until user is pressed.

3.EC asserts VSUS_ON to enable VSUS power.

4.At least 20mS after VSUS power is stable.

5.EC asserts RSTWARN.

6.SUSC_ON is asserted at least 20mS (de-bounce) after receiving PWR_SW#.

7.PM_RSMRST# is deasserted at least 5mS after SUSC power is stable.

8.At least 5mS after PM_RSMRST# is deasserted, SUSB_ON is enabled.

9.CPU_VRON is deasserted at least 10mS after SUSB power is stable.

10.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.

11.At least 10mS after receiving CPUPWR_GD, PM_PWROK is asserted, and then deasserts RSTWARN.

12.Waiting for RSTRDY# until deasserted by SCH.

13.RESET# can be deasserted at lease 100uS after ICH_PWROK is asserted.

S0 to S3/S4/S5

This sequence will occur when system entry to sleep states, or all power planes are shut down.

Initial EC state: VSUS_ON=1, SUSB_ON=1, SUSC_ON=1, CPU_VRON=1, ICH_PWROK=1, and PM_RSMRST#=1, RESET#=1, RSTWARN=0, PM_PWRBTN#=1.

1.Waiting for PWR_SW# until user is pressed (go to 2), or waiting for SLPRDY# is asserted (go to 3).

2.At least 20mS after PWR_SW# is asserted, EC asserts PM_PWRBTN# (50mS width) to SCH.

3.Waiting for SLPRDY# until has been asserted.

4.EC asserts RSTWARN to SCH to begin internal sequence.

5.SCH asserts RSTRDY# to EC to indicate all outstanding transactions are completed.

6.EC asserts RESET# after detecting RSTRDY# asserted.

7.EC deasserts ICH_PWROK.

8.EC deasserts SUSB_ON and CPU_VRON to turn off power planes.

This completes the entry to S3 (SLPMODE=1).

If SLPMODE=0, this indicates S4/S5 was the desired state, EC takes additional actions:

9.EC asserts PM_RSMRST#.

10.EC deasserts SUSC_ON to turn off the other power planes.

11.EC deasserts VSUS_ON if in battery mode.

12.EC deasserts RSTWARN to save more power.

Power Sequence Description: S3 to S0

This sequence will occur in S3, and wake event is detected by EC or SCH.

Initial EC state: SUSB_ON=0, CPU_VRON=0, ICH_PWROK=0, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=0.

1.For internal wake event, SCH deasserts SLPRDY# to EC, than 4.

2.For external wake event (PWR_SW#, keyboard wake up), then

3.EC asserts PM_PWRBTN# at least 50mS to wake SCH, and waiting for SLPRDY# until SCH deasserted.

4.EC asserts SUSB_ON to enable SUSB power.

5.CPU_VRON is deasserted at least 100mS after SUSB power is stable.

6.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.

7.At least 5mS after receiving CPUPWR_GD, ICH_PWROK is asserted.

8.Deasserts RSTWARN after ICH_PWROK is asserted.

9.RESET# can be deasserted 100uS after RSTWARN is deasserted.

Warm Reset (SLPMODE=1)

The warm reset sequence results in reset without remove any power supplies.

Initial EC state: SUSB_ON=1, CPU_VRON=1, ICH_PWROK=1, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=1.

1.SCH asserts RSTRDY# at the same time as driving SLPMODE=1 to EC.

2.EC asserts RSTWARN to SCH.

3.EC asserts RESET# for 1200mS to SCH after asserts RSTWARN.

4.EC deasserts RSTWARN.

5.EC deasserts RESET# after at least 100uS delay from RSTWARN.

Cold Reset (SLPMODE=0)

The cold reset sequence results in a power cycling of all but the RTC power well.

Initial EC state: SUSB_ON=1, CPU_VRON=1, ICH_PWROK=1, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=1.

1.SCH asserts RSTRDY# at the same time as driving SLPMODE=0 to EC.

2.EC asserts RSTWARN to SCH.

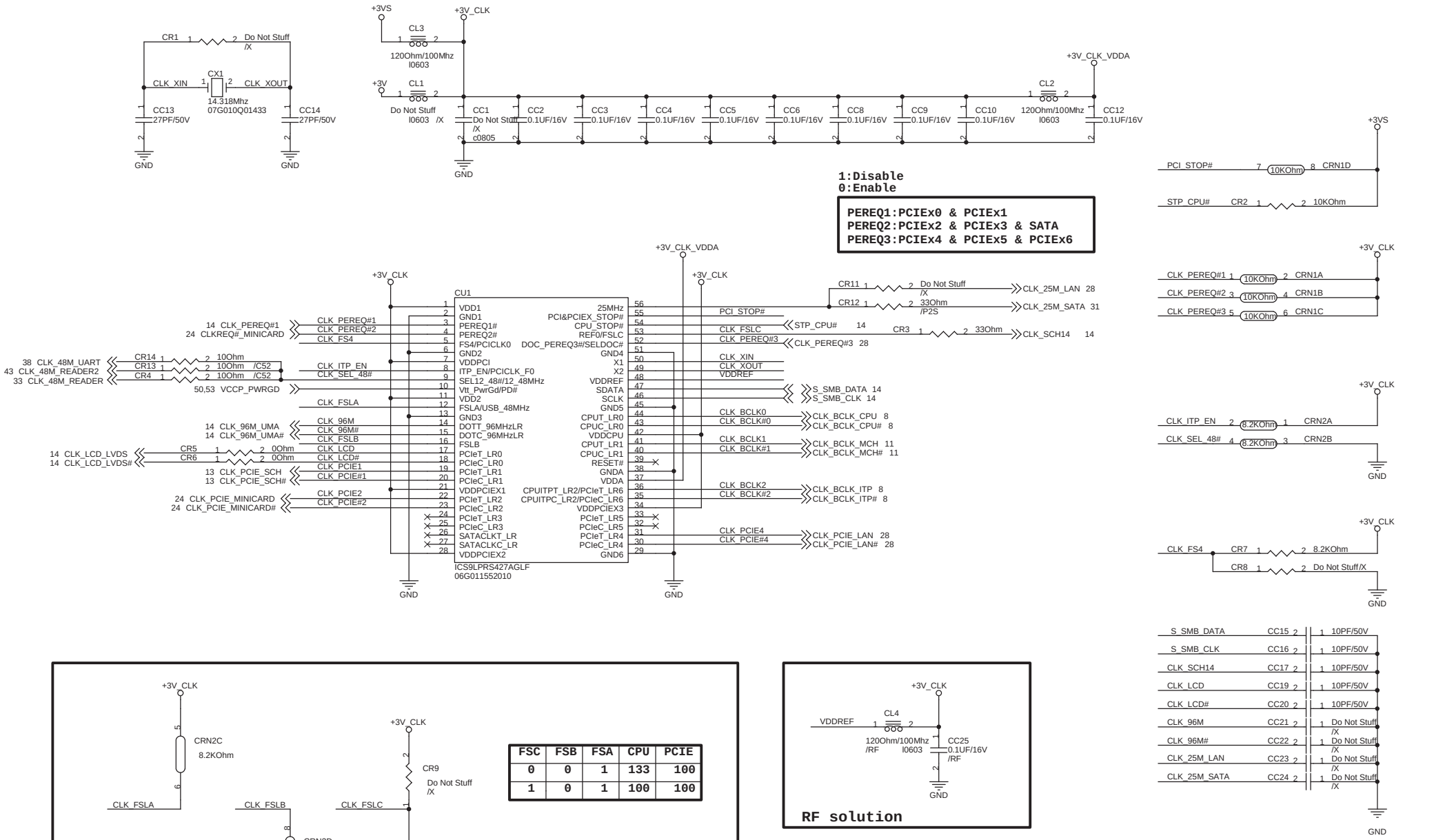
3.EC asserts RESET# to SCH after asserts RSTWARN.

4.EC deasserts PM_PWROK and disables SUSB_ON and CPU_VRON power.

5.EC asserts PM_RSMRST# after CPU_VRON power is off.

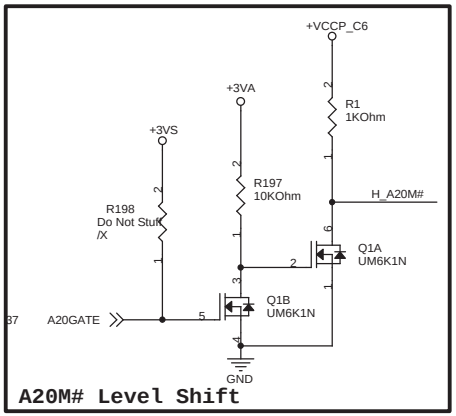
6.EC disables SUSC_ON power for 3~5 seconds.

7.S4/S5 to S0 sequence is automatically followed to bring the system back to S0 when SUSC_ON power is enable.

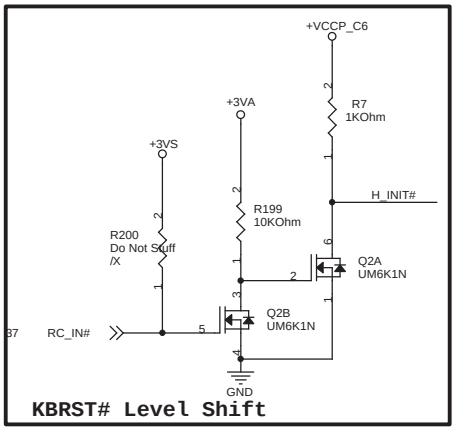


0106 1025

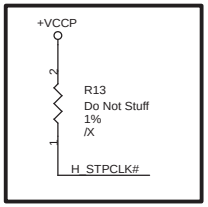
ASUSTek Computer INC.	Title : Clock Gen_ICS9LPRS427	
	Engineer: *Jerry Liu*	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 7 of 57	

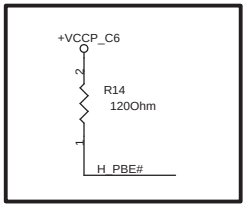


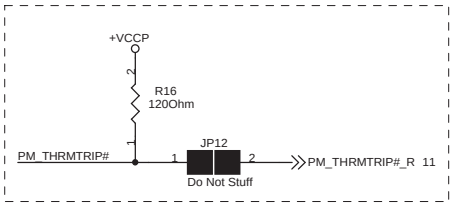
A20M# Level Shift

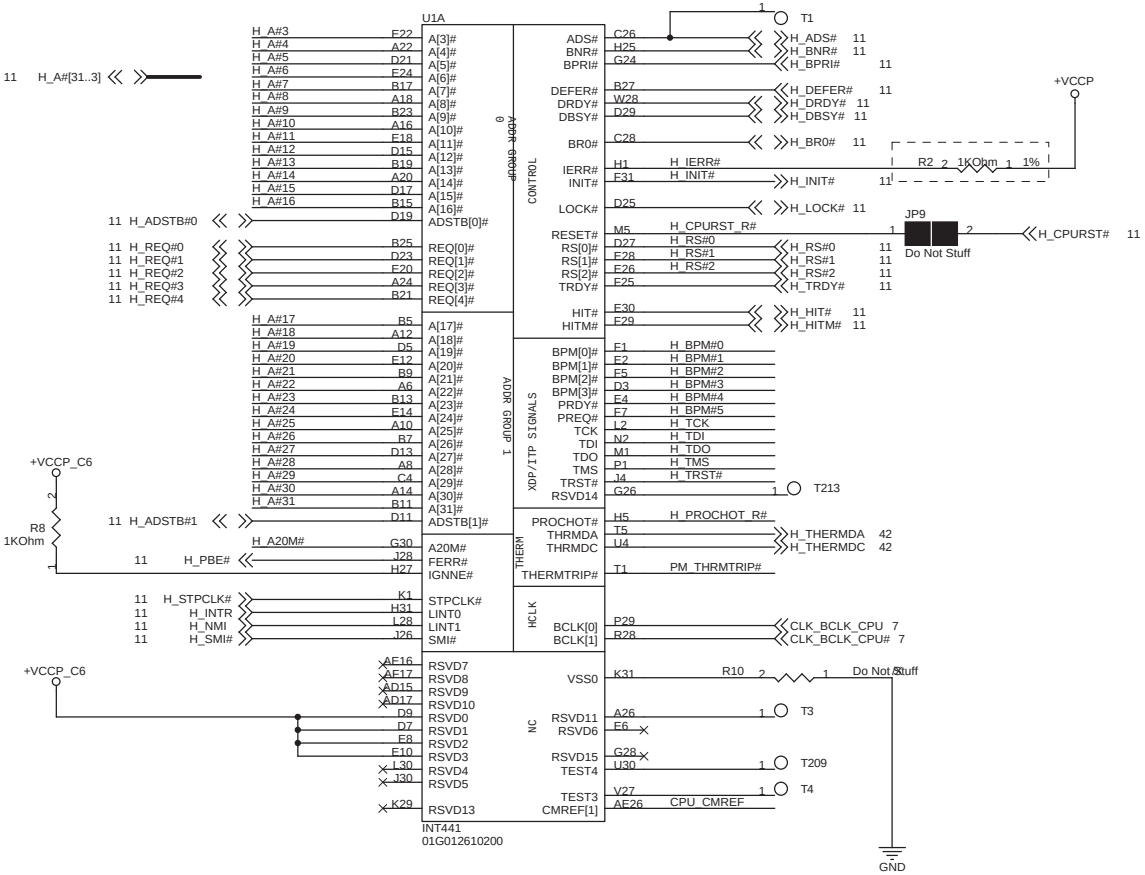


KBRST# Level Shift









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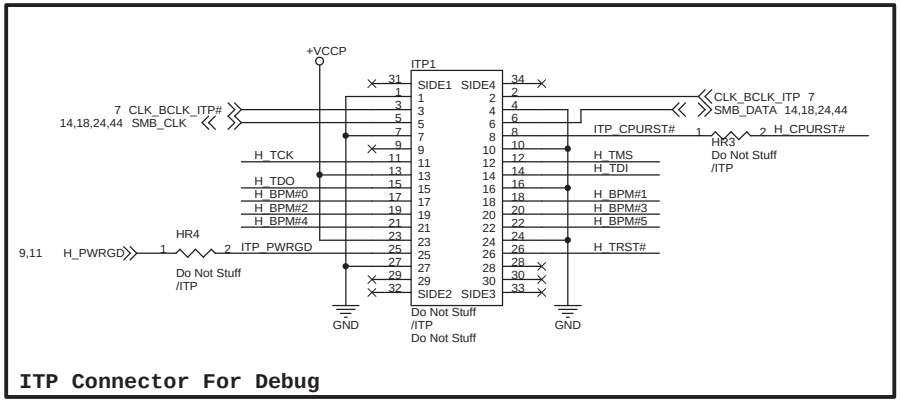
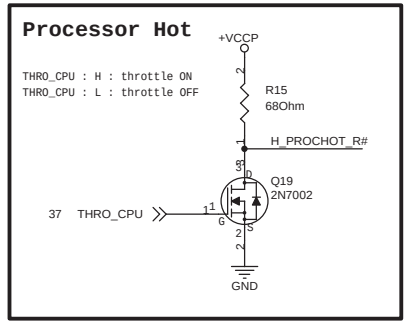
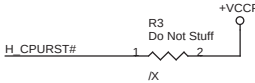
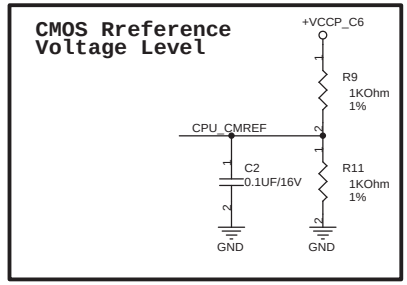
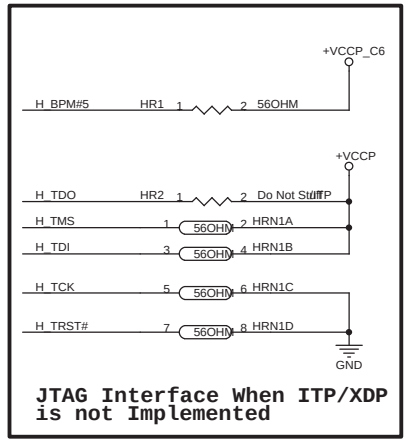


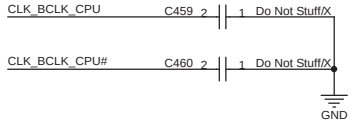
ITP Connector For Debug











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ASUSTeK COMPUTER INC

Title : CPU-SLIVERTHORNE(1)

Engineer: Jerry Liu

Size	Project Name	Rev
Custom	T91	1.2G

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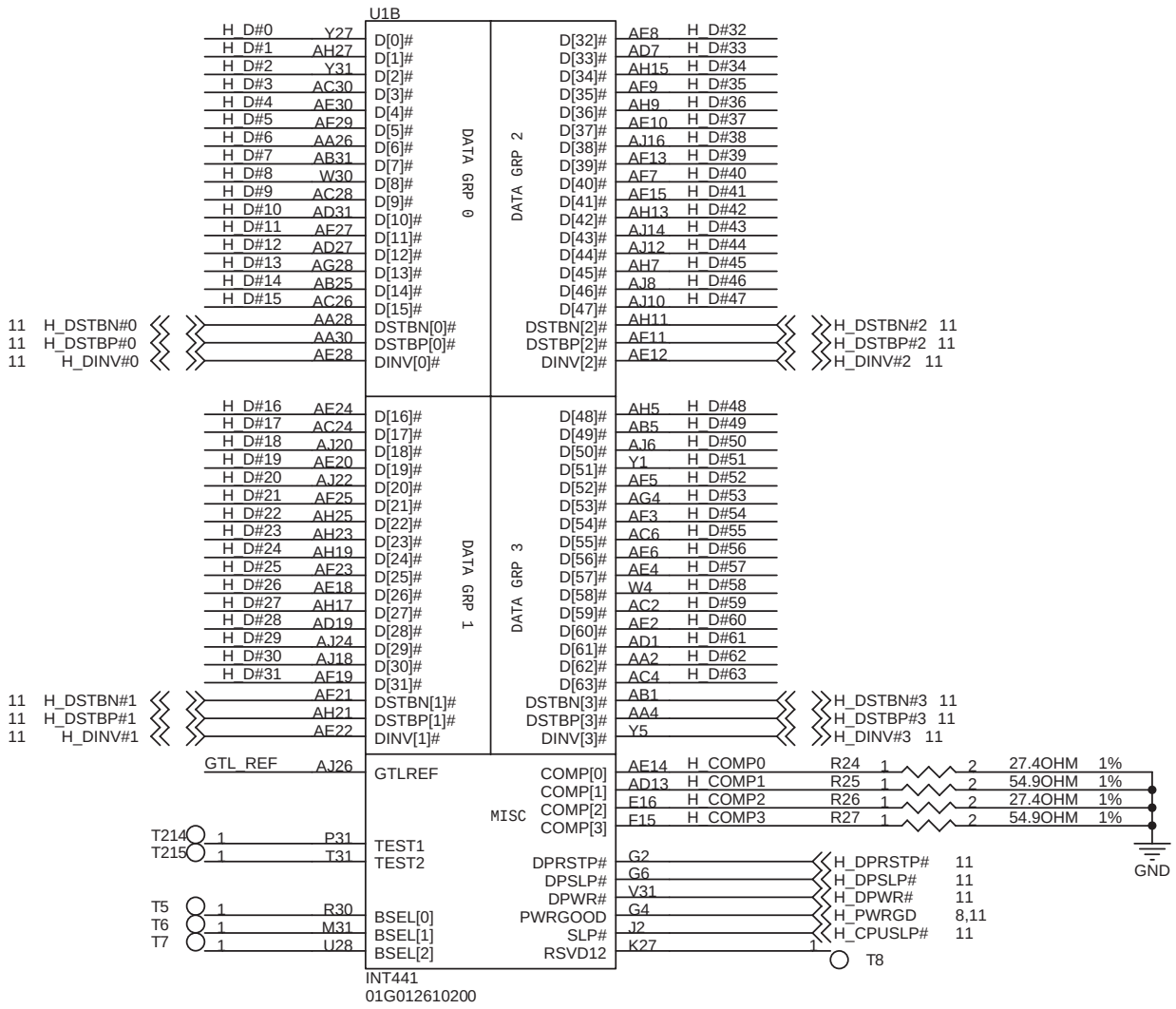
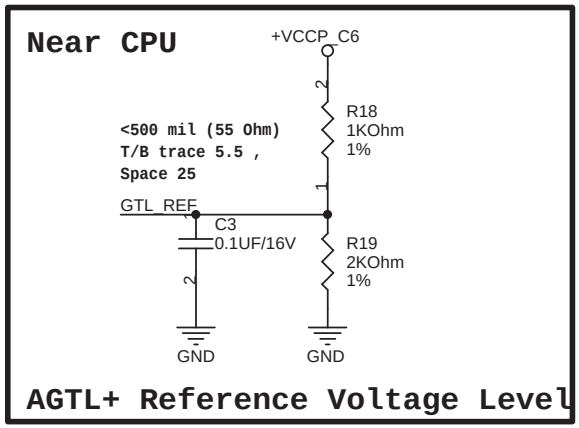


H_D#[63:0] H_D#[63:0] 11



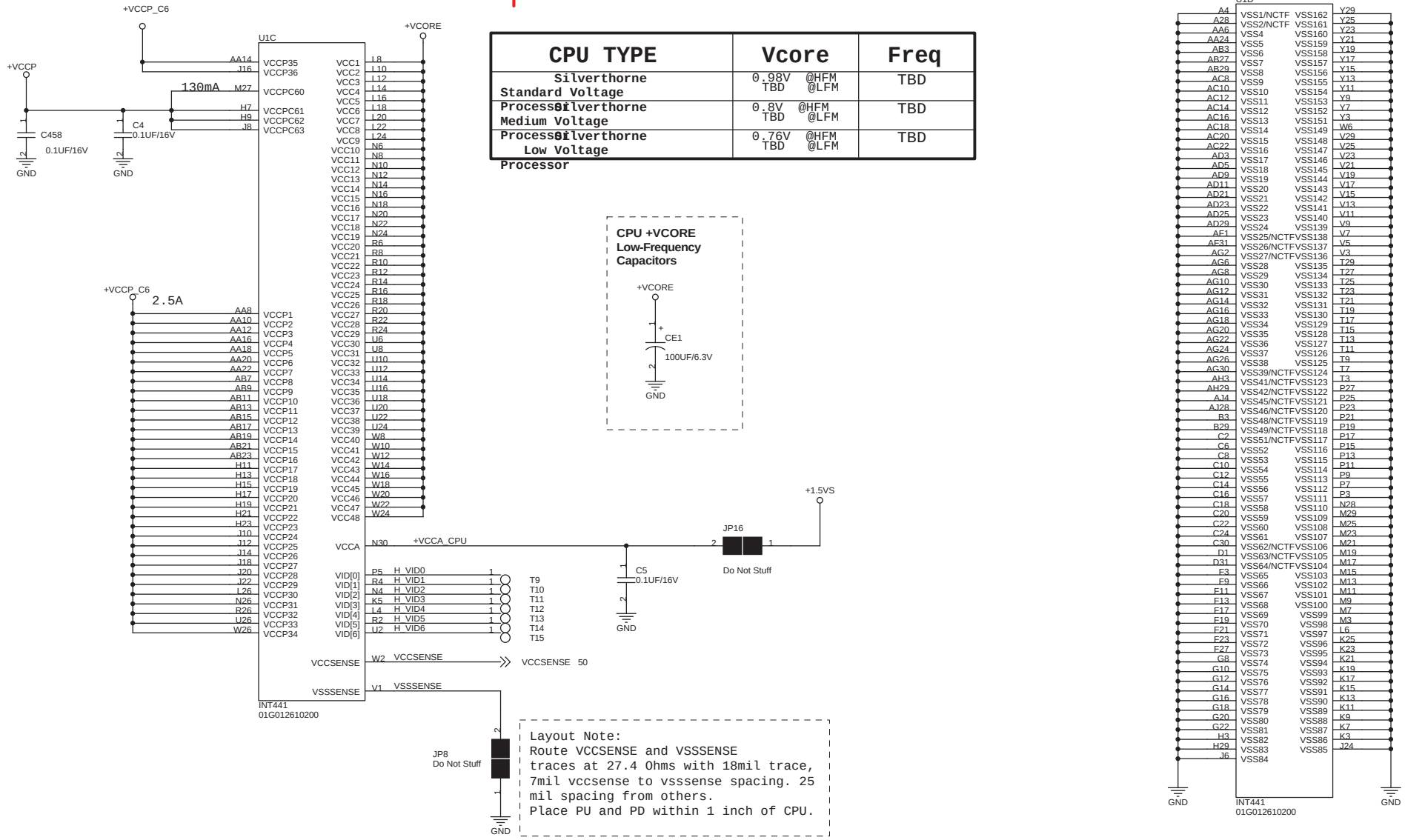
Layout Note
COMP 0 2 connect with Z0=27.4 ohm,L<0.5"
COMP 1 3 connect with Z0=55 ohm,L<0.5"

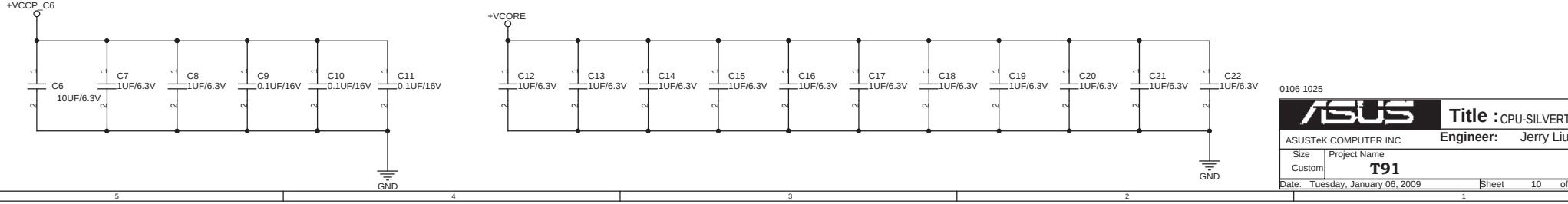
0106 1025

ASUSTeK COMPUTER INC	Title : CPU-SLIVERTHORNE(1)	
	Engineer: Jerry Liu	
Size: A4	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 9 of 57	

CPU TYPE	Vcore	Freq
Silverthorne Standard Voltage	0.98V @HFM TBD @LFM	TBD
Processor Silverthorne Medium Voltage	0.8V @HFM TBD @LFM	TBD
Processor Silverthorne Low Voltage	0.76V @HFM TBD @LFM	TBD

Processor





0106 1025

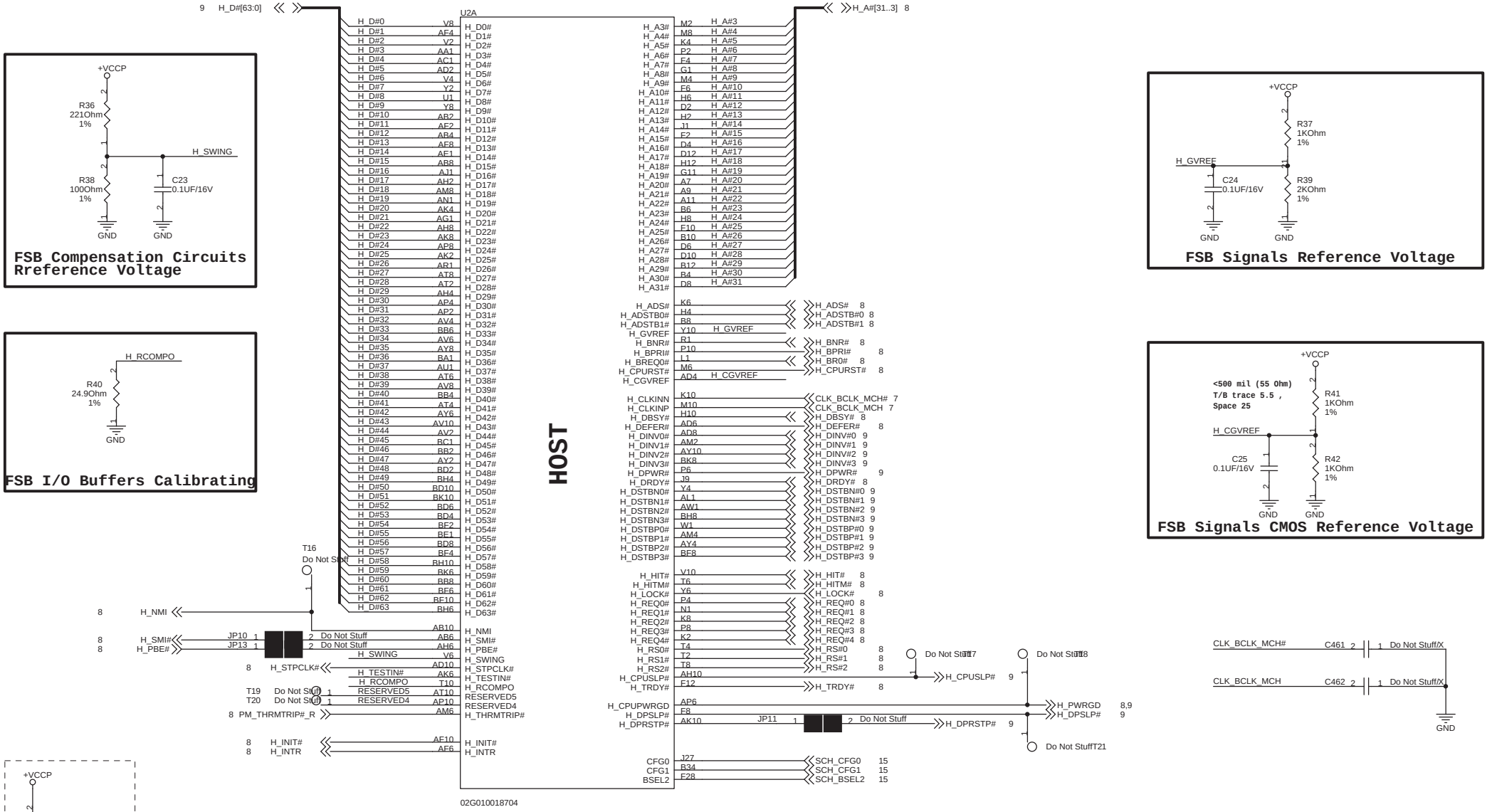
ASUSTeK COMPUTER INC

Title : CPU-SILVERTHORNE (2)

Engineer: Jerry Liu

Size	Project Name	Rev
Custom	T91	1.2G

Date: Tuesday, January 06, 2009 Sheet 10 of 57



US15W D2 stage : 02G010018704

0106 1025

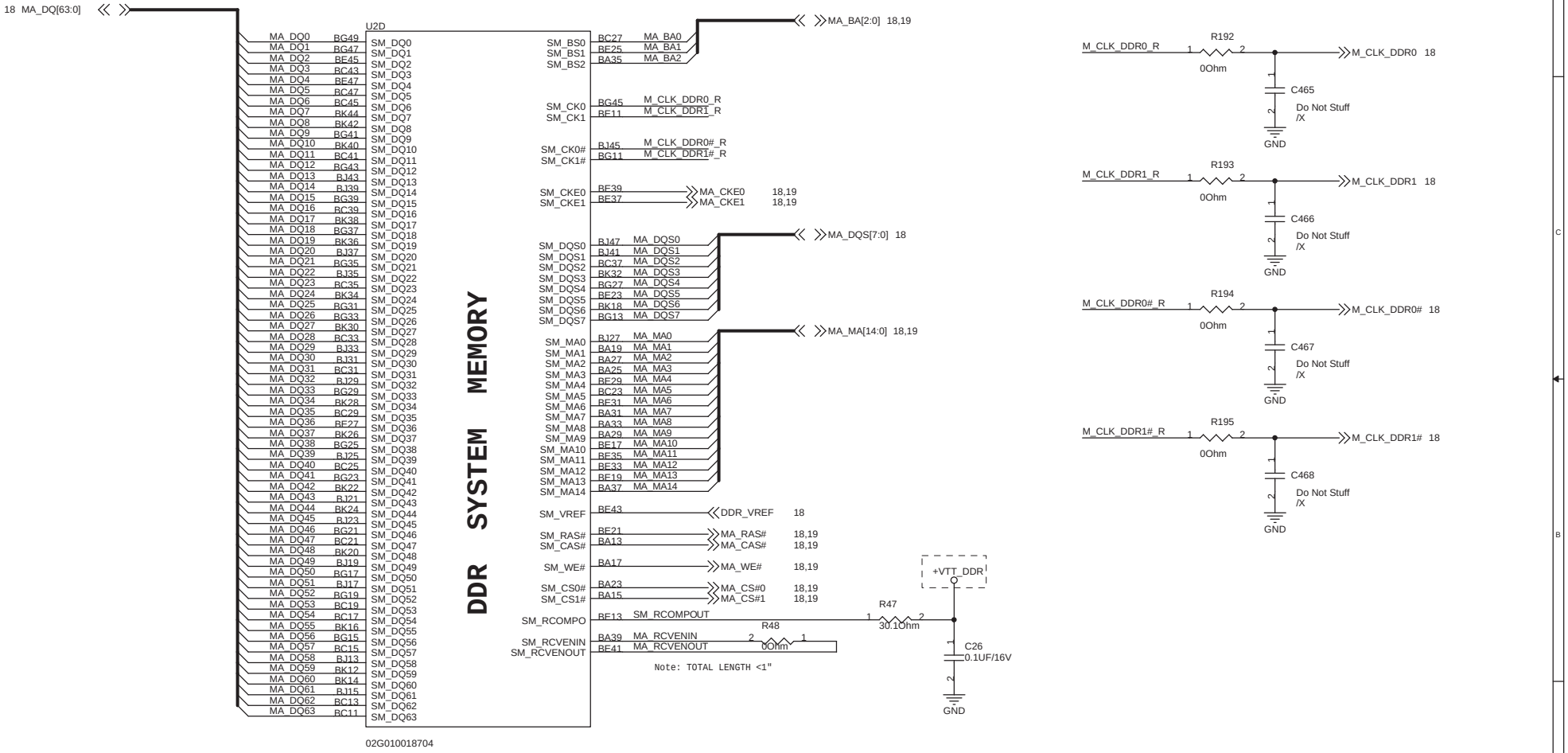
ASUSTeK COMPUTER INC

Title : Poulsbo_HOST (1)

Engineer: Jerry Liu

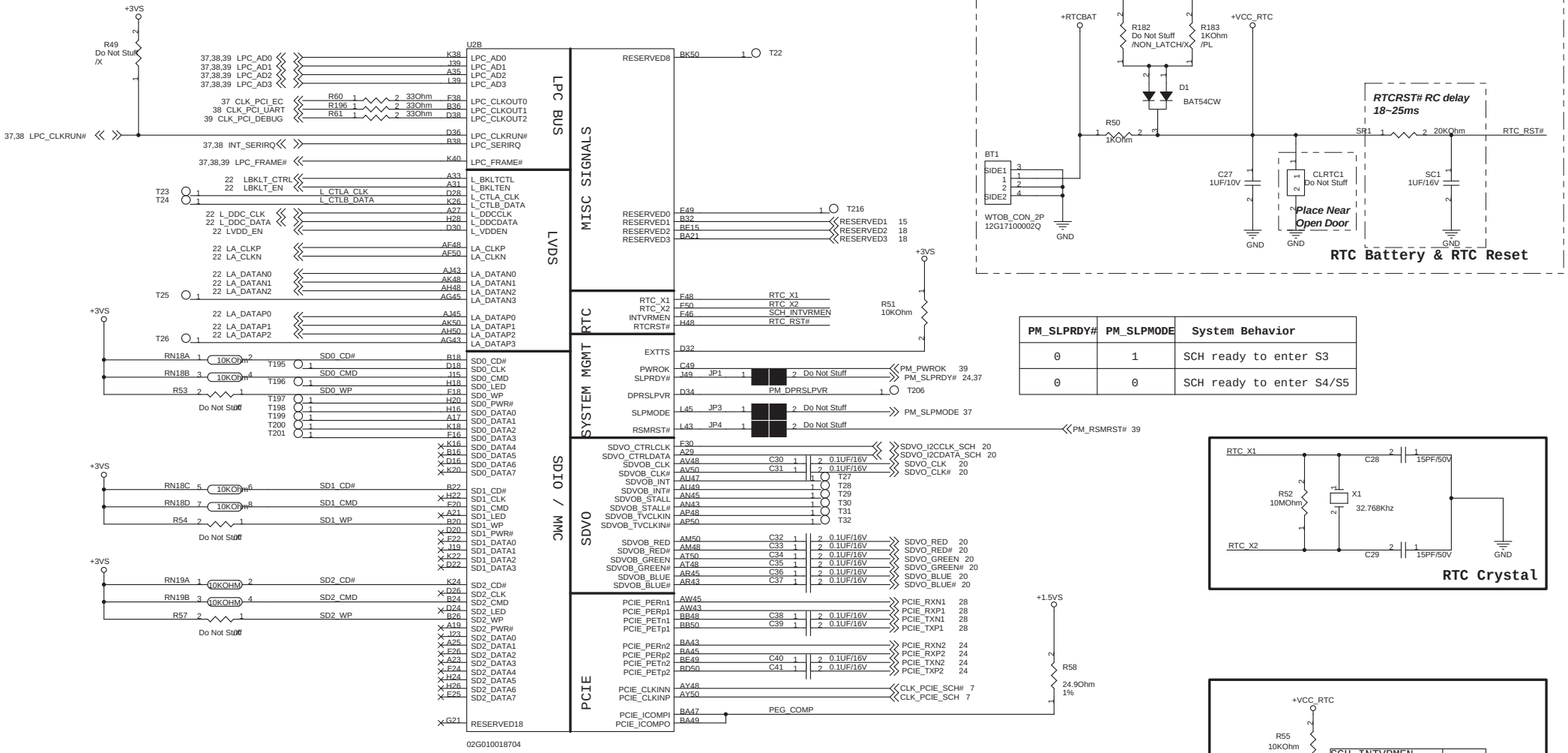
Size	Project Name	Rev
Custom	T91	1.2G

Date: Tuesday, January 06, 2009 Sheet 11 of 57

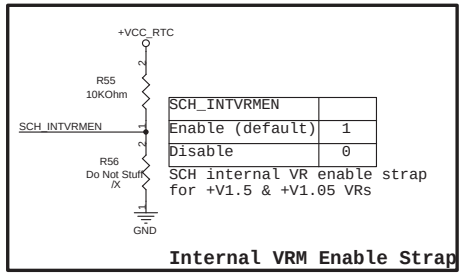


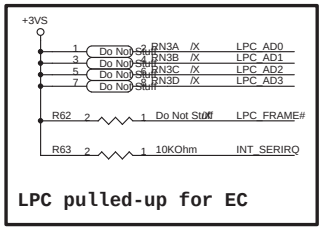
0106 1025

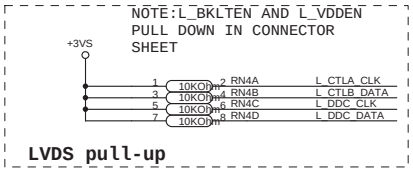
ASUSTek Computer INC.	Title : Poulsbo_DDR2 (2)	
	Engineer: *Jerry Liu*	
Size: Custom	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 12 of 57	



PM_SLPRDY#	PM_SLPMODE	System Behavior
0	1	SCH ready to enter S3
0	0	SCH ready to enter S4/S5



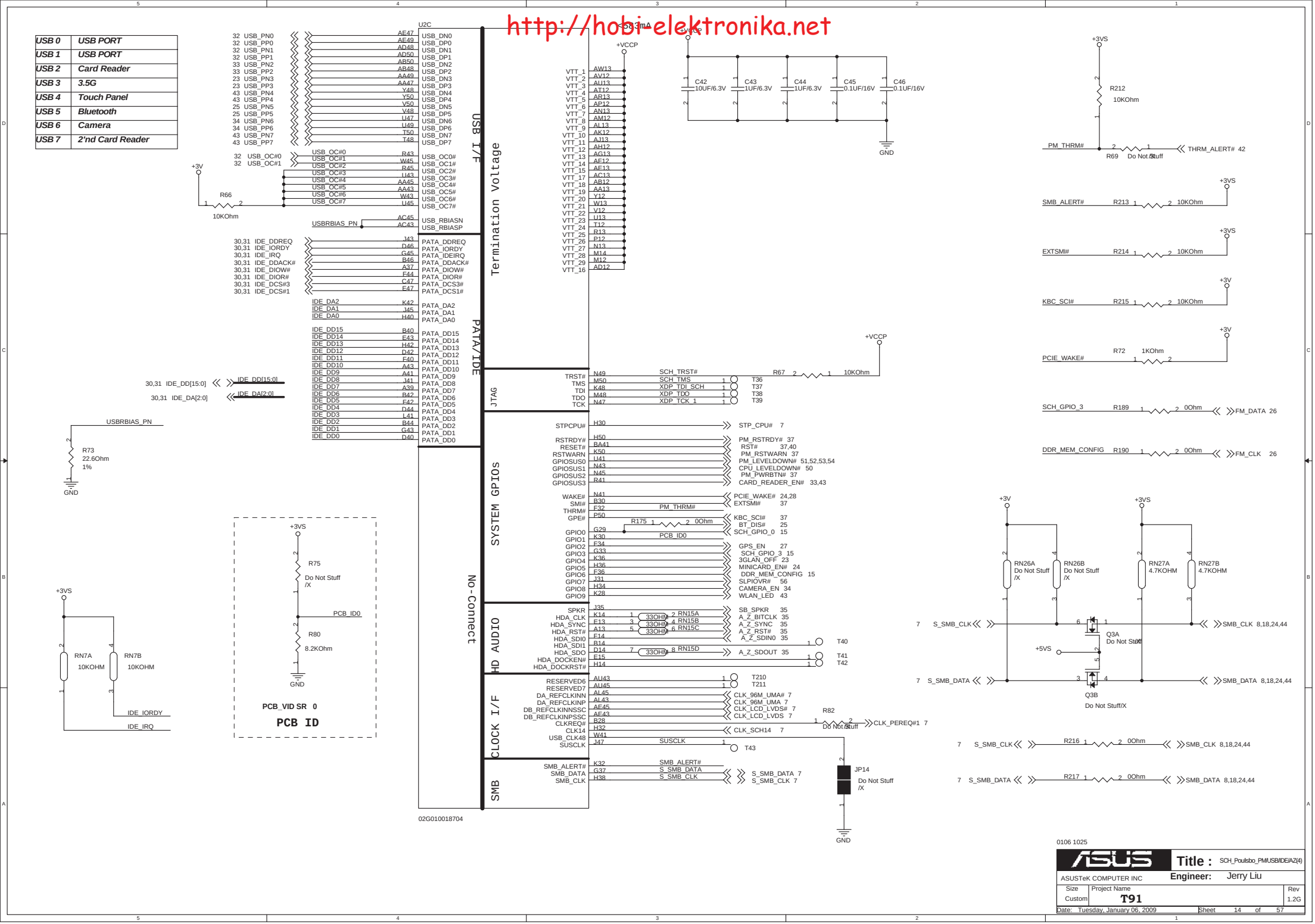




0106 1025

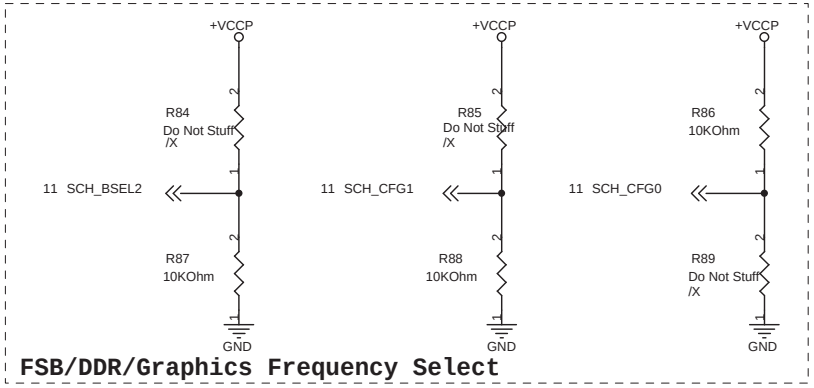
ASUSTeK COMPUTER INC	Title : Poulsbo_LVDS/SDVO	
	Engineer: Jerry Liu	
Size: Custom	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 13 of 57	

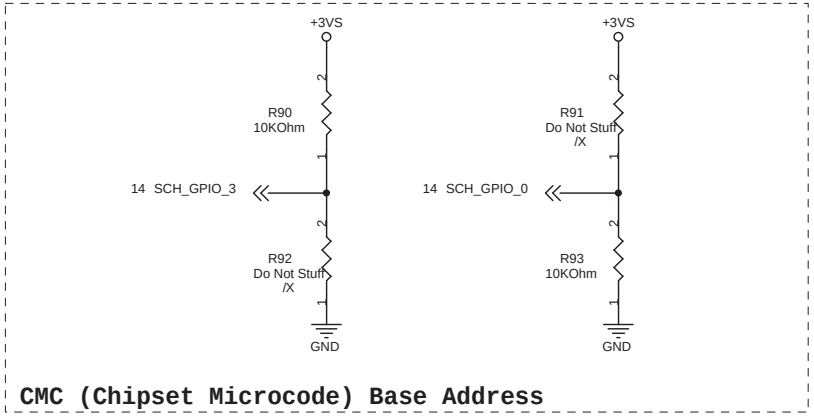
USB 0	USB PORT
USB 1	USB PORT
USB 2	Card Reader
USB 3	3.5G
USB 4	Touch Panel
USB 5	Bluetooth
USB 6	Camera
USB 7	2'nd Card Reader

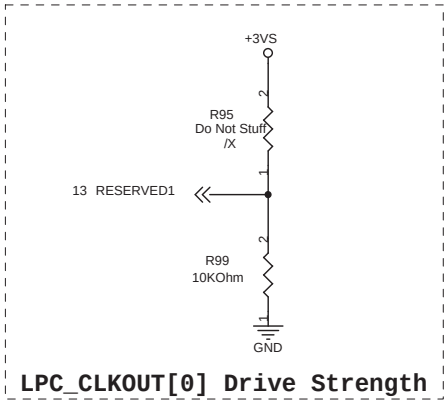


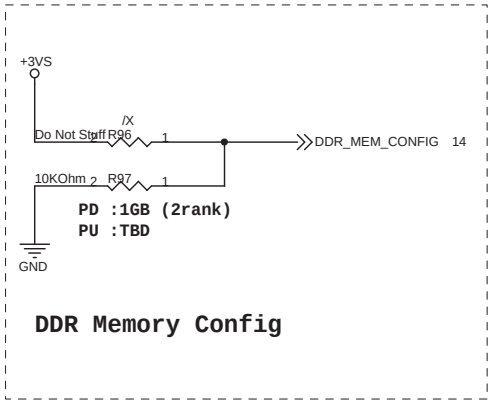
0106 1025

ASUSTeK COMPUTER INC	Title :	SCH_Poulsbo_PMUSB/IDE/AZ(4)
	Engineer:	Jerry Liu
Size: Custom	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 14 of 57	





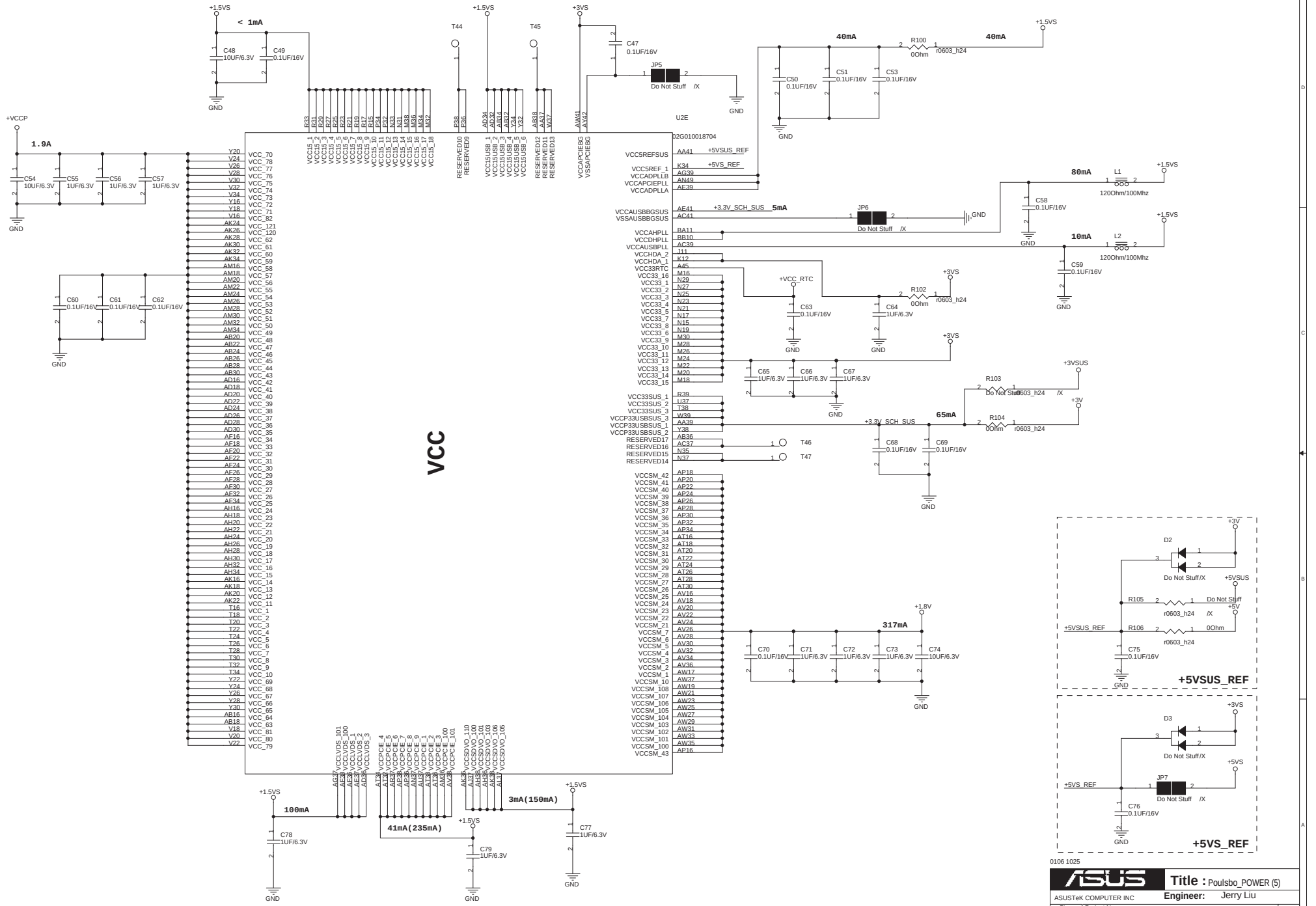




Strap Function	Singal Name			Strap		Comment
FSB/DDR Frequency Select Graphics Frequency Select	SCH_BSEL2	SCH_CFG1	SCH_CFG0	Gfx_Freq	FSB	Note: Clock Frequencies are in Mhz Default Frequency determined by FSB speed
	0	0	0	200	400	
	0	0	1	200	533	
CMC (Chipset Microcode) Base Address	GPIO3	GPIO0		Address		Selects the starting address that the CMC will use to start fetching code. (GPIO3 is the most significant)
	0	0		0xFFFB0000		
	0	1		0xFFFC0000		
	1	0		0xFFFD0000 (default)		
	1	1		0xFFFE0000		
LPC_CLKOUT[0] Buffer Strength	RESERVED1			Value		Selects the drive strength of the LPC_CLKOUT[0] clock.
	0			Reserved		
	0			1 Load (Default)		
	1			Reserved		
	1			2 Loads		

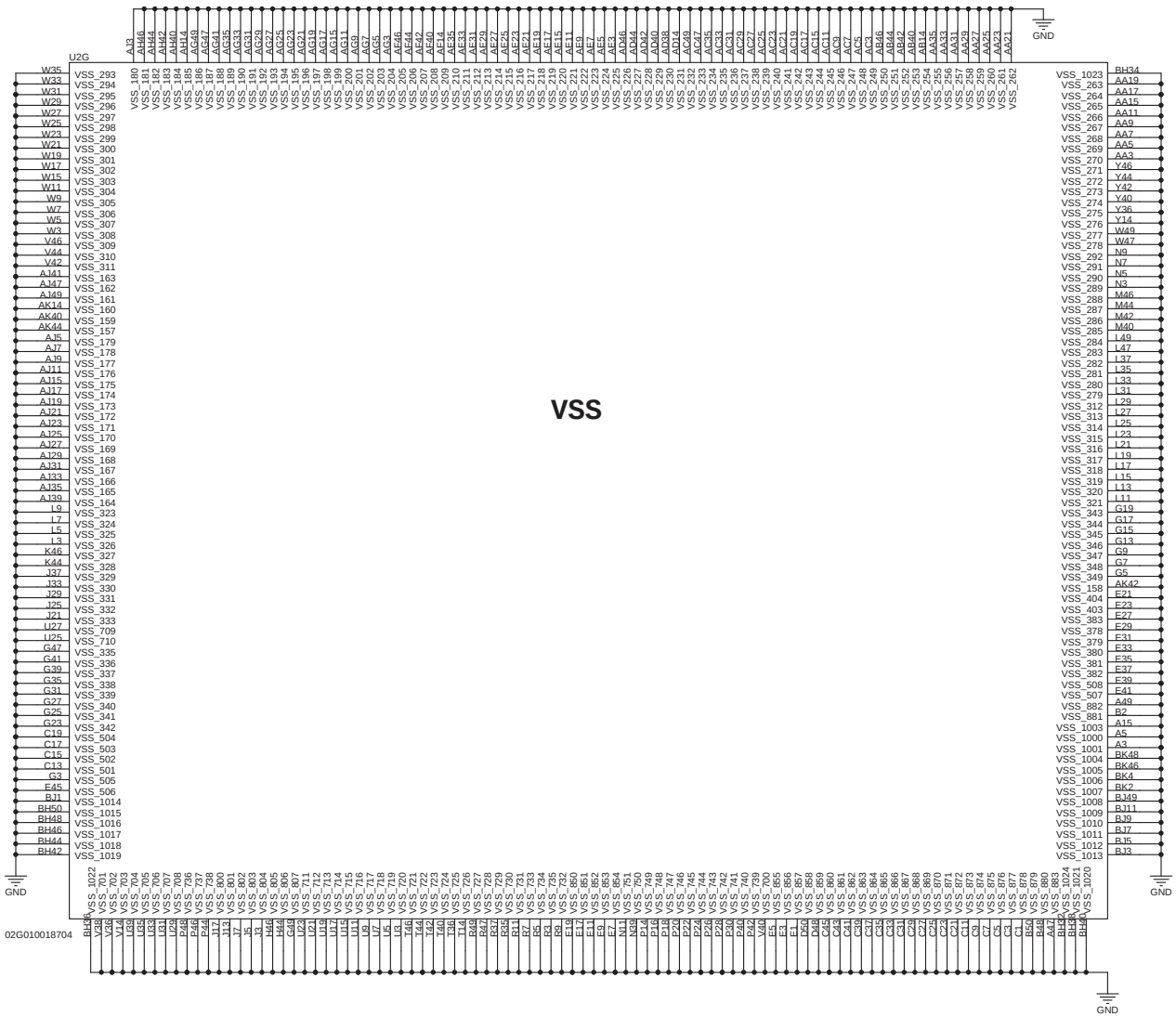
0106 1025

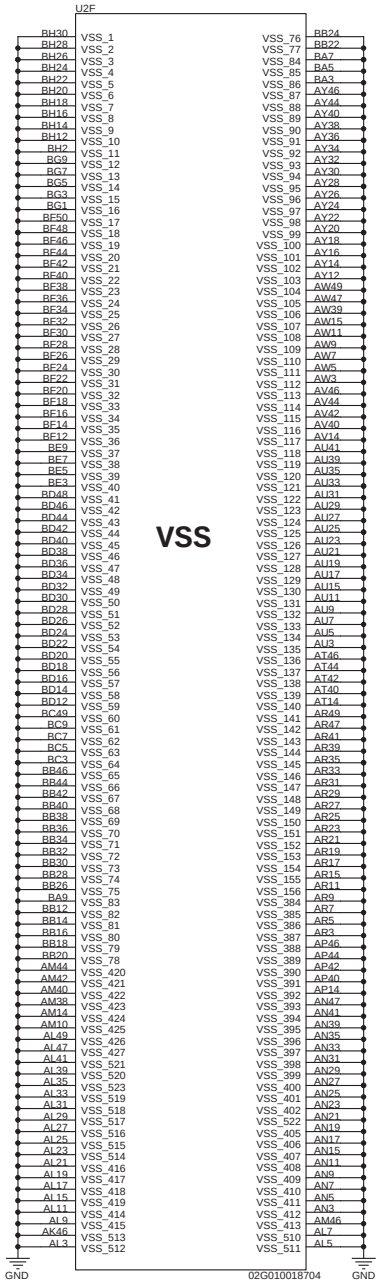
ASUSTek Computer INC.	Title : POULSBO_STRAP(5)	
	Engineer: *Jerry Liu*	
Size: B	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 15 of 57	



0106 1025

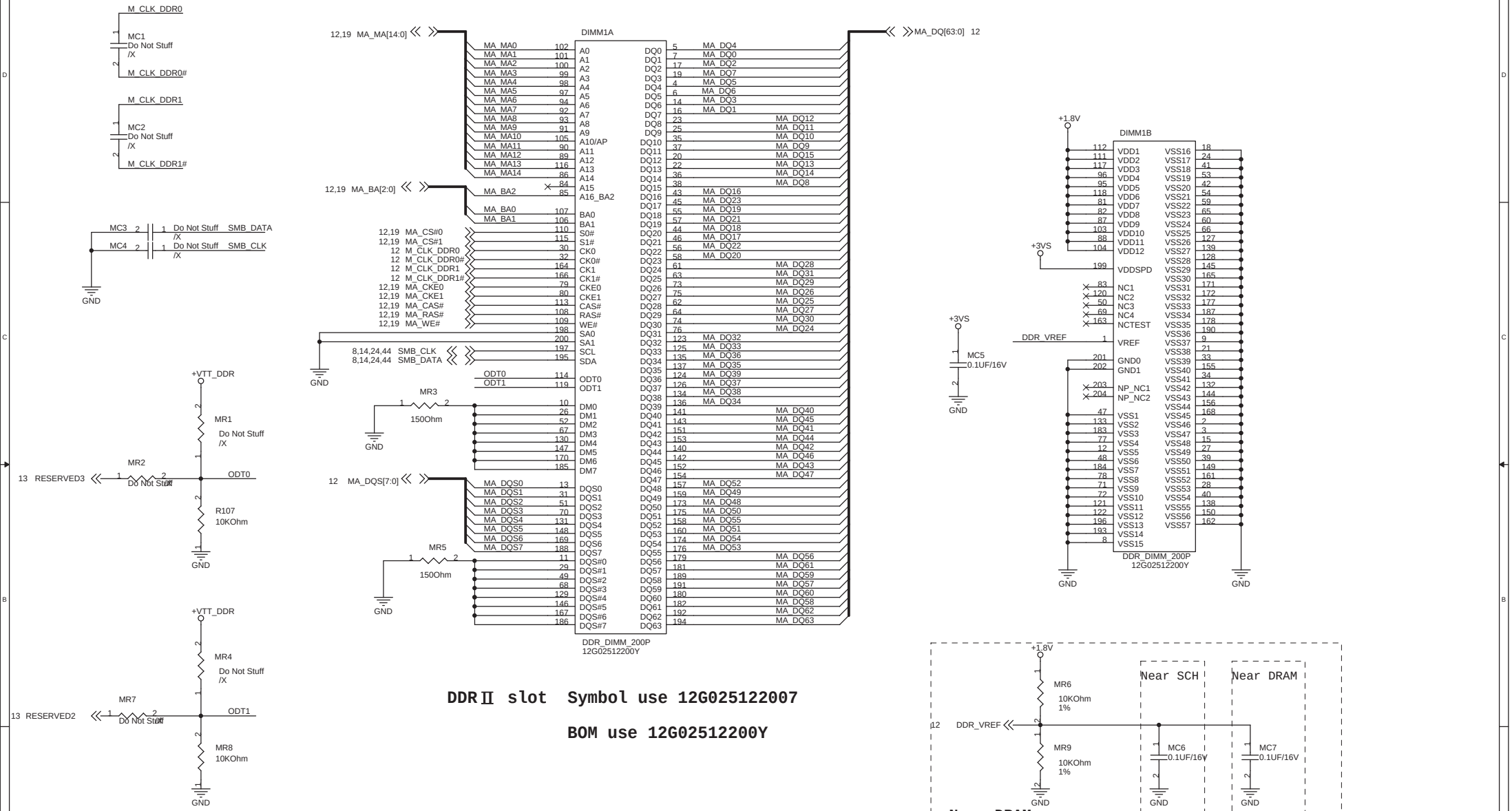
ASUSTeK COMPUTER INC	Title : Poulsbo_POWER (5)	
	Engineer: Jerry Liu	
Size: Custom	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 16 of 57	





0106 1025

ASUSTeK COMPUTER INC	Title : POULSBO_GND (6)	
	Engineer: Jerry Liu	
Size: Custom	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 17 of 57	

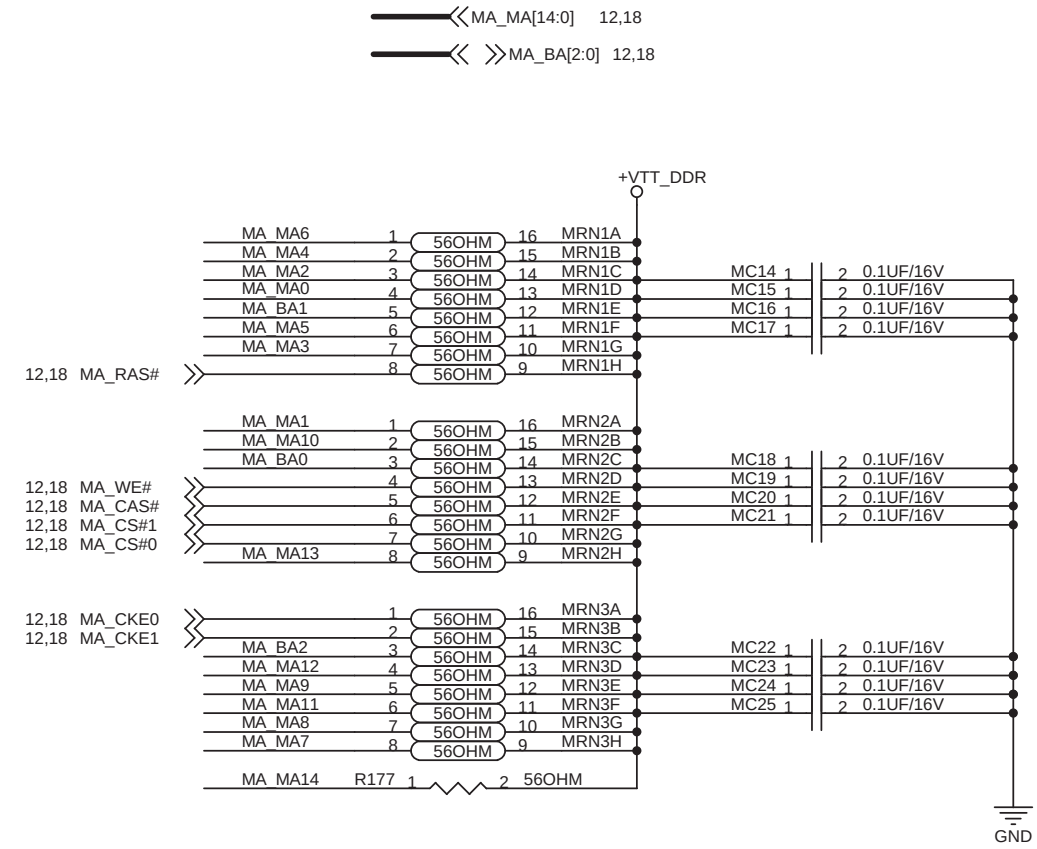


DDR Ⅱ slot Symbol use 12G025122007

BOM use 12G02512200Y

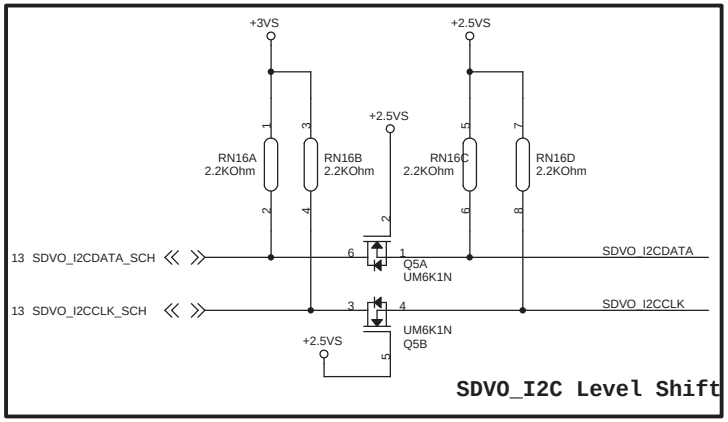
0106 1025

ASUSTek Computer INC.	Title : DDR2 SODIMM	
	Engineer: *Jerry Liu*	
Size: A3	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 18 of 57	



0106 1025

ASUSTek Computer INC.	Title : DDR2_Termination	
	Engineer: *Jerry Liu*	
Size: A4	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 19 of 57	



13 SDVO_RED
13 SDVO_RED#
13 SDVO_GREEN
13 SDVO_GREEN#
13 SDVO_BLUE
13 SDVO_BLUE#
13 SDVO_CLK
13 SDVO_CLK#

+2.5VS — L3 120Ohm/100Mhz — +2.5VS_DVDD_CH

C82 10UF/6.3V, C83 0.1UF/16V, C84 0.1UF/16V, C85 0.1UF/16V — GND

R121 10KOhm 1% — GND

U5 — CH7317A-TF-TR

1 T1	64 AVDD3	48 NC8	
2 SD_DDC	63 SDVO_CLK-	47 NC9	
3 SC_DDC	62 SDVO_CLK+	46 NC10	
4 SD_PROM	61 AGND3	45 AGND_PLL2	
5 SC_PROM	60 SDVO_B-	44 POCLK-	
6 DVDD1	59 SDVO_B+	43 POCLK+	
7 RESET*	58 AVDD2	42 AVDD_PLL2	
8 AS	57 SDVO_G-	41 AVDD_PLL1	
9 DGND1	56 SDVO_G+	40 XO	
10 DGND2	55 AGND2	39 XI/FIN	
11 SPD	54 SDVO_R-	38 AGND_PLL1	
12 SPC	53 SDVO_R+	37 DGND3	
13 DVDD2	52 AVDD1	36 VSYNC	
14 BSCAN	51 T2	35 DVDD3	
15 T3	50 RPLL	34 CHSYNC	
16 VDAC2	49 AGND1	33 V5V	
17 GDAC2	18 NC1	19 VDAC1	20 DACA[2]
21 NC2	22 NC3	23 GDAC1	24 DACA[1]
25 NC4	26 NC5	27 VDAC0	28 DACA[0]
29 NC6	30 NC7	31 GDAC0	32 ISET

21 CRT_DDC_DATA
21 CRT_DDC_CLK

+2.5VS — R115 Do Not Stuff /X — High:70H
+2.5VS — R116 Do Not Stuff /X — Low:72H
2,5,8,16,26,27,28,30,31,37,38,40 BUF_RST#
+2.5VS_DVDD_CH
GND
SDVO_I2CDATA
SDVO_I2CCLK
+2.5VS_DVDD_CH
IntPD
T191Do Not Stuff

+2.5VS_SDVO_PLL — L4 120Ohm/100Mhz — +2.5VS
C86 0.1UF/16V, C87 10UF/6.3V — GND
XO_SDVO
XIN_SDVO
GND
CRT_VSYNC — CRT_VSYNC 21
+2.5VS_DVDD_CH
CRT_HSYNC — CRT_HSYNC 21

+3VS — L5 120Ohm/100Mhz
C88 0.1UF/16V, C89 10UF/6.3V — GND

+3VS — L6 120Ohm/100Mhz
+3VS_VDAC_CH
C91 0.1UF/16V, C92 0.1UF/16V, C93 10UF/6.3V — GND

CRT_ISET — R119 1.2KOhm 1% — GND

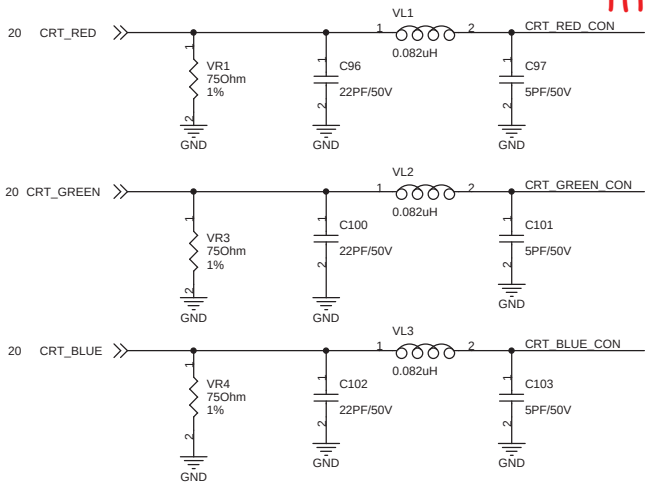
21 CRT_RED
21 CRT_GREEN
21 CRT_BLUE

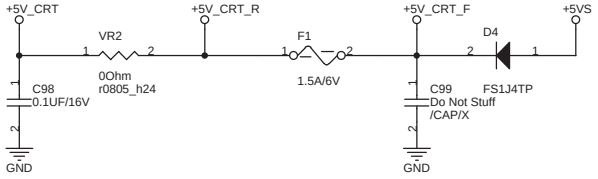
R118 Do Not Stuff /X
XIN_SDVO — XO_SDVO
07G010712701 27Mhz — X2
C94 16PF/50V, C95 16PF/50V — GND

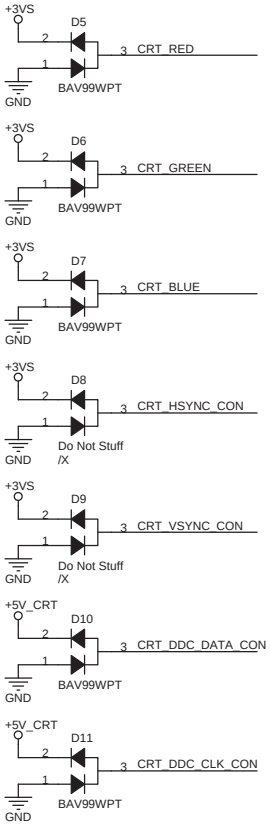
XTAL Height 1mm

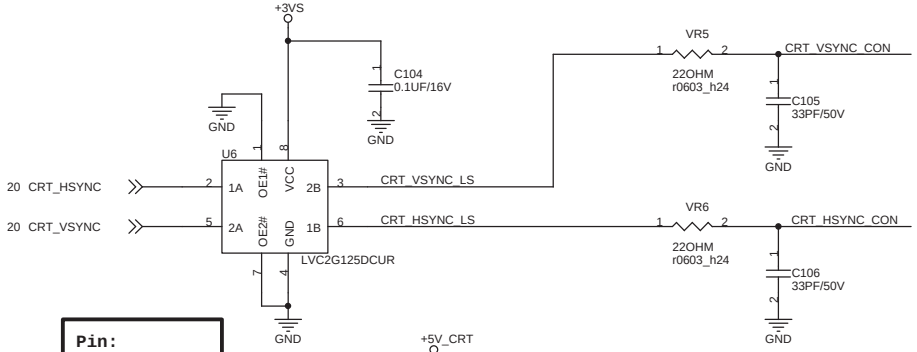
0106 1025

ASUSTek COMPUTER INC	Title : CH7317_SDVO_CRT	
	Engineer: *Leon_Sun*	
Size: A3	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 20 of 57	







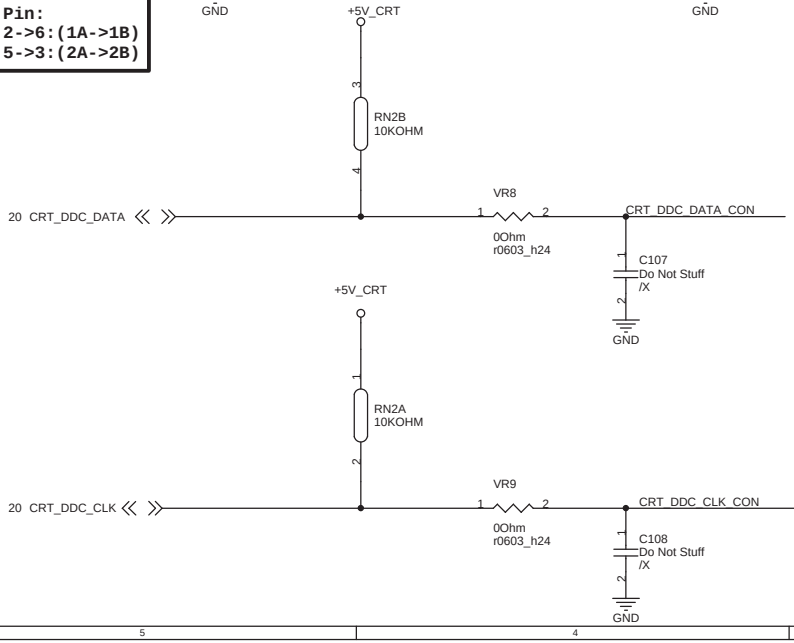


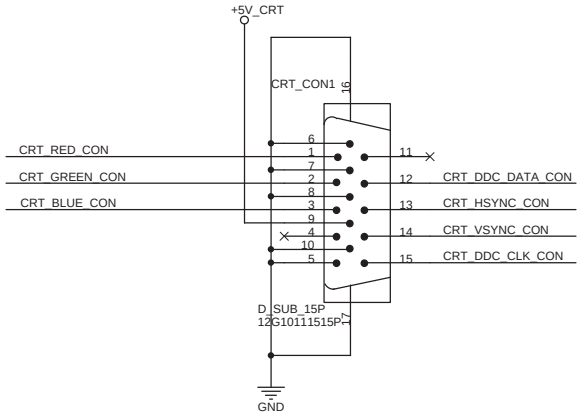
Pin:
2->6:(1A->1B)
5->3:(2A->2B)

C105 C106 for EA measurement

U6上:VR5 & VR6-->22 OHM
U6 /X :VR5 & VR6 -->0 OHM

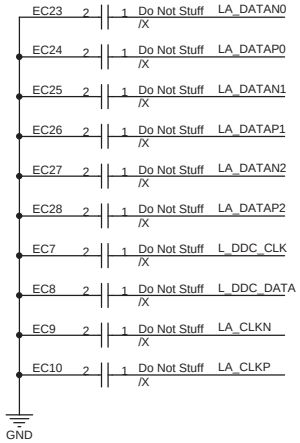
BUS BUFFER:
Unidirectional buffers (high impedance buffers) are required on both HSYNC and VSYNC to prevent potential electrical overstress and illegal operation of the GMCH, since some display monitors may attempt to drive HSYNC and VSYNC signals back to GMCH.

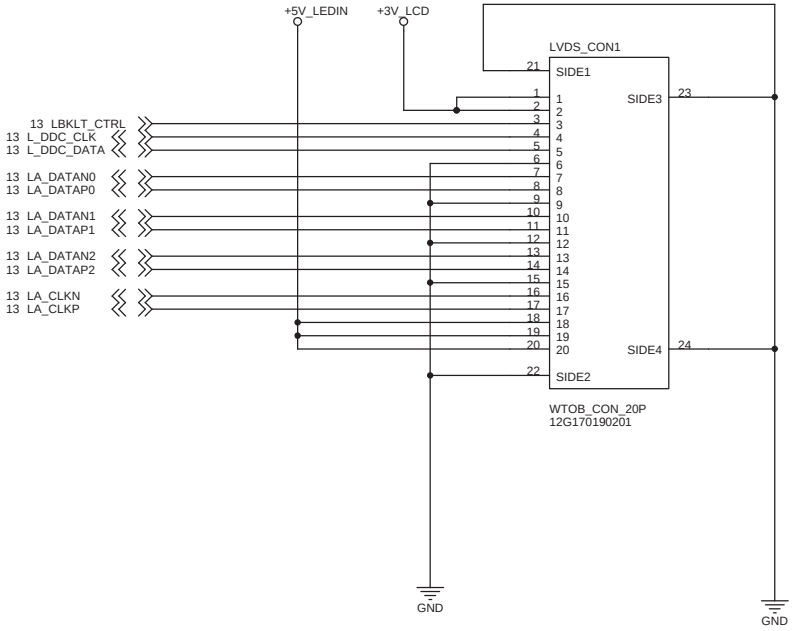


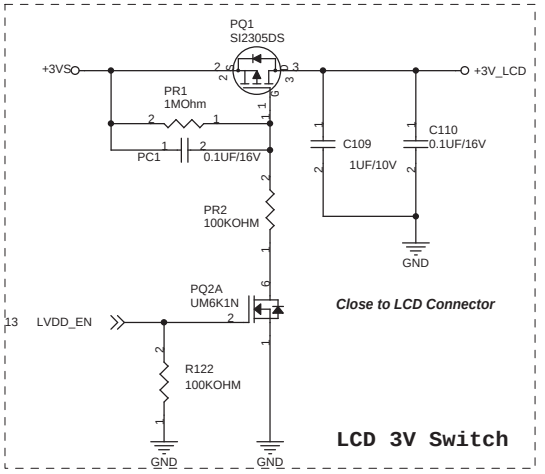


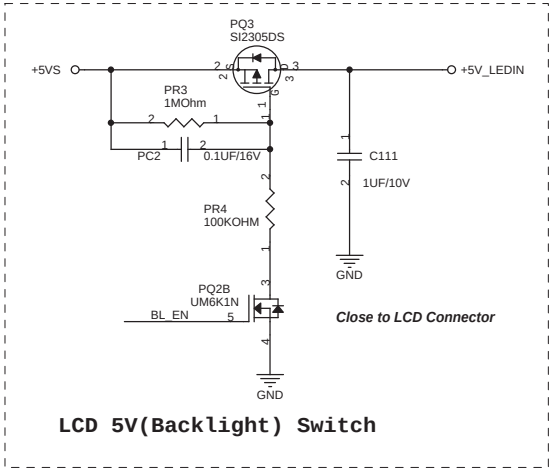
0106 1025

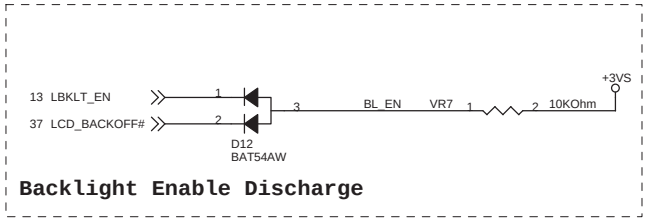
ASUSTek Computer INC.	Title : Onboard VGA	
	Engineer: *Leon Sun*	
Size: A3	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 21 of 57	











0106 1025

ASUSTek Computer INC.	Title : LVDS Conn	
	Engineer: *Jerry Liu*	
Size: A3	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 22 of 57	

H1 CT177B67D47 GND
H2 CT177B67D47 GND

MINI CARD NUT(2.8mm) *2

2008/03/11 change to high rated current bead

+3VS
GC9 100UF/6.3V
3GLAN_OFF
GR4 1KOhm
GC8 0.1UF/16V
GQ2 SI7121DN-T1-GE3
GR3 Do Not Stuff /X r0603_h24
GL1 70Ohm/100Mhz
GC1 33PF/50V
GC2 22PF/50V
GC3 100UF/6.3V
+3VS_3G
R1.1G

+3VS_3G
GR7 Do Not Stuff /X
3GLAN_OFF#
GQ1 2N7002
3GLAN_OFF 14

CAP Near SIM Socket

USIM_PWR
GC4 33PF/50V /3G
USIM_RESET
GC5 33PF/50V /3G
USIM_CLK
GC6 33PF/50V /3G
USIM_DATA
GC7 33PF/50V /3G
GR2 Do Not Stuff /3G/X
USIM1
NP_NC1 PWR GND RST VPP CLK DATA NP_NC2
SIM_6P 12G253000681 /3G

SIM_CON_8P

+3VS_3G
T217 T218
3G_GPS_CARD1
WAKE# Reserved1 Reserved2 CLKREQ# GND1 REFCLK- REFCLK+ GND2
3.3V_1 GND7 1.5V_1 UIM_PWR UIM_DATA UIM_CLK UIM_RESET UIM_VPP
USIM_PWR USIM_DATA USIM_CLK USIM_RESET
Reserved/UIM_C8 Reserved/UIM_C4 GND3 PERn0 PERp0 GND4 GND5 PETn0 PETp0 GND6 Reserved3 Reserved4 Reserved5 Reserved6 Reserved7 Reserved8 Reserved9 Reserved10
GND8 W_DISABLE# PERST# +3.3Vaux GND9 1.5V_2 SMB_CLK SMB_DATA GND10 USB_D- USB_D+ GND11 LED_WWAN# LED_WLAN# LED_WPAN# 1.5V_3 GND12 3.3V_2
USBPN3 USBPP3 LED_3GLAN# Do Not Stuff
GND13 GND14 NP_NC2 NP_NC1
MINI_PCI_LATCH_52P 12G03010052X
3GLAN_OFF# GR5 0Ohm
GR6 0Ohm GR1 0Ohm 3GLAN_OFF#
BUF_RST# 20,24,26,27,28,30,31,37,38,40
38 EXT_RX 38 EXT_CTS# 38 EXT_TX 38 EXT_RTS#
+3VS GL2 120Ohm/100Mhz GC10 0.1UF/16V

GPS/DTV Antenna

RF1
P2 P3
RF_CON_2P 12G3100840000 /TV

WRN5B 0OHM
14 USB_PN3
USBPN3
WL1
14 USB_PP3
Do Not Stuff /X
USBPP3
WRN5A 0OHM

0106 1025

3.5G Module & External Antenna

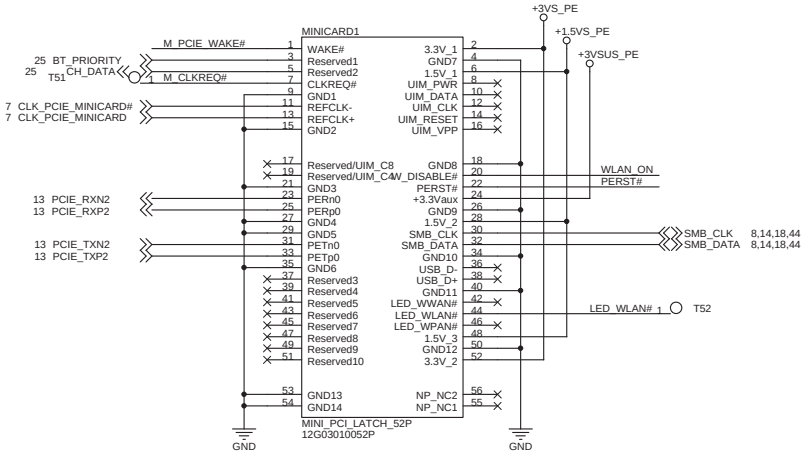
ASUSTek Computer INC.

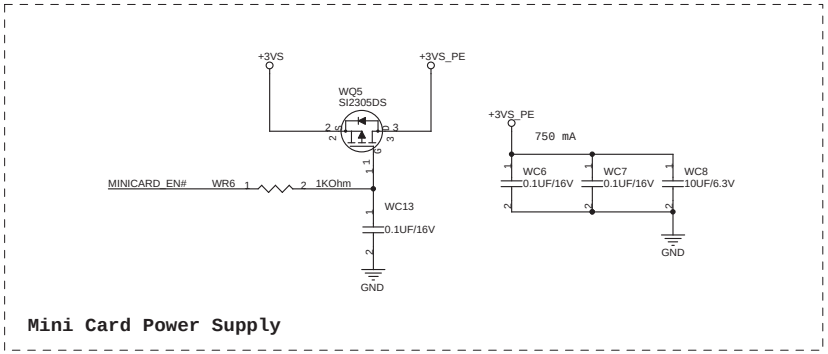
Title :

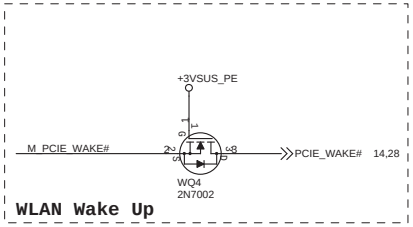
Engineer: *Leon Sun*

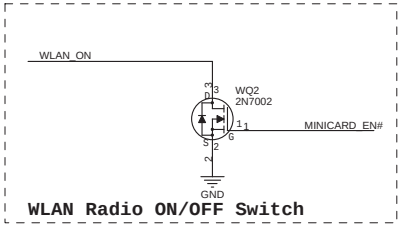
Size	Project Name	Rev
A3	**T91**	1.2G

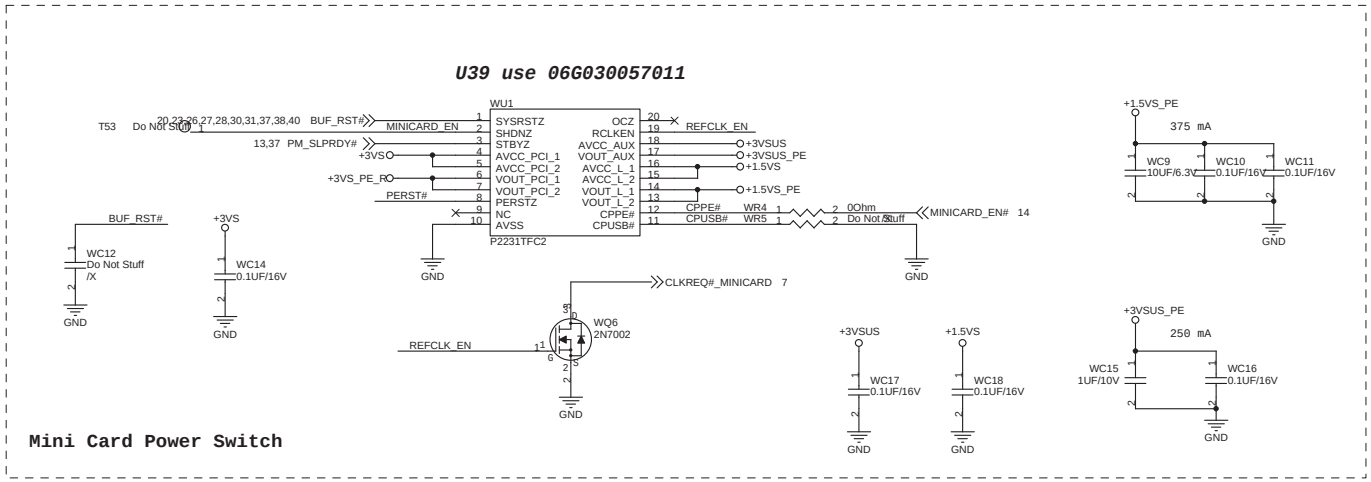
Date: Tuesday, January 06, 2009 Sheet 23 of 57

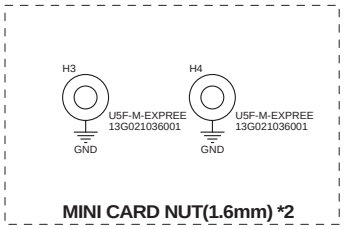






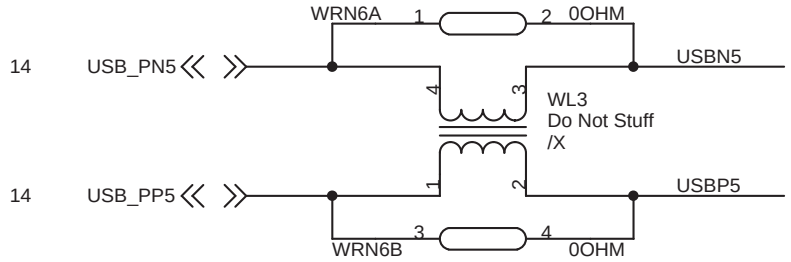




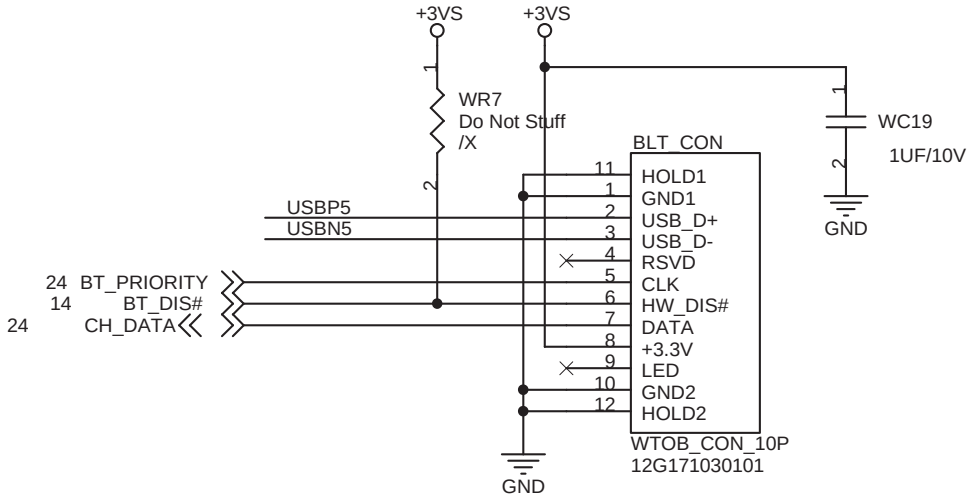


0106 1025

ASUS	Title : Mini WIFI	
ASUSTek Computer INC.	Engineer: Jerry Liu	
Size: Custom	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 24 of 57	



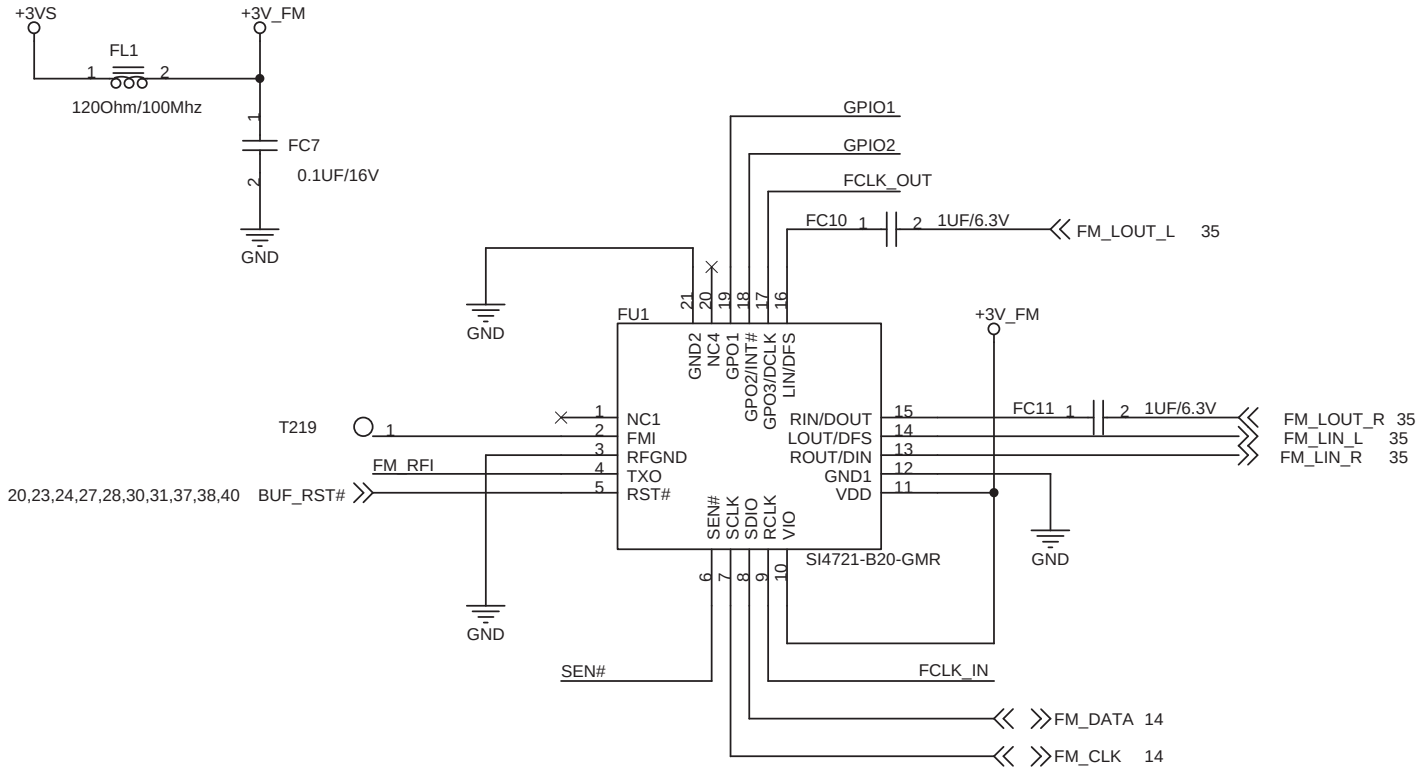
BT USB Port Common Choke

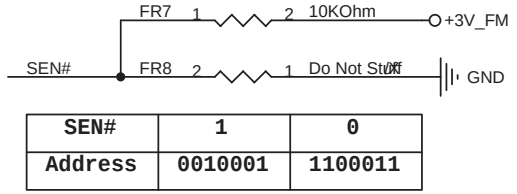


BT Conn

0106 1025

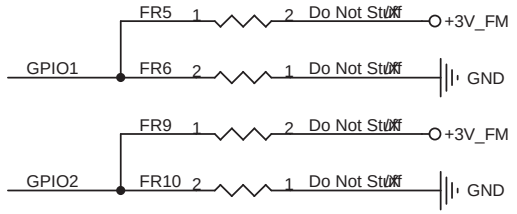
ASUSTek Computer INC.	Title : Bluetooth	
	Engineer: *Jerry Liu*	
Size: A	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 25 of 57	





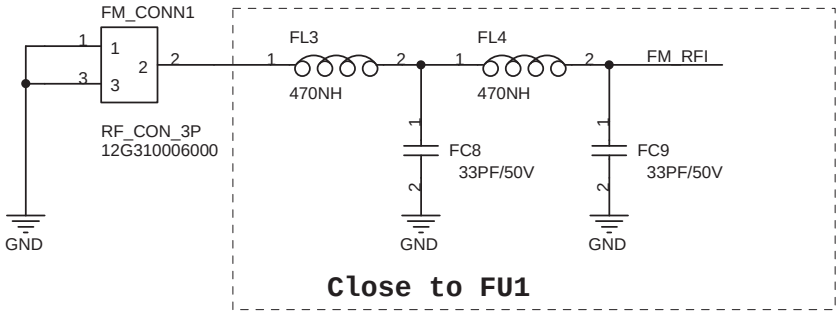
SEN#	1	0
Address	0010001	1100011

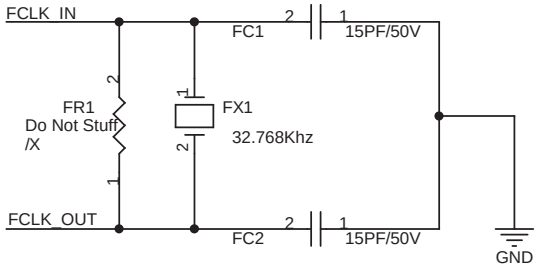
seven-bit device address Selection



BUS Mode	GPIO1	GPIO2/INT
2-Wire	1	0
SPI	1	1(Must Drive)
3-Wire	0(Must Drive)	0

Bus Mode Selection





0106 1025

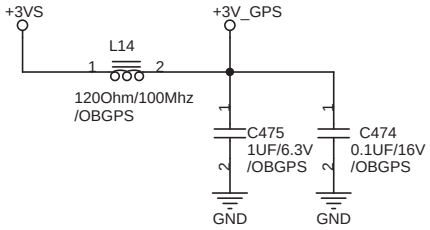
ASUSTek Computer INC.

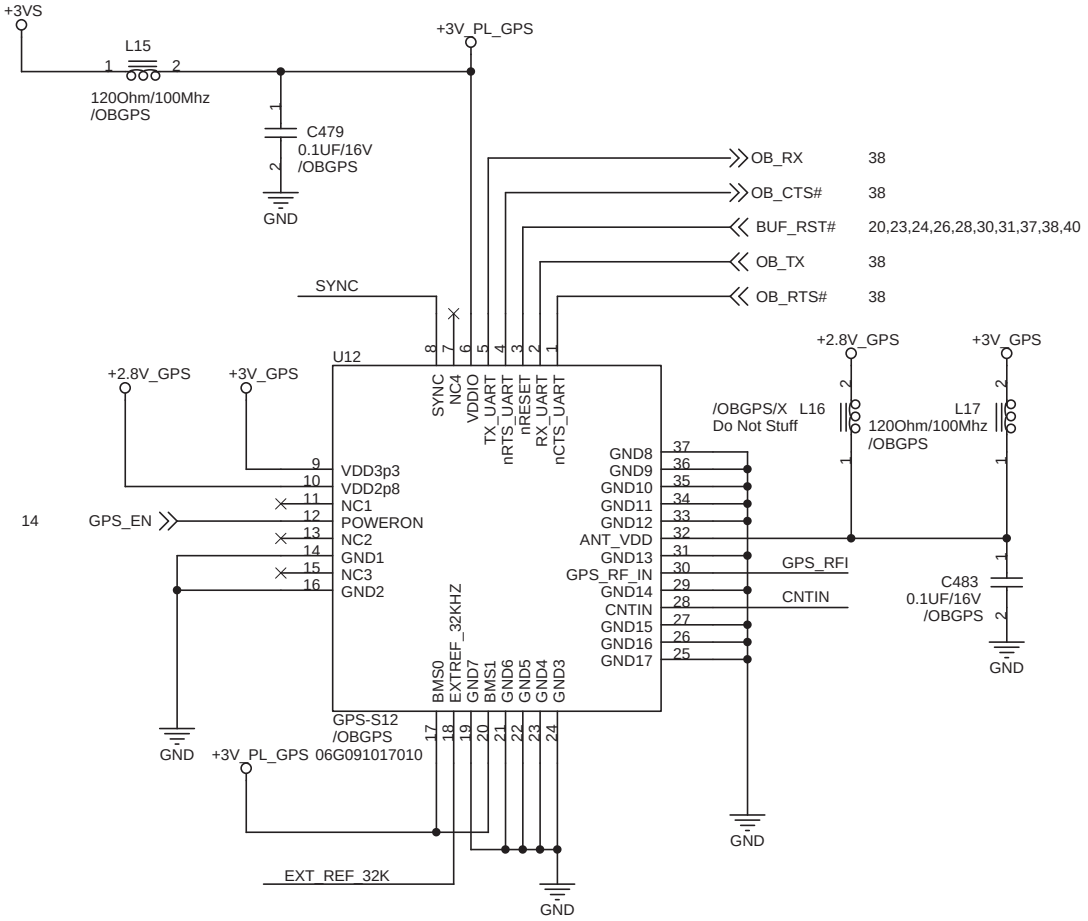
Title : FM RADIO

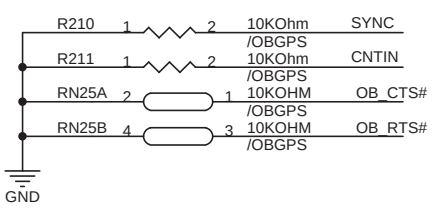
Engineer: *Jerry Liu*

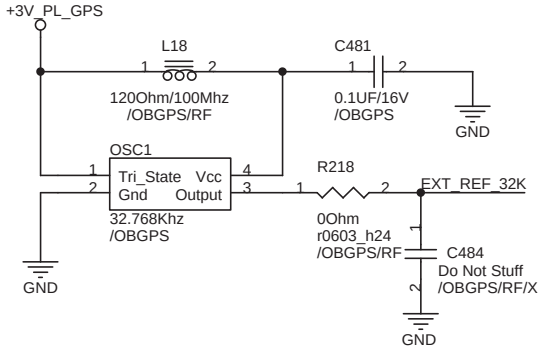
Size	Project Name	Rev
A4	**T91**	1.2G

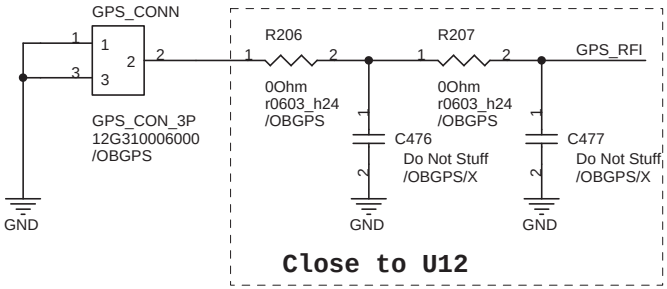
Date: Tuesday, January 06, 2009 Sheet 26 of 57

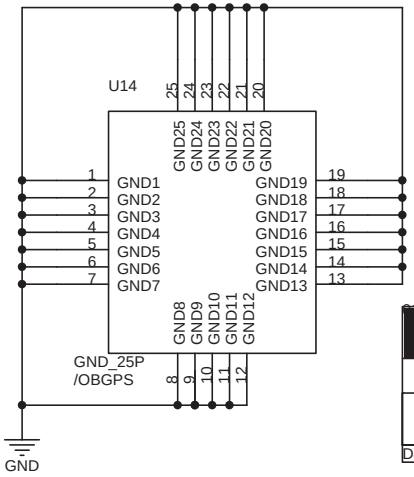




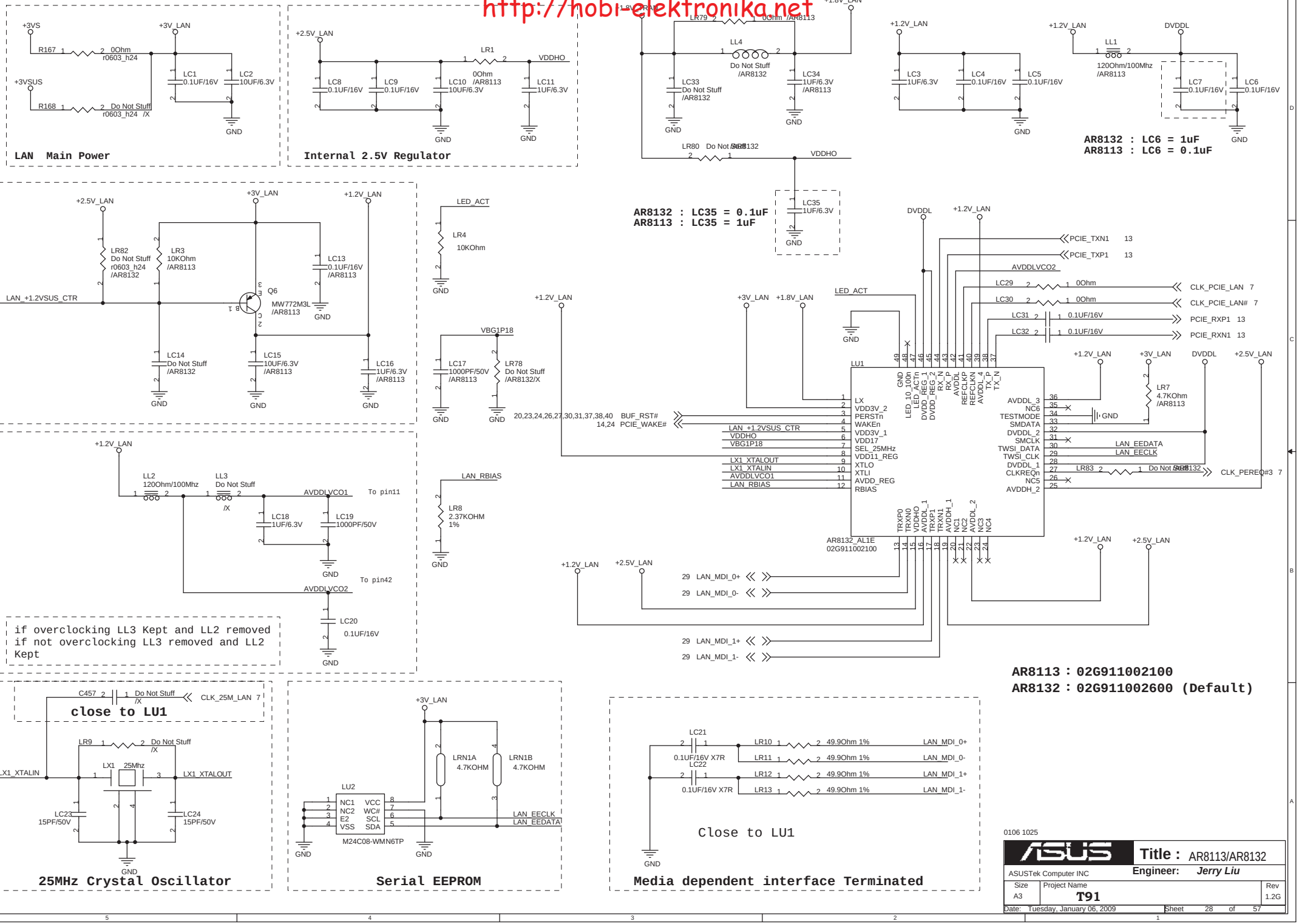


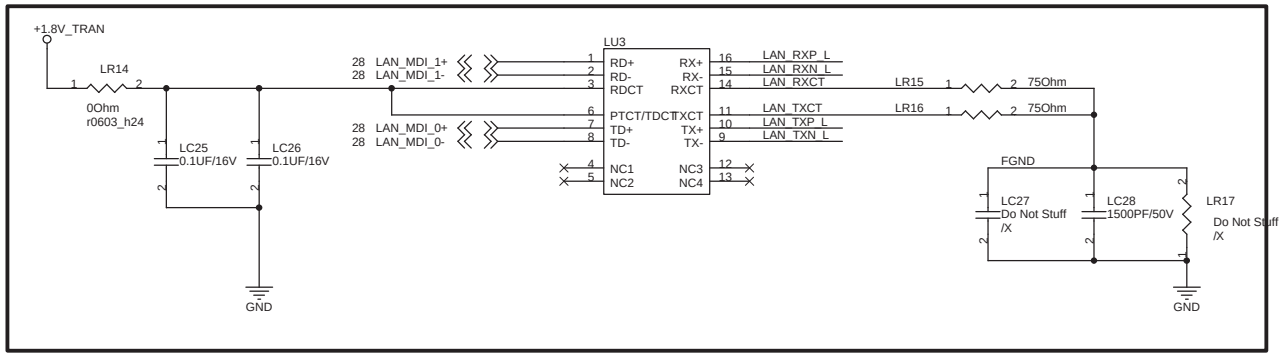


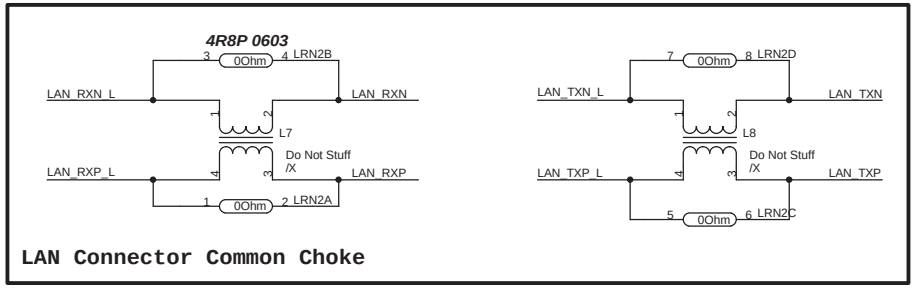


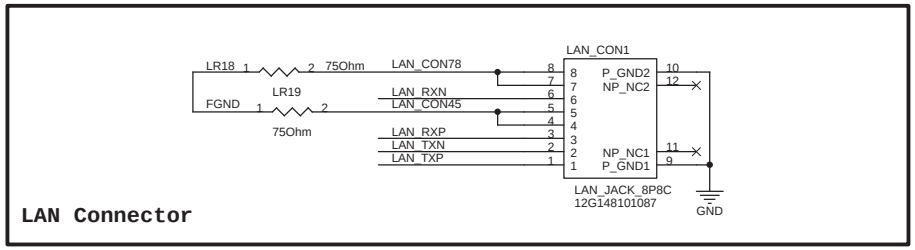


ASUS	Title : Onboard GPS		
ASUSTek Computer INC.	Engineer: Jerry Liu		
Size: Custom	Project Name: T91		Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 27 of 57		



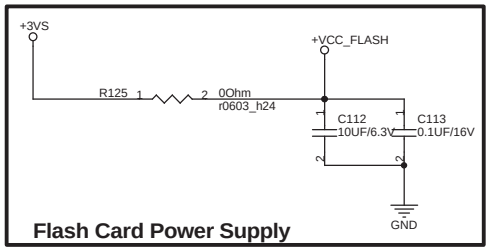




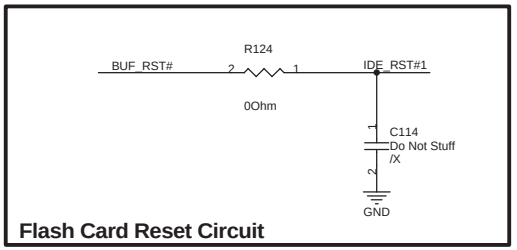


0106 1025

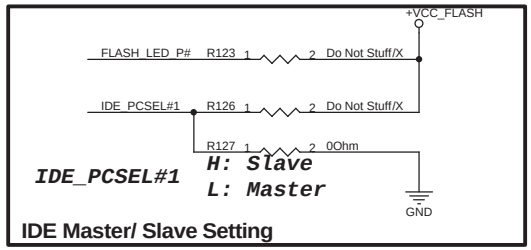
ASUSTek Computer INC.	Title : RJ45	
	Engineer: *Jerry Liu*	
Size: A3	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 29 of 57	



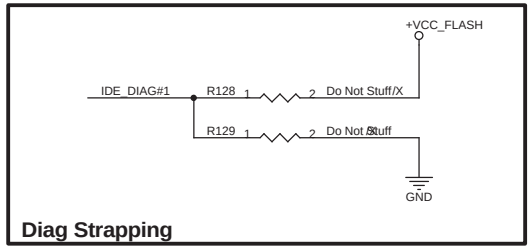
Flash Card Power Supply



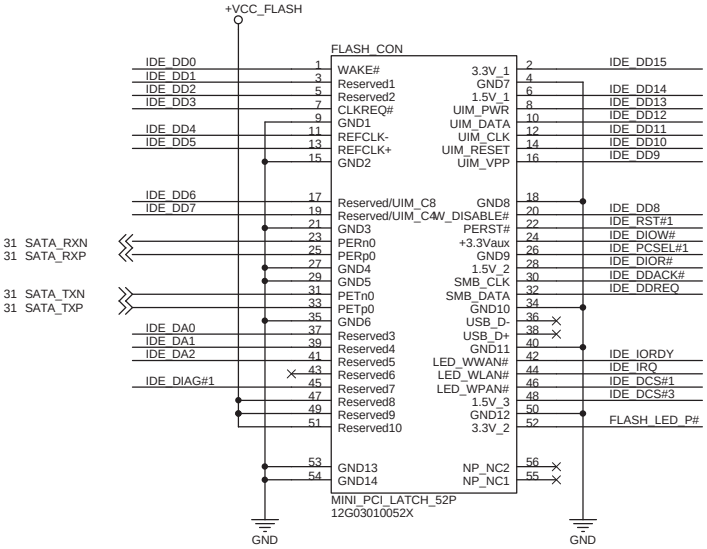
Flash Card Reset Circuit



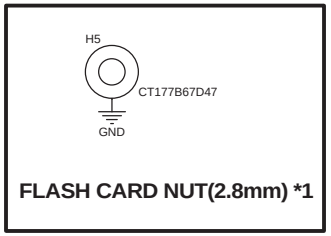
IDE Master/ Slave Setting



Diag Strapping



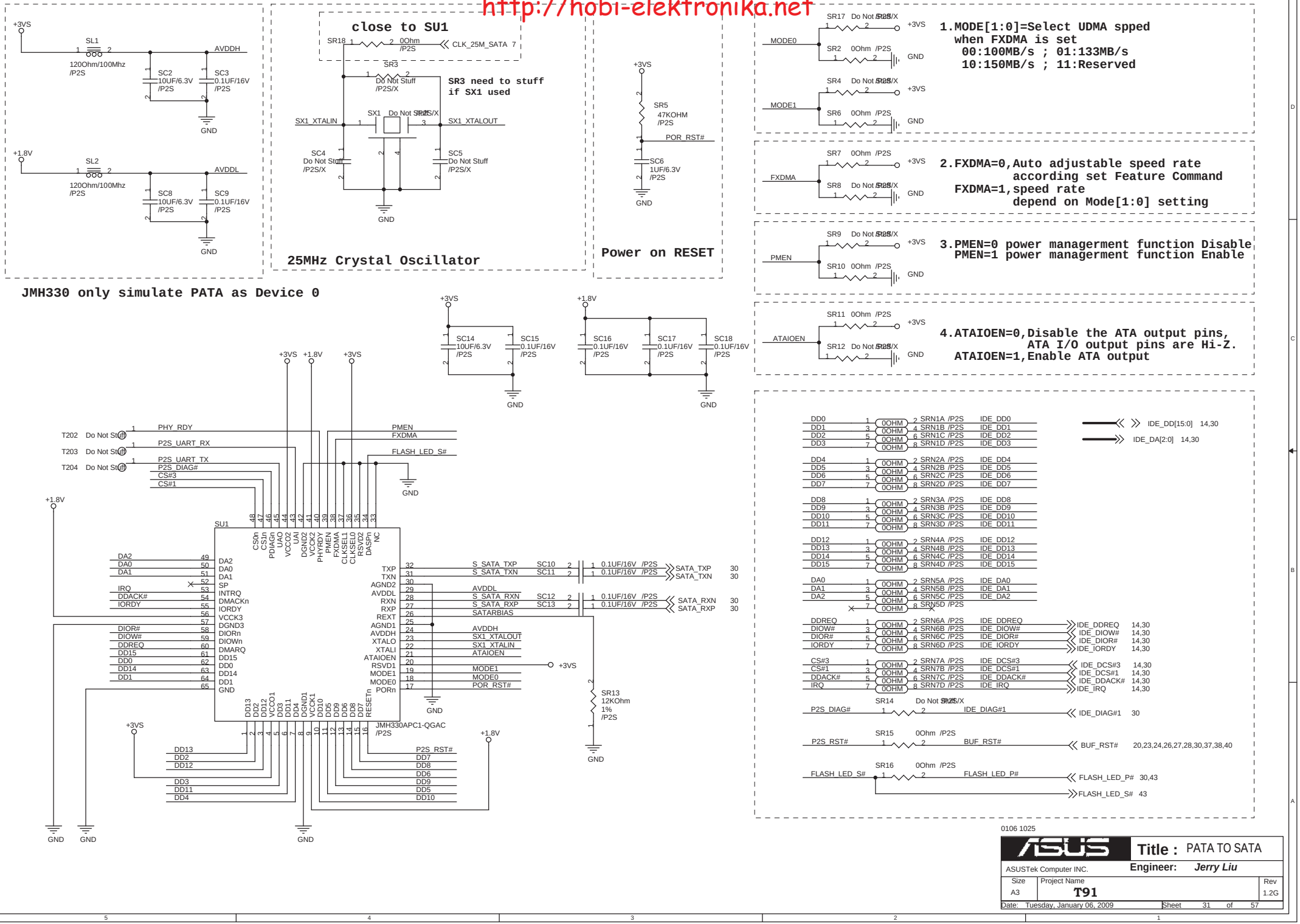
IDE_DD[15:0] 14,31
IDE_DA[2:0] 14,31
IDE_DDACK# 14,31
IDE_DDREQ 14,31
IDE_DIOR# 14,31
IDE_DIOW# 14,31
IDE_IORDY 14,31
IDE_DCS#1 14,31
IDE_DCS#3 14,31
IDE_IRQ 14,31
BUF_RST# 20,23,24,26,27,28,31,37,38,40
FLASH_LED_P# 31,43
IDE_DIAG#1 31



FLASH CARD NUT(2.8mm) *1

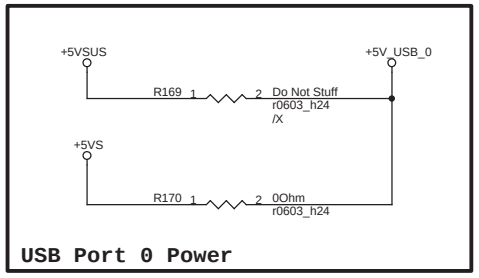
0106 1025

ASUSTek Computer INC.	Title : Flash Conn	
	Engineer: *Jerry Liu*	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 30 of 57	

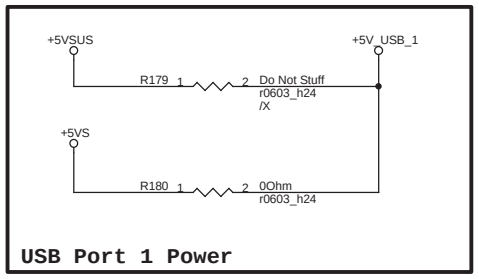


0106 1025

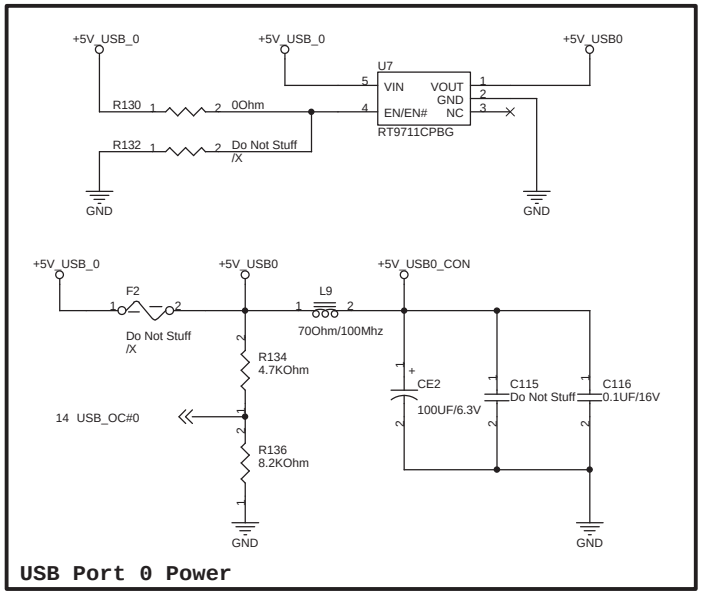
ASUSTek Computer INC.	Title : PATA TO SATA	
	Engineer: *Jerry Liu*	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 31 of 57	



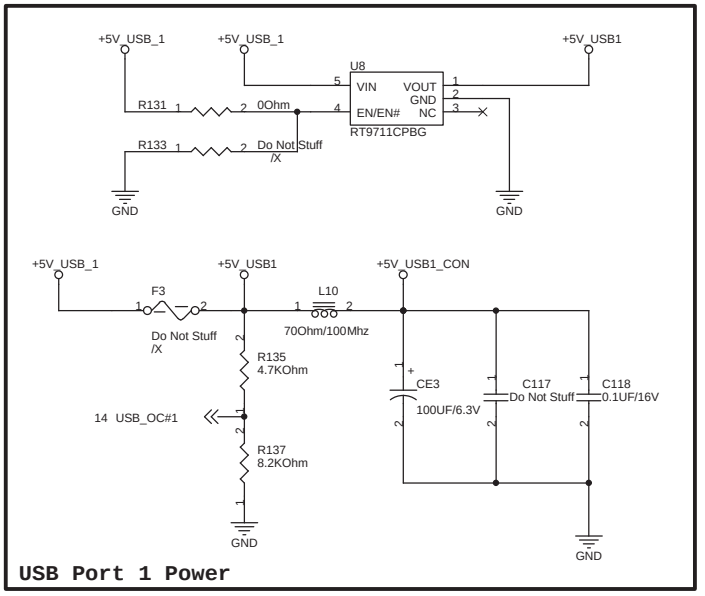
USB Port 0 Power



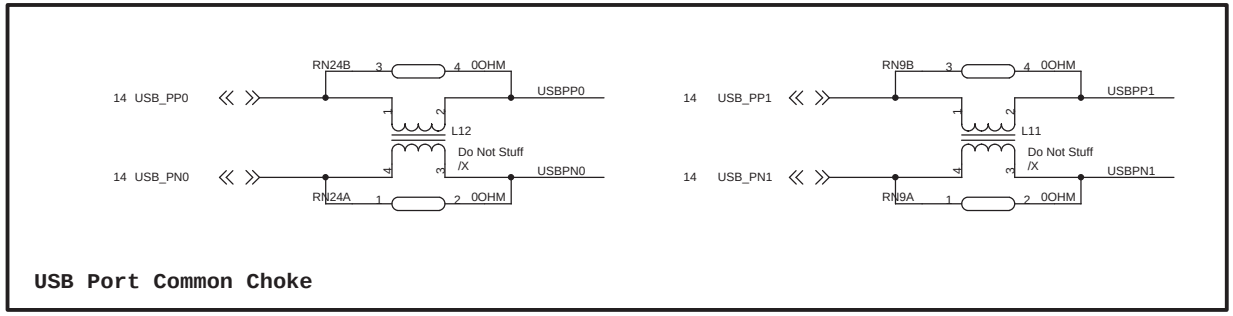
USB Port 1 Power



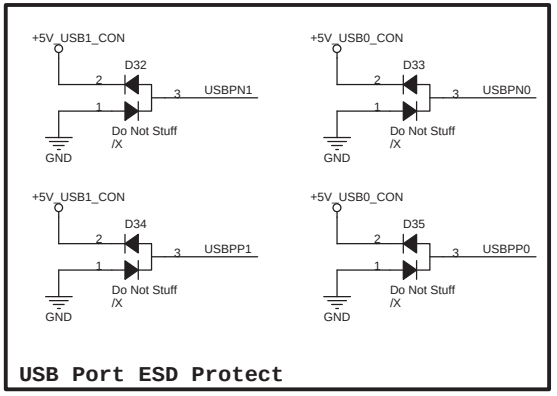
USB Port 0 Power



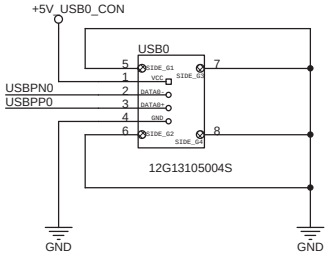
USB Port 1 Power



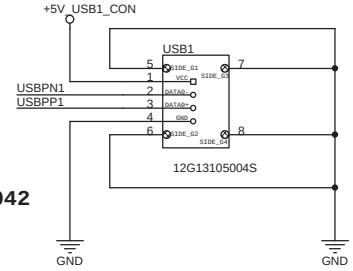
USB Port Common Choke



USB Port ESD Protect



Symbol use 12G131030042
BOM use 12G13105004S

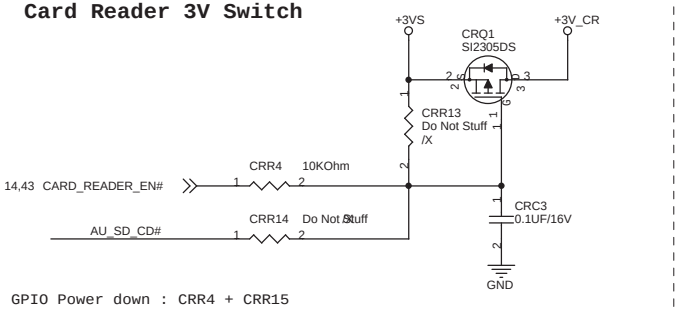


USB Connector

0106 1025

ASUSTek Computer INC.	Title : USB Port	
	Engineer: *Jerry Liu*	
Size: A3	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 32 of 57	

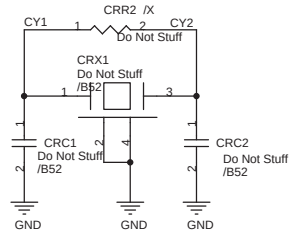
Card Reader 3V Switch



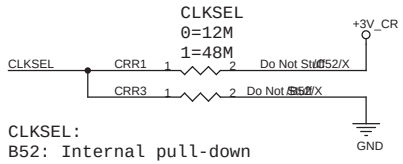
GPIO Power down : CRR4 + CRR15
(remove CRR13 + CRR14 + CRR16)

SD card Power down : CRR13 + CRR14 + CRR16
(remove CRR4 + CRR15)

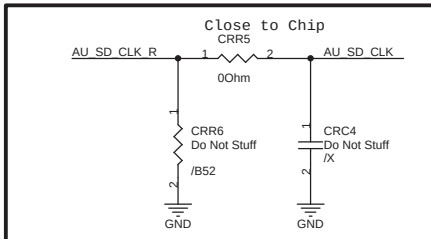
12MHz Crystal Oscillator

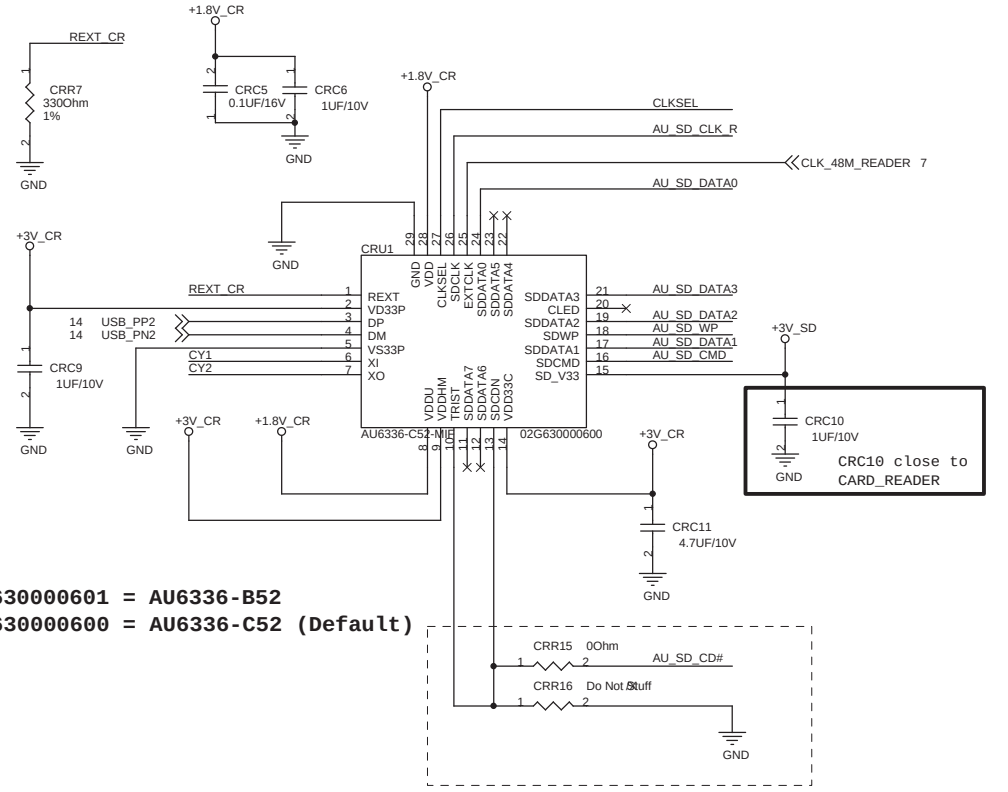


Clock Setting



CLKSEL:
B52: Internal pull-down
C52: Internal pull-up



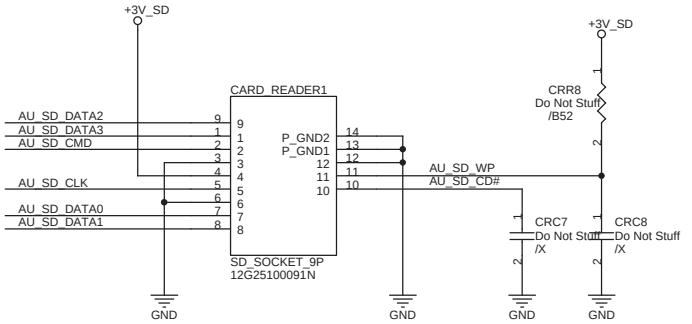


02G630000601 = AU6336-B52
02G630000600 = AU6336-C52 (Default)

SDWP: Internal Pull-up

SDCDN: Internal Pull-up

SDWP = 1 Write protect
SDWP = 0 Write-able
SDCDN = 1 No card
SDCDN = 0 Card inserted

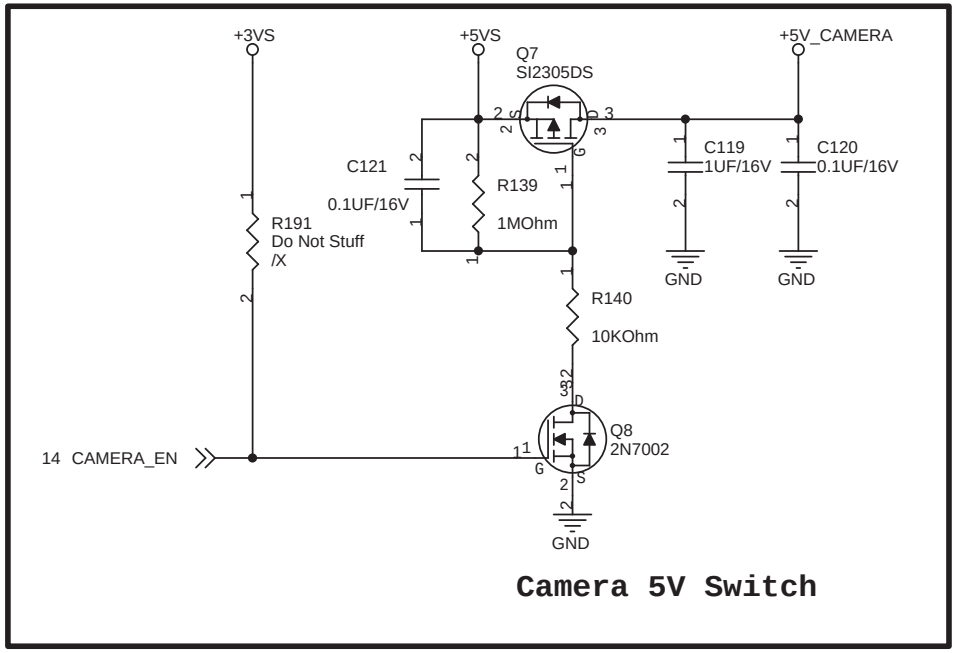


Card Insert: Pin.10 and Pin.12 are Shorted.
Card not Insert: Pin.10 and Pin.12 are Opened.
Write Protect: Pin.11 and Pin.12 are Opened.
Write Enable: Pin.11 and Pin.12 are Shorted.

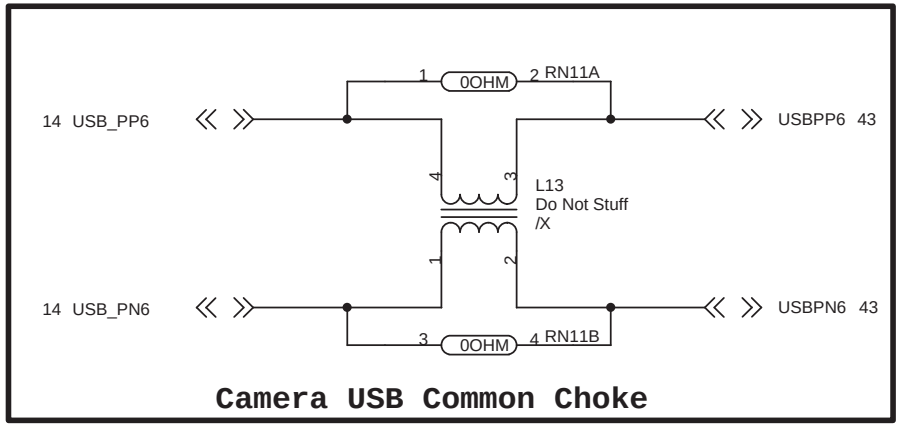
Card Reader Connector

0106 1025

ASUSTek Computer Inc.	Title : AU6336-C52	
	Engineer: Jerry Liu	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 33 of 57	



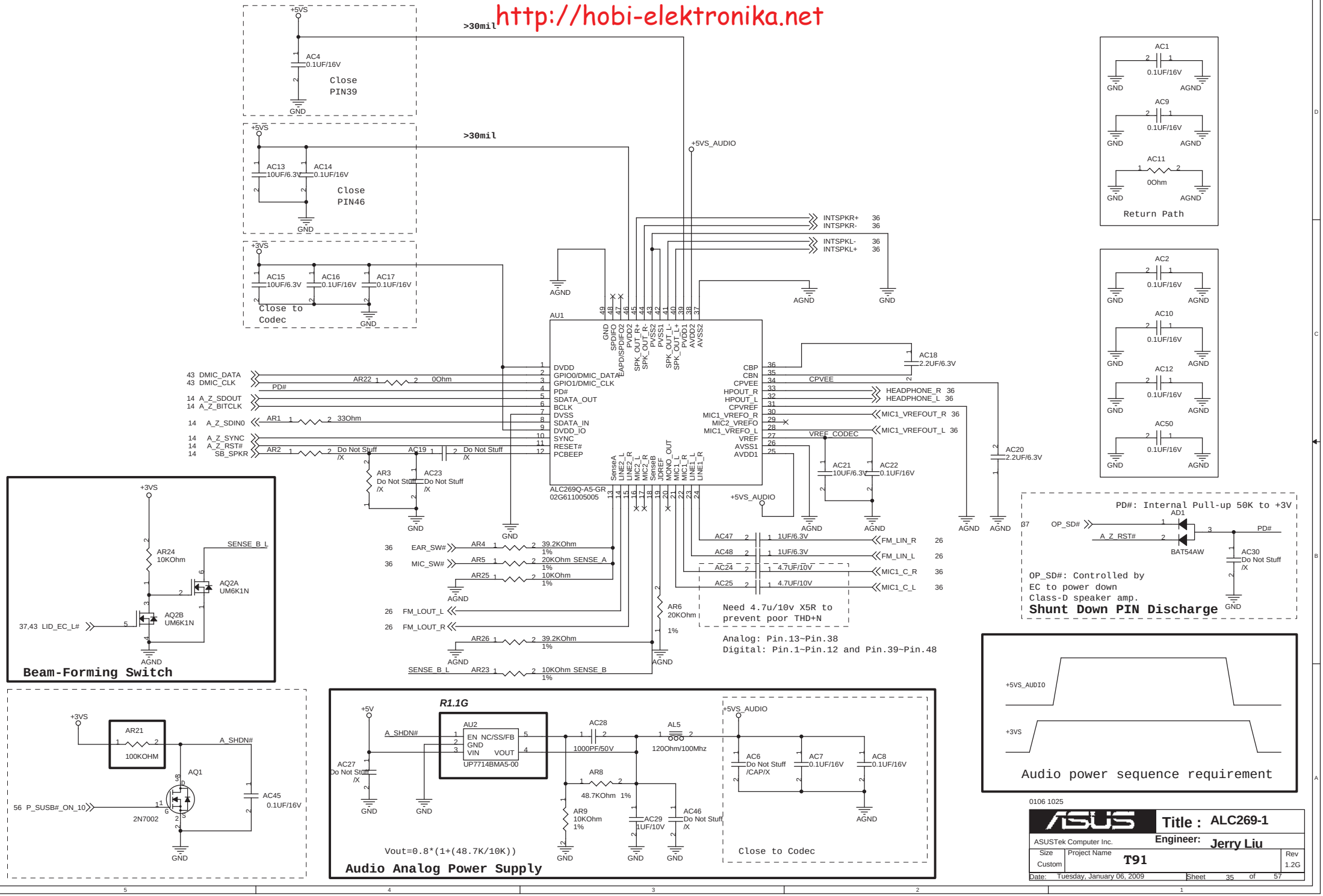
Camera 5V Switch

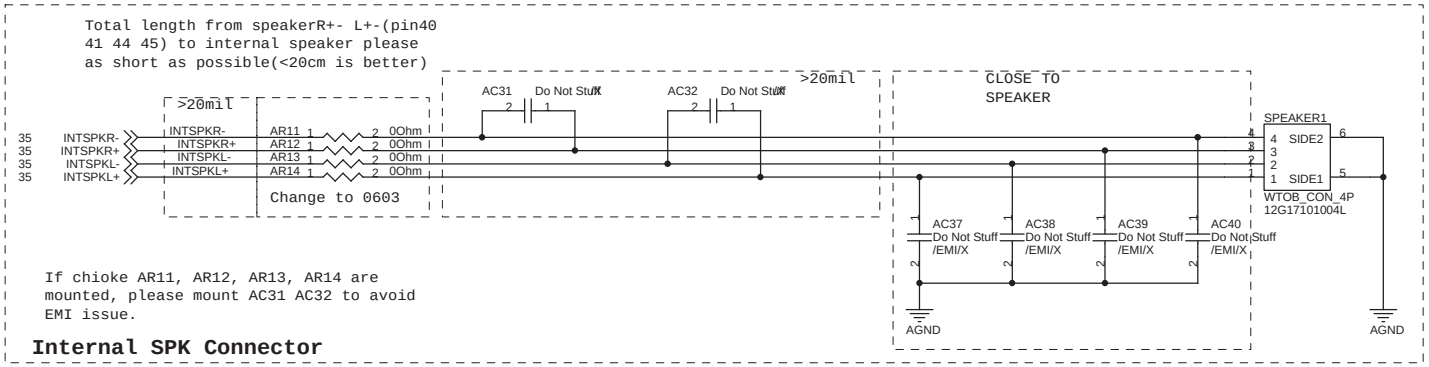


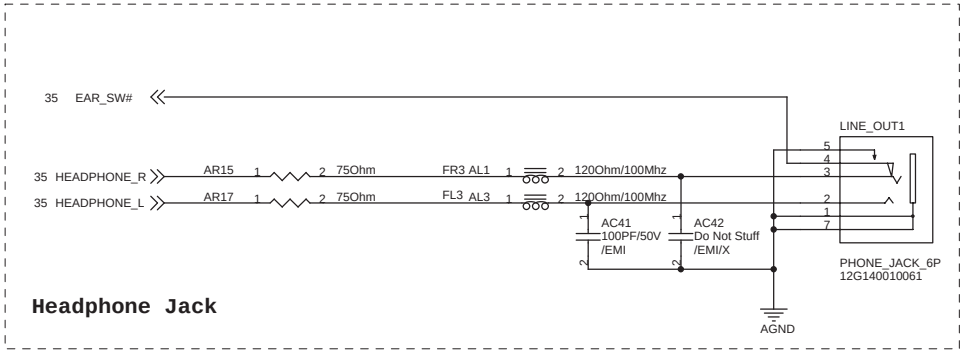
Camera USB Common Choke

0106 1025

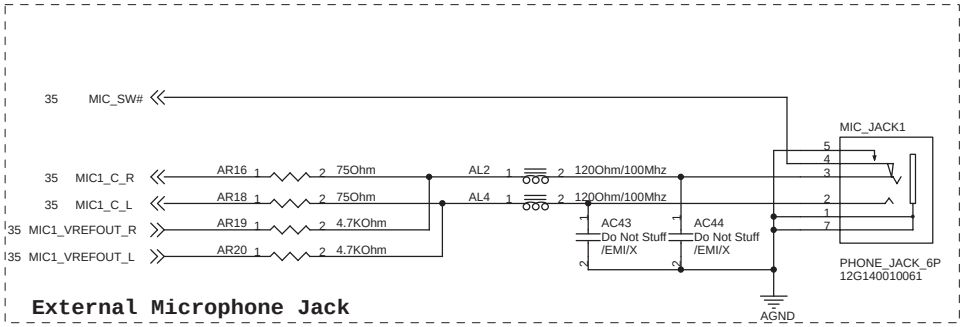
ASUSTek Computer INC.	Title : Camera Conn	
	Engineer: *Jerry Liu*	
Size: A4	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 34 of 57	





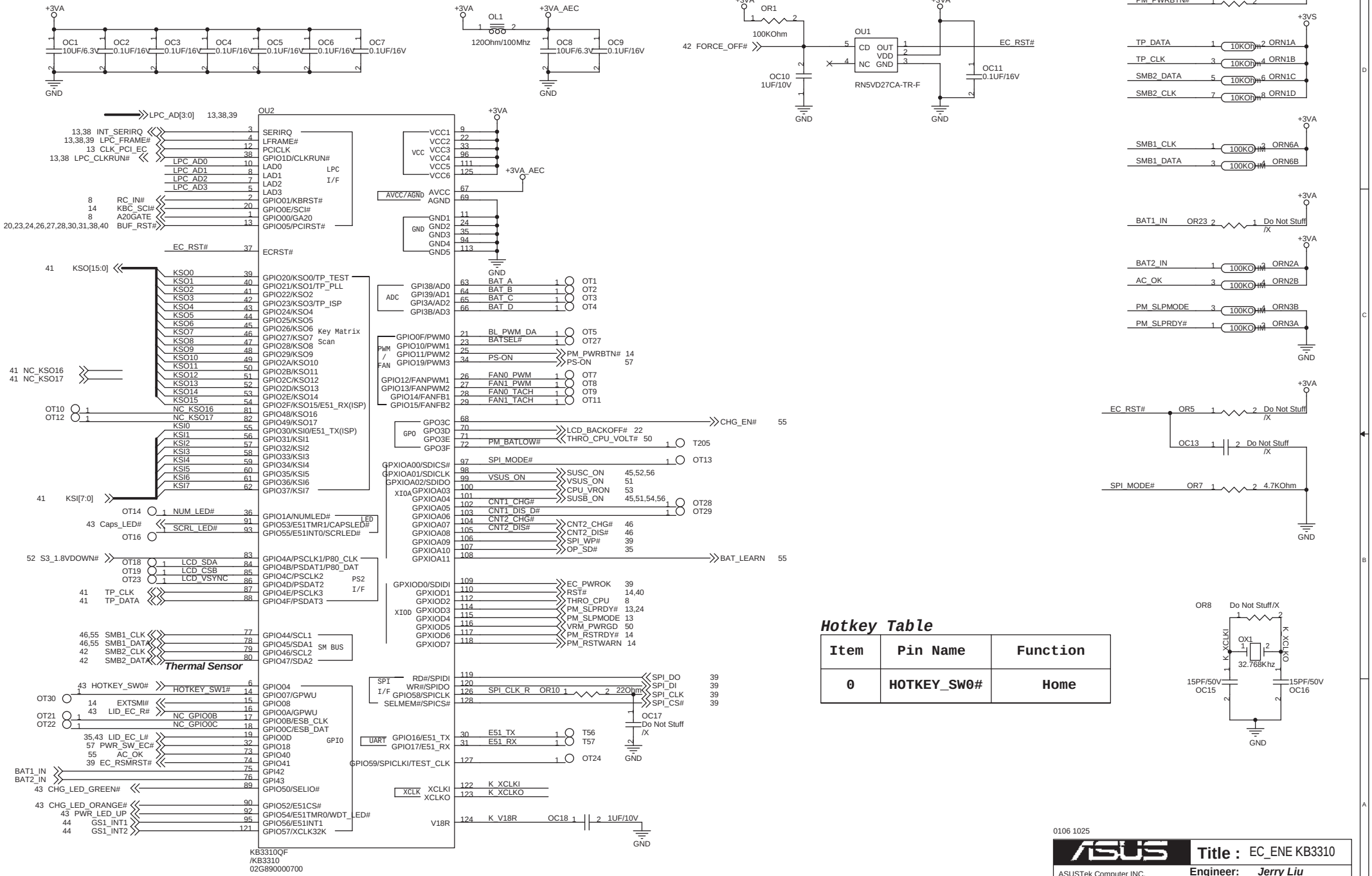


Symbol use 12G140010060
BOM use 12G140010061



0106 1025

ASUSTek Computer Inc.	Title : ALC269-2	
	Engineer: Jerry Liu	
Size A3	Project Name T91	Rev 1.2G
Date: Tuesday, January 06, 2009	Sheet 36 of 57	



Hotkey Table

Item	Pin Name	Function
0	HOTKEY_SW0#	Home

HOTKEY_SW0# - HOTKEY_SW3# internal PU

0106 1025

ASUSTek Computer INC.

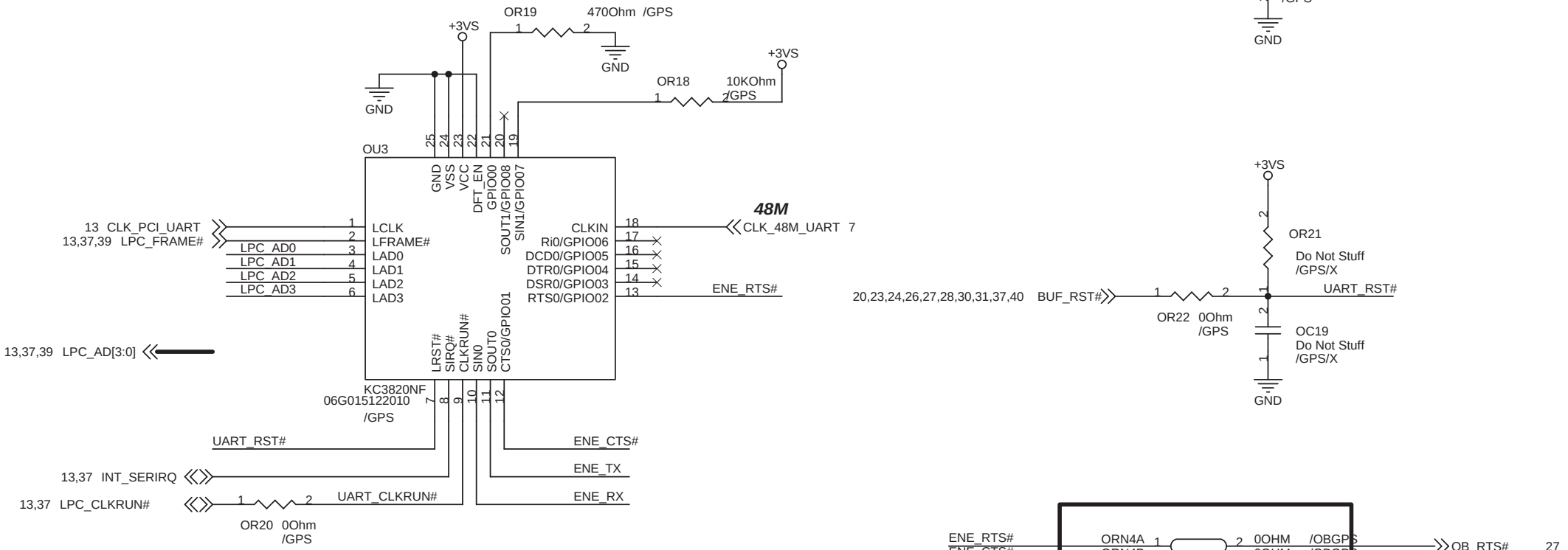
Title : EC_ENE KB3310

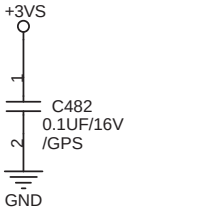
Engineer: Jerry Liu

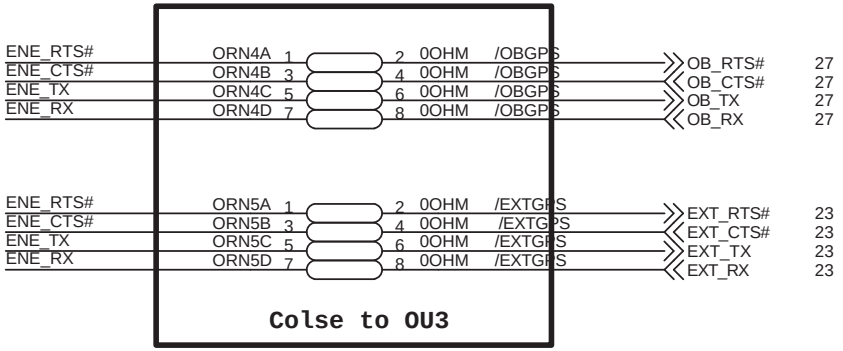
Size	Project Name	Rev
A3	T91	1.2G

Date: Tuesday, January 06, 2009 Sheet 37 of 57

GPIO00
Hardware strap(internal pull-high)
Low:4E 4F
High:2E 2F







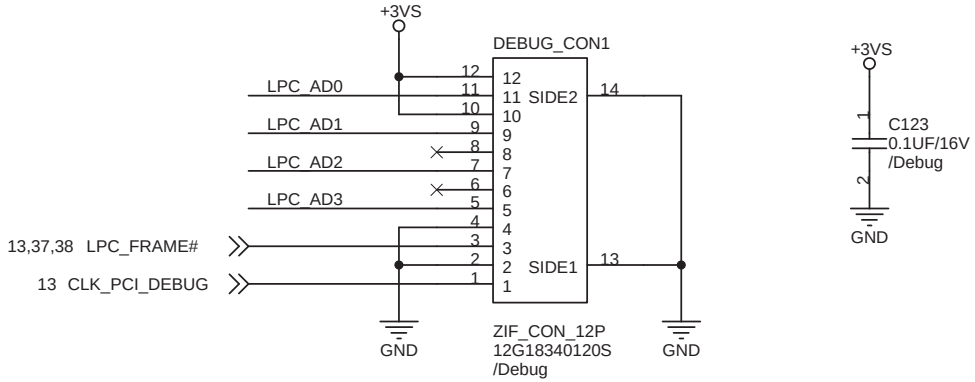
UART Control IC for using GPS module due to no UART on ENE EC

0106 1025

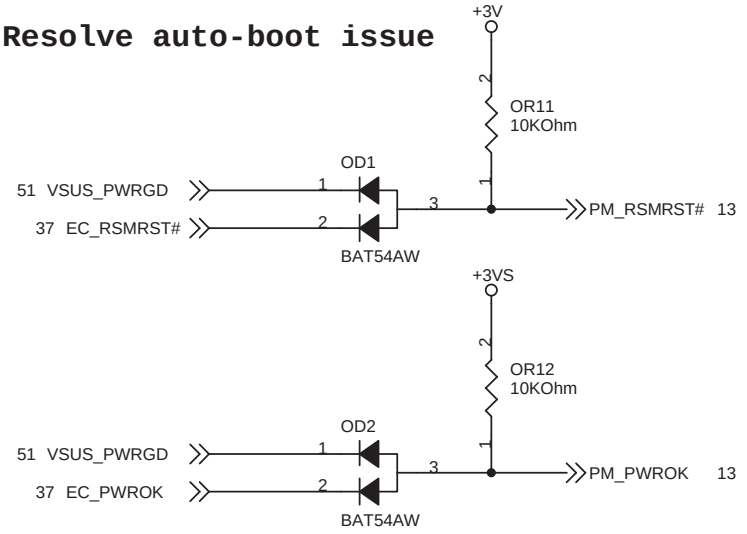
ASUSTek Computer INC.	Title : EC_UART_KC3820	
	Engineer: *Jerry_Liu*	
Size: A4	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 38 of 57	

For Debug

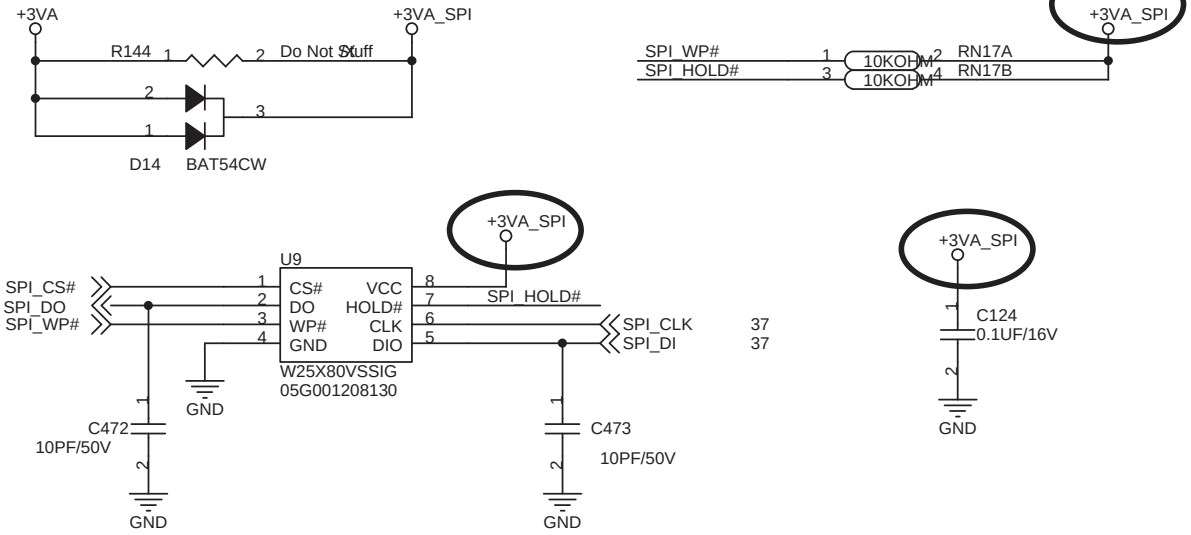
LPC_AD[3:0] 13,37,38



Resolve auto-boot issue

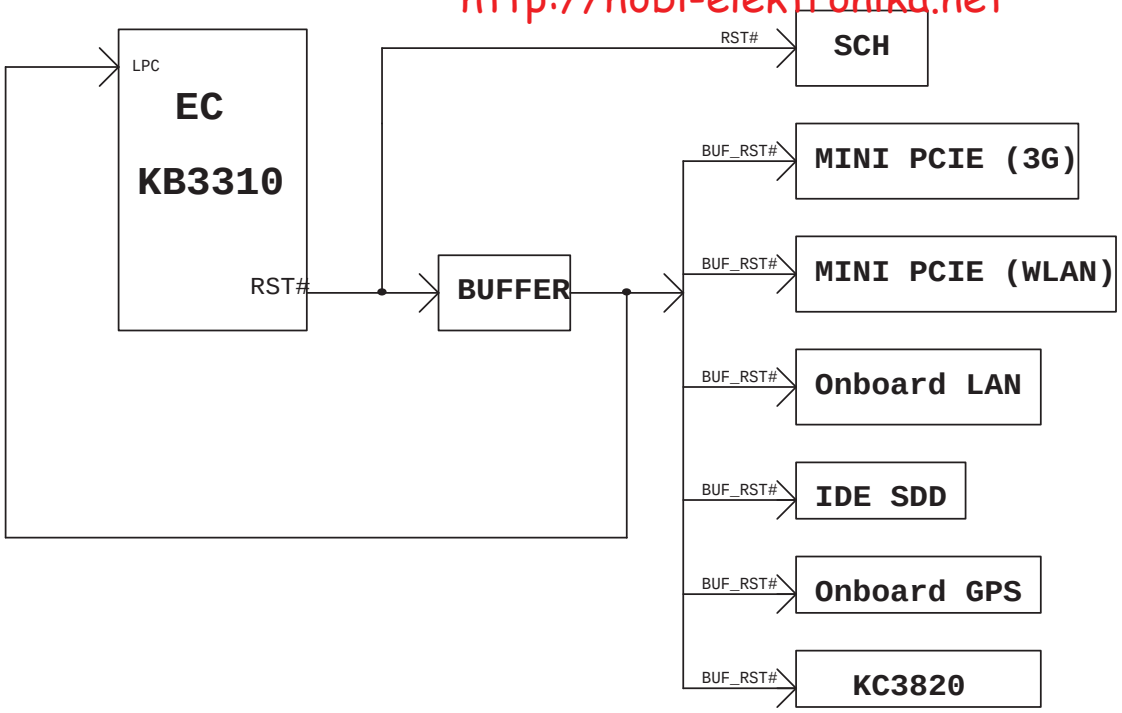


SPI ROM

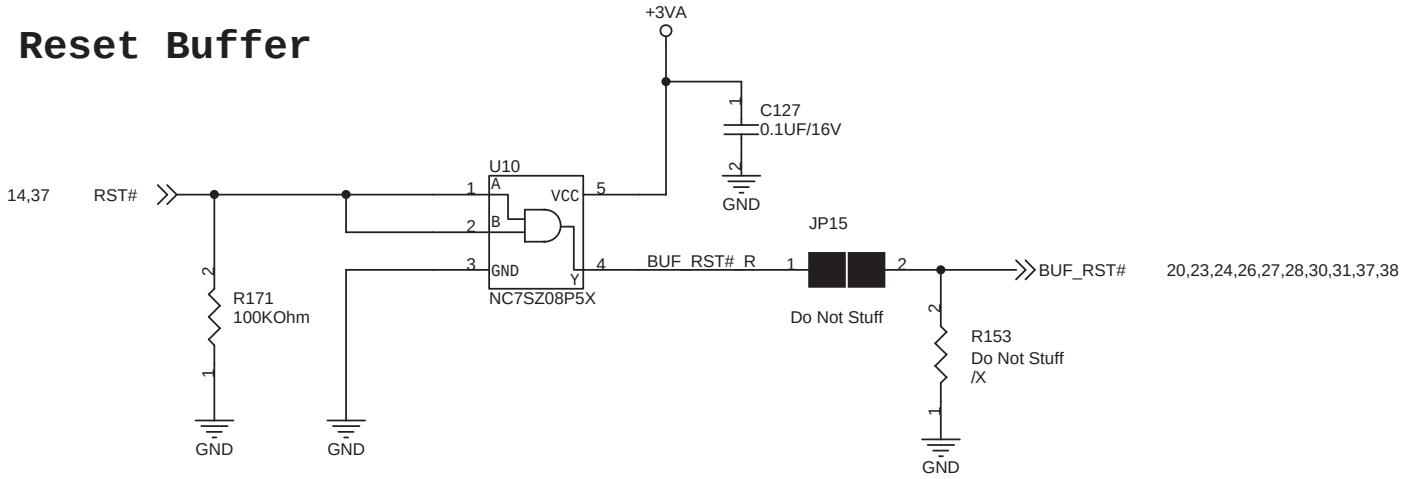


0106 1025

ASUSTek Computer INC.	Title : SPI ROM/ Debug	
	Engineer: *Jerry Liu*	
Size: A4	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 39 of 57	

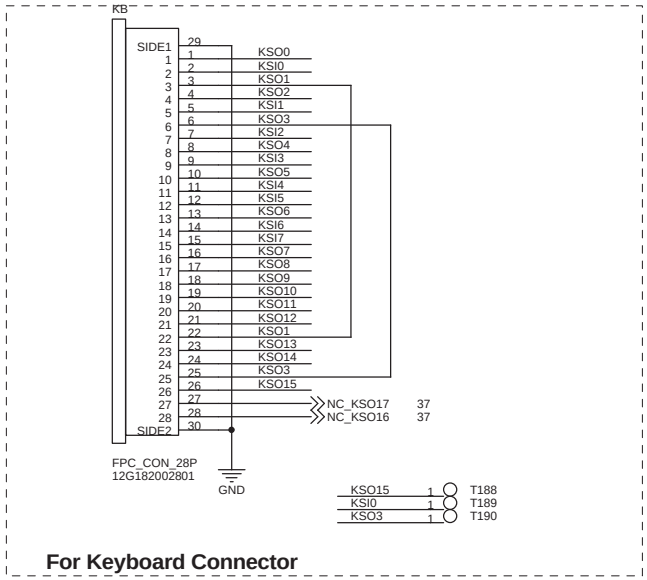


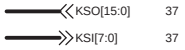
Reset Buffer

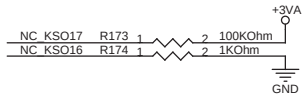


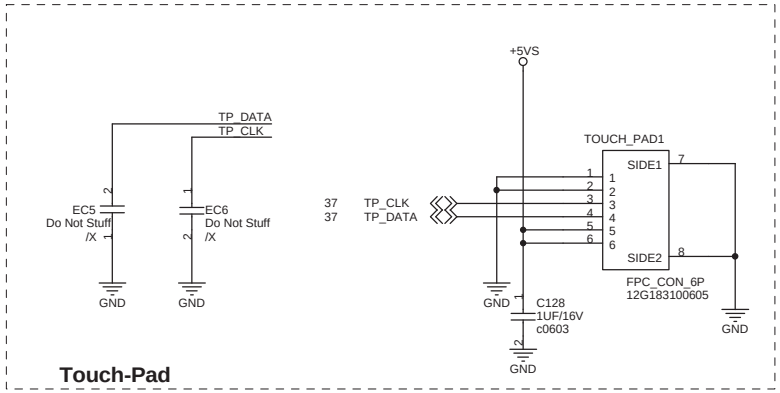
0106 1025

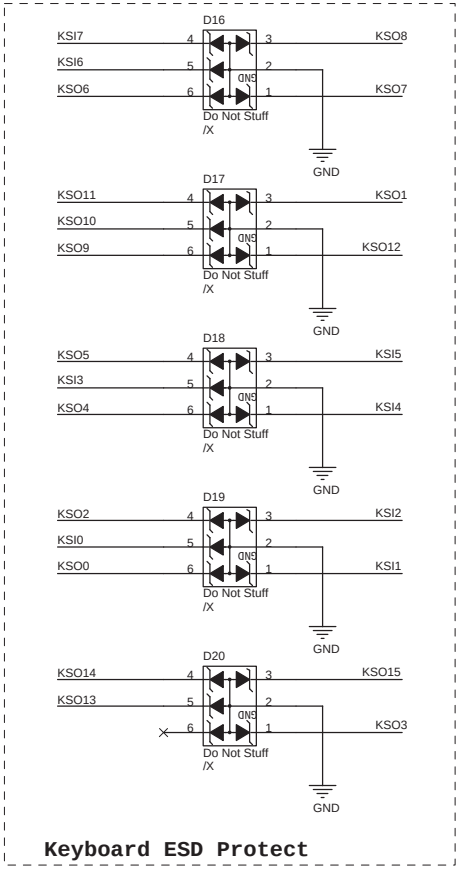
ASUSTeK COMPUTER INC	Title : Reset Map	
	Engineer: Jerry Liu	
Size: A4	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 40 of 57	





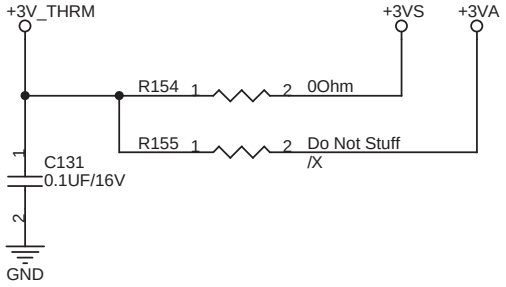






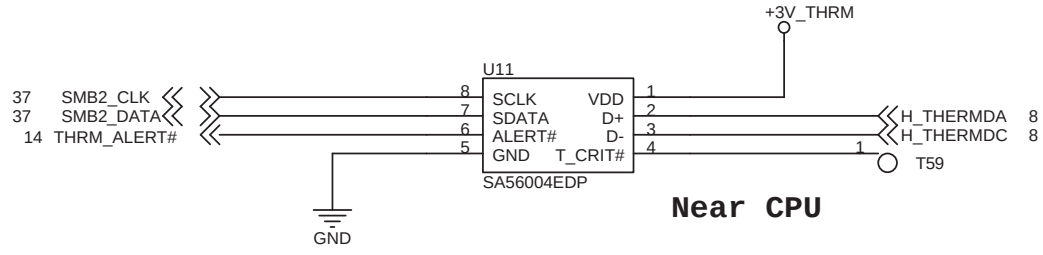
0106 1025

ASUSTek Computer INC.	Title : KB_Touch Pad	
	Engineer: *Jerry Liu*	
Size: A3	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 41 of 57	

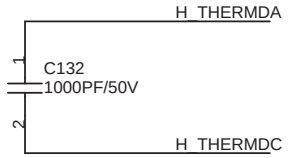


Thermal Sensor Power Supply

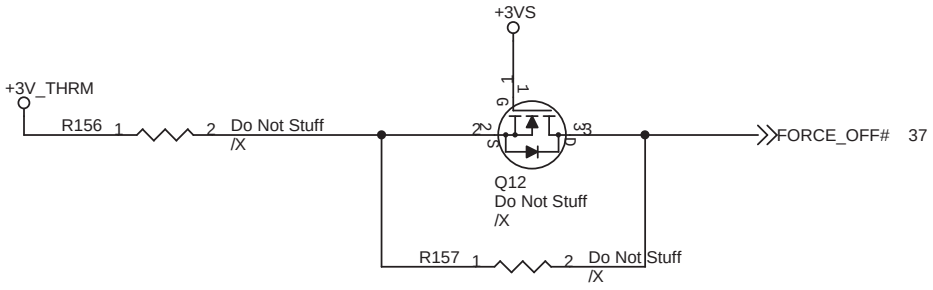
Thermal Sensor



Near CPU

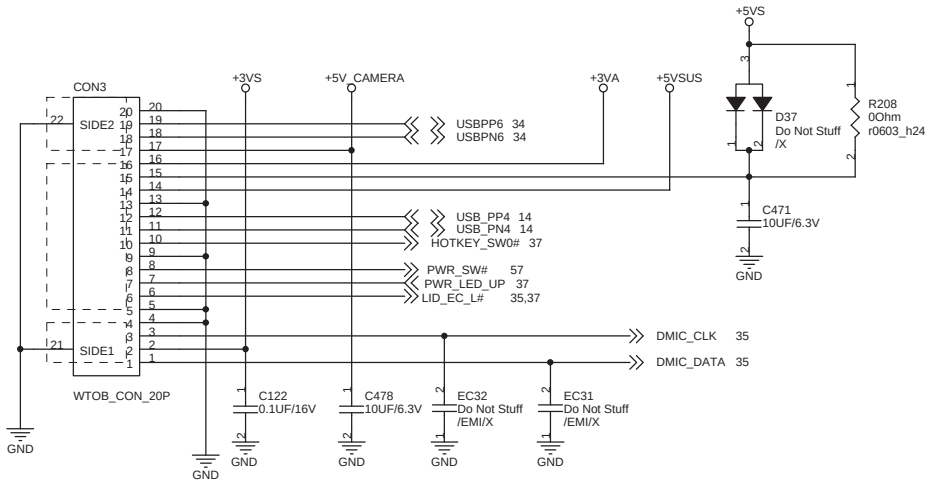


U11 use 06G023044020,
second source 06G023055010

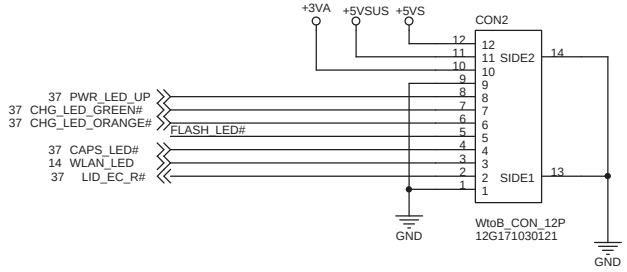


0106 1025

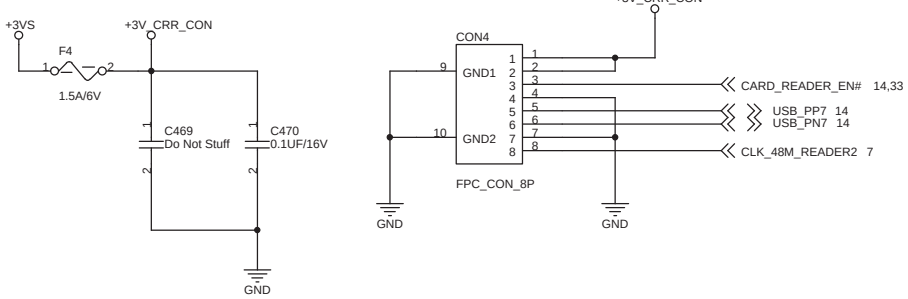
ASUSTek Computer INC.	Title : Thermal Sensor	
	Engineer: *Jerry Liu*	
Size: A4	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 42 of 57	



Left Small Board

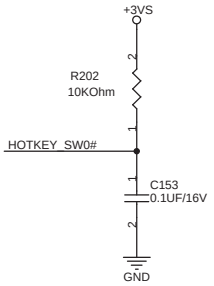


Right Small Board



2nd SD Card Reader

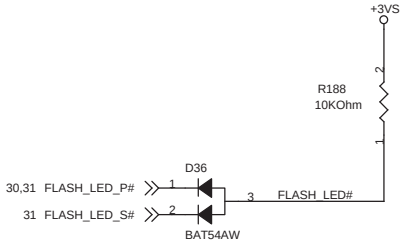
Home Key



Hotkey Table

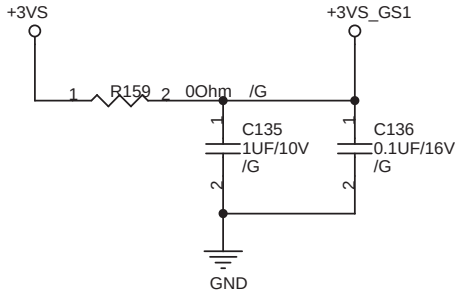
Item	Pin Name	Function
0	HOTKEY_SW0#	HOME

Flash LED

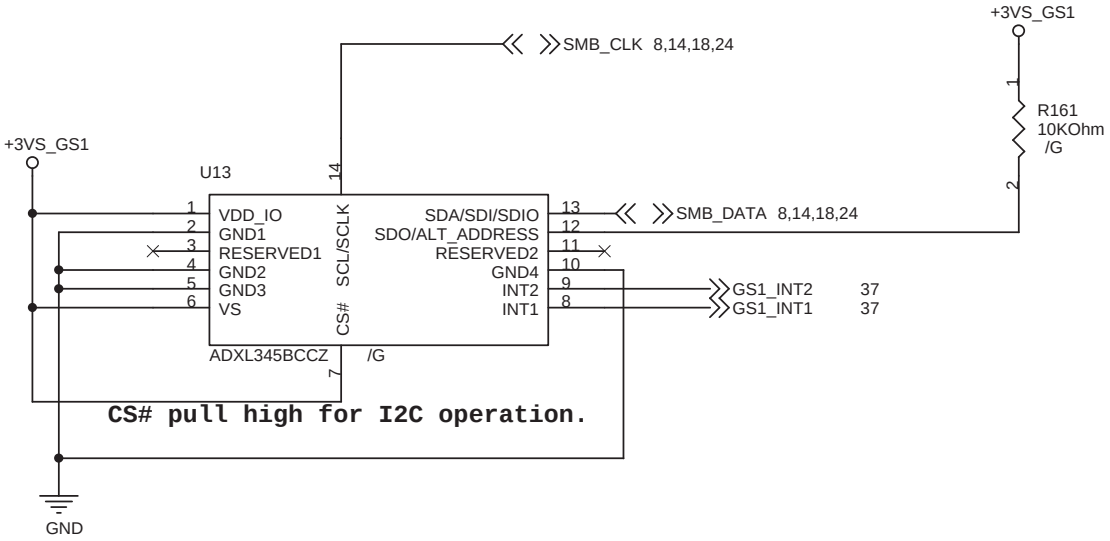


0106 1025

ASUSTek Computer INC.	Title : Small Board Conn	
	Engineer: *Jerry Liu*	
Size A3	Project Name **T91**	Rev 1.2G
Date: Tuesday, January 06, 2009	Sheet 43 of 57	

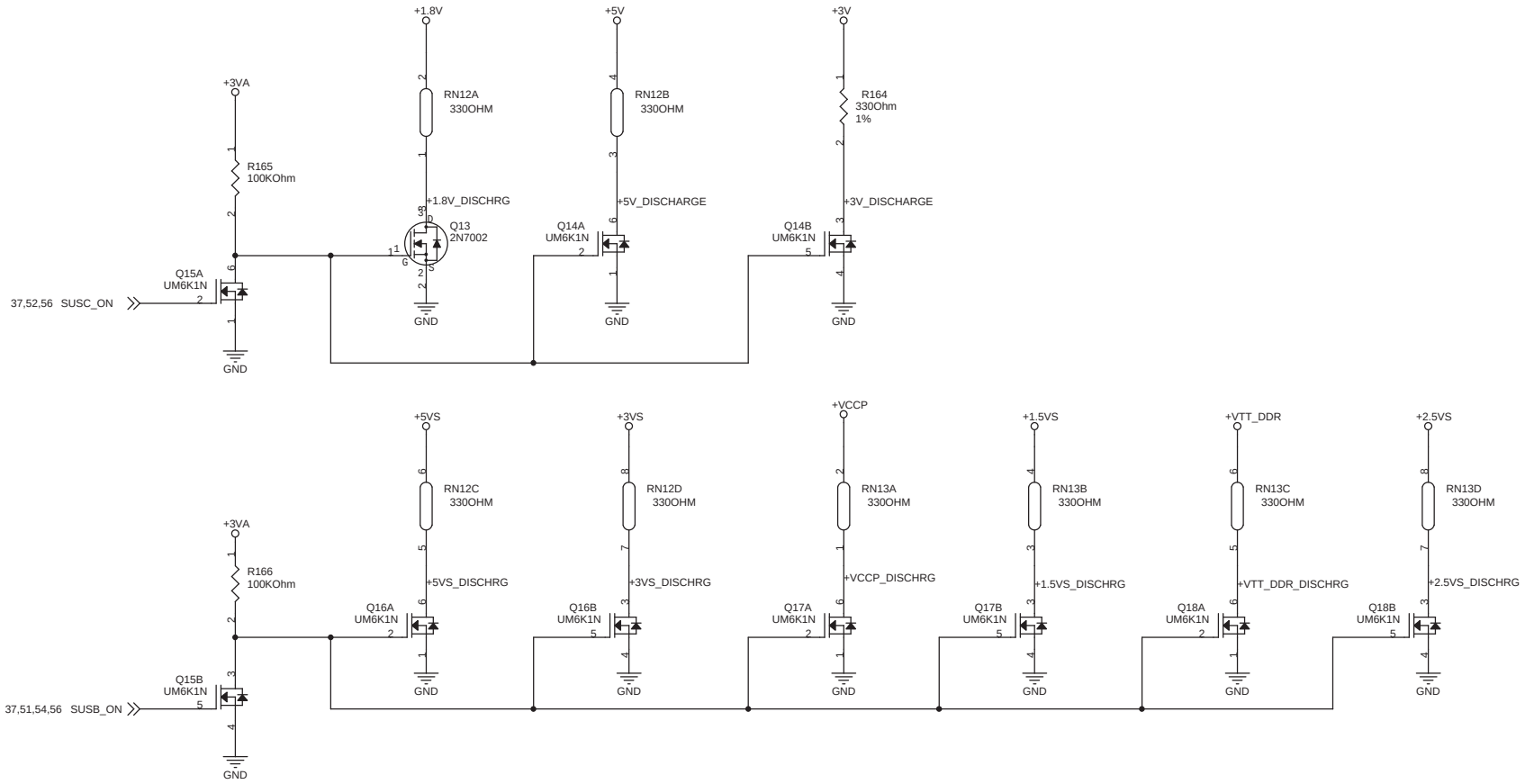


SMBUS Address: 0X1D



0106 1025

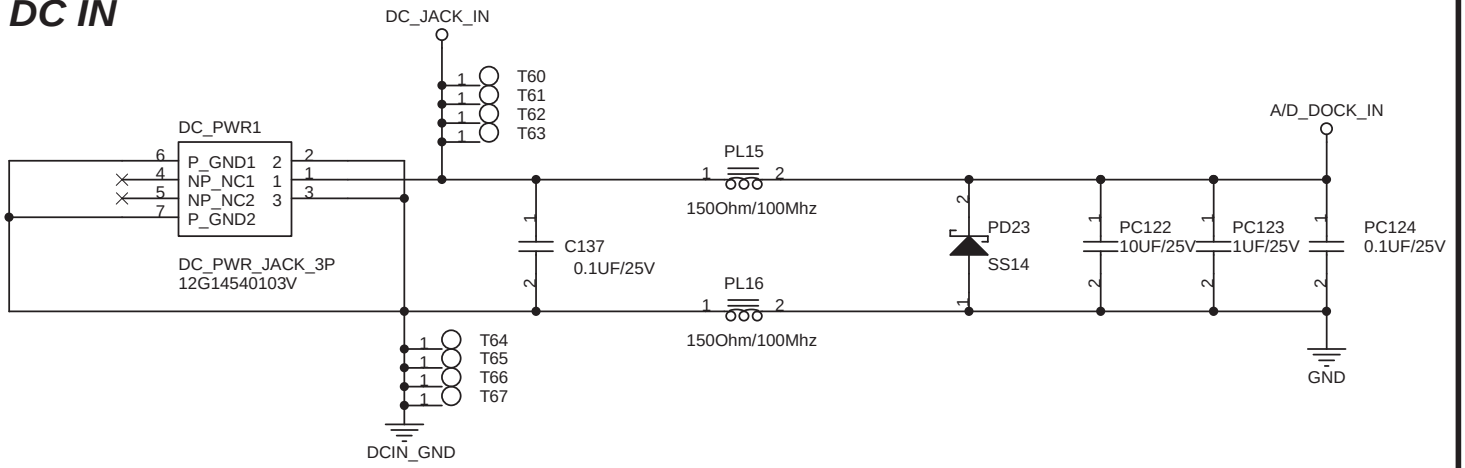
ASUSTek Computer INC.	Title : G-Sensor	
	Engineer: *Jerry Liu*	
Size: A4	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 44 of 57	



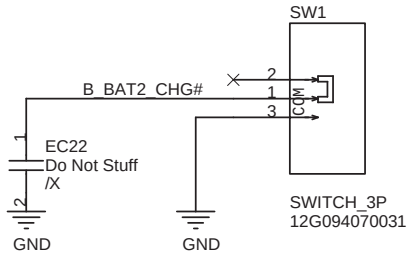
0106 1025

ASUSTek Computer INC.	Title : Discharge	
	Engineer: *Jerry Liu*	
Size: A3	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 45 of 57	

DC IN

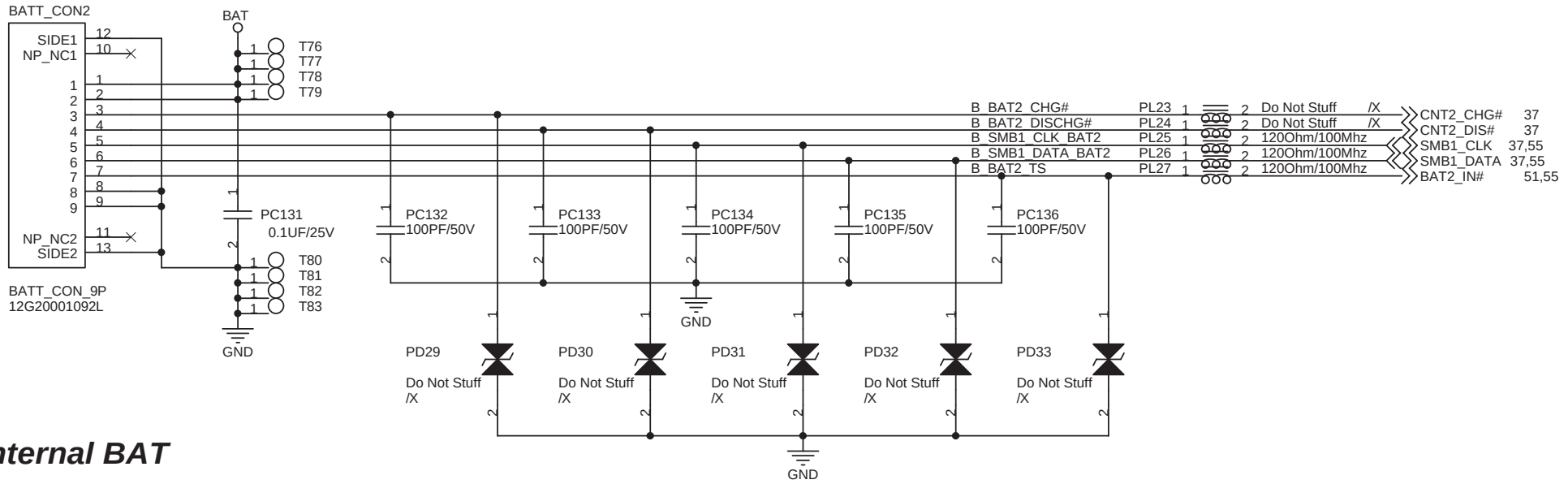


Battery Switch



CNT2_CHG# : Low : Battery ON

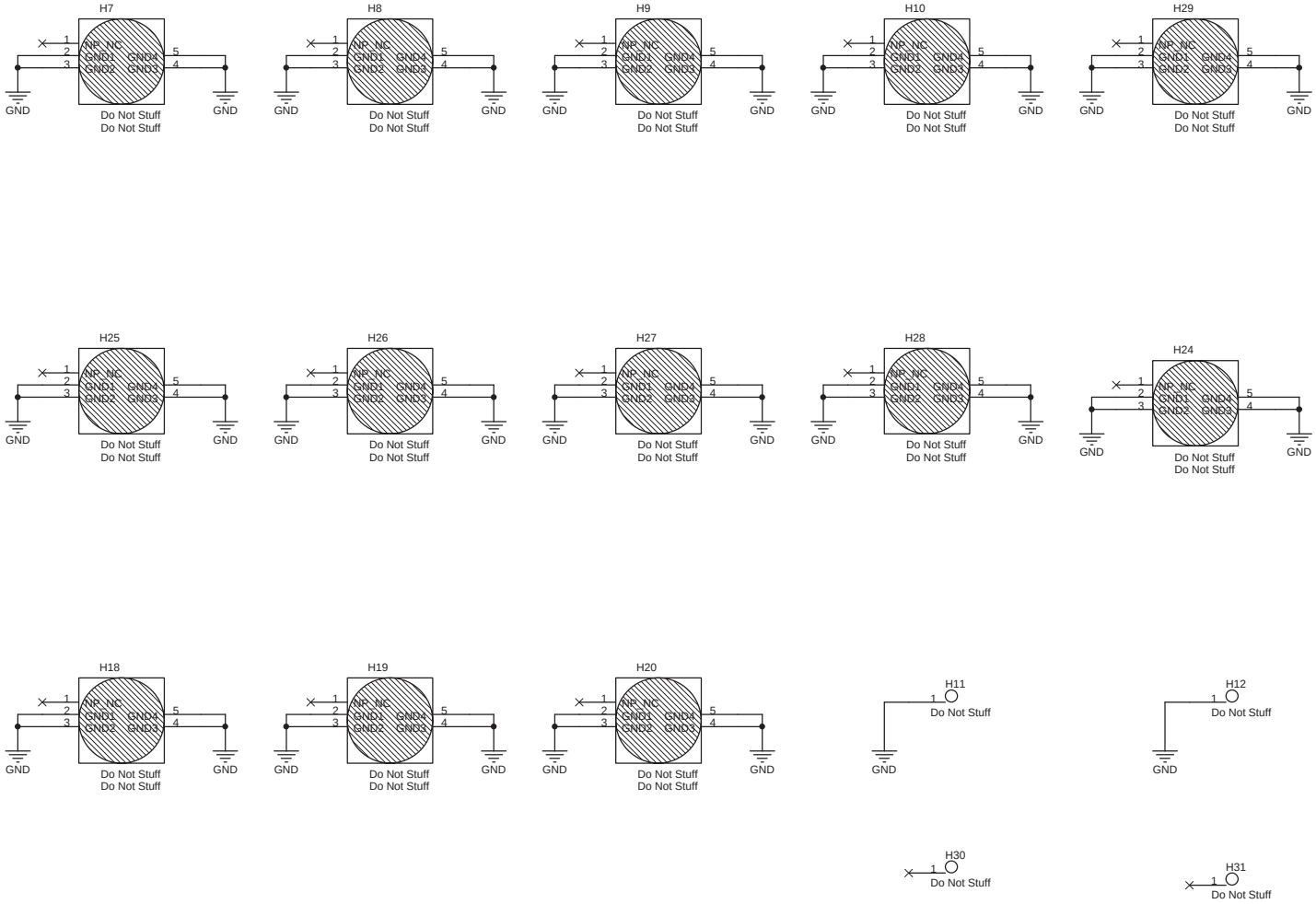
CNT2_CHG# : open : Battery OFF



Internal BAT

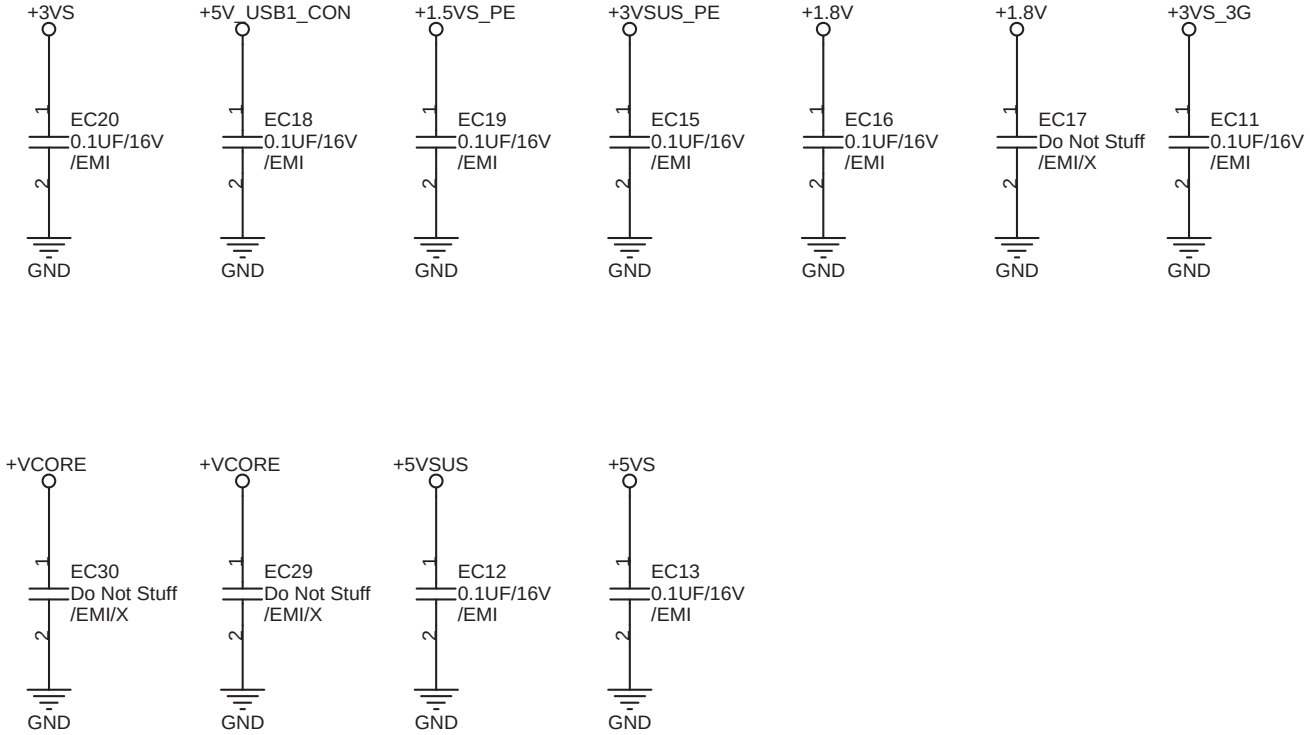
0106 1025

ASUSTek Computer INC.	Title : PWR Jack	
	Engineer: *Jerry Liu*	
Size: A4	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 46 of 57	



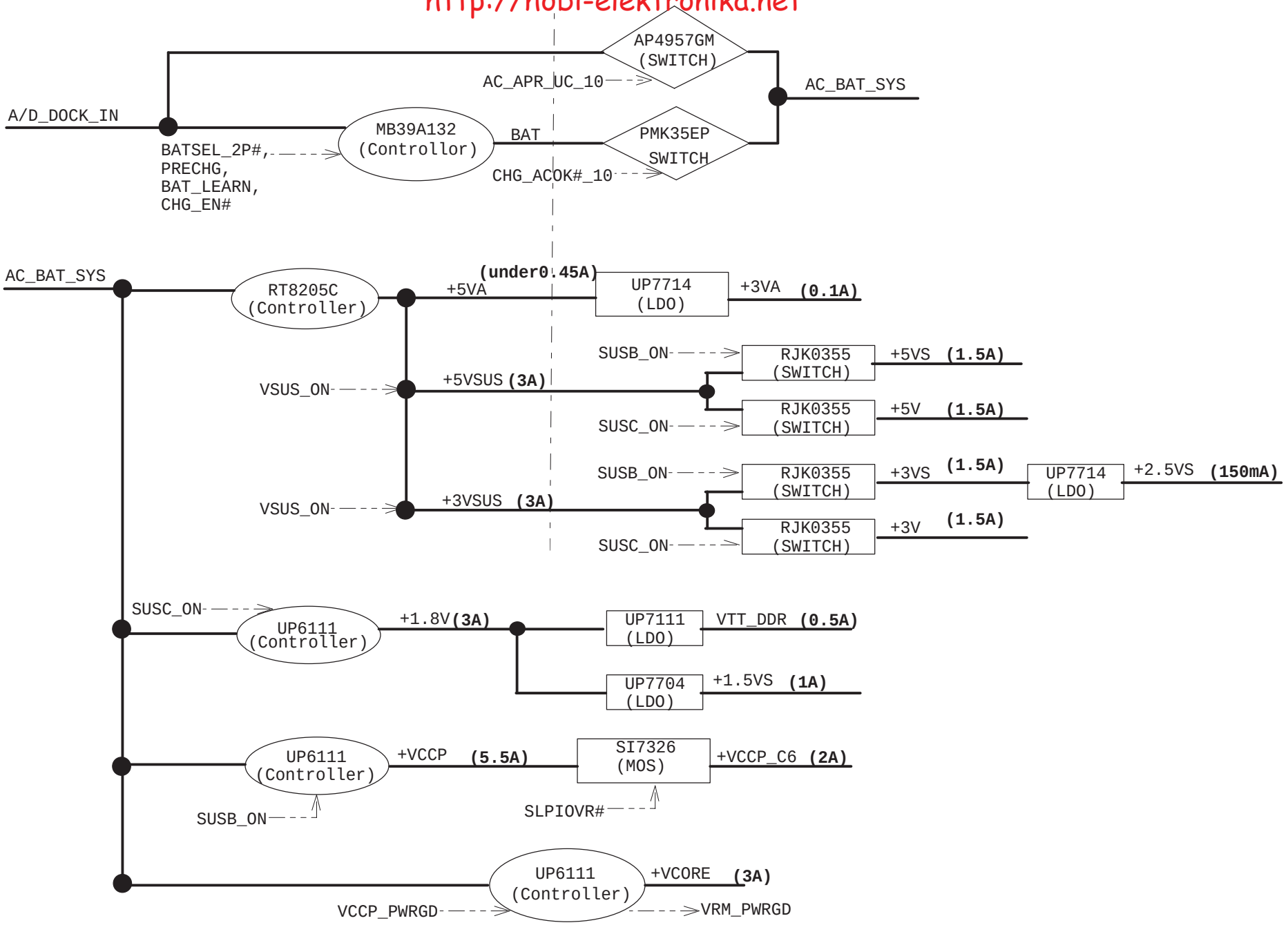
0106 1025

ASUSTek Computer INC.	Title : Screw Hole	
	Engineer: *Jerry Liu*	
Size: A3	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 47 of 57	



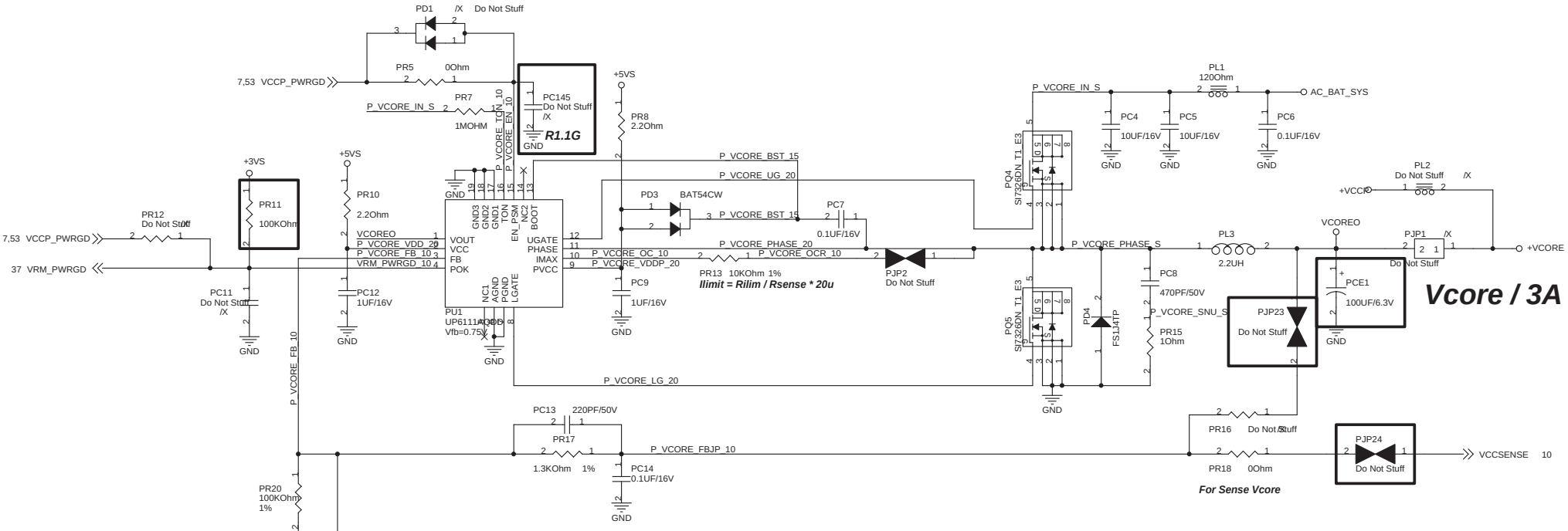
0106 1025

ASUSTek Computer INC.	Title : EMI	
	Engineer: *Jerry Liu*	
Size: A	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 48 of 57	



0106 1025

ASUSTek Computer INC.	Title : Power Flow	
	Engineer: *Jerry Liu*	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 49 of 57	

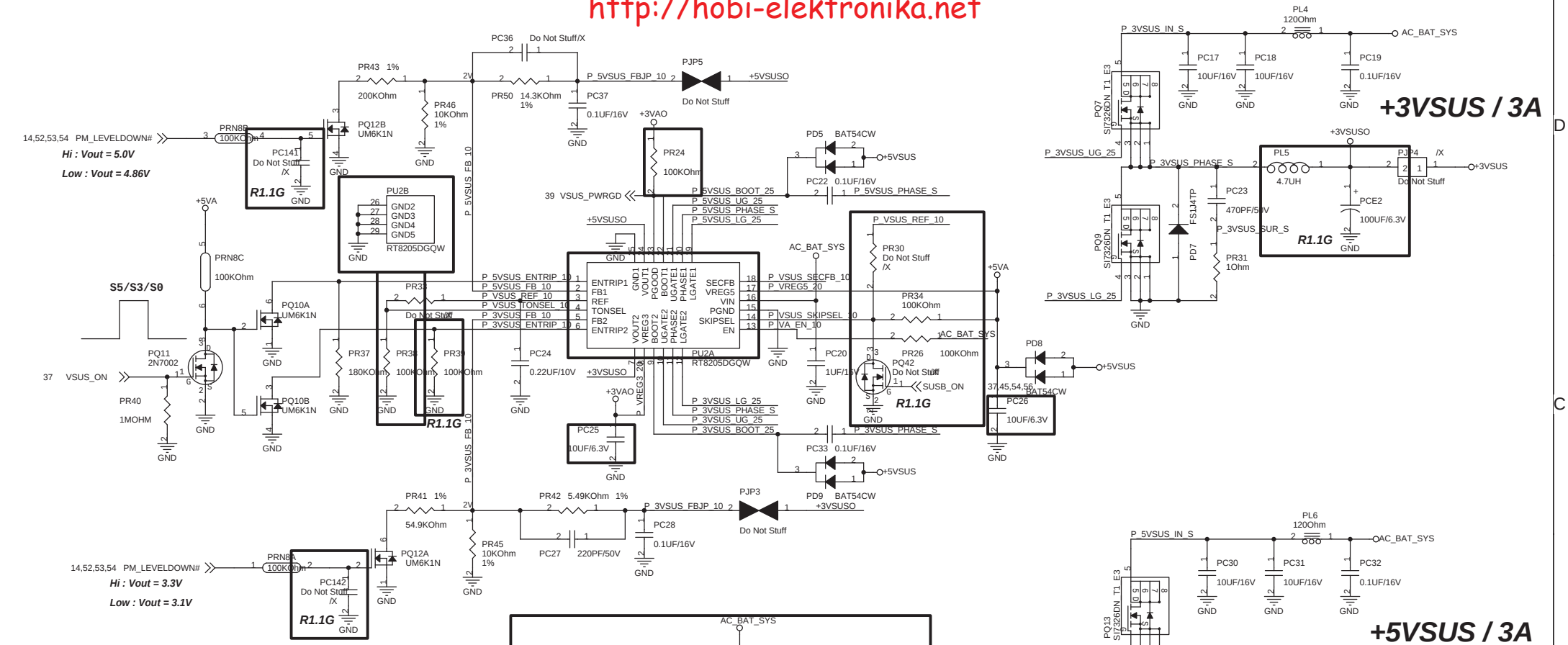


R1.2G

	Status			
THRO_CPU_VOLT#	H	L	H	L
CPU_LEVELDOWN#	H	H	L	L
Voltage	1.0484V	0.9509V	0.8573V	0.7598V
	Normal	Normal + Throttle	Power Saving	Power Saving + Throttle

0106 1025

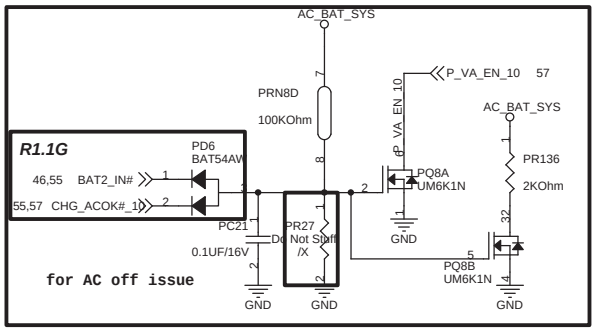
ASUSTek Computer INC.	Title : Vcore	
	Engineer: Joy_Zhou	
Size: Custom	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 50 of 57	

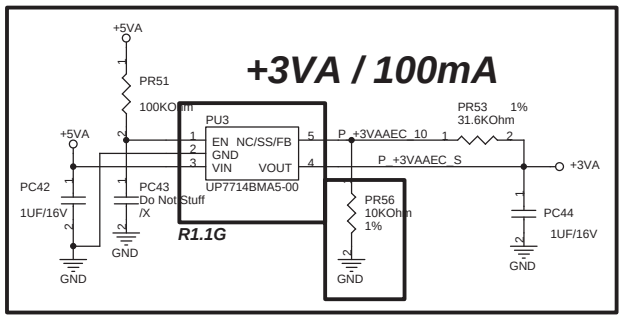


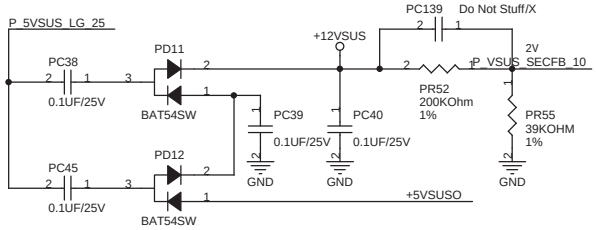
SKIPSEL:
- +5V => Ultrasonic mode
- REF => DEM mode
- GND => PWM mode

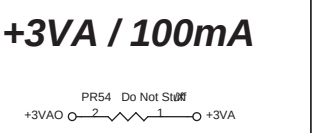
ENTRIP:
- GND => Disable
- OCP => (10uA x R) / 10 / Rdson

TONSEL:
- +5V => 400KHz / 500KHz
- REF => 300KHz / 375KHz
- GND => 200KHz / 250KHz



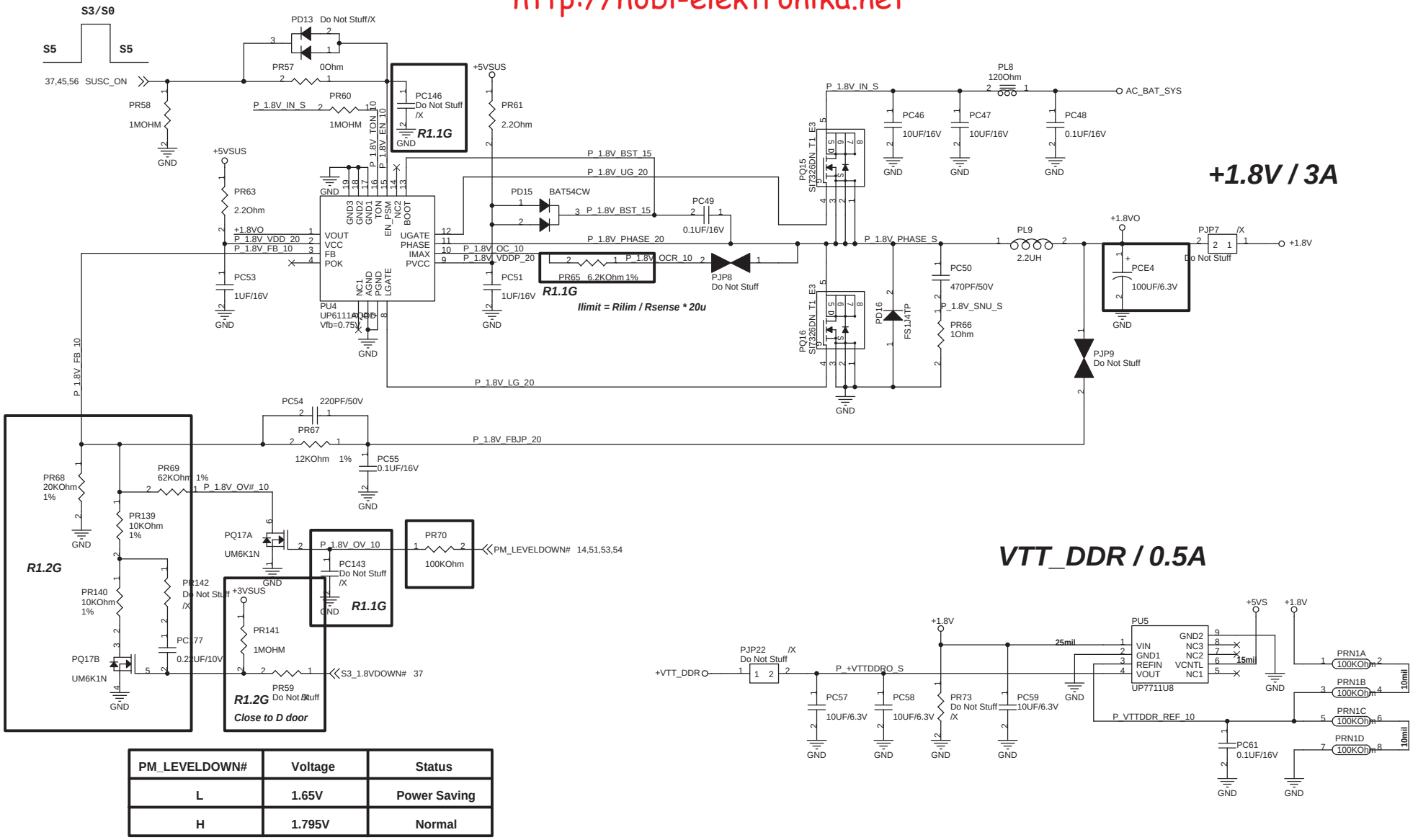






0106 1025

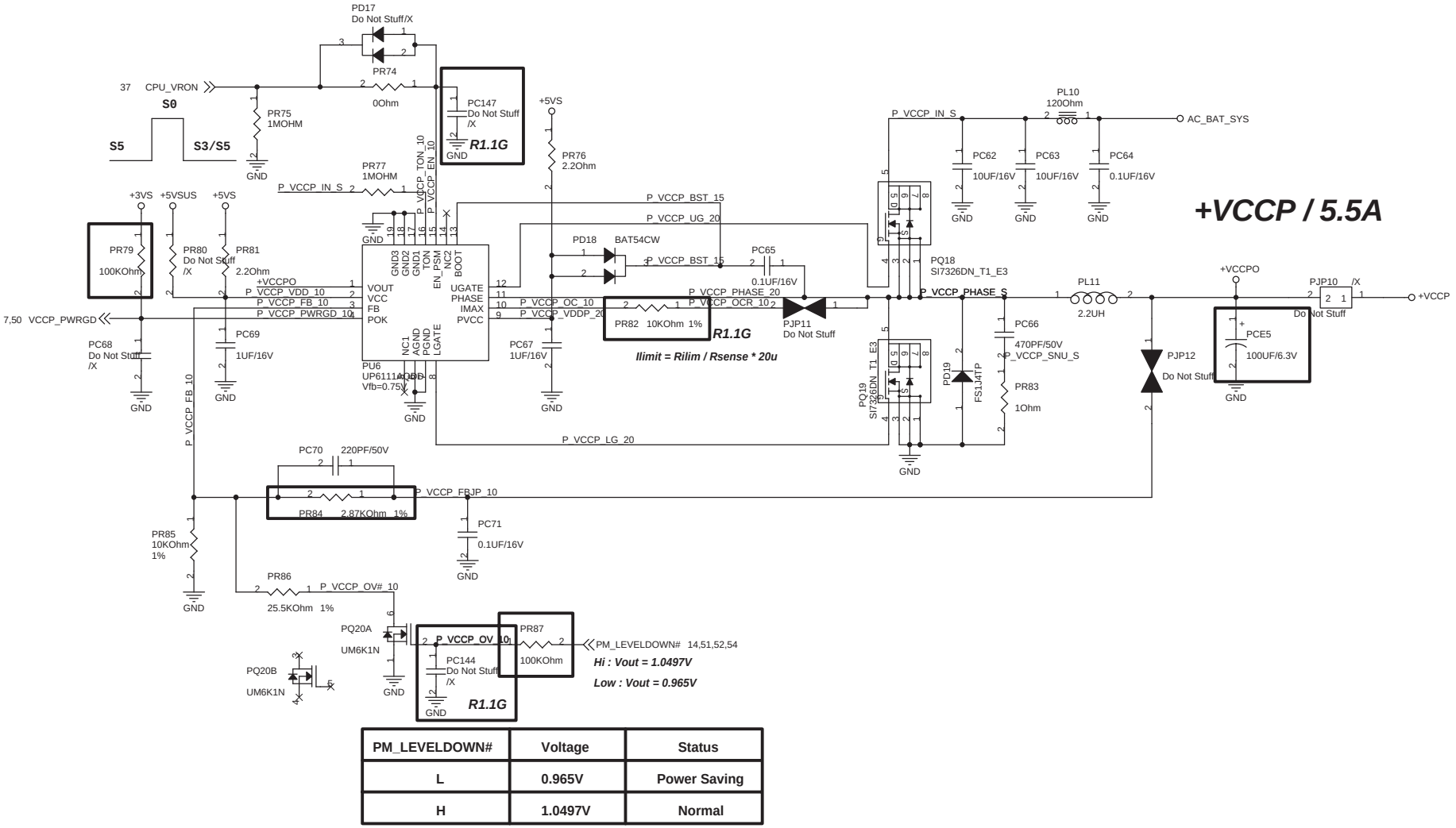
ASUSTeK COMPUTER INC	Title: +3VSUS & +5VSUS & +3VA	
	Engineer: N/A	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 51 of 57	



PM_LEVELDOWN#	Voltage	Status
L	1.65V	Power Saving
H	1.795V	Normal

0106 1025

ASUSTek Computer INC.	Title : +1.8V & VTTDDR	
	Engineer: Joy_Zhou	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 52 of 57	

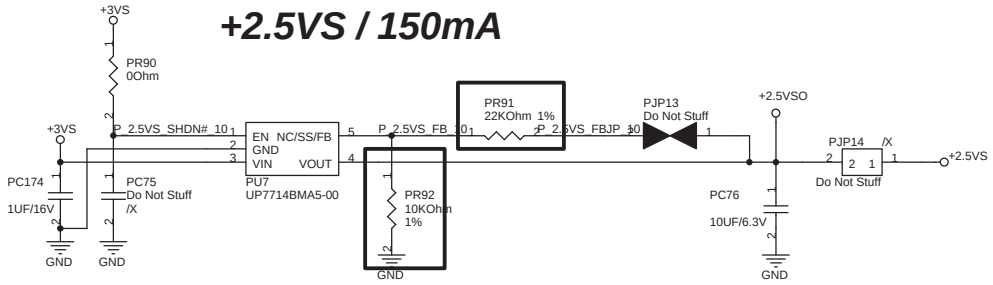


PM_LEVELDOWN#	Voltage	Status
L	0.965V	Power Saving
H	1.0497V	Normal

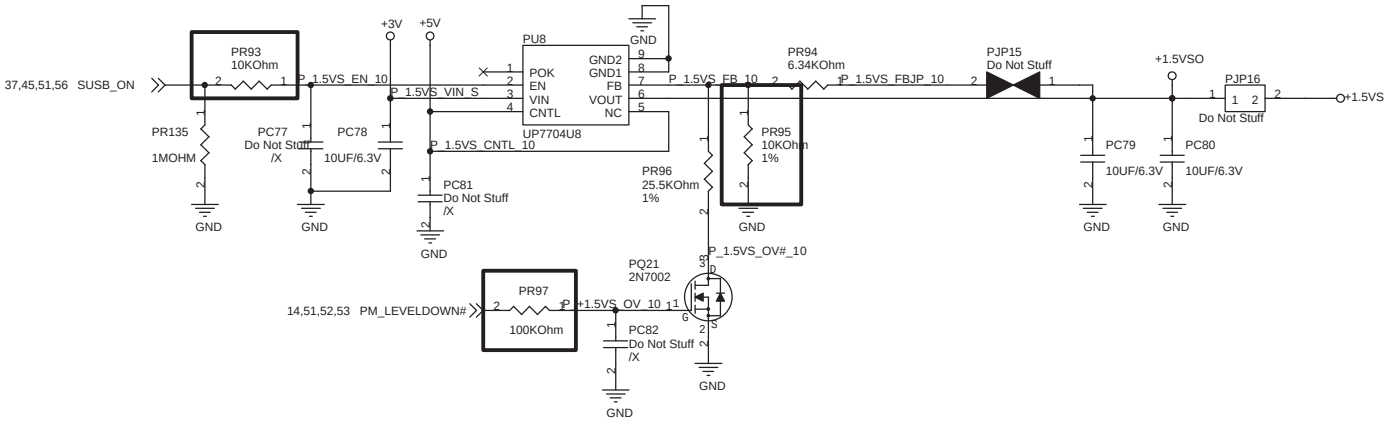
0106 1025

ASUSTek Computer INC.	Title : VCCP	
	Engineer: Joy_Zhou	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 53 of 57	

+2.5VS / 150mA

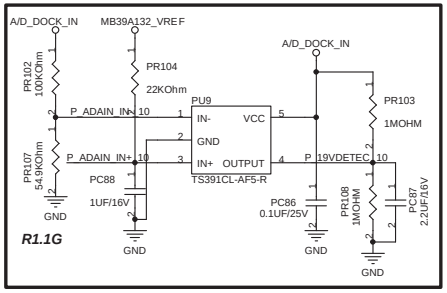


+1.5VS / 1A



0106 1025

ASUSTek Computer INC.	Title : +1.5VS & +2.5VS	
	Engineer: Joy_Zhou	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 54 of 57	



Prevent Input from 19V :

Adaptor > 14.2V, PQ603B Turn-off

Adaptor < 12.4V, PQ603B Turn-on

VREF = 5.0V

fosc(KHz) = 17000 / RT (KOhm)

*Soft start: ts(s) = 0.13 * CS (uF)*

VTH of -IN1: 5V / 62 * (100+62) = 13.06V

VTH of ACIN: 1.25V / 25 * (185+25) = 10.5V
Change PR607 and PR608 value

Prevent Input from 19V :

Adaptor > 13.06V, PQ603B Turn-off

Adaptor < 13.06V, PQ603B Turn-on

Battery Cell Selection :

BAT_LEARN = 1, Battery discharges

BAT_ID = 1, 2 Cells; Vadj2 = 0.998V

=> Icharge = 1.477A

BAT_ID = 0, 4/6 Cells; Vadj2 = 1.648V

=> Icharge = 2.517A

Pre-Charging Mode :

Precharging current = 150mA

Vadj2 = 168.75mV

Adaptor Max. Current :

PR600=235.8K; Ilimit = 2.170A; 20.615W (9.5V/22W)

PR600=185.3K; Ilimit = 2.677A; 32.124W (12V/36W)

ACIN Threshold = 1.25V

Adaptor > 10.5V, System Powered by Adaptor

Adaptor < 10.5V, System Powered by Battery

Battery Charging Voltage :

Vadj3 > 4.1V ==> Vbat = 4.2V /cell

2.2V>Vadj3>1.1V ==> Vbat = 2*Vadj3 /cell

Battery Charging Current :

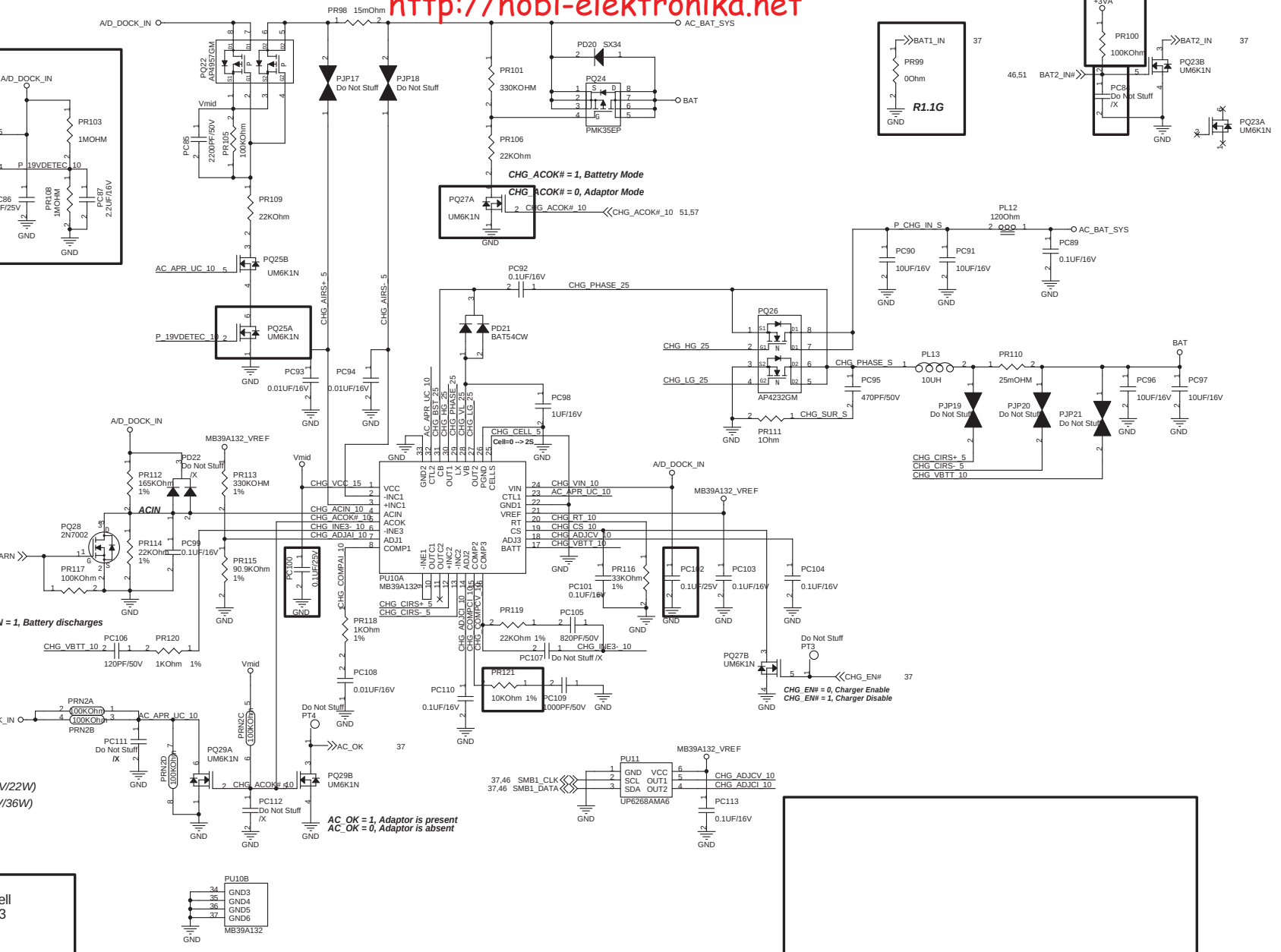
4.4V > Vadj2 >= 0V ==>

Ichg =

(Vadj2-0.075)/(25*Rs)

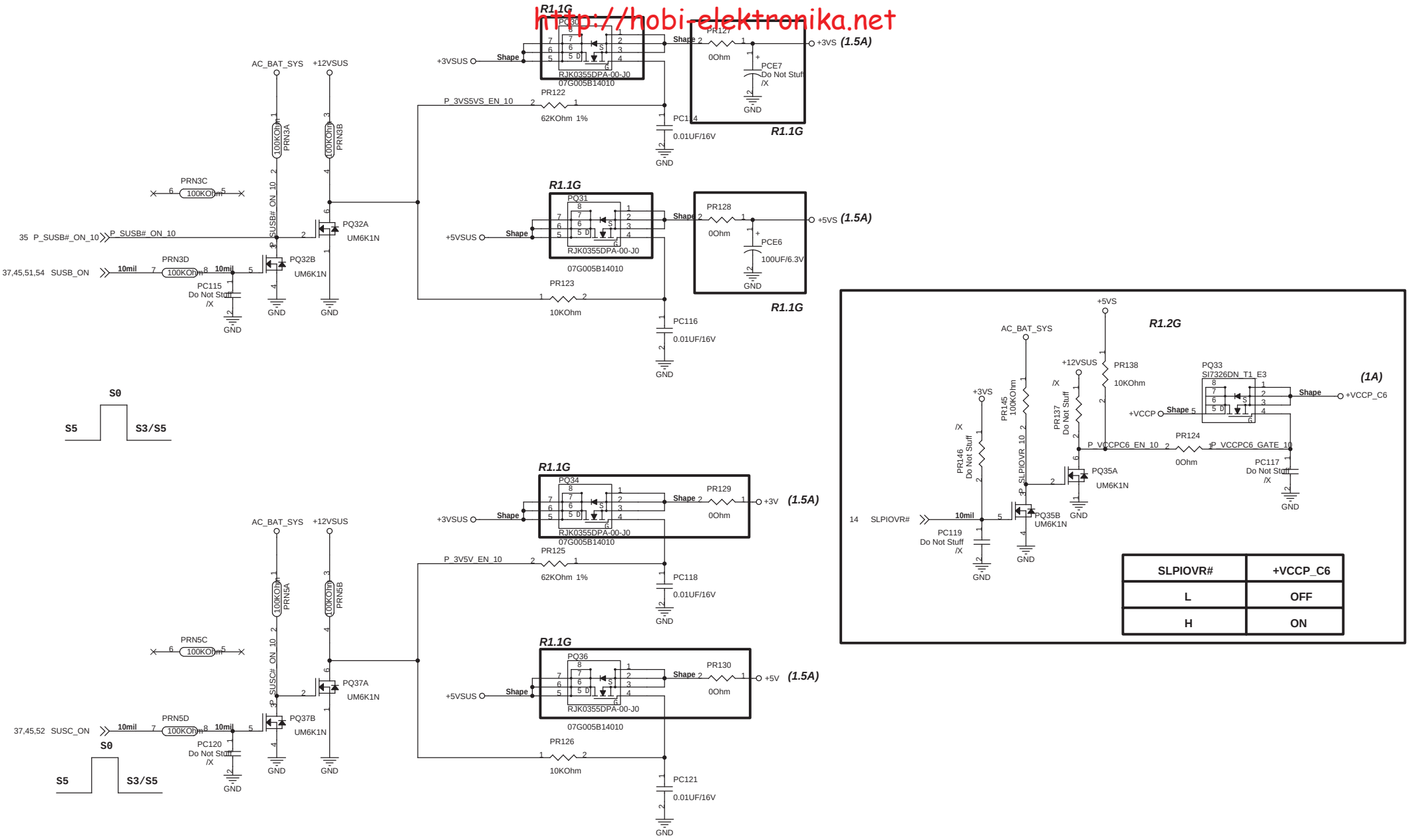
Input Adaptor Max. Current Limit :

Ilimit_current = (Vadj1-0.075) / (25*Rs)



0106 1025

ASUSTek Computer INC.	Title : CHARGER	
	Engineer: Yaohwa_Chen	
Size: Custom	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 55 of 57	



SLPIOVR#	+VCCP_C6
L	OFF
H	ON

0106 1025

Title: <Title>		
Size: A3	Document Number: <Doc>	Rev: <RevCode>
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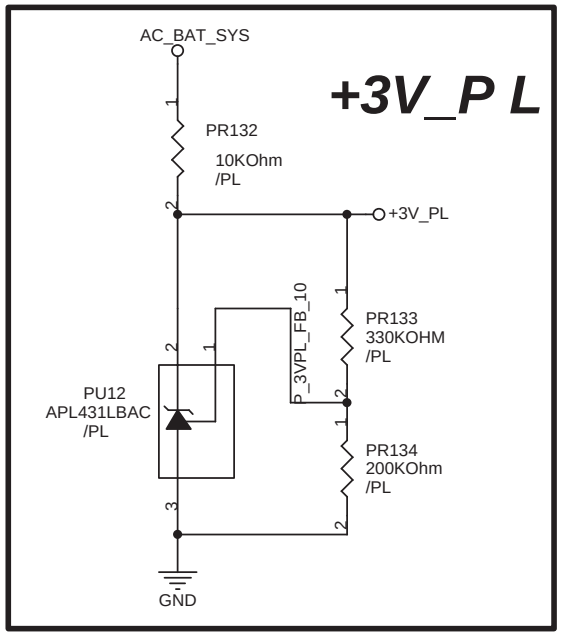

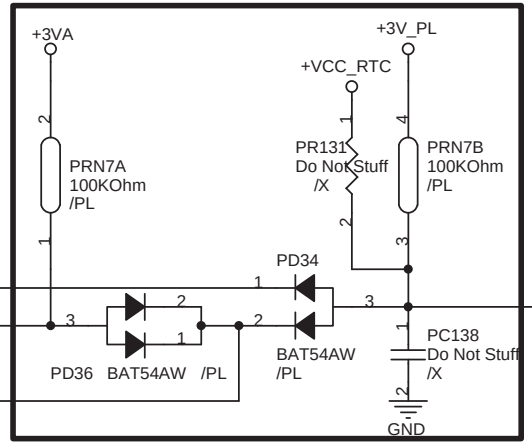

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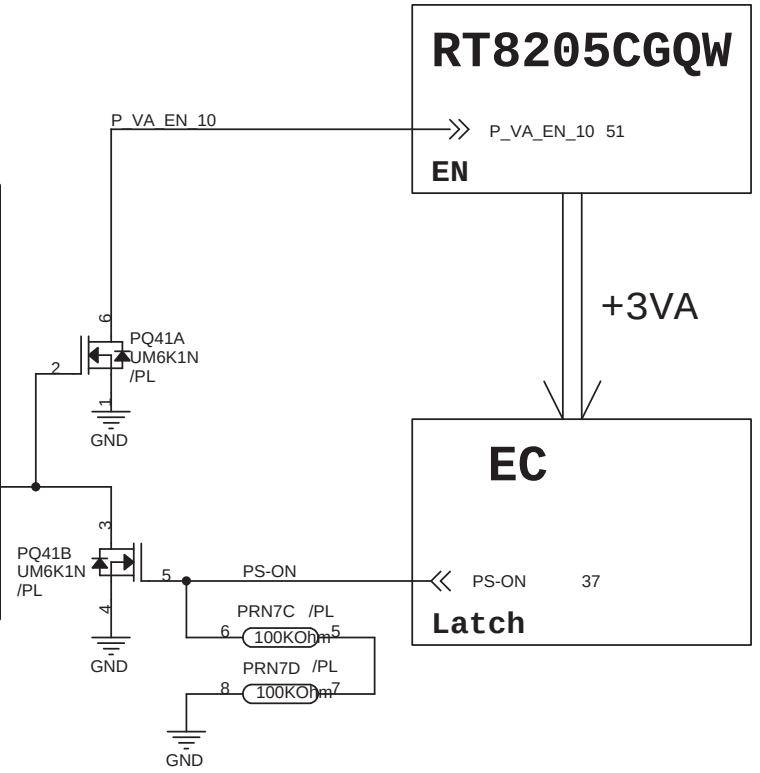

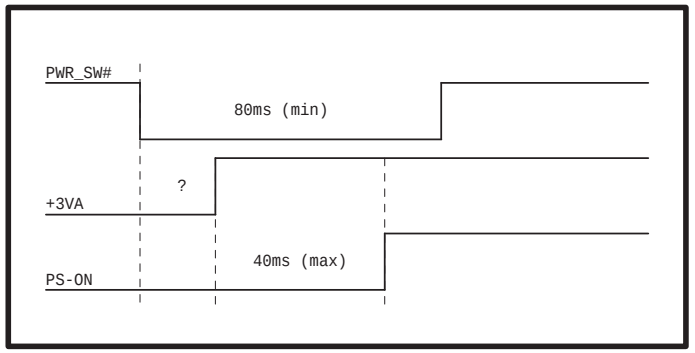

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ASUSTek Computer INC.	Title : Power Latch	
	Engineer: Jerry Liu	
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