

A8E/A8S Merom/GM965/PM965 BLOCK DIAGRAM

Sub block Diagram /
BOM option

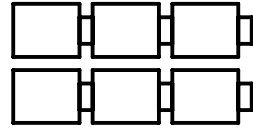
64

CLOCK GEN
ICS9LPR363AGLF-T

29

BATTERY
TYPE

3S2P



CPU
MEROM

3, 4

CPU
CAP

5

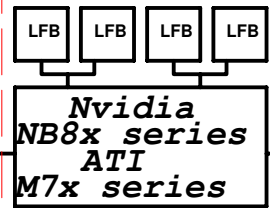
POWER
SEQUENCE

2

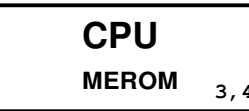
DVI Dual
CH. 47

CRT & TV
CON 46

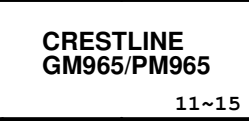
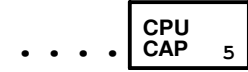
LVDS & INV
CON 45



PCI-E
x16

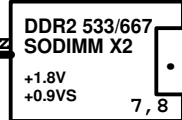


HOST BUS



11~15

DDR2 SDRAM 533/667MHz



7, 8

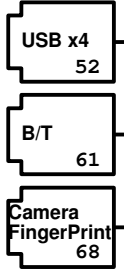


9



50

VCORE
SYSTEM
1.5VS & 1.05VS
DDR & VTT
+3VAO & +2.5VS
CHARGER
PIC
DETECT
PROTECT
LOAD SWITCH
FLOWCHART
SIGNAL



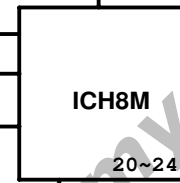
B/T 61



USB2.0

SATA

PATA

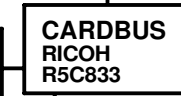
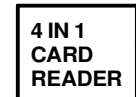


20~24

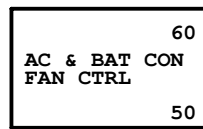
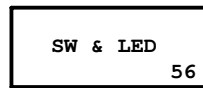
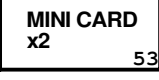
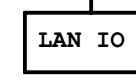
PCI EXPRESS X1

PCI BUS 3.3V, 33MHz

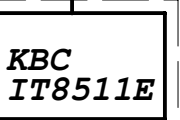
ACZ



1394



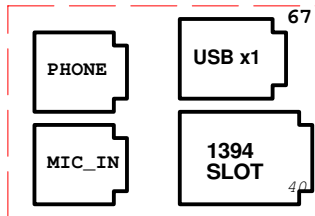
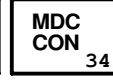
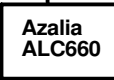
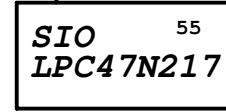
60



30, 31



NEW CARD
(DEBUG)

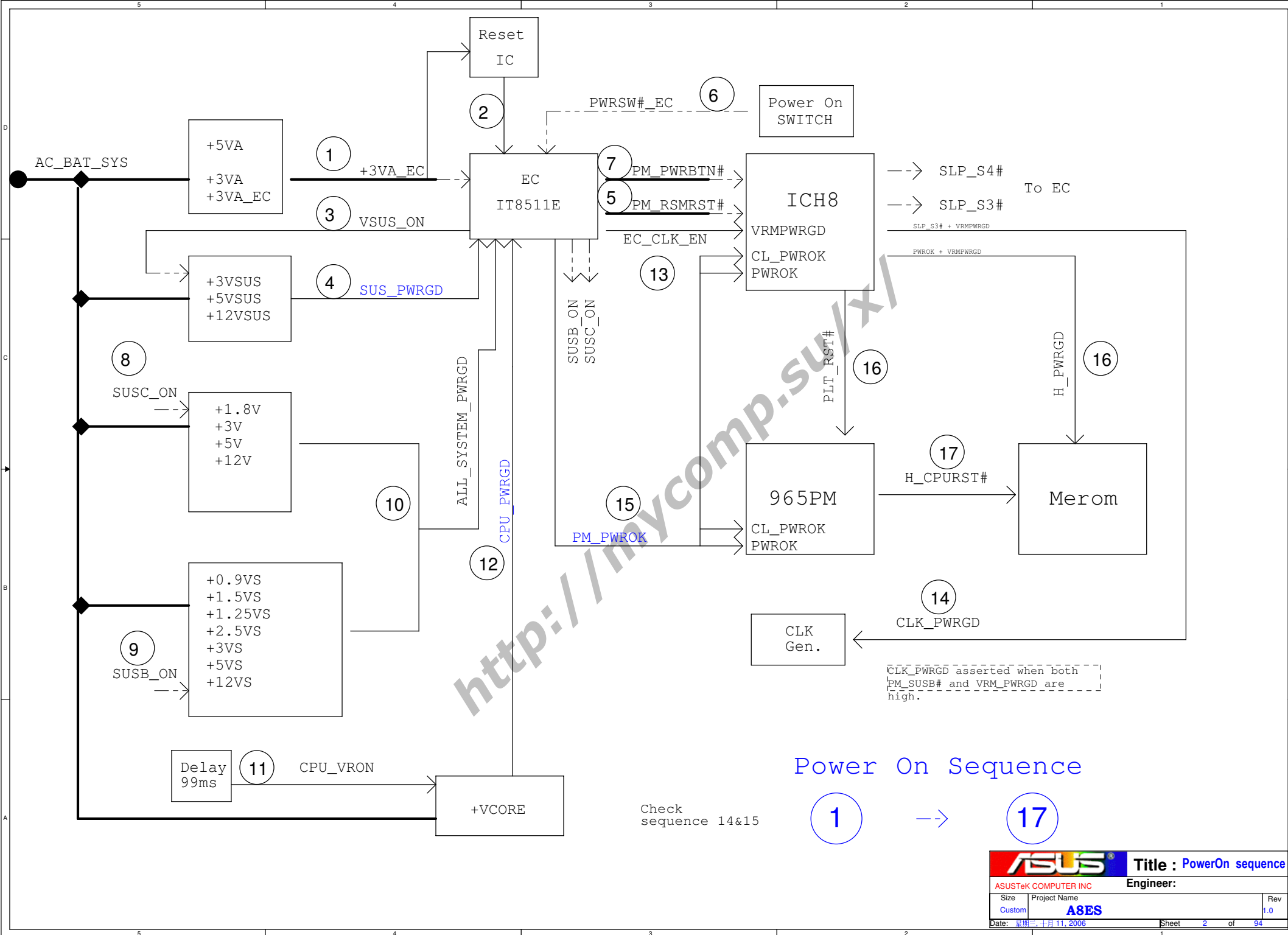


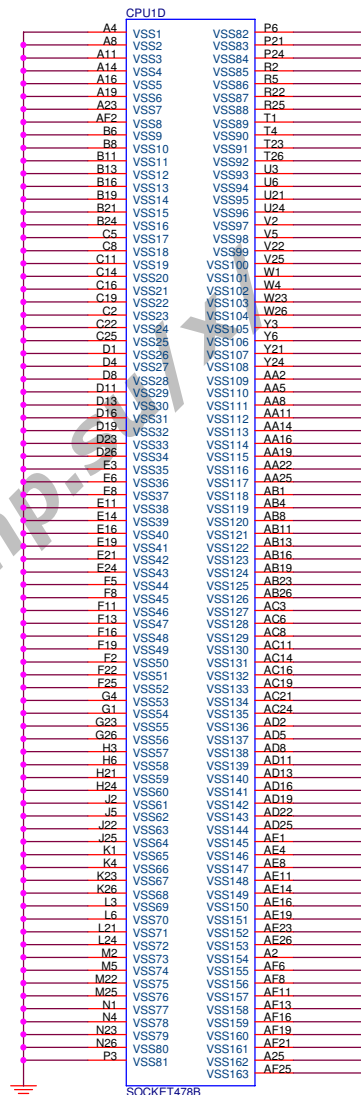
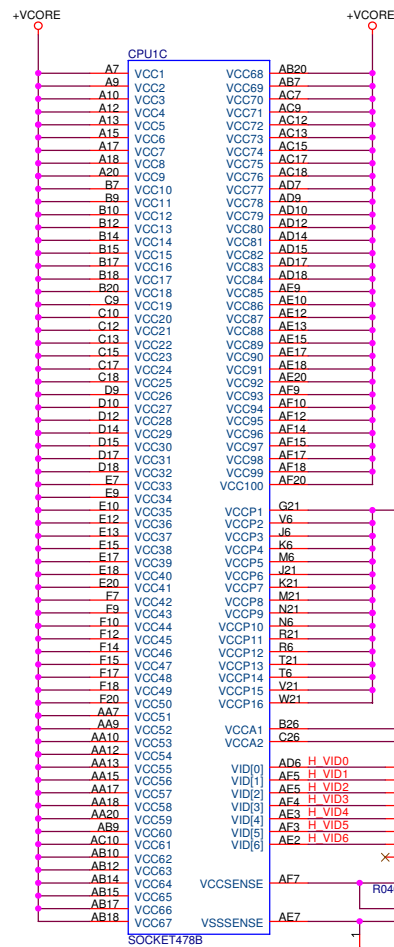
67

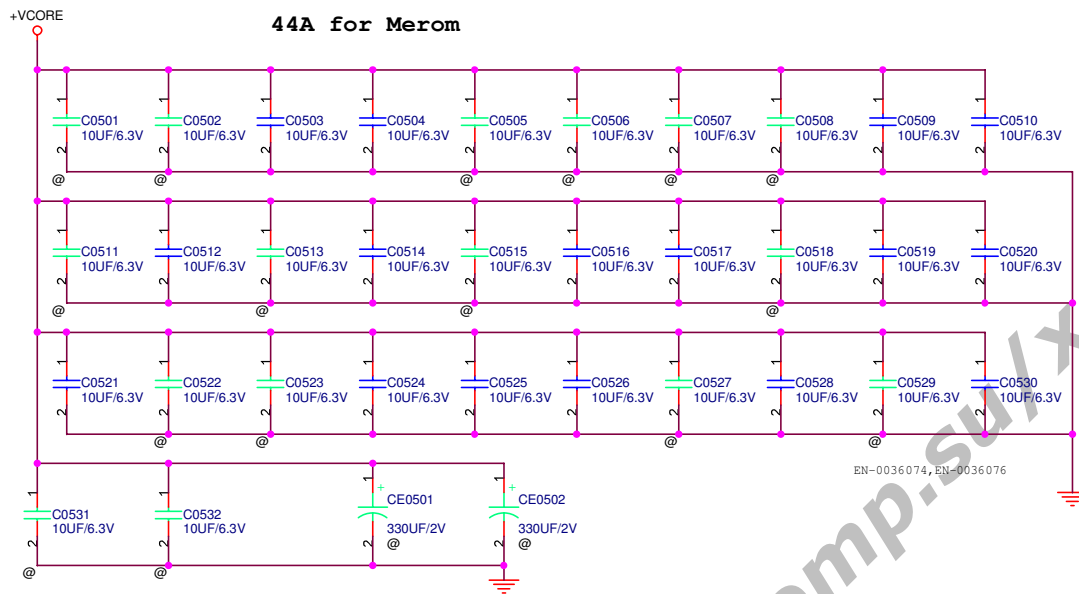
40

<Variant Name>

ASUS		Title : BLOCKDIAGRAM	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	2.0	
Date: 星期一, 一月 29, 2007		Sheet	1 of 94





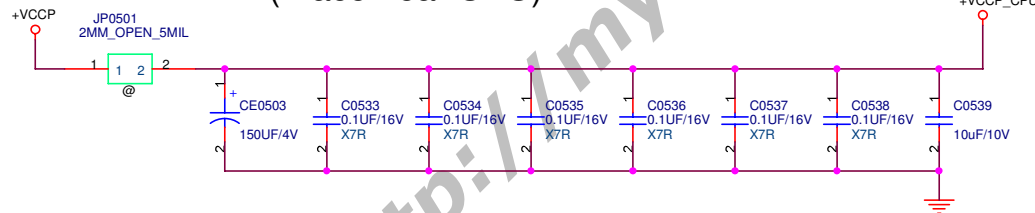


Decoupling guide from INTEL

VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

VCORE	10uF/10V	* 32pcs
	330uF/2V	* 0pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU
	10uF/10V	* 1pcs

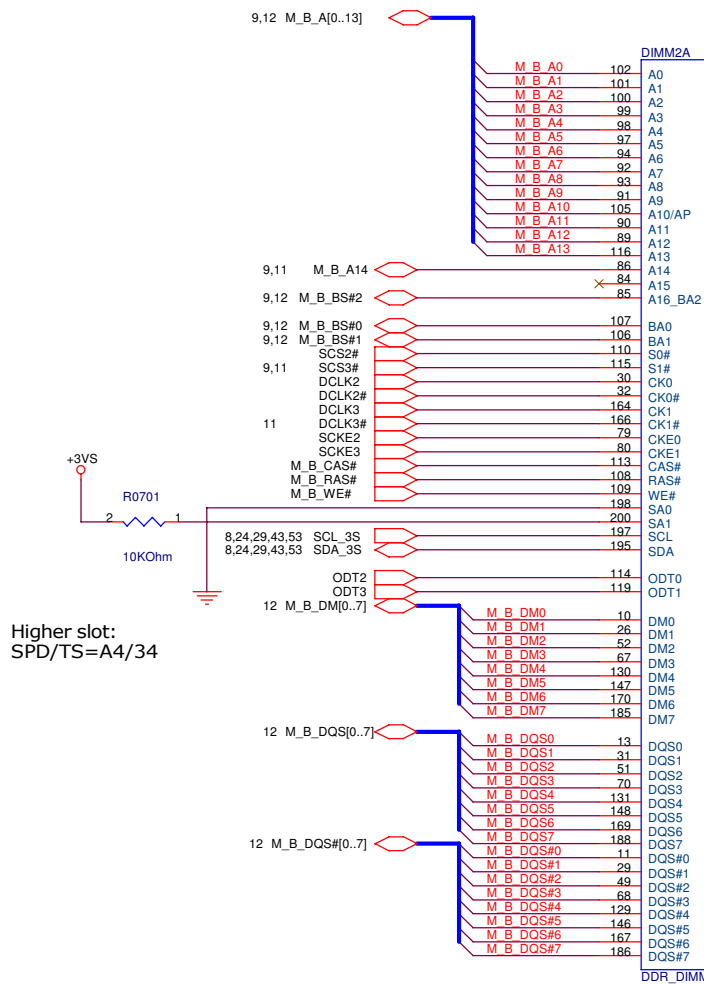
**+VCCP Decoupling Capacitor
(Place near CPU)**



	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

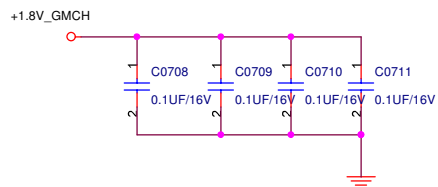
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: 星期三, 十月 11, 2006		Sheet 6 of 94	

<http://mycomp.su/x/>

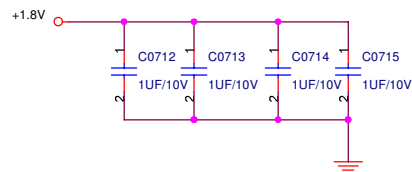


Higher slot:
SPD/TS=A4/34

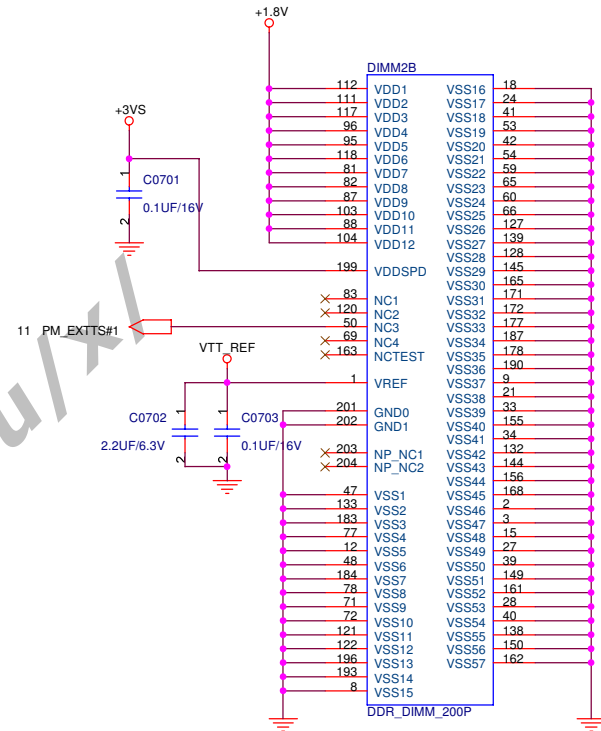
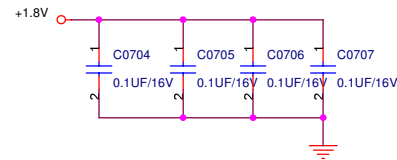
Layout Note: Place these High-Freq decoupling Caps near the GMCH



Layout Note: Place these Caps near SO DIMM 0



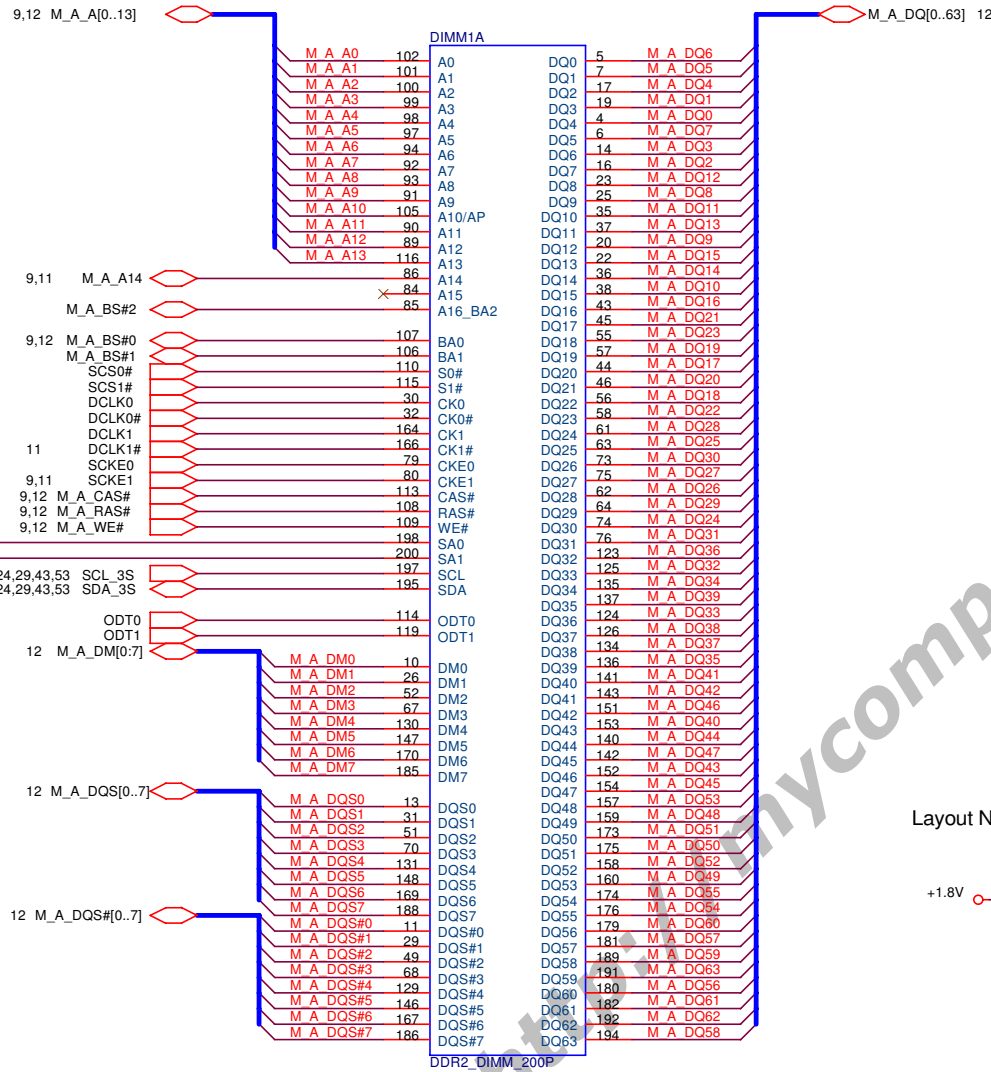
Layout Note: Place these Caps near SO DIMM 0



Upper:Channel B

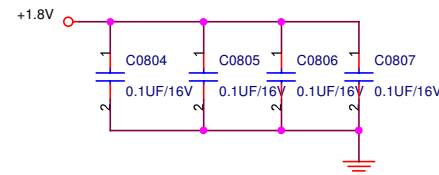
ASUS		Title :DDR SO-DIMM	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	1.0	
Date: 星期二, 三月 06, 2007	Sheet 7 of 94		

Lower slot:
SPD/TS=A0/30

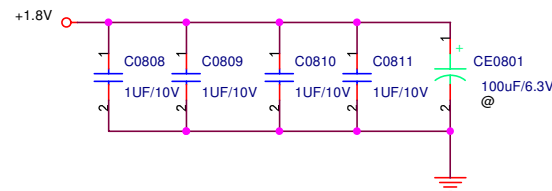


12G025022004 A8ES.PR

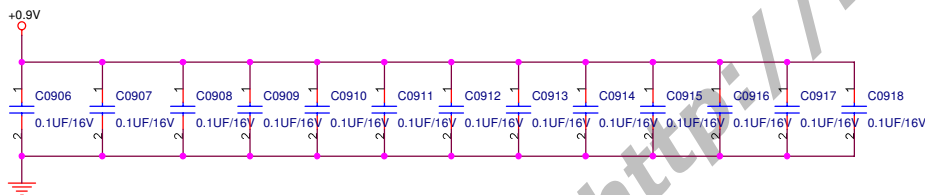
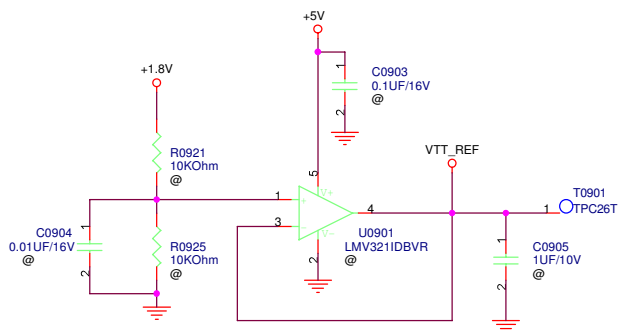
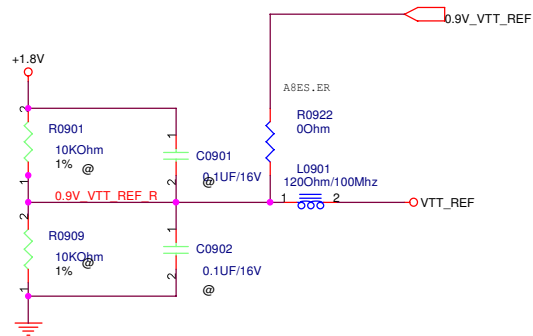
Layout Note: Place these Caps near SO DIMM 1



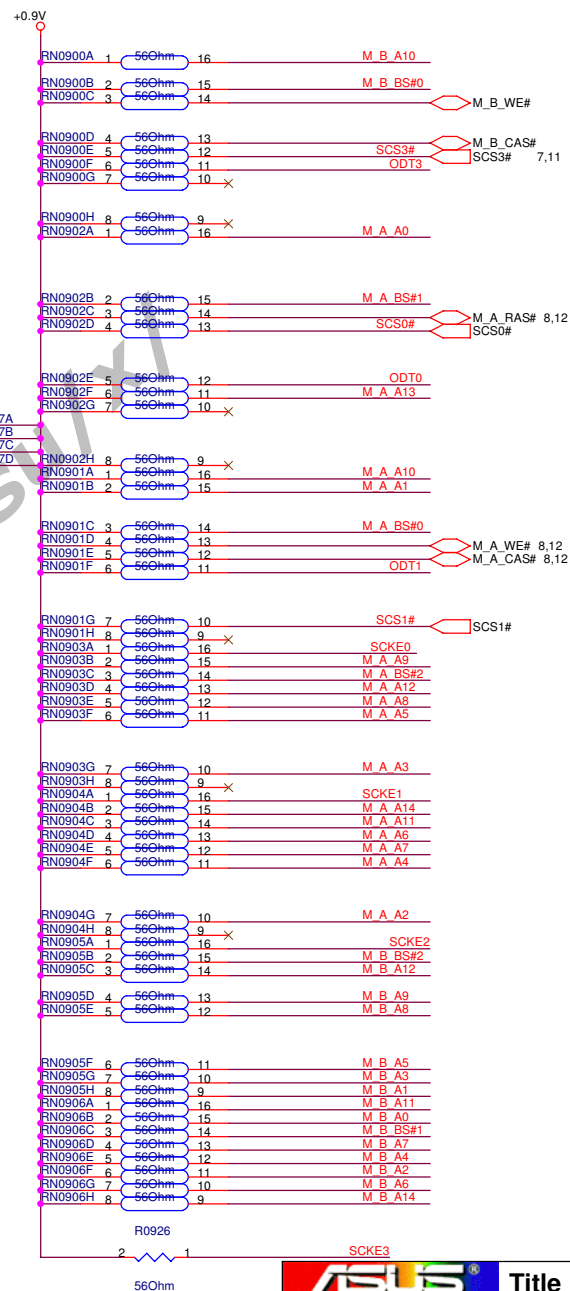
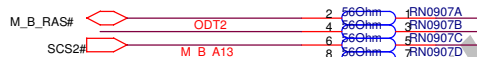
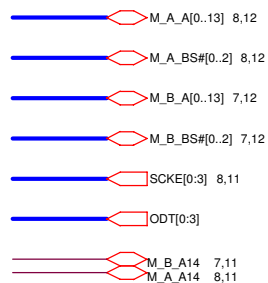
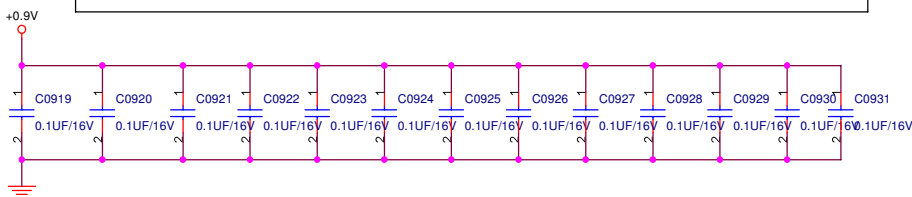
Layout Note: Place these Caps near SO DIMM 1

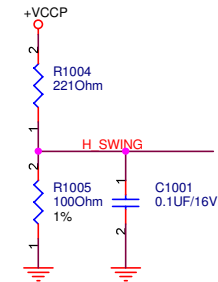
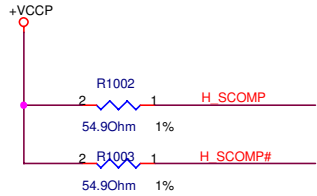


Lower:Channel A



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V





T1001
TPC26T

H_CPURST#
H_CPUSLP#

+VCCP

C1002
0.1UF/10V

R1007
1KOhm
1%

H_VREF

R1008
2KOhm
1%

H_D#0	E2	H_D#_0
H_D#1	G2	H_D#_1
H_D#2	G2	H_D#_2
H_D#3	M6	H_D#_3
H_D#4	H7	H_D#_4
H_D#5	H3	H_D#_5
H_D#6	G4	H_D#_6
H_D#7	F3	H_D#_7
H_D#8	N8	H_D#_8
H_D#9	H2	H_D#_9
H_D#10	M10	H_D#_10
H_D#11	N12	H_D#_11
H_D#12	N9	H_D#_12
H_D#13	H5	H_D#_13
H_D#14	P13	H_D#_14
H_D#15	K9	H_D#_15
H_D#16	M2	H_D#_16
H_D#17	W10	H_D#_17
H_D#18	Y8	H_D#_18
H_D#19	V4	H_D#_19
H_D#20	M3	H_D#_20
H_D#21	J1	H_D#_21
H_D#22	N5	H_D#_22
H_D#23	N3	H_D#_23
H_D#24	W6	H_D#_24
H_D#25	W9	H_D#_25
H_D#26	N2	H_D#_26
H_D#27	Y7	H_D#_27
H_D#28	Y9	H_D#_28
H_D#29	P4	H_D#_29
H_D#30	W3	H_D#_30
H_D#31	N1	H_D#_31
H_D#32	AD12	H_D#_32
H_D#33	AE3	H_D#_33
H_D#34	AD9	H_D#_34
H_D#35	AC9	H_D#_35
H_D#36	AC7	H_D#_36
H_D#37	AC14	H_D#_37
H_D#38	AD11	H_D#_38
H_D#39	AB2	H_D#_39
H_D#40	AD7	H_D#_40
H_D#41	AB1	H_D#_41
H_D#42	Y3	H_D#_42
H_D#43	Y3	H_D#_43
H_D#44	AC6	H_D#_44
H_D#45	AE2	H_D#_45
H_D#46	AC5	H_D#_46
H_D#47	AG3	H_D#_47
H_D#48	AJ9	H_D#_48
H_D#49	AH8	H_D#_49
H_D#50	AJ14	H_D#_50
H_D#51	AE9	H_D#_51
H_D#52	AE11	H_D#_52
H_D#53	AH12	H_D#_53
H_D#54	AJ5	H_D#_54
H_D#55	AH5	H_D#_55
H_D#56	AJ6	H_D#_56
H_D#57	AE7	H_D#_57
H_D#58	AJ7	H_D#_58
H_D#59	AJ2	H_D#_59
H_D#60	AE5	H_D#_60
H_D#61	AJ3	H_D#_61
H_D#62	AH2	H_D#_62
H_D#63	AH13	H_D#_63

H_SWING B3
H_RCOMP C2
H_SCOMP W1
H_SCOMP# W2

H_CPURST# B6
H_CPUSLP# E5

H_AVREF B9
H_DVREF A9

CRESTLINE_965PM

HOST

H_A#_3	J13	H_A#3
H_A#_4	B11	H_A#4
H_A#_5	C11	H_A#5
H_A#_6	M11	H_A#6
H_A#_7	C15	H_A#7
H_A#_8	E16	H_A#8
H_A#_9	L13	H_A#9
H_A#_10	G17	H_A#10
H_A#_11	C14	H_A#11
H_A#_12	K16	H_A#12
H_A#_13	B13	H_A#13
H_A#_14	L16	H_A#14
H_A#_15	J17	H_A#15
H_A#_16	B14	H_A#16
H_A#_17	K19	H_A#17
H_A#_18	P15	H_A#18
H_A#_19	B17	H_A#19
H_A#_20	B16	H_A#20
H_A#_21	H20	H_A#21
H_A#_22	L19	H_A#22
H_A#_23	D17	H_A#23
H_A#_24	M17	H_A#24
H_A#_25	N16	H_A#25
H_A#_26	J19	H_A#26
H_A#_27	B18	H_A#27
H_A#_28	E19	H_A#28
H_A#_29	B17	H_A#29
H_A#_30	B15	H_A#30
H_A#_31	E17	H_A#31
H_A#_32	C18	H_A#32
H_A#_33	A19	H_A#33
H_A#_34	B19	H_A#34
H_A#_35	N19	H_A#35

H_ADS#	G12	H_ADS#
H_ADSTB#_0	H17	H_ADSTB#0
H_ADSTB#_1	G20	H_ADSTB#1
H_BNR#	C8	H_BNR#
H_BPRI#	E8	H_BPRI#
H_BREQ#	F12	H_BREQ#
H_DEFER#	D6	H_DEFER#
H_DBSY#	C10	H_DBSY#
HPLL_CLK	AM5	CLK_MCH_BCLK
HPLL_CLK#	AM7	CLK_MCH_BCLK#
H_DPWR#	H8	H_DPWR#
H_DRDY#	K7	H_DRDY#
H_HIT#	E4	H_HIT#
H_HITM#	C6	H_HITM#
H_LOCK#	G10	H_LOCK#
H_TRDY#	B7	H_TRDY#

H_DINV#_0	K5	H_DINV#0
H_DINV#_1	L2	H_DINV#1
H_DINV#_2	AD13	H_DINV#2
H_DINV#_3	AE13	H_DINV#3

H_DSTBN#_0	M7	H_DSTBN#0
H_DSTBN#_1	K3	H_DSTBN#1
H_DSTBN#_2	AD2	H_DSTBN#2
H_DSTBN#_3	AH11	H_DSTBN#3

H_DSTBP#_0	L7	H_DSTBP#0
H_DSTBP#_1	K2	H_DSTBP#1
H_DSTBP#_2	AC2	H_DSTBP#2
H_DSTBP#_3	AJ10	H_DSTBP#3

H_REQ#_0	M14	H_REQ#0
H_REQ#_1	E13	H_REQ#1
H_REQ#_2	A11	H_REQ#2
H_REQ#_3	H13	H_REQ#3
H_REQ#_4	B12	H_REQ#4

H_RS#_0	E12	H_RS#0
H_RS#_1	D7	H_RS#1
H_RS#_2	D8	H_RS#2

3 H_A#[35:3] H_A#[35:3]

3 H_REQ#[4:0] H_REQ#[4:0]

3 H_D#[63:0] H_D#[63:0]



Title :965PM -- CPU (1)

ASUSTeK COMPUTER INC

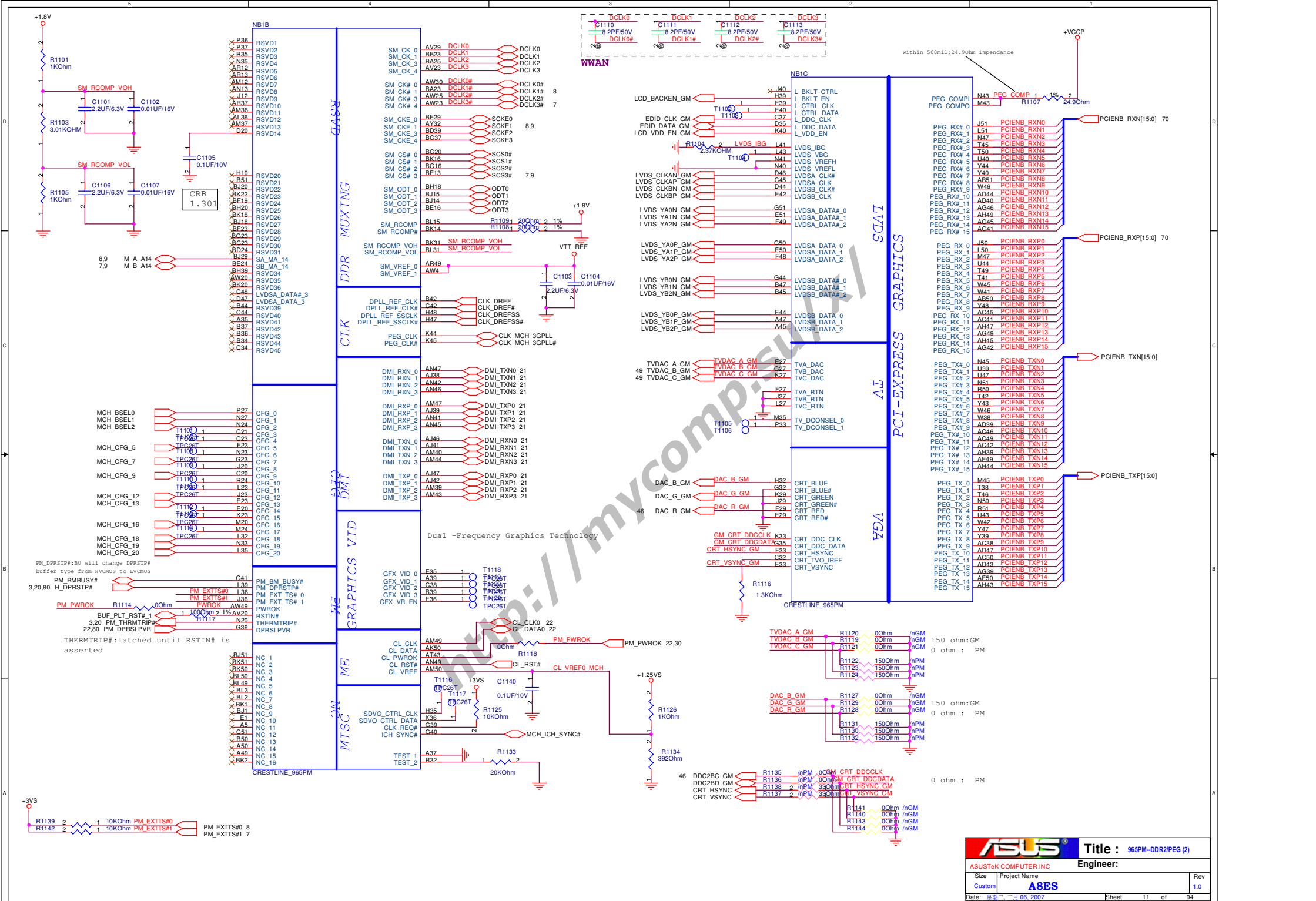
Engineer:

Size Project Name
Custom A8ES

Rev
1.0

Date: 星期二, 06, 2007

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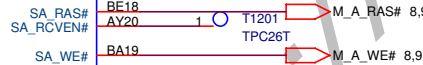
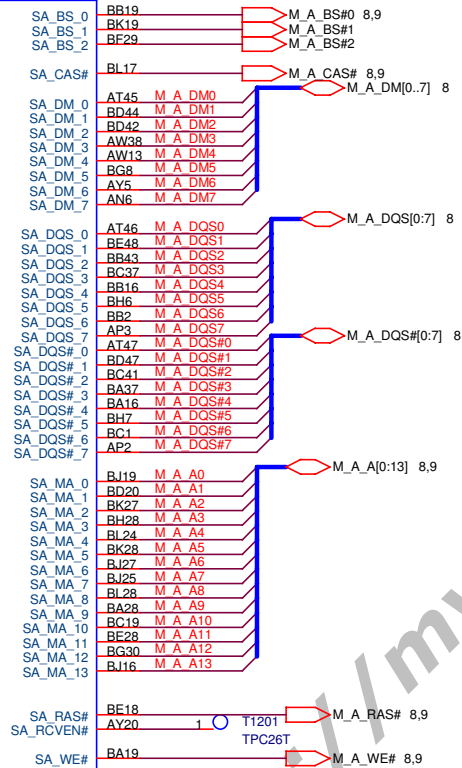


8 M_A_DQ[0:63]

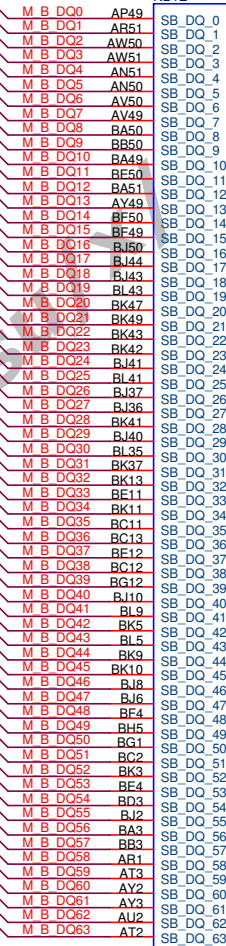


CRESTLINE_965PM

DDR SYSTEM MEMORY A

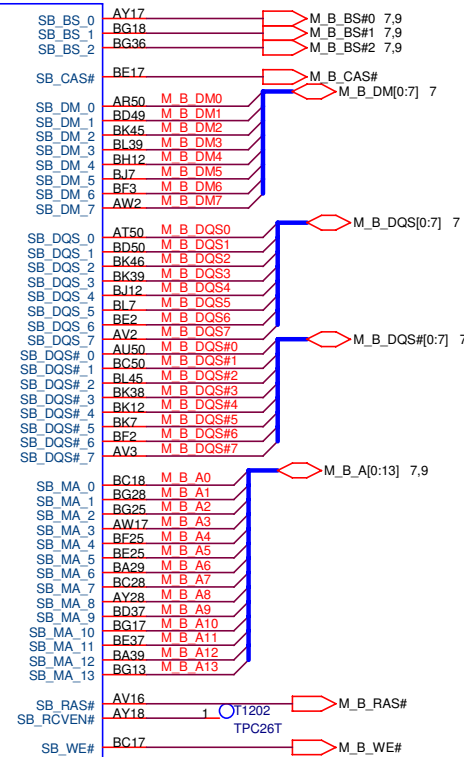


7 M_B_DQ[0:63]



CRESTLINE_965PM

DDR SYSTEM MEMORY B

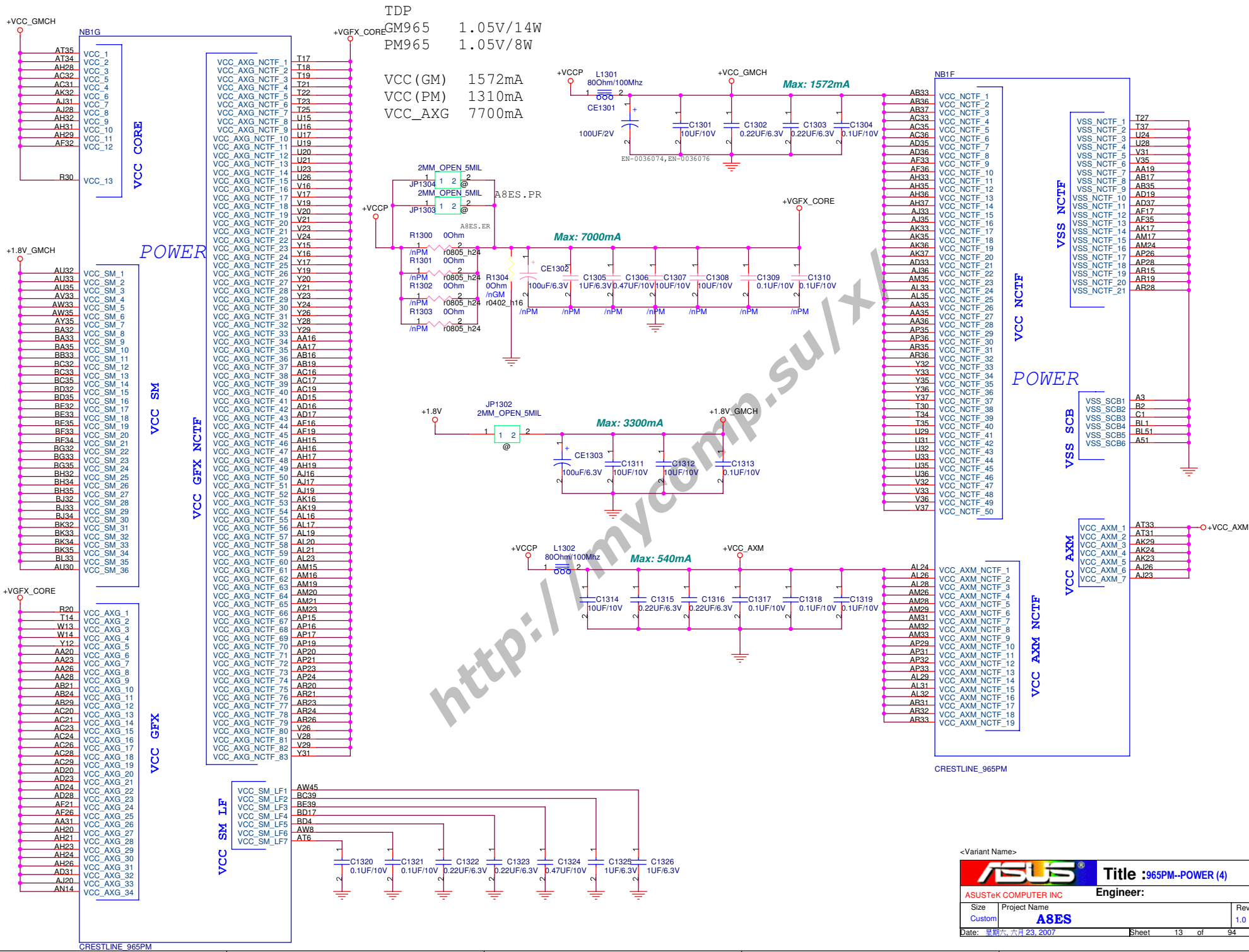


Title : 965PM--DDR2 bus (3)

ASUSTek COMPUTER INC

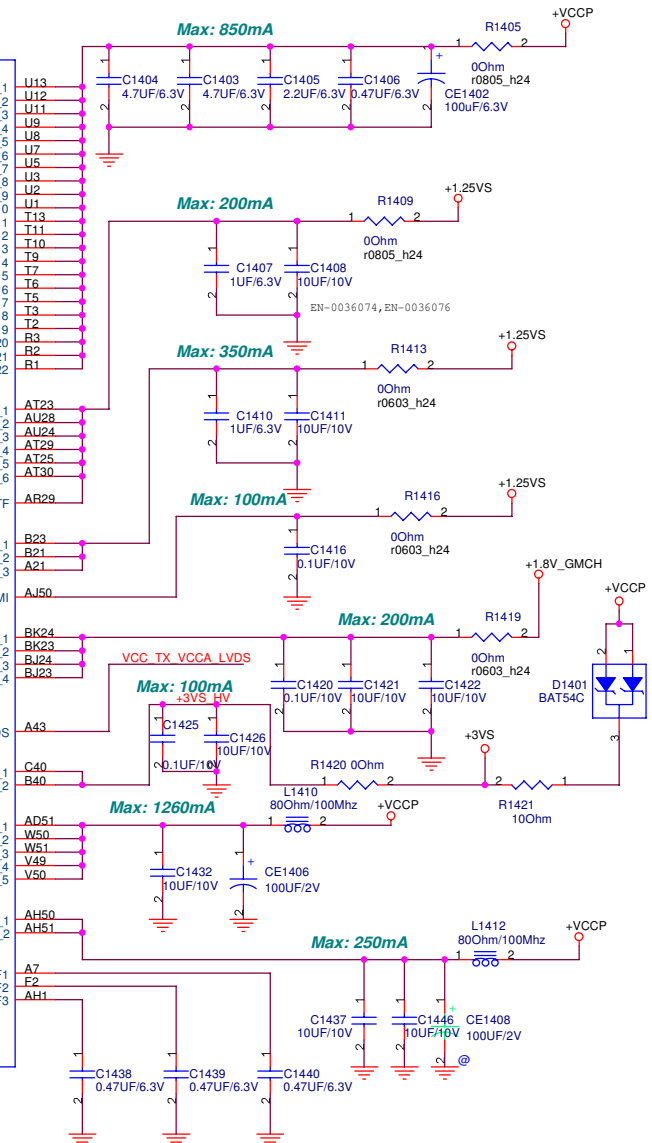
Engineer:

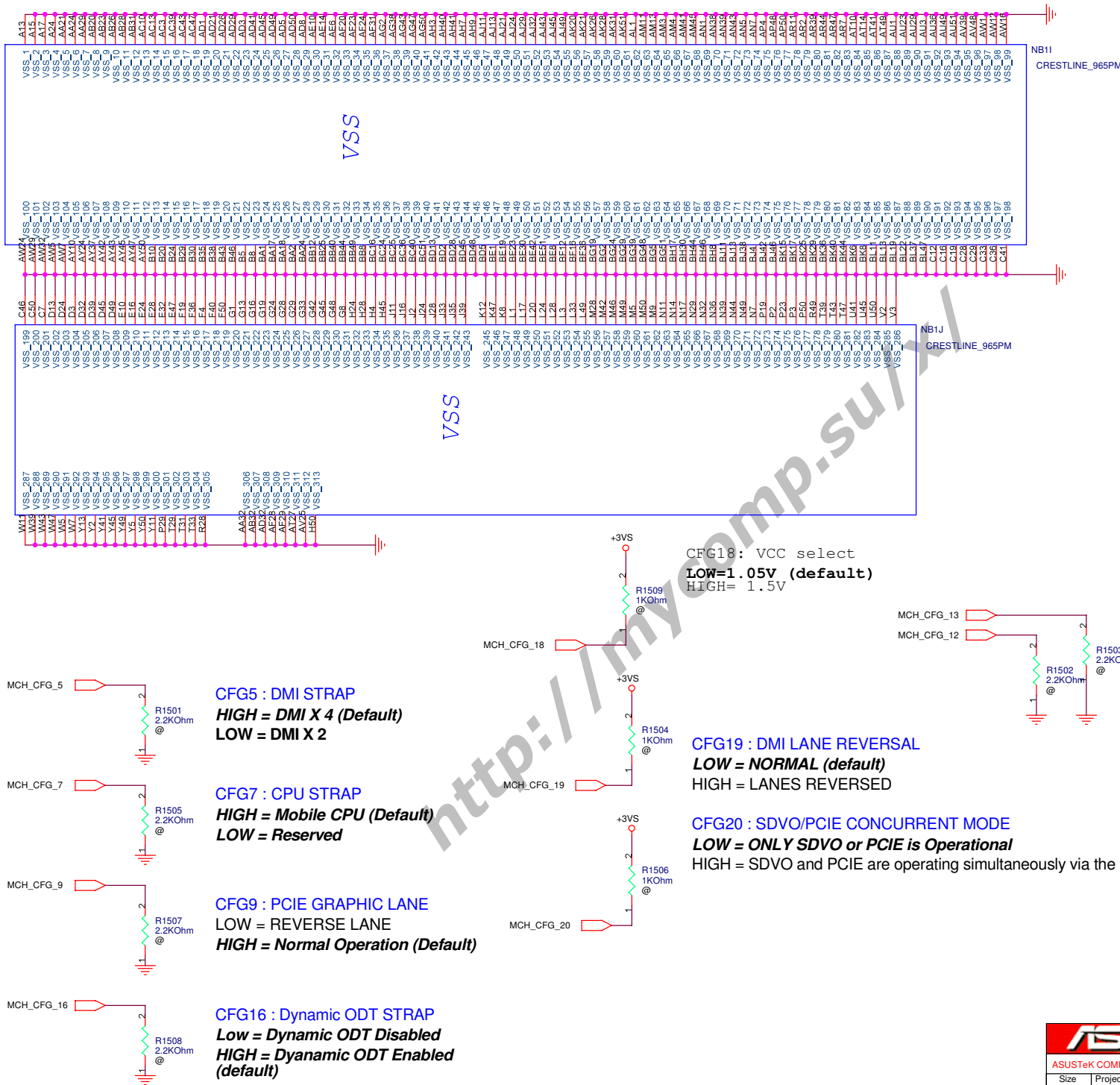
Size	Project Name	Rev
B	A8ES	1.0
Date: 星期 三月 06, 2007	Sheet 12 of 94	



<Variant Name>

		Title : 965PM--POWER (4)	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	1.0	
Date:	星期六, 六月 23, 2007	Sheet	13 of 94





		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: 星期三, 十月 11, 2006		Sheet 16 of 94	

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

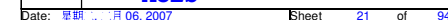
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: 星期三, 十月 11, 2006		Sheet 17 of 94	

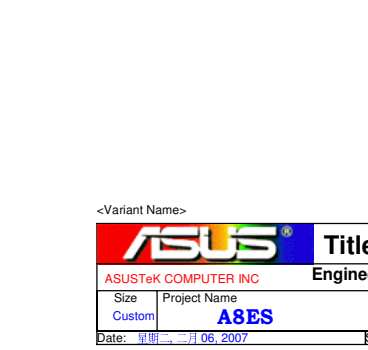
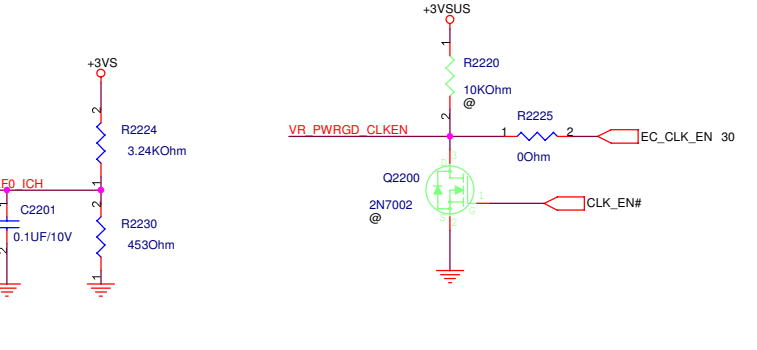
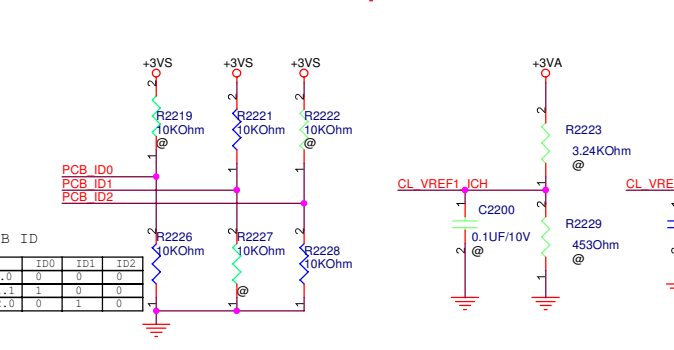
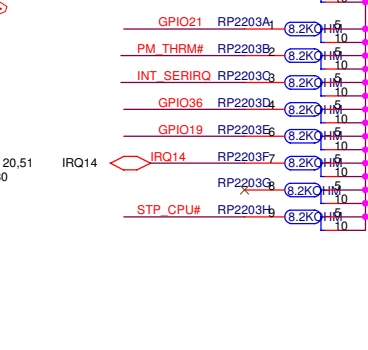
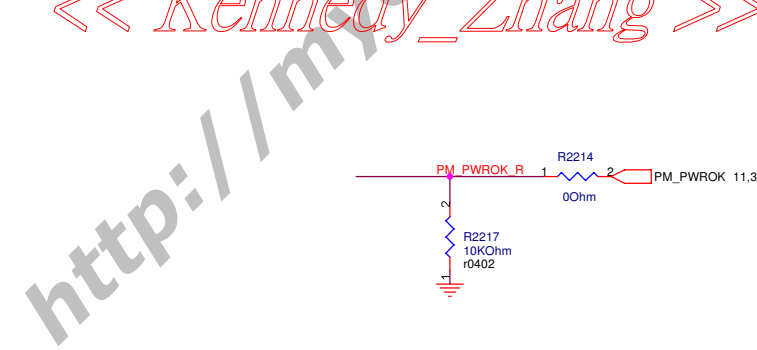
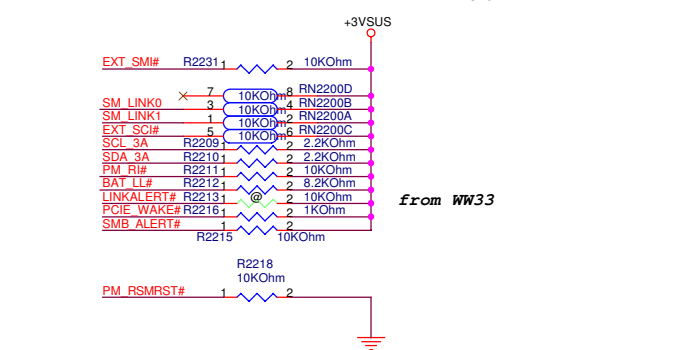
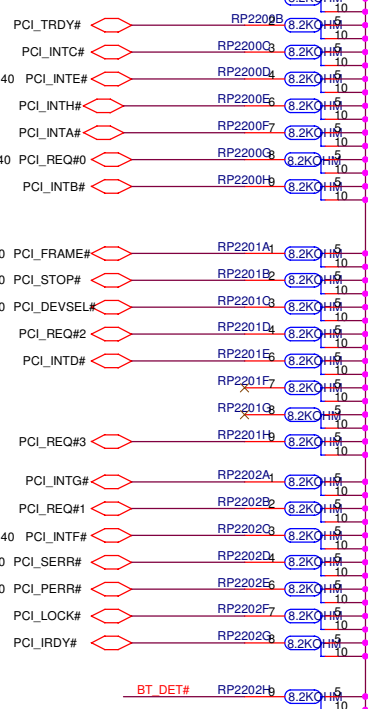
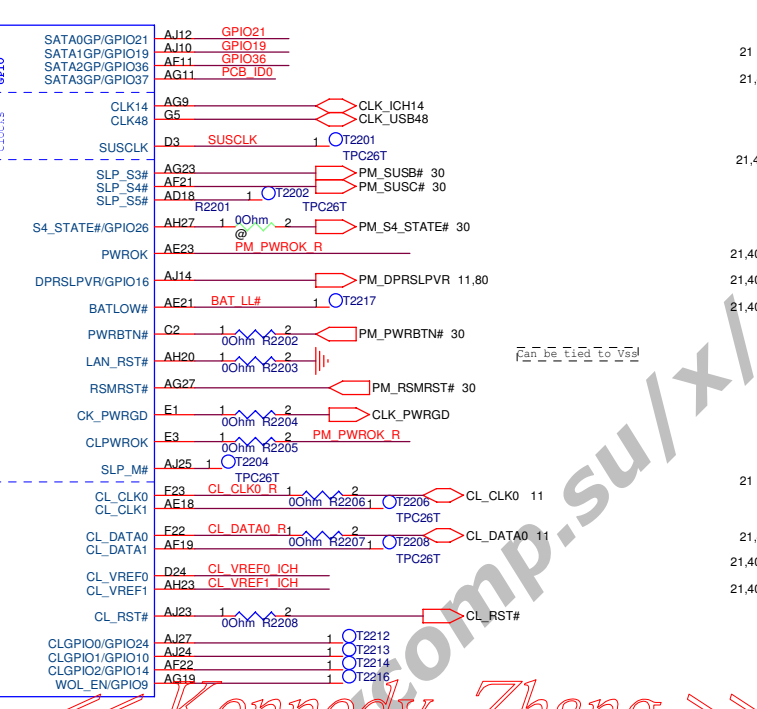
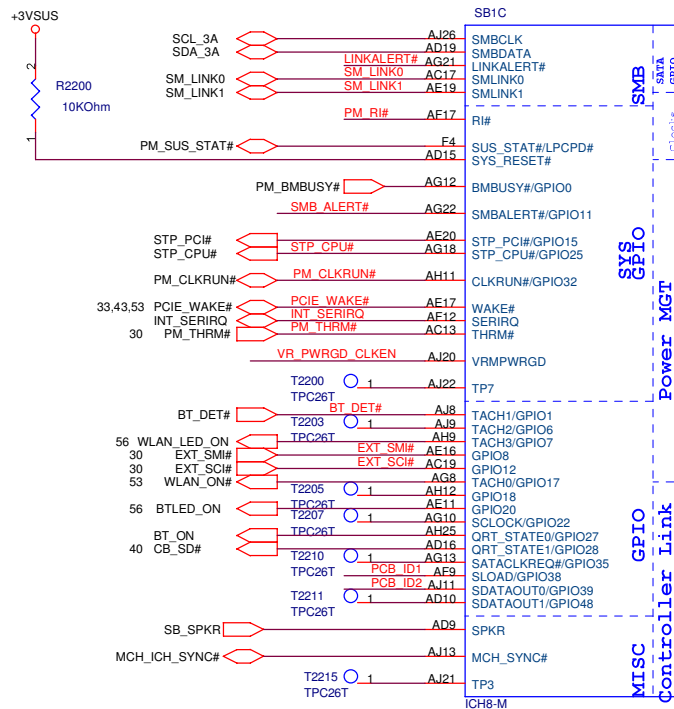
<http://mycomp.su/xl>

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: 星期三, 十月 11, 2006		Sheet	18 of 94

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
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PCB ID	ID0	ID1	ID2
1.0	0	0	0
1.1	1	0	0
2.0	0	1	0

PCB ID	ID0	ID1	ID2
1.0	0	0	0
1.1	1	0	0
2.0	0	1	0

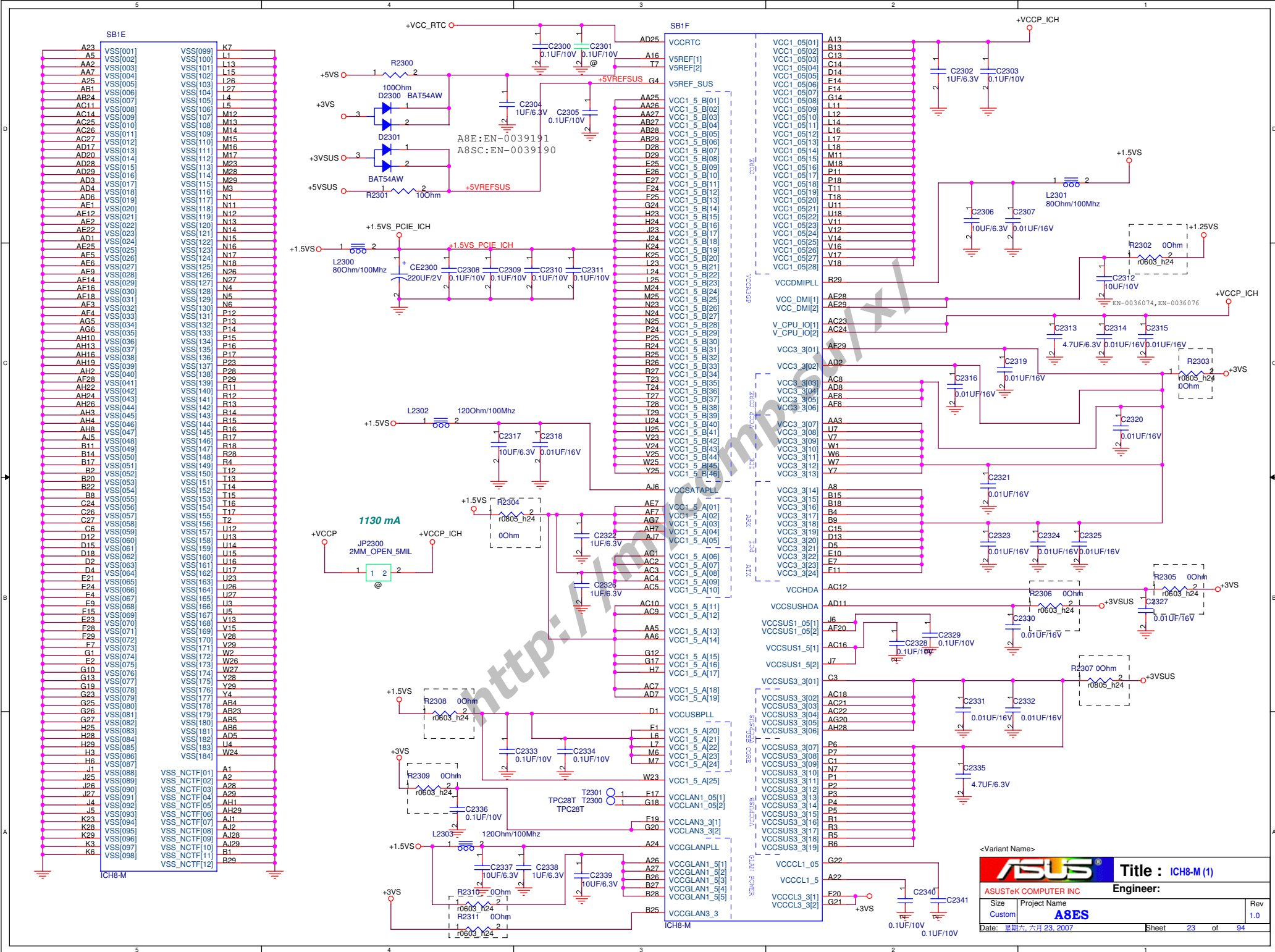
PCB ID	ID0	ID1	ID2
1.0	0	0	0
1.1	1	0	0
2.0	0	1	0

http://mycomp.su/x/

<< Kennedy_Zhang >>

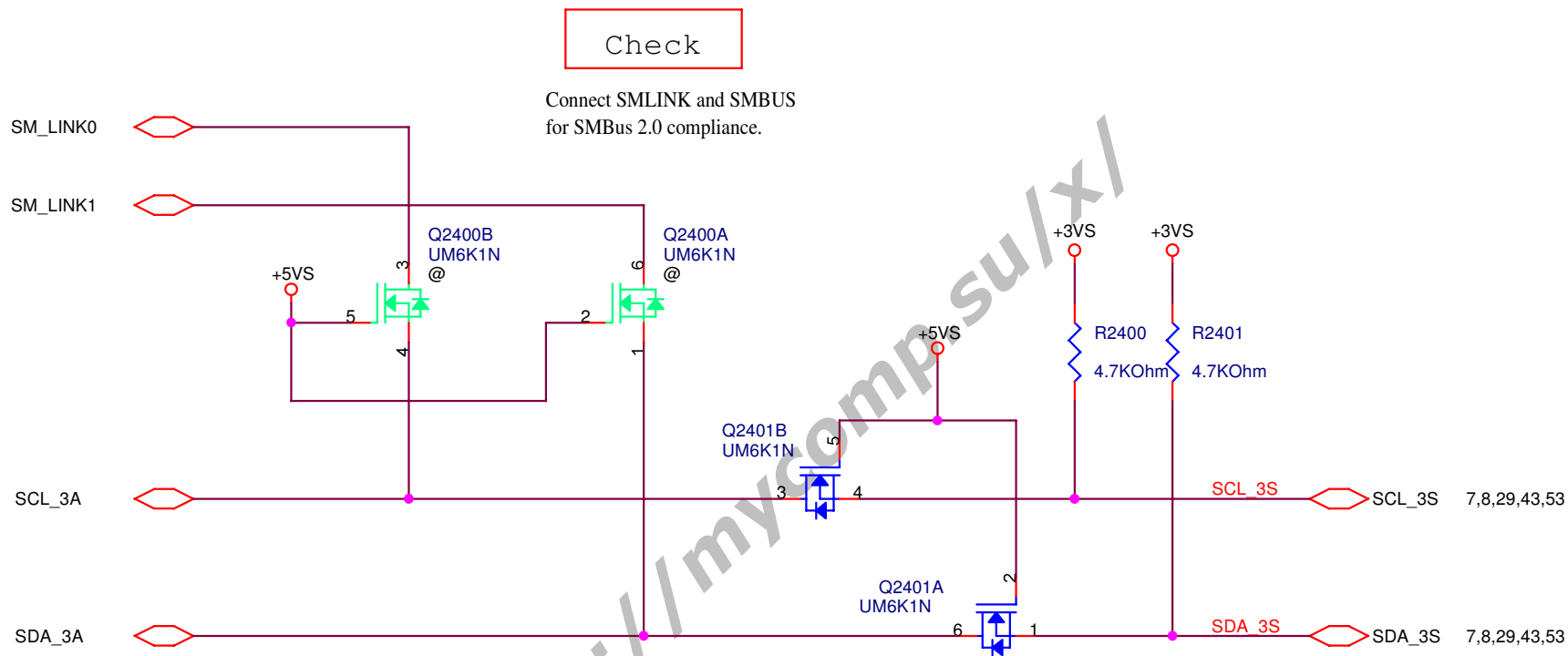
<Variant Name>

ASUS		Title : ICH8-M (3)	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	1.0	
Date: 星期三, 3月06, 2007	Sheet	22	of 94



ICH8-M

ICH8-M



<Variant Name>

		Title : BLOCK DIAGRAM	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 1.0
Date: 星期二, 二月 06, 2007		Sheet 24	of 94

ICH8-M GPIO Assignment

Name	H/W Pin Definition	Type	Tolerance	Power Wel	Default	Mux	Native Name	Real Name	Note
GPIO0	PM_BMBUSY#	IO	3.3V	Core	GPI	Yes	BMBUSY	PM_BMBUSY#	
GPIO1	BT_DET#	IO	3.3V	Core	GPI	No			
GPIO2	PCI_INTE#	IOD	5V	Core	GPI	Yes	PIRQE#	PCI_INTE#	
GPIO3	PCI_INTF#	IOD	5V	Core	GPI	Yes	PIRQF#	PCI_INTF#	
GPIO4	PCI_INTG#	IOD	5V	Core	GPI	Yes	PIRQG#	PCI_INTG#	
GPIO5	PCI_INTH#	IOD	5V	Core	GPI	Yes	PIRQH#	PCI_INTH#	
GPIO6	BIOS_REC	IO	3.3V	Core	GPI	No			
GPIO7	WLAN_LED_ON	IO	3.3V	Core	GPI	No			
GPIO8	EXT_SM#	IO	3.3V	Resume	GPI	No			
GPIO9	LAN_WOL_EN	IO	3.3V	Resume	GPI	Yes	WOL_EN		
GPIO10	ME_ALERT#	IO	3.3V	Resume	GPI	Yes	CLGPIO1		
GPIO11		IO	3.3V	Resume	Native	Yes	SMBALERT#	pull high +3VSUS	
GPIO12	EXT_SCI#	IO	3.3V	Resume	GPI	No			
GPIO13	ODD_DET	IO	3.3V	Resume	Native	Yes	GLAN_DOCK#		removing from EC
GPIO14	NETDETECT	IO	3.3V	Resume	GPI	Yes	CLGPIO2		
GPIO15	STP_PCI#	IO	3.3V	Resume	Native	No	STP_PCI#	STP_PCI#	
GPIO16	PM DPRSLPVR	IO	3.3V	Core	Native	Yes	DPRSLPVR	PM DPRSLPVR	
GPIO17	WLAN_ON#	IO	3.3V	Core	GPI	No			
GPIO18		IO	3.3V	Core	GPO	No			
GPIO19		IO	3.3V	Core	GPI	Yes	SATA1GP		
GPIO20	BTLED_ON	IO	3.3V	Core	GPO	No			
GPIO21		IO	3.3V	Core	GPI	Yes	SATA0GP		
GPIO22		IO	3.3V	Core	GPI	Yes	SCLOCK		
GPIO23		IO	3.3V	Core	Native	Yes	LDRQ1#		
GPIO24	PS_CPPE#	IO	3.3V	Resume	GPO	Yes	CLGPIO0		removing from EC; note by Alan
GPIO25	STP_CPU#	IO	3.3V	Resume	Native	No	STP_CPU#	STP_CPU#	
GPIO26	PM_S4_STATE#	IO	3.3V	Resume	Native	Yes	S4_STATE#		
GPIO27	BT_ON#BT_ON	IO	3.3V	Resume	GPO	Yes	QRT_STATE0		
GPIO28	CB_SD#	IO	3.3V	Resume	GPO	Yes	QRT_STATE1		Cardbus_Shutdown#
GPIO29	OC5#	IO	3.3V	Resume	Native	Yes	OC5#		OC#
GPIO30	OC6#	IO	3.3V	Resume	Native	Yes	OC6#		OC#
GPIO31	OC7#	IO	3.3V	Resume	Native	Yes	OC7#		OC#
GPIO32	PM_CLKRUN#	IO	3.3V	Core	Native	No	CLKRUN#	PM_CLKRUN#	
GPIO33		IO	3.3V	Core	GPO	Yes	HDA_DOCK_EN#		
GPIO34		IO	3.3V	Core	GPO	Yes	HDA_DOCK_RST#		
GPIO35	SATACLKREQ#	IO	3.3V	Core	GPO	Yes	SATACLKREQ#		
GPIO36	EMAIL_LED#	IO	3.3V	Core	GPI	Yes	SATA2GP		
GPIO37	PCB_ID0	IO	3.3V	Core	GPI	Yes	SATA3GP		
GPIO38	PCB_ID1	IO	3.3V	Core	GPI	Yes	SLOAD		
GPIO39	PCB_ID2	IO	3.3V	Core	GPI	Yes	SDATAOUT0		
GPIO40	OC4#	IO	3.3V	Resume	Native	Yes	OC4#		OC#
GPIO41	OC3#	IO	3.3V	Resume	Native	Yes	OC3#		OC#
GPIO42	OC2#	IO	3.3V	Resume	Native	Yes	OC2#		OC#
GPIO43	OC1#	IO	3.3V	Resume	Native	Yes	OC1#		OC#
GPIO44		IO	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO45		IO	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO46		IO	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO47		IO	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO48		IO	3.3V	Core	GPI	Yes	SDATAOUT1		
GPIO49	H_PWRGD	IO	V_CPU_IO	V_CPU_IO	Native	Yes	CPUPWRGD	H_PWRGD	
GPIO50	PCI_REQ1#	IO	5.5V	Core	Native	Yes	REQ1#		
GPIO51	PCI_GNT1#	IO	3.3V	Core	Native	Yes	GNT1#		
GPIO52	PCI_REQ2#	IO	5.5V	Core	Native	Yes	REQ2#		
GPIO53	PCI_GNT2#	IO	3.3V	Core	Native	Yes	GNT2#		
GPIO54		IO	5.5V	Core	Native	Yes	REQ3#		reserved for GPIO
GPIO55		IO	3.3V	Core	Native	Yes	GNT3#		reserved for GPIO

Title : BLANK

Engineer:

ASUSTek COMPUTER INC

Project Name
A8ES

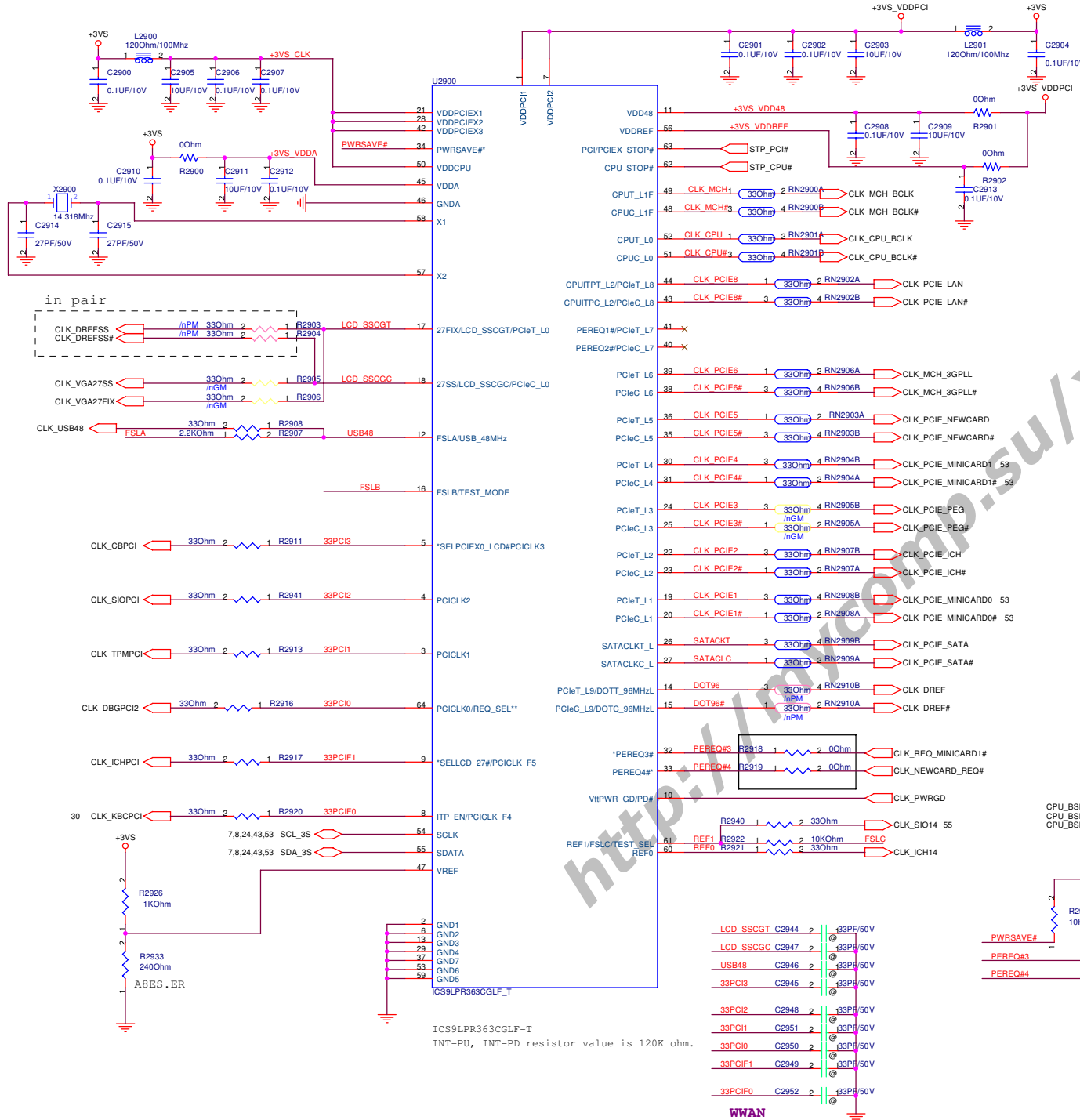
Rev
0

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		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
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		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
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		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
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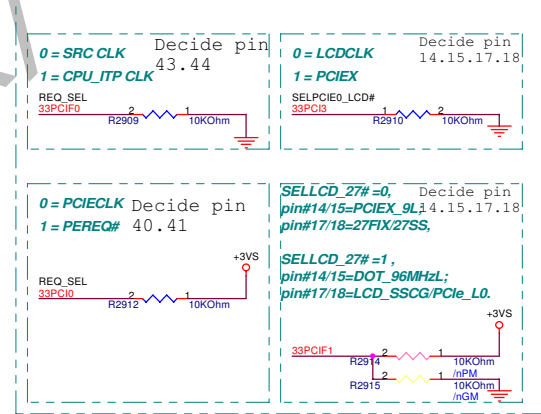
PEREQ#3: 0 = Enable control PCIeX4/2 through I2C
1 = Disable PCIeX4/2 Controlled
PEREQ#4: 0 = Enable control PCIeX7/5/3 through I2C
1 = Disable PCIeX7/5/3 Controlled

-->DISABLE PCIeX4
-->DISABLE PCIeX5

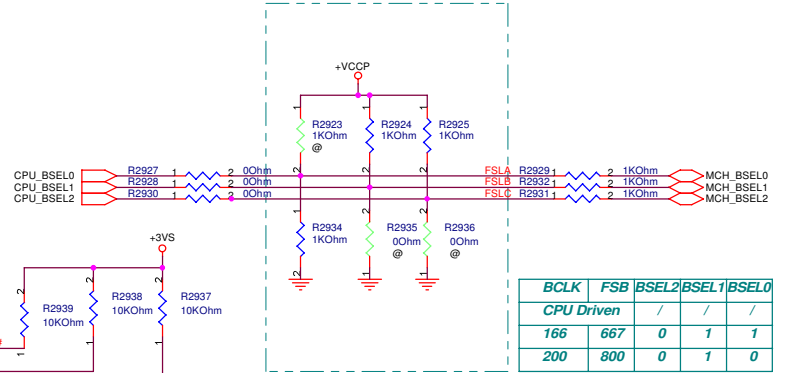
Latch Select Table

Pin5	Pin9	Pin14/15	Pin17/18
SELPCIE_X_LCD#/ PC13 = 0 (low)	SELLCD_27# = 0 SELLCD_27# = 1	PCIE9 DOT96	27FWSS LCD
SELPCIE_X_LCD#/ PC13 = 1 (high)	SELLCD_27# = 0 SELLCD_27# = 1	PCIE9 DOT96	PCIE_X PCIE_X

Latched Input Select



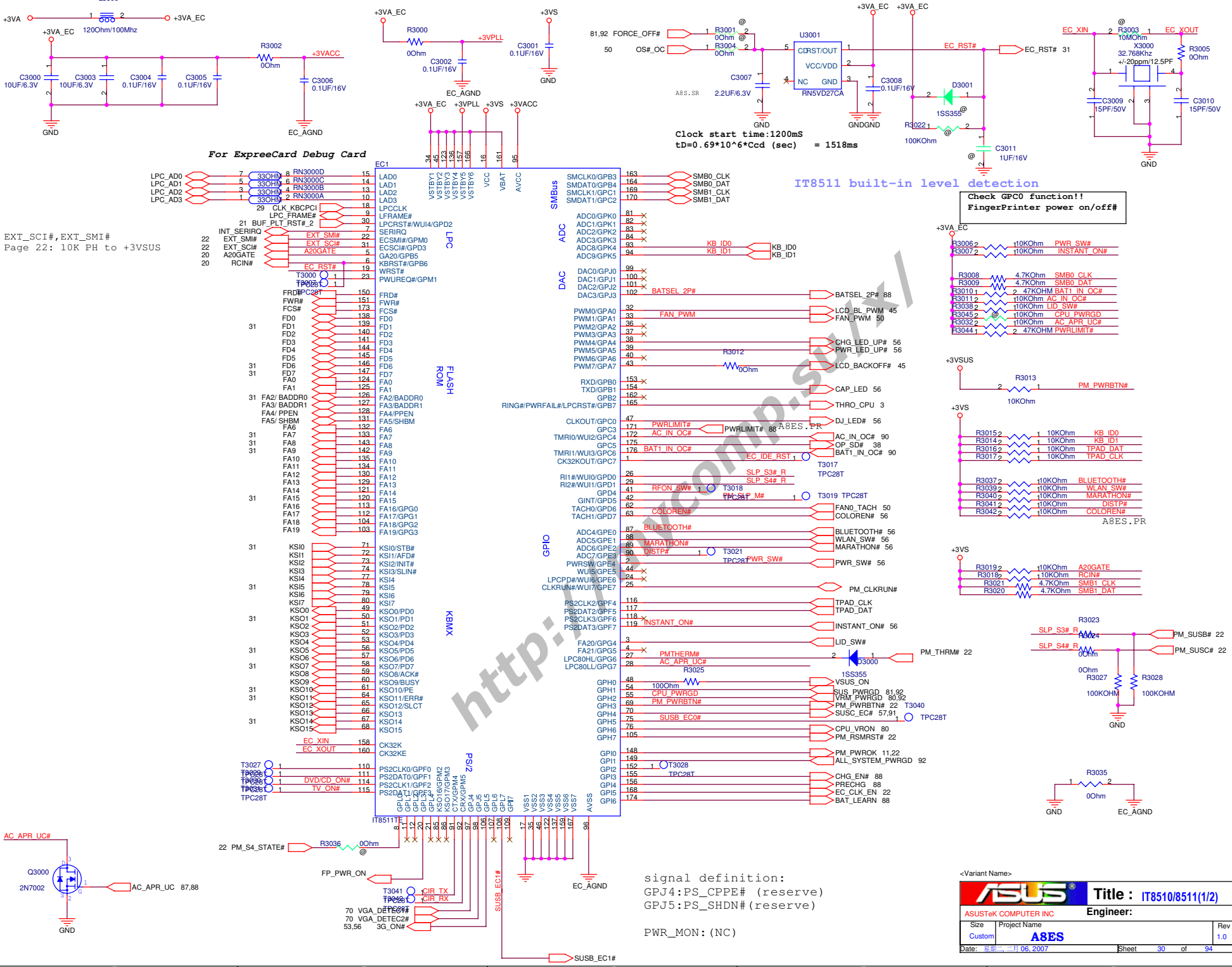
Reserved for R1.0 Debug



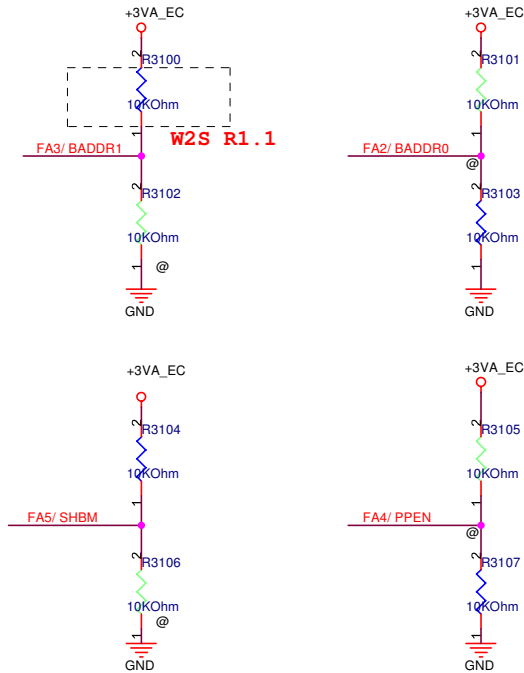
BCLK	FSB	BSEL2	BSEL1	BSEL0
CPU Driven	/	/	/	/
166	667	0	1	1
200	800	0	1	0

ICS9LPR363CGLF-T
INT-PU, INT-PD resistor value is 120K ohm.

- LCD_SSCGT C2944 2 33PF/50V
- LCD_SSCGC C2947 2 33PF/50V
- USB48 C2946 2 33PF/50V
- 33PC13 C2945 2 33PF/50V
- 33PC12 C2948 2 33PF/50V
- 33PC11 C2951 2 33PF/50V
- 33PC10 C2950 2 33PF/50V
- 33PCIF1 C2949 2 33PF/50V
- 33PCIF0 C2952 2 33PF/50V



10:Determined by EC

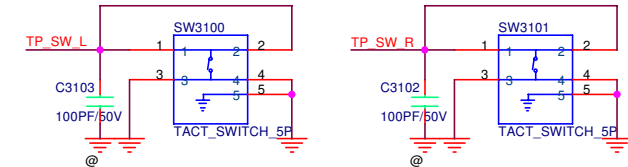
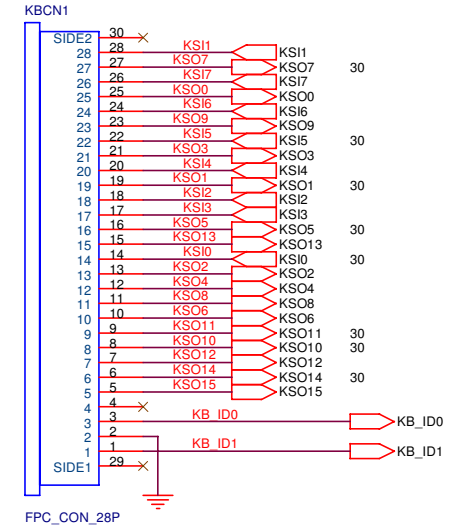


SHBM
No pull up:
disable shared memory with host BIOS
Ext 10K up:
enable shared memory with host BIOS

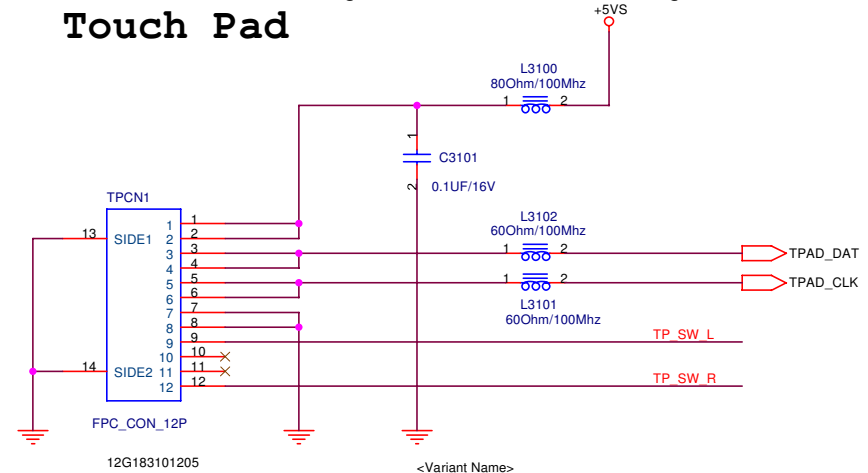
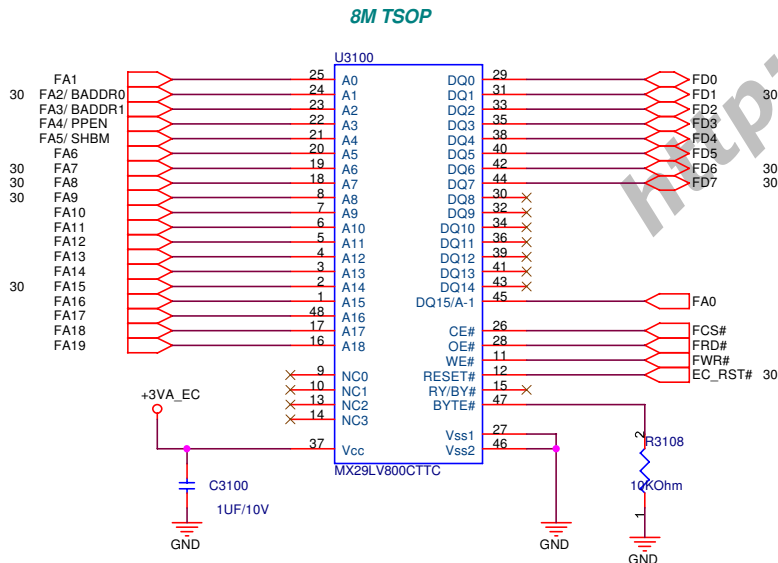
BADDR[1:0]
No pull up:
The register pair to access PNPCFG is 002Eh and 002Fh.
Ext 10K up on BADDR0:
The register pair to access PNPCFG is 004Eh and 004Fh.
Ext 10K up on BADDR1:
The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.

PPEN
No pull up:
Normal
Ext 10K up:
KBS interface pins are switched to parallel port interface for in-system programming.

KBDDT1	KBDDT0	Matrix
1	1	US
1	0	UK
0	1	JP



Touch Pad



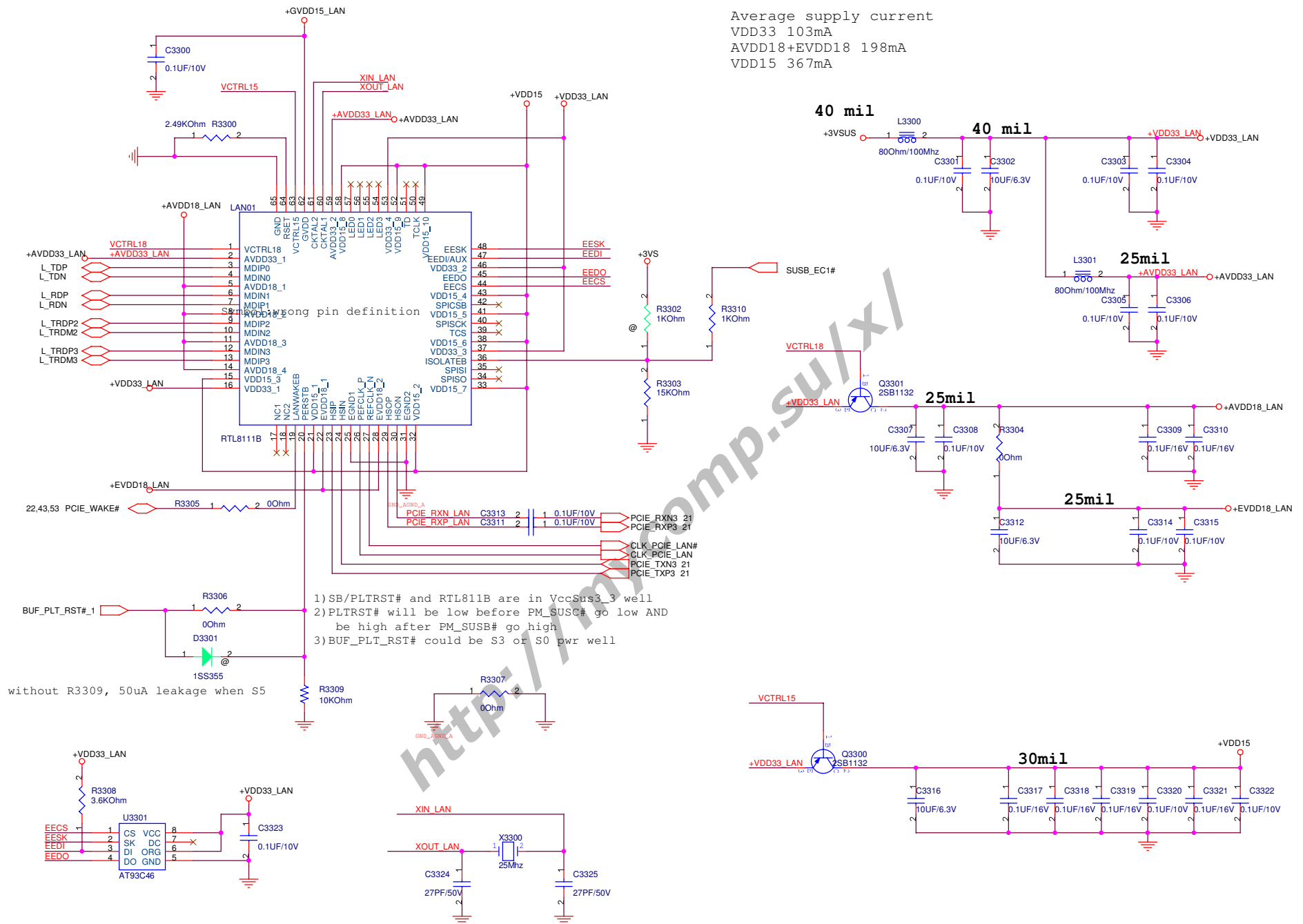
<Variant Name>

ASUS		Title : IT8510/8511(2/2)	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	1.0	
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	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
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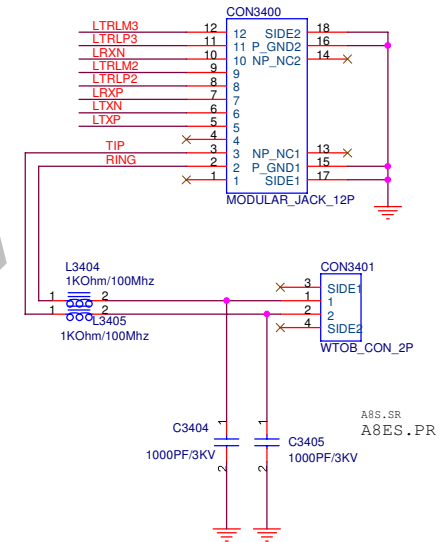
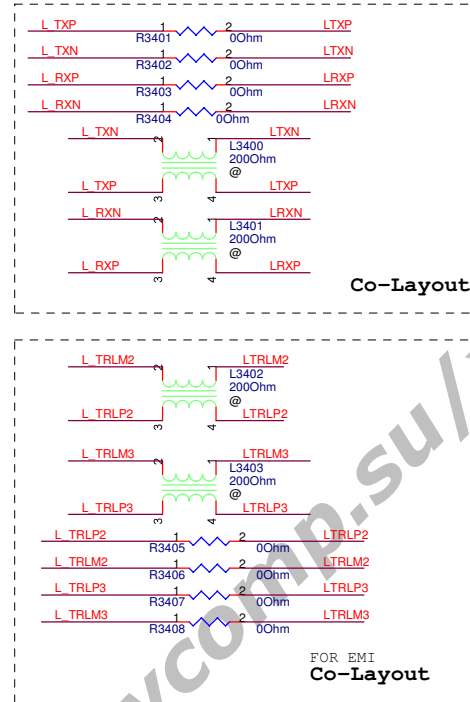
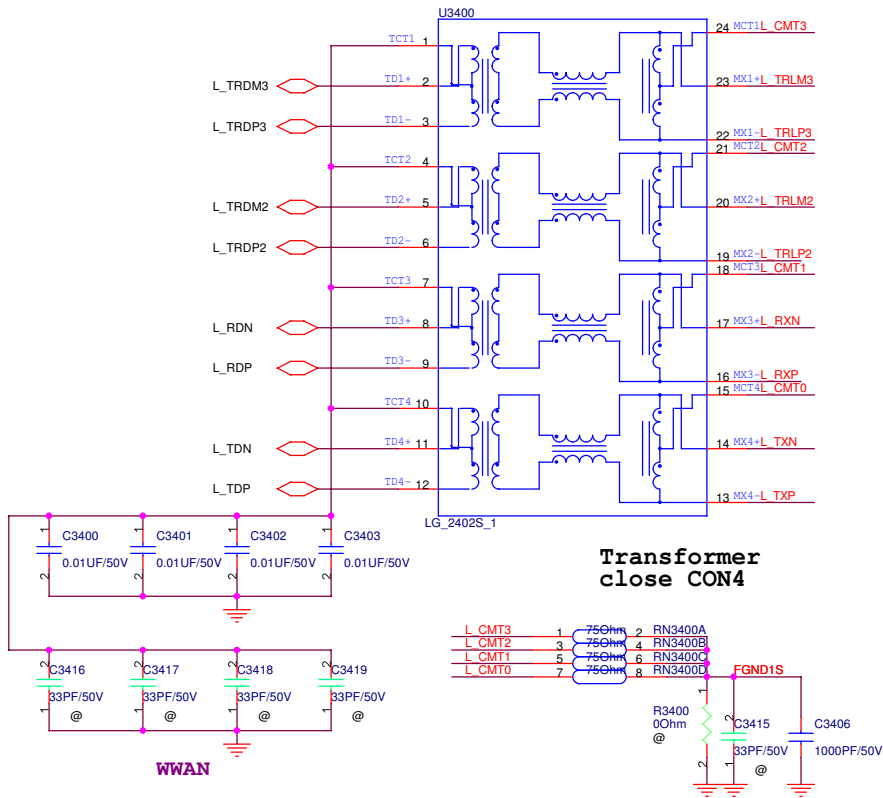
Average supply current
VDD33 103mA
AVDD18+EVDD18 198mA
VDD15 367mA



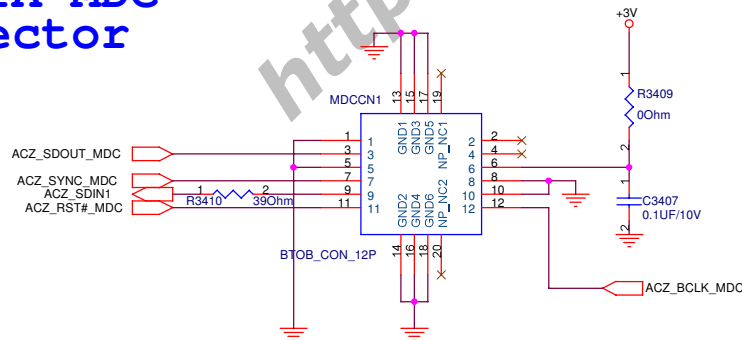
<Variant Name>

ASUS		Title : GigaLAN	
ASUSTeK COMPUTER INC		Engineer:	
Size Custom	Project Name A8ES		Rev 1.0
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2402S have issue after IR reflow,
alternative part:LG-2410S-1



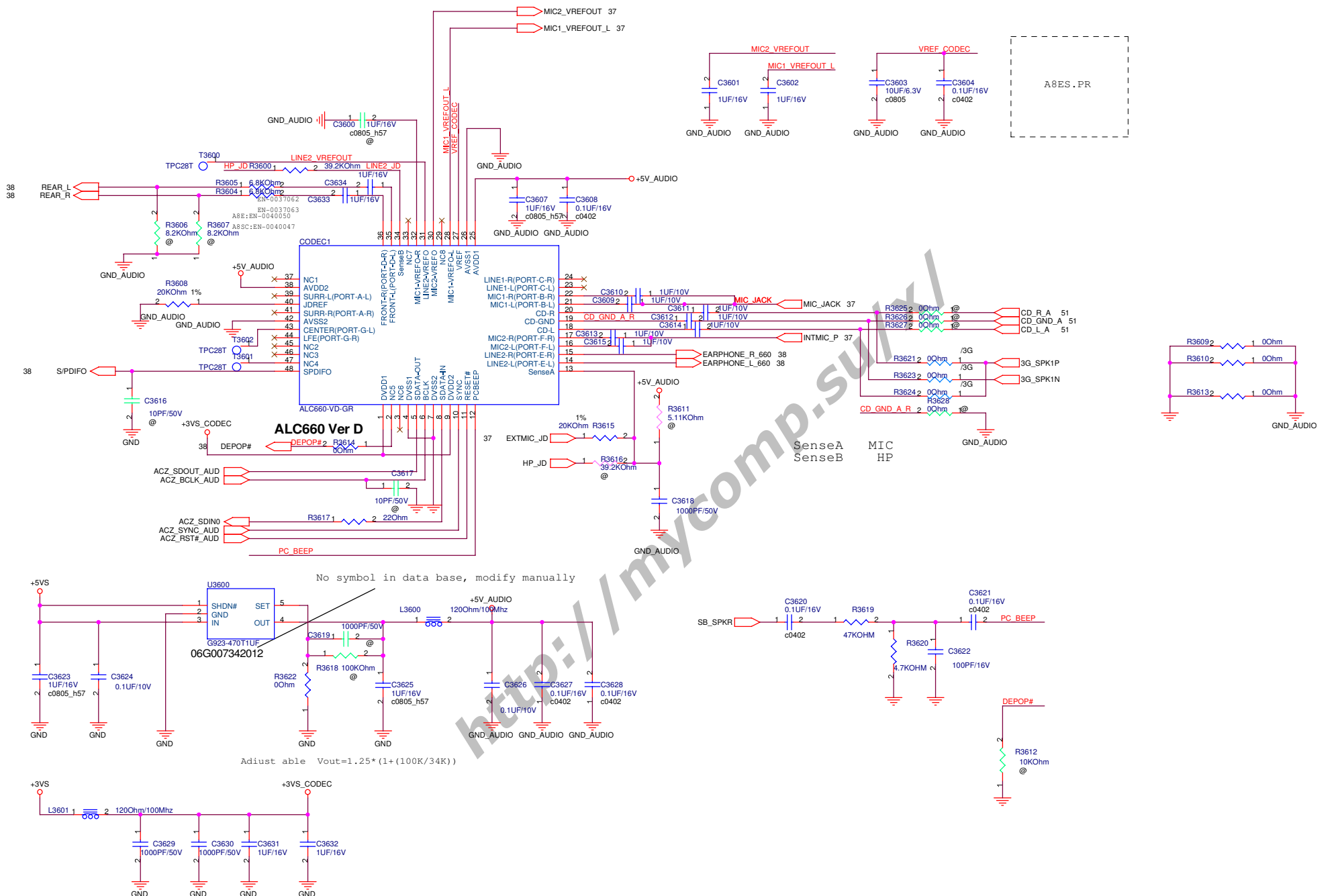
AZALIA MDC Connector

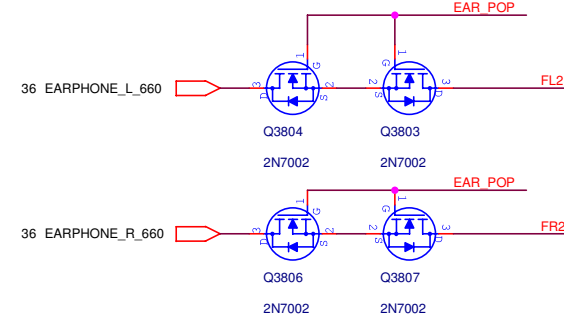
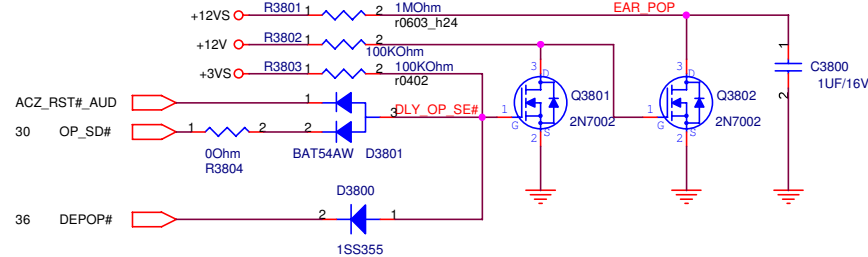
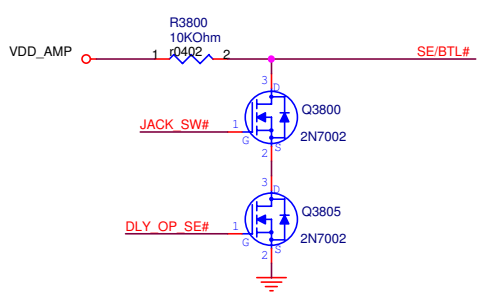


<Variant Name>

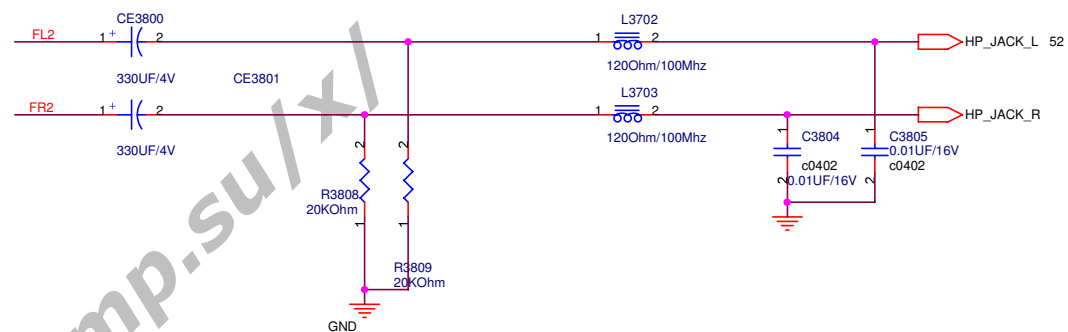
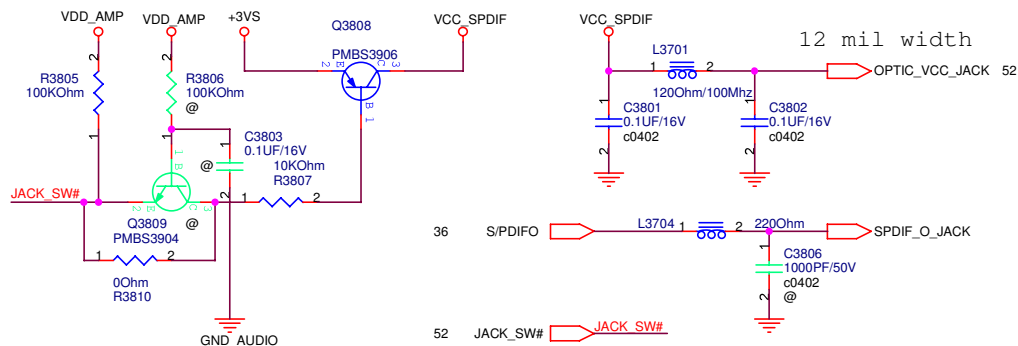
ASUS		Title : RJ11+45, MDC	
ASUSTeK COMPUTER INC		Engineer:	
Size Custom	Project Name A8ES		Rev 1.0
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		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
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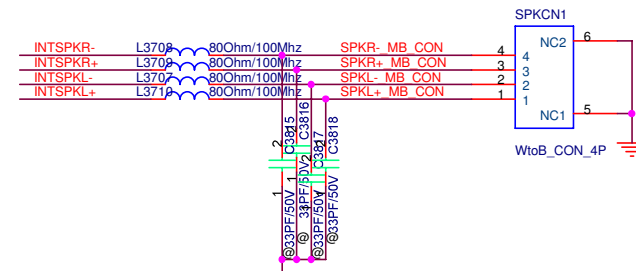
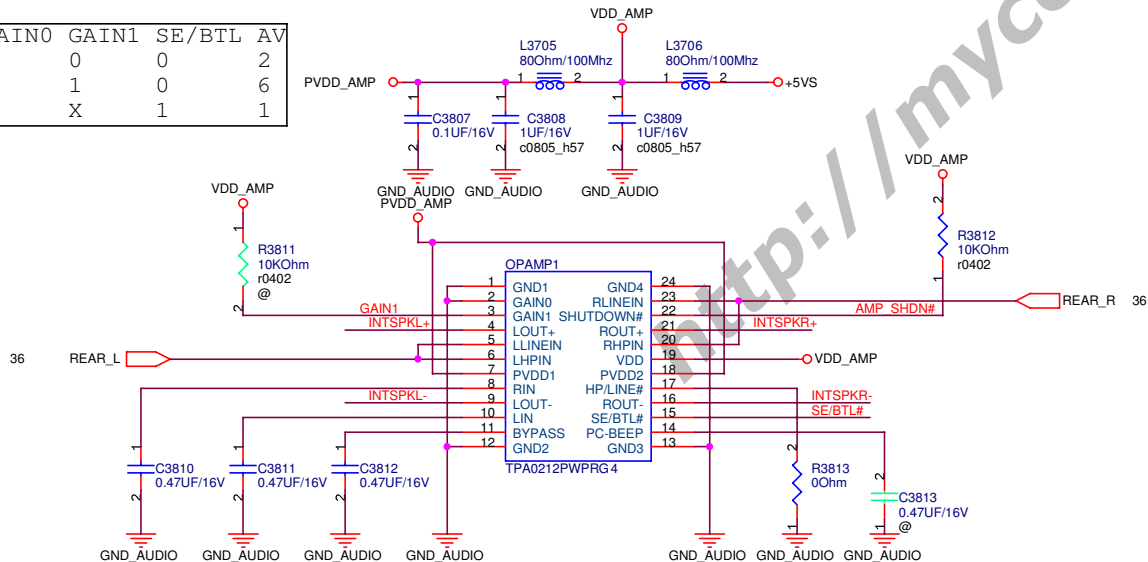




DEPOP



GAIN0	GAIN1	SE/BTL	AV
0	0	0	2
0	1	0	6
X	X	1	1



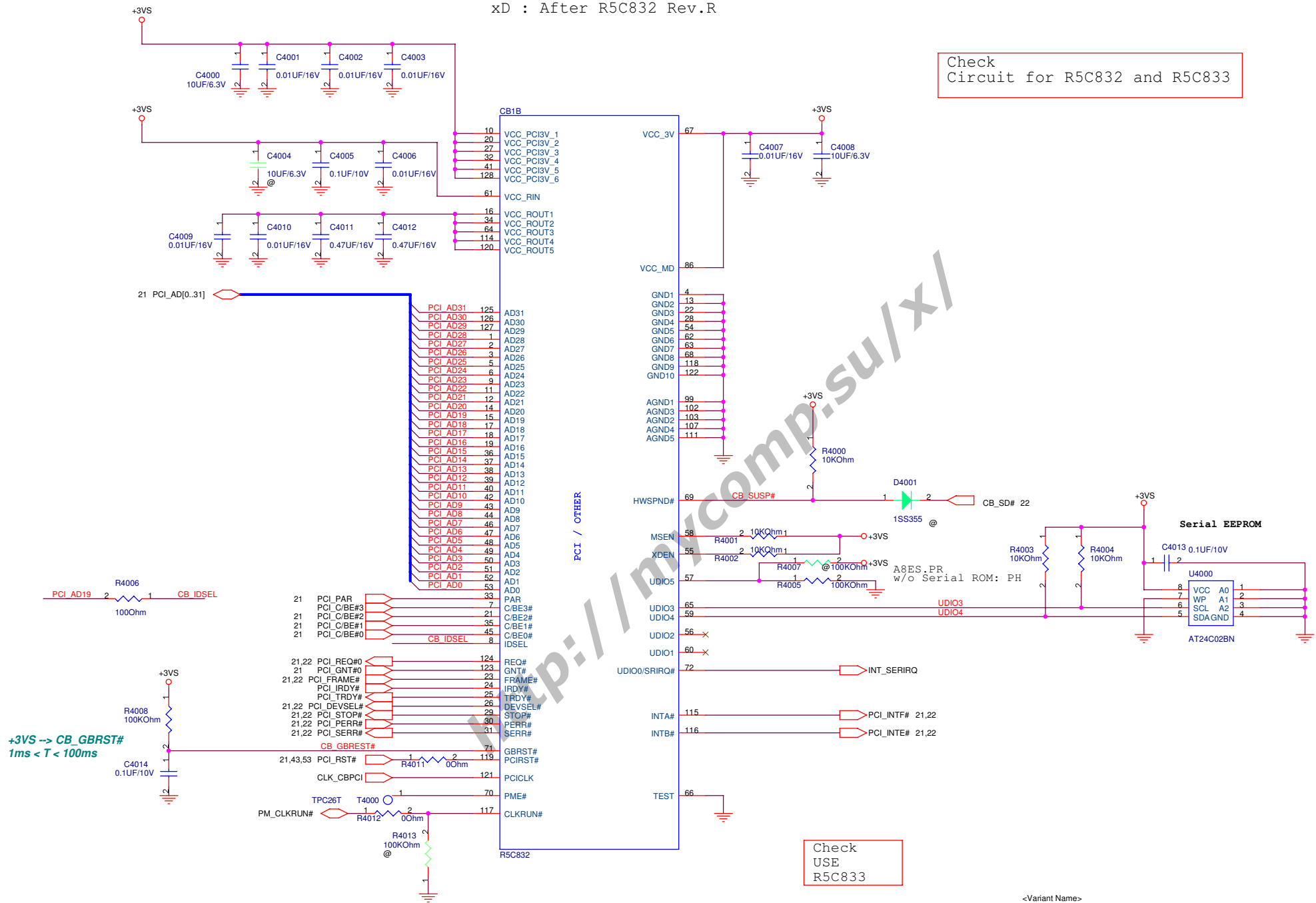
<Variant Name>

ASUS		Title : AUDIO-OP	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
B	A8ES	1.0	
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	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
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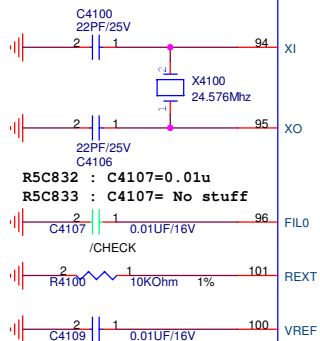
Check
Circuit for R5C832 and R5C833



<Variant Name>

ASUS		Title : RICOH R5C832/PCI B	
ASUSTek COMPUTER INC		Engineer:	
Size Custom	Project Name A8ES	Rev 1.0	
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as close as possible to R5C832

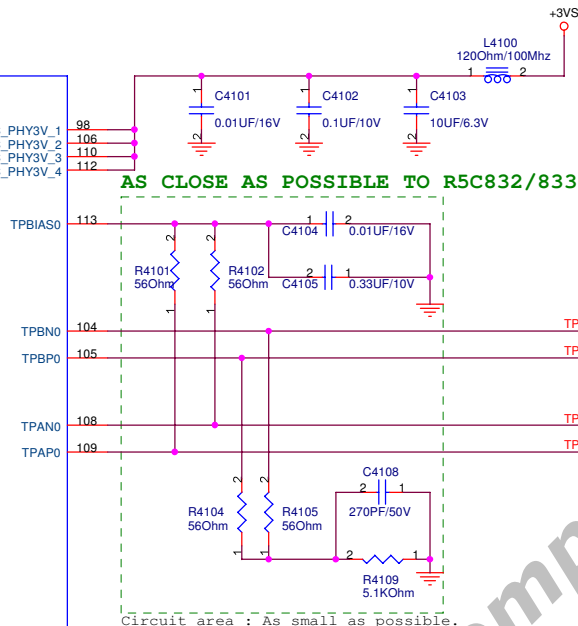


CB1A

IEEE1394/SD

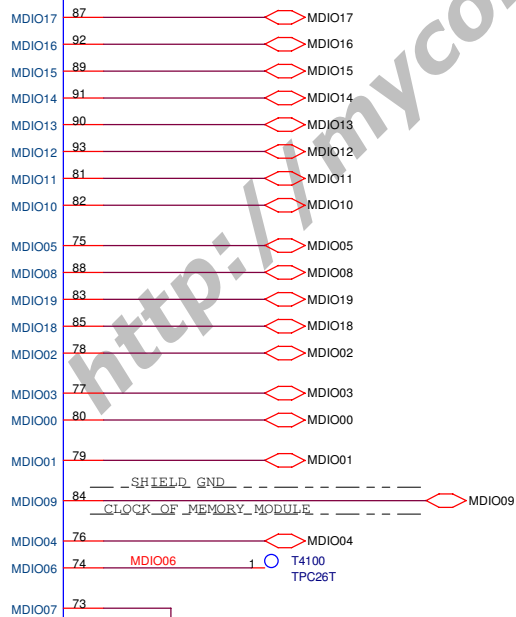
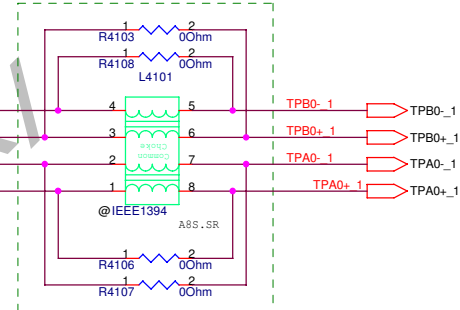
AVCC_PHY3V_1
 AVCC_PHY3V_2
 AVCC_PHY3V_3
 AVCC_PHY3V_4

AS CLOSE AS POSSIBLE TO R5C832/833



Circuit area : As small as possible.

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.

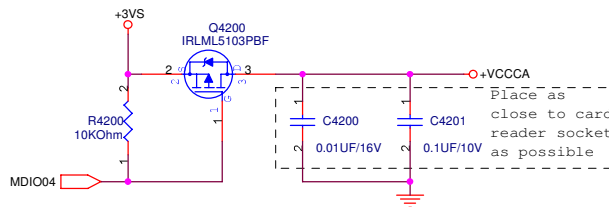


MDIO02--> xDCE#
 MDIO05--> SD Power Control 1 / xDWP
 MDIO06--> xD/MS/SD LED Control
 MDIO14--> xD Data
 MDIO15--> xD Data
 MDIO16--> xD Data
 MDIO17--> xD Data
 MDIO18--> xD CLE
 MDIO19--> xD ALE

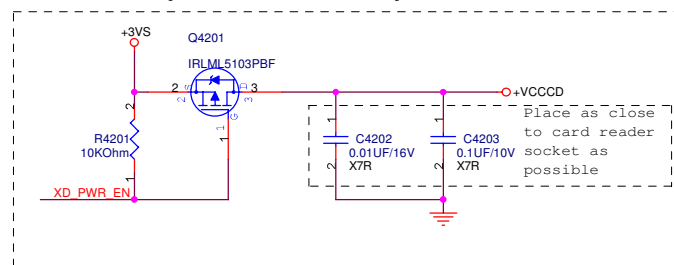
MDIO01--> MS Card Detect
 MDIO03--> SD Write Protect
 MDIO04--> SD Card Power0 Control/
 MS Power Control
 MDIO07--> SD External Clock/
 MS External Clock
 MDIO08--> SD Command/MS Bus State
 MDIO09--> SD Clock/MS Clock
 MDIO10--> SD Data 0/MS Data 0
 MDIO11--> SD Data 1/MS Data 1
 MDIO12--> SD Data 2/MS Data 2
 MDIO13--> SD Data 3/MS Data 3

<Variant Name>

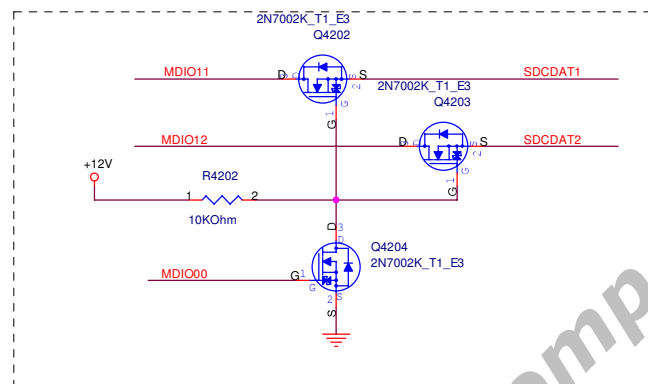
ASUS		Title : RICOH R5C832/PCI A	
ASUSTek COMPUTER INC		Engineer:	
Size Custom	Project Name A8ES	Rev 1.0	
Date: 早期 三月 06, 2007		Sheet 41 of 94	



To correct the problem when MS Duo adaptor is in use.



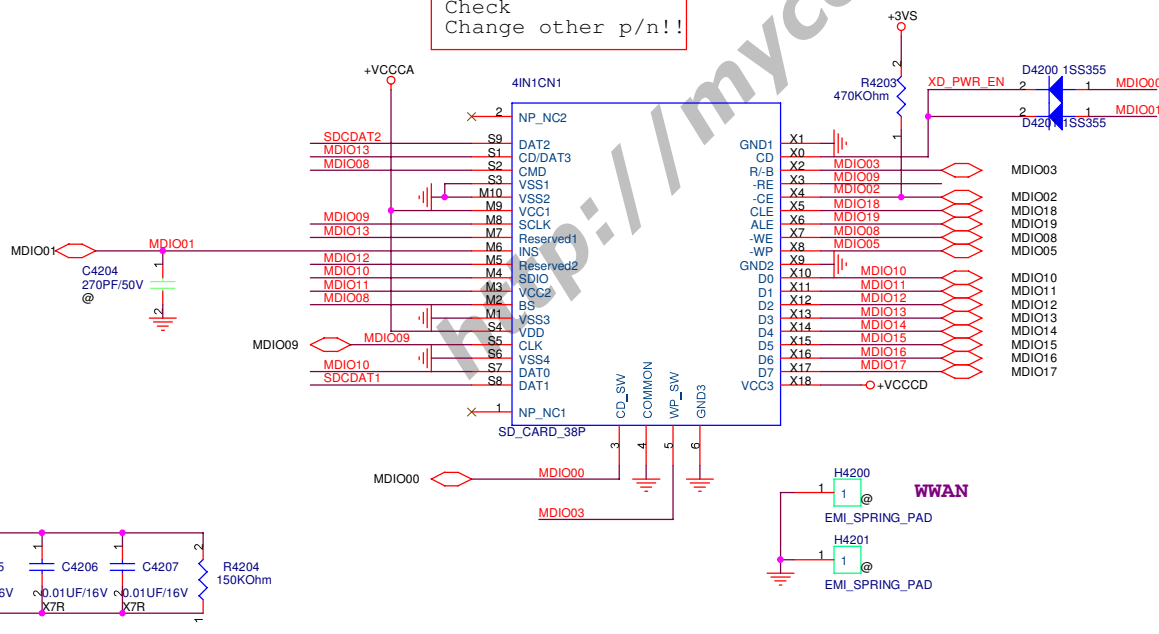
Solve MS Duo Adaptor short issue.



A8ES.PR
Change to 07G005000214, 2KV ESD

MDIO00-->	SD Card Detect
MDIO01-->	MS Card Detect
MDIO03-->	SD Write Protect
MDIO04-->	SD Card Power0 Control/ MS Power Control
MDIO08-->	SD Command/MS Bus State
MDIO09-->	SD Clock/MS Clock
MDIO10-->	SD Data 0/MS Data 0
MDIO11-->	SD Data 1/MS Data 1
MDIO12-->	SD Data 2/MS Data 2
MDIO13-->	SD Data 3/MS Data 3

Check
Change other p/n!!

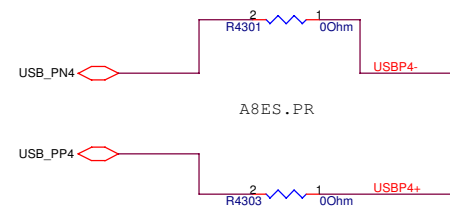
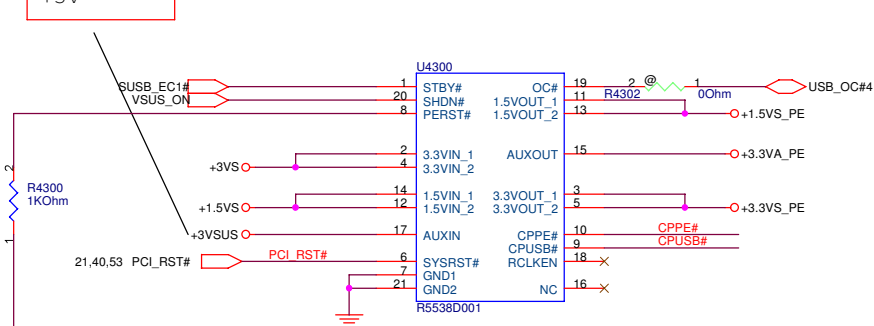


MDIO02-->	xDCE#
MDIO05-->	SD Power Control 1 / xDWP
MDIO06-->	xD/MS/SD LED Control
MDIO14-->	xD Data
MDIO15-->	xD Data
MDIO16-->	xD Data
MDIO17-->	xD Data
MDIO18-->	xD CLE
MDIO19-->	xD ALE

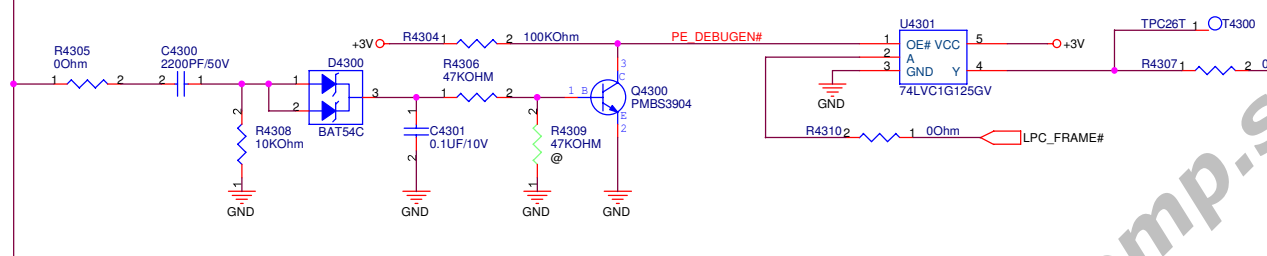
<Variant Name>

ASUS		Title : CardReader	
ASUSTeK COMPUTER INC		Engineer:	
Size Custom	Project Name A8ES	Rev 1.0	
Date: 2007.06.06	Sheet 42 of 94		

Check
+3V

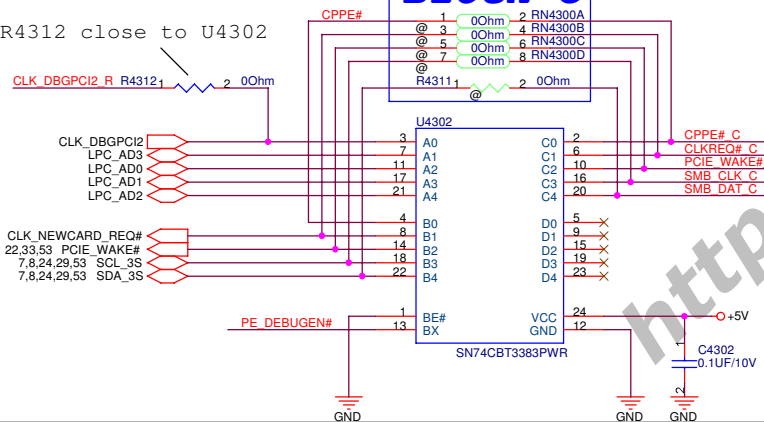


Block A

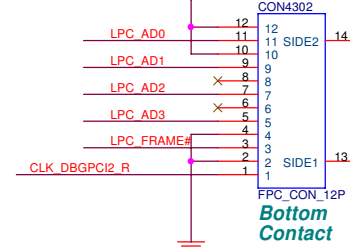
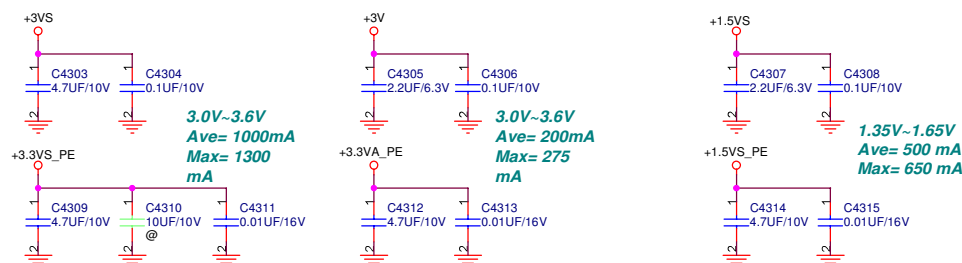
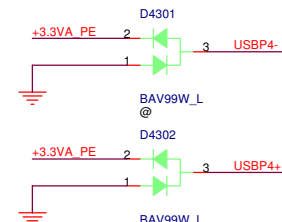
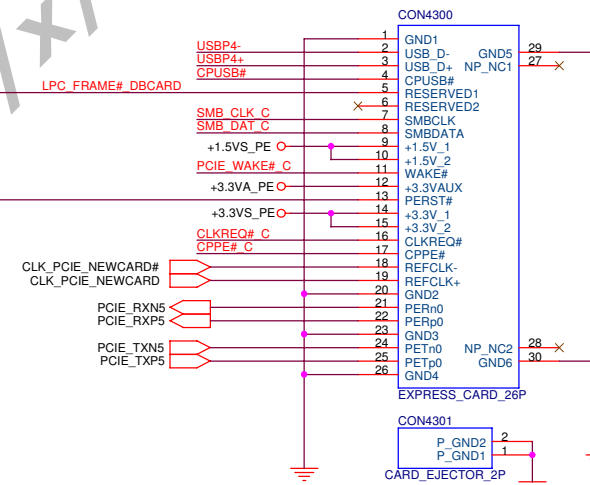


Block C

Put R4312 close to U4302



If don't support NewCard Debug Card, Pls do
(a) DNI all components of block A
(b) Mount Block C (RN5401, R6975)

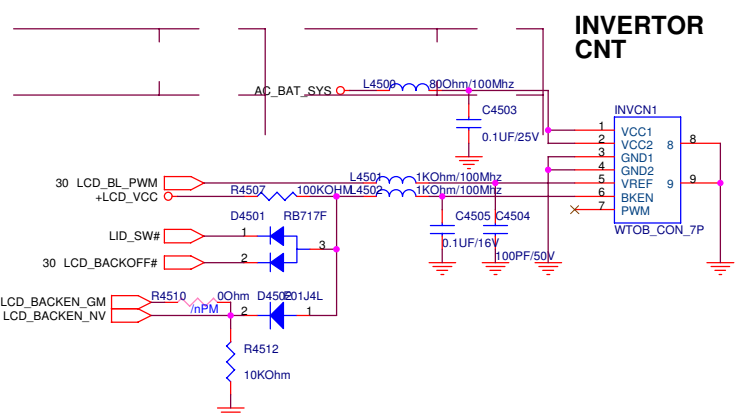
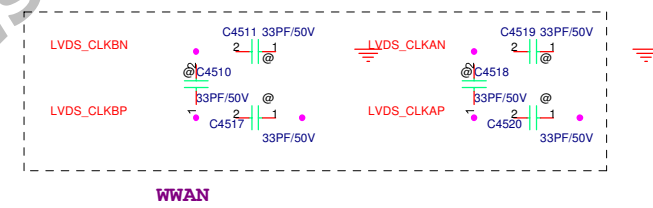
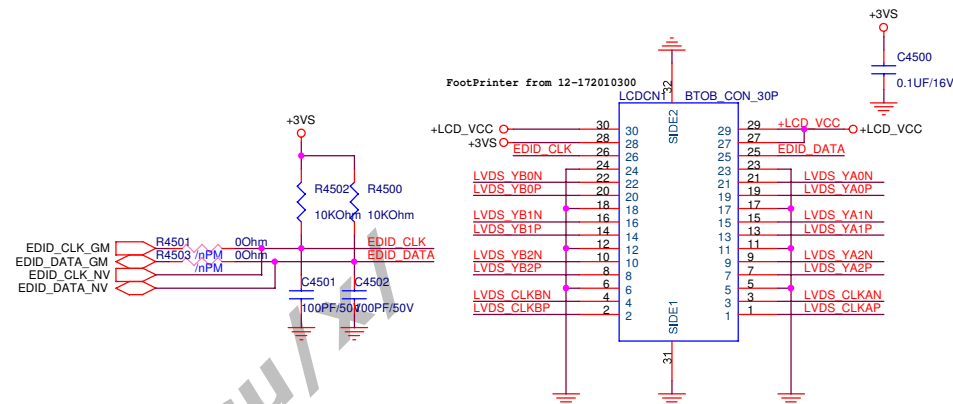
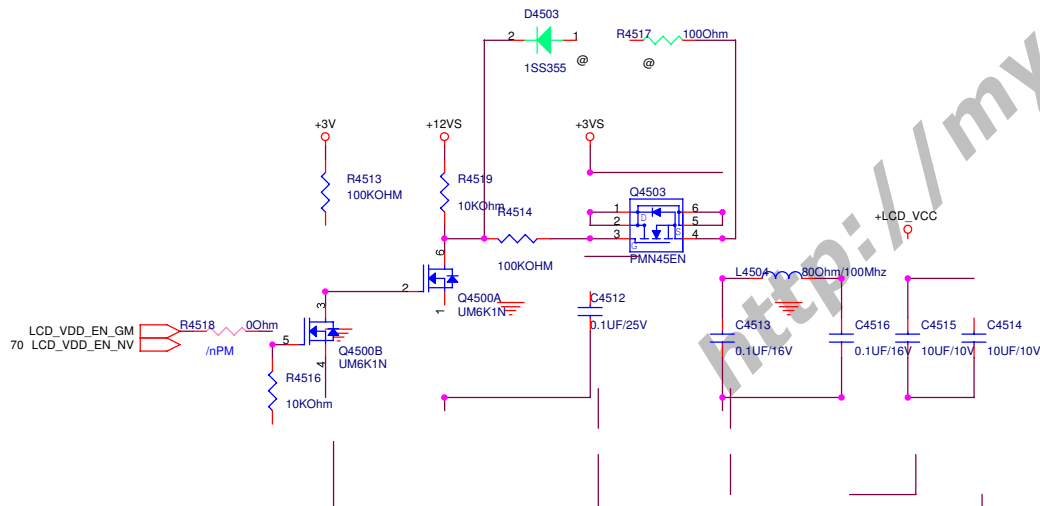
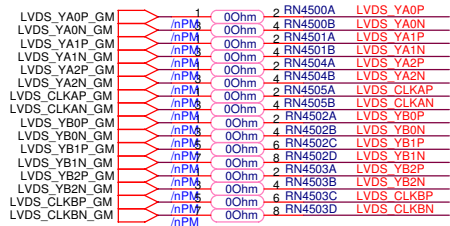
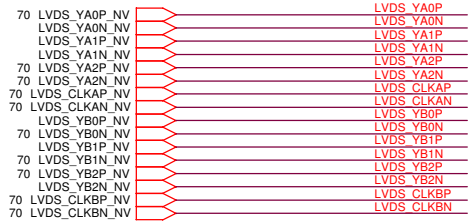


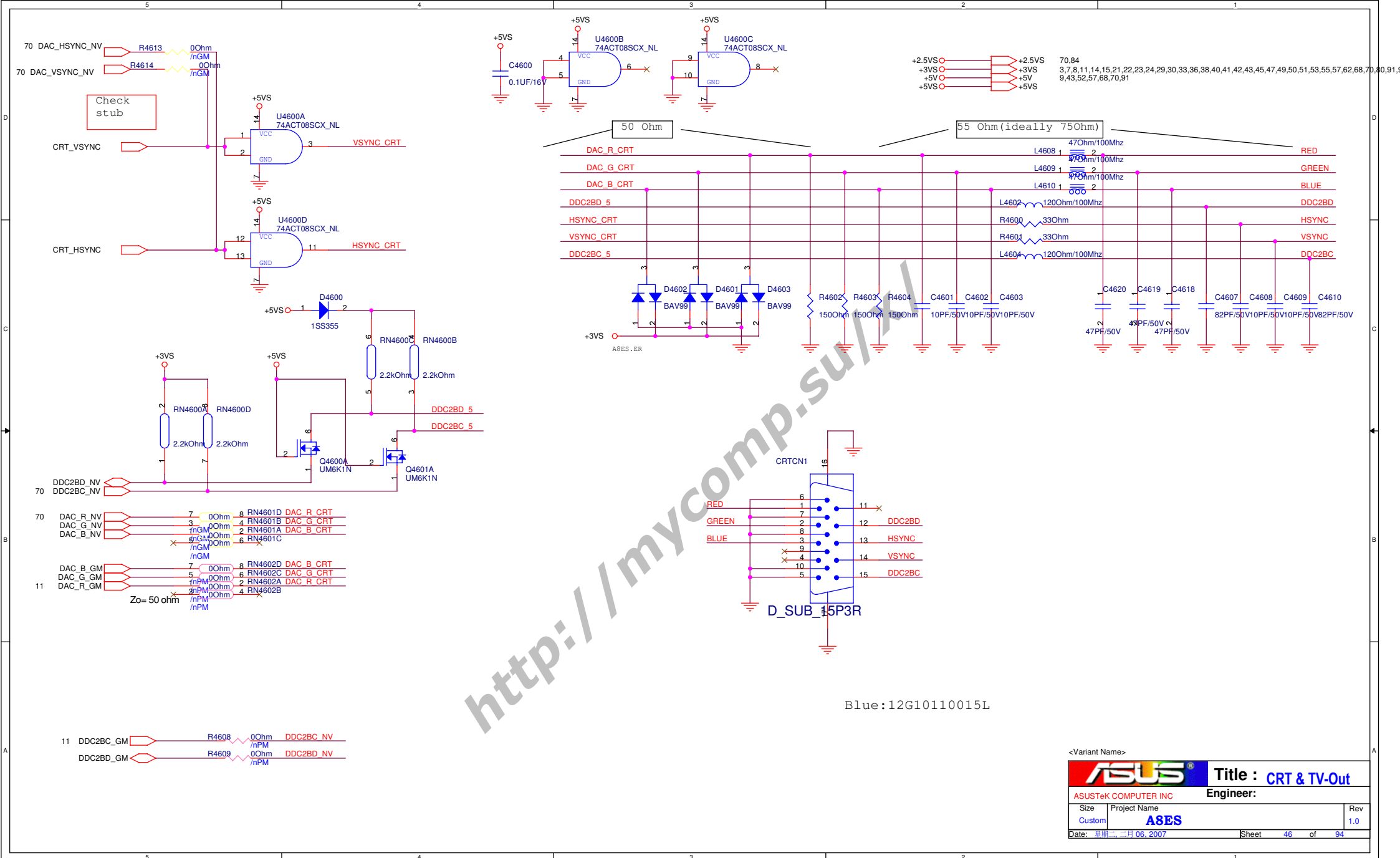
<Variant Name>

		Title : Express Card	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	1.0	
Date: 2007.06.06		Sheet 43 of 94	

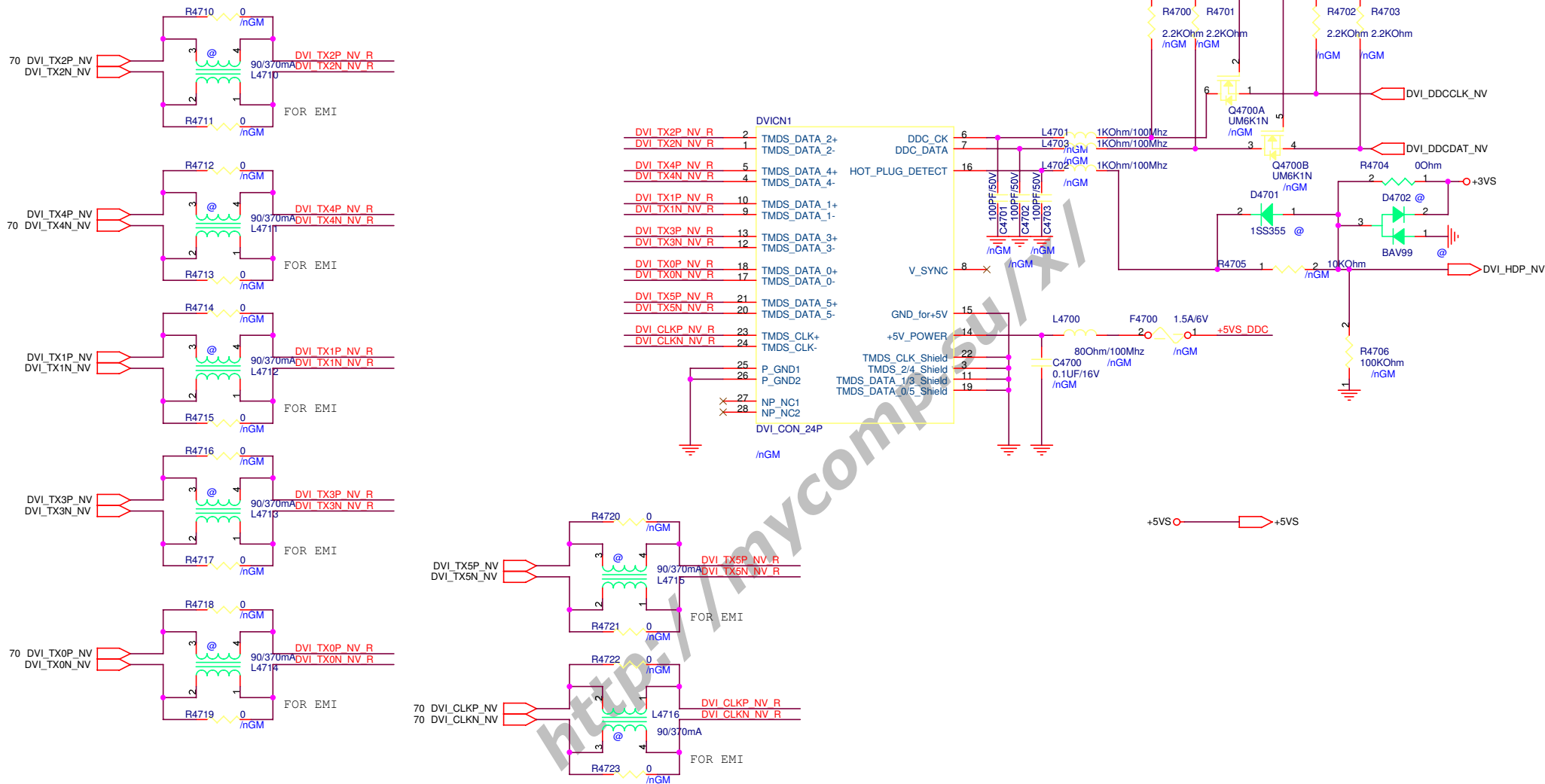
	5	4	3	2	1						
D											
C											
B											
A	 Title : Blank Engineer: <table><tr><td>Size</td><td>Project Name</td><td>Rev</td></tr><tr><td>A</td><td>A8ES</td><td>1.0</td></tr></table> Date: 星期三, 十月 11, 2006Sheet 44 of 94					Size	Project Name	Rev	A	A8ES	1.0
Size	Project Name	Rev									
A	A8ES	1.0									
	5	4	3	2	1						

Check stub

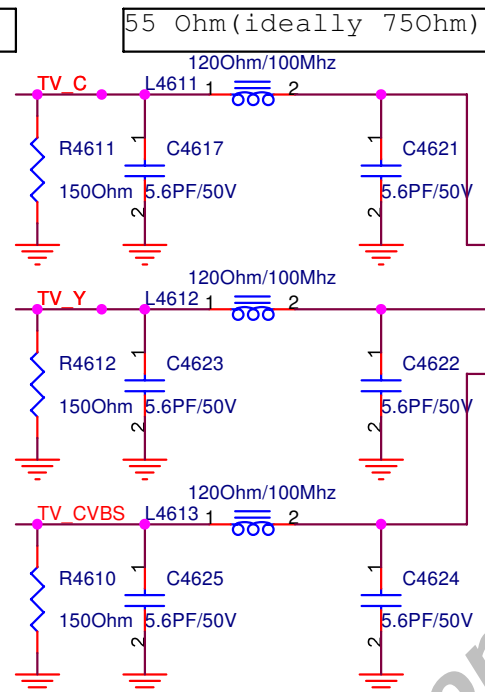
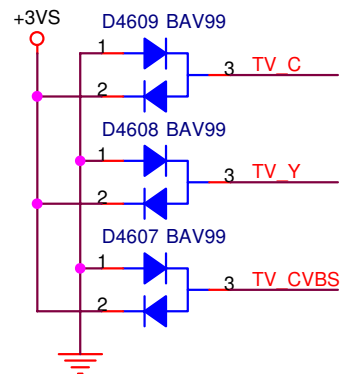




Add DVI Choke 09G092145000 for EMI

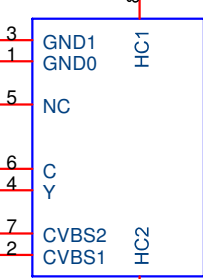


		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: 星期三, 十月 11, 2006		Sheet 48 of 94	

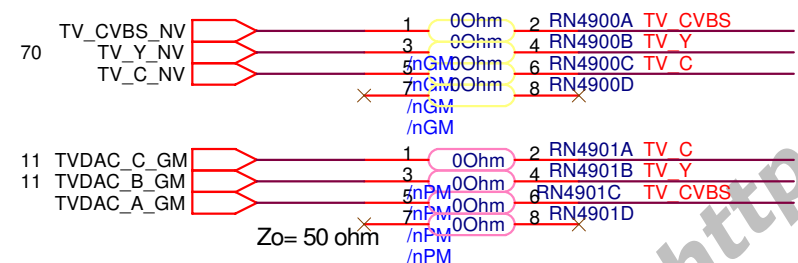
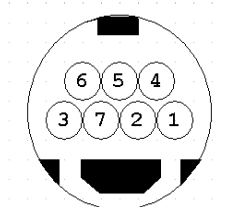


HDTV_EN#

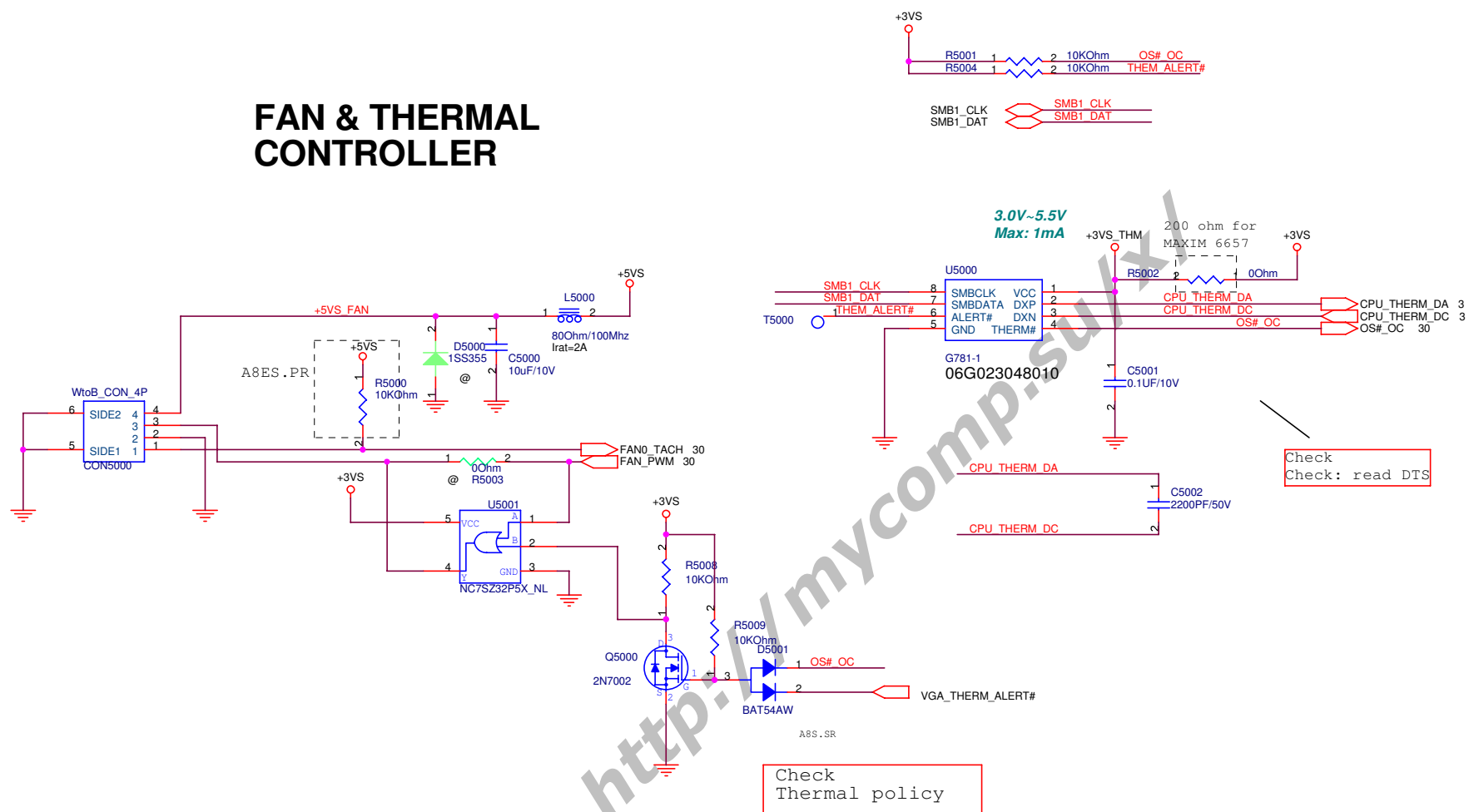
12-141011077



TVSCN1
MINI_DIN_7P
12G141011077

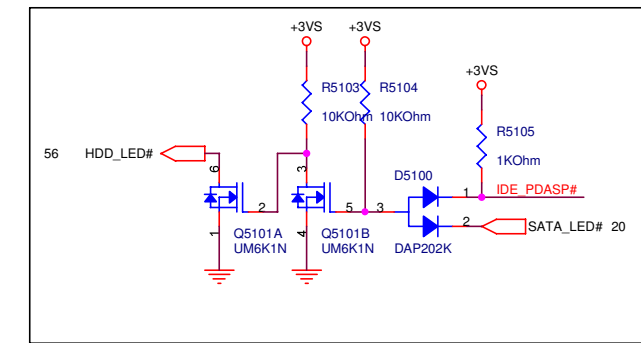
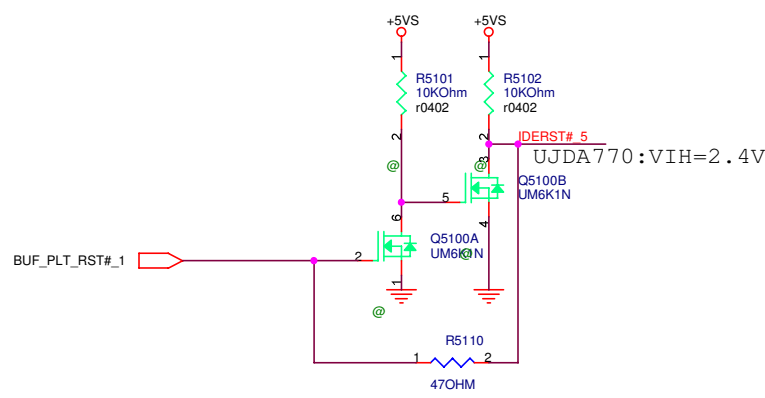
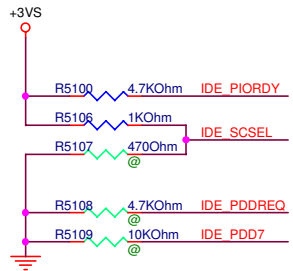


FAN & THERMAL CONTROLLER



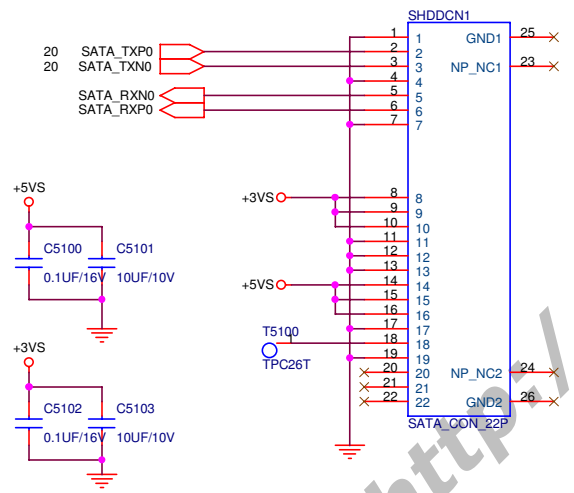
<Variant Name>

ASUS		Title : FAN & THERMAL	
ASUSTeK COMPUTER INC		Engineer:	
Size B	Project Name A8ES	Rev 1.0	
Date: 星期二, 三月 06, 2007		Sheet 50 of 94	



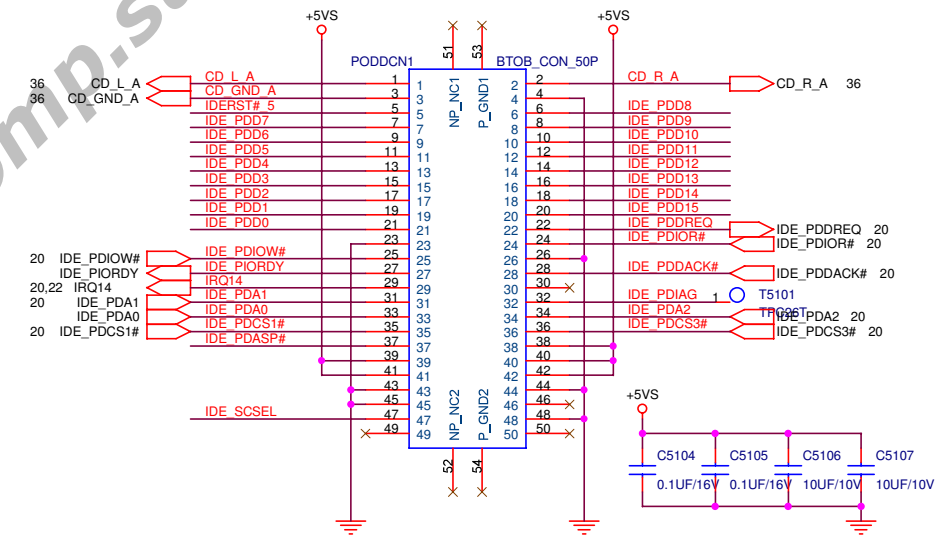
20 IDE_PDD[0..15] IDE_PDD[0..15]

SATA HDD CON



+3VS +3VS 3,7,8,11,14,15,21,22,23,24,29,30,33,36,38,40,41,42,43,45,46,47,49,50,53,55,57,62,68,70,80,91,92
 +5VS +5VS
 +5V +5V 9,43,52,57,68,70,91

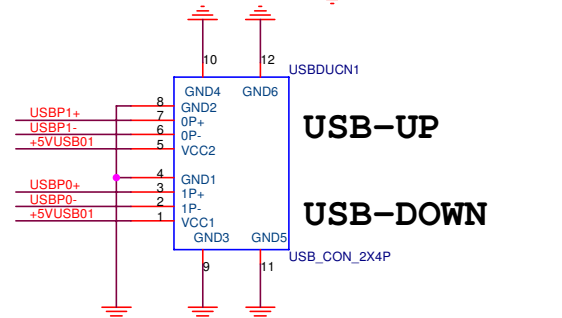
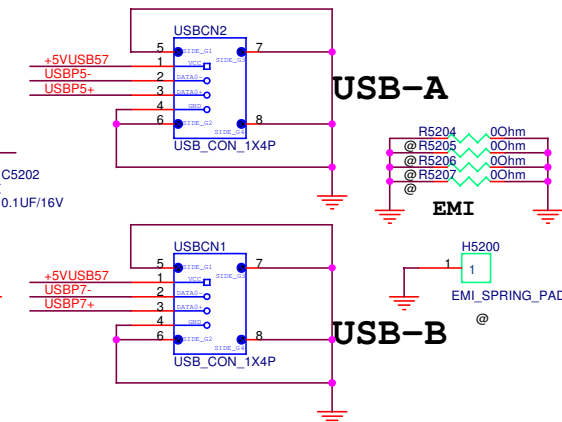
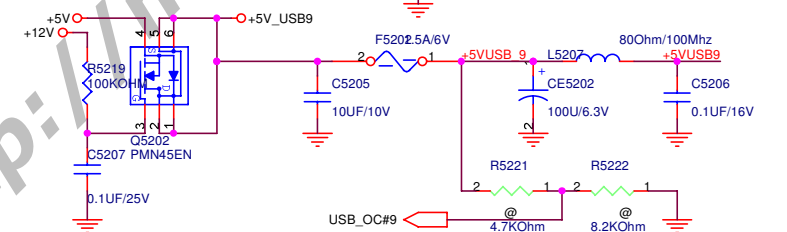
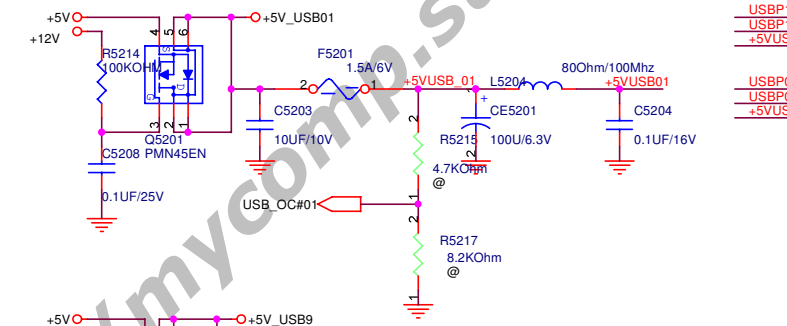
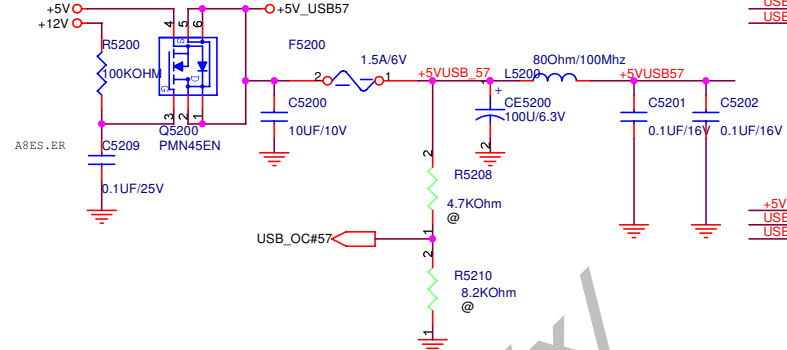
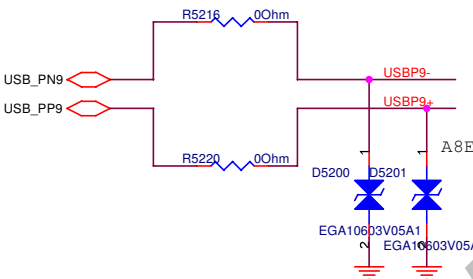
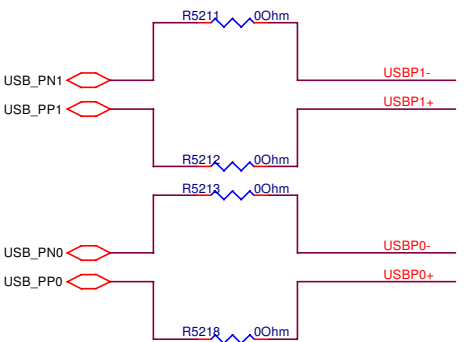
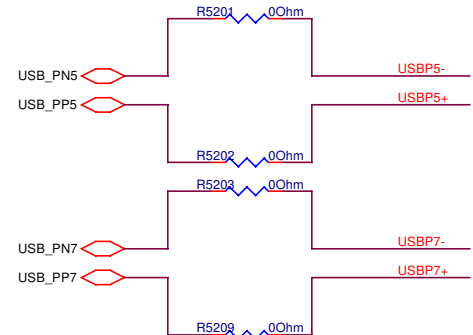
PATA CD-ROM CON



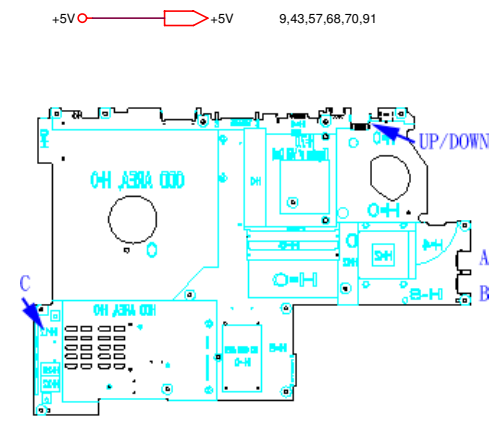
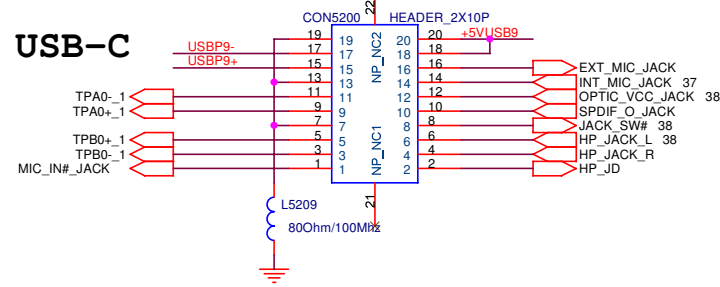
ASUS		Title : HDD & ODD	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
B	A8ES	1.0	
Date: 星期三, 三月 06, 2007	Sheet 51	of 94	

A8ES.PR
Remove USB
common
choke
co-lay

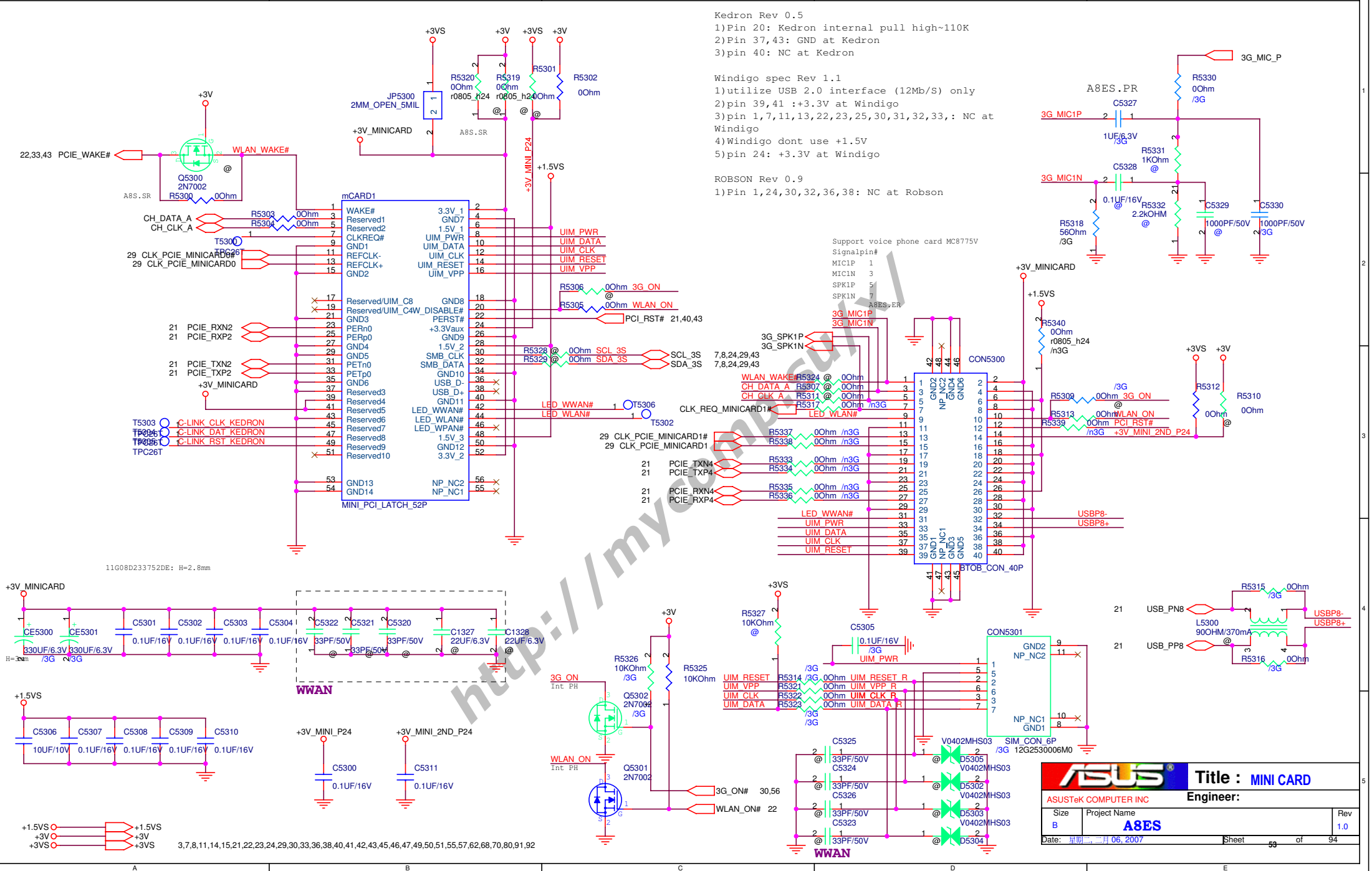
A8ES.PR EMI
H5201
EMI_SPRING_PAD



SUB-PCB: USB/1394/MIC/EARPHONE



ASUS		Title : USB/SUB PCB	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	1.0	
Date: 2007.06.06		Sheet	52 of 94

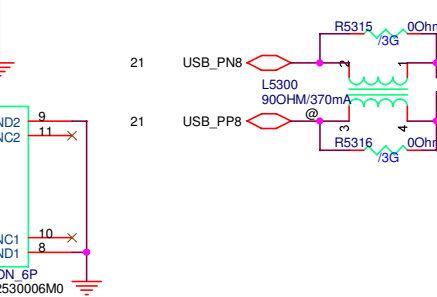
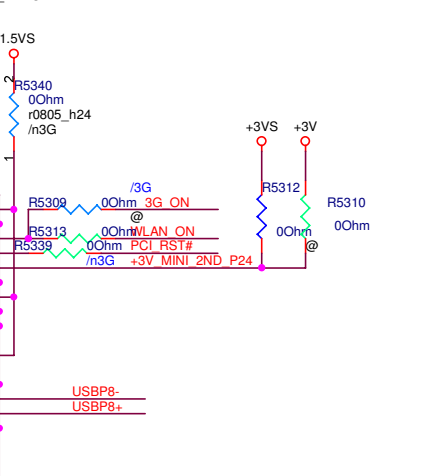
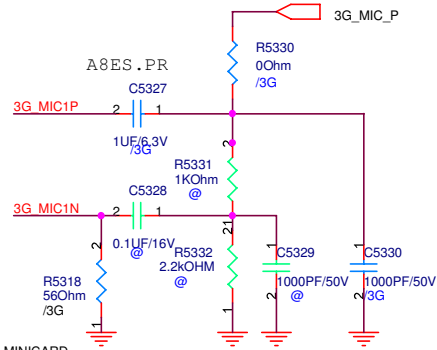


Kedron Rev 0.5
1) Pin 20: Kedron internal pull high~110K
2) Pin 37,43: GND at Kedron
3) pin 40: NC at Kedron

Windigo spec Rev 1.1
1) utilize USB 2.0 interface (12Mb/S) only
2) pin 39,41 :+3.3V at Windigo
3) pin 1,7,11,13,22,23,25,30,31,32,33,: NC at Windigo
4) Windigo dont use +1.5V
5) pin 24: +3.3V at Windigo

ROBSON Rev 0.9
1) Pin 1,24,30,32,36,38: NC at Robson

Support voice phone card MC8775V
Signalpin#
MIC1P 1
MIC1N 3
SPK1P 5
SPK1N 7
A8ES,ER

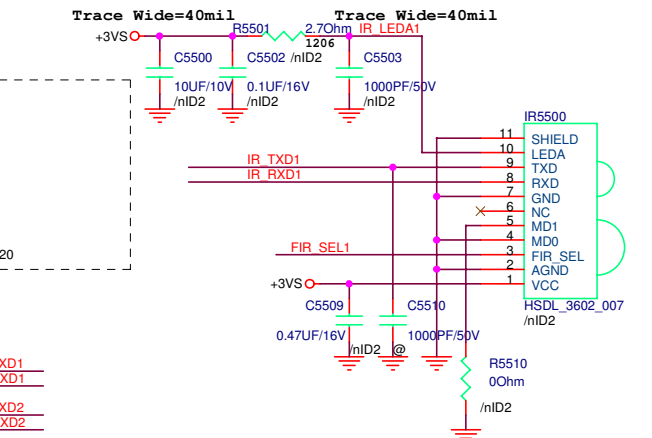
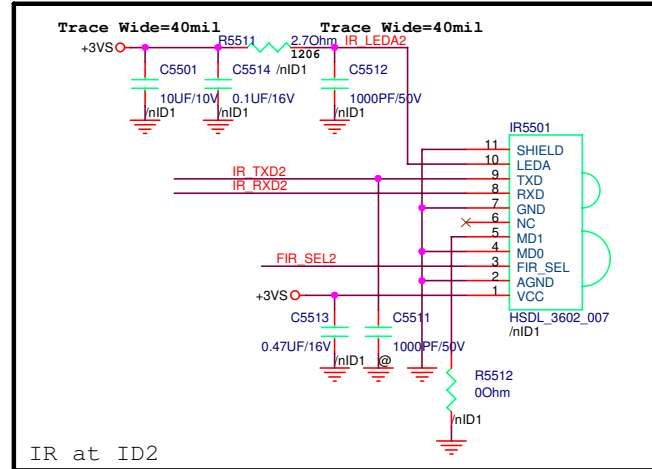
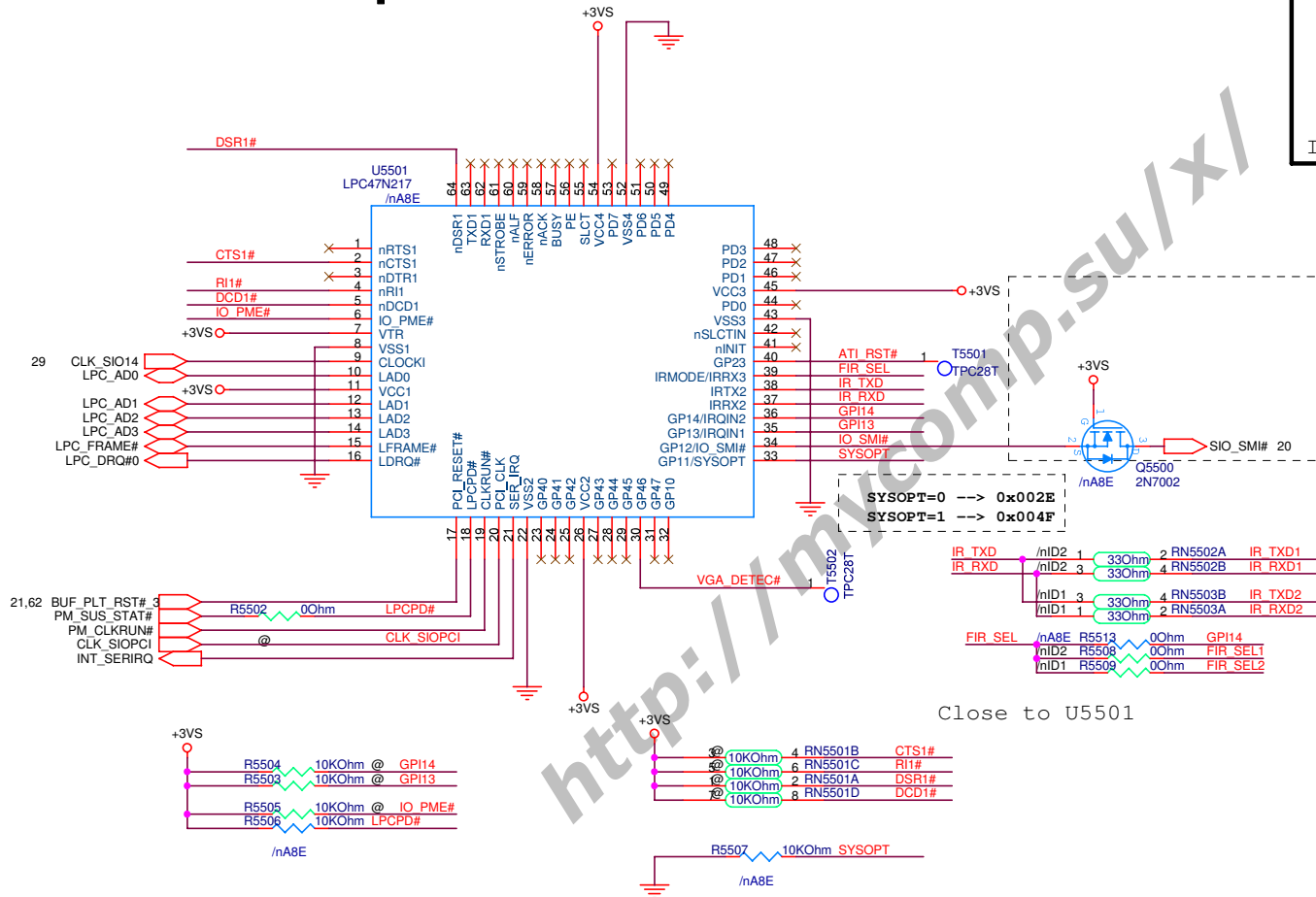


ASUS		Title : MINI CARD	
ASUSTek COMPUTER INC		Engineer:	
Size B	Project Name A8ES	Rev 1.0	
Date: 星期日, 三月 06, 2007	Sheet 59	of	94

		Title : BLANK	
ASUSTeK COMPUTER INC			
Engineer:			
Size	Project Name		Rev
Custom	A8ES		0
Date: 2006. 11. 11		Sheet 54 of 94	

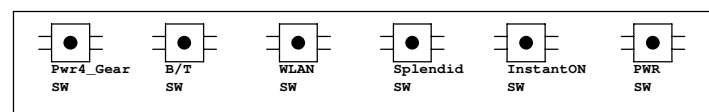
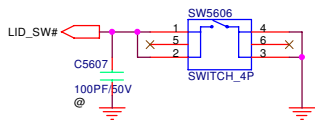
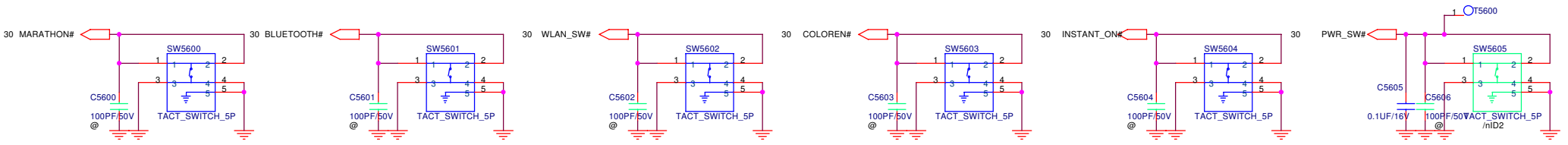
<http://mycomp.su/xl>

Super I/O

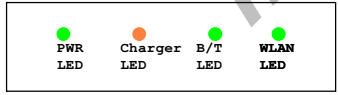
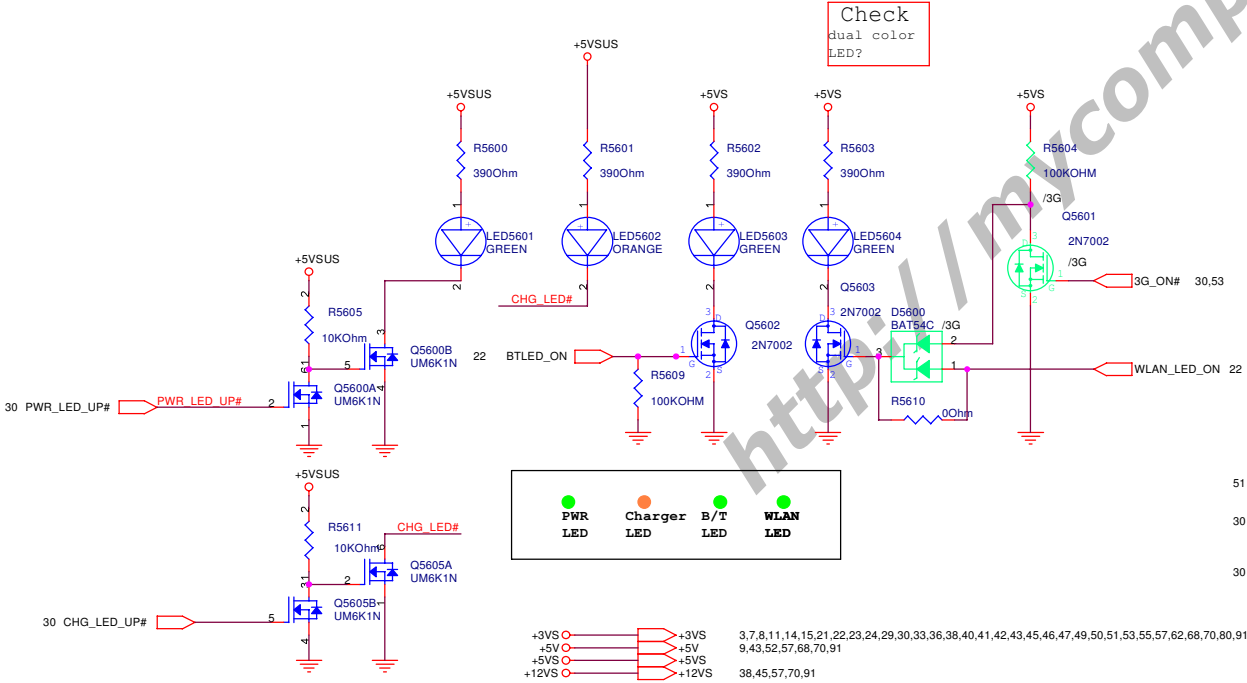
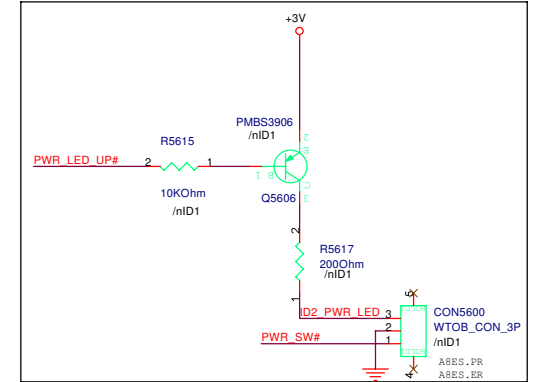


Transceiver Control Truth Table

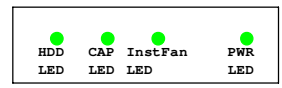
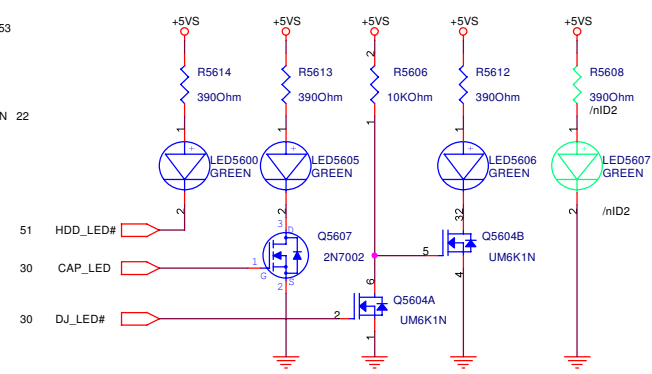
Mode 0	Mode 1	FIR_SEL	RX Function	TX Function
1	0	X	Shutdown	Shutdown
0	0	0	SIR	Full Distance Power
0	1	0	SIR	2/3 Distance Power
1	1	0	SIR	1/3 Distance Power
0	0	1	MIR/FIR	Full Distance Power
0	1	1	MIR/FIR	2/3 Distance Power
1	1	1	MIR/FIR	1/3 Distance Power



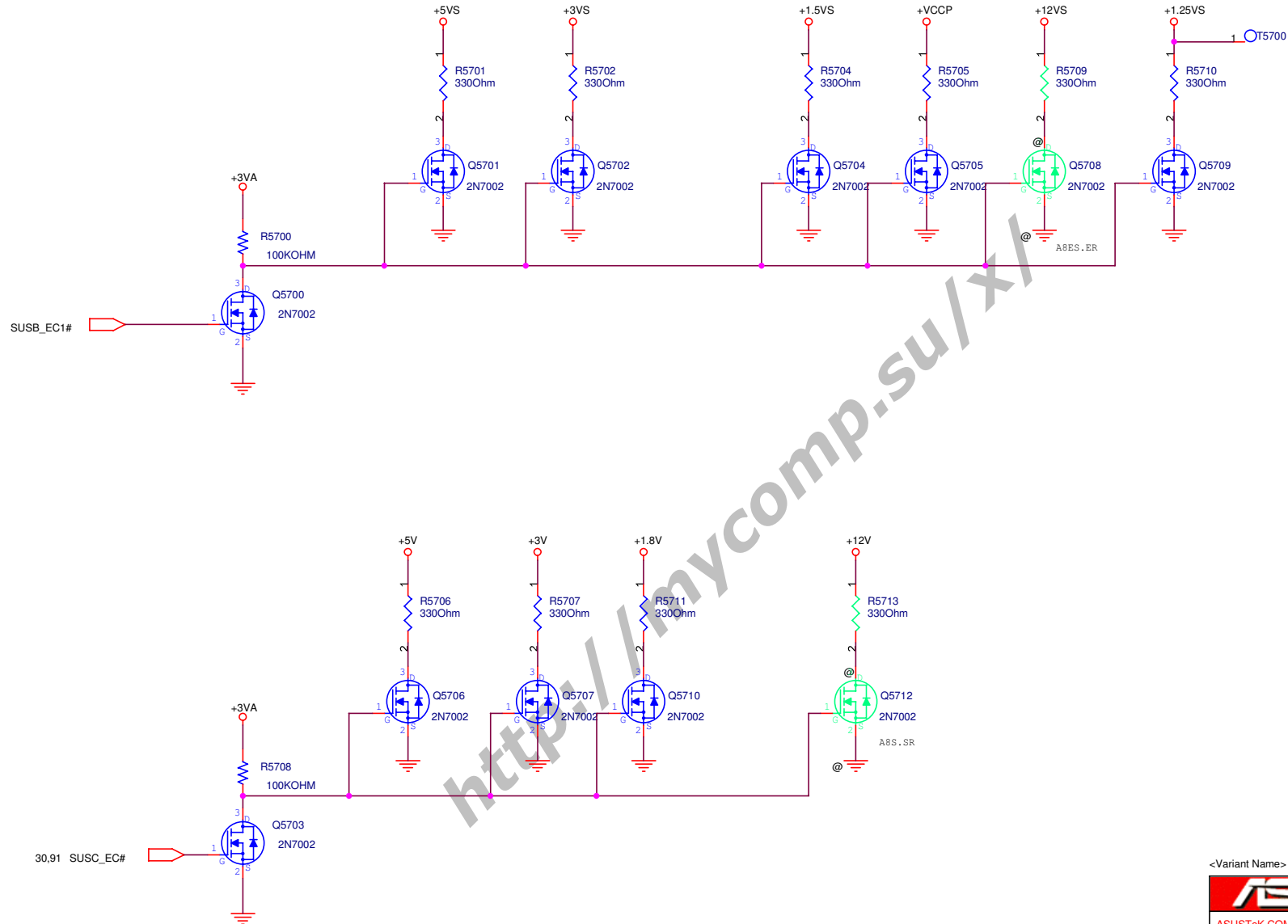
Reserve for ID2



+3VS	3,7,8,11,14,15,21,22,23,24,29,30,33,36,38,40,41,42,43,45,46,47,49,50,51,53,55,57,62,68,70,80,91,92
+5V	9,43,52,57,68,70,91
+5VS	38,45,57,70,91
+12VS	



Discharge Circuit



<Variant Name>

ASUS		Title : Discharge	
ASUSTeK COMPUTER INC		Engineer:	
Size B	Project Name A8ES		Rev 1.0
Date: 星期二, 06月06, 2007	Sheet 57 of 94		

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

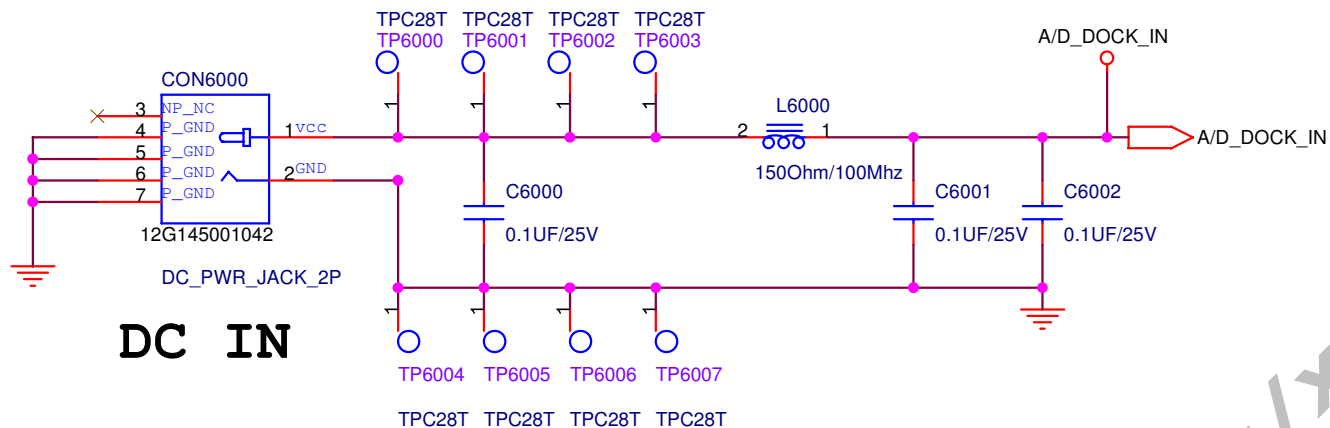
<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	A8ES		1.0
Date: 星期三, 十月 11, 2006		Sheet	of 94

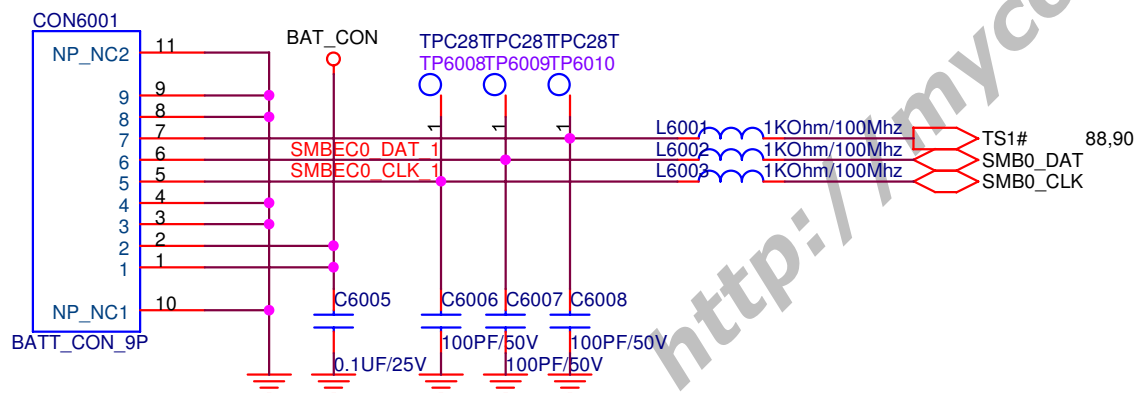
	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

<http://mycomp.su/xl>

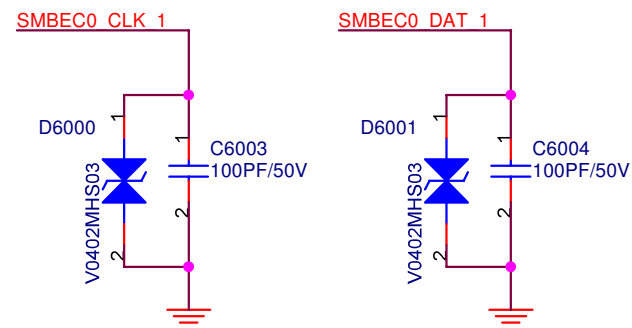
					A
Title					
<Title>					
Size	Document Number			Rev	
A	W2S			1.1	
Date:	星期三, 十月 11, 2006			Sheet	
	2			59 of 94	1



DC IN

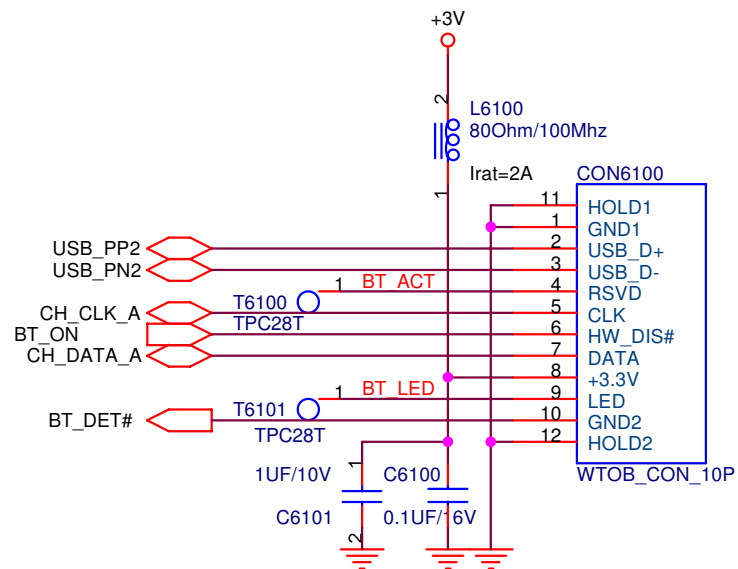


Battery Connector



<Variant Name>

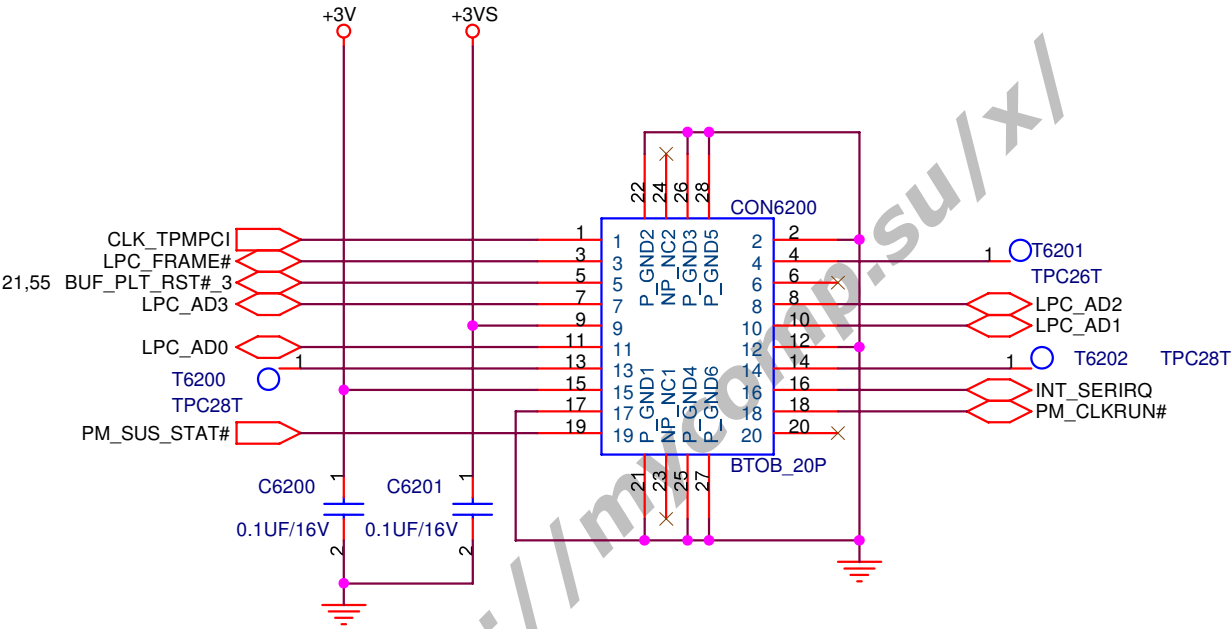
		Title : DC IN / BAT	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 1.0
Date: 星期二, 二月 06, 2007		Sheet	60 of 94



Bluetooth Module CON

ASUS		Title :BT/CAMERA	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 1.0
Date: 星期二, 二月 06, 2007		Sheet	61 of 94

TPM 1.2 Module



<Variant Name>

		Title :TPM	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	A8ES		1.0
Date: 星期二, 二月 06, 2007		Sheet	62 of 94

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

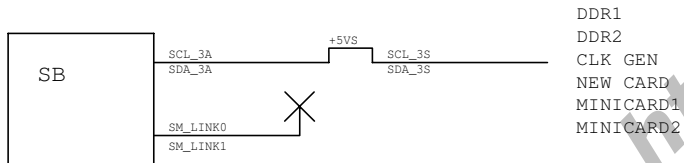
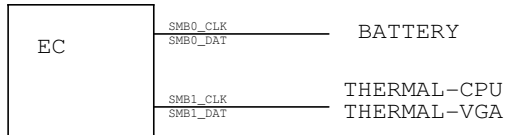
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: 星期三, 十月 11, 2006		Sheet 63 of 94	

http://mycomp.su/xl

PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 (Internal)		
CARDBUS	AD19	0	F,E

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0 (low)	
SPD/TS	A0/30
SO-DIMM 1(high)	
SPD/TS	A4/34
G781-1	9A
G781(VGA board)	98

Thermal Sensor (CPU)
SM-Bus Mapping 1001100



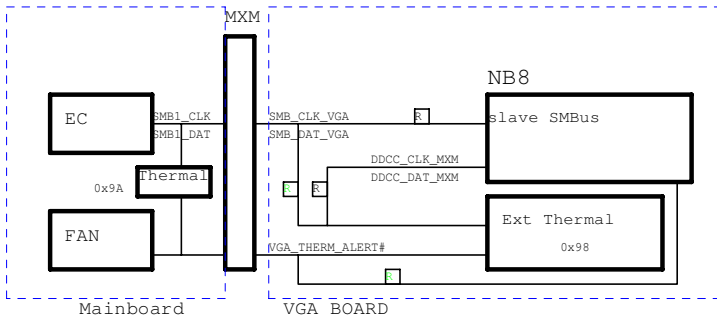
BOM option

nGM:yellow
 nPM:light red
 =====
 @ : no stuff for all
 nGM :no stuff for A8E
 nPM :no stuff for A8S
 nGM1:no stuff for A8E, A8E/SR mount for debugging A8S in advance
 3G :for Windigo,SIERRA MC8775V
 nA8E :no stuff Irda for A8E

Support ID2:

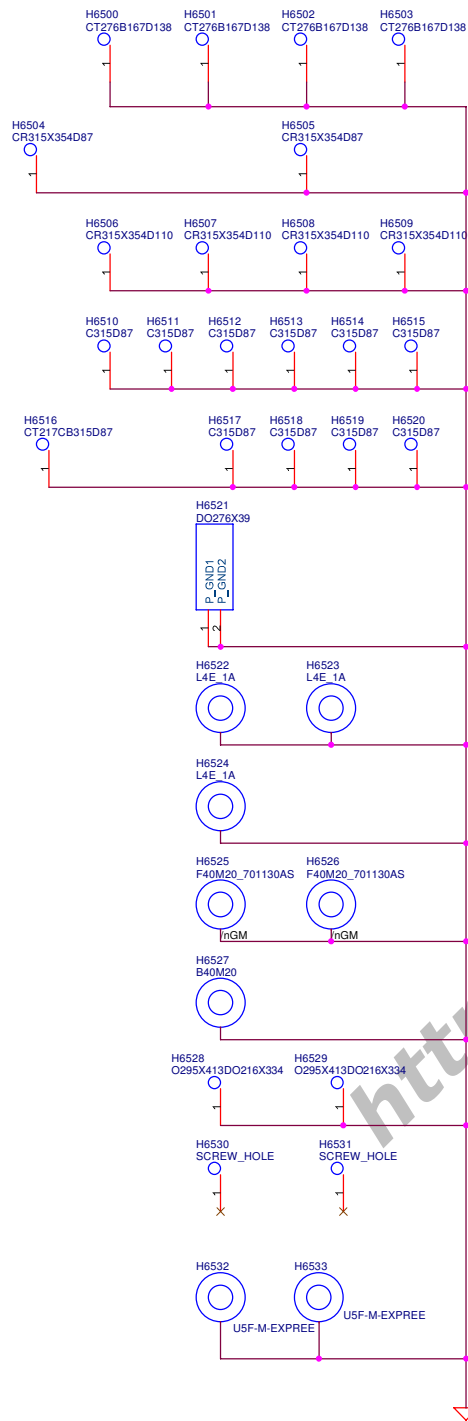
Support ID2:
 page 68,Finger print
 page 55,IR
 Page 56,pwr switch and LED

Thermal block diagram



<Variant Name>

ASUS		Title :	
ASUSTeK COMPUTER INC		Engineer:	
Size B	Project Name A8ES	Rev 1.0	
Date: 星期二, 06 06, 2007	Sheet 64 of 94		



CPU

SCREW

U HOLE

SCREW

IO Board

MDC_NUT

TPM_NUT

VGA_NUT

KB_NUT

KEYBOARD

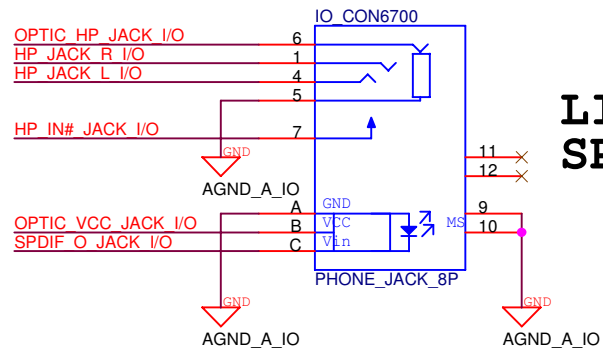
FIXED HOLE

miniCard

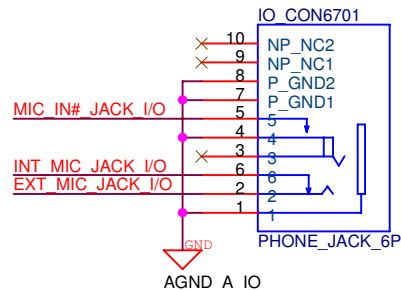
Title		
<Title>		
Size	Document Number	Rev
CustomW2S		1.1
Date:	日期: 十二月 26, 2006	Sheet 65 of 94

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
B	A8ES		0
Date: 星期三, 十月 11, 2006		Sheet	66 of 94

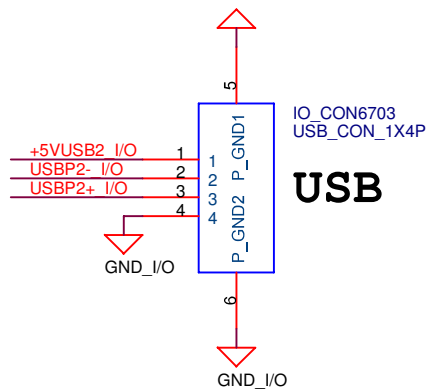
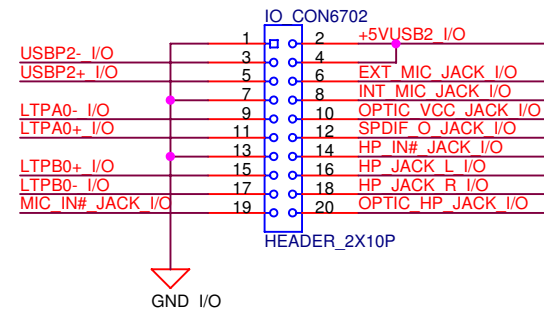
<http://mycomp.su/xl>



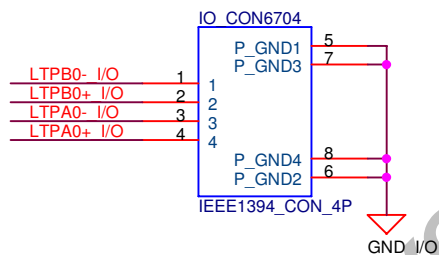
LINE_OUT SPDIF



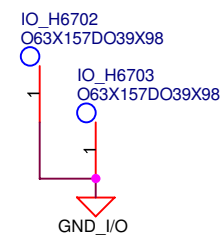
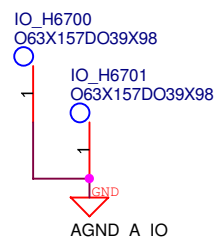
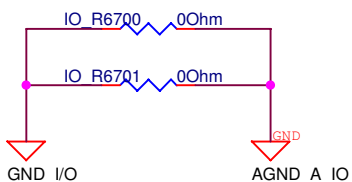
MIC



USB



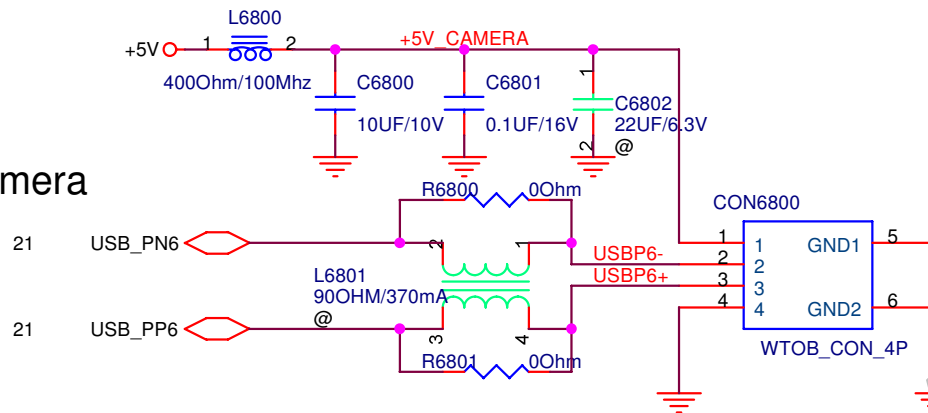
1394A



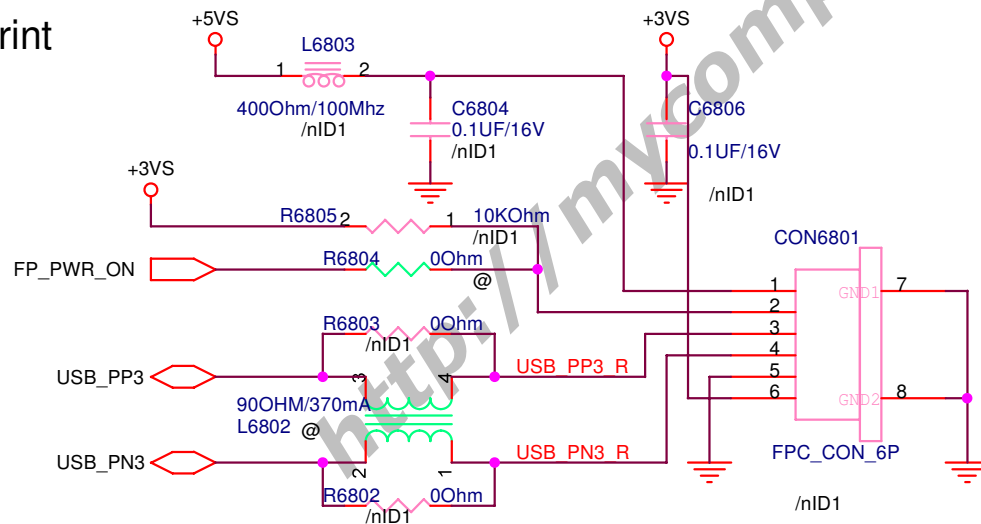
<Variant Name>

ASUS		Title :SUB_PCB	
ASUSTeK COMPUTER INC		Engineer:	
Size A4	Project Name A8ES		Rev 1.0
Date: 星期二, 一月 30, 2007		Sheet 67 of 94	

Camera



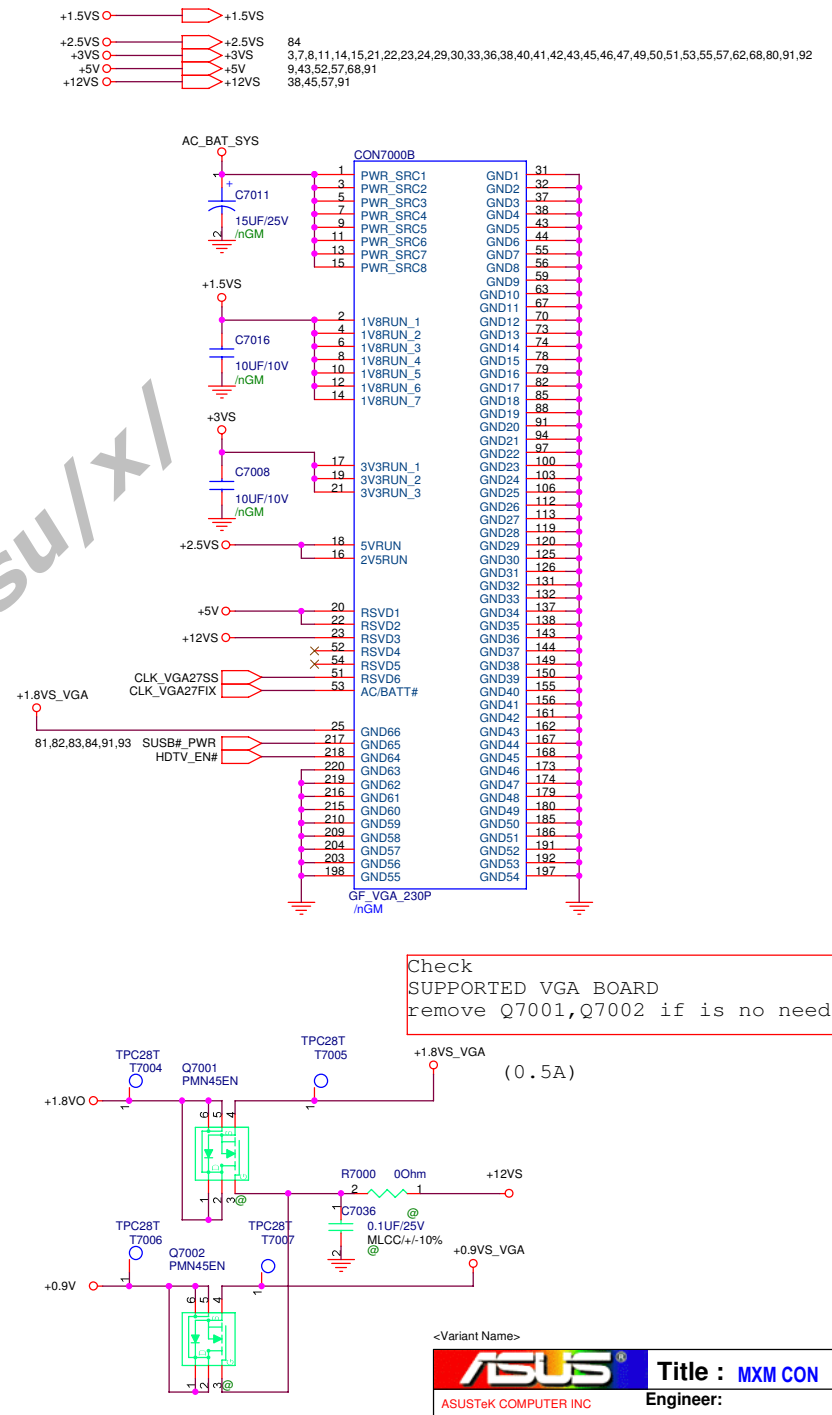
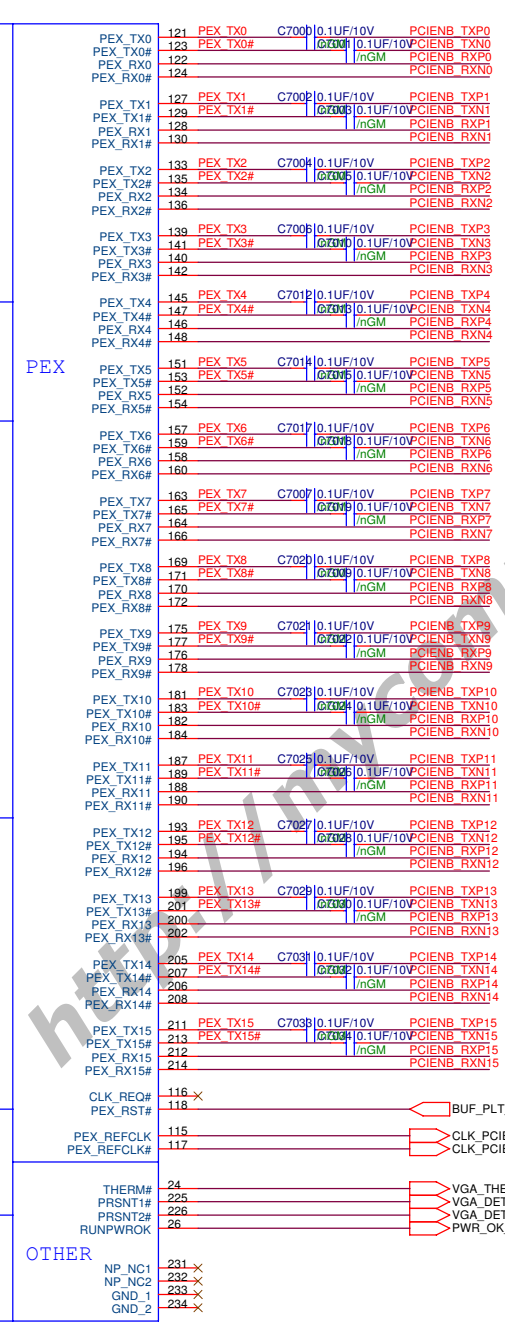
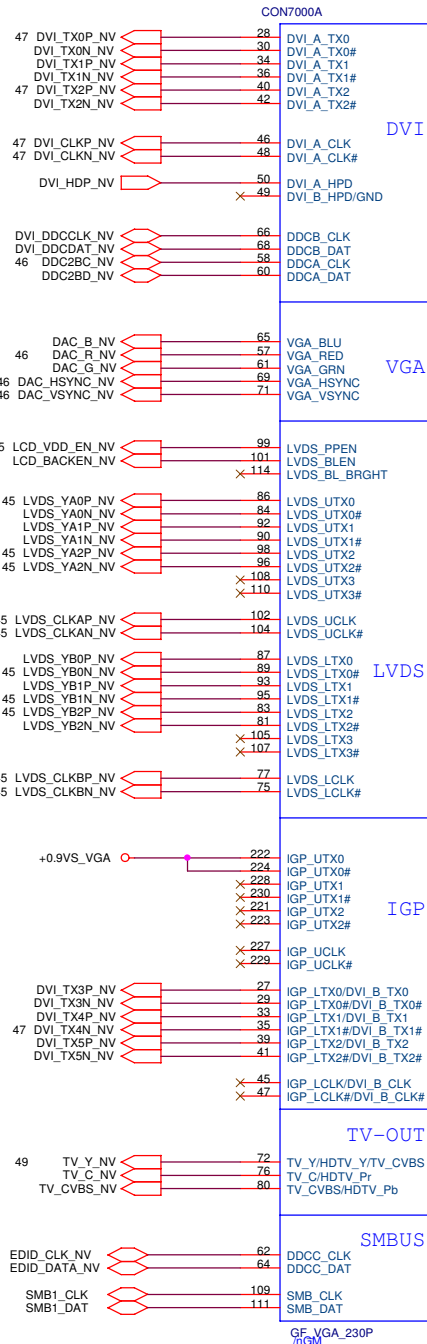
Finger Print

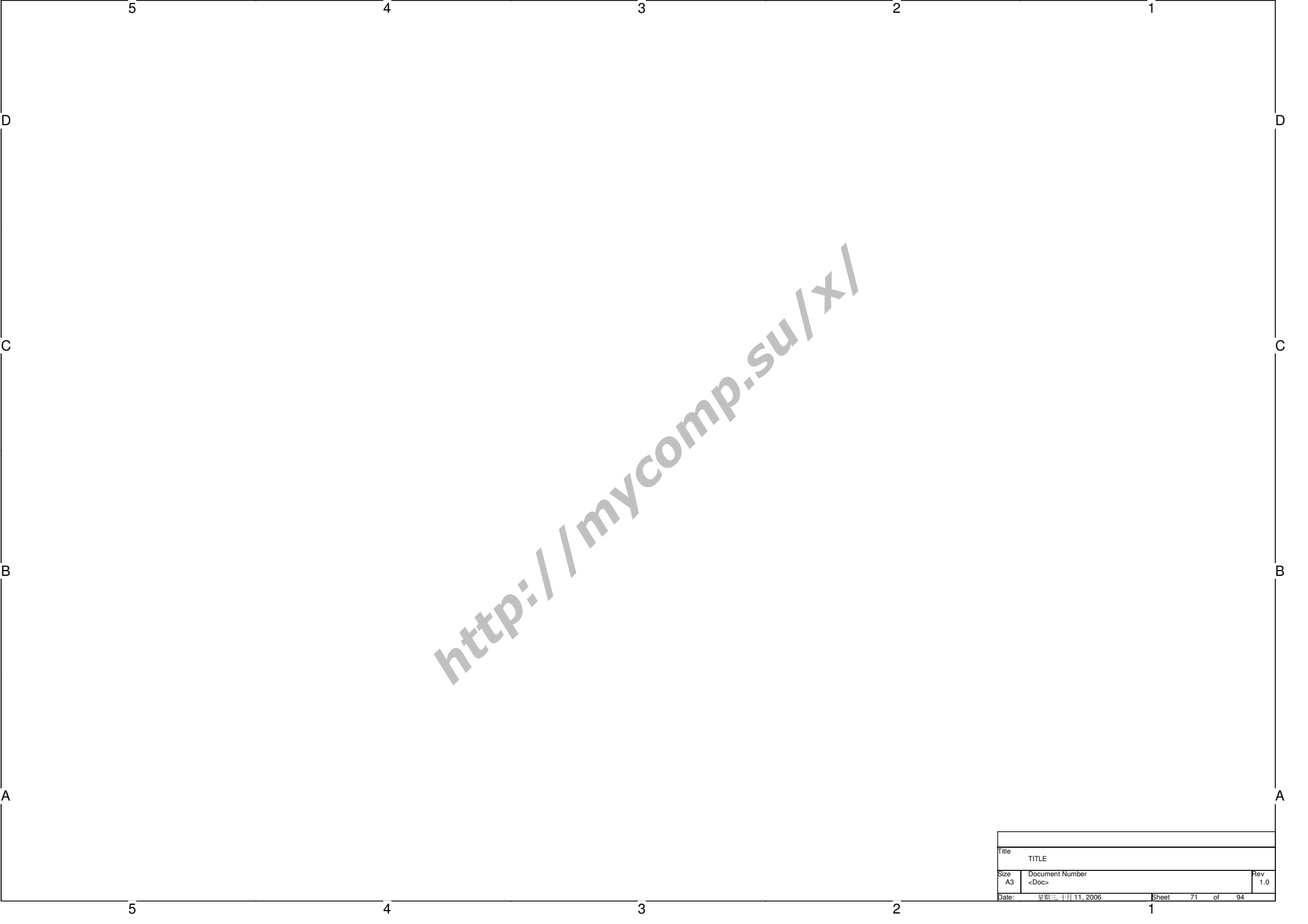


<Variant Name>

ASUS		Title : CAMERA/FingerPrinter	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 1.0
Date: 星期三, 二月 06, 2007		Sheet 60	of 94

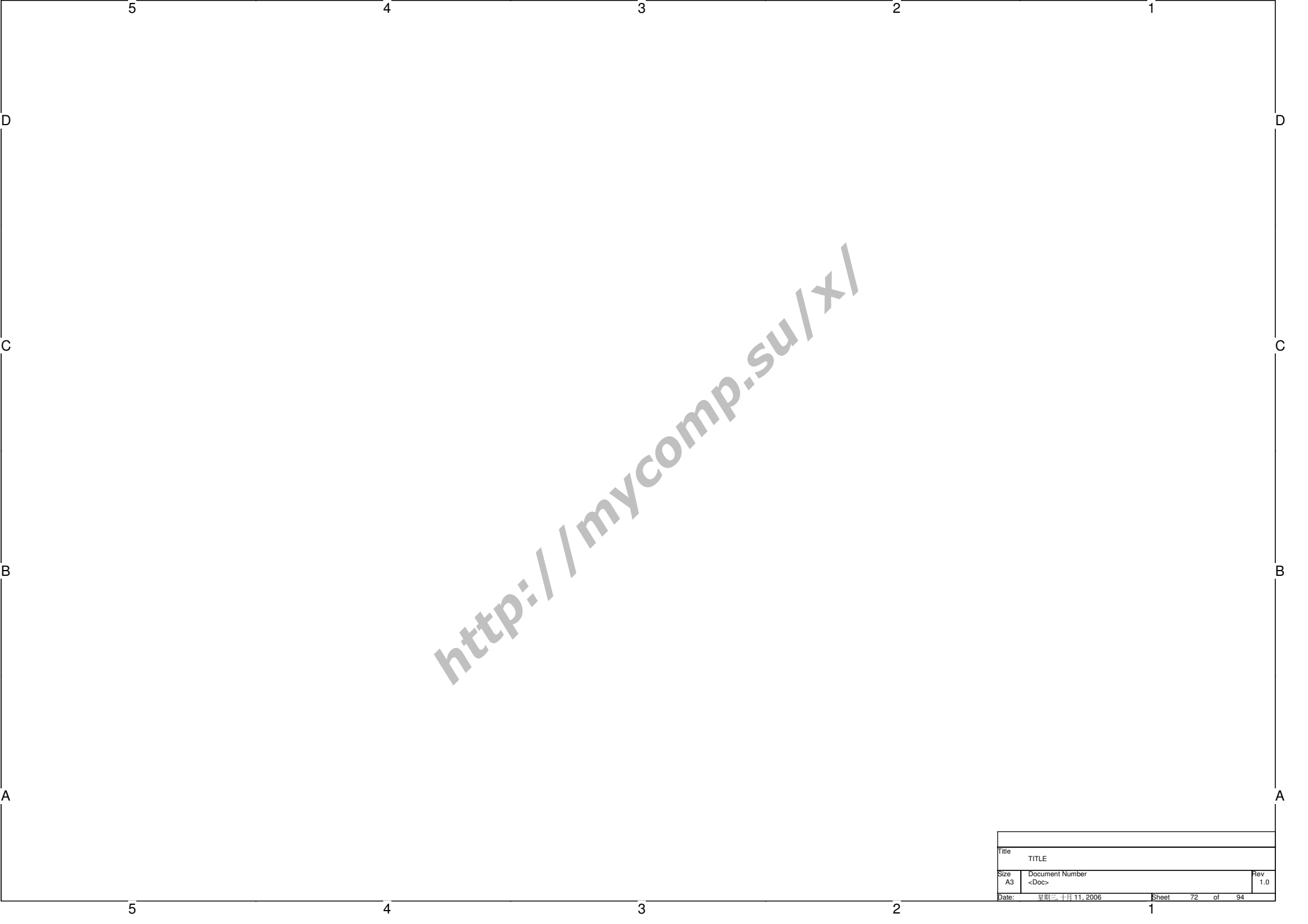
		Title: BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: 星期三, 十月 11, 2006		Sheet 69 of 94	

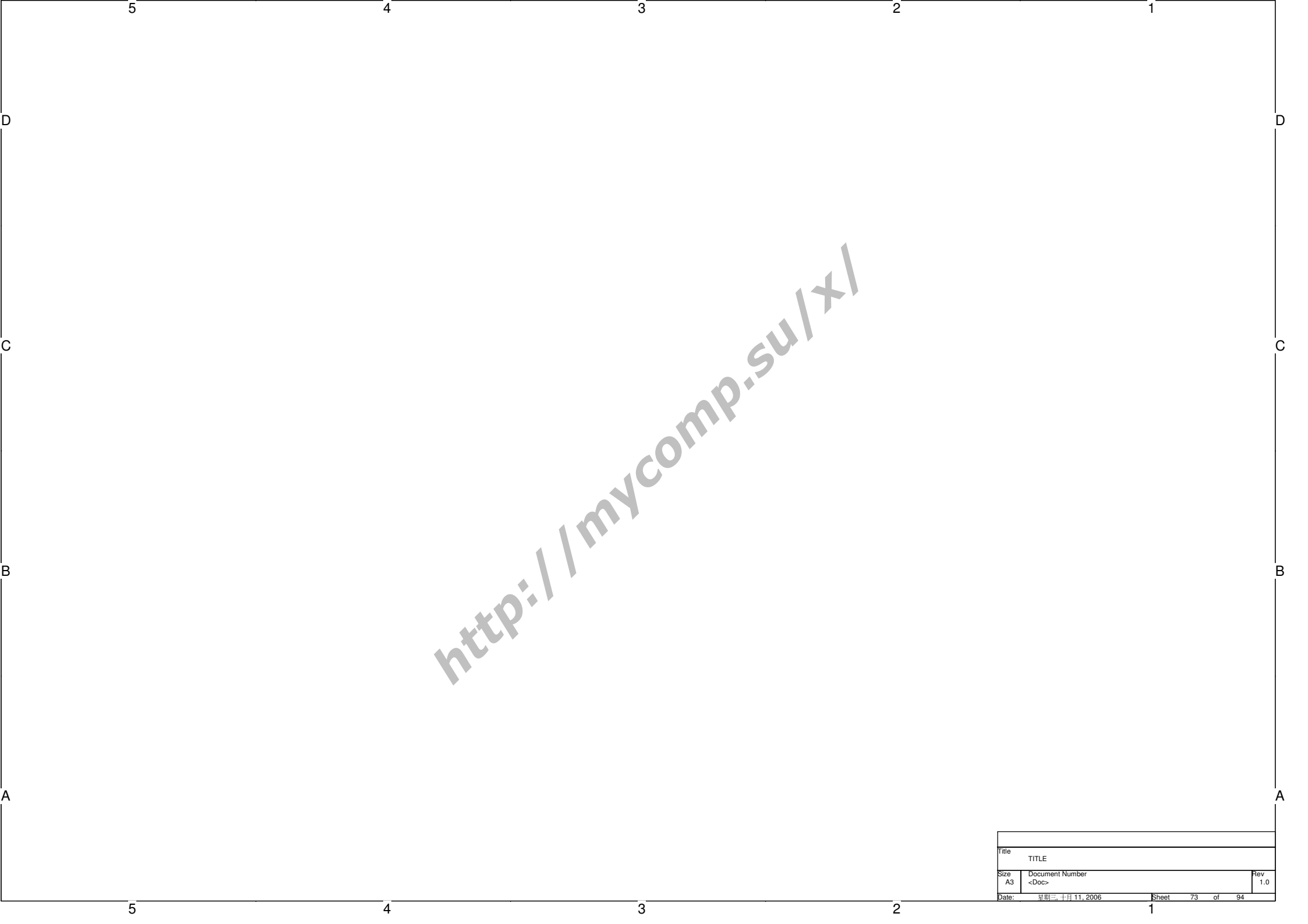




<http://mycomp.su/xl>

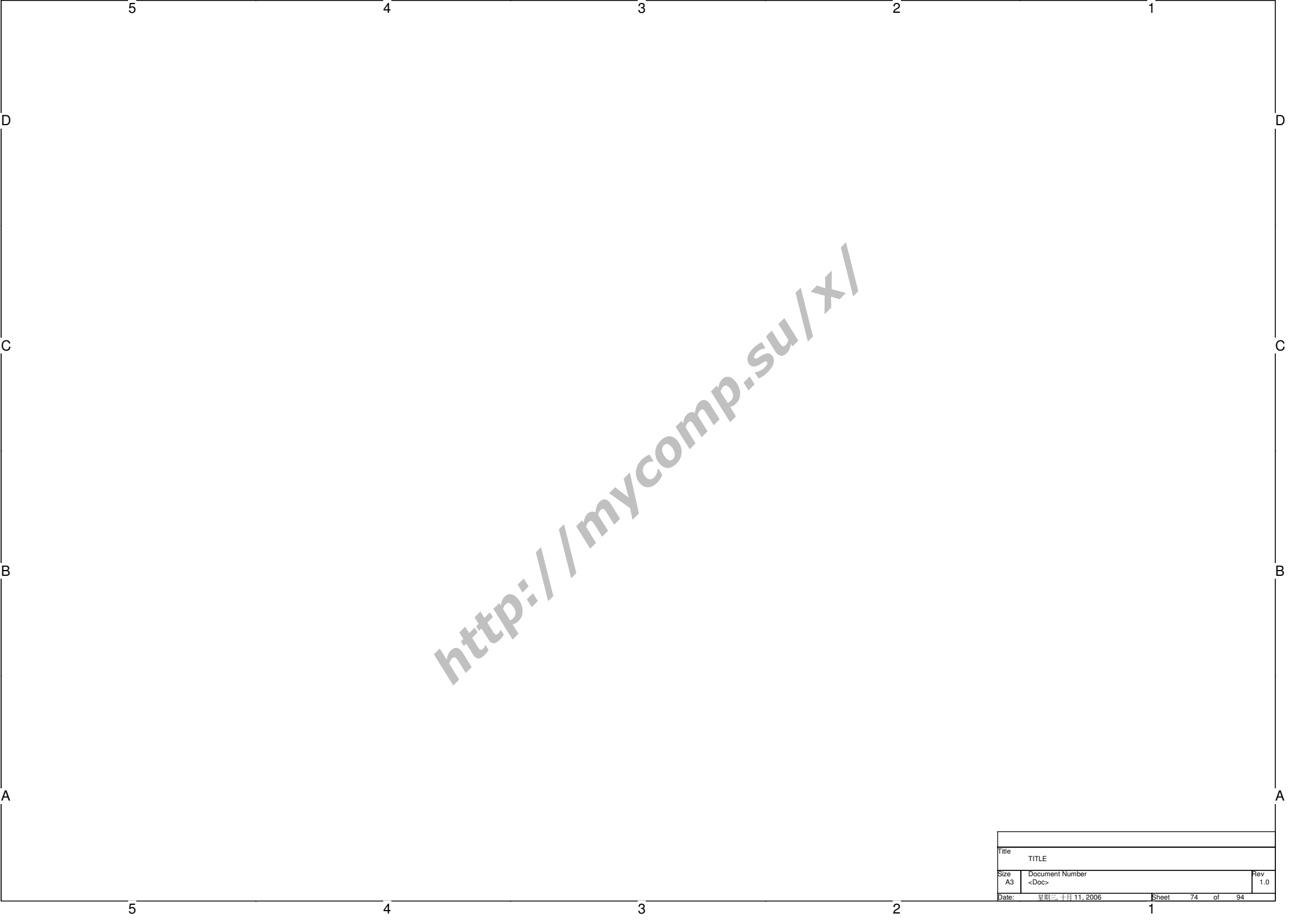
Title			TITLE		
Size	Document Number				Rev
A3	<Doc>				1.0
Date: 星期二, 十月 11, 2006			Sheet 71 of 94		

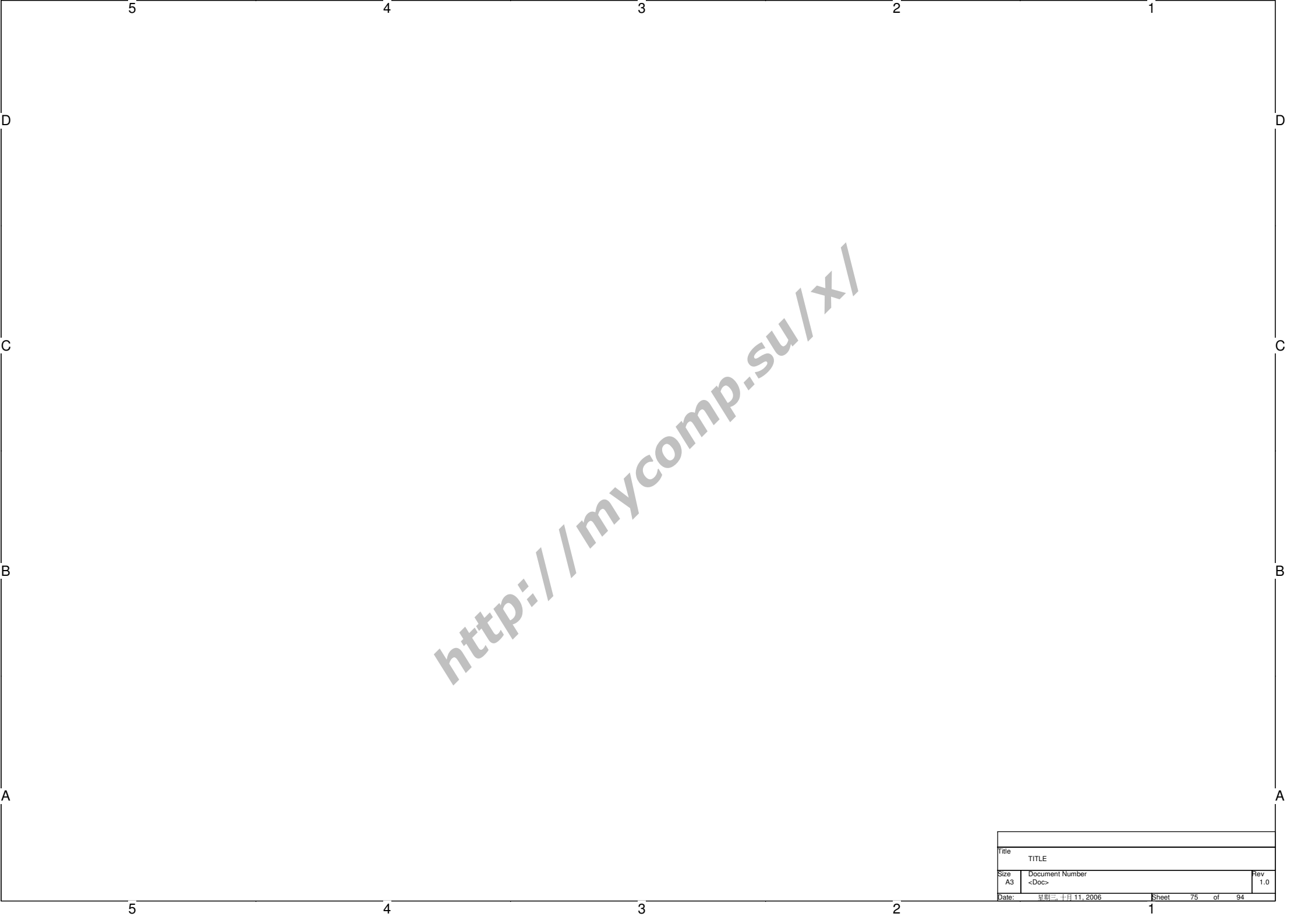


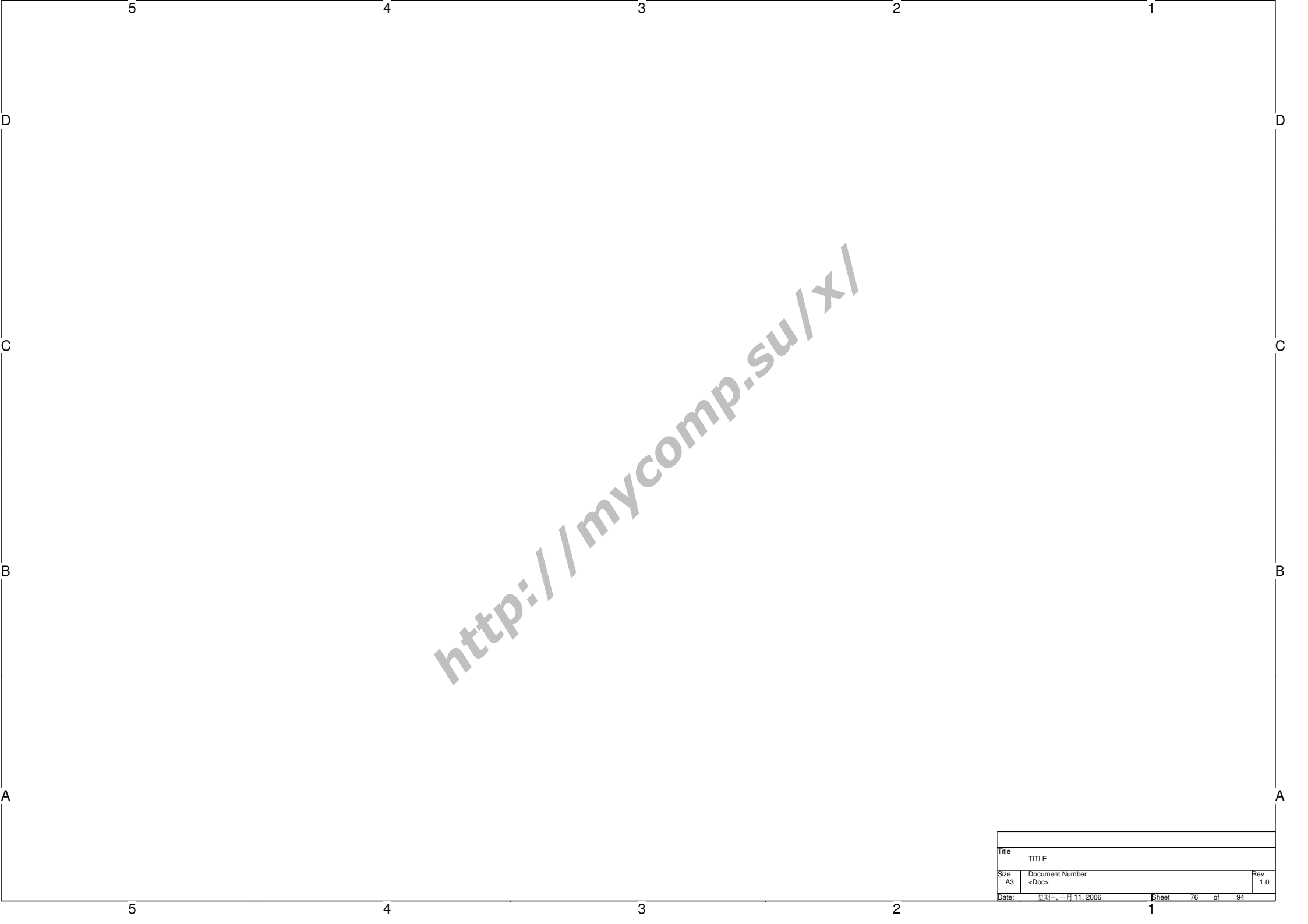


http://mycomp.su/xl

Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date: 星期二, 十月 11, 2006		
Sheet 73 of 94		

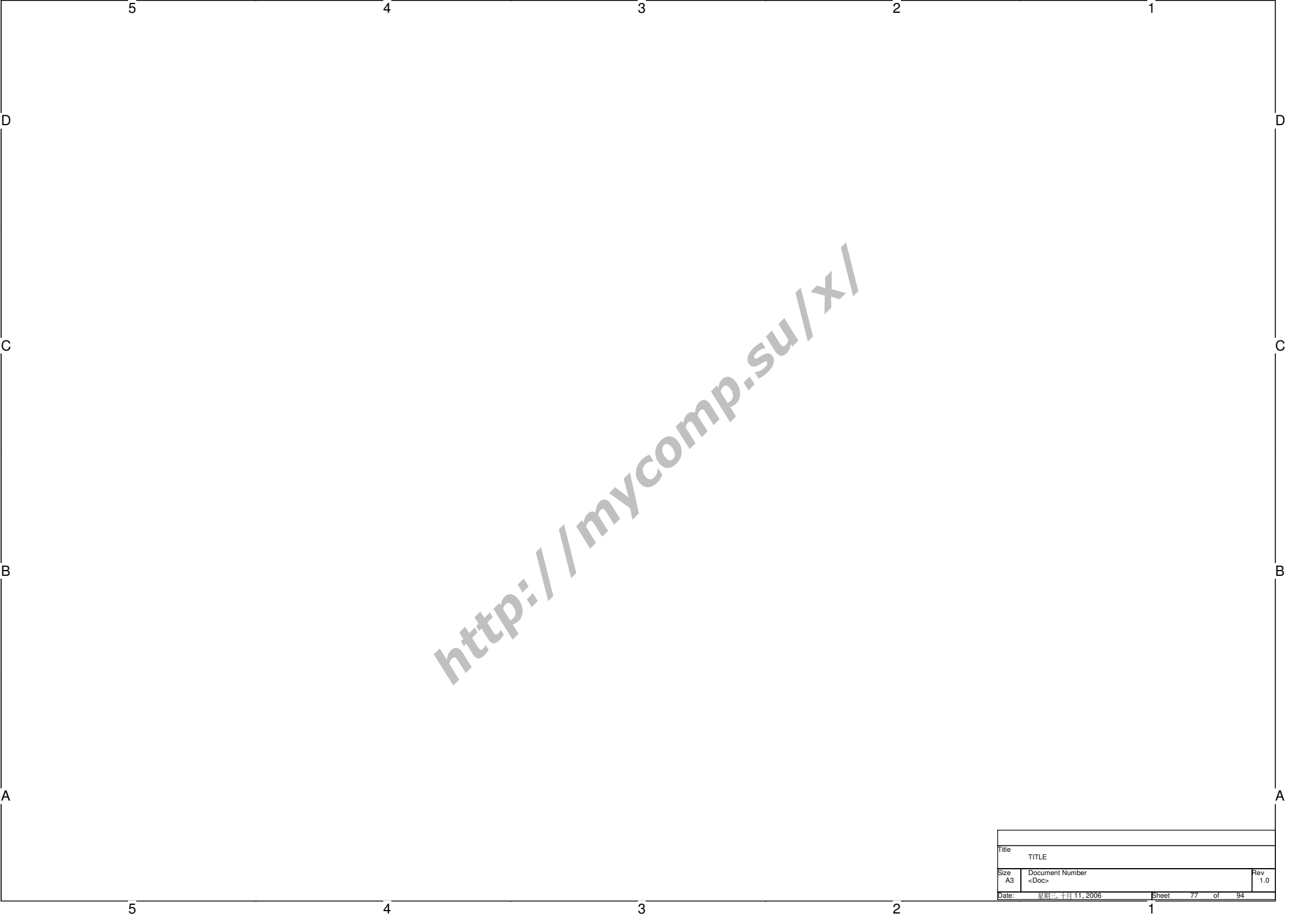






http://mycomp.su/xl

Title			TITLE
Size	Document Number		Rev
A3	<Doc>		1.0
Date:	星期二, 十月 11, 2006		Sheet 76 of 94



http://mycomp.su/xl

Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date:	星期二, 十月 11, 2006	Sheet 77 of 94

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
B	A8ES		0
Date: 星期三, 十月 11, 2006		Sheet	78 of 94

<http://mycomp.su/xl>

W2S

Change Note:
EE :

1. 965PM pin defined modification, C48/D47/BJ29/BE24 from RSVD pin to LVDSA_DATA#_3 / LVDSA_DATA_3 / SA_MA_14 / SB_MA_14
2. CE46 / CE25 --> 11G08D210791
3. Rst button circuit
4. BT_SW pull-high to different plane issue.
5. Remove RN3104
6. VTT_REF reserve in S3.
7. VTT stop in S3.
8. CIR PME# function.

Layout :

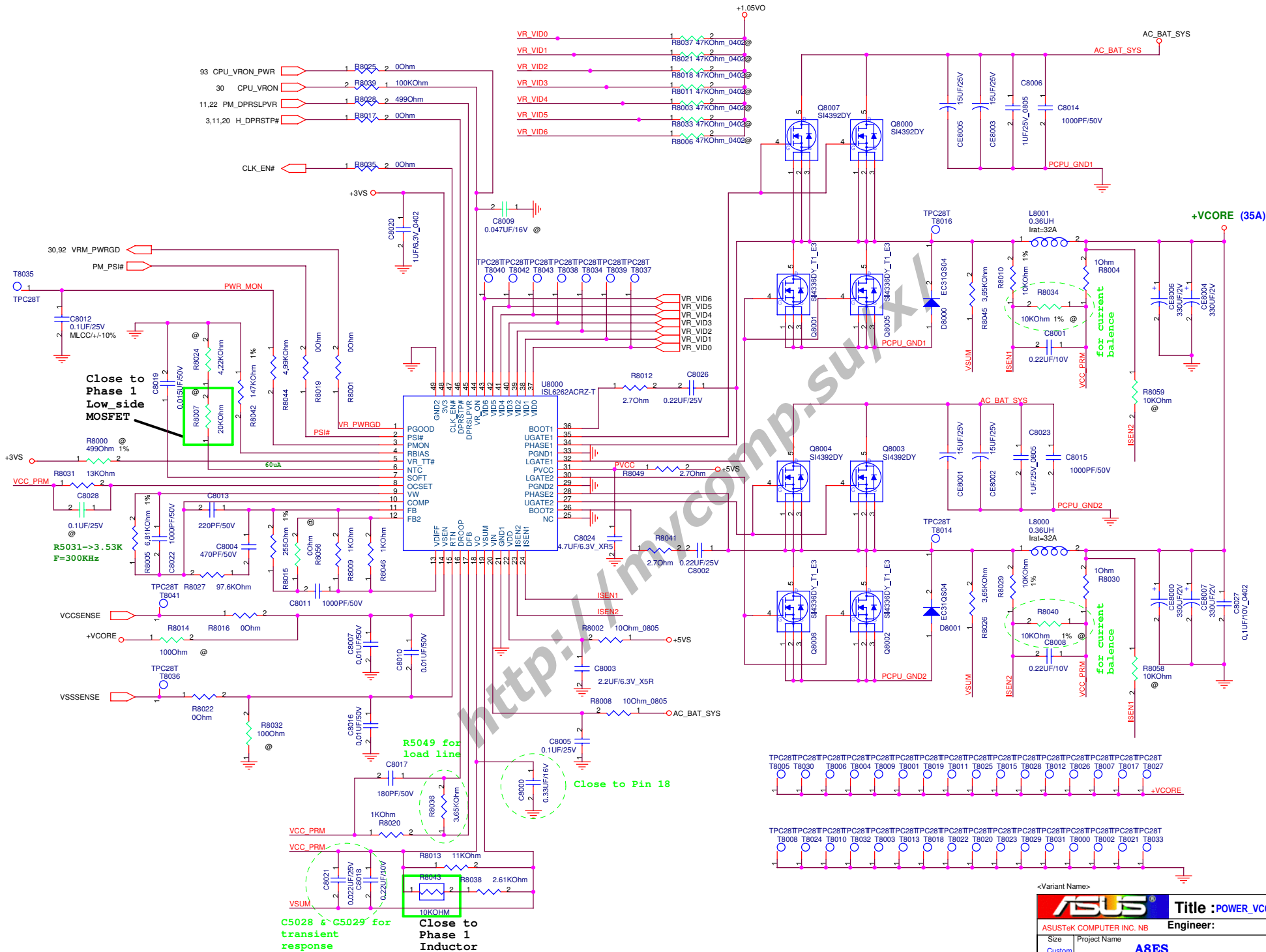
1. CPU side, per GND pin within per Via, don't share vias.
2. 0.9V_VTT_REF trace width.
3. single end trace width more than 3.5mil

SMT :

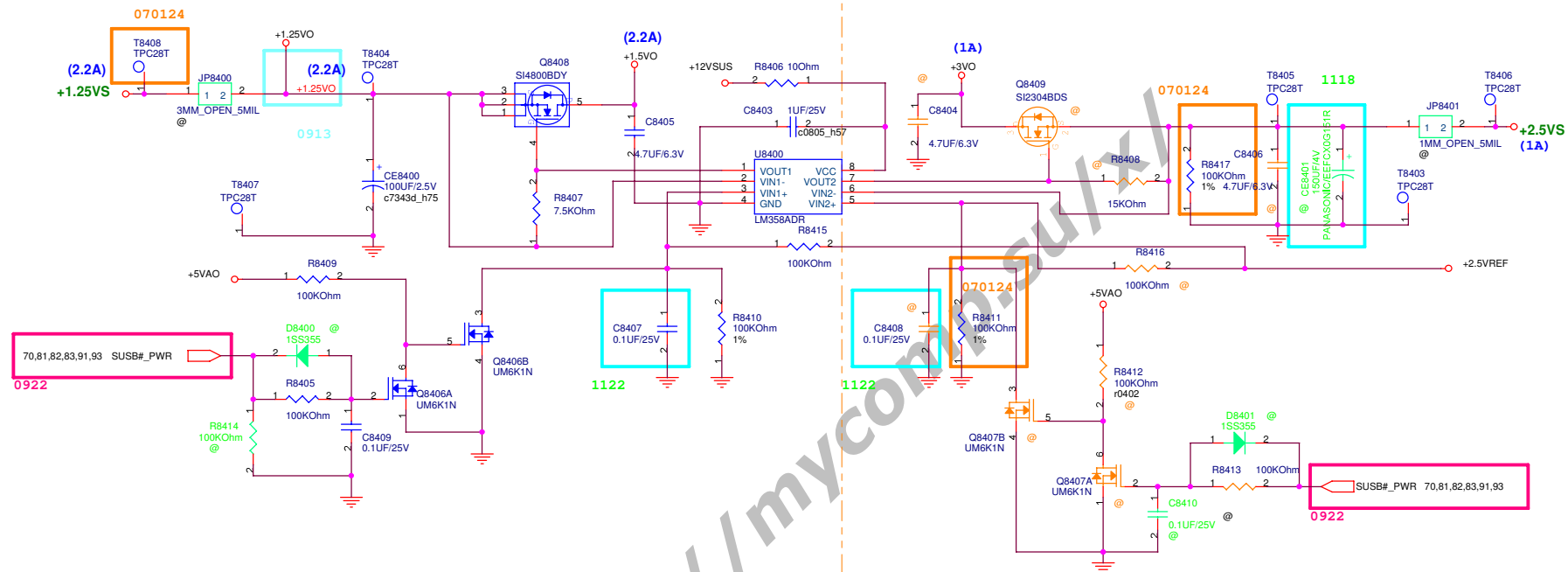
1. 開鋼板JP1, JP2

<Variant Name>

		Title : History	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	A8ES		1.0
Date: 星期一, 1月11, 2006		Sheet	79 of 94



+1.25VS & +2.5VS



<Variant Name>

ASUS		Title : POWER_I/O_+3VA & +2.5V	
<OrgName>		Engineer:	
Size	Project Name		Rev
Custom	A8ES		2.0
Date: 06.06.2007		Sheet	84 of 94

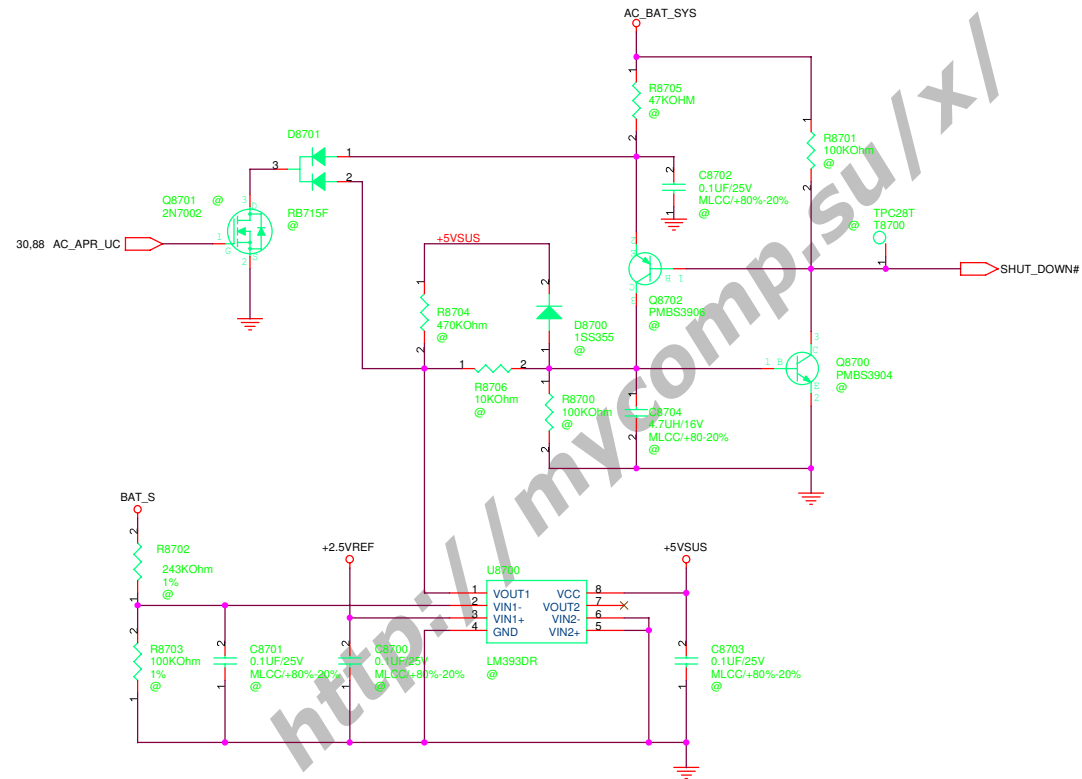
<http://mycomp.su/xl>

<Variant Name>			
		Title :POWER,VGA,CORE & RAM	
<OrgName>		Engineer:	
Size	Project Name	Rev	
C	ROSA	1.1	
Date: 星期日, 一月 25, 2007		Sheet	85 of 94

<http://mycomp.su/xl>

<Variant Name>		
		Title : N/A
<OrgName>		Engineer:
Size B	Project Name ROSA	Rev 1.1
Date: 星期四, 一月 25, 2007		Sheet 86 of 94

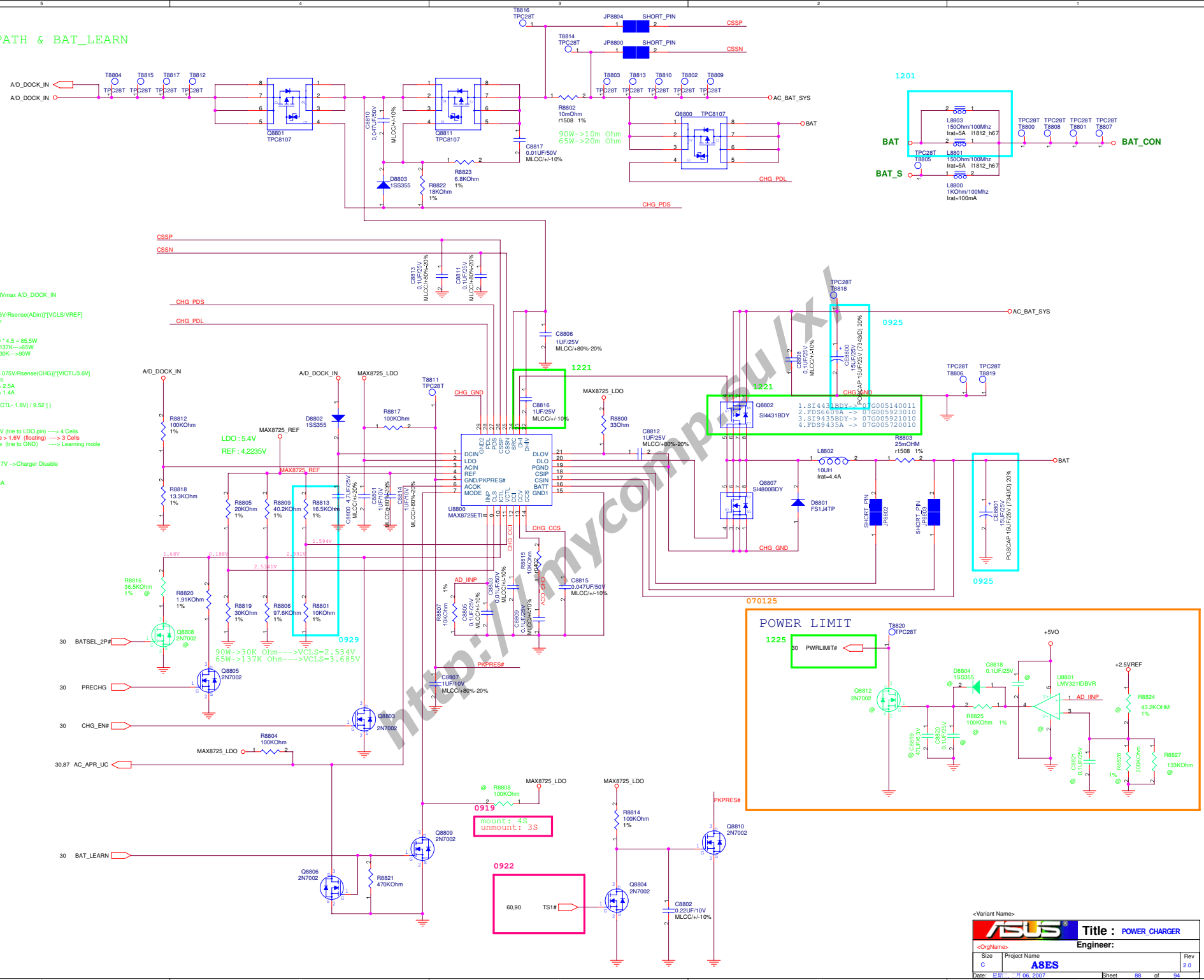
PIC only



<Variant Name>

ASUS		Title : POWER_SHUTDOWN#	
<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	2.0	
Date: 2007-06-06		Sheet 87 of 94	

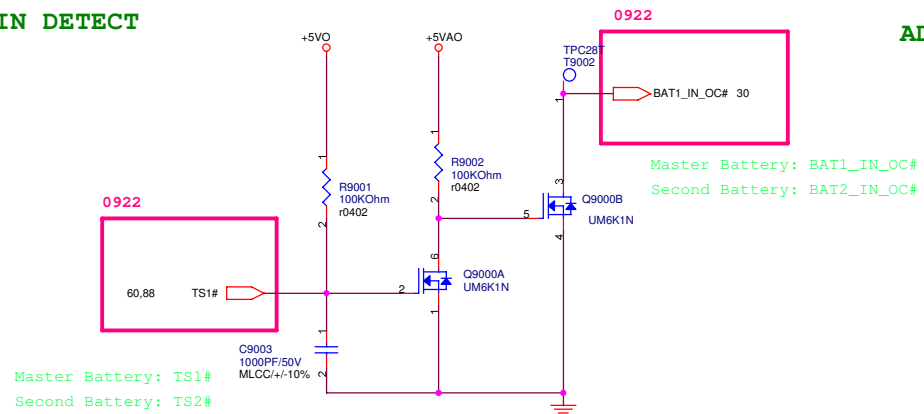
POWER PATH & BAT_LEARN



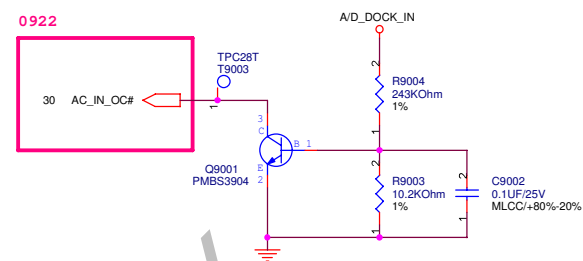
<http://mycomp.su/xl>

<Variant Name>			
		Title : N/A	
Engineer:			
<OrgName>			
Size	Project Name		Rev
Custom	ROSA		1.1
Date: 華爾街, 一月 25, 2007		Sheet 89 of 94	

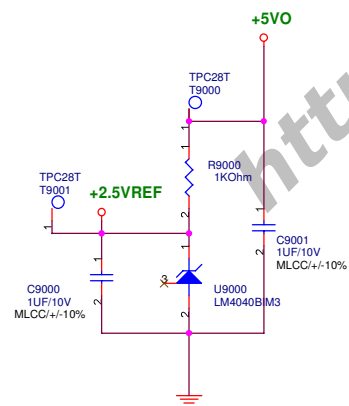
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF

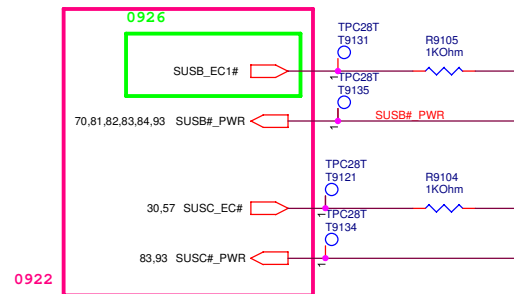
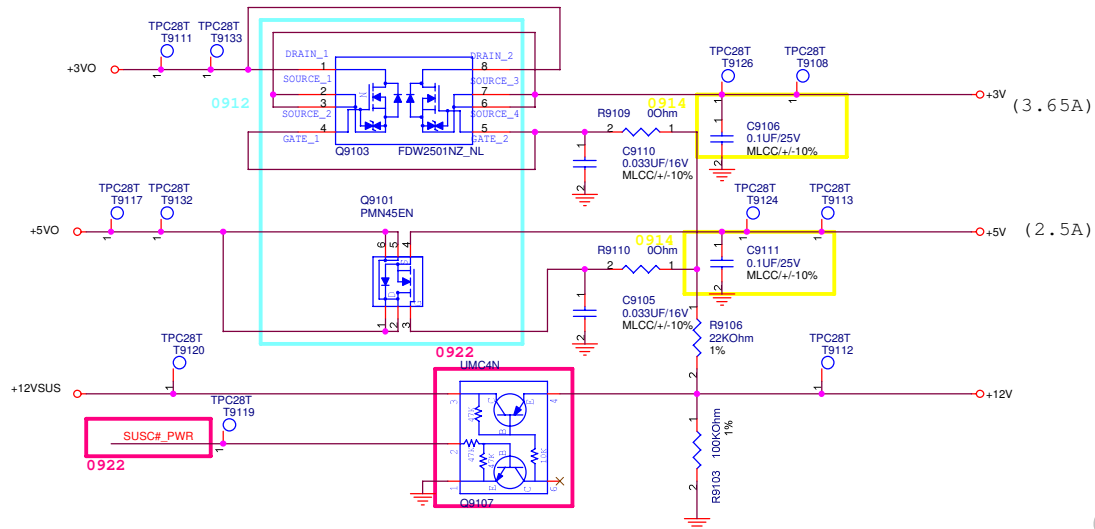


<Variant Name>

ASUS		Title : POWER_DETECT	
<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom	ASUS	2.0	
Date: 2007-06-06		Sheet	90 of 94

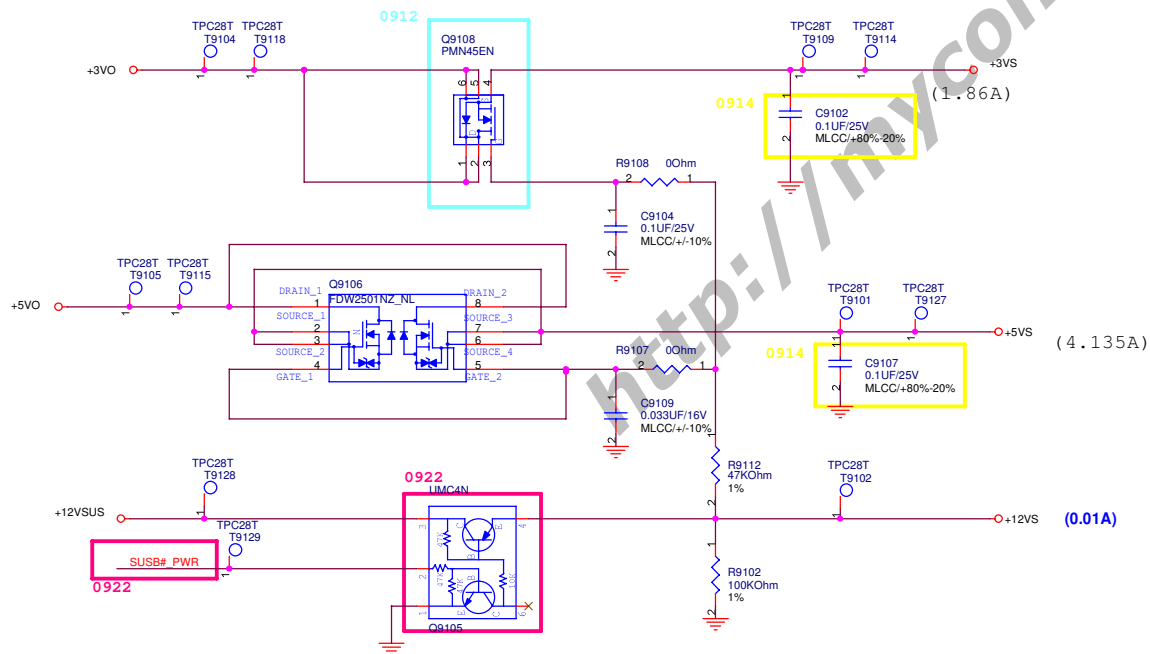
SUSC#_PWR POWER

0922



SUSB#_PWR POWER

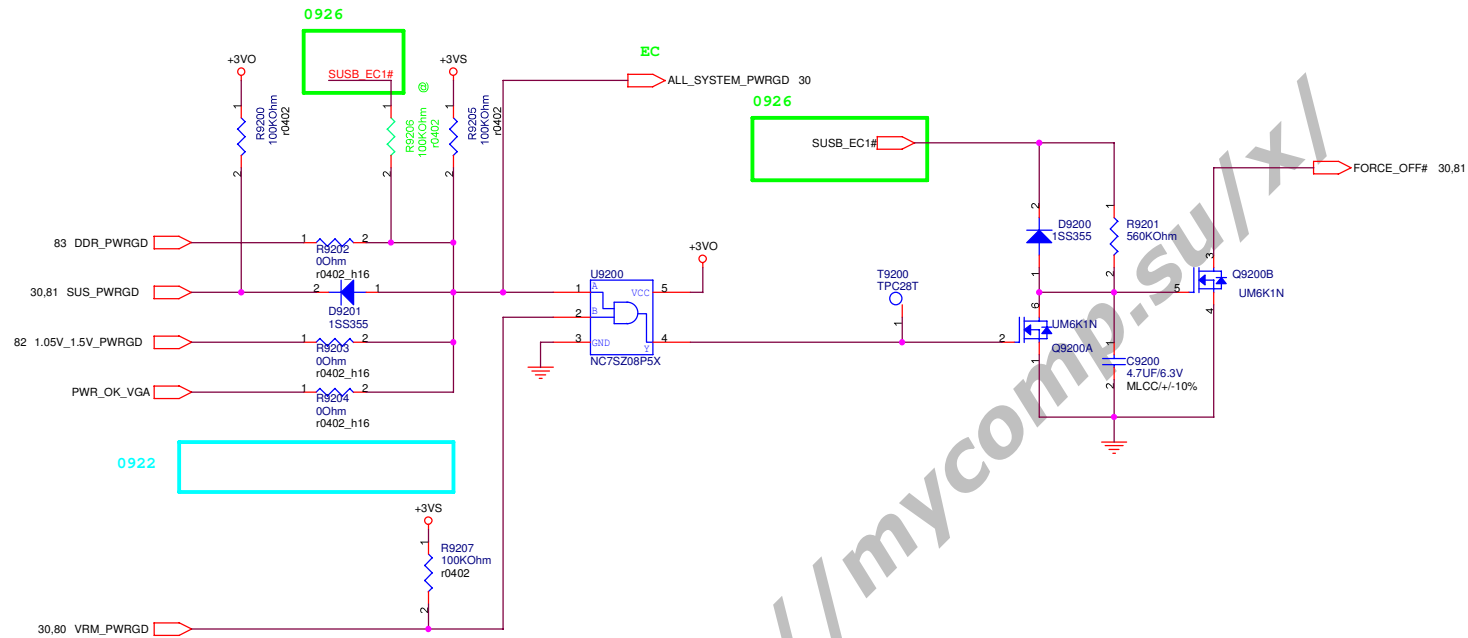
0922



<Variant Name>

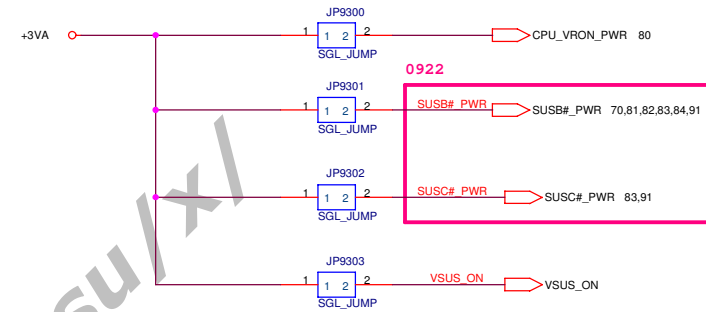
ASUS		Title : POWER_LOAD SWITCH	
<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom	ASUS	2.0	
Date: 2007-06-06	Sheet 91	of 94	

POWER GOOD DETECTOR



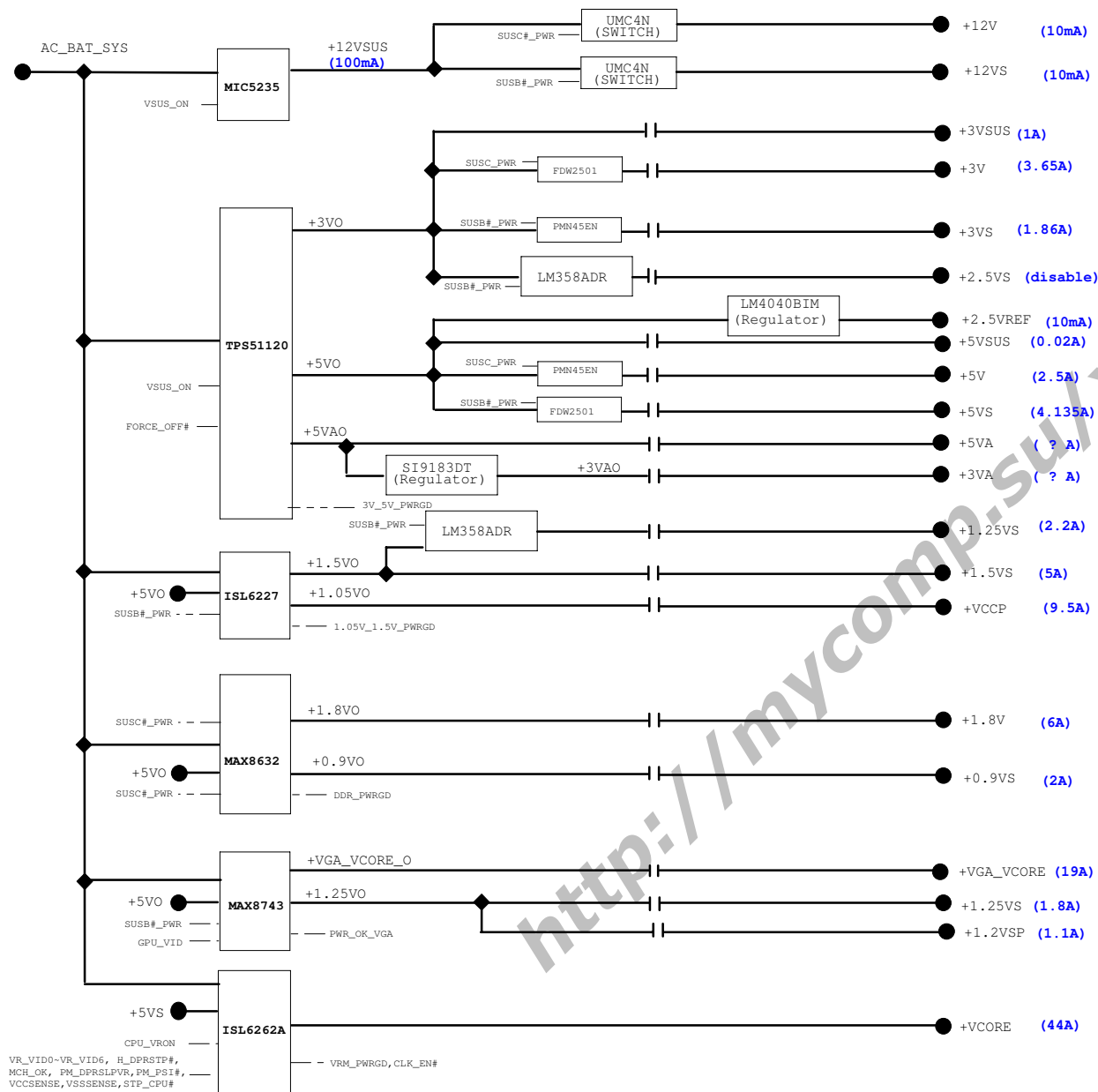


FOR POWER TEST



<Variant Name>

ASUS		Title : POWER SIGNAL	
<OrgName>		Engineer: <OrgAddr1>	
Size Custom	Project Name ASUS		Rev 2.0
Date: 2007-06-06		Sheet 93 of 94	



<Variant Name>

ASUS		Title : POWER_VCORE	
<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	2.0	
Date: 11/10/11	H 25, 2007	Sheet	94 of 94