COMPAL CONFIDENTIAL

MODEL NAME : *JAL20*
PCB NO : *LA-4043P (DA80000CV0L)*
BOM NO : *43164831L01(TPM)*
43XXXXXXX (Non TPM)

M09 Maybach UMA

uFCPGA Mobile Penryn
Intel Cantiga GM + ICH9M

2008-10-22

REV : 0.1(X00)

@ : Nopop Component
3@ : disable TPM
4@ : enable TPM

Fix Function Field

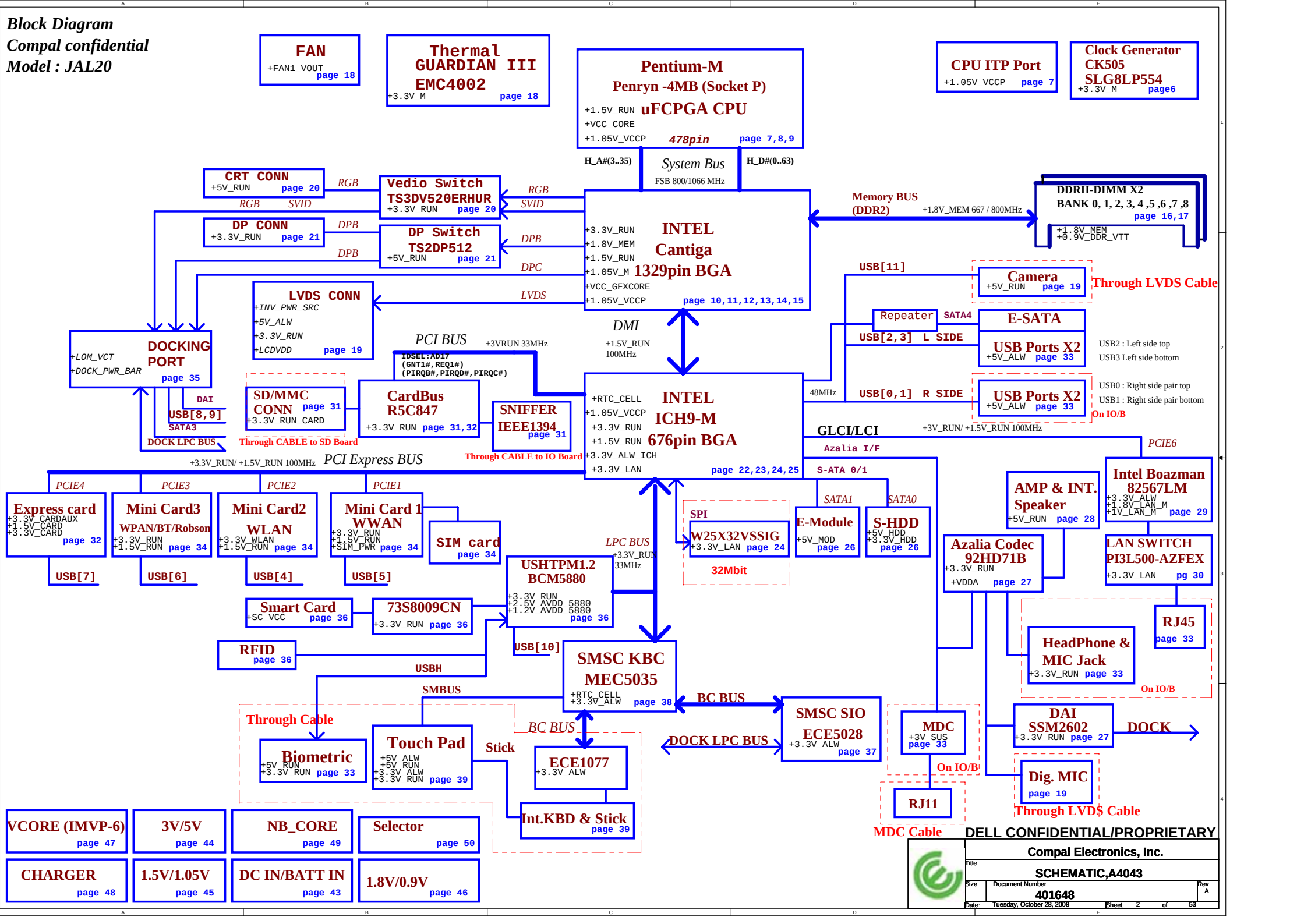
MB PCB

Part Number	Description
DA80000CV0L	PCB 03N LA-4043P REV0 M/B LOW COST

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title	SCHEMATIC,A4043	
Size	Document Number 401648	Rev A
Date: Tuesday, October 28, 2008	Sheet 1 of 53	


Block Diagram
Compal confidential
Model : JAL20
FAN
+FAN1_VOUT
page 18
Thermal
GUARDIAN III
EMC4002
+3.3V_M
page 18
Pentium-M
Penryn -4MB (Socket P)
+1.5V_RUN
uFCPGA CPU
+VCC_CORE
+1.05V_VCCP
478pin
page 7,8,9
CPU ITP Port
+1.05V_VCCP
page 7
Clock Generator
CK505
SLG8LP554
+3.3V_M
page6
H_A#(3..35)
System Bus
FSB 800/1066 MHz
H_D#(0..63)
CRT CONN
+5V_RUN
page 20
RGB
Vedio Switch
TS3DV520ERHUR
+3.3V_RUN
page 20
RGB
SVID
DP CONN
+3.3V_RUN
page 21
DPB
DP Switch
TS2DP512
+5V_RUN
page 21
DPB
DPC
LVDS CONN
+INV_PWR_SRC
+5V_ALW
+3.3V_RUN
+LCDVDD
page 19
LVDS
INTEL
Cantiga
1329pin BGA
+3.3V_RUN
+1.8V_MEM
+1.5V_RUN
+1.05V_M
+VCC_GFXCORE
+1.05V_VCCP
page 10,11,12,13,14,15
Memory BUS
(DDR2)
+1.8V_MEM 667 / 800MHz
DDRII-DIMM X2
BANK 0, 1, 2, 3, 4 ,5 ,6 ,7 ,8
page 16,17
+1.8V_MEM
+0.9V_DDR_VTT
DMI
+1.5V_RUN
100MHz
PCI BUS
+3VRUN 33MHz
IDSEL:AD17
(GNT1#,REQ1#)
(PIRQB#,PIRQD#,PIRQC#)
DOCKING
PORT
+LOM_VCT
+DOCK_PWR_BAR
page 35
DAI
USB[8,9]
SATA3
DOCK LPC BUS
SD/MMC
CONN
page 31
+3.3V_RUN_CARD
Through CABLE to SD Board
CardBus
R5C847
+3.3V_RUN
page 31,32
SNIFFER
IEEE1394
page 31
Through CABLE to IO Board
INTEL
ICH9-M
676pin BGA
+RTC_CELL
+1.05V_VCCP
+3.3V_RUN
+1.5V_RUN
+3.3V_ALW_ICH
+3.3V_LAN
page 22,23,24,25
48MHz
USB[11]
Camera
+5V_RUN
page 19
Through LVDS Cable
Repeater
SATA4
E-SATA
USB[2,3] L SIDE
USB Ports X2
+5V_ALW
page 33
USB2 : Left side top
USB3 Left side bottom
USB[0,1] R SIDE
USB Ports X2
+5V_ALW
page 33
USB0 : Right side pair top
USB1 : Right side pair bottom
On IO/B
GLCI/LCI
+3V_RUN/ +1.5V_RUN 100MHz
Azalia I/F
PCIE6
S-ATA 0/1
SATA1
SATA0
+3.3V_RUN/ +1.5V_RUN 100MHz
PCI Express BUS
PCIE4
PCIE3
PCIE2
PCIE1
Express card
+3.3V_CARDAUX
+1.5V_CARD
+3.3V_CARD
page 32
Mini Card3
WPAN/BT/Robson
+3.3V_RUN
+1.5V_RUN
page 34
Mini Card2
WLAN
+3.3V_WLAN
+1.5V_RUN
page 34
Mini Card 1
WWAN
+3.3V_RUN
+1.5V_RUN
+SIM_PWR
page 34
SIM card
page 34
USB[7]
USB[6]
USB[4]
USB[5]
SPI
W25X32VSSIG
+3.3V_LAN
page 24
32Mbit
E-Module
+5V_MOD
page 26
S-HDD
+5V_HDD
+3.3V_HDD
page 26
AMP & INT.
Speaker
+5V_RUN
page 28
Intel Boazman
82567LM
+3.3V_ALW
+1.8V_LAN_M
+1V_LAN_M
page 29
Azalia Codec
92HD71B
+3.3V_RUN
+VDDA
page 27
LAN SWITCH
PI3L500-AZFEX
+3.3V_LAN
pg 30
RJ45
page 33
HeadPhone &
MIC Jack
+3.3V_RUN page 33
On IO/B
LPC BUS
+3.3V_RUN
33MHz
USHTPM1.2
BCM5880
+3.3V_RUN
+2.5V_AVDD_5880
+1.2V_AVDD_5880
page 36
Smart Card
+SC_VCC
page 36
73S8009CN
+3.3V_RUN page 36
RFID
page 36
USB[10]
USBH
SMBUS
SMSC KBC
MEC5035
+RTC_CELL
+3.3V_ALW
page 38
BC BUS
SMSC SIO
ECE5028
+3.3V_ALW
page 37
DOCK LPC BUS
MDC
+3V_SUS
page 33
On IO/B
DAI
SSM2602
+3.3V_RUN page 27
DOCK
Dig. MIC
page 19
Through LVDS Cable
Through Cable
Biometric
+5V_RUN
+3.3V_RUN page 33
Touch Pad
+5V_ALW
+5V_RUN
+3.3V_ALW
+3.3V_RUN page 39
Stick
BC BUS
ECE1077
+3.3V_ALW
Int.KBD & Stick
page 39
RJ11
MDC Cable
VCORE (IMVP-6)
page 47
3V/5V
page 44
NB_CORE
page 49
Selector
page 50
CHARGER
page 48
1.5V/1.05V
page 45
DC IN/BATT IN
page 43
1.8V/0.9V
page 46
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Title
SCHEMATIC,A4043
Size
Document Number
401648
Rev
A
Date: Tuesday, October 28, 2008
Sheet 2 of 53

POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

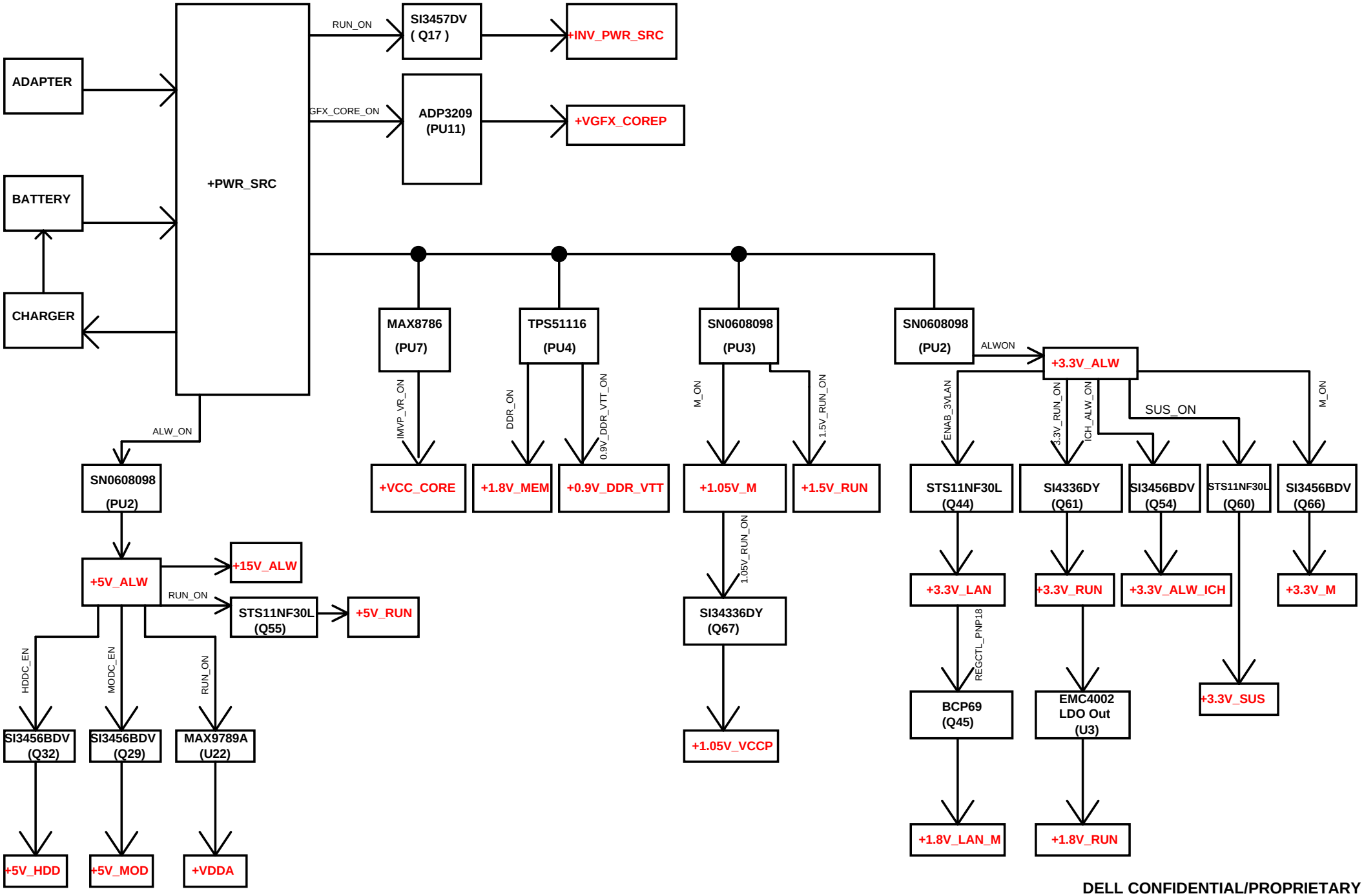
power plane / State	+15V_ALW +5V_ALW +3.3V_ALW_ICH +3.3V_RTC_LDO	+3.3V_SUS +1.8V_MEM	+5V_RUN +3.3V_RUN +2.5V_RUN +1.5V_RUN +0.9V_DDR_VTT +VCC_GFXCORE +VCC_CORE +1.05V_VCCP	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C847	AD17	REQ#1 / GNT#1	PIRQ[B..D]

	USB PORT#	DESTINATION
ICH9-M	0	JUSB1 (Ext Right Side Top)
	1	JUSB1 (Ext Right Side Bottom)
	2	JESA1 (Ext Left Side Top)
	3	JESA1 (Ext Left Side Bottom)
	4	WLAN
	5	WWAN
	6	WPAN
	7	Card Bus/Express card
	8	DOCKING
	9	DOCKING
	10	USH->BIO
	11	Camera

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 BT/UWB
Lane 4	EXPRESS CARD
Lane 5	None
Lane 6	10/100/1G LAN



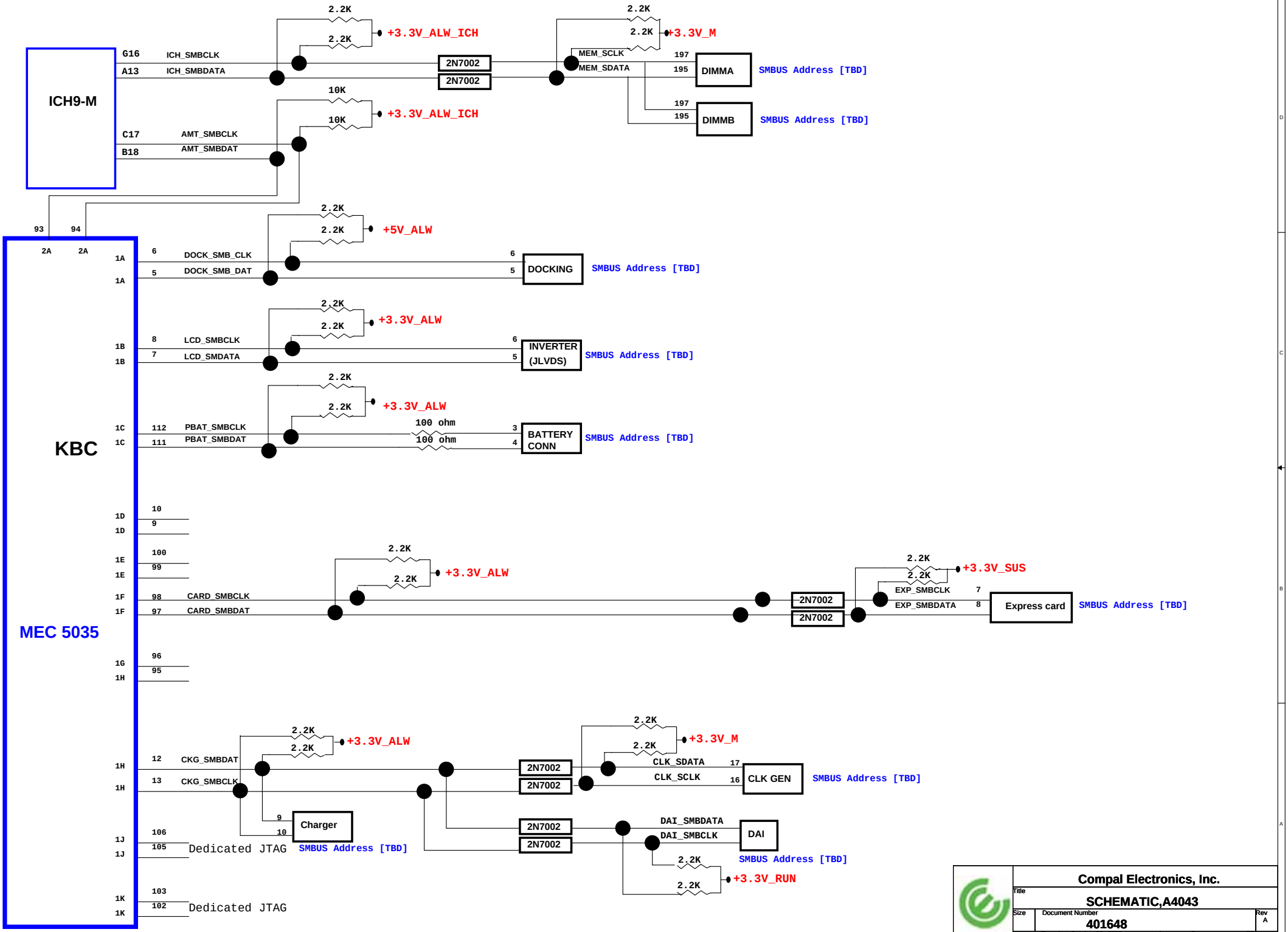
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

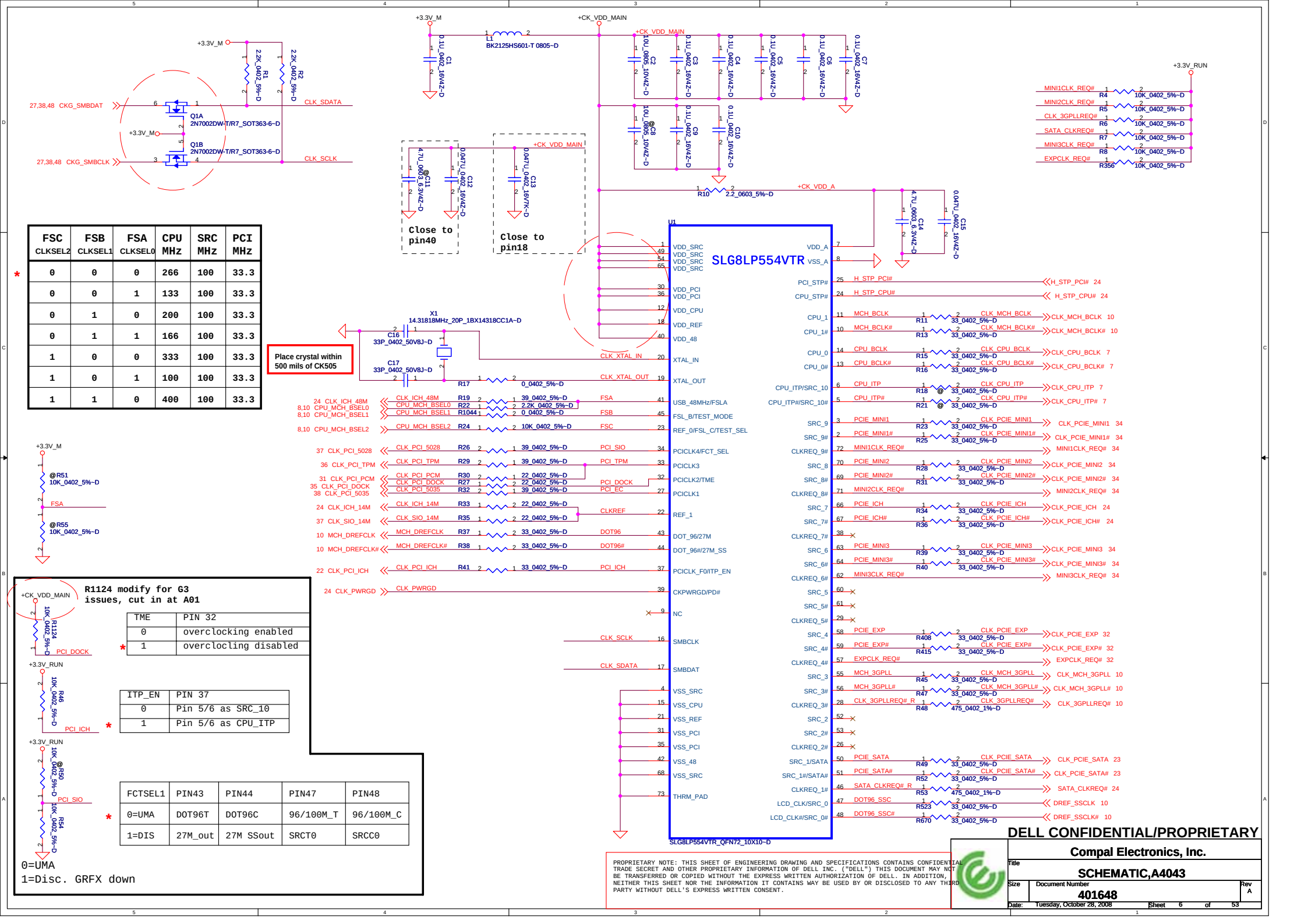
Title: SCHEMATIC,A4043

Size | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 4 of 53



Compal Electronics, Inc.	
Title	SCHEMATIC,A4043
Size	Document Number 401648 Rev A
Date: Tuesday, October 28, 2008	Sheet 5 of 53



FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
* 0	0	0	266	100	33.3
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3

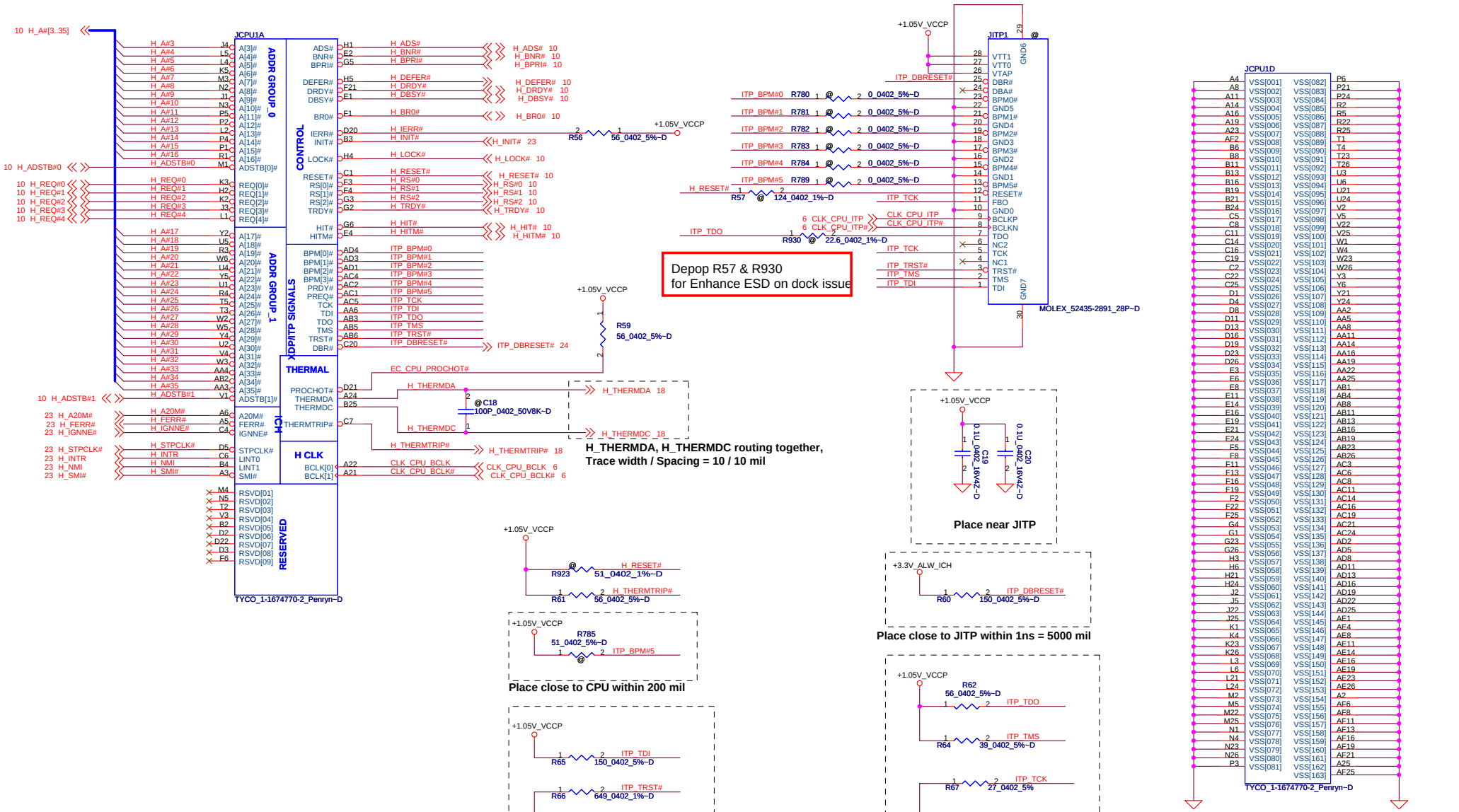
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SCHEMATIC,A4043

Size: | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 6 of 53

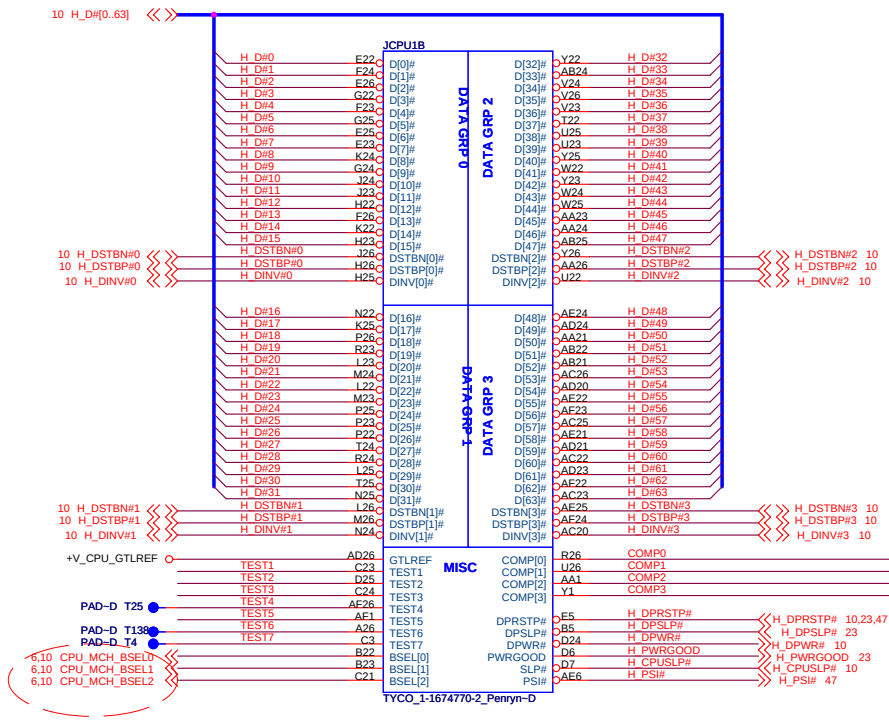


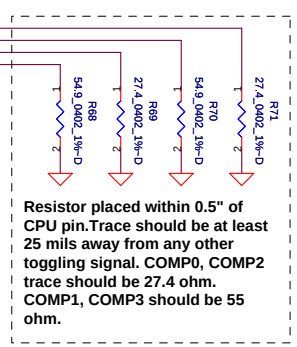
Compal Electronics, Inc.

Title: SCHEMATIC,A4043

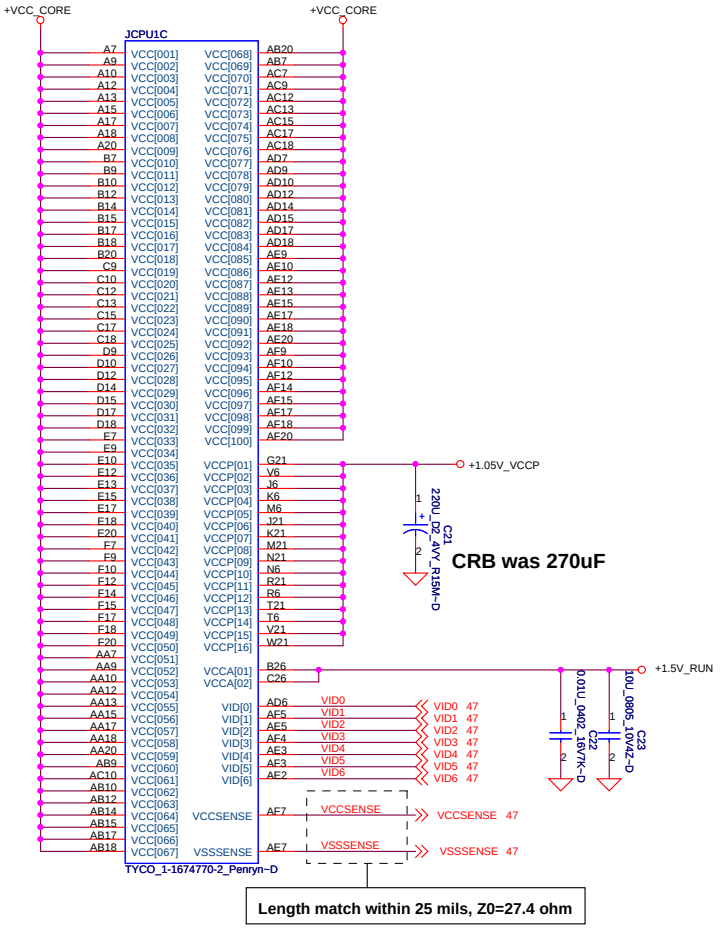
Size | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 7 of 53

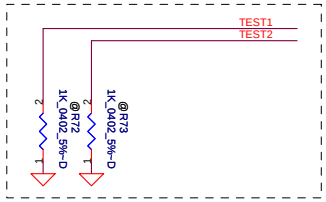


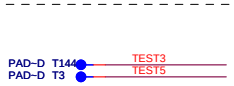


Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP0, COMP2 trace should be 27.4 ohm. COMP1, COMP3 should be 55 ohm.



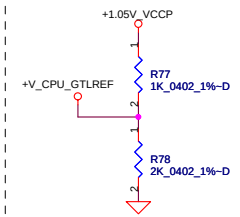
Length match within 25 mils, Z0=27.4 ohm





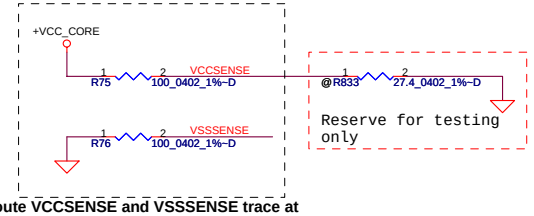
For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0



Layout close CPU PIN AD26 55 ohm, 0.5 inch (max)

Place R75 and R76 near CPU



Route VCCSENSE and VSSSENSE trace at 27.4 ohms, 7 mils spacing and the placement should be within 1 inch (max)

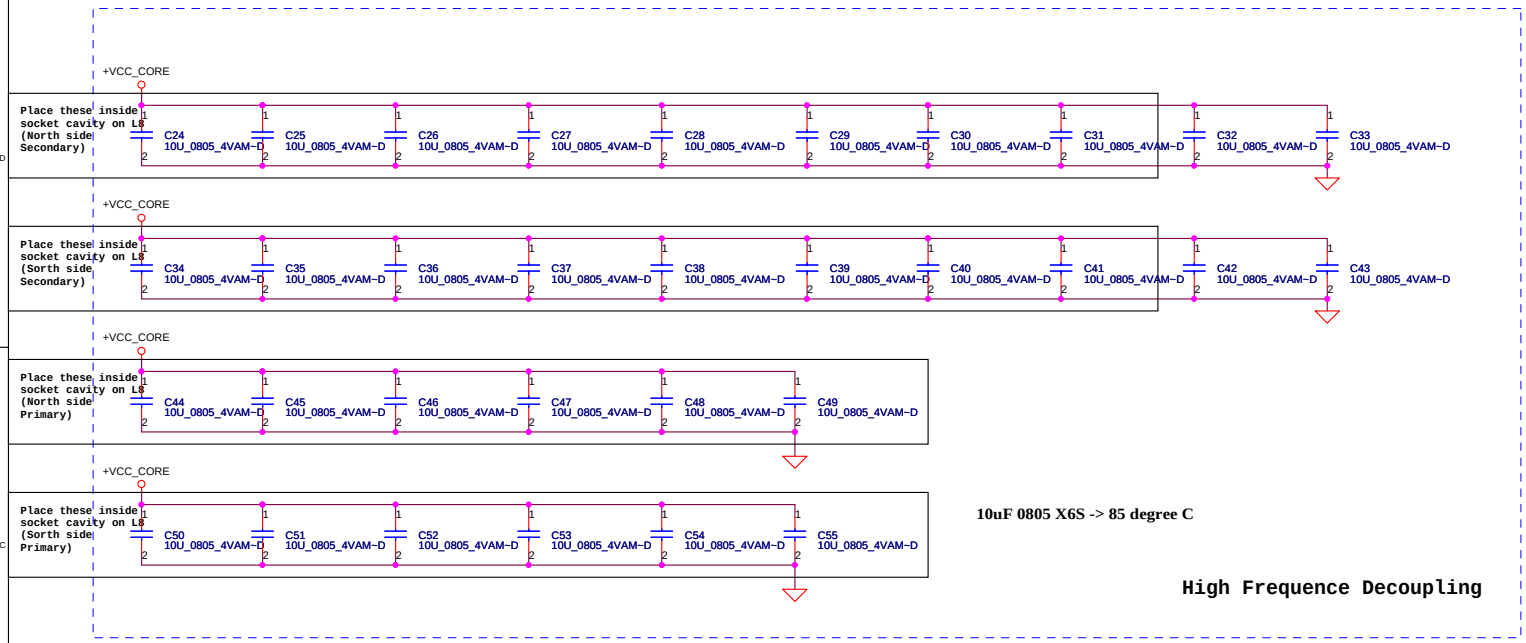
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SCHEMATIC,A4043

Size | Document Number: 401648 | Rev: A

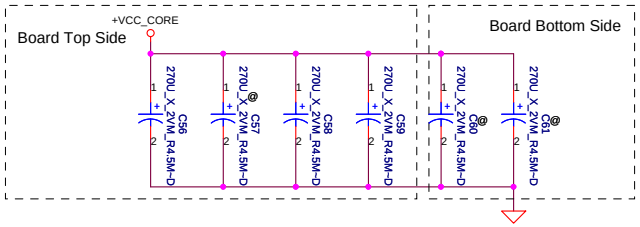
Date: Tuesday, October 28, 2008 | Sheet 8 of 53



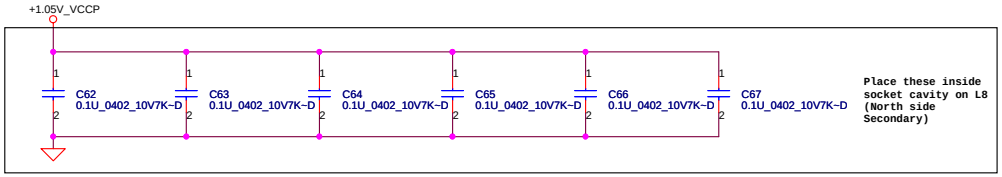
10uF 0805 X6S -> 85 degree C

High Frequence Decoupling

Near VCORE regulator.



ESR <= 1.5m ohm
Capacitor > 1320uF

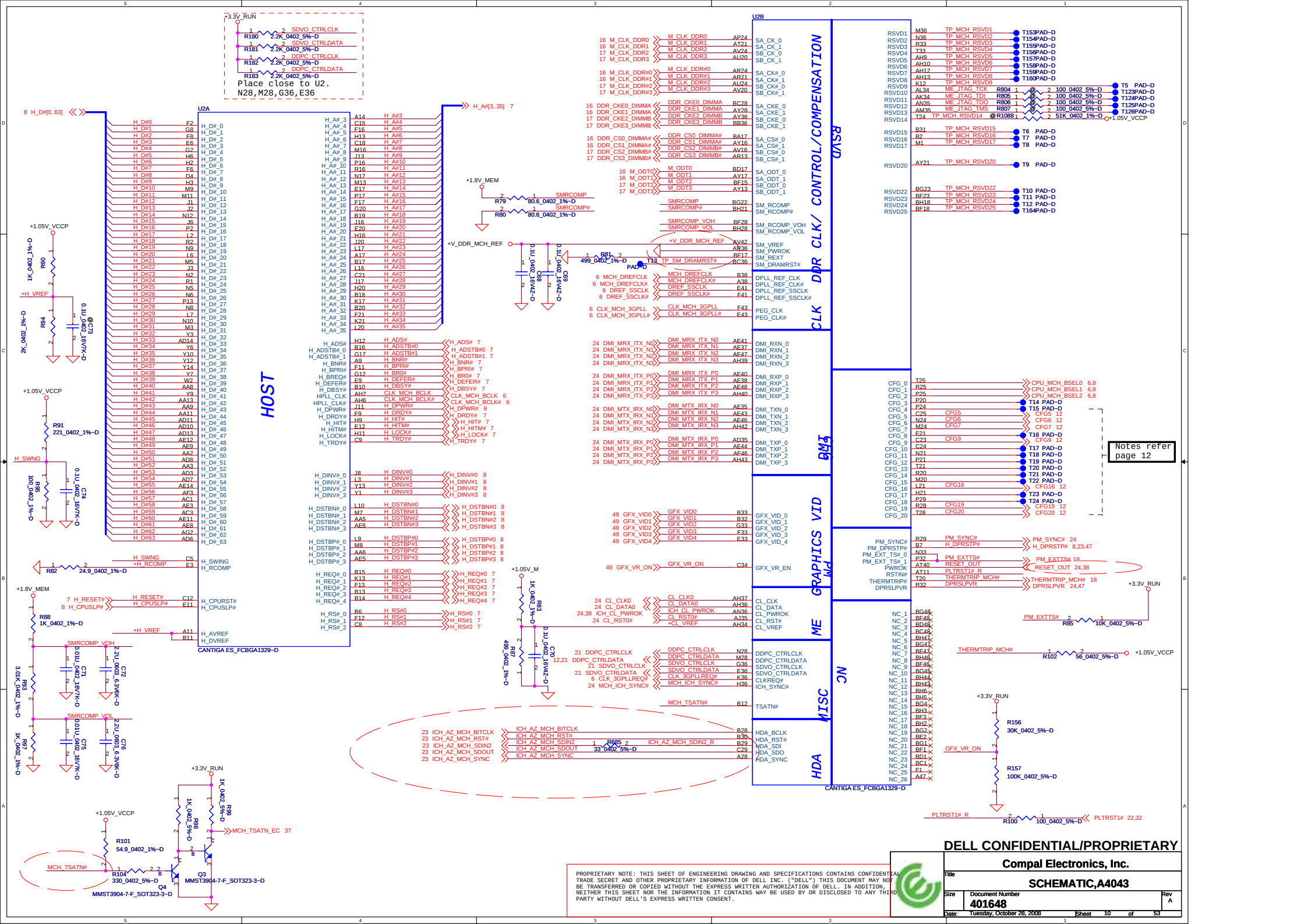


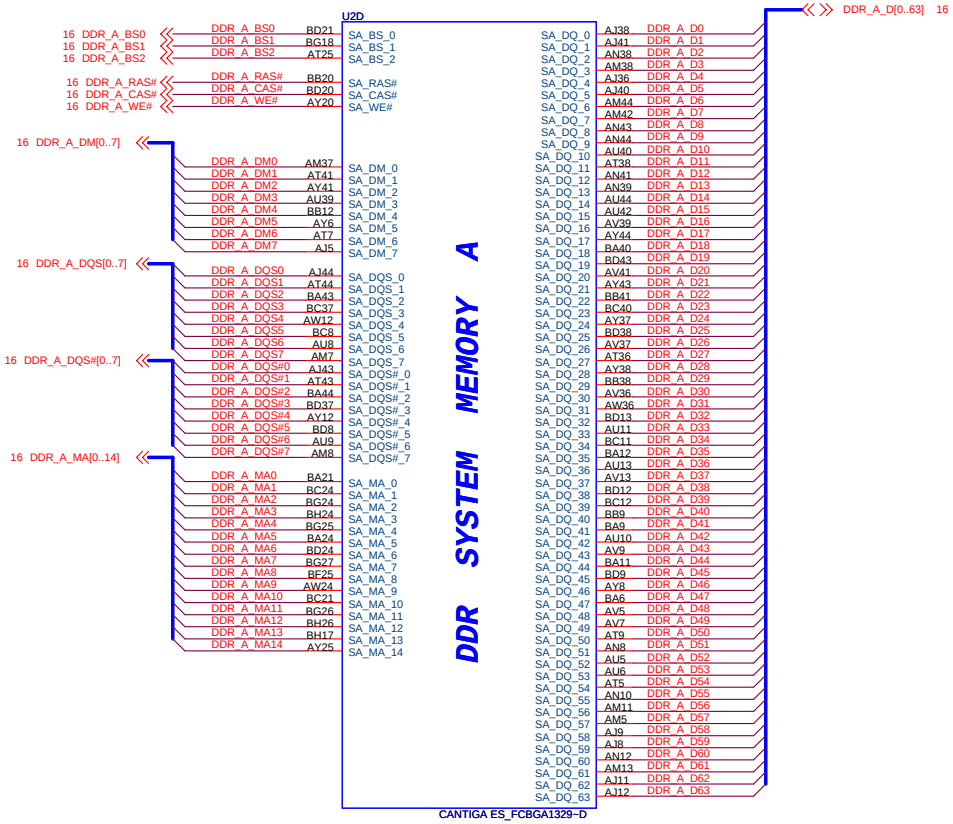
Compal Electronics, Inc.

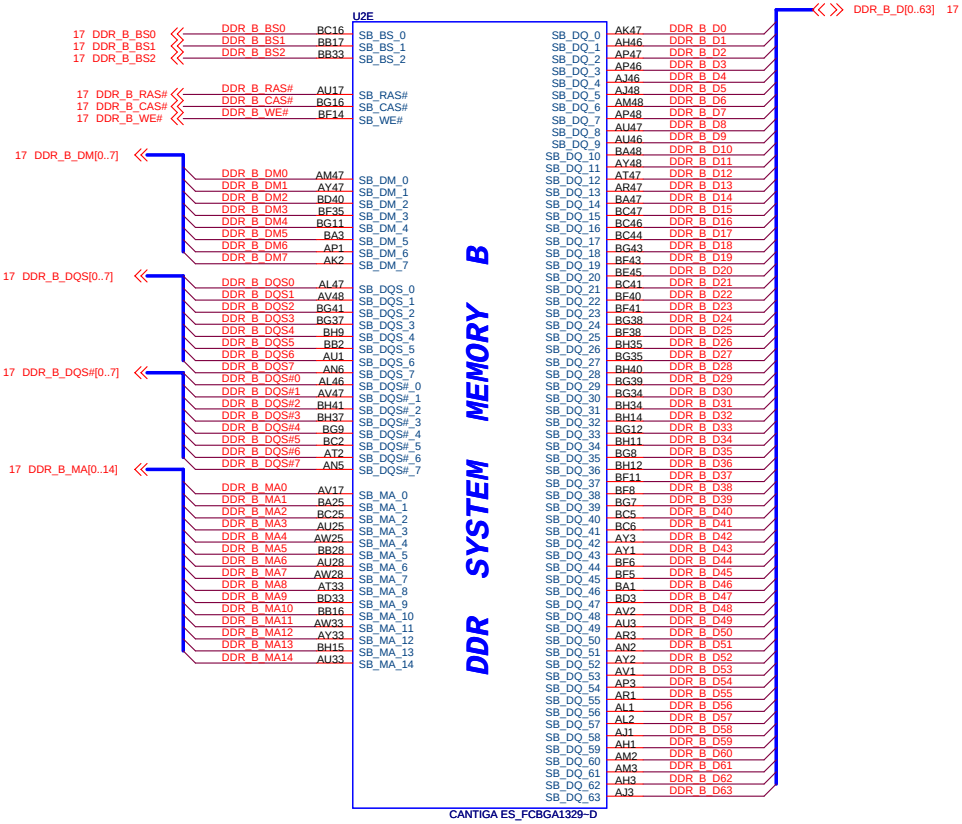
Title: SCHEMATIC,A4043

Size | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 9 of 53


+3.3V_RUN
R180 2.2K_0402_5%~D SDVO_CTRLCLK
R181 2.2K_0402_5%~D SDVO_CTRLDATA
R182 2.2K_0402_5%~D DDPC_CTRLCLK
R183 2.2K_0402_5%~D DDPC_CTRLDATA
Place close to U2.
N28,M28,G36,E36
U2A
HOST
U2B
DDR CLK/ CONTROL/COMPENSATION
RSVD
CLK
DMI
GRAPHICS VID
PWR
ME
NC
MISC
HDA
CANTIGA ES_FCBGA1329~D
Notes refer page 12
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
SCHEMATIC,A4043
401648
Tuesday, October 28, 2008
Sheet 10 of 53



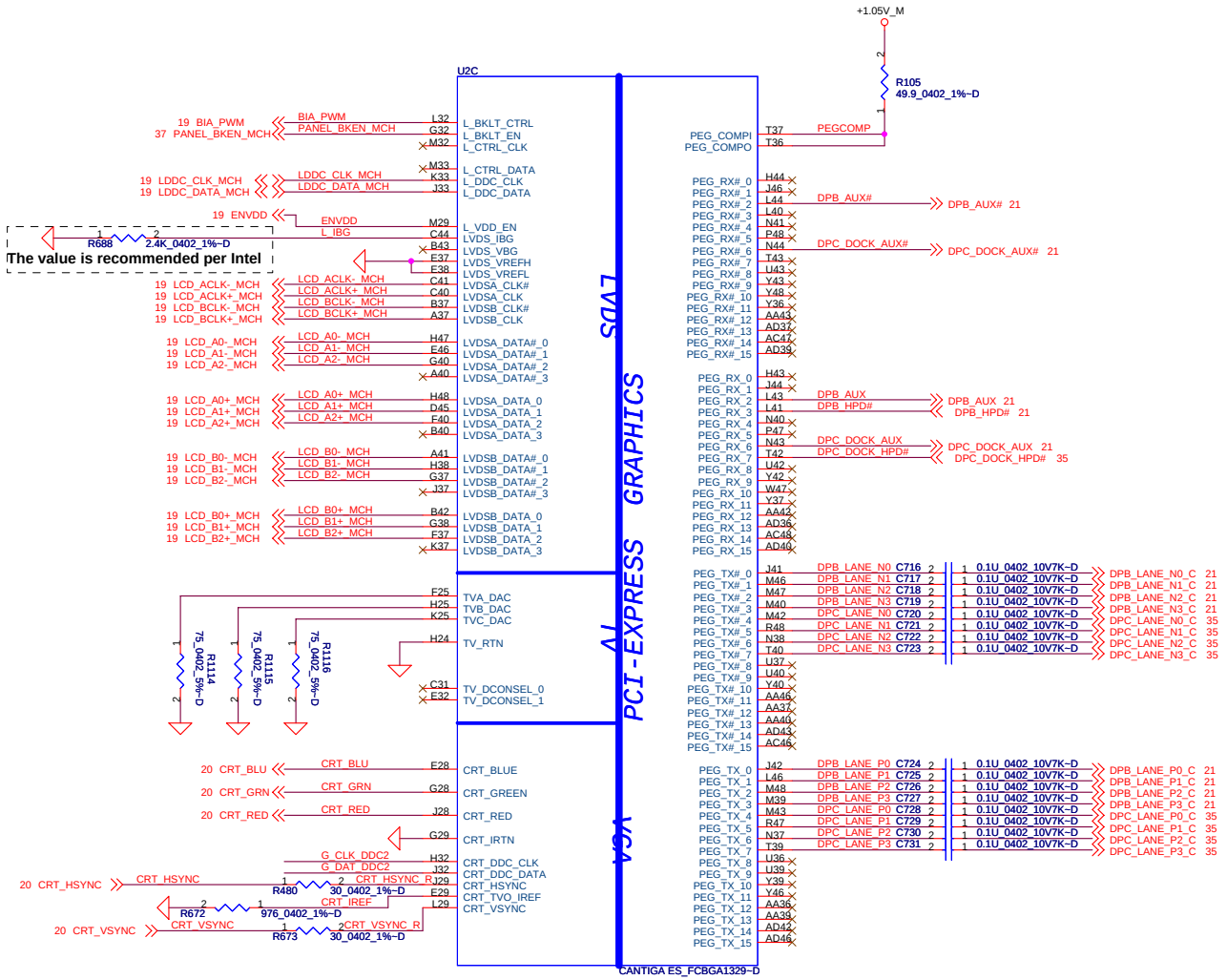


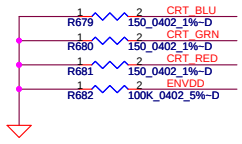
Compal Electronics, Inc.

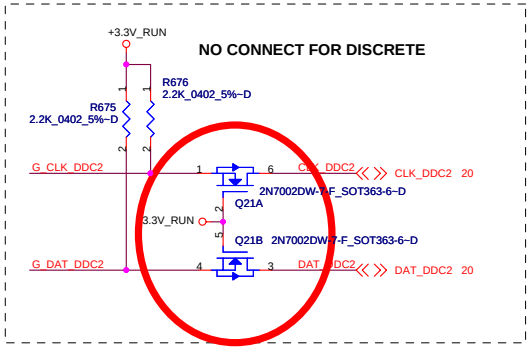
Title: SCHEMATIC,A4043

Size | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 11 of 53

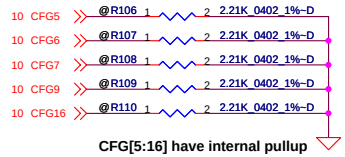


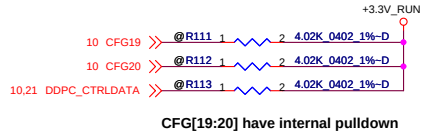




Strap Pin Table

CFG5	DMI X2 Select	Low = DMI x 2 High = DMI x 4 (Default)
CFG6	iTPM Host Interface	Low = iTPM enable High = iTPM disable(Defult)
CFG7	Management Engine Crypto Strap	Low = TLS cipher suite with no confidentiality High = TLS cipher suite with confidentiality(Default)
CFG9	PCI Express Graphic Lane	Low = Reverse Lane High = Normal Operation(Default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (default) High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CRTL_DATA		Low=No SDVO Device Present (default) High=SDVO Device Present
DDPC_CTRLDATA		Low=DisplayPort disabled (default) High=DisplayPort device present





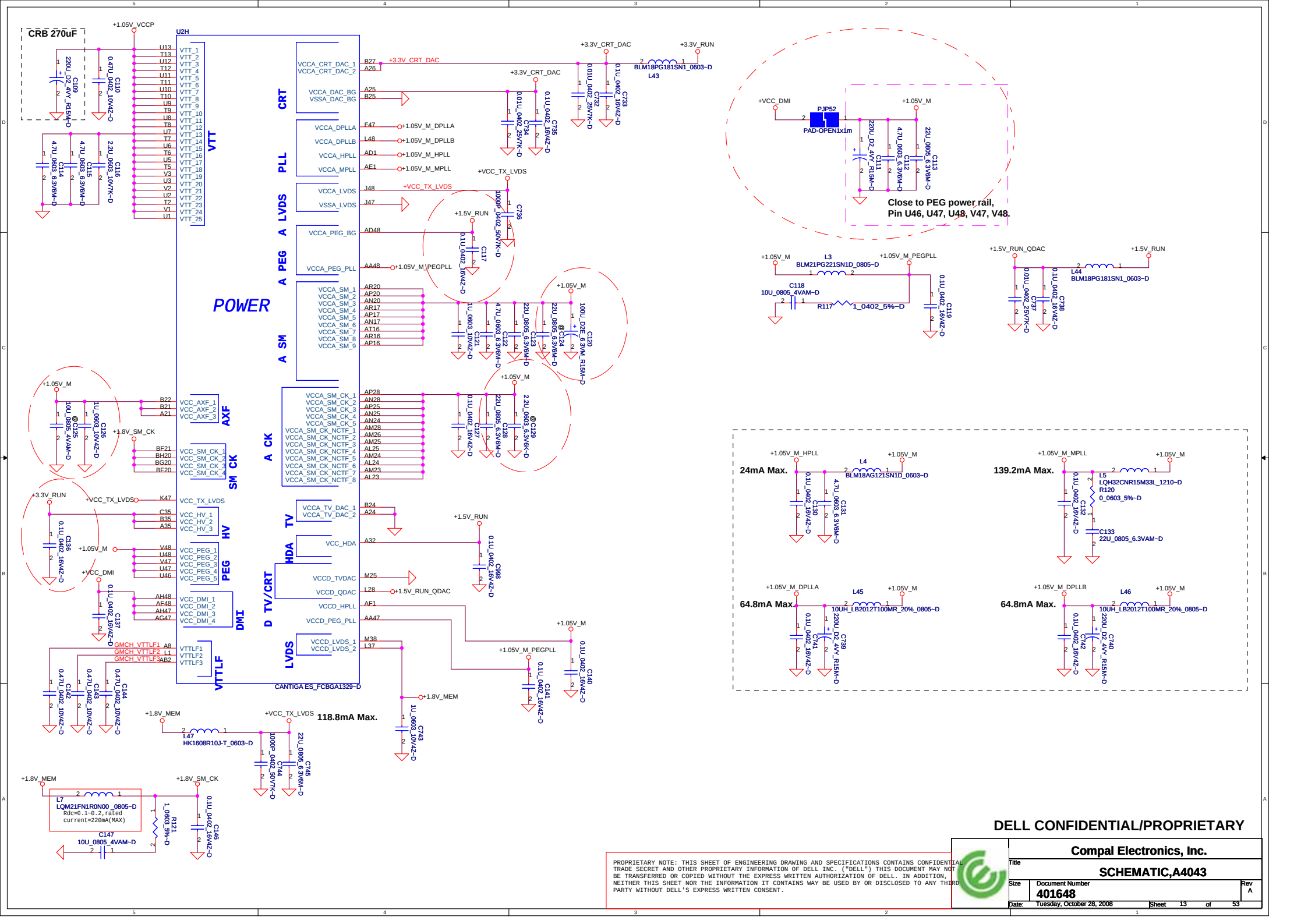
DELL CONFIDENTIAL/PROPRIETARY

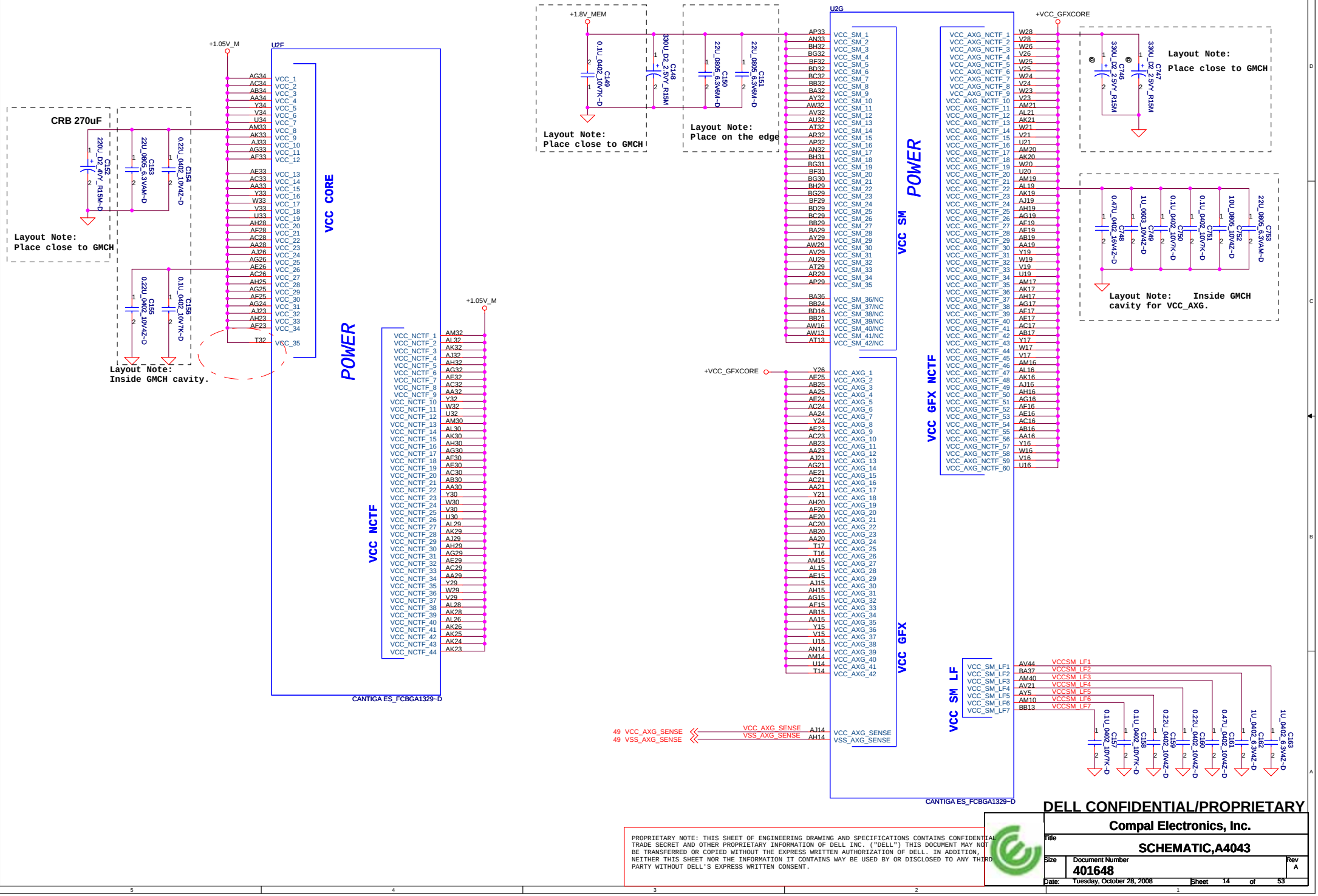
Compal Electronics, Inc.

Title: SCHEMATIC,A4043

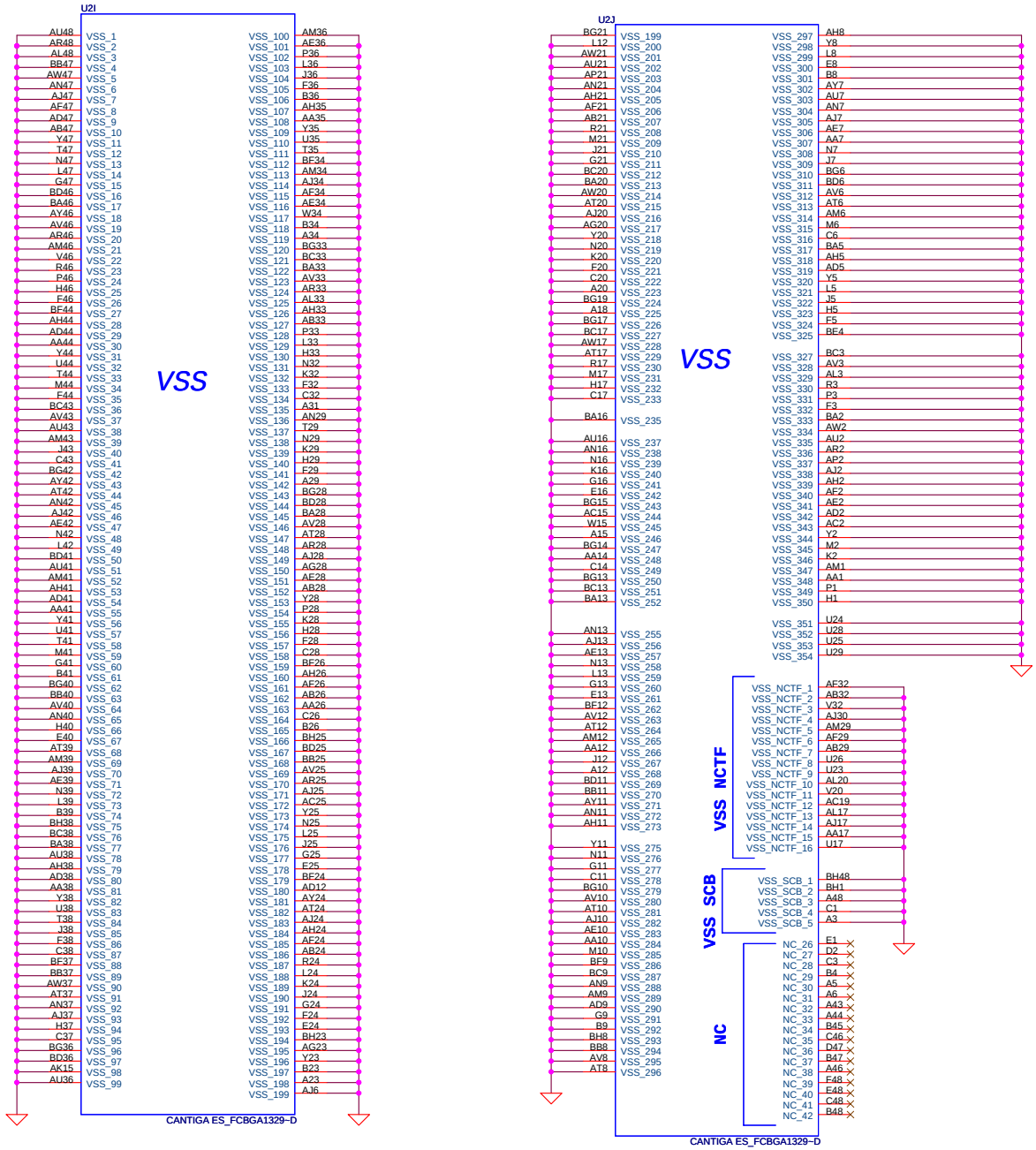
Size | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 12 of 53


POWER
CRB 270uF
+1.05V_VCCP
U2H
VTT
CRT
PLL
A LVDS
A PEG
A SM
A CK
SM CK
AXF
HV
PEG
DMI
D TV/CRT
TV
HDA
LVDS
VTTLF
CANTIGA ES_FCBGA1329~D
+3.3V_CRT_DAC
+3.3V_RUN
+VCC_TX_LVDS
+1.5V_RUN
+1.05V_M
+1.8V_SM_CK
+VCC_DMI
+1.8V_MEM
+1.05V_M_PEGPLL
+1.5V_RUN_QDAC
118.8mA Max.
Close to PEG power rail,
Pin U46, U47, U48, V47, V48.
24mA Max.
139.2mA Max.
64.8mA Max
64.8mA Max.
DELL CONFIDENTIAL/PROPRIETARY
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.
Compal Electronics, Inc.
Title
SCHEMATIC,A4043
Size
Document Number
401648
Rev
A
Date: Tuesday, October 28, 2008
Sheet 13 of 53



PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

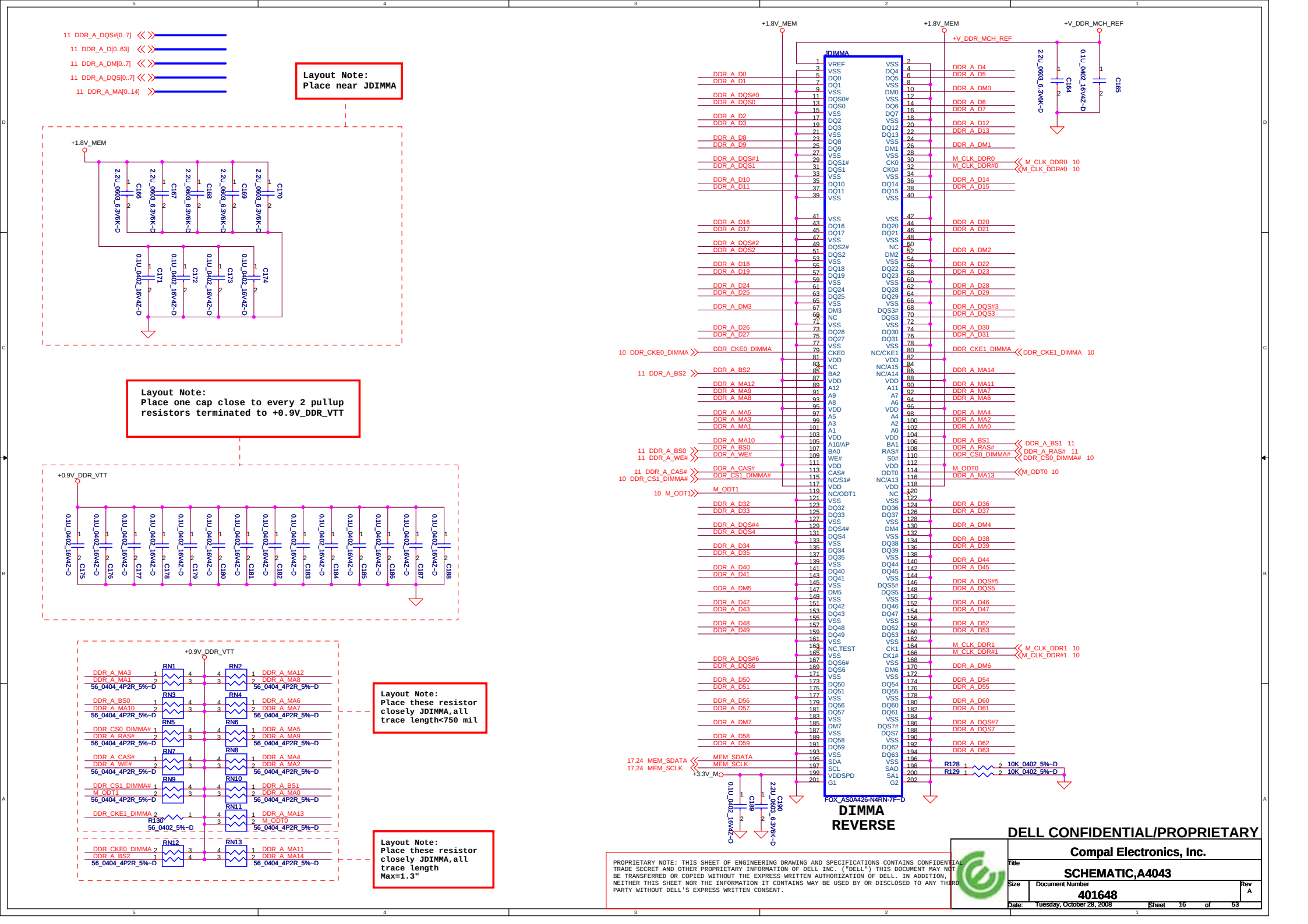


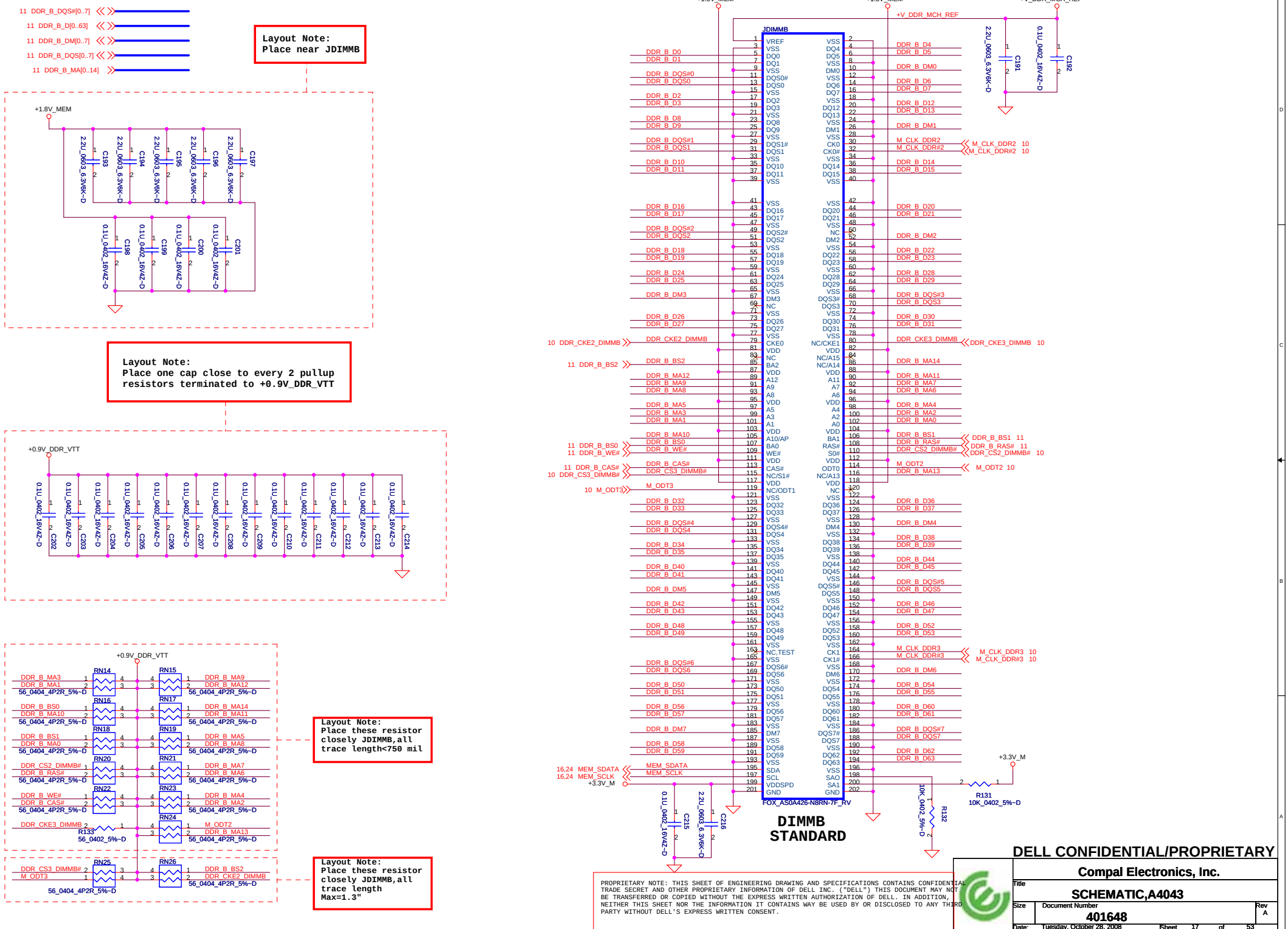
Compal Electronics, Inc.

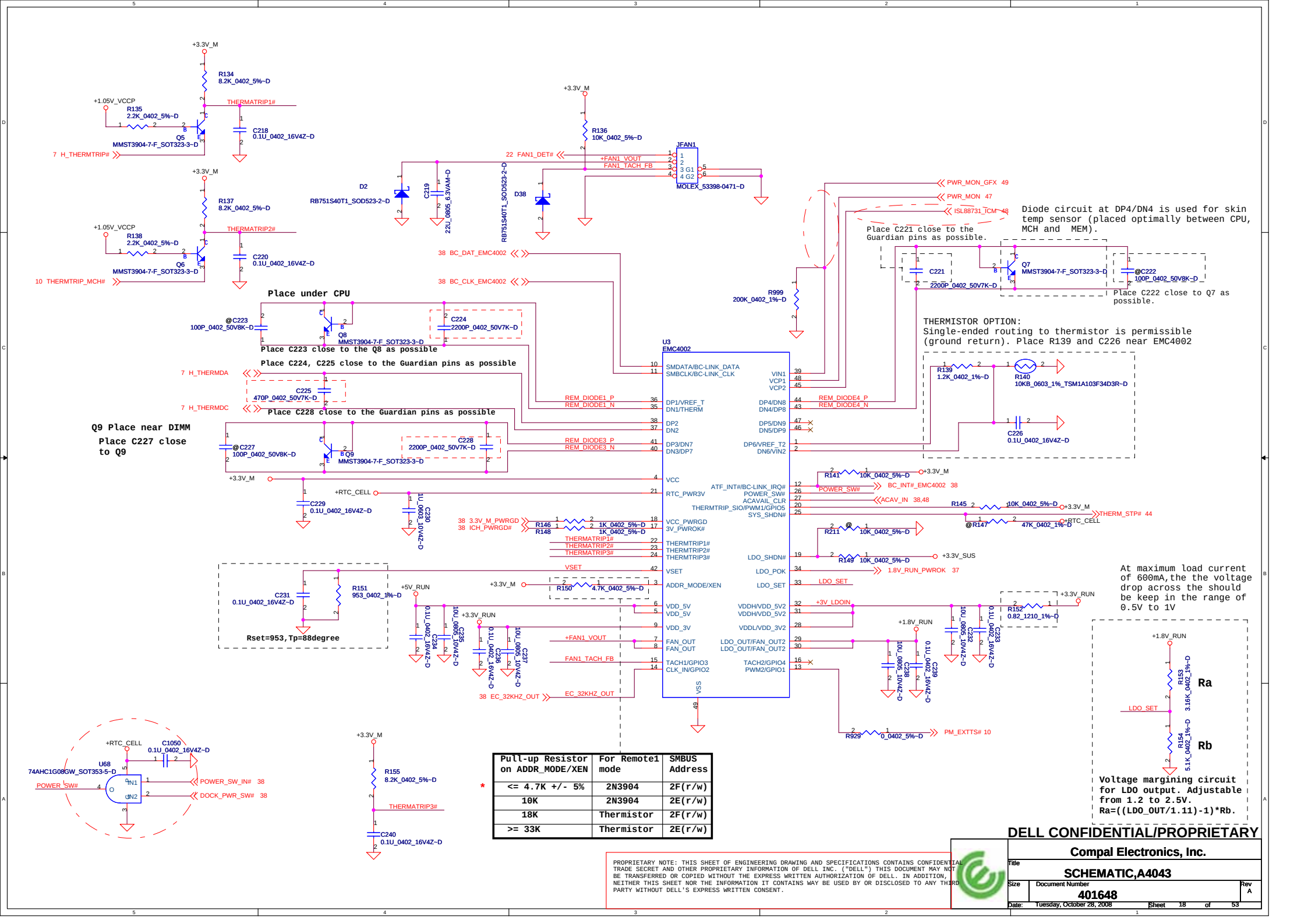
Title: SCHEMATIC,A4043

Size | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 15 of 53


11 DDR_A_DQS#[0..7]
11 DDR_A_D[0..63]
11 DDR_A_DM[0..7]
11 DDR_A_DQS[0..7]
11 DDR_A_MA[0..14]
Layout Note:
Place near JDIMMA
+1.8V_MEM
C166 2.2U_0603_6.3V6K~D
C167 2.2U_0603_6.3V6K~D
C168 2.2U_0603_6.3V6K~D
C169 2.2U_0603_6.3V6K~D
C170 2.2U_0603_6.3V6K~D
C171 0.1U_0402_16V4Z~D
C172 0.1U_0402_16V4Z~D
C173 0.1U_0402_16V4Z~D
C174 0.1U_0402_16V4Z~D
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT
+0.9V_DDR_VTT
C175 0.1U_0402_16V4Z~D
C176 0.1U_0402_16V4Z~D
C177 0.1U_0402_16V4Z~D
C178 0.1U_0402_16V4Z~D
C179 0.1U_0402_16V4Z~D
C180 0.1U_0402_16V4Z~D
C181 0.1U_0402_16V4Z~D
C182 0.1U_0402_16V4Z~D
C183 0.1U_0402_16V4Z~D
C184 0.1U_0402_16V4Z~D
C185 0.1U_0402_16V4Z~D
C186 0.1U_0402_16V4Z~D
C187 0.1U_0402_16V4Z~D
C188 0.1U_0402_16V4Z~D
+0.9V_DDR_VTT
RN1 DDR_A_MA3 DDR_A_MA1 DDR_A_MA12 DDR_A_MA8 56_0404_4P2R_5%~D
RN3 DDR_A_BS0 DDR_A_MA10 DDR_A_MA6 DDR_A_MA7 56_0404_4P2R_5%~D
RN5 DDR_CS0_DIMMA# DDR_A_RAS# DDR_A_MA5 DDR_A_MA9 56_0404_4P2R_5%~D
RN7 DDR_A_CAS# DDR_A_WE# DDR_A_MA4 DDR_A_MA2 56_0404_4P2R_5%~D
RN9 DDR_CS1_DIMMA# M_ODT1 DDR_A_BS1 DDR_A_MA0 56_0404_4P2R_5%~D
RN11 DDR_CKE1_DIMMA R130 56_0402_5%~D DDR_A_MA13 M_ODT0 56_0404_4P2R_5%~D
RN12 DDR_CKE0_DIMMA DDR_A_BS2 DDR_A_MA11 DDR_A_MA14 56_0404_4P2R_5%~D
Layout Note:
Place these resistor
closely JDIMMA,all
trace length<750 mil
Layout Note:
Place these resistor
closely JDIMMA,all
trace length
Max=1.3"
+1.8V_MEM
+1.8V_MEM
+V_DDR_MCH_REF
+V_DDR_MCH_REF
C164 2.2U_0603_6.3V6K~D
C165 0.1U_0402_16V4Z~D
JDIMMA
DDR_A_D0 DDR_A_D1 DDR_A_DQS#0 DDR_A_DQS0 DDR_A_D2 DDR_A_D3 DDR_A_D8 DDR_A_D9 DDR_A_DQS#1 DDR_A_DQS1 DDR_A_D10 DDR_A_D11
DDR_A_D4 DDR_A_D5 DDR_A_DM0 DDR_A_D6 DDR_A_D7 DDR_A_D12 DDR_A_D13 DDR_A_DM1 M_CLK_DDR0 M_CLK_DDR#0 DDR_A_D14 DDR_A_D15
DDR_A_D16 DDR_A_D17 DDR_A_DQS#2 DDR_A_DQS2 DDR_A_D18 DDR_A_D19 DDR_A_D24 DDR_A_D25 DDR_A_DM3
DDR_A_D20 DDR_A_D21 DDR_A_DM2 DDR_A_D22 DDR_A_D23 DDR_A_D28 DDR_A_D29 DDR_A_DQS#3 DDR_A_DQS3
10 DDR_CKE0_DIMMA DDR_A_D26 DDR_A_D27
DDR_A_D30 DDR_A_D31 DDR_CKE1_DIMMA
11 DDR_A_BS2 DDR_A_BS2
DDR_A_MA14 DDR_A_MA12 DDR_A_MA9 DDR_A_MA8
DDR_A_MA11 DDR_A_MA7 DDR_A_MA6
DDR_A_MA5 DDR_A_MA3 DDR_A_MA1
DDR_A_MA4 DDR_A_MA2 DDR_A_MA0
DDR_A_MA10
11 DDR_A_BS0 DDR_A_BS0
11 DDR_A_WE# DDR_A_WE#
DDR_A_BS1 DDR_A_RAS# DDR_CS0_DIMMA#
11 DDR_A_CAS# DDR_A_CAS#
10 DDR_CS1_DIMMA# DDR_CS1_DIMMA#
M_ODT0
DDR_A_MA13
10 M_ODT1 M_ODT1
DDR_A_D32 DDR_A_D33 DDR_A_DQS#4 DDR_A_DQS4 DDR_A_D34 DDR_A_D35 DDR_A_D40 DDR_A_D41 DDR_A_DM5
DDR_A_D36 DDR_A_D37 DDR_A_DM4 DDR_A_D38 DDR_A_D39 DDR_A_D44 DDR_A_D45 DDR_A_DQS#5 DDR_A_DQS5
DDR_A_D42 DDR_A_D43 DDR_A_D48 DDR_A_D49
DDR_A_D46 DDR_A_D47 DDR_A_D52 DDR_A_D53
M_CLK_DDR1 M_CLK_DDR#1
DDR_A_DQS#6 DDR_A_DQS6
DDR_A_D50 DDR_A_D51 DDR_A_D56 DDR_A_D57 DDR_A_DM7
DDR_A_D54 DDR_A_D55 DDR_A_D60 DDR_A_D61 DDR_A_DQS#7 DDR_A_DQS7
DDR_A_D58 DDR_A_D59
DDR_A_D62 DDR_A_D63
17,24 MEM_SDATA MEM_SDATA
17,24 MEM_SCLK MEM_SCLK
R128 10K_0402_5%~D
R129 10K_0402_5%~D
+3.3V_M
C189 0.1U_0402_16V4Z~D
C190 2.2U_0603_6.3V6K~D
FOX_AS0A426-N4RN-7F~D
DIMMA
REVERSE
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Title
SCHEMATIC,A4043
Size
Document Number
401648
Rev
A
Date: Tuesday, October 28, 2008
Sheet 16 of 53


11 DDR_B_DQS#[0..7]
11 DDR_B_D[0..63]
11 DDR_B_DM[0..7]
11 DDR_B_DQS[0..7]
11 DDR_B_MA[0..14]
Layout Note:
Place near JDIMMB
+1.8V_MEM
2.2U_0603_6.3V6K~D
0.1U_0402_16V4Z~D
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT
+0.9V_DDR_VTT
RN14
RN15
RN16
RN17
RN18
RN19
RN20
RN21
RN22
RN23
RN24
RN25
RN26
56_0404_4P2R_5%~D
R133
56_0402_5%~D
Layout Note:
Place these resistor
closely JDIMMB,all
trace length<750 mil
Layout Note:
Place these resistor
closely JDIMMB,all
trace length
Max=1.3"
+1.8V_MEM
+V_DDR_MCH_REF
+V_DDR_MCH_REF
JDIMMB
DDR_B_D0
DDR_B_D1
DDR_B_DQS#0
DDR_B_DQS0
DDR_B_D2
DDR_B_D3
DDR_B_D8
DDR_B_D9
DDR_B_DQS#1
DDR_B_DQS1
DDR_B_D10
DDR_B_D11
DDR_B_D16
DDR_B_D17
DDR_B_DQS#2
DDR_B_DQS2
DDR_B_D18
DDR_B_D19
DDR_B_D24
DDR_B_D25
DDR_B_DM3
DDR_B_D26
DDR_B_D27
10 DDR_CKE2_DIMMB
DDR_CKE2_DIMMB
11 DDR_B_BS2
DDR_B_MA12
DDR_B_MA9
DDR_B_MA8
DDR_B_MA5
DDR_B_MA3
DDR_B_MA1
DDR_B_MA10
11 DDR_B_BS0
DDR_B_BS0
11 DDR_B_WE#
DDR_B_WE#
11 DDR_B_CAS#
10 DDR_CS3_DIMMB#
DDR_CS3_DIMMB#
10 M_ODT3
M_ODT3
DDR_B_D32
DDR_B_D33
DDR_B_DQS#4
DDR_B_DQS4
DDR_B_D34
DDR_B_D35
DDR_B_D40
DDR_B_D41
DDR_B_DM5
DDR_B_D42
DDR_B_D43
DDR_B_D48
DDR_B_D49
DDR_B_DQS#6
DDR_B_DQS6
DDR_B_D50
DDR_B_D51
DDR_B_D56
DDR_B_D57
DDR_B_D7
DDR_B_D58
DDR_B_D59
16,24 MEM_SDATA
16,24 MEM_SCLK
+3.3V_M
MEM_SDATA
MEM_SCLK
FOX_AS0A426-N8RN-7F_RV
DDR_B_D4
DDR_B_D5
DDR_B_DM0
DDR_B_D6
DDR_B_D7
DDR_B_D12
DDR_B_D13
DDR_B_DM1
M_CLK_DDR2 10
M_CLK_DDR#2 10
DDR_B_D14
DDR_B_D15
DDR_B_D20
DDR_B_D21
DDR_B_DM2
DDR_B_D22
DDR_B_D23
DDR_B_D28
DDR_B_D29
DDR_B_DQS#3
DDR_B_DQS3
DDR_B_D30
DDR_B_D31
DDR_CKE3_DIMMB
DDR_CKE3_DIMMB 10
DDR_B_MA14
DDR_B_MA11
DDR_B_MA7
DDR_B_MA6
DDR_B_MA4
DDR_B_MA2
DDR_B_MA0
DDR_B_BS1
DDR_B_RAS#
DDR_CS2_DIMMB#
DDR_B_BS1 11
DDR_B_RAS# 11
DDR_CS2_DIMMB# 10
M_ODT2
M_ODT2 10
DDR_B_MA13
DDR_B_D36
DDR_B_D37
DDR_B_DM4
DDR_B_D38
DDR_B_D39
DDR_B_D44
DDR_B_D45
DDR_B_DQS#5
DDR_B_DQS5
DDR_B_D46
DDR_B_D47
DDR_B_D52
DDR_B_D53
M_CLK_DDR3
M_CLK_DDR#3
M_CLK_DDR3 10
M_CLK_DDR#3 10
DDR_B_DM6
DDR_B_D54
DDR_B_D55
DDR_B_D60
DDR_B_D61
DDR_B_DQS#7
DDR_B_DQS7
DDR_B_D62
DDR_B_D63
+3.3V_M
R131
10K_0402_5%~D
R132
10K_0402_5%~D
2.2U_0603_6.3V6K~D
C191
0.1U_0402_16V4Z~D
C192
0.1U_0402_16V4Z~D
C215
2.2U_0603_6.3V6K~D
C216
DIMMB
STANDARD
DELL CONFIDENTIAL/PROPRIETARY
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL
TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT
BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION,
NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD
PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.
Compal Electronics, Inc.
Title
SCHEMATIC,A4043
Size
Document Number
401648
Rev
A
Date: Tuesday, October 28, 2008
Sheet 17 of 53



Pull-up Resistor on ADDR_MODE/XEN	For Remote1 mode	SMBUS Address
<= 4.7K +/- 5%	2N3904	2F(r/w)
10K	2N3904	2E(r/w)
18K	Thermistor	2F(r/w)
>= 33K	Thermistor	2E(r/w)

*

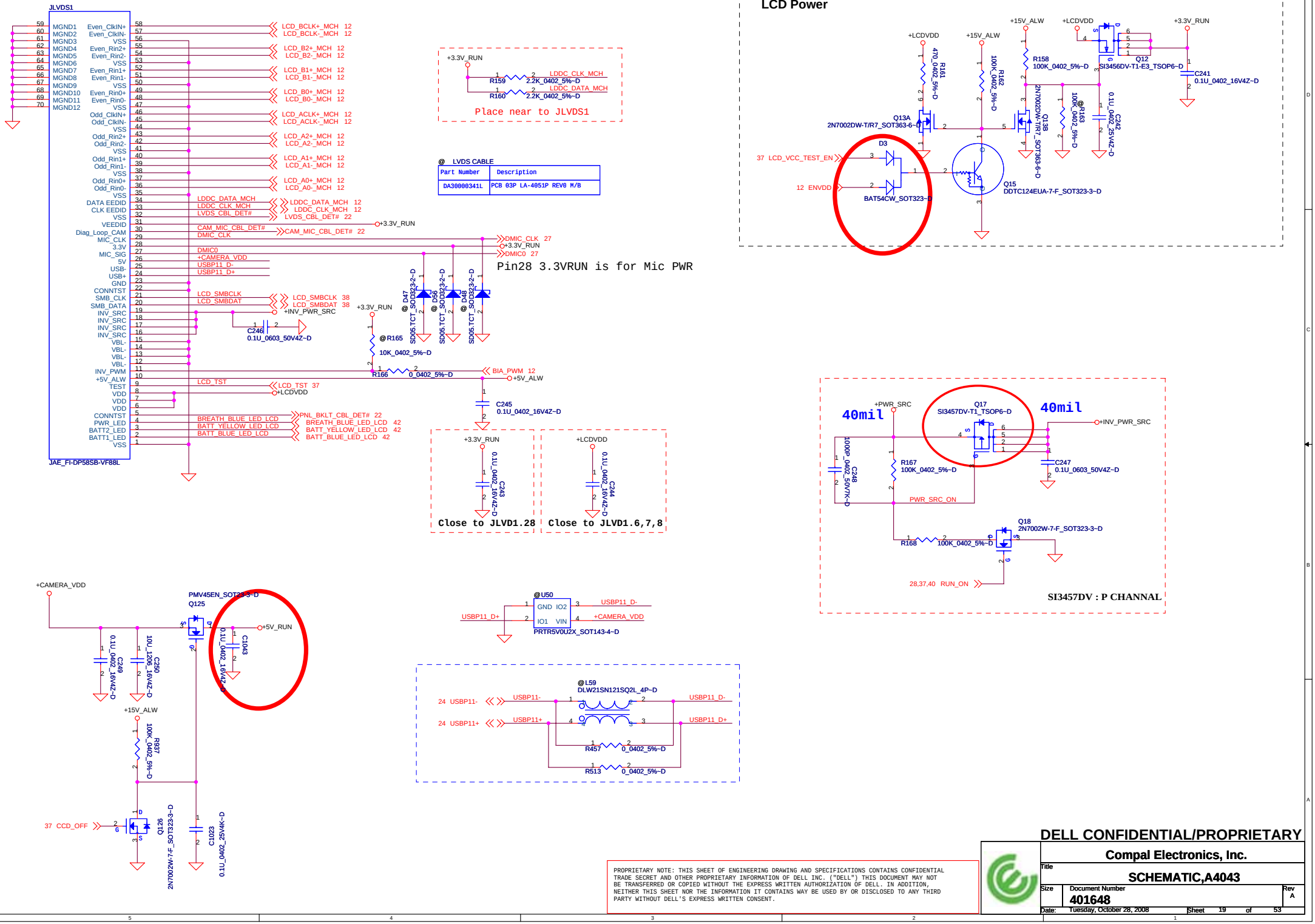
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SCHEMATIC,A4043

Size | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 18 of 53



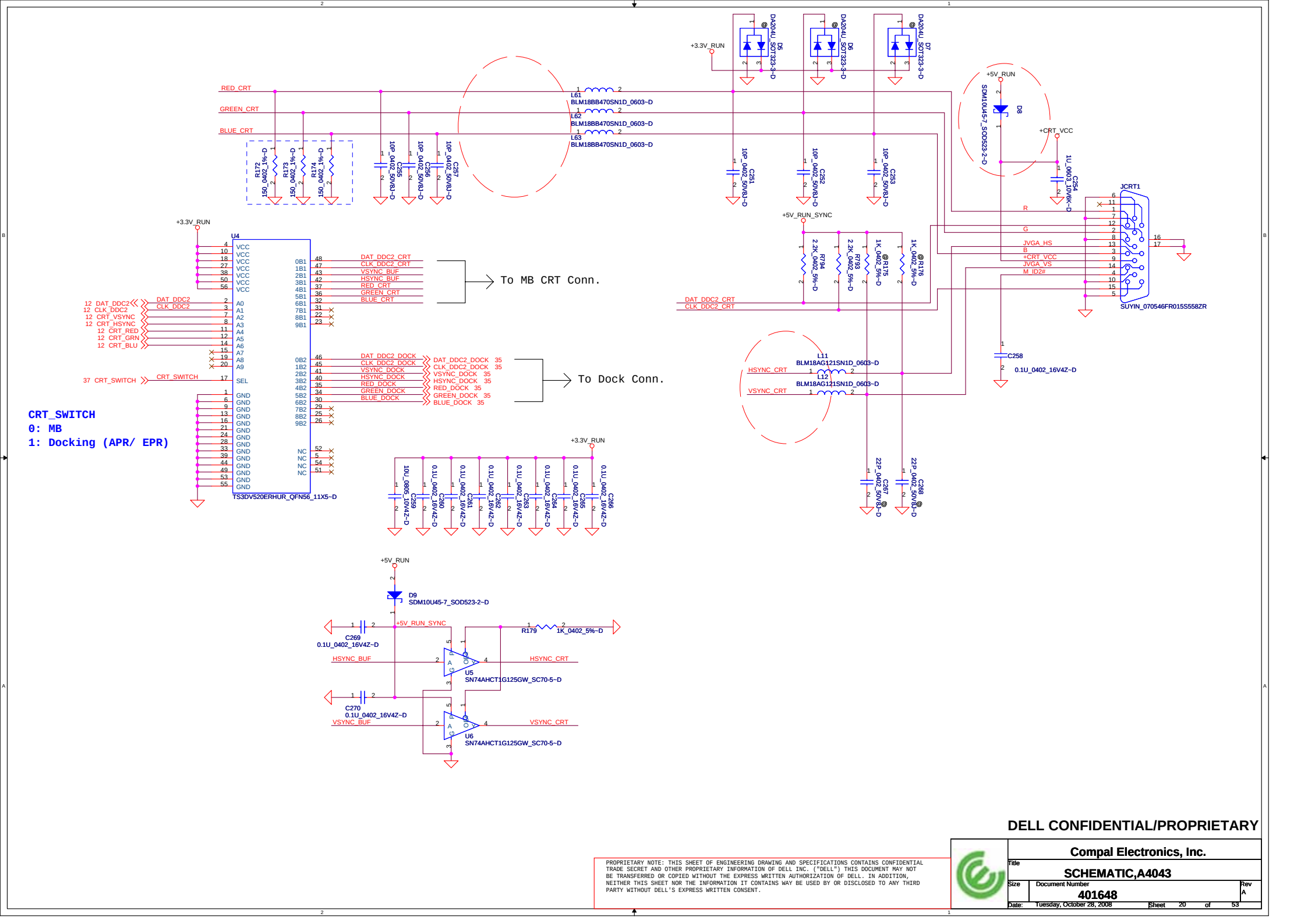
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SCHEMATIC,A4043

Size | Document Number: 401648 | Rev: A

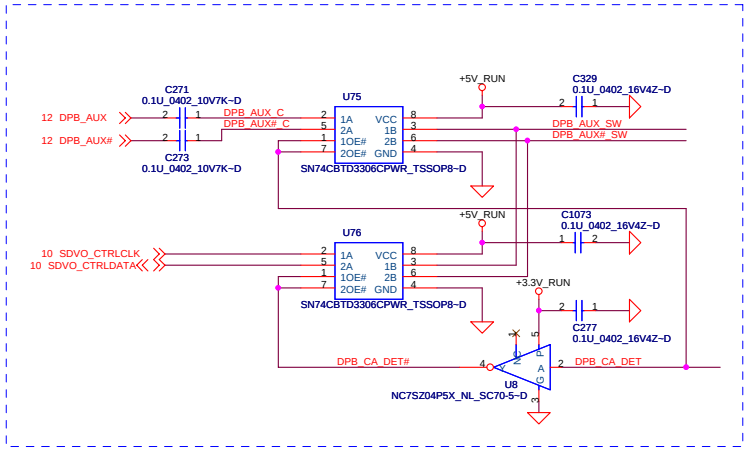
Date: Tuesday, October 28, 2008 | Sheet 19 of 53



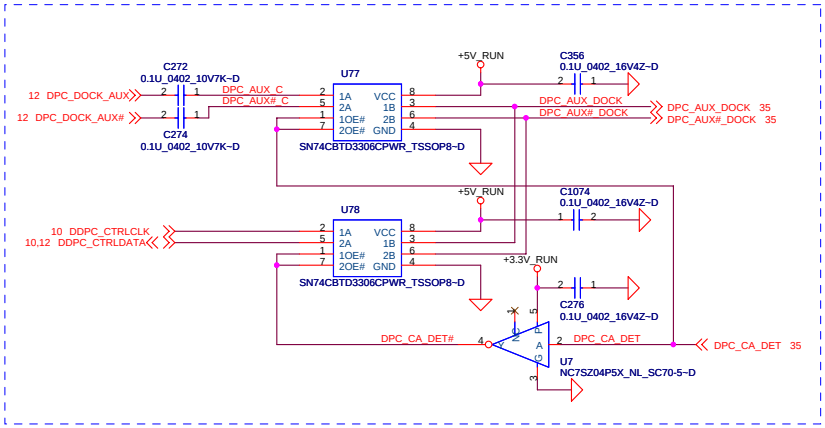
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	SCHEMATIC,A4043
Size	Document Number 401648 Rev A
Date: Tuesday, October 28, 2008	Sheet 20 of 53

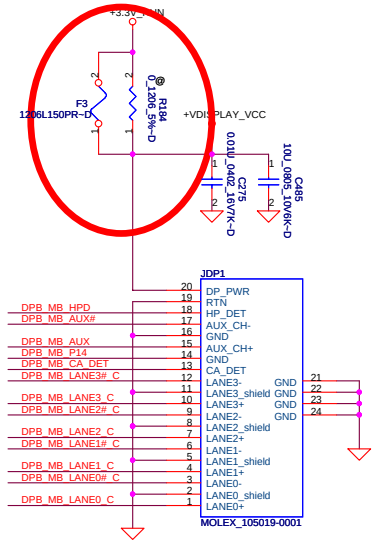
SW for MB side

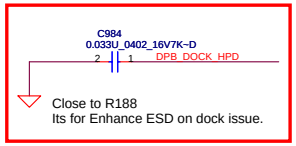


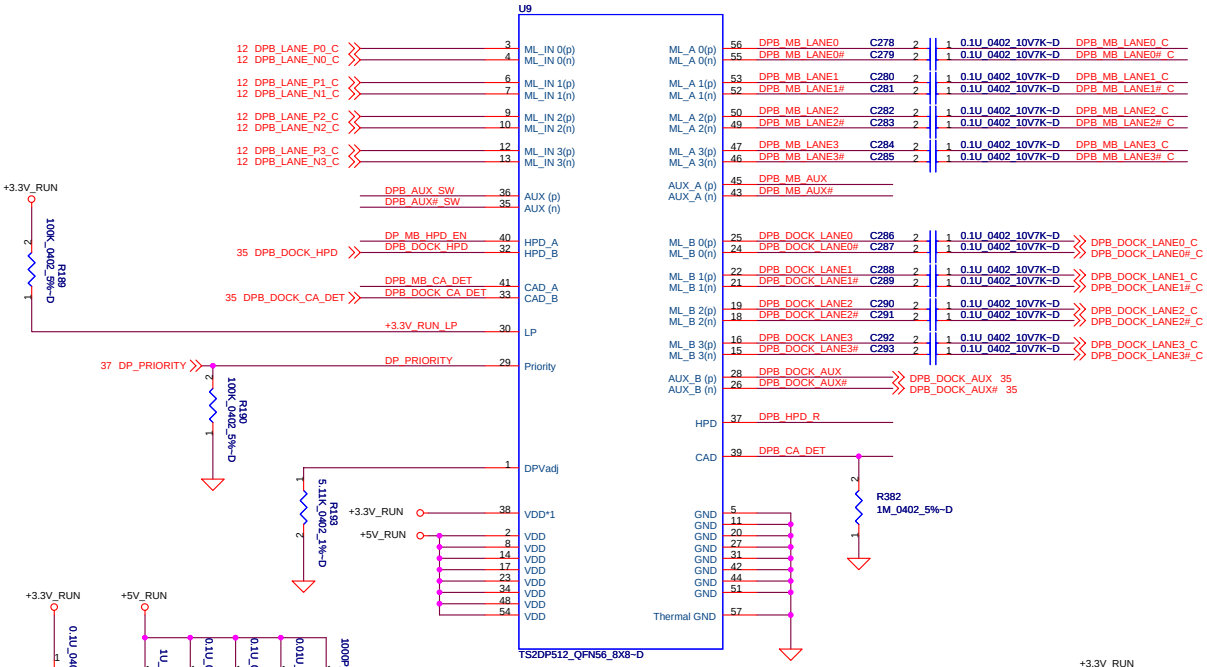
SW for eDOCK side

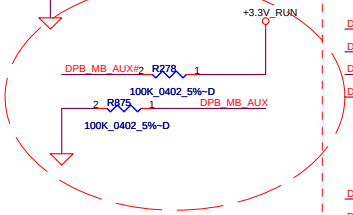


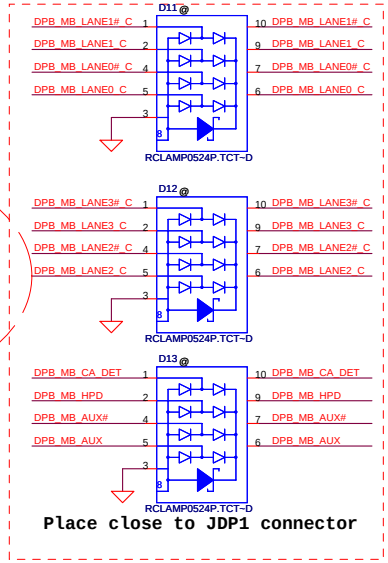
Display port Connector

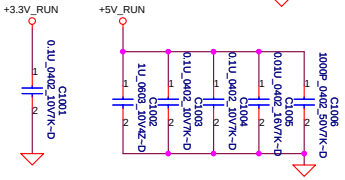


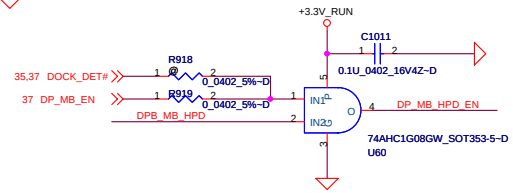


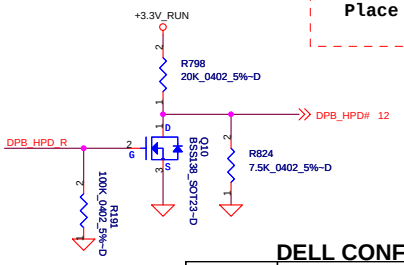












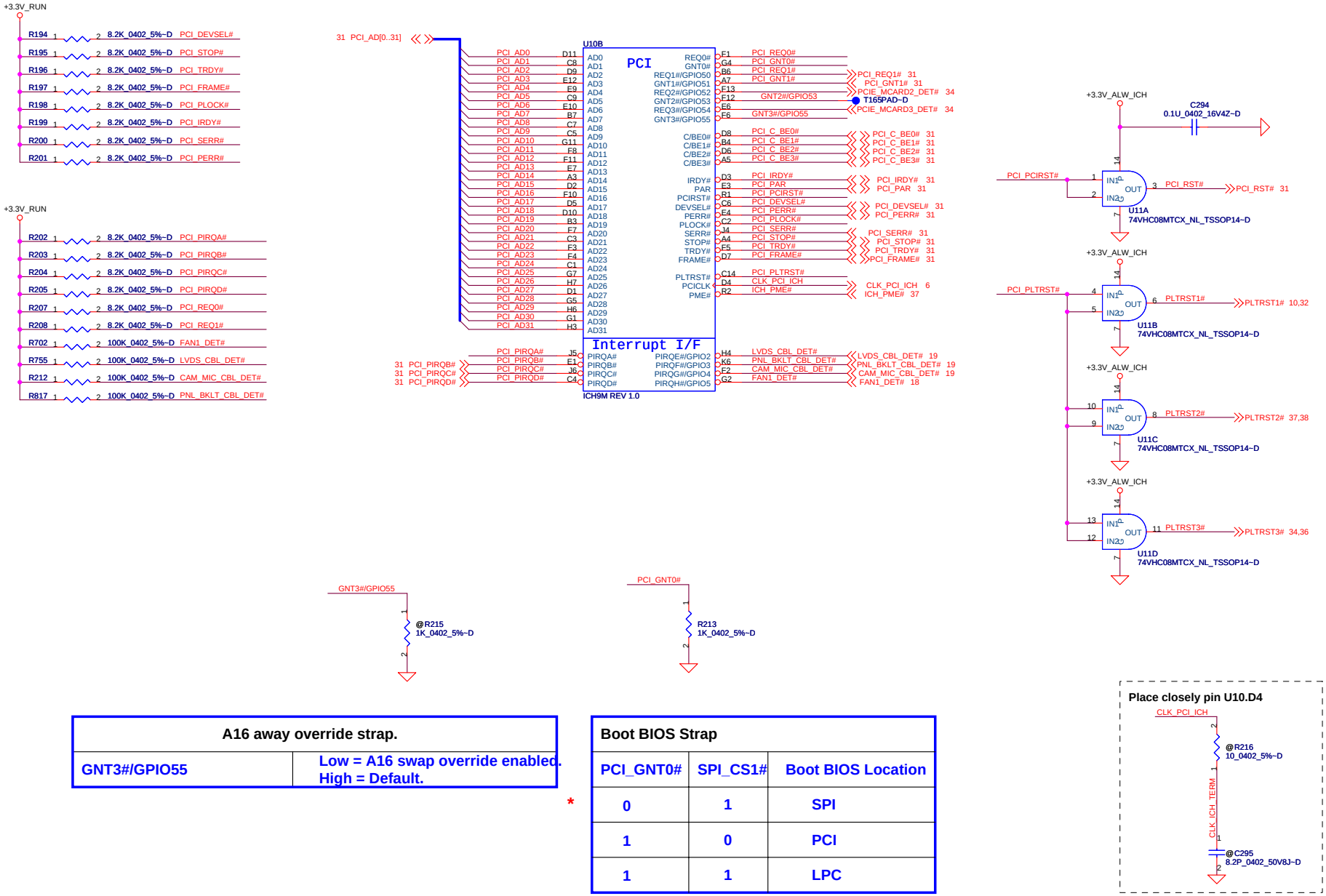
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SCHEMATIC,A4043

Size: | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 21 of 53



A16 away override strap.	
GNT3#/GPIO55	Low = A16 swap override enabled. High = Default.

*

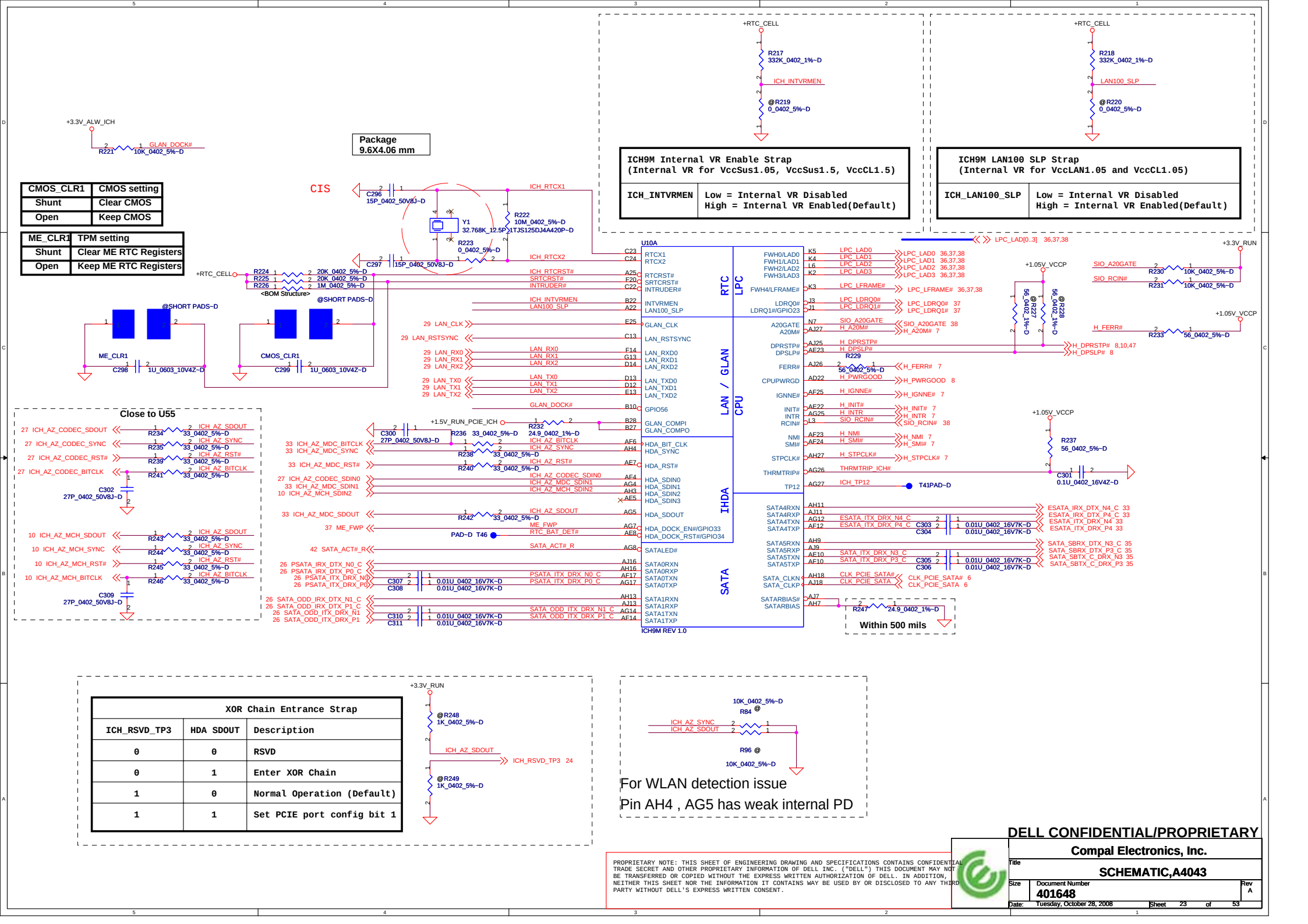
Boot BIOS Strap		
PCI_GNT0#	SPI_CS1#	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC

Compal Electronics, Inc.

Title: SCHEMATIC,A4043

Size | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 22 of 53


CIS
Package
9.6X4.06 mm
CMOS_CLR1 | CMOS setting
Shunt | Clear CMOS
Open | Keep CMOS
ME_CLR1 | TPM setting
Shunt | Clear ME RTC Registers
Open | Keep ME RTC Registers
ICH9M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)
ICH_INTVRMEN | Low = Internal VR Disabled
High = Internal VR Enabled(Default)
ICH9M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)
ICH_LAN100_SLP | Low = Internal VR Disabled
High = Internal VR Enabled(Default)
Close to U55
XOR Chain Entrance Strap
ICH_RSVD_TP3 | HDA SDOUT | Description
0 | 0 | RSVD
0 | 1 | Enter XOR Chain
1 | 0 | Normal Operation (Default)
1 | 1 | Set PCIE port config bit 1
For WLAN detection issue
Pin AH4 , AG5 has weak internal PD
Within 500 mils
ICH9M REV 1.0
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Title
SCHEMATIC,A4043
Size
Document Number
401648
Rev
A
Date: Tuesday, October 28, 2008
Sheet 23 of 53

TPM_ID:
H: Enable
L: Disable

iTPM function	
R270	No stuff = Disable
	Stuff = Enable

No Reboot Strap	
SPKR	Low = Default
	High = No Reboot

Option to " Disable " clkrun. Pulling it down will keep the clks running.

MiniWWAN (Mini Card 1)--->
MiniWLAN (Mini Card 2)--->
BT/UWB--->
Express card--->
10/100/1G LAN --->

200 MIL SO8
Flash ROM

Within 500 mils

----->

Place closely pin U10.H1

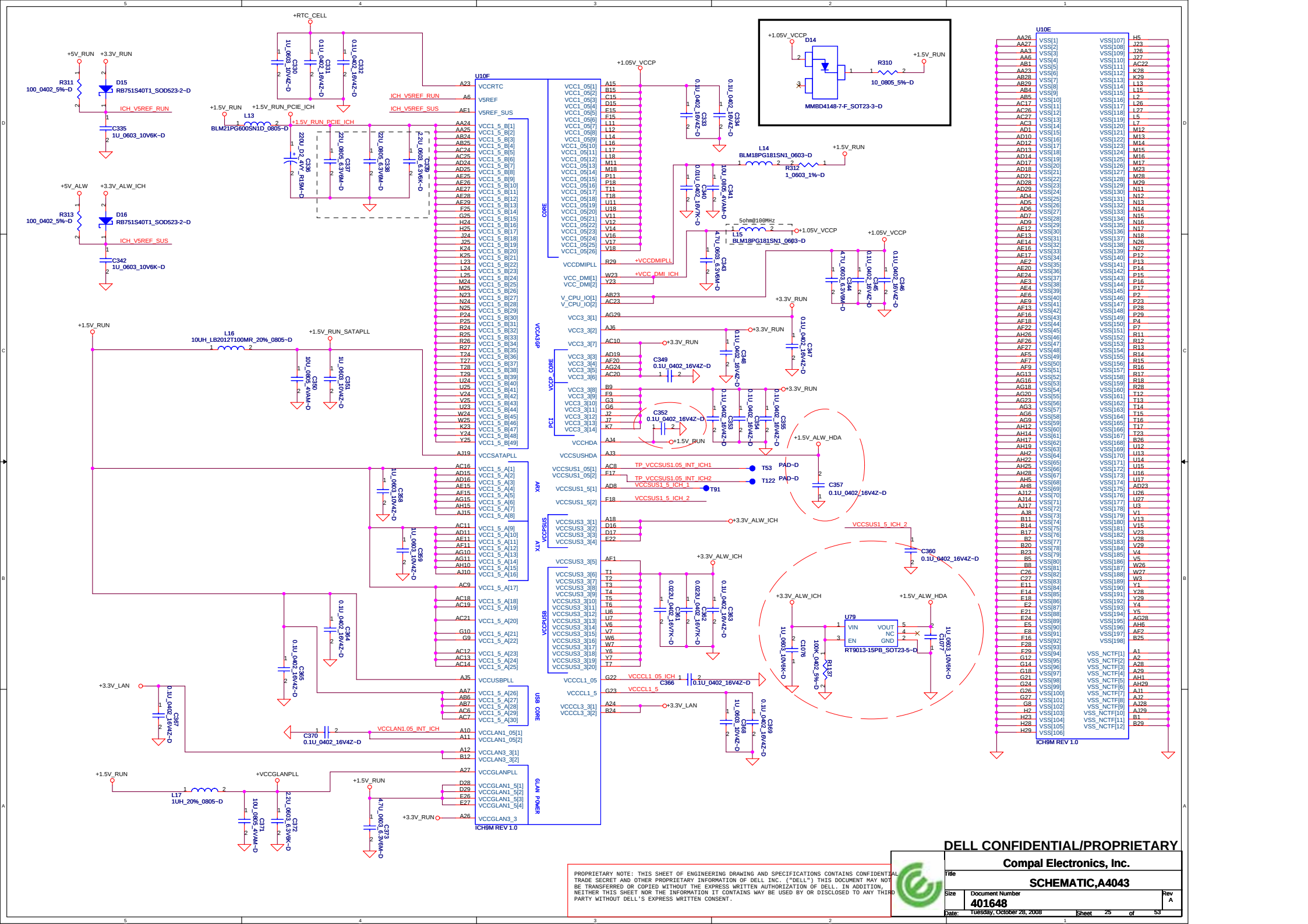
Place closely pin U10.AF3

Compal Electronics, Inc.

Title: SCHEMATIC,A4043

Size: | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 24 of 53

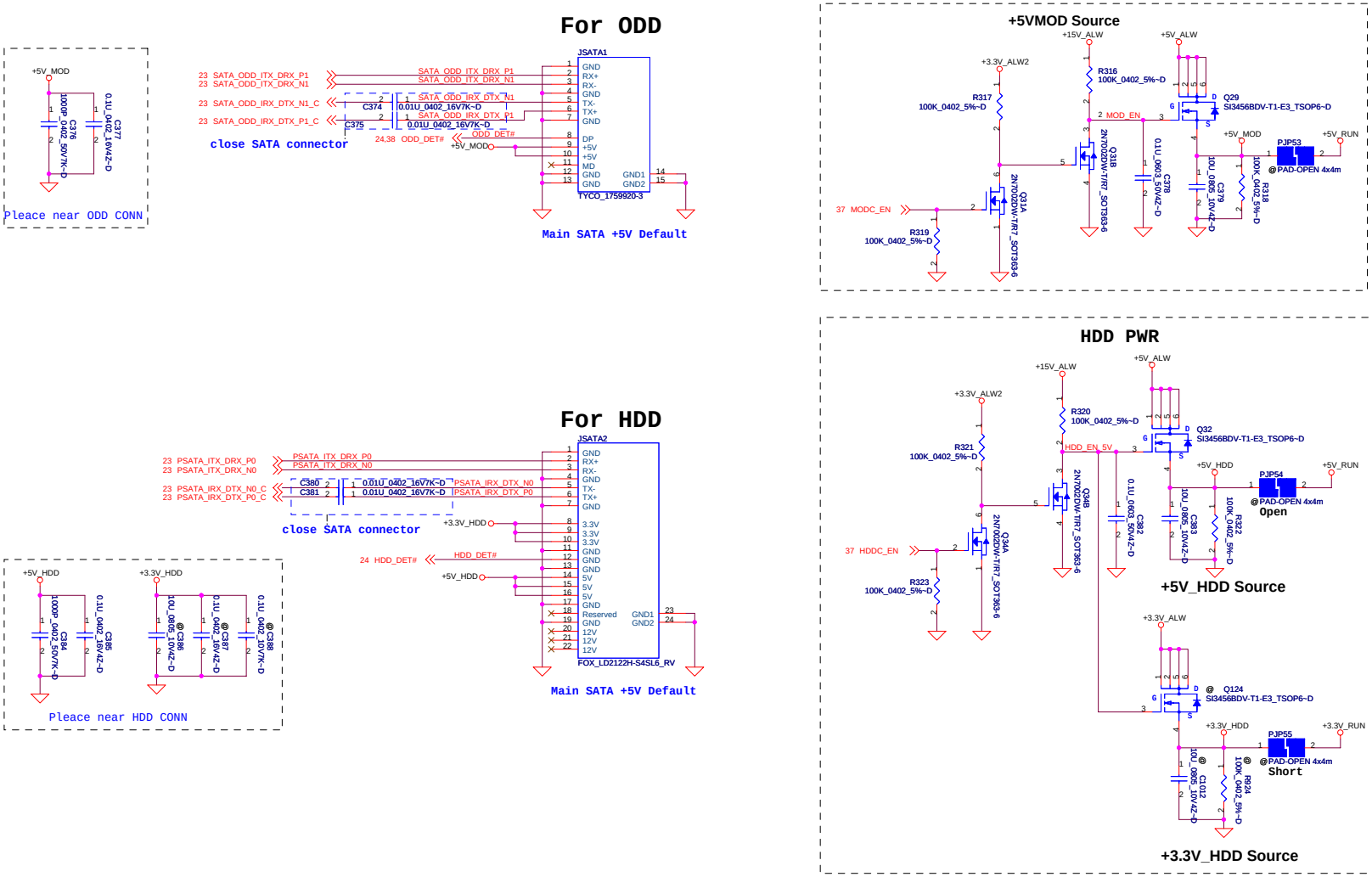


Compal Electronics, Inc.

Title: SCHEMATIC,A4043

Size: | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 25 of 53

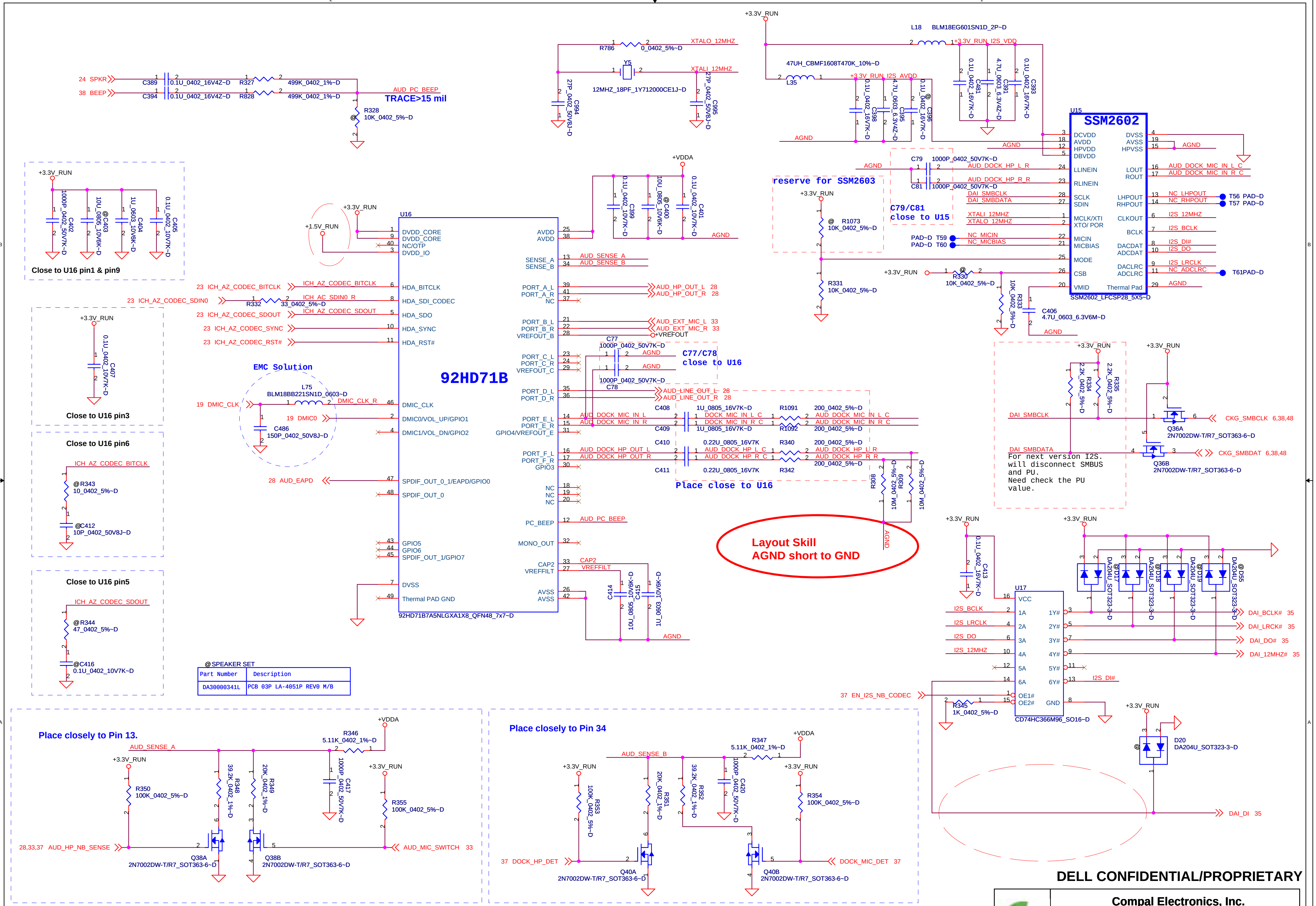


Compal Electronics, Inc.

Title: SCHEMATIC,A4043

Size | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 26 of 53



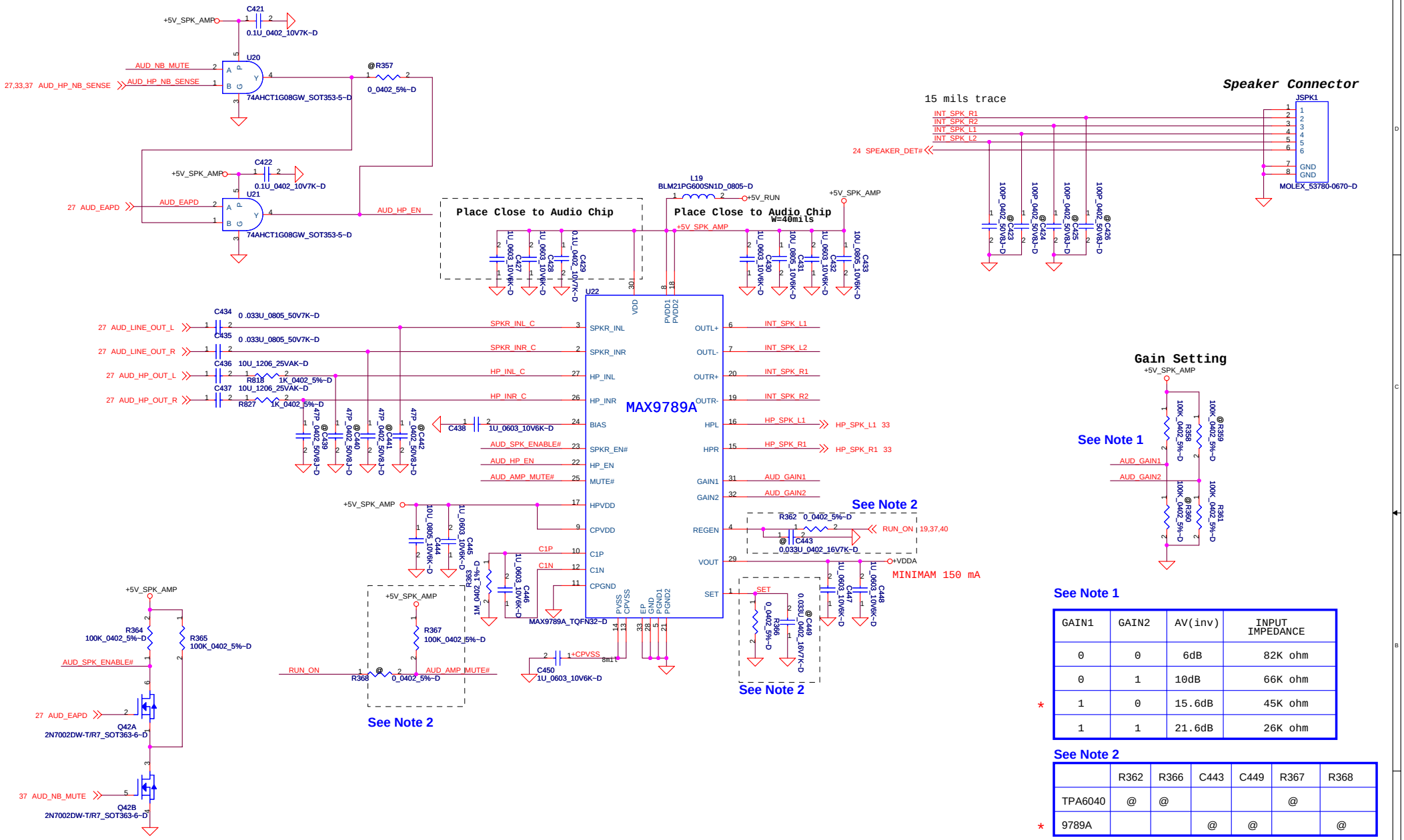
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: SCHEMATIC,A4043

Size	Document Number	Rev
	401648	A

Date: Tuesday, October 28, 2008 Sheet 27 of 53



GAIN1	GAIN2	AV(inv)	INPUT IMPEDANCE
0	0	6dB	82K ohm
0	1	10dB	66K ohm
* 1	0	15.6dB	45K ohm
1	1	21.6dB	26K ohm

See Note 2

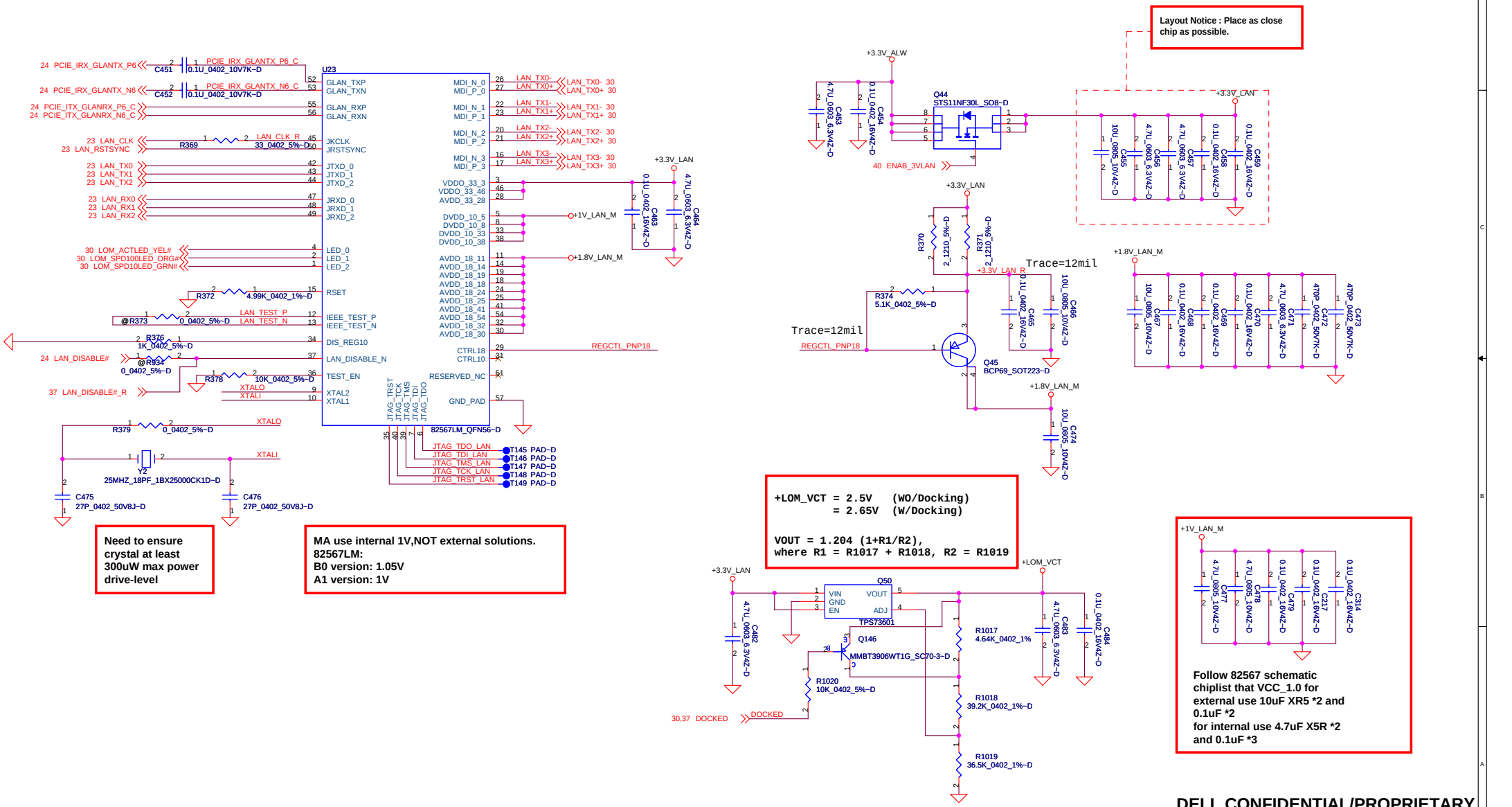
	R362	R366	C443	C449	R367	R368
TPA6040	@	@			@	
* 9789A			@	@		@

Compal Electronics, Inc.

Title: SCHEMATIC,A4043

Size | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 28 of 53



Need to ensure crystal at least 300uW max power drive-level

MA use internal 1V,NOT external solutions.
82567LM:
B0 version: 1.05V
A1 version: 1V

Layout Notice : Place as close chip as possible.

Follow 82567 schematic chiplist that VCC_1.0 for external use 10uF XR5 *2 and 0.1uF *2
for internal use 4.7uF X5R *2 and 0.1uF *3

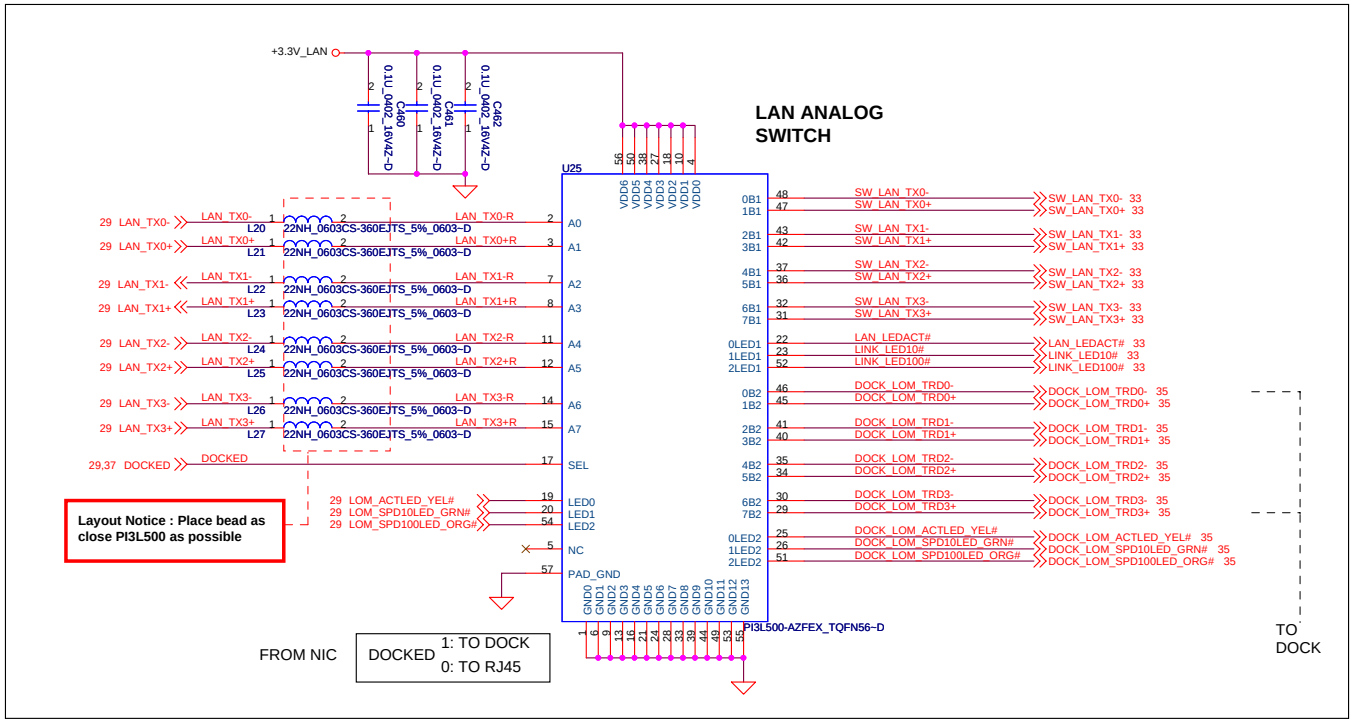
DELL CONFIDENTIAL/PROPRIETARY

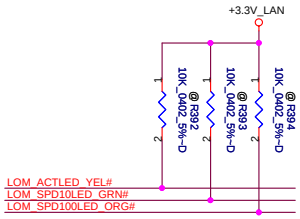
Compal Electronics, Inc.

Title: SCHEMATIC,A4043

Size | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 29 of 53





DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	SCHEMATIC,A4043
Size	Document Number: 401648 — Rev: A
Date: Tuesday, October 28, 2008	Sheet 30 of 53

U26A

R5C847-CSP208Q

16 bit PC card I/F

RST & INT & AUDIO

CLK

1394 I/F

USB TEST

Media Card I/F

R5C847-CSP208Q_CSP208-D

must have clean layout

For MMC PLUS

R416/C397 close to R5C847

close to U26

Close to U26

Close to Pin A16,B16

Close to JSD1

Close to JSD1

U27

R5531V002-E2-FA_SSOP16-D

JS1394

TYCO_2-1734820-0_20P-T

JSD1

TYCO_1-1775737-6

U28

TPS2051BDBVR_SOT23-5-D

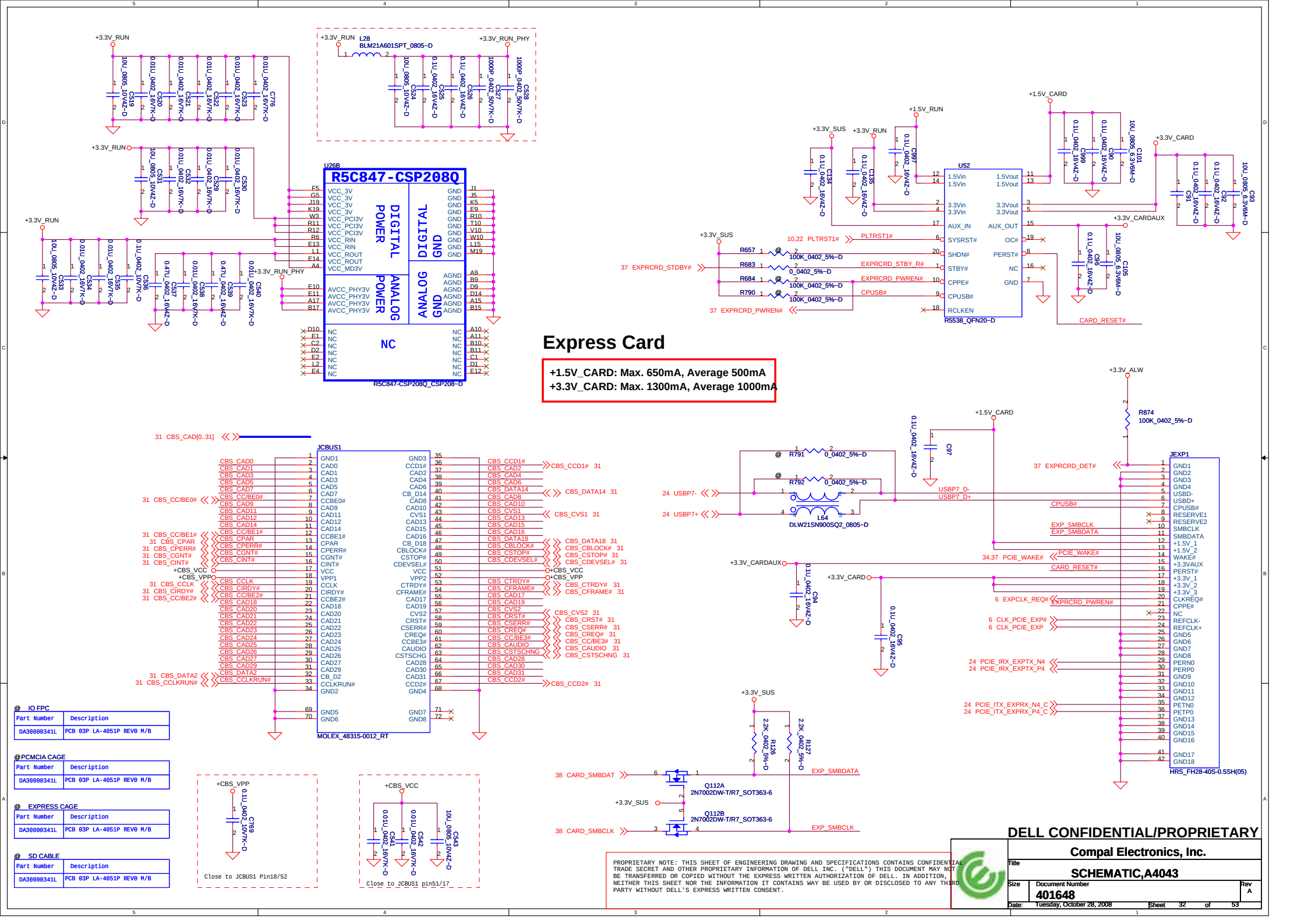
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SCHEMATIC,A4043

Size: | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 31 of 53



@ IO FPC

Part Number	Description
DA30000341L	PCB 03P LA-4051P REV0 M/B

@PCMCIA CAGE

Part Number	Description
DA30000341L	PCB 03P LA-4051P REV0 M/B

@ EXPRESS CAGE

Part Number	Description
DA30000341L	PCB 03P LA-4051P REV0 M/B

@ SD CABLE

Part Number	Description
DA30000341L	PCB 03P LA-4051P REV0 M/B

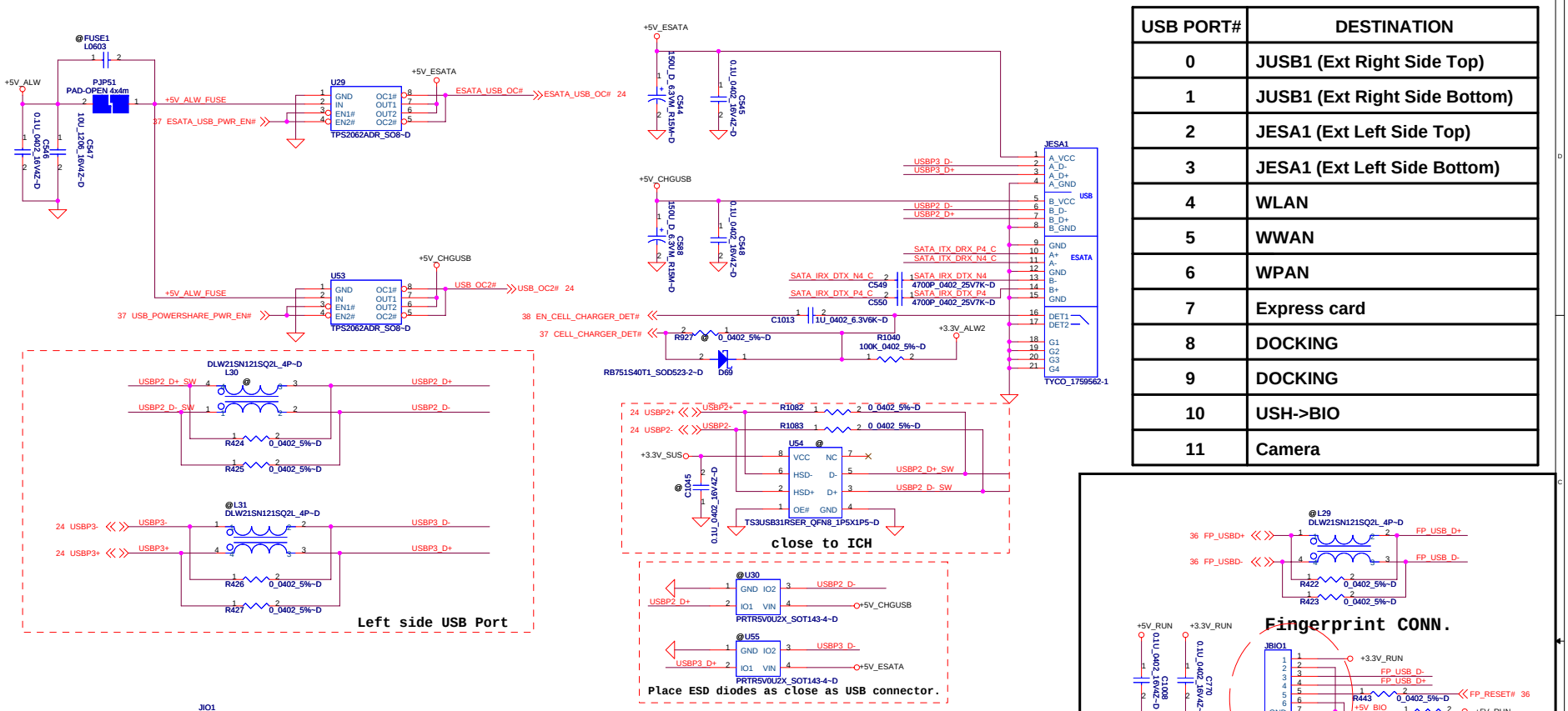
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SCHEMATIC,A4043

Size: | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 32 of 53



USB PORT#	DESTINATION
0	JUSB1 (Ext Right Side Top)
1	JUSB1 (Ext Right Side Bottom)
2	JESA1 (Ext Left Side Top)
3	JESA1 (Ext Left Side Bottom)
4	WLAN
5	WWAN
6	WPAN
7	Express card
8	DOCKING
9	DOCKING
10	USH->BIO
11	Camera

Compal Electronics, Inc.

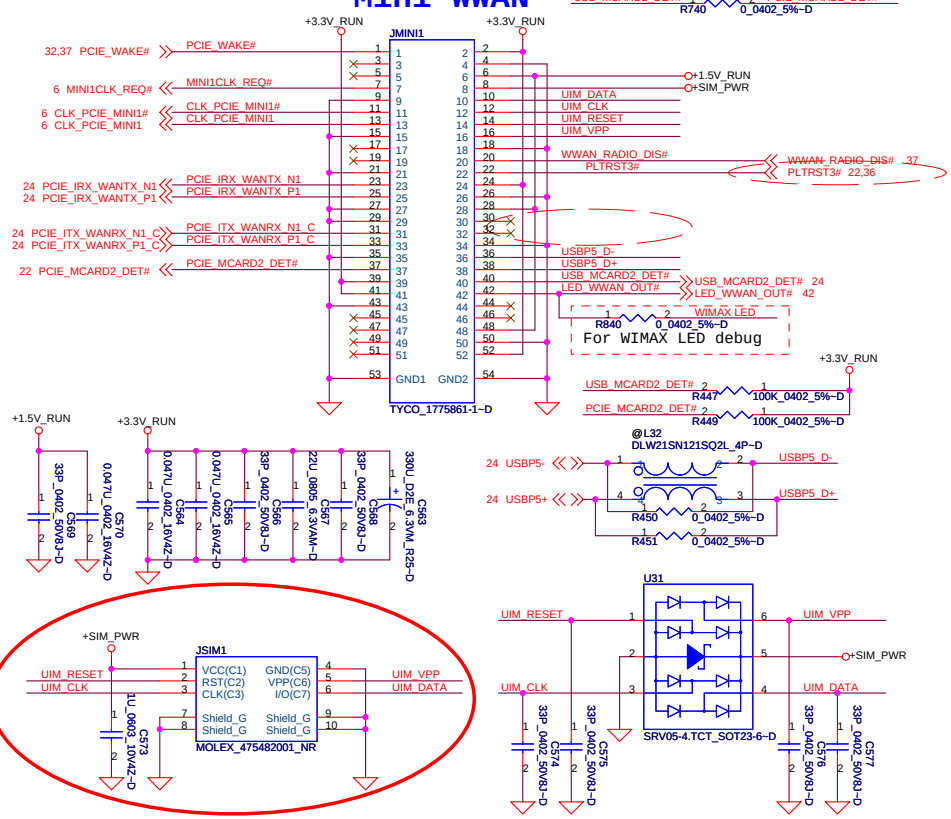
Title: SCHEMATIC,A4043

Size: Document Number: 401648 Rev: A

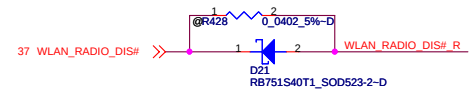
Date: Tuesday, October 28, 2008 Sheet 33 of 53

Delete SM bus

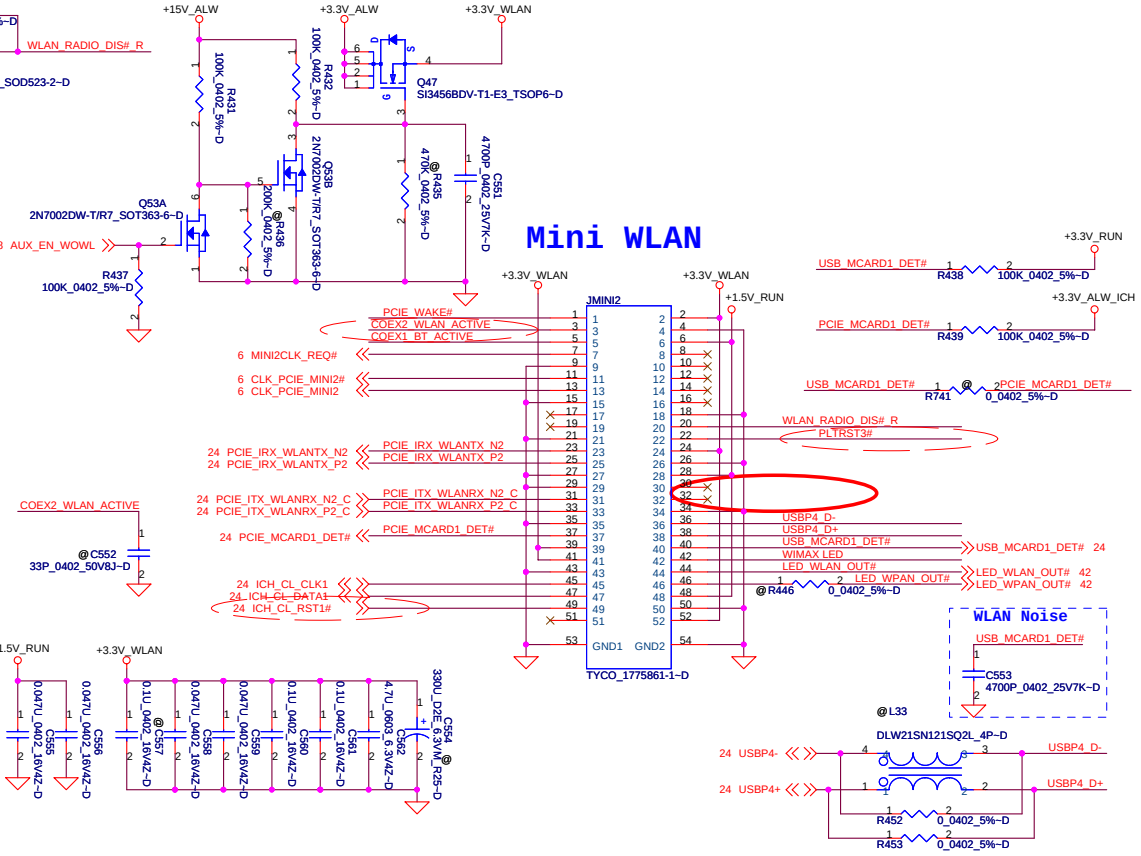
Mini WWAN



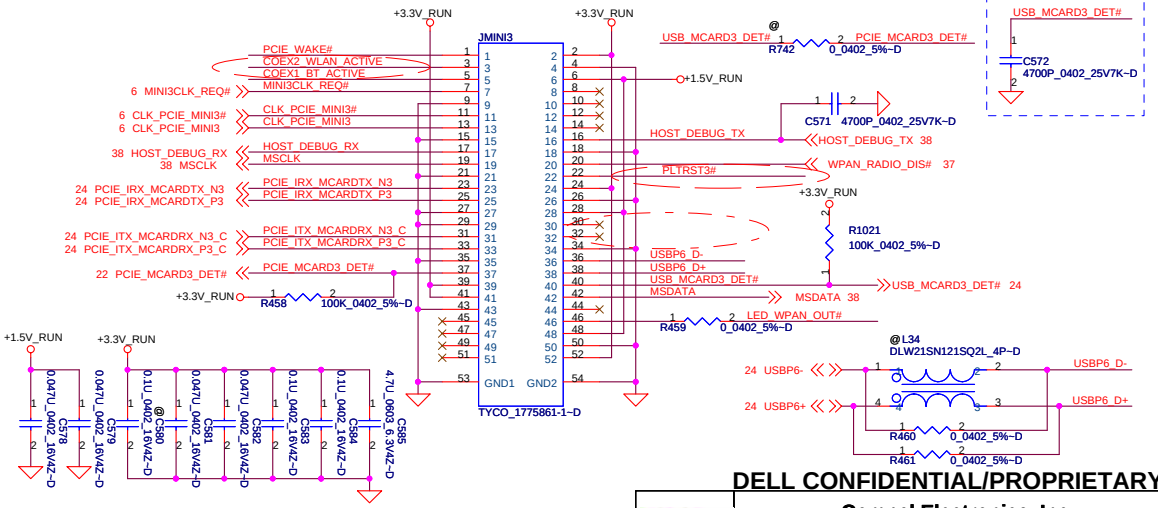
PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA



Mini WLAN



WPAN Card

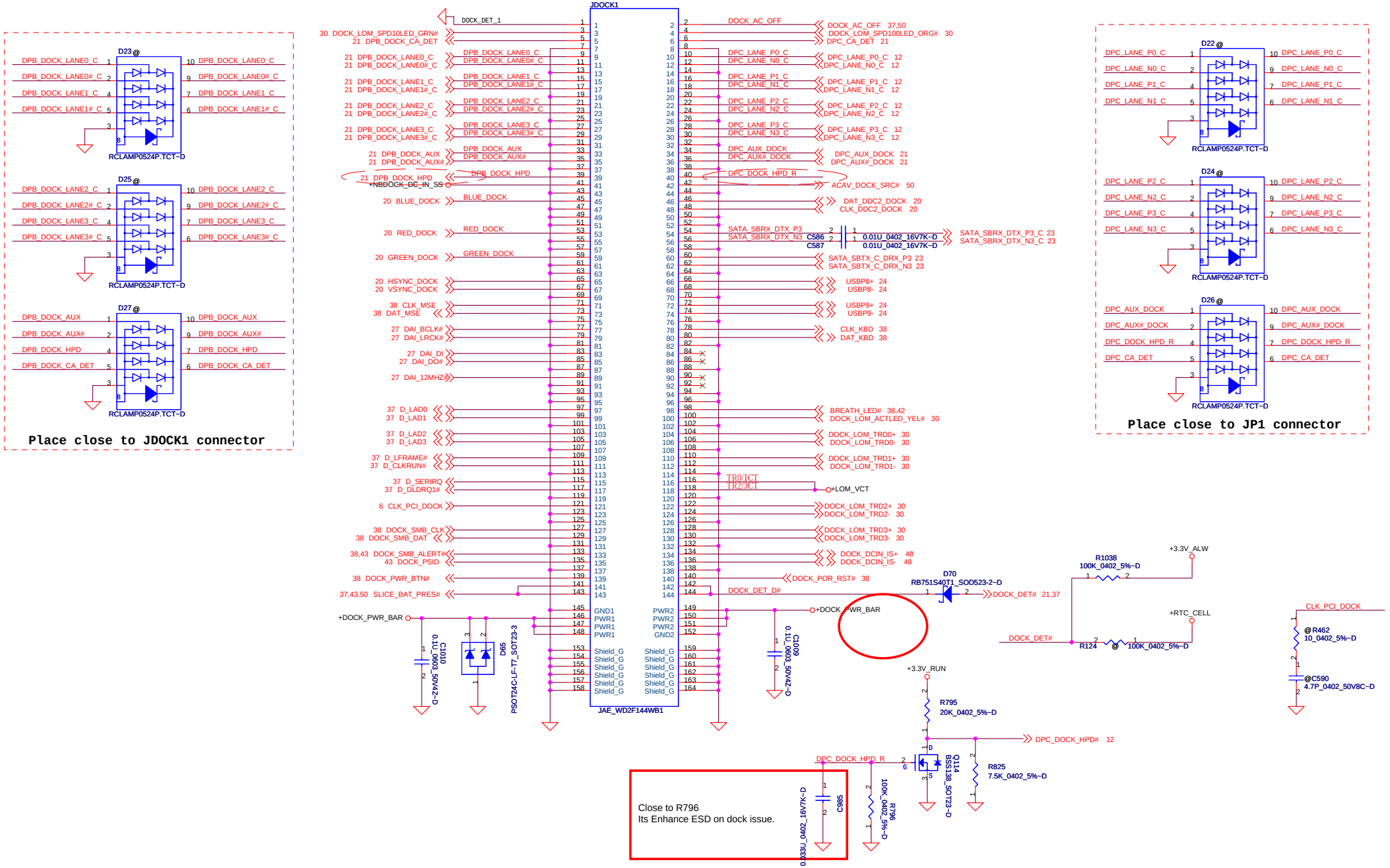


Compal Electronics, Inc.

Title: SCHEMATIC,A4043

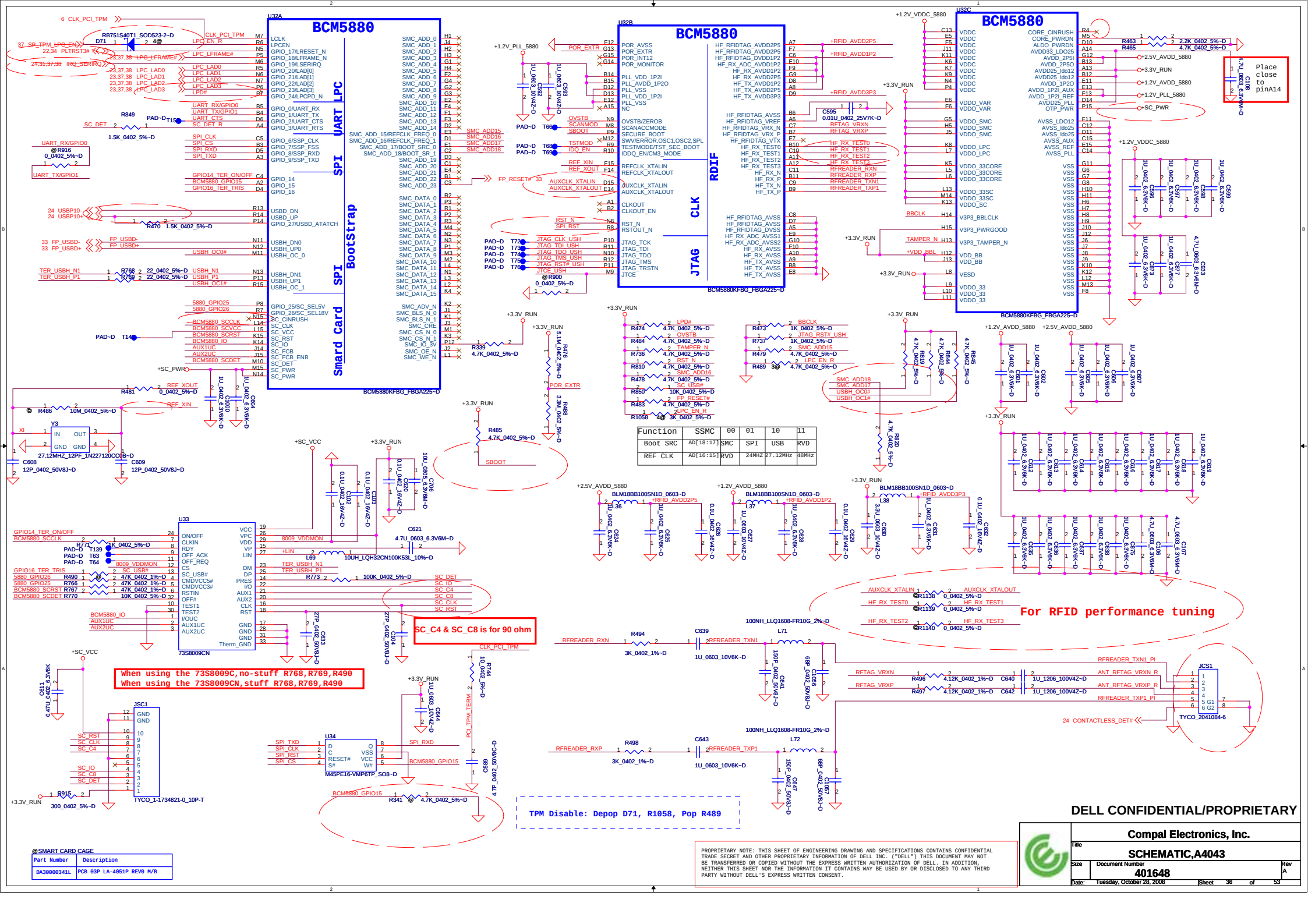
Size: | Document Number: 401648 | Rev: A

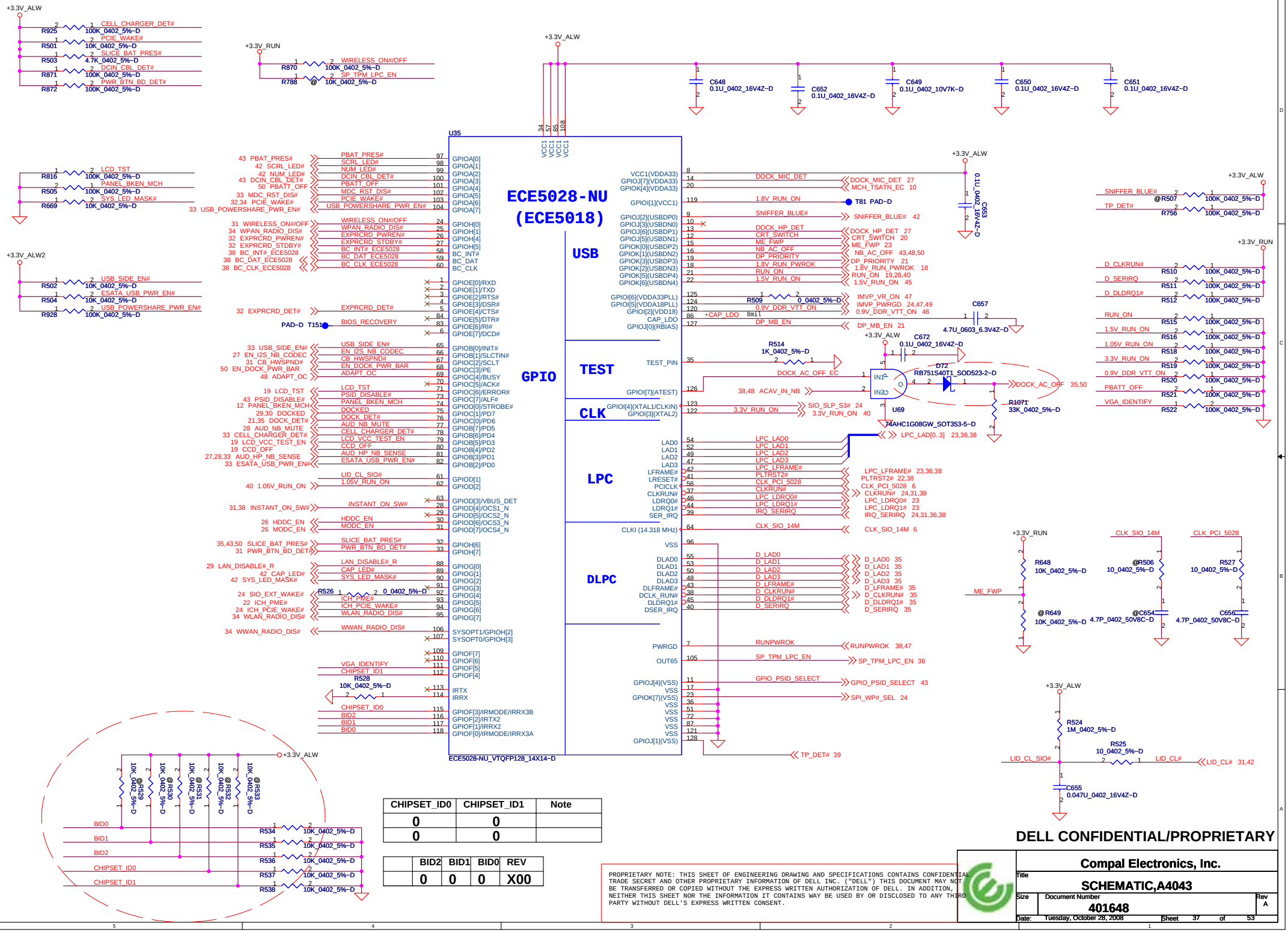
Date: Tuesday, October 28, 2008 | Sheet 34 of 53



PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.		
Title: SCHEMATIC,A4043		
Size	Document Number: 401648	Rev: A
Date: Tuesday, October 28, 2008	Sheet 35 of 53	


U32A
BCM5880
BCM5880KFBG_FBGA225~D
U32B
BCM5880
BCM5880KFBG_FBGA225~D
U32C
BCM5880
BCM5880KFBG_FBGA225~D
SMART CARD
SPI
UART
LPC
BOOTSTRAP
RDIF
CLK
JTAG
U33
73S8009CN
U34
M45PE16-VMP6TP_SO8~D
JSC1
TYCO_1-1734821-0_10P-T
JCS1
TYCO_2041084-6
Function | SSMC | 00 | 01 | 10 | 11
Boot SRC | AD[18:17] | SMC | SPI | USB | RVD
REF CLK | AD[16:15] | RVD | 24MHz | 27.12MHz | 48MHz
When using the 73S8009C,no-stuff R768,R769,R490
When using the 73S8009CN,stuff R768,R769,R490
SC_C4 & SC_C8 is for 90 ohm
For RFID performance tuning
TPM Disable: Depop D71, R1058, Pop R489
@SMART CARD CAGE
Part Number | Description
DA30000341L | PCB 03P LA-4051P REV0 M/B
DELL CONFIDENTIAL/PROPRIETARY
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.
Compal Electronics, Inc.
Title
SCHEMATIC,A4043
Size
Document Number
401648
Rev
A
Date: Tuesday, October 28, 2008
Sheet 36 of 53



CHIPSET_ID0	CHIPSET_ID1	Note
0	0	
0	0	

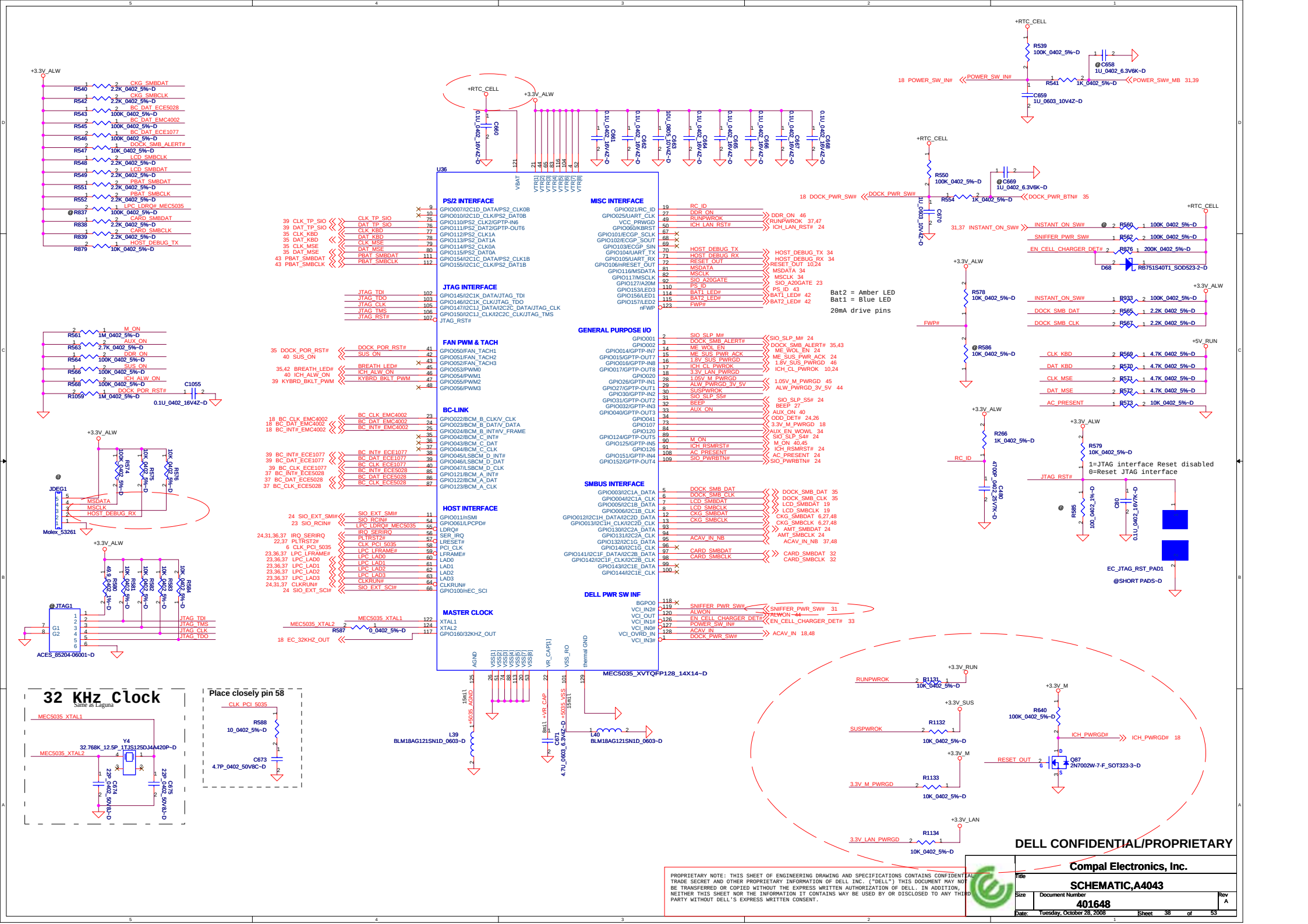
	BID2	BID1	BID0	REV
	0	0	0	X00

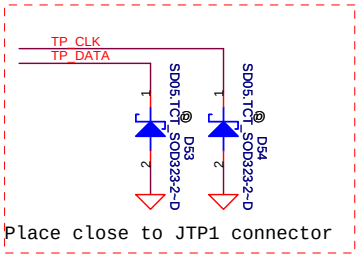
Compal Electronics, Inc.

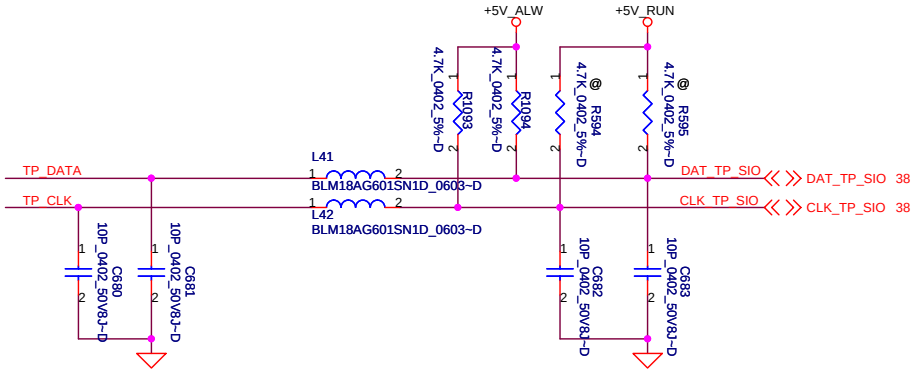
Title: SCHEMATIC,A4043

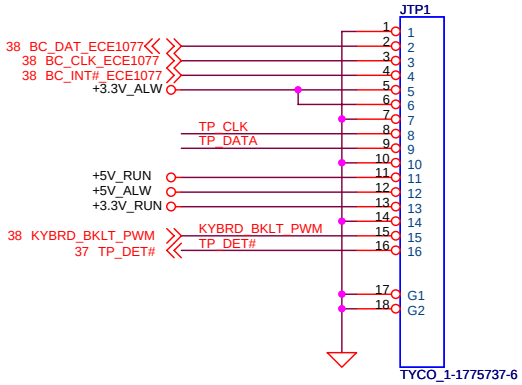
Size | Document Number: 401648 | Rev: A

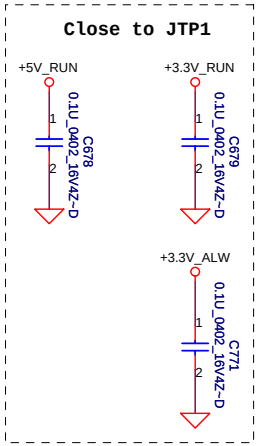
Date: Tuesday, October 28, 2008 | Sheet 37 of 53

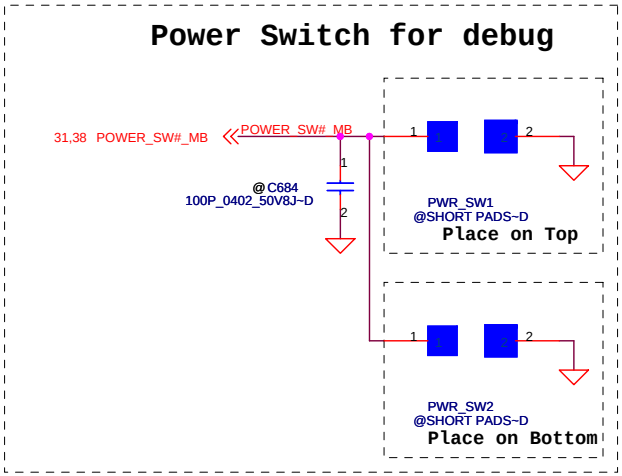

U36
MEC5035_XVTQFP128_14X14~D
PS/2 INTERFACE
JTAG INTERFACE
FAN PWM & TACH
BC-LINK
HOST INTERFACE
MASTER CLOCK
MISC INTERFACE
GENERAL PURPOSE I/O
SMBUS INTERFACE
DELL PWR SW INF
Bat2 = Amber LED
Bat1 = Blue LED
20mA drive pins
1=JTAG interface Reset disabled
0=Reset JTAG interface
32 KHz Clock
Same as Laguna
Place closely pin 58
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
SCHEMATIC,A4043
401648
Tuesday, October 28, 2008
38
53









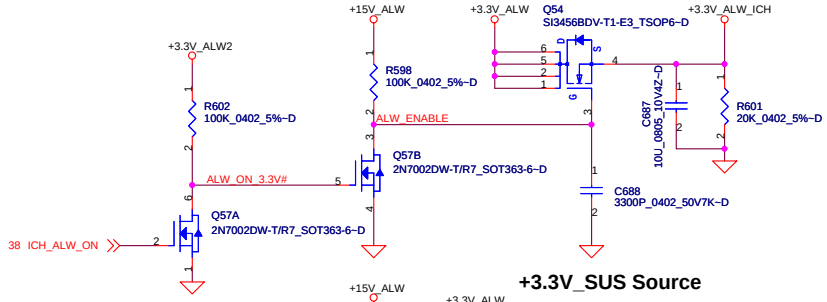


DELL CONFIDENTIAL/PROPRIETARY

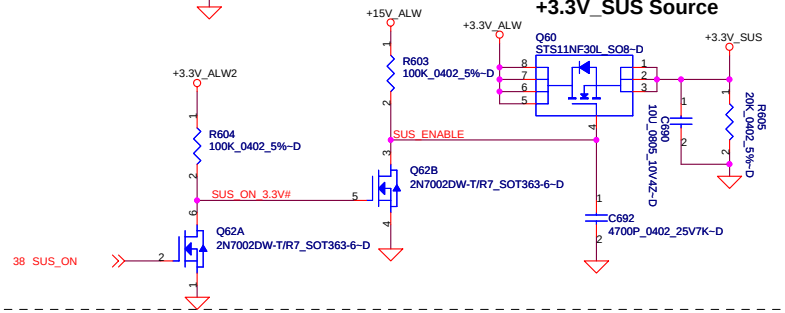
Compal Electronics, Inc.	
Title	SCHEMATIC,A4043
Size	Document Number 401648 Rev A
Date: Tuesday, October 28, 2008	Sheet 39 of 53

DC/DC Interface

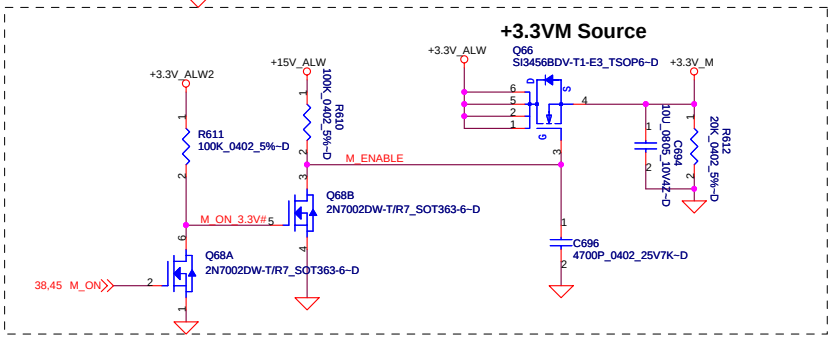
+3.3V_ALW_ICH Source



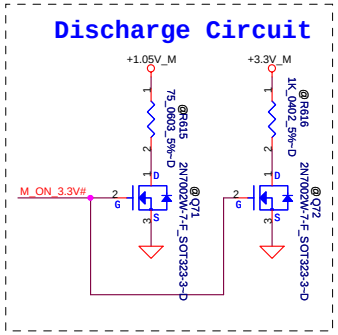
+3.3V_SUS Source



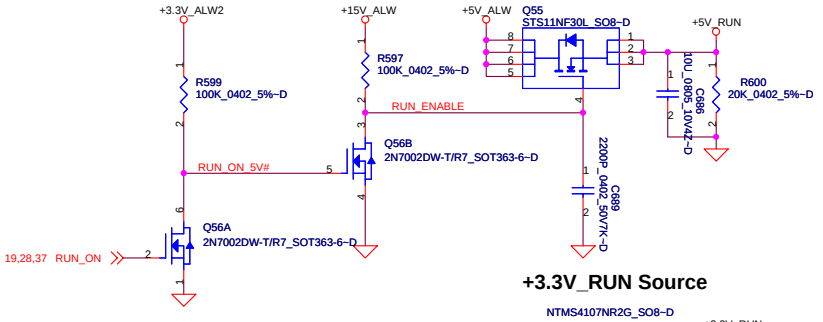
+3.3VM Source



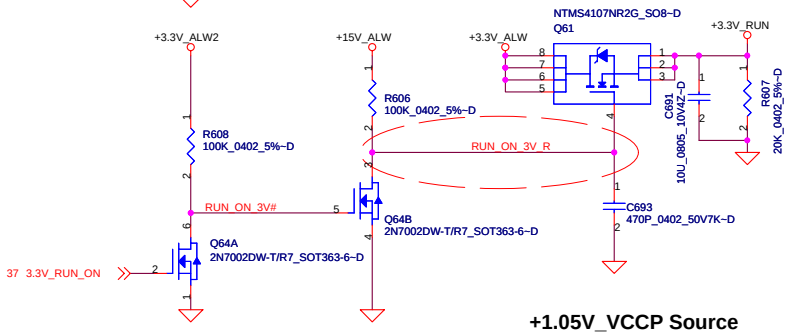
Discharge Circuit



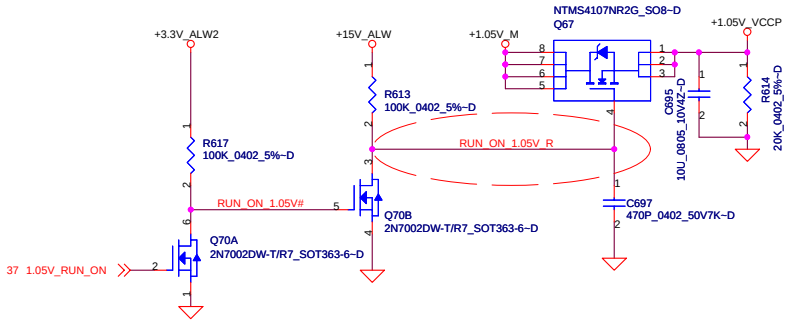
+5VRUN Source

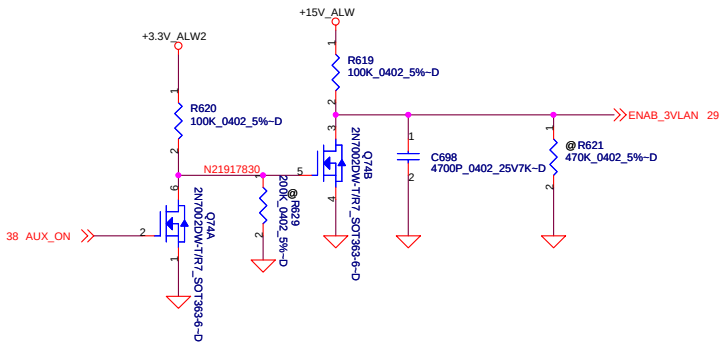


+3.3V_RUN Source

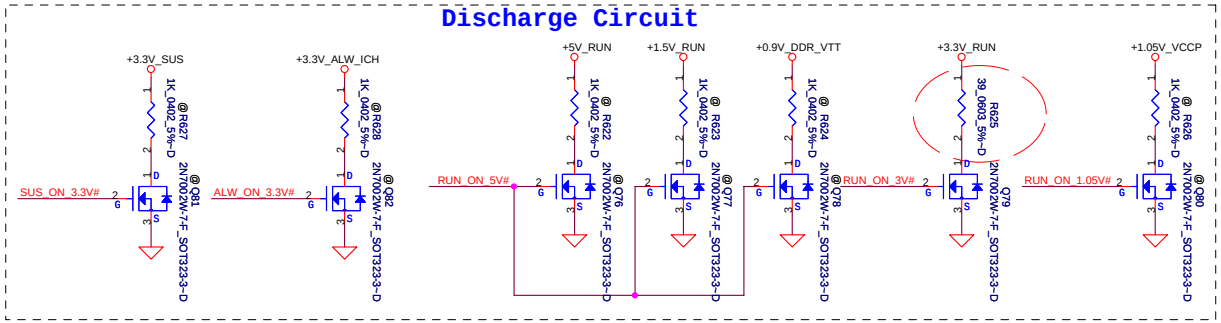


+1.05V_VCCP Source





Discharge Circuit

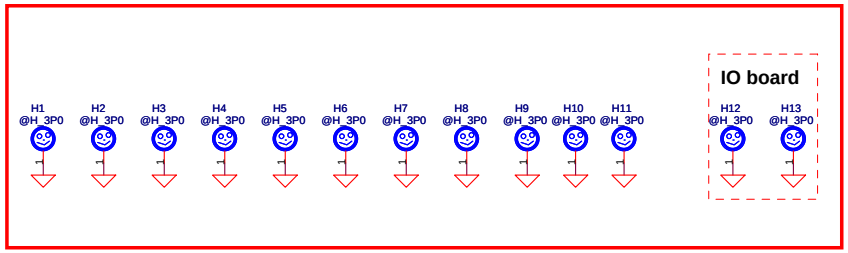


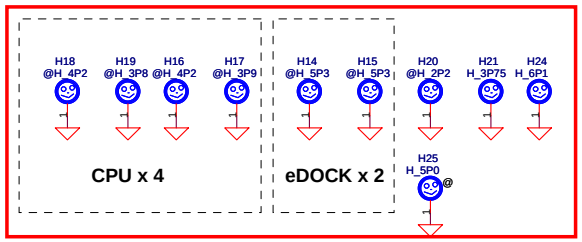
Compal Electronics, Inc.

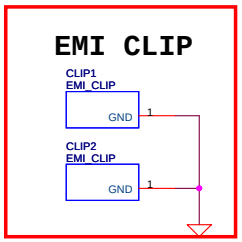
Title: SCHEMATIC,A4043

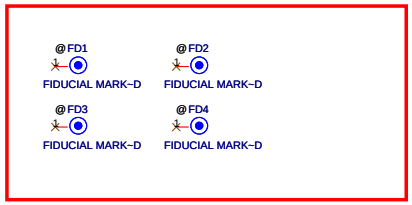
Size | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 40 of 53



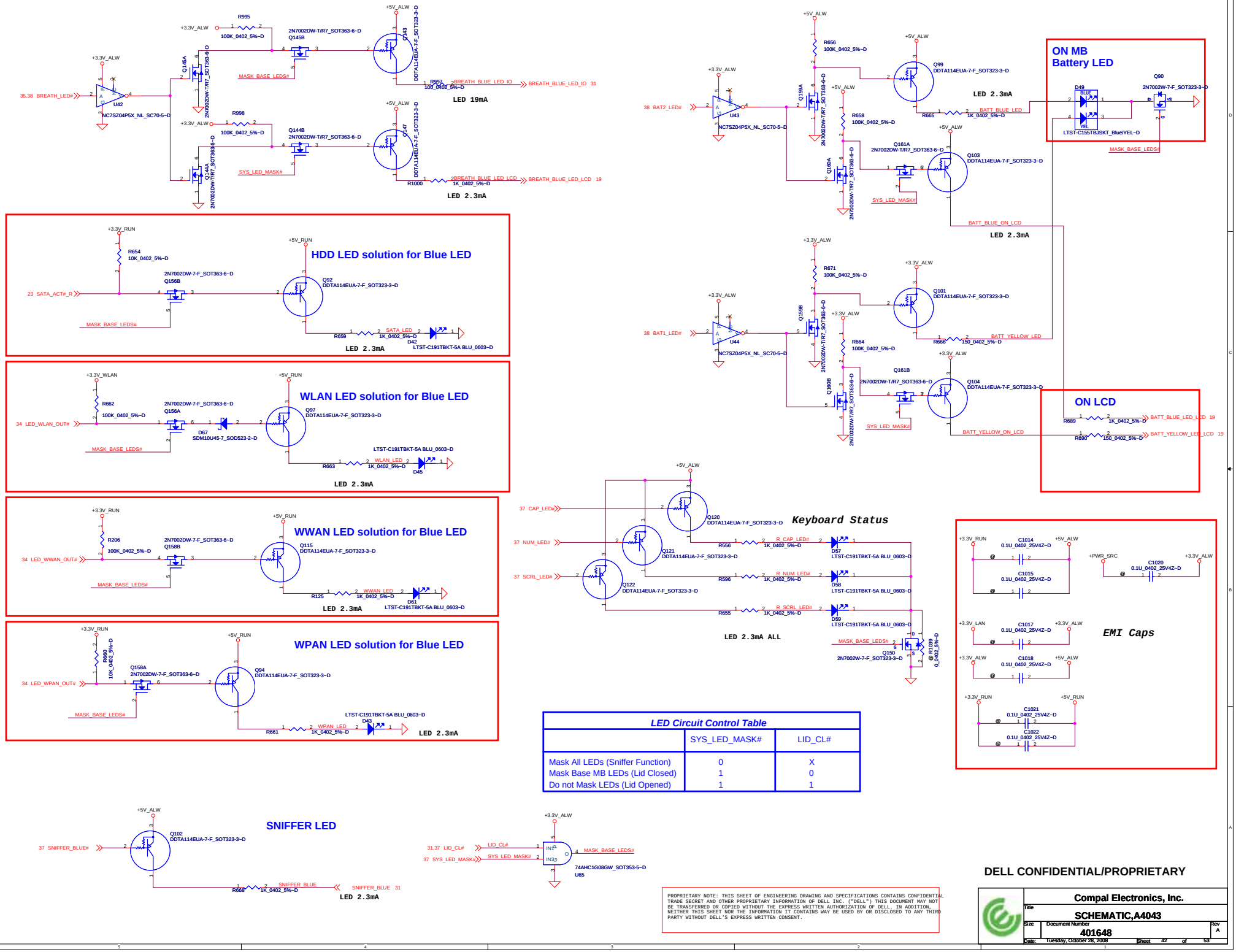






DELL CONFIDENTIAL/PROPRIETARY

	Compal Electronics, Inc.
Title	SCHEMATIC,A4043
Size	Document Number: 401648 — Rev: A
Date: Tuesday, October 28, 2008	Sheet 41 of 53



LED Circuit Control Table

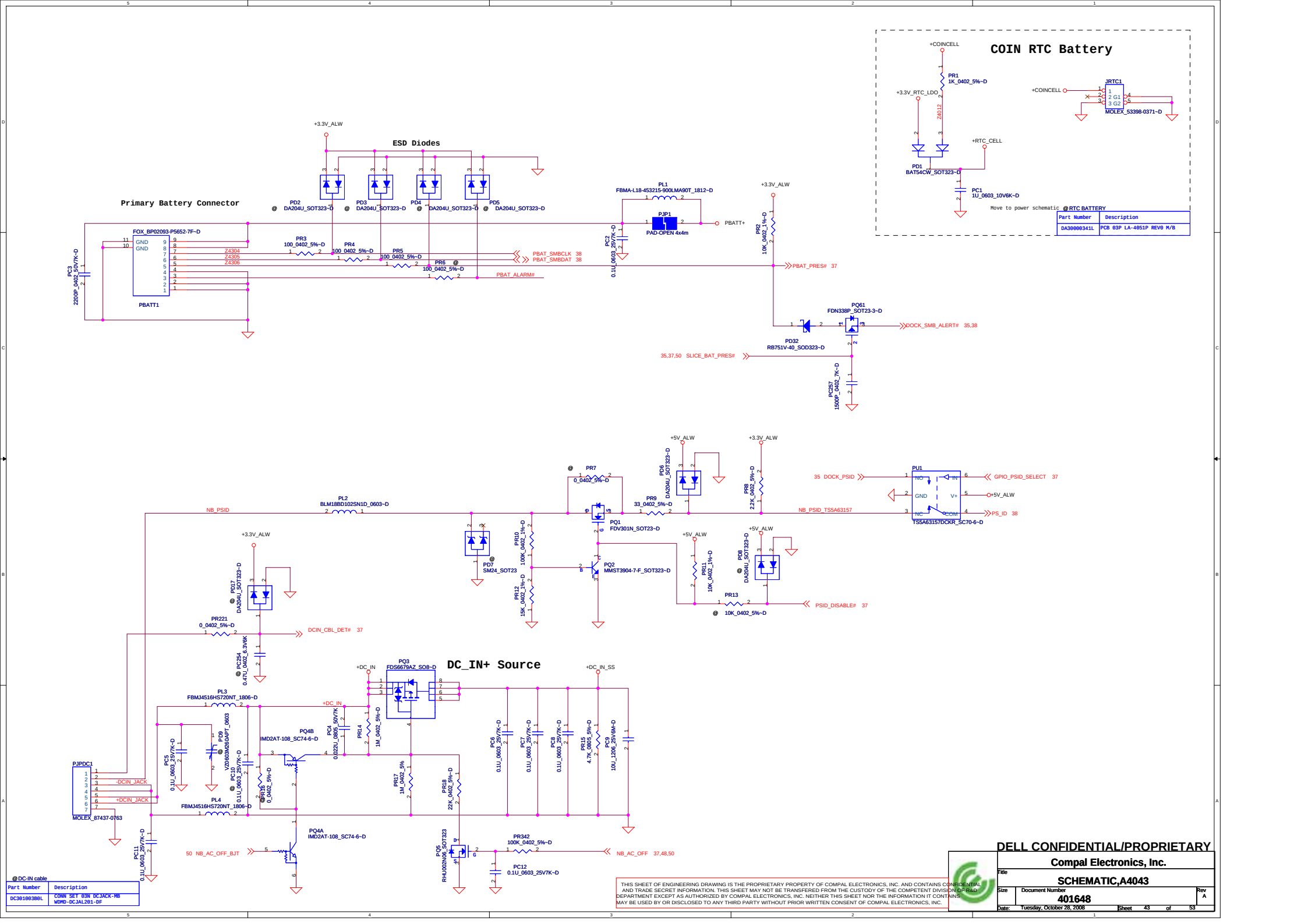
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Compal Electronics, Inc.

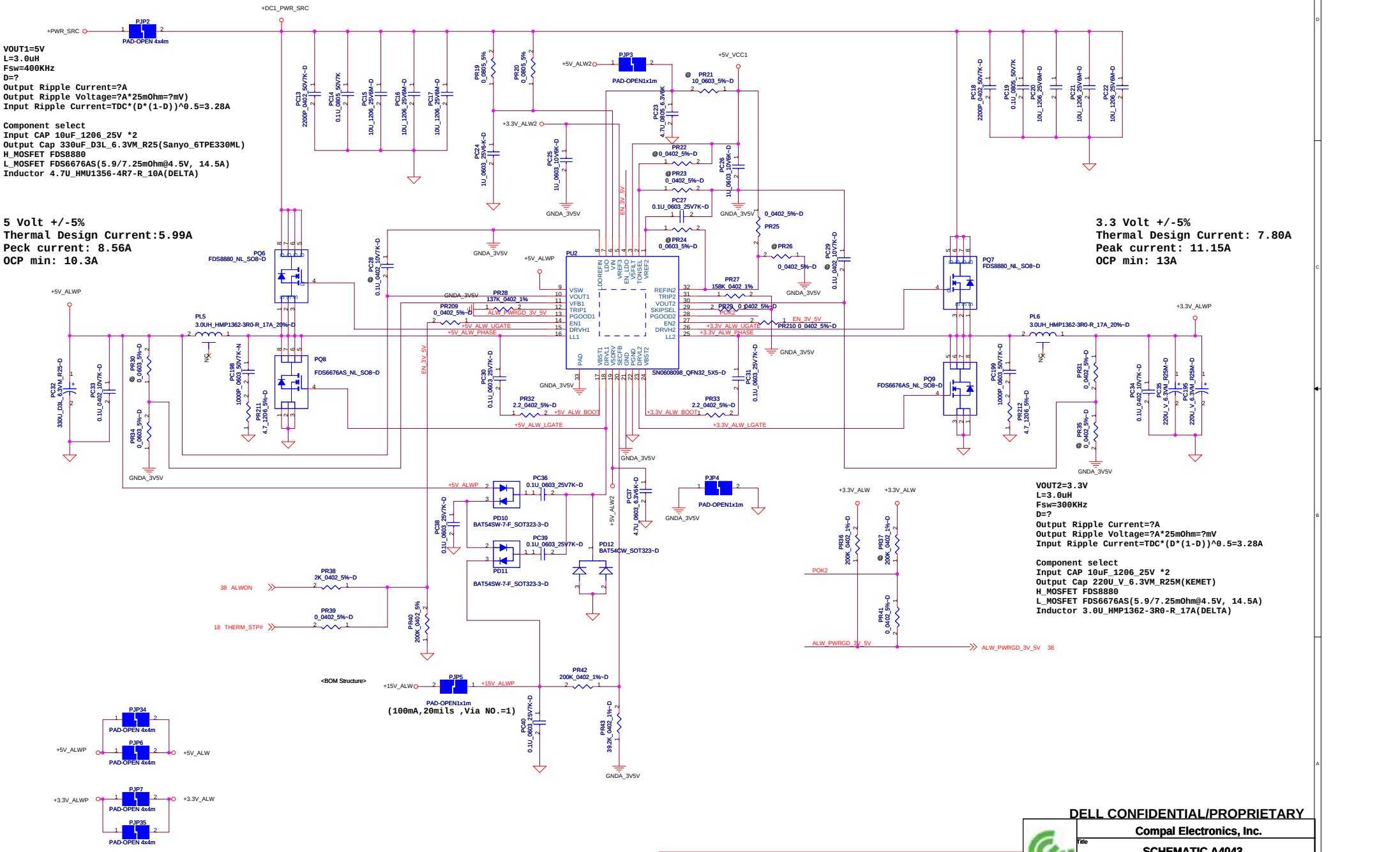
Title: SCHEMATIC,A4043

Size: Document Number: 401648 Rev: A

Date: Tuesday, October 28, 2008 Sheet 42 of 53

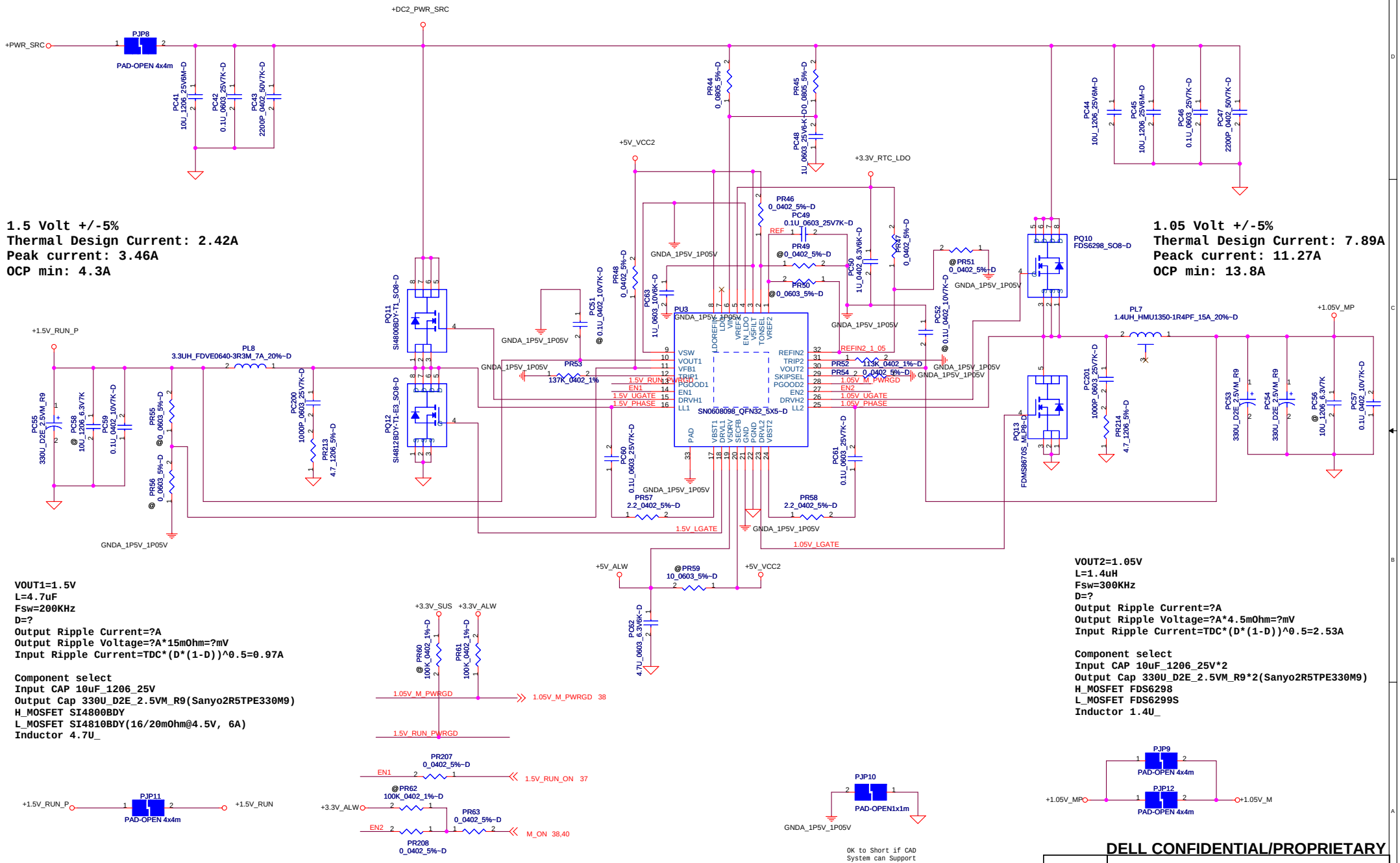


+3.3V_ALWP/ +5V_ALWP/ +5V_ALW2 / +15V_ALWP



Compal Electronics, Inc.	
Title	SCHEMATIC,A4043
Size	Document Number: 401648
Rev	A
Date: Tuesday, October 28, 2008	Sheet 44 of 53

+1.5V_RUN / +1.05V_M/ +3.3V_RTC_LDO



Compal Electronics, Inc.

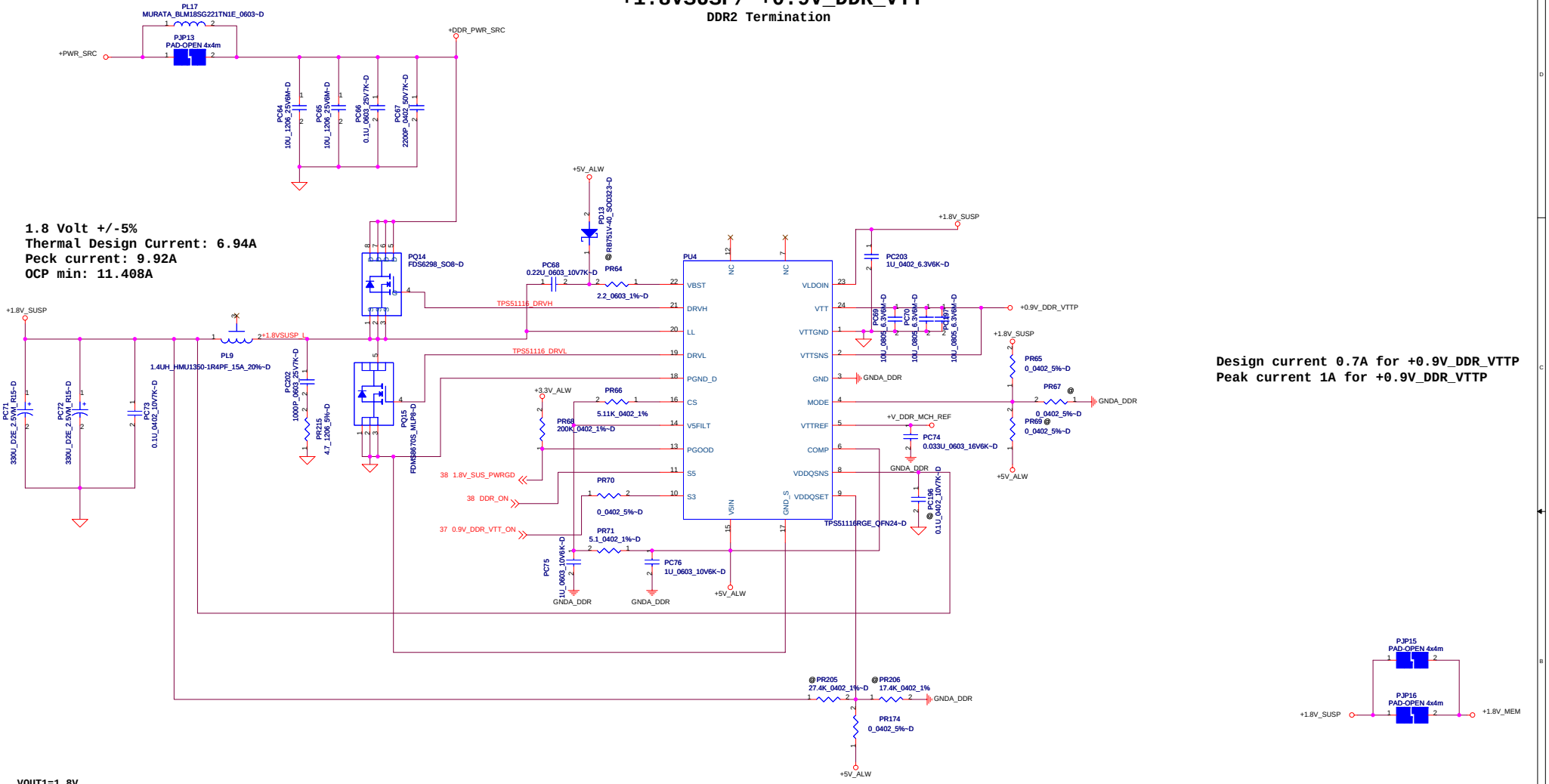
Title: SCHEMATIC,A4043

Size | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 45 of 53

+1.8VSUSP/ +0.9V_DDR_VTT

DDR2 Termination

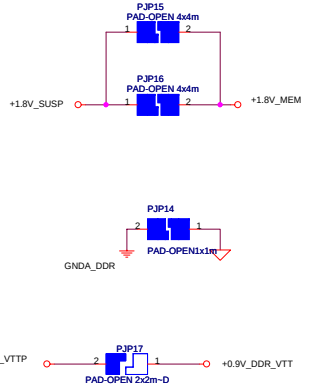


1.8 Volt +/-5%
Thermal Design Current: 6.94A
Peck current: 9.92A
OCP min: 11.408A

Design current 0.7A for +0.9V_DDR_VTTP
Peak current 1A for +0.9V_DDR_VTTP

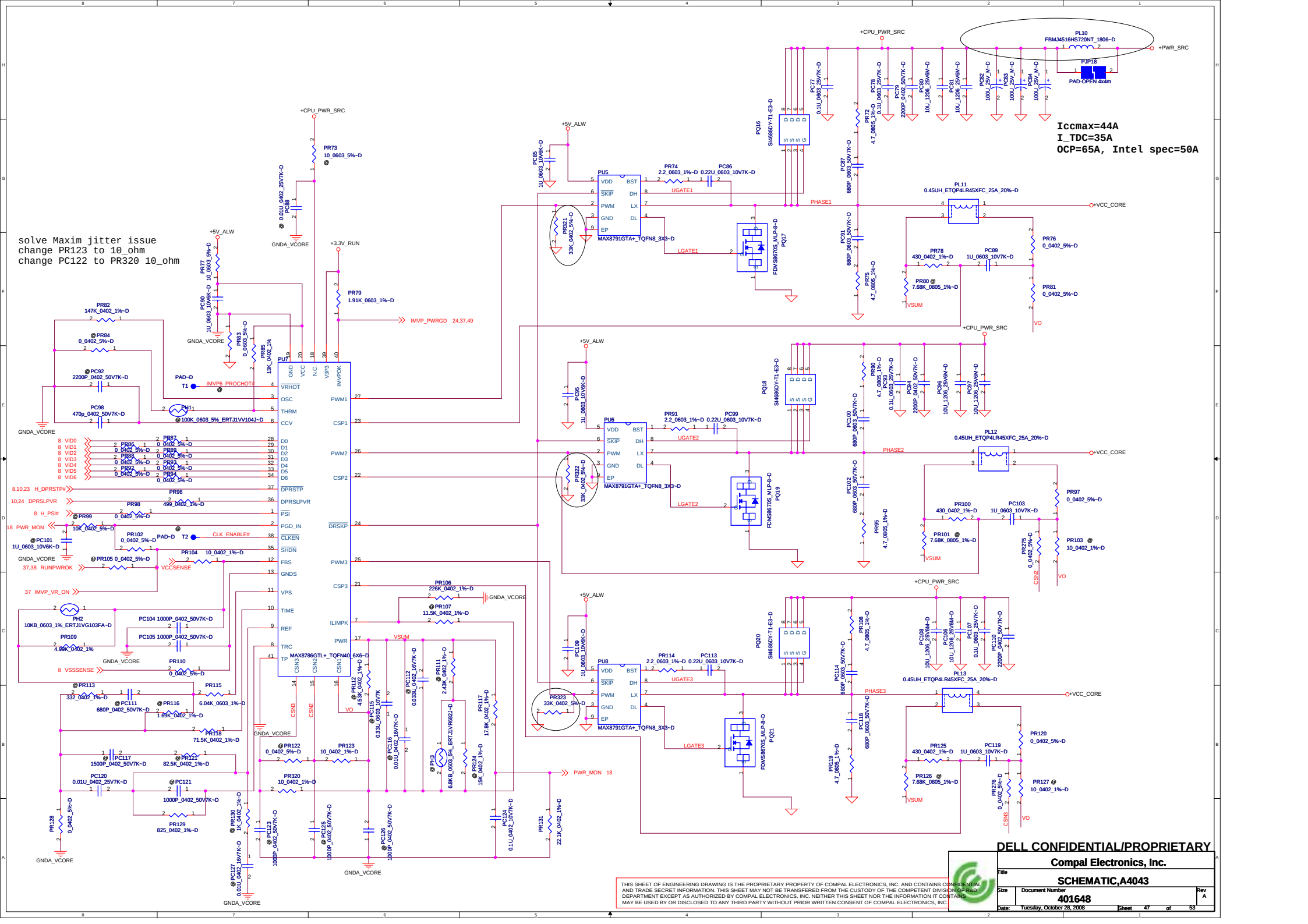
VOUT1=1.8V
L=1.4uH
Fsw=400KHz
D=?
Output Ripple Current=?A
Output Ripple Voltage=?A*15mOhm=?mV
Input Ripple Current=TDC*(D*(1-D))^0.5=0.97A

Component select
Input CAP 10uF_1206_25V
Output Cap 330U_D2E_2.5VM_R9*2(Sanyo2R5TPE330M9)
H_MOSFET FDS6298
L_MOSFET FDS6299S
Inductor 1.4U_



Compal Electronics, Inc.

Title	SCHEMATIC,A4043	
Size	Document Number 401648	Rev A
Date: Tuesday, October 28, 2008	Sheet 46 of 53	


solve Maxim jitter issue
change PR123 to 10_ohm
change PC122 to PR320 10_ohm
Iccmax=44A
I_TDC=35A
OCP=65A, Intel spec=50A
MAX8786GTL+_TQFN40_6X6~D
MAX8791GTA+_TQFN8_3X3~D
SI4686DY-T1-E3~D
FDMS8670S_MLP-8~D
PL10 FBMJ4516HS720NT_1806~D
PL11 0.45UH_ETQP4LR45XFC_25A_20%~D
PL12 0.45UH_ETQP4LR45XFC_25A_20%~D
PL13 0.45UH_ETQP4LR45XFC_25A_20%~D
+CPU_PWR_SRC
+5V_ALW
+3.3V_RUN
+VCC_CORE
+PWR_SRC
GNDA_VCORE
VSUM
VO
IMVP_PWRGD 24,37,49
PWR_MON 18
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
SCHEMATIC,A4043
401648
Tuesday, October 28, 2008
Sheet 47 of 53

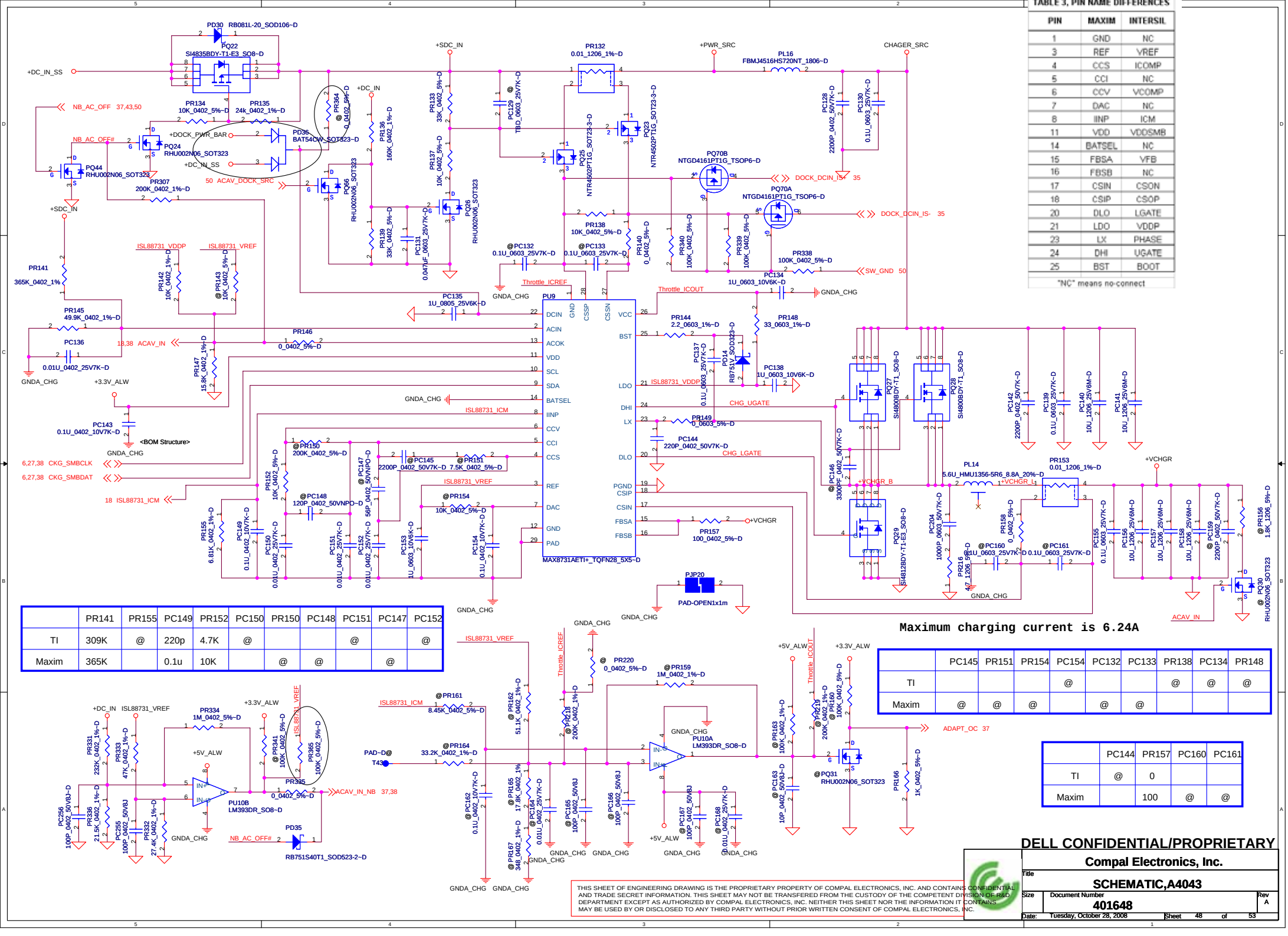


TABLE 3, PIN NAME DIFFERENCES

PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT

"NC" means no-connect

	PR141	PR155	PC149	PR152	PC150	PR150	PC148	PC151	PC147	PC152
TI	309K	@	220p	4.7K	@			@		@
Maxim	365K		0.1u	10K		@	@		@	

	PC145	PR151	PR154	PC154	PC132	PC133	PR138	PC134	PR148
TI				@			@	@	@
Maxim	@	@	@		@	@			

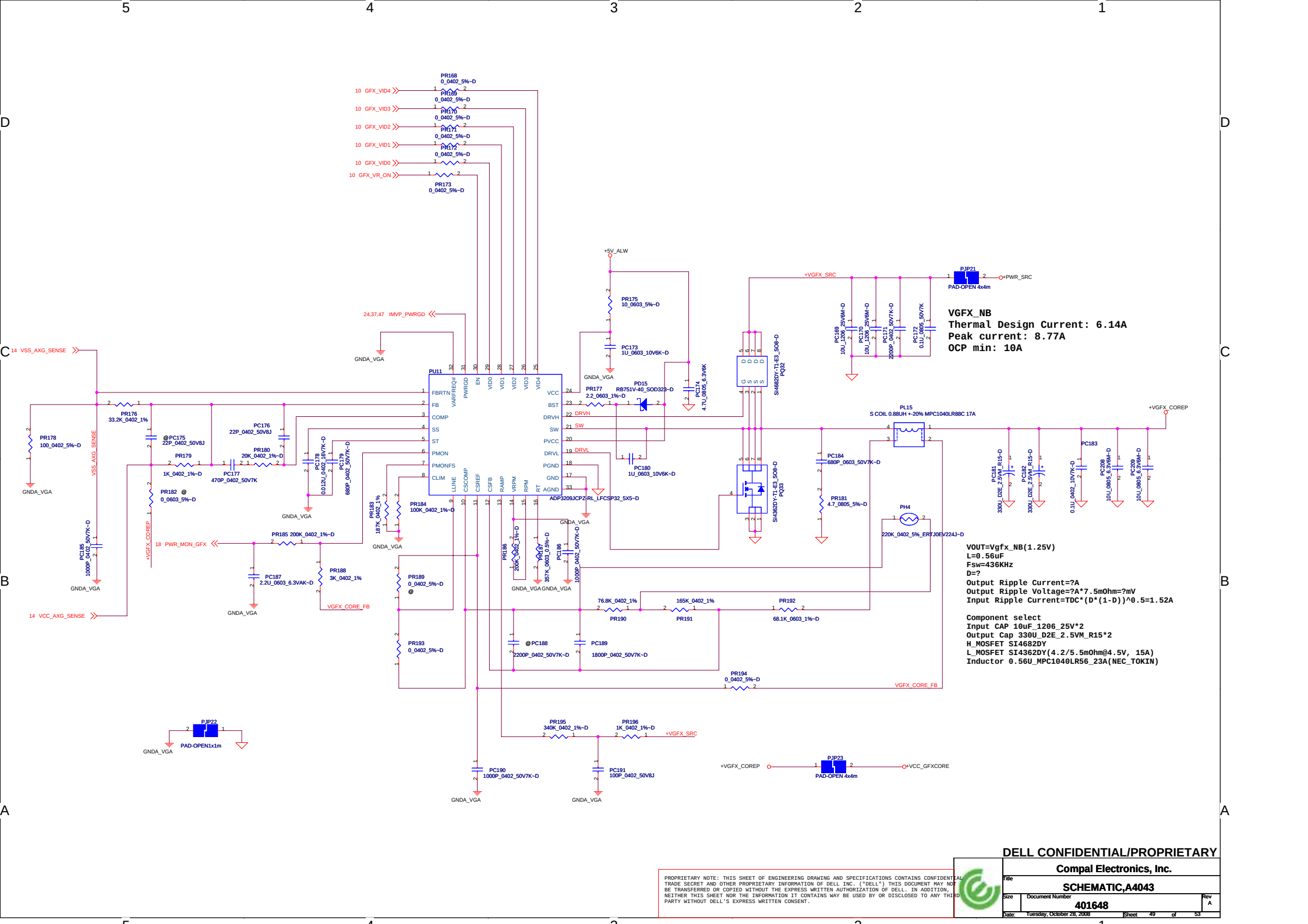
	PC144	PR157	PC160	PC161
TI	@	0		
Maxim		100	@	@

Compal Electronics, Inc.

Title: SCHEMATIC,A4043

Size: | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 48 of 53

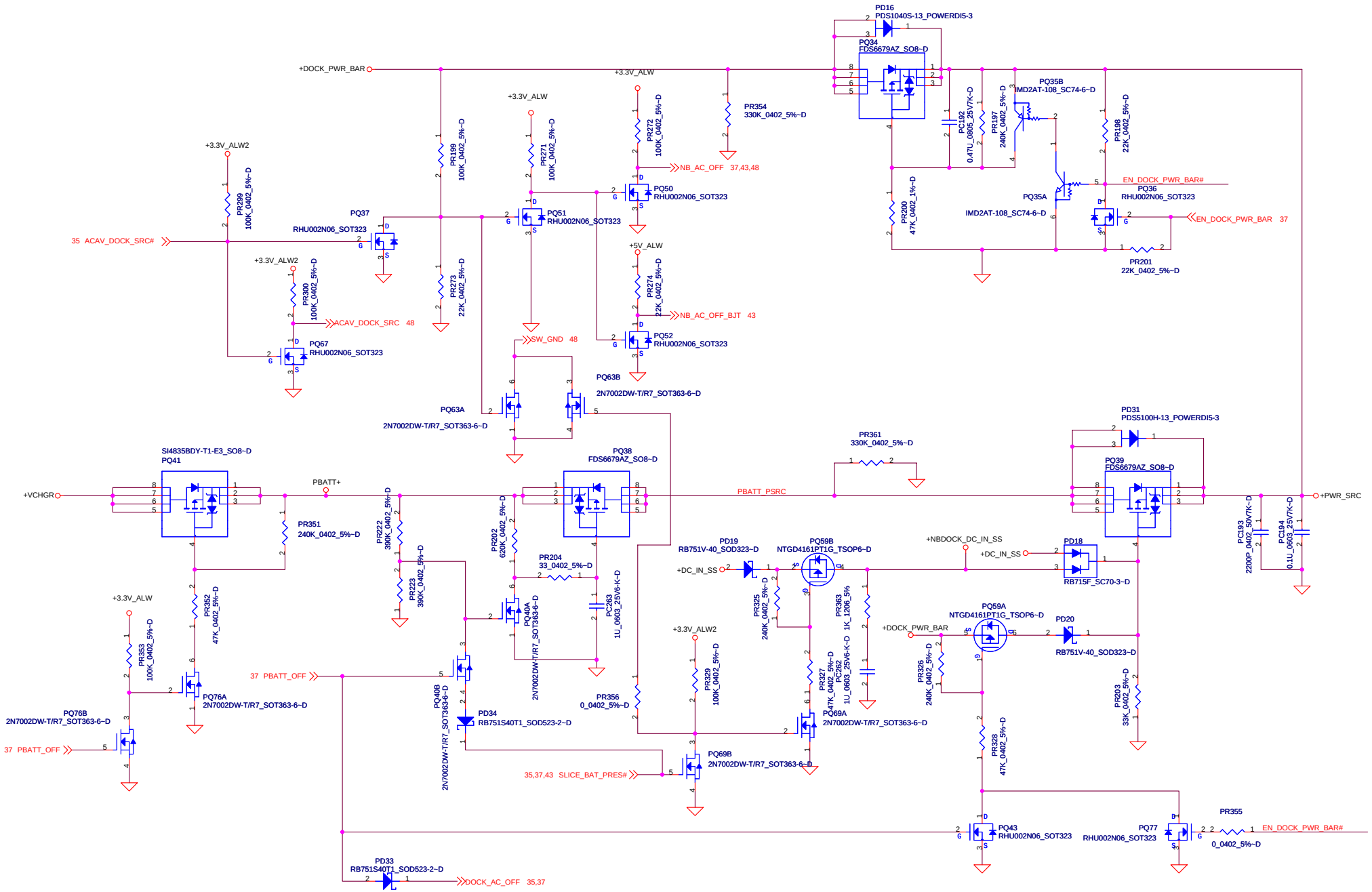


Compal Electronics, Inc.

Title: SCHEMATIC,A4043

Size: | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 49 of 53



DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: SCHEMATIC,A4043

Size | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 50 of 53

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	10	MCH HDA	09/23/2008	Compal	Support 1.5V MDC module. Delete bi-derectional level shift circuit.	Delete U67 and enable circuit, delete R42, R44, R686, R687 and change R685 to 33ohm.	X00
2	10	MCH	09/23/2008	Compal	Eliminate Power Sequence circuit, ICH_PWRGD change to RESET_OUT	Change U2.AT40 (Cantiga PWROK) to RESET_OUT	X00
3	18	Thermal	09/23/2008	Compal	Eliminate 2.5V_RUN_PWRGD. System do not use +2.5V_RUN power plan.	Delete U3 Pin 34 (4002 LDO_POK).	X00
4	24	ICH	09/23/2008	Compal	Eliminate Power Sequence circuit, ICH_PWRGD change to RESET_OUT	Change U10.G20 (ICH9M PWROK) to RESET_OUT	X00
5	25	MDC	09/23/2008	Compal	Support 1.5V MDC module. Delete bi-derectional level shift circuit.	Delete R314 R315, change +3.3V/1.5V_RUN_HDA to +1.5V_RUN, add U79 RICHTEK RT9013-15PB SOT23-5 to transfer +3.3V_ALW to +1.5V_ALW_HDA	X00
6	38	EC	09/23/2008	Compal	Eliminate Power Sequence circuit. RUNPWROK, SUSPWROK, 3.3V_M_PWRGD,3.3V_LAN_PWRGD become floating.	RUNPWROK add R1131 10K and pull high to +3.3V_RUN SUSPWROK add R1132 10K and pull high to +3.3V_SUS 3.3V_M_PWRGD add R1133 10K and pull high to +3.3V_M 3.3V_LAN_PWRGD add R1134 10K and pull high to +3.3V_LAN	X00
7	37	SIO	09/23/2008	Compal	Delete sniffer yellow circuit	Delete U35 Pin 10 sniffer yellow since don't used yellow LED.	X00
8	37	SIO	09/23/2008	Compal	Eliminate Power Sequence circuit, 2.5V_RUN_PWRGD change to 1.8V_RUN_PWRGD.	Change U3.34 (LDO_POK) and U35.18 to 1.8V_RUN_PWRGD.	X00
9	34	Mini Card	09/25/2008	Dell	By Dell comment , remove SM bus circuit of Mini card.To reach cost down.	Remove R429 R430 Q48 R433 R434 Q49.	X00
10	21	Display Port	09/25/2008	Compal	Change DP switch to Pericom PI2VDP8100.	Change U9 to PI2VDP8100, delete switch on mother board side (U75, U76 and circuit around).	X00
11	33	ESATA	09/25/2008	Compal	For cost down consideration.Change cheaper ESATA reapter.	Change ESATA reapter from SA00002D80L to SA00002YQ0L.	X00
12	38	EC	09/25/2008	Compal	Follow MINICOOPER named RESET_OUT# as RESET_OUT	Rename RESET_OUT# to RESET_OUT	X00
13	27	Codec	09/25/2008	Compal	Support 1.5V MDC module. Delete bi-derectional level shift circuit.	Change U16 Pin3 (DVDD_IO) from +3.3V_RUN to +1.5V_RUN.	X00
14	25	ICH	09/26/2008	Compal	Change +1.5V_ALW_HDA source plane.	Change U79 Pin1 to +3.3V_ALW_ICH.	X00
15	33	MDC	09/26/2008	Compal	Support 1.5V MDC module.	Change JIO1 Pin 35 from +3.3V_SUS to +3.3V_ALW_ICH. Add Pin 39 +1.5V_ALW_HDA.	X00
16	24	Flash ROM	10/02/2008	Compal	Depop 2nd SPI flash ROM	Depop R214,R387,R386,R1060,R375,R383,C392,R384,U13	X00
17	23	SB	10/02/2008	Compal	For low cost consideration, change Y1 for cheaper crystal.	Change Y1 form 32.768KHZ_12.5PF_1TJE125DP1 to 32.768KHZ 12.5PF 1TJS125DJ2A07	X00
18	36	USH I/F	10/03/2008	Compal	By Broadcom require to reserve location for RFID performance tuning.	Add R1138, R1139,R1140 but depop.	X00
19	33 37	BIO RFID	10/07/2008	Compal	Change connector type	Change JBIO1 to TYCO_2041070-6_6P-T. Chnage JCS1 to TYCO_2041084-6_6P-T	X00
20	34	SIM CARD	09/23/2008	Compal	Change SIM card slot.	Change JSIM1 to cost down SIM slot LTCX000EZ0L (TEMP: SP070711300)	X00

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	43	+DC_IN	11/17	leverage Roush	Battery slice need detect NB battery is insert or not.	Add PQ61 NTR4502PT1G, and PD32 RB751_SOD323 Connect to DOCK_SMB_ALERT# and SLICE_BAT_PRES#	X01
2	43	+DC_IN	11/17	leverage Roush	DCIN_CBL_DET# damage ECE5028	Add ESD diedo PD17 DA204U_SOT323 at DCIN_CBL_DET# Series PR221 1K_0402_5% between PJPDC1, PIN1 and DCIN_CBL_DET# Parallel PC254 0.47uF_0402_6.3V on DCIN_CBL_DET#	X01
3	43	+DC_IN	11/17	leverage Roush	Roush component and rework changes for Dcoking test	PC4 change form 0.47uF_0805_25V to 0.1uF_0805_25V PR14 change form 240K_0402_5% to 1M_0402_5% PR17 change form 47K_0402_1% to 220K_0402_5% PR18 change form 47K_0402_1% to 22K_0402_5% PR342 change form 0_0402_1% to 100K_0402_5%	X01
4	48	Charger	11/17	leverage Roush	NB DC blocking MOSFET won't turn off when Dock AC insert.	Add PQ44 RHU002N06 control NB DC blocking MOSFET. Control singal is NB_AC_OFF Series PR284 200K_0402_1% between PQ44 PIN1 and ACAV_IN Add PD30 B540C parallel PQ34	X01
5	48	Charger	11/17	leverage Roush	Charger of ISL88731 will turn off When ACIN is no power	Add LM393 to replace ISL88731 ACOK function(PU11B)	X01
6	48 50	Charger Selector	11/17	leverage Roush	+PWR_SRC exist on Docking connector through the DOCK_DCIN_IS+ and -	Add PQ62 NTGD4161PT1G series DOCK_DCIN_IS+ and - Add PQ63 RHU002N06 to control PQ62 on/off	X01
7	48 50	Charger Selector	11/17	leverage Roush	A global signal name change for all notebooks	From "ACAV_IN_DOCK" to "ACAV_DOCK_SRC" From "ACAV_IN_DOCK#" to "ACAV_DOCK_SRC#"	X01
8	48	Charger	11/17	leverage Roush	SCH165050: Validate EMC4002 VIN1/VCP1/VCP2 for UMA & Discrete for PT1 SMT	Depop UL circuit.	X01
9	50	Selector	11/17	leverage Roush	PBATT DC blocking MOSFET won't turn off when Docking AC insert. It will cause Battery or adapter protect.	Add PD18 RB715F_SOT323, PD20 and PD19 RB751V_SOD323, PR329 100K_0402_5% PR328 and PR327 47K_0402_5%, PR326 and PR325 240K_0402_5% PQ69 2N7002DW-7-F_SOT363-6, PQ59 NTG6161PT1G_TSOP6 Extra net name add +NBDOCK_DC_IN_SS from Docking connector	X01
10	43	+DCIN	11/20	EE / SCH165224	follow HW change	To delete the RTC detection circuit	X01
11	48 50	Selector charger	11/30	Dell	for slice function implement	change charger output to FB pin15 net name from PBATT+ to +VCHGR Add PQ41 PQ70 PR351 PR352 PR353 between +VCHGR and PBATT+	X01
12	43	+DCIN	12/17	Dell	change DCIN connector for ESD issue of "DCIN_CBL_DET#"	from Molex_87437_0663 to MOLEX_87437-0763	X02
13	50	Selector	12/28	leverage Roush	follow Roush	change PQ63 from RHU002N06 to 2N7002DW ADD PD33 RB751V ADD PR354 ADD PQ77 RHU002N06 and PR355 0 ohm	X02
14	48	Charger	12/28	leverage Roush	follow Roush	Change PC131 from TBD to 0.047uF	X02

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
15	47	+Vcore	02/18	Dell / Maxim	Reduce Ring-backwithin 20mV when change bulk caps from 4*220uF to 3*270uF	PR129 change from 909 ohm to 825 ohm	
16	50	Selector	02/18	Merle DELL	Fix BITS CR196131 and CR196130	Add PR363 1K_1206 and PC262 1U_0603_25V from +NBDOCK_DC_IN_SS to ground Add PD35 RB751S40T1_SOD523-2 from NB_AC_OFF# to ACAV_IN_NB	
17	47	+Vcore	02/18	Maxim	Fix Jitter issue	change PR123 to 10_ohm change PC122 to PR320 10_ohm	
18	48/50	charger / selector	02/26	Compal	location change for Charger 2nd source X76 BOM control	change PR141 to PR217 change PR217 to PR141 change PR228 to PR218 change PR218 to PR351 change PR230 to PR219 change PR219 to PR352 change PR229 to PR220 change PR220 to PR353 change PR284 to PR307 change PQ62 to PQ70 change PQ70 to PQ76	
19	48	Charger	03/06	Compal	Delete non-use circuit	delete +DC_IN_SS to PR217 and PR217.	
20	50	Selector	03/06	Compal	For slice battery hot docking issue	Change PQ40 from IMD2AT to 2N7002DW change PR202 from240K_ohm ot 620k_ohm change PR204 from 47K_ohm to 33_ohm add PR222 390K_ohm and PR223 390K_ohm add PD34 RB751S40T1	
21	47	+Vcore	03/11	Maxim	For driver IC power down issue	Add PR321 PR322 PR323 from IC pin 2 to GND	
22	44-50	All	03/19	Compal	EMI solution	Change PR32 PR33 PR57 PR58 PR64 PR74 PR91 PR144 PR177 to 2.2_ohm Add PC198 PR211 PC199 PR212 PC200 PR213 PC201 PR214 PC202 PR215 PC87 PR72 PC91 PR75 PC100 PR90 PC102 PR95 PC114 PR108 PC118 PR119 PC204 PR216 PC184 PR181 PC128 PC130	
23	45	1.5V/1.05v	4/23	Compal	change non-lead free part to lead free part	PR47 change from SD03415830L to SD03415838L	
24	47	Vcore	4/23	Maxim	Driver IC power down issue need change resistor value	change PR321 PR322 PR323 to 33K	
25	49	ADP3209	4/23	Intel Compal	Follow Roush VGFX DC load line slope change to -7.5mOhm	Change PR192 from 75K_0603 to 68.1K_0603	
26	43	DC-IN	6/3	Compal	Glitch issue on SLICE_BAT_PRES#	Add PC257:SE074152K8L(S CER CAP 1500P 50V +-10% X7R 0402) between pin2 of PQ61 and GND.	
27	50	Selector	6/4	Compal	Reserve a pull high resistor between +3.3V_ALW2 and SLICE_BAT_PRES#	Add un-pop PR330:SD02847018L(S RES 1/16W 4.7K +-5% 0402) between +3.3V_ALW2 and PQ40B.5.	
28	48	Charger	9/11	Dell	reduce charger IC power consumption when battery mode	Add location PD36, PR364, PR365. Pop PD36 PR365. Un-pop PR364	
29	48	Charger	9/11	Dell / Compal	De-pop UL circuit	De-pop PR161 PR162 PR220 PR159 PR163 PR160 PC162 PR165 PR167 PC164 PC165 PC166 PC167 PC168 PC163 PQ31 Pop PR166	
30	48	Charger	10/22	Dell	using Guardian for UL compliance need to change PR155	change PR155 from 8.45K to 6.81K	

Compal Electronics, Inc.

Title: SCHEMATIC,A4043

Size: C | Document Number: 401648 | Rev: A

Date: Tuesday, October 28, 2008 | Sheet 53 of 53