MODEL NAME : *PLW00*

PCB NO : *LA-7451P*

BOM P/N : *TBD*

TBD

Dell/Compal Confidential

Schematic Document

Breitling (Huron River)

Sandy Bridge(BGA) + Cougar Point(standard)

DISCRETE VGA N12P-GV-S-A1 (optimus)

2011-07-12

Rev: 1.0

Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.

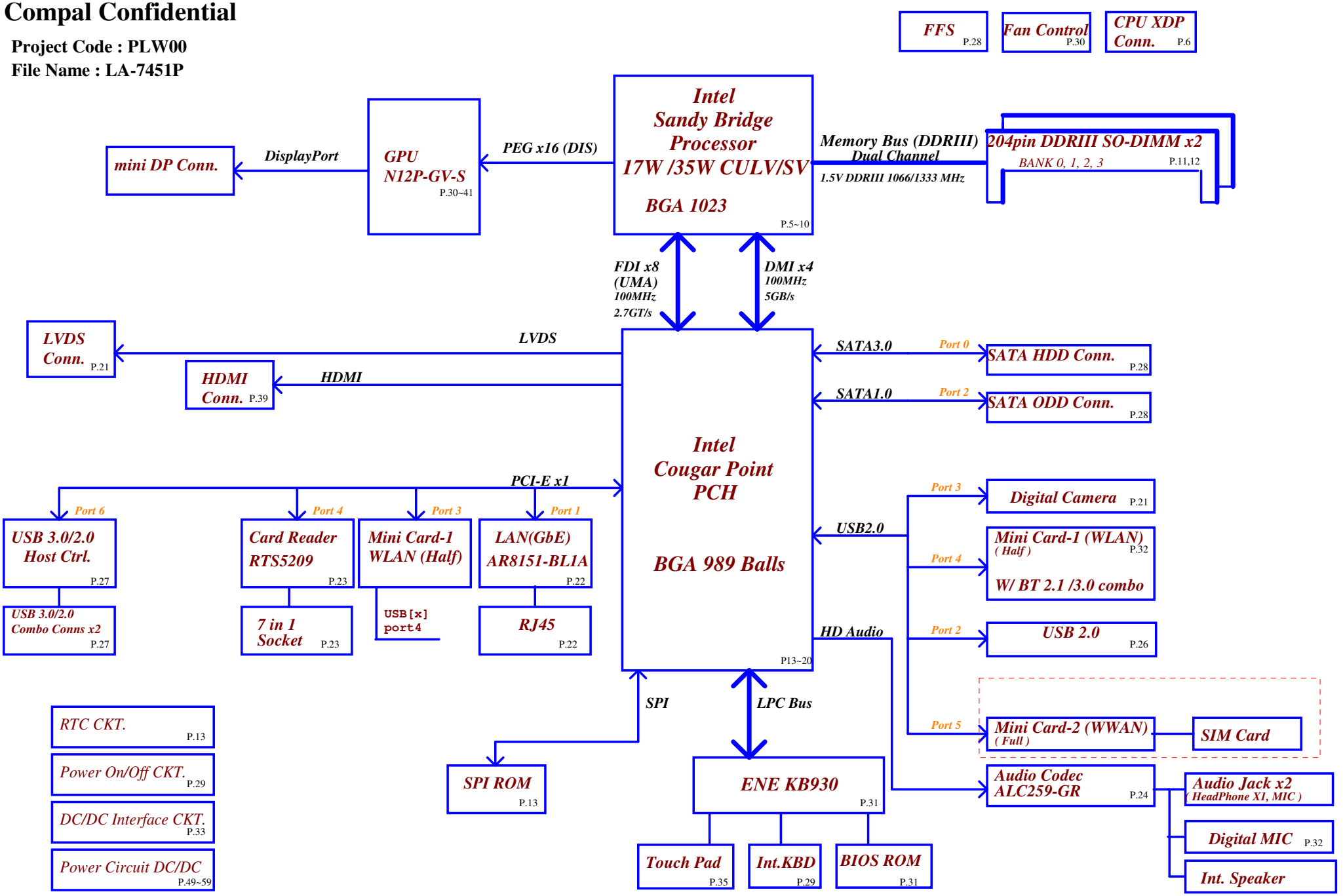
Title: *Cover Page*

Size | Document Number: *LA-7451P* | Rev: 1.0

Date: Thursday, July 28, 2011 | Sheet 1 of 49

Compal Confidential

Project Code : PLW00
File Name : LA-7451P



Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.

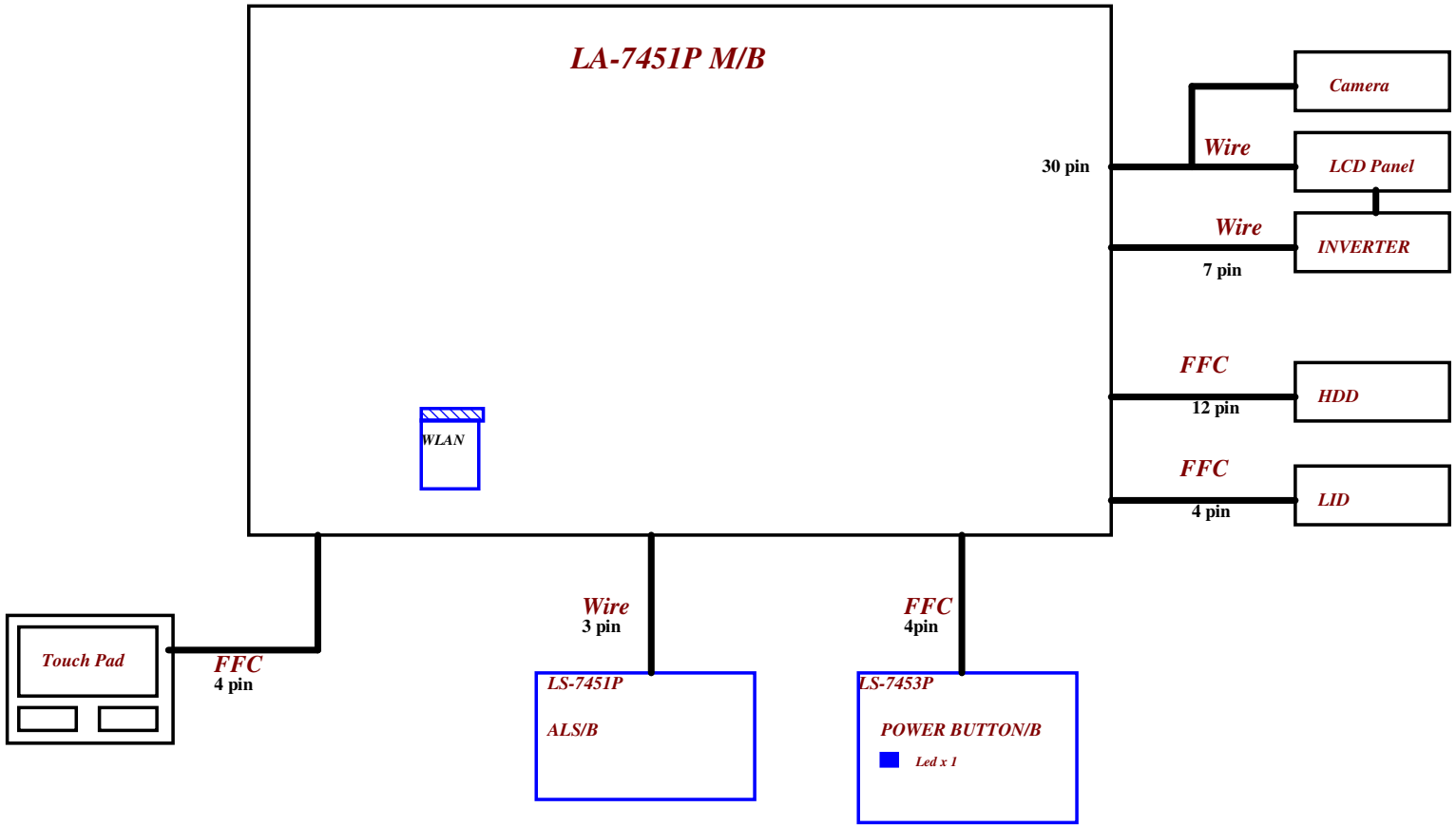
Title: **Block Diagram**

Size	Document Number	Rev
	LA-7451P	1.0

Date: Thursday, July 28, 2011 | Sheet 2 of 49

Compal Confidential

Project Code : PLW00
File Name : LA-7451P



Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.

Title: **Block Diagram**

Size	Document Number	Rev
		1.0

Date: Thursday, July 28, 2011 | Sheet 3 of 49

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

SMBUS Control Table

	SOURCE	BATT	SODIMM	SODIMM	FFS	VGA Thermal Sensor	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB930	V						
EC_SMB_CK2 EC_SMB_DA2	KB930							
PCH_SML0CLK PCH_SML0DATA	PCH							
PCH_SML1CLK PCH_SML1DATA	PCH						V	
MEM_SMBCLK MEM_SMBDATA	PCH		V	V	V			V

Link

PCH	USB PORT#	DESTINATION
	0	None
	1	JUSB1 (2.0 Ext UP Side)
	2	None
	3	CAMERA
	4	JMINI1 (WLAN)
	5	JMINI2 (WWAN)
	6	None
	7	None
	8	None
	9	None
	10	None
	11	None
	12	None
	13	None

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	MINI CARD-2 WWAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	USB 3.0		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

SATA	DESTINATION
SATA0	HDD
SATA1	ODD
SATA2	None
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	None
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

Symbol Note :

: means Digital Ground

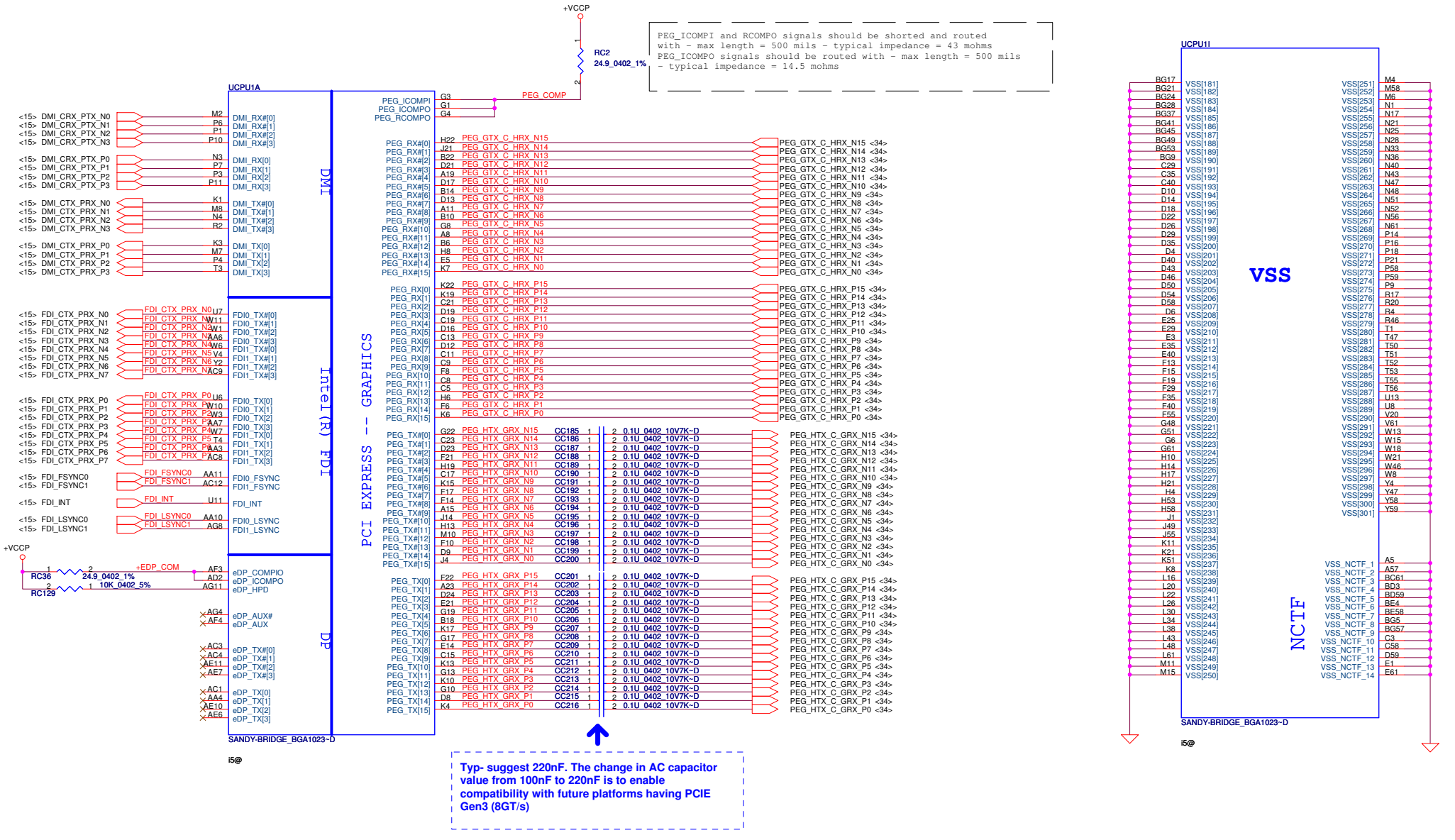
: means Analog Ground

Compal Electronics, Inc.

Title: Notes List

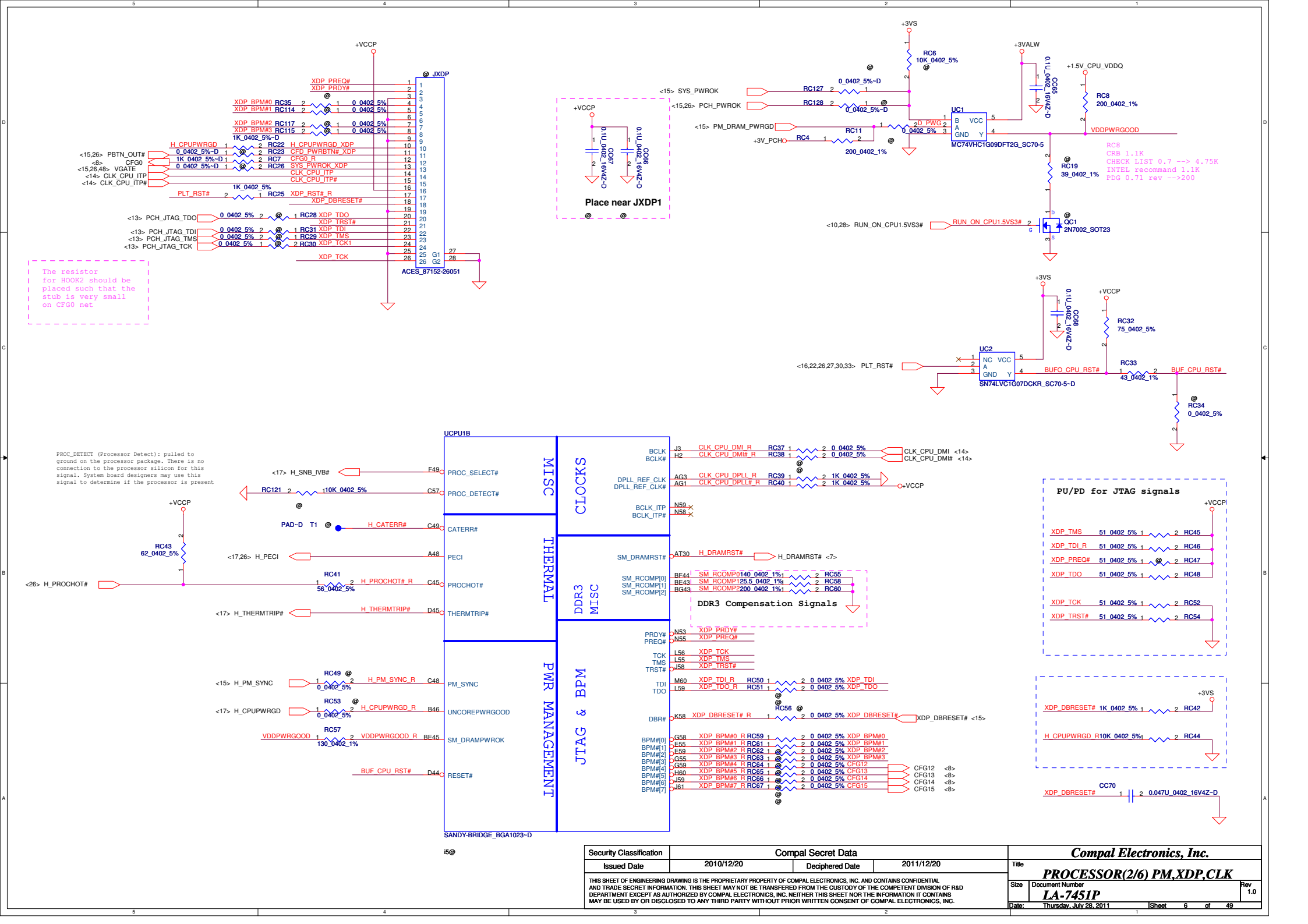
Size | Document Number: LA-7451P | Rev: 1.0

Date: Thursday, July 28, 2011 | Sheet 4 of 49



Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.			
Title: PROCESSOR(1/6) DMI,FDI,PEG			
Size	Document Number: LA-7451P		Rev: 1.0
Date: Thursday, July 28, 2011		Sheet 5 of 49	



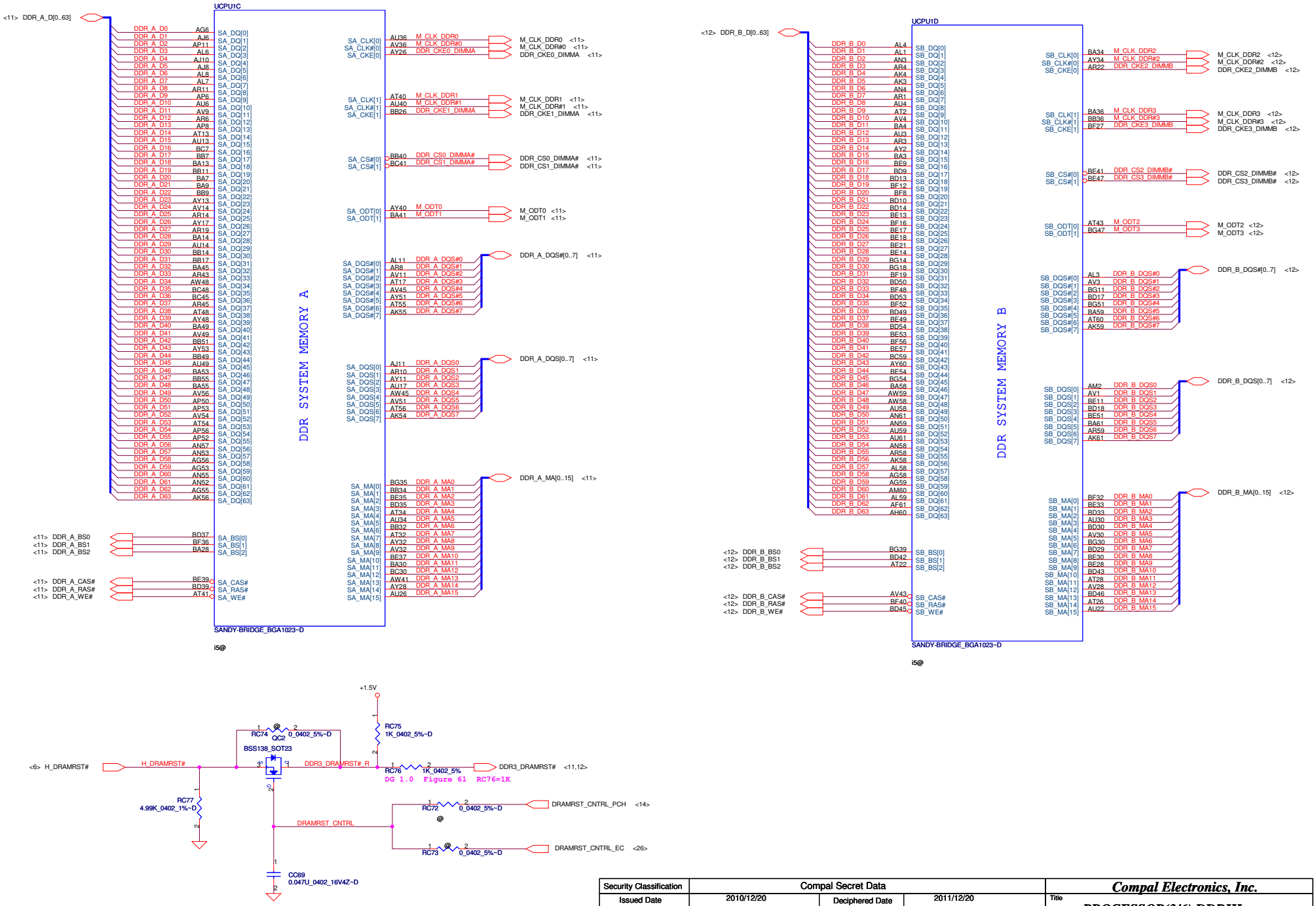
Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.

Title: PROCESSOR(2/6) PM,XDP,CLK

Size	Document Number	Rev
	LA-7451P	1.0

Date: Thursday, July 28, 2011 Sheet 6 of 49



Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

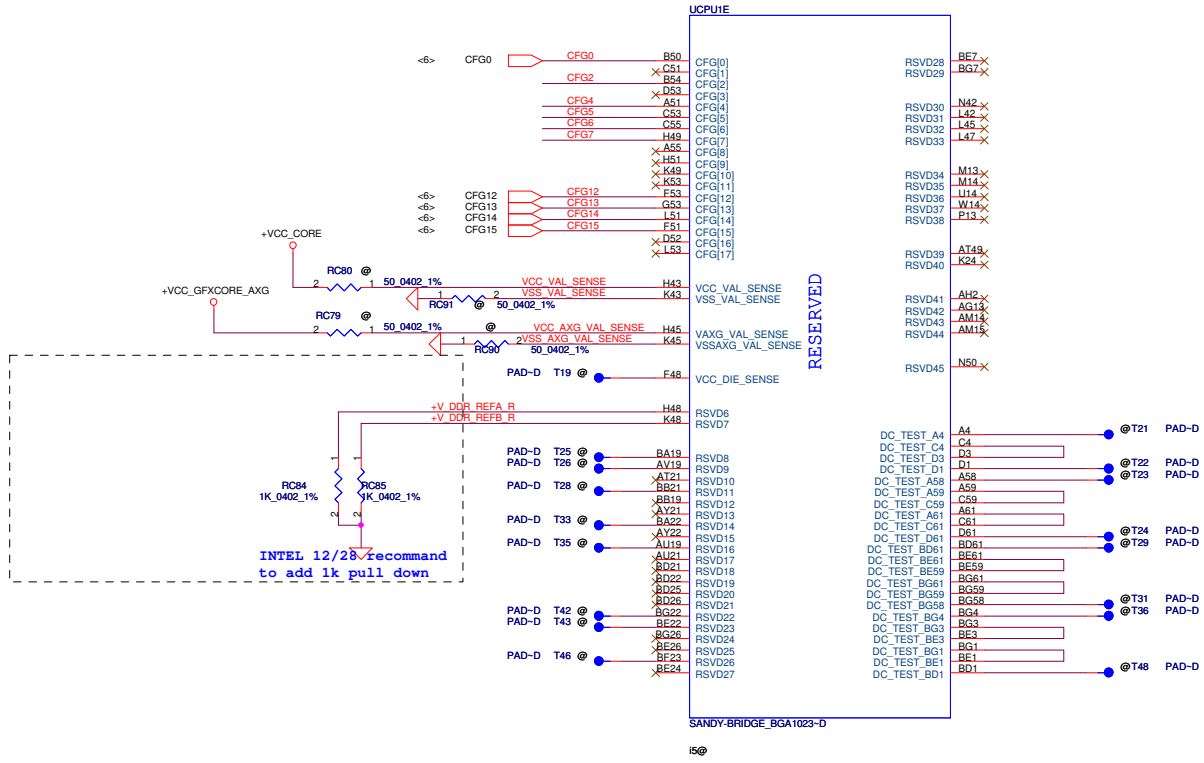
Compal Electronics, Inc.

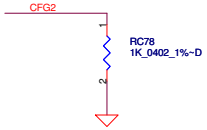
Title: **PROCESSOR(3/6) DDRIII**

Size	Document Number	Rev
	LA-7451P	1.0

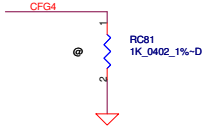
Date: Thursday, July 28, 2011 | Sheet 7 of 49

CFG Straps for Processor

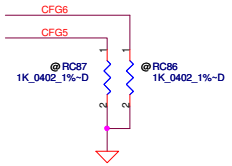




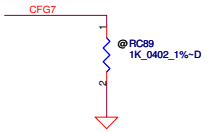
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	*1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	*1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.

Title: PROCESSOR(4/6) RSVD,CFG

Size	Document Number	Rev
	LA-7451P	1.0

Date: Thursday, July 28, 2011 Sheet 8 of 49

SV type CPU

53A

UCPU1F

18A

+1.05V

+VCCP

+VCC_CORE

POWER

CORE SUPPLY

PEG AND DDR

Cap quantity follow 43890_HR_CHKLST_Rev07

QUIET RAILS

SVID

SENSE LINES

High-Frequency Decoupling

Voltage selection for VCCIO: For Huron River platforms, this pin must be pulled high on the motherboard.

choose low or high

Place the PU resistors close to CPU

Place the PU resistors close to VR

SANDY-BRIDGE_BGA1023~D

i5@

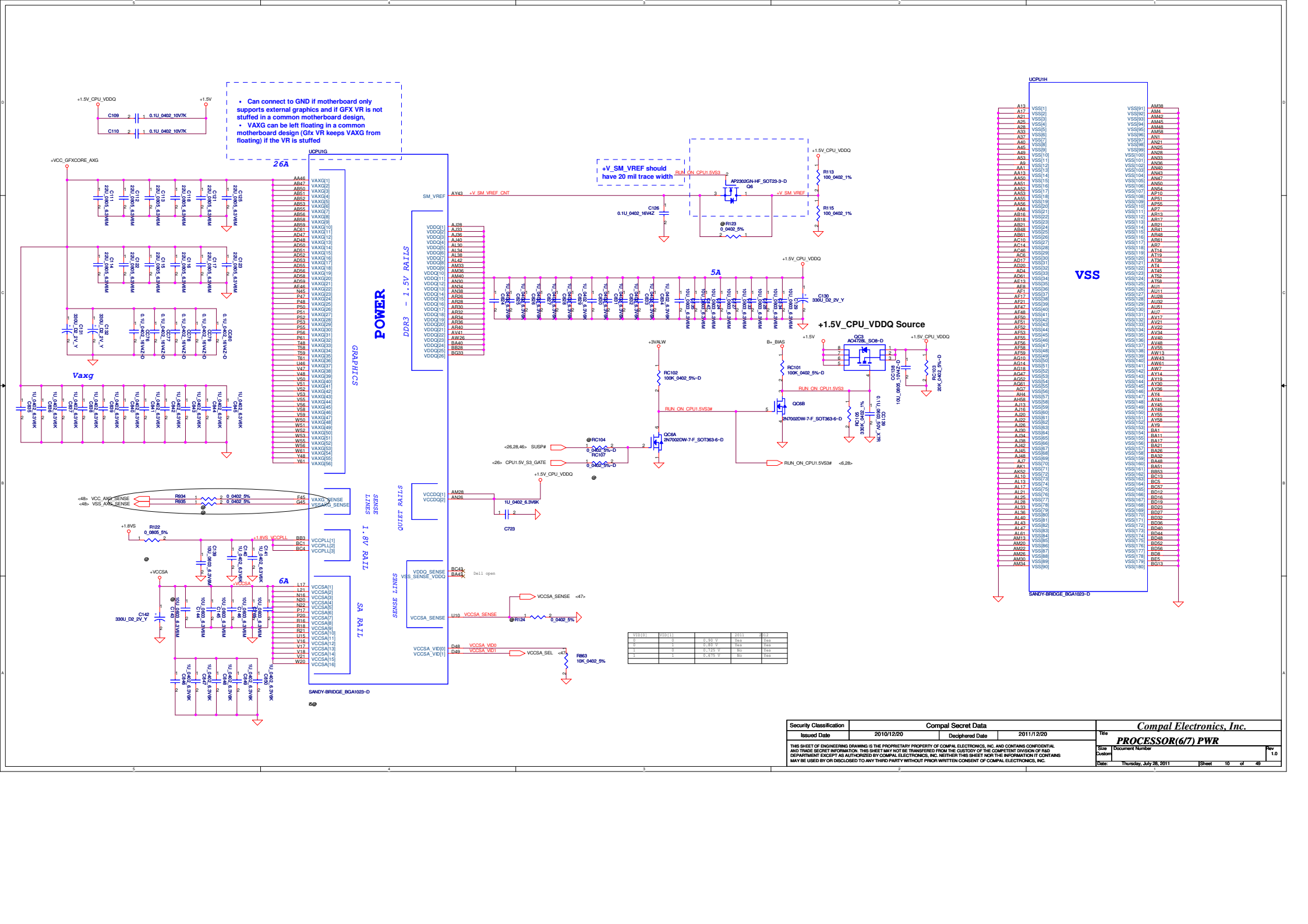
Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

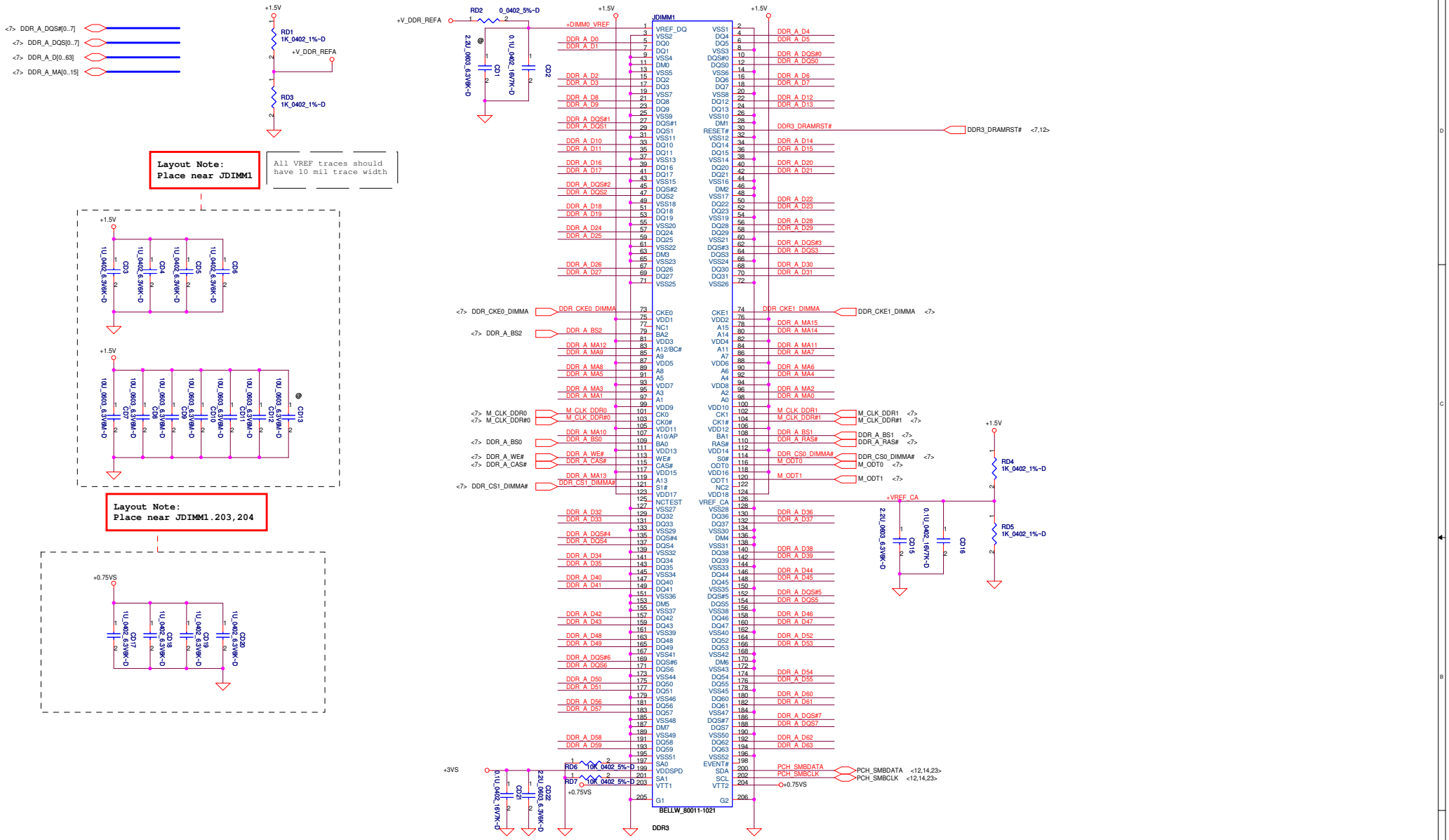
Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size	Document Number	Rev
Custom		1.0

Date: Thursday, July 28, 2011 | Sheet 9 of 49


• Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
• VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed
+V_SM_VREF should have 20 mil trace width
+1.5V_CPU_VDDQ Source
UCPU1G
UCPU1H
POWER
GRAPHICS
DDR3 - 1.5V RAILS
SENSE LINES
1.8V RAIL
QUIET RAILS
SA RAIL
Vaxg
VSS
SANDY-BRIDGE_BGA1023-D
Security Classification
Compal Secret Data
Issued Date
2010/12/20
Deciphered Date
2011/12/20
Compal Electronics, Inc.
PROCESSOR(6/7) PWR
Size
Custom
Document Number
Rev
1.0
Date:
Thursday, July 28, 2011
Sheet
10
of
49



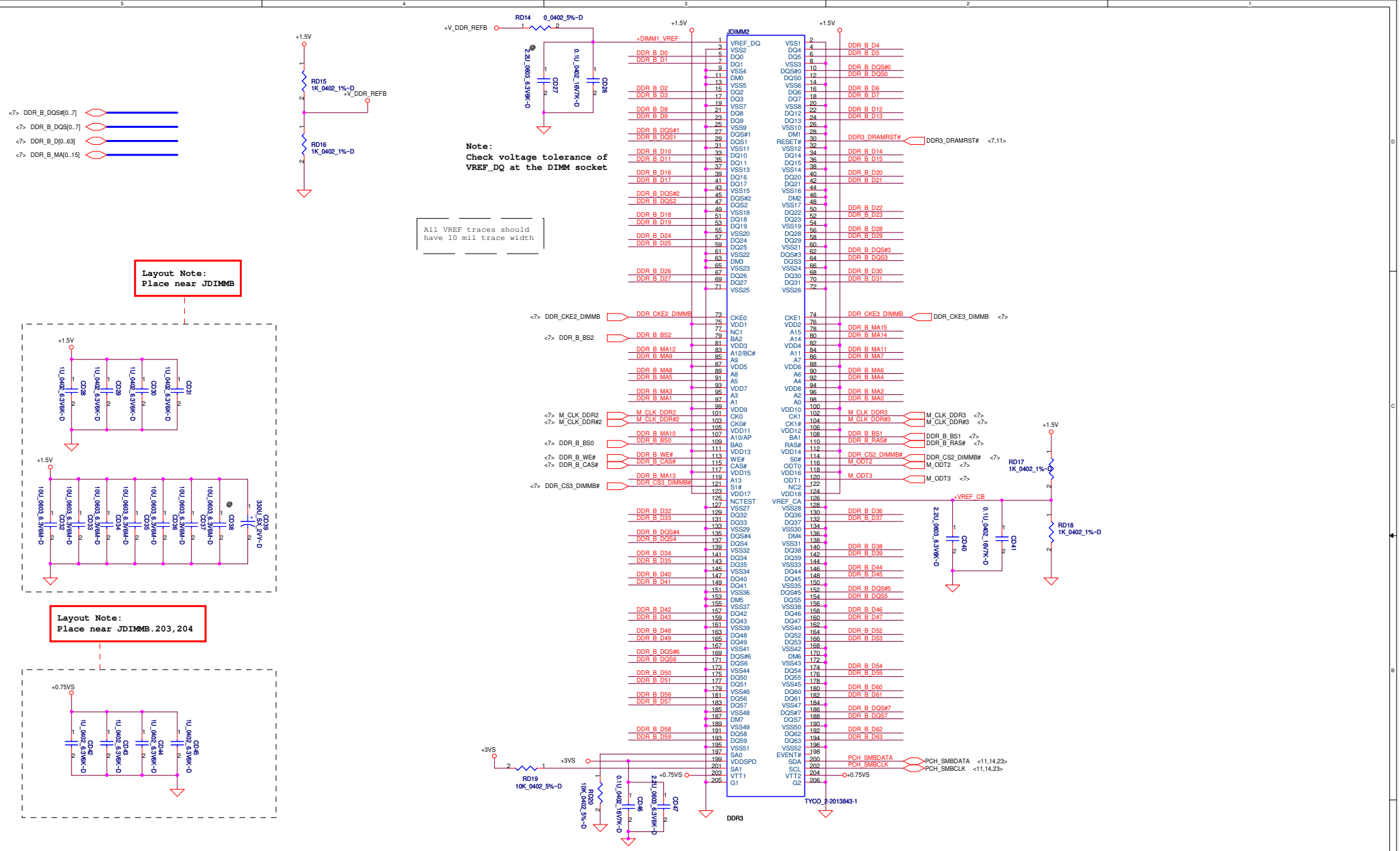
Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.

Title: **DDRIII DIMMA**

Size	Document Number	Rev
	LA-7451P	1.0

Date: Thursday, July 28, 2011 | Sheet 11 of 49



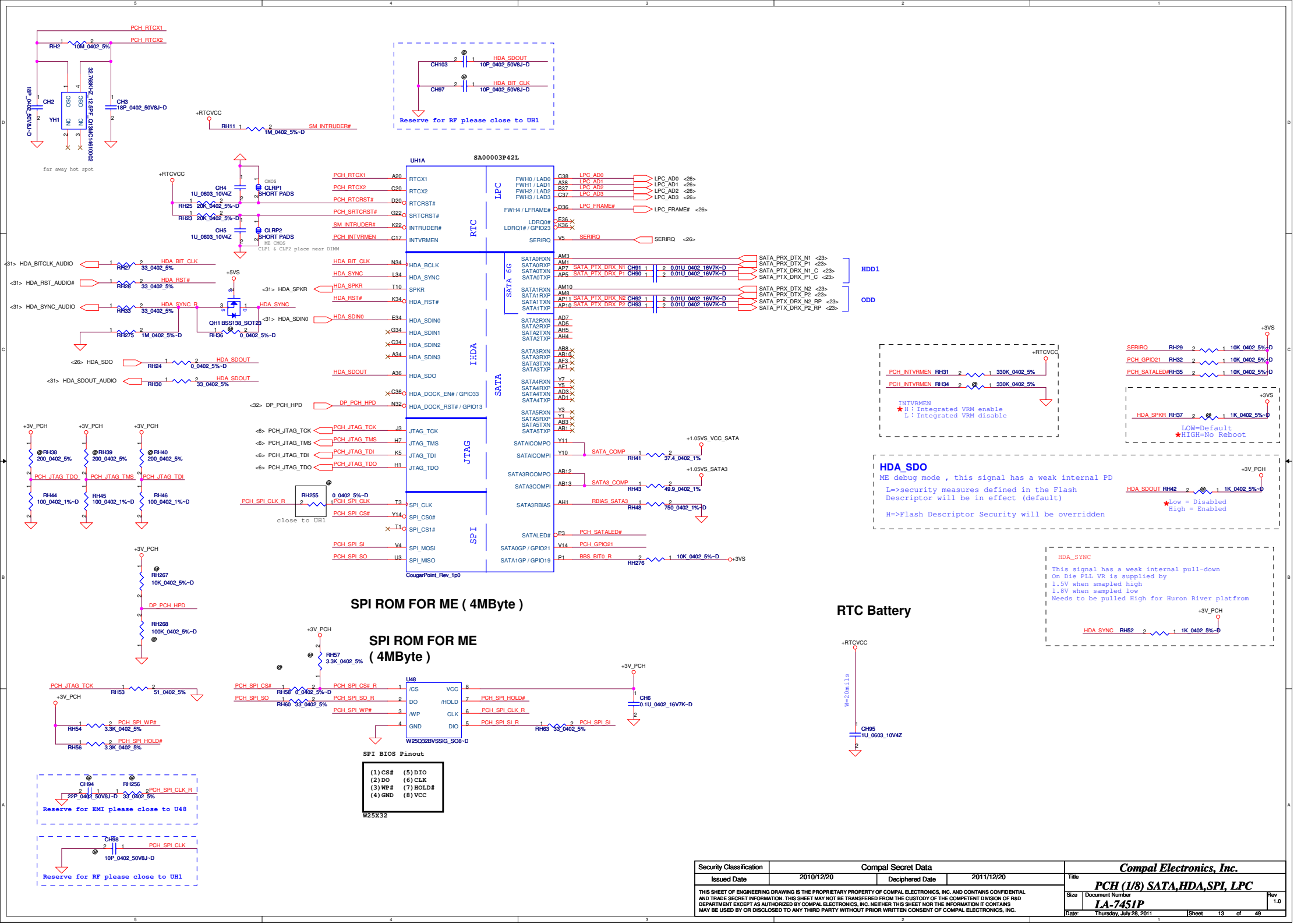
Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.

Title: **DDRIII DIMMB**

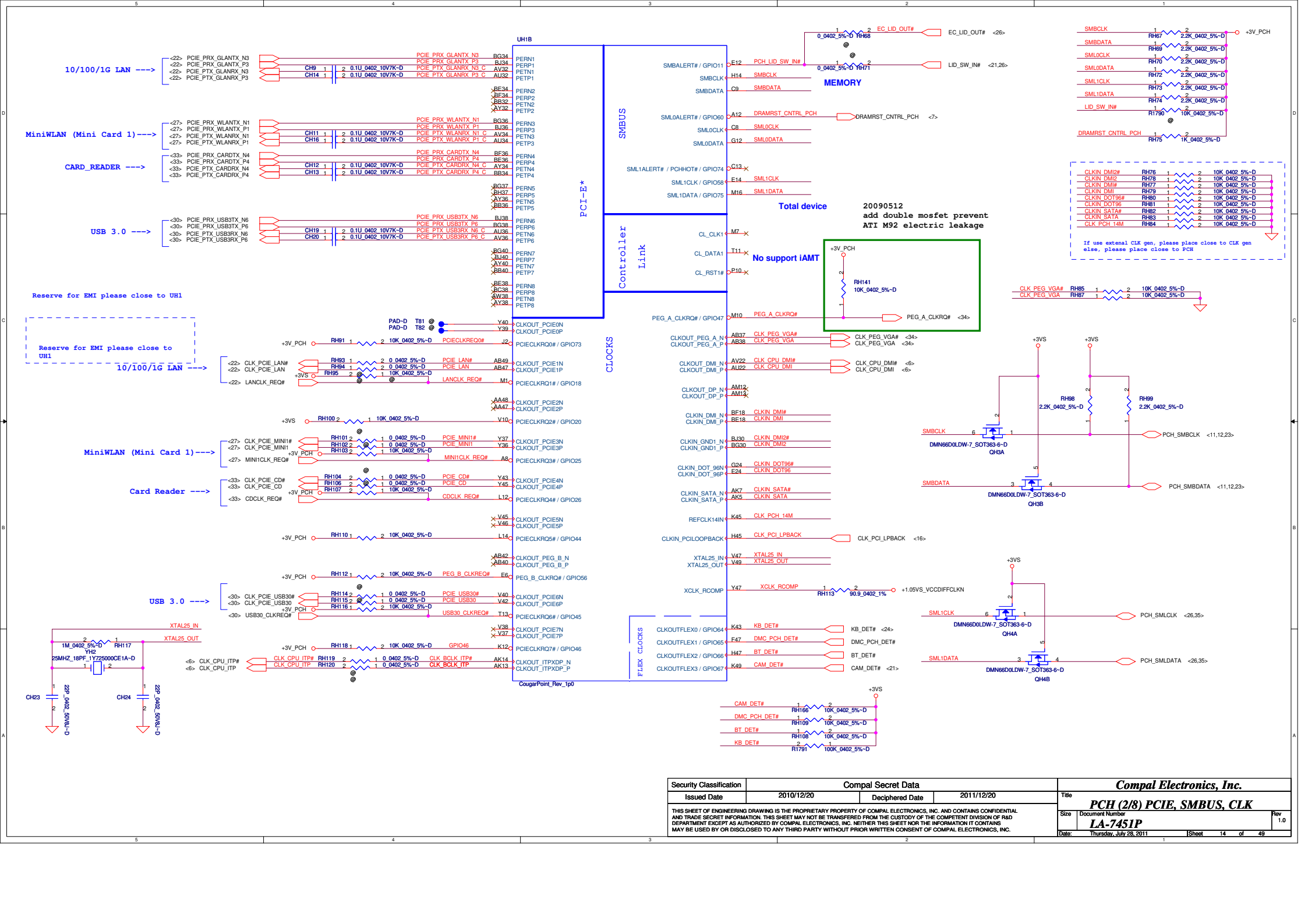
Size	Document Number	Rev
	LA-7451P	1.0

Date: Thursday, July 28, 2011 | Sheet 12 of 49



Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.	
Title	PCH (1/8) SATA,HDA,SPI, LPC
Size	Document Number: LA-7451P
Rev	1.0
Date: Thursday, July 28, 2011	Sheet 13 of 49



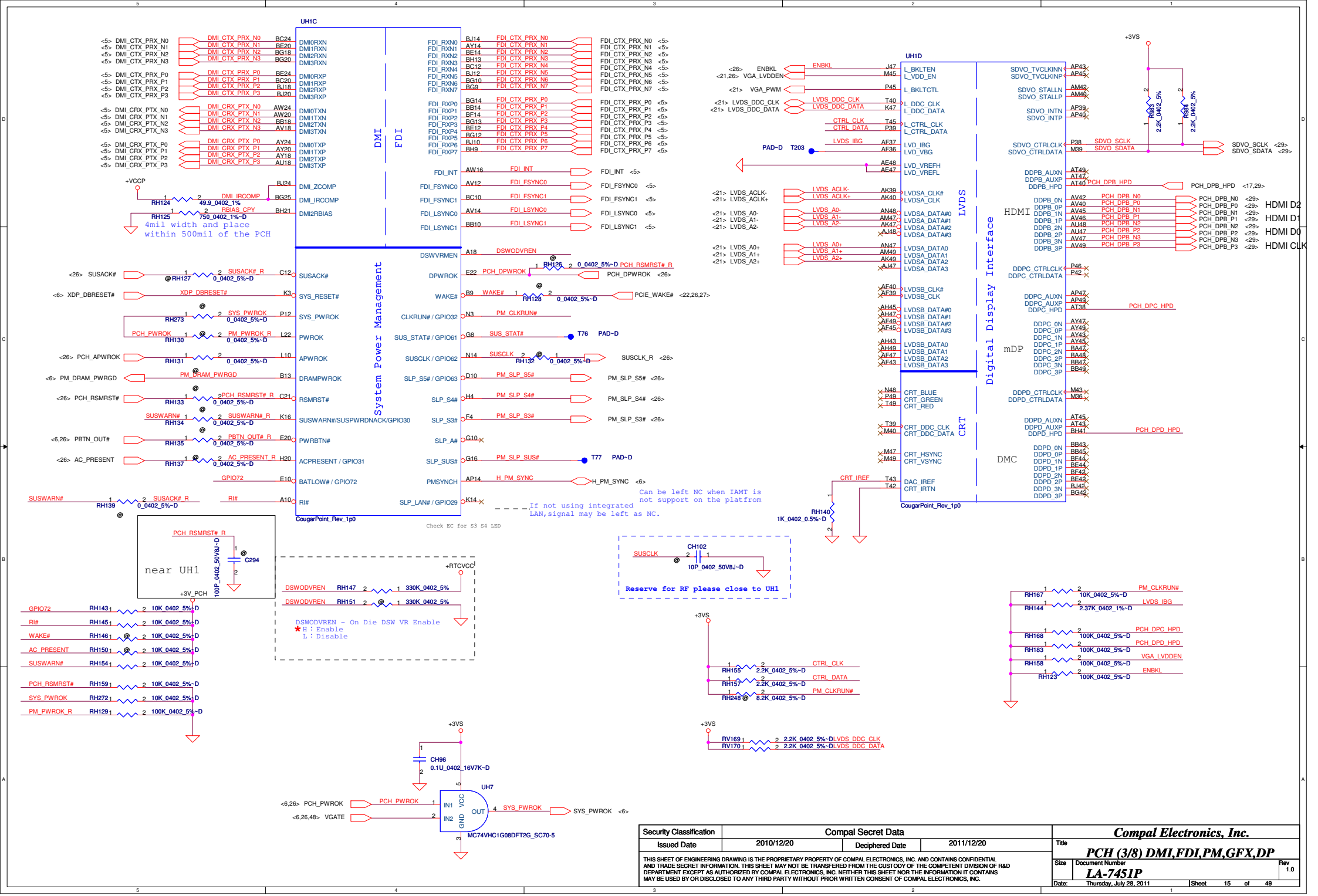
Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.

Title: **PCH (2/8) PCIE, SMBUS, CLK**

Size	Document Number	Rev
	LA-7451P	1.0

Date: Thursday, July 28, 2011 | Sheet 14 of 49



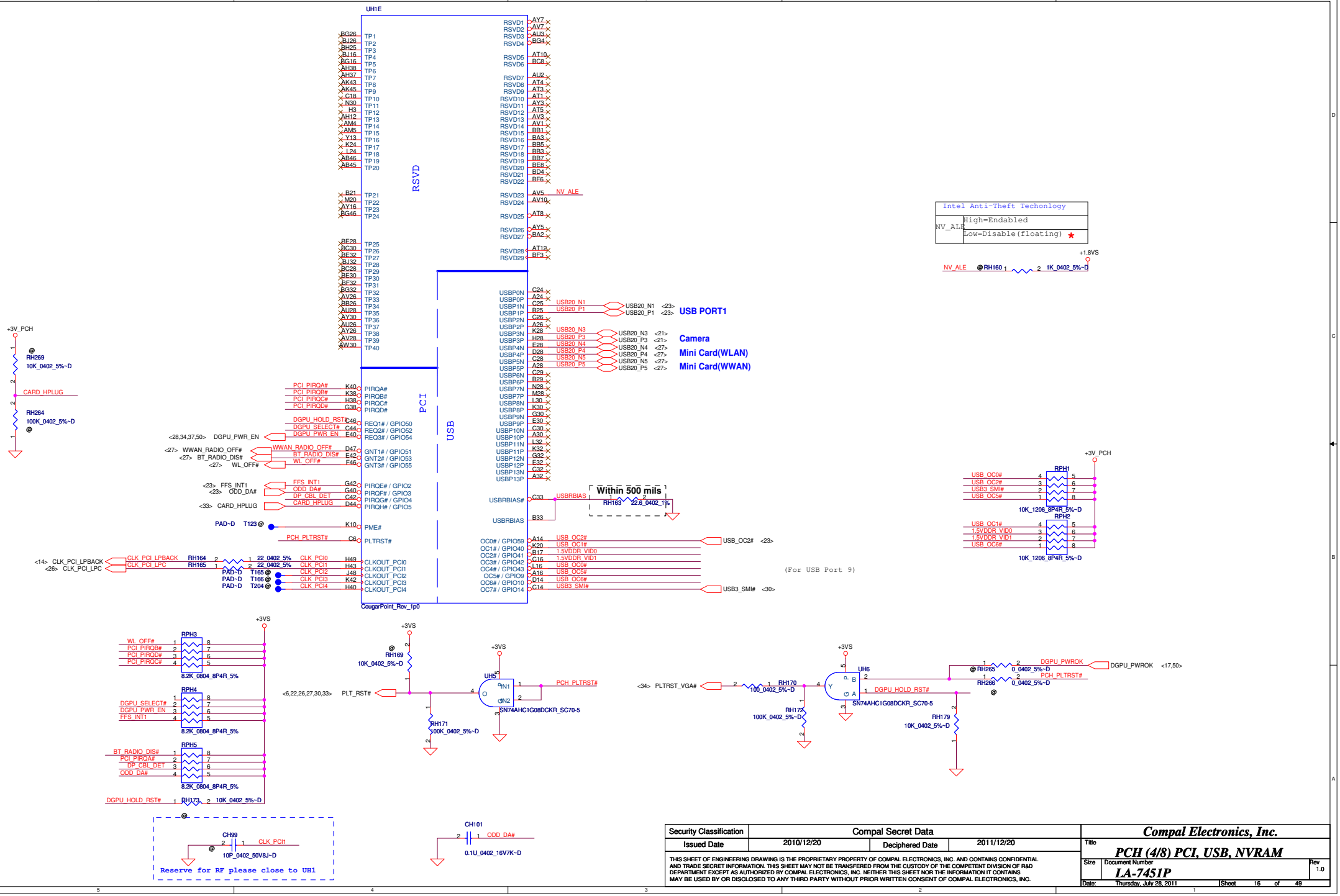
Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.

Title: **PCH (3/8) DMI,FDI,PM,GFX,DP**

Size	Document Number	Rev
	LA-7451P	1.0

Date: Thursday, July 28, 2011 | Sheet 15 of 49



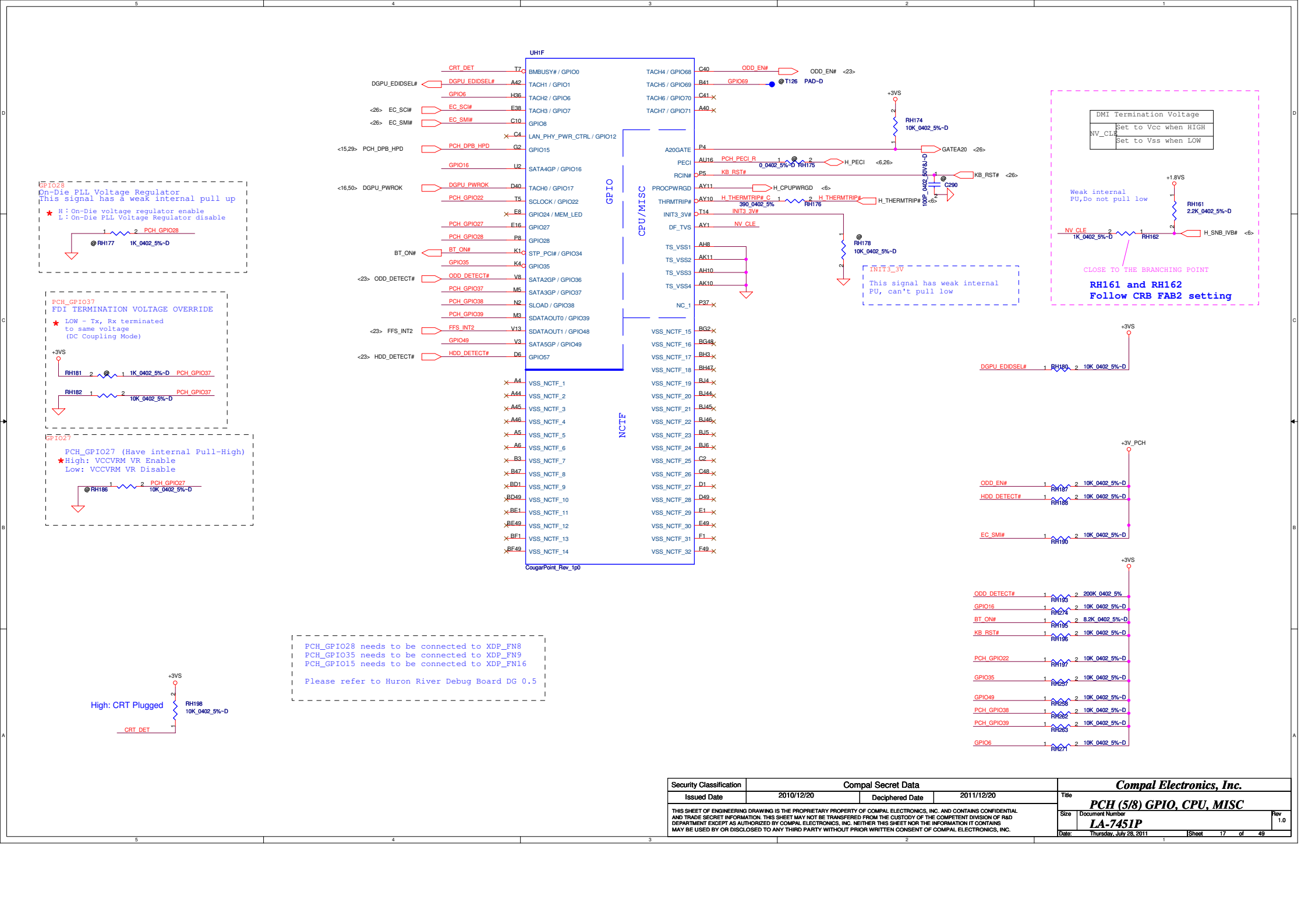
Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.

Title: **PCH (4/8) PCI, USB, NVRAM**

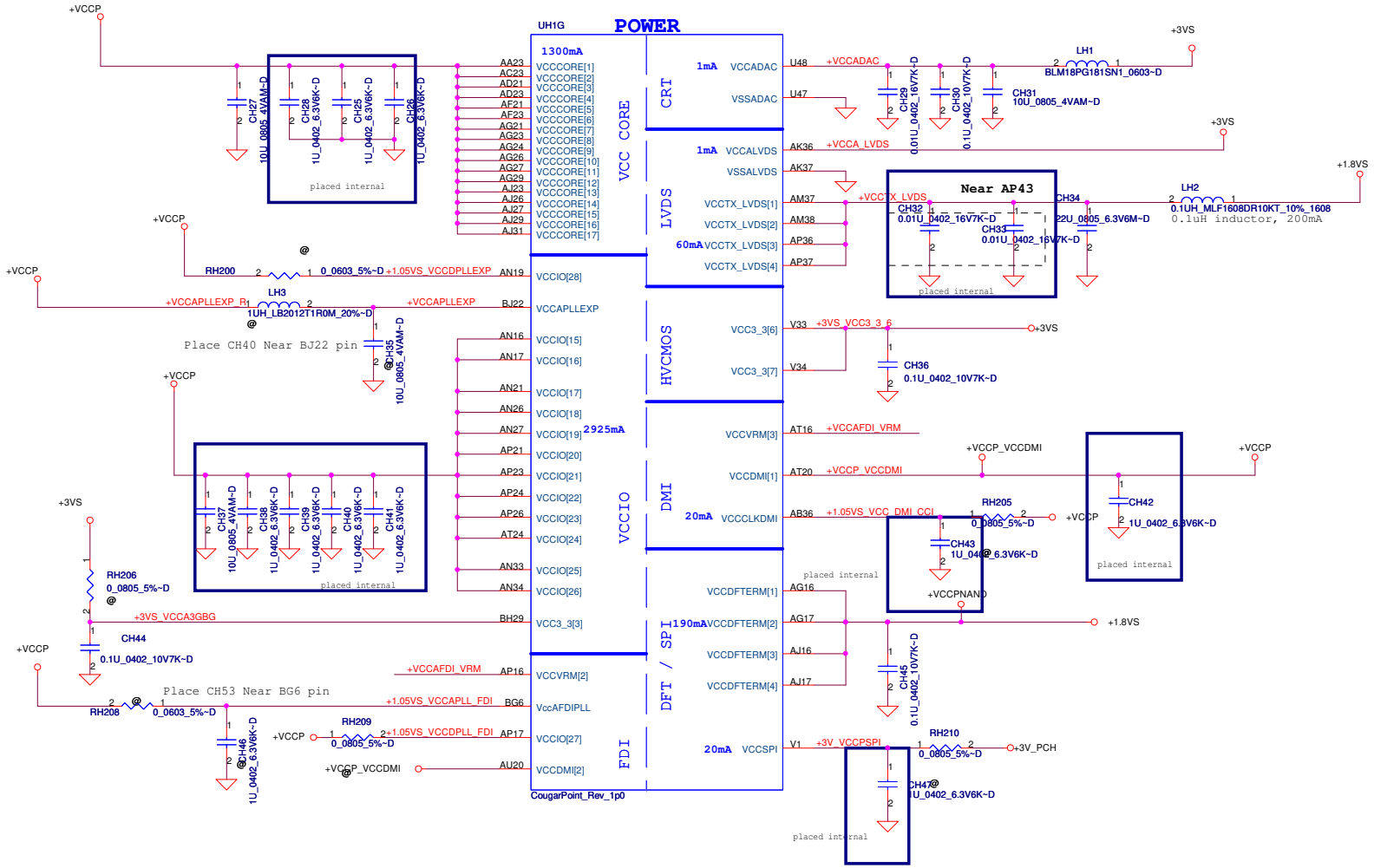
Size	Document Number	Rev
	LA-7451P	1.0

Date: Thursday, July 28, 2011 | Sheet 16 of 49



Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.			
Title	PCH (5/8) GPIO, CPU, MISC		
Size	Document Number		Rev
	LA-7451P		1.0
Date:	Thursday, July 28, 2011	Sheet	17 of 49



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

VCCVRM = 160mA detal waiting for newest spec

Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.

Title: PCH (6/8) PWR

Size: | Document Number: LA-7451P | Rev: 1.0

Date: Thursday, July 28, 2011 | Sheet 18 of 49

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

UH1J POWER

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | CPU | MISC | RTC | HDA

CougarPoint_Rev_1p0

<BOM Structure>

5/18 delete RH229

If it support 3.3V audio signals
POP:RH228
Depop RH233/RH234

If it support 1.5V audio signals
POP:RH233/RH234
Depop R228

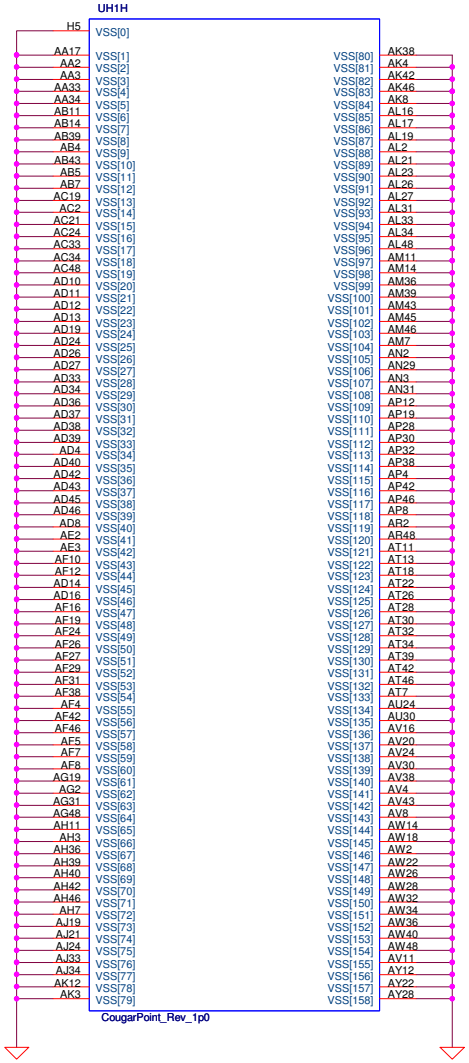
Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

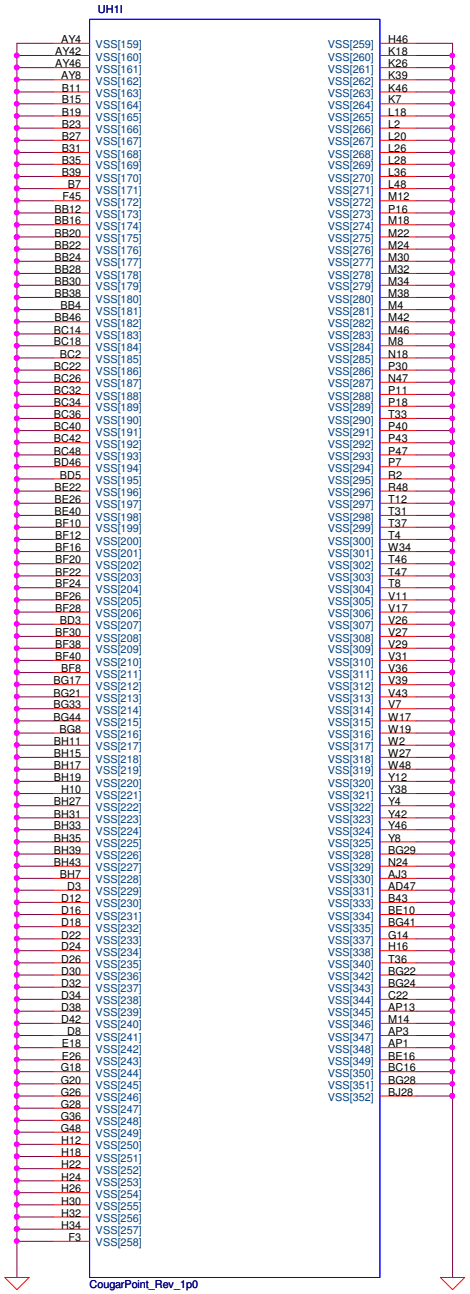
Compal Electronics, Inc.

Title: PCH (7/8) PWR

Size: | Document Number: LA-7451P | Rev: 1.0

Date: Thursday, July 28, 2011 | Sheet 19 of 49





Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

Size	Document Number	Rev
	LA-7451P	1.0

Date: Thursday, July 28, 2011 Sheet 20 of 49

LOGO Board CONN

PWR BTN Board CONN

Touchpad CONN

close to JTPMB 7/26

KB_LED control circuit

LVDS Conn.

EN_CAM# control circuit

close to JLVDS

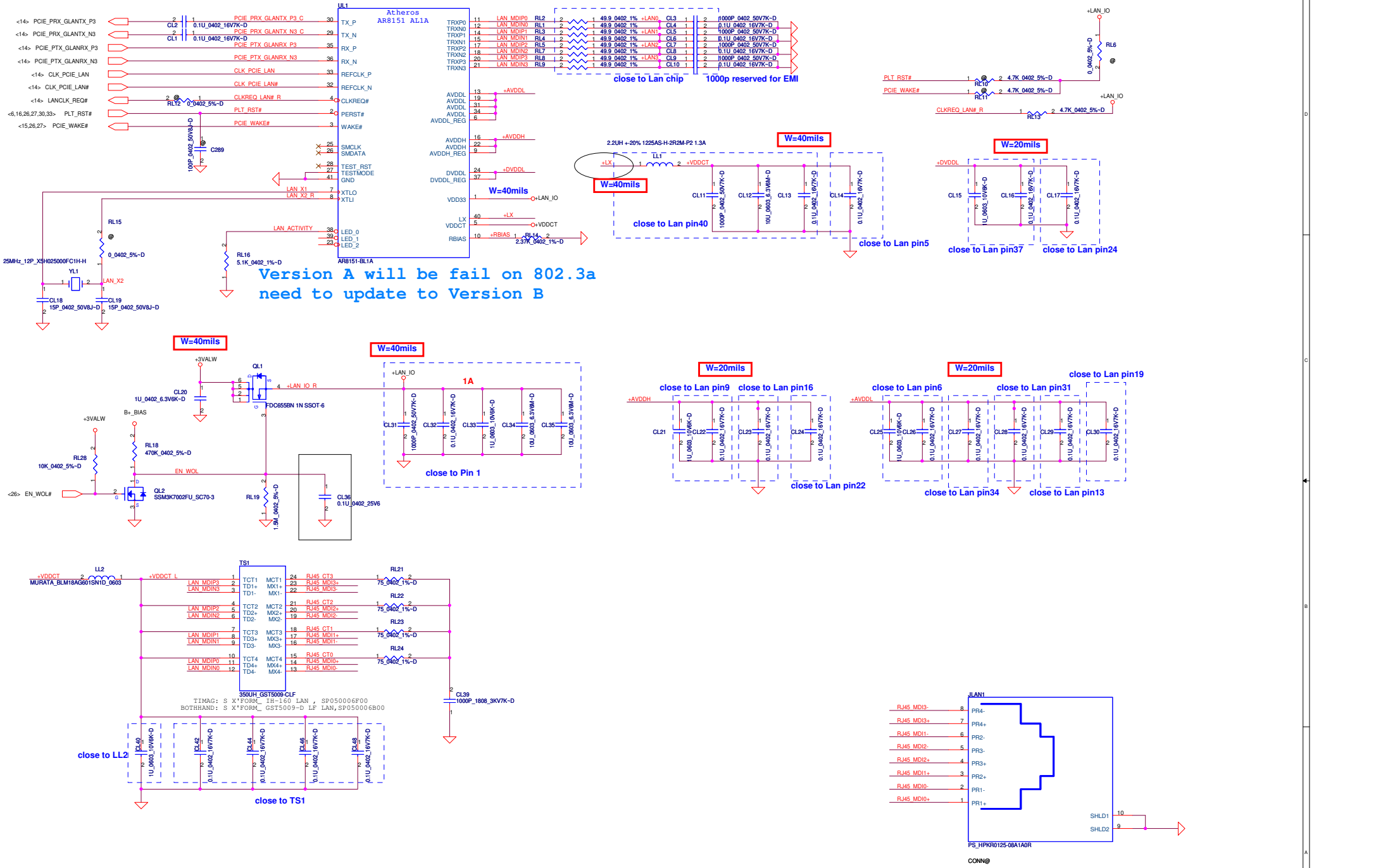
Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.

Title: VGA / LVDS /camera conn.

Size	Document Number	Rev
	LA-7451P	1.0

Date: Thursday, July 28, 2011 | Sheet 21 of 49



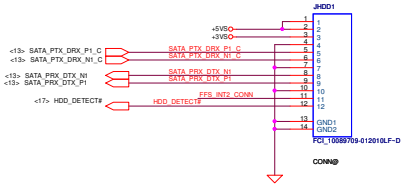
Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.

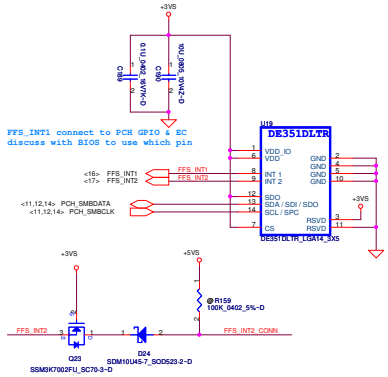
Title: **GLAN AR8151 AL1A/ RJ45**

Size	Document Number	Rev
	LA-7451P	1.0

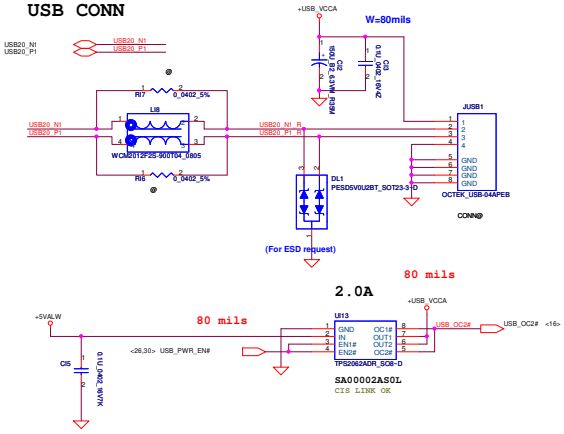
Date: Thursday, July 28, 2011 | Sheet 22 of 49

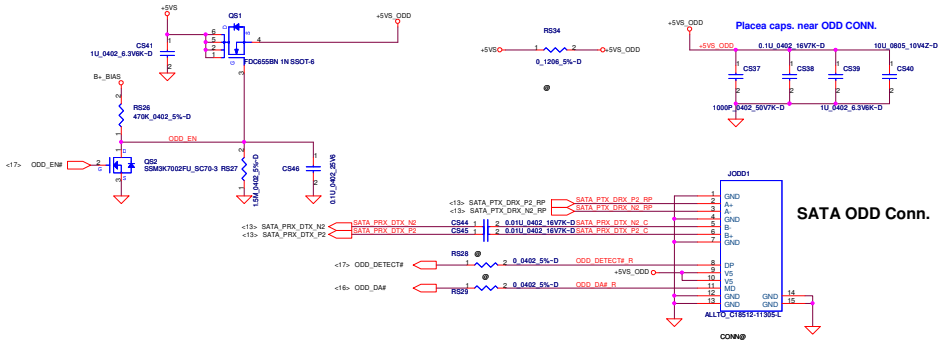


Free Fall Sensor



USB CONN





Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.

Title: FFS /HDD /ODD /USB Connector

Size: | Document Number: LA-7451P | Rev: 1.0

Date: Thursday, July 28, 2011 | Sheet 23 of 51

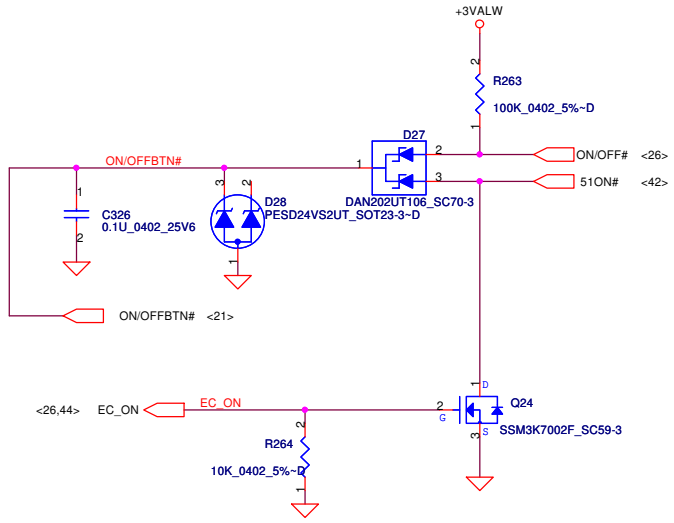
ON/OFF switch

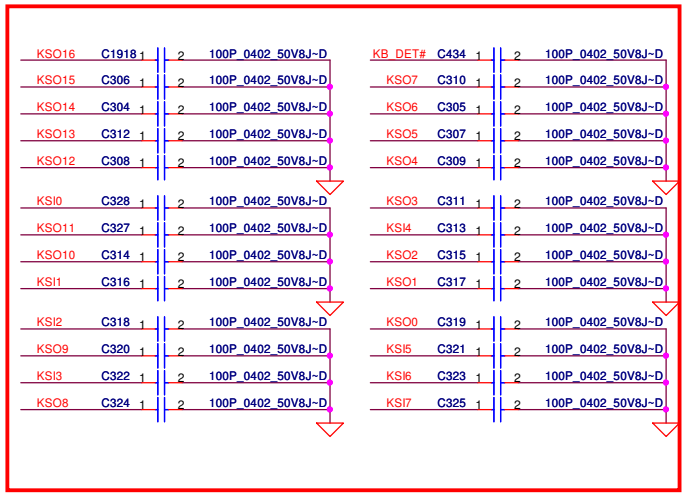
Power Button

TOP Side

Bottom Side

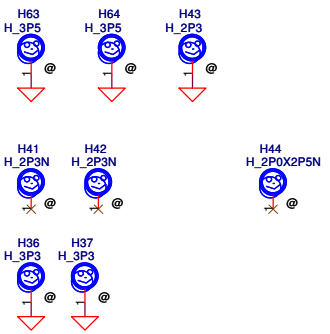
Test Only

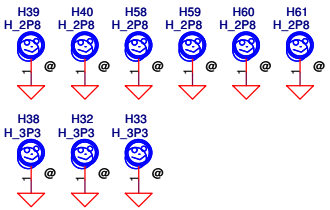


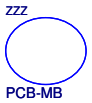


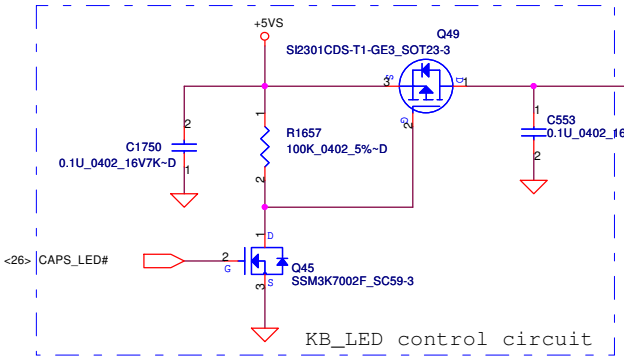
KSI[0..7] KSI[0..7] <26>
KSO[0..16] KSO[0..16] <26>

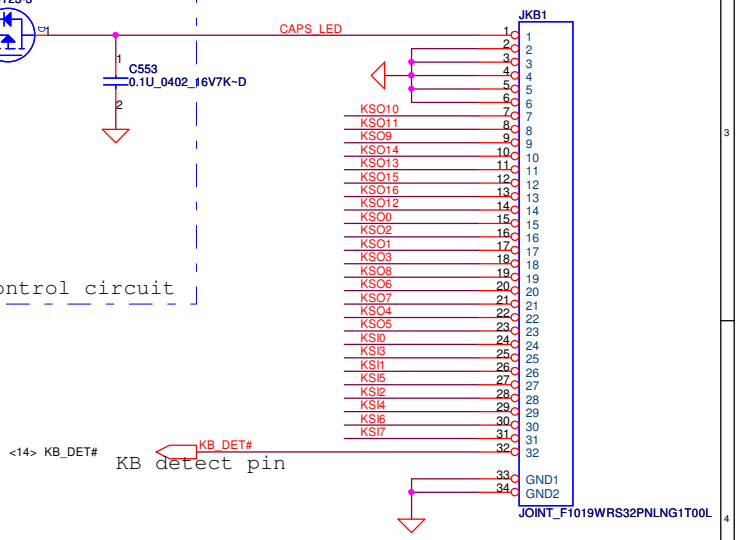
INT_KBD Conn.











Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

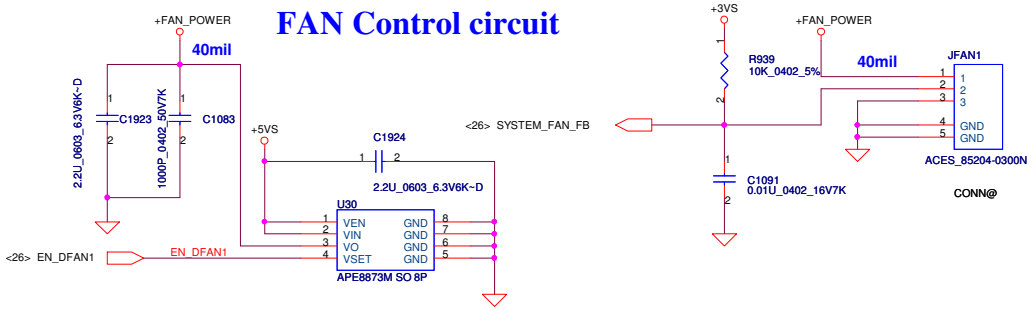
Compal Electronics, Inc.

Title: PWRBTN/SCREWH/KB

Size: | Document Number: LA-7451P | Rev: 1.0

Date: Thursday, July 28, 2011 | Sheet 24 of 51

FAN Control circuit



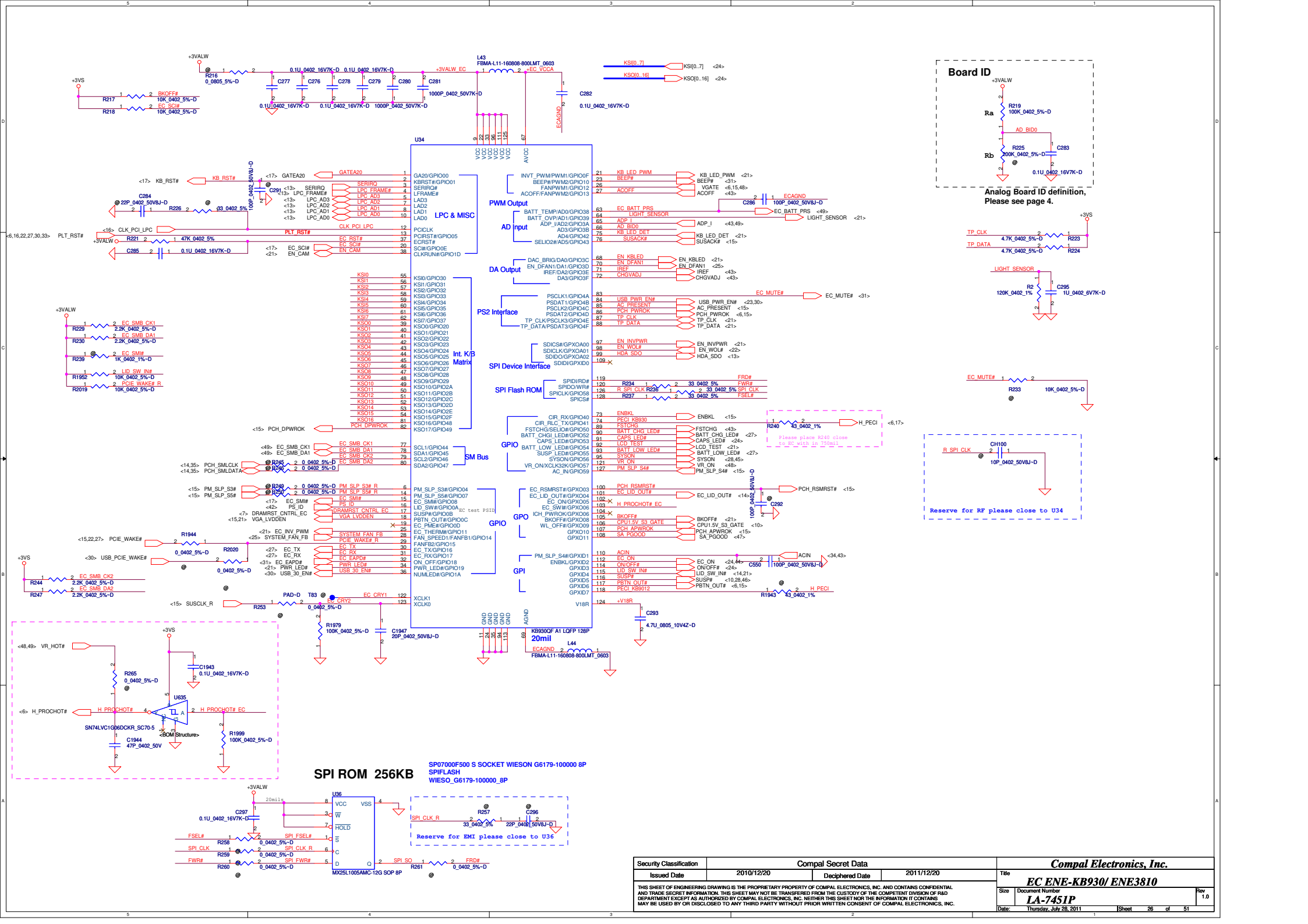
Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.

Title: **FAN Controller**

Size	Document Number	Rev
	LA-7451P	1.0

Date: Thursday, July 28, 2011 Sheet 25 of 51


U34
KB930QF A1 LQFP 128P
20mil
SPI ROM 256KB
SP07000F500 S SOCKET WIESON G6179-100000 8P
SPIFLASH
WIESO_G6179-100000_8P
MX25L1005AMC-12G SOP 8P
Board ID
Analog Board ID definition,
Please see page 4.
Reserve for RF please close to U34
Reserve for EMI please close to U36
Please place R240 close to EC with in 750mil
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
Int. K/B Matrix
SM Bus
GPIO
GPO
GPI
Security Classification
Compal Secret Data
Issued Date
2010/12/20
Deciphered Date
2011/12/20
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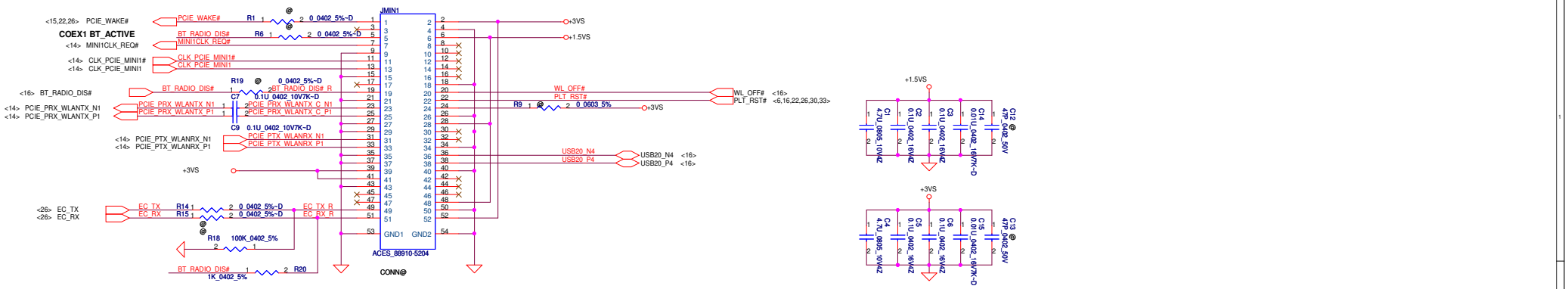
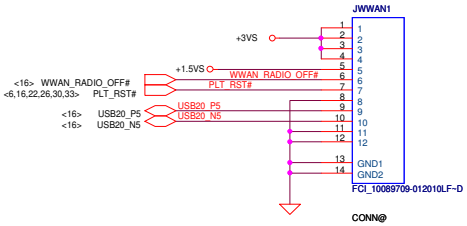
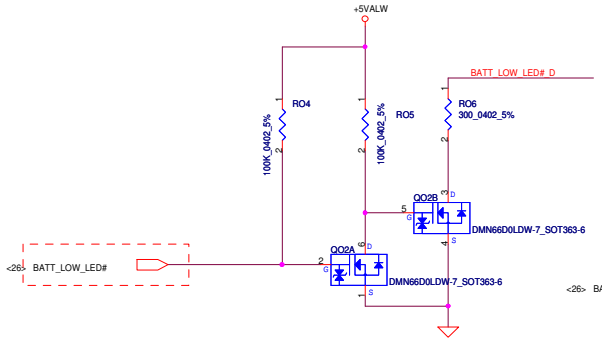
Compal Electronics, Inc.
Title
EC ENE-KB930/ ENE3810
Size
Document Number
LA-7451P
Rev
1.0
Date: Thursday, July 28, 2011
Sheet 26 of 51



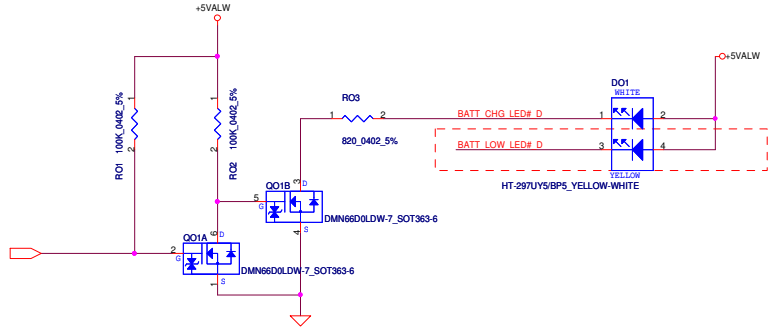
TO WWAN BOARD



BATT LOW



BATT CHARGE



Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

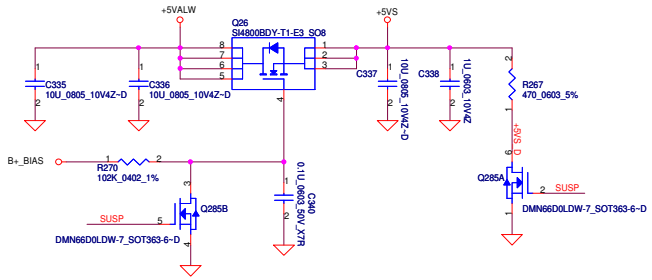
Compal Electronics, Inc.

Title: **LED/ WLAN / WWAN CONN**

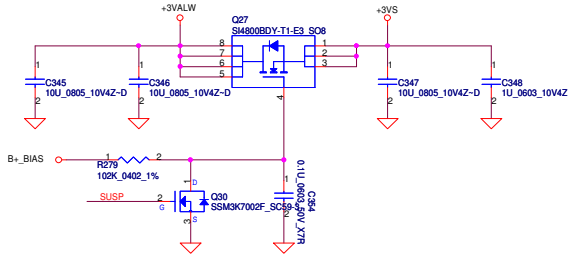
Size	Document Number	Rev
	LA-7451P	1.0

Date: Thursday, July 28, 2011 | Sheet 27 of 51

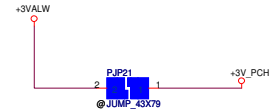
+5VALW to +5VS



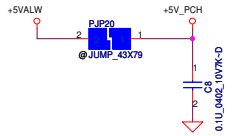
+3VALW to +3VS

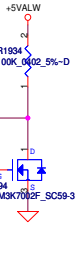


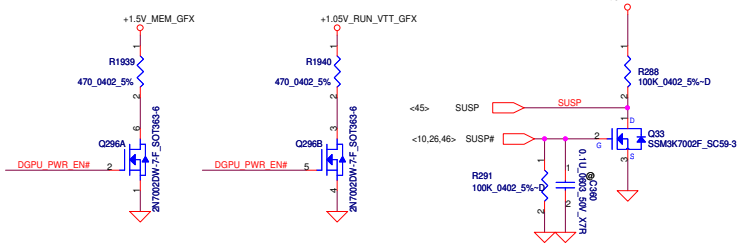
+3VALW to +3V_PCH



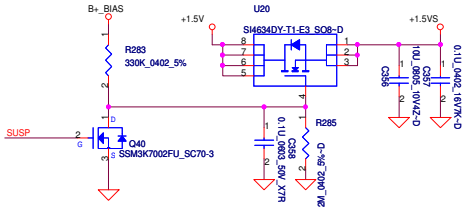
+5VALW to +5V_PCH

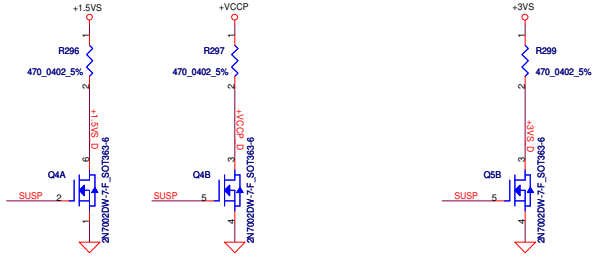


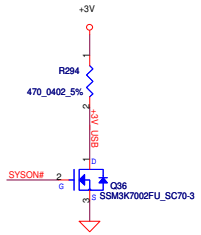


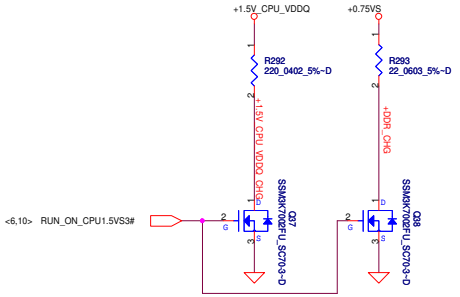


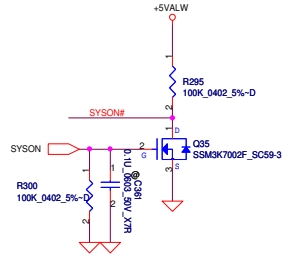
+1.5V To +1.5VS











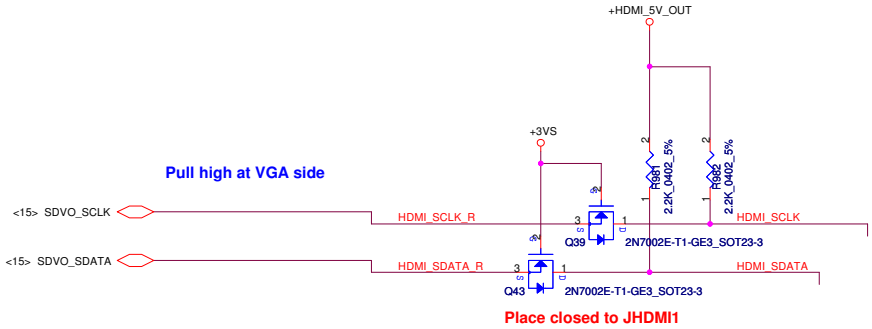
Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

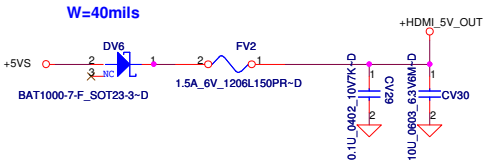
Compal Electronics, Inc.

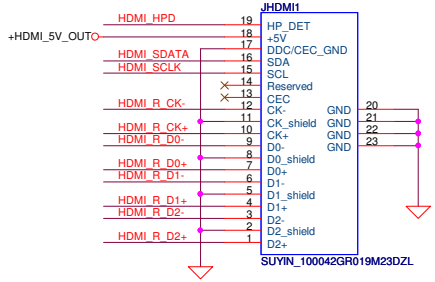
Title: **DC/DC Interface**

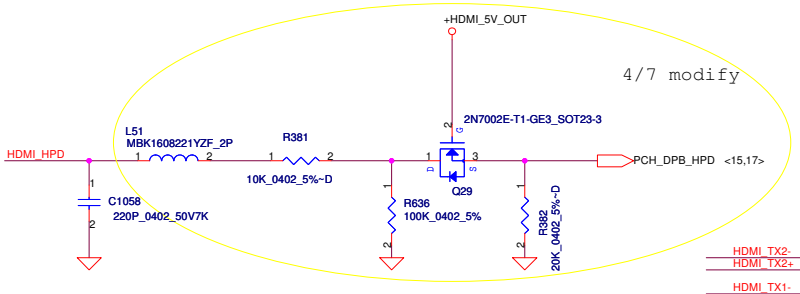
Size	Document Number	Rev
	LA-7451P	1.0

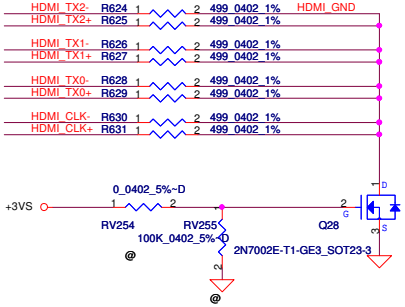
Date: Thursday, July 28, 2011 | Sheet 28 of 51

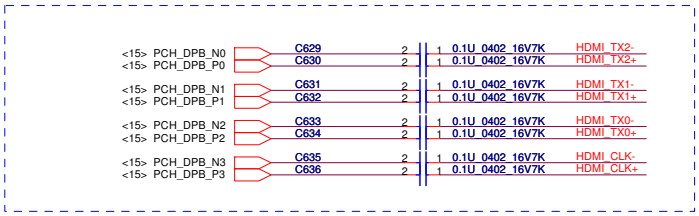




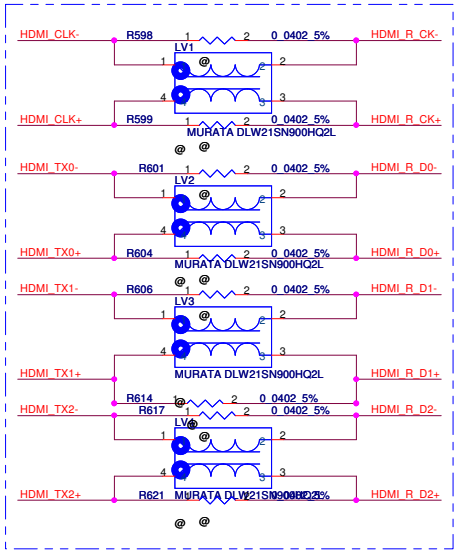








Place close JHDMI1



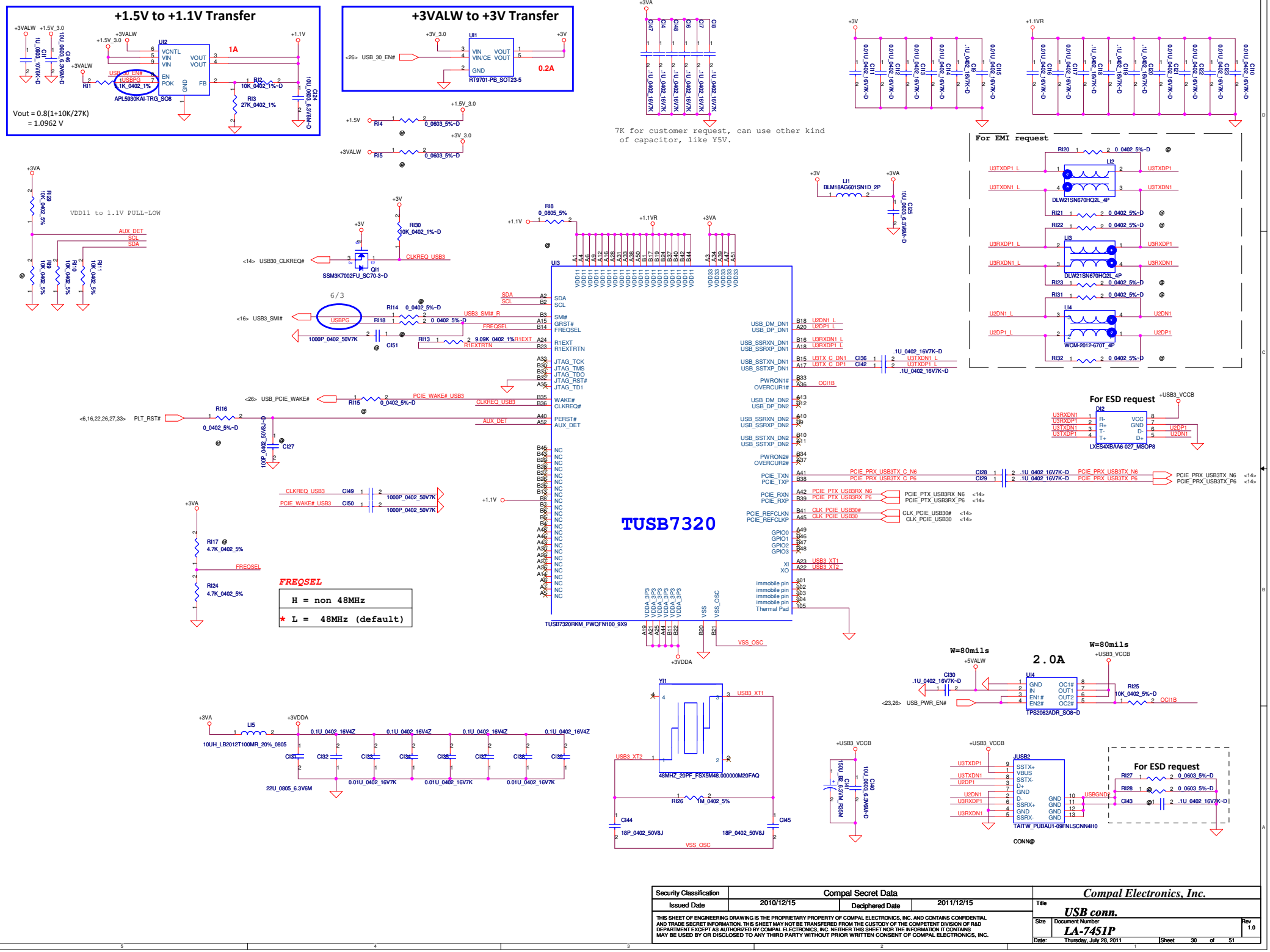
Security Classification	Compal Secret Data		
Issued Date	2010/12/20	Deciphered Date	2011/12/20

Compal Electronics, Inc.

Title: **HDMI**

Size	Document Number	Rev
Custom	LA-7451P	1.0

Date: Thursday, July 28, 2011 | Sheet 29 of 51


+1.5V to +1.1V Transfer
+3VALW to +3V Transfer
TUSB7320
TUSB7320RKM_PWQFN100_9X9
FREQSEL
H = non 48MHz
L = 48MHz (default)
For EMI request
For ESD request
W=80mils
2.0A
Vout = 0.8(1+10K/27K)
= 1.0962 V
7K for customer request, can use other kind of capacitor, like Y5V.
VDD11 to 1.1V PULL-LOW
APL5930KAI-TRG_SO8
RT9701-PB_SOT23-5
SSM3K7002FU_SC70-3-D
DLW21SN670HQ2L_4P
WCM-2012-670T_4P
LXES4XBAA6-027_MSOP8
TPS2062ADR_SO8-D
TAITW_PUBAU1-09FNLSCNN4H0
48MHZ_20PF_FSX5M48.000000M20FAQ
BLM18AG601SN1D_2P
Security Classification
Compal Secret Data
Issued Date
2010/12/15
Deciphered Date
2011/12/15
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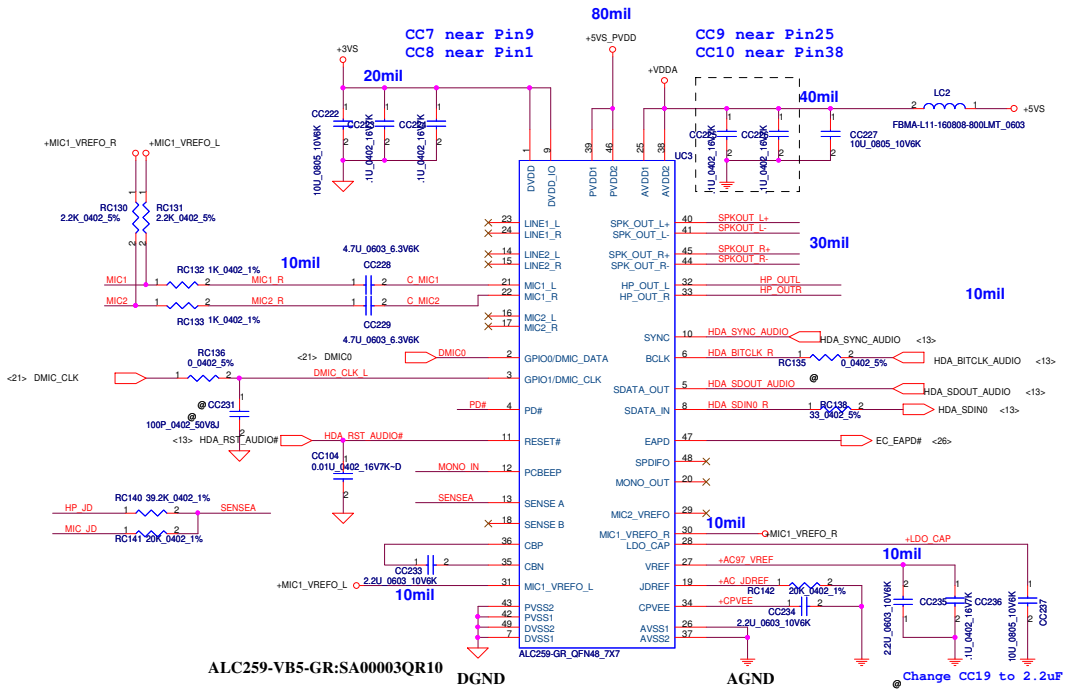
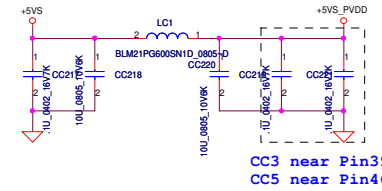
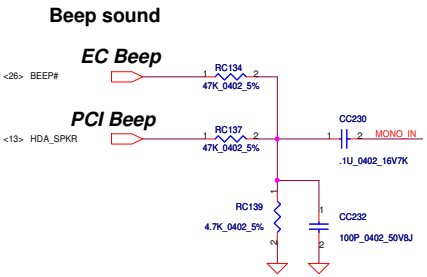
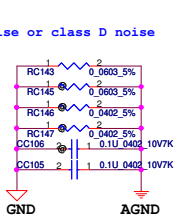
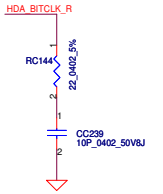
Compal Electronics, Inc.
Title
USB conn.
Size
Document Number
LA-7451P
Rev
1.0
Date: Thursday, July 28, 2011
Sheet 30 of 51





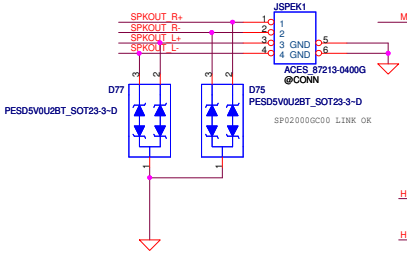




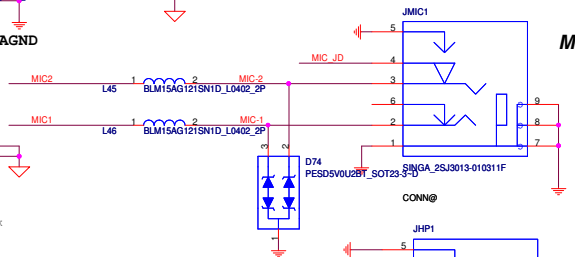


Change CC19 to 2.2uF for pop noise or class D noise

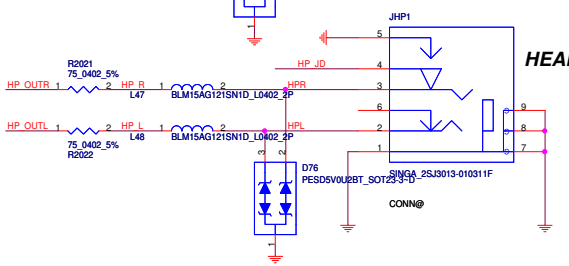
Speaker Connector



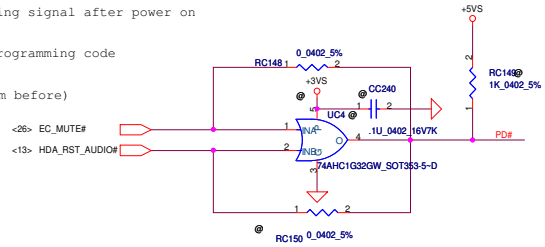
MICROPHONE IN JACK



HEADPHONE OUT JACK

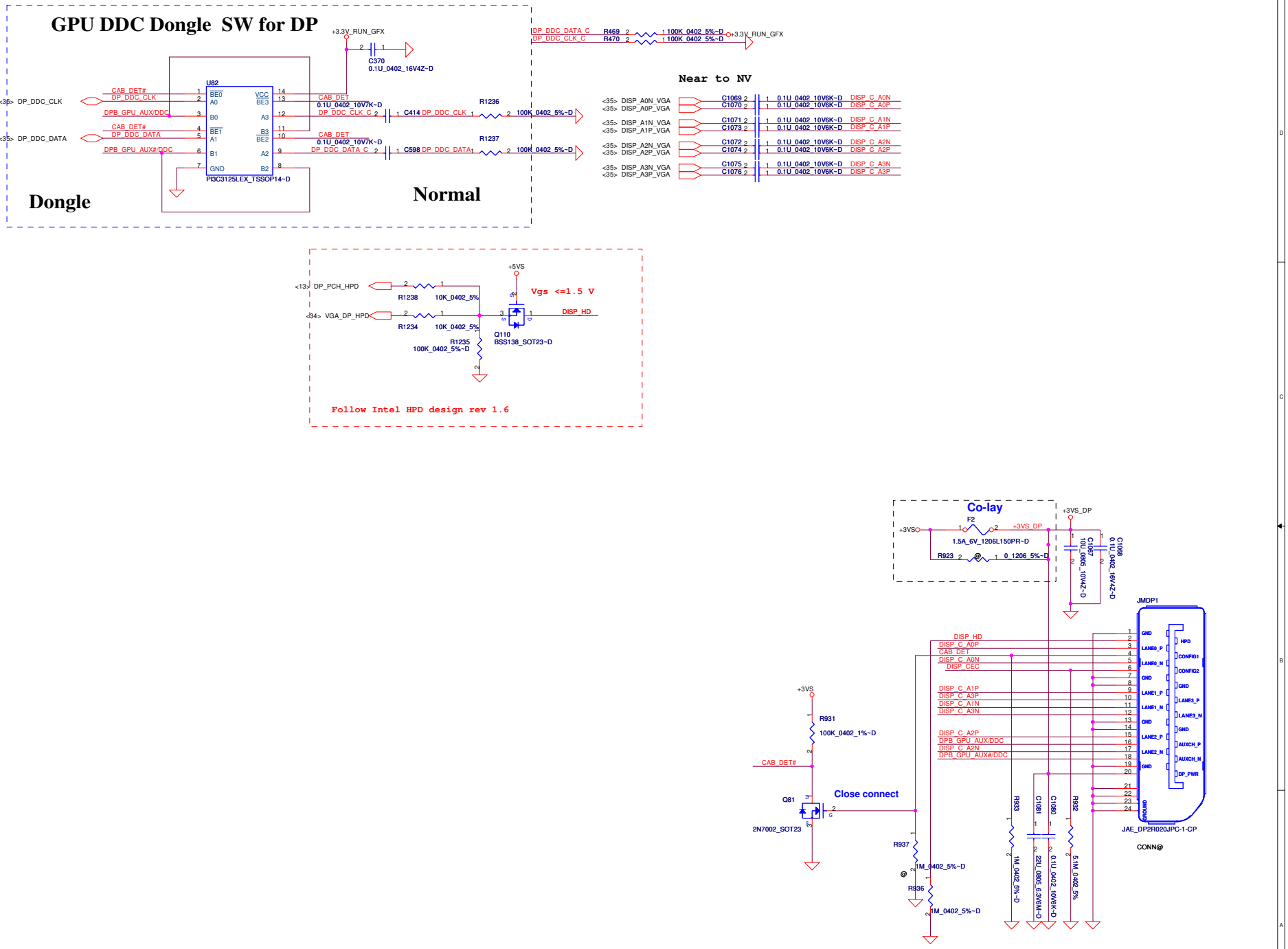


For Power on/off de-pop circuit and system booting warning signal:
Please system BIOS Engineer Note:
1.If you want the system make warning signal after power on
Please let EC_MUTE# high first
2.When you want to exit your BIOS programming code
Please let EC_MUTE# Low.
(The programming is difference from before)



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: Codec ALC259		
Size	Document Number: LA-7451P	Rev: 1.0
Date: Thursday, July 28, 2011	Sheet 31 of 51	



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Issued Date	2009/07/25	Deciphered Date 2011/07/06	Title: mini DP
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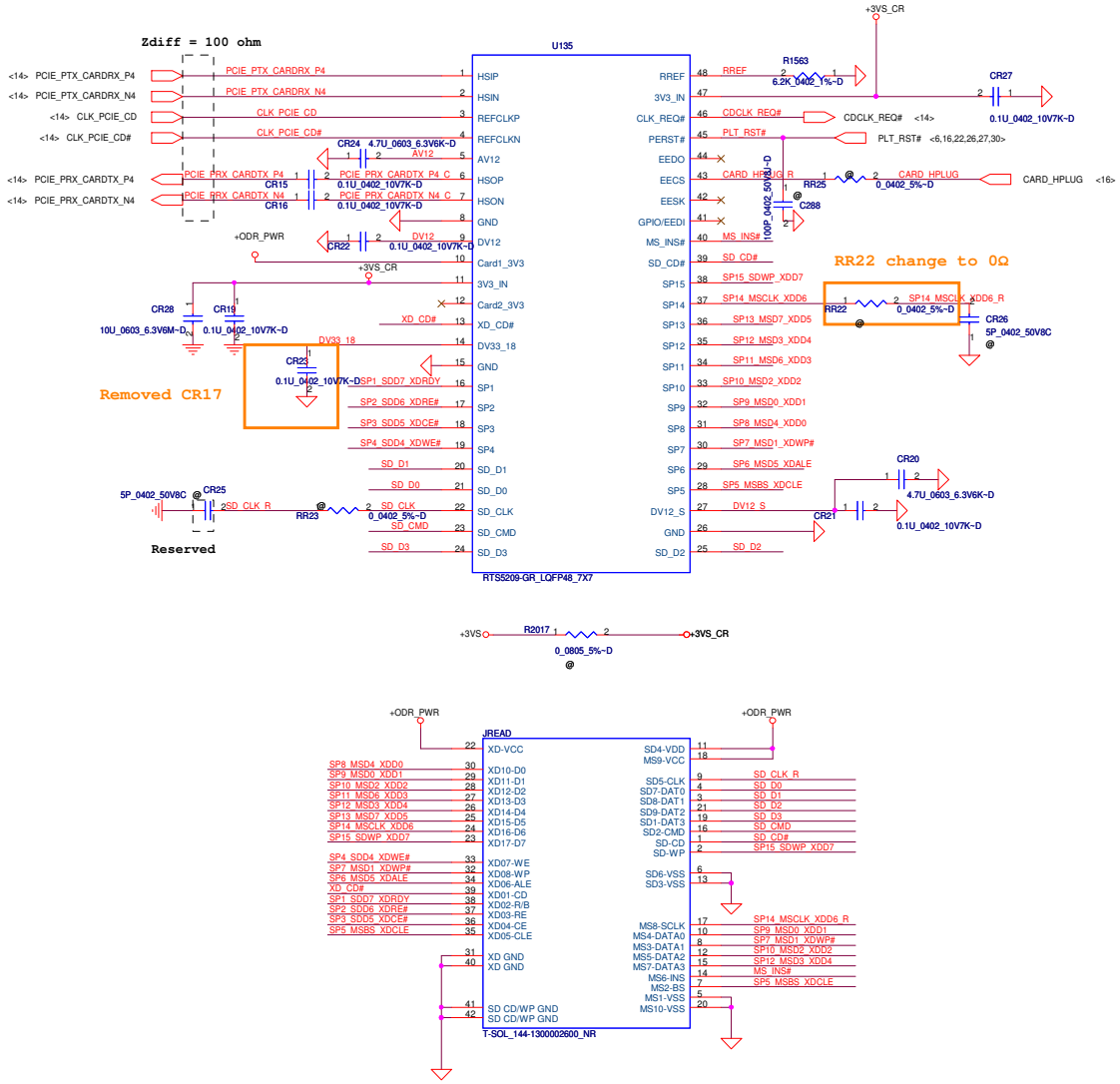
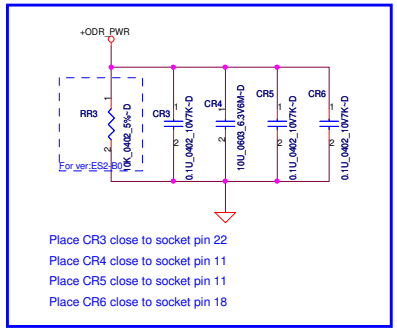
			Date: Thursday, July 28, 2011; Sheet 32 of 51





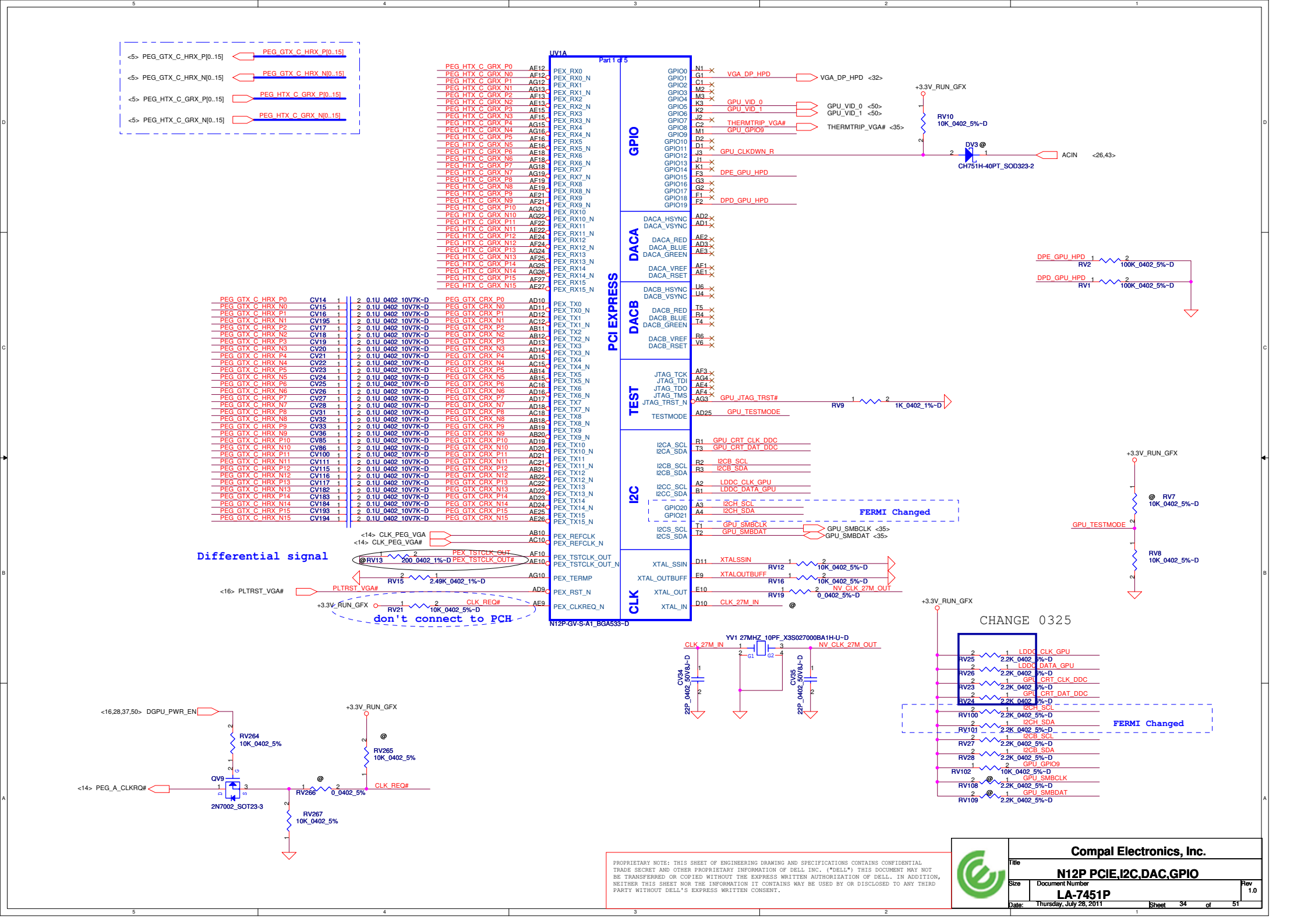
Security Classification	Compal Secret Data		
Issued Date	2010/12/15	Deciphered Date	2011/12/15

Compal Electronics, Inc.

Title: **Card Reader RTS5209**

Size	Document Number	Rev
	LA-7451P	1.0

Date: Thursday, July 28, 2011 | Sheet 33 of 51



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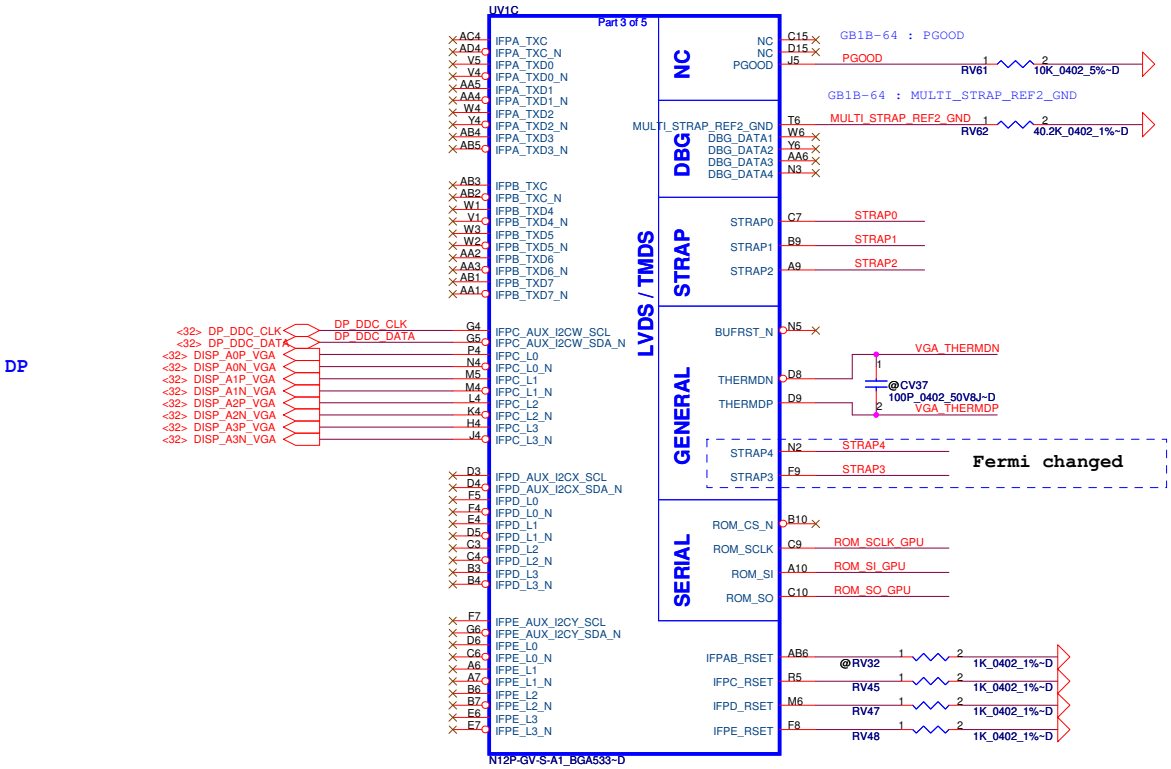
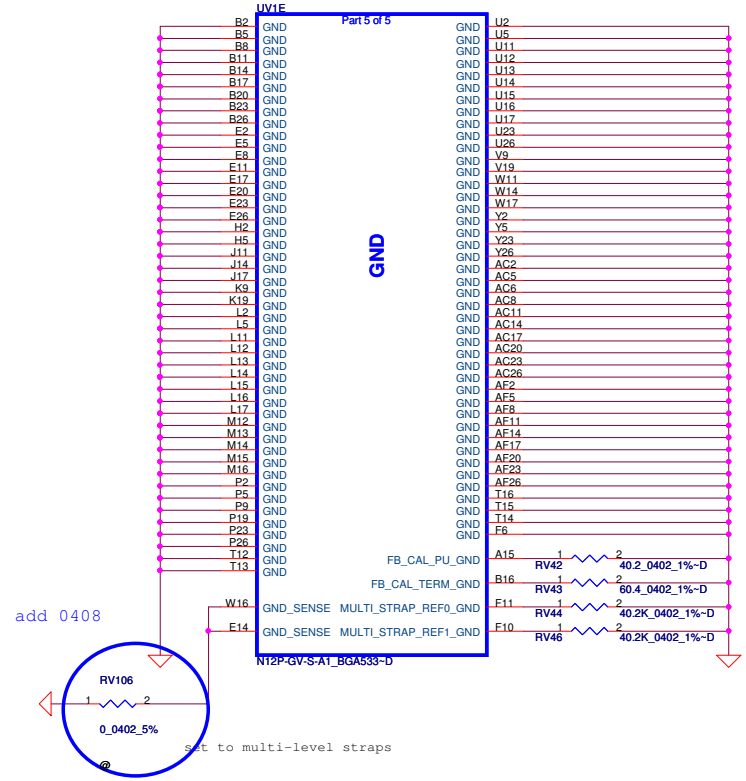
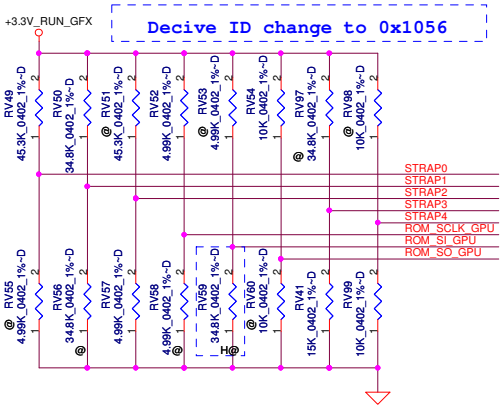
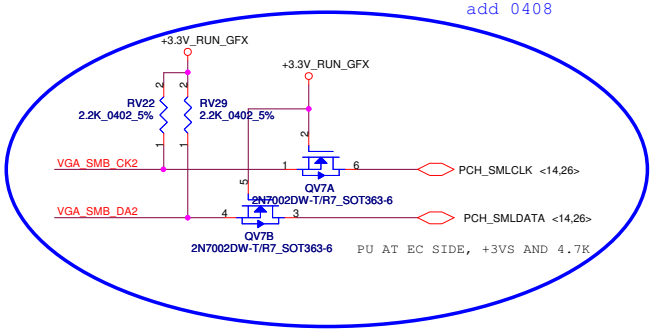
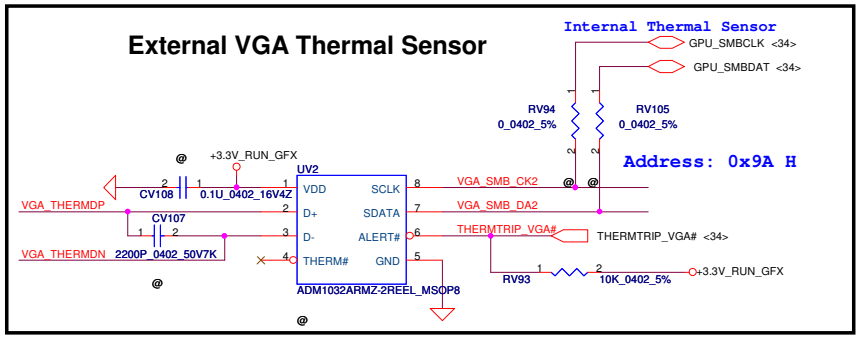










Resistor Values	Pull-up to +3V	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

ROM_SCLK	PCIDEVID_EXT, SUB_VENDOR, SLOT_CLK, PEX_PLL_EN
ROM_SI	RAM_CFG[3:0]
ROM_SO	XCLK_417, FB_0_BAR_SIZE, ALT_ADOOR, VGA_DEVICE

STRAP0	USER[3:0]
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]
STRAP2	PCI_DEVID[3:0]

** Hynix 64Mx16 DDR3 part stuff RV59=15K
Samsung 64Mx16 DDR3 part stuff RV59=20K

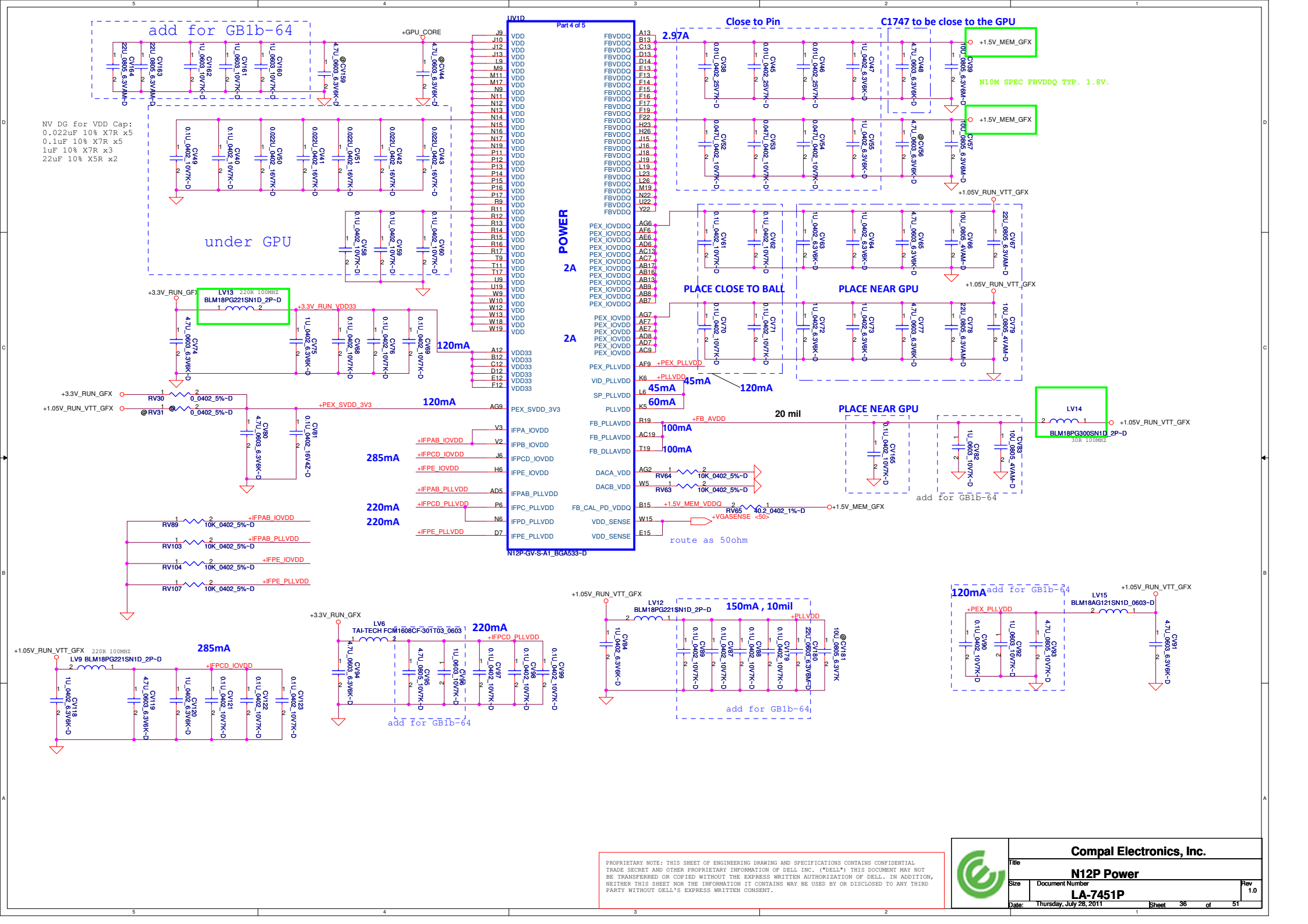
Hynix 128Mx16 DDR3 part stuff RV59=35K
Samsung 128Mx16 DDR3 part stuff RV59=45.3K

Compal Electronics, Inc.

Title: N12P DP, STRAP, GND

Size | Document Number: LA-7451P | Rev: 1.0

Date: Thursday, July 28, 2011 | Sheet 35 of 51



FBAD[0..63] FBAD[0..63] <38,39>
FBA_CMD[0..30] FBA_CMD[0..30] <38,39>
DQMA#[0..7] DQMA#[0..7] <38,39>
DQSA_RN[0..7] DQSA_RN[0..7] <38,39>
DQSA_WP[0..7] DQSA_WP[0..7] <38,39>

FBA_CMD3 RV66 10K_0402_5%~D CKE_1
FBA_CMD19 RV68 10K_0402_5%~D ODT_2
FBA_CMD0 RV71 10K_0402_5%~D ODT_1
FBA_CMD16 RV72 10K_0402_5%~D CKE_2
FBA_CMD20 RV75 10K_0402_5%~D RST

+1.5V_MEM_GFX
RV77 @ 1.1K_0402_1%~D
RV78 @ 1.1K_0402_1%~D
16mil
+FB_VREF
CV128 @ 0.01U_0402_25V7K~D

UV1B
Part 2 of 5
MEMORY INTERFACE
N12P-GV-S-A1_BGA533~D

FBAD		FBA_D		FBA_CMD		FBA_CMD
FBAD0	D22	FBA_D0	FBA_CMD0	G24	FBA_CMD0	
FBAD1	E24	FBA_D1	FBA_CMD1	F27	FBA_CMD1	PAD~D TV6@
FBAD2	E22	FBA_D2	FBA_CMD2	F25	FBA_CMD2	
FBAD3	D24	FBA_D3	FBA_CMD3	F26	FBA_CMD3	
FBAD4	D26	FBA_D4	FBA_CMD4	G26	FBA_CMD4	
FBAD5	D27	FBA_D5	FBA_CMD5	G27	FBA_CMD5	
FBAD6	C27	FBA_D6	FBA_CMD6	G25	FBA_CMD6	
FBAD7	B27	FBA_D7	FBA_CMD7	J25	FBA_CMD7	
FBAD8	A21	FBA_D8	FBA_CMD8	J24	FBA_CMD8	
FBAD9	B21	FBA_D9	FBA_CMD9	H24	FBA_CMD9	
FBAD10	C21	FBA_D10	FBA_CMD10	H22	FBA_CMD10	
FBAD11	C19	FBA_D11	FBA_CMD11	J26	FBA_CMD11	
FBAD12	C18	FBA_D12	FBA_CMD12	G22	FBA_CMD12	
FBAD13	D18	FBA_D13	FBA_CMD13	G23	FBA_CMD13	
FBAD14	B18	FBA_D14	FBA_CMD14	J22	FBA_CMD14	
FBAD15	C16	FBA_D15	FBA_CMD15	J27	FBA_CMD15	
FBAD16	E21	FBA_D16	FBA_CMD16	M24	FBA_CMD16	
FBAD17	F21	FBA_D17	FBA_CMD17	L24	FBA_CMD17	PAD~D TV5@
FBAD18	D20	FBA_D18	FBA_CMD18	J23	FBA_CMD18	
FBAD19	F20	FBA_D19	FBA_CMD19	K23	FBA_CMD19	
FBAD20	D17	FBA_D20	FBA_CMD20	K22	FBA_CMD20	
FBAD21	F18	FBA_D21	FBA_CMD21	M23	FBA_CMD21	
FBAD22	D16	FBA_D22	FBA_CMD22	K24	FBA_CMD22	
FBAD23	E16	FBA_D23	FBA_CMD23	M27	FBA_CMD23	
FBAD24	A22	FBA_D24	FBA_CMD24	N27	FBA_CMD24	
FBAD25	C24	FBA_D25	FBA_CMD25	M26	FBA_CMD25	
FBAD26	D21	FBA_D26	FBA_CMD26	K26	FBA_CMD26	
FBAD27	B22	FBA_D27	FBA_CMD27	K27	FBA_CMD27	
FBAD28	C22	FBA_D28	FBA_CMD28	K25	FBA_CMD28	
FBAD29	A25	FBA_D29	FBA_CMD29	M25	FBA_CMD29	
FBAD30	B25	FBA_D30	FBA_CMD30	L22	FBA_CMD30	
FBAD31	A26	FBA_D31				
FBAD32	U24	FBA_D32	FBA_DQM0	C26	DQMA#0	
FBAD33	V24	FBA_D33	FBA_DQM1	B19	DQMA#1	
FBAD34	V23	FBA_D34	FBA_DQM2	D19	DQMA#2	
FBAD35	R24	FBA_D35	FBA_DQM3	D23	DQMA#3	
FBAD36	T23	FBA_D36	FBA_DQM4	T24	DQMA#4	
FBAD37	R23	FBA_D37	FBA_DQM5	AA23	DQMA#5	
FBAD38	P24	FBA_D38	FBA_DQM6	AB27	DQMA#6	
FBAD39	P22	FBA_D39	FBA_DQM7	T26	DQMA#7	
FBAD40	AC24	FBA_D40				
FBAD41	AB23	FBA_D41	FBA_DQS_RN0	D25	DQSA_RN0	
FBAD42	AB24	FBA_D42	FBA_DQS_RN1	A18	DQSA_RN1	
FBAD43	W24	FBA_D43	FBA_DQS_RN2	E18	DQSA_RN2	
FBAD44	AA22	FBA_D44	FBA_DQS_RN3	B24	DQSA_RN3	
FBAD45	W23	FBA_D45	FBA_DQS_RN4	R22	DQSA_RN4	
FBAD46	W22	FBA_D46	FBA_DQS_RN5	Y24	DQSA_RN5	
FBAD47	V22	FBA_D47	FBA_DQS_RN6	AA27	DQSA_RN6	
FBAD48	AA25	FBA_D48	FBA_DQS_RN7	R27	DQSA_RN7	
FBAD49	W27	FBA_D49				
FBAD50	W26	FBA_D50	FBA_DQS_WP0	C25	DQSA_WP0	
FBAD51	W25	FBA_D51	FBA_DQS_WP1	A19	DQSA_WP1	
FBAD52	AB25	FBA_D52	FBA_DQS_WP2	E19	DQSA_WP2	
FBAD53	AB26	FBA_D53	FBA_DQS_WP3	A24	DQSA_WP3	
FBAD54	AD26	FBA_D54	FBA_DQS_WP4	T22	DQSA_WP4	
FBAD55	AD27	FBA_D55	FBA_DQS_WP5	AA24	DQSA_WP5	
FBAD56	V25	FBA_D56	FBA_DQS_WP6	AA26	DQSA_WP6	
FBAD57	R25	FBA_D57	FBA_DQS_WP7	T27	DQSA_WP7	
FBAD58	V26	FBA_D58				
FBAD59	V27	FBA_D59	FB_VREF	A16	+FB_VREF	
FBAD60	R26	FBA_D60				
FBAD61	T25	FBA_D61	FBA_CLK0	F24	CLKA0 <38>	
FBAD62	N25	FBA_D62	FBA_CLK0_N	F23	CLKA0# <38>	
FBAD63	N26	FBA_D63				
			FBA_CLK1	N24	CLKA1 <39>	
			FBA_CLK1_N	N23	CLKA1# <39>	
			FBA_DEBUG	M22	RV76 10K_0402_5%~D +1.5V_MEM_GFX	

Mode E – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

+3.3V_RUN_GFX Source

<16,28,34,50> DGPU_PWR_EN
RV257 10K_0402_5%
QV6 SSM3K7002FU_SC70-3
CV370 0.1U_0402_16V4Z~D
CV186 0.1U_0402_16V4Z~D
+3VALW
RV92 100K_0402_5%
RV256 1K_0402_5%
+3VS
3VS_Dgate
QV5 SI7121DN-T1-GE3_POWERPAK8-5 60mil(1.4A)
RV90 470_0603_5%
QV8 SSM3K7002FU_SC70-3
+3.3V_RUN_GFX

+1.5V_MEM_GFX Source

<28> DGPU_PWR_EN#
RV259 0_0402_5%
QV2 PMF3800SN_SC70-3
CV371 0.1U_0603_25V7K @
RV67 330K_0402_5%
RV258 470_0402_5%
RV260 2M_0402_5%~D
CV125 0.1U_0603_25V7K
QV1 SI4634DY-T1-E3_SO8~D
CV372 0.1U_0402_16V4Z~D
CV124 10U_0805_6.3V6M~D
CV373 10U_0805_10V4Z~D
+1.5VS
+1.5V_MEM_GFX
B+

+1.05V_RUN_VTT_GFX Source

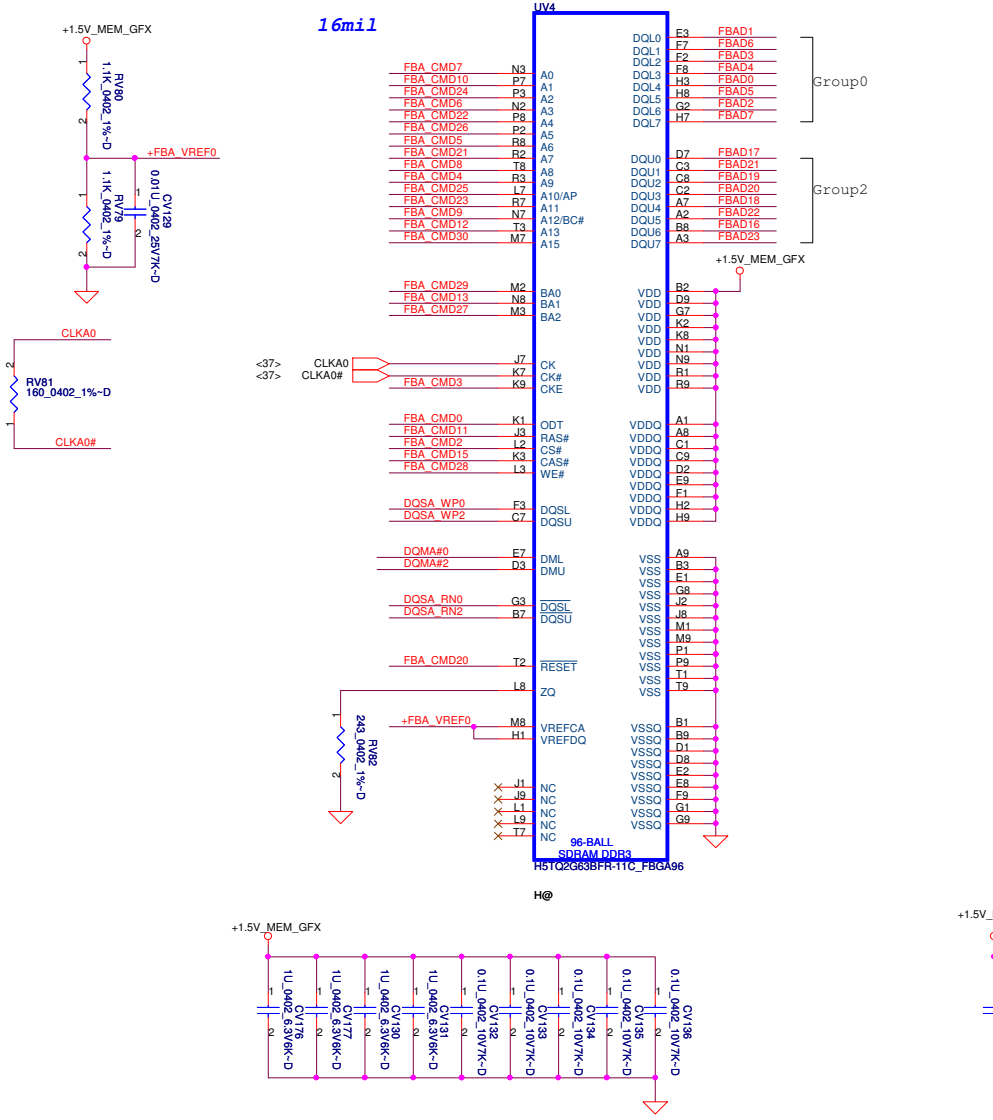
RV262 0_0402_5%
DGPU_PWR_EN#1
0.1U_0603_25V7K @
CV375
QV4 2N7002_SOT23
RV263 @ 2M_0402_5%~D
RV2611 0_0402_5%
CV127 0.1U_0603_25V7K
RV73 510K_0402_5%
CV374 10U_0805_10V4Z
QV3 SI4634DY-T1-E3_SO8~D
CV126 10U_0805_6.3V6M~D
CV376 0.1U_0402_16V4Z~D
+VCCP
+1.05V_RUN_VTT_GFX
B+

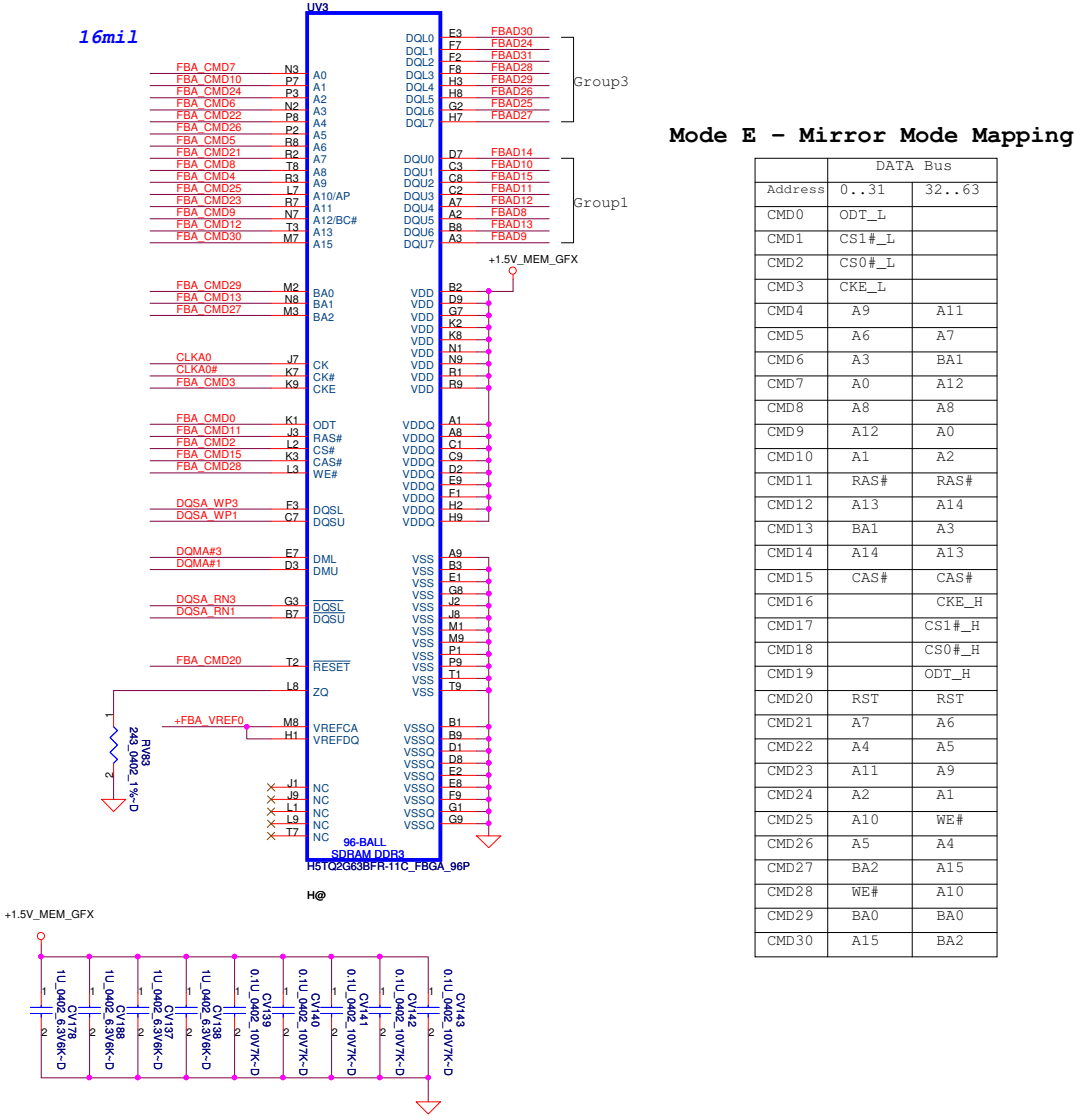
Compal Electronics, Inc.
Title: N12P Memory
Size: Document Number: LA-7451P
Rev: 1.0
Date: Thursday, July 28, 2011
Sheet 37 of 51

Memory Partition A - Lower 32 bits

change to Hynix

FBA_CMD[0..30] FBA_CMD[0..30] <37,39>
FBAD[0..63] FBAD[0..63] <37,39>
DQMA#[0..7] DQMA#[0..7] <37,39>
DQSA_RN[0..7] DQSA_RN[0..7] <37,39>
DQSA_WP[0..7] DQSA_WP[0..7] <37,39>



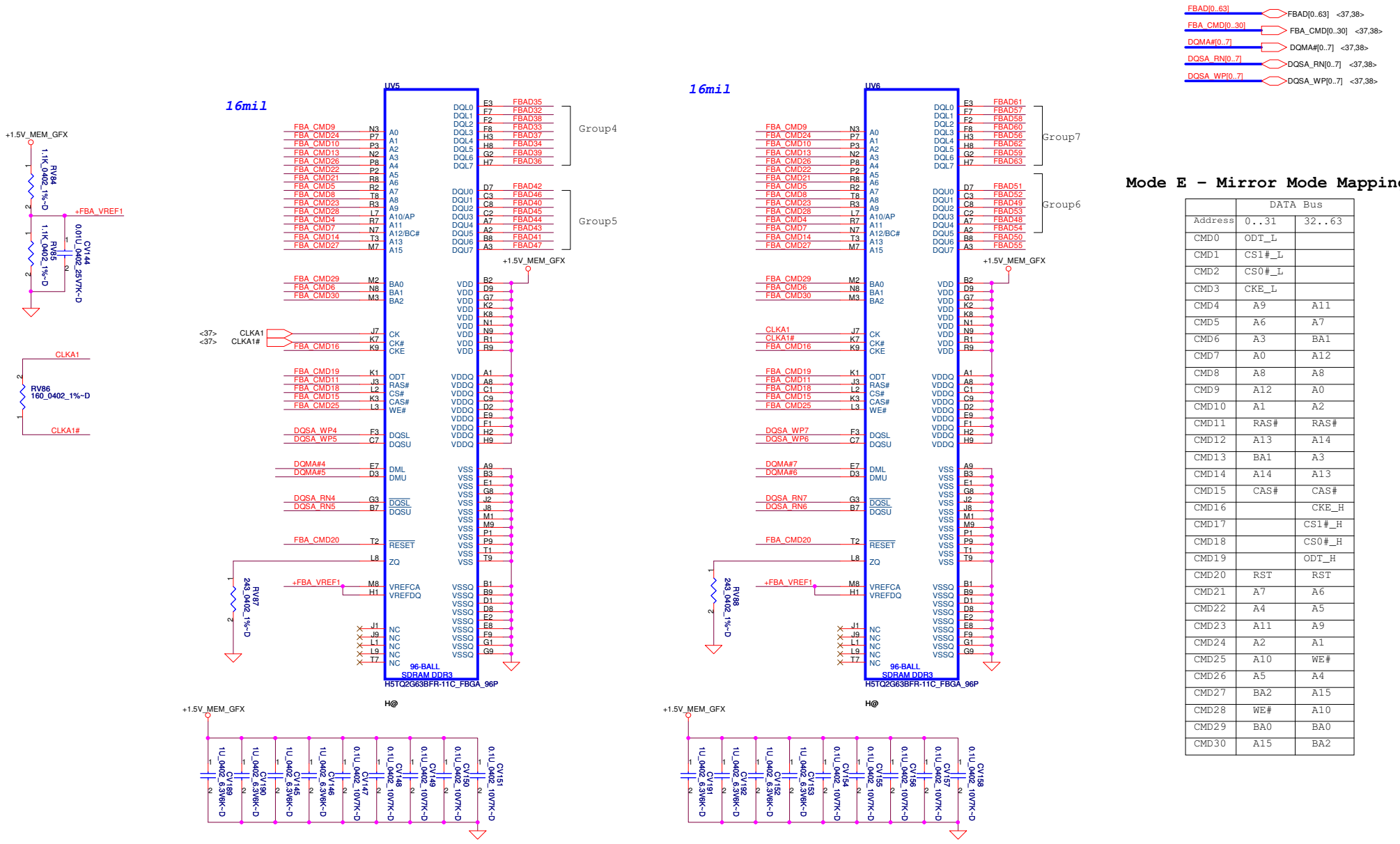


Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

Compal Electronics, Inc.
Title: VRAM A Lower
Size: Document Number: LA-7451P
Rev: 1.0
Date: Thursday, July 28, 2011
Sheet 38 of 51

Memory Partition A - Upper 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

Compal Electronics, Inc.
Title: VRAM A Upper
Size: Document Number: LA-7451P
Rev: 1.0
Date: Thursday, July 28, 2011
Sheet 39 of 51

Version change list (P.I.R. List)

EE section

Item	Reason for change	PG#	Modify List	Date	Phase
1	SMbus signal Pull HIGH	15	Add R983,R984	2011/04/07	PT
2	SMbus signal Pull HIGH	25	Add RV22 ,RV29,QV7	2011/04/07	PT
3	vss pull low	35	Add RV106	2011/04/07	PT
4	hdmi HPD	29	Add R636	2011/04/07	PT
5	GPU_CLKDWN_R PULL HIGH	34	Add RV10	2011/04/07	PT
6	PEG_A_CLKRQ# CONTROL	34	Add RV264, RV265, RV266, RV267, QV9		PT
7	sounds too small	31	Change RC134, RC137 from 47K to 560ohm	2010/10/15	PT
8	protect HDMI plug in noise	29	add CV101	2010/10/15	PT
9	Modify USB3.0 solution	30		2010/10/15	PT
10	change Lan symbol	22	JLAN1	2010/10/15	PT
11	Power LED no light when S3	21	Change JBTN1 Pin1 from +5VS to +5VALW net	2010/10/15	PT
12	ESD request		Add CC70	2010/10/15	PT
13	ESD request		Add CH101	2010/10/17	PT
14	ESD request		Add CC71~CC75	2010/10/17	PT
15	ESD request		Add CC76~CC80	2010/10/17	PT
16	ESD request		Del CFG1,3,8,9,10,11,16,17	2010/10/20	PT
17	USB 3.0 Wake issue	30	Del RI19,Add CI51	2010/10/20	PT
18	USB 3.0 Wake issue	30	Change RI18 Pin1 to UI2 pin7	2010/10/22	PT
19	T		Change BOM UV2,CV107,CV108,RV108,RV109 to remove	2010/10/22	ST
20	LCD timing		Change BOM C549 to SEI24474K80	2010/10/22	ST
21			Change BOM U48 to SA00003R80	2010/10/22	ST
22			Change BOM UV1 to SA00004Q40L	2010/10/22	ST
23				2010/10/24	
24				2010/10/24	PT
25				2010/10/26	PT
26				2010/12/1	ST
27				2010/12/1	ST
28				2010/12/1	ST
29				2010/12/1	ST
30				2010/12/1	ST
31				2010/12/6	ST
32				2010/12/6	ST
33				2010/12/6	ST
34				2010/12/6	ST
35				2010/12/8	ST
36				2010/12/8	ST
37				2010/12/8	ST
38				2010/12/8	ST
39				2010/12/9	ST
40					
41					
42					
43					
44					
45					
46					
47					
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50					
51					
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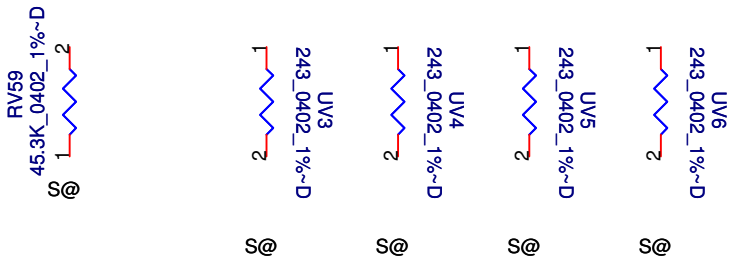
53					
54					

Compal Electronics, Inc.

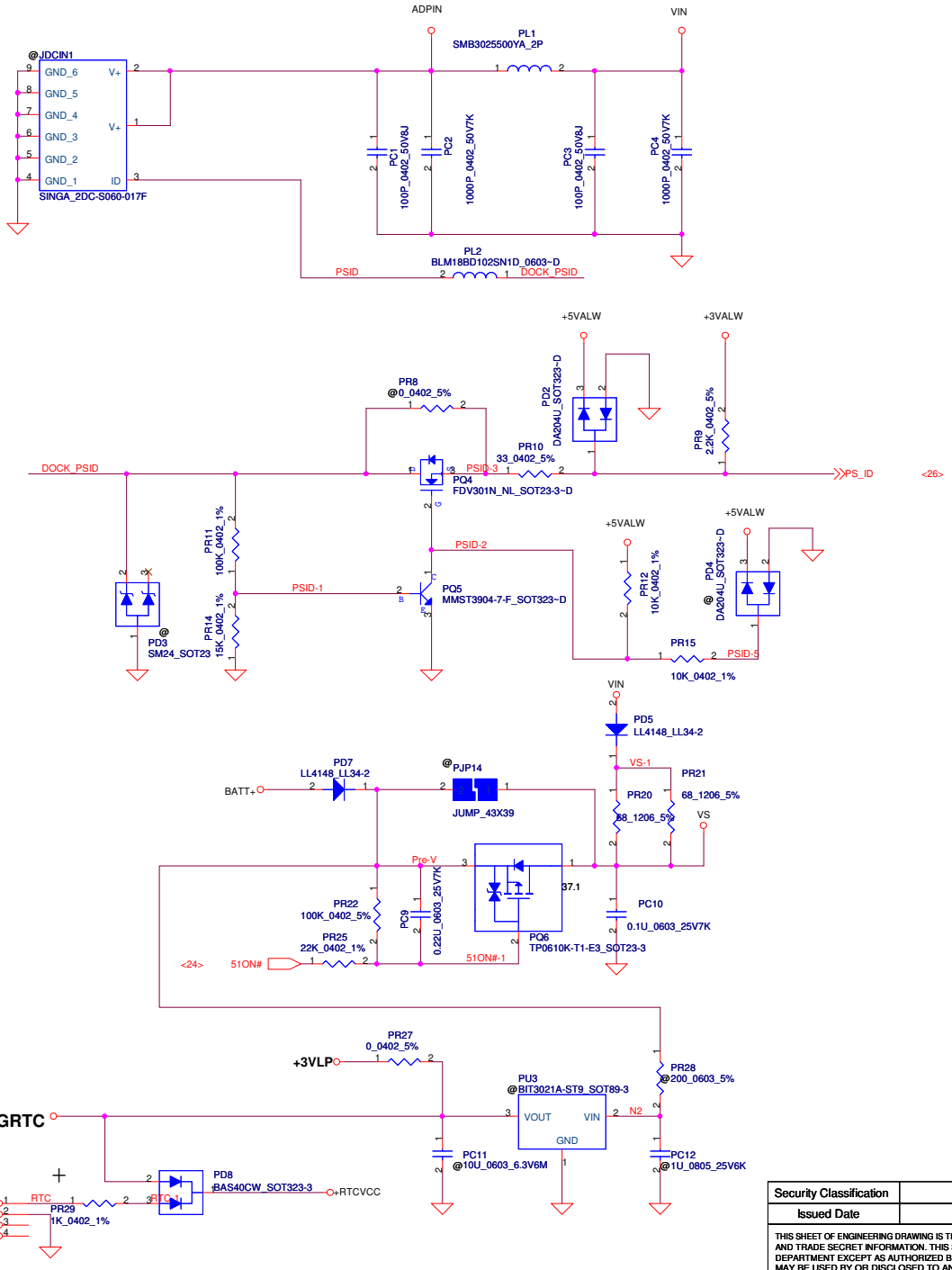
Title: HW Changed-List History-1

Size | Document Number: LA-6961P | Rev: 1.0

Date: Thursday, July 28, 2011 | Sheet 40 of 51



Title	<Title>	
Size: A	Document Number: LA-7451P	Rev: 0.2
Date: Thursday, July 28, 2011	Sheet 41 of 51	



Compal Electronics, Inc.

Title: PWR-DCIN / Vin Detector

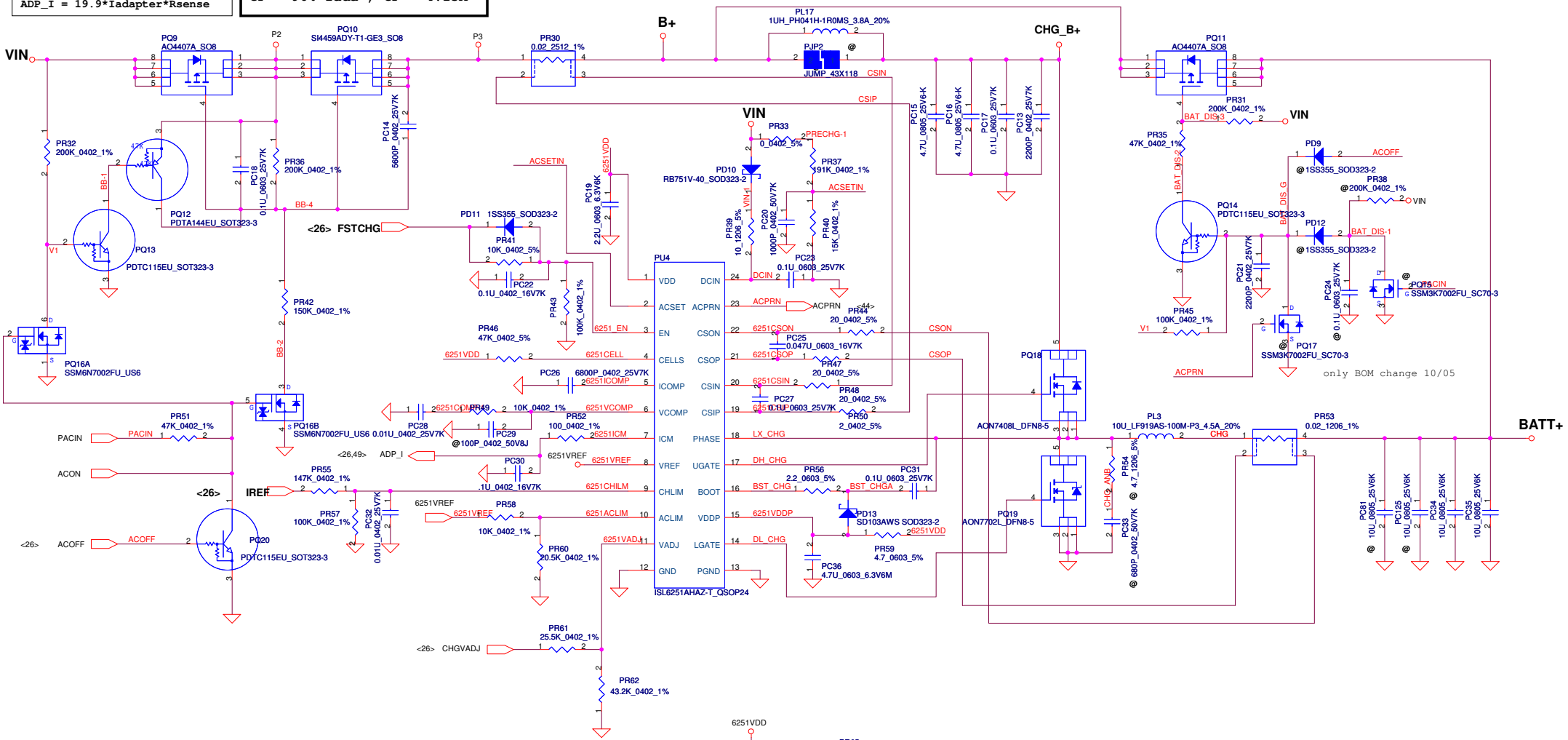
Size: Custom | Document Number | Rev: 1.0

Date: Thursday, July 28, 2011 | Sheet 42 of 51

Iada=0~4.615A(90W/19.5V=4.615A)

ADP_I = 19.9*Iadapter*Rsense

CP = 90%*Iada ; CP = 4.15A



CP mode

Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)

Vaclim=2.39*((20.5K//152K)/((10K//152K)+(20.5K//152K)))

CC=2.8A

IREF=1*Icharge

IREF=0.25V~3.3V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 4S LI-ON Cells	14800mV	14.80V

CHGVADJ	CV mode
0V	3.99V per cell
1.93V	4.2V per cell
3.3V	4.35V per cell

Security Classification	Compal Secret Data		
Issued Date	2010/12/24	Deciphered Date	2011/12/24

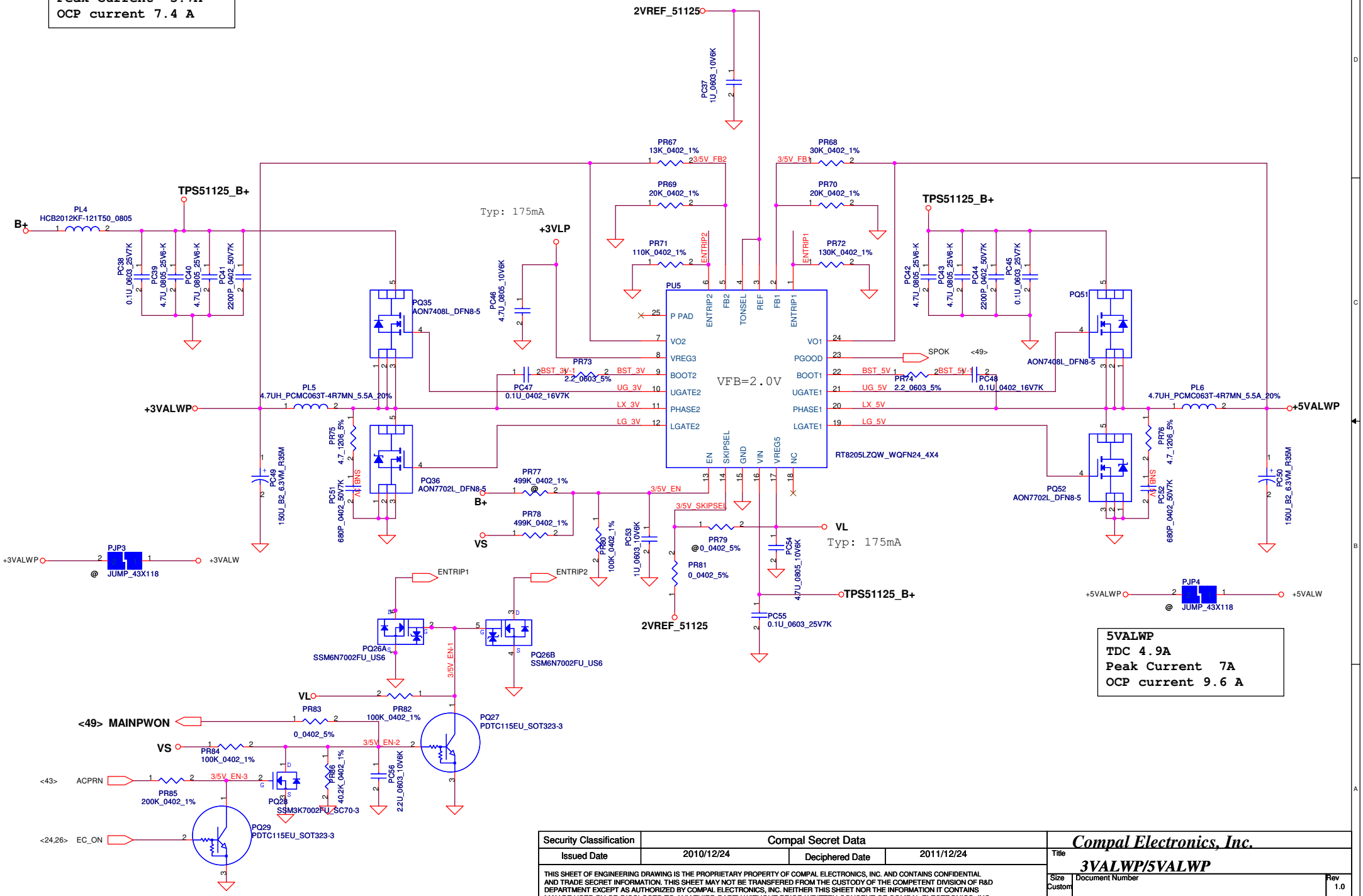
Compal Electronics, Inc.

Title: PWR-CHARGER

Size: Custom | Document Number | Rev: 1.0

Date: Thursday, July 28, 2011 | Sheet 43 of 51

3.3VALWP
TDC 4.02 A
Peak Current 5.7A
OCP current 7.4 A



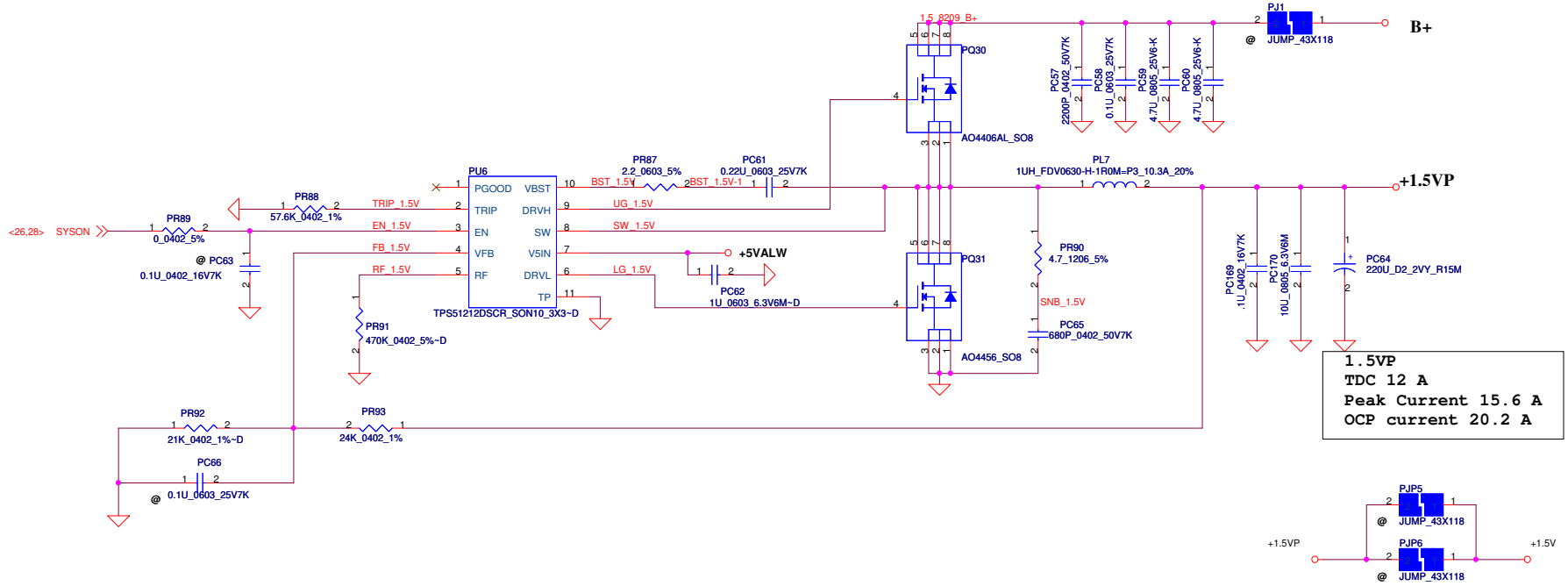
5VALWP
TDC 4.9A
Peak Current 7A
OCP current 9.6 A

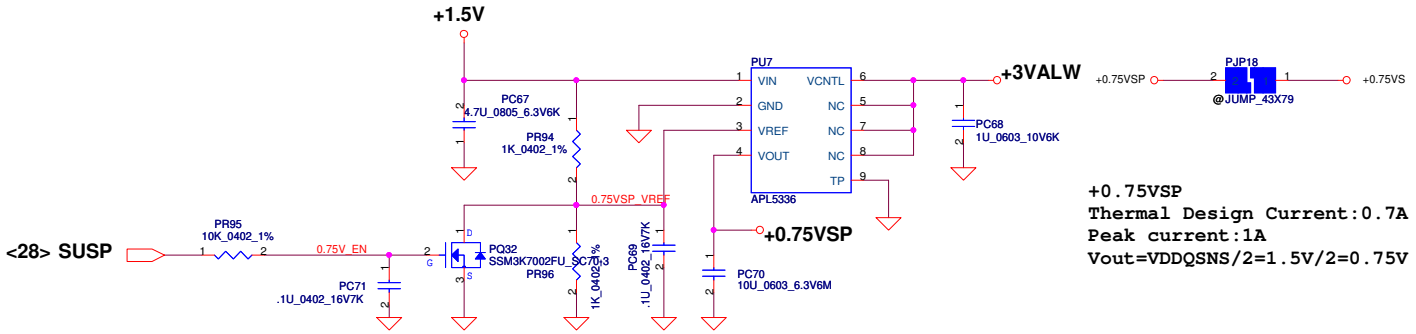
Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number | Rev: 1.0

Date: Thursday, July 28, 2011 | Sheet 44 of 51





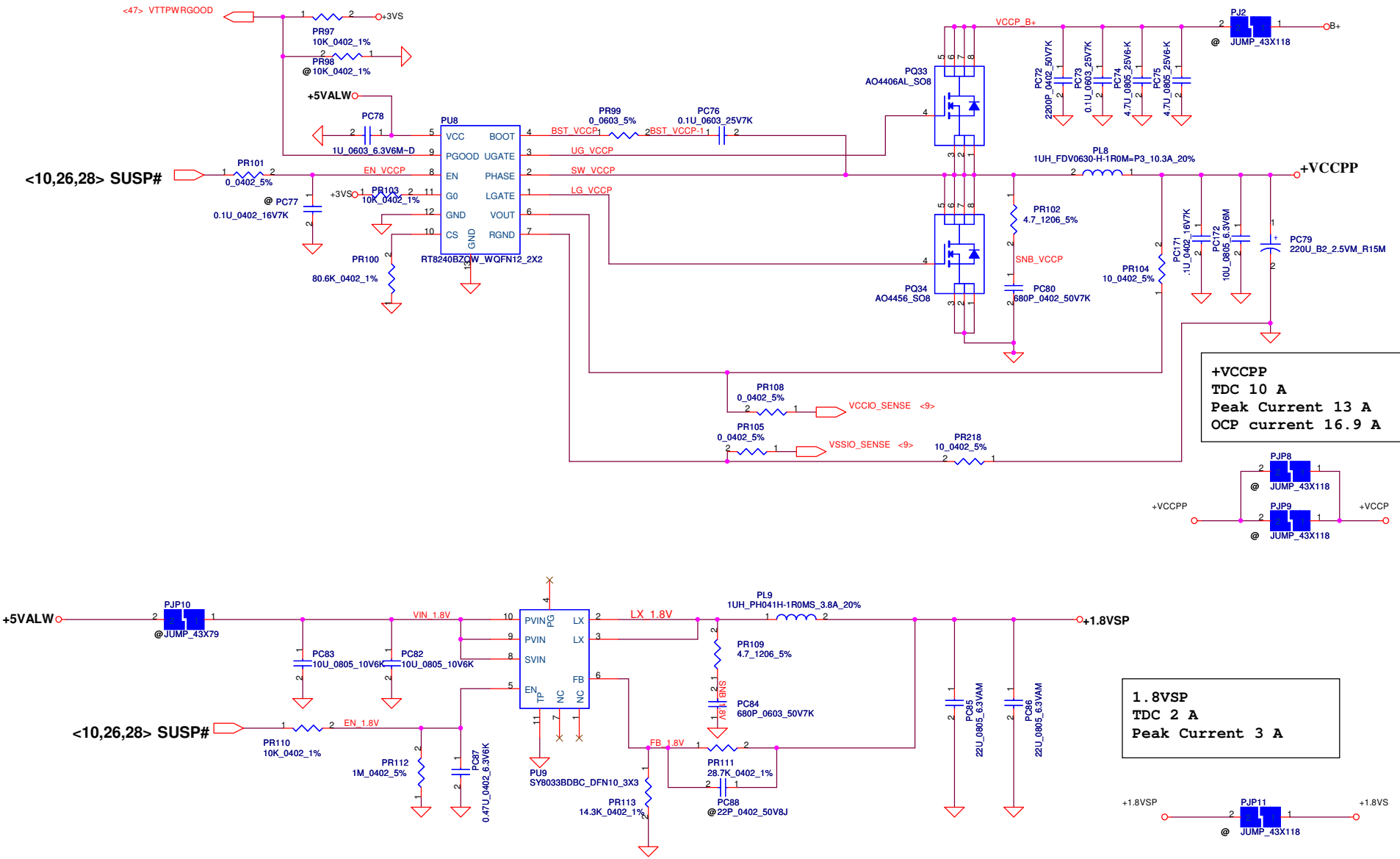
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: ***PWR-+1.5VP/+0.75V***

Size	Document Number	Rev
Custom		1.0

Date: Thursday, July 28, 2011 | Sheet 45 of 51



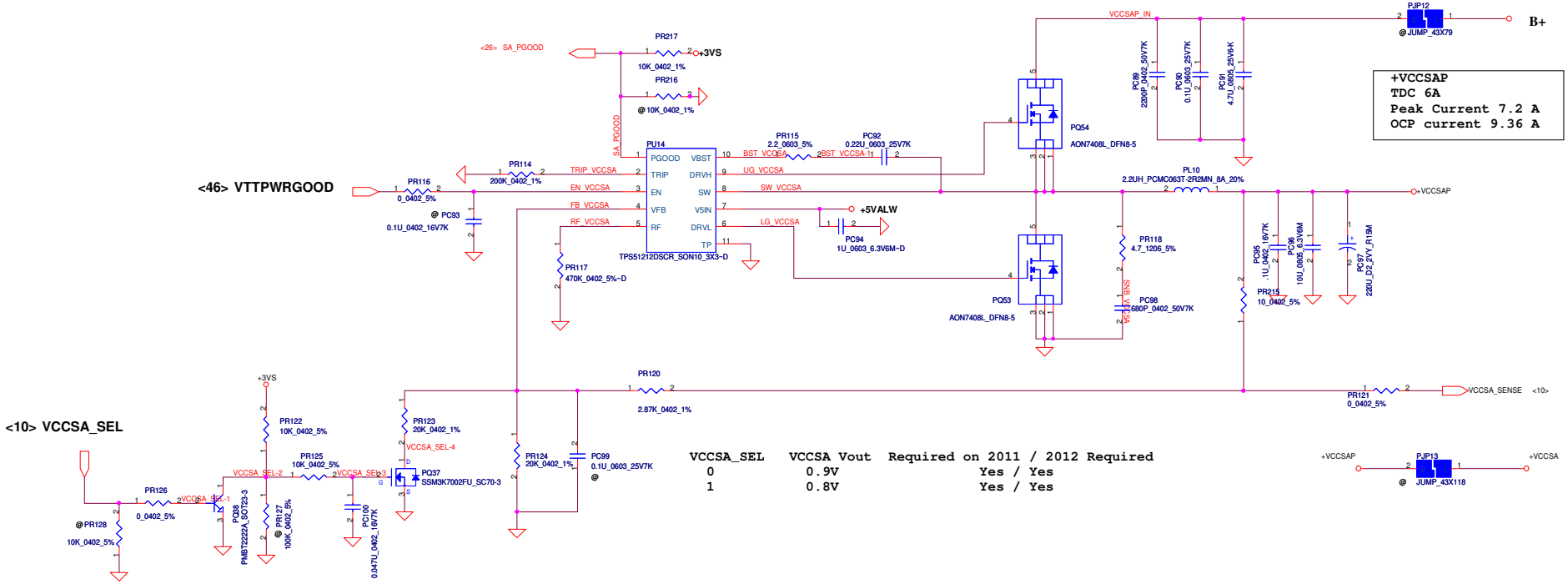
Security Classification	Compal Secret Data		
Issued Date	2010/12/24	Deciphered Date	2011/12/24

Compal Electronics, Inc.

Title: +VCCP/+1.8VSP

Size	Document Number	Rev
Custom		1.0

Date: Thursday, July 28, 2011 Sheet 46 of 51



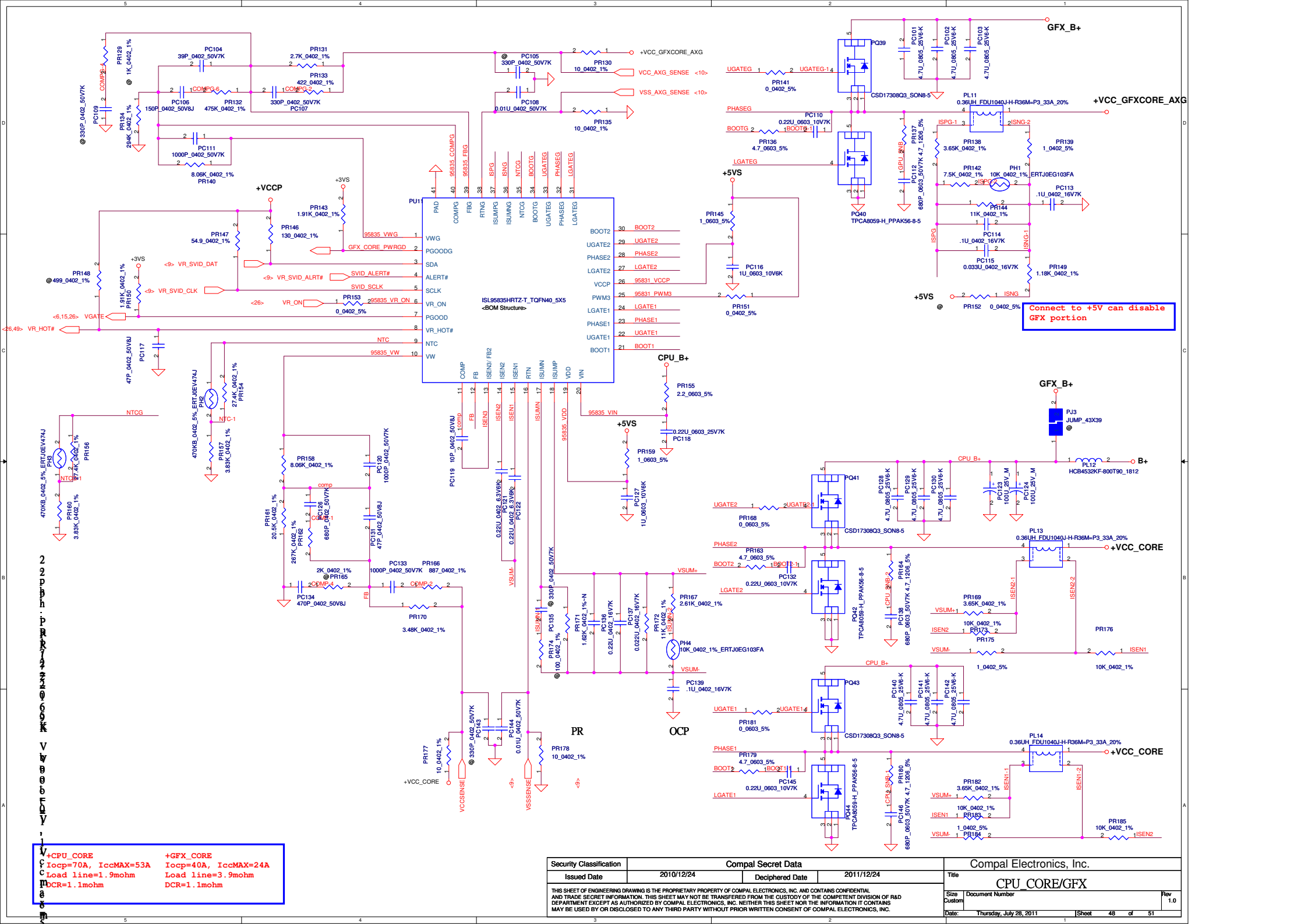
Security Classification	Compal Secret Data		
Issued Date	2010/12/24	Deciphered Date	2011/12/24

Compal Electronics, Inc.

Title: *+VCCSAP*

Size	Document Number	Rev
C		1.0

Date: Thursday, July 28, 2011 | Sheet 47 of 51


ISL95835HRTZ-T_TQFN40_5X5
<BOM Structure>
PU11
PAD
COMPG
FBG
RTNG
ISUMPG
ISUMNG
NTCG
BOOTG
UGATEG
PHASEG
LGATEG
VWG
PGOODG
SDA
ALERT#
SCLK
VR_ON
PGOOD
VR_HOT#
NTC
VW
BOOT2
UGATE2
PHASE2
LGATE2
VCCP
PWM3
LGATE1
PHASE1
UGATE1
BOOT1
COMP
FB
ISEN3/ FB2
ISEN2
ISEN1
RTN
ISUMN
ISUMP
VDD
VIN
+VCCP
+3VS
+5VS
CPU_B+
GFX_B+
+VCC_GFXCORE_AXG
+VCC_CORE
B+
VCC_AXG_SENSE <10>
VSS_AXG_SENSE <10>
95835_VWG
GFX_CORE_PWRGD
SVID_ALERT#
SVID_SCLK
VR_ON
95835_VR_ON
95835_VIN
95835_VDD
95831_VCCP
95831_PWM3
VSUM+
VSUM-
VCCSENSE
VSSSENSE
CSD17308Q3_SON8-5
TPCA8059-H_PPAK56-8-5
PR
OCP
Connect to +5V can disable GFX portion
+CPU_CORE
Iocp=70A, IccMAX=53A
Load line=1.9mohm
DCR=1.1mohm
+GFX_CORE
Iocp=40A, IccMAX=24A
Load line=3.9mohm
DCR=1.1mohm
Security Classification
Compal Secret Data
Issued Date
2010/12/24
Deciphered Date
2011/12/24
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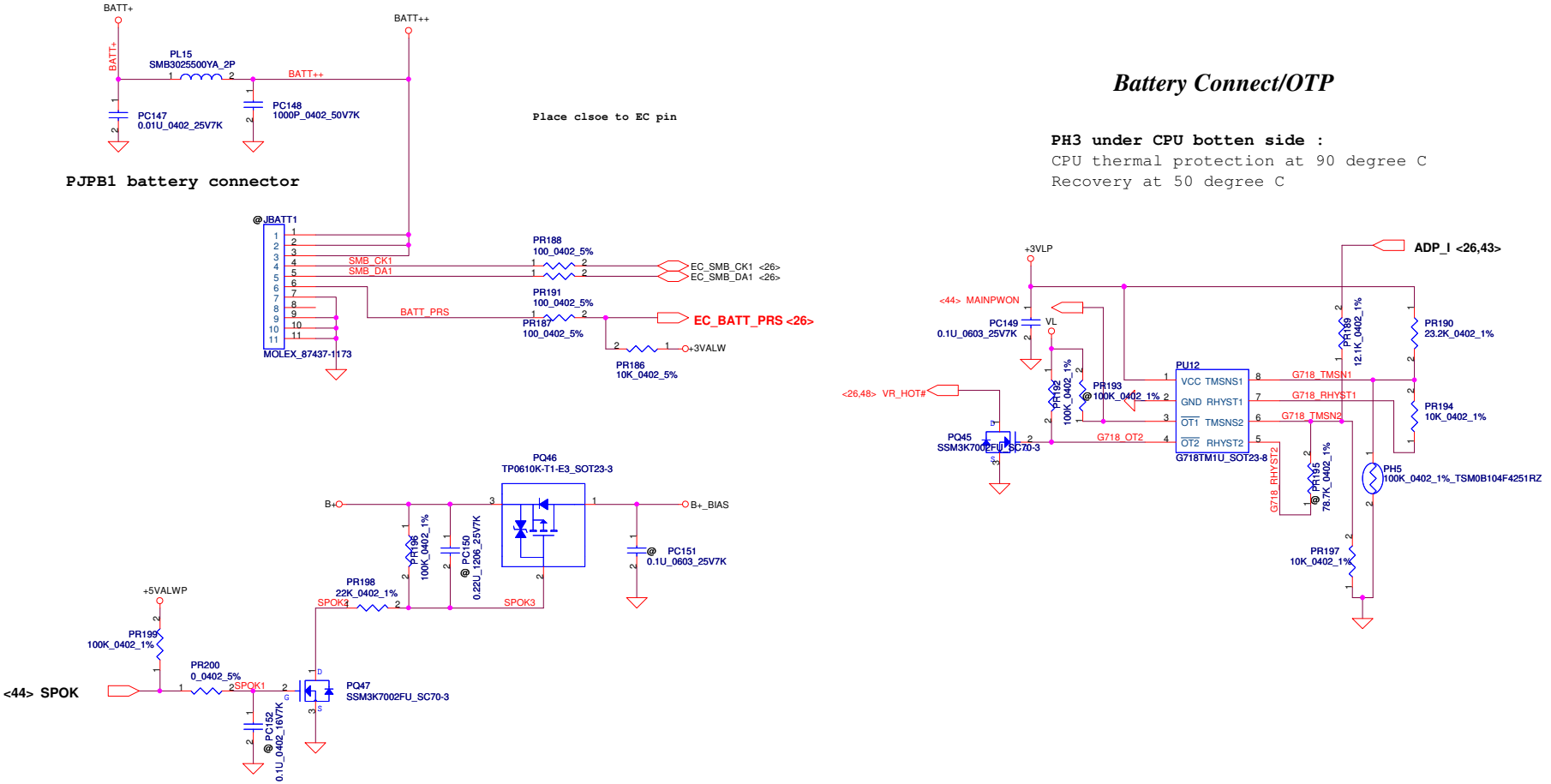
Compal Electronics, Inc.
Title
CPU_CORE/GFX
Size
Custom
Document Number
Rev
1.0
Date:
Thursday, July 28, 2011
Sheet
48
of
51

Battery Connect/OTP



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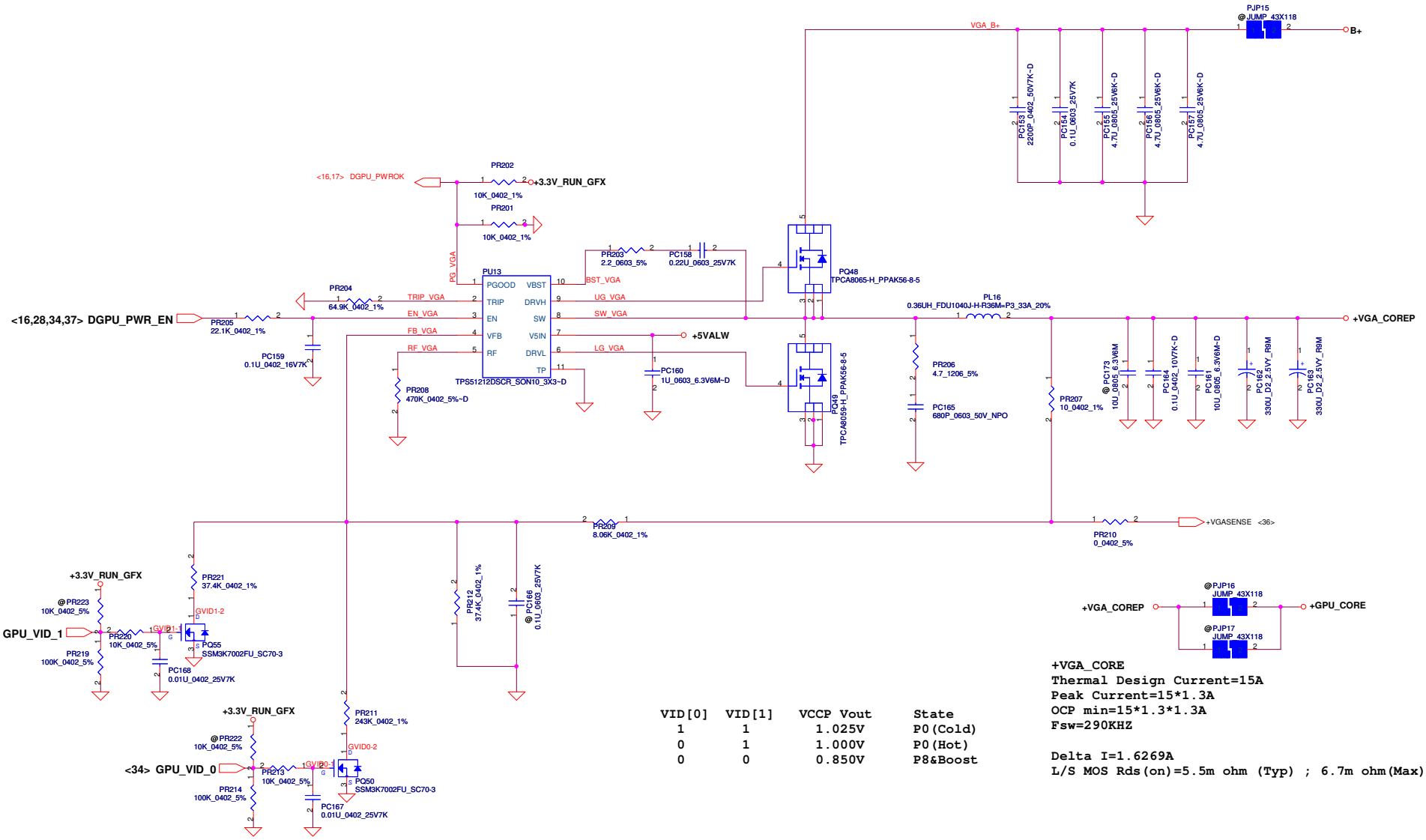
Issued Date	2010/12/24	Deciphered Date	2011/12/24

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN		
Size: Custom	Document Number		Rev: 1.0
Date: Thursday, July 28, 2011	Sheet 49 of 51		



VID[0]	VID[1]	VCCP Vout	State
1	1	1.025V	P0(Cold)
0	1	1.000V	P0(Hot)
0	0	0.850V	P8&Boost

+VGA_CORE
Thermal Design Current=15A
Peak Current=15*1.3A
OCP min=15*1.3*1.3A
Fsw=290KHZ

Delta I=1.6269A
L/S MOS Rds(on)=5.5m ohm (Typ) ; 6.7m ohm(Max)

Security Classification	Compal Secret Data		
Issued Date	2010/12/24	Deciphered Date	2011/12/24

Compal Electronics, Inc.

Title: VGA_CORE

Size	Document Number	Rev
Custom		1.0

Date: Thursday, July 28, 2011 | Sheet 50 of 51

Version change list (P.I.R. List)

Item	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	modify Vcore and GFX boost resistance		P48	change PR136,PR163,PR179 to 2.2 +-5% 0603.	2011.2.10	before SSI
2	modify VGA FB resistance		P50	change PR211 to 243K +-1% 0402. PR221 to 37.4K +-1% 0402.	2011.3.24	SSI
3	modify 1.5V Enable signal		P45	change PR81 connect to SYSON.	2011.3.24	SSI
4	modify ADP_I protection		P49	change PR189 to 12.1k +-5% 0402.	2011.3.24	SSI
5	integrate mosfet		P45	change PQ53 PQ54 to AON7408L		
6	modify Vcore and GFX's loadline and OCP		P48	change PR171 to 1.62K +-1% 0402 change PR170 to 3.48K +-1% 0402 change PR149 to 1.18K +1% 0402 change PR131 to 2.7K +-1% 0402 change PC115 to .033U 16V K X7R 0402		
7	modify VGA for HW team suggest item		P50	add PR219 100K +-5% 0402 remove PR223 10K +-5% 0402 change PR205 to 22.1K +-1% 0402		
8	integrate mosfet		P45 P47	change PQ32 to SSM3K7002FU 1N SC70-3 change PQ37 to SSM3K7002FU 1N SC70-3		
9	add capacitance for RF team suggest item		P43 P45 P46 P50	change PC81 PC125 to 10U 25V K X5R 0805 H1.25 change PC169 to .1U 16V K X7R 0402 change PC170 to 10U 6.3V M X5R 0805 H1.25 change PC171 to .1U 16V K X7R 0402 change PC172 to 10U 6.3V M X5R 0805 H1.25 change PC173 to 10U 6.3V M X5R 0805 H1.25		
10	modify 1.5V OCP resistance		P45	change PR88 to 57.6K +-1% 0402		
11	modify VCCP OCP resistance		P46	change PR100 to 80.6K +-1% 0402		
12	modify choke footprint for DFX requirement			change PL5,PL6,PL7,PL8,PL10 to TAI-T_VMPI0703AR-100M-Z01_2P		
13	modify PQ11 Vgs resistance		P43	change PR31 to 200K +-1% 0402 change PR35 to 47K +-1% 0402		
14	modify the net name of SPOK-'		P49	change the net name of PQ47 pin2 to SPOK1 change the net name of PQ47 pin1 to SPOK2 change the net name of PQ46 pin2 to SPOK3		
15	modify PU12 vcc power from +3VALW to +3VLP		P49	change PR190.1 to +3VLP change PR149.1 to +3VLP change PU12.1 to +3VLP		
16	modify OTP resistance		P49	change PR190 to 23.2K +-1% 0402 change PR194 to 10K +-1% 0402		
17	modify VCORE VCCP resistance		P48	change PR145 to 1 +-5% 0603		

Size	Document Number	Rev
Custom		1.0

Date: Thursday, July 28, 2011 Sheet 51 of 51