QIQY6

Brandy3.0 (Y500)

LA-8692P Rev0.2 Schematic

Intel IVY Bridge Processor with DDRIII + Panther Point PCH
nVIDIA N13P GT-1 + 2nd VGA N13P GT-1

2012-02-05 Rev0.2

Security Classification	LC Future Center Secret Data		
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Title	Cover Page		
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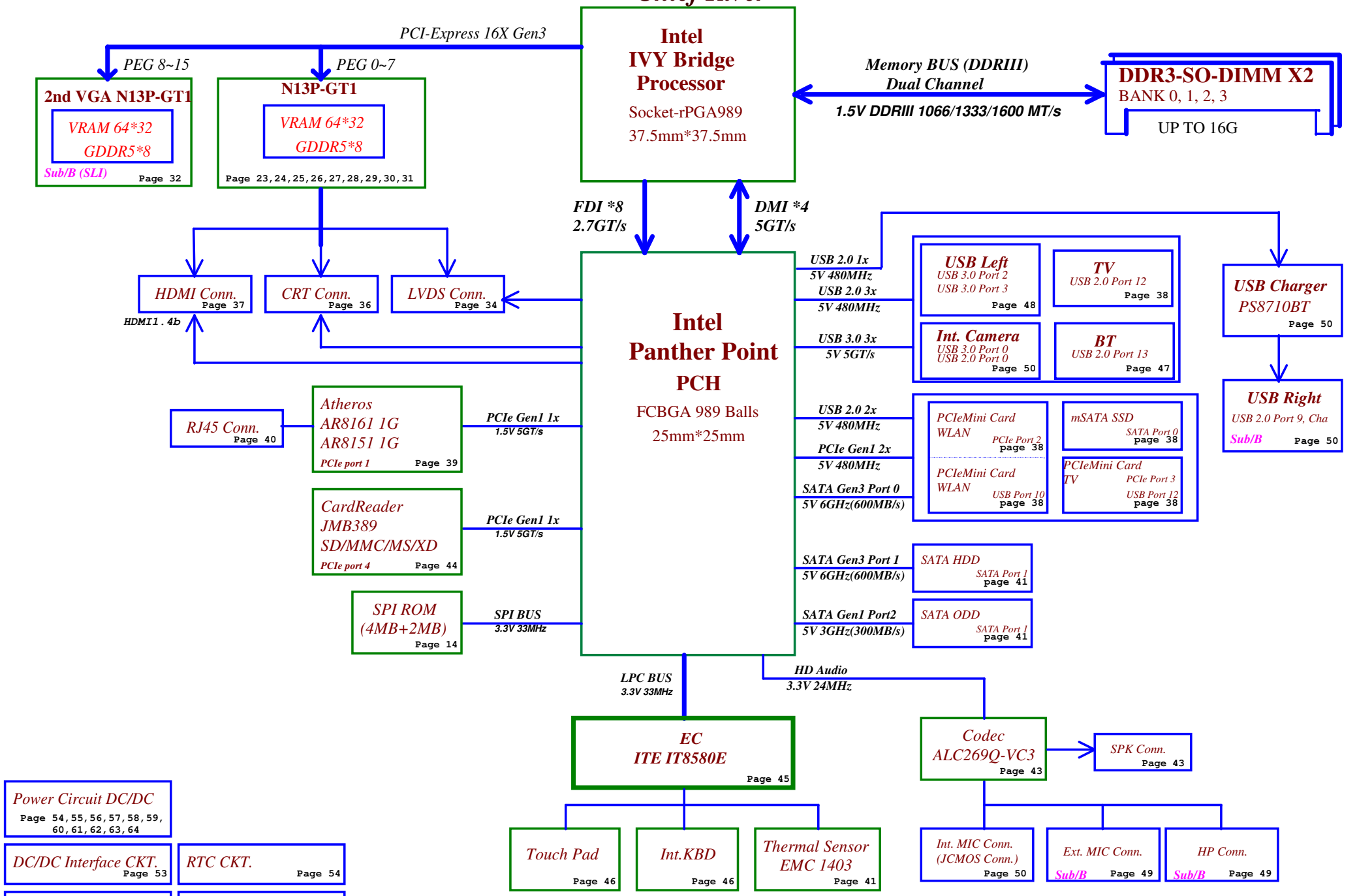
Chief River



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Title	MB Block Diagram		
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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	IT8580E +3VALW	X	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	IT8580E +3VALW	X	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	V +3VS	X	V +3VS	X	X	V +3VS	X

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
	1	0	Camera Camera
	XHCI 2	1	
EHCI1	3	2	USB Port (Left Side) USB Port (Left Side)
	4	3	USB Port (Left Side) USB Port (Left Side)
		4	
		5	
		6	
		7	
EHCI2		8	
		9	USB Port (Right Side)
		10	Mini Card(WLAN)
		11	
		12	Mini Card(TV)
		13	Blue Tooth

PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	TV
4	Card Reader
5	
6	
7	
8	

BOM Structure Table

BOM Structure	BTO Item
HDMI@	HDMI part
TV@	TV module part
CMOS@	CMOS Camera part
8161@	AR8161 LAN part
8151@	AR8151 LAN part
8161S@	AR8161 LAN surge part
8151S@	AR8151 LAN surge part
SURGE@	AR8151&8161 LAN surge part
X76@	X76 Level part for VRAM
GC6@	NV CG6 support part
NOGC6@	NV no CG6 support part
AOAC@	AOAC support part
KBL@	K/B Light part
ME@	ME part
OPT@	For optimus function part
SLI@	For SLI function part
DS3@	Deep S3 support part
GT@	NV chip part
@	Unpop

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Master VGA	0x9E
Slave VGA	0x9C

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

zzz

DA80000T20J

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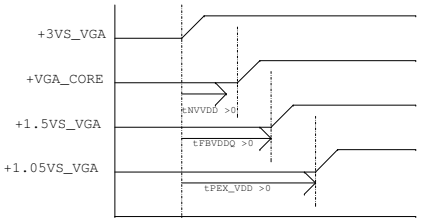
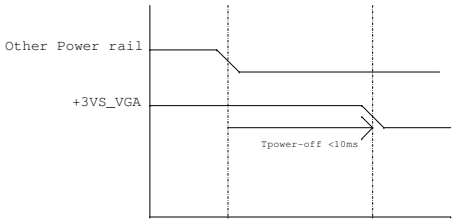
Hot plug detect for IFP link E

VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	_	VGA_BL_PWM
GPIO3	OUT	_	VGA_ENVDD
GPIO4	OUT	_	VGA_ENBKL
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	_	DPRSLPVR_VGA
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GPIO9
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	_	FB_CLAMP_TOGGLE_REQ#
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	_	GPIO16
GPIO17	IN	N/A	GPIO17
GPIO18	IN	-	dGPU_HDMI_HPD
GPIO19	IN	_	GPIO19



1. all power rail ramp up time should be larger than 40us



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID
N13P-GT (28nm)	0x0FDB

	setting	I2C Slave addrees ID
SMB_ALT_ADDR (ROM_SO Bit 1)	0	0x9E
	1	0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GT1 28nm	PU 10K	PU 25K GC6@ PU 5K OPT@,SLI@	PU 45K	PD 5K	PD 10K	PU 5K SLI@ PD 5K OPT@	PD 45K

GPU		N13P-GT		
FB Memory (GDDR5)		ROM_SI		
Samsung 2500MHz	K4G10325FD-FC04			
	32Mx32	PD 45K		
Hynix 2500MHz	H5GQ1H24BFR-T2C			
	32Mx32	PD 35K		
Samsung 2500MHz	K4G20325FD-FC04			
	64Mx32	PD 30K		
Hynix 2500MHz	H5GQ2H24AFR-T2C			
	64Mx32	PD 25K		

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Title: VGA Notes List

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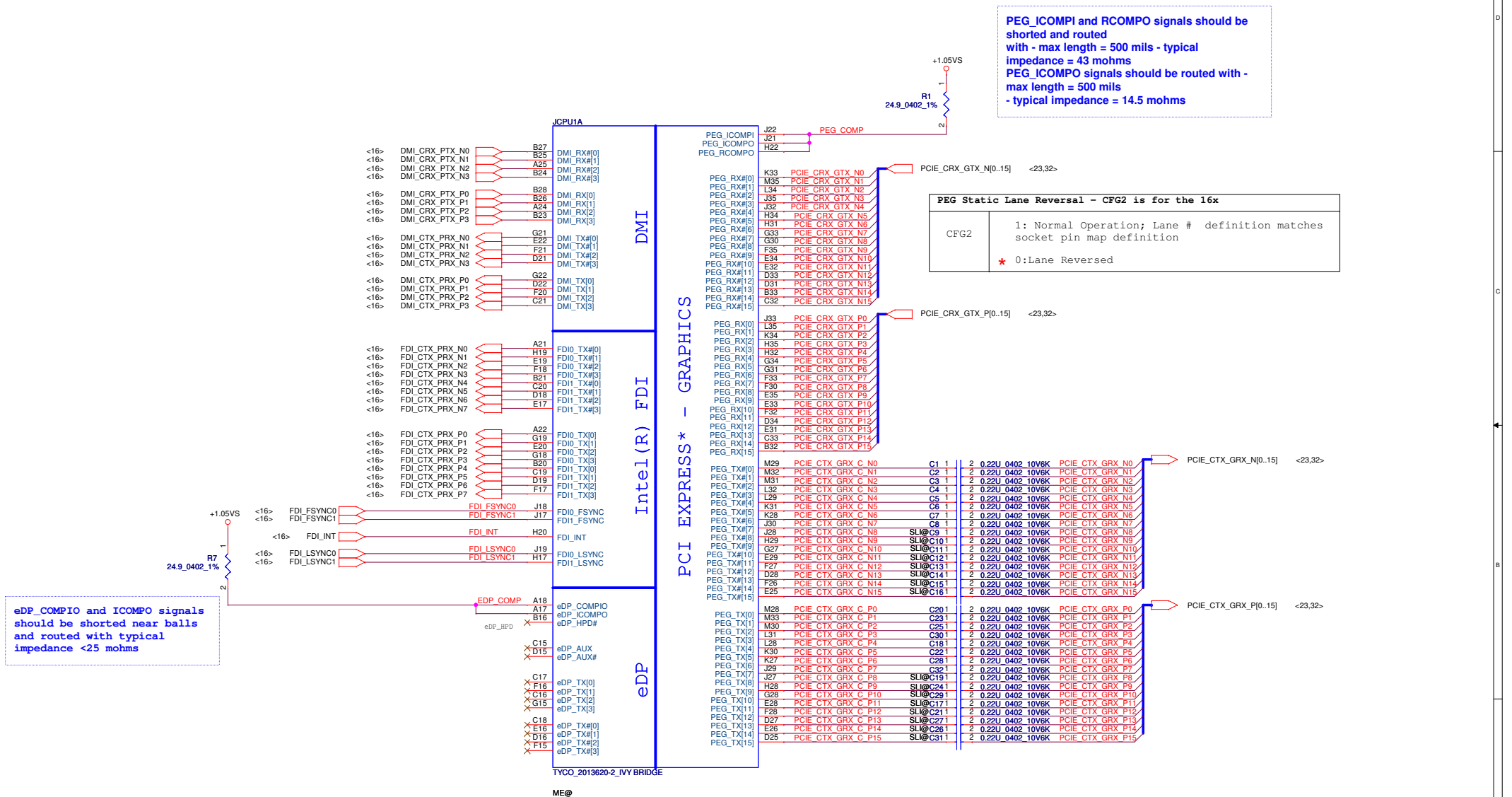

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Title: PROCESSOR(1/7) DMI,FDI,PEG

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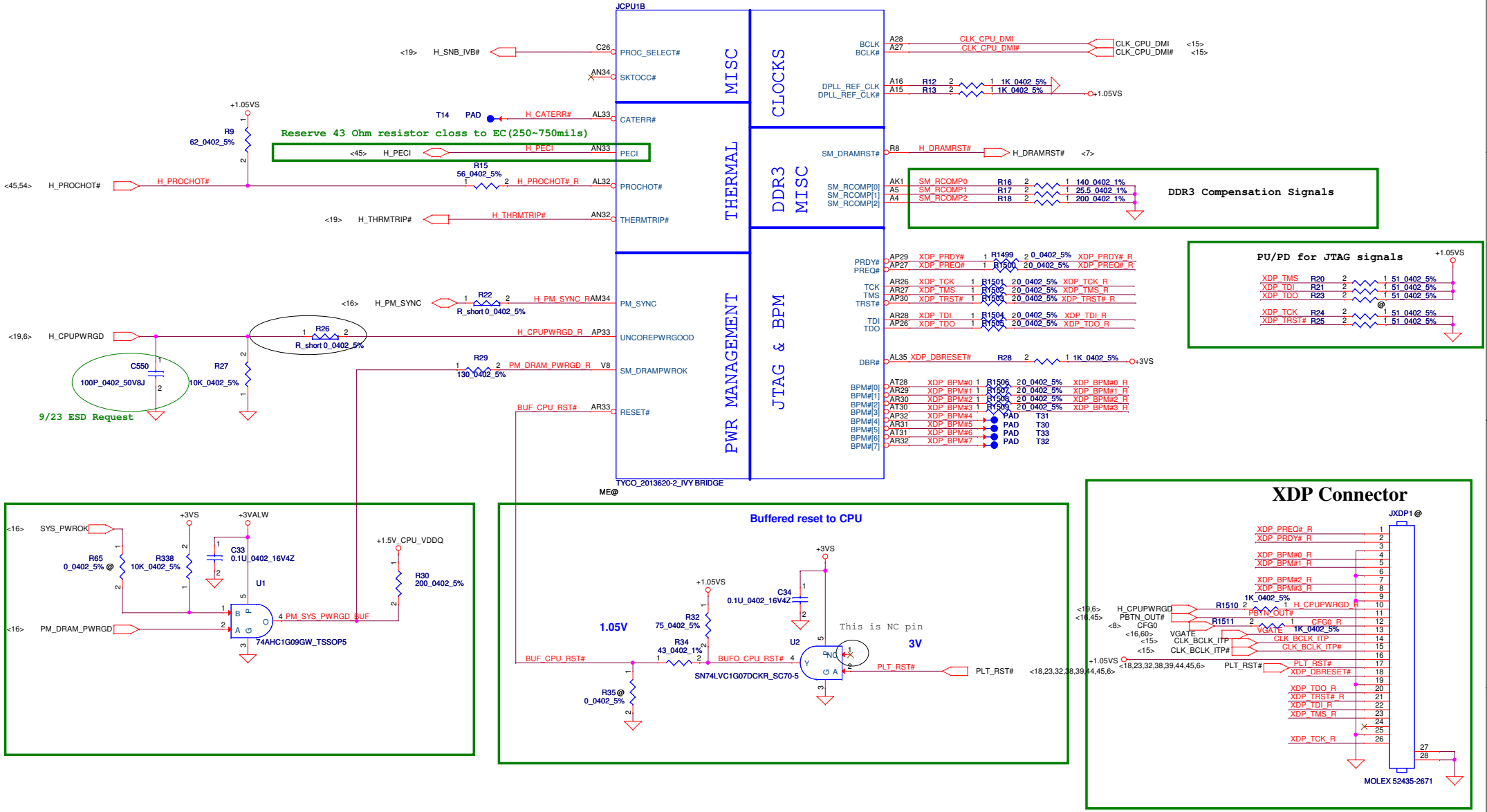

Security Classification	LC Future Center Secret Data		
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Title	PROCESSOR(2/7) PM,XDP,CLK		
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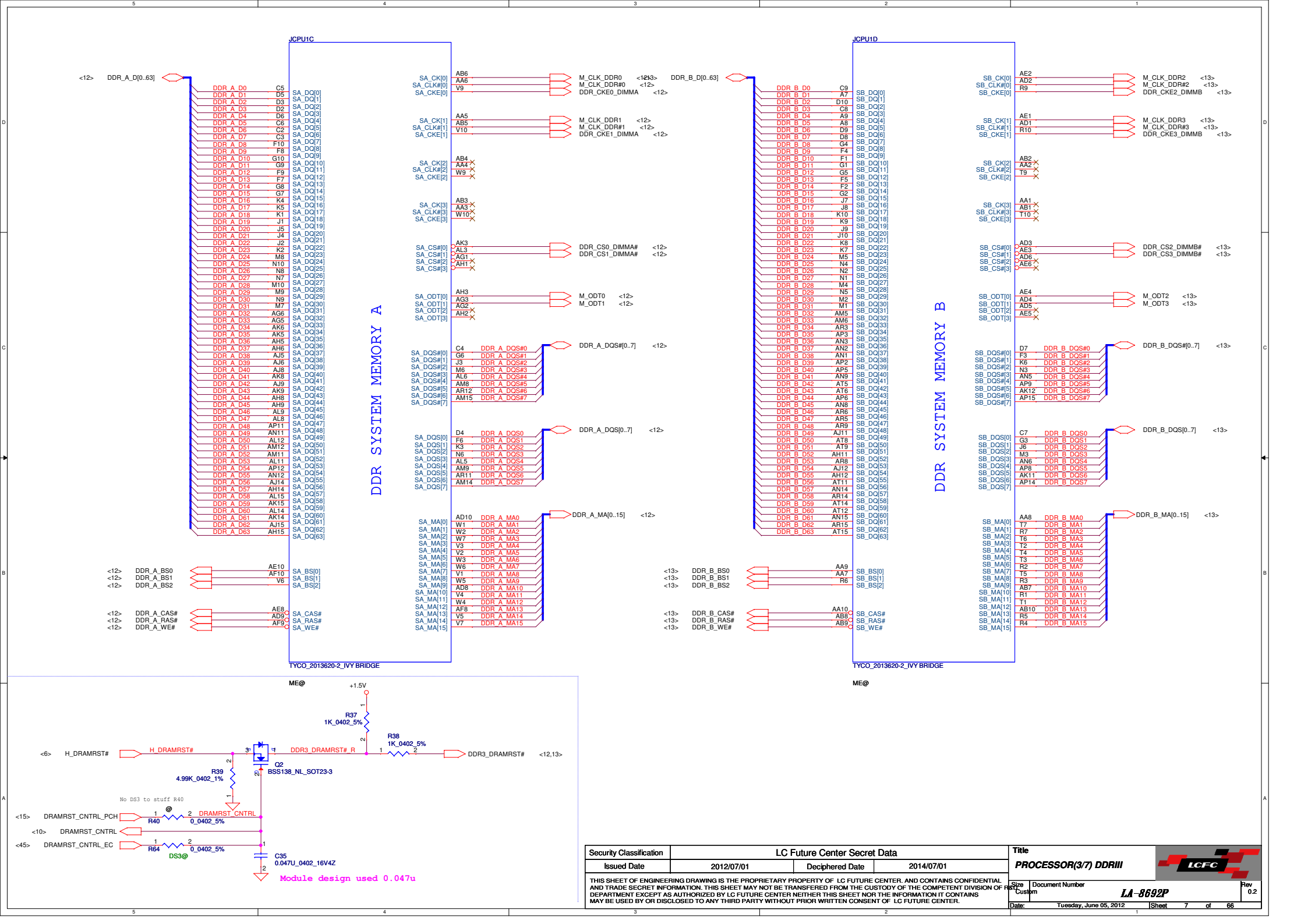

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Title: PROCESSOR(3/7) DDRIII

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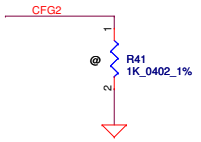
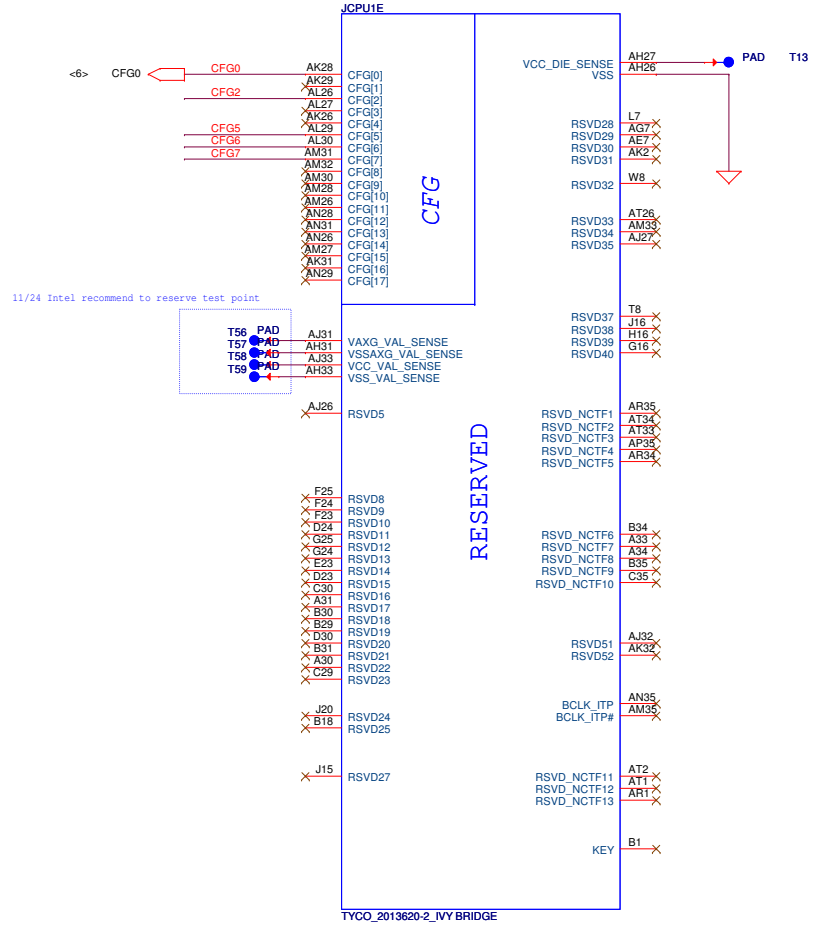
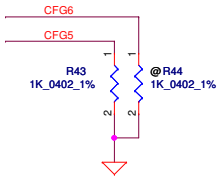
CFG Straps for Processor



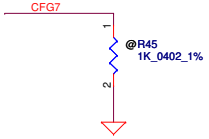
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 – Device 1 functions 1 and 2 disabled *10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title	PROCESSOR(4/7) RSVD,CFG		
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POWER

JCPU1F

+VCC_CORE

QC=94A
DC=53A

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
V35	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P35	VCC91
P34	VCC92
P33	VCC93
P32	VCC94
P31	VCC95
P30	VCC96
P29	VCC97
P28	VCC98
P27	VCC99
P26	VCC100

CORE SUPPLY

PEG AND DDR

+1.05VS

8.5A

VCCIO1	AH13
VCCIO2	AH10
VCCIO3	AG10
VCCIO4	AC10
VCCIO5	Y10
VCCIO6	U10
VCCIO7	P10
VCCIO8	L10
VCCIO9	J14
VCCIO10	J13
VCCIO11	J12
VCCIO12	J11
VCCIO13	H14
VCCIO14	H12
VCCIO15	H11
VCCIO16	G14
VCCIO17	G13
VCCIO18	G12
VCCIO19	F14
VCCIO20	F13
VCCIO21	F12
VCCIO22	F11
VCCIO23	E14
VCCIO24	E12
VCCIO25	E11
VCCIO26	D14
VCCIO27	D13
VCCIO28	D12
VCCIO29	D11
VCCIO30	C14
VCCIO31	C13
VCCIO32	C12
VCCIO33	C11
VCCIO34	B14
VCCIO35	B12
VCCIO36	A14
VCCIO37	A13
VCCIO38	A12
VCCIO39	A11
VCCIO40	J23

SVID

Reserve 0.1u to avoid noise

+1.05VS

Place the PU resistor close to CPU

C36 0.1U_0402_10V7K

R46 75_0402_5%

VIDALERT# AJ29 H_CPU_SVIDALRT# R47 43_0402_5%

VIDSCLK AJ30 H_CPU_SVIDCLK R48 R_short 0_0402_5%

VIDSOUT AJ28 H_CPU_SVIDDAT R49 R_short 0_0402_5%

VR_SVID_ALRT# <60>

VR_SVID_CLK <60>

VR_SVID_DAT <60>

R50 130_0402_5% +1.05VS

Place the PU resistor close to CPU

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

SENSE LINES

+VCC_CORE

R51 100_0402_1%

VCC_SENSE AJ35 VCCSENSE_R R52 R_short 0_0402_5%

VSS_SENSE AJ34 VSSSENSE_R R53 R_short 0_0402_5%

VCCSENSE <60>

VSSSENSE <60>

R1294 10_0402_1% +1.05VS

VCCIO_SENSE B10 VCCIO_SENSE

VSS_SENSE_VCCIO A10 VSSIO_SENSE

VCCIO_SENSE <58>

R1297 10_0402_1%

R54 100_0402_1%

VSS_SENCE 100ohm +-1% pull-down to GND near processor

TYCO_2013620-2_IVYBRIDGE

ME@

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Title: PROCESSOR(5/7) PWR,BYPASS

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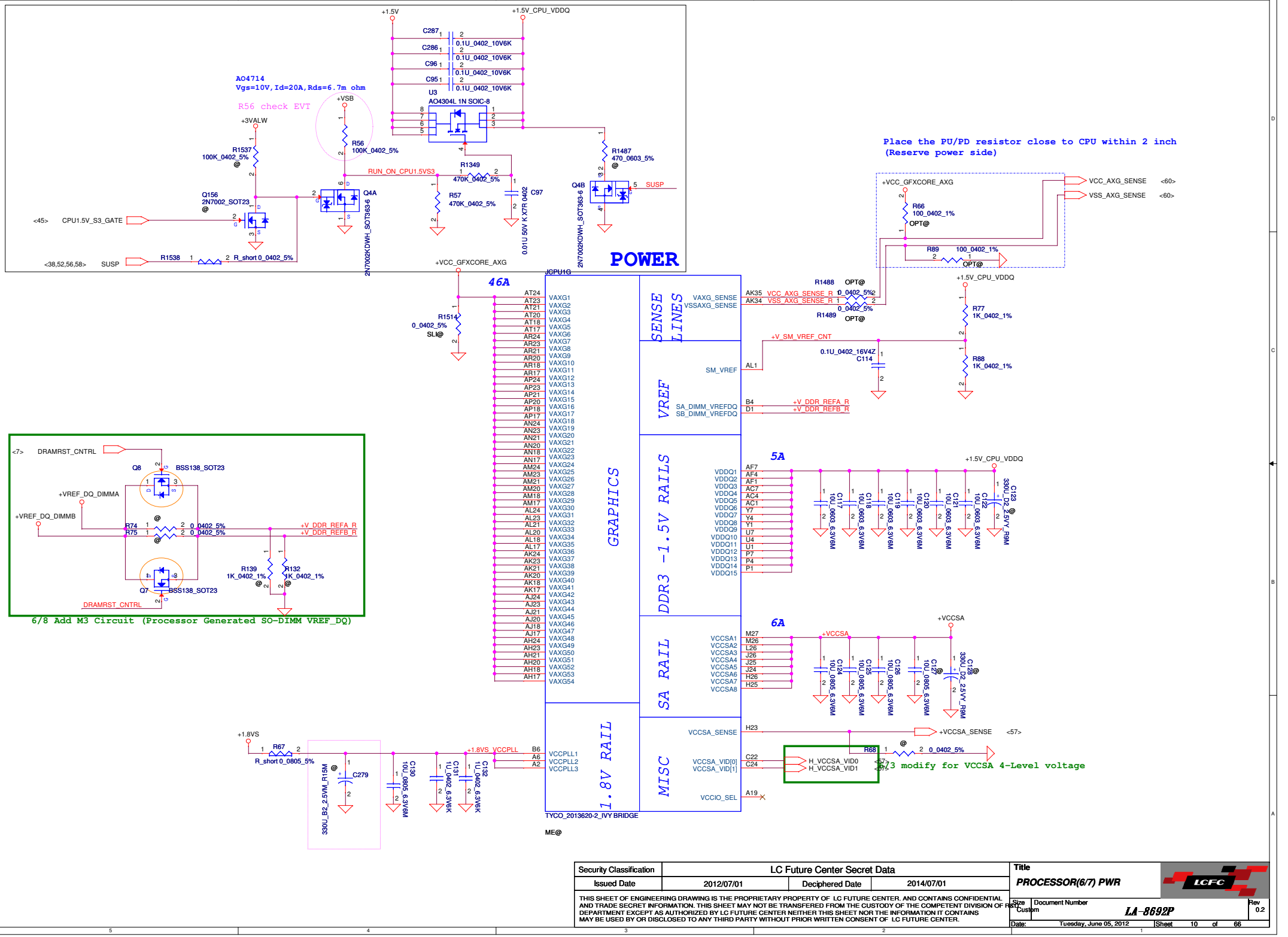

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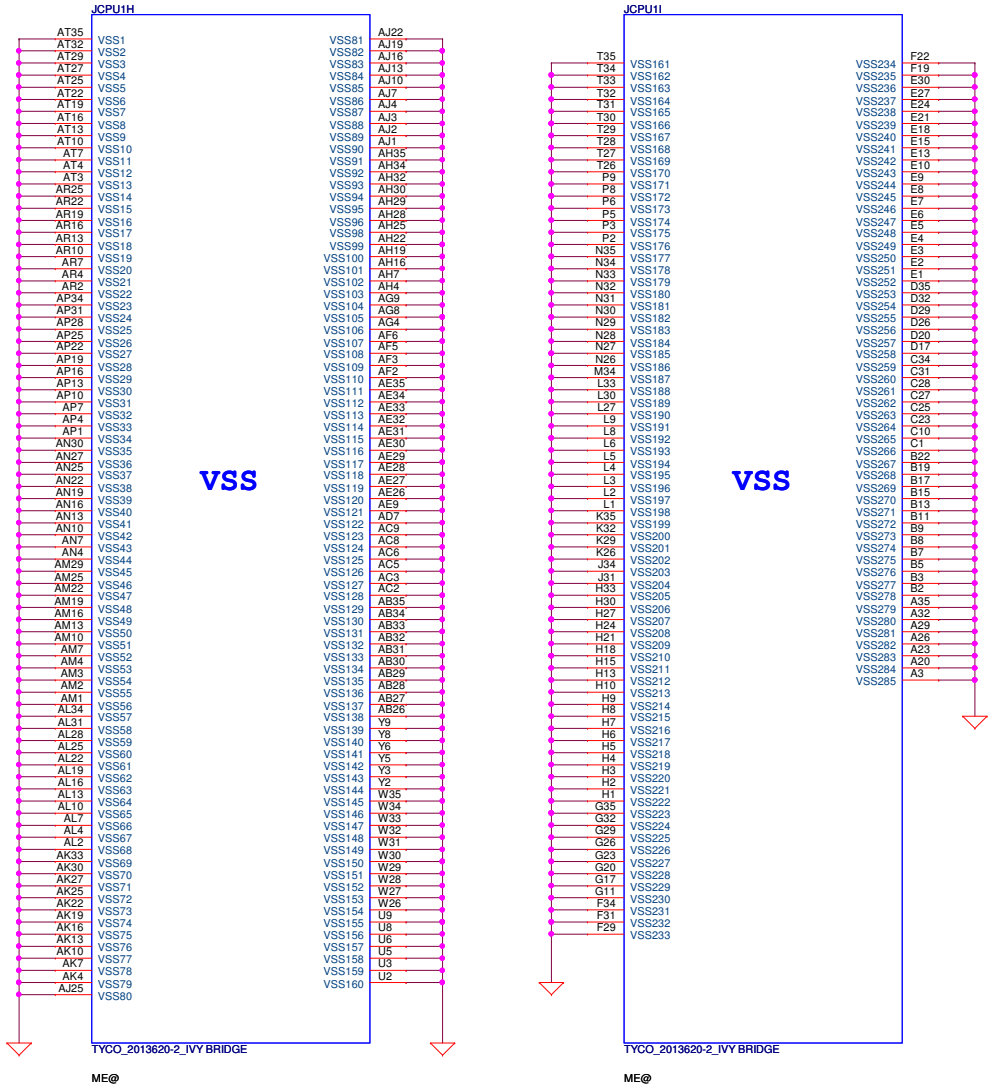

Security Classification	LC Future Center Secret Data		
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Title: **PROCESSOR(7/7) VSS**

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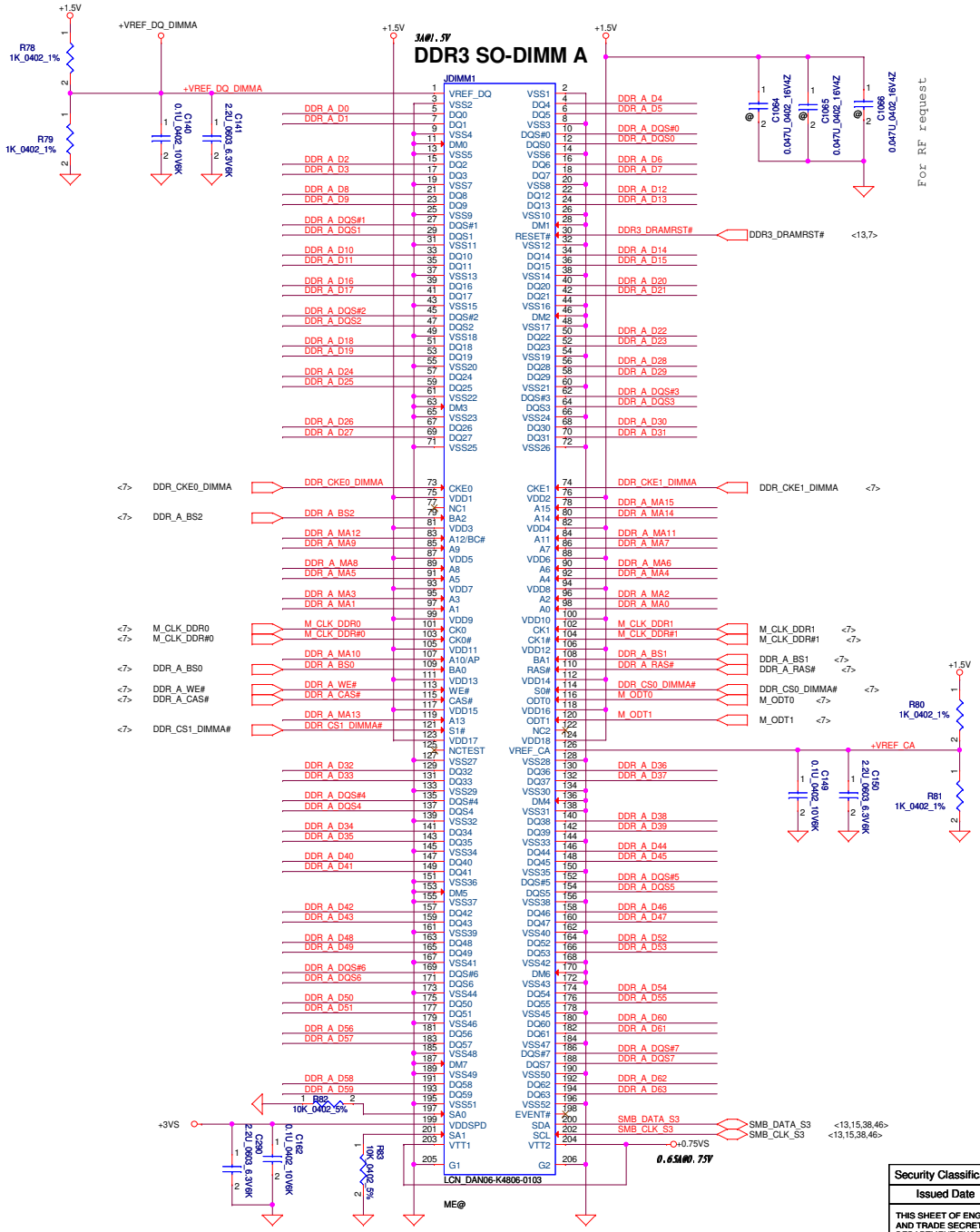
DDR3 SO-DIMM A

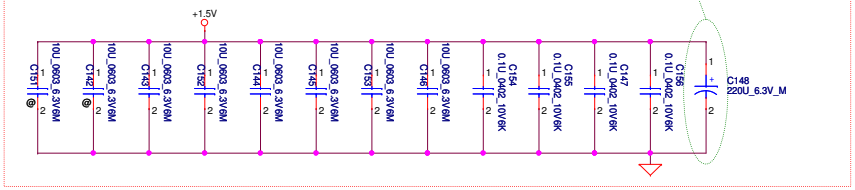
JDIMM1



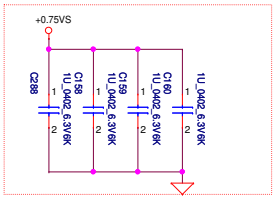
<7> DDR_A_D[0..63]
<7> DDR_A_DQS[0..7]
<7> DDR_A_DQS#[0..7]
<7> DDR_A_MA[0..15]

OSCON (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Layout Note:
Place near DIMM



Layout Note:
Place near DIMM



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Title: DDRIII-SODIMM SLOT1

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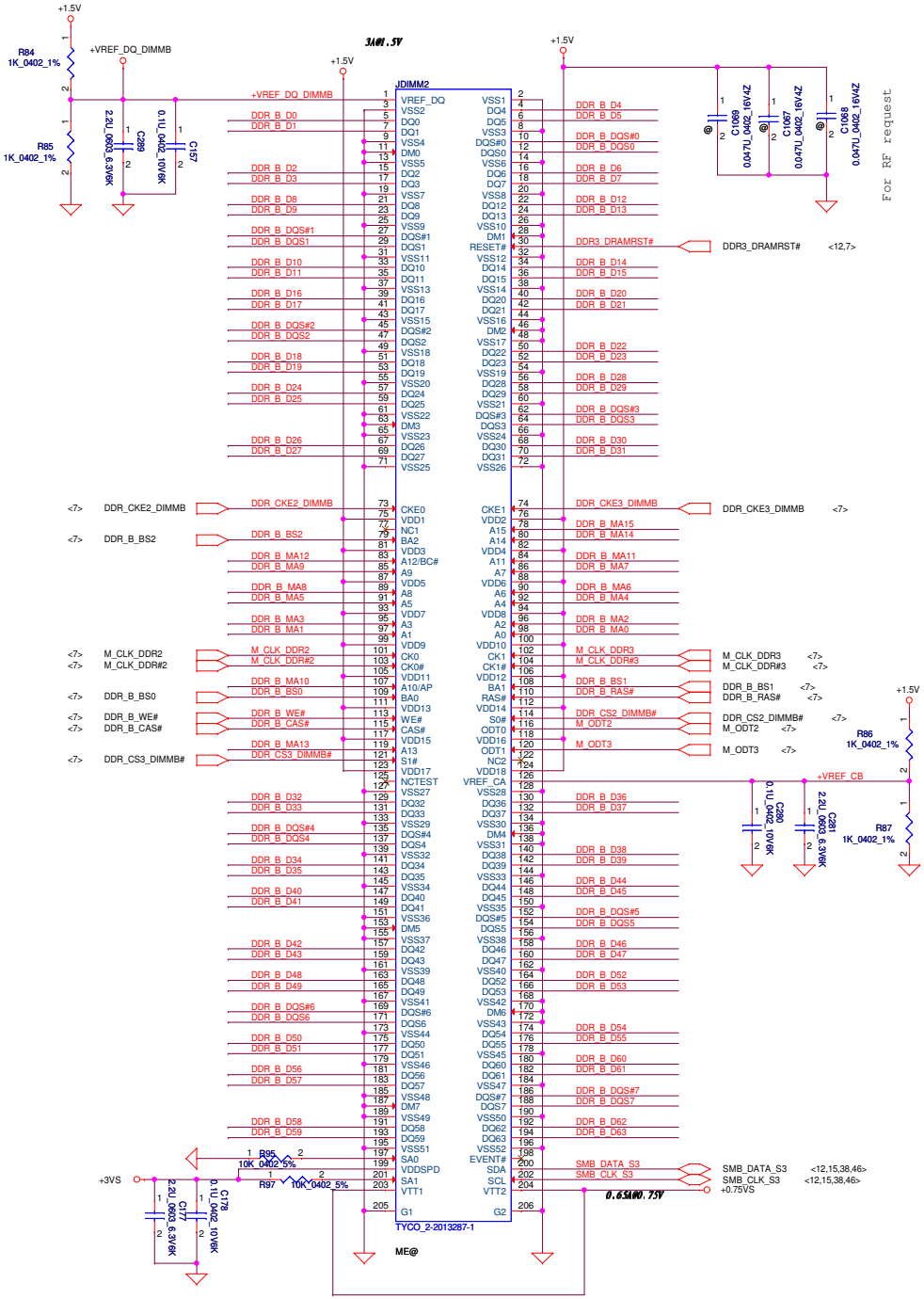

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Title: DDRIII-SODIMM SLOT2

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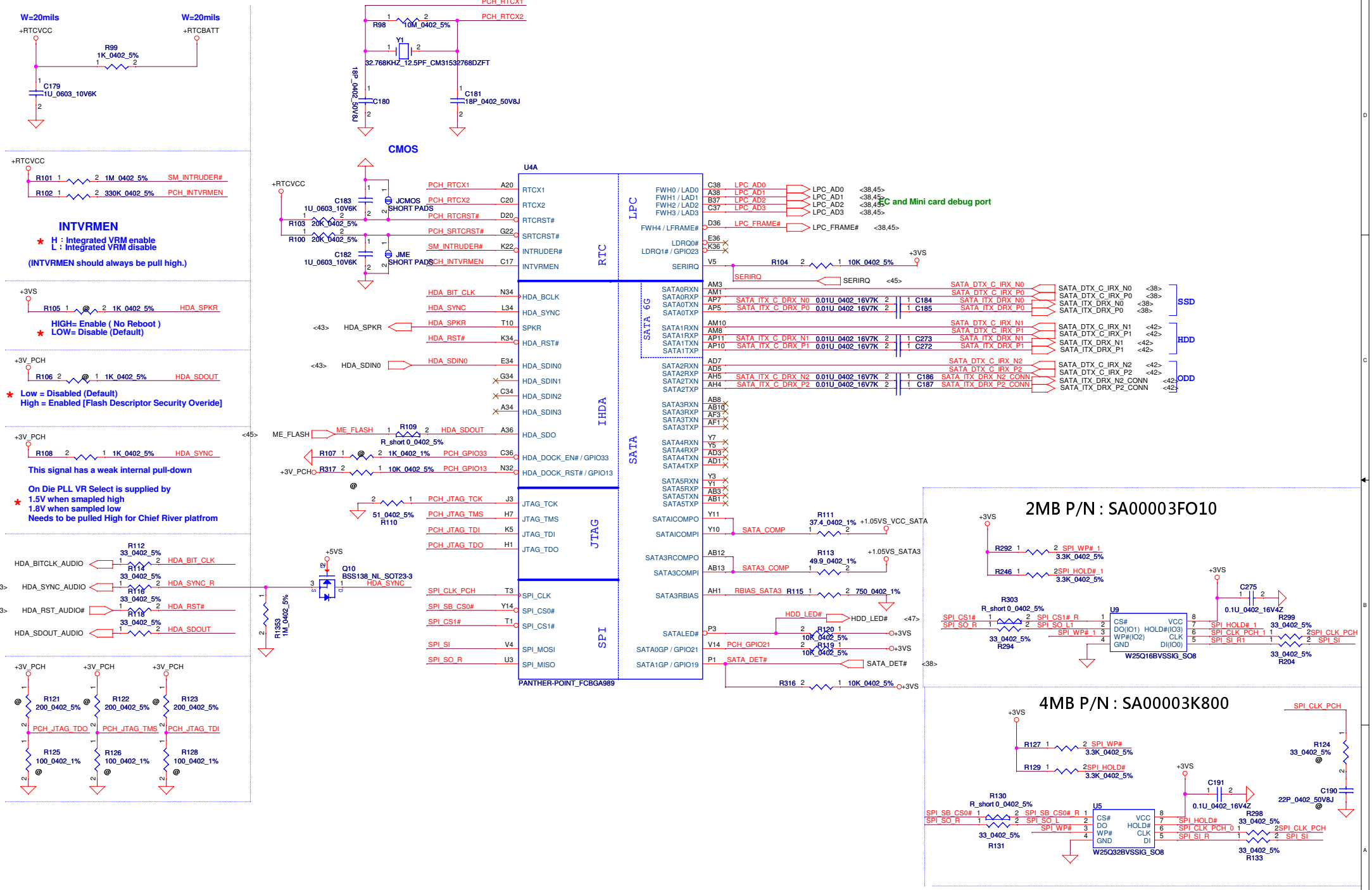

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Title	PCH (1/9) SATA,HDA,SPI, LPC, XDP		
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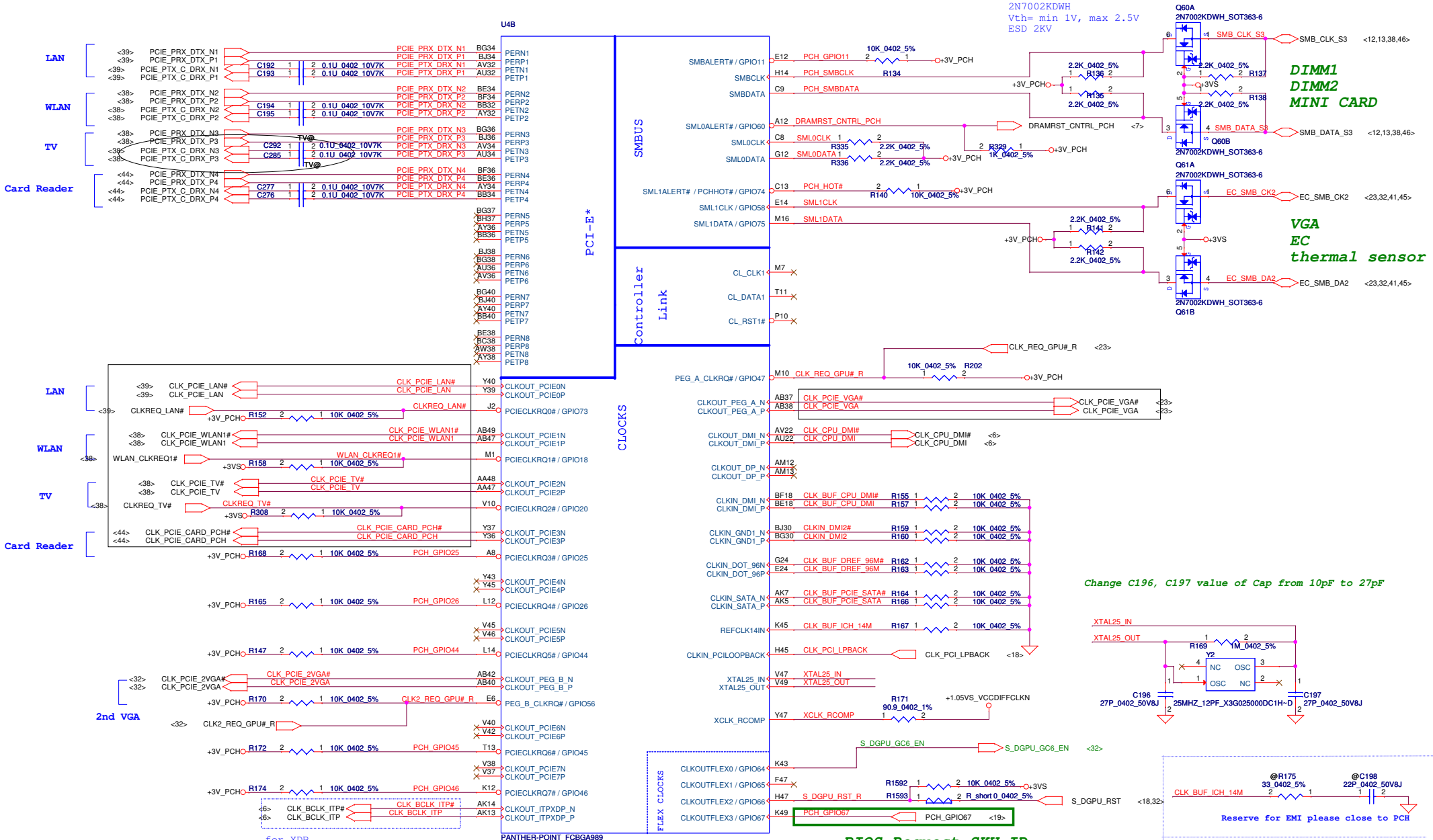
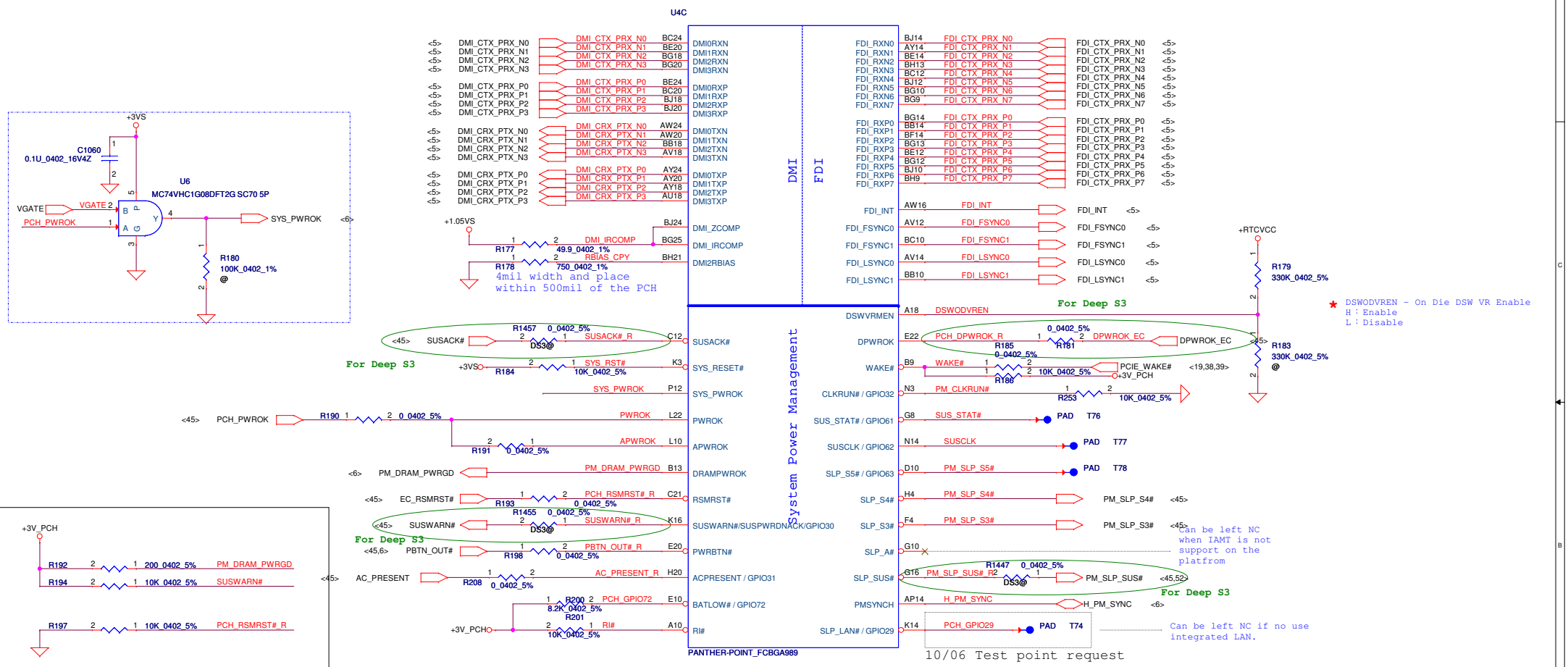


Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: PCH (2/9) PCIE, SMBUS, CLK

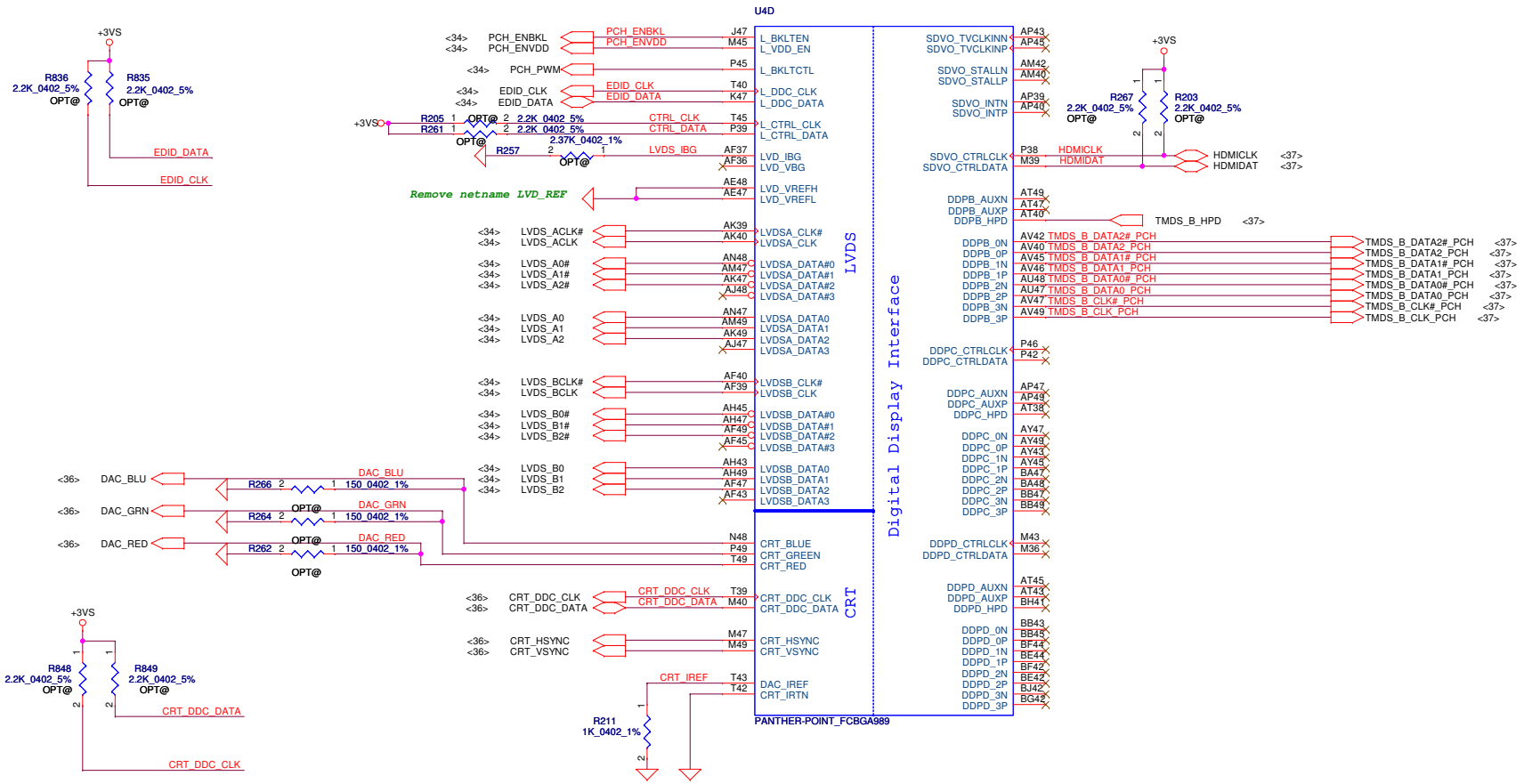
Size	Document Number	Rev
Custom	LA-8692P	0.2

Date: Tuesday, June 05, 2012 Sheet 15 of 66



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	PCH (3/9) DMI,FDI,PM,		
Size: Custom	Document Number: LA-8692P		Rev: 0.2
Date: Tuesday, June 05, 2012	Sheet 16 of 66		

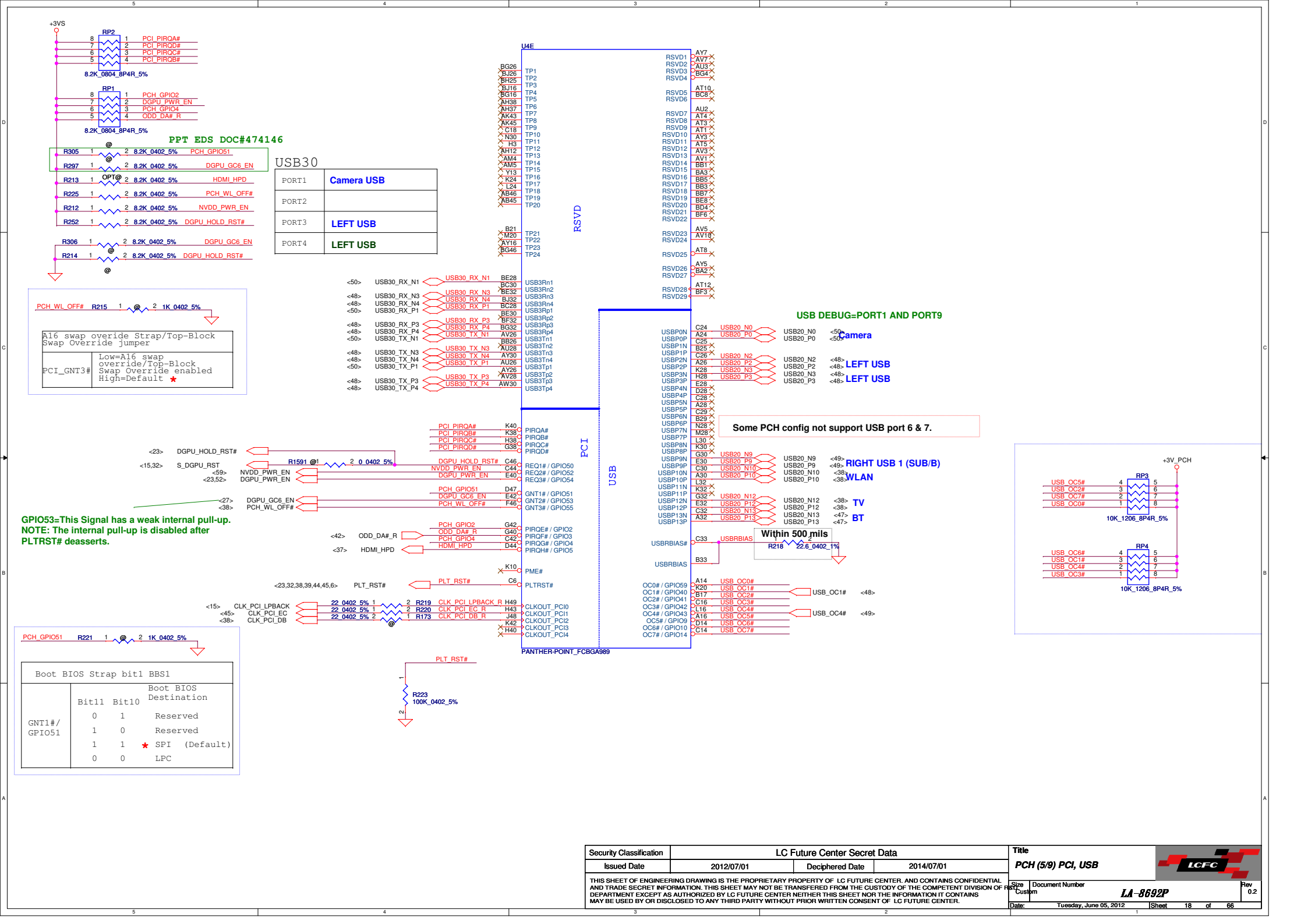


Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size	Document Number	Rev
Custom	LA-8692P	0.2

Date: Tuesday, June 05, 2012 Sheet 17 of 66



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: PCH (5/9) PCI, USB

Size: Custom	Document Number: LA-8692P	Rev: 0.2
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Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70
Optimus	0	0	X
Reserve	0	1	X
DIS (SLI)	1	0	X
Reserve	1	1	X
14"	X	X	0
15"	X	X	1

SKU ID

+3VS
R711 2.2K_0402_5% SLI@
R708 10K_0402_5% @
R704 10K_0402_5%
PCH_GPIO38
<15> PCH_GPIO67
PCH_GPIO67
PCH_GPIO70
R712 2.2K_0402_5% OPT@
R709 10K_0402_5%
R706 10K_0402_5% @

+3V_PCH
R1493 10K_0402_5% EC_SCI#
R235 10K_0402_5% EC_SMI#

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable
R240 @ 1K_0402_5% PCH_GPIO28

* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

+3VALW
R207 AOAC@ 10K_0402_5%
R245 @ 10K_0402_5% DS3_WAKE#_R

+3VS
R250 200K_0402_5% ODD_DETECT#
+3V_PCH
R251 10K_0402_5% SLAVE_PRESENT#
R259 10K_0402_5% PCH_GPIO37

<23> GC6_EVENT# GC6_EVENT#
+3VS R233 10K_0402_5%

U4F

T7	BMBUSY# / GPIO0	TACH4 / GPIO68	C40 S_DGPU_PWROK → S_DGPU_PWROK <32>
A42	TACH1 / GPIO1	TACH5 / GPIO69	B41 S_DGPU_PWR_EN → S_DGPU_PWR_EN <32,52>
H36	TACH2 / GPIO6	TACH6 / GPIO70	C41 PCH_GPIO70 — 9/18 Reseve for SKU ID
E38	TACH3 / GPIO7	TACH7 / GPIO71	A40 S_NVDD_PWR_EN → S_NVDD_PWR_EN <32>
C10	GPIO8		
C4	LAN_PHY_PWR_CTRL / GPIO12		
G2	GPIO15	A20GATE	P4 → GATEA20 <45>
U2	SATA4GP / GPIO16	PECI	AU16
D40	TACH0 / GPIO17	RCIN#	P5 KBRST# → KBRST# <45>
T5	SCLOCK / GPIO22	PROCPWRGD	AY11 → H_CPUPWRGD <6>
E8	GPIO24	THRMTRIP#	AY10 PCH_THRMTRIP#_R 1 R239 390_0402_5% 2 H_THRMTRIP# → H_THRMTRIP# <6>
E16	GPIO27	INIT3_3V#	T14 → PCH_THRMTRIP#_R <23,32>
P8	GPIO28	DF_TVS	AY1 NV_CLE
K1	STP_PCI# / GPIO34	TS_VSS1	AH8
K4	GPIO35	TS_VSS2	AK11
V8	SATA2GP / GPIO36	TS_VSS3	AH10
M5	SATA3GP / GPIO37	TS_VSS4	AK10
N2	SLOAD / GPIO38	NC_1	P37
M3	SDATAOUT0 / GPIO39		
V13	SDATAOUT1 / GPIO48	VSS_NCTF_15	BG2
V3	SATA5GP / GPIO49 / TEMP_ALERT#	VSS_NCTF_16	BG48
D6	GPIO57	VSS_NCTF_17	BH3
		VSS_NCTF_18	BH47
A4	VSS_NCTF_1	VSS_NCTF_19	BJ4
A44	VSS_NCTF_2	VSS_NCTF_20	BJ44
A45	VSS_NCTF_3	VSS_NCTF_21	BJ45
A46	VSS_NCTF_4	VSS_NCTF_22	BJ46
A5	VSS_NCTF_5	VSS_NCTF_23	BJ5
A6	VSS_NCTF_6	VSS_NCTF_24	BJ6
B3	VSS_NCTF_7	VSS_NCTF_25	C2
B47	VSS_NCTF_8	VSS_NCTF_26	C48
BD1	VSS_NCTF_9	VSS_NCTF_27	D1
BD49	VSS_NCTF_10	VSS_NCTF_28	D49
BE1	VSS_NCTF_11	VSS_NCTF_29	E1
BE49	VSS_NCTF_12	VSS_NCTF_30	E49
BF1	VSS_NCTF_13	VSS_NCTF_31	F1
BF49	VSS_NCTF_14	VSS_NCTF_32	F49

GPIO | CPU/MISC | NCTF

PANTHER-POINT_FCBGA989

<38> PCH_BT_DISABLE# R238 10K_0402_5% PCH_BT_DISABLE# T5
<42> ODD_EN ODD_EN E8
<16,38,39> PCIE_WAKE# 0_0402_5% R224 DS3_WAKE#_R E16
R241 10K_0402_5% PCH_GPIO28 P8
<38,47> PCH_BT_ON# R242 10K_0402_5% PCH_BT_ON# K1
R243 10K_0402_5% PCH_GPIO35 K4
<42> ODD_DETECT# ODD_DETECT# V8
PCH_GPIO37 M5
PCH_GPIO38 N2
R247 10K_0402_5% PCH_GPIO39 M3
R248 10K_0402_5% PCH_GPIO48 V13
R249 10K_0402_5% PCH_GPIO49 V3
<32> SLAVE_PRESENT# SLAVE_PRESENT# D6

<27,56,59> DGPU_PWROK DGPU_PWROK D40

<45> EC_LID_OUT# EC_LID_OUT# G2
<32> S_Toggle_REQ#
R231 10K_0402_5%
R232 @ 10K_0402_1%

<45> EC_SCI# EC_SCI# E38
<45> EC_SMI# EC_SMI# C10
+3V_PCH R229 @ 10K_0402_5% PCH_GPIO12 C4
R230 10K_0402_5% EC_LID_OUT#

S_DGPU_PWR_EN R1589 10K_0402_5% +3VS
S_NVDD_PWR_EN R1590 10K_0402_5%

R236 10K_0402_5% +3VS

INIT3_3V
This signal has weak internal PU, can't pull low

Intel schematic reviwe recommand.

S_DGPU_PWROK R255 10K_0402_5% +3VS
KBRST# R226 10K_0402_5%
PCH_THRMTRIP#_R R244 10K_0402_5%

PROC_SEL	H : Sandy Bridge
	L : Ivy Bridge

+1.8VS
R216 2.2K_0402_5%
NV_CLE R217 1K_0402_5% H_SNB_IVB# <6>
CLOSE TO THE BRANCHING POINT

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: PCH (6/9) GPIO, CPU, MISC

Size	Document Number	Rev
Custom	LA-8692P	0.2

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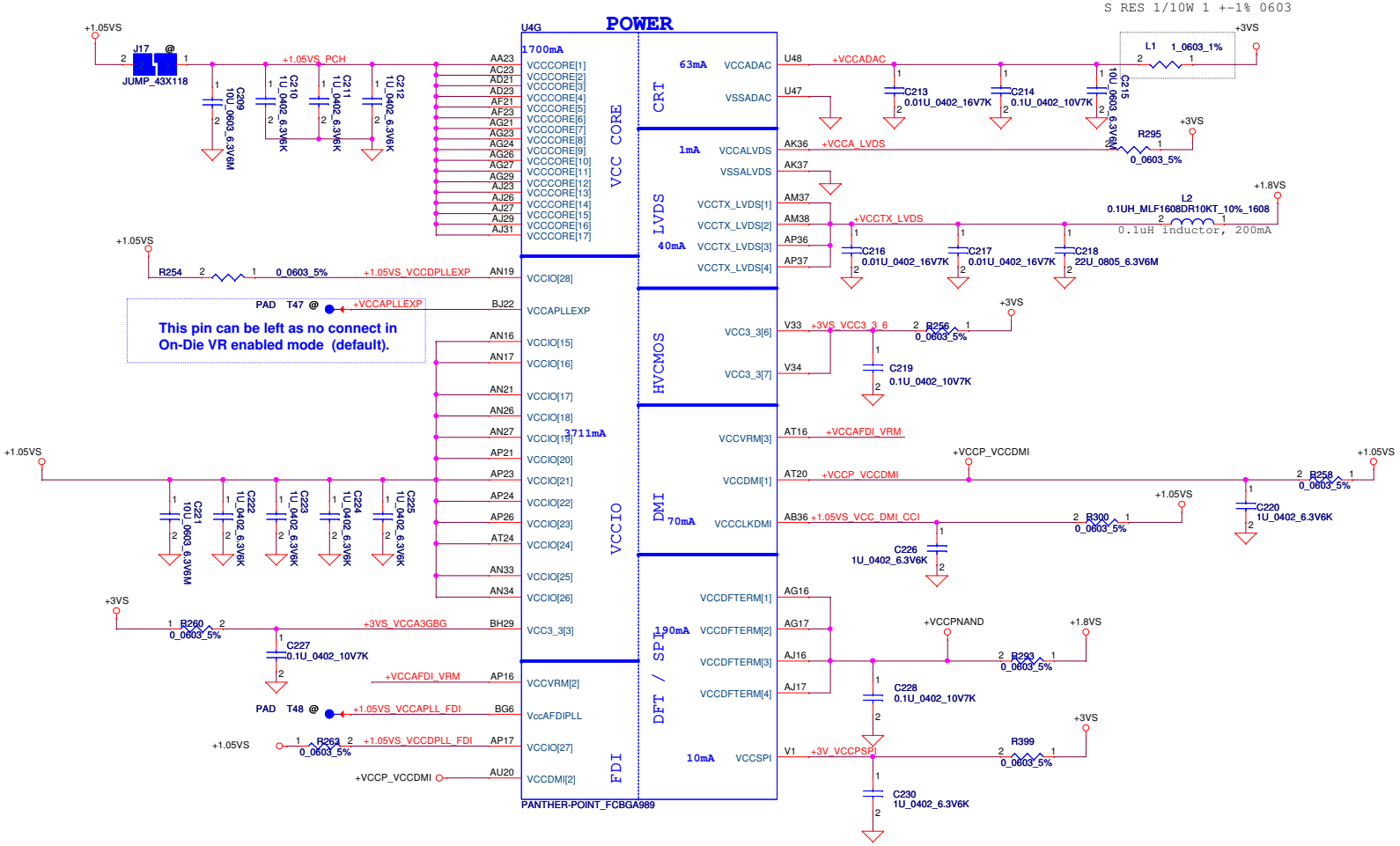

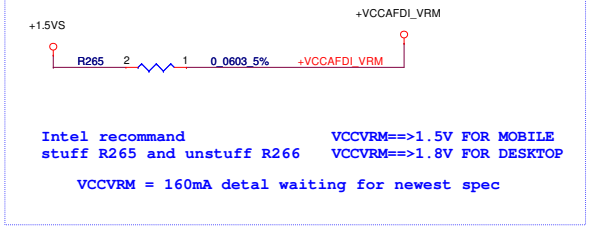

PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.05	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: PCH (7/9) PWR

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Have internal VRM

VCC3_3 = 266mA detal waiting for newest spec

VCCDMI = 42mA detal waiting for newest spec

POWER

U4J

+3VS

R280 0_0603_5% — +3VS_VCC_CLKF33 — C231 10U_0805_10V4Z — C232 1U_0402_6.3V6K

On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2 , VCCAPLLSATA

+3VALW — R269 0_0603_5% — +VCCPDSW — C234 0.1U_0402_10V7K

+3VS_VCC_CLKF33

+1.05VS — R271 0_0603_5% — +VCCDPLL_CPY

+VCCSUS1 — @C239 1U_0402_6.3V6K

+1.05VS — R277 0_0805_5% — +1.05VM_VCCASW — C241 22U_0805_6.3V6M — C242 22U_0805_6.3V6M — C244 1U_0402_6.3V6K — C245 1U_0402_6.3V6K — C246 1U_0402_6.3V6K

+1.05VS — L5 BLM18PG181SN1D_0603 — +1.05VS_VCCA_DPL

L6 BLM18PG181SN1D_0603 — +1.05VS_VCCA_B_DPL — C250 22U_0805_6.3V6M — C251 1U_0402_6.3V6K — C252 22U_0805_6.3V6M — C253 1U_0402_6.3V6K

Before gerber out change to 22u_0805

C258 0.1U_0402_10V7K — +VCCRTCEXT — +VCCAFDI_VRM

+1.05VS — R274 0_0603_5% — C256 1U_0402_6.3V6K — +1.05VS_VCCA_A_DPL

+1.05VS_VCCDIFFCLKN — +1.05VS — R304 0_0603_5% — C259 1U_0402_6.3V6K — +1.05VS_VCCDIFFCLKN

+1.05VS_SSCVCC

+1.05VS — R284 0_0603_5% — C262 1U_0402_6.3V6K — +VCCSST

C263 0.1U_0402_10V7K

+1.05VS — R286 0_0603_5% — +V_CPU_IO

+RTCVCC — C265 4.7U_0603_6.3V6K — C266 0.1U_0402_10V7K — C267 0.1U_0402_10V7K@ — C268 1U_0402_6.3V6K — C269 0.1U_0402_10V7K — C270 0.1U_0402_10V7K@

U4J

AD49	VCCACLK		
T16	VCCDSW3_3	1mA	
V12	DCPSUSBYP		
T38	VCC3_3[5]		
BH23	VCCAPLLDMI2		
AL29	VCCIO[14]		
AL24	DCPSUS[3]		
AA19	VCCASW[1]		
AA21	VCCASW[2]	903mA	Clock and Miscellaneous
AA24	VCCASW[3]		
AA26	VCCASW[4]		
AA27	VCCASW[5]		
AA29	VCCASW[6]		
AA31	VCCASW[7]		
AC26	VCCASW[8]		
AC27	VCCASW[9]		
AC29	VCCASW[10]		
AC31	VCCASW[11]		
AD29	VCCASW[12]		
AD31	VCCASW[13]		
W21	VCCASW[14]		
W23	VCCASW[15]		
W24	VCCASW[16]		
W26	VCCASW[17]		
W29	VCCASW[18]		
W31	VCCASW[19]		
W33	VCCASW[20]		
N16	DCPRTC		
Y49	VCCVRM[4]		
BD47	VCCADPLLA	80mA	
BF47	VCCADPLLB	80mA	
AF17	VCCIO[7]		
AF33	VCCDIFFCLKN[1]	52mA	
AF34	VCCDIFFCLKN[2]		
AG34	VCCDIFFCLKN[3]		
AG33	VCCSSC	95mA	
V16	DCPSST		
T17	DCPSUS[1]		
V19	DCPSUS[2]		
BJ8	V_PROC_IO	1mA	CPU
A22	VCCRTC		RTC
N26	VCCIO[29]		USB
P26	VCCIO[30]		
P28	VCCIO[31]		
T27	VCCIO[32]		
T29	VCCIO[33]		
T23	VCCSUS3_3[7]	228mA	
T24	VCCSUS3_3[8]		
V23	VCCSUS3_3[9]		
V24	VCCSUS3_3[10]		
P24	VCCSUS3_3[6]		
T26	VCCIO[34]		
M26	V5REF_SUS	1mA	
AN23	DCPSUS[4]		
AN24	VCCSUS3_3[1]		
P34	V5REF	1mA	PCI/GPIO/LPC
N20	VCCSUS3_3[2]		
N22	VCCSUS3_3[3]		
P20	VCCSUS3_3[4]		
P22	VCCSUS3_3[5]		
AA16	VCC3_3[1]		
W16	VCC3_3[8]		
T34	VCC3_3[4]		
AJ2	VCC3_3[2]		SATA
AF13	VCCIO[5]		
AH13	VCCIO[12]		
AH14	VCCIO[13]		
AF14	VCCIO[6]		
AK1	VCCAPLLSATA		
AF11	VCCVRM[1]		
AC16	VCCIO[2]		
AC17	VCCIO[3]		
AD17	VCCIO[4]		
T21	VCCASW[22]		MISC
V21	VCCASW[23]		
T19	VCCASW[21]		
P32	VCCSUSHDA	10mA	SUSHDA

+1.05VS — R270 0_0603_5% — +1.05VS_VCCUSBCORE — C233 1U_0402_6.3V6K

+3V_PCH — R272 0_0603_5% — +3V_VCCPUSB — C236 0.1U_0402_10V7K

+3V_PCH — R273 0_0603_5% — +3V_VCCAUBG — C238 0.1U_0402_10V7K

+1.05VS — R276 0_0603_5% — +1.05VS_VCCAUPLL

+PCH_V5REF_SUS

C243 @ 1U_0402_6.3V6K — +VCCA_USBSUS

+3V_VCCPSUS

+PCH_V5REF_RUN

+3V_PCH — R278 0_0603_5% — C247 1U_0402_6.3V

+3VS — R281 0_0603_5% — C249 0.1U_0402_10V7K — +3VS_VCCPCORE

+3VS — R282 0_0603_5% — C254 0.1U_0402_10V7K — +3VS_VCCPPCI

+3VS — R283 0_0603_5% — C255 0.1U_0402_10V7K — +VCC3_3_2

+1.05VS_SATA3 — R285 0_0603_5% — C257 1U_0402_6.3V6K

+1.05VS_VCC_SATA — R288 0_0603_5% — C261 1U_0402_6.3V6K

+VCCAFDI_VRM

+1.05VS — C271 0.1U_0402_16V4Z — +VCCSUSHDA — R287 0_0603_5% — +3V_PCH

+5V_PCH — R275 10_0402_5% — +3V_PCH — D1 CH751H-40PT_SOD323-2 — +PCH_V5REF_SUS — C240 0.1U_0603_25V7K

+5VS — R279 10_0402_5% — +3VS — D2 CH751H-40PT_SOD323-2 — +PCH_V5REF_RUN — C248 1U_0603_10V6K

On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2 , VCCAPLLSATA

PANTHER-POINT_FCBGA989

Title	PCH (8/9) PWR		
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Custom	LA-8692P		0.2
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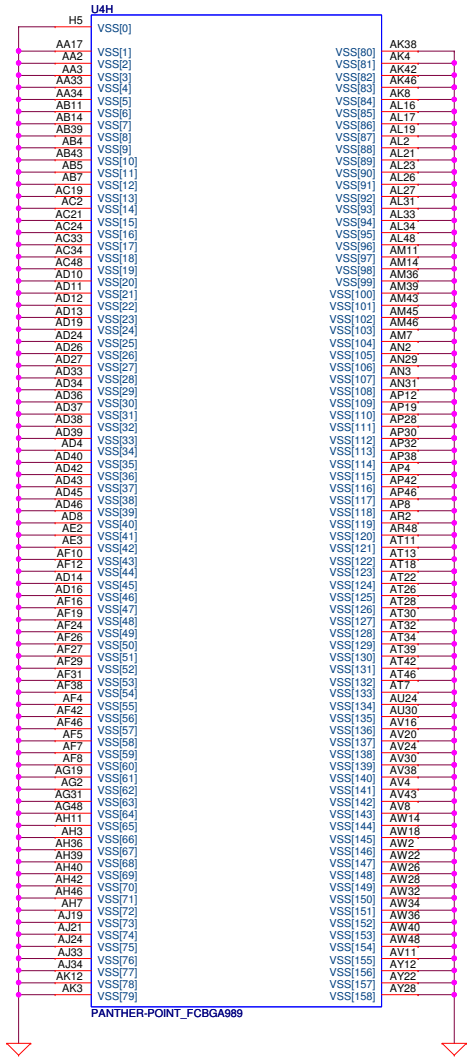

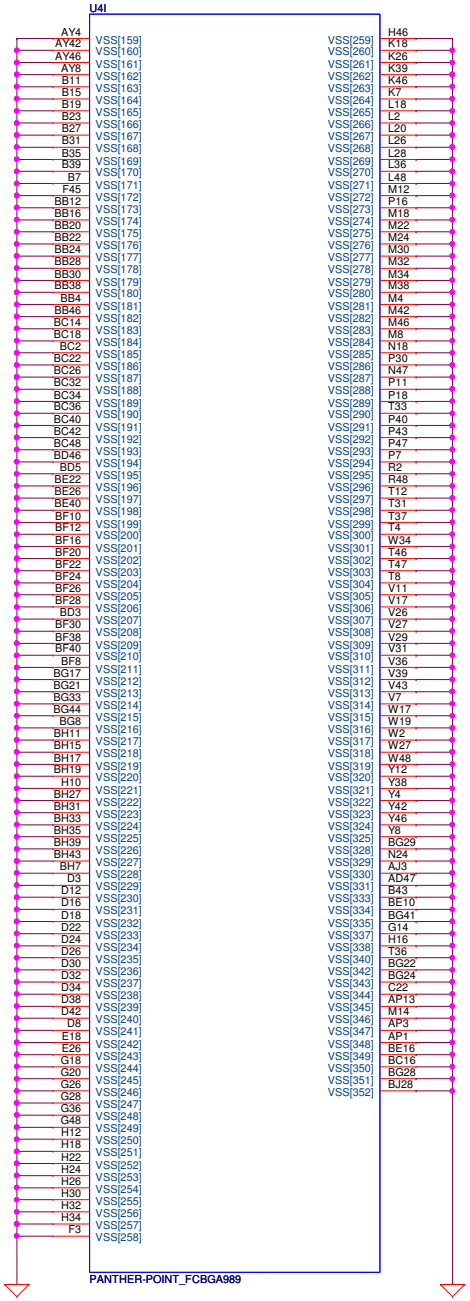

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: PCH (9/9) VSS

Size	Document Number	Rev
Custom	LA-8692P	0.2

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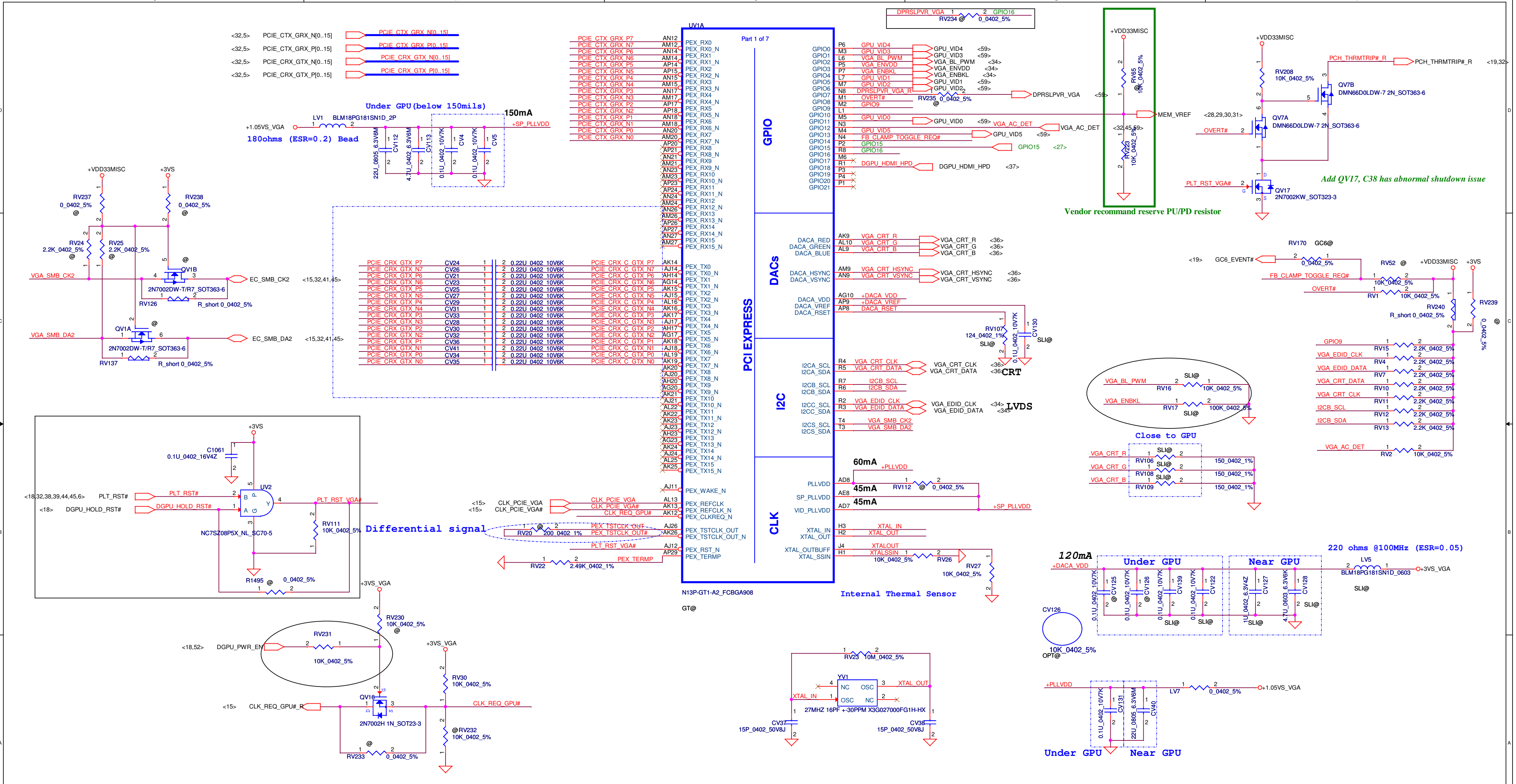
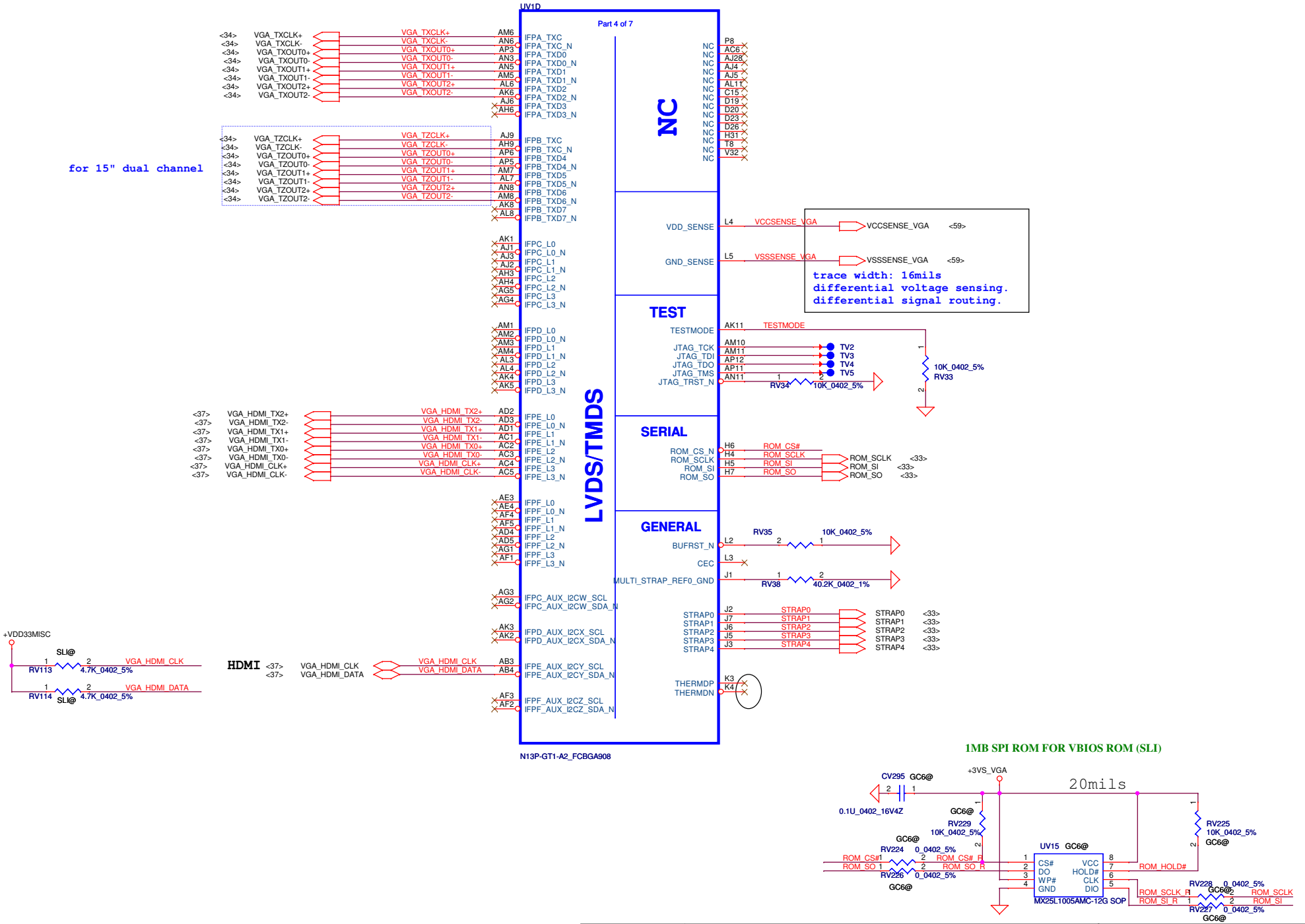


Security Classification	LC Future Center Secret Data		Title
Issued Date	2012/07/01	Deciphered Date 2014/07/01	N13P-PCIE/DAC/GPIO

Size: Custom | Document Number: LA-8692P | Rev 0.2

Date: Tuesday, June 05, 2012 |

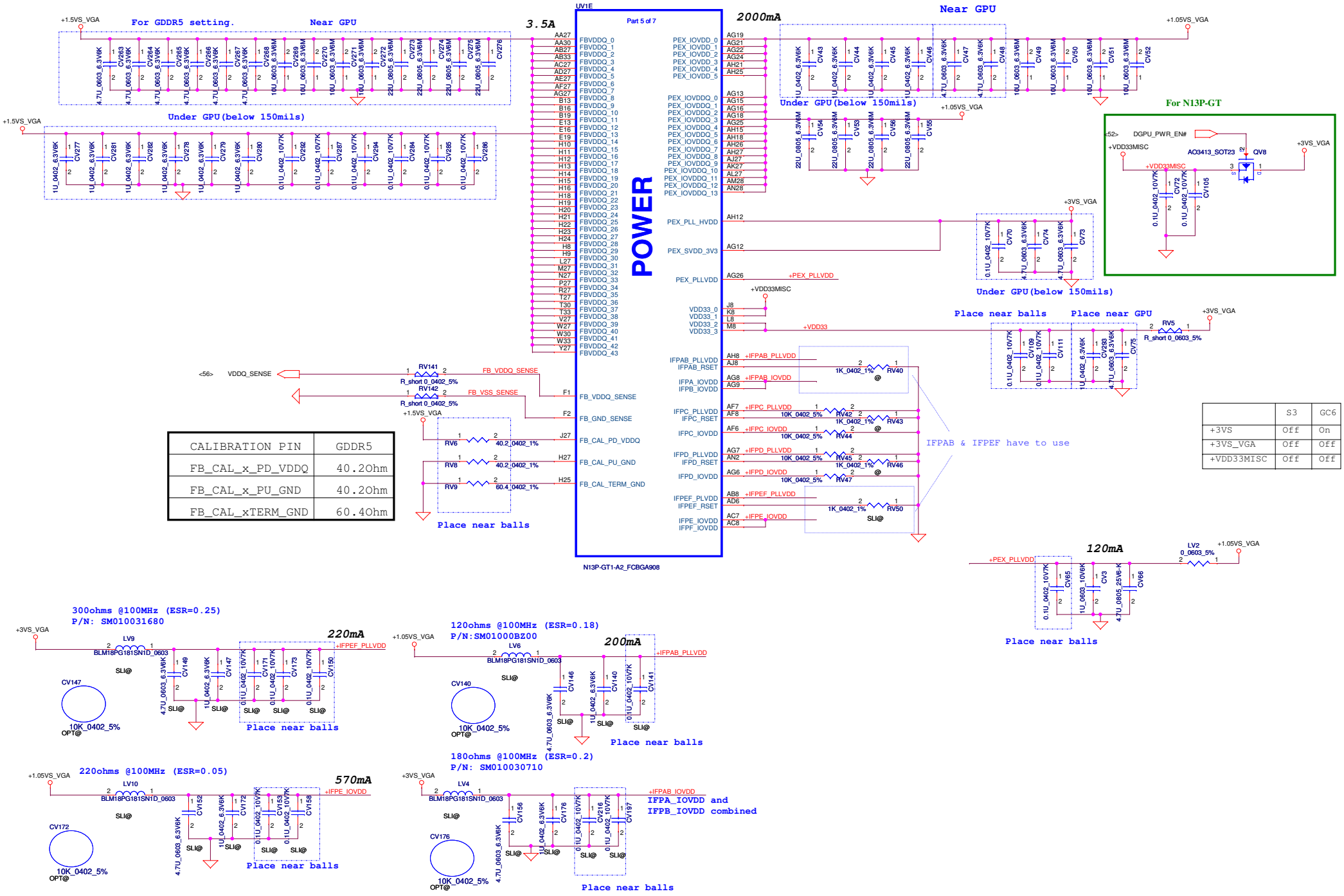


Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: N13P-LVDS/HDMI/DP/THM

Size: Custom | Document Number: LA-8692P | Rev: 0.2

Date: Tuesday, June 05, 2012 | Sheet 24 of 66



CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm

	S3	GC6
+3VS	Off	On
+3VS_VGA	Off	Off
+VDD33MISC	Off	Off

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: N13P-POWER

Size: Custom | Document Number: LA-8682P | Rev: 0.2

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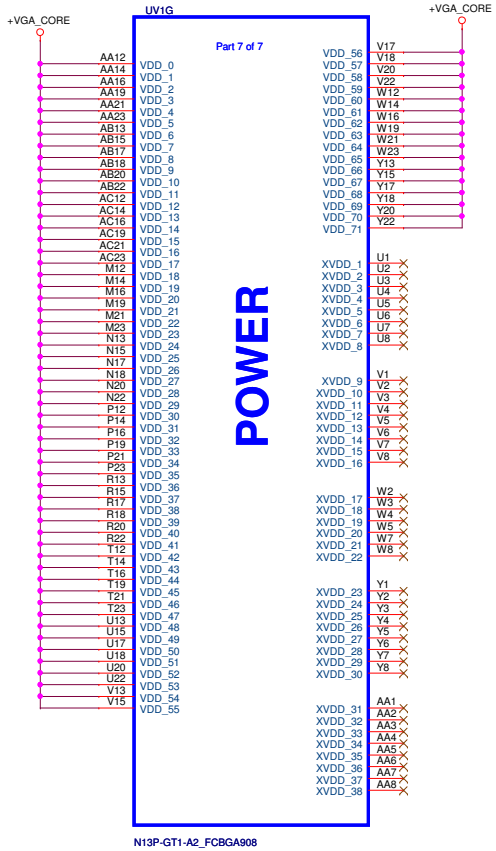

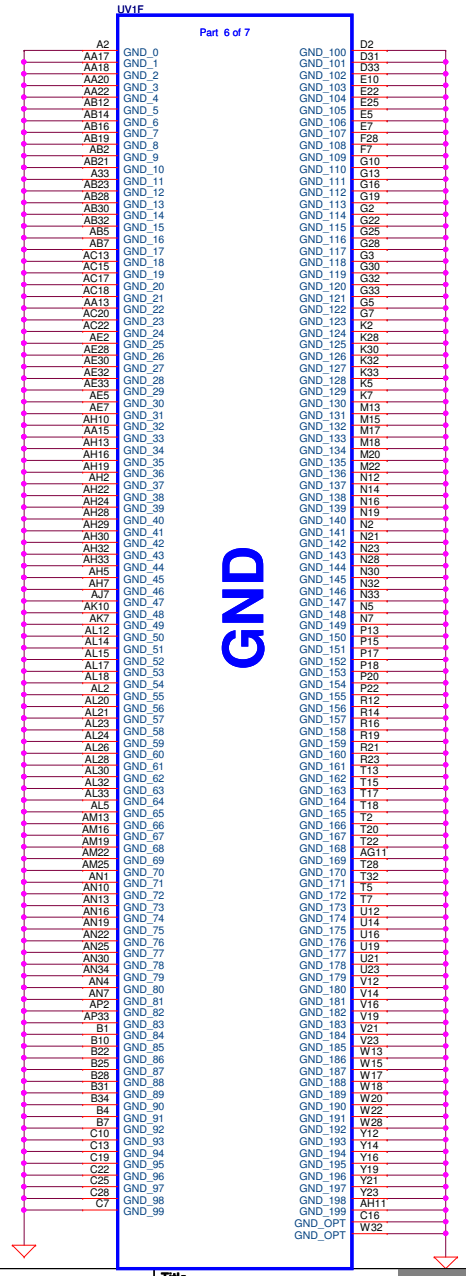

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: N13P-VGA CORE, GND

Size: Custom	Document Number: LA-8692P	Rev: 0.2
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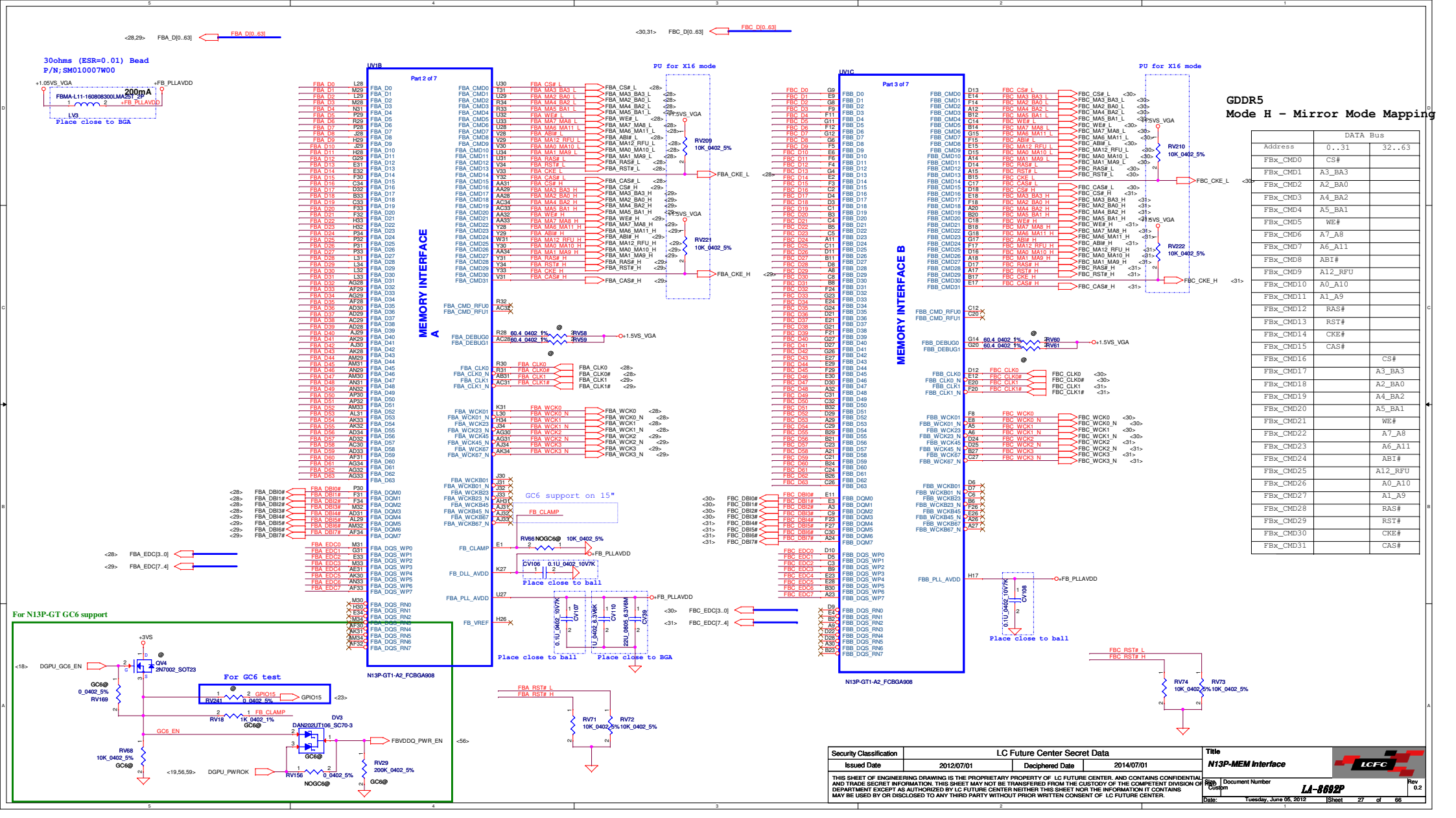

Security Classification	LC Future Center Secret Data
Issued Date	2012/07/01
Deciphered Date	2014/07/01

Title: N13P-MEM Interface

Size: Custom | Document Number: LA-8692P | Rev: 0.2

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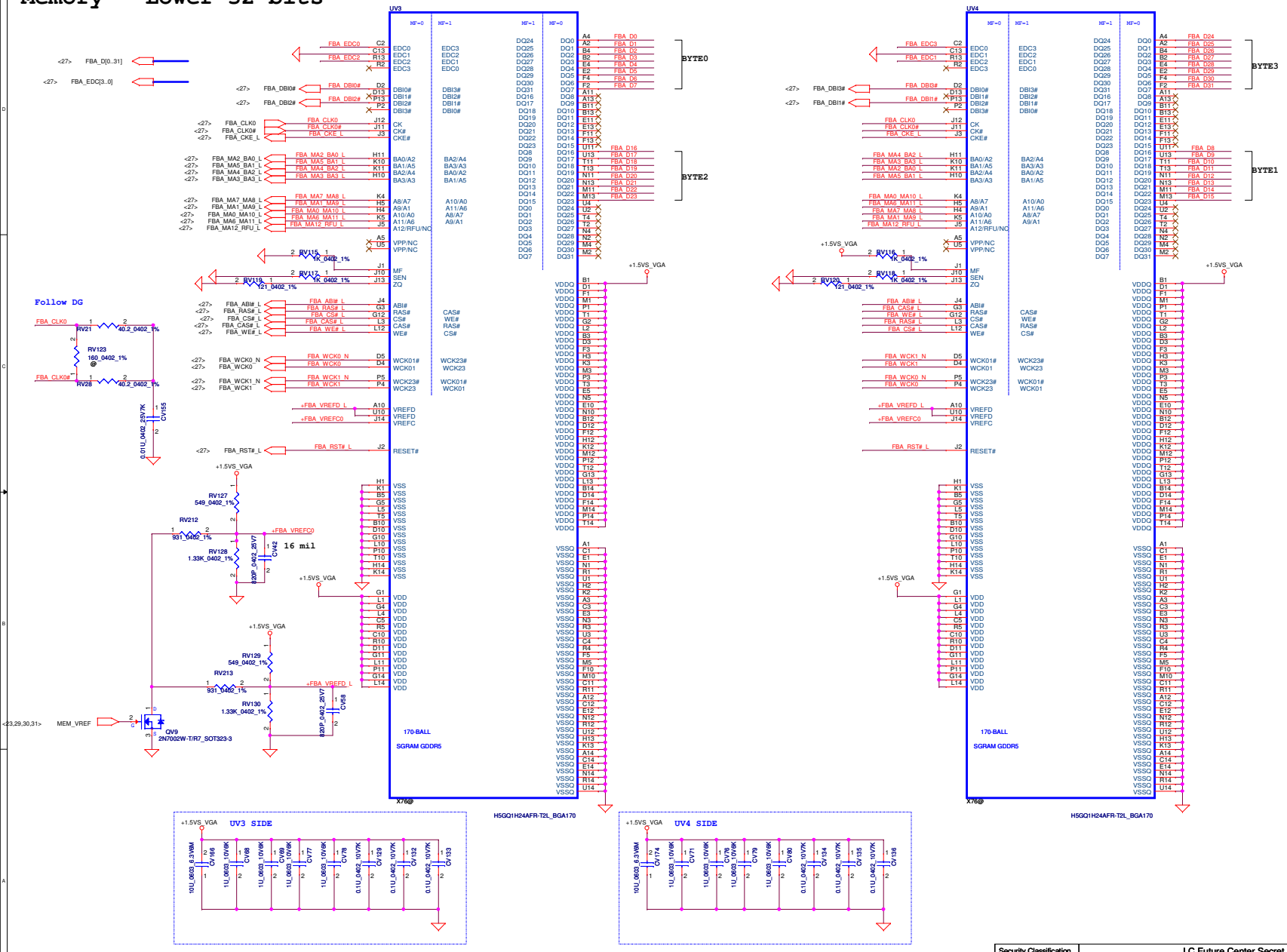
Memory - Lower 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Title: N13P-VRAM A Lower

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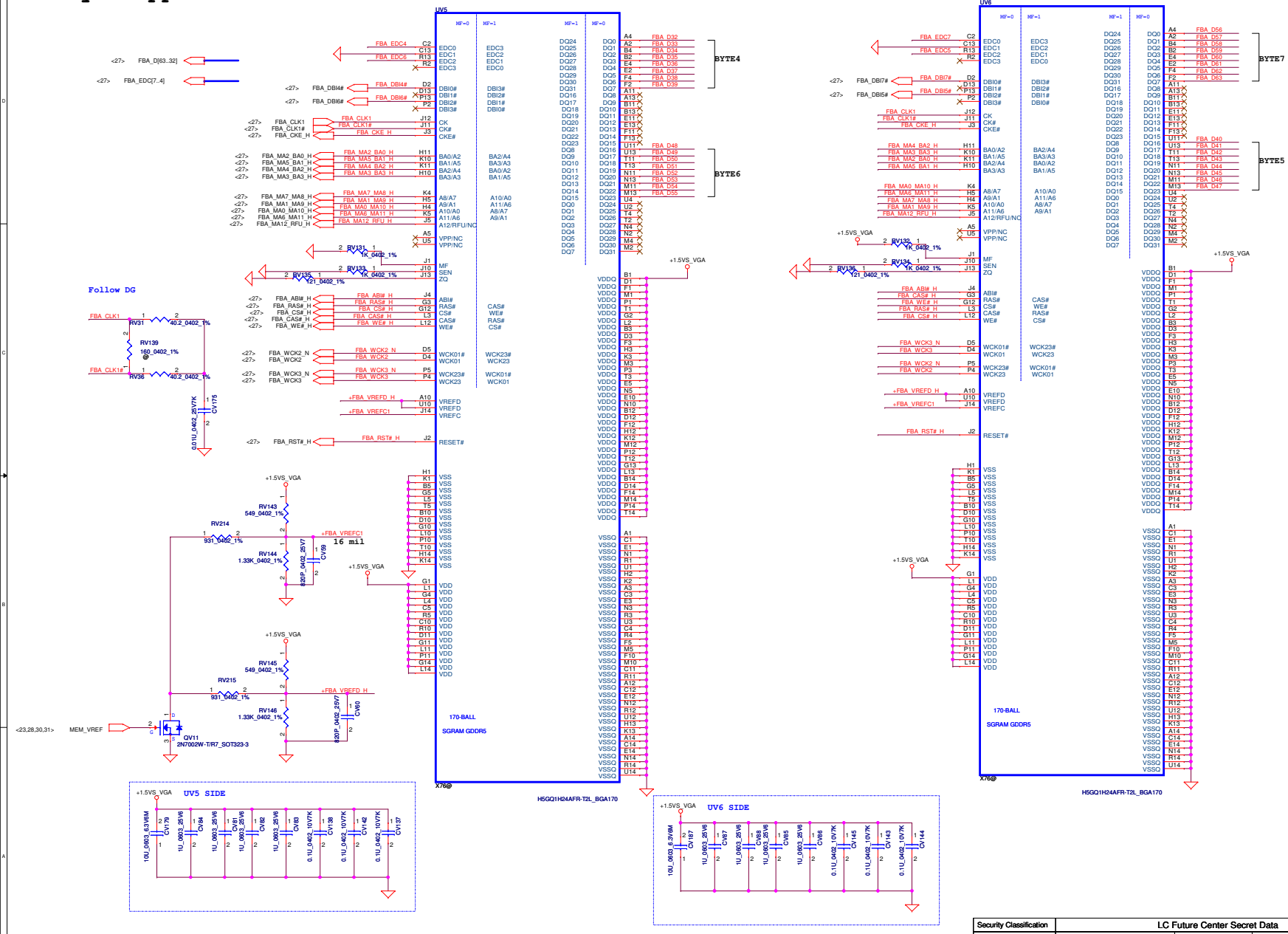
Memory - Upper 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Title: N13P-VRAM A Upper

Size: Custom | Document Number: LA-8652P | Rev: 0.2

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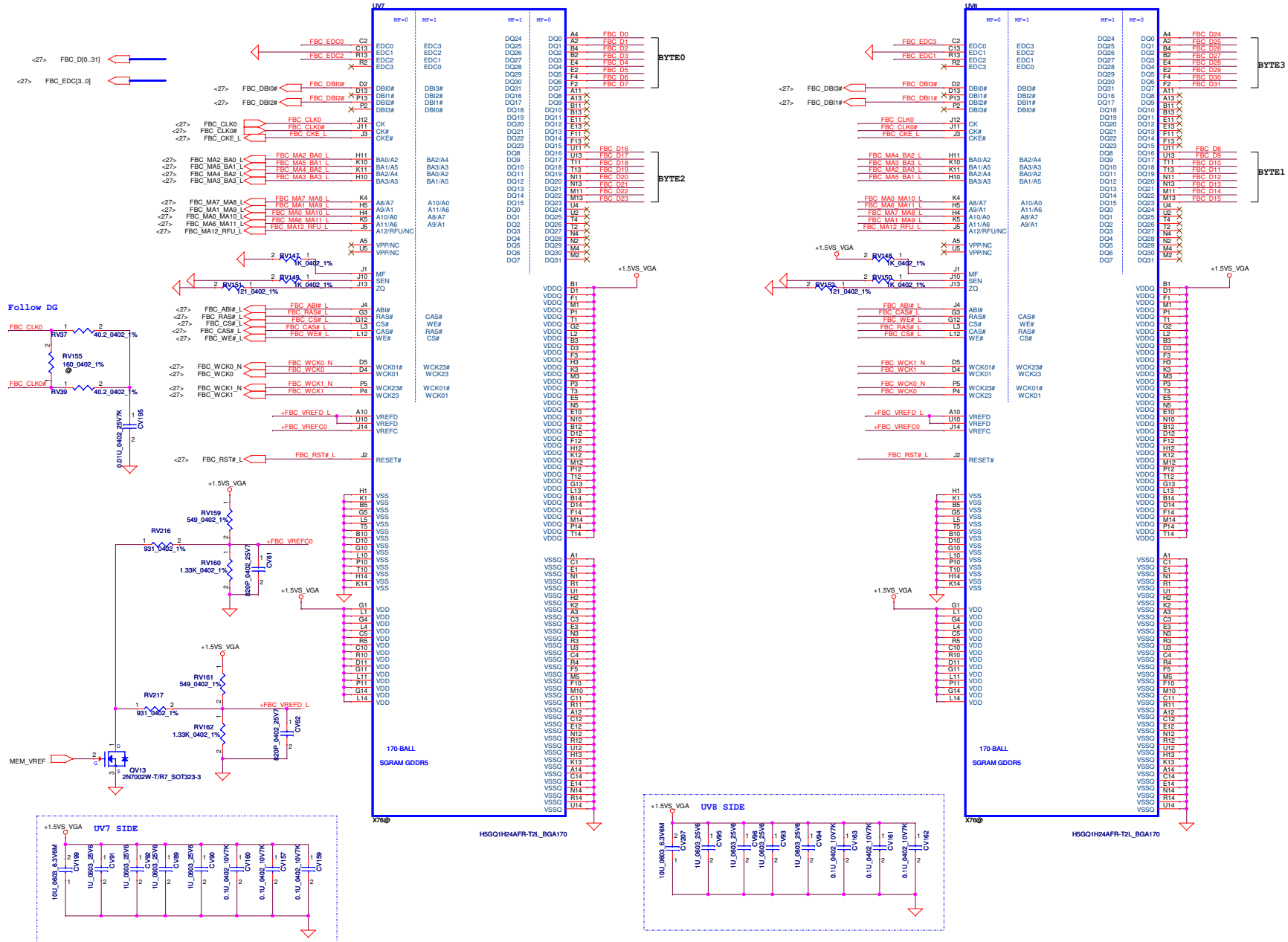
Memory Partition C – Lower 32 bits

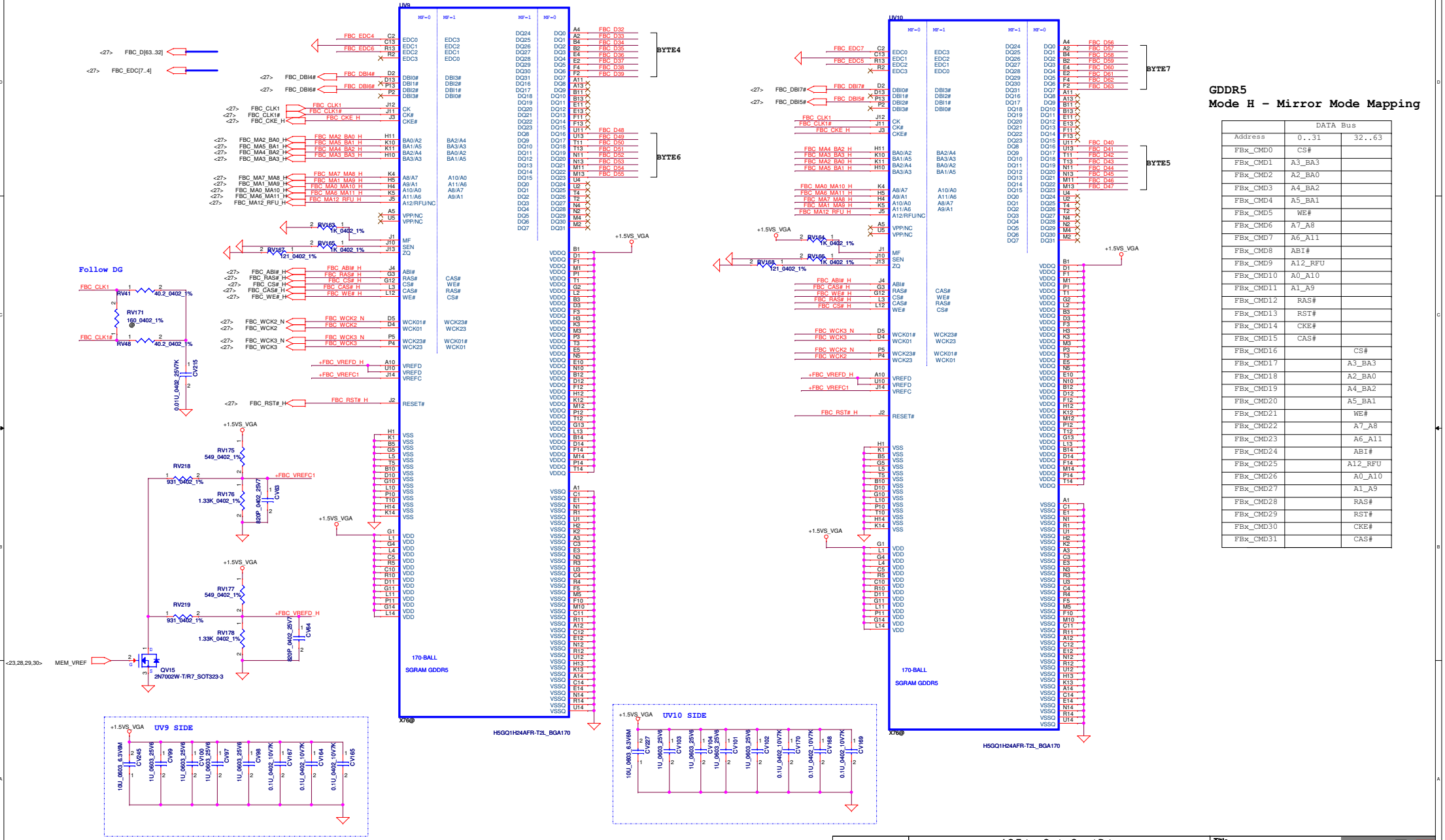


GDDR5
Mode H – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Title		
N12P-VRAM C Lower		
Size: Custom	Document Number: LA-8692P	Rev: 0.2
Date: Tuesday, June 05, 2012	Sheet 30 of 66	

Memory Partition C – Upper 32 bits



GDDR5
Mode H – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: N12P-VRAM C Upper

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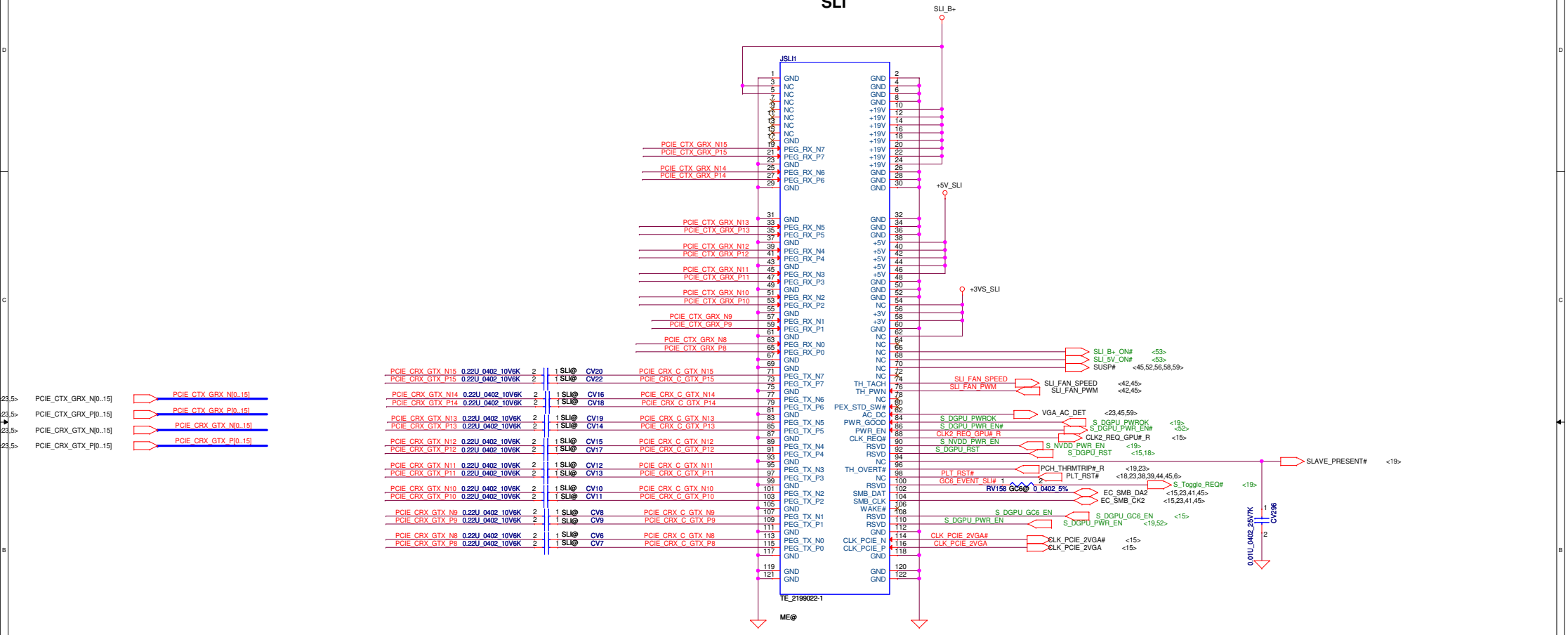
SLI



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	DDRIII-SODIMM SLOT1		
Size	Document Number		Rev
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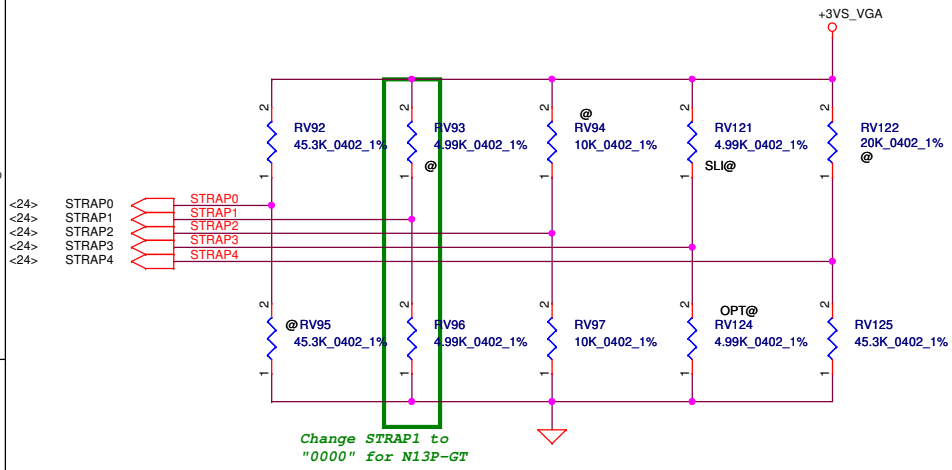

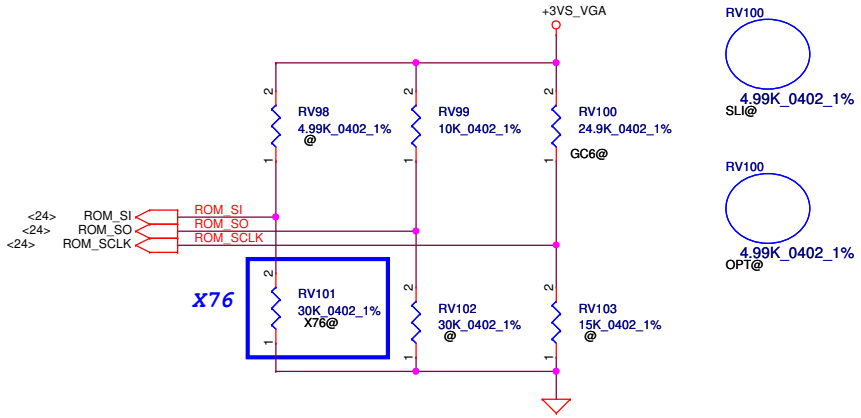

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

X76

GPU	FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	Samsung	K4G20325FD-FC04 2G	PD 30K	PU 10K	PU 25K GC6@	PU 45K	PD 5K	PD 10K	PU 5K SLI@	PD 45K	64Mx32
		K4G10325FG-HC04 1G	PD 45K								32Mx32
	Hynix	H5GQ2H24AFR-T2C 2G	PD 25K		PU 5K OPT@,SLI@				PD 5K OPT@		64Mx32
		H5GQ1H24BFR-T2C 1G	PD 35K								32Mx32

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0000	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

USER Straps	
User[3:0]	
1000-1100	Customer defined

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

Security Classification	LC Future Center Secret Data		
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Title: N13P_MISC

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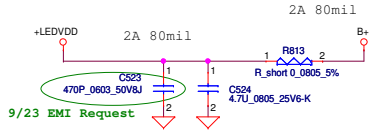

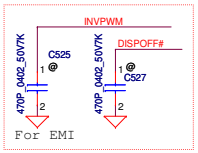

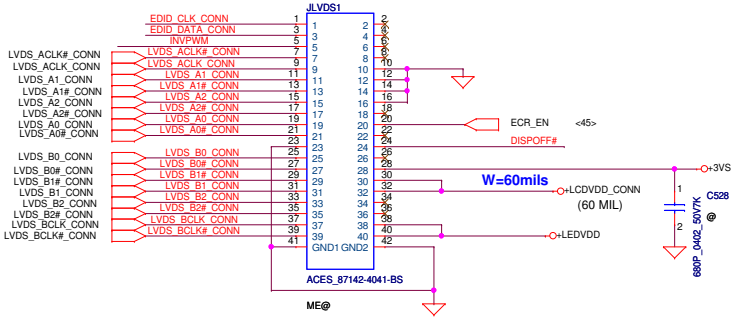

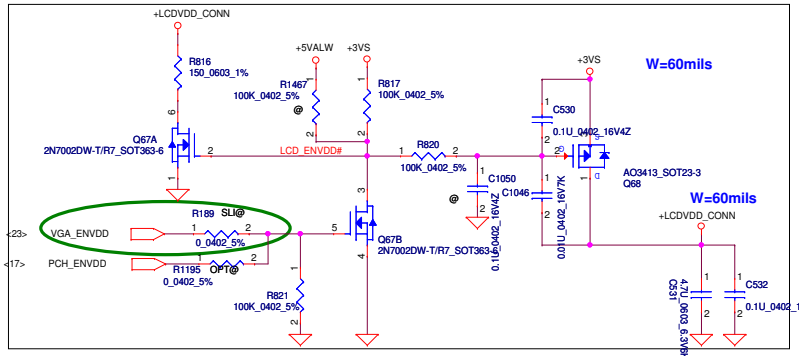

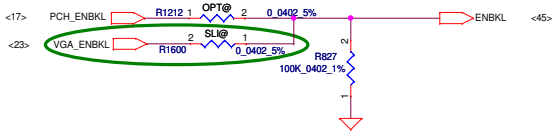

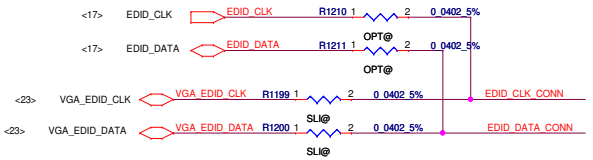

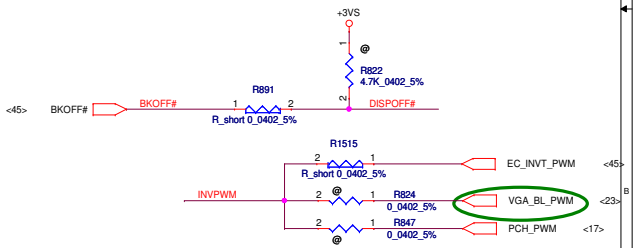

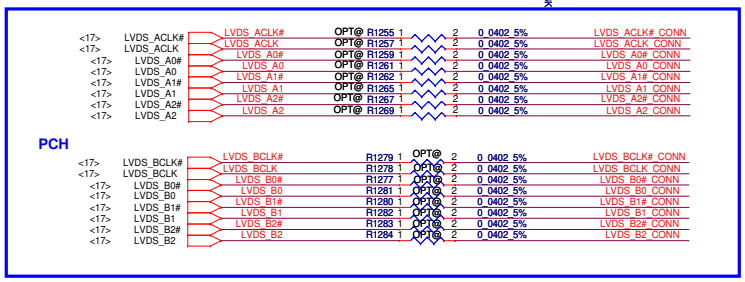

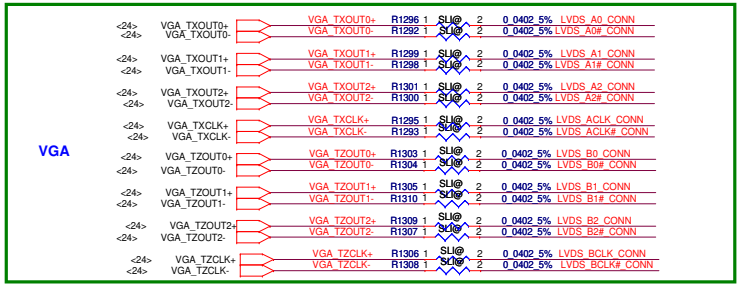

Security Classification	LC Future Center Secret Data		
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Title: LVDS

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No use NVSR chip for DVT

Title		
NO NVSR		
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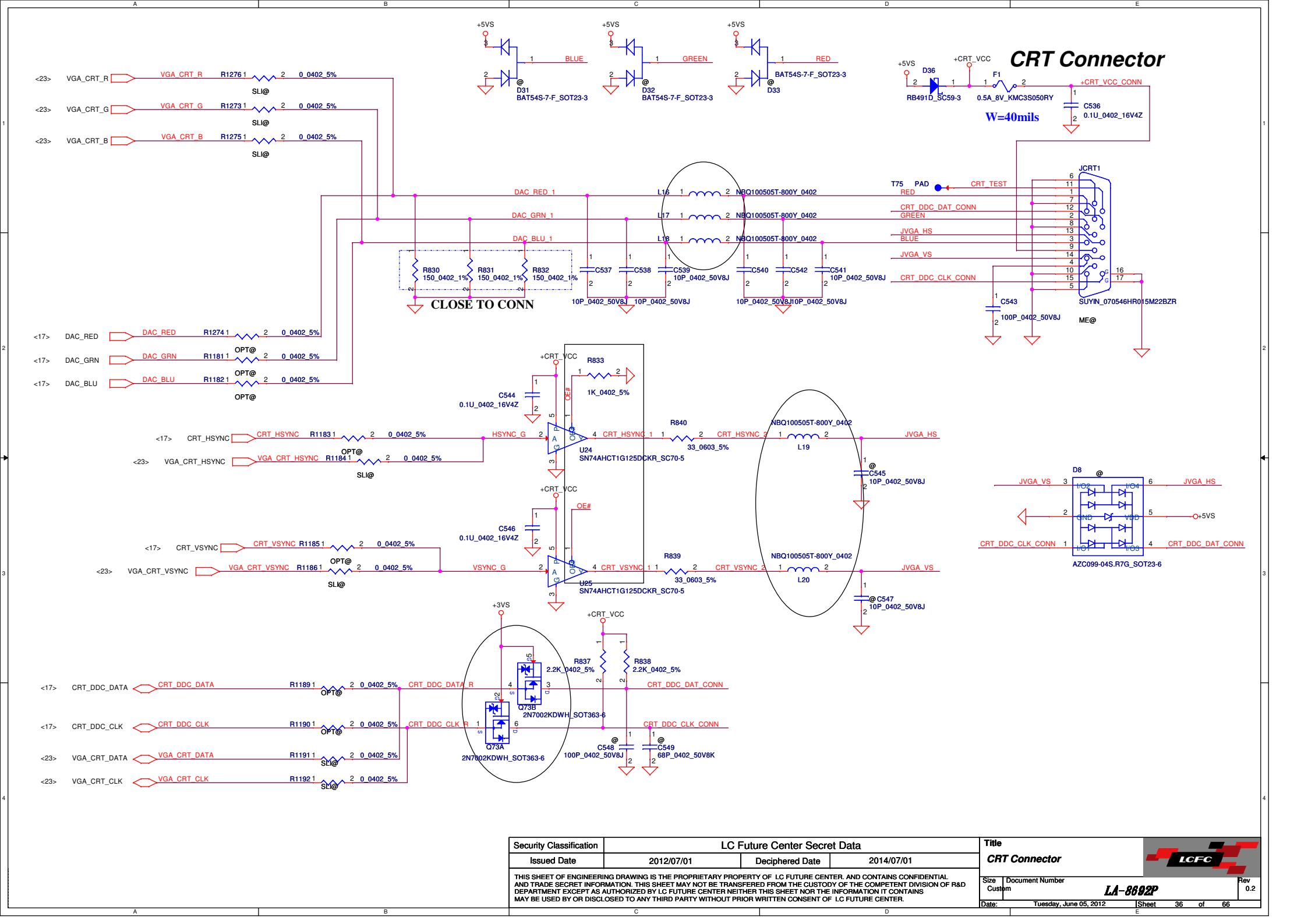
CRT Connector



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	CRT Connector		
Size	Document Number		Rev
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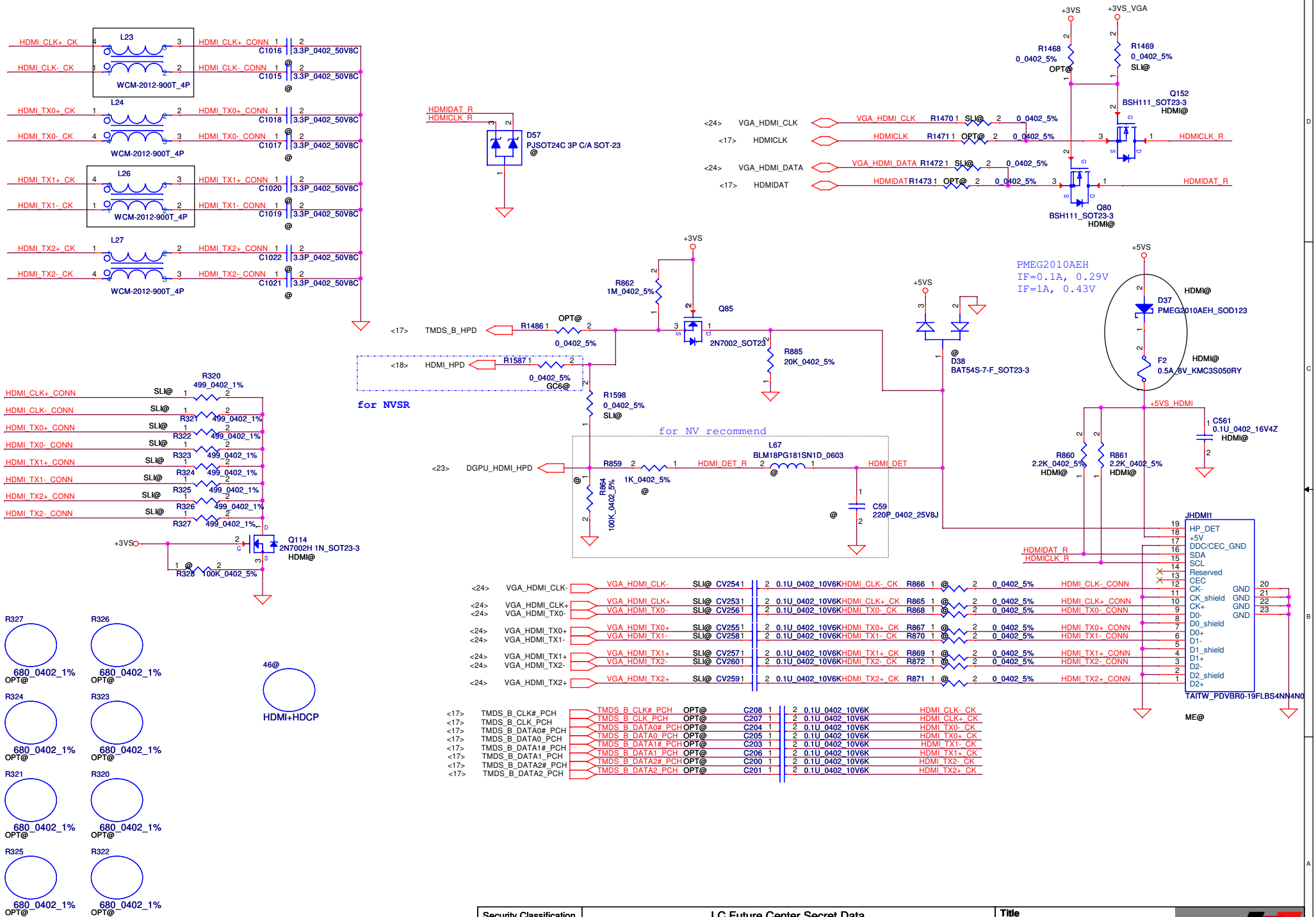

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: **HDMI CONN**

Size	Document Number	Rev
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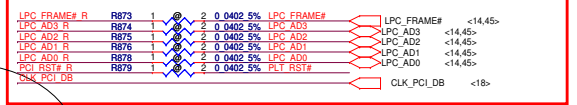
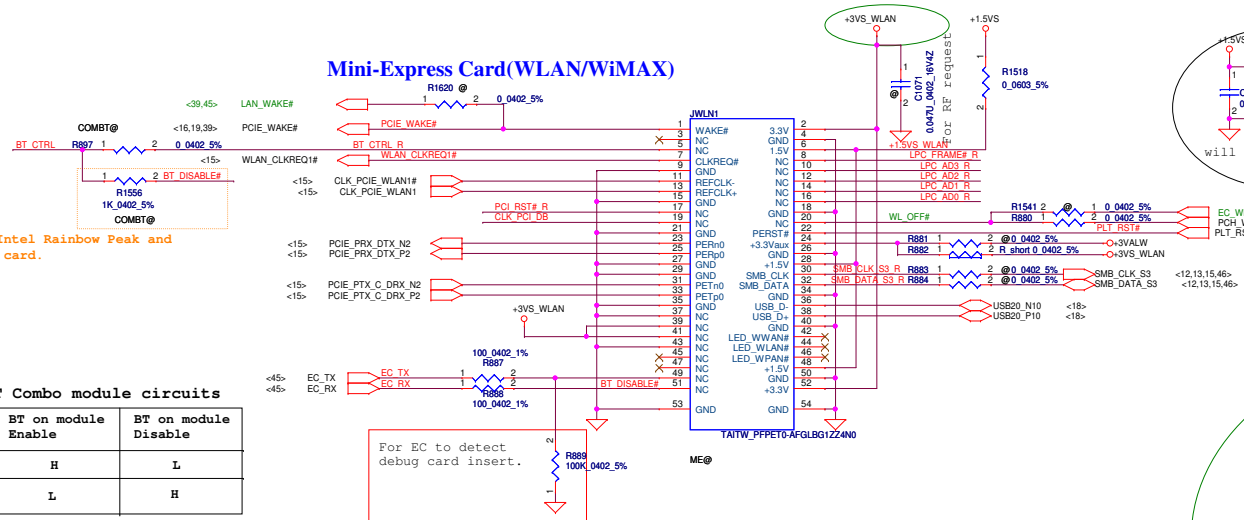
Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)

9/18 JP1 Pin2,24,52 contact to +3VS_WLAN for AOAC function

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



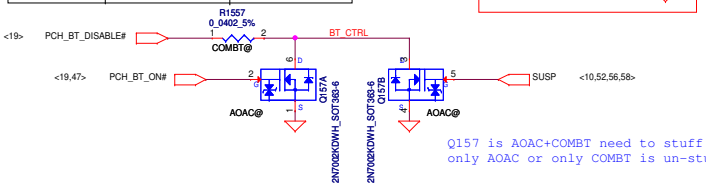
Mini-Express Card(WLAN/WiMAX)



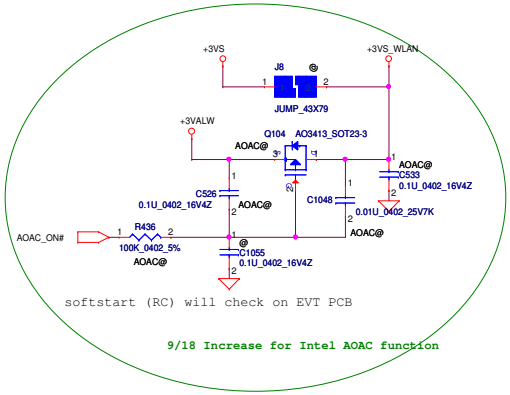
For isolate Intel Rainbow Peak and Compal debug card.

WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CRTL	H	L
PCH_BT_ON#	L	H



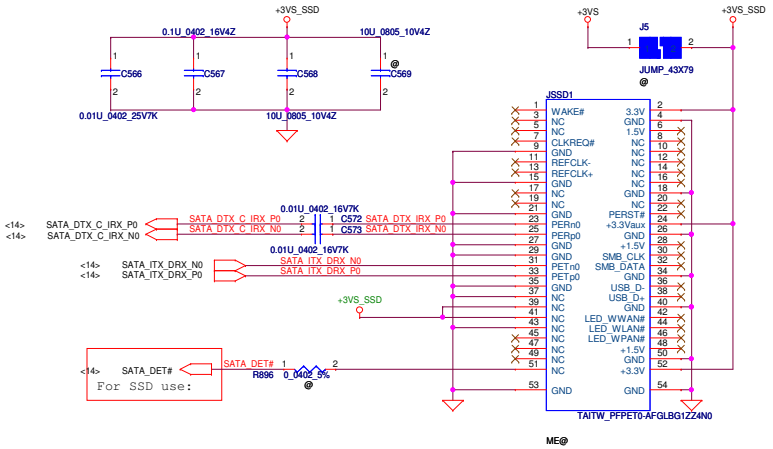
Q157 is AOAC+COMBT need to stuff
only AOAC or only COMBT is un-stuff



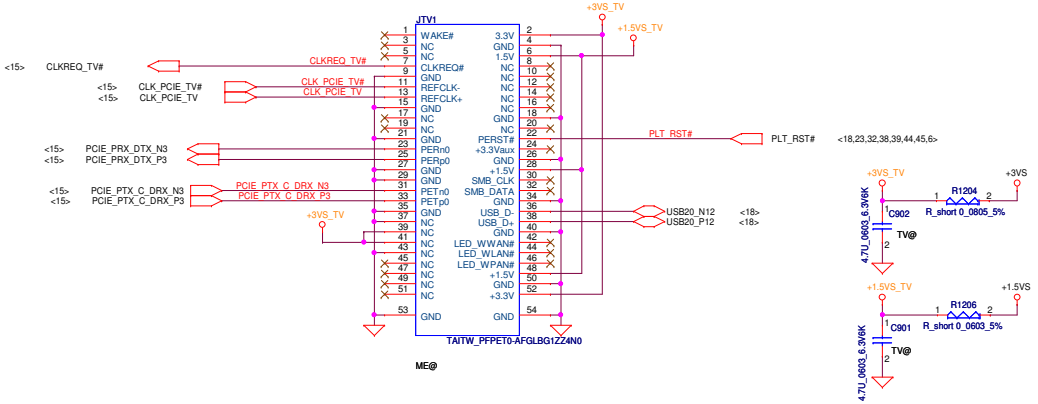
9/18 Increase for Intel AOAC function

Mini-Express Card(SSD)

SSD Active:4.5W(1.5A)



Mini-Express Card(TV)



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	Mini-Card		
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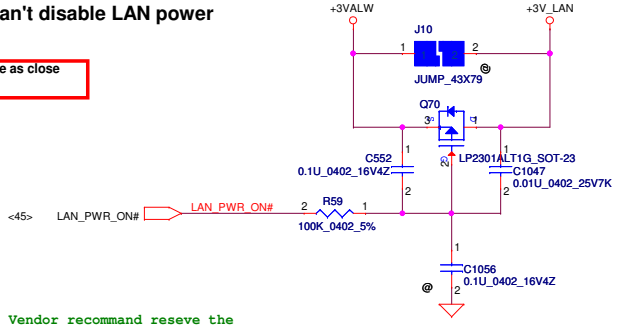
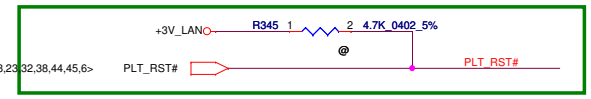
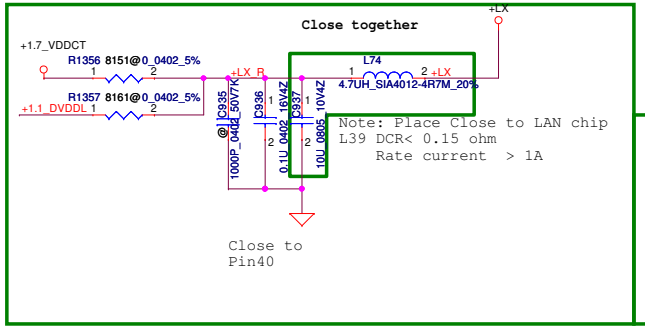
Atheros request can't disable LAN power

Layout Notice : Place as close chip as possible.

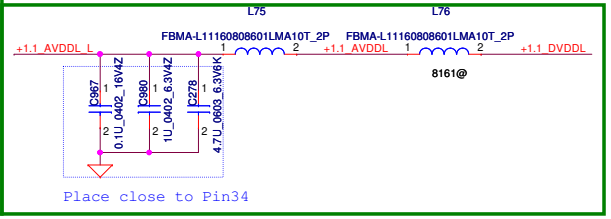


Vendor recommand reseve the PU resistor close LAN chip

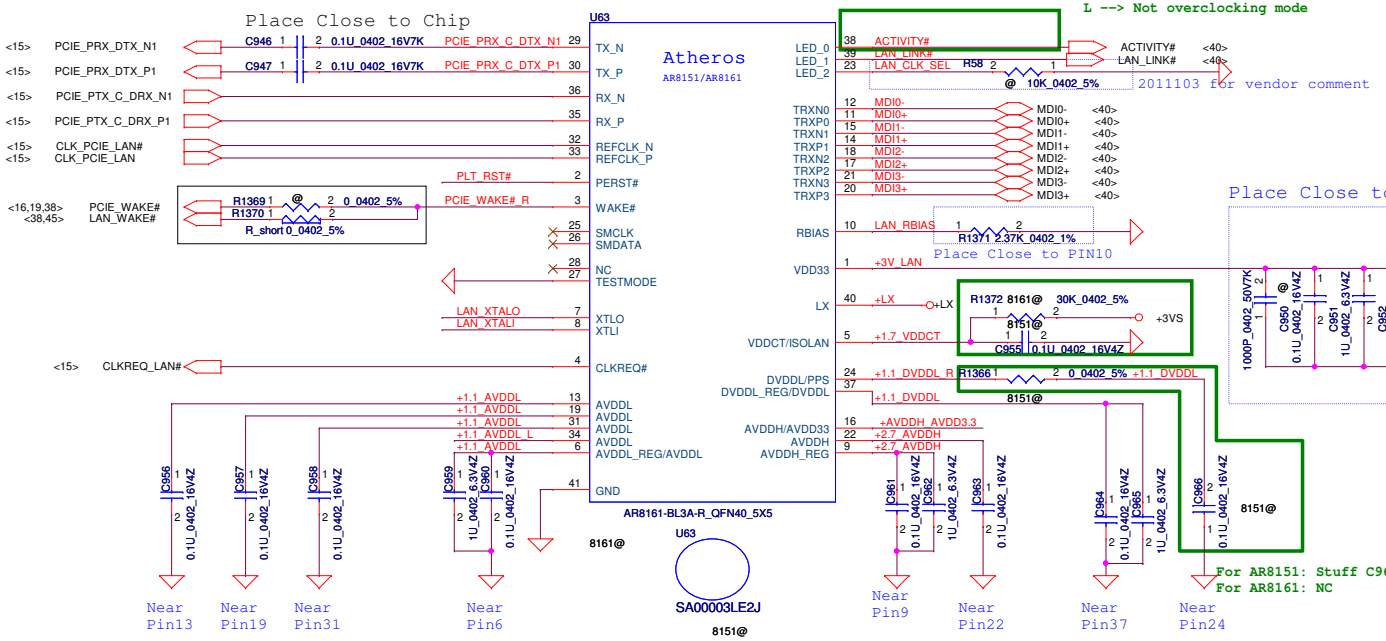


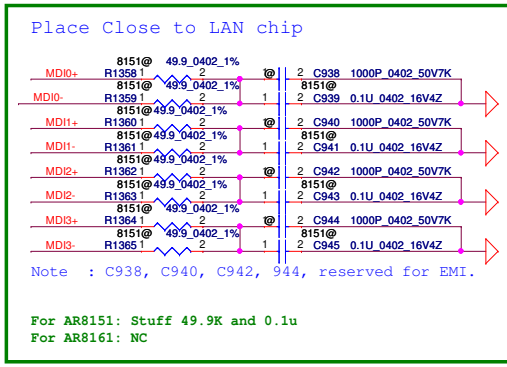


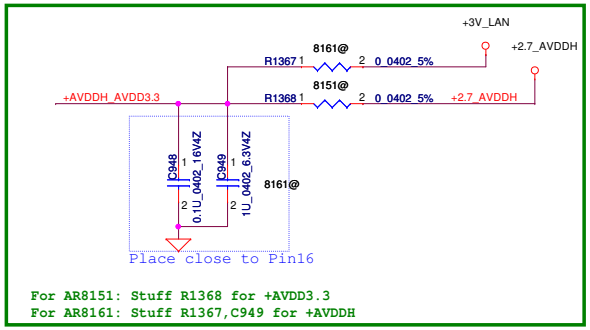
	LX Voltage <Pin 40>	Configure
AR8151	+1.7V <VDDCT>	R1356,C955
AR8161	+1.1V <DVDDL,AVDDL>	R1357,R1372,L76

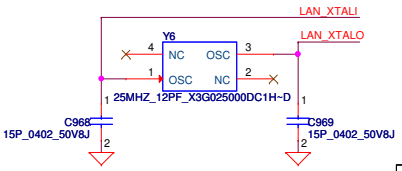


H --> Overclocking mode
L --> Not overclocking mode









Change C968, C969 value of Cap from 33pF to 15pF for TXC recommend

Security Classification	LC Future Center Secret Data		
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Title: **LAN-AR8151/8161**

Size	Document Number	Rev
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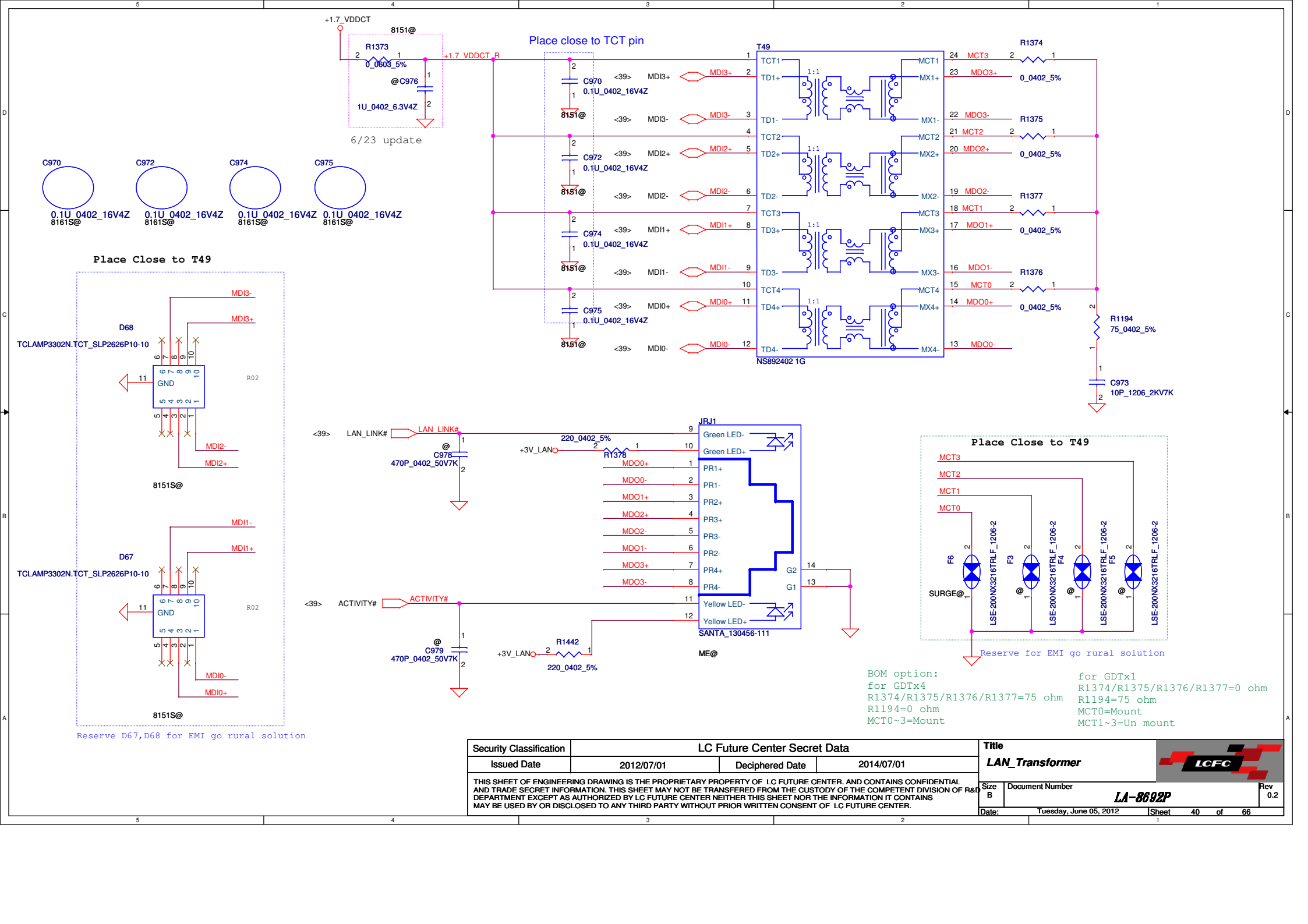

Title			
LAN_Transformer			
Size: B	Document Number: LA-8692P		Rev: 0.2
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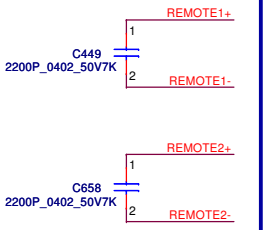
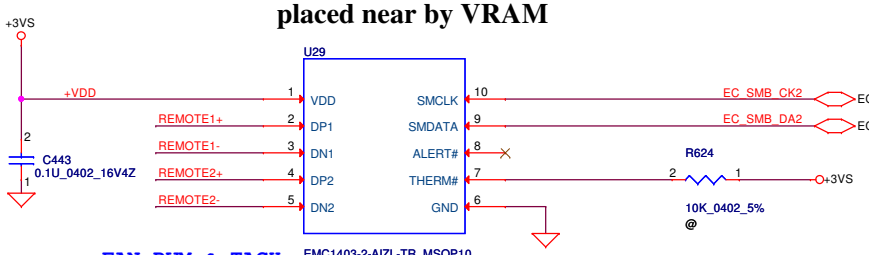
Close U29



SMSC thermal sensor placed near by VRAM

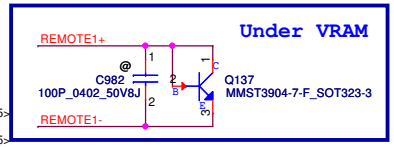


FAN_PWM & TACH for PWM FAN

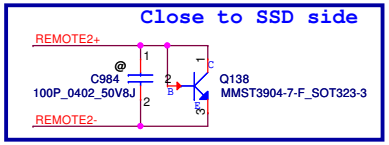
Address 1001_101xb

internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp

Under VRAM

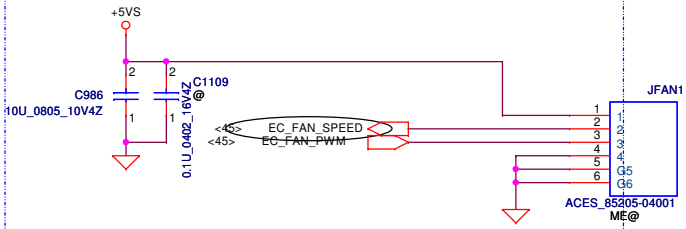


Close to SSD side



REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: *EMC1403/2103_Thermal sensor/FAN*

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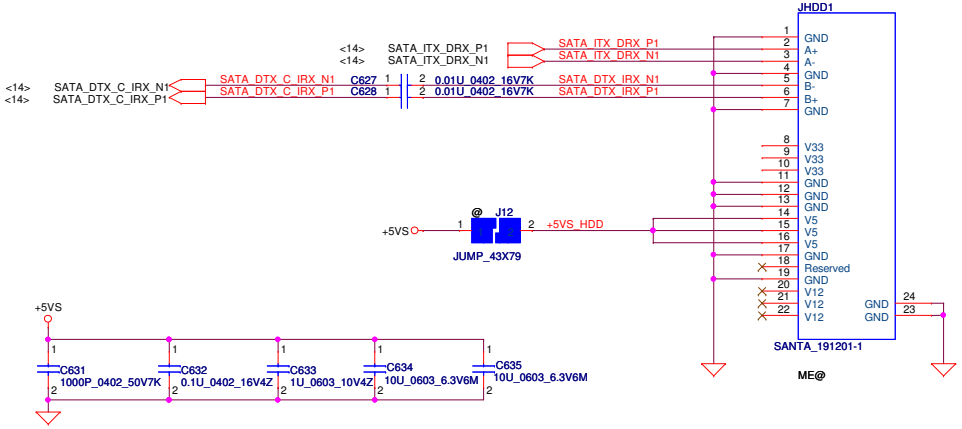
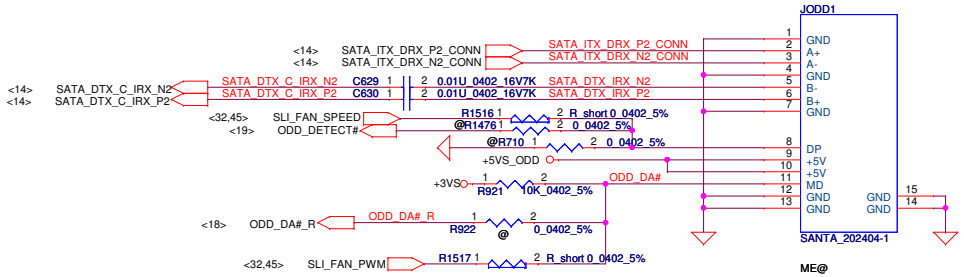
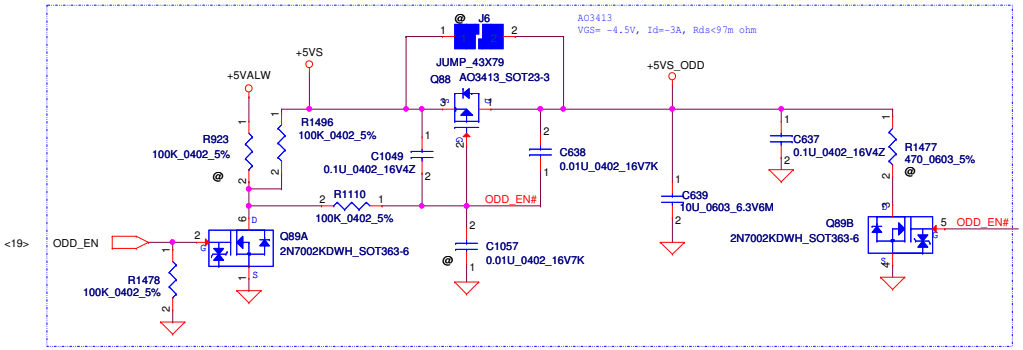
SATA HDD Conn.



SATA ODD Conn.



ODD Power Control



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	HDD/ODD Connector		
Size	Document Number		Rev
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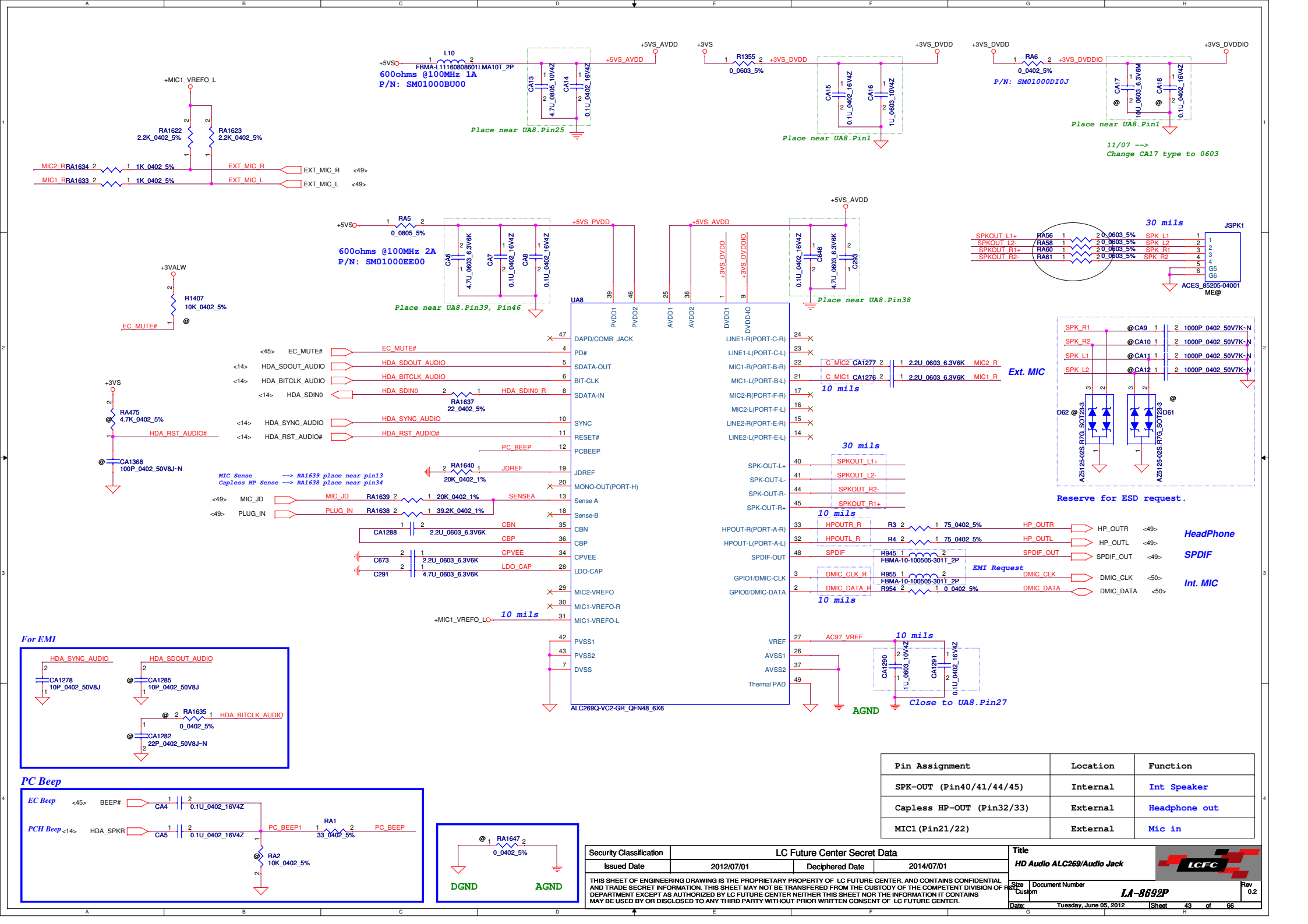

Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1(Pin21/22)	External	Mic in

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	HD Audio ALC269/Audio Jack		
Size	Document Number		Rev
Custom	LA-8692P		0.2
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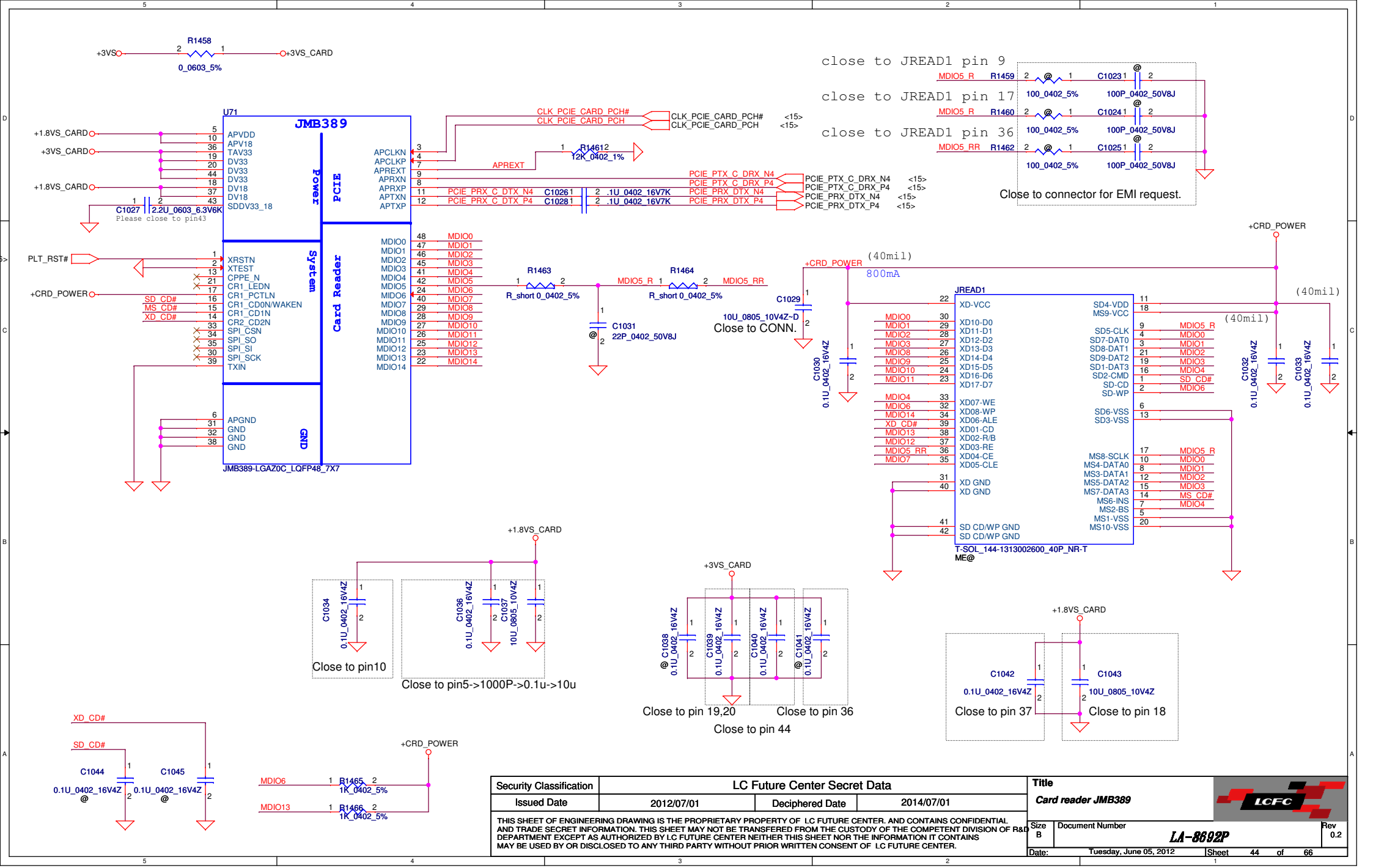

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	Card reader JMB389		
Size B	Document Number LA-8692P		Rev 0.2
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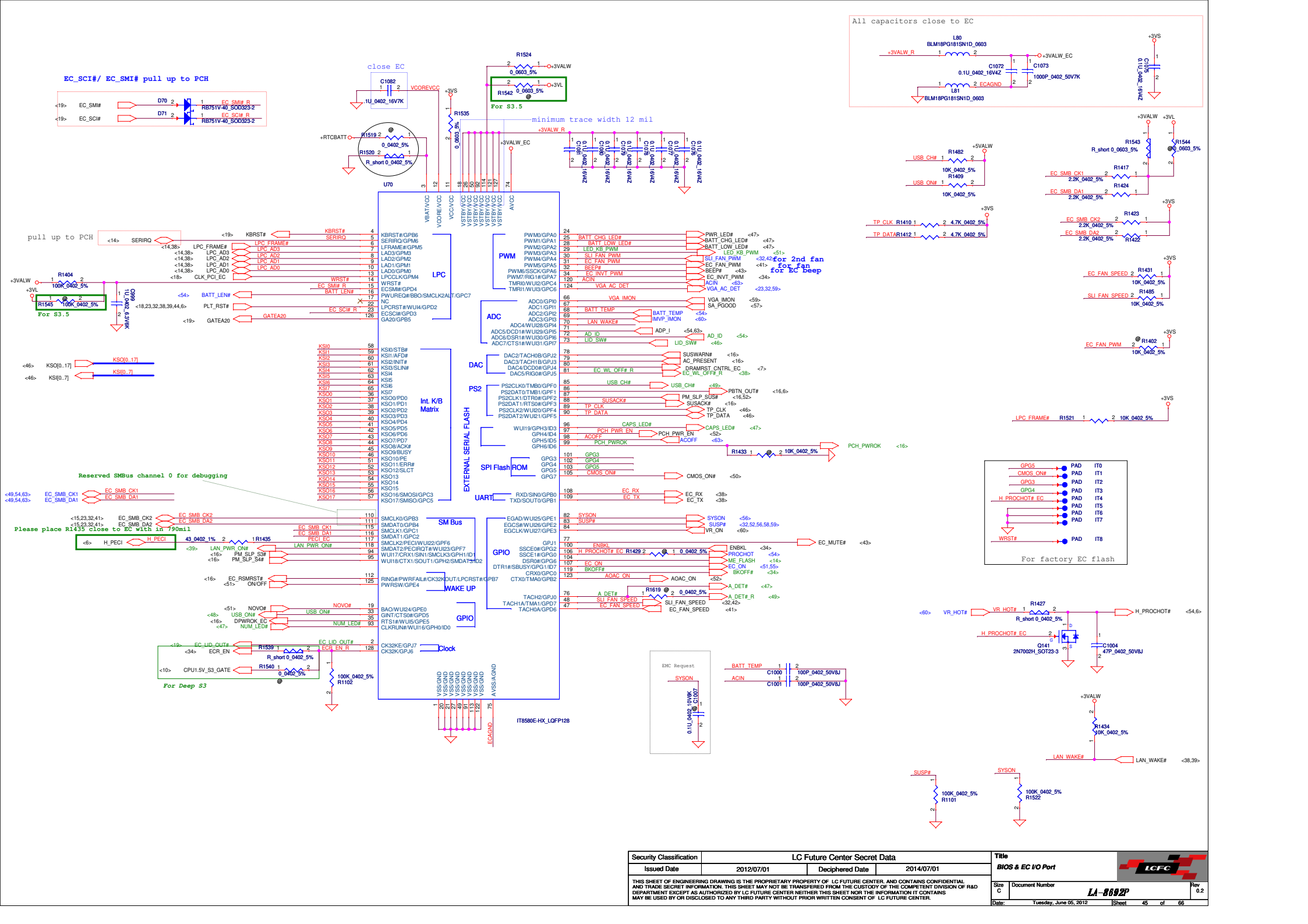

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title	BIOS & EC I/O Port
Size	C
Document Number	LA-8692P
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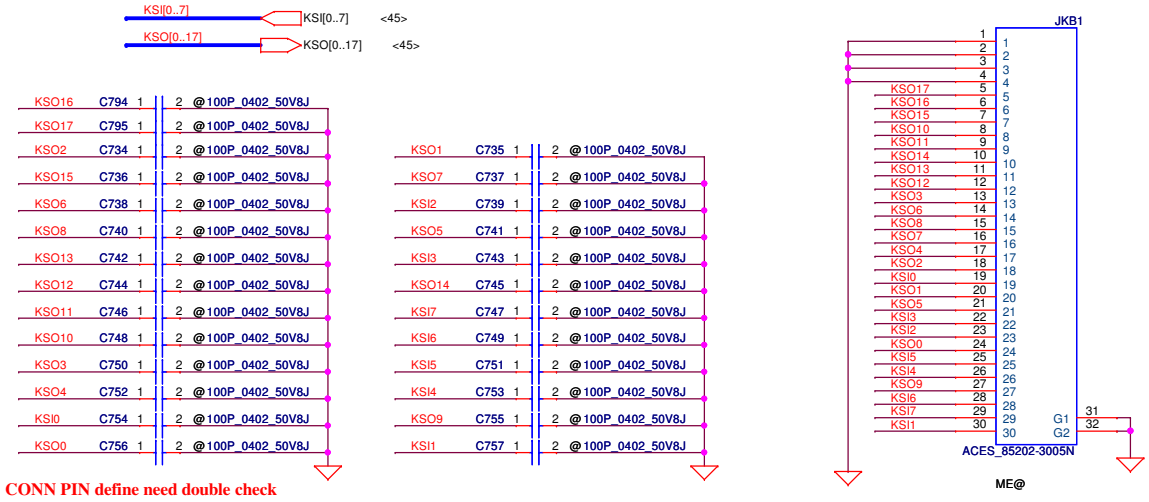
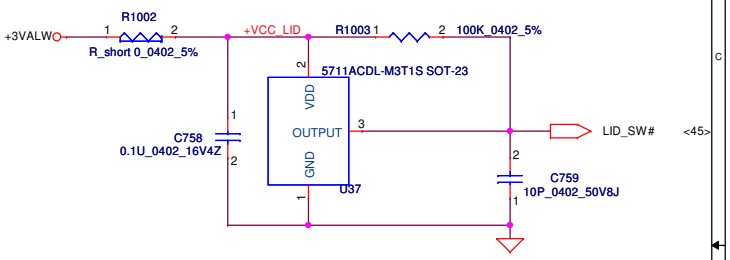
15" INT_KBD Conn.

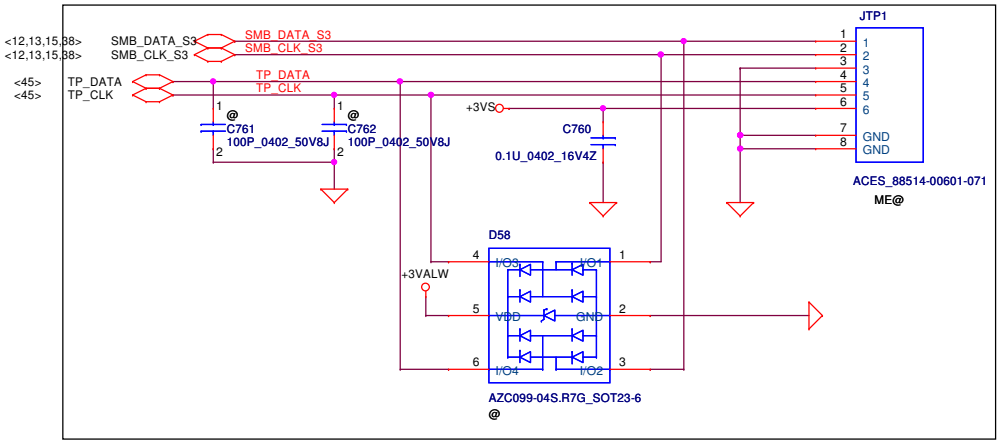


CONN PIN define need double check

Lid Switch



To TP/B Conn.



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	KB /SW /LPC Debug Conn.		
Size B	Document Number LA-8692P		Rev 0.2
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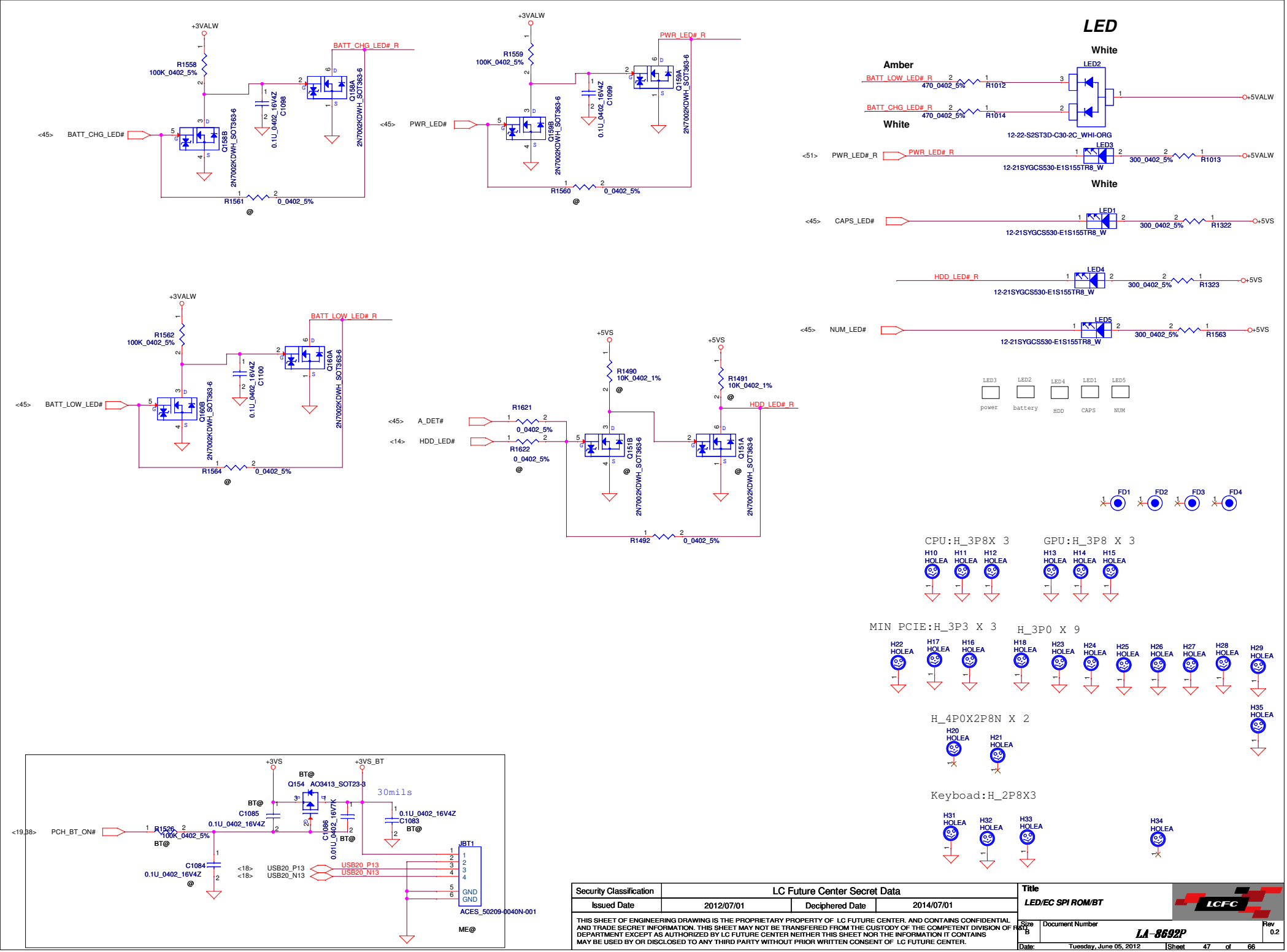

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	LED/EC SPI ROM/BT		
Size	Document Number		Rev
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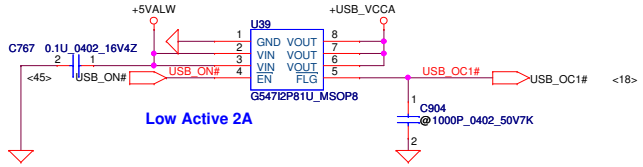
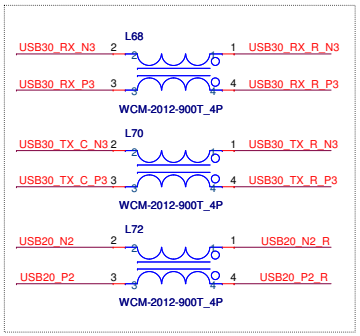
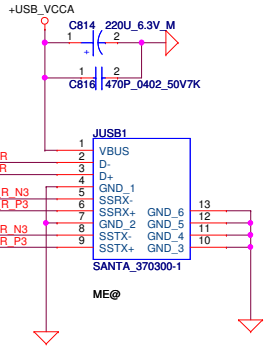
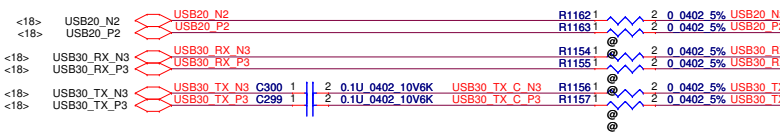
LEFT SIDE USB3.0 PORT X1



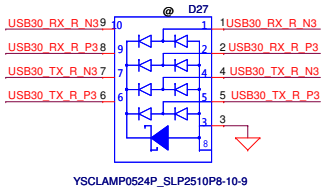
For EMI request
USB2.0 choke --> SM070000I00
USB3.0 Choke --> SM070001U00

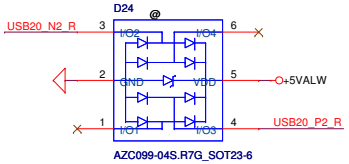


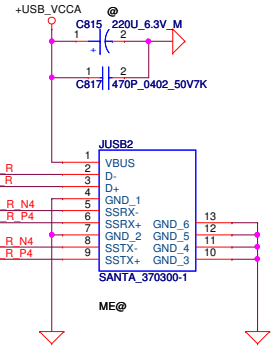




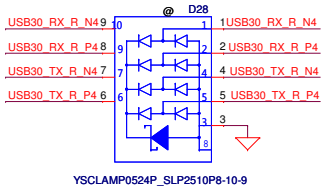
For ESD request

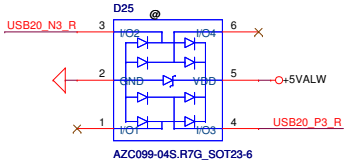




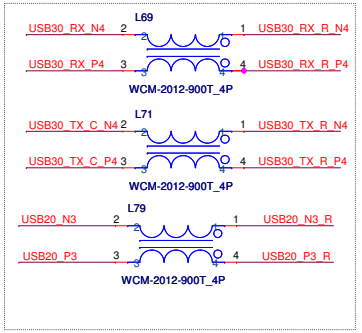


For ESD request





For EMI request
USB2.0 choke --> SM070000I00
USB3.0 Choke --> SM070001U00



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	USB3.0 ports		
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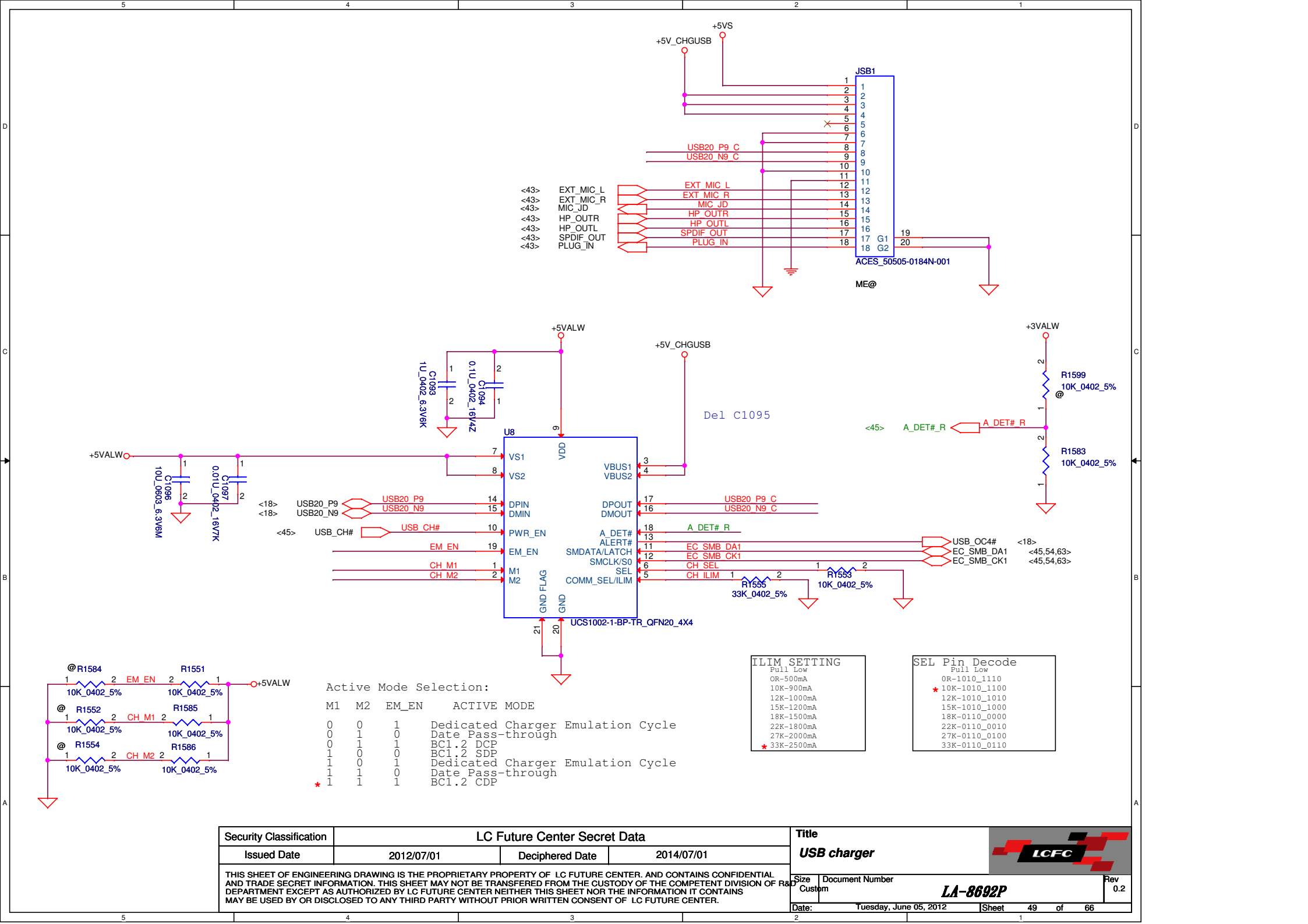
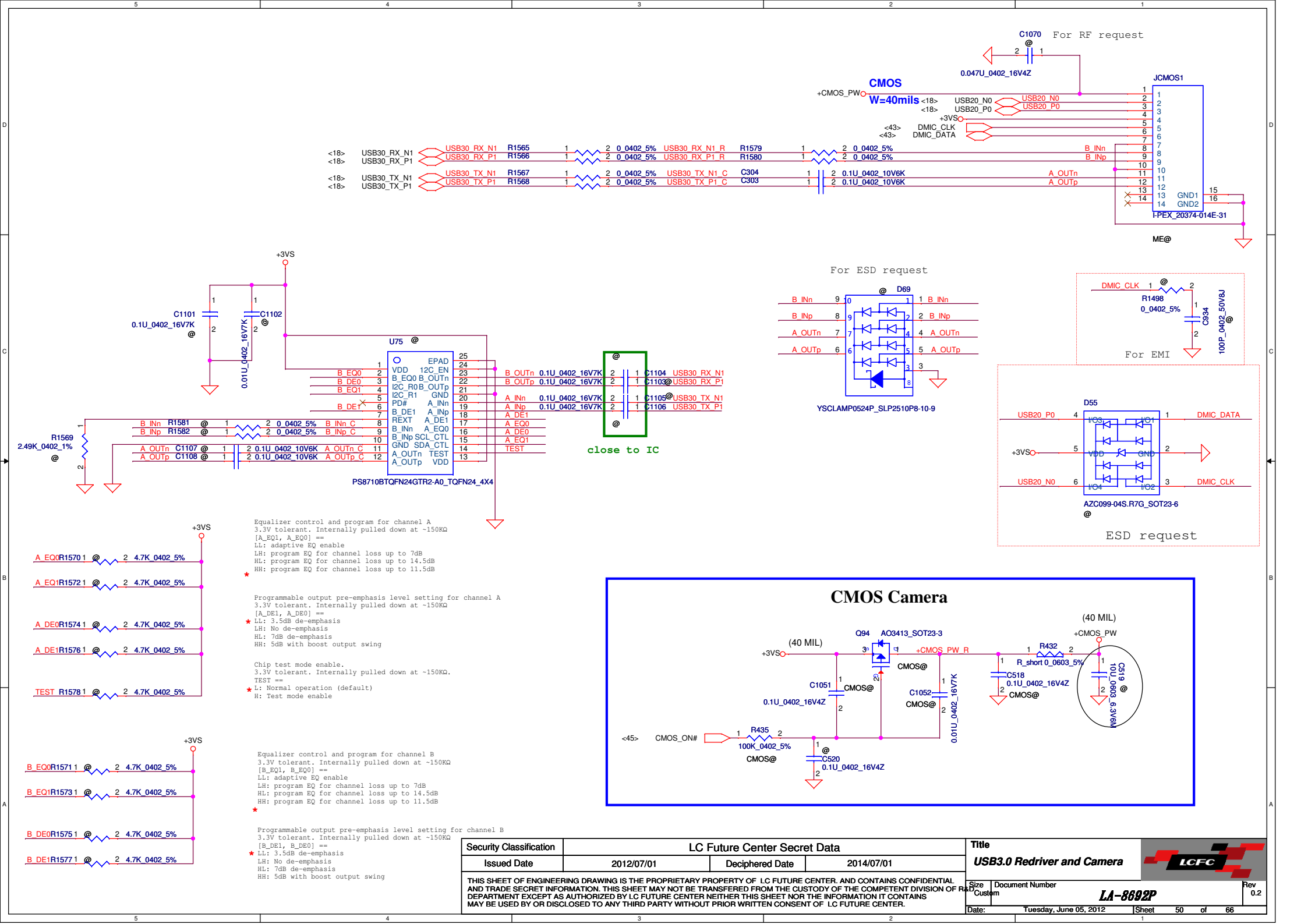


Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: **USB charger**

Size	Document Number	Rev
Custom	LA-8692P	0.2

Date: Tuesday, June 05, 2012 Sheet 49 of 66



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: **USB3.0 Redriver and Camera**

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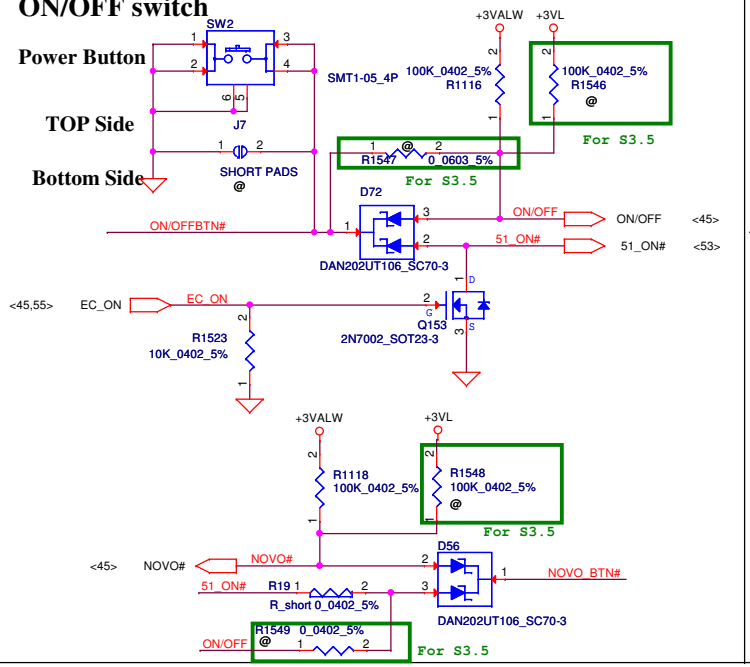
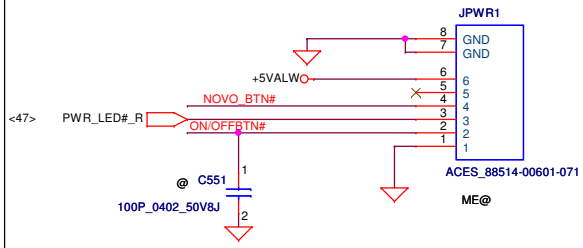
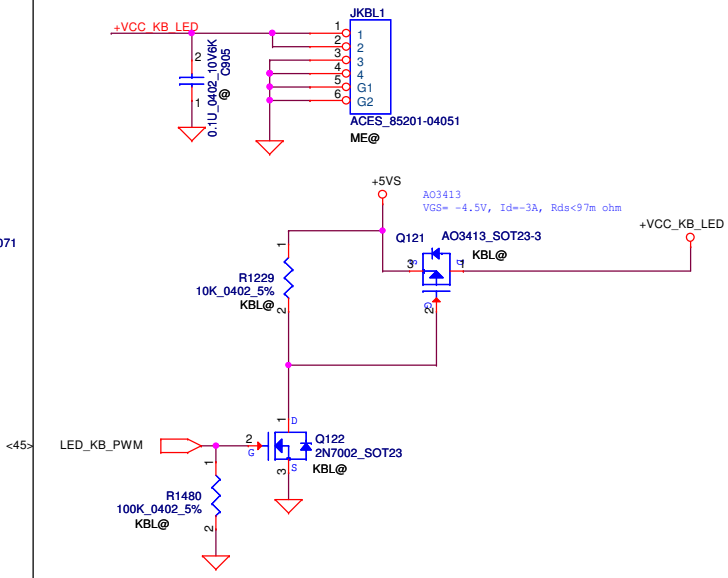
ON/OFF switch



Power Button/B link to Function/B Conn. 10pin



KB Lighting CONN.4pin



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: *other IO connector*

Size	Document Number	Rev
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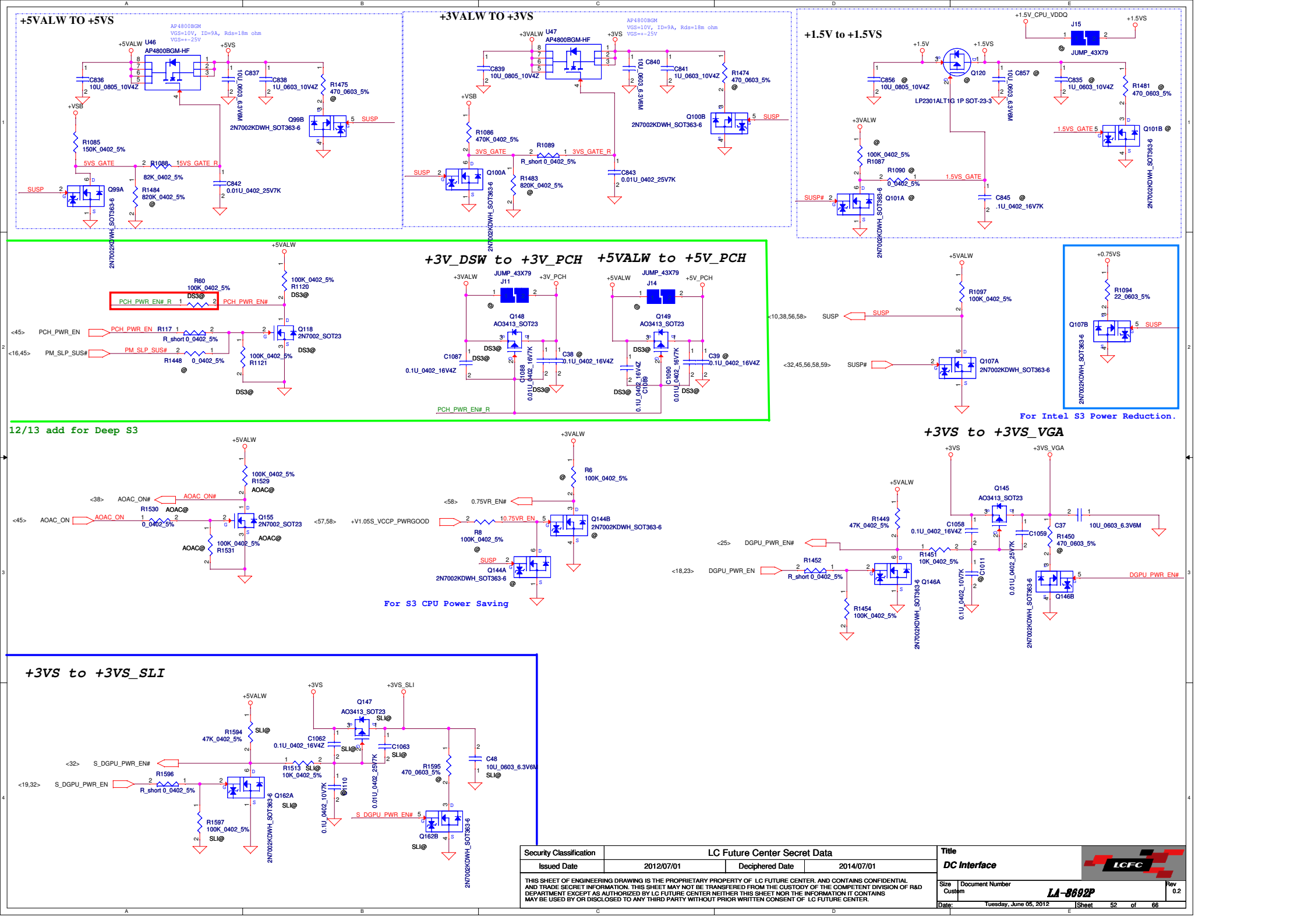

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	DC Interface		
Size	Document Number		Rev
Custom	LA-8692P		0.2
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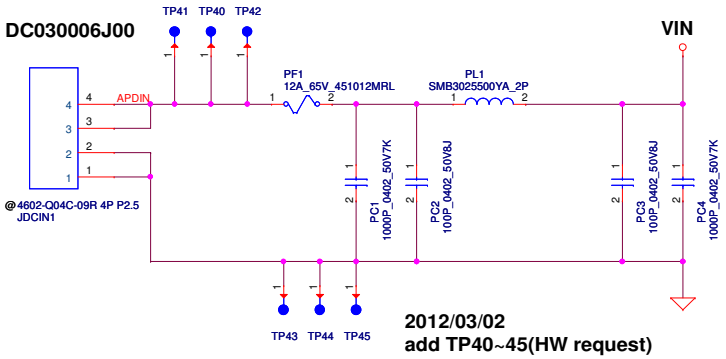

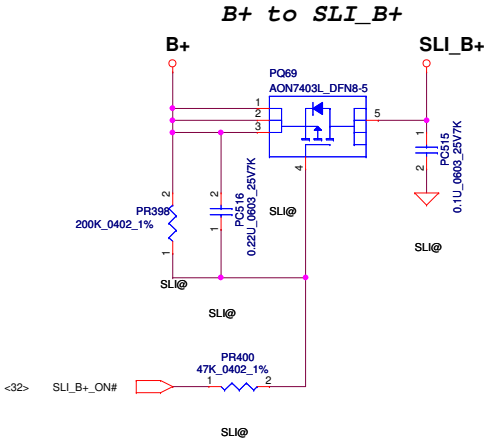

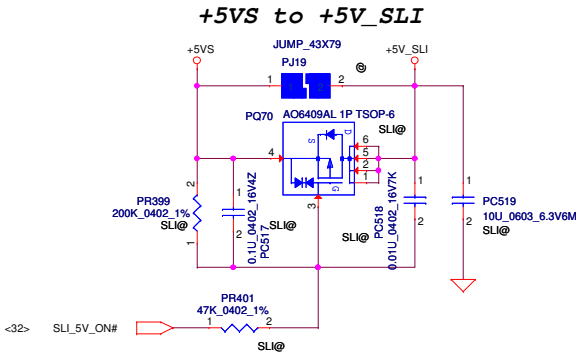

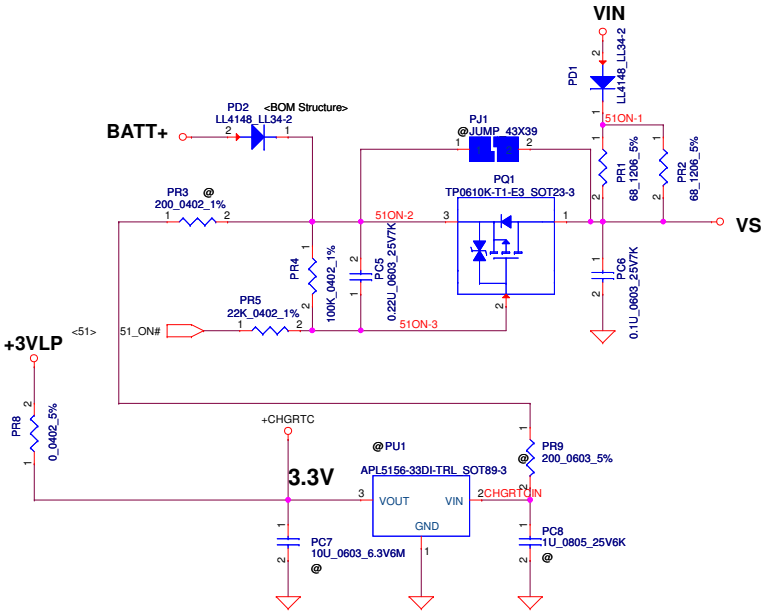

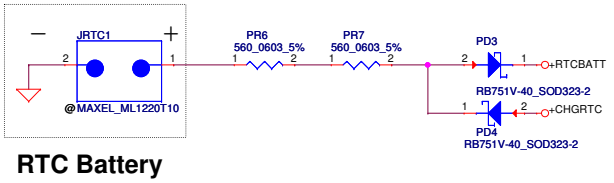

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	Vin Detector		
Size	Document Number		Rev
Custom	LA-8692P		0.2
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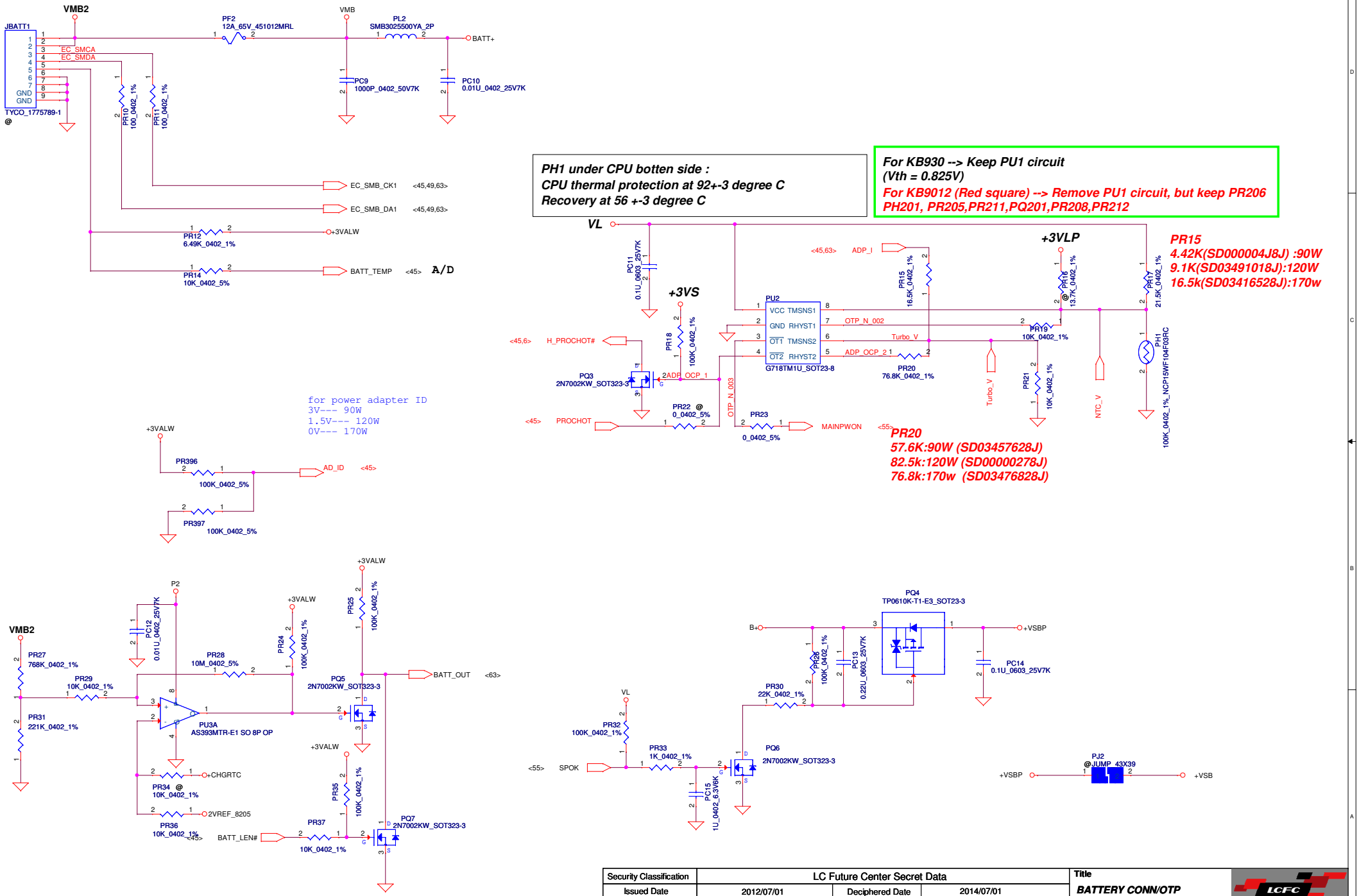

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	BATTERY CONN/OTP		
Size: Custom	Document Number: LA-8692P		Rev: 0.2
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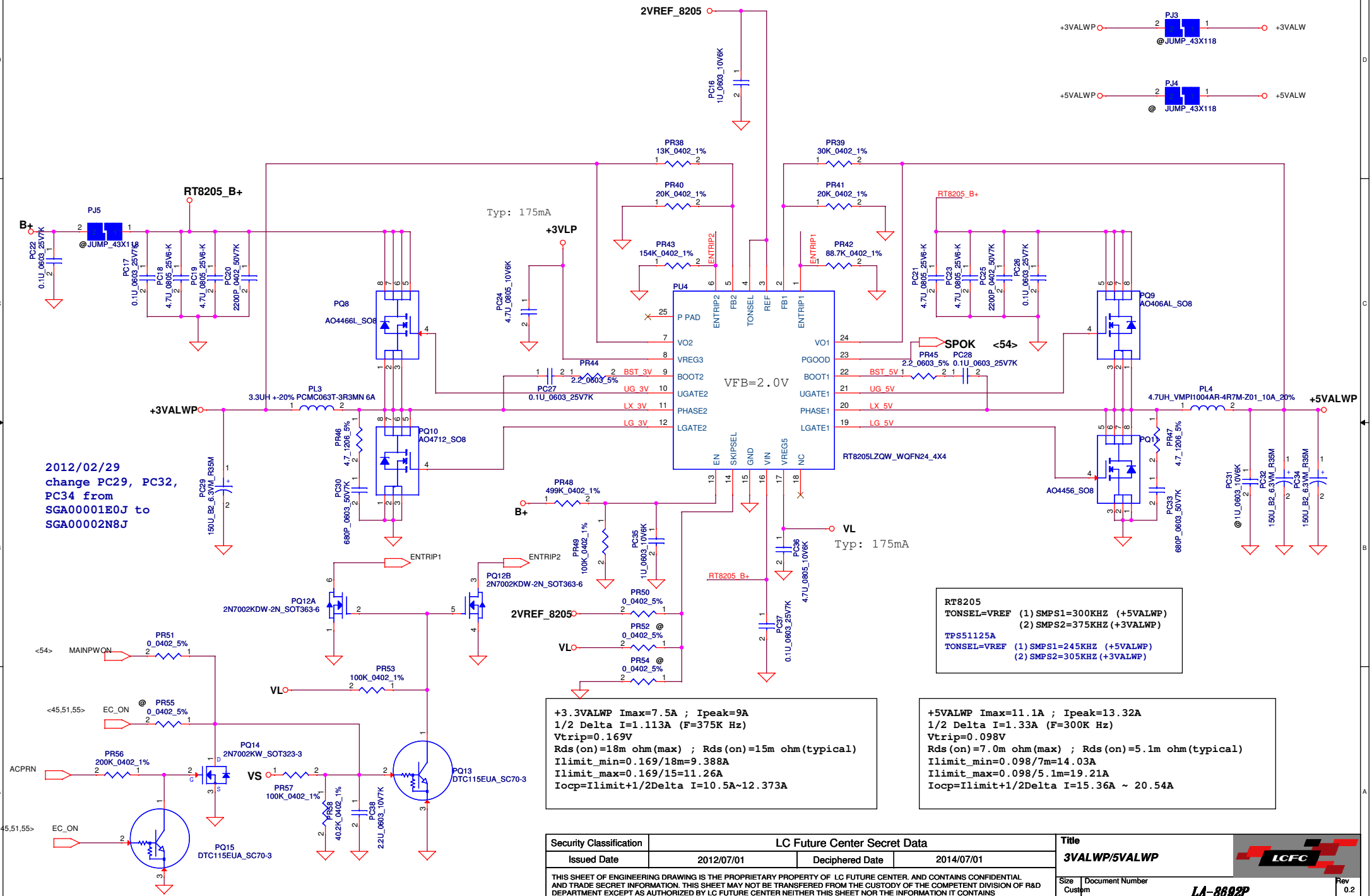
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



RT8205
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ(+3VALWP)
TPS51125A
TONSEL=VREF (1)SMPS1=245KHZ (+5VALWP)
(2)SMPS2=305KHZ(+3VALWP)

+3.3VALWP Imax=7.5A ; Ipeak=9A
1/2 Delta I=1.113A (F=375K Hz)
Vtrip=0.169V
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Ilimit_min=0.169/18m=9.388A
Ilimit_max=0.169/15=11.26A
Iocp=Ilimit+1/2Delta I=10.5A~12.373A

+5VALWP Imax=11.1A ; Ipeak=13.32A
1/2 Delta I=1.33A (F=300K Hz)
Vtrip=0.098V
Rds(on)=7.0m ohm(max) ; Rds(on)=5.1m ohm(typical)
Ilimit_min=0.098/7m=14.03A
Ilimit_max=0.098/5.1m=19.21A
Iocp=Ilimit+1/2Delta I=15.36A ~ 20.54A

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: 3VALWP/5VALWP

Size: Custom | Document Number: LA-8692P | Rev: 0.2

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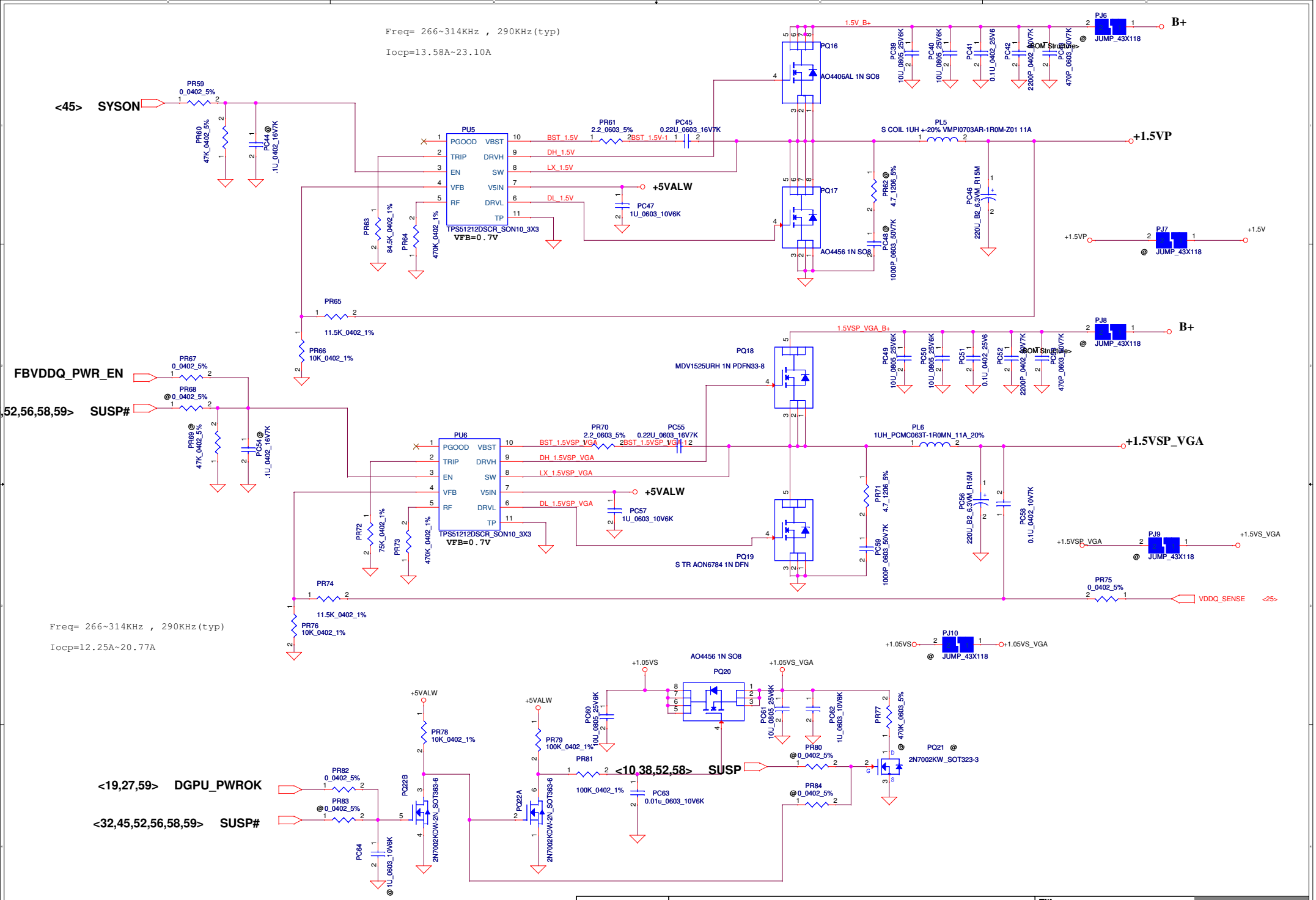

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: 1.5VP/1.5VSP_VGA/1.05VSP_VGA

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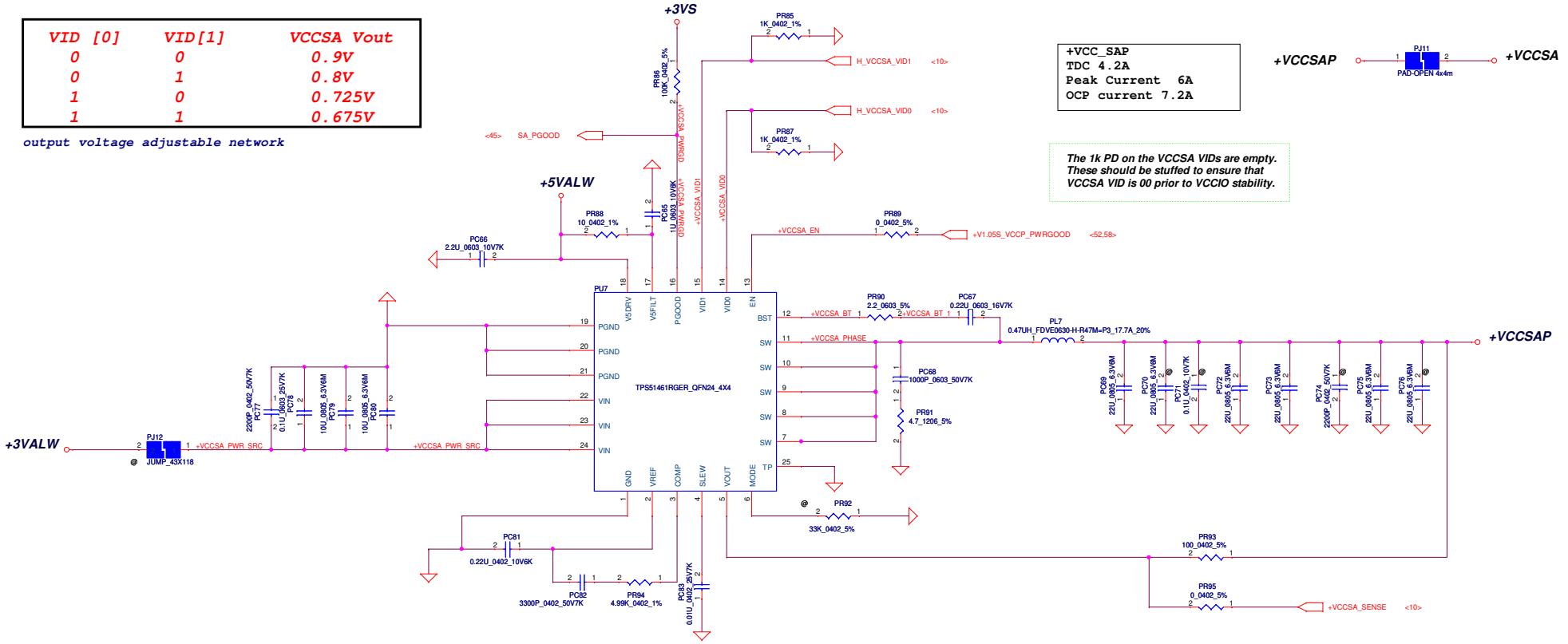
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: VCCSAP/1.05S_VCCPP

Size	Document Number	Rev
C	LA-8692P	0.2

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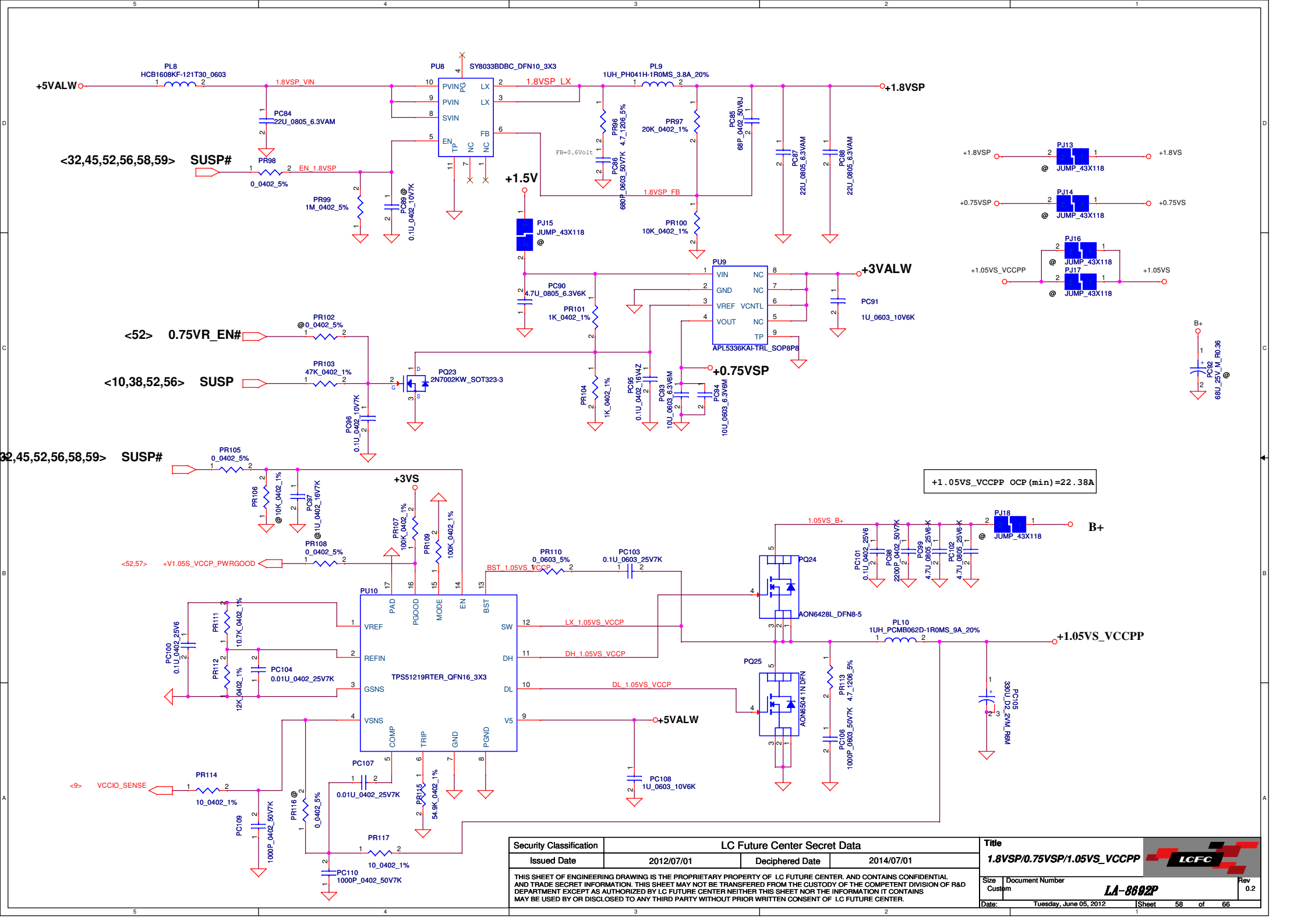

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	1.8VSP/0.75VSP/1.05VS_VCCPP		
Size	Document Number		Rev
Custom	LA-8692P		0.2
Date:	Tuesday, June 05, 2012	Sheet	58 of 66

GL1:0.9V(110000)
GT:0.975V(101010)

2012/04/26
change PC352 from @
to Mount

2012/04/26
change PR313 from 0
to 75K

PQ801@GL1
PQ802@GL1

PQ806@GL1
PQ808@GL1

+VGA_CORE Under VGA Core

+VGA_CORE Near VGA Core

PC818
PC825,PC827,PC828,PC829
PC839,PC841,PC844,PC845

Layout Note:
Place near Phase1 Choke

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title	VGA_COREP		
Size C	Document Number	LA-8682P	Rev 0.2
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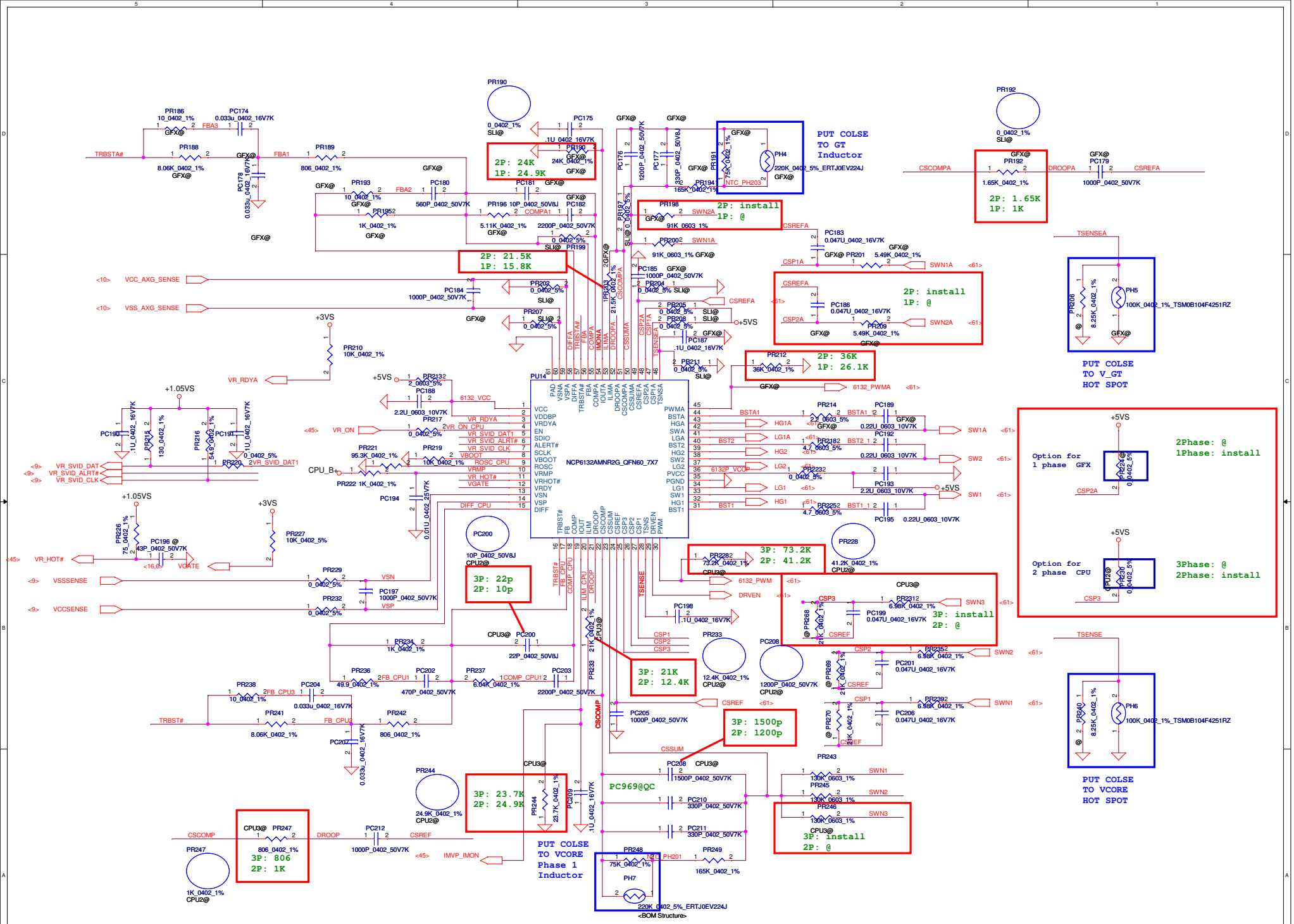

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: CPU_CORE

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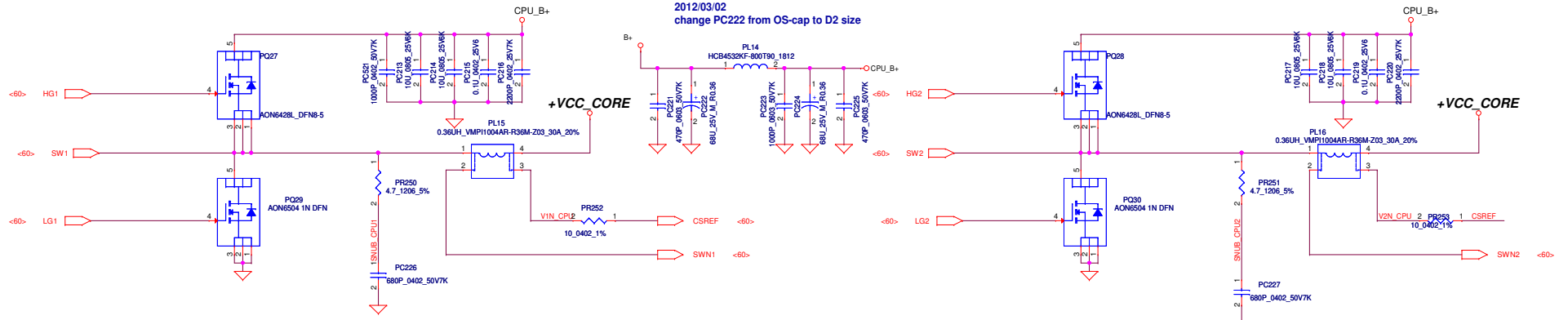
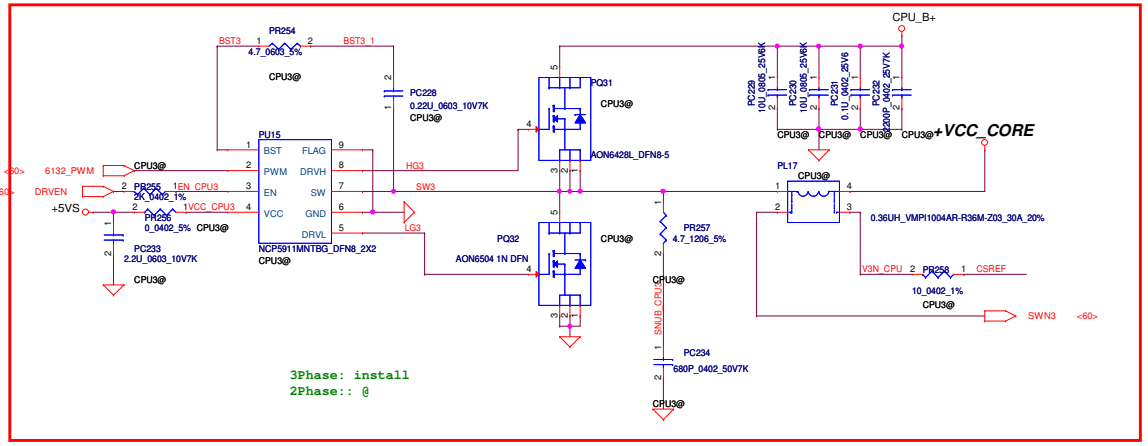
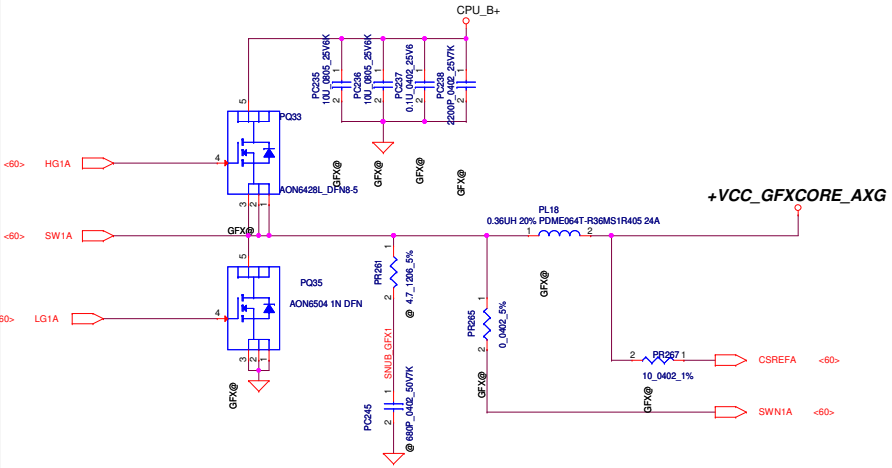
2012/03/02
change PC222 from OS-cap to D2 size

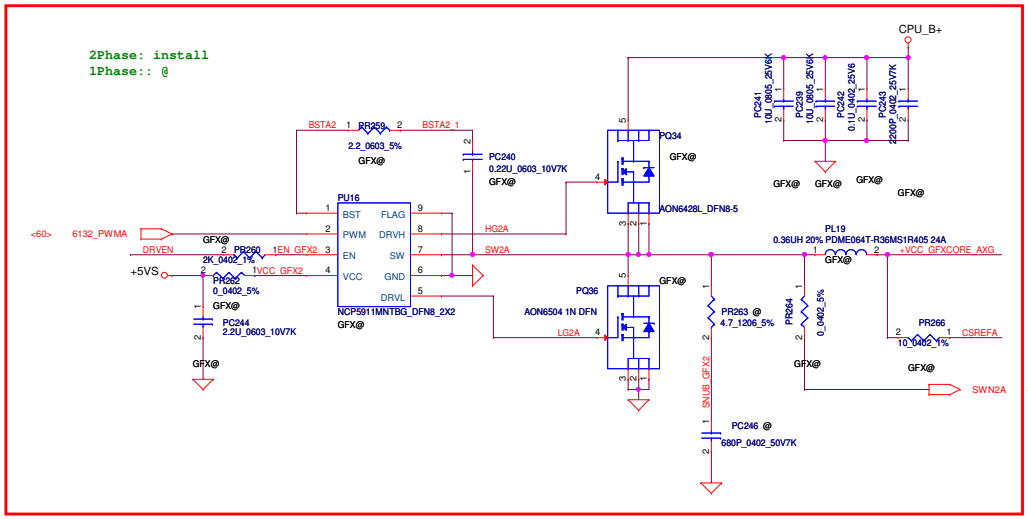




QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP~110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A





QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP~55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

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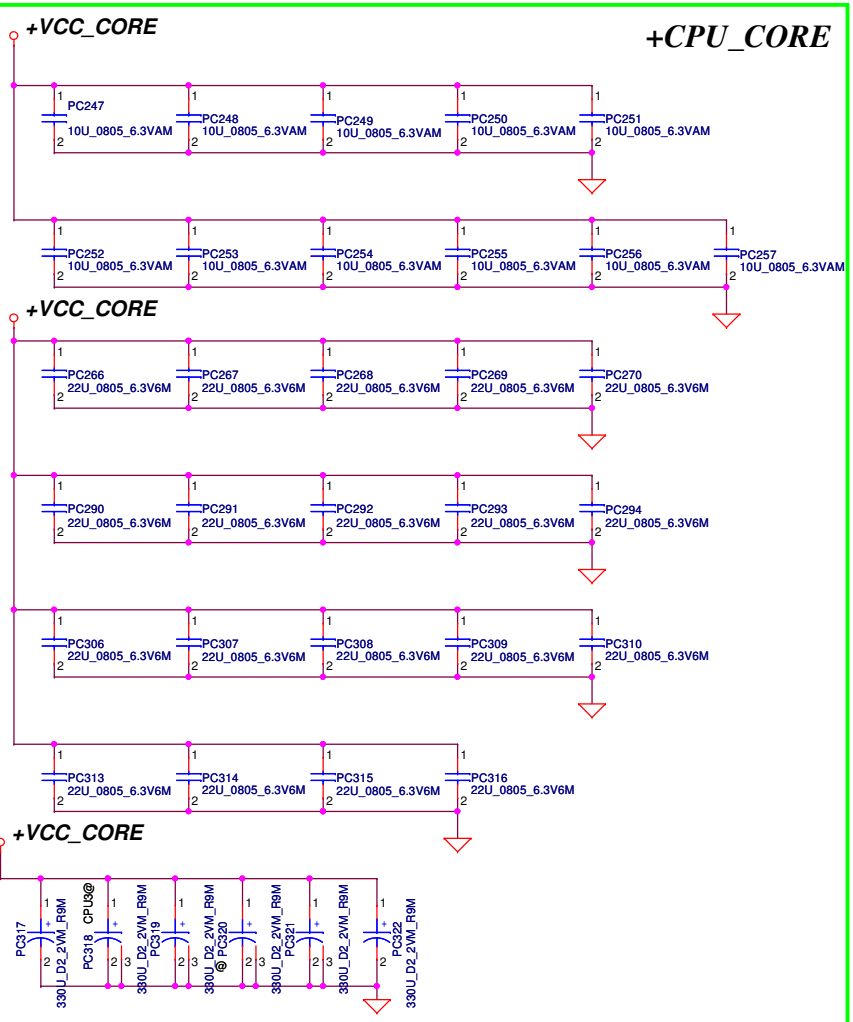
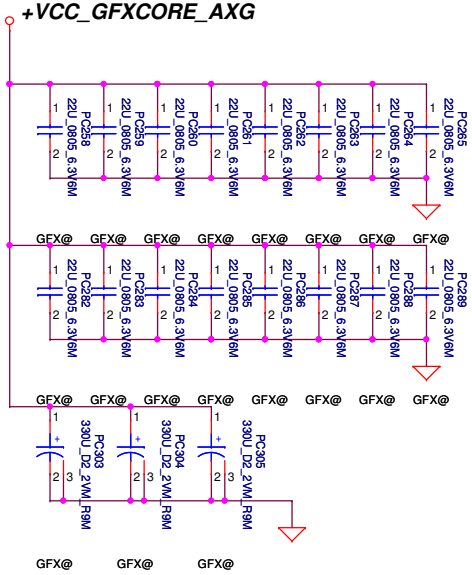
+CPU_CORE



2012/02/29
DC:PC317, PC319, PC321, PC322 (330uF/9m +-20% *4)
QC:PC317, PC318, PC319, PC321, PC322 (330uF/9m +-20% *5)
P/N:SGA0000610J (no link)

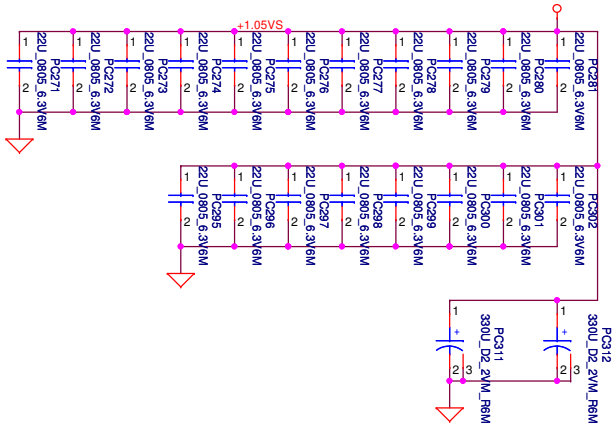
+VCC_GFXCORE_AXG



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites

+1.05VS



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Title: CPU_CORE1

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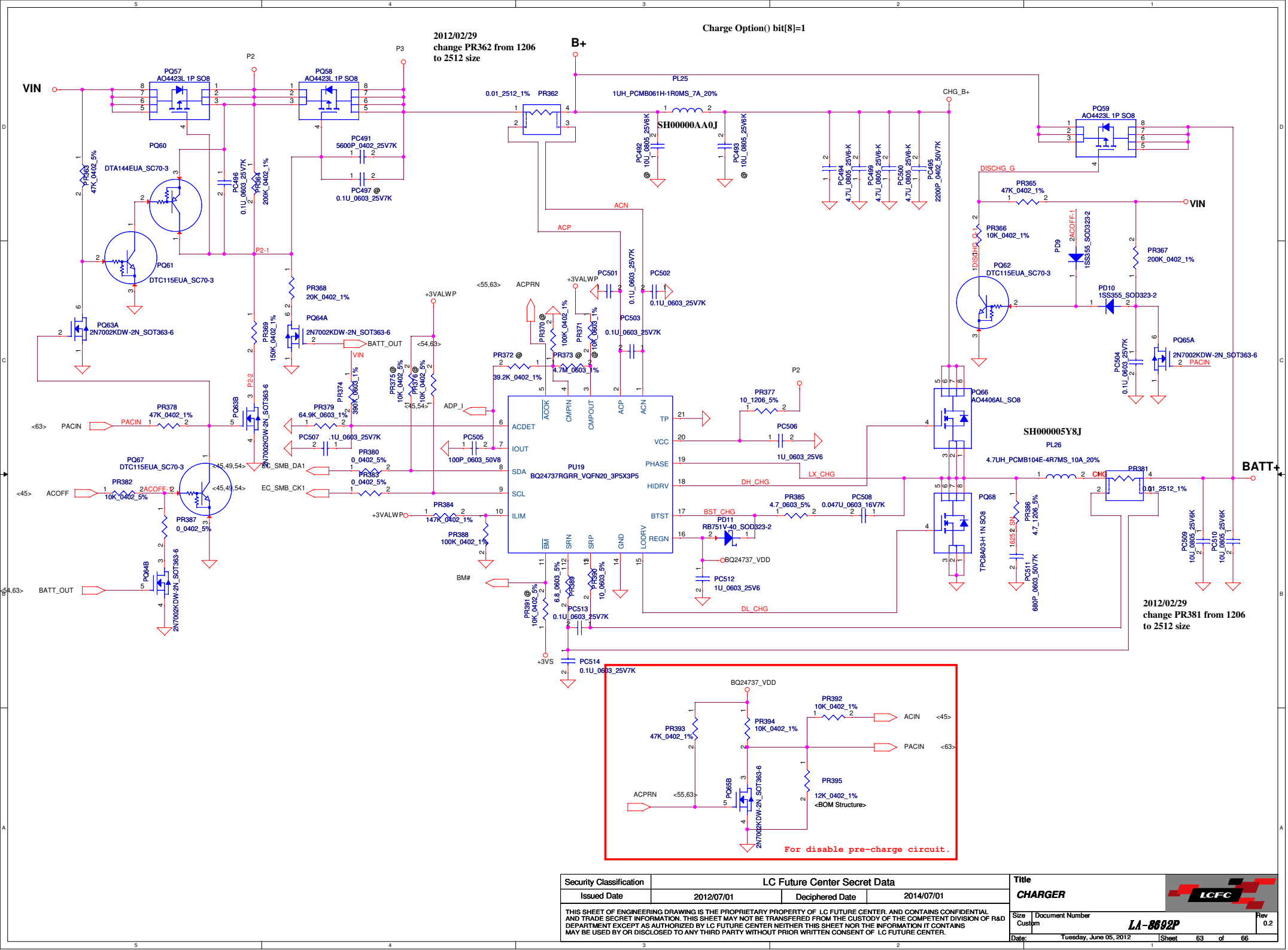

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: CHARGER

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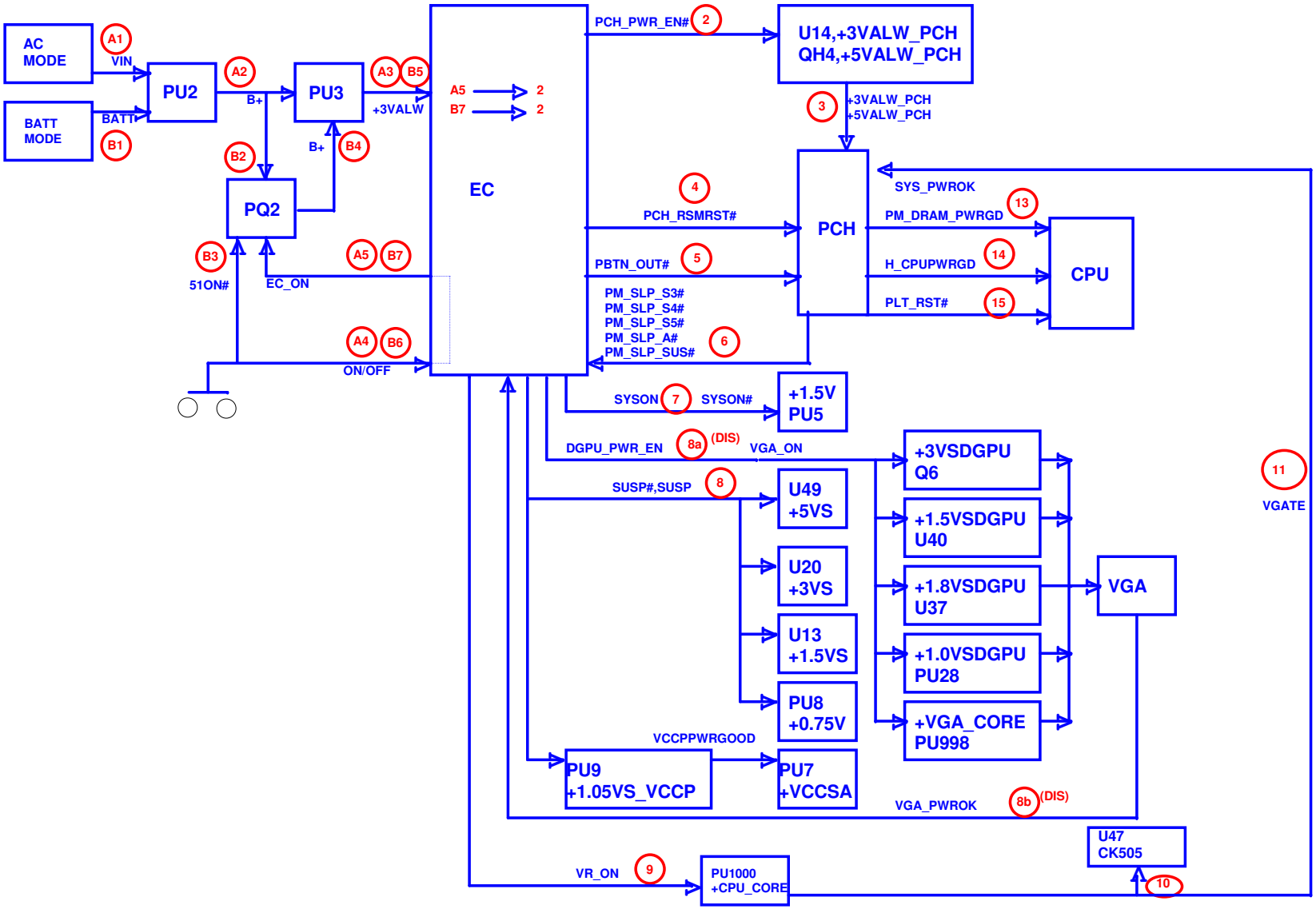

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: *Power sequence*

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Reserve 0.1uF for Charger IC	51	Reserve PC321	201109/27	B test
2	EMI Request		change PR322,PR407,PR408,PR503,PR511,PR606,PR804,PR827 to 2.2 ohm add PC526,PC527,PC970,PC971(470uF)	201109/27	B test
3	Combine 1.05V	51	Remove one power rail +V1.05S_VCCPP Pop PR722,PR712,PR718	201109/27	B test
4	Discharge for +1.05VS_VGA by NV Request	53	Reserve PR528	201109/27	B test
5	Set VGA_CORE VBOOT voltage	56	unpop PR806 change PR813 to 147K ohm	201109/27	B test
6	For VGA_CORE power saving by NV Request	56	add PR838 0ohm	201109/27	B test
7	for CPU_CORE load line adjust	57	add PC969	201109/27	B test
8	to prevent MOS over temperature	55/58	change PQ702,PQ901,PQ902,PQ905 TPCA8065	201109/27	B test
9	for CPU_CORE test	59	Reserve PC77,PC78	201109/27	B test
10	for VGA VID R-short	59	change PR318,PR319,PR320,PR321,PR322,PR323 footprint	201205/31	B test
11	Charger boost resistor For EMI	63	Change PR385 from 2.2ohm to 4.7ohm	201206/04	B test
12					
13					
14					
15					
16					
17					

QIWY3 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
				EVT TO DVT
1		P7	Reserve R64	Reserve EC DRAMRST control pin for Deep S3
2		P16	Reserve R1457,R1455,R1447	Reserve SUSACK#,SUSWARN#,SLP_SUS# control signal for Deep S3
3		P16	Reserve Q118,R1120,R1121	Reverse SLP_SUS# to control +3V_PCH&+5V_PCH
4		P16	Change AC_PRESENT Pull high source to +3V_DSW	For Deep S3 function
5		P21	Remove R289	+5V_PCH control circuit change for Deep S3
6		P36	Reserve J8,Q104,C533,C526,R436	Reserve for AOAC function
7		P36	Change JP1 pin2,24,52 power source to +3VS_WLAN_AOAC	Reserve for AOAC function
8		P42	Change EC GPIO pin setting (Impact pin 18,71,72,126,128)	For DeepS3/AOAC function
9		P48	Reserve J11,J14,Q148,Q149,C38,C39	+3V_PCH&+5V_PCH control circuit for Deep S3
10		P45	change U49 symbol (without GND pad)	For DFx issue
11		P46	change U40,U69 symbol (without GND pad)	For DFx issue
12		P47	change JP10 type to SP01001B800	For DFx issue
13		P19	Reserve R207,R224 to contact WLAN wake even	Reserve for AOAC function
14		P41	Change JSPK1 type to SP02000H700	For DFx issue
14		P19	Reserve R704 and R706 for GPIO69 PU&PD	For SKU ID
15		P23	Change CV37,CV38 to 22P	For Crystal EA request
16		P37	Change C968,C969 to 33P	For Crystal EA request

Title			
PIR (HW)			
Size: Custom	Document Number: LA-8692P		Rev: 0.2
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