Compal Confidential

QCL70 MB Schematic Document

LA-8222P

Rev: 1.0

2012.01.09

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QCL70

ZZZ1
PCB-MB
PCB P/N for Load BOM
DAZ0NE00100

NV N13P-GL / GS (N13M-GE1)
Page 20 ~ 29

PEG 16X

Mobile
Ivy Bridge
Processor
rPGA 988B Socket
Page 4 ~ 9
+VCC_CORE, +VCCP, +VCC_GFXCORE_AVG, +1.5V_CPU_VDDQ, +1.8VS, _VCCSA

DDR3 1333/1600MHz 1.5V
Dual Channel

DDR3-SO-DIMM X 2
BANK 0, 1, 2, 3
+1.5V, +0.75VS
Page 10, 11

FDI x8 (UMA) 100MHz 2.7GT/s

DMI x4 100MHz 5GB/s

Intel PANTHER-POINT PCH
HM76/HM75
FCBGA 989 Balls
Page 12 ~ 19
+1.05VS, +1.8VS, +3VS, +3V_PCH, +5V_PCH, +RTCVCC, +VCCAFDI_VRM

LCD conn
Page 30
LVDS, EDID, DISPOFF#, PWM

CRT Conn
Page 30
RGB, HV Sync, DDC

HDMI
Page 35
HDMI, DDC

USB2.0
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port 3 — Camera Page 30
port 4 — Card Reader RTS5137 Page 34 → Memory Card Slot SD/MMC Page 34
port 10 — MiniCard-2 Page 41

USB3.0
port 0,2 / port 1,3 — USB3.0 conn x2 Page 37

Azalia
Realtek ALC269 Page 33
→ Audio Jack (HP) Page 33
→ Audio Jack (MIC) Page 33
→ Speaker Connector Page 33

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port 0 — 2.5" SATA HDD Connector Page 31
port 1 — 2.5" SATA HDD Connector Page 31
port 2 — SATA ODD Connector Page 31

PCI-e
port 1 — LAN/CRT Board 10/100/1000 LAN Realtek GbE RTL8111F Page 32
port 2 — Mini Card-1 WLAN Bluetooth Page 41

SPI
SPI ROM 4MB For win7 8MB For win8 Page 12

LPC BUS

ENE KB9012QF
Reserve KB930QF
+3VLP/+3VALW
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Touch Pad CONN. Page 39

Int. KBD Page 39

SPI ROM 128KB Page 40

DC/DC Interface CKT. Page 29,42

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X76@:

VRAMX16X8 ZZZ X76L01@ 2G SAM ZZZ2 X76L02@ 2G B HYN ZZZ5 X76L05@ 1G SAM ZZZ6 X76L06@ 1G HYN	**HYN 128*16*8** ZZZ3 X76L15@ 2G D HYN	
VRAMX16X8-GS ZZZ11 X76L12@ GS 2G SAM ZZZ12 X76L11@ GS 2G HYN	**N13P-GS** **GS@** U10 GS@ N13P-GS	**N13P-GL** **GL@** U10 GL@ N13P-GL
GEL@: N13M-GE1 or N13P-GL **GS@:** N13P-GS **DIS@:** VGA componet **9012@:** EC(ENE 9012 chip) **XDP@:** Intel debug port **930@:** EC(ENE 930 chip) **IU3@:** USB3.0 by PCH **USB30@:** USB3.0 controller IC **AI@:** AI Charger **NAI@:** Non AI Charger	**N13M-GE1** **GE@** U10 GE@ N13M-GE1	**N13M-GE1 x8** **GE8@** U10 GE8@ N13M-GE1 x8
W7@: WIN7 **W8@:** WIN8	**PS8520** ZZZ9 PAR8520@ PS8520	**ASM1466** ZZZ10 ASM1466@ ASM1466

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	LPC Debug Port
PCI4	None

	USB3 PORT	DESTINATION
PCH	1	USB2.0+3.0
	2	USB2.0+3.0
	3	None
	4	None

	USB2 PORT	DESTINATION
PCH	0	USB2.0+3.0
	1	USB2.0+3.0
	2	USB2
	3	CAMERA
	4	Card Reader
	5	USB2
	6	None
	7	None
	8	None
	9	None
	10	JMINI1 (WLAN) Bluetooth
	11	None
	12	None
	13	None

Voltage Rails

Power Plane	Description	S1	S3	Deep S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+3VLP	3.3V power rail for 51ON power management	ON	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+LAN_IO	3.3V power rail for ethernet	ON	ON	OFF	OFF
+3VS_WLAN	3.3V power rail for WLAN/BT Combo	ON	OFF	OFF	OFF
+3V_PCH	3.3V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+3VS	3.3V power rail for DDR SPI,PCH,HDD,Audio,Card Reader	ON	OFF	OFF	OFF
+3VSG	3.3V power rail for VGA	ON	OFF	OFF	OFF
+LCDVDD	3.3V power rail for LCD	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+5V_PCH	5V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+5VS	5V power rail for HDD,AUDIO,FAN,Touch PAD	ON	OFF	OFF	OFF
+5VS_ODD	5V power rail for SATA ODD	ON	OFF	OFF	OFF
+1.8VS	1.8V power rail for CPU,PCH	ON	OFF	OFF	OFF
+1.05VS	1.05V power rail for PCH	ON	OFF	OFF	OFF
+VCCP	1.05V power rail for CPU VCCIO,PCH	ON	OFF	OFF	OFF
+1.05VSG	1.05V power rail for N13P	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR3 system memory	ON	ON	ON	OFF
+1.5V_CPU_VDDQ	1.5V power rail CPU VDDQ	ON	OFF	OFF	OFF
+1.5VSG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+1.5VS	1.5V power rail for PCH,WLAN/BT combo	ON	OFF	OFF	OFF
+0.75VS	0.75V power rail for DDR VREF	ON	OFF	OFF	OFF
+VCCSA	VCCSA for CPU system agent	ON	OFF	OFF	OFF
+VCC_CORE	CORE Voltage for CPU	ON	OFF	OFF	OFF
+VCC_GFXCORE_AXG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+VGA_CORE	CORE Voltage for N13P Graphics ON OFF OFF	ON	OFF	OFF	OFF

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD WLAN
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

SMBUS Control Table

	SOURCE	MINI1	BATT	PCH	EC	SODIMM	DGPU
EC_SMB_CK1 EC_SMB_DA1	KB930	X	**V**	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	**V**	X	X	**V**
PCH_SMBCLK PCH_SMBDATA	PCH	**V**	X	X	X	**V**	X
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	**V**	X	**V**

SATA	DESTINATION
SATA0	HDD
SATA1	HDD
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLK	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	CLK_SD_48M
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :

: means Digital Ground

: means Analog Ground

QCL70 * 16 (LA8222P)
Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board Id	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
	33K +/- 5%	0.634 V	0.819V	0.945 V

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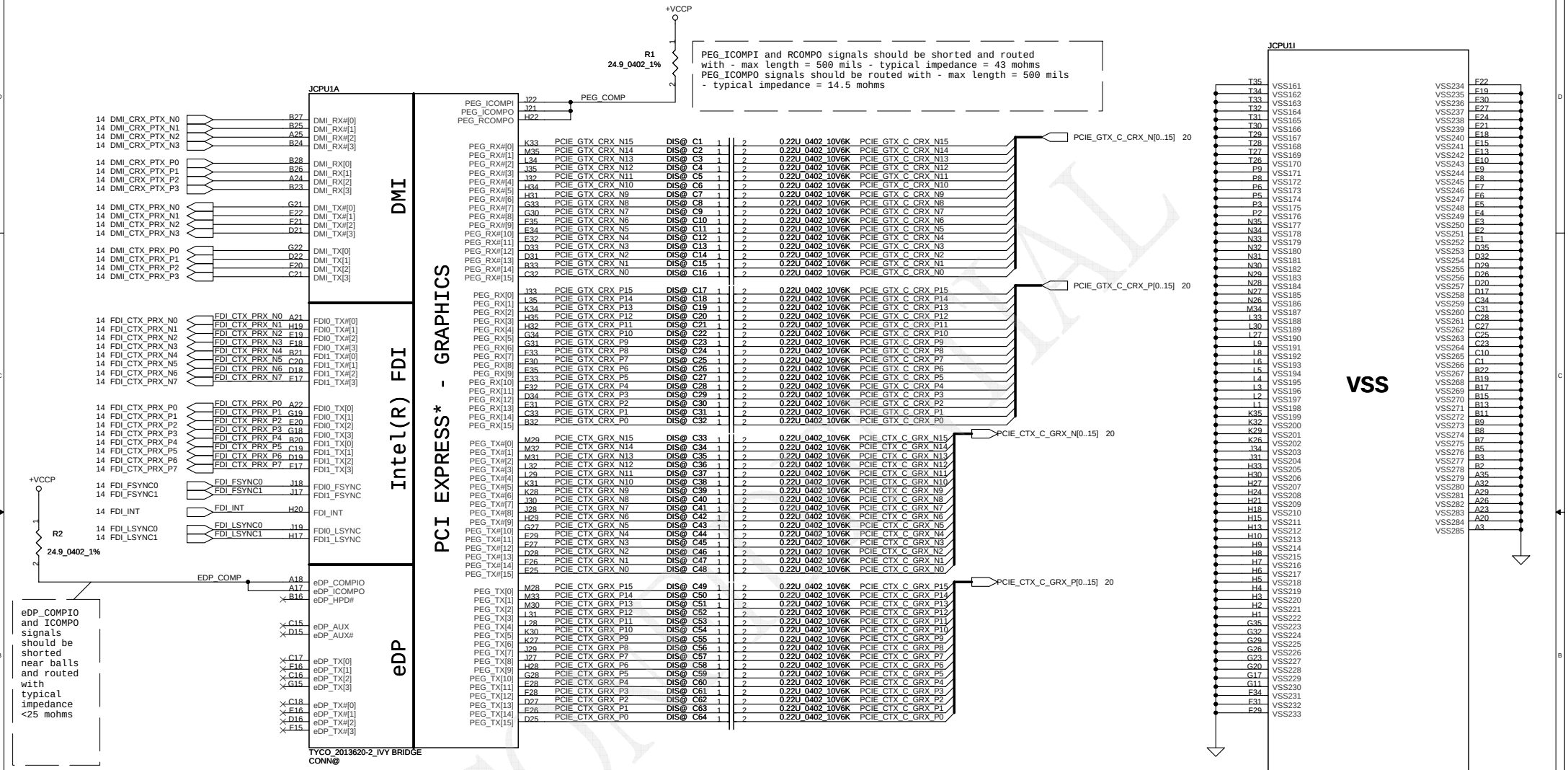

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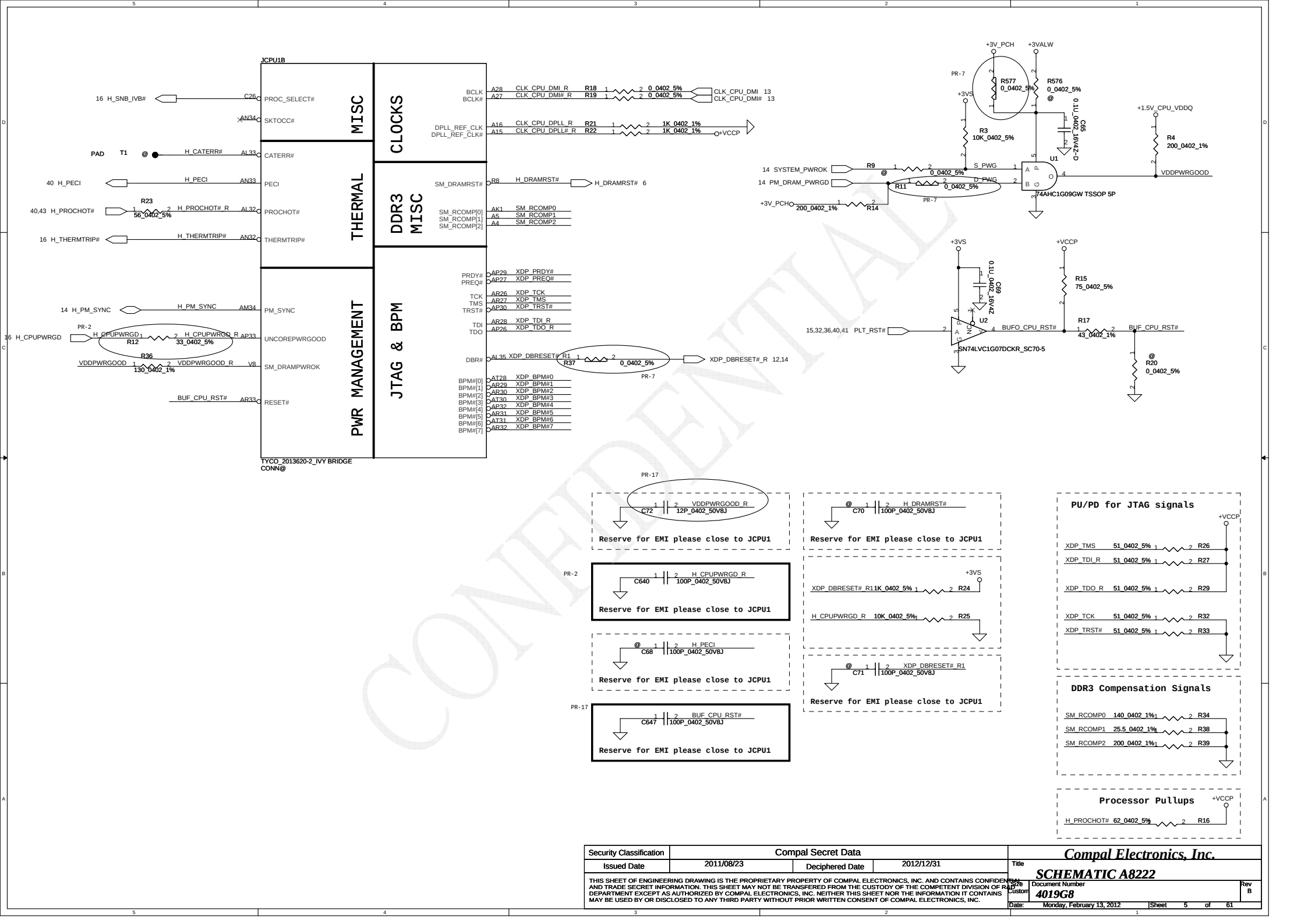

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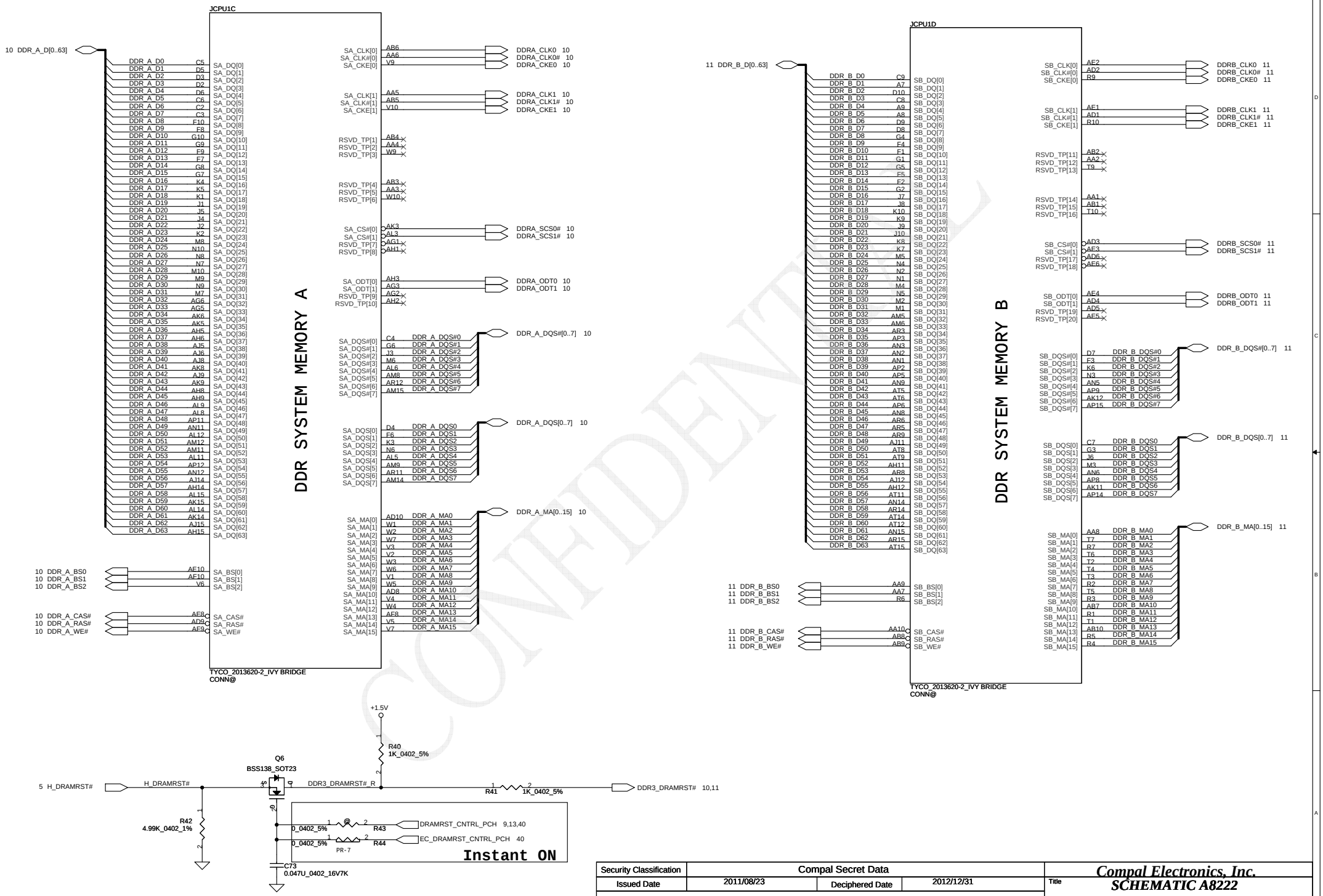

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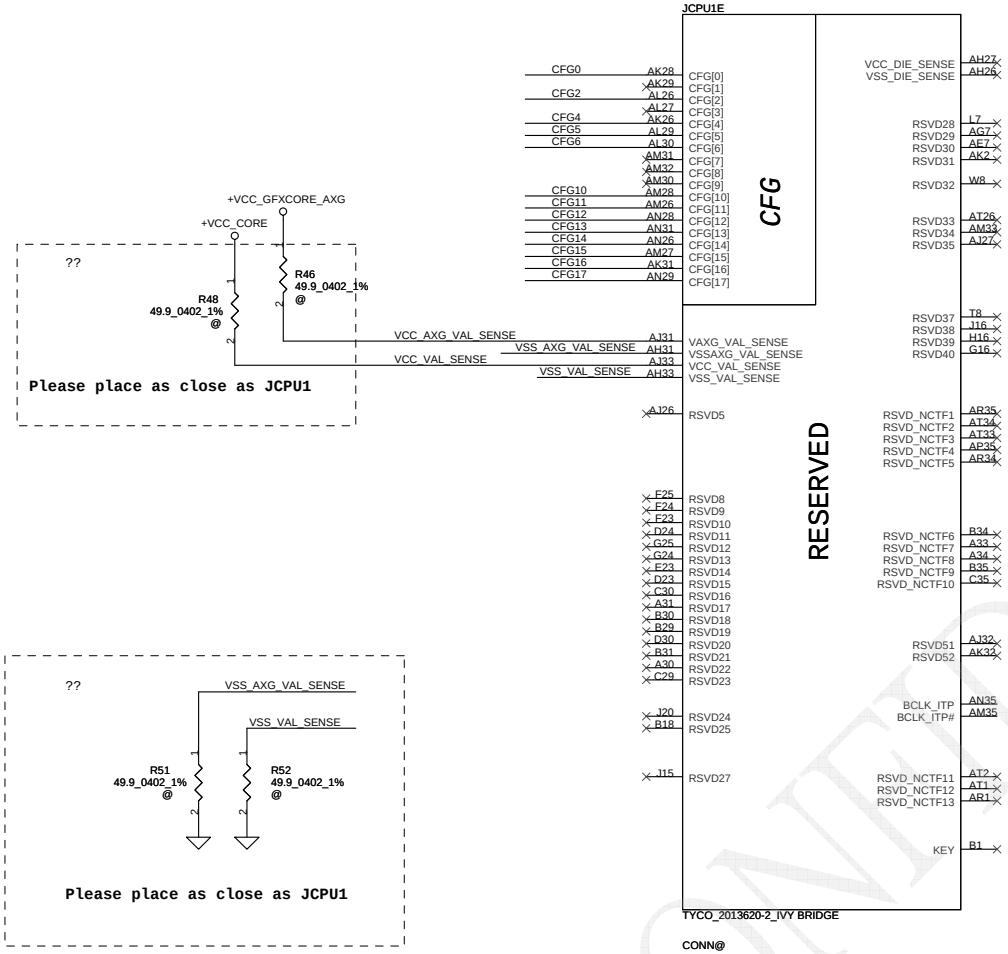
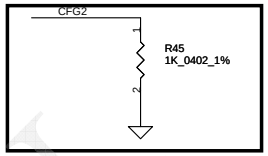
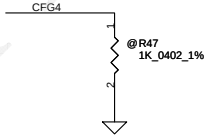


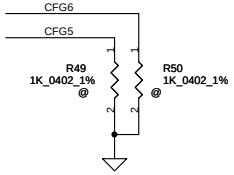
CFG Straps for Processor



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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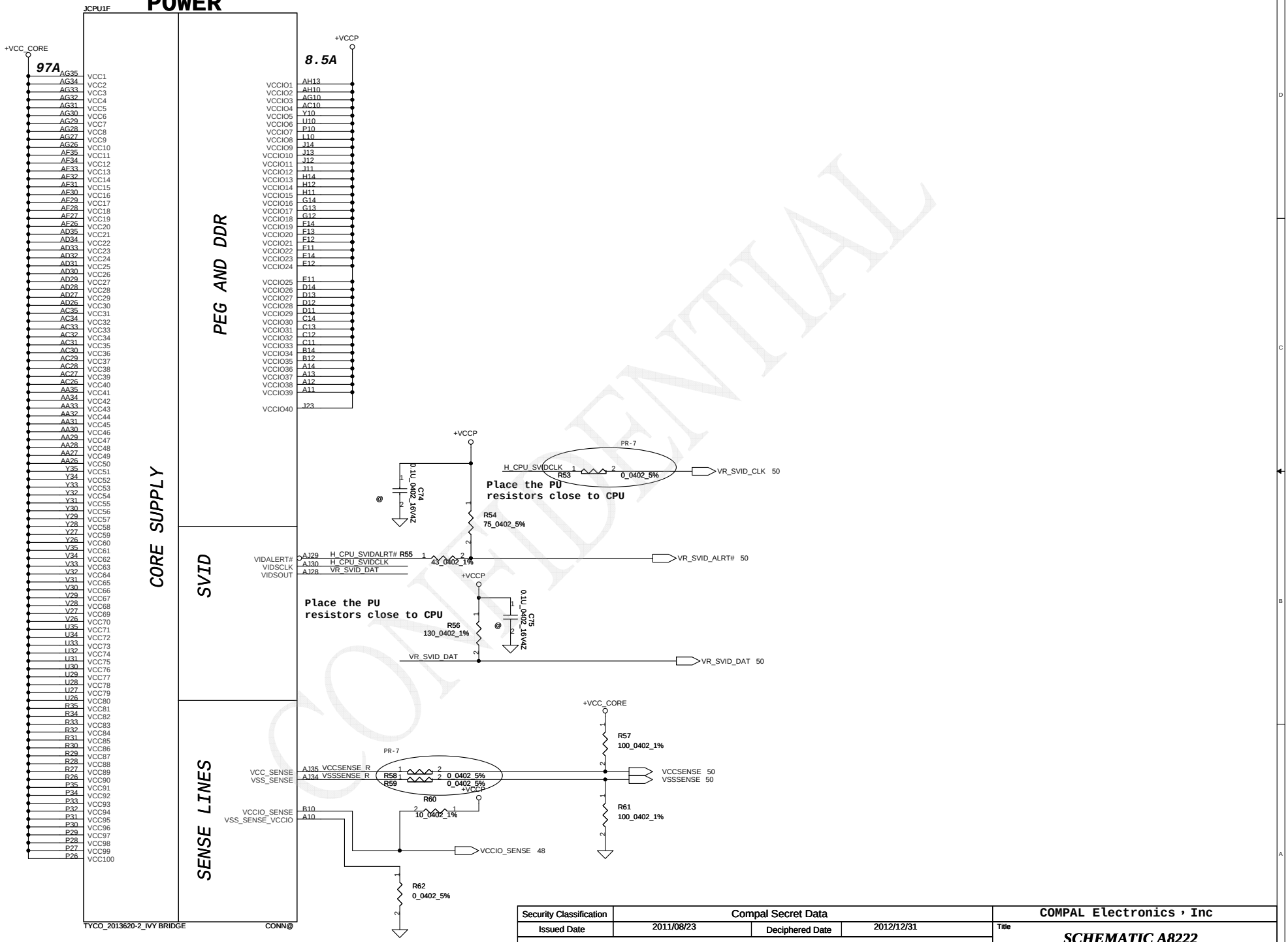
POWER



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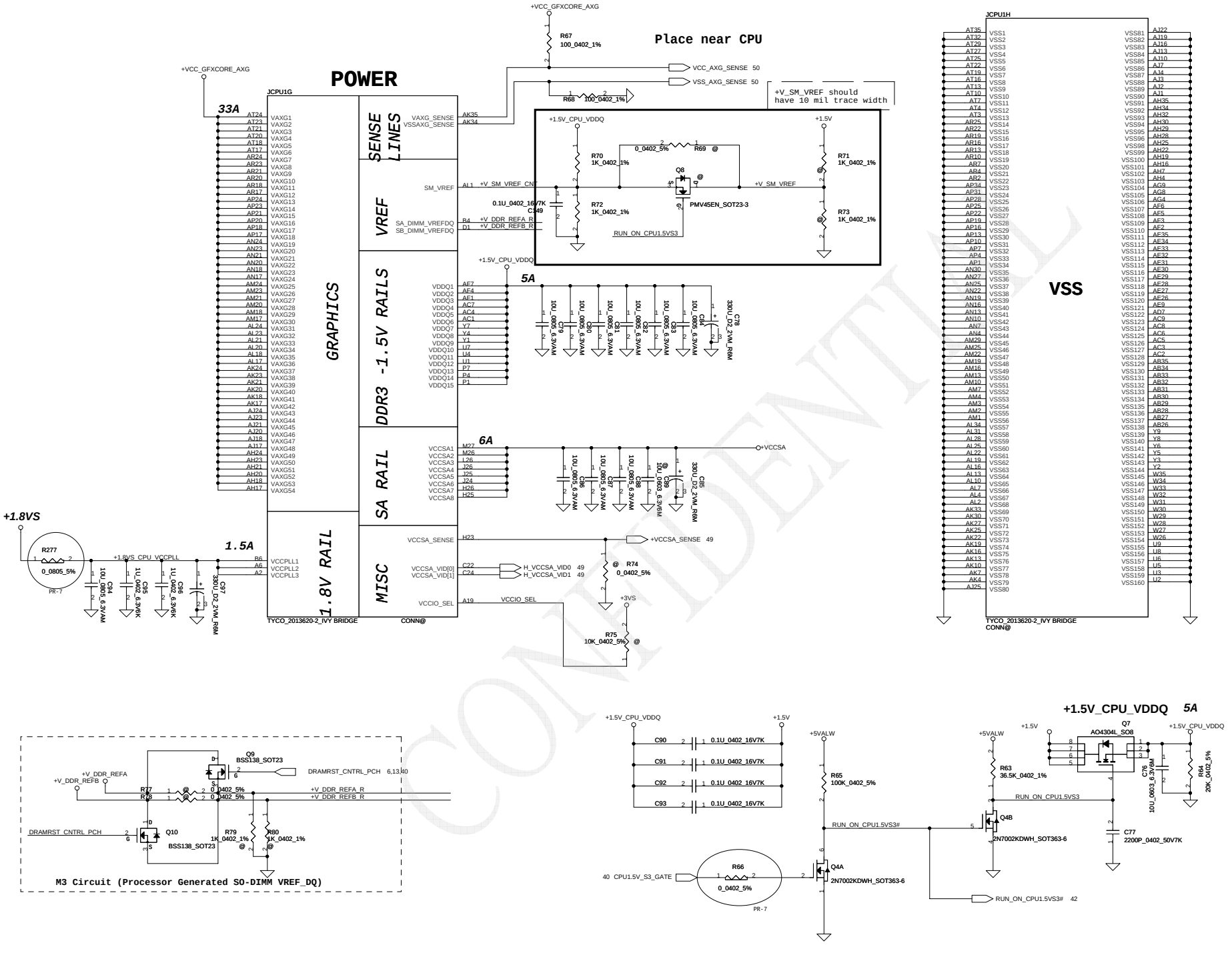

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3.56A

DDR3 SO-DIMM A

JDIMM1

+1.5V

R81 1K_0402_1%

+V_DDR_REFA

R82 1K_0402_1%

C98 0.1U_0402_10V6K

C99 2.2U_0402_6.3V6M

6 DDR_A_D[0..63]
6 DDR_A_DQS[0..7]
6 DDR_A_DQS#[0..7]
6 DDR_A_MA[0..15]

	VREF_DQ	1	2	VSS1	DDR_A_D4
	VSS2	3	4	DQ4	DDR_A_D5
DDR_A_D0	DQ0	5	6	DQ5	
DDR_A_D1	DQ1	7	8	VSS3	DDR_A_DQS#0
	VSS4	9	10	DQS#0	DDR_A_DQS0
	DM0	11	12	DQS0	
DDR_A_D2	VSS5	13	14	VSS6	DDR_A_D6
DDR_A_D3	DQ2	15	16	DQ6	DDR_A_D7
	DQ3	17	18	DQ7	
DDR_A_D8	VSS7	19	20	VSS8	DDR_A_D12
DDR_A_D9	DQ8	21	22	DQ12	DDR_A_D13
	DQ9	23	24	DQ13	
DDR_A_DQS#1	VSS9	25	26	VSS10	
DDR_A_DQS1	DQS#1	27	28	DM1	
	DQS1	29	30	RESET#	DDR3_DRAMRST#
DDR_A_D10	VSS11	31	32	VSS12	DDR_A_D14
DDR_A_D11	DQ10	33	34	DQ14	DDR_A_D15
	DQ11	35	36	DQ15	
DDR_A_D16	VSS13	37	38	VSS14	
DDR_A_D17	DQ16	39	40	DQ20	DDR_A_D20
	DQ17	41	42	DQ21	DDR_A_D21
DDR_A_DQS#2	VSS15	43	44	VSS16	
DDR_A_DQS2	DQS#2	45	46	DM2	
	DQS2	47	48	VSS17	
DDR_A_D18	VSS18	49	50	DQ22	DDR_A_D22
DDR_A_D19	DQ18	51	52	DQ23	DDR_A_D23
	DQ19	53	54	VSS19	
DDR_A_D24	VSS20	55	56	DQ28	DDR_A_D28
DDR_A_D25	DQ24	57	58	DQ29	DDR_A_D29
	DQ25	59	60	VSS21	
	VSS22	61	62	DQS#3	DDR_A_DQS#3
	DM3	63	64	DQS3	DDR_A_DQS3
	VSS23	65	66	VSS24	
DDR_A_D26	DQ26	67	68	DQ30	DDR_A_D30
DDR_A_D27	DQ27	69	70	DQ31	DDR_A_D31
	VSS25	71	72	VSS26	
6 DDRA_CKE0	DDRA_CKE0	73	74	CKE1	DDRA_CKE1 DDRA_CKE1 6
	CKE0	75	76	VDD2	
	VDD1	77	78	A15	DDR_A_MA15
6 DDR_A_BS2	NC1	79	80	A14	DDR_A_MA14
	BA2	81	82	VDD4	
DDR_A_MA12	VDD3	83	84	A11	DDR_A_MA11
DDR_A_MA9	A12/BC#	85	86	A7	DDR_A_MA7
	A9	87	88	VDD6	
DDR_A_MA8	VDD5	89	90	A6	DDR_A_MA6
DDR_A_MA5	A8	91	92	A4	DDR_A_MA4
	A5	93	94	VDD8	
DDR_A_MA3	VDD7	95	96	A2	DDR_A_MA2
DDR_A_MA1	A3	97	98	A0	DDR_A_MA0
	A1	99	100	VDD10	
6 DDRA_CLK0	VDD9	101	102	CK1	DDRA_CLK1 DDRA_CLK1 6
6 DDRA_CLK0#	CK0	103	104	CK1#	DDRA_CLK1# DDRA_CLK1# 6
	CK0#	105	106	VDD12	
DDR_A_MA10	VDD11	107	108	BA1	DDR_A_BS1 DDR_A_BS1 6
6 DDR_A_BS0	A10/AP	109	110	RAS#	DDR_A_RAS# DDR_A_RAS# 6
	BA0	111	112	VDD14	
6 DDR_A_WE#	VDD13	113	114	S0#	DDRA_SCS0# DDRA_SCS0# 6
6 DDR_A_CAS#	WE#	115	116	ODT0	DDRA_ODT0 DDRA_ODT0 6
	CAS#	117	118	VDD16	
DDR_A_MA13	VDD15	119	120	ODT1	DDRA_ODT1 DDRA_ODT1 6
6 DDRA_SCS1#	A13	121	122	NC2	
	S1#	123	124	VDD18	
	VDD17	125	126	VREF_CA	+VREF_CA
	NCTEST	127	128	VSS28	
DDR_A_D32	VSS27	129	130	DQ36	DDR_A_D36
DDR_A_D33	DQ32	131	132	DQ37	DDR_A_D37
	DQ33	133	134	VSS30	
DDR_A_DQS#4	VSS29	135	136	DM4	
DDR_A_DQS4	DQS#4	137	138	VSS31	
	DQS4	139	140	DQ38	DDR_A_D38
DDR_A_D34	VSS32	141	142	DQ39	DDR_A_D39
DDR_A_D35	DQ34	143	144	VSS33	
	DQ35	145	146	DQ44	DDR_A_D44
DDR_A_D40	VSS34	147	148	DQ45	DDR_A_D45
DDR_A_D41	DQ40	149	150	VSS35	
	DQ41	151	152	DQS#5	DDR_A_DQS#5
	VSS36	153	154	DQS5	DDR_A_DQS5
	DQS#5	155	156	VSS38	
	DM5	157	158	DQ46	DDR_A_D46
DDR_A_D42	VSS37	159	160	DQ47	DDR_A_D47
DDR_A_D43	DQ42	161	162	VSS40	
	DQ43	163	164	DQ52	DDR_A_D52
DDR_A_D48	VSS39	165	166	DQ53	DDR_A_D53
DDR_A_D49	DQ48	167	168	VSS42	
	DQ49	169	170	DM6	
DDR_A_DQS#6	VSS41	171	172	VSS43	
DDR_A_DQS6	DQS#6	173	174	DQ54	DDR_A_D54
	DQS6	175	176	DQ55	DDR_A_D55
DDR_A_D50	VSS44	177	178	VSS45	
DDR_A_D51	DQ50	179	180	DQ60	DDR_A_D60
	DQ51	181	182	DQ61	DDR_A_D61
DDR_A_D56	VSS46	183	184	VSS47	
DDR_A_D57	DQ56	185	186	DQS#7	DDR_A_DQS#7
	DQ57	187	188	DQS7	DDR_A_DQS7
	VSS48	189	190	VSS50	
DDR_A_D58	DM7	191	192	DQ62	DDR_A_D62
DDR_A_D59	VSS49	193	194	DQ63	DDR_A_D63
	DQ58	195	196	VSS52	
	DQ59	197	198	EVENT#	
	VSS51	199	200	SDA	PCH_SMBDATA PCH_SMBDATA 11,13,39,41
	SA0	201	202	SCL	PCH_SMBCLK PCH_SMBCLK 11,13,39,41
	VDDSPD	203	204	VTT2	+0.75VS
	SA1	205	206	G2	
	VTT1				
	G1				

TYCO_2-1932323-1_204P
CONN@

+3VS

C119 0.1U_0402_10V6K
C153 2.2U_0402_6.3V6M
R85 10K_0402_5%
R86 10K_0402_5%

C109 0.1U_0402_10V6K
C109 2.2U_0402_6.3V6M
R83 1K_0402_1%
R84 1K_0402_1%

0.65A@0.75V

9.2H

Layout Note: Place near JDIMM1

C100 330U_B2_2.5VM_R15M
C101 10U_0603_6.3V6M
C102 10U_0603_6.3V6M
C103 10U_0603_6.3V6M
C104 10U_0603_6.3V6M
C105 10U_0603_6.3V6M
C106 10U_0603_6.3V6M
C107 @ 10U_0603_6.3V6M

Layout Note: Place these 4 Caps near Command and Control signals of JDIMM1

C110 1U_0402_6.3V6K
C111 1U_0402_6.3V6K
C112 1U_0402_6.3V6K
C113 1U_0402_6.3V6K

Layout Note: Place near JDIMM1.203,204

C114 1U_0402_6.3V6K
C115 1U_0402_6.3V6K
C116 1U_0402_6.3V6K
C117 1U_0402_6.3V6K

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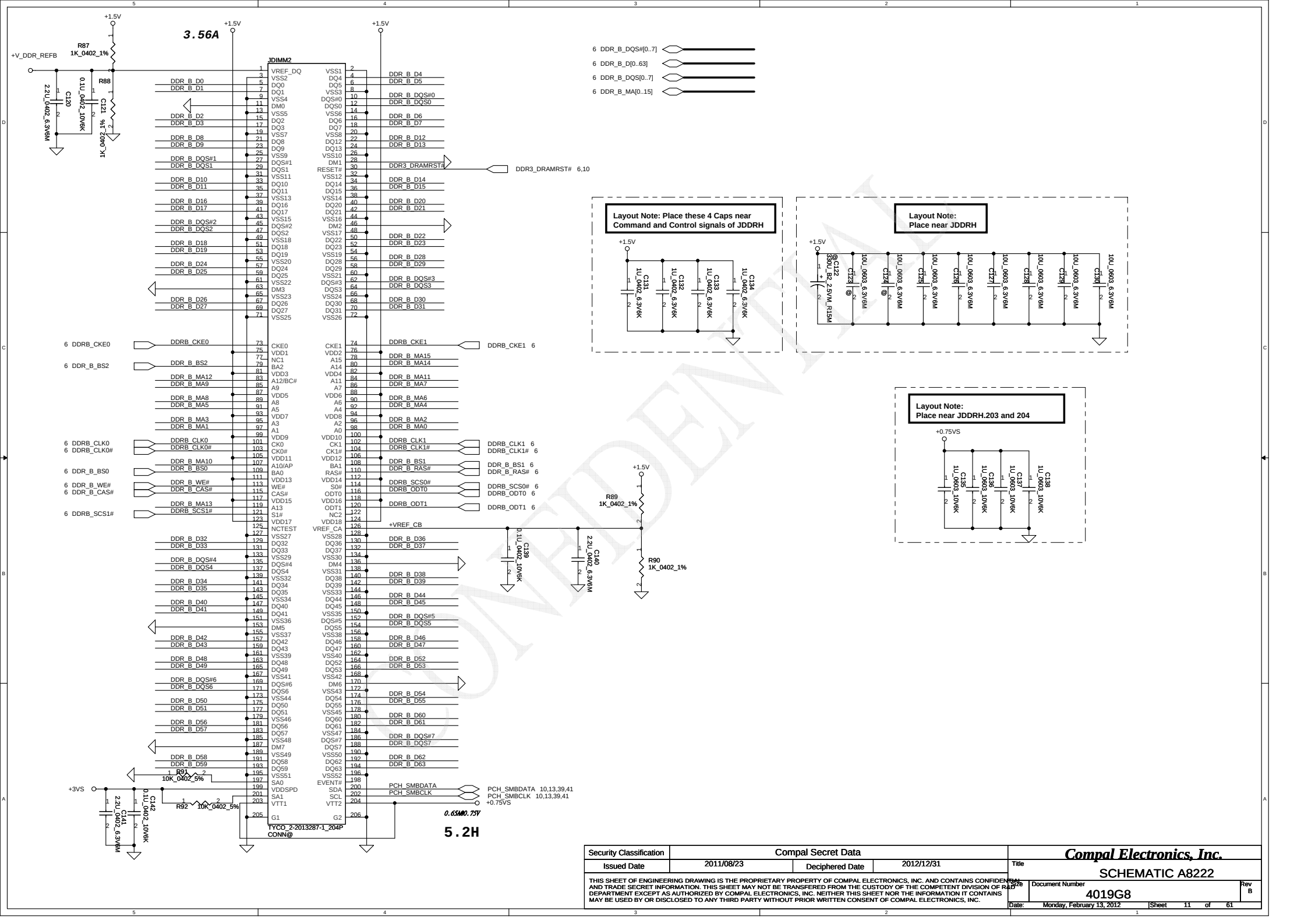

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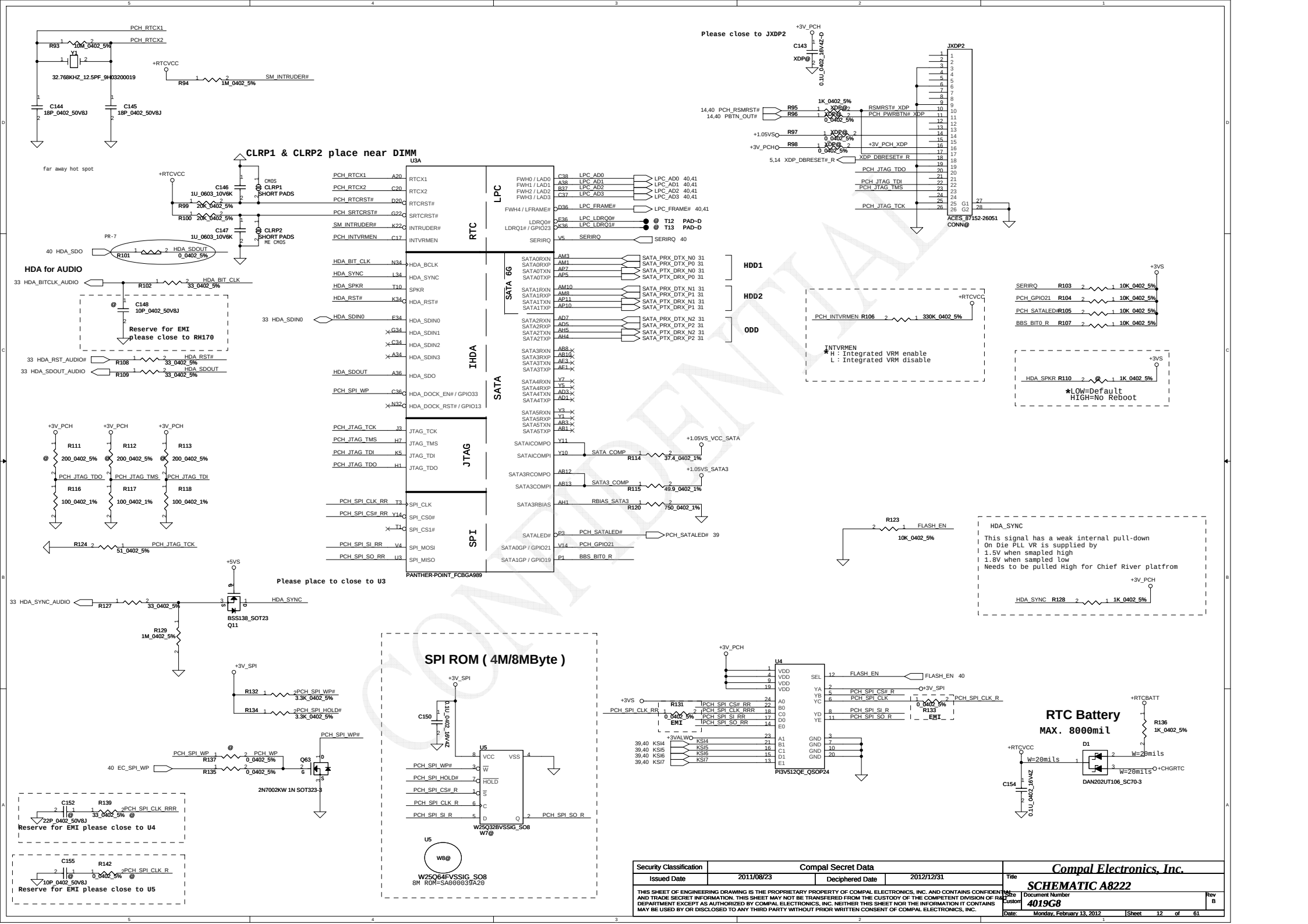

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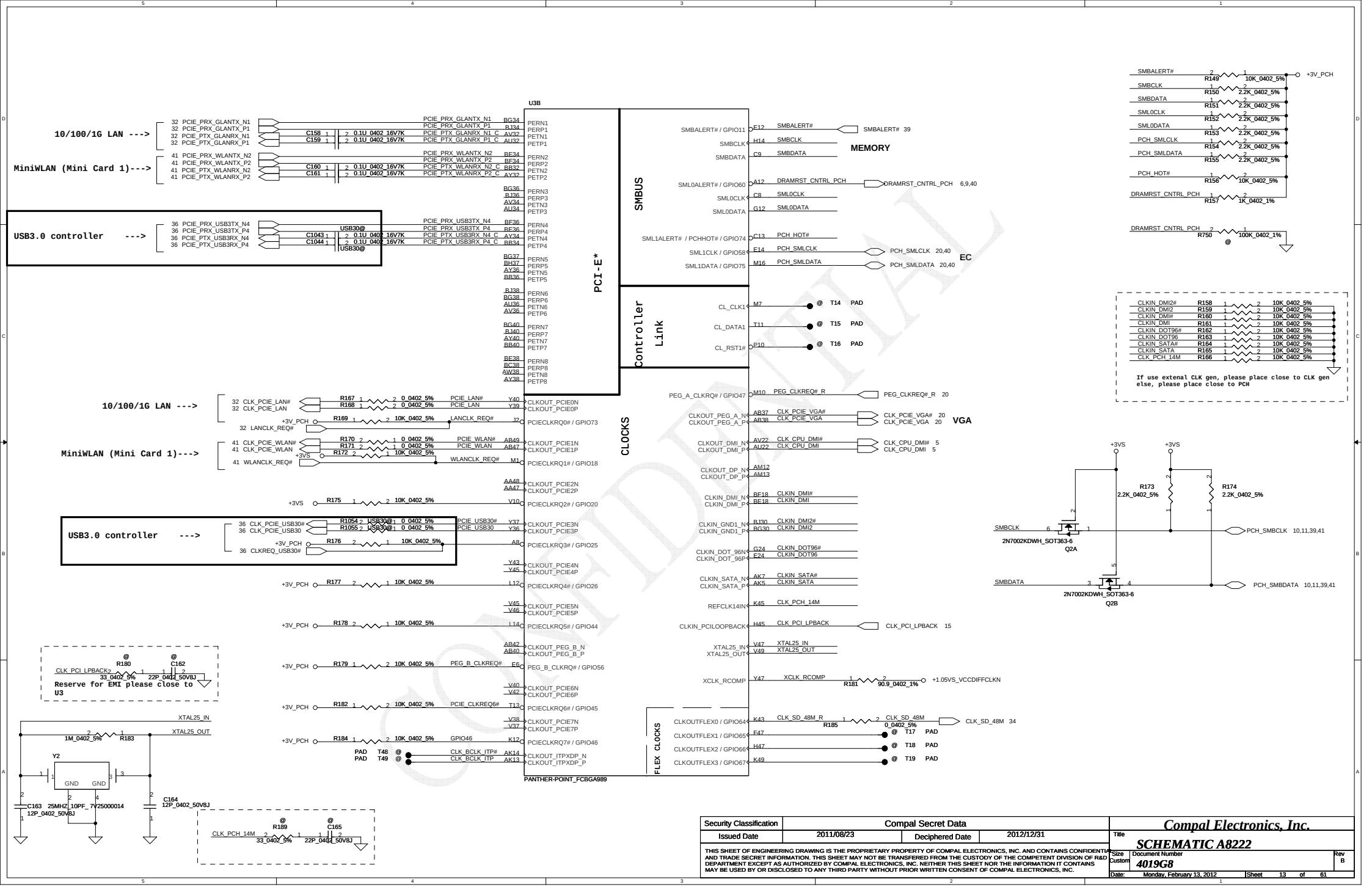

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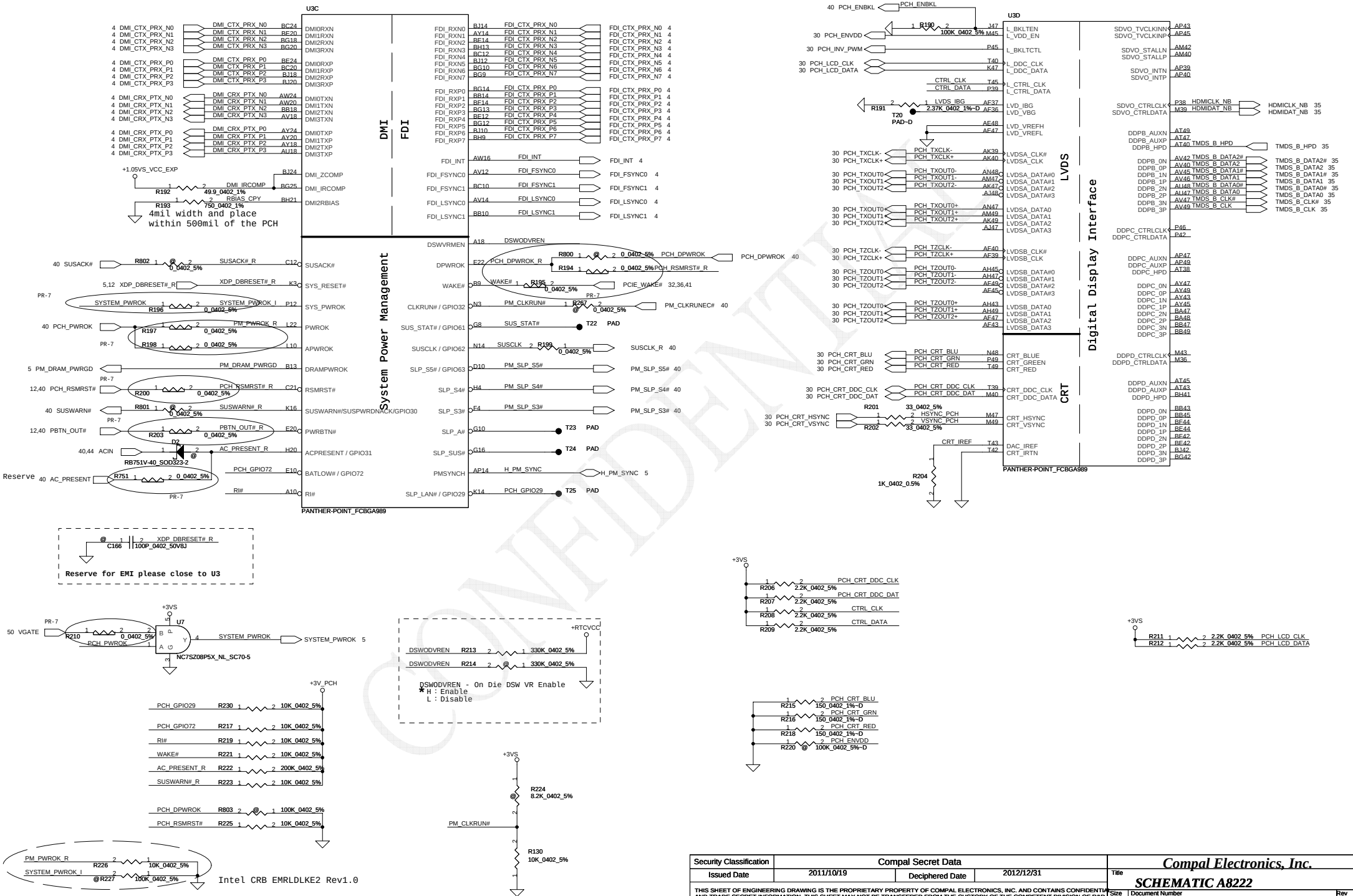

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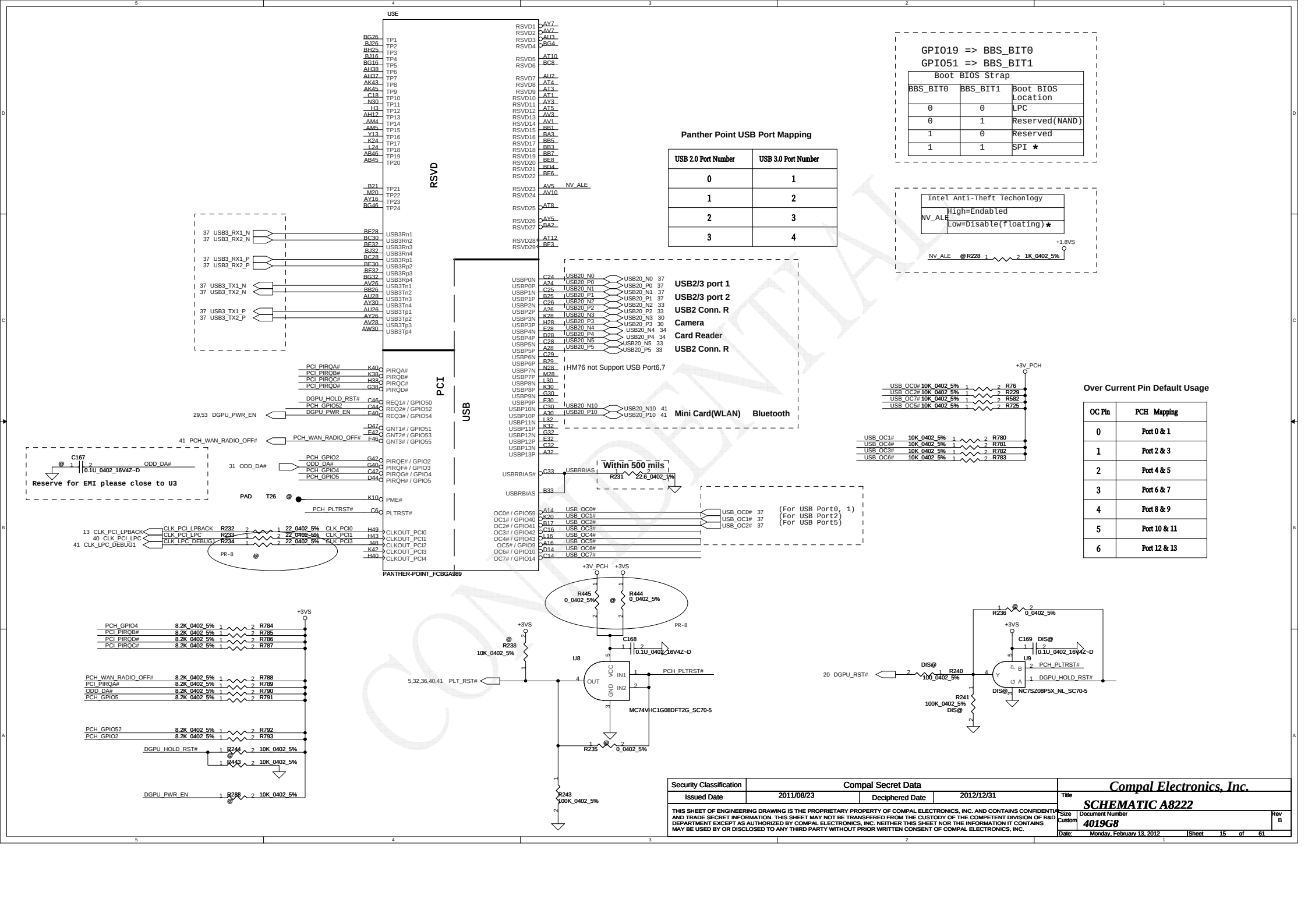

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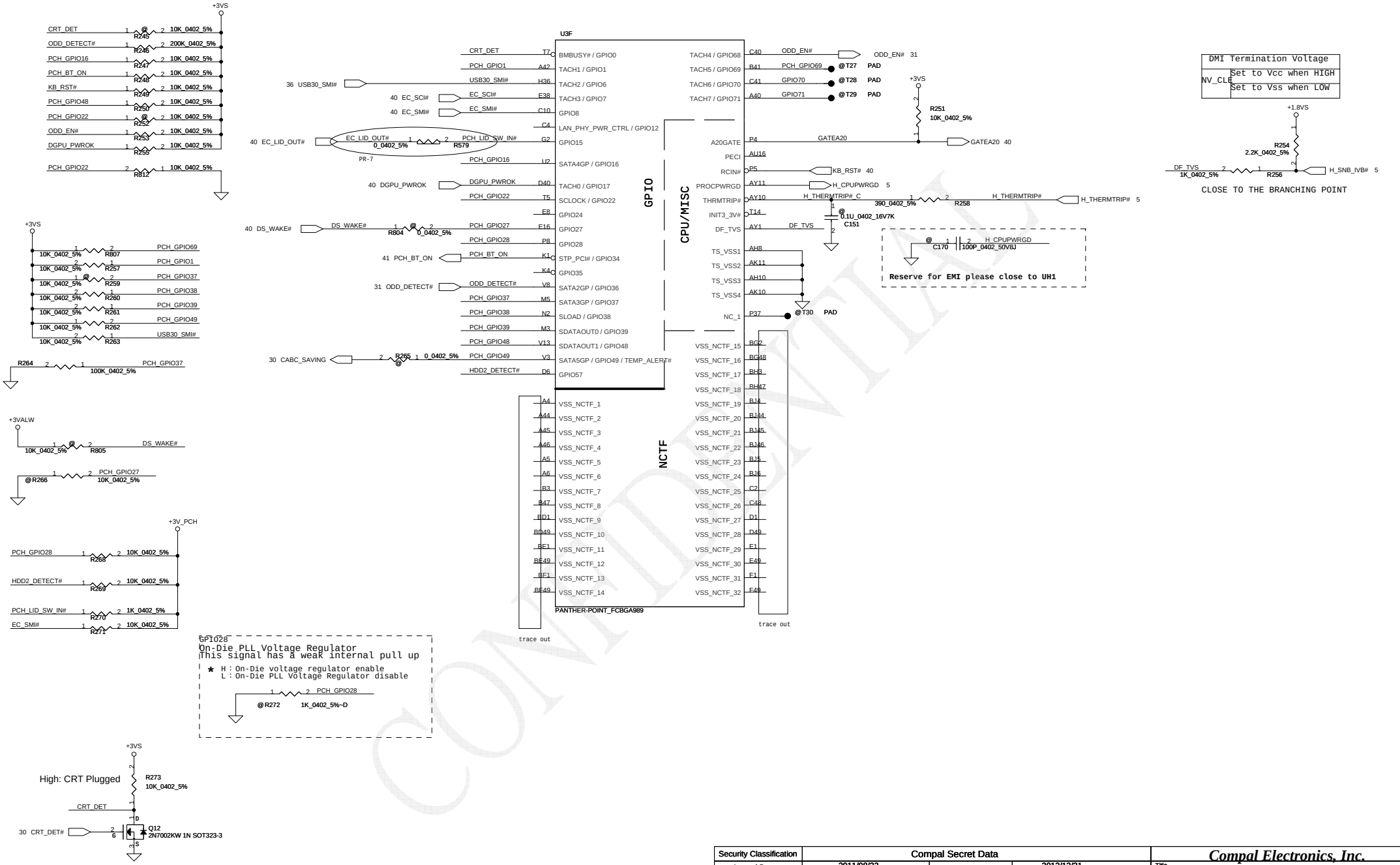

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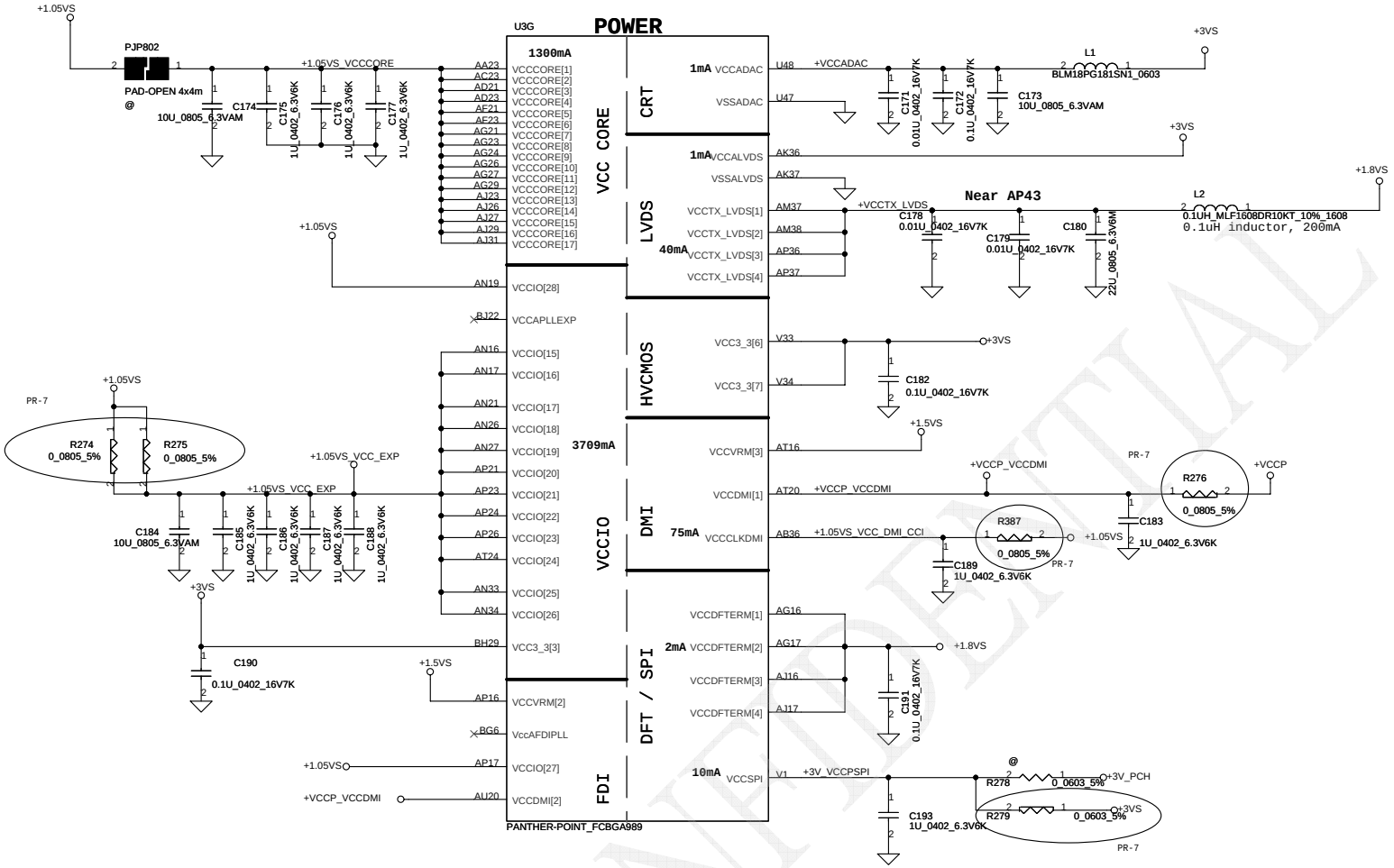

PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

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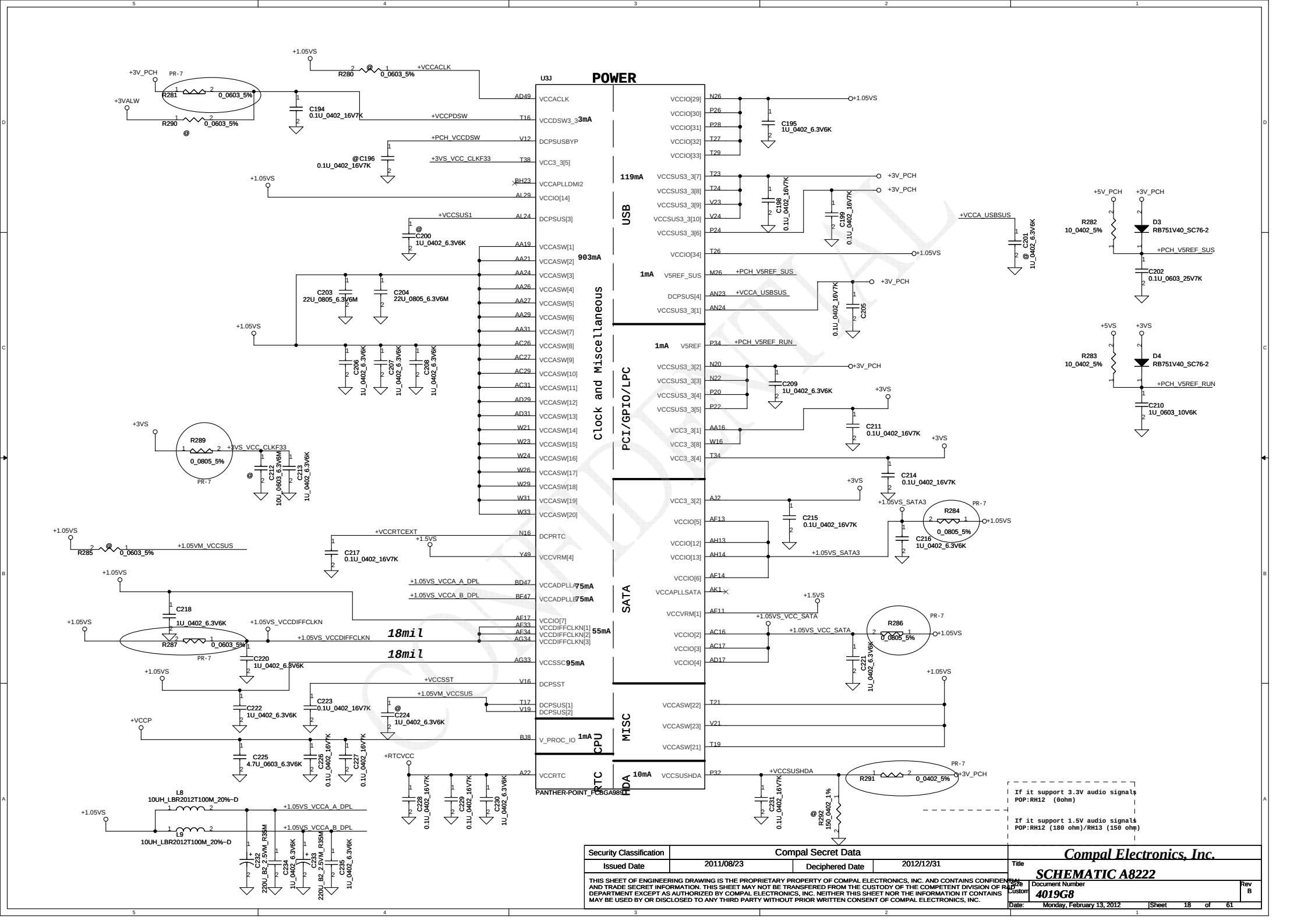

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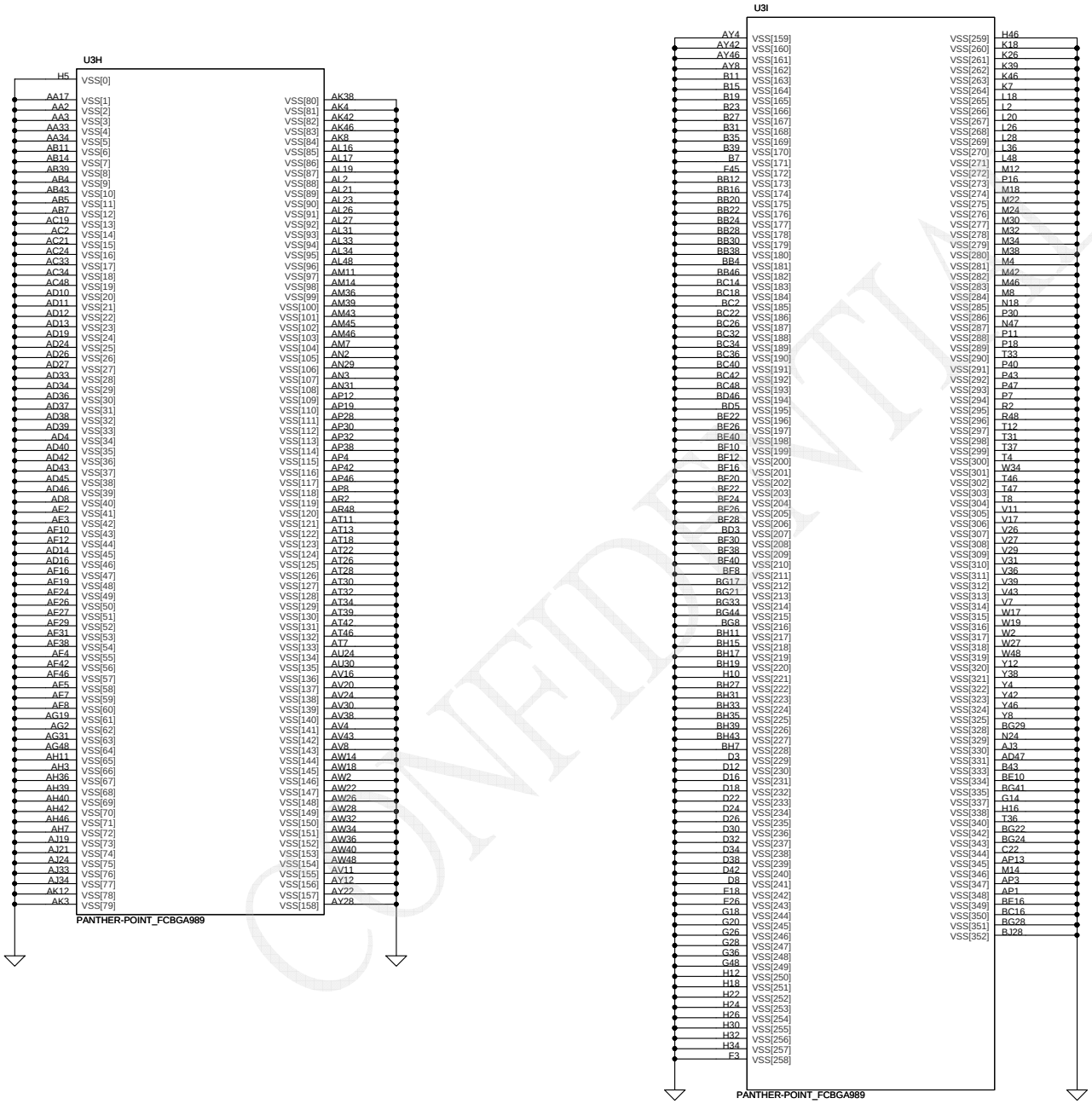

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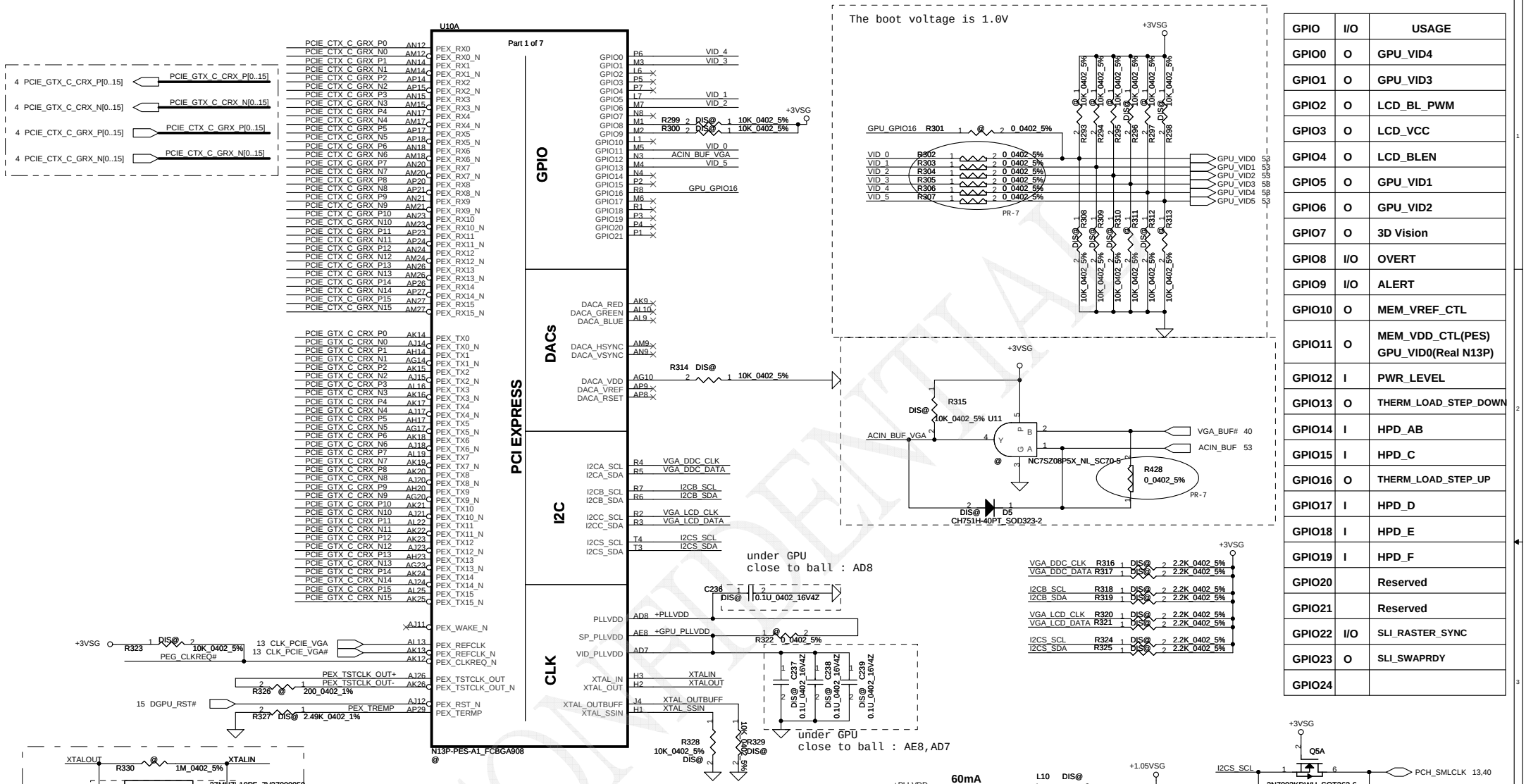

GPIO	I/O	USAGE
GPIO0	O	GPU_VID4
GPIO1	O	GPU_VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	GPU_VID1
GPIO6	O	GPU_VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	MEM_VDD_CTL(PES) GPU_VID0(Real N13P)
GPIO12	I	PWR_LEVEL
GPIO13	O	THERM_LOAD_STEP_DOWN
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	THERM_LOAD_STEP_UP
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved
GPIO22	I/O	SLI_RASTER_SYNC
GPIO23	O	SLI_SWAPRDY
GPIO24		

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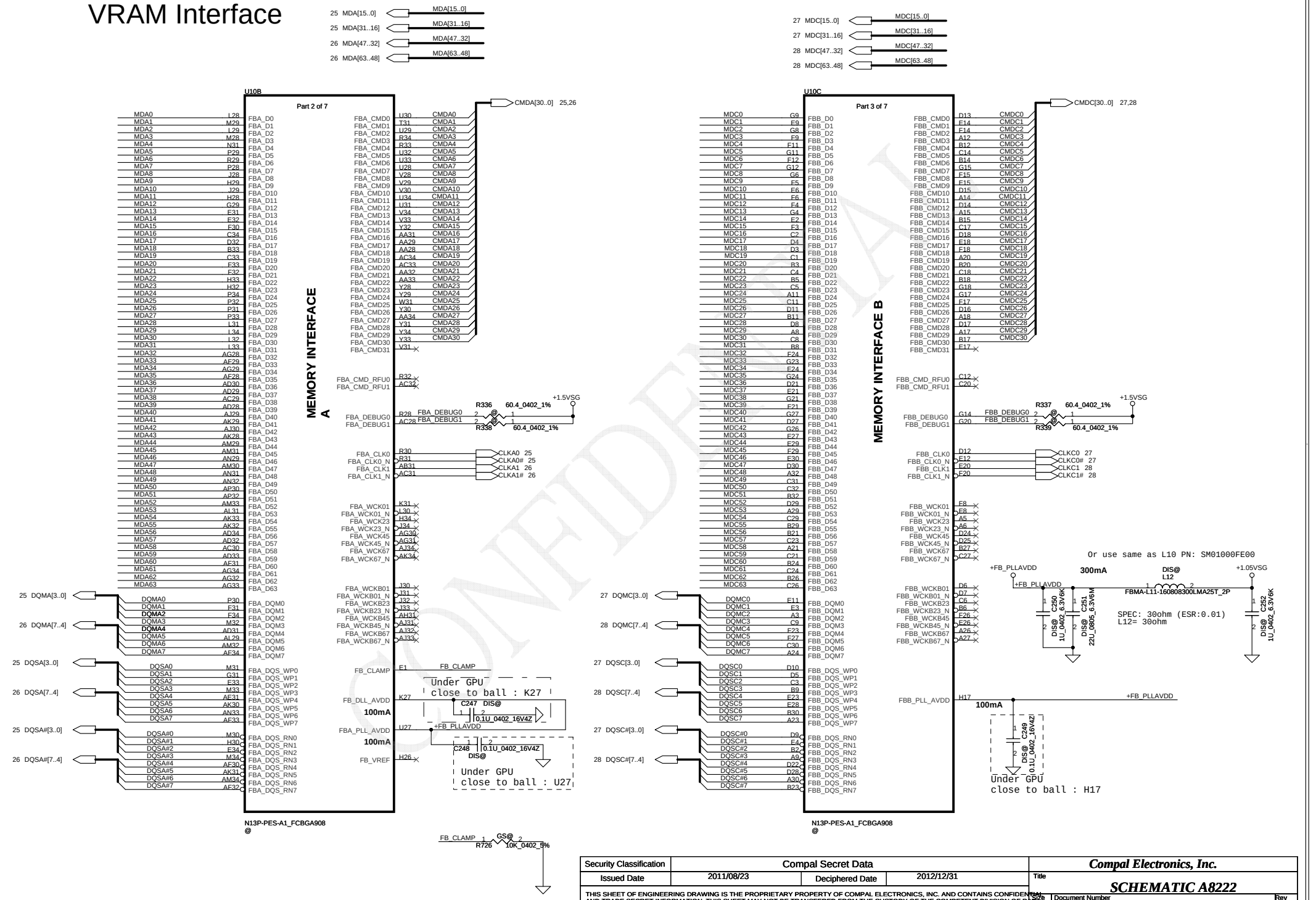
VRAM Interface



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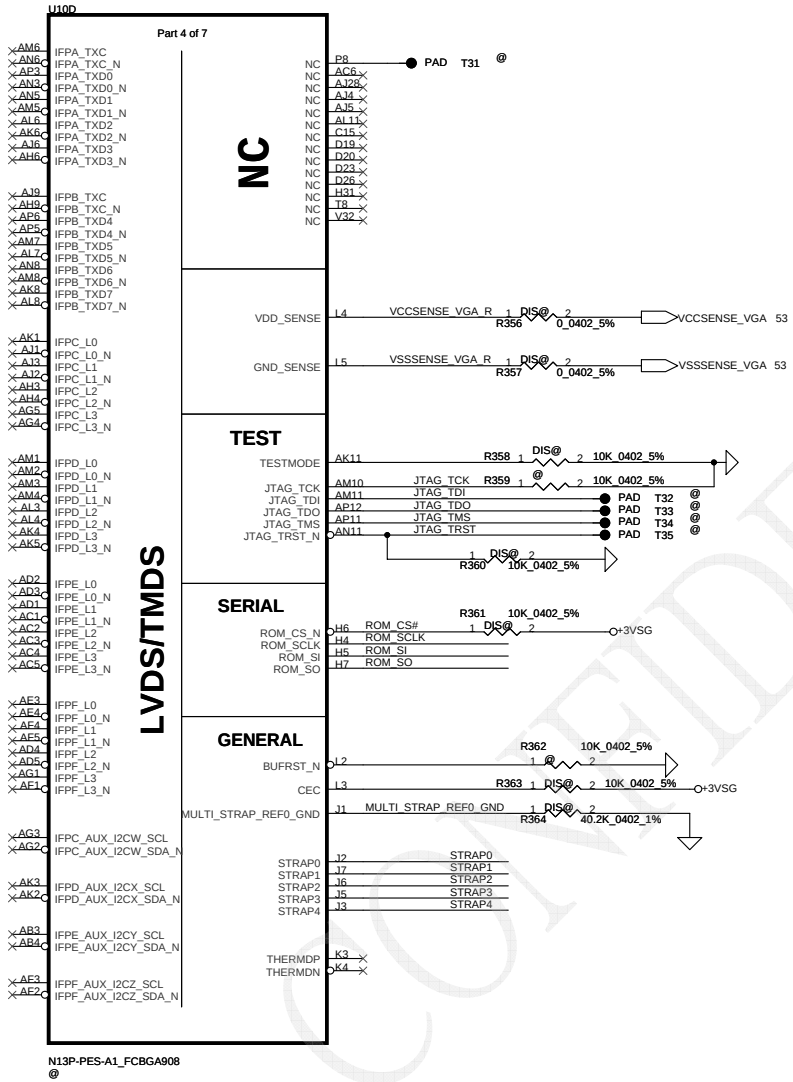

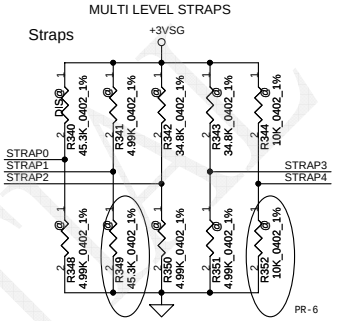

Need check with NVIDIA

For N13P-GS strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	128M* 16* 8 2GB	Samsung SA000047QA0	R PU 45K	R PD 5K	R PD 15K	R PD 25K	R PD 45K	R PD 45K	R PU 10K	R PU 5K
N13P-GS	900 MHz	128M* 16* 8 2GB	Hynix B SA00003YO30	R PU 45K	R PD 5K	R PD 15K	R PD 25K	R PD 45K	R PD 35K	R PU 10K	R PU 5K
N13P-GS	900 MHz	64M* 16* 8 1GB	Samsung SA00004GS30	R PU 45K	R PD 5K	R PD 15K	R PD 25K	R PD 45K	R PD 20K	R PU 10K	R PU 5K
N13P-GS	900 MHz	64M* 16* 8 1GB	Hynix SA000041S60	R PU 45K	R PD 5K	R PD 15K	R PD 25K	R PD 45K	R PD 15K	R PU 10K	R PU 5K
N13P-GS	900 MHz	128M* 16* 8 2GB	Hynix D SA00003YO30						R PD 30K		

For N13P-GL strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GL	900 MHz	128M* 16* 8 2GB	Samsung SA000047QA0	R PU 45K	R PD 45K	R PU 10K	R PD 5K	R PD 10K	R PD 45K	R PU 10K	R PD 15K
N13P-GL	900 MHz	128M* 16* 8 2GB	Hynix B SA00003YO30	R PU 45K	R PD 45K	R PU 10K	R PD 5K	R PD 10K	R PD 35K	R PU 10K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Samsung SA00004GS30	R PU 45K	R PD 45K	R PU 10K	R PD 5K	R PD 10K	R PD 20K	R PU 10K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Hynix SA000041S60	R PU 45K	R PD 45K	R PU 10K	R PD 5K	R PD 10K	R PD 15K	R PU 10K	R PD 15K
N13P-GL	900 MHz	128M* 16* 8 2GB	Hynix D SA00003YO30						R PD 30K		

For N13M-GE1 strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GE1	900 MHz	128M* 16* 4 1GB	Samsung SA000047QA0	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 45K	R PU 10K	R PU 5K
N13M-GE1	900 MHz	128M* 16* 4 1GB	Hynix SA00003YO30	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 35K	R PU 10K	R PU 5K

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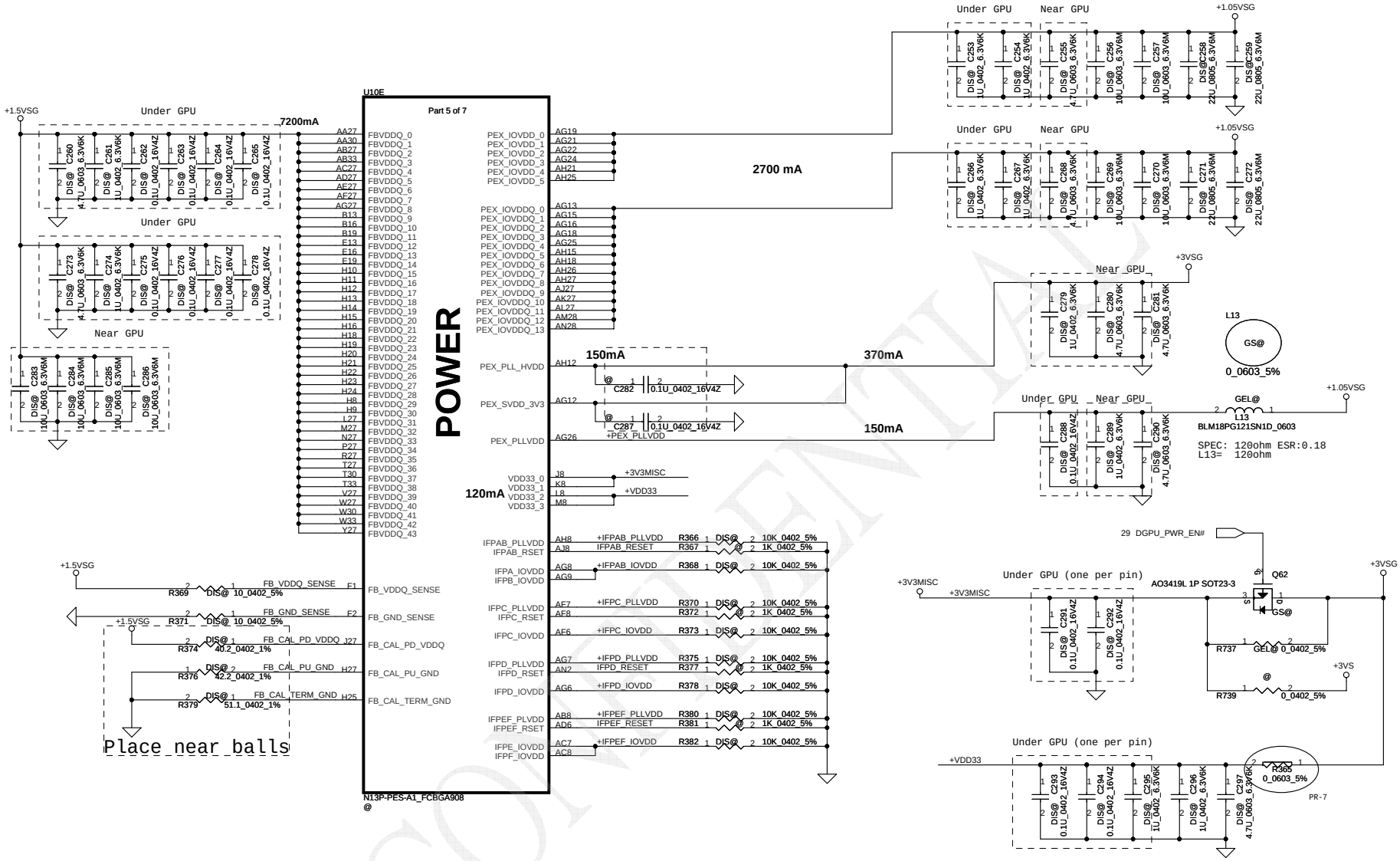

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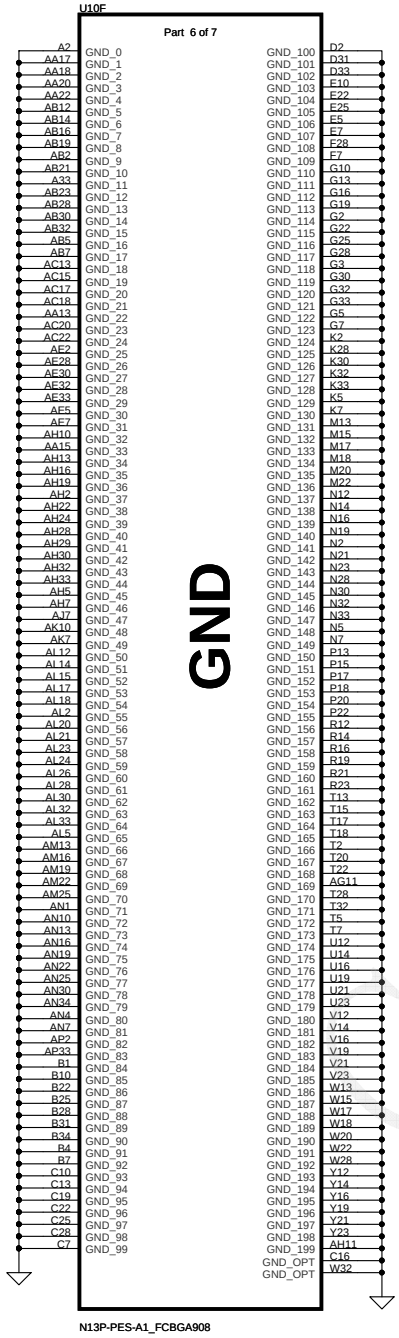

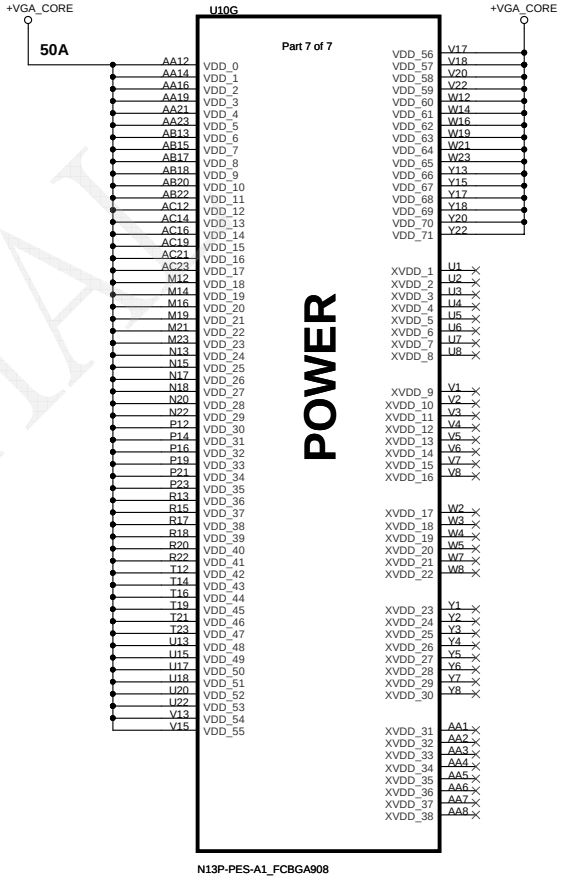

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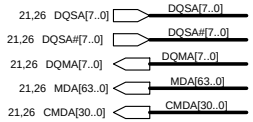
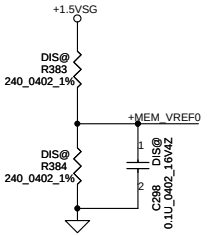
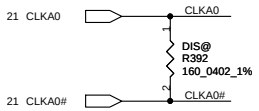
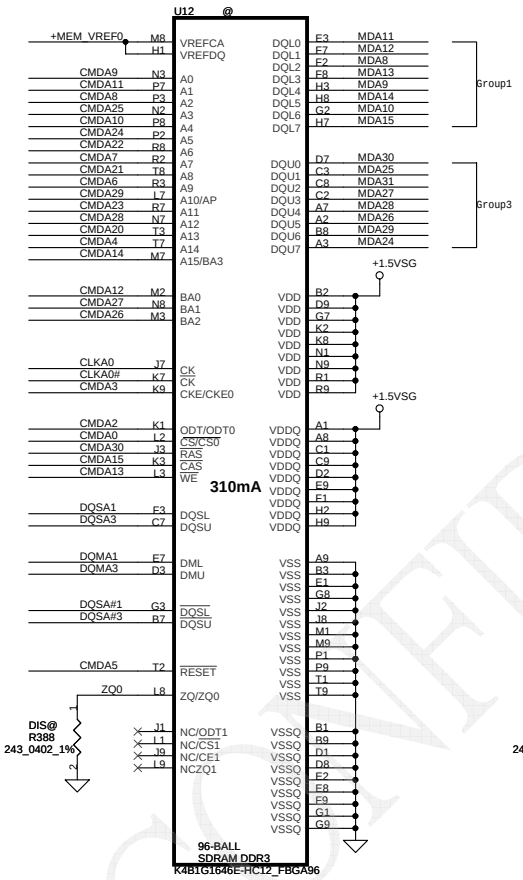
VRAM DDR3 chips (1GB)

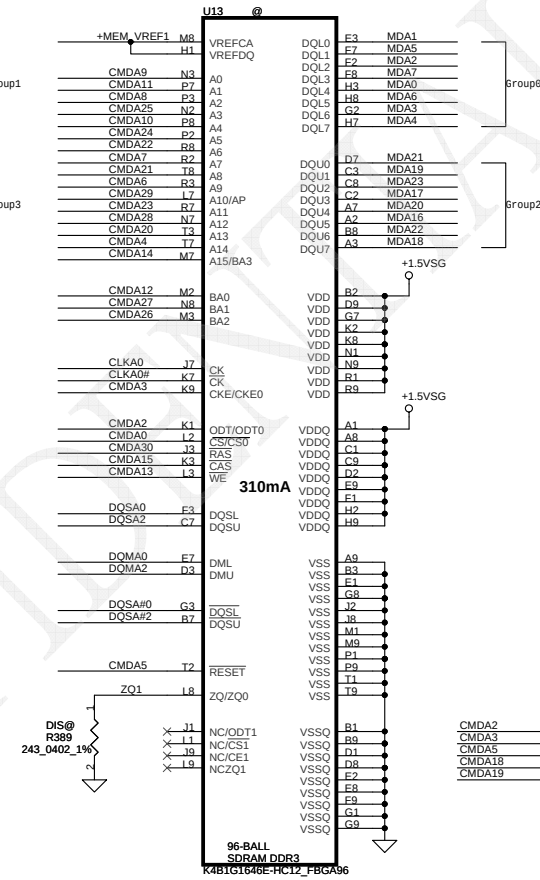
64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB

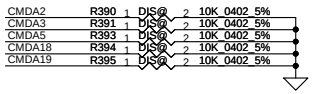




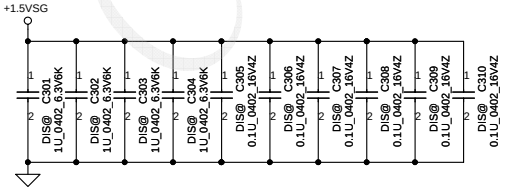


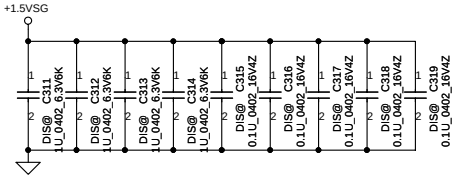






	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination





Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
AMD :SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

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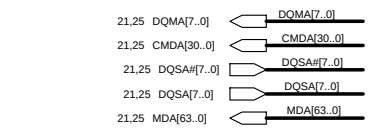
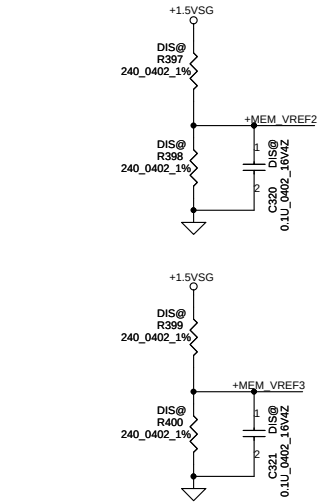
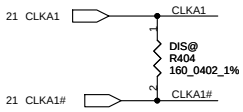
VRAM DDR3 chips (1GB)

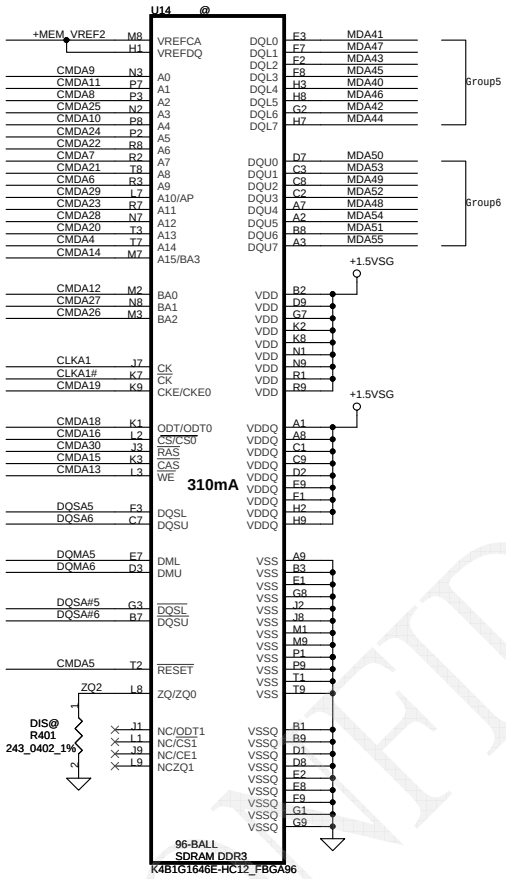
64Mx16 DDR3 *8==>1GB

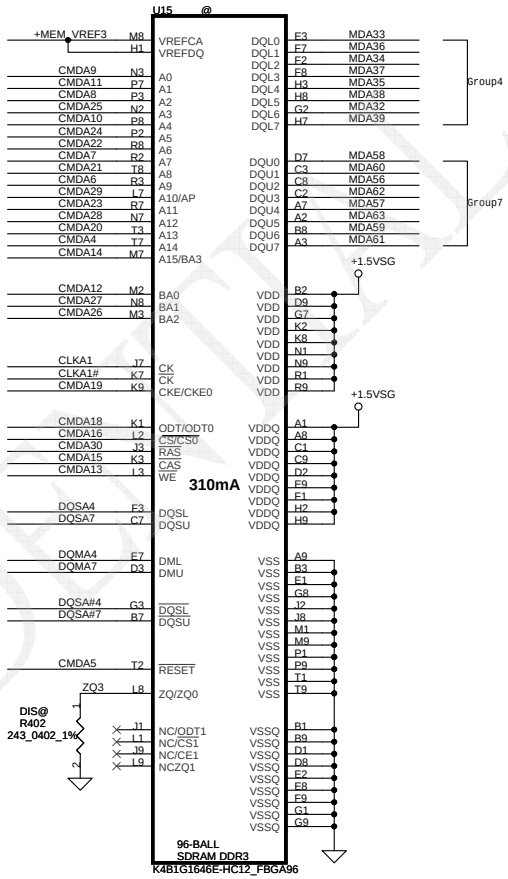
128Mx16 DDR3 *8==>2GB

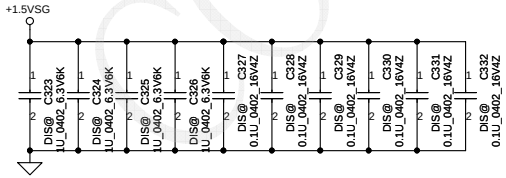


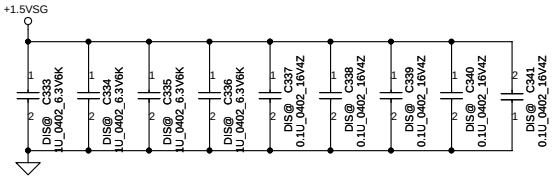












Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

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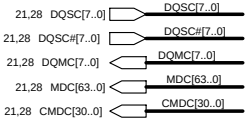
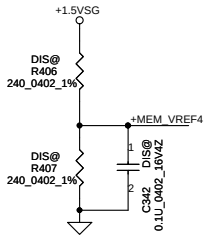
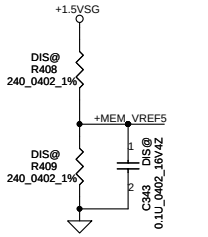
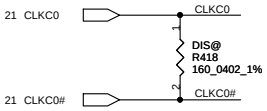
VRAM DDR3 chips (1GB)

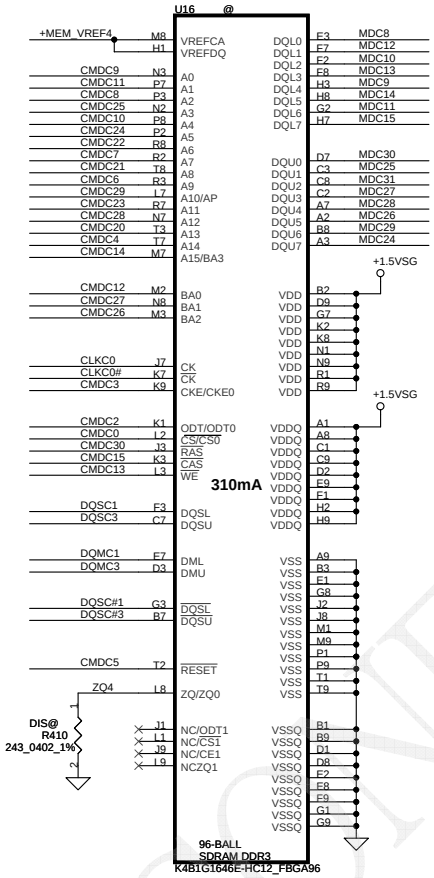
64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB

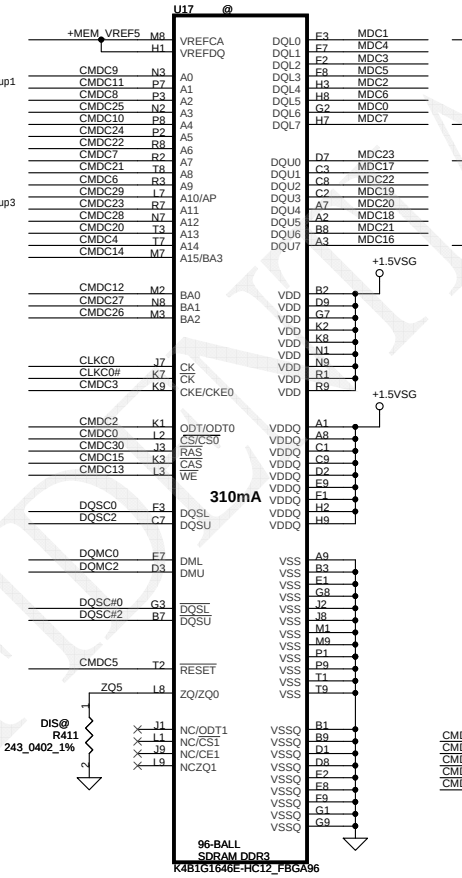


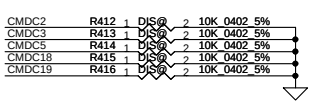






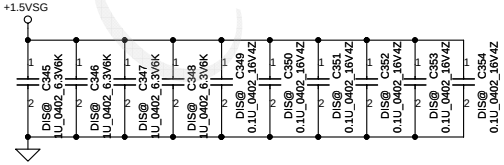


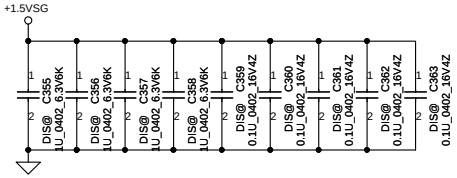




Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination





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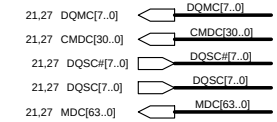
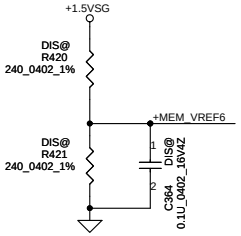
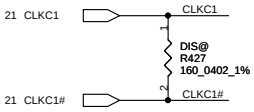
VRAM DDR3 chips (1GB)

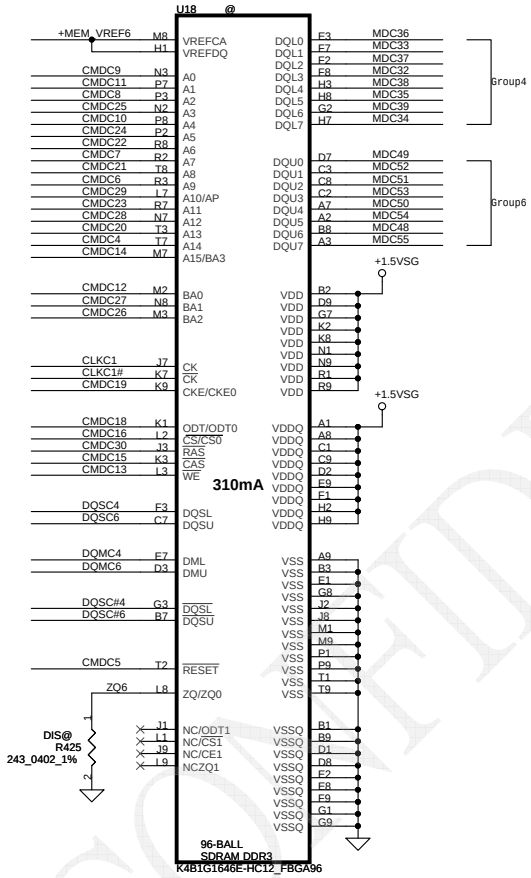
64Mx16 DDR3 *8==>1GB

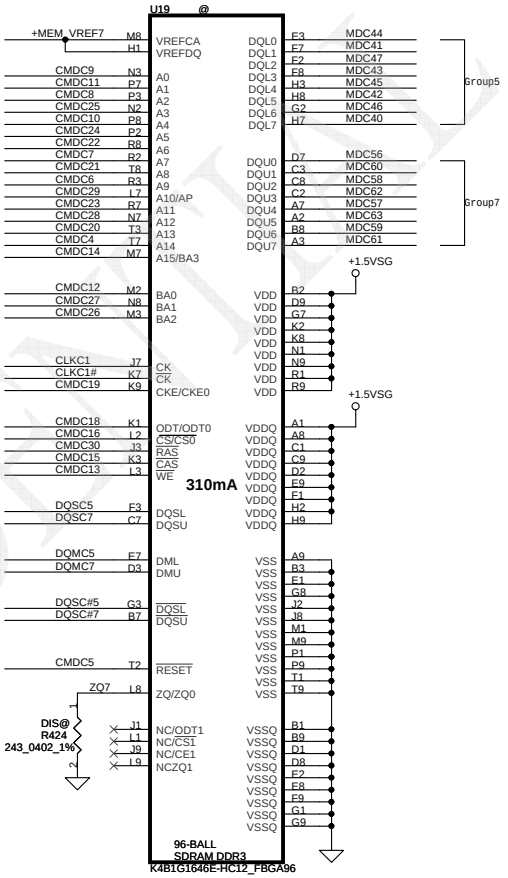
128Mx16 DDR3 *8==>2GB

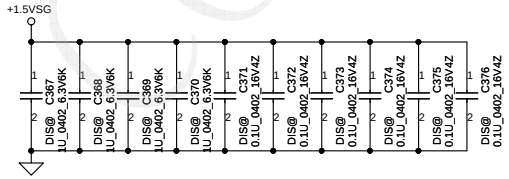


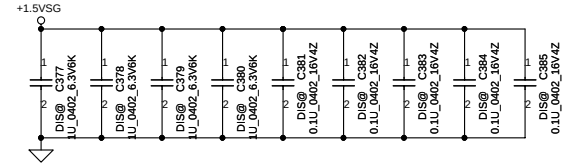












Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

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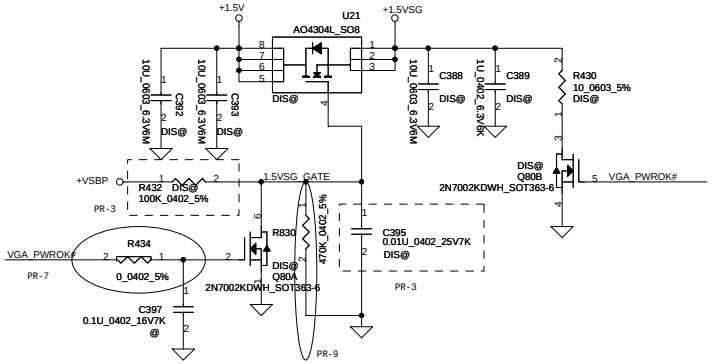
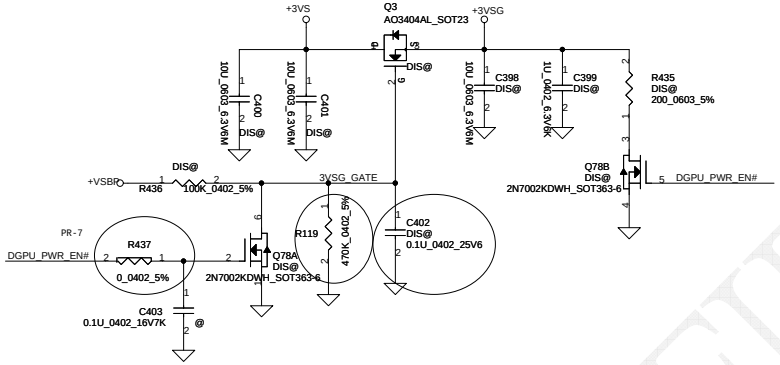
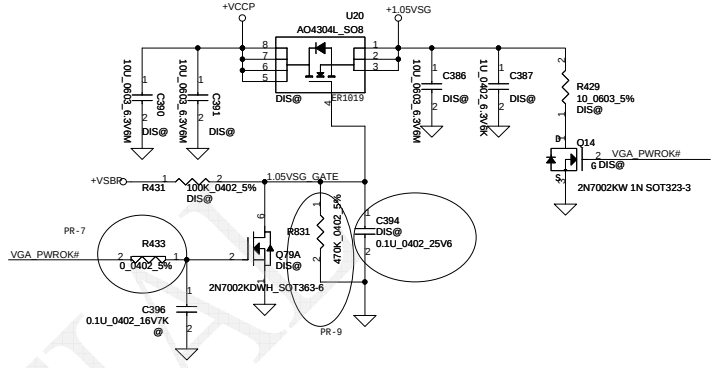
+1.5V to +1.5VSG

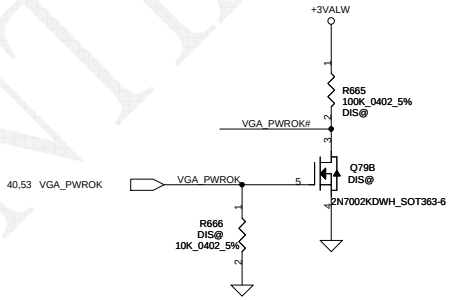


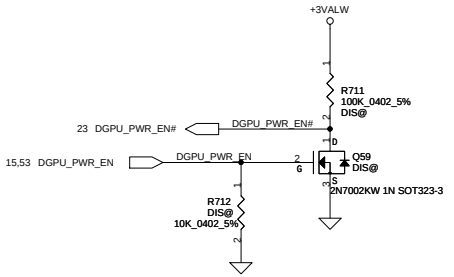
+3VS to +3VSG

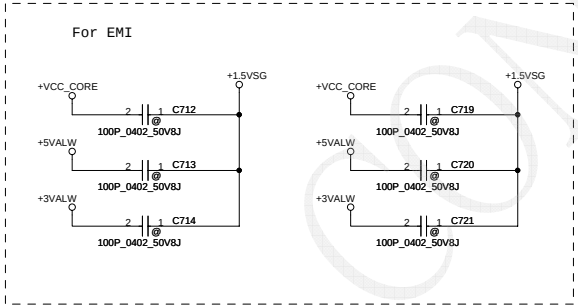


+VCCP to +1.05VSG









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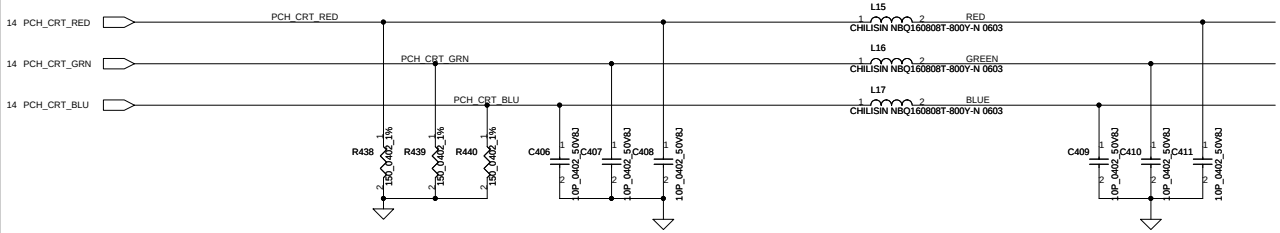
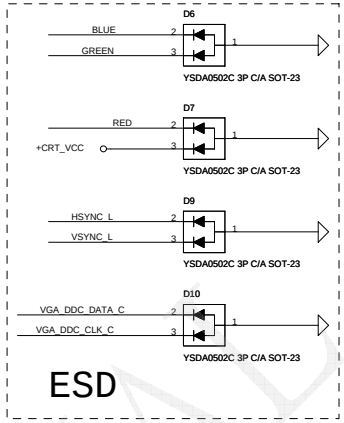
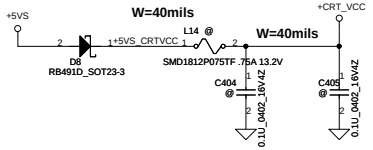
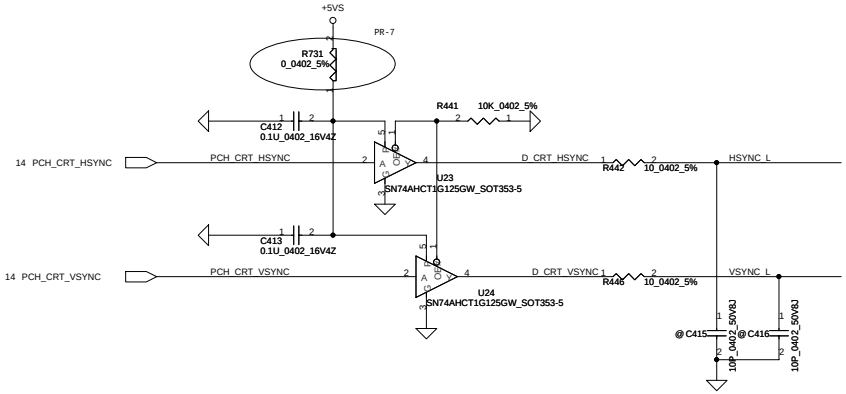
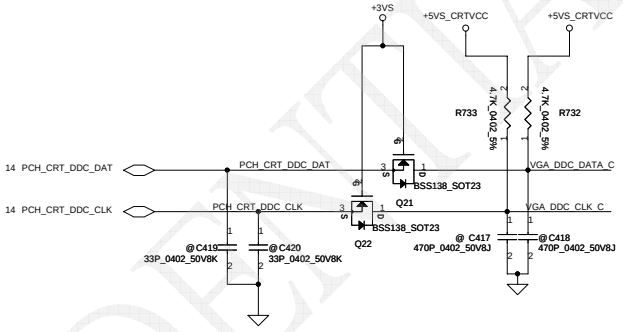
CRT

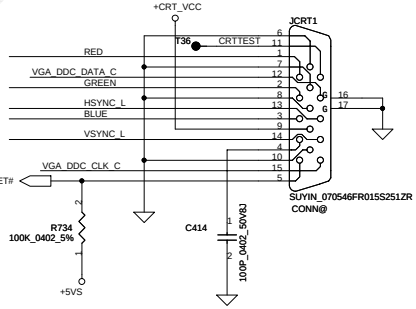




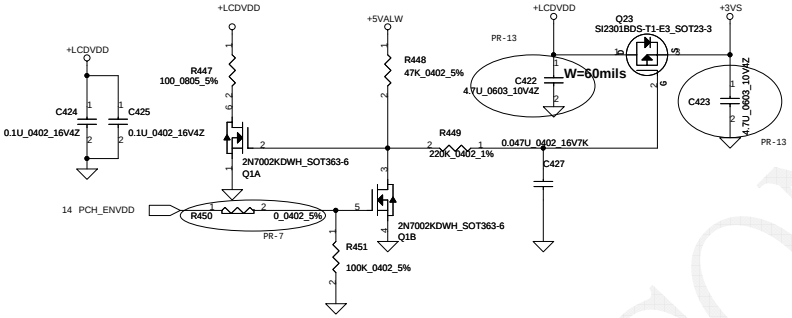


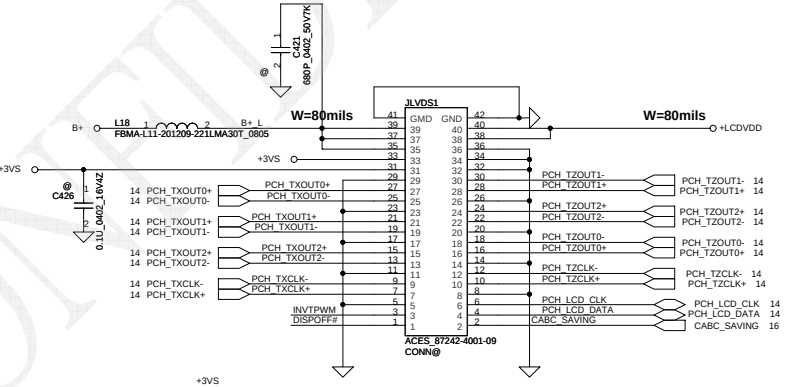


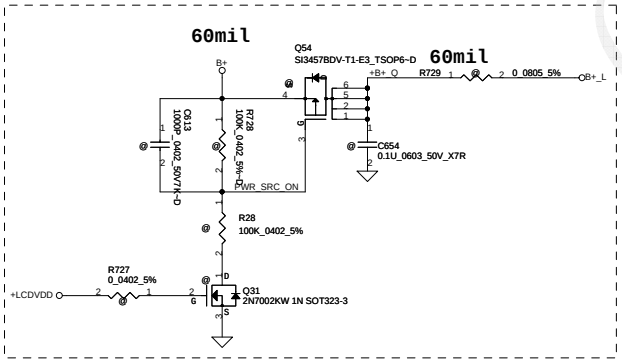




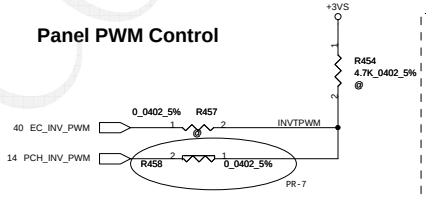
LCD POWER CIRCUIT



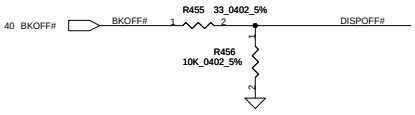




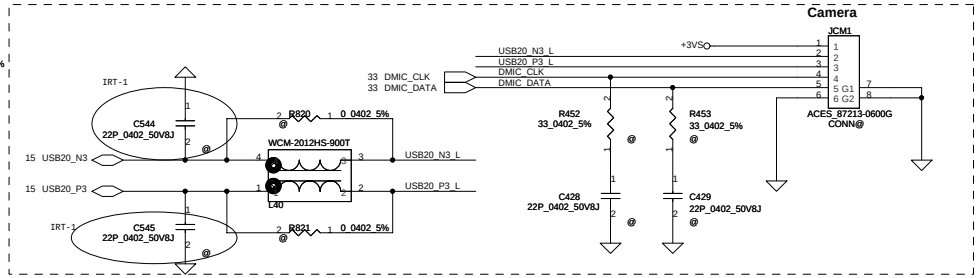
Panel PWM Control



Panel Backlight Control



Camera



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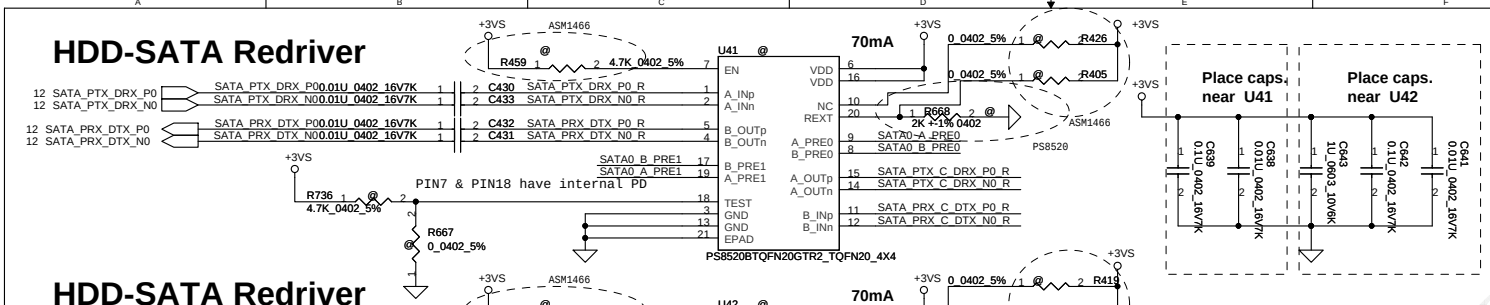
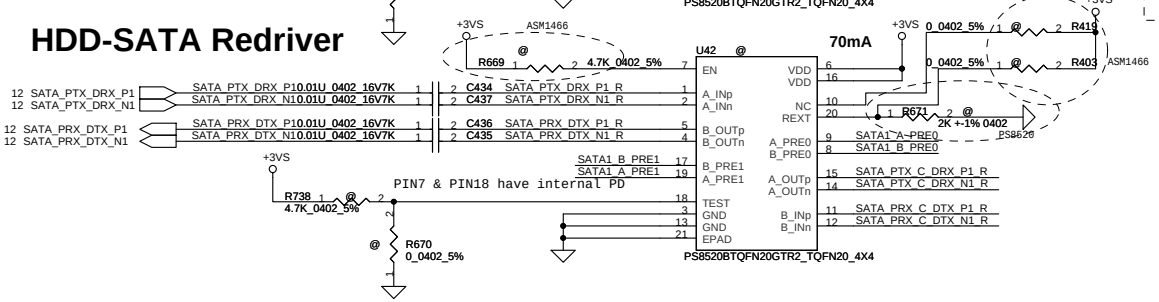
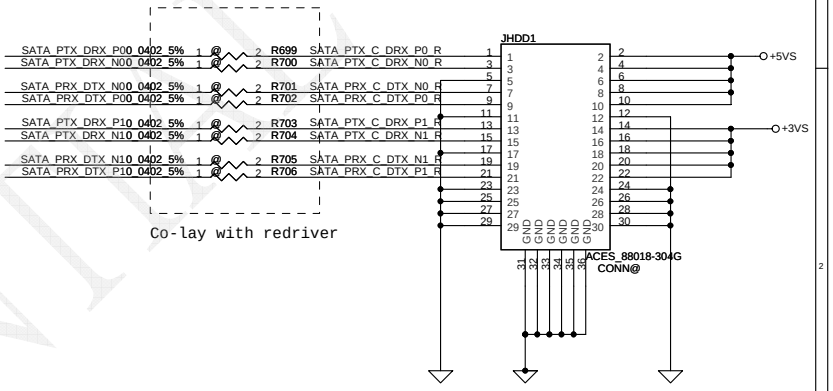
HDD-SATA Redriver



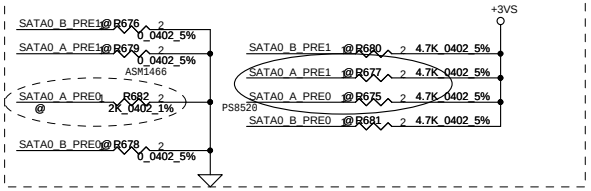
HDD-SATA Redriver



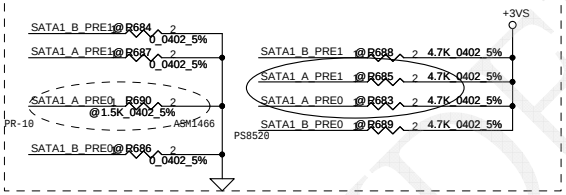
SATA HDD BTB Conn.

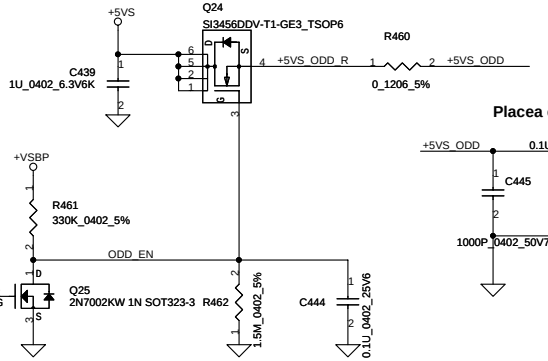


Add EQ pin for PS8520BTQFN20GTR2 FOR SATA0

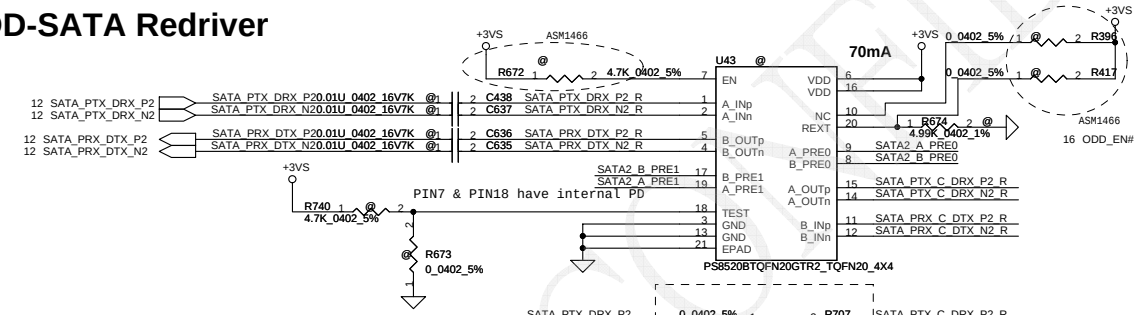


Add EQ pin for PS8520BTQFN20GTR2 FOR SATA1

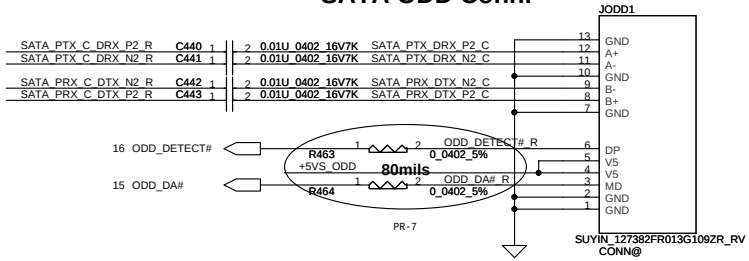




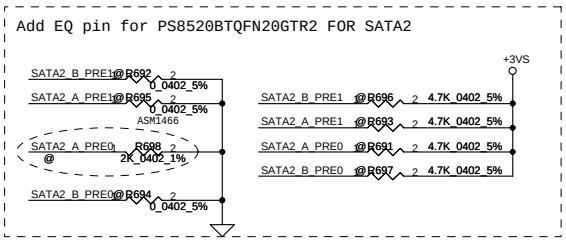
ODD-SATA Redriver

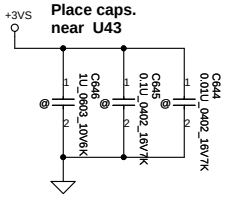


SATA ODD Conn.



Add EQ pin for PS8520BTQFN20GTR2 FOR SATA2





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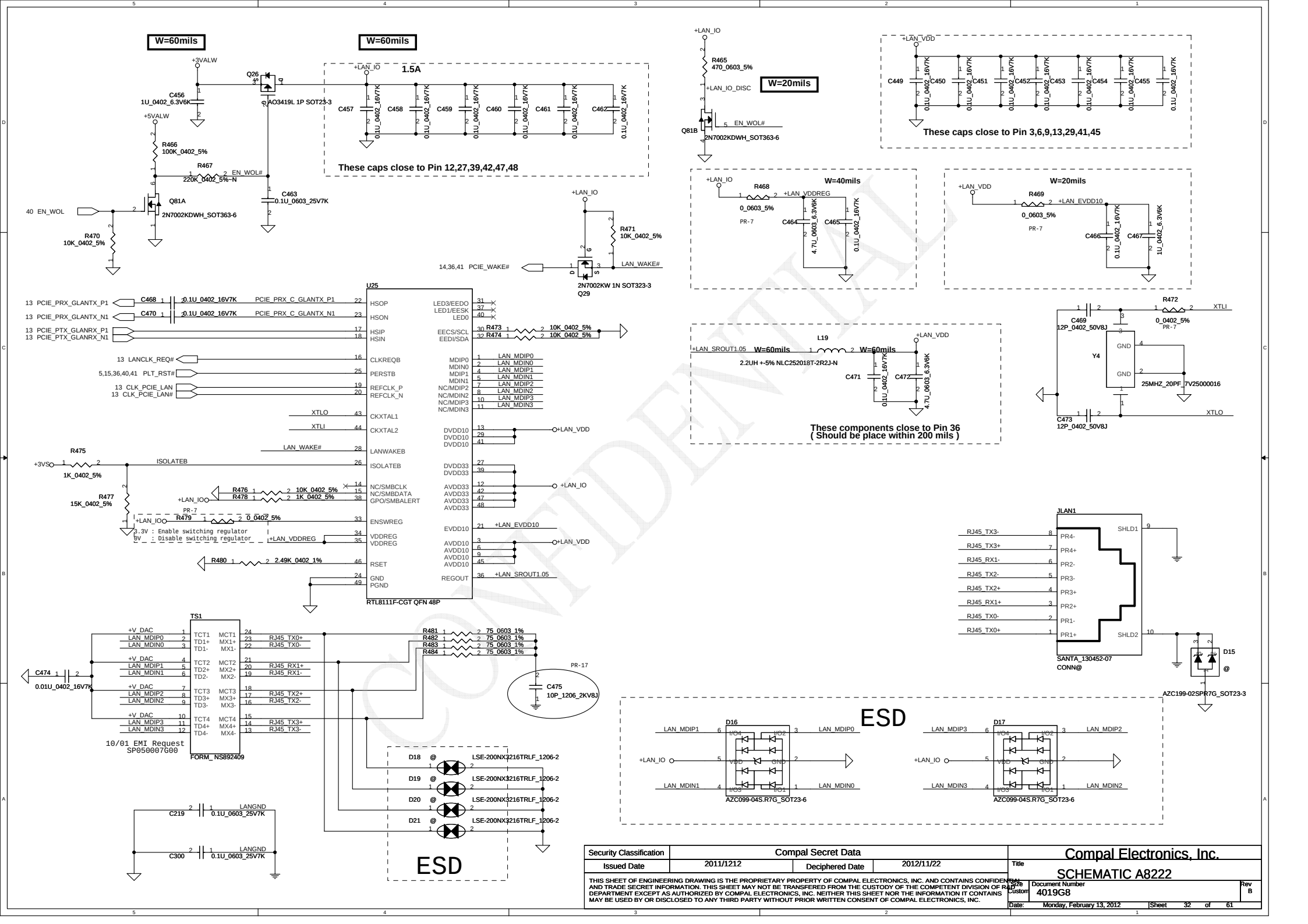

Security Classification	Compal Secret Data		
Issued Date	2011/1212	Deciphered Date	2012/11/22

Compal Electronics, Inc.

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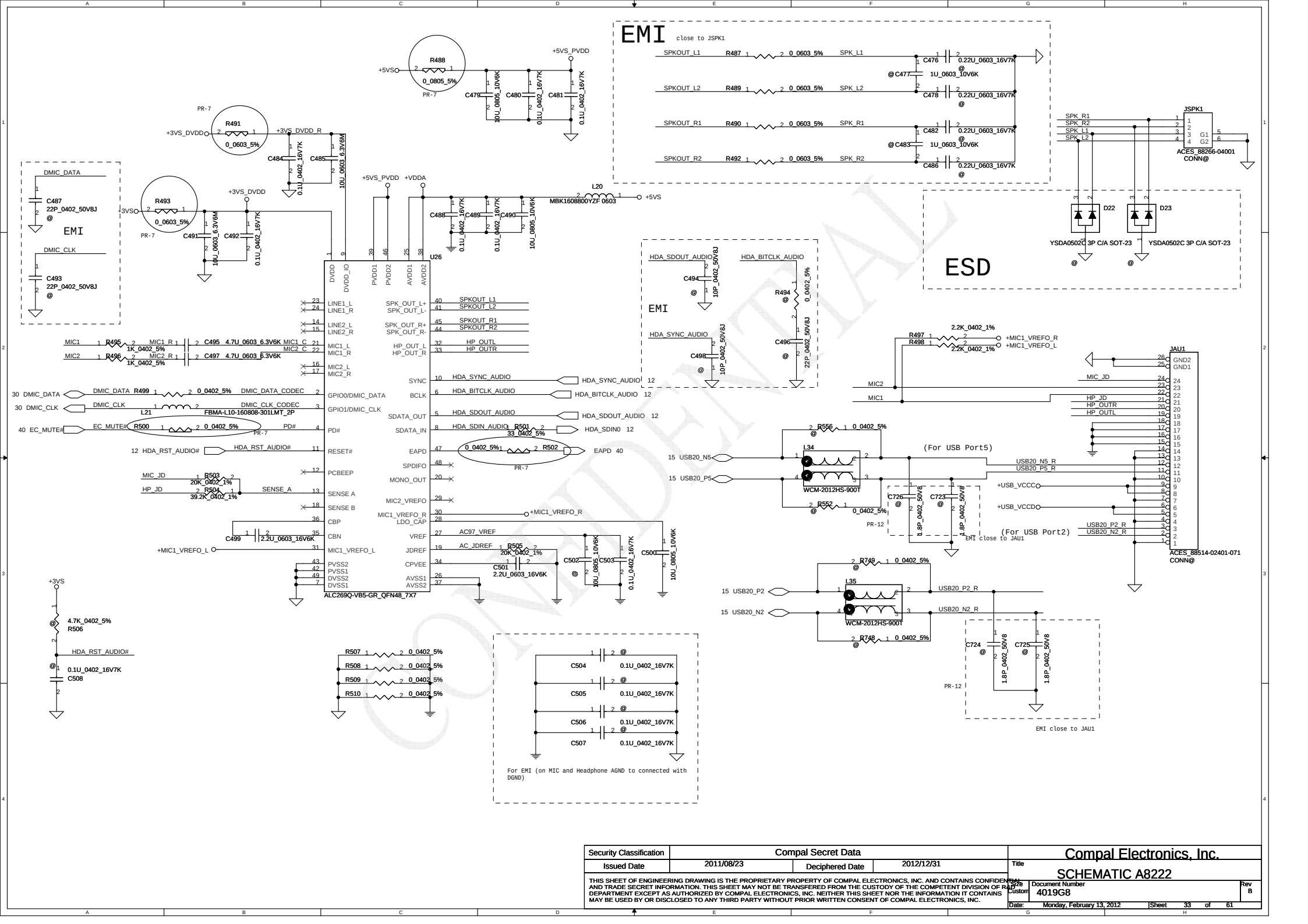

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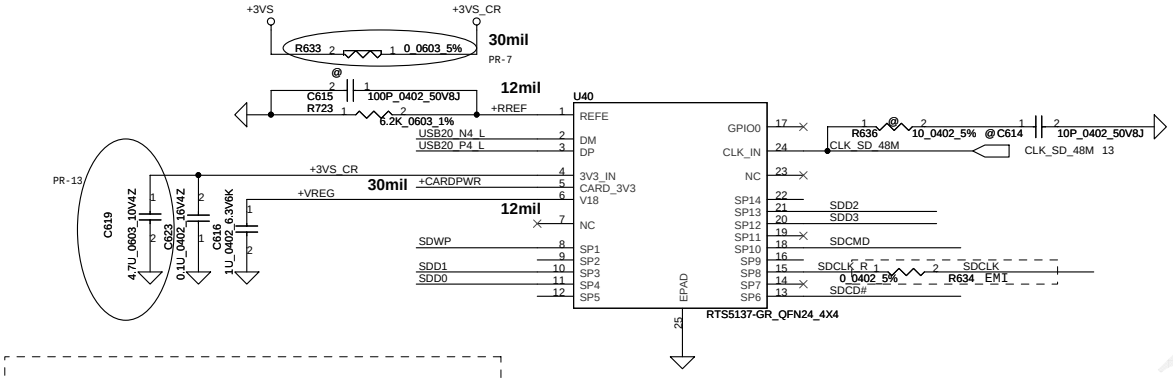
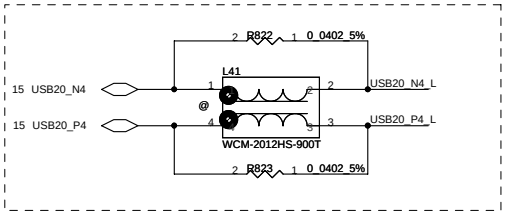
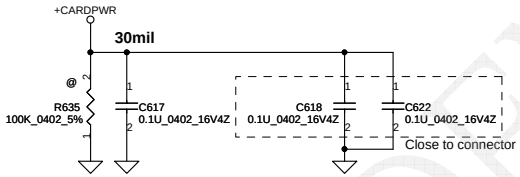
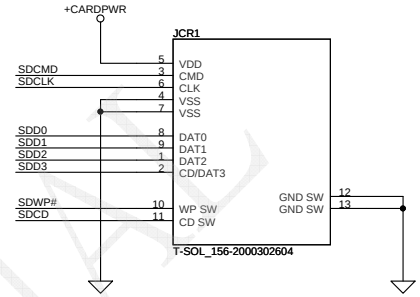
Card Reader RTS5137
(only SD/MMC/MS function)

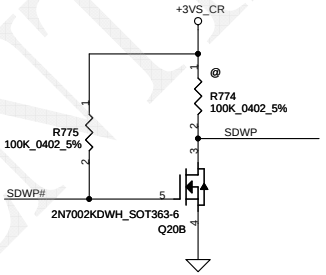


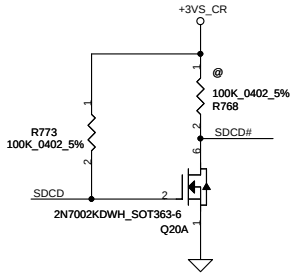


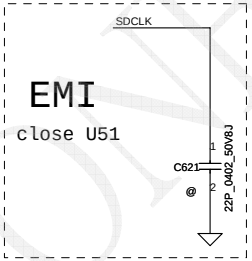


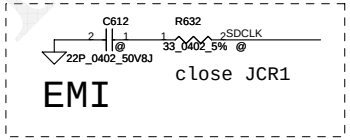
Card Reader Connector











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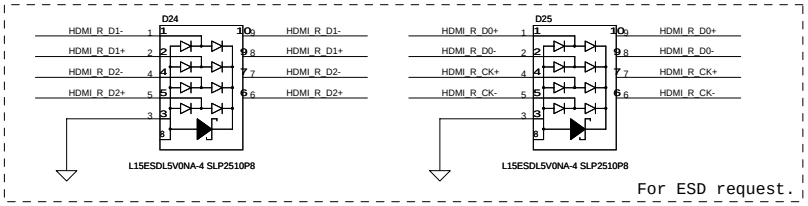

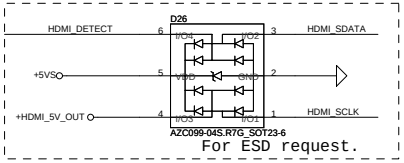

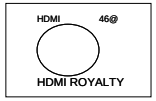

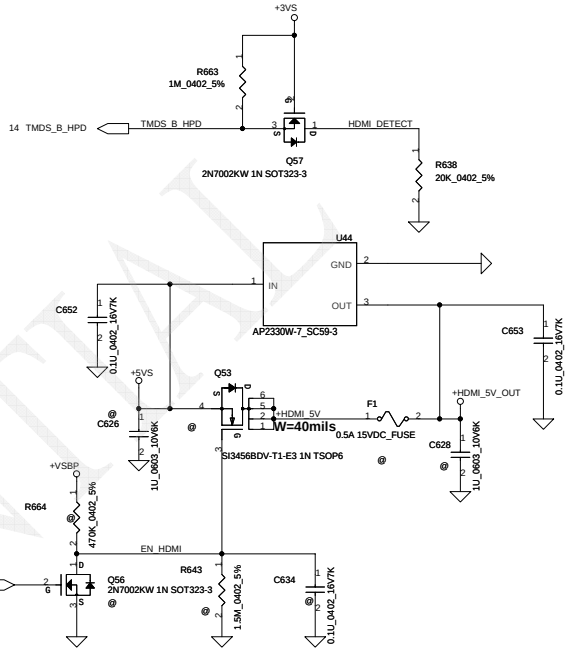

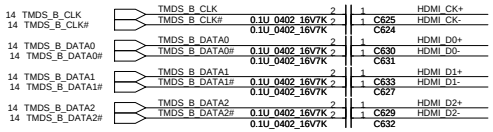

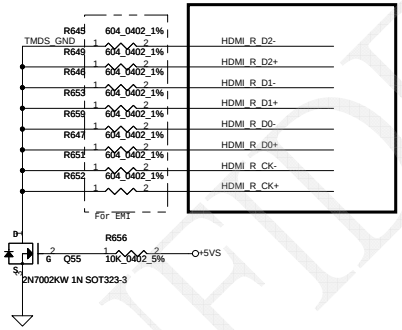

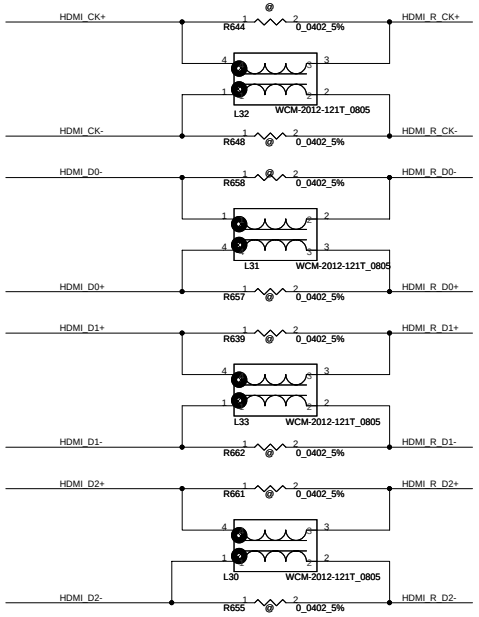

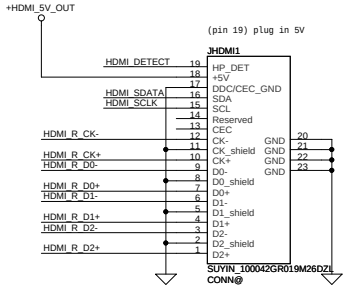

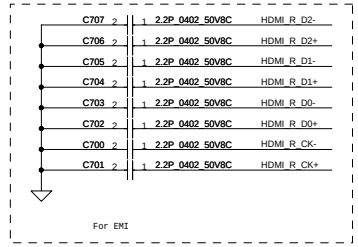

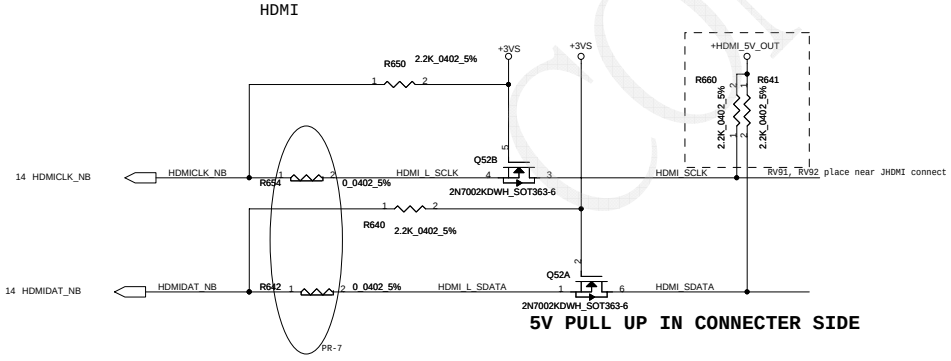

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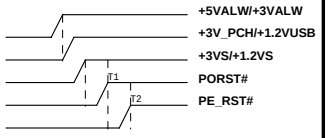
	S3	S4/S5
+3V_PCH	V	X
+3VS	X	X
+1.2VUSB	V	X
+1.2VS	X	X

Power Sequence

ASM1042



T1: 2~80ms
T2: >200ms

For WAKE Function

USB_PEPWRDET

	R1034	R1022
S1	Mount	@
* S3	@	Mount

USB_PESEL

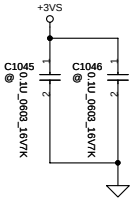
	R1033
* Other applaction	@
Express Card/Mini Card	Mount

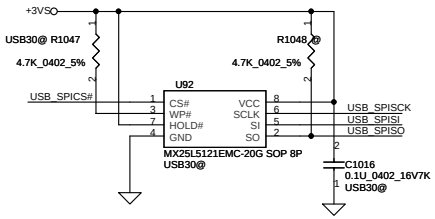
7~10mil

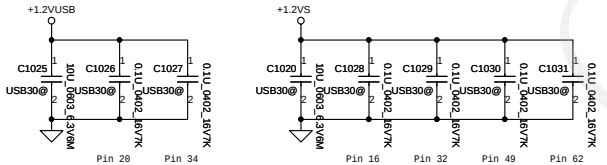
USB_PE_REXT R1030 1 USB30@ 2 12.1K_0402_1%
USB_UREXT R1032 1 USB30@ 2 12.1K_0402_1%

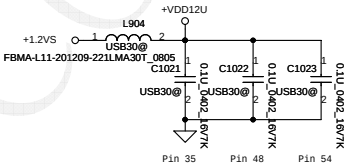
USB30_XT1 — C1004 @ 22P_0402_50V8J — C1005 12P_0402_50V8J USB30@ — Y9 20MHZ_12PF_X3G020000FC1H-X USB30@ — C1006 22P_0402_50V8J — USB30_XT2

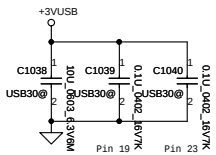
EMC Caps C1045, C1046 should be placed at board(-8430.00 -3530.00)

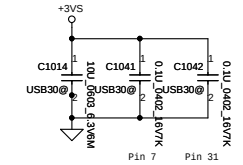


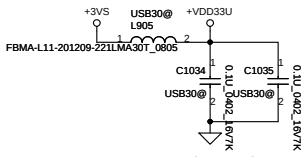




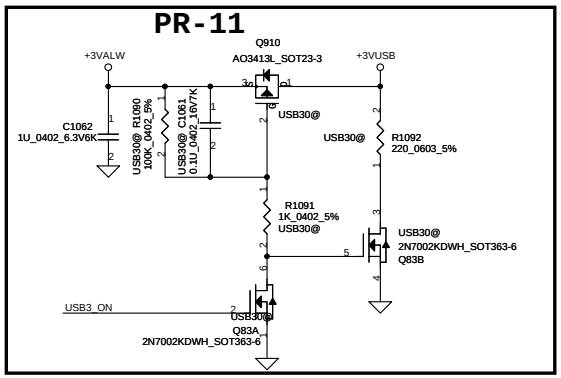




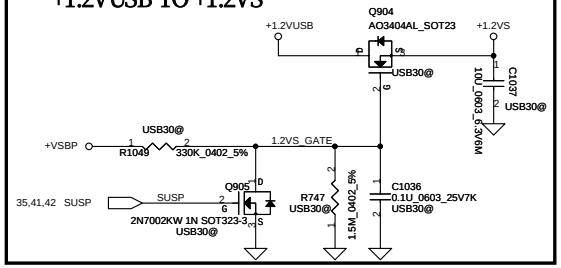




PR-11

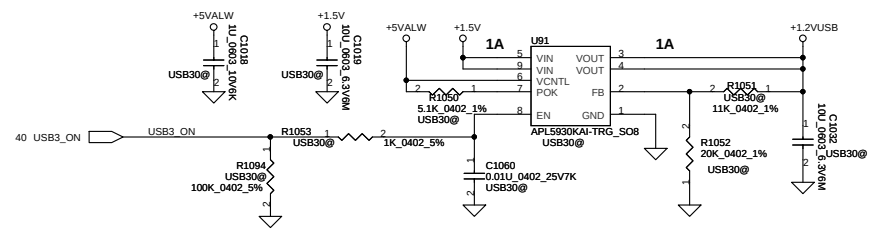


+1.2VUSB TO +1.2VS



PR-11

+1.5Vto +1.2VUSB Transfer



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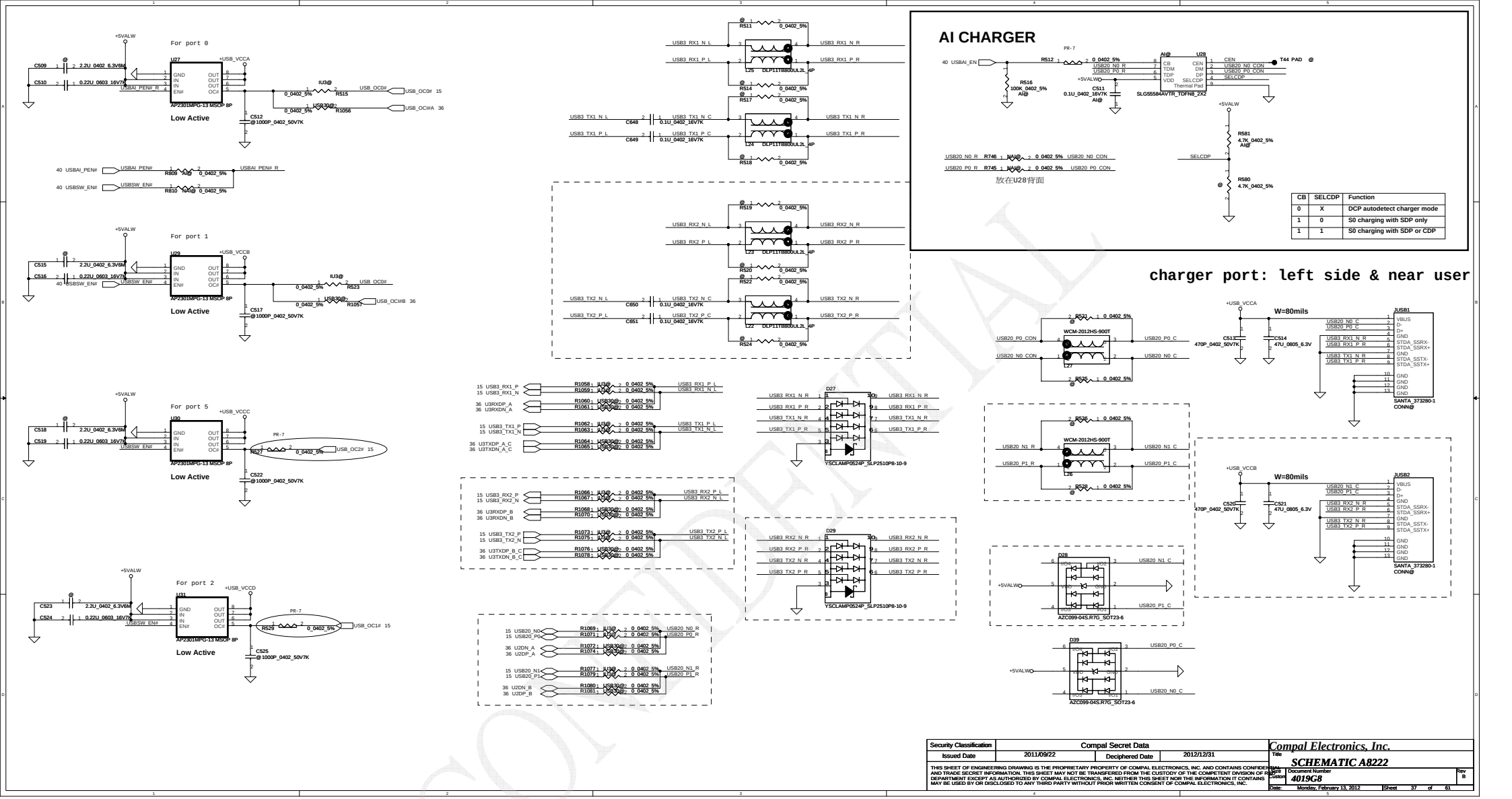

CB	SELCDP	Function
0	X	DCP autodetect charger mode
1	0	S0 charging with SDP only
1	1	S0 charging with SDP or CDP

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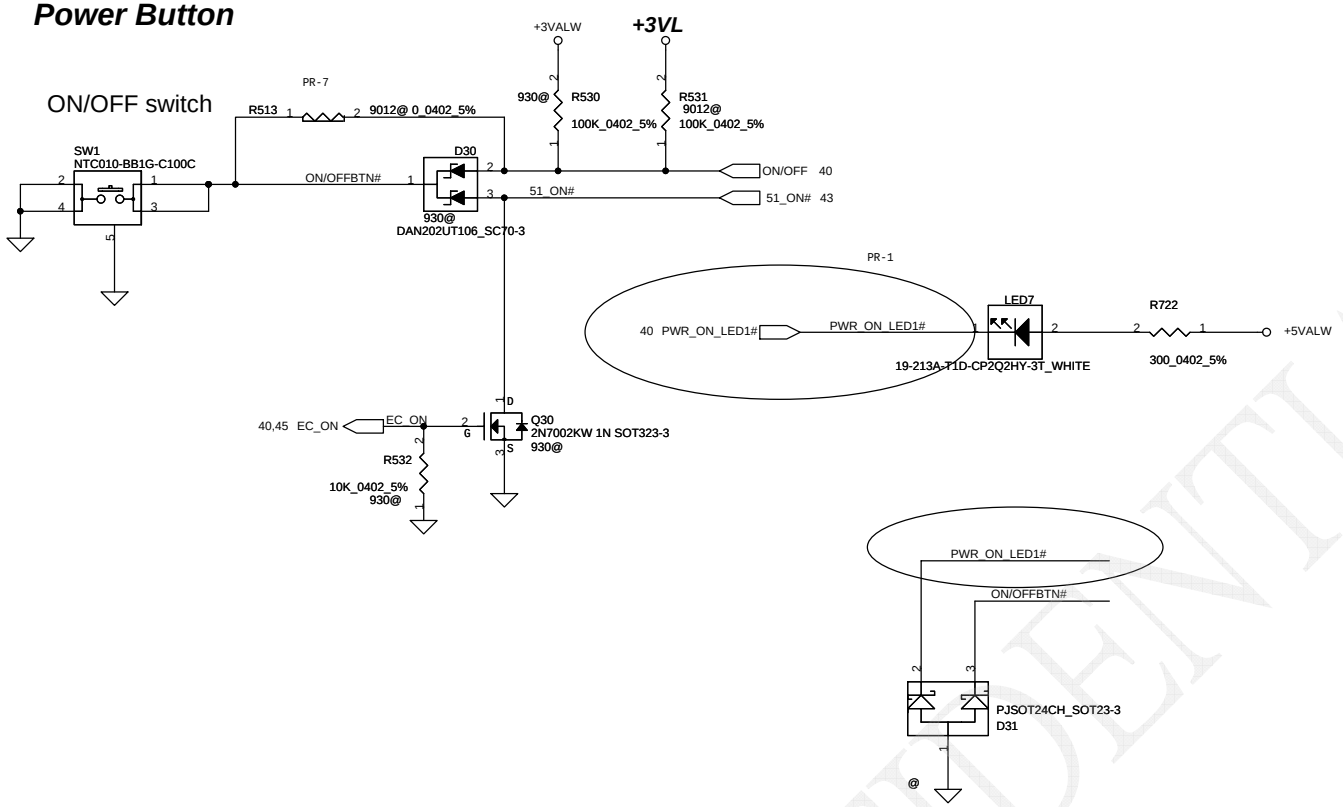
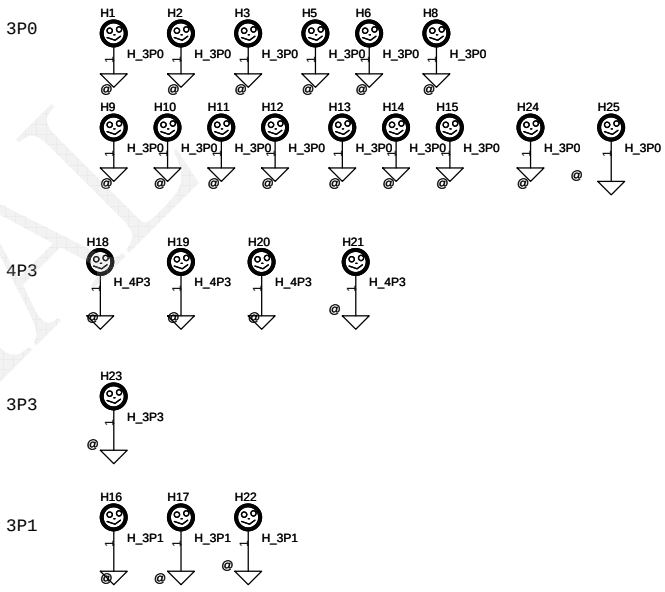
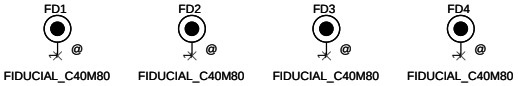
Power Button

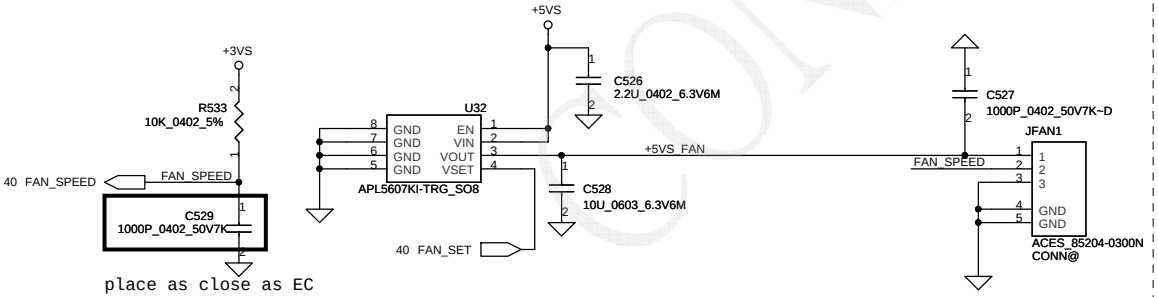


Screw Hole





Fan Control Circuit



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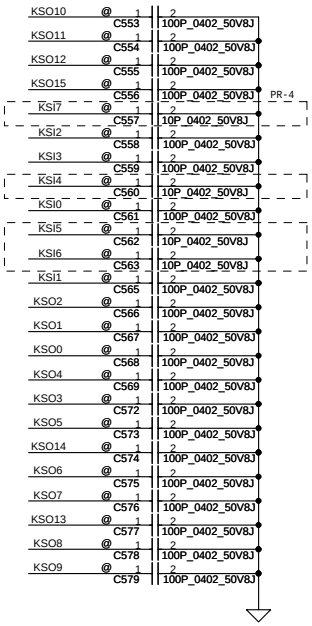
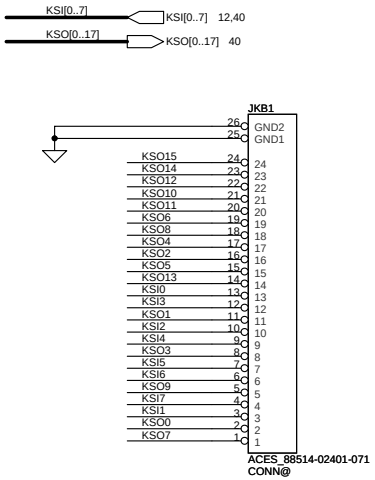
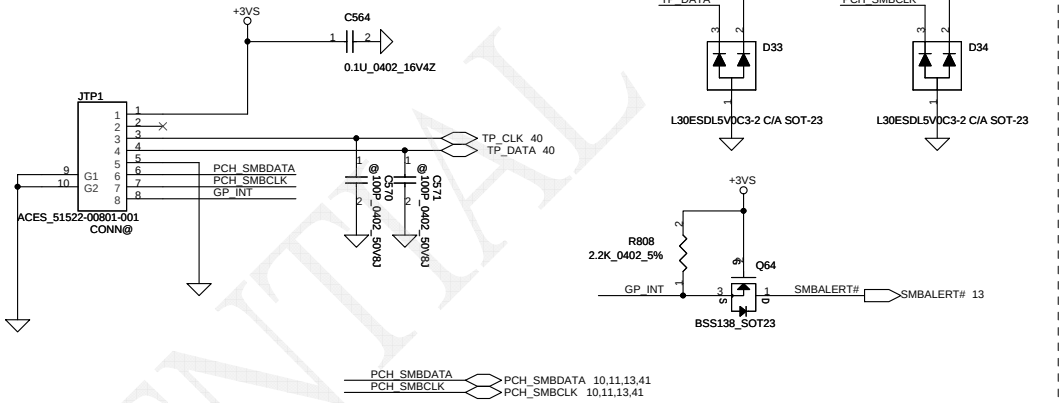


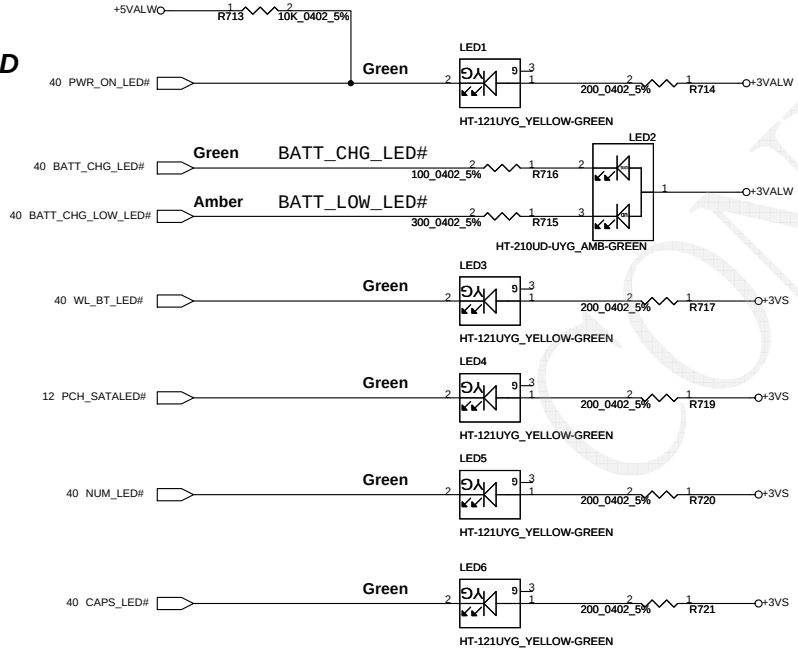
INT_KBD Conn.



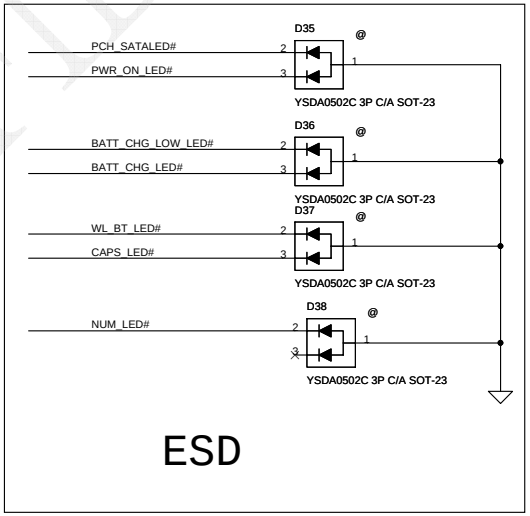
Touch/B Connector



LED

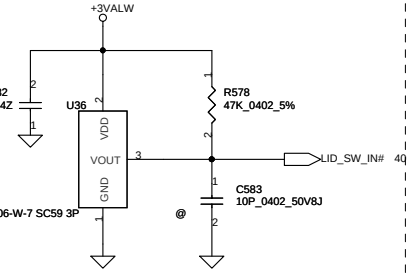


ESD



Lid Switch

(Hall Effect Switch)



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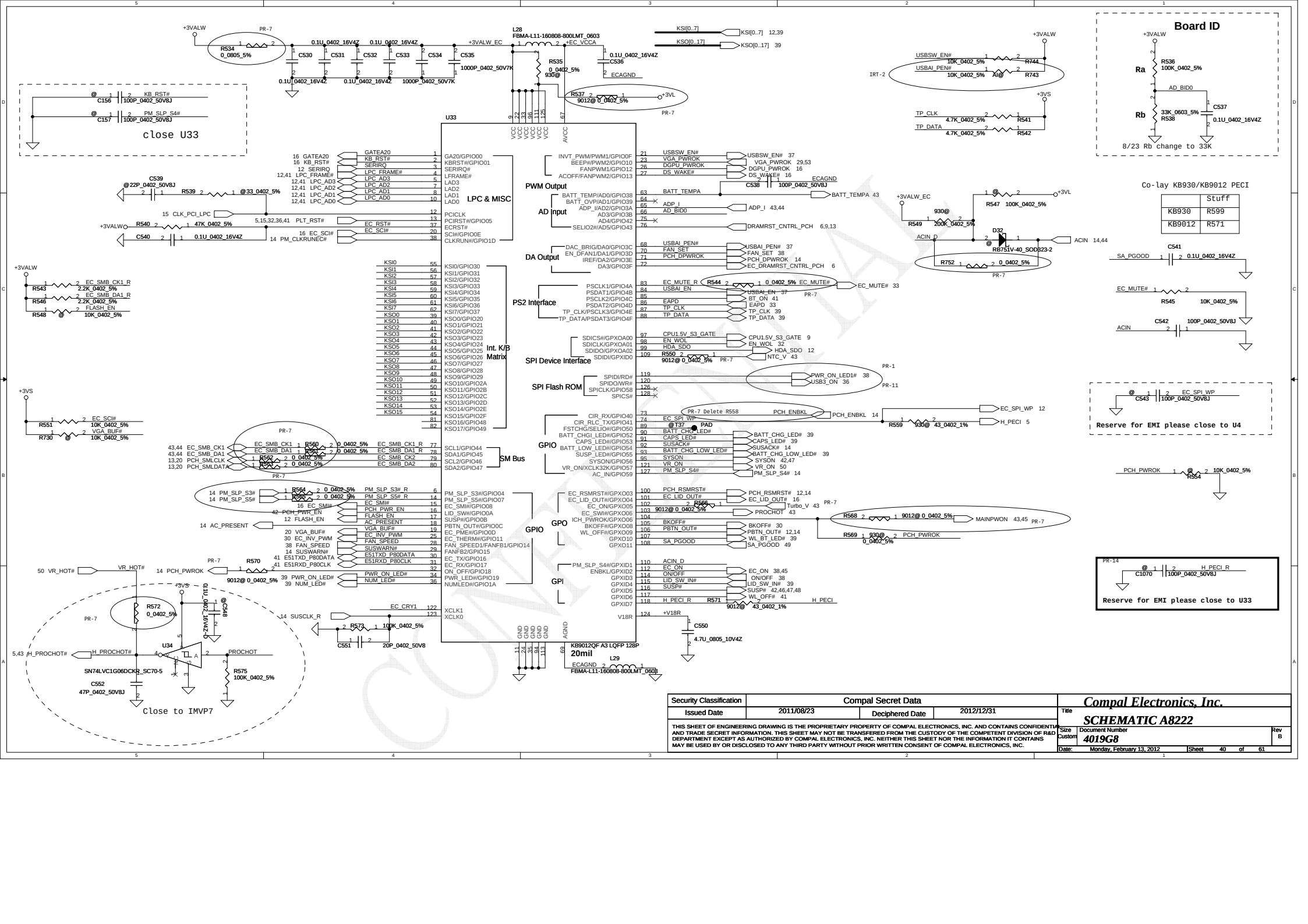
close U33
Close to IMVP7
Board ID
8/23 Rb change to 33K
Co-lay KB930/KB9012 PECI
Reserve for EMI please close to U4
Reserve for EMI please close to U33
U33
KB9012QF A3 LQFP 128P
20mil
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
GPIO
GPO
GPI
LPC & MISC
Int. K/B Matrix
SM Bus
U34
SN74LVC1G06DCKR_SC70-5
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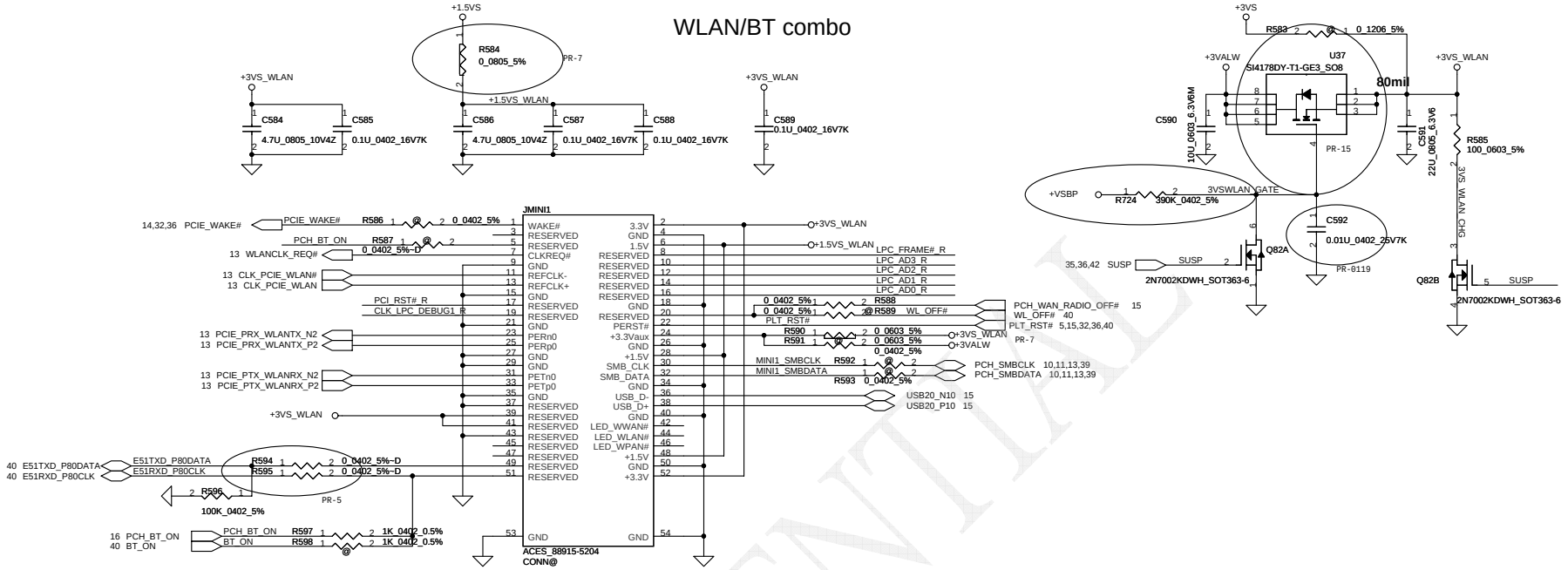
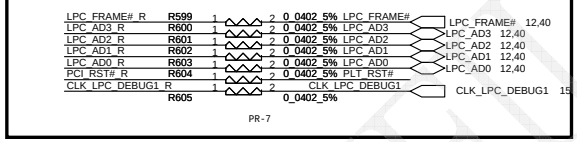
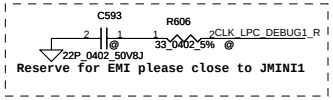
WLAN/BT combo



5.2 mm High

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.





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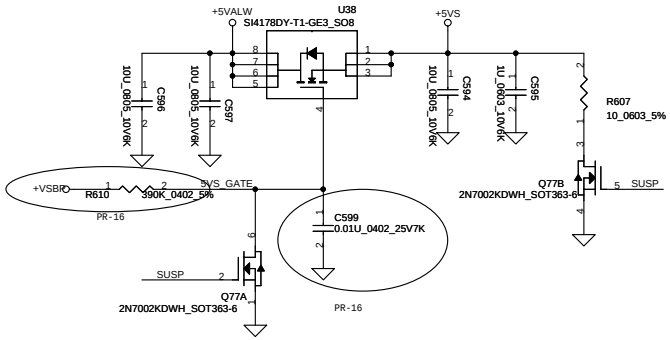
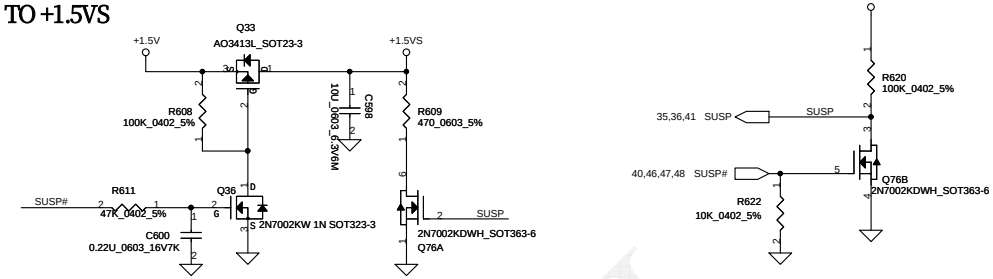
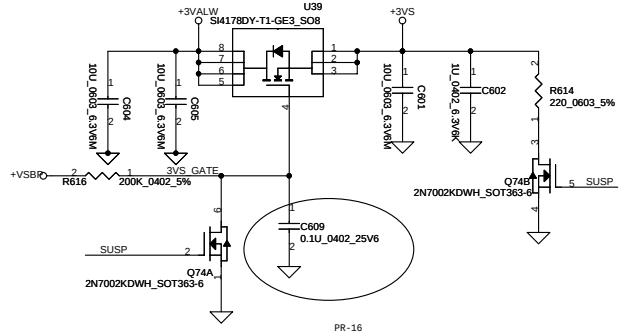
+5VALW TO +5VS

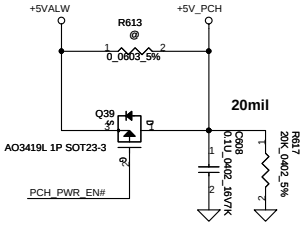


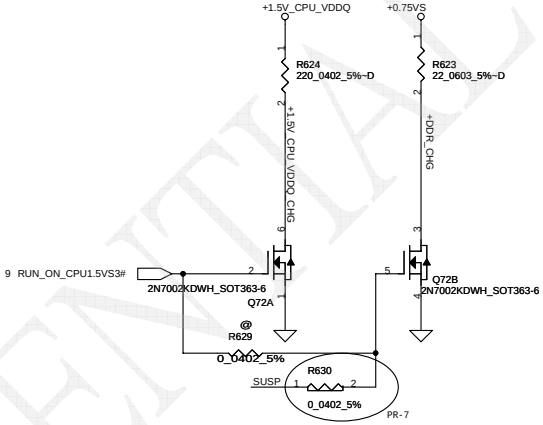
+1.5V TO +1.5VS

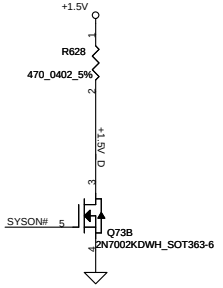


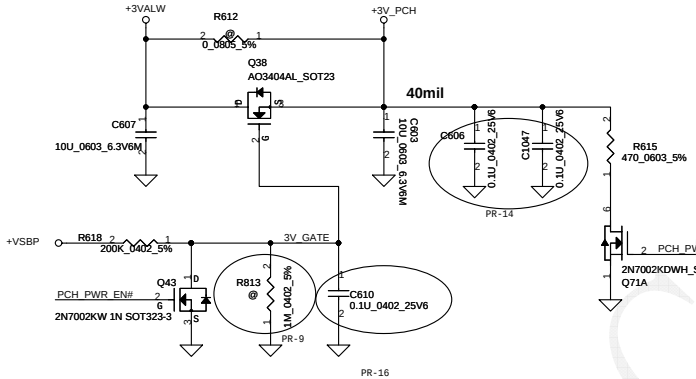
+3VALW TO +3VS

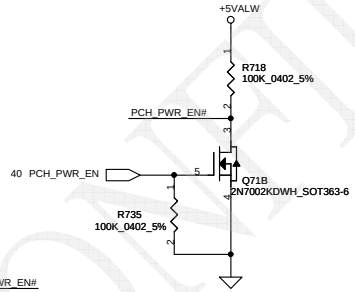


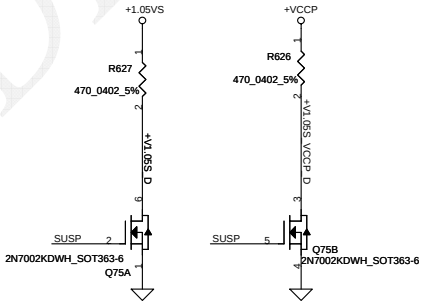


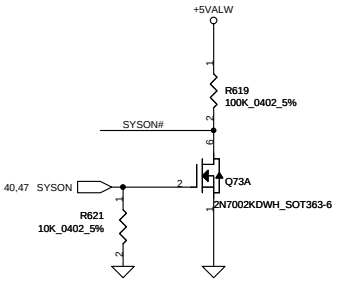












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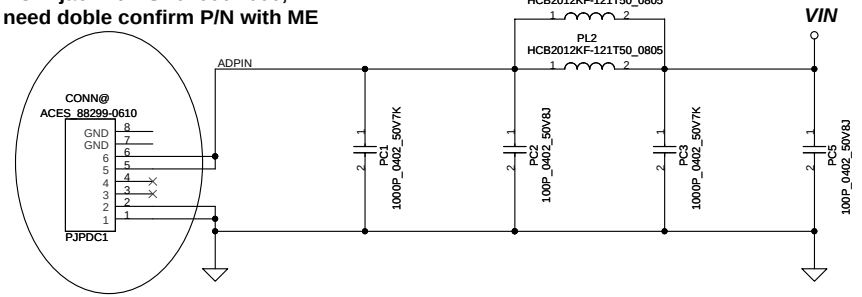
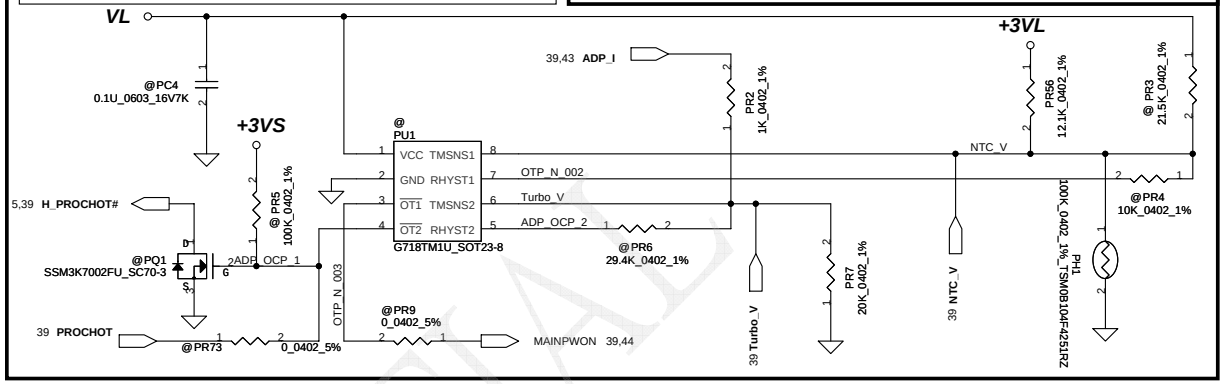
DCIN jack P/N:SP02000N000,
need doble confirm P/N with ME

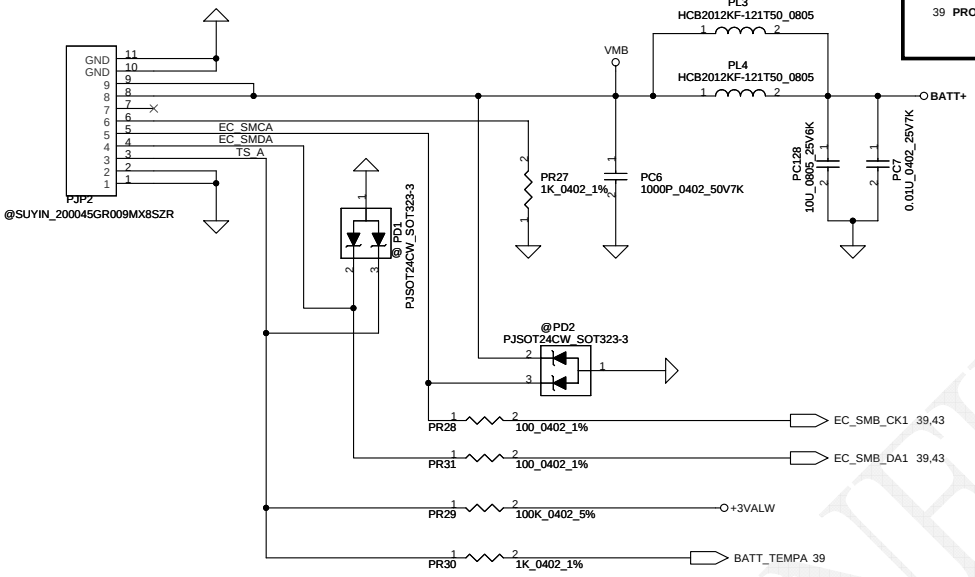


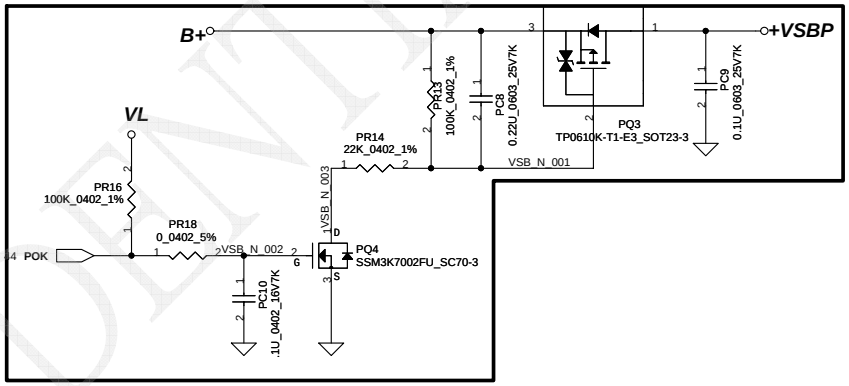
PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

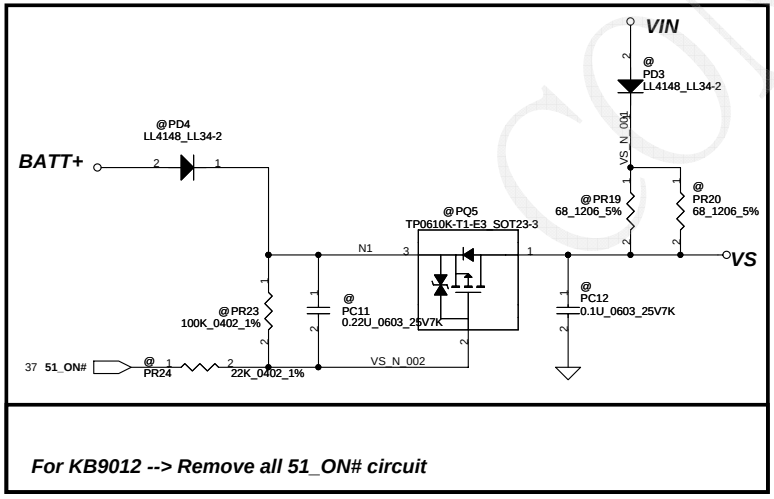
For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU1 circuit, but keep PR56
PH1, PR2, PQ1, PR7,PQ15,PR73,PR56



Change DC040007T0L to DC041112050

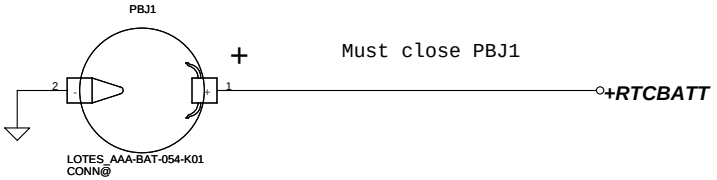






For KB9012 --> Remove all 51_ON# circuit

RTC Battery



Change RTC For Cost Down
SP07000H700

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for reverse input protection

PQ106 SI1304BDL-T1-E3_SC70-3
PR103 1M_0402_5%
PR104 3M_0402_5%

1UH_FDSD0630-H-1R0M-P3_11A_20%

VIN
PQ101 TPCA8059-H_PPAK56-8-5
P1
PQ102 DMG4406LSS-13 1N SO8
P2
PL102
PR101 0.01_1206_1%
B+
PQ103 DMG4406LSS-13 1N SO8

PC112 2200P_0402_50V7K
PR105 @ 0_0402_5%
PC110 0.1U_0402_25V6
PC129 10U_0805_25V6K
PC130 10U_0805_25V6K
PC111 10U_0805_25V6K
PC105 10U_0805_25V6K
PC104 10U_0805_25V6K
PC103 10U_0805_25V6K
PC102 @ 0.1U_0402_25V6
PC101 0.1U_0402_25V6
PC114 0.01U_0402_50V7K
PR106 @ 0_0402_5%

BQ24725_ACDRV
BQ24725_BATDRV
PR107 4.12K_0603_1%

PD101 BAS40CW_SOT323-3
PC115 0.1U_0402_25V6
PC113 0.1U_0402_25V6
0.047U_0402_25V7K
PC116
PR110 10_1206_1%
PR111 2.2_0603_5%
PD102 RB751V-40_SOD323-2
PC117 0.1U_0603_25V7K
PC118 1U_0603_25V6K
PC119 1U_0603_25V6K
PQ104 AON7408L
PR125 0_0402_5%
DH_CHG
PR108 4.12K_0603_1%
PR109 4.12K_0603_1%
PL101 4.7UH_ETQP3W4R7WFN_5.5A_20%
PR102 0.02_1206_1%
BATT+
PQ105 AO4468L_SO8
PR114 @ 4.7_1206_5%
PC123 @ 680P_0402_50V7K
PC121 0.1U_0402_25V6
PC122 0.1U_0402_25V6
PC120 @ 10U_0805_25V6K
PC106 10U_0805_25V6K
PC107 10U_0805_25V6K
PC108 2200P_0402_50V7K
PC109 0.01U_0402_50V7K

PU101
BQ24725RGRR_VQFN20_3P5X3P5
PAD VCC PHASE HIDRV BTST REGN
ACN LODRV
ACP GND
CMSRC SRP
ACDRV SRN
ACOK BATDRV
ACDET IOUT SDA SCL ILIM

PR115 10_0603_1%
PR116 6.8_0603_5%
PC124 0.1U_0603_16V7K

Remember to change PC124 from SE000006S80
to SE025104K80 (2011-02-22)

+3VALW
@PR117 10K_0402_1%
+3VL
PR126 10K_0402_1%
14,20,39 ACIN
PR118 10K_0402_1%
VIN
PR120 255K_0402_1%
Pre_chg
@PD8 RB751V-40_SOD323-2
PR119 120K_0402_1%
PR121 100K_0402_1%
PC125 0.01U_0402_25V7K
PR122 154K_0402_1%
PC126 0.1U_0402_25V6
PR123 66.5K_0402_1%
PR124 100_0402_5%
PC127 100P_0402_50V8J

EC_SMB_CK1 39,42
EC_SMB_DA1 39,42
ADP_I 39,42

Please locate the RC
Near EC chip
2011-02-22

Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	

ILIM and external DPM
3.97A

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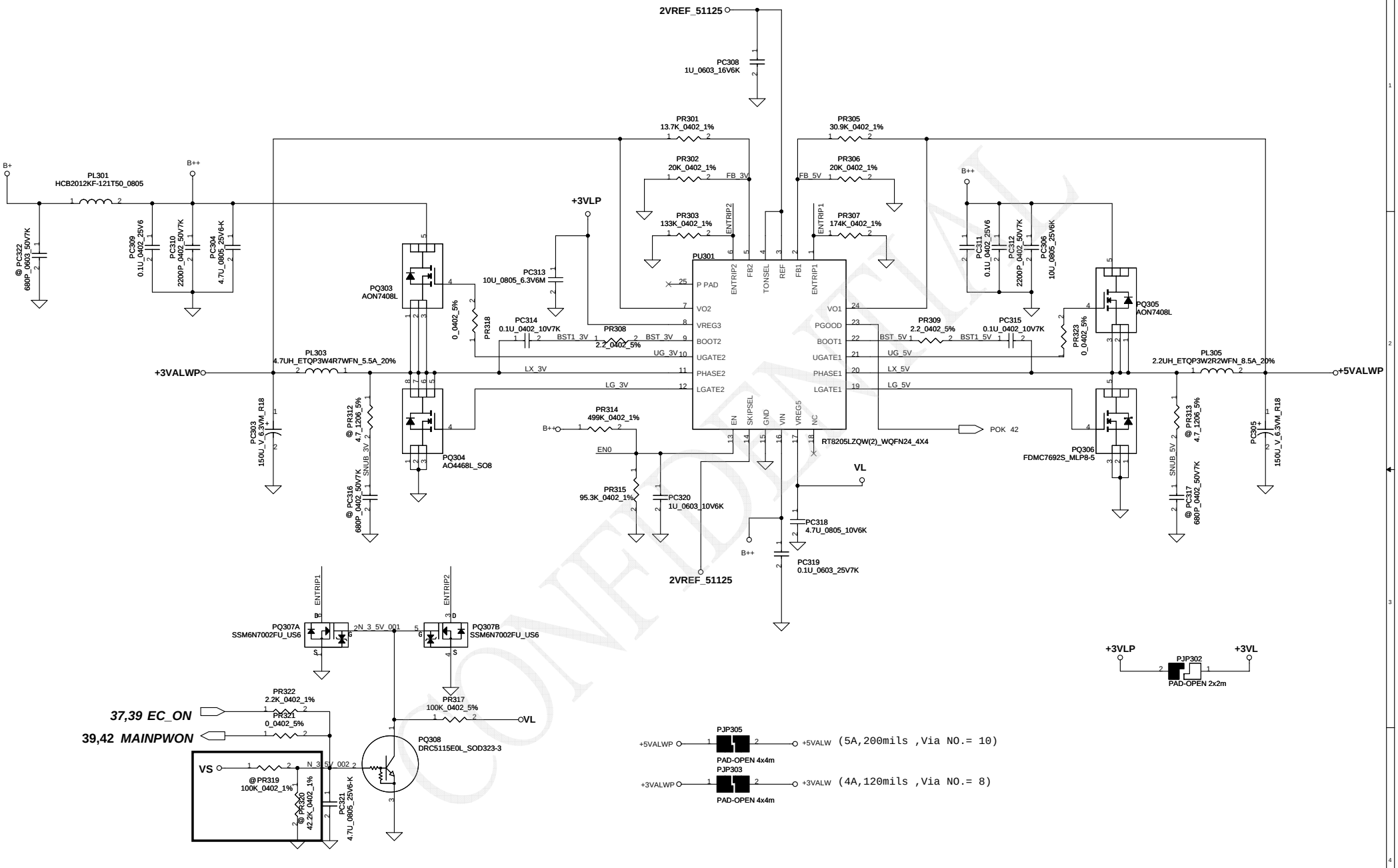

For KB930 --> Keep PR319, Remove PR322
For KB9012 (Red square) --> Remove PR319
Keep PR322

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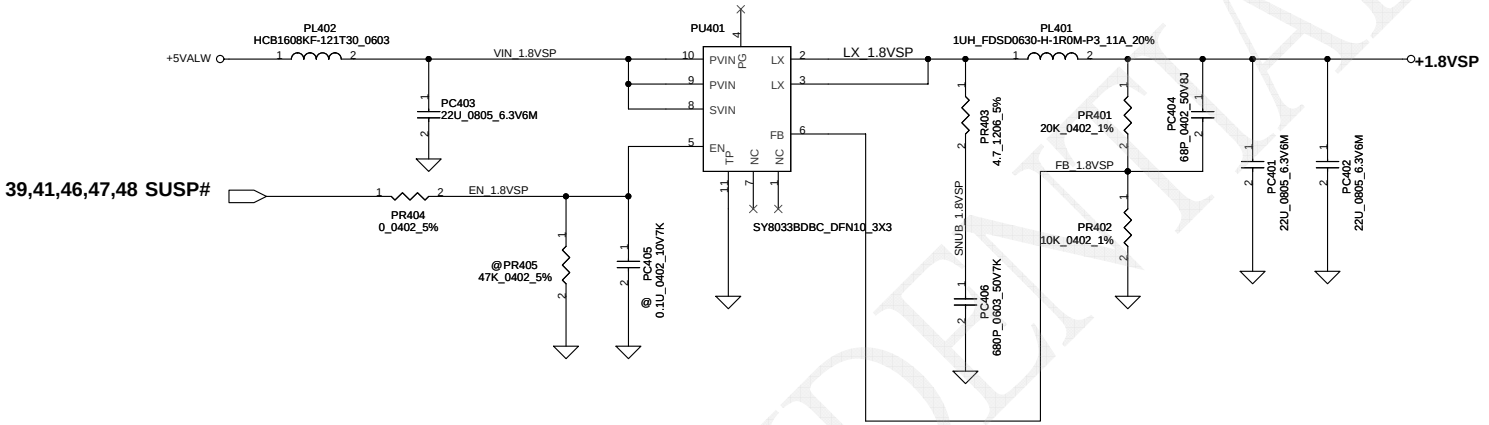

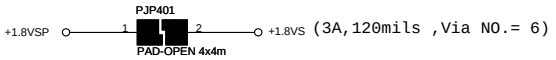

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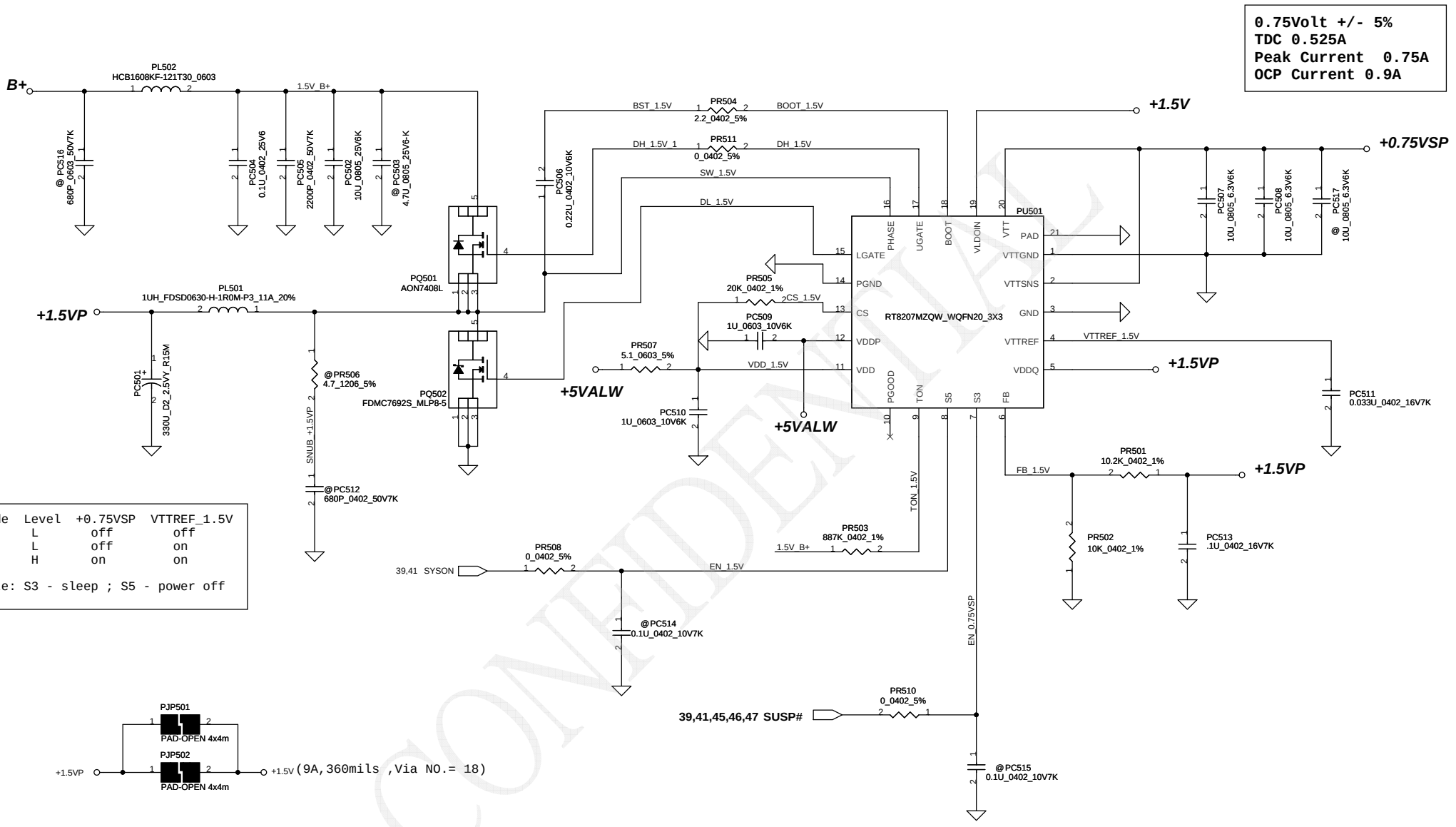

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

Compal Electronics, Inc.

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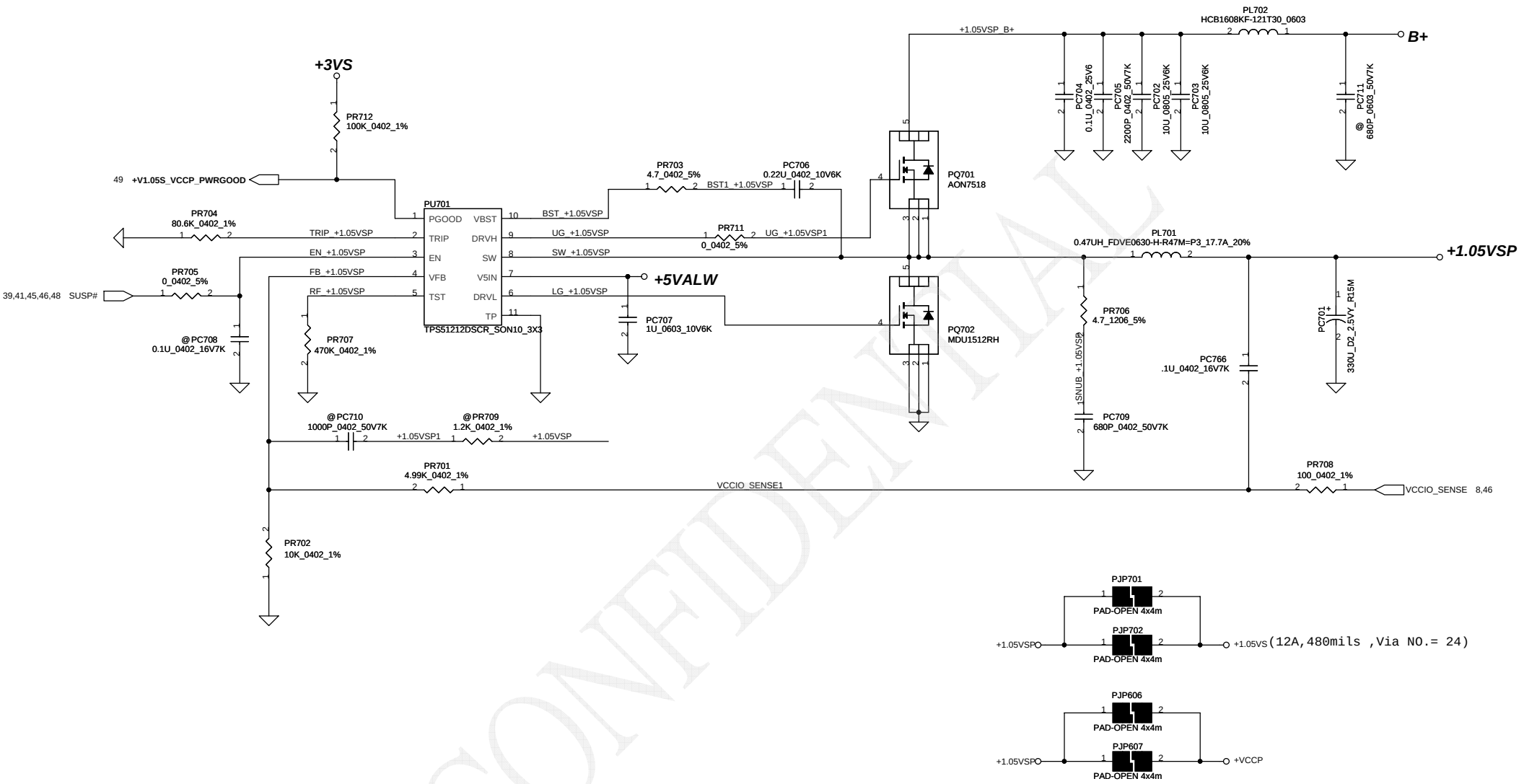

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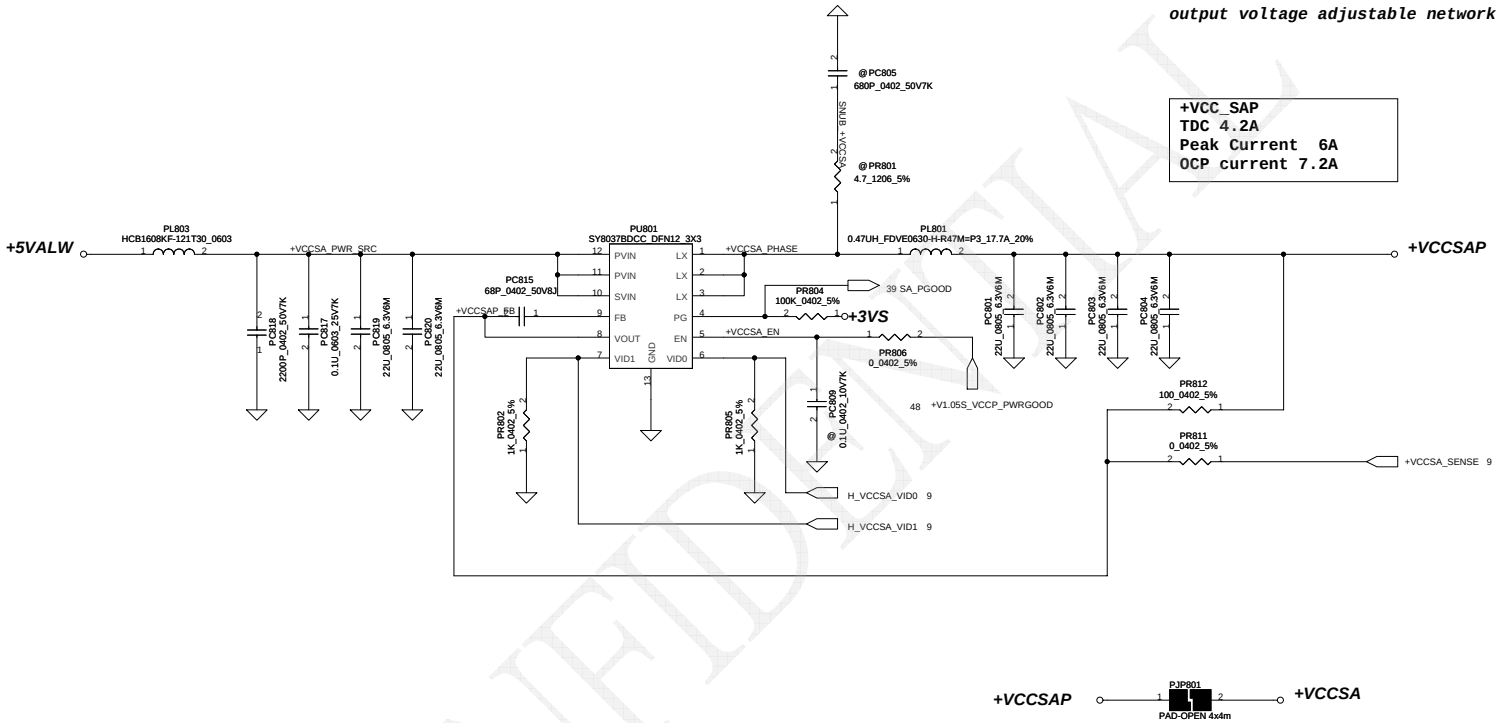
The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A



Security Classification	Compal Secret Data		
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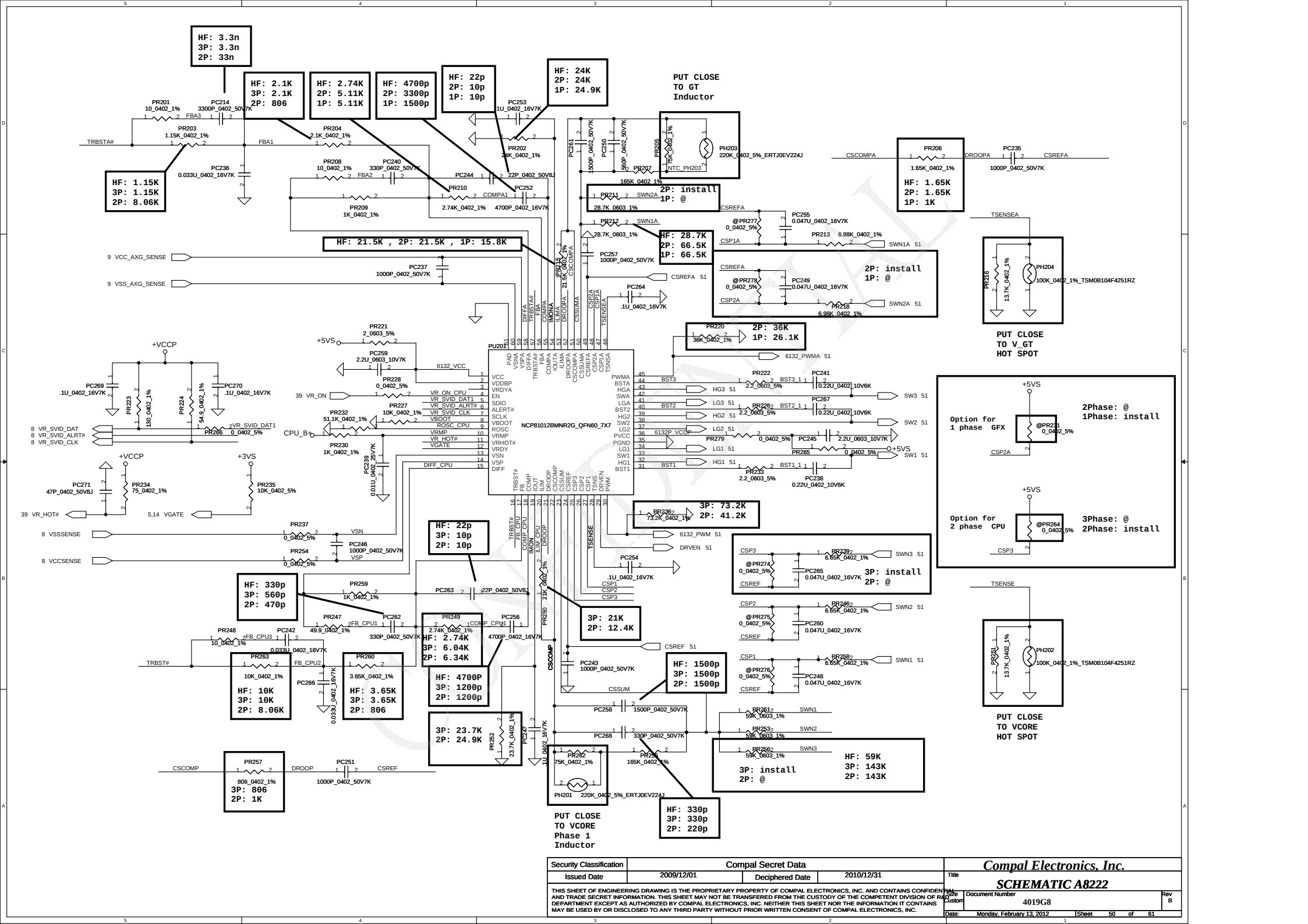

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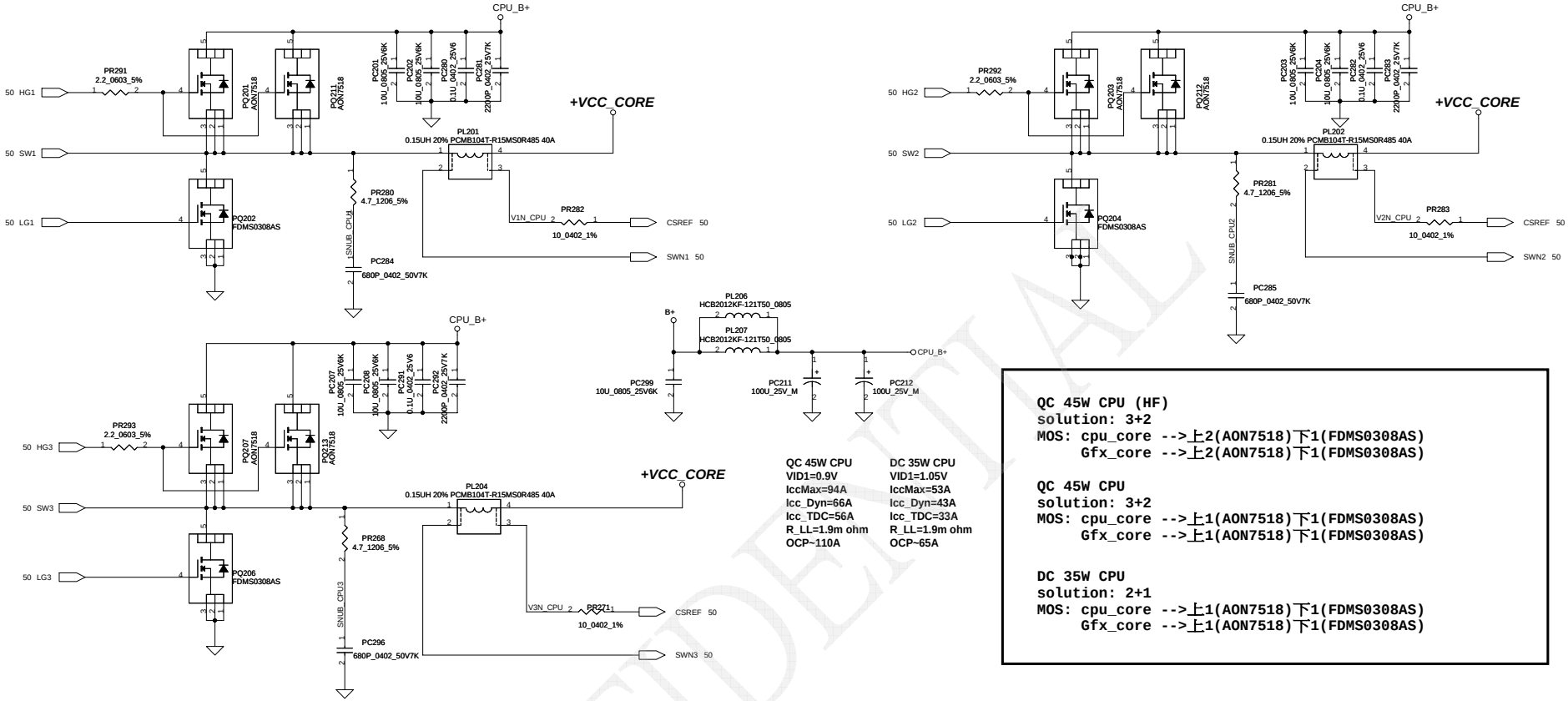
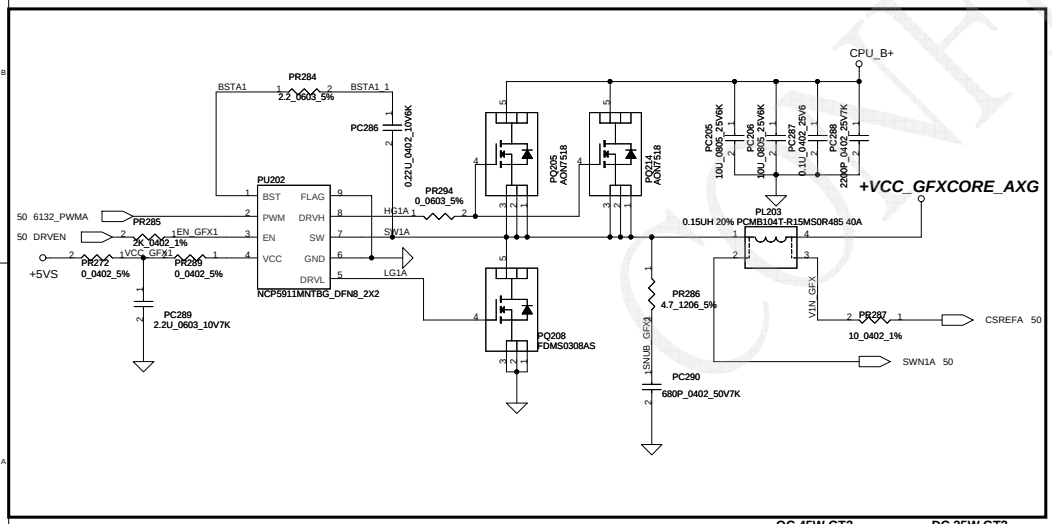


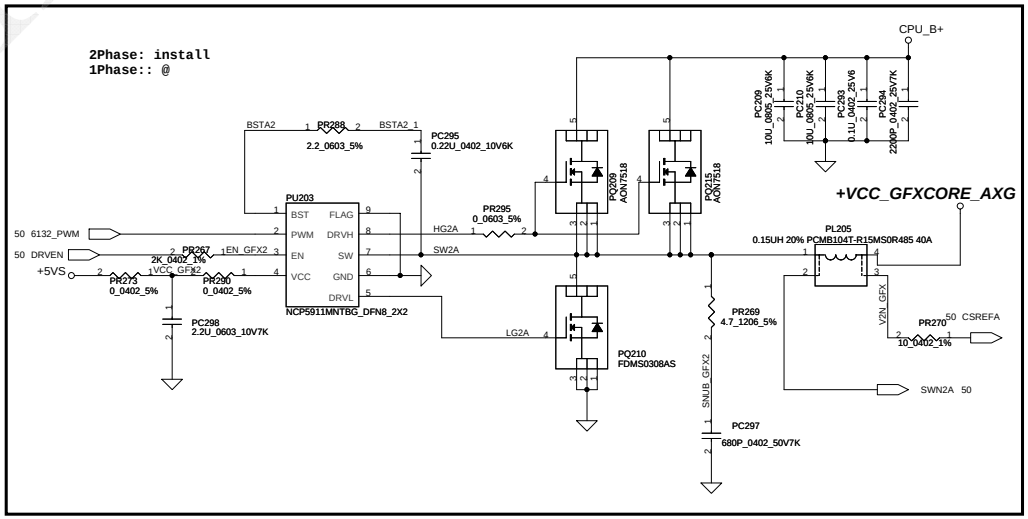
QC 45W CPU	DC 35W CPU
VID1=0.9V	VID1=1.05V
IccMax=94A	IccMax=53A
Icc_Dyn=66A	Icc_Dyn=43A
Icc_TDC=56A	Icc_TDC=33A
R_LL=1.9m ohm	R_LL=1.9m ohm
OCP~110A	OCP~65A

QC 45W CPU (HF)
solution: 3+2
MOS: cpu_core -->上2(AON7518)下1(FDMS0308AS)
Gfx_core -->上2(AON7518)下1(FDMS0308AS)

QC 45W CPU
solution: 3+2
MOS: cpu_core -->上1(AON7518)下1(FDMS0308AS)
Gfx_core -->上1(AON7518)下1(FDMS0308AS)

DC 35W CPU
solution: 2+1
MOS: cpu_core -->上1(AON7518)下1(FDMS0308AS)
Gfx_core -->上1(AON7518)下1(FDMS0308AS)





QC 45W GT2	DC 35W GT2
VID1=1.23V	VID1=1.23V
IccMax=46A	IccMax=33A
Icc_Dyn=37A	Icc_Dyn=20.2A
Icc_TDC=38A	Icc_TDC=21.5A
R_LL=3.9m ohm	R_LL=3.9m ohm
OCP~55A	OCP~40A

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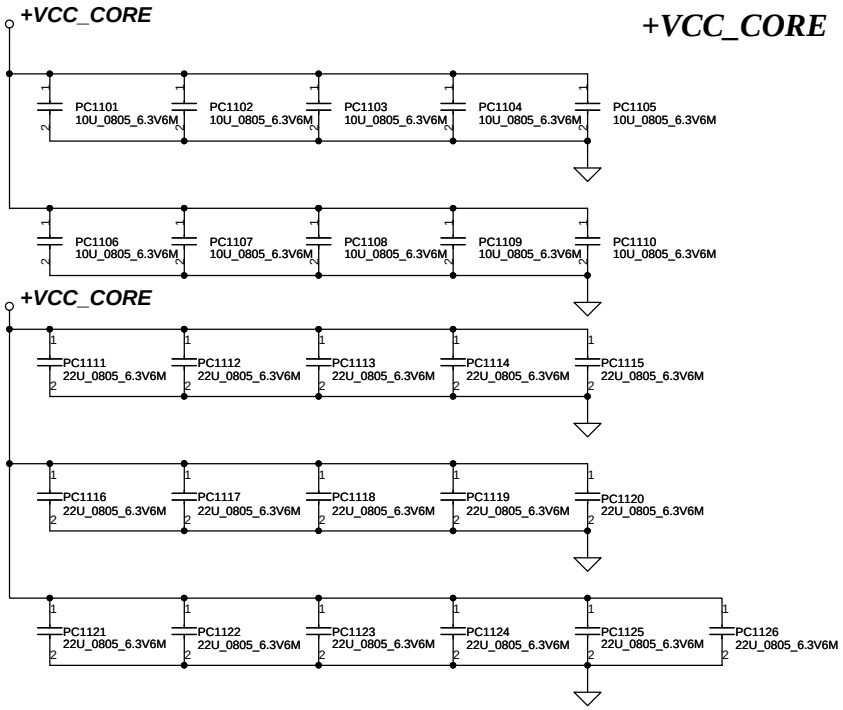

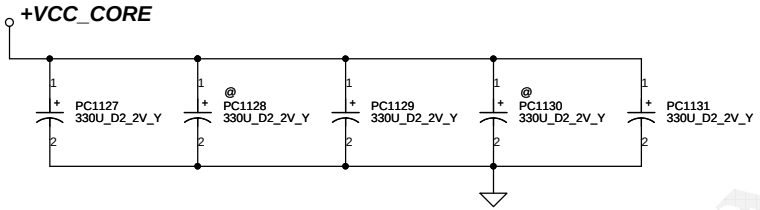

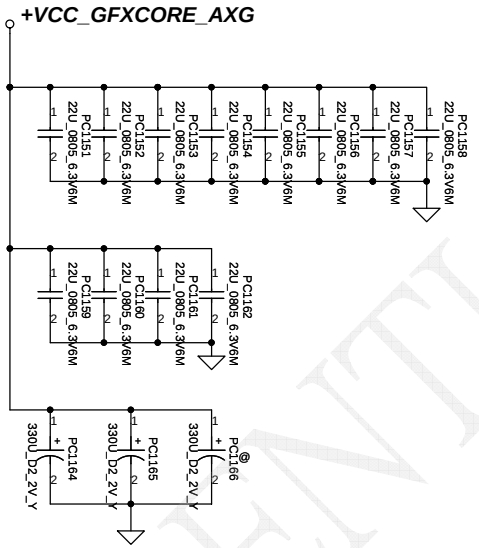

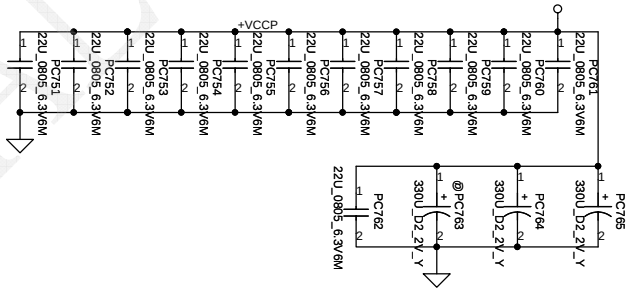

Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites

Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

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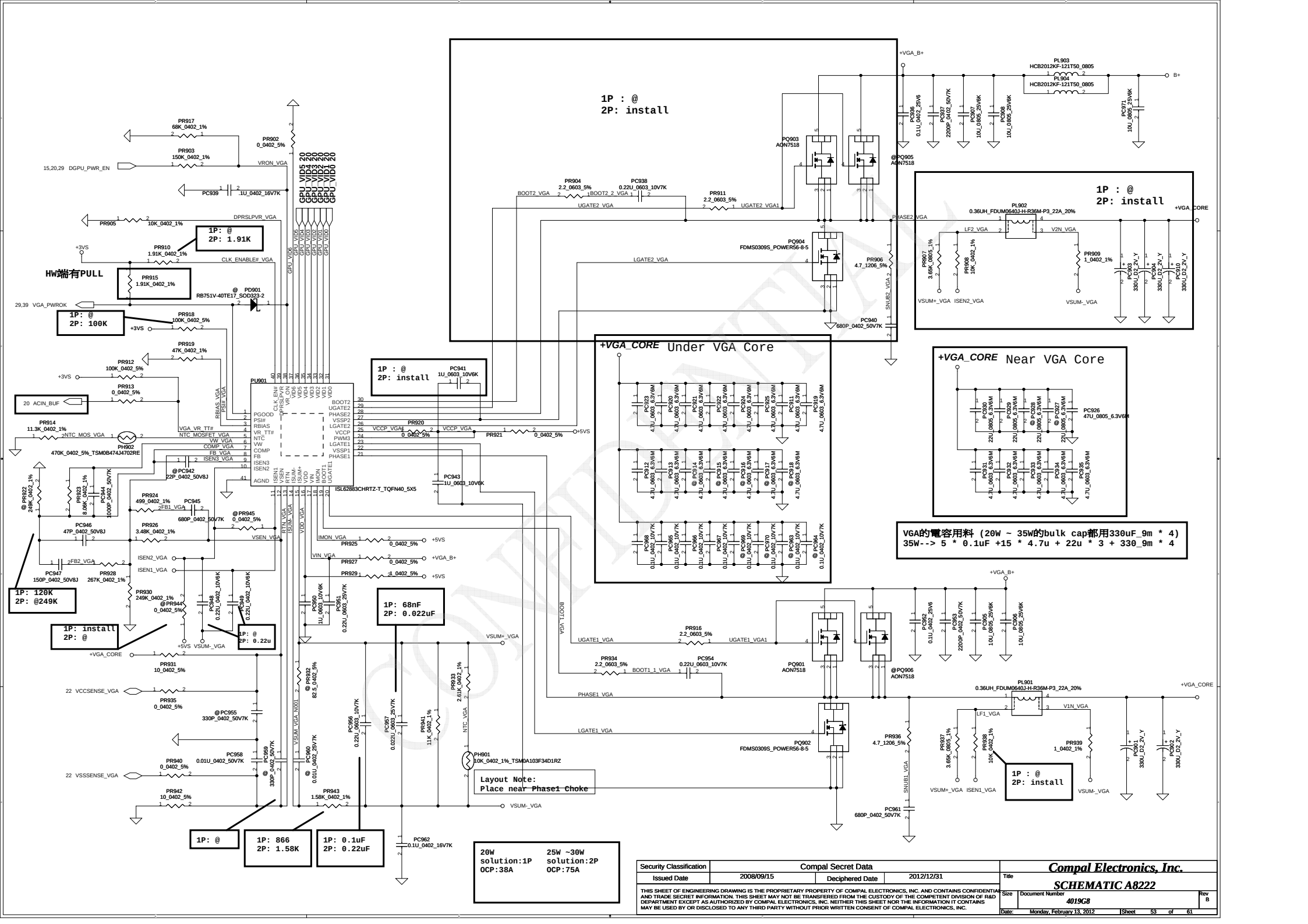
1P : @
2P: install
+VGA_B+
PL903
HCB2012KF-121T50_0805
PL904
HCB2012KF-121T50_0805
B+
PC936 0.1U_0402_25V6
PC937 2200P_0402_50V7K
PC907 10U_0805_25V6K
PC908 10U_0805_25V6K
PC971 10U_0805_25V6K
PQ903 AON7518
@PQ905 AON7518
PR904 2.2_0603_5%
PC938 0.22U_0603_10V7K
BOOT2_VGA
BOOT2_2_VGA
UGATE2_VGA
PR911 2.2_0603_5%
UGATE2_VGA1
PHASE2_VGA
LGATE2_VGA
PQ904 FDMS0309S_POWER56-8-5
PR906 4.7_1206_5%
SNUB2_VGA
PC940 680P_0402_50V7K
1P : @
2P: install
+VGA_CORE
PL902
0.36UH_FDUM0640J-H-R36M-P3_22A_20%
LF2_VGA
V2N_VGA
PR907 3.65K_0805_1%
PR908 10K_0402_1%
PR909 1_0402_1%
PC903 330U_D2_2V_Y
PC904 330U_D2_2V_Y
PC910 330U_D2_2V_Y
VSUM+_VGA
ISEN2_VGA
VSUM-_VGA
+VGA_CORE Under VGA Core
PC923 4.7U_0603_6.3V6M
PC920 4.7U_0603_6.3V6M
PC921 4.7U_0603_6.3V6M
PC922 4.7U_0603_6.3V6M
PC924 4.7U_0603_6.3V6M
PC925 4.7U_0603_6.3V6M
PC911 4.7U_0603_6.3V6M
PC919 4.7U_0603_6.3V6M
PC912 4.7U_0603_6.3V6M
PC913 4.7U_0603_6.3V6M
@ PC914 4.7U_0603_6.3V6M
PC915 4.7U_0603_6.3V6M
@ PC916 4.7U_0603_6.3V6M
PC917 4.7U_0603_6.3V6M
@ PC918 4.7U_0603_6.3V6M
PC868 0.1U_0402_10V7K
PC865 0.1U_0402_10V7K
PC866 0.1U_0402_10V7K
PC867 0.1U_0402_10V7K
@ PC869 0.1U_0402_10V7K
@ PC870 0.1U_0402_10V7K
@ PC863 0.1U_0402_10V7K
@ PC864 0.1U_0402_10V7K
+VGA_CORE Near VGA Core
PC926 47U_0805_6.3V6M
PC930 22U_0805_6.3V6M
PC929 22U_0805_6.3V6M
@ PC928 22U_0805_6.3V6M
@ PC927 22U_0805_6.3V6M
PC931 4.7U_0603_6.3V6M
PC932 4.7U_0603_6.3V6M
PC933 4.7U_0603_6.3V6M
PC934 4.7U_0603_6.3V6M
PC935 4.7U_0603_6.3V6M
VGA的電容用料 (20W ~ 35W的bulk cap都用330uF_9m * 4)
35W--> 5 * 0.1uF +15 * 4.7u + 22u * 3 + 330_9m * 4
PR917 68K_0402_1%
PR902 0_0402_5%
PR903 150K_0402_1%
15,20,29 DGPU_PWR_EN
VRON_VGA
PC939 .1U_0402_16V7K
GPU_VID5 20
GPU_VID4 20
GPU_VID3 20
GPU_VID2 20
GPU_VID1 20
GPU_VID0 20
PR905 10K_0402_1%
DPRSLPVR_VGA
1P: @
2P: 1.91K
+3VS
PR910 1.91K_0402_1%
CLK_ENABLE#_VGA
HW端有PULL
PR915 1.91K_0402_1%
@ PD901 RB751V-40TE17_SOD323-2
29,39 VGA_PWROK
1P: @
2P: 100K
PR918 100K_0402_5%
PR919 47K_0402_1%
PR912 100K_0402_5%
PR913 0_0402_5%
20 ACIN_BUF
PU901
PGOOD
PSI#
RBIAS
VR_TT#
NTC
VW
COMP
FB
ISEN3
ISEN2
AGND
CLK_EN#
DPRSLPVR
VR_ON
VID5
VID4
VID3
VID2
VID1
VID0
BOOT2
UGATE2
PHASE2
VSSP2
LGATE2
VCCP
PWM3
LGATE1
VSSP1
PHASE1
ISL62883CHRTZ-T_TQFN40_5X5
RBIAS_VGA
PSI#_VGA
VGA_VR_TT#
NTC_MOS_VGA
NTC_MOSFET_VGA
VW_VGA
COMP_VGA
FB_VGA
ISEN3_VGA
PH902 470K_0402_5%_TSM0B474J4702RE
PR914 11.3K_0402_1%
@ PC942 22P_0402_50V8J
PR922 249K_0402_1%
PR923 8.06K_0402_1%
PC944 1000P_0402_50V7K
PR924 499_0402_1%
FB1_VGA
PC945 680P_0402_50V7K
@ PR945 0_0402_5%
PC946 47P_0402_50V8J
PR926 3.48K_0402_1%
VSEN_VGA
FB2_VGA
PC947 150P_0402_50V8J
PR928 267K_0402_1%
1P: 120K
2P: @249K
PR930 249K_0402_1%
@ PR944 0_0402_5%
1P: install
2P: @
PC948 0.22U_0402_10V6K
PC949 0.22U_0402_10V6K
1P: @
2P: 0.22u
+5VS
VSUM-_VGA
+VGA_CORE
PR931 10_0402_5%
22 VCCSENSE_VGA
PR935 0_0402_5%
@ PC955 330P_0402_50V7K
22 VSSSENSE_VGA
PR940 0_0402_5%
PC958 0.01U_0402_50V7K
PC959 330P_0402_50V7K
PR942 10_0402_5%
1P: @
1P: 866
2P: 1.58K
1P: 0.1uF
2P: 0.22uF
PC962 0.1U_0402_16V7K
1P : @
2P: install
PC941 1U_0603_10V6K
PR920 0_0402_5%
VCCP_VGA
PR921 0_0402_5%
+5VS
PC943 1U_0603_10V6K
IMON_VGA
PR925 0_0402_5%
VIN_VGA
PR927 0_0402_5%
+VGA_B+
PR929 0_0402_5%
PC950 1U_0603_10V6K
PC951 0.22U_0603_25V7K
1P: 68nF
2P: 0.022uF
PR932 82.5_0402_5%
PR933 2.61K_0402_1%
PC956 0.22U_0603_10V7K
PC957 0.022U_0603_25V7K
PR941 11K_0402_1%
NTC_VGA
PH901 10K_0402_1%_TSM0A103F34D1RZ
Layout Note:
Place near Phase1 Choke
PC960 0.01U_0402_25V7K
VSUM_VGA_N001
BOOT1_VGA
UGATE1_VGA
PR916 2.2_0603_5%
UGATE1_VGA1
PR934 2.2_0603_5%
BOOT1_1_VGA
PC954 0.22U_0603_10V7K
PQ901 AON7518
@PQ906 AON7518
PC952 0.1U_0402_25V6
PC953 2200P_0402_50V7K
PC905 10U_0805_25V6K
PC906 10U_0805_25V6K
PHASE1_VGA
LGATE1_VGA
PQ902 FDMS0309S_POWER56-8-5
PR936 4.7_1206_5%
SNUB1_VGA
PC961 680P_0402_50V7K
PL901
0.36UH_FDUM0640J-H-R36M-P3_22A_20%
LF1_VGA
V1N_VGA
PR937 3.65K_0805_1%
PR938 10K_0402_1%
PR939 1_0402_1%
PC901 330U_D2_2V_Y
PC902 330U_D2_2V_Y
VSUM+_VGA
ISEN1_VGA
VSUM-_VGA
1P : @
2P: install
20W
solution:1P
OCP:38A
25W ~30W
solution:2P
OCP:75A
Security Classification
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Issued Date
2008/09/15
Deciphered Date
2012/12/31
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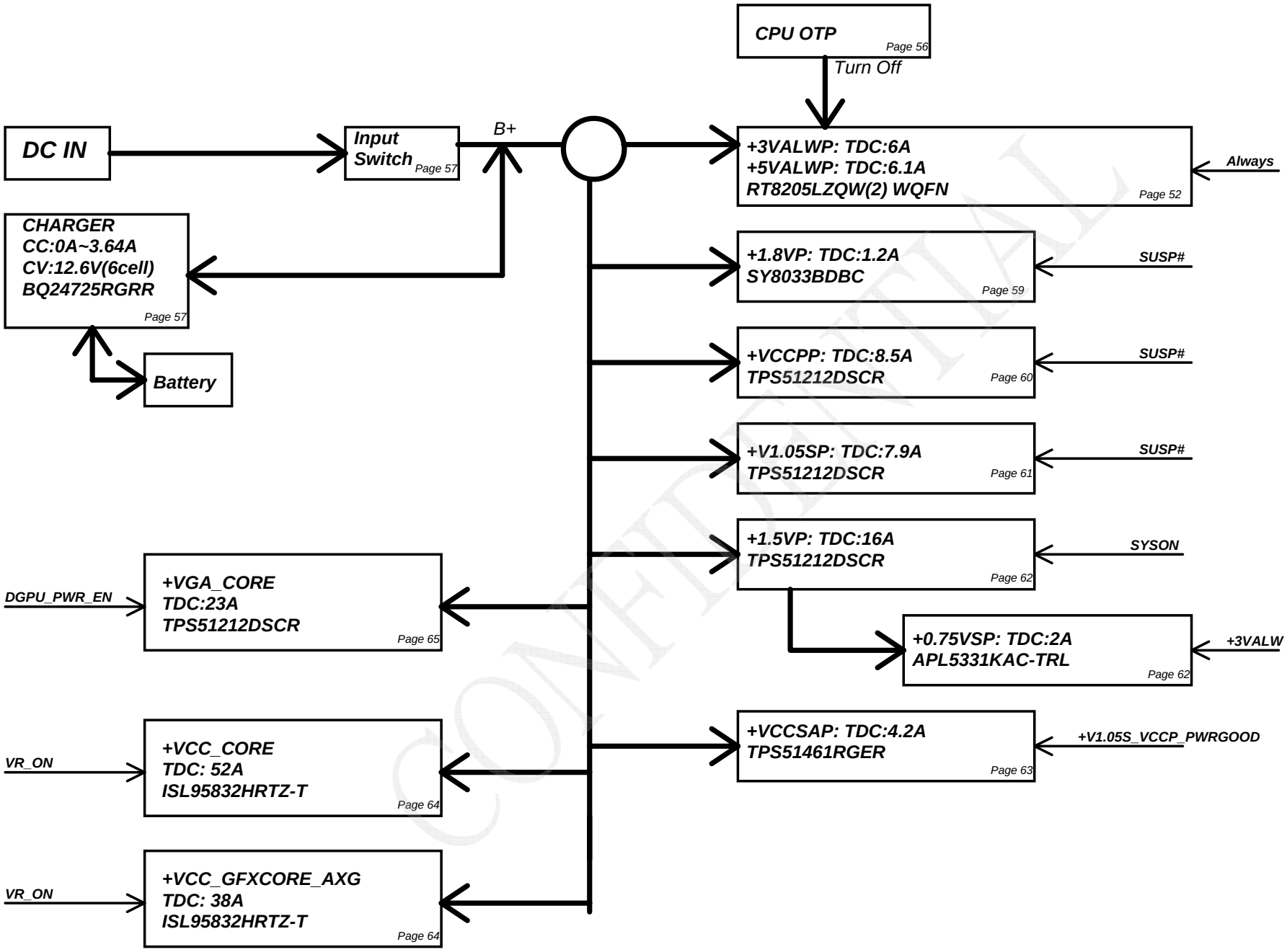
Power block



Security Classification	Compal Secret Data		
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Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

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Issued Date	2008/09/15	Deciphered Date	2012/12/31

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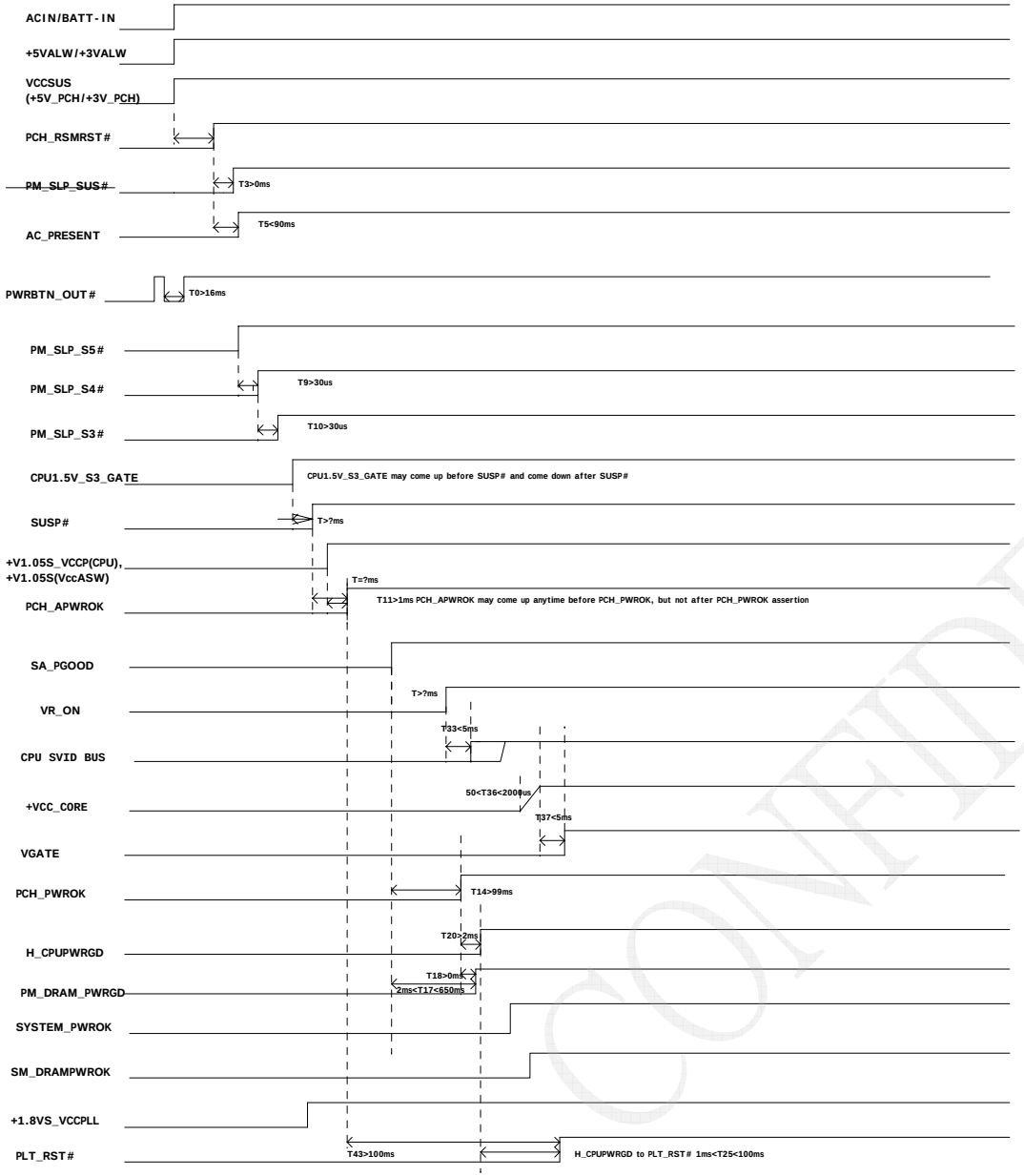
Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER01		HW Design	0.2	14 05	Delete R205 Un-stuff R577, Stuff R576	09/21	
ER02		For non AI co-lay	0.2	37	Add R745,R746 for non AI AI parts change to AI@	09/21	
ER03	+3VS Leakage	HW Design	0.2	12 13 40	Change R132/R134 PU power to +3V_SPI Delete Q3.A/B Add R135, R137 Delete R552, R556	09/21	
ER04	Can`t detect USB30 (JUSB2)	HW Design	0.2	36	Swap U90.39/40 to U90.36/37 net Change R1040 to 47K from 4.7K ohm Add Reserve R1029	09/21	
ER05		Design change for card reader	0.2	34	Add Q20,R773,R775 Reserve R768, R774 Change Card reader Conn	09/22	(10/3 - follow K45 change Dual FET location from Q63 to Q20)
ER06		HW Design / VGA sequence	0.2	29	Change to Q3(AO3404L) from U22(AO4430L) Change R433 to 0 ohm, R432 to 10K ohm Un stuff C396	09/21	
ER07		HW Design	0.2	36	Change R1049 to 330k Change Q904 to AO3404L from AP2301GN Delete R1046, Add R747	09/21	
ER08		HW Design	0.2	42	Change Q33 to AO3413L from AP2301GN	09/21	
ER09		HW Design	0.2	18	Add un stuff R290	09/23	
ER10		Refer to ORB	0.2	05	Change R577.2 power rail from +3VS to +3V_PCH	10/04	
ER11		Refer to ORB	0.2	13	Del R135, R137. Change SML1CLK to PCH_SML1CLK Change SML1DATA to PCH_SML1DATA	10/04	
ER12		HW Design	0.2	40	Del Y5 , C545 , C546	10/04	
ER13		Refer to purchaser suggestion	0.2	15	Replace R230 NR with R780-R783. Replace R237 NR with R784-R787. Replace R242 NR with R792, R793, R288.	10/04	
ER14		Refer to purchaser suggestion	0.2	29 31 42	Change C387, C389, C399, C447, C602 PN	10/04	
ER15		HW Design	0.2	40	Del U33.123 EC_CRY2 net name	10/04	
ER16	DRAMRST_CNTRL_PCH signal timing	Reserved for Instant-On function.	0.2	13	Add R750	10/04	(10/06 - Change location from R1082 to R750, And Change its tolerance from 1% to 5%).
ER17		EMC request to reserve these caps.	0.2	36	Add C1045-C1048	10/04	
ER18			0.2	43-55	Update Power circuit (1003)	10/04	
ER19		Instant-On function - DRAMRST control by PCH.	0.2	13	Un-stuff R157, Stuff R750	10/06	
ER20		ME Design Change.	0.2	38	Change H16, H17, H22 screw hole type to 3P5. (dGPU & VRAM)	10/07	
ER21			0.2	43-55	Update Power circuit (1011) - Del PC1163.	10/11	
ER22		Refer to ORB design	0.2	14 40	un-stuff D2, Add R751 un-stuff D32, R547, Add R752 Assign U33.18 to AC_PRESENT signal.	10/13	
ER23		Fine-tune timing.	0.2	29 42	change R432 from 100R to 10K. change R435 from 10R to 200R. change R607 from 220R to 10R.	10/13	

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER24		Follow to ORB	0.2	05	Un-stuff R576, Stuff 0R to R577.	10/13	
ER25		change for GPU H/W strapping STRAP1 to PL 45K ohm to enhanced the PCIe PEG driving.	0.2	22	Change R349 from 34.8K to 45.3K	10/13	
ER26		Refer to Intel review feedback item 5.	0.2	09	Add R277 0R 0805 5%	10/13	
ER27		Refer to Intel review feedback item 11.	0.2	09	Add 149	10/13	
ER28		Refer to Intel review feedback item 33.	0.2	31	Revise SATA P/N signals.	10/13	
ER29		Refer to Intel review feedback item 37.	0.2	18	Del L6, Add R289	10/13	
ER30		Refer to Intel review feedback item 40.	0.2	17	Del L4, Add R293	10/13	
ER31		Refer to Intel review feedback item 42.	0.2	42	Add R230	10/13	
ER32		Refer to Intel review feedback item 43.	0.2	42	on Stuff R244	10/18	
ER33		Refer test report to fine-tune oscillation frequency	0.2	12	Change Y1 P/N, Change C144, C145 to 18pF.	10/14	
ER34		Refer test report to fine-tune oscillation frequency	0.2	13	Change Y2 P/N, Change C163, C164 to 12pF.	10/14	
ER35		Refer test report to fine-tune oscillation frequency	0.2	20	Change Y3 P/N, Change C901, C900 to 12pF.		
ER36		Refer test report to fine-tune oscillation frequency	0.2	32	Change Y4 P/N, Change C469, C4735 to 12pF.	10/14	
ER37		Refer test report to fine-tune oscillation frequency	0.2	36	Change Y9 P/N.	10/14	
ER38			0.2	43-55	Update Power circuit (1014) - Modify Choke footprint.		
ER39		For EMI request	0.2	32	R484 and R486 change to C219 and C300 to 0.1u.	10/17	
ER40		For LED issue	0.2	39	change LED2 footprint to LED_HT-210UD-UYG_3P	10/17	
ER41		For EMI request	0.2	05	Add R12 0 ohm at H_CPUPWRGD	10/17	
ER42		For SATA GEN2 EA pass.	0.2	31	change R671 to 3.3k ohm.	10/17	
ER43		For EMI request	0.2	16	Add C151 0.1uF to GND on H_THERMTRIP#	10/17	
ER44		For EMI request	0.2	33	1.GND pin3→pin1,USBN9 pin1→Pin2,USBP9 pin2→Pin3 2.GND pin5→pin7,+USB_VCCD pin6,7→pin5,6	10/17	
ER45		For EMI request	0.2	33	Add L34 , L35 , reserve R552, R556 ,R748 , R749	10/17	
ER46		For EMI request	0.2	5 7	remove T2,T3,T4,T5,T6,T7,T8,T9,T46,T47 T38,T39,T40,T41,T42,T43,T10,T11,T45	10/17	
ER47		For Power request	0.2	38 40	Change +3VLP to +3VL	10/17	
ER48		SATA Re-driver 2nd source.	0.2	38	PAR8520@ : U41-U43, R671=3.3K ASM1466@ : 1) Add R426,R405,R419,R403,R396,R417 U41-U43 2) R459, R669, R672 = 4.7K 3) R682, R690, R698 = 2K	10/17	

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER49		For EMI request	0.2	34	remove C620 , C611 , C631	10/18	
ER50		for HW design	0.2	39	change U36 PN to SA00003B900 and C583 unpop	10/18	
ER51		For EMI request.	0.2	05	H_CPUPWRGD net name change to H_CPUPWRGD_R	10/20	
ER52		For T88 request for ROM WP function	0.2	12	Reserve R137 , Q63, pop R135 change EC_PECI to EC_SPI_WP	10/26	
ER53		For EMI request	0.2	13	Add R185	10/20	
ER54		to prevent +3VSG leakage when Optimus.	0.2	20 40	Change ACIN_BUF circuit unstuff R730	10/20	
ER55		For remove MS fuction	0.2	34	Delete R637	10/20	
ER56		For AP2301 EOS issue	0.2	37	change C510,C516,C519,C524 PN to SE026224K80	10/20	
ER57		for EMI request	0.2	40	Add C156 , C157	10/21	
ER58		Reserve for Deep Sx	0.2	14 40	Add unstuff R800,R801,R802,R803,R804,R805 Add PCH_DPWROK,DS_WAKE#,SUSACK#,SUSWARN#	10/19	
ER59		for EMI request	0.2	35	Change L31~L33 PN to SM070000N00	10/26	
ER2-1		For SATA signal driving	0.3	31	Change R668,R671 to 2K ohm for PAR8520 Add 10K ohm (R675,R677,R683,R685) for PAR8520 Unstuff R396,R417,R698,U43 for ASm1466 Unstuff C644,C645,C646	11/22	
ER2-2		For EMI request	0.3	32	Add 0.1uF (C219,C300) Change TS1 to SP050007G00 from SP050006L00	11/22	
ER2-3		For Card reader function	0.3	34	Change SDD2 to U40.21 and SDD3 to U40.20	11/22	
ER2-4		For USB charge & wake function	0.3	37	Add 0 ohm (R809,R810)	11/22	
ER2-5		For WIN8	0.3	12	Add U5 SPI ROM 8M for Win8	11/22	
ER2-6		For change Click Pad from Glide Pad.	0.3	13 39 40 39	Connect SMBUS to click pad. Del SW3,SW4. change JTP1 Add Q64 , R808 Change PU to +3VS (TP_CLK,TP_DATA) Update JTP1(SP01001AE00) connector 8 pin	12/12	
ER2-7		For HDMI LOYALTY	0.3	35	Add 46@ HDMI LOYALTY	11/22	
ER2-8		Change Main source for HDMI power switch	0.3	35	Change U44 SA00004ZB00 to SA00004ZA00	11/22	
ER2-9		For +3VSG leackag when boot first time	0.3	15	Add R443 10k pull down , unstuff R244	12/01	
ER2-		For N13M-GS DID	0.3	22	Update strap pin table	12/01	

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER2-10		HW Design	0.3	42	Change 2N7002 single to dual channel< Q71~Q77> Del R625, Q64 Change Q38 SI4178DY to AO3404AL Add R813 PD 1.5M ohm	12/12	
ER2-11		For USB3.0 chip sequence	0.3	36	Change C1011 to 2.2uf from 1uF << 0402 to 0603 Change R1040 to 51.1k +-1% ohm	12/05	
ER2-12		HW Design	0.3	29 32 41	Change 2N7002 single to dual channel <Q78~Q80> Change 2N7002 single to dual channel <Q81> Change 2N7002 single to dual channel <Q82>	12/05	
ER2-13		HW Design for power saving	0.3	12	Un stuff R111~R113	12/05	
ER2-14		HW Design	0.3	06 42 17	Change C73 SE070473Z80 to SE076473K80 Change C600 SE027224Z80 to SE026224K80 Change C180 SE000008L80 to SE000000I10	12/07	
ER2-15		HW Design	0.3	12 35 42	Change 1U(0603) SE052105Z80 to SE080105K80 Page PCH,HDMI,DCDC,DIMM	12/07	
ER2-16	EMI	EMI request	0.3	15 30 33 34 37 41	Change USB2.0 port & OC#	12/15	
ER2-17		HW Design	0.3	16	Add R812 to GPIO22 PD 10k ohm , Unstuff R252	12/09	
ER2-18		HW Design	0.3	14 40	Un-Stuff R554, Stuff R226 (Change to 10k)	12/12	
ER2-19		Intel New chip of PCH HM76 rev.C1	0.3	PCH	Change U3 PN to SA00005FH10	12/12	
ER2-20		HW Design	0.3		Change All 2n7002 to SB00009Q80 from SB00009620 Change 0.1uF SE102104K00 to SE076104K80	12/12	
ER2-21		EMI request	0.3	35 30	Add 2pF C700~C707 Add R820,R821 & L40(Unstuff)	12/12	
ER2-22		HW Design	0.3	20	Change Q900.2 control pin to +3VSG	12/12	
ER2-23		For EMI request	0.3	39	Change U36 to SA000058600	12/14	
ER2-24		For EMI request	0.3	29	Add Reverse 100pf C710~C715,C717~C723 to +1.5VSG and other power plan	12/15	
ER2-25		For EMI request	0.3	05	Add R12 1k ohm and C640 0.1u Capacitor	12/19	
PR-1		For ASUS request	1.0	40 38	Add PWR_ON_LED1# on U33 Pin 119	01/02	
PR-2		For EMI request	1.0	05	R12 change to 33ohm (SD028330A80)and C640 change to 100p(SE071101J80)	01/03	
PR-3		For power consumption @ AC S5	1.0	29	R432 change to 100K(SD028100380)and C395 change to 0.01u (SE075103K80)	01/03	
PR-4		For ENE request	1.0	39	reserve KSI4,5,6,7 cap 10p to GND	01/06	
PR-5		For debug function	1.0	41	stuff R595	01/06	
PR-6		For GS gen3 support	1.0	22	R352 ,R349 bom structure change to @	01/06	
PR-7		For HW design	1.0	41	change 0 ohm footrprint to R_short change R584 footrprint 1206 to 0805 R_short	01/06	
PR-8		For PLT_RST# leakage when power on	1.0	15	Add R445 and reserve R444 unstuff R234	01/06	
PR-9		For Mos max Vgs voltage tolerance	1.0	29 42	Add R830 amd R831 470k ohm to GND Add R813 1M ohm to GND	01/19	
PR-10		For Asmedia SATA redriver	1.0	31	Change R690 to 1.5K ohm to GND	01/06	

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PR-11		For power consumption	1.0	36 40	modify asmedia power schematic Add USB3_ON at U33 pin 120	01/09	
PR-12		For EMI	1.0	33	Reserve C723~C726 1.8P capacitor to GND	01/13	
PR-13		For HW design	1.0	30 34	C422,C423,C619 footprint change to 0603 from 0805	01/13	
PR-14		For EMI	1.0	42 40	Change C1047 and C606 to 0.1uF Add Reserve C1070	01/17	
PR-15		For HW deaign	1.0	41	Change U37 to SI4178DY-T1-GE3 from AO4478 (WLAN power MOS)	01/17	
PR-16		For power consumption @ AC S5	1.0	42 41	Change R610,R724 to 390k from 47k ohm C599,C592 change to 0.01uF.	01/19	
PR-17		For EMI	1.0	32 5	Change C475 to 10P (SE00000UO00) Change C72 to 12P Add C647	01/30	
IRT-1		For EMI	1.A	30	Add C544 C545	02/08	
IRT-1		For check AI charger exit or not	1.A	40	Change R743 bom structure to AI@	02/10	

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