Compal Confidential

VSKTA Schematics Document

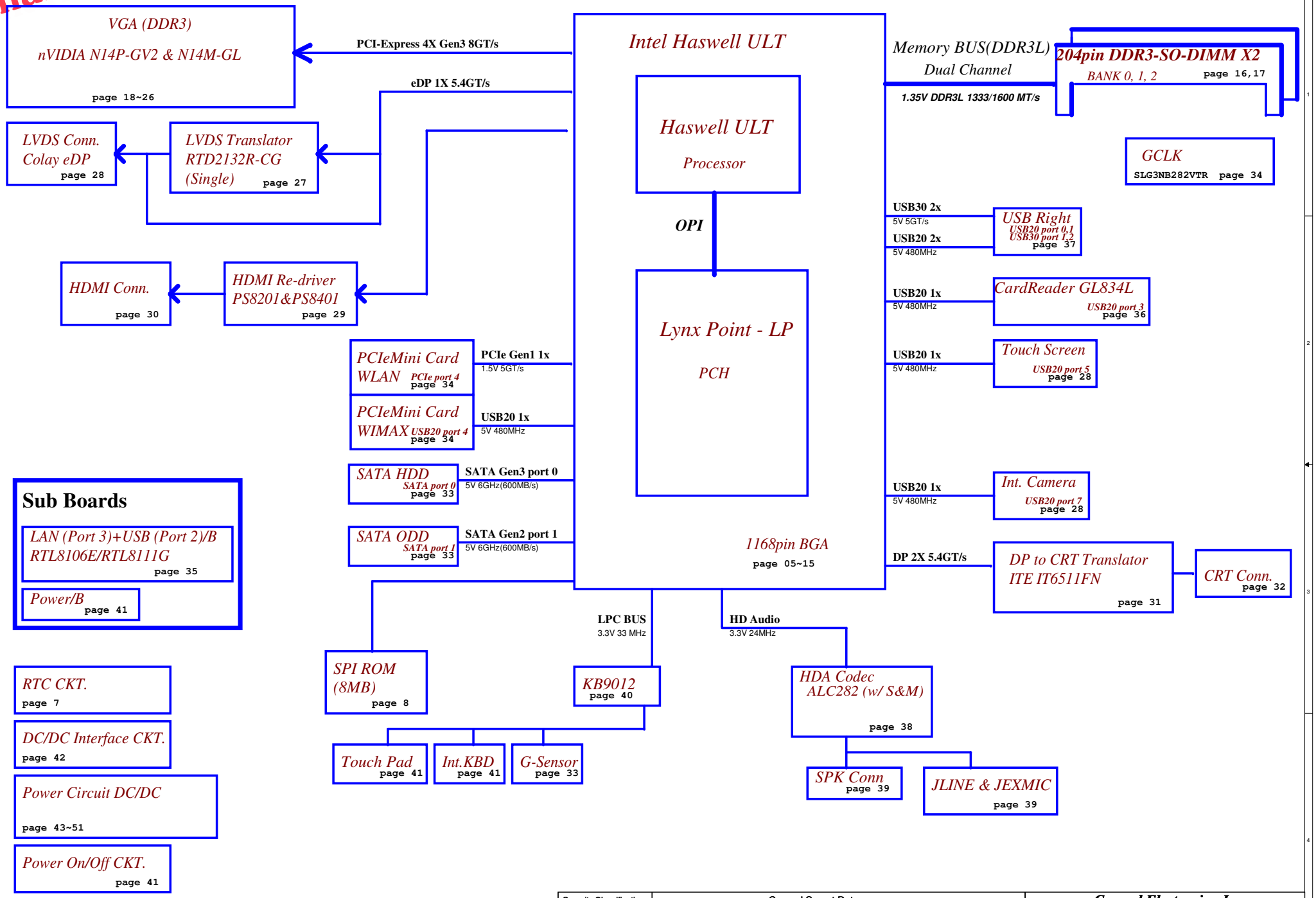
Haswell ULT with DDR3L

nVIDIA N14P-GV2 (Dual Rank)
nVIDIA N14M-GL

LA-9865P REV 2.0 Schematic

Intel Processor (Haswell)
2013-06-21 Rev 2.0

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/10/19	Deciphered Date	2015/10/19
Title	Cover Page		
Size Custom	Document Number VSKTA		Rev 2.0
Date: Friday, June 21, 2013	Sheet 1 of 57		

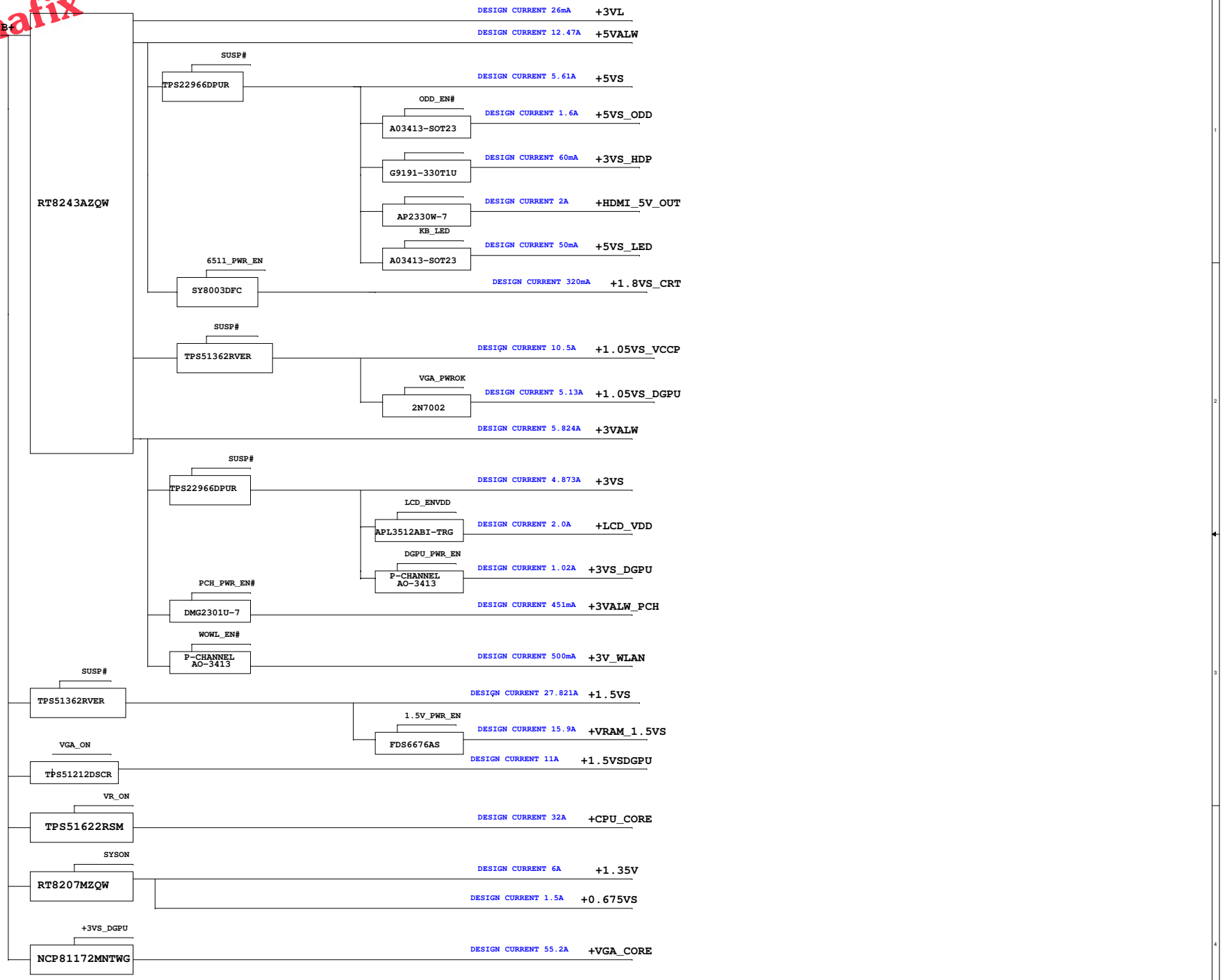


Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

Compal Electronics, Inc.

Title: Block Diagram

Size: B/26	Document Number: VSKTA	Rev: 2.0
Date: Friday, June 21, 2013	Sheet 2 of 57	



Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

Compal Electronics, Inc.			
Title: Power Map			
Size: Custom	Document Number: VSKTA		Rev: 2.0
Date: Friday, June 21, 2013	Sheet 3 of 57		

Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.5VALW +VSB	+1.35V	+5VS +3VS +1.8VS_CRT +1.5VS +CPU_CORE +VGA_CORE +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU +1.05VS_VTT
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

Platform	SKU	CPU	PCH	VGA
				nVIDIA N13P-GL (N13PGL@)

BTO Option Table

Function	SKU	MIC	LAN			
description						
explain						
BTO						

Function							
description							
explain							
BTO							

Function							
description							
explain							
BTO							

Function		
description		
explain		
BTO		

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b

Power	Device	HEX	Address

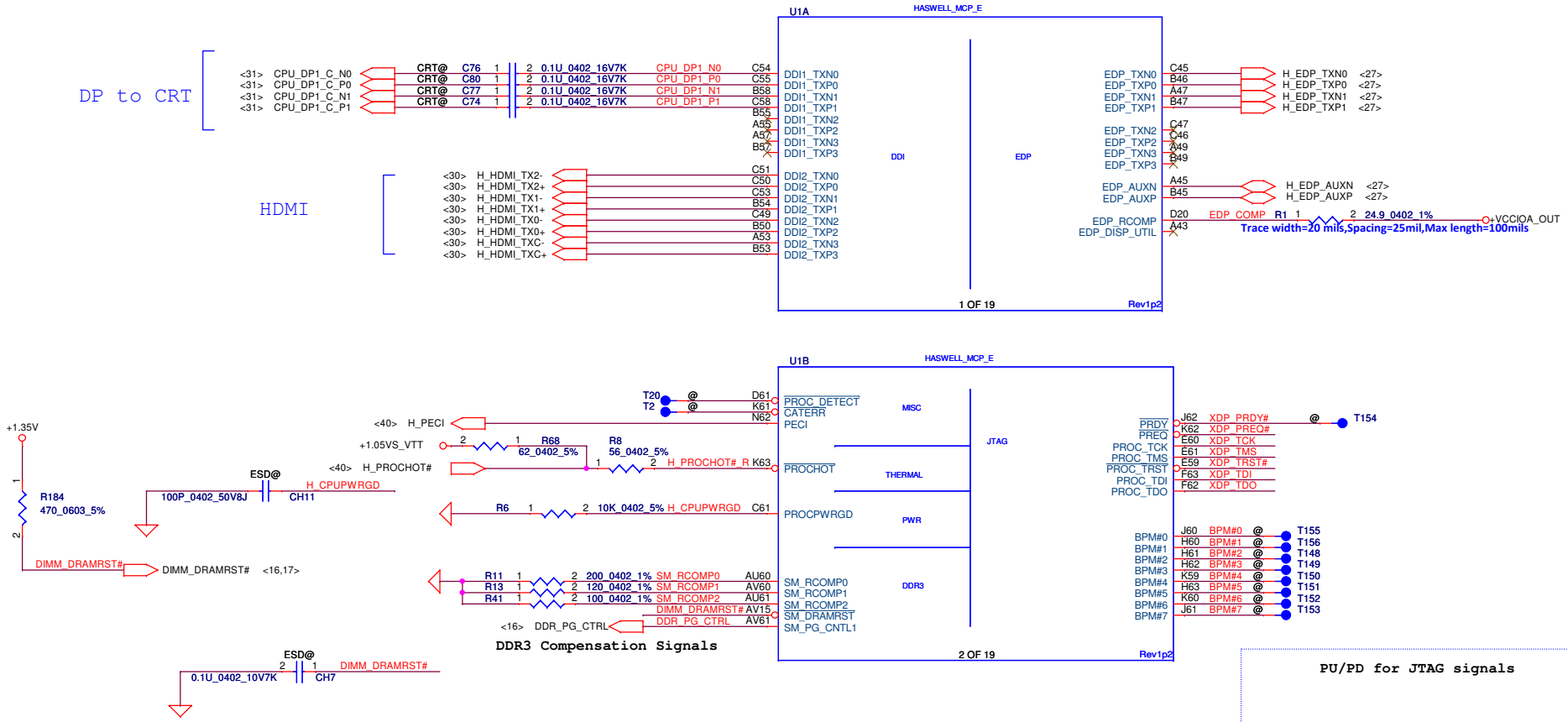
EC SM Bus2 Address

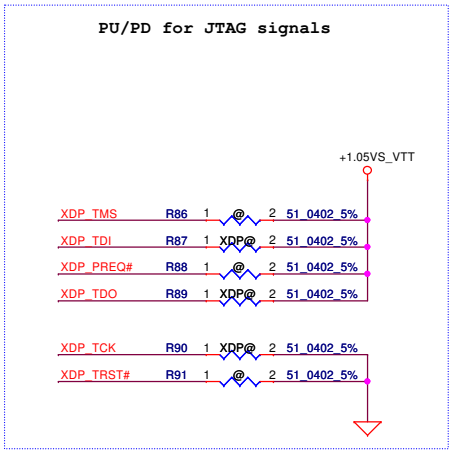
Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9E H	1001 1010 b

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/10/19	Deciphered Date 2015/10/19	Title: Notes List

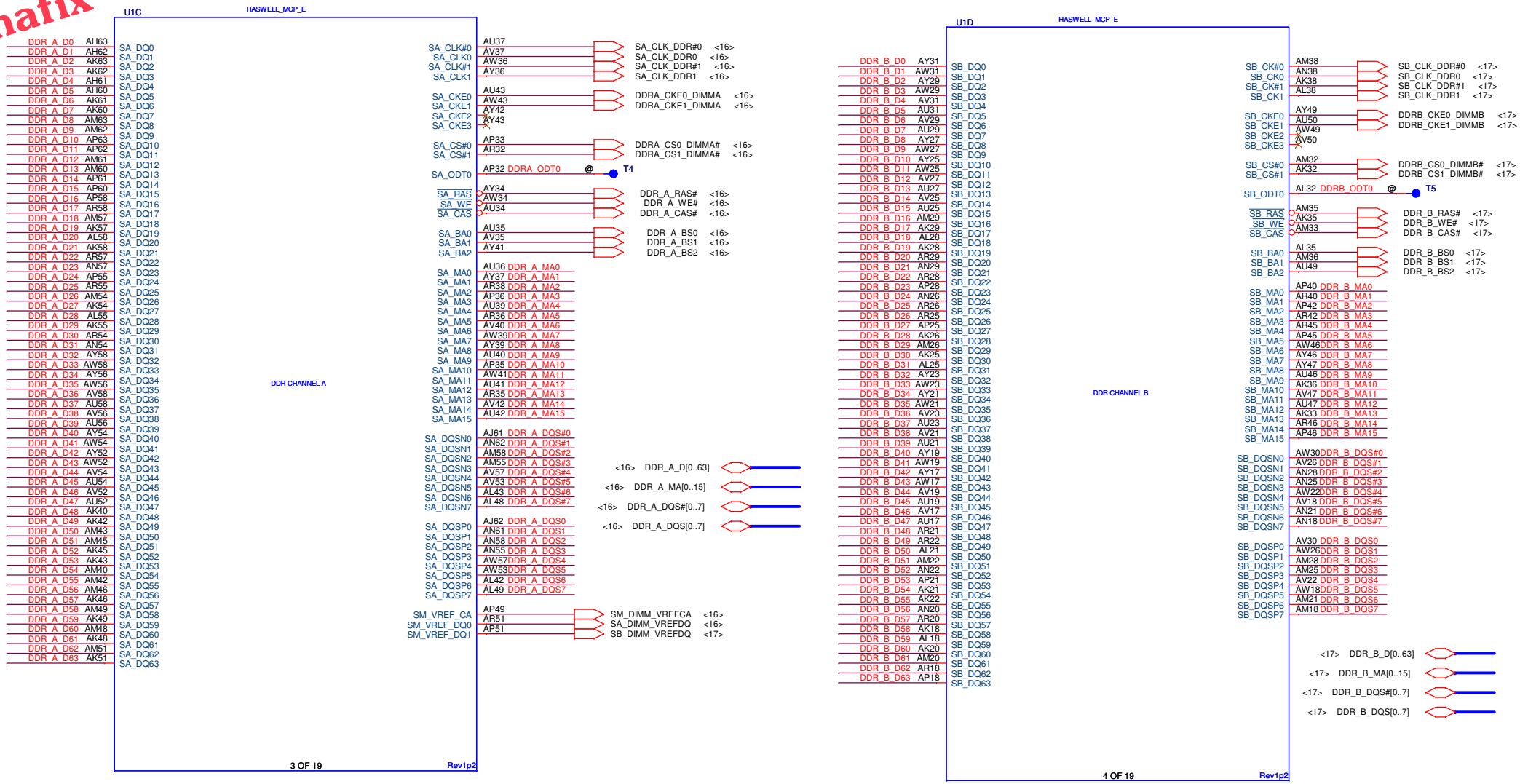
Size: Custom	Document Number: VSKTA		Rev: 2.0
Date: Friday, June 21, 2013	Sheet 4 of 57		





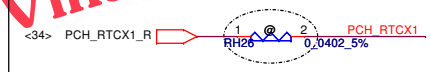
Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

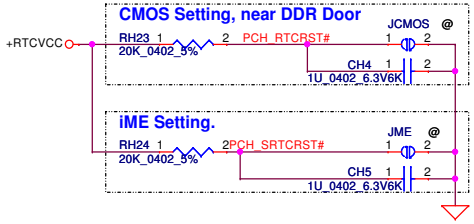
Compal Electronics, Inc.			
Title	HSW MCP(1/11) DDI,MSIC,XDP		
Size: Custom	Document Number: VSKTA		Rev: 2.0
Date: Friday, June 21, 2013	Sheet 5 of 57		

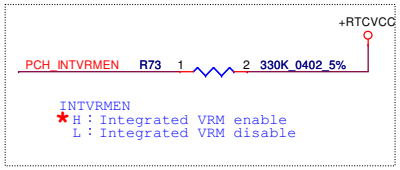


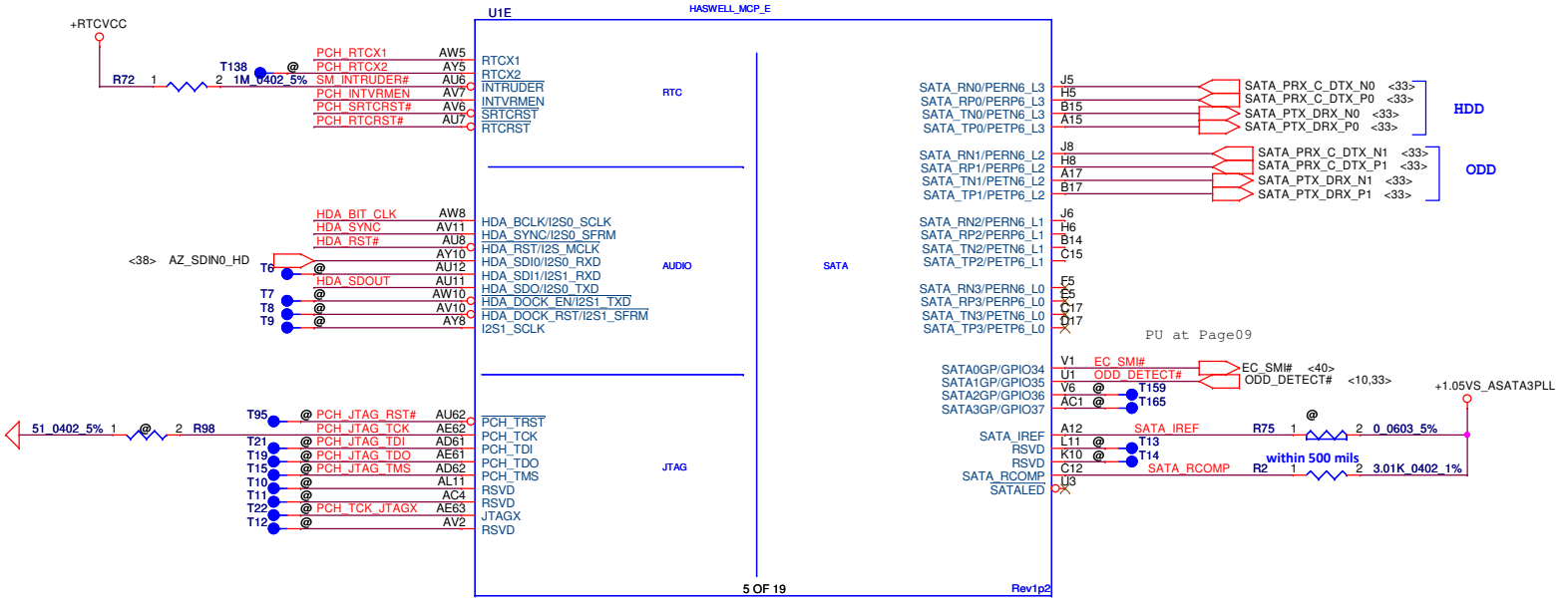
Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

Compal Electronics, Inc.	
Title	HSW MCP(2/11) DDRIII
Size: Custom	Document Number: VSKTA
Rev	2.0
Date: Friday, June 21, 2013	Sheet 6 of 57

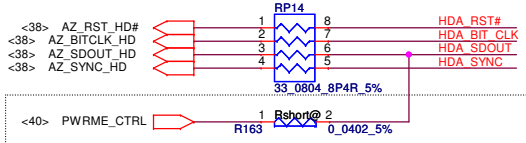




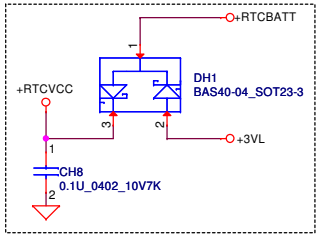




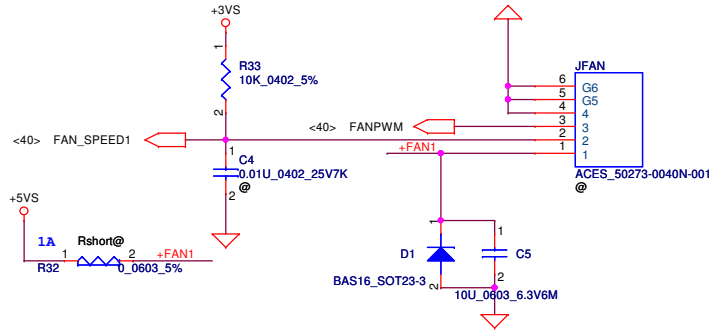
HDA for AUDIO



ME Debug

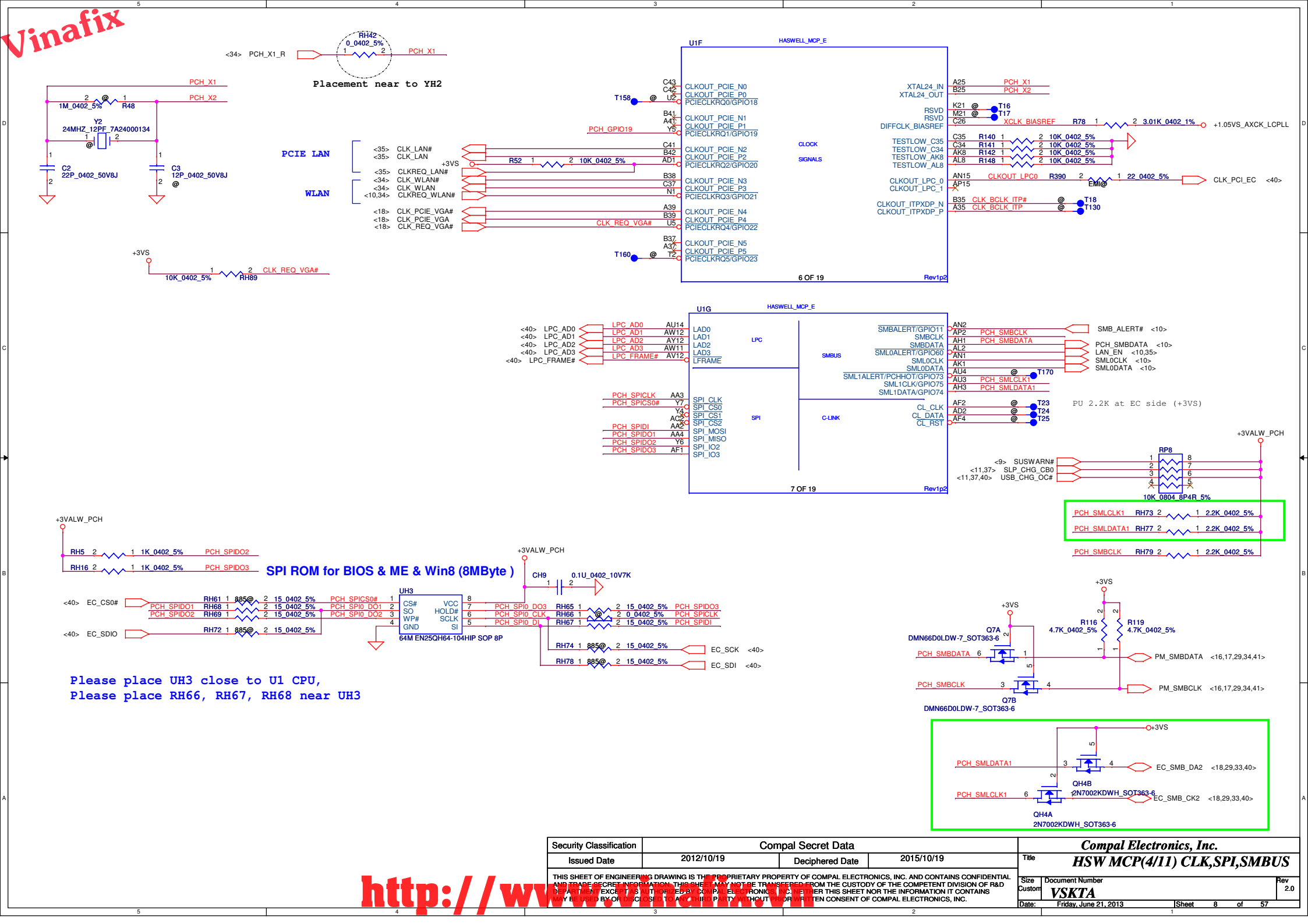


FAN Control Circuit



Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

Compal Electronics, Inc.			
Title	HSW MCP(3/11) RTC,SATA,XDP		
Size Custom	Document Number VSKTA		Rev 2.0
Date: Friday, June 21, 2013	Sheet 7 of 57		



Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

Compal Electronics, Inc.			
Title: HSW MCP(4/11) CLK,SPI,SMBUS			
Size: Custom	Document Number: VSKTA		Rev: 2.0
Date: Friday, June 21, 2013	Sheet 8 of 57		

+3VS
R227
10K_0402_5%
SYS_RESET#

PCH_PWROK
DH9
CH751H-40PT_SOD323-2
PCH_RSMRST#
<40,47> POK
DH10
CH751H-40PT_SOD323-2

+3VALW_PCH
EC_SW# RH171 1K_0402_5%

DSWODVREN - On Die DSW VR Enable
* H : Enable(DEFAULT)
L : Disable

+RTCVCC
R124 330K_0402_5%

U1H
HASWELL_MCP_E
SYSTEM POWER MANAGEMENT

PM_APWROK R64 0_0402_5% PCH_PWROK_R
SUSWARN# R206 0_0402_5% SUSACK# AK2
SUSACK
SYS_RESET# AC3
SYS_RESET
SYS_PWROK R61 0_0402_5% SYS_PWROK_R AG2
SYS_PWROK
PCH_PWROK R62 0_0402_5% PCH_PWROK_R AY7
PCH_PWROK
R63 0_0402_5% PM_APWROK AB5
APWROK
PLT_RST# AG7
PLTRST
<40> PCH_PWROK
<12,40> VCCST_PG_EC
<40> PLT_RST#

DSWVRMEN AW7 DSWODVREN
DPWROK AV5 PCH_RSMRST#_R
WAKE AJ5 EC_SWI#
EC_SWI# <35,40>

CLKRUN/GPIO32 V5 CLKRUN# R157 8.2K_0402_5% +3VS
SUS_STAT/GPIO61 AG4 T104
SUSCLK/GPIO62 AE6
SLP_S5/GPIO63 AP5 PM_SLP_S5#
CLK_EC <40>
PM_SLP_S5# <40>

10K_0402_5% R117 PCH_RSMRST# <40> PCH_RSMRST#
PCH_RSMRST# R79 PCH_RSMRST#_R AW6
RSMRST
SUSWARN# AV4
SUSWARN/SUSPWRDNACK/GPIO30
<8> SUSWARN#
<40> PBTN_OUT# AL7
PWRBTN
PCH_ACIN AJ8
ACPRESENT/GPIO31
+3VALW_PCH R156 8.2K_0402_5% PCH_BATLOW# AN4
BATLOW/GPIO72
T31 AF3
SLP_S0
AM5
SLP_WLAN/GPIO29

SLP_S4 AJ6 PM_SLP_S4#
SLP_S3 AT4 PM_SLP_S3#
SLP_A AL5 T30
SLP_SUS AP4 T96
SLP_LAN AJ7 PM_SLP_LAN#
T27 T28 T29
PM_SLP_S4# <40>
PM_SLP_S3# <40>
R118 10K_0402_5% +3VALW_PCH

8 OF 19
Rev1p2

not support Deep S4,S5 can NC

+3VALW_PCH
R245
100K_0402_5%
D21
<40,45> ACIN
PCH_ACIN
RB751V40_SC76-2

DDPB_CTRLDATA: Port B Detected
DDPC_CTRLDATA: Port C Detected
* 1: Port B or C is detected 0: Port B or C is not detected (Have internal PD)

U1I
HASWELL_MCP_E

<27> PCH_PWM_TL RH17 LVDS@ 0_0402_5%
<28> PCH_PWM_EDP RH18 IEDP@ 0_0402_5%
<27,28,40> EC_ENBKL RH19 IEDP@ 0_0402_5%
PCH_PWM B8 EDP_BKLCTL
EC_ENBKL_R A9 EDP_BKLEN
C6 EDP_VDDEN
eDP SIDEBAND
<28> LCD_ENVDD

DDPB_CTRLCLK B9
DDPB_CTRLDATA C9
DDPC_CTRLCLK D9
DDPC_CTRLDATA D11
R271 2.2K_0402_5% +3VS
UMA_HDMI_CLK <29,30>
UMA_HDMI_DATA <29,30>

<22,51> VGA_PWROK U6
<10,22> DGPU_PWR_EN P4 PIRQA/GPIO77
<10> DGPU_HOLD_RST# N4 PIRQB/GPIO78
<10,41> TP_INTR# N2 PIRQC/GPIO79
AD4 PIRQD/GPIO80
T26 PME
GPIO
DISPLAY

DDPB_AUXN C5
DDPC_AUXN B6
DDPB_AUXP B5
DDPC_AUXP A6
DDI1_AUX_DN <31>
DDI1_AUX_DP <31>

PCH_GPIO55 U7
T157 L1 GPIO55
PCH_GPIO54 L3 GPIO52
PCH_GPIO51 R5 GPIO54
PCH_GPIO53 L4 GPIO51
GPIO53

DDPB_HPD C8
DDPC_HPD A8
EDP_HPD D6 H_EDP_HPD
CPU_DP_HPD <31>
HDMI_HPD <10,29,30>
H_EDP_HPD <27,28>

9 OF 19
Rev1p2

R65 0_0402_5%
+3VS
PCH_PWROK
VGATE_3V
U43
MC74VHC1G08DFT2G_SC70-5
SYS_PWROK
R208 10K_0402_5%
R207 10K_0402_5%

+1.05VS_VTT
+3VS
U17
<12,50> VGATE
NC
A
GND
VCC
Y
VGATE_3V
74AUP1G07GW_TSSOP5
R310 10K_0402_5%

+3VS
PLT_RST#
DGPU_HOLD_RST#
U37
MC74VHC1G08DFT2G_SC70-5
OPT@
IN1
IN2
GND
VCC
OUT
PLTRST_VGA# <18>
R391 100K_0402_5% OPT@

H_EDP_HPD
R417 100K_0402_5%
R403 0_0402_5%
+3VS
PLT_RST#
U30
MC74VHC1G08DFT2G_SC70-5
PLT_RST_BUF# <34,35>
R416 100K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

Compal Electronics, Inc.
Title: HSW MCP(5/11) PM,GPIO,DDI
Size: Custom | Document Number: VSKTA | Rev: 2.0
Date: Friday, June 21, 2013 | Sheet 9 of 57

Note: need check all GPIO PU need or not after BIOS post

+3VS

RP23 1 8 DEVSLP0 7 SERIRQ 6 ODD_EN# 5 10K_0804_8P4R_5% 4 — TP_INTR# <41,9>

RP27 1 8 SPK_DET 7 ODD_DA# 6 5 10K_0804_8P4R_5% 4 — DGPU_HOLD_RST# <9>, CLKREQ_WLAN# <34,8>

+3VALW_PCH

RP34 1 8 LAN_EN <35,8>, 7 USB_OC#0 <11,37,40>, 6 SMB_ALERT# <8>, 5 SML0CLK <8>, 10K_0804_8P4R_5%; 8 1 SML0DATA <8>, 7 2 SLP_CHG_CB1, 6 3 PCH_SMBDATA <8>, 5 4 USB_OC#2 <11,35,40>, RP9 2.2K_0804_8P4R_5%

+3VS

RP28 1 8 PCH_GPIO27 2 7 PASSWORD_CLEAR# 3 6 4 5 10K_0804_8P4R_5% — ODD_DETECT# <33,7>, DGPU_PWR_EN <22,9>

U1J HASWELL_MCP_E

T162 @	P1	BMBUSY/GPIO76		THERMTRIP	D60 H_THERMTRIP#
T167 @	AU2	GPIO8		RCIN/GPIO82	V4 KB_RST#
	AM7	LAN_PHY_PWR_CTRL/GPIO12		SERIRQ	T4 SERIRQ
<40> EC_LID_OUT#	AD6	GPIO15	CPU/MISC	PCH_OPI_RCOMP	AW15 PCH_OPIRCOMP 1 2 R145 49.9_0402_1%
<42> ODD_EN#	Y1	GPIO16		RSVD	AF20 @ T106
<33> ODD_DA#	T3	GPIO17		RSVD	AB21 @ T32
PCH_GPIO24	AD5	GPIO24			
PCH_GPIO27	AN5	GPIO27			
PCH_GPIO28	AD7	GPIO28			
PCH_GPIO26	AN3	GPIO26			
PASSWORD_CLEAR#	AG6	GPIO56		GSPI0_CS/GPIO83	R6 PCH_GPIO83
T166 @	AP1	GPIO57		GSPI0_CLK/GPIO84	L6 PCH_GPIO84
PCH_GPIO58	AL4	GPIO58		GSPI0_MISO/GPIO85	N6 PCH_GPIO85
PCH_GPIO59	AT5	GPIO59		GSPI0_MOSI/GPIO86	L8 PCH_GPIO86
<37> SLP_CHG_CB1	AK4	GPIO44		GSPI1_CS/GPIO87	R7 DGPU_PRSNT#
PCH_GPIO47	AB6	GPIO47		GSPI1_CLK/GPIO88	L5 PCH_GPIO88
SM_DET	U4	GPIO48		GSPI1_MISO/GPIO89	N7 PCH_GPIO89
T163 @	Y3	GPIO49		GSPI_MOSI/GPIO90	K2 @ T135
T139 @	P3	GPIO50		UART0_RXD/GPIO91	J1 @ T134
PCH_GPIO71	Y2	HSIOPC/GPIO71		UART0_TXD/GPIO92	K3 PCH_GPIO92
T168 @	AT3	GPIO13		UART0_RTS/GPIO93	J2 PCH_GPIO93
PCH_GPIO14	AH4	GPIO14	LPIO	UART0_CTS/GPIO94	G1 @ T114
T169 @	AM4	GPIO25		UART1_RXD/GPIO0	K4 — HDMI_HPD <29,30,9>
PCH_GPIO45	AG5	GPIO45		UART1_TXD/GPIO1	G2 @ T111
PCH_GPIO46	AG3	GPIO46		UART1_RST/GPIO2	J3 @ T133
				UART1_CTS/GPIO3	J4 PCH_GPIO3
PCH_GPIO9	AM3	GPIO9		I2C0_SDA/GPIO4	F2 @ T132
<40> EC_SCI#	AM2	GPIO10		I2C0_SCL/GPIO5	F3 PCH_GPIO5
<33> DEVSLP0	P2	DEVSLP0/GPIO33		I2C1_SDA/GPIO6	G4 PM_I2CSDA1
<39> SPK_DET	C4	SDIO_POWER_EN/GPIO70		I2C1_SCL/GPIO7	F1 PM_I2CSCL1 — PM_I2CSDA1 <41>, PM_I2CSCL1 <41>
T136 @	L2	DEVSLP1/GPIO38		SDIO_CLK/GPIO64	E3 PCH_GPIO64
PCH_GPIO39	N5	DEVSLP2/GPIO39		SDIO_CMD/GPIO65	F4 PCH_GPIO65
<38> PCH_SPKR	V2	SPKR/GPIO81		SDIO_D0/GPIO66	D3 PCH_GPIO66
				SDIO_D1/GPIO67	E4 PCH_GPIO67
				SDIO_D2/GPIO68	C3 PCH_GPIO68
				SDIO_D3/GPIO69	E2 PROJECT_ID

10 OF 19 — Rev1p2

JPW @

+1.05VS_VTT

R144 1K_0402_5%

H_THERMTRIP# — ESD@ CH12 0.1U_0402_10V7K

ODD_DA# — ESD@ CH6 180P_0402_50V8J

+3VS

PM_I2CSDA1 R274 1 @ 2 1K_0402_5%

PM_I2CSCL1 R272 1 @ 2 1K_0603_5%

+3VS

R306 10K_0402_5% UMA@

DGPU_PRSNT#

R219 10K_0402_5% OPT@

	GPIO87 DGPU_PRSNT#
DIS,Optimus	0
UMA	1

+3VS

R307 10K_0402_5% SM@

SM_DET

R220 10K_0402_5% NOSM@

Non-Harman detection		
GPIO70 SPK_DET	0	ONKYO
	1	Non-Brand

GPIO48 SM_DET	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	SM@
0		Non Harman	NOSM@

PROJECT_ID

R215 0_0402_5% @

	GPIO69 PROJECT_ID
VSKTA	0
VSKAA	1

+3VS

R269 1 @ 2 1K_0402_1% PCH_SPKR

SPKR / GPIO81 : NO REBOOT

1: ENABLED

* 0: DISABLED (Have internal PD)

+3VALW_PCH

R247 1 2 10K_0402_5% EC_LID_OUT#

GPIO15 : TLS Confidentiality

1: Intel ME TLS with confidentiality

* 0: Intel ME TLS with no confidentiality (Have internal PD)

PCH_GPIO86 R273 1 @ 2 1K_0402_5%

GSPI0_MOSI / GPIO86 : Boot BIOS Strap

1: ENABLED

* 0: SPI ROM (Have internal PD)

PCH_GPIO66 R270 1 @ 2 1K_0402_1%

SDIO_D0 / GPIO66 : Top-Block Swap Override

* 1: ENABLED (Have internal PU)

0: DISABLED

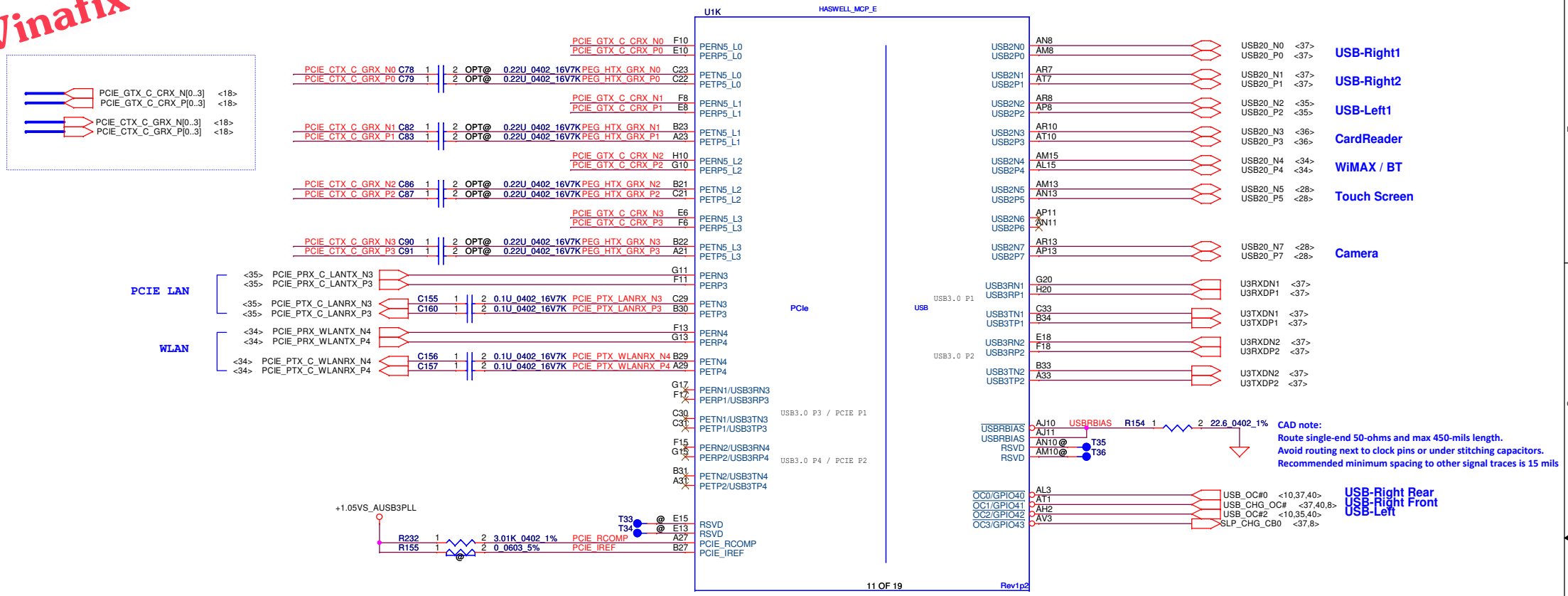
Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

Compal Electronics, Inc.

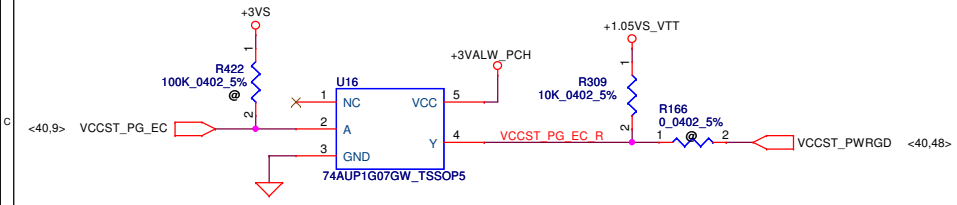
Title: HSW MCP(6/11) GPIO,LPIO

Size: Custom | Document Number: VSKTA | Rev: 2.0

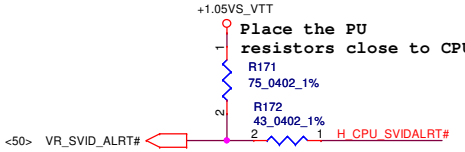
Date: Friday, June 21, 2013 | Sheet 10 of 57



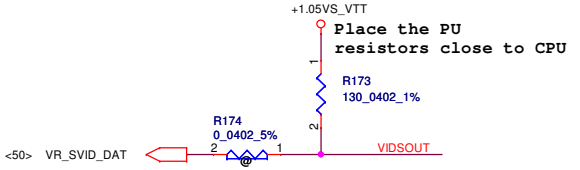
Compal Electronics, Inc.	
Title	HSW MCP(7/11) PCIE,USB
Size: Custom	Document Number: VSKTA
Rev	2.0
Date: Friday, June 21, 2013	Sheet 11 of 57

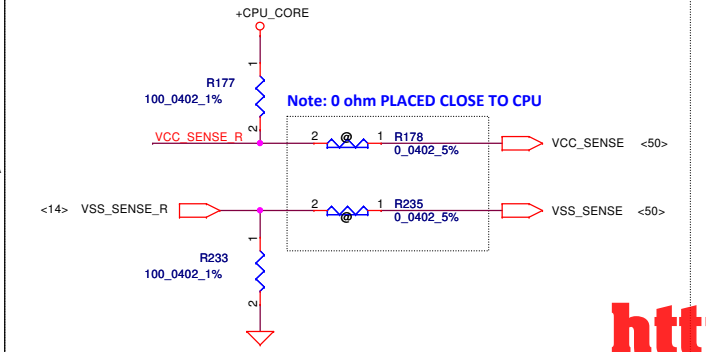


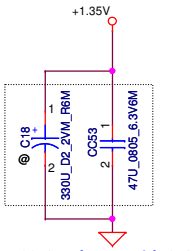
SVID ALERT



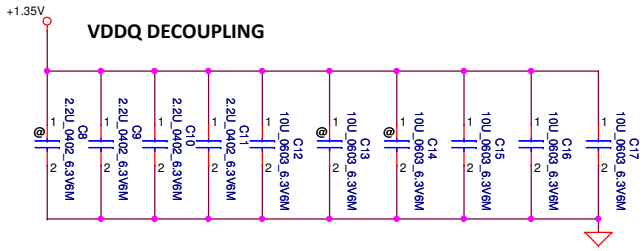
SVID DATA

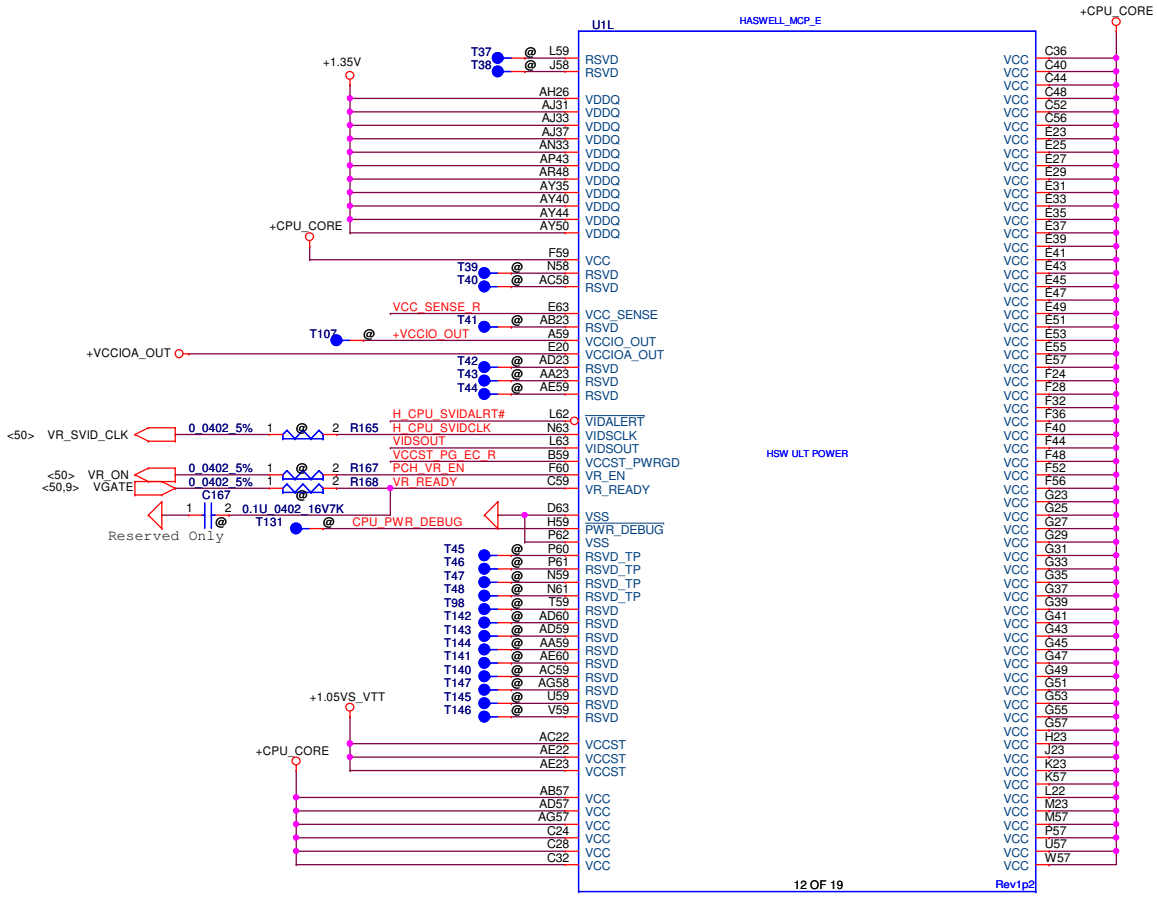






CC53 co-layout with C18

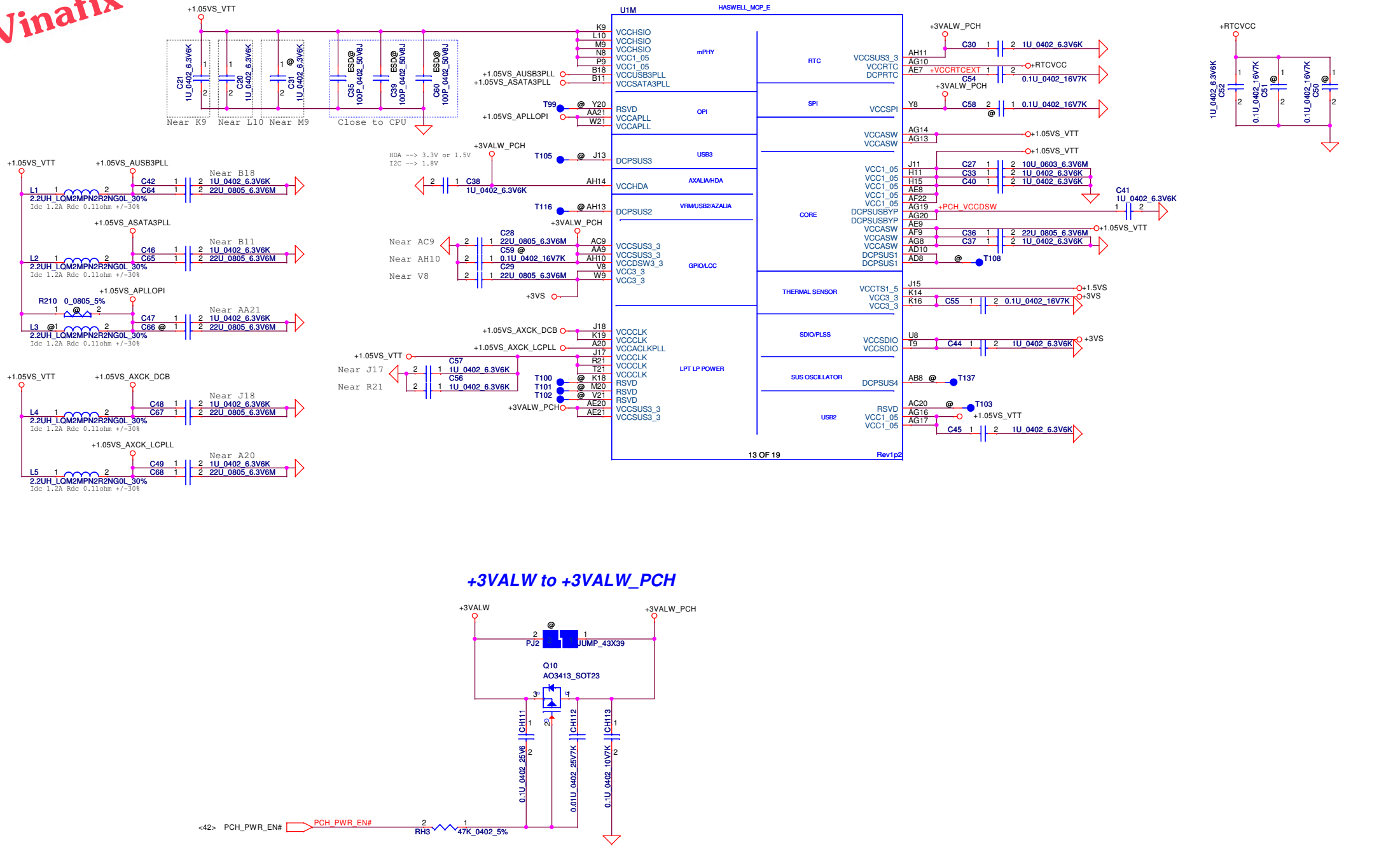




+1.35V : 470UF/2V/7343 *2
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4

Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

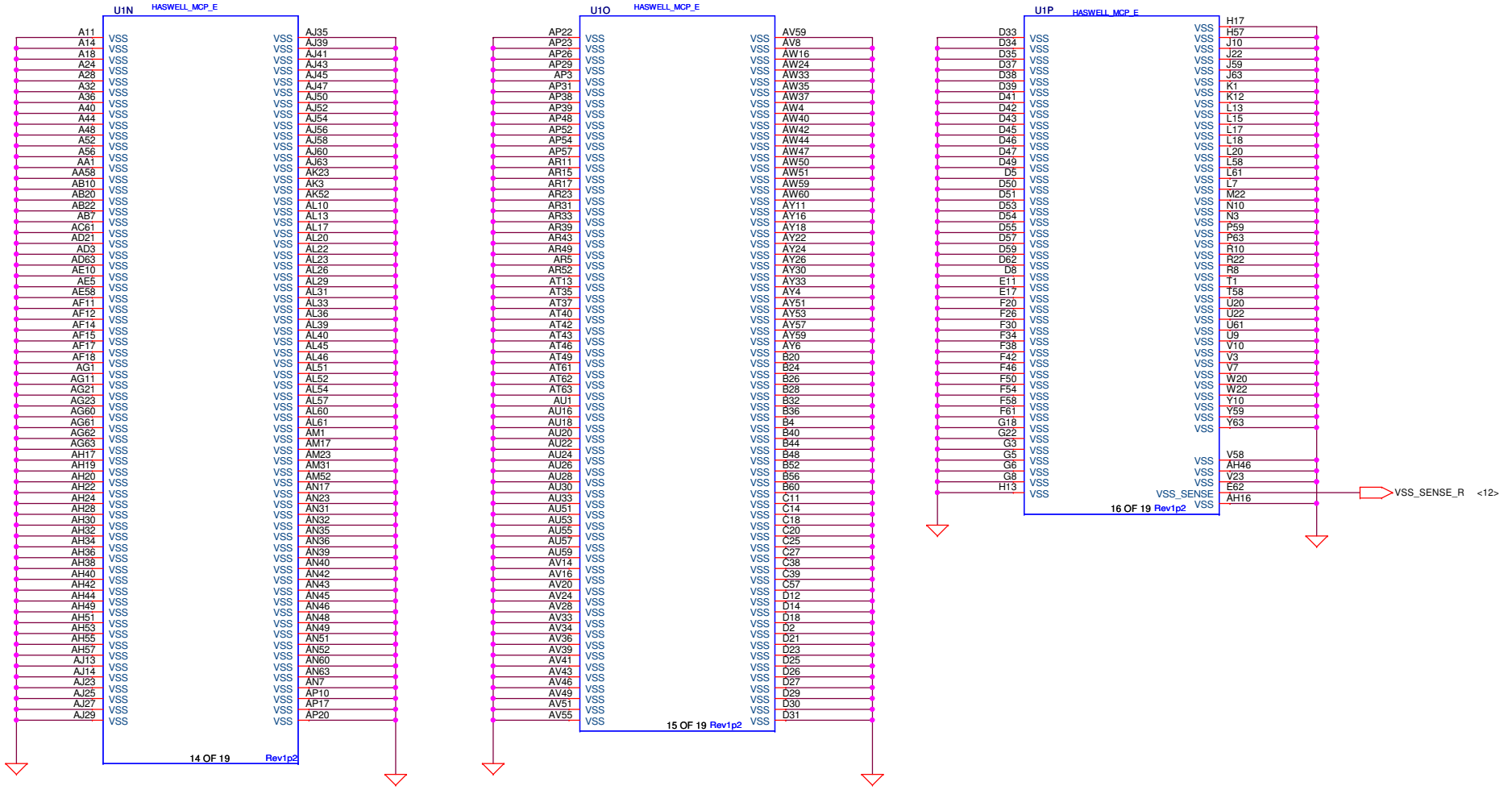
Compal Electronics, Inc.			
Title: HSW MCP(8/11) Power			
Size: Custom	Document Number: VSKTA		Rev: 2.0
Date: Friday, June 21, 2013	Sheet 12 of 57		



+3VALW to +3VALW_PCH

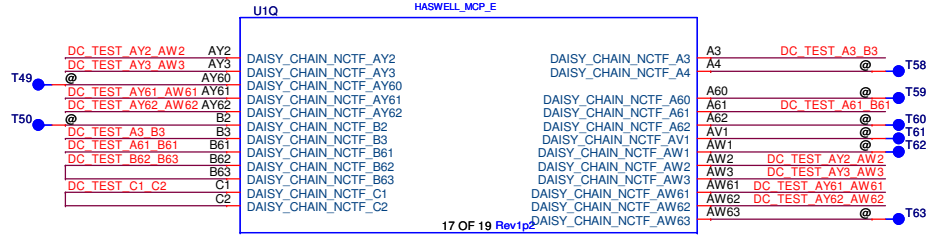
Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

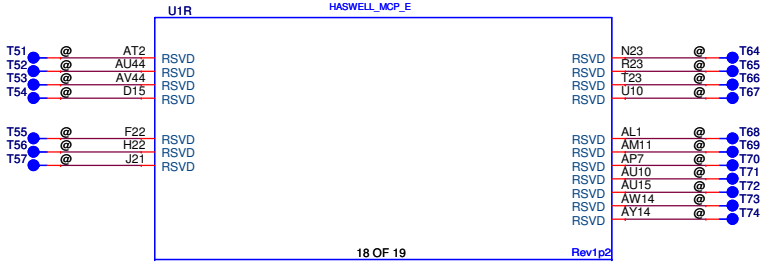
Compal Electronics, Inc.			
Title: HSW MCP(9/11) Power			
Size: Custom	Document Number: VSKTA		Rev: 2.0
Date: Friday, June 21, 2013	Sheet 13 of 57		

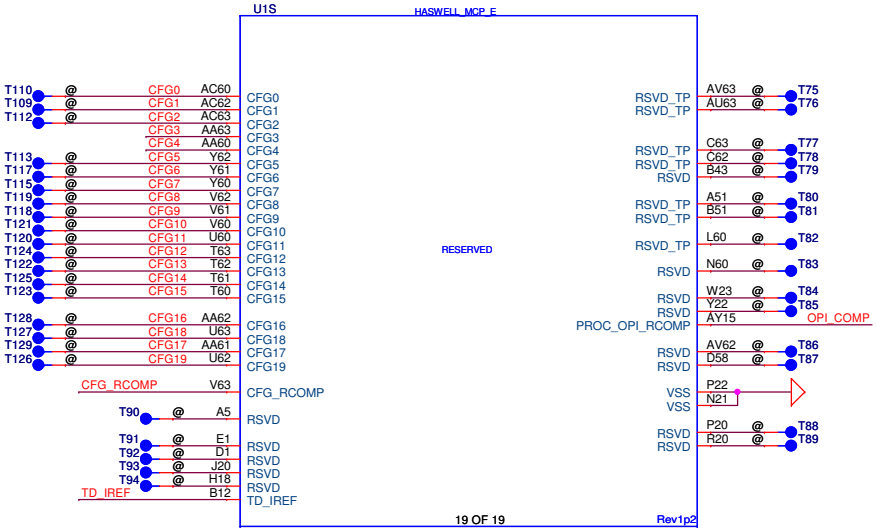


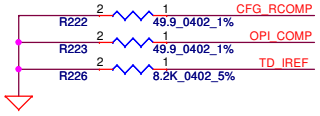
Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

Compal Electronics, Inc.			
Title: HSW MCP(10/11) GND			
Size: Custom	Document Number: VSKTA		Rev: 2.0
Date: Friday, June 21, 2013	Sheet 14 of 57		

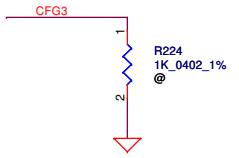




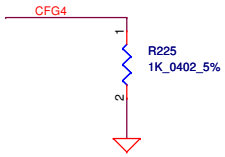




CFG Straps for Processor



Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

Compal Electronics, Inc.			
Title	HSW MCP(11/11) RSVD		
Size: Custom	Document Number: VSKTA		Rev: 2.0
Date: Friday, June 21, 2013	Sheet 15 of 57		

DDR3 SO-DIMM A
Reverse Type
H=4.0mm

Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1.203,204

All VREF traces should have 10 mil trace width

JDDR3L

LCN_DAN06-K4406-0103_204P

U45 74AUP1G07GW_TSSOP5

U18 LBSS138LT1G_SOT-23-3

Note: Depend on Project

Note: Depend on Project

Note: Depend on Project

Channel A

<Address: SA1:SA0=00>

DIMM_1 STD H:4mm

Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

Compal Electronics, Inc.			
Title: DDRIII DIMMA			
Size: Custom	Document Number: VSKTA		Rev: 2.0
Date: Friday, June 21, 2013	Sheet 16 of 57		

DDR3 SO-DIMM B
Reverse Type
H=9.0mm

Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1.203,204

All VREF traces should have 10 mil trace width

Channel B

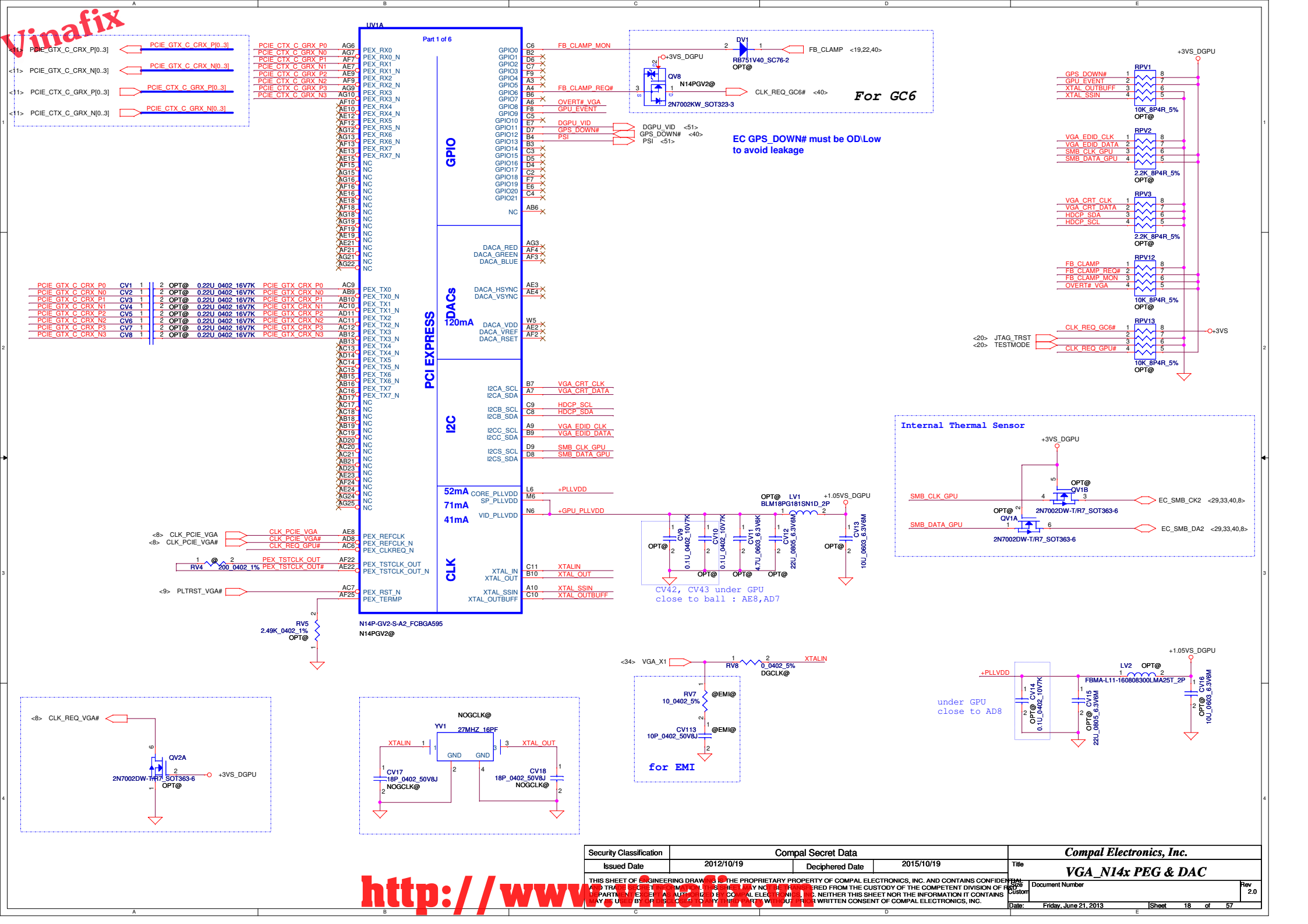
<Address: SA1:SA0=10>

DIMM_2 STD H:4mm

Note: Depend on Project

Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

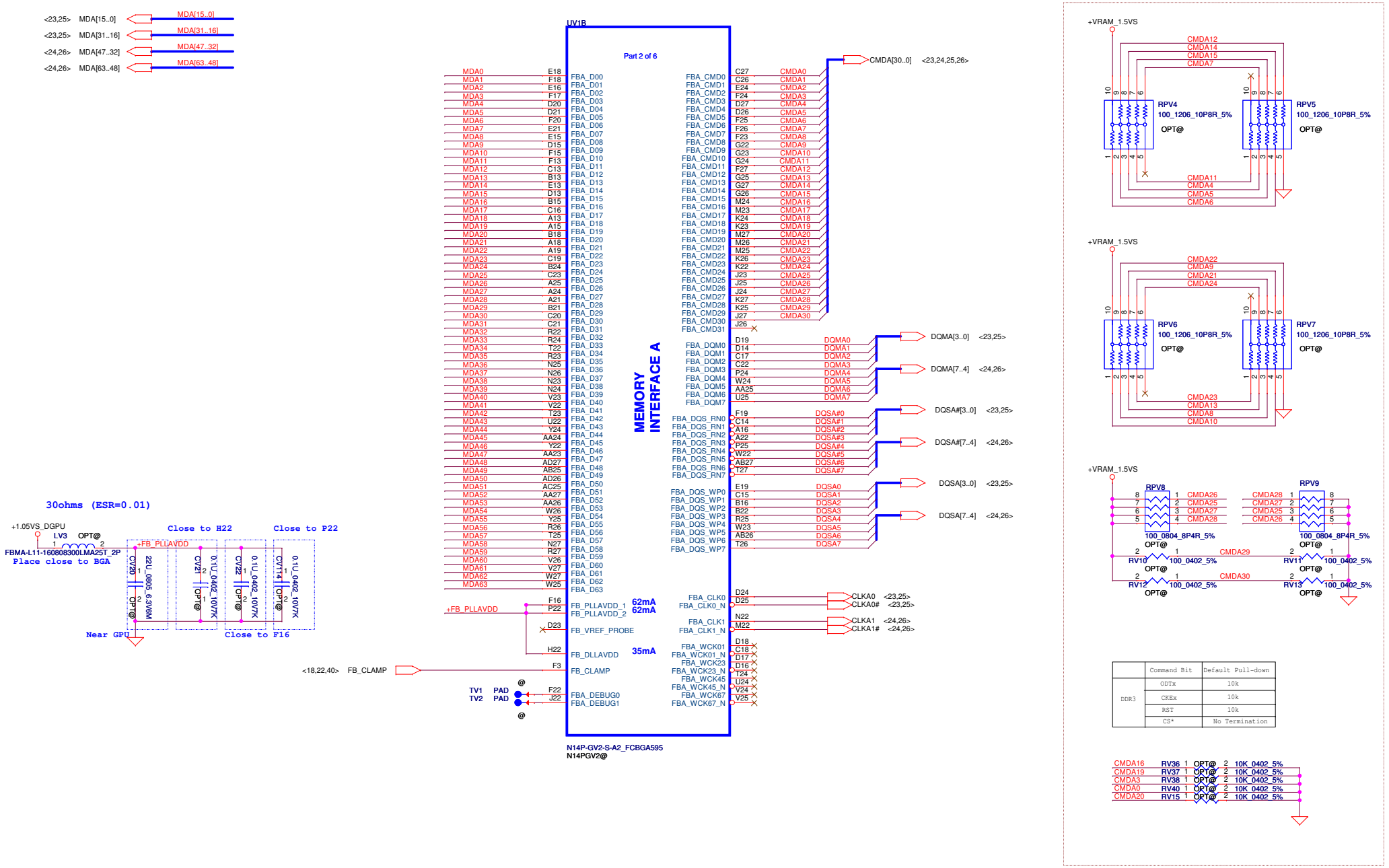
Compal Electronics, Inc.			
Title: DDRIII DIMMB			
Size: Custom	Document Number: VSKTA		Rev: 2.0
Date: Friday, June 21, 2013	Sheet 17 of 57		



Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

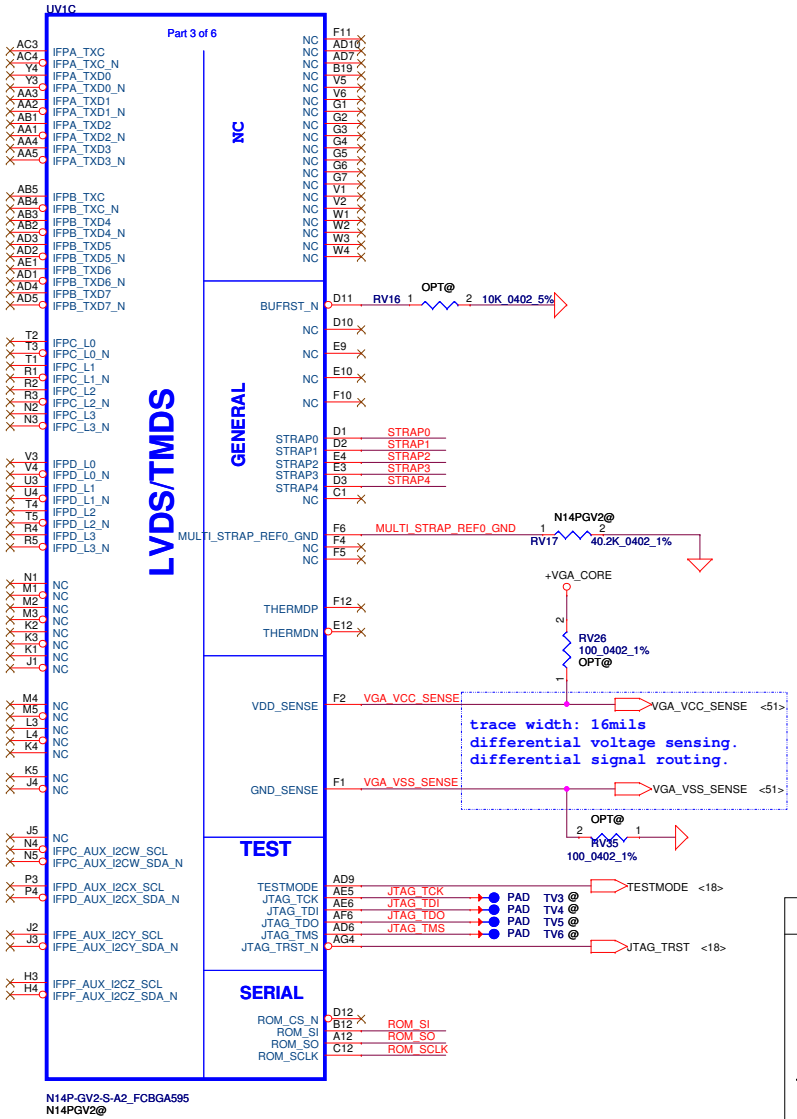
Compal Electronics, Inc.	
Title	VGA_N14x PEG & DAC
Size: Custom	Document Number
Rev	2.0
Date: Friday, June 21, 2013	Sheet 18 of 57

VRAM Interface



Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

Compal Electronics, Inc.			
Title: N14x VRAM Interface			
Size: Custom	Document Number		Rev: 2.0
Date: Friday, June 21, 2013	Sheet 19 of 57		

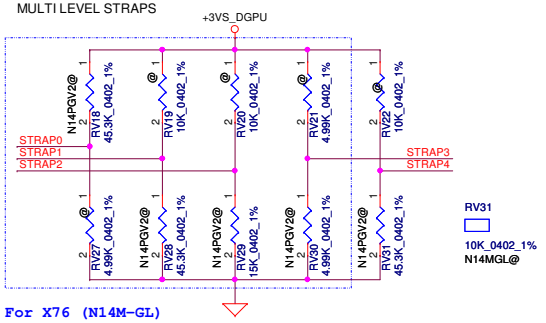


Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	**PCI_DEVID[4]**	SUB_VENDOR	**PCI_DEVID[5]**	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	**RAMCFG[3]**	**RAMCFG[2]**	**RAMCFG[1]**	**RAMCFG[0]**
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_DGPU	**PCI_DEVID[3]**	**PCI_DEVID[2]**	**PCI_DEVID[1]**	**PCI_DEVID[0]**
STRAP3	+3VS_DGPU	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_DGPU	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

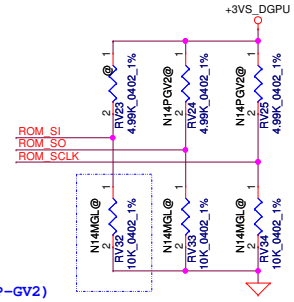
SKU	Device ID	biit5 to bit0
N14P-GV2	TBD	010010
N14M-GL	0x1140	000000

Resistor Values	Pull-up to +3VS _DGPU	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

MULTI LEVEL STRAPS



For X76 (N14M-GL)



For X76 (N14P-GV2)

GPU		FB Memory gDDR3			ROM_SI
N14P-GV2	128M x 16	Samsung	900MHz	K4W2G1646E-BC11	PD 45K
			1GHz	K4W2G1646E-BC1A	
		Hynix	900MHz	H5TQ2G63DFR-11C	PD 34.8K
			1GHz	H5TQ2G63DFR-N0C	
		Micron	900MHz	MT41K128M16JT-107G	PD 30K
	256M x 16	Samsung	900MHz	K4W4G1646B-HC11	PD 20K
		Micron	900MHz	MT41K256M16HA-107G	PD 10K

GPU		FB Memory gDDR3			STRAP[3:0]
N14M-GL	128M x 16	Samsung	900MHz	K4W2G1646E-BC11	0101
			1GHz	K4W2G1646E-BC1A	
		Hynix	900MHz	H5TQ2G63DFR-11C	0110
			1GHz	H5TQ2G63DFR-N0C	
		Micron	900MHz	MT41K128M16JT-107G	0001
	256M x 16	Samsung	900MHz	K4W4G1646B-HC11	1011
		Hynix	900MHz	H5TC4G63AFR-11C	0100
		Micron	900MHz	MT41K256M16HA-107G	1101

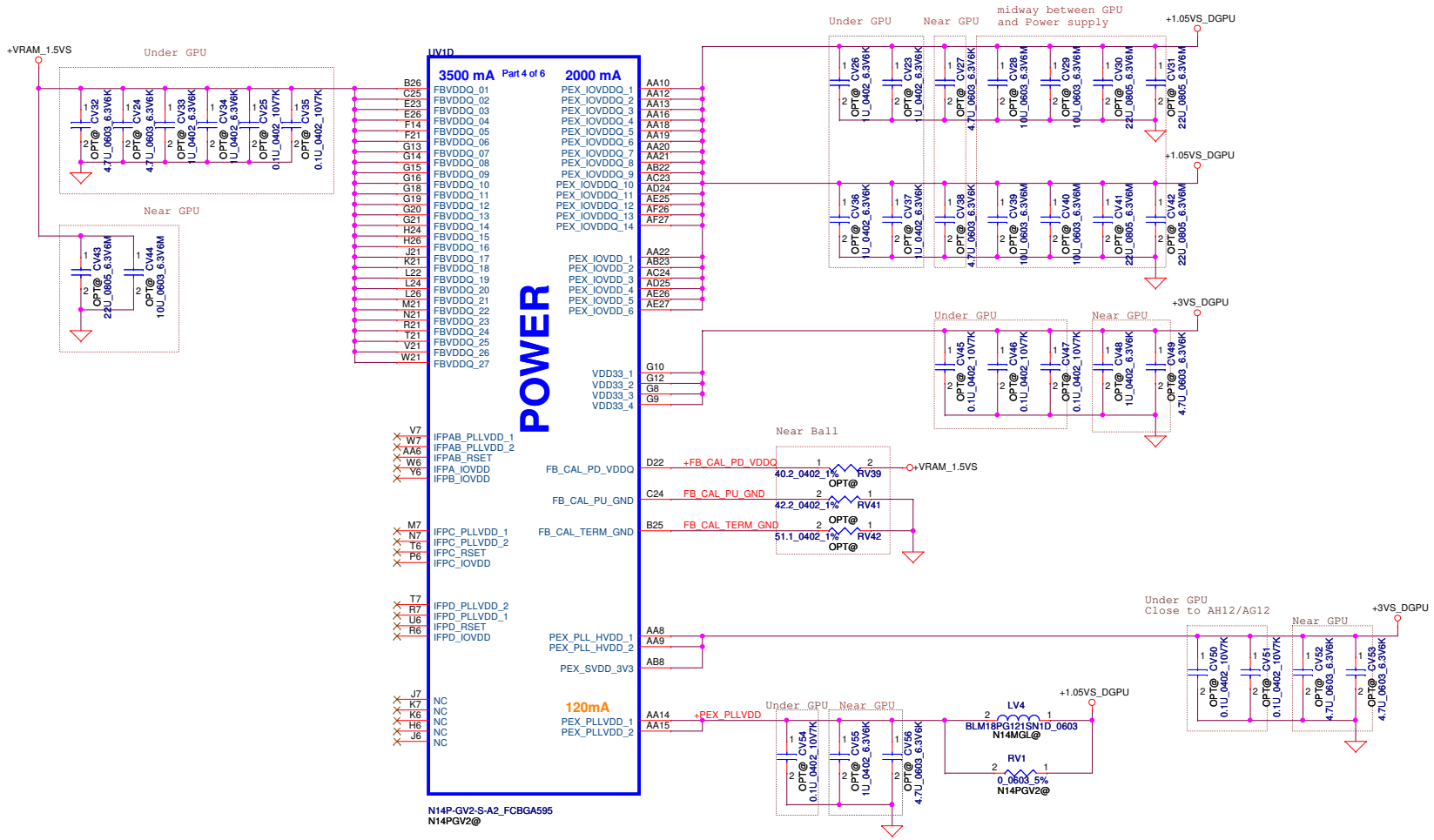
Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

Compal Electronics, Inc.

Title: VGA_N14x LVDS&TMDS

Size: Custom | Document Number | Rev 2.0

Date: Friday, June 21, 2013 | Sheet 20 of 57



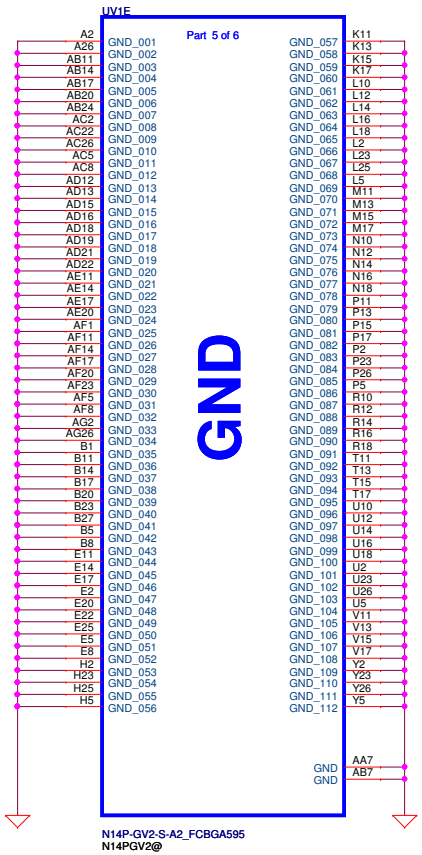
Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

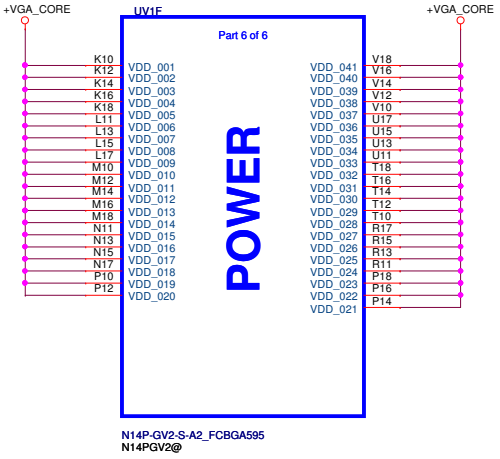
Compal Electronics, Inc.

Title: VGA_N14x POWER

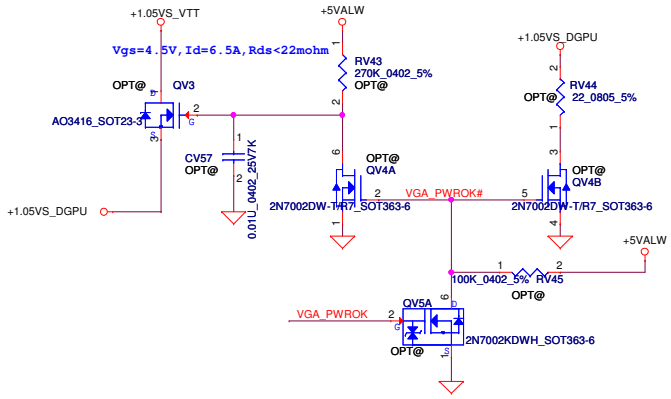
Size	Document Number	Rev
Custom		2.0

Date: Friday, June 21, 2013 Sheet 21 of 57

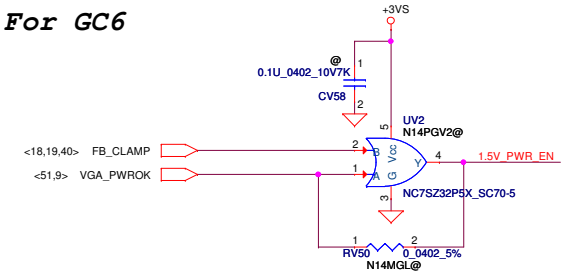




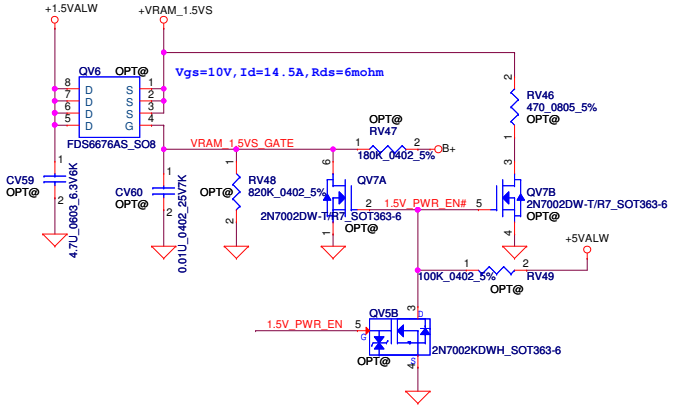
+1.05VS_VCCP to +1.05VS_DGPU



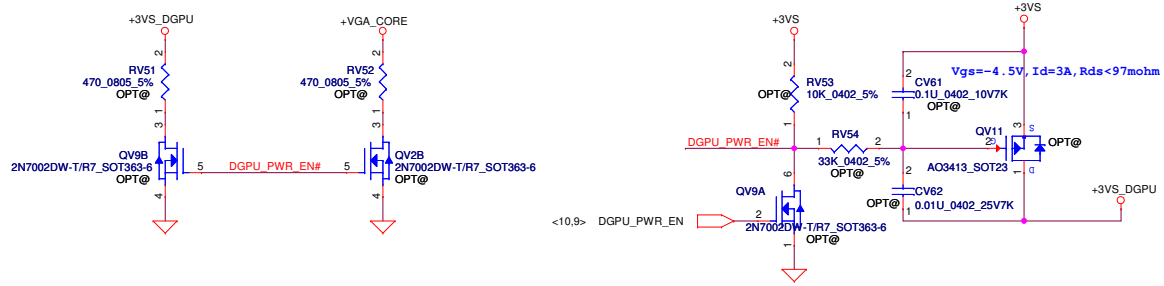
For GC6



+1.5VALW to +VRAM_1.5VS

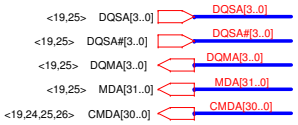


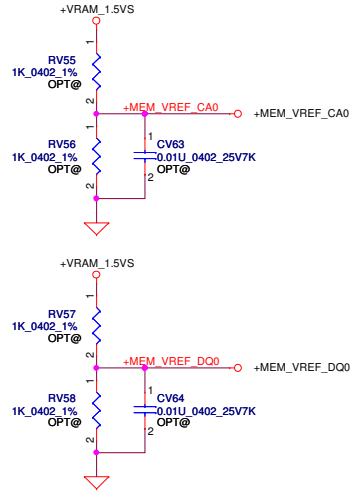
+3VS to +3VS_DGPU

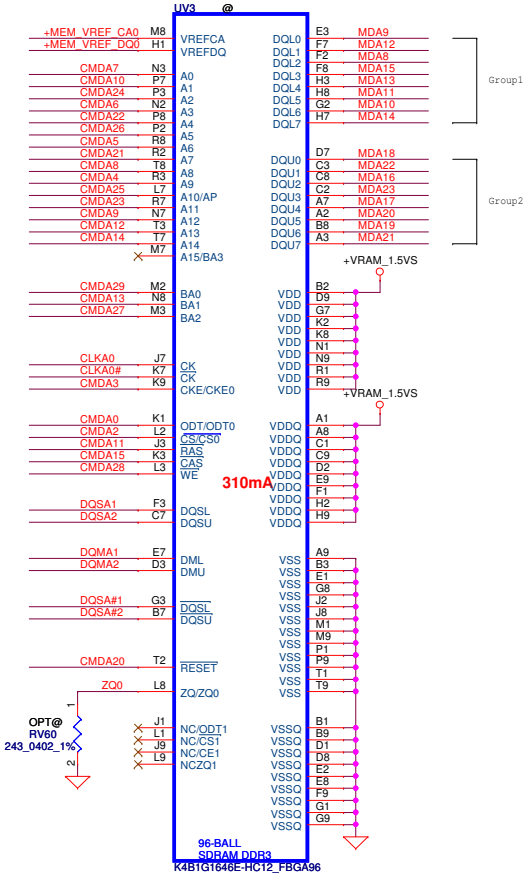


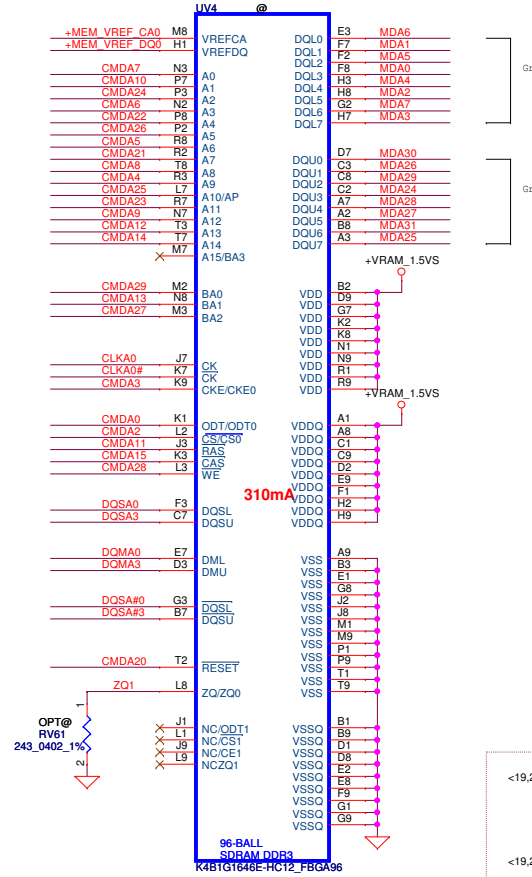
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/10/19	Deciphered Date 2015/10/19	Title: VGA_N14x POWER & GND
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: Custom; Document Number; Rev: 2.0
			Date: Friday, June 21, 2013; Sheet 22 of 57

RANK 0 [31...0]
VRAM DDR3 Chips



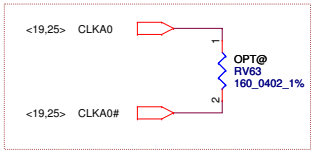




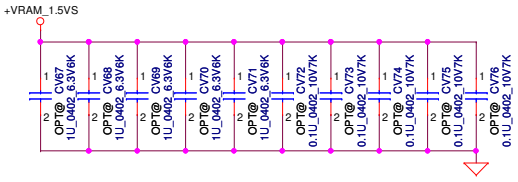


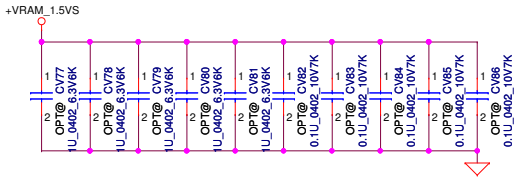
Mode E Address	Rank 0 0..31	Rank 0 32..63	Rank 1 0..31	Rank 1 32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

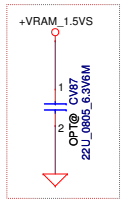
Place close to the first T point



Place close to RANK0 VRAM

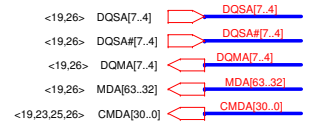


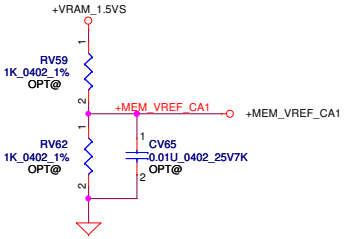


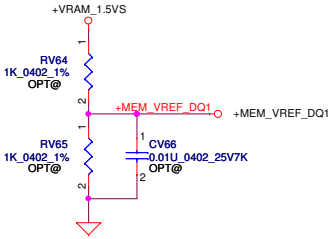


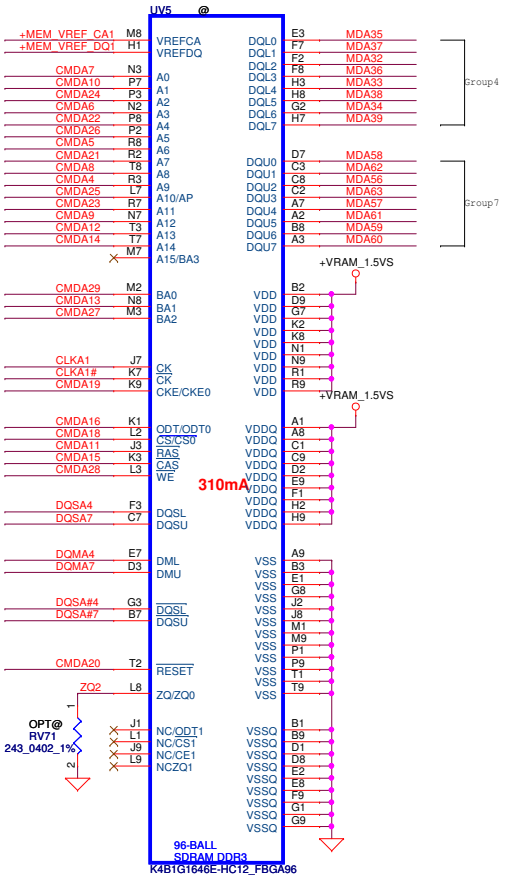
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/10/19	Deciphered Date 2015/10/19	Title: VGA_N14x VRAM RANK 0L
			Size: Custom; Document Number; Rev 2.0
			Date: Friday, June 21, 2013; Sheet 23 of 57

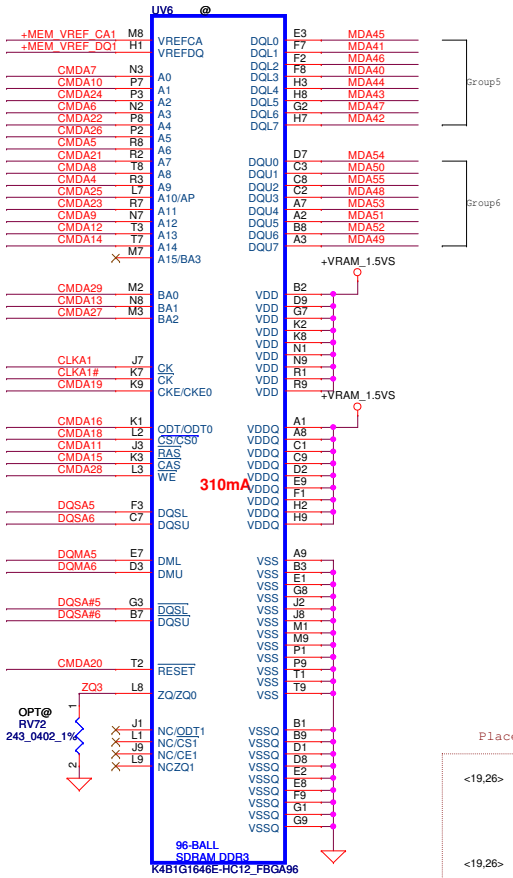
RANK_0 [63...32]
VRAM DDR3 Chips





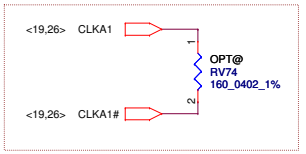


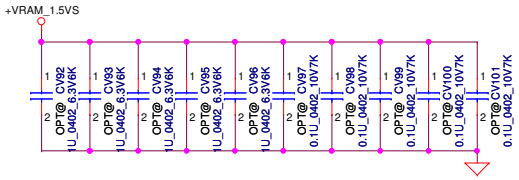


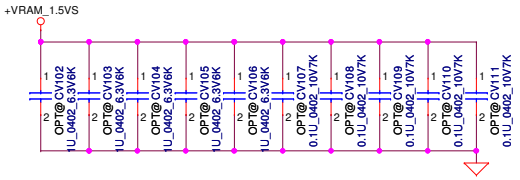


Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

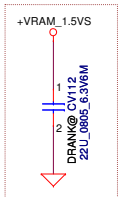
Place close to the first T point







Place close to RANK1 VRAM



Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

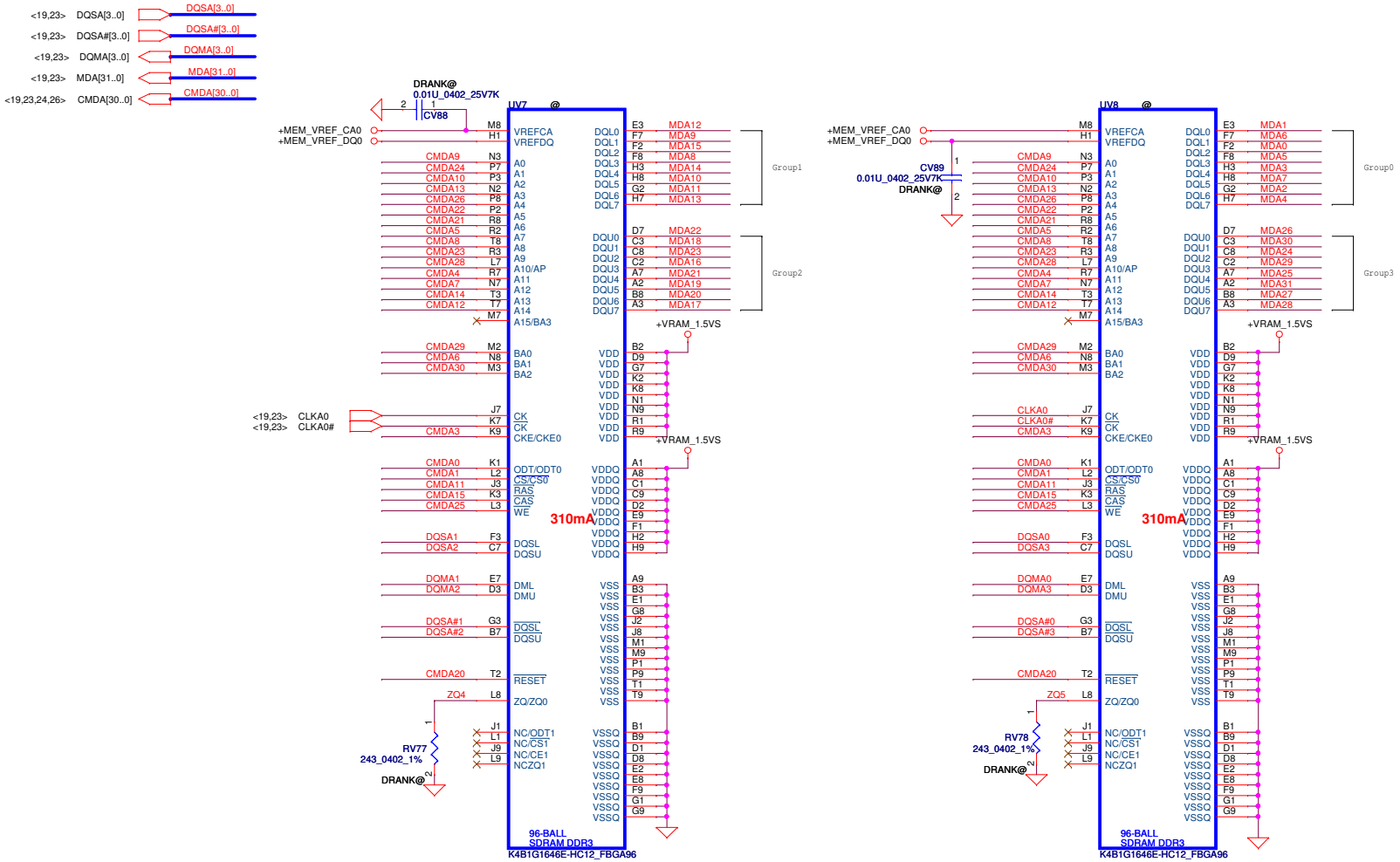
Compal Electronics, Inc.

Title: VGA_N14x VRAM RANK 0H

Size: Custom | Document Number | Rev 2.0

Date: Friday, June 21, 2013 | Sheet 24 of 57

RANK 1 [31..0]
VRAM DDR3 Chips



Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

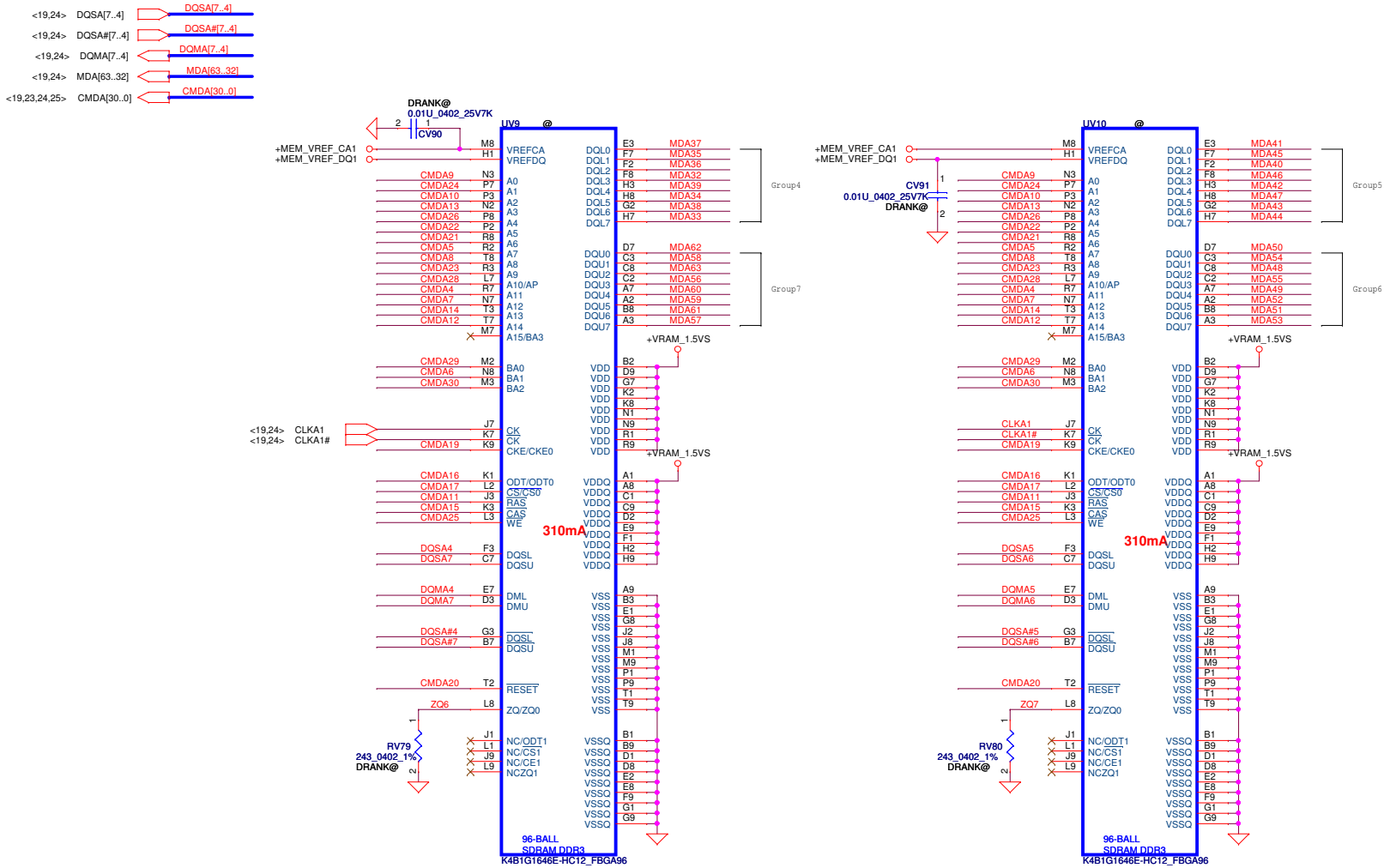
Compal Electronics, Inc.

Title: VGA_N14x VRAM RANK 1L

Size: Custom | Document Number | Rev: 2.0

Date: Friday, June 21, 2013 | Sheet 25 of 57

RANK 1 [63...32]
VRAM DDR3 Chips



Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

Compal Electronics, Inc.

Title: VGA_N14x VRAM RANK 1H

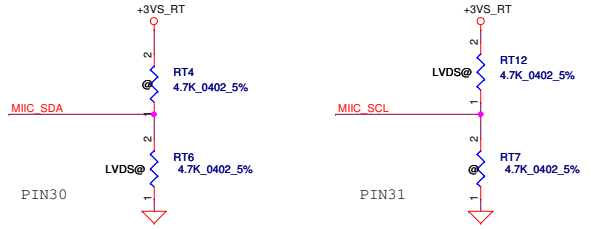
Size: Custom | Document Number | Rev: 2.0

Date: Friday, June 21, 2013 | Sheet 26 of 57

Mode Configure

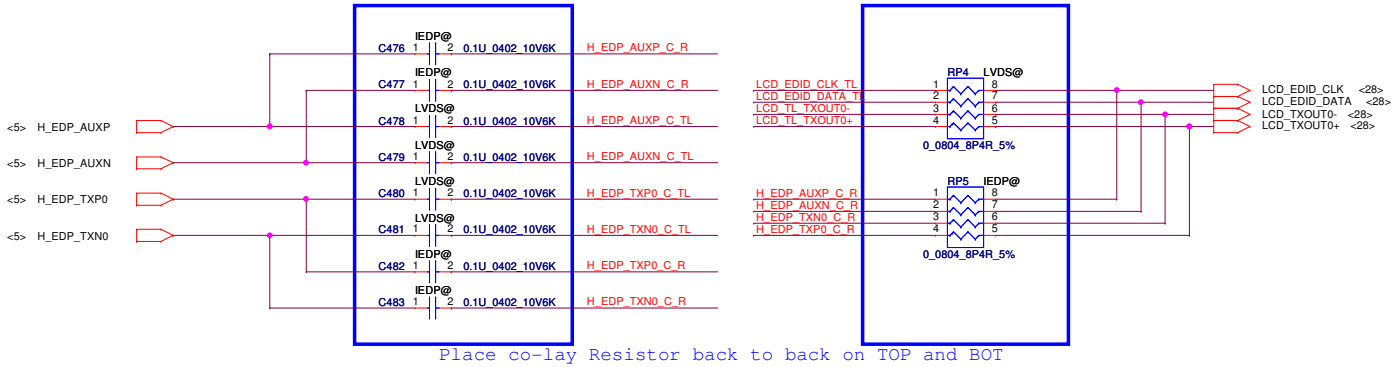
※ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.
EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.
EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.

〈 ※Default mode 〉

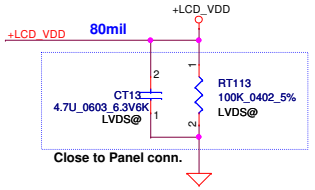


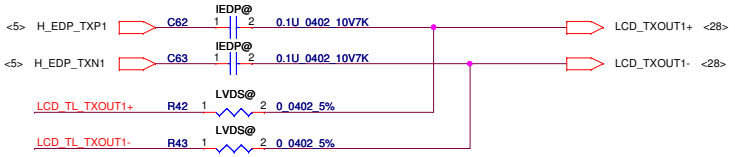
SWR / LDO Mode select

※LDO mode is adopted as default power regulator mode.
Also can implement SWR mode by add inductor.



Place co-lay Resistor back to back on TOP and BOT





	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

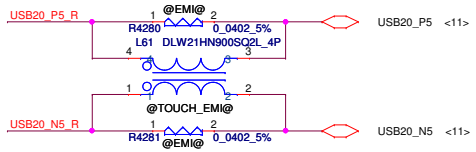
PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5~3.3V

* Version R has internal level shifter, remove level shifter circuit on AMD platform

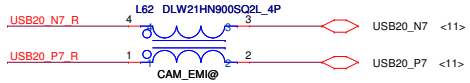
Different between 2132S and 2132R	
2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/10/19	Deciphered Date 2015/10/19	Title: LVDS Translator - RTD2132R-CG
			Size: Custom; Document Number: VSKTA; Rev: 2.0
			Date: Friday, June 21, 2013; Sheet 27 of 57

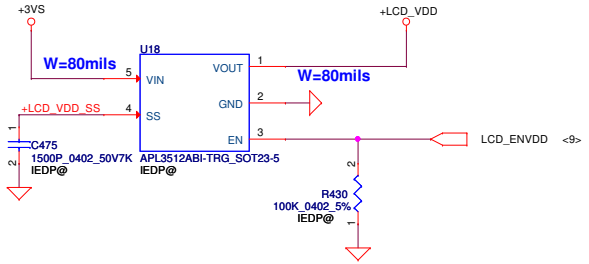
BTO : TOUCH_EMI@



EMI request - Close to JEDP connector

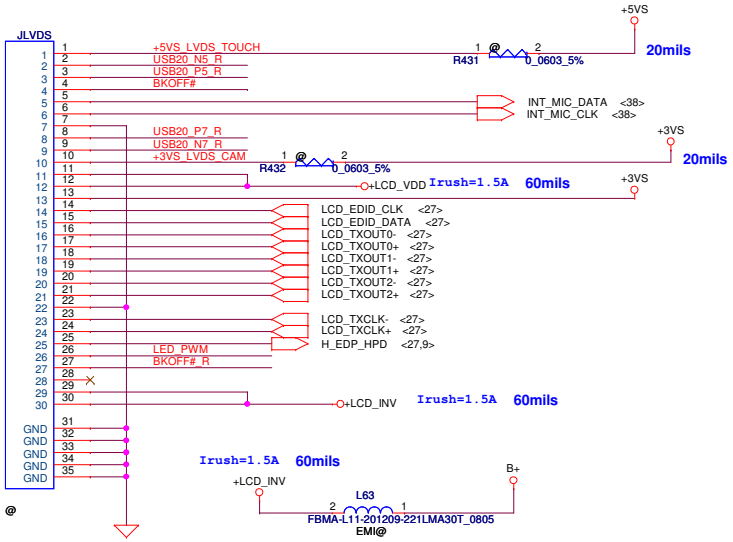


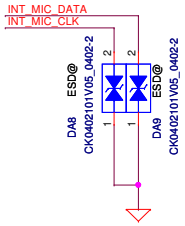
LCD POWER CIRCUIT (For EDP panel only)

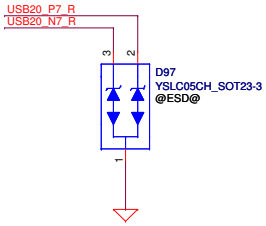


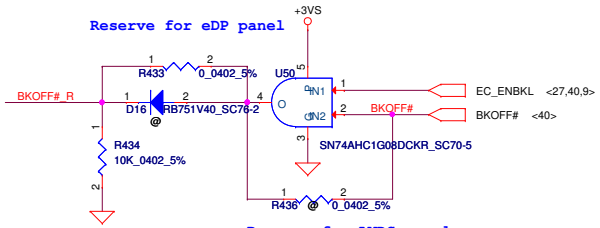
LVDS colay eDP cable

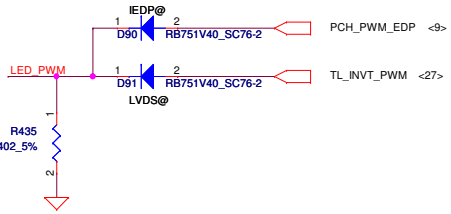
Pin define will be change after ME ready











Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

Compal Electronics, Inc.

Title: LVDS

Size: Custom	Document Number: VSKTA	Rev: 2.0
Date: Friday, June 21, 2013	Sheet 28 of 57	

Default to PS8401 & PS8201 I2C Control Mode

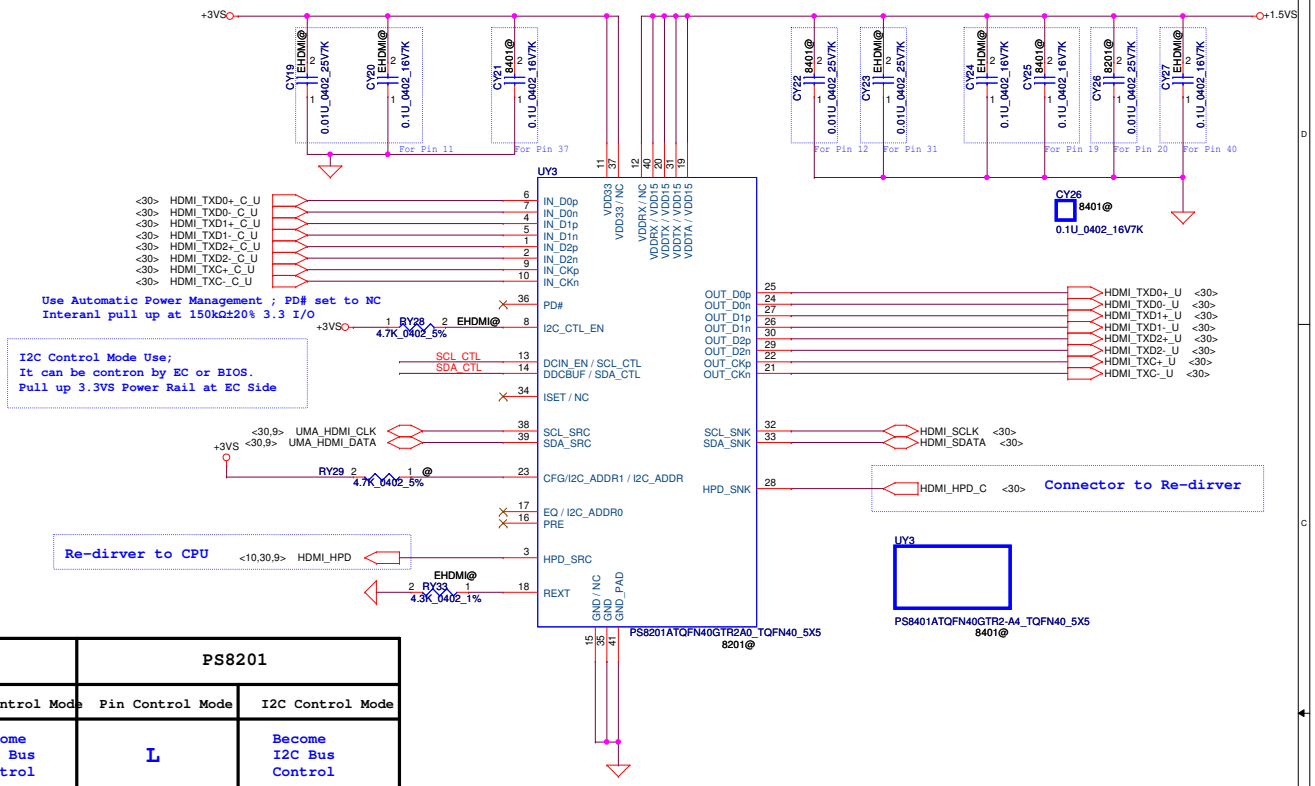
I2C Mode HDMI ID Setting

If PS8401 use I2C Mode , EQ=I2C_ADDR0 , CFG = I2C_ADDR1

For PS8401
I2C control bus address LSB; Internal pull down at 150kohz±20%, 3.3V I/O.
[I2C_ADDR1, I2C_ADDR0] ; I2C Address (W/R)=
- LL: 0x4C/4D (default)
- LH: 0x5C/5D
- HL: 0xCC/CD
- HH: 0xEC/ED

If PS8401 use I2C Mode , EQ=I2C_ADDR

For PS8201
I2C control bus address LSB; Internal pull down at ~150k ohz, 3.3V I/O.
[I2C_ADDR] ; I2C Address (W/R)=
- L: 0x64/65 (default)
- H: 0xE4/E5



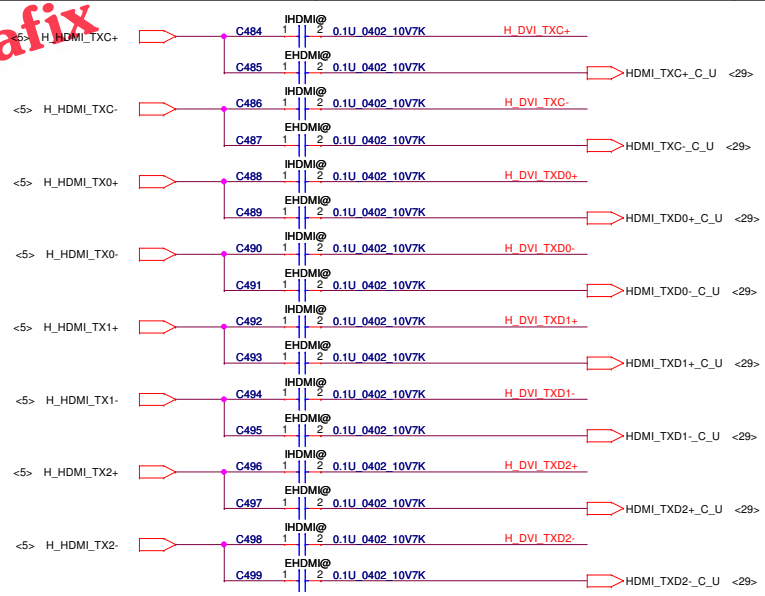
Strap H:3.3V M:1.65V L:0V

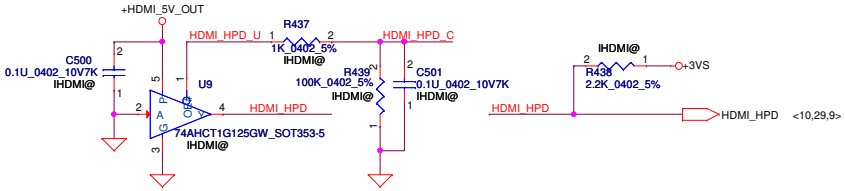
Net name	Description	PS8401		PS8201	
		Pin Control Mode	I2C Control Mode	Pin Control Mode	I2C Control Mode
DCIN_EN	DC cou;ing enable; Internal pull down at 150k ohz ±20%, 3.3V I/O. L: default, AC coupling input H: DC coupling input	L	Become I2C Bus Control	L	Become I2C Bus Control
DDCBUF	Enable active DDC buffer; Internal pull down at 150k?±20%, 3.3V I/O. L: default, passive DDC pass-through H: active DDC buffer with default threshold M: active DDC buffer without internal pull up resistor	M	Become I2C Bus Control	M	Become I2C Bus Control
ISET	TMDS output swing adjustment; Internal pull down at 150kΩ±20%, 3.3V I/O. For PS8401 Only ISET = L: Default H: Increase +13% M: Reduce -13%	L	NC	NC	NC
CFG	CFG: Configuration pin, 3.3V IO, internal pull down at 150kΩ±20%. 3.3V I/O CFG = L: HDMI ID disable H: HDMI ID enable	H	NC	H	NC
EQ	EQ:Receiver equalization setting;; Internal pull down at ~150k?, 3.3V I/O For PS801 EQ = L:programmable EQ for channel loss up to 6.5dB @ 3.0Gbps H:programmable EQ for channel loss up to 9.5dB @ 3.0Gbps M:programmable EQ for channel loss up to 3dB @ 3.0Gbps For PS8401 EQ = L:programmable EQ for channel loss up to 12.4dB H:programmable EQ for channel loss up to 4.3dB M:programmable EQ for channel loss up to 8.6dB	M	NC	M	NC
PRE	Output pre-emphasis setting; Internal pull down at 150kΩ±20%, 3.3V I/O. PRE = L: No pre-emphasis H: 1.6dB pre-emphasis M: 2.5dB pre-emphasis	L	NC	L	NC
I2C_CTL_EN	I2C Control enable. Internal pull down at 150kΩ±20%. 3.3V I/O I2C_CTL_EN = LOW (L): Pin Control is selected. HIGH (H): I2C Control is selected.	L	H	L	H

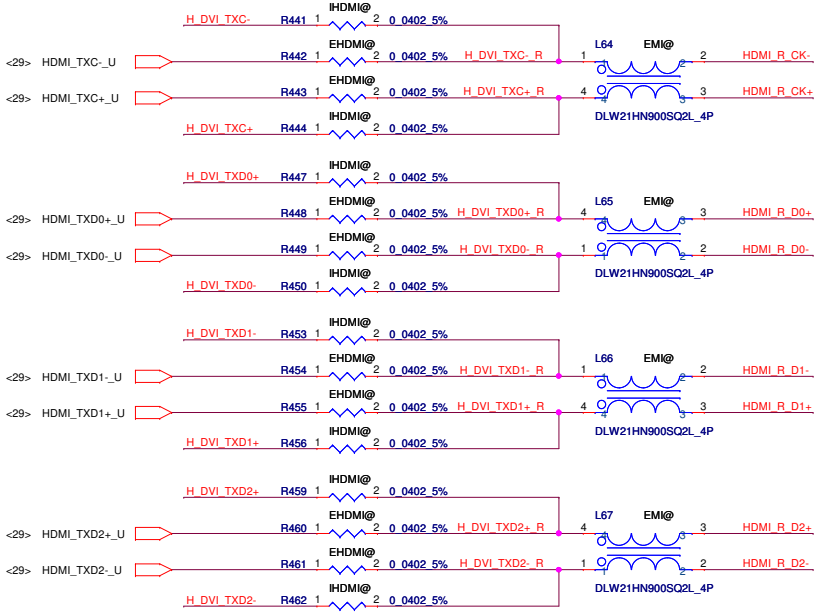
Note: PS8401 have Jitter cleaning function and can control TMDS output swing , PS8201 don't have.

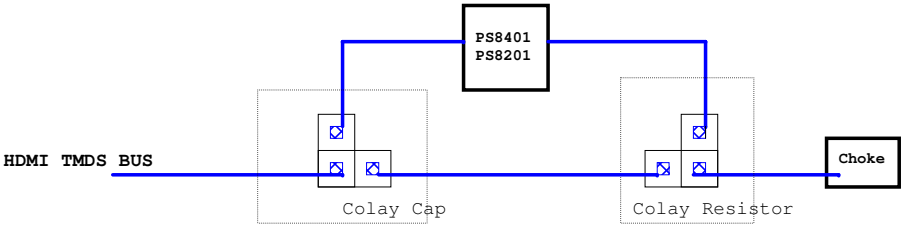
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/10/19	Deciphered Date	2015/10/19

Title	HDMI Re-driver		
Size	Document Number	PS8201A & PS8401A	Rev 2.0
Date: Friday, June 21, 2013		Sheet 29 of 57	



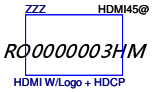






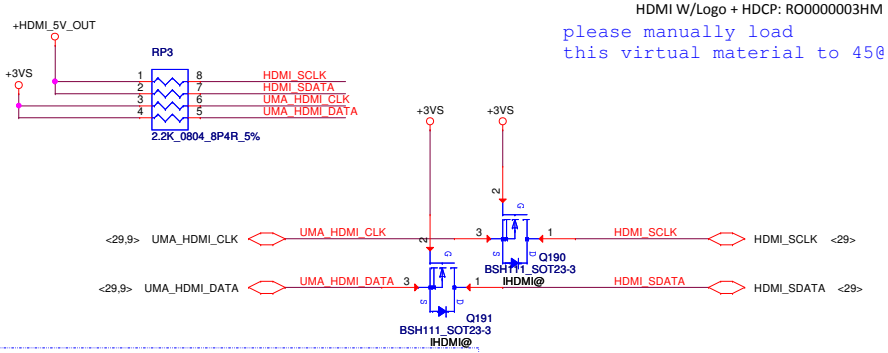
Componet close to Conn.
Impedance depend on platform design guide

HDMI Royalty



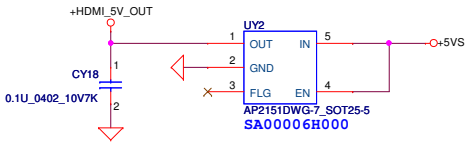
HDMI W/O Logo: RO0000001HM
HDMI W/Logo: RO0000002HM
HDMI W/Logo + HDCP: RO0000003HM

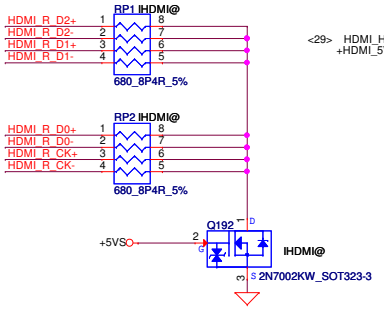
please manually load
this virtual material to 45@ BOM

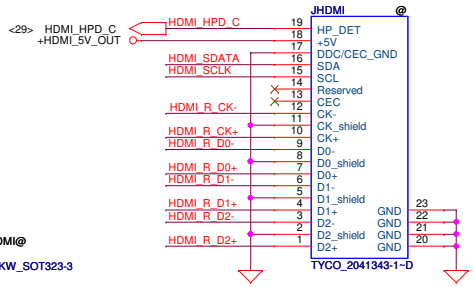


HDMI POWER CIRCUIT

VIN = 5V, IOUT = 0.5A , RDS(ON) TYP=95m ; MAX=115m
Current Limit: TYP=0.8A ; MAX=1A



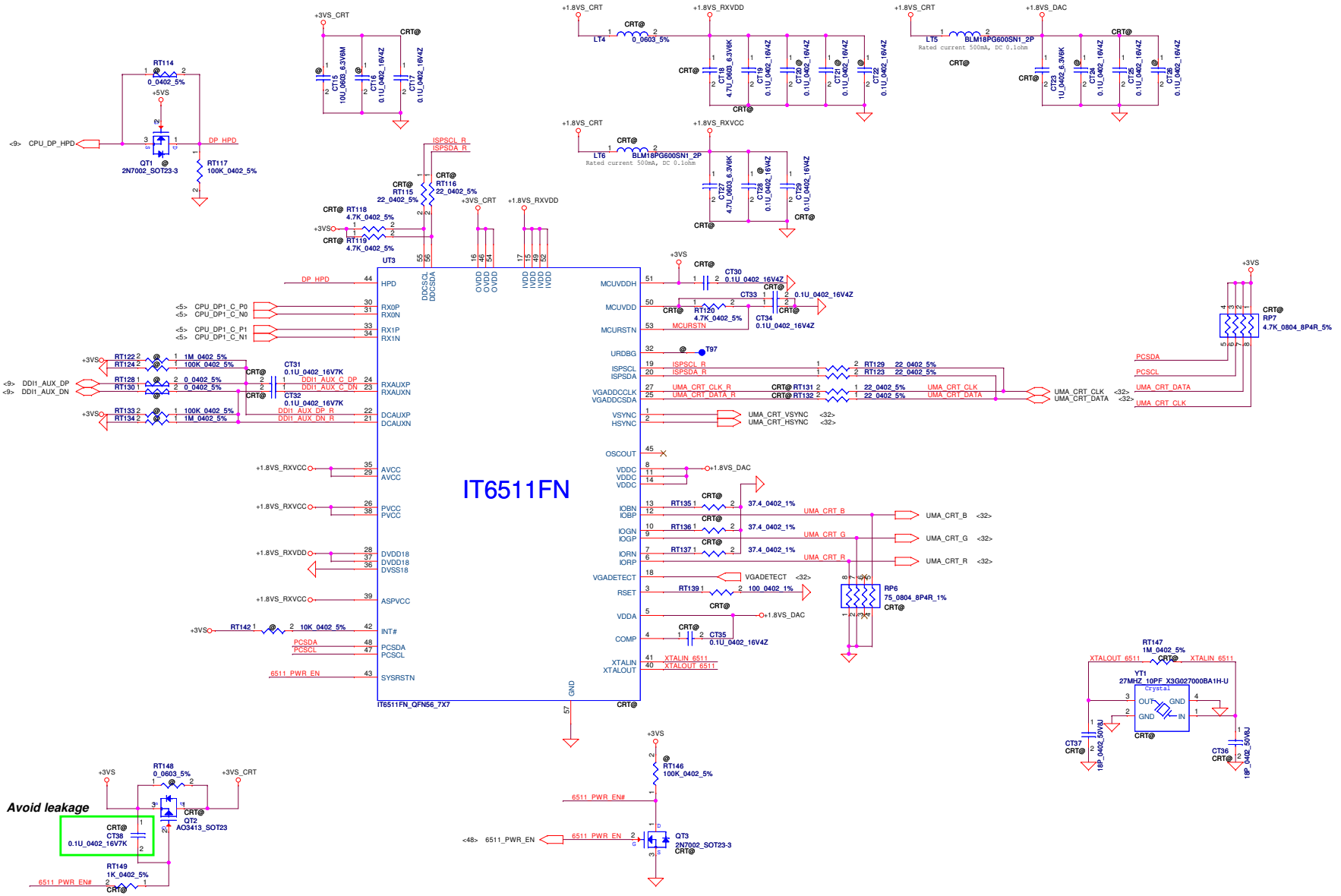




HDMI Connector

Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

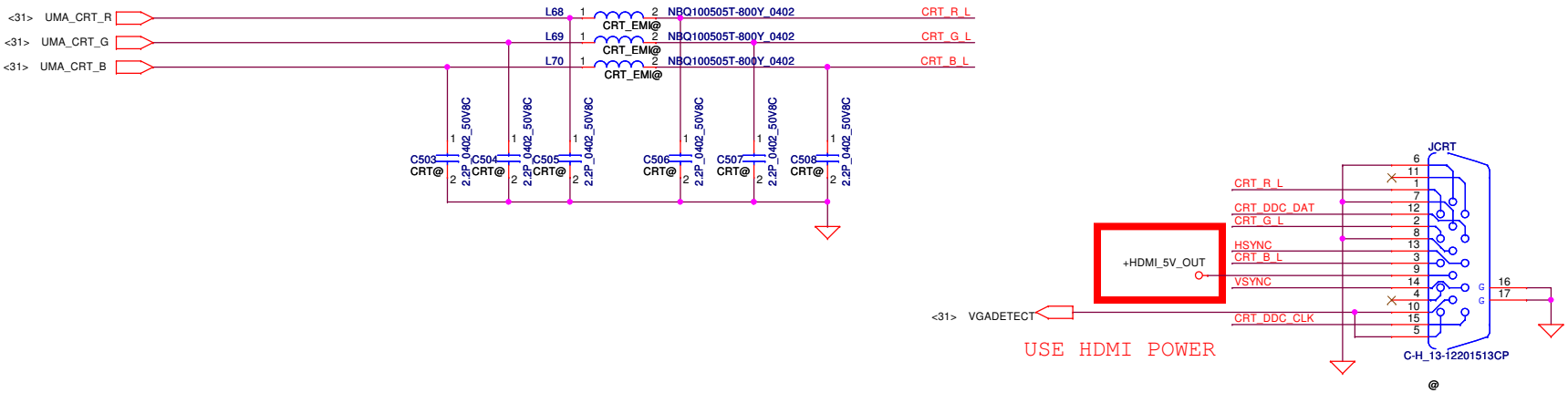
Compal Electronics, Inc.			
Title	HDMI Conn.		
Size	Document Number	VSKTA	Rev 2.0
Date: Friday, June 21, 2013	Sheet 30 of 57		

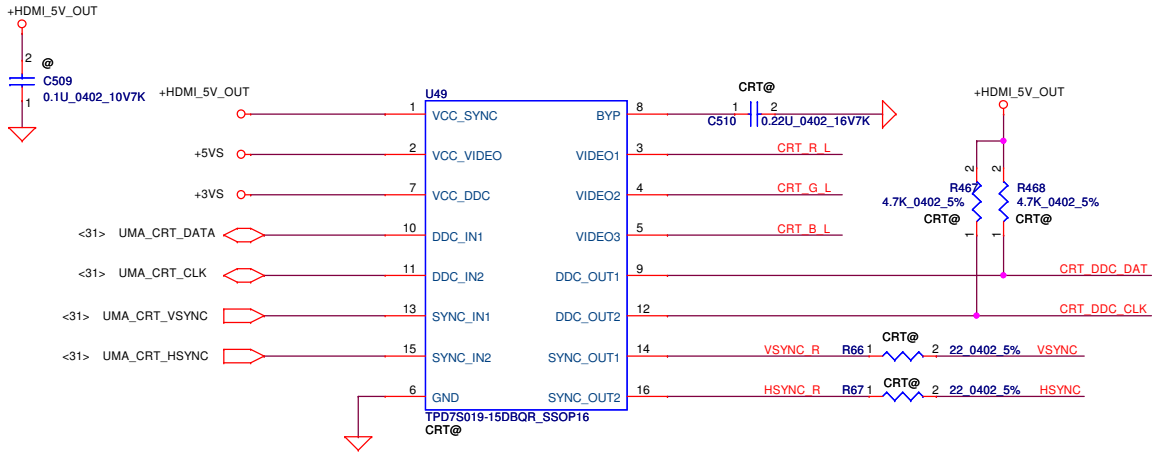


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/10/19	Deciphered Date	Title: DP-CRT_ITE IT6511FN
			Size: Document Number: DP to VGA — Rev: 2.0
			Date: Friday, June 21, 2013 — Sheet 31 of 57

CRT CONNECTOR

BTO : CRT_EMI@





Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

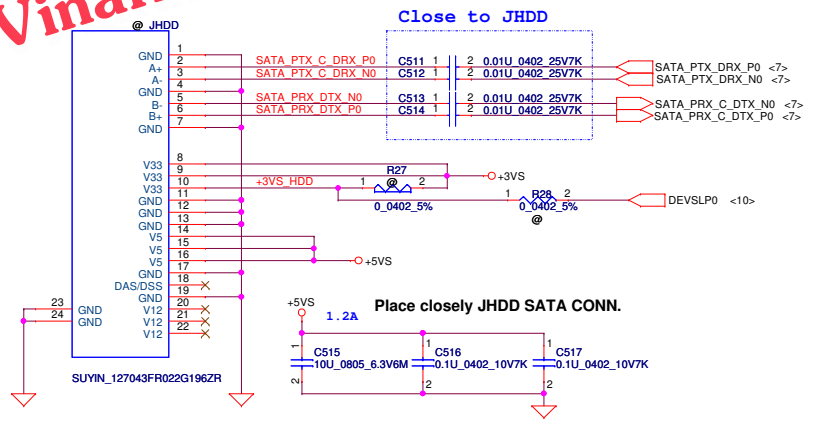
Compal Electronics, Inc.

Title: CRT

Size | Document Number: VSKTA | Rev: 2.0

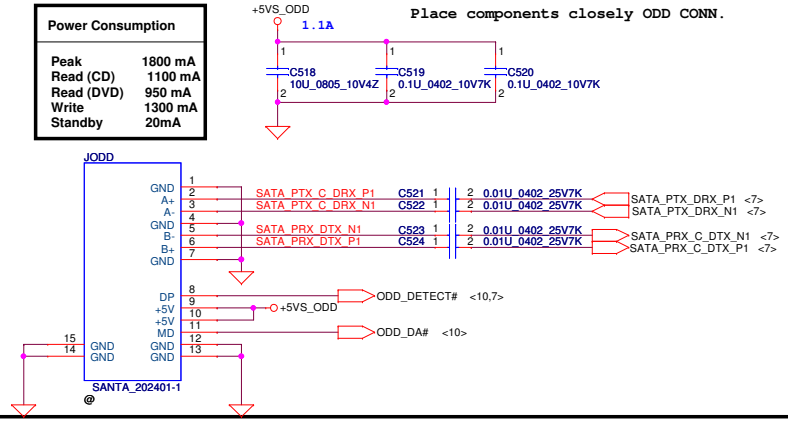
Date: Friday, June 21, 2013 | Sheet 32 of 57

SATA HDD Conn.

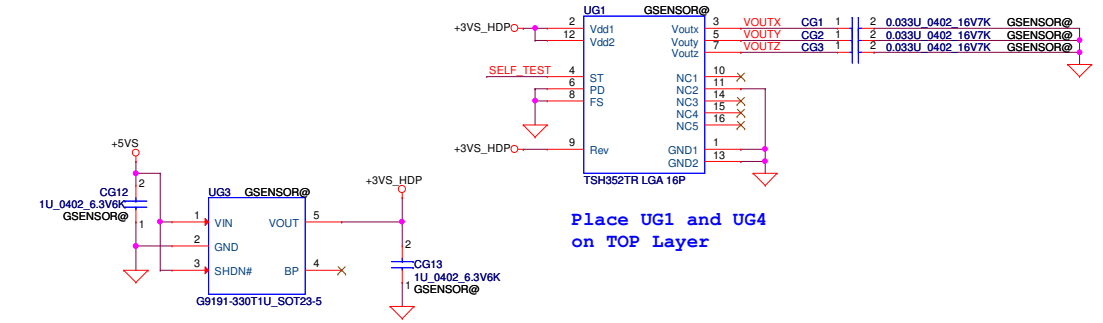


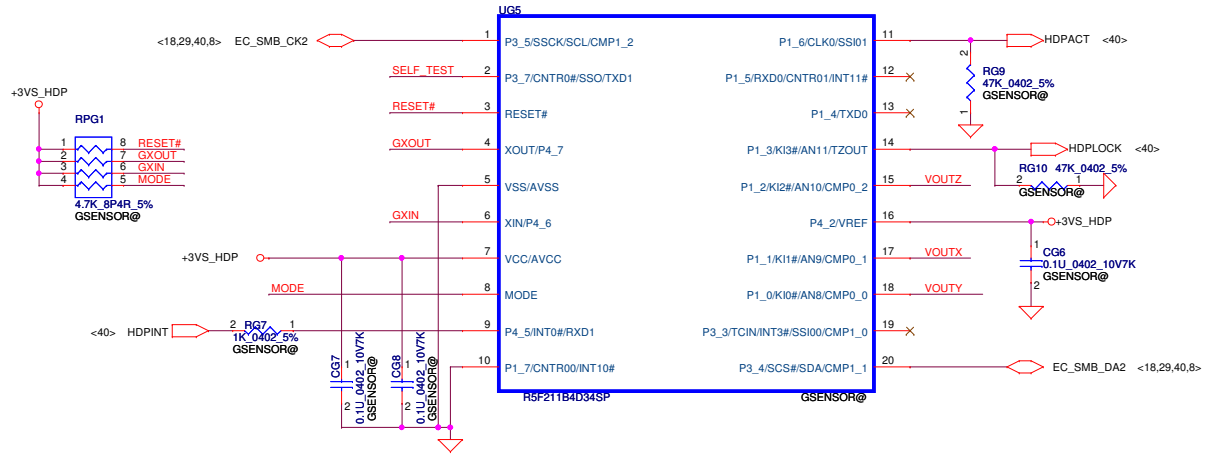
SATA ODD Conn

Power Consumption	
Peak	1800 mA
Read (CD)	1100 mA
Read (DVD)	950 mA
Write	1300 mA
Standby	20mA



G-Sensor





Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

Compal Electronics, Inc.

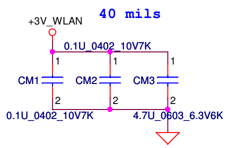
Title: HDD/ODD/Gsensor

Size: Document Number: VSKTA Rev: 2.0

Date: Friday, June 21, 2013 Sheet 33 of 57

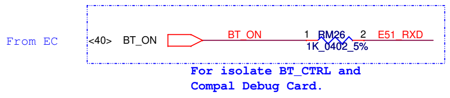
Vinafix

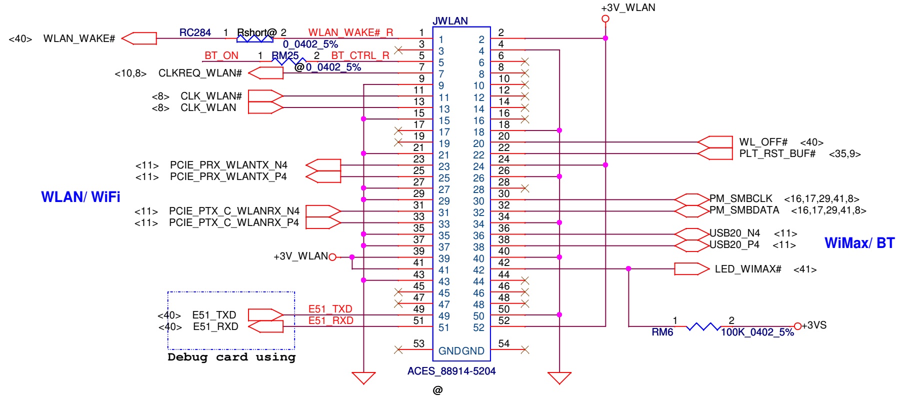
Slot 1 Half PCIe Mini Card-WLAN



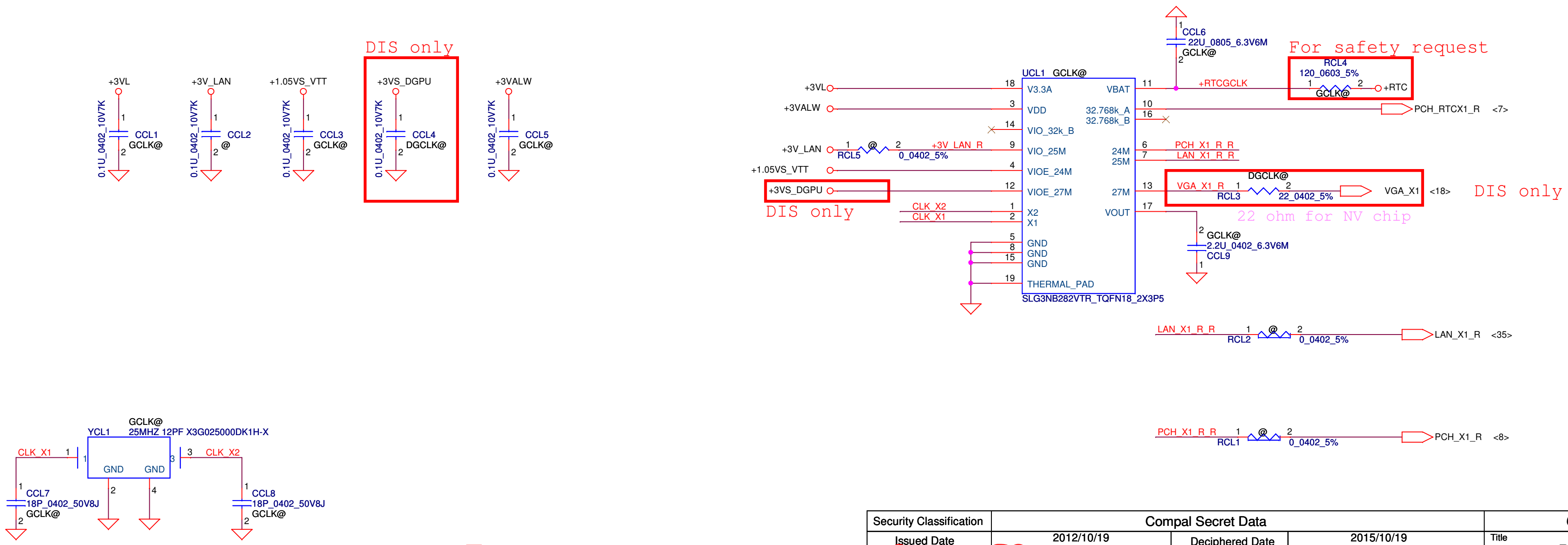
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON	H	L





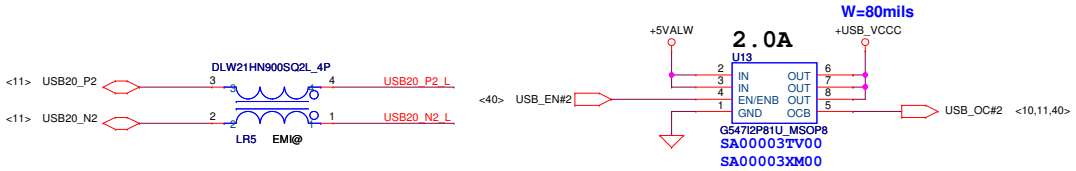
WLAN/ WiFi
WiMax/ BT
JWLAN
ACES_88914-5204
+3V_WLAN
<40> WLAN_WAKE#
RC284
Rshort@
0_0402_5%
WLAN_WAKE#_R
BT_ON
RM25
@0_0402_5%
BT_CTRL_R
<10,8> CLKREQ_WLAN#
<8> CLK_WLAN#
<8> CLK_WLAN
<11> PCIE_PRX_WLANTX_N4
<11> PCIE_PRX_WLANTX_P4
<11> PCIE_PTX_C_WLANRX_N4
<11> PCIE_PTX_C_WLANRX_P4
+3V_WLAN
<40> E51_TXD
<40> E51_RXD
E51_TXD
E51_RXD
Debug card using
WL_OFF# <40>
PLT_RST_BUF# <35,9>
PM_SMBCLK <16,17,29,41,8>
PM_SMBDATA <16,17,29,41,8>
USB20_N4 <11>
USB20_P4 <11>
LED_WIMAX# <41>
RM6
100K_0402_5%
+3VS
GND GND



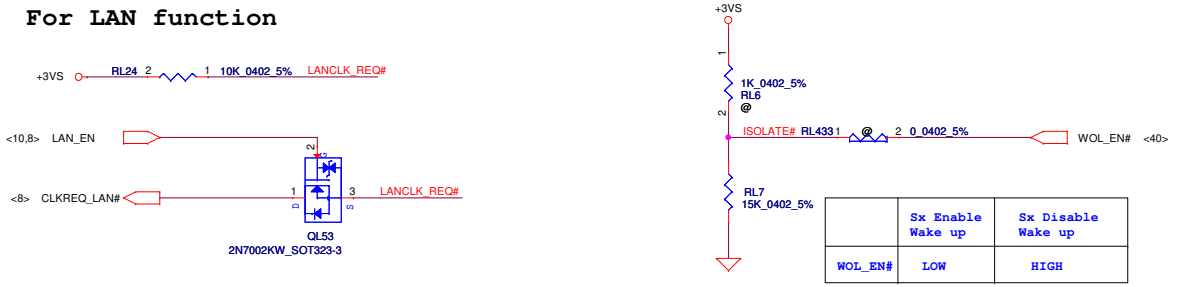
DIS only
+3VL
+3V_LAN
+1.05VS_VTT
+3VS_DGPU
+3VALW
CCL1 GCLK@
CCL2 @
CCL3 GCLK@
CCL4 DGCLK@
CCL5 GCLK@
0.1U_0402_10V7K
CCL6
22U_0805_6.3V6M
GCLK@
For safety request
RCL4
120_0603_5%
GCLK@
+RTC
+RTCGCLK
UCL1 GCLK@
V3.3A
VBAT
VDD
32.768k_A
32.768k_B
VIO_32k_B
VIO_25M
VIOE_24M
VIOE_27M
X2
X1
24M
25M
27M
VOUT
GND
THERMAL_PAD
SLG3NB282VTR_TQFN18_2X3P5
PCH_RTCX1_R <7>
RCL5
+3V_LAN_R
0_0402_5%
PCH_X1_R_R
LAN_X1_R_R
DGCLK@
VGA_X1_R
RCL3
22_0402_5%
VGA_X1 <18>
22 ohm for NV chip
CLK_X2
CLK_X1
GCLK@
2.2U_0402_6.3V6M
CCL9
RCL2
0_0402_5%
LAN_X1_R <35>
RCL1
PCH_X1_R <8>
YCL1
25MHZ 12PF X3G025000DK1H-X
CCL7
18P_0402_50V8J
CCL8
18P_0402_50V8J

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/10/19	Deciphered Date	2015/10/19	Title: PCIe-WLAN/GCLK
				Size / Document Number: VSKTA / Rev 2.0
				Date: Friday, June 21, 2013 / Sheet 34 of 57

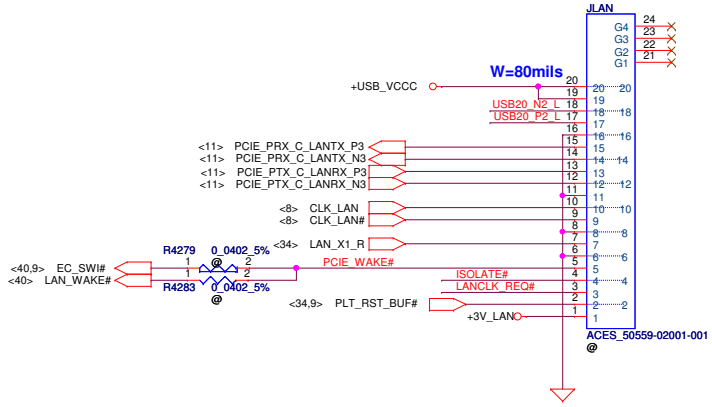
Left USB 2.0 x 1



For LAN function



	Sx Enable Wake up	Sx Disable Wake up
WOL_EN#	LOW	HIGH



+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

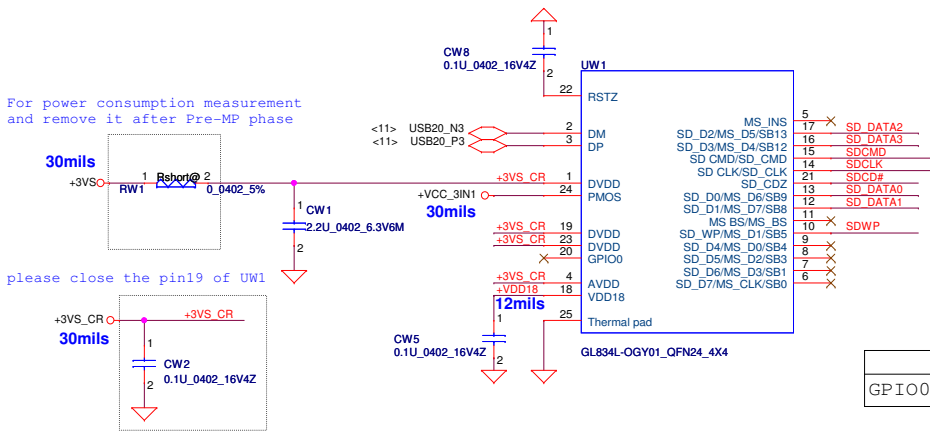
Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

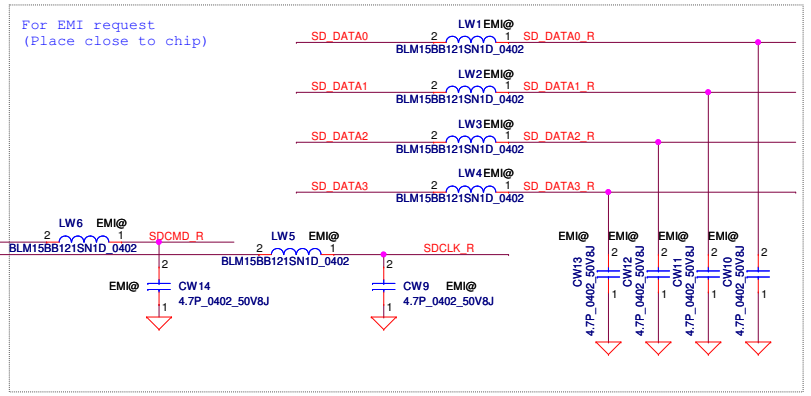
Compal Electronics, Inc.

Title: PCIe-LAN-RTL8111G-CG/LUSB

Size: Custom | Document Number: VSKTA | Rev: 2.0

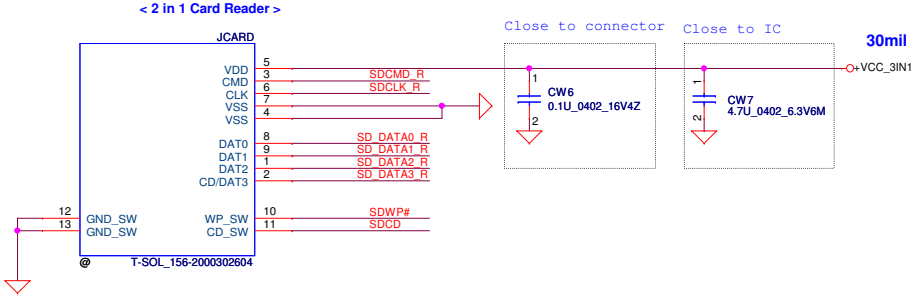
Date: Friday, June 21, 2013 | Sheet 35 of 57





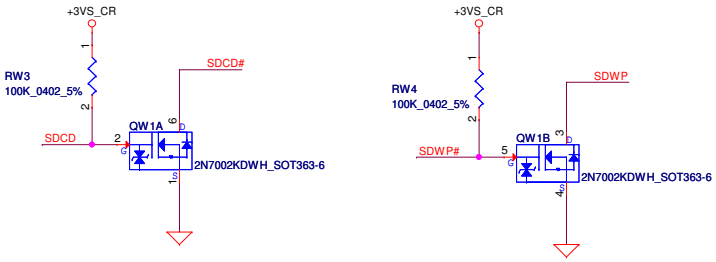
	NC (default)	10K pull down
GPIO0	Power saving mode	Normal mode

De-coupling and Bulk capacitor should place near to Cardreader chip and Combo Socket



"Normal Close" type connector

	CD_SW	WP_SW	
		Protect disable	Protect Enable
Card Uninsertion	Close	Close	Close
Card Insertion	Open	Open	Close

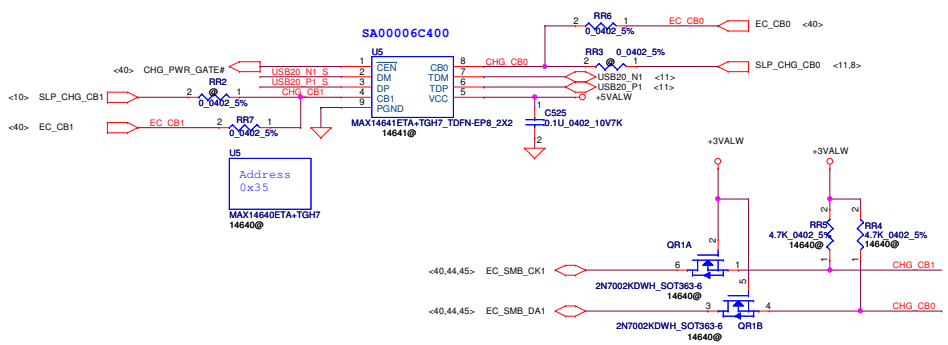


Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

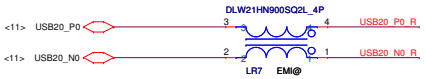
Compal Electronics, Inc.			
Title: USB-CardReader Genesys GL834L-OGY			
Size: Custom	Document Number: VSKTA		Rev: 2.0
Date: Friday, June 21, 2013	Sheet: 36	of: 57	

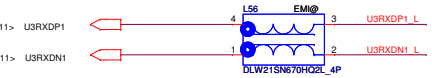
USB Sleep & Charge

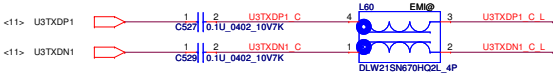
State table for MAX14641			
CB0	CB1	Mode	STATUS
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.

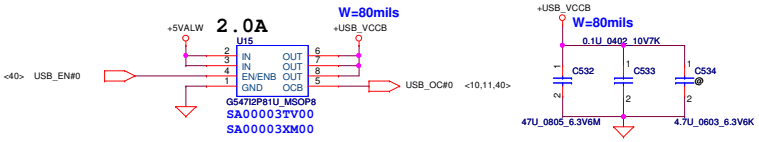


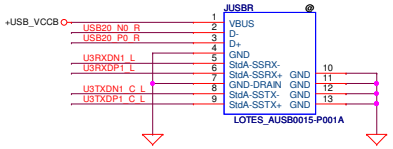
Right rear USB3.0 Conn.

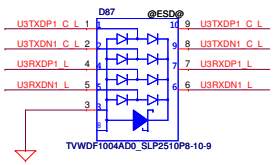




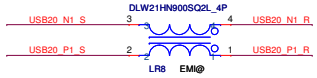


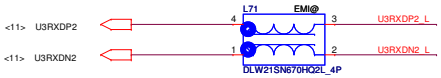


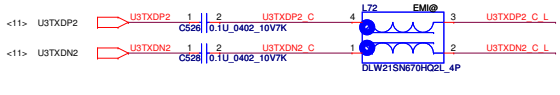


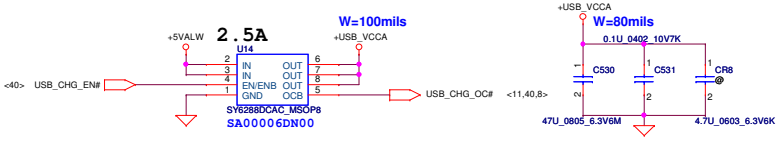


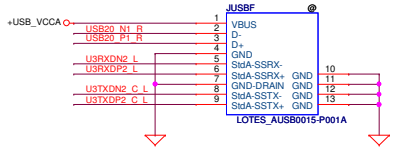
Right front USB3.0 Conn. (Support S&C function)

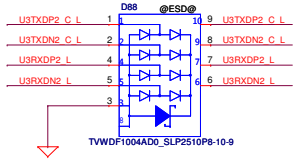












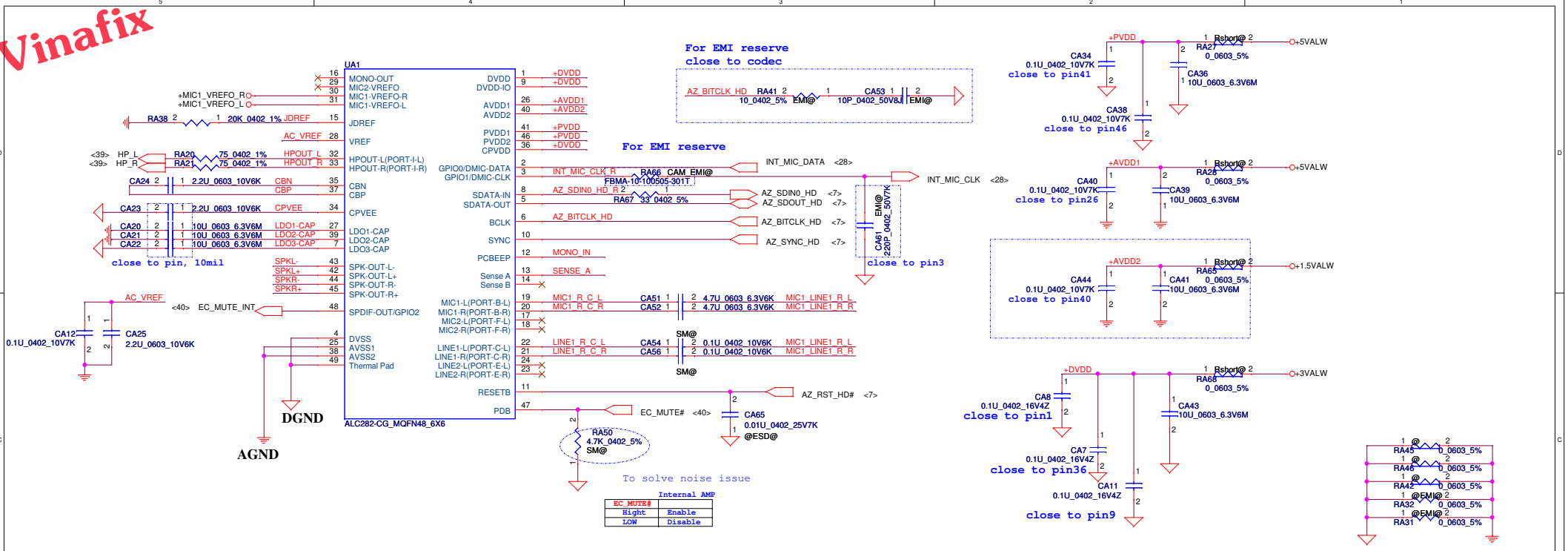
Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

Compal Electronics, Inc.

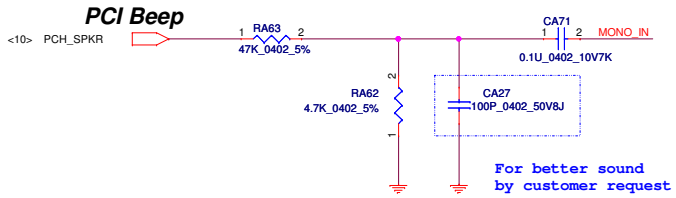
Title: RUSB/S&C MAXIM MAX14641

Size: Custom | Document Number: VSKTA | Rev: 2.0

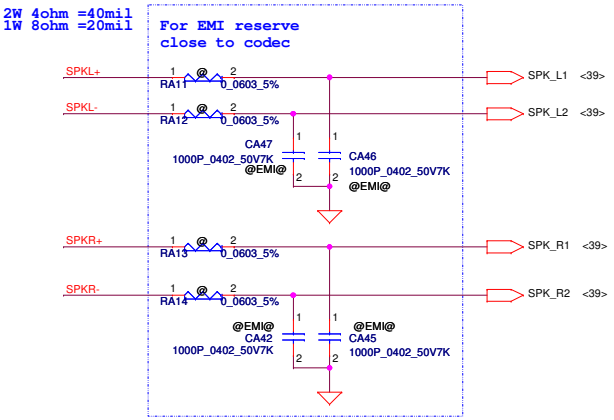
Date: Friday, June 21, 2013 | Sheet 37 of 57



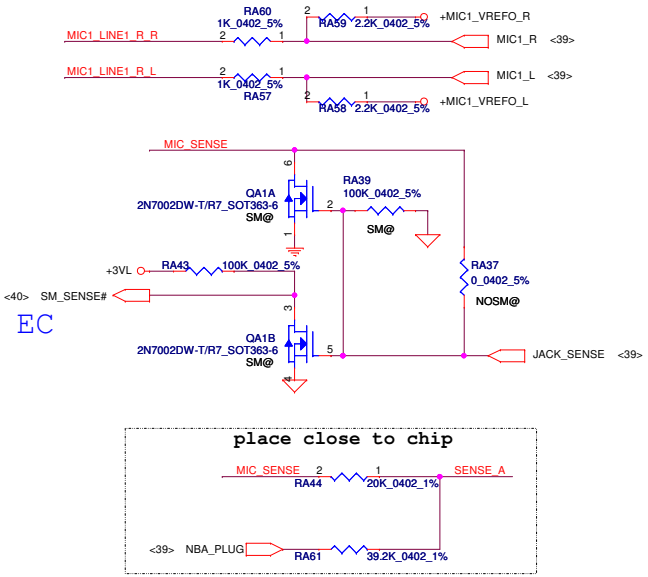
Beep sound



SPK



MIC/LINE IN



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

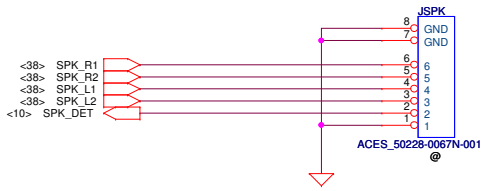
Compal Electronics, Inc.

Title: Cover Sheet

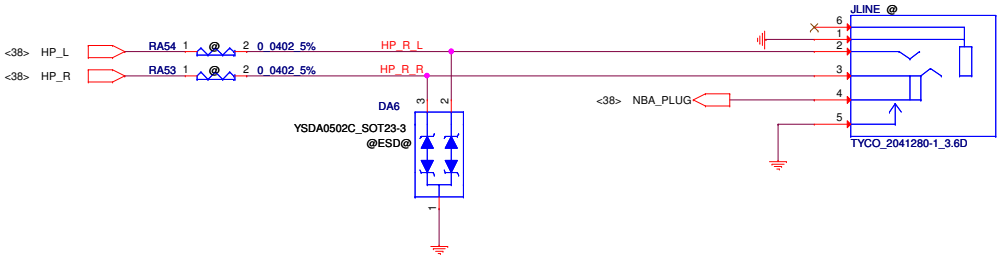
Size: Custom | Document Number | Rev: 2.0

Date: Friday, June 21, 2013 | Sheet 38 of 57

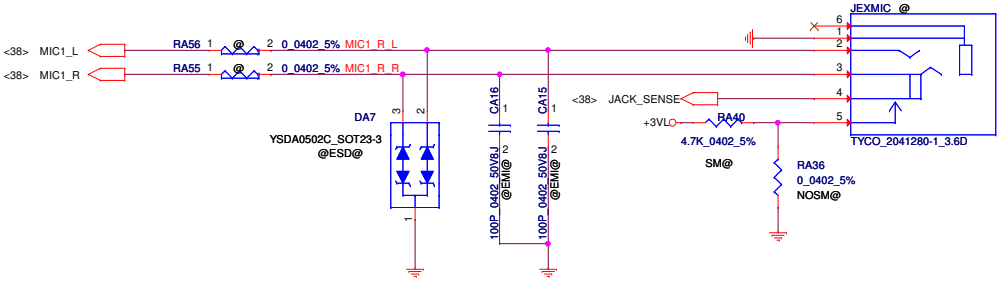
SPK Conn.



HeadPhone/LINE Out JACK



MIC/LINE IN JACK



Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

Compal Electronics, Inc.

Title: Conn

Size: Custom | Document Number | Rev: 2.0

Date: Friday, June 21, 2013 | Sheet 39 of 57

For EMI

CLK_PCI_EC
RB4 10_0402_5% @EMI@
CB11 22P_0402_50V8J @EMI@

+3VL
RB2 47K_0402_5%
EC_RST#
CB12 0.1U_0402_10V7K

ESD@ CB13 0.1U_0402_10V7K PLT_RST#

<41> KSI[0..7] KSI[0..7]
<41> KSO[0..15] KSO[0..15]

+3VL
RB12 10K_0402_5% CHG_PWR_GATE#

RPB1 2.2K_8P4R_5%
+3VL EC_SMB_CK1
EC_SMB_DA1
+3VS EC_SMB_CK2
EC_SMB_DA2

RB27 100K_0402_5% E51_TXD
RB39 4.7K_0402_5% EC_MUTE_INT_R

Signal pull high is default status (ROM only mode).
If signal pull low, EC will send translator code to chip.(EP mode)

+3VL
LVDS@ RB26 10K_0402_5%
TRANS_SEL
@ RB25 10K_0402_5%
For Translator select

0.1U_0402_10V7K: CB1, CB2, @CB4, @CB5, CB3
CB4 0.1U_0402_10V7K

UB1 KB9012QF-A3_LQFP128_14X14
9012@ UB1 NPCE885NB0DX LQFP 128P 885@

EC_VDD/VCC, EC_VDD/AVCC

PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
GPIO
GPO
GPI
LPC & MISC
Int. K/B Matrix
SM Bus

GATEA20/GPIO00
KBRST#/GPIO01
SERIRQ
LPC_FRAME#
LPC_AD3
LPC_AD2
LPC_AD1
LPC_AD0
CLK_PCI_EC
PLT_RST#
EC_RST#
EC_SCI#/GPIO0E
GPIO1D

KSI0/GPIO30
KSI1/GPIO31
KSI2/GPIO32
KSI3/GPIO33
KSI4/GPIO34
KSI5/GPIO35
KSI6/GPIO36
KSI7/GPIO37
KSO0/GPIO20
KSO1/GPIO21
KSO2/GPIO22
KSO3/GPIO23
KSO4/GPIO24
KSO5/GPIO25
KSO6/GPIO26
KSO7/GPIO27
KSO8/GPIO28
KSO9/GPIO29
KSO10/GPIO2A
KSO11/GPIO2B
KSO12/GPIO2C
KSO13/GPIO2D
KSO14/GPIO2E
KSO15/GPIO2F
KSO16/GPIO48
KSO17/GPIO49
TRANS_SEL
CHG_PWR_GATE#

EC_SMB_CK1/GPIO44
EC_SMB_DA1/GPIO45
EC_SMB_CK2/GPIO46
EC_SMB_DA2/GPIO47

PM_SLP_S3#/GPIO04
PM_SLP_S5#/GPIO07
EC_SMI#/GPIO08
GPIO0A
GPIO0B
GPIO0C
GPIO0D
EC_INVT_PWM/GPIO11
FAN_SPEED1/GPIO14
EC_PME#/GPIO15
EC_TX/GPIO16
EC_RX/GPIO17
PCH_PWROK/GPIO18
SUSP_LED#/GPIO19
NUM_LED#/GPIO1A

XCLKI/GPIO5D
XCLKO/GPIO5E

GPIO0F
BEEP#/GPIO10
GPIO12
ACOFF/GPIO13
BATT_TEMP/GPIO38
GPIO39
ADP_I/GPIO3A
GPIO3B
GPIO42
IMON/GPIO43
DAC_BRIG/GPIO3C
EN_DFAN1/GPIO3D
IREF/GPIO3E
CHGVADJ/GPIO3F
EC_MUTE#/GPIO4A
USB_EN#/GPIO4B
CAP_INT#/GPIO4C
EAPD/GPIO4D
TP_CLK/GPIO4E
TP_DATA/GPIO4F
CPU1.5V_S3_GATE/GPXIOA00
WOL_EN/GPXIOA01
ME_EN/GPXIOA02
VCIN0_PH/GPXIOD00
SPIDI/GPIO5B
SPIDO/GPIO5C
SPICLK/GPIO5B
SPICS#/GPIO5A
ENBKL/GPIO40
PECI_KB930/GPIO41
FSTCHG/GPIO50
BATT_CHG_LED#/GPIO52
CAPS_LED#/GPIO53
PWR_LED#/GPIO54
BATT_LOW_LED#/GPIO55
SYSON/GPIO56
VR_ON/GPIO57
PM_SLP_S4#/GPIO59
EC_RSMRST#/GPXIOA03
EC_LID_OUT#/GPXIOA04
PROCHOT_IN/GPXIOA05
H_PROCHOT#_EC/GPXIOA06
VCOUT0_PH/GPXIOA07
BKOFF#/GPXIOA08
PBTN_OUT#/GPXIOA09
PCH_APWROK/GPXIOA10
SA_PGOOD/GPXIOA11
AC_IN/GPXIOD01
EC_ON/GPXIOD02
ON/OFFBTN#/GPXIOD03
LID_SW#/GPXIOD04
SUSP#/GPXIOD05
GPXIOD06
PECI_KB9012/GPXIOD07
V18R

WL_BT_LED# <41>
USB_EN#0 <37>
FANPWM <7>
CLK_REQ_GC6# <18>
BATT_PRES
BATT_PRES <44>
USB_OC#0 <10,11,37>
ADP_I <44,45>
ADP_V <45>
HDPLOCK <33>
EC_ENBKL <27,28,9>
HDPINT <33>
885_EC_ON
CB0_WAKE#
VCCST_PWRGD <12,48>
EC_MUTE# <38>
PM_SLP_S4# <9>
EC_SMB_CK3 <27>
EC_SMB_DA3 <27>
TP_CLK <41>
TP_DATA <41>
EC_CB1 <37>
GPS_DOWN# <18>
PWRME_CTRL <7>
VCIN0_PH <44>
EC_SDIO <8>
EC_SDI <8>
EC_SCK <8>
EC_CS0# <8>
WLAN_WAKE#
EC_SMI# <35>
HDPACT <33>
BATT_FULL_LED# <41>
CAPS_LED# <41>
PWR_SUSP_LED# <41>
BATT_CHG_LOW_LED# <41>
SYSON <46>
VCCST_PG_EC <12,9>
FB_CLAMP <18,19,22>
PCH_RSMRST# <9>
EC_LID_OUT# <10>
PROCHOT_IN <44>
H_PROCHOT# EC
VCOUT0_PH_L
BKOFF# <28>
PBTN_OUT# <9>
PCH_PWR_EN <42,49>
EC_SWI# <35,9>
ACIN
EC_ON_R
ON/OFFBTN# <41>
LID_SW# <41>
SUSP# <42,48>
+VTT_EC
EC_PECI
+EC_V18R
ACIN <45,9>
+1.05VS_VTT
H_PECI <5>

Reserve this signal to EC by SW demand 2011/10/18a
VCIN0_PH connect to power portion (9012 only)
PROCHOT_IN connect to power portion (9012 only)
VCOUT0_PH connect to power portion (9012 only)

<50> VR_HOT# RB11 @ 2_0_0402_5% H_PROCHOT# <5>
H_PROCHOT# EC
QB1 2N7002_SOT23-3
CB8 47P_0402_50V8J

BATT_PRES @CB9 100P_0402_50V8J
ACIN CB10 100P_0402_50V8J

CB0_WAKE# RR8 0_0402_5% LAN_WAKE# <35>
RR9 0_0402_5% EC_CB0 <37>

H_PROCHOT# EC RB6 10K_0402_5%
LID_SW# RB35 47K_0402_5%
WLAN_WAKE# RB37 47K_0402_5%

TP_CLK RB8 4.7K_0402_5%
TP_DATA RB9 4.7K_0402_5%
EC_SMB_CK3 RB15 2.2K_0402_5%
EC_SMB_DA3 RB16 2.2K_0402_5%

SYSON RB10 4.7K_0402_5%
SUSP# RB21 10K_0402_5%

VCOUT0_PH_L RB34 0_0402_5% VS_ON <47>

<38> EC_MUTE_INT RB38 0_0402_5% EC_MUTE_INT_R
<9> CLK_EC RB5 0_0402_5%
<47,9> POK RB7 0_0402_5% POK_R
@ RB22 100K_0402_5% CB16 20P_0402_50V8 @

RB31 885@ 0_0402_5%
RB19 43_0402_5%
CB15 4.7U_0805_10V4Z

885@ RB20 330K_0402_5% +3VL
9012@ RB36 0_0402_5% EC_ON <47>
QB2 2N7002K_SOT23-3 885@
CB50 1U_0402_6.3V6K @
885_EC_ON RB24 885@ 10K_0402_5%
For KB9012 EC_ON low pulse work around

Close to EC
SUSP# ESD@ CB14 0.1U_0402_10V7K

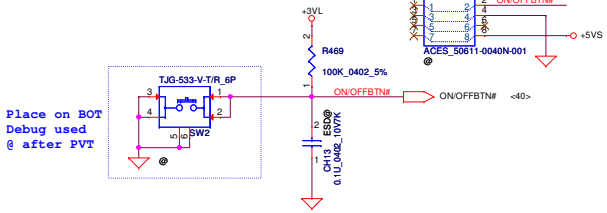
Voltage Comparator Pins FOR 9012 A3

VCIN0 pin109 VCIN1 pin102	>1.2V	<1.2V
VCOUT0 pin104	HIGH (default)	LOW
VCOUT1 pin103	HIGH (default)	LOW

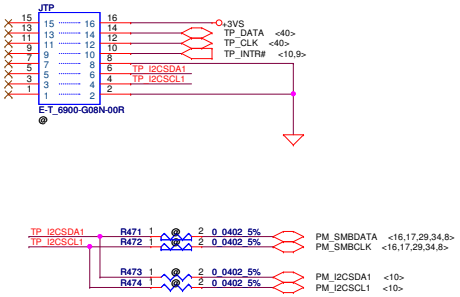
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/10/19	Deciphered Date 2015/10/19	Title: LPC-EC-KB9012&930
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: Document Number: Rev 2.0
			Date: Friday, June 21, 2013 Sheet 40 of 57

Power Button

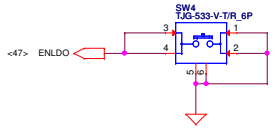
Conn.



Touchpad Connector

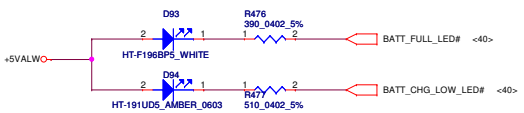


Battery Reset



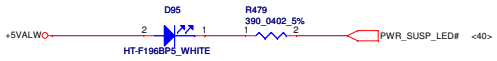
LED/LID

BATT CHARGE /FULL LED



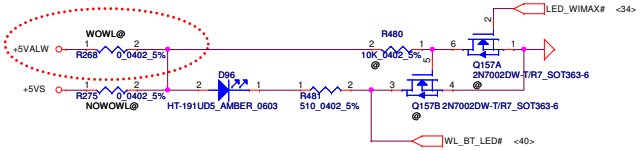
White LED bright when both AC-adaptor is plugged in and Battery is full charged
Amber LED bright while charging battery from AC-adaptor.
Amber LED blink during Critical Low Battery

POWER LED



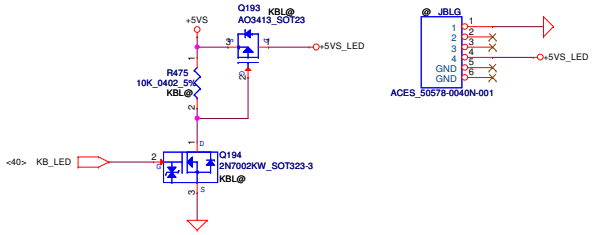
White LED bright when system is power on.
White LED blink when system is sleep mode.

WLAN/WiMAX LED

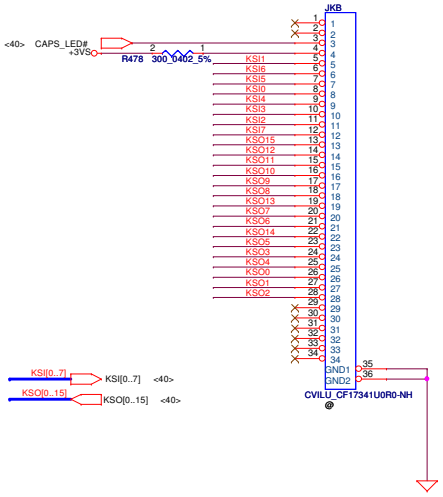


Amber LED bright while Wireless and/or WiMAX turns on.

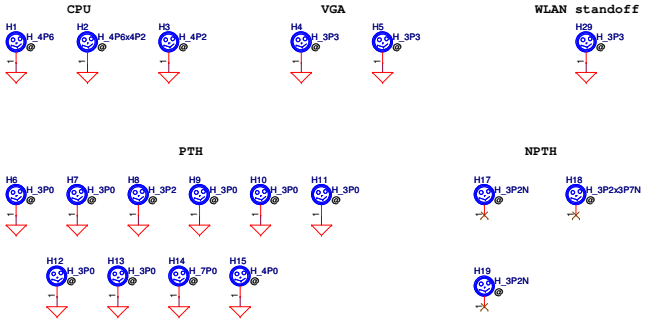
Keyboard LED



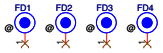
NEW KEYBOARD CONN.



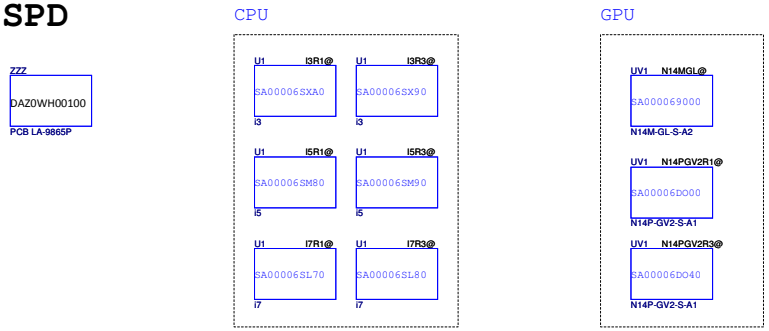
Screw Hole



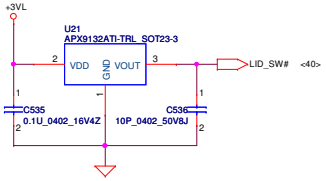
PCB Fedical Mark PAD



ISPD



Lid SW



Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

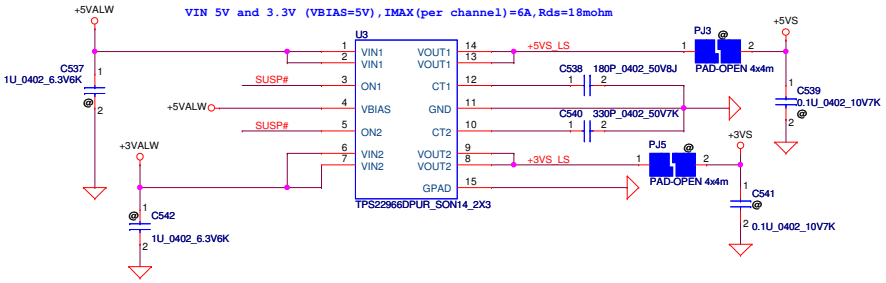
Compal Electronics, Inc.

Title: TP/ISPD/KB/Screw

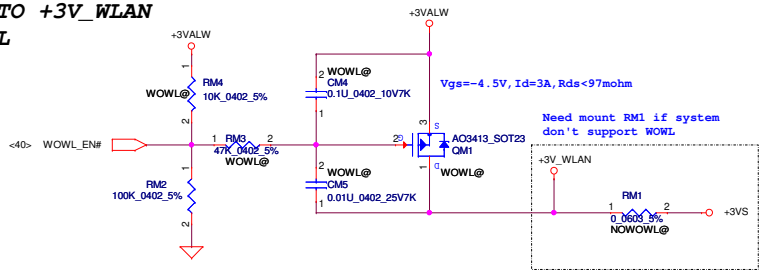
Size	Document Number	Rev
	VSKTA	2.0

Date: Friday, June 21, 2013 Sheet 41 of 57

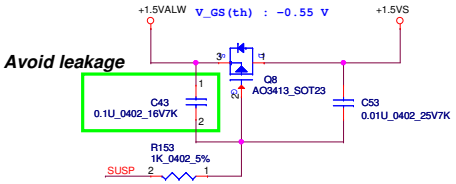
+3VALW TO +3VS
+5VALW TO +5VS
Load Switch

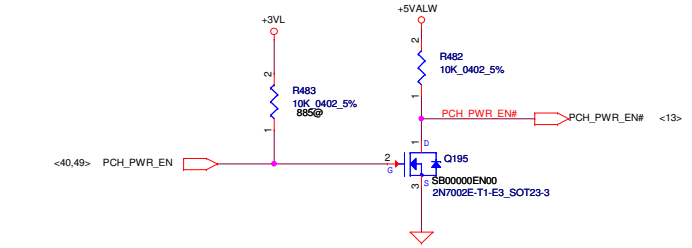


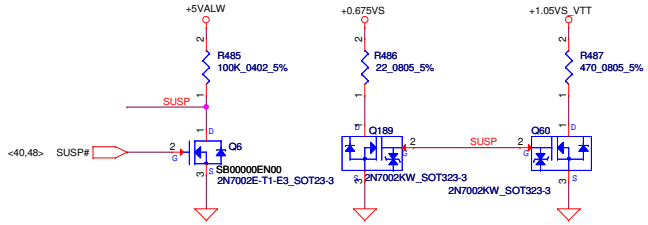
+3VALW TO +3V_WLAN
for WOWL



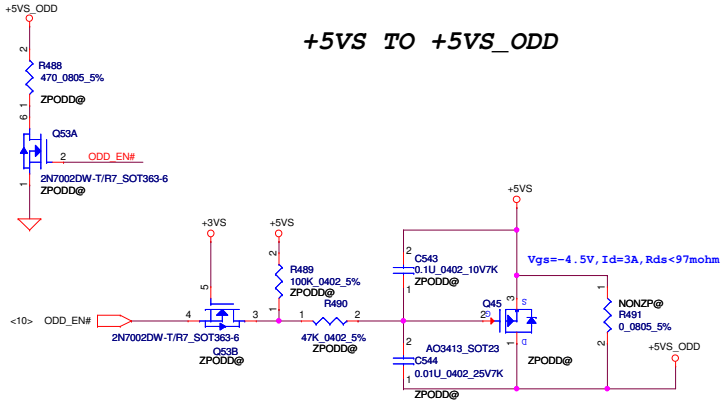
+1.5VALW to +1.5VS







+5VS TO +5VS_ODD



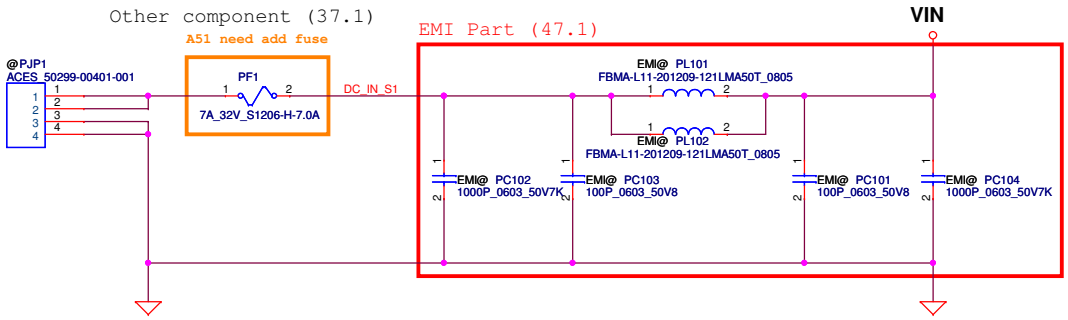
Security Classification	Compal Secret Data		
Issued Date	2012/10/19	Deciphered Date	2015/10/19

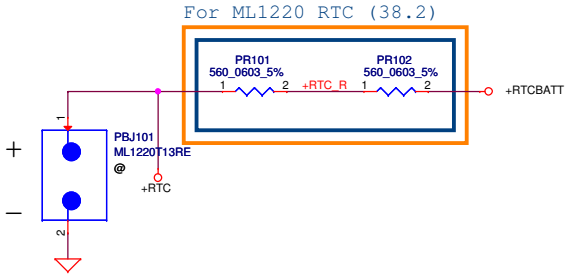
Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size | Document Number: VSKTA | Rev: 2.0

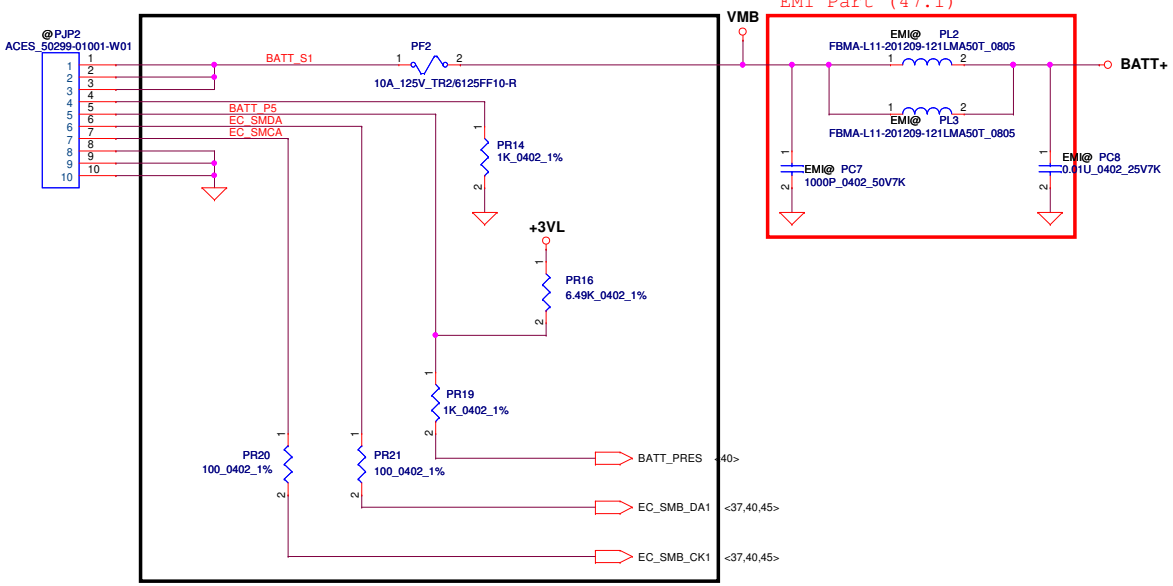
Date: Friday, June 21, 2013 | Sheet 42 of 57



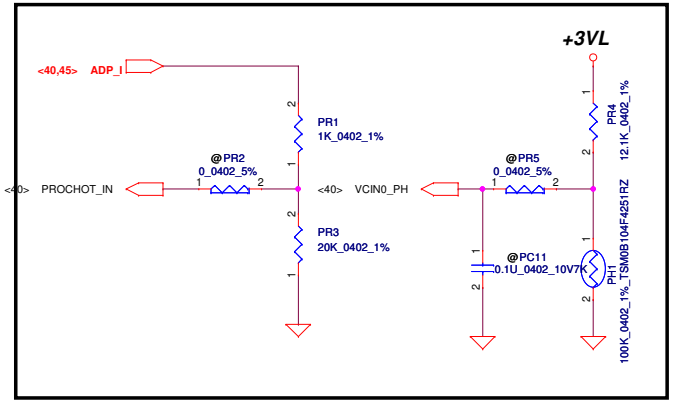


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: DCIN
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: Document Number: VSKTA — Rev: 2.0
			Date: — Sheet 43 of 57

Other component (37.1)



OTP (39.7)



	Initial	Recovery
45W Int GPU	0.55V	0.43V
75W N14P-GV2	0.90V	0.72V

	Initial	Recovery
CPU OTP	90 C	70 C

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: BATTERY CONN / OTP
			Size: Document Number: VSKTA — Rev: 2.0
			Date: — Sheet 44 of 57

Charger controller (40.1), Support component (40.2)

for reverse input protection

PQ209 SSM3K7002FU_SC70-3
PR225 1M_0402_5%
PR226 3M_0402_5%

EMI Part (47.1)

VIN P1 P2 B+
PQ203 TPCA8057-H_PPAK56-8-5
PQ205 SI7716ADN-T1-GE3_POWERPAK8-5
PR211 0.01_1206_1%
EMI@ PL201 1UH_NRS4018T1R0NDGJ_3.2A_30%
PC214 @EMI@ 2200P_0402_25V7K
PC211 10U_0805_25V6K
PC213 10U_0805_25V6K
PQ207 SI7716ADN-T1-GE3_POWERPAK8-5
PC230 2200P_0402_50V7K
PC231 0.1U_0402_25V6
PC234 0.01U_0402_50V7K
PC236 0.1U_0402_25V6
PD230 BAS40CW_SOT323-3
PC237 0.047U_0402_25V7K
PC238 0.1U_0603_25V7K
PC235 0.1U_0402_25V6
PR228 10_1206_1%
PR229 2.2_0603_5%
PD231 RB751V-40_SOD323-2
PR210 0_0603_5%
PQ201 AON7408L
PC239 1U_0603_25V6K
PC205 1U_0603_25V6K
PR234 4.12K_0603_1%
PR235 4.12K_0603_1%
PR233 4.12K_0603_1%
PL202 4.7UH_ETQP3W4R7WFN_5.5A_20%
PR227 0.01_1206_1%
BATT+
PQ202 AON7406L
@EMI@ PR206 47_1206_5%
@EMI@ PC206 680P_0603_50V8J
PC240 0.1U_0402_25V6
PC241 0.1U_0402_25V6
PC222 10U_0805_25V6K
PC223 10U_0805_25V6K
PC242 0.1U_0603_16V7K

EMI Part (47.1)

PU200 BQ24735RGRR_QFN20_3P5X3P5

PAD	VCC	PHASE	HIDRV
BTST	REGN	ACN	LODRV
ACP	GND	CMSRC	SRP
ACDRV	SRN	ACOK	BATDRV
ACDET	IOUT	SDA	SCL
ILIM			

PR236 10_0603_1%
PR237 6.8_0603_5%

+3VL PR239 10K_0402_1%
<40,9> ACIN
+3VALW
PR241 357K_0402_1%
PR242 100K_0402_1%
PC243 0.01U_0402_25V7K
PR244 422K_0402_1%
PR245 66.5K_0402_1%
PC244 0.1U_0402_25V6
PC245 100P_0402_50V8J
@PR246 0_0402_5%
@PC246 0.1U_0402_10V7K
Please locate the RC Near EC chip

EC_SMB_CK1 <37,40,44>
EC_SMB_DA1 <37,40,44>
ADP_I <40,44>

PR247 309K_0402_1%
PR248 10K_0402_1%
PR249 47K_0402_1%
@PC247 0.1U_0402_10V7K
ADP_V <40>
For A51 ADP_V function

Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	

ILIM and external DPM 3.61A

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

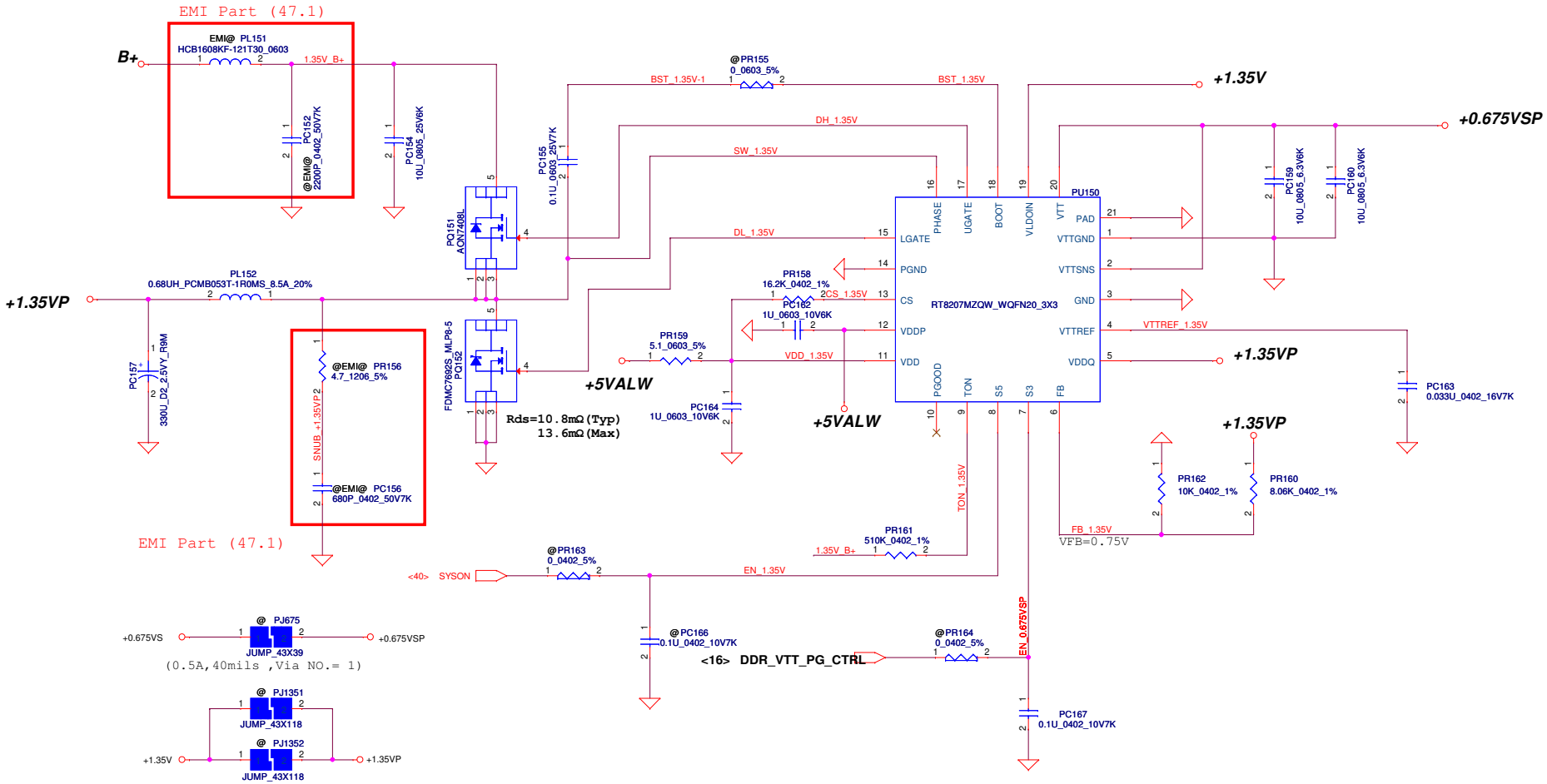
Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: VSKTA | Rev: 2.0

Date: | Sheet 45 of 57

DDR controller (35.3), Support component (35.4)



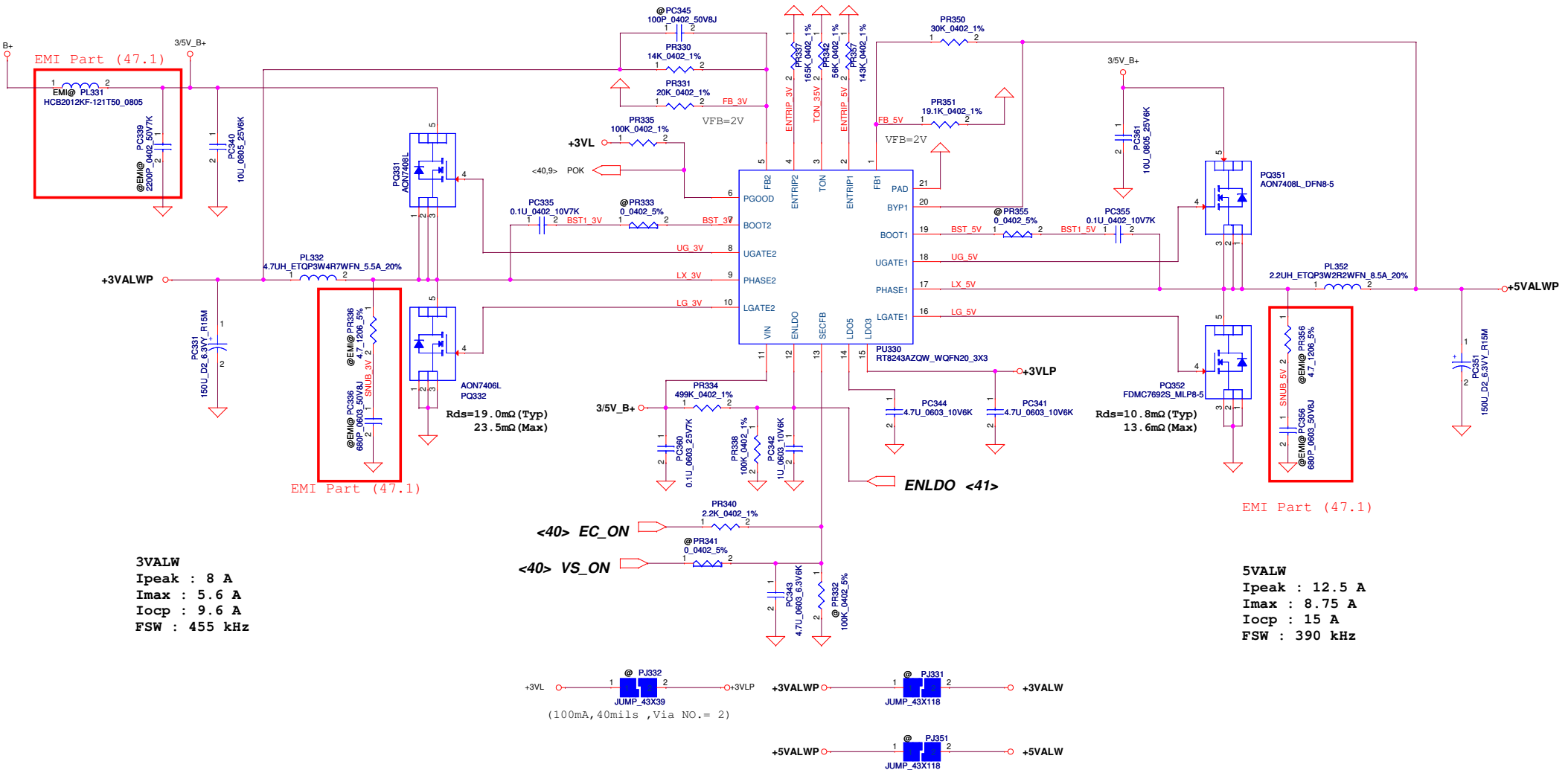
DDR 1.35V
Ipeak : 10 A
Imax : 7A
Iocp : 12 A
FSW : 495 kHz

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

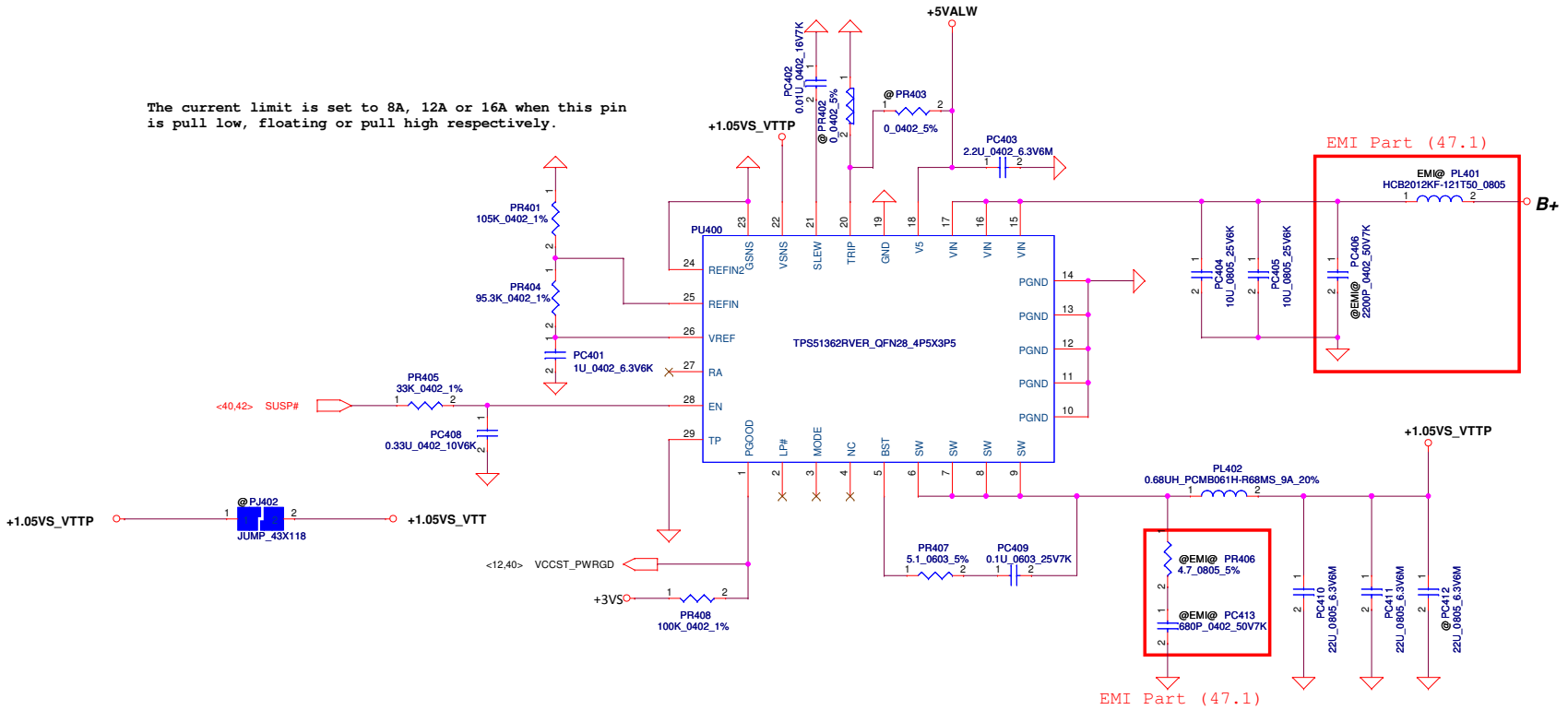
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: 1.35VP/0.675VSP
Size: Custom	Document Number: VSKTA		Rev: 2.0
Date:		Sheet 46 of 57	

3/5VALW controller (35.1), Support component (35.2)

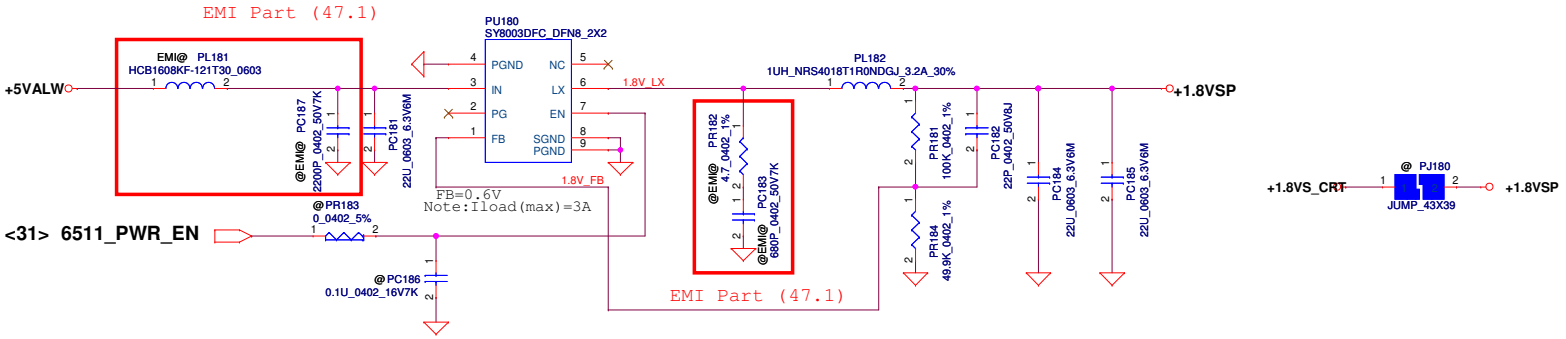


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: 3VALW/5VALW
			Size: Document Number: VSKTA Rev: 2.0
			Date: Sheet 47 of 57

1.05VCCP controller (35.5), Support component (35.6)

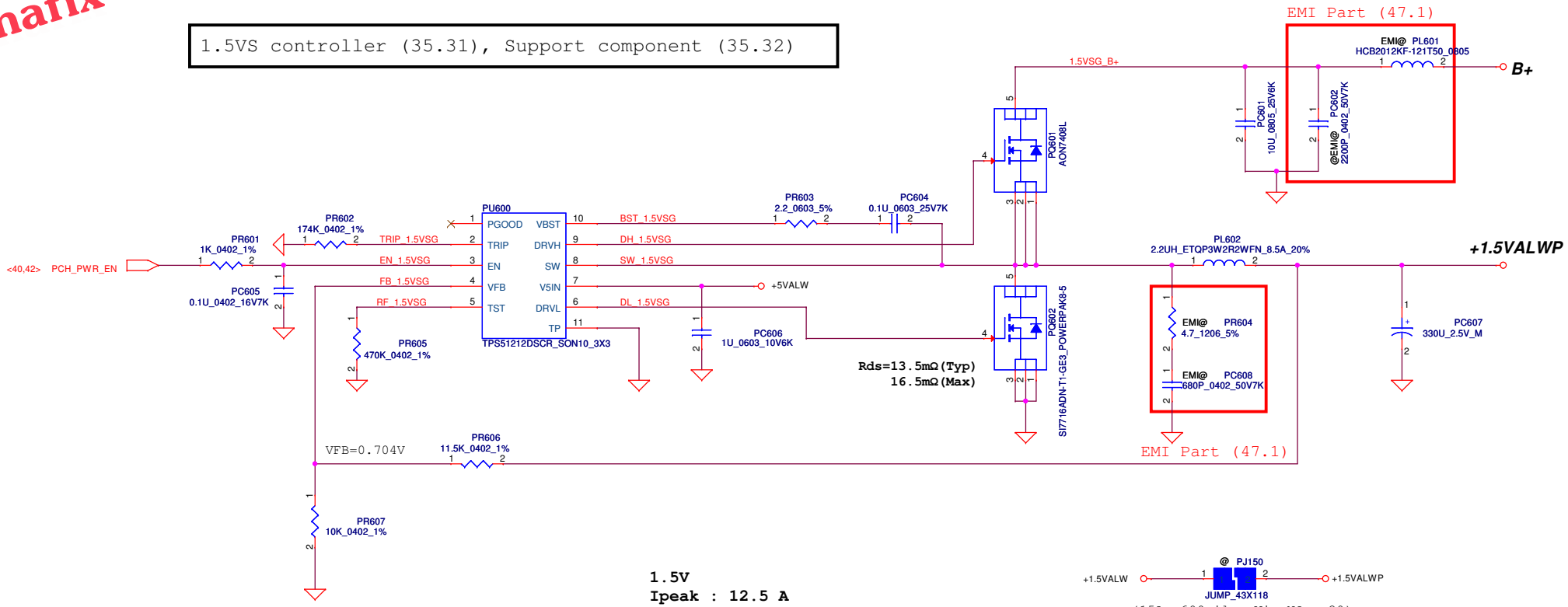


1.8VS controller (35.15), Support component (35.16)



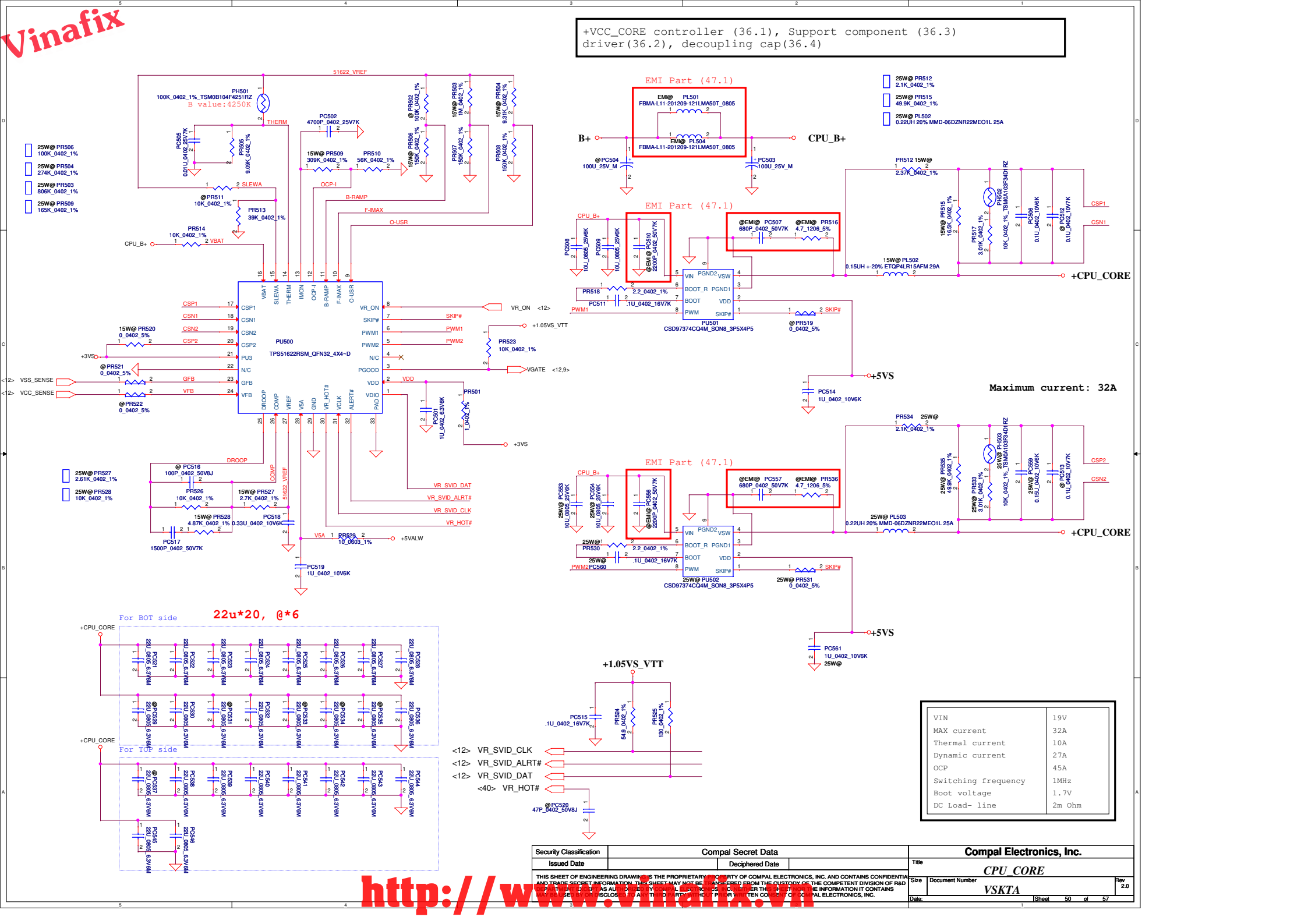
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: +1.05VS_VCCP/1.8VSP
			Size: Document Number: VSKTA Rev: 2.0
			Date: Sheet 48 of 57

1.5VS controller (35.31), Support component (35.32)



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: +1.5VS
			Size: Document Number: VSKTA Rev: 2.0
			Date: Sheet 49 of 57

+VCC_CORE controller (36.1), Support component (36.3)
driver(36.2), decoupling cap(36.4)



VIN	19V
MAX current	32A
Thermal current	10A
Dynamic current	27A
OCP	45A
Switching frequency	1MHz
Boot voltage	1.7V
DC Load- line	2m Ohm

Security Classification	Compal Secret Data	
Issued Date		Deciphered Date

Compal Electronics, Inc.		
Title: CPU_CORE		
Size	Document Number: VSKTA	Rev: 2.0
Date:	Sheet 50 of 57	

+VGA_CORE Under VGA Core

GB4-128 package

PC903 4.7U_0603_6.3V6M
PC904 4.7U_0603_6.3V6M
PC905 4.7U_0603_6.3V6M
PC909 4.7U_0603_6.3V6M
PC907 4.7U_0603_6.3V6M
PC908 4.7U_0603_6.3V6M
PC958 4.7U_0603_6.3V6M
PC911 4.7U_0603_6.3V6M
PC912 4.7U_0603_6.3V6M
PC913 4.7U_0603_6.3V6M
@PC950 4.7U_0603_6.3V6M
PC951 4.7U_0603_6.3V6M
@PC949 4.7U_0603_6.3V6M
@PC902 4.7U_0603_6.3V6M
PC918 0.1U_0402_10V7K
PC919 0.1U_0402_10V7K
PC920 0.1U_0402_10V7K
PC921 0.1U_0402_10V7K

+VGA_CORE Near VGA Core

PC923 22U_0603_6.3V6M
PC924 47U_0805_6.3V6M
PC925 4.7U_0603_6.3V6M
PC926 4.7U_0603_6.3V6M
PC927 4.7U_0603_6.3V6M
PC928 4.7U_0603_6.3V6M
PC929 4.7U_0603_6.3V6M
@PC952 4.7U_0603_6.3V6M
@PC953 4.7U_0603_6.3V6M
@PC955 4.7U_0603_6.3V6M
@PC954 4.7U_0603_6.3V6M
@PC956 4.7U_0603_6.3V6M

VGA_CORE controller (43.1), Support component (43.2)

EMI Part (47.1)

PRV11 = 71.5K ==>Fsw = 450KHz

	N14P-GV2	N14M-GL
R1 PR913	20 Kohm	39 Kohm
R2 PR915	20 Kohm	30 Kohm
R3 PR930	2 Kohm	3 Kohm
R4 PR914	18 Kohm	27 Kohm
C PC940	2.7 nF	1.8 nF

GL@ PR913 39K_0402_1%
GL@ PR915 30K_0402_1%
GL@ PR930 3K_0402_1%
GL@ PR914 27K_0402_1%
GL@ PC940 1800P_0402_50V7K

NCP81172MNTWG_QFN24_4X4

PU900

PQ901 AON7518
PQ902 TPCA8059
PQ903 AON7518
PQ904 TPCA8059

PL903 0.22UH_MMD-06DZNR22MEO1L_25A_20%
PL904 0.22UH_MMD-06DZNR22MEO1L_25A_20%

7x7

Rds=3.8mΩ (Typ)
4.8mΩ (Max)

+VGA_CORE

+VGA_B+

B+

EMI@ PL901 SUPPRE_FBMA-L11-453215-800LMA90T_1812

Compal Electronics, Inc.

Title: VGA_CORE

Size | Document Number: VSKTA | Rev: 2.0

Date: | Sheet 51 of 57

PWR PIR (Product Improve Record)

VSKTA LA-9865P Schematic Change List

Item	Time (When)	Page (Where)	Location / Discription (How / What)	Request (Who)	Reson (Why)
1	EVT--2012/11/28		Add / PC101, PC103, PC102, PC104, PC7, PC8, PL151, PC181, PL2, PC3, PL101, PL102, PL331, PL401, PL601, PL501, PL901	EMI	EMI request
2	EVT--2012/11/28	P50-PWR-CPU_CORE	Value change / PR529, PR520, PR528, PR503, PR507, PR515, PR527, PR509, PR510, PR504, PC516, PL502, PC543, PC544, PC545, PC546, PC514, PC519	PWR	TPS51622 for 15W CPU setting
3	EVT--2012/11/28	P48-PWR-1.05VS_VCCP/1.8VSP	Value change / PR407, PR401, PR404, PR405, PC404, PC405	PWR	For TPS51362 design change
4	EVT--2012/11/28	P46-PWR-1.35VP/0.675VSP	Short pad reserve / PR163	PWR	
5	EVT--2012/11/28	P47-PWR-3VALW/5VALW	PC351 reserve / PC352 mount	PWR	ME limitation
6	EVT--2012/11/28	P50-PWR-CPU_CORE	PC504 reserve	PWR	ME limitation
7	EVT--2012/11/28	P44-PWR-BATTERY CONN / OTP	PF2 change vendor	PWR	for common design change
8	EVT--2012/11/29	P46-PWR-1.35VP/0.675VSP	change material / PL152	PWR	for common design change
9	DVT-2012/12/13	P43-PWR-DCIN	modify PBJ101 footprint	PWR	for common design change
10	DVT-2012/12/13	P44-PWR-BATTERY CONN / OTP	modify PR20, PR21 pin define	PWR	for layout module request
11	DVT-2012/12/13	P46-PWR-1.35VP/0.675VSP	change PR160 to 8.06K	PWR	for output voltage level
12	DVT-2012/12/13	P46-PWR-1.35VP/0.675VSP	modify PL152, PC155, PR164 pin define	PWR	for layout module request
13	DVT-2012/12/13	P47-PWR-3VALW/5VALW	del PC331, PC351	PWR	ME limitation
14	DVT-2012/12/13	P47-PWR-3VALW/5VALW	modify PL332, PR337, PR342, PR357 pin define	PWR	for layout module request
15	DVT-2012/12/13	P47-PWR-3VALW/5VALW	modify the VS_ON direction	PWR	input signal
16	DVT-2012/12/13	P48-PWR-1.05VS_VCCP/1.8VSP	change the 1.8VSP EN to 6511_PWR_EN	PWR	for High enable
17	DVT-2012/12/13	P48-PWR-1.05VS_VCCP/1.8VSP	modify PR401, PC402, PR182 pin define	PWR	for layout module request
18	DVT-2012/12/13	P49-PWR-1.5VALWP	change PR603 to 0ohm	PWR	VBST resistor
19	DVT-2012/12/13	P49-PWR-1.5VALWP	modify PR602, PR606, PL601 pin define	PWR	for layout module request
20	DVT-2012/12/13	P50-PWR-CPU_CORE	change the B+ EMI bead	PWR	ME limitation
21	DVT-2012/12/13	P50-PWR-CPU_CORE	modify PC516, PR526, PR527, PC517, PR529, PR512, PR516, PR518, PR534, PR536, PR530, PR524 pin define	PWR	for layout module request
22	DVT-2012/12/13	P51-PWR-VGA_CORE	PR912/add 10K ohm	PWR	pull high +3VS_DGPU
23	DVT-2012/12/13	P51-PWR-VGA_CORE	PC934 change to 0.01u	PWR	VREF pull down cap
24	DVT-2012/12/13	P51-PWR-VGA_CORE	modify PL901, PR908, PR907, PR901, PR923, PR924, PR927, PC946, PR913, PR915, PR914, PR904, PR928, PR931, PR932, PR909 pin define	PWR	for layout module request
25	PVT-2013/01/25	P47-PWR-3VALW/5VALW	change PC332,PC352,PR409 location to PC331,PC351,PR335	PWR	for common design change
26	PVT-2013/01/25	P46-PWR-1.35VP/0.675VSP	change PL152 value from 1uH to 0.68uH	PWR	for common design change
27	PVT-2013/01/25	P46-PWR-1.35VP/0.675VSP	change PC157 to 390uF 5*5.7	PWR	layout request
28	PVT-2013/01/25	P51-PWR-VGA_CORE	change PC934 part number	PWR	for common design change
29	PVT-2013/02/04	P50-PWR-CPU_CORE	PC529,531,533,534,535,537 reserve PC505 0.1uF change to 10nF PR527 4.99k change to 2.7k PR509 374k change to 309k PC506 0.15u change to 0.1u PR510 39k change to 56k	PWR	for TPS51622 date code 2BI design change
30	PVT-2013/02/04	P51-PWR-VGA_CORE	PC947 330u reserve	PWR	for common design change
31	PVT-2013/02/04	P51-PWR-VGA_CORE	PL903,904 change PN	PWR	for common design change
32	PVT-2013/02/04	P49-PWR-1.5VALWP	net name change from 1.5VALW_EN to PCH_PWR_EN	HW	for common design change
33	PVT-2013/02/07	P49-PWR-1.5VALWP	PR604 PC608 mount PR603 change from 0ohm to 2.2ohm	EMI	EMI request
34	PVT-2013/02/07	P49-PWR-1.5VALWP	PL602 change from 4.7u to 2.2u	PWR	For design change
35	PVT-2013/02/07	P48-PWR-1.05VS_VCCP/1.8VSP	PL402 change PN from RX00 (H1.8) to 5K80 (H3.0)	PWR	change Material for useful height
36	PreMP-2013/03/18	P46-PWR-1.35VP/0.675VSP	PC157 footprint change to C_D2	PWR	
37	PreMP-2013/03/18	P46-PWR-1.35VP/0.675VSP	PR155 0 ohm resistor change to short pad	EMI	EMI request
38	PreMP-2013/03/18	P47-PWR-3VALW/5VALW	PR333,PR355 0 ohm resistor change to short pad	EMI	EMI request
39	PreMP-2013/03/18	P46-PWR-1.35VP/0.675VSP	PR164 0 ohm resistor change to short pad	HW	HW requset
40	PreMP-2013/03/26	P49-PWR-1.5VALWP	PR602 change to 174kohm	PWR	adjust OCP setting
41	PreMP-2013/03/26	P51-PWR-VGA_CORE	PR914 change to 27kohm PR904,PC945,PR918,PR928 Remove	PWR	Remove Richteck colay solution
42	PreMP-2013/03/26	P48-PWR-1.05VS_VCCP/1.8VSP	PL401 change PN	PWR	for common design change
43	PreMP-2013/03/26	P49-PWR-1.5VALWP	PL601 change PN	PWR	for common design change

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: PIR (PWR)
			Size: Document Number: VSKTA — Rev: 2.0
			Date: Friday, June 21, 2013 — Sheet 52 of 57

HW PIR (Product Improve Record)

VSKTA LA-9865P Schematic Change List

REVISION: 0.1 to 0.2

Item	Date	Page	Solution	Request
1.	12/05	P37	Update CHG_CB1,0 level shifter (QR1) circuit	For USB S & C level shifter circuit
2.	12/05	P37	U5.1 (CHG_PWR_GATE#) was connected to the EC(GPIO49) Pin82	For USB S & C
3.	12/05	P40	Add pull high RB12 to +3VL on CHG_PWR_GATE#	For USB S & C
4.	12/05	P32	Add R66,R67 22ohm for CRT undershoot issue	For CRT VSYNC and HSYNC
5.	12/05	P18	Rotate DV1	For GC6
6.	12/05	P18	FB_CLAMP_MON be pulled up to +3VS_DGPU on RPV12.6	For GC6
7.	12/05	P22	Change UV2 from SA007320120 to SA007320300	For GC6
8.	12/05	P40	Change PM_SLP_S4# from UB1.127 to UB1.84	For EC GPIO setting
9.	12/05	P40	Change USB_EN#0 from UB1.84 to UB1.23.	For EC GPIO setting
10.	12/05	P40	Change FB_CLAMP from UB1.23 to UB1.127.	For EC GPIO setting
11.	12/06	P18	Change CV9,CV10,CV11,CV12,CV13,LV1 to OPT@	For DIS BOM config.
12.	12/06	P18	Change RV8 from OPT@ to DGCLK@	For DIS GCLK config.
13.	12/06	P18,34	Change 27M_R to VGA_X1	For VGA CLK
14.	12/06	P34	Change 27M to VGA_X1_R	For VGA CLK
15.	12/06	P31	Change RT128, RT130 to 0 ohm short pad.	For DP to CRT circuit
16.	12/06	P31	Change RT129, RT123 from CRT@ to @.	For DP to CRT circuit
17.	12/06	P31	Change RT140,RT141,RT138 to RP6 (75 ohm row resistor).	For DP to CRT circuit
18.	12/06	P31	Change RT121,RT126,RT143,RT144 to RP7 (4.7K ohm row resistor).	For DP to CRT circuit
19.	12/07	P09	Change RH17 from IEDP@ to LVDS@	For LVDS panel backlight control
20.	12/07	P09	Change RH18 from LVDS@ to IEDP@	For LVDS panel backlight control
21.	12/07	P29	Change R23,R24 from @ to mount	For SMBUS control by EC
22.	12/07	P29	Change R25,R26 from mount to @	For SMBUS control by EC
23.	12/07	P30	Change L64,L65,L66,L67 from SM070001S00 to SM070001R00.	For HDMI choke
24.	12/10	P08	Change UH3,UH4 from 45@ to always mount.	For DVT build
25.	12/10	P10	Change R274,R272 from mount to @	For touch pad function
26.	12/10	P29	Change UY3,CY26 from EHDMI@ to 8201@	For touch pad function
27.	12/11	P29	Delete RT125,RT127	For DP to CRT ISP programming data pin
28.	12/12	P38	Change CA51,CA52 from 2.2uF to 4.7uF	Follow Codec ALC269 common design
29.	12/13	P32	Delete R464,R465,R466	For CRT impedance matching resistors
30.	12/13	P30	Mirror vertically for L64,L65,L66,L67	For HDMI choke layout
31.	12/13	P27	Swap RP5 net name	For EDP row resistor layout
32.	12/17	P31	Swap RP6,RP7 net name	For DP to CRT row resistor layout
33.	12/18	P08	Delete UH4,RH96,RH97,RH92,RH93,RH94,CH10	Remove SPI ROM for Win8 (2MByte) circuit
34.	12/18	P08	Change UH3 from SA00003K820 to SA00006MK00	Change SPI ROM to 8MByte
35.	12/18	P08,40	Change EC_CS1# to EC_CS0#	For 8MB SPI ROM
36.	12/18	P08	Delete PCH_SPICS1#	For use 8MB SPI ROM
37.	12/18	P08	Change UH3.1 from PCH_SPICS1# to PCH_SPICS0#	For use 8MB SPI ROM
38.	12/20	P27	CT9 change to 10UF (the same as CT4)	For use 8MB SPI ROM
39.	12/20	P27	Delete LT3 and +SWR_LX then short +SWR_V12 to UT2.12	For LVDS Translator
40.	12/20	P27	Delete EC_SMB_CK3 and EC_SMB_DA3	For LVDS Translator
41.	12/20	P27	UT2 change to RTD2132R	For LVDS Translator
42.	12/20	P27	UT2 change 2132S@ to LVDS@	For LVDS Translator
43.	12/20	P27	Change UT2.15 from TL_ENVDD to +LCD_VDD	For LVDS panel control
44.	12/20	P27,28	Delete TL_ENVDD	For LVDS panel control
45.	12/20	P27	Delete RT106	For LVDS
46.	12/20	P28	Delete R429	For LVDS
47.	12/20	P27	Change RT4,RT7 from 2132S@ to @	For LVDS
48.	12/20	P27	Change RT6,RT12 from 2132R@ to LVDS@	For LVDS
49.	12/20	P28	Change U18,C475,R426,R430 from 2132S@ to IEDP@	For LCD power circuit
50.	12/20	P28	Delete C475,U18,R430,R426 IEDP symbol	For LCD power circuit
51.	12/20	P29	Change UY3 symbol from SA00005CW00 to SA00005CW10	For HDMI re-driver

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/10/19	Deciphered Date	2015/10/19
Title	HW-PIR-1		
Size	Document Number		Rev
Custom			2.0
Date: Friday, June 21, 2013	Sheet 53 of 57		

HW PIR (Product Improve Record)

VSKTA LA-9865P Schematic Change List

REVISION: 0.1 to 0.2

Item	Date	Page	Solution	Request
52.	12/21	P40	Change CB4,CB5,CB9 to @	For part count reduce
53.	12/21	P40	Delete CB6,CB7	For part count reduce
54.	12/21	P29	Change R23,R24 from mount to EHDMI@	For EHDMI SMBUS
55.	12/21	P40	Delete RB7, RB11	For LVDS Translator
56.	12/21	P40	Delete TRANS_SEL, EC_SMB_CK3,EC_SMB,DA3	For LVDS Translator
57.	12/21	P40	Add a 0ohm resistor on UB1.81 and unmount, then connect to PCIE_WAKE#	For PCIE wake
58.	12/21	P09	U1.AJ5 change to PCIE_WAKE#_R	For PCIE wake
59.	12/21	P09	Add a 0ohm resistor then connect to PCIE_WAKE#_R and PCIE_WAKE#	For PCIE wake
60.	12/21	P09	Change RH1711.1 connect to PCIE_WAKE#_R	For PCIE wake
61.	12/24	P13	Change C22,C23,C24,C32,C61 from 100uF_1206 to 22u_0805	For PCH power
62.	12/24	P13	Add C35,C39,C60 close to CPU	For ESD request
63.	12/24	P05	Change CH11 from unmount to mount	For ESD request
64.	12/24	P40	Change CB13 from 180pF to 100pF	For ESD request
65.	12/24	P37	Change C530,C532 package size from 1206 to 0805	For no use 1206 package size
66.	12/24	P08	Change RH61,RH68,RH69,RH72,RH65,RH67,RH74,RH78 from 33ohm to 15ohm	For SPI ROM
67.	12/24	P38	Add CA61 (220pF) between INT_MIC_CLK and GND	For EMI request
68.	12/24	P12	Add CC53 (47uF) and co-layout with C18	For +1.35V power rail
69.	12/24	P12	Change C18 from mount to @	For +1.35V power rail
70.	12/26	P07	Delete CH2,CH3,YH1,RH2 and add test point T138 for PCH_RTCX2	Delete Crystal circuit
71.	12/26	P18	Change DV1 from SCS00000Z00 to SCS00002G00	BOM reduction
72.	12/27	P31	Change RT128,RT130 to @	For CRT
73.	12/27	P27	Change CT13 and RT113 to LVDS@	For LVDS
74.	12/27	P22	Change RV43 from 330K ohm to 270K ohm	For GC6 timing requirements
75.	12/27	P22	Change RV53 from 100K ohm to 10K ohm	For GC6 timing requirements
76.	12/27	P22	Change RV54 from 47K ohm to 33K ohm	For GC6 timing requirements
77.	12/27	P22	Change RV50 from unmount to N14MGL@	N14M-GL doesn't support GC6
78.	12/27	P22	Change UV2 from OPT@ to N14PGV2@	N14M-GL doesn't support GC6
79.	12/27	P22	Change CV58 from OPT@ to unmout	Cost reduction
80.	12/27	P18	Change QV8 from OPT@ to N14PGV2@	N14M-GL doesn't support GC6

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/10/19	Deciphered Date	2015/10/19
Title	HW-PIR-2		
Size	Document Number		Rev
Custom			2.0
Date:	Friday, June 21, 2013	Sheet	54 of 57

HW PIR (Product Improve Record)

VSKTA LA-9865P Schematic Change List

REVISION: 0.2 to 0.3

Item	Date	Page	Solution	Request
1.	01/21	P38,40	Add EC_MUTE_INT	For audio codec
2.	01/21	P31	Update ISPSCL /ISPSDA connection	For CRT
3.	01/30	P18,40	UV1 GPIO12 (GPS_DOWN#) be connected to EC GPXIOA01	For GPS
4.	01/30	P28	Change L61 form TOUCH@EMI@ change to TOUCH_EMI@	For EMI BOM Config
5.	01/30	P32	Change L68,L69,L70,C503,C504,C505,C506,C507,C508 form CRT@EMI@ change to CRT_EMI@	For EMI BOM Config
6.	02/01	P28	Delete R426 and change U18.1 connected to +LCD_VDD	For LVDS
7.	02/01	P28	Delete R427 and change U18.3 connected to LCD_ENVDD	For LVDS
8.	02/01	P40	Change UB1.81 from PCIE_WAKE# to TRANS_SEL, and add pull-high resistor RB26 and reserve RB25 to GND	For LVDS
9.	02/01	P35	PCIE_WAKE# add R4279 and reserve R4283 to LAN_WAKE# to EC	For WAKE function
10.	02/01	P9	Change RH171 from 10Kohm to 1Kohm	For WAKE function
11.	02/01	P9	Delete RH136 and change U1.AJ5 from PCIE_WAKE#_R to WAKE# and connected to R4279.1 and RH171.1	For WAKE function
12.	02/01	P35	Add RC284 between JWLAN.1 to WLAN_WAKE#	For WAKE function
13.	02/01	P28	Add DA8 on INT_MIC_CLK	For ESD's request
14.	02/01	P28	Add DA9 on INT_MIC_DATA	For ESD's request
15.	02/01	P28	Reserve D97 on USB20_P7_R, USB20_N7_R	For ESD's request
16.	02/04	P10	Reserve D98 to GND on H_THERMTRIP#	For ESD's request
17.	02/04	P41	Reserve D99 to GND for ON/OFFBTN#	For ESD's request
18.	02/04	P28	Delete R427 and U18.3 connected to LCD_ENVDD	For LVDS
19.	02/04	P28	Add R4280, R4281 to co-layout L61	For LVDS
20.	02/04	P40	Change RB135,RB136 BOM config from LVDS@ to @	For LVDS
21.	02/08	P29	Change RY33 from 4.99Kohm to 4.3Kohm	For HDMI test
22.	02/08	P42	Change RM4 from 100Kohm to 10Kohm	For WLAN issue
23.	02/08	P38	Change RA41, CA53 from @EMI@ to EMI@	For EMI 216MHz noise (24MHz harmonic).
24.	02/08	P40	Change QB1 from SB000009080 to SB570020020	For EL code
25.	02/21	P28	Change L61 from TOUCH_EMI@ to @TOUCH_EMI@	For EMI touch
25.	02/21	P28	Add R4280,R4281 on USB20_P5/USB20_N5	For EMI touch
26.	02/23	P36	Change RW2 from 0ohm to 33ohm	For EMI's request
27.	02/23	P36	Change CW9 BOM config from @EMI@ to EMI@.	For EMI's request
28.	02/23	P31	Change YT1 from SJ10000DK00 to SJ100009700	For crystal vendor's recommend
29.	02/23	P28,35,37	Change L61,L62,LR5,LR7,LR8 from SM070000K00 to SM070001N00.	For EMI's request
30.	02/23	P30	Change L64,L65,L66,L67 from SM070001R00 to SM070001N00.	For EMI's request
31.	02/23	P37	Change L56,L60,L71,L72 from SM070001U00 to SM070001R00.	For EMI's request
32.	02/23	P38,40	Add EC_MUTE_INT on UA1.48 and connected RB38 to UB1.122	For audio codec
33.	02/23	P9,40	Change UB1.123 from CLK_EC to CLK_EC_R and connected to RB7 and a reserve resistor RB5; and RB5 connected to CLK_EC; and RB7 connected to POK	For CLK_EC and POK
34.	02/27	P31	Change RT118, RT119, RT115, RT116 from @ to CRT@.	For DP to CRT vendor's recommend

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/10/19	Deciphered Date 2015/10/19	Title HW-PIR-3

Size C	Document Number Custom		Rev 2.0
Date: Friday, June 21, 2013	Sheet 55 of 57		

HW PIR (Product Improve Record)

VSKTA LA-9865P Schematic Change List

REVISION: 0.3 to 1.0

Item	Date	Page	Solution	Request
01.	03/04	P27	Add EC_SMB_CK3,EC_SMB_DA3 circuit	For LVDS translator SMBUS
02.	03/04	P28,37	Swap L56,L60,LR7,L71,L72,LR8,L62,L61 for layout	For layout routing
03.	03/04	P31	Change RT123, RT129 from CRT@ to @	For DP to CRT translator
04.	03/05	P40	Change CLK_EC_R to POK_R	For Power's request
05.	03/05	P36	Add RW5,RW6,RW7,RW8 on SD_DATA for EMI request	For CardReader
06.	03/05	P10	RP35 (10K) change to RP9 (2.2K)	For pull-high row resistor
07.	03/05	P41	Change SW2 to @	For Pre-MP BOM
08.	03/05	P36	Change RW1 to short pad	For reduce part count
09.	03/05	P07	Change R163 to short pad	For reduce part count
10.	03/05	P34	Change RC284 to short pad	For reduce part count
11.	03/05	P38	Change RA27,RA28,RA65,RA68 to short pad	For reduce part count
12.	03/05	P07	Change R32 to short pad	For reduce part count
13.	03/07	P08	Add RH79 for PCH_SMBCLK pull high	For SMBUS
14.	03/07	P31	Add RT147 and update YT1 symbol	For DP to CRT translator
15.	03/08	P08	Change RP8 to 10K	For pull-high row resistor
16.	03/11	P36	Modify CardReader circuit	For CardReader
17.	03/11	P41	Change WLAN/WiMAX LED power plane from +5VS to +5VLAW	For WLAN/WiMAX LED
18.	03/11	P36	Change LW1~LW6 to SM010005X00	For EMI part
19.	03/11	P41	Add BOM structure for WLAN LED	For BOM config.
20.	03/13	P36	Change CW7 from 2.2u to 4.7u	For CardReader
21.	03/13	P40	Change LAN_WAKE# from UB1.108 to UB1.71	For WAKE
22.	03/13	P09,35,40	Change WAKE# to EC_SWI# and connect to UB1.108	For WAKE
23.	03/14	P12	Change C18 footprint from C_D2 to C_D2-S	For layout's request
24.	03/14	P05,10,41	Change CH7,D98,D99 BOM config from @ESD@ to ESD@	For ESD's request
25.	03/14	P40	Change CB14 BOM config from @ to ESD@	For ESD's request
26.	03/18	P05,40	Change CH7, CB14 from 180PF to 0.1UF	For ESD's request
27.	03/18	P10,41	Change D98,D99 to CH12, CH13	For ESD's request
28.	03/18	P05	Change CH11 from 180PF to 100PF	For ESD's request
29.	03/18	P40	Change CB13 from 100PF to 0.1UF	For ESD's request
30.	03/18	P33,09,41,07,08,31	Change R27,R65,R471,R472,RH26,RH42,RT114 to 0ohm short-pad resistor	For reduce part count
31.	03/19	P36	Change CW13,CW12,CW11,CW10,CW9 from 10PF to 4.7PF	For EMI request
32.	03/19	P36	Change CW14 from @EMI@ to EMI@	For EMI request
33.	03/19	P40	Add RR8 then connected to CB0_WAKE# and LAN_WAKE#	For LAN_WAKE#
34.	03/19	P40	Change UB1.71 from LAN_WAKE# to CB0_WAKE#	For USB Sleep and Charge
35.	03/19	P40	Add RR9 then connected to CB0_WAKE# and EC_CB0	For USB Sleep and Charge
36.	03/19	P40	UB1.97 connected to EC_CB1	For USB Sleep and Charge
37.	03/19	P37	Change RR2 and RR3 from 0ohm to 0ohm short-pad	For USB Sleep and Charge
38.	03/19	P37	Add RR6 then connected to CHG_CB0 and EC_CB0	For USB Sleep and Charge
39.	03/19	P37	Add RR7 then connected to CHG_CB1 and EC_CB1	For USB Sleep and Charge
40.	03/19	P37	Add RB11 on EC_CB0 then pull-high to +3VALW_PCH	For USB Sleep and Charge
41.	03/19	P37	Add RB13 on EC_CB1 then pull-high to +3VALW_PCH	For USB Sleep and Charge
42.	03/20	P28	Change U50 BOM config from IEDP@ to always mount	For LVDS issue
43.	03/20	P28	Change R436 BOM config from LVDS@ to @	For LVDS issue
44.	03/20	P32	Change C503,C504,C505,C506,C507,C508 BOM config from CRT_EMI@ to CRT@	For CRT BOM ocnfig
45.	03/20	P40,35,13,28	Change RB7,R4279,R210,R4280,R4281,RR9 to 0ohm short pad	For reduce part count
46.	03/20	P40,37	Change RR8,RR2,RR3 to 0 ohm	For option
47.	03/22	P37	Change RR6, RR7 from un-mount to mount	For EC controls USB S & C
48.	03/23	P41	Change MB DA8 P/N from DA8000XK000 to DA8000XK010	For Pre-MP BOM
49.	03/23	P35,37	Change U13,U15 from SA00004KB00 to SA00003TV00	For power switch issue on Rosetta
50.	03/26	P05	Change C74,C76,C77,C80 BOM config to CRT	For CRT BOM config.
51.	03/26	P37	Change RB11,RB13 from un-mount to mount	For EC controls USB S & C
52.	05/09	P37	Add CPU R1 & R3 PN in ISPD sheet	For CPU BOM config.
53.	06/11	P41	Add GPU N14P-GV2 R1 & R3 PN in ISPD sheet	For GPU BOM config.
54.	06/11	P42	Change Q6 PN from SB570020110 to SB00000EN00	For X1 code
55.	06/11	P30	Change Q190,Q191 PN from SB501110010 to SB00000PF00	For main source
56.	06/11	P38	Change RA66 PN from SM01000CY00 to SM01000I000	For X1 code
57.	06/11	P31	Change RT123, RT129 from @ to mount	For DP to CRT translator (vendor's recommand)
58.	06/11	P08	Change C2 from 12pF to 22pF	For Pre-MP issue
59.	06/11	P08	Change C2 BOM config from NOGCLK@ to mount	For Pre-MP issue
60.	06/11	P08	Change R48,Y2,C3 BOM config from NOGCLK@ to @	For BOM config.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/10/19	Deciphered Date 2015/10/19	Title HW-PIR-4

Size C Custom	Document Number		Rev 2.0
Date: Friday, June 21, 2013	Sheet 56 of 57		

HW PIR (Product Improve Record)

VSKTA LA-9865P Schematic Change List

REVISION: 1.0 to 2.0

Item	Date	Page	Solution	Request
01.	06/20	P31	Change RT117 from CRT@ to always mount	For ZRMAA issue
02.	06/21	P08	Change RH42 from 0ohm short pad to 0ohm and always mount	For HDD lost issue

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/10/19	Deciphered Date	2015/10/19
Title	HW-PIR-5		
Size: C, Custom	Document Number		Rev: 2.0
Date: Friday, June 21, 2013	Sheet 57 of 57		