

1

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Compal Confidential

Schematics Document

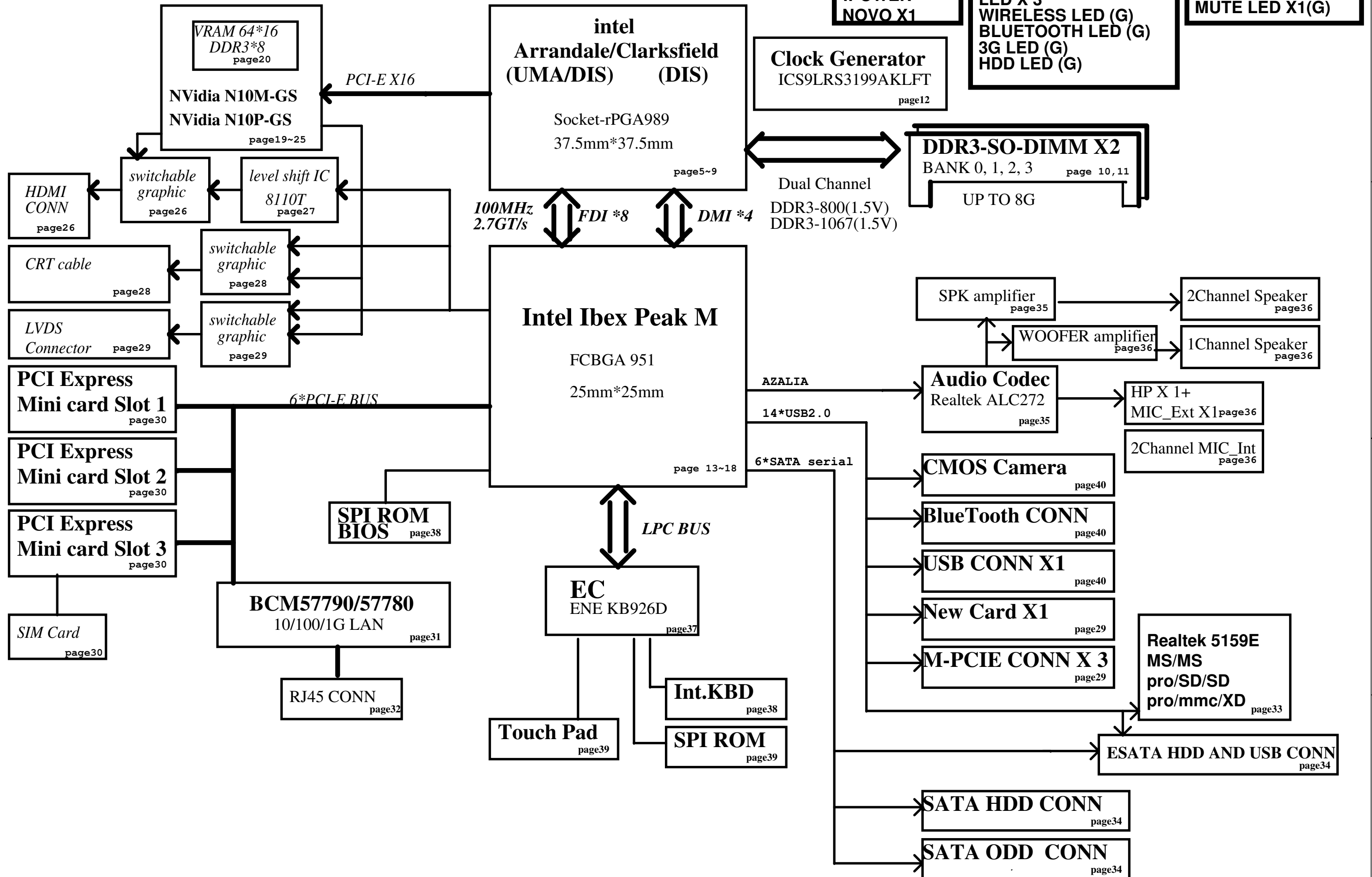
Arrandale/Clarksville

with Intel IBEX PEAK-M core logic

NIWBA

REV: 0.1

Security Classification	Compal Secret Data			Compal Electronics, Ltd.	
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title Cover Sheet	
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				Date: Tuesday, March 24, 2009	Rev 0.1
				Sheet 1 of 52	



Security Classification		Compal Secret Data		 Compal Electronics, Inc. MB Block Diagram Size Custom Document Number NIWBA LA5371P Date: Tuesday, March 24, 2009 1 Sheet 2 of 52 Rev 0.1	
Issued Date	2008/03/24	Deciphered Date	2008/04/		
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DDR3 Voltage Rails

power plane State				+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
	+B	+5VALW +3VALW	+1.5V	
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	RAM M2	BATT	KE926	SODIMM	CLK CHIP	WLAN WWAN	N10x Thermal Sensor	N10x	Cap sensor board	NEW CARD	PCH
SMB_EC_CK1	KB926	X	V	X	X	X	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW									
SMB_EC_CK2	KB926	X	X	X	X	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW											+3VALW
SMBCLK	PCH	V	X	X	V	V	X	X	X	X	V	X
SMBDATA	+3VALW	+3VALW			+3VS	+3VS					+3VS	
SML0CLK	PCH	X	X	X	X	X	X	X	X	X	X	X
SML0DATA	+3VALW											
SML1CLK	PCH	X	X	V	X	X	X	V	X	V	X	X
SML1DATA	+3VALW			+3VALW				+3VS		+3VS		

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

@ FUNCTION

EVT		NON-USE	
45@	(45 BOM)		
GIGA@	(GIGA LAN)	100@	(100 LAN)
NO TVSW@	(NON TV POWER SW)	TVSW@	(TV POWER SW)
ARRAY@	(ARRAY MIC)	MONO@	(MONO MIC)
S512@	FOR X76 BOM		
H512@	FOR X76 BOM		
S1024@	FOR X76 BOM		
H1024@	FOR X76 BOM		
X76@	(X76 BOM)		
M1@	(DDR M1 MODE)		
3G@	(3G MODE)		
10M@	FOR 10M CHIP		
10P@	FOR 10P CHIP		
UMA@	FOR Auberndale		
DIS@	FOR Auberndale/Clarksfield		
VGA@	FOR NVIDIA PART		

PCIE PORT LIST

PORT	DEVICE
1	NEW CARD
2	WLAN
3	LAN
4	3G
5	
6	TV TUNNER
7	
8	

USB PORT LIST

PORT	DEVICE
0	LEFT SIDE
1	RIGHT SIDE
2	CMOS
3	
4	RIGHT SIDE
5	CARD READER
6	
7	
8	WIRELESS
9	TV TUNNER
10	NEW CARD
11	BT
12	
13	3G

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VGA and DDR3 Voltage Rails (N10x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	GPU VID2
GPIO8	I/O	L	Thermal Catastrophic Overtemp
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT		Memory VREF switch
GPIO11	I/O	L	SLI raster sync
GPIO12	IN	-	AC power detect pin
GPIO13	OUT	-	MEM_VID orPower supply control
GPIO14	OUT	-	Power supply control
GPIO15	IN	-	Hot plug detect for IFP Link E
GPIO16	OUT	-	Programmable Fan Control
GPIO17	IN	-	
GPIO18	IN	-	
GPIO19	IN	-	Hot plug detect for IFP Link D
GPIO20	IN	-	
GPIO21	IN	-	Hot plug detect for IFP link F
GPIO22	IN	-	SLI swap ready signal
GPIO23	I/O		

GPIO6	GPIO5	N10M-GS	N10P-GS
GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.8V	12
0	1	0.85V	12
1	1	0.9V	0, 10

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

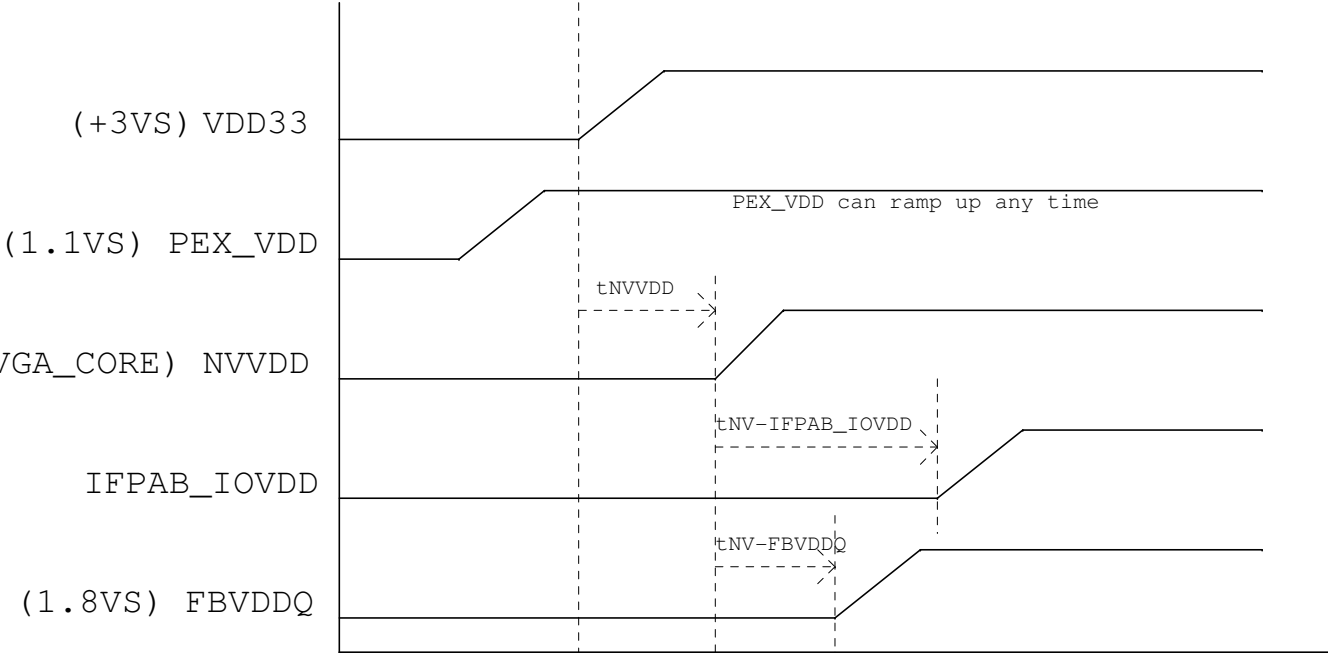
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK (MHz)	NVVDD			FBVDD (1.5V)		FBVDDQ (GPU+Mem) (1.5V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)		(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N10P-GS 128bit 1024MB DDR3	21.07	6.67	TBD	TBD	18.25	17.34	2.06	3.09	4.09	6.14	850	0.89	75	0.14	63	0.07	55	0.18
N10P-GE 128bit 1024MB DDR3	20.97	6.73	TBD	TBD	19.17	17.25	2.03	3.05	4.09	6.14	840	0.88	75	0.14	63	0.07	55	0.18
N10P-LP 128bit 1024MB DDR3	15.48	6.44	TBD	TBD	13.95	11.86	1.90	2.85	3.99	5.99	810	0.85	75	0.14	63	0.07	55	0.18

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

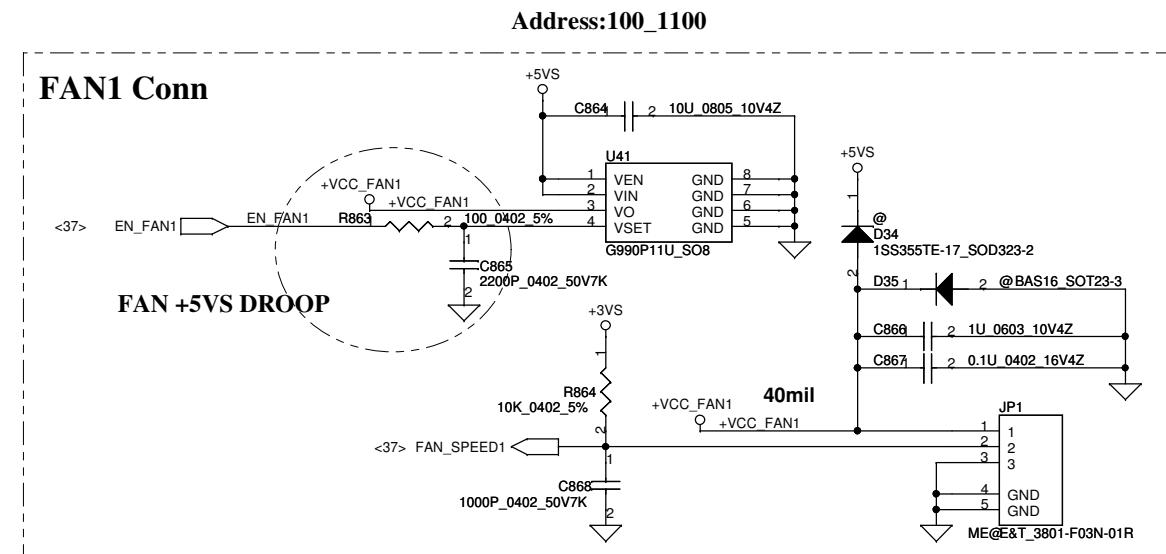
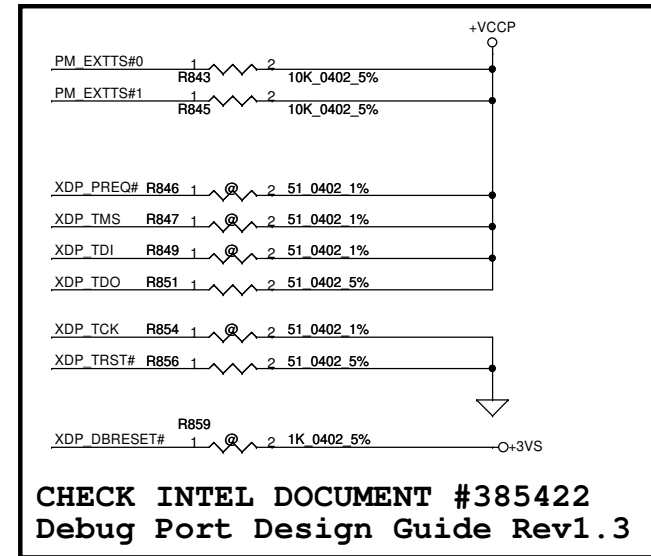
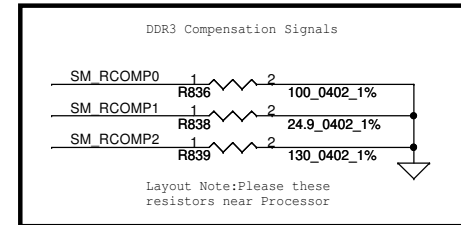
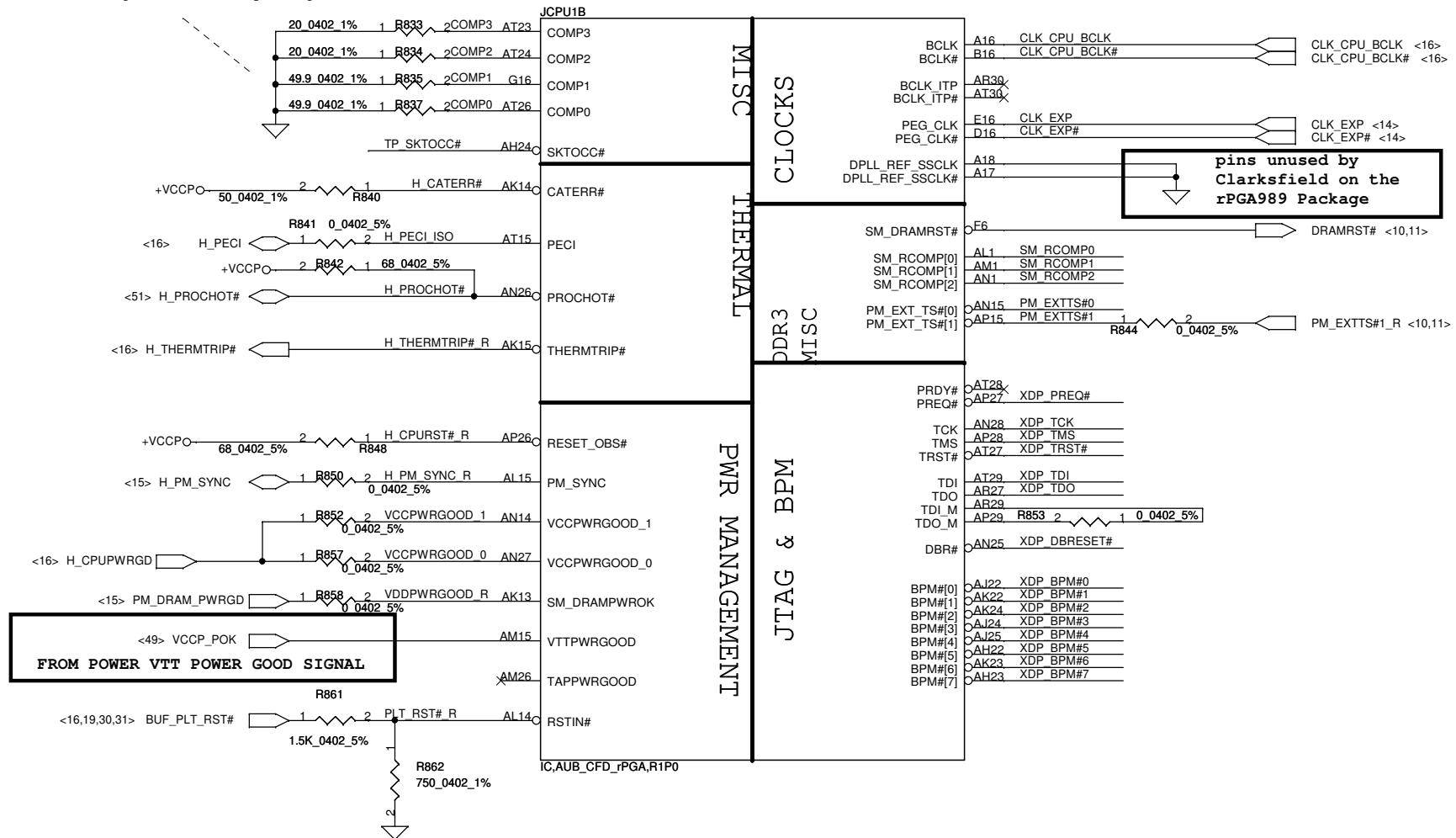
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK (MHz)	NVVDD			FBVDD (1.5V)		FBVDDQ (GPU+Mem) (1.5V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)		(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N10M-GE 64bit 512MB DDR3	13.36	2.93	TBD	TBD	11.89	10.70	0.66	0.99	2.16	3.24	792	0.83	75	0.14	63	0.07	100	0.33
N10M-GS 64bit 512MB DDR3	14.29	3.10	TBD	TBD	11.53	11.53	0.70	1.05	2.28	3.42	817	0.86	75	0.14	63	0.07	100	0.33
N10M-LP 64bit 512MB DDR3	8.28	2.91	TBD	TBD	6.60	5.61	0.62	0.93	2.20	3.3	782	0.82	75	0.14	63	0.07	100	0.33

Power Sequence

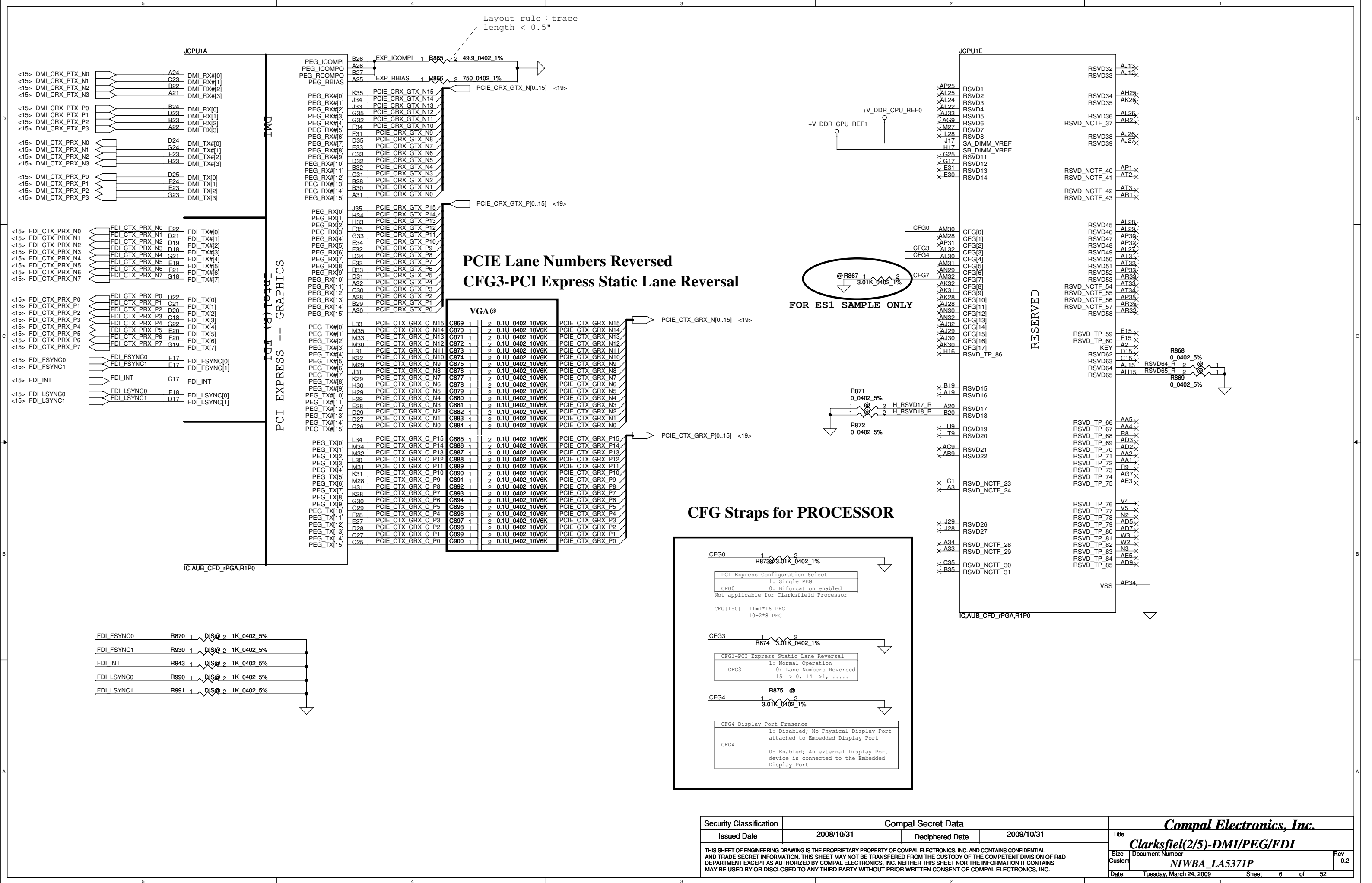
The ramp time for any rail must be more than 40us

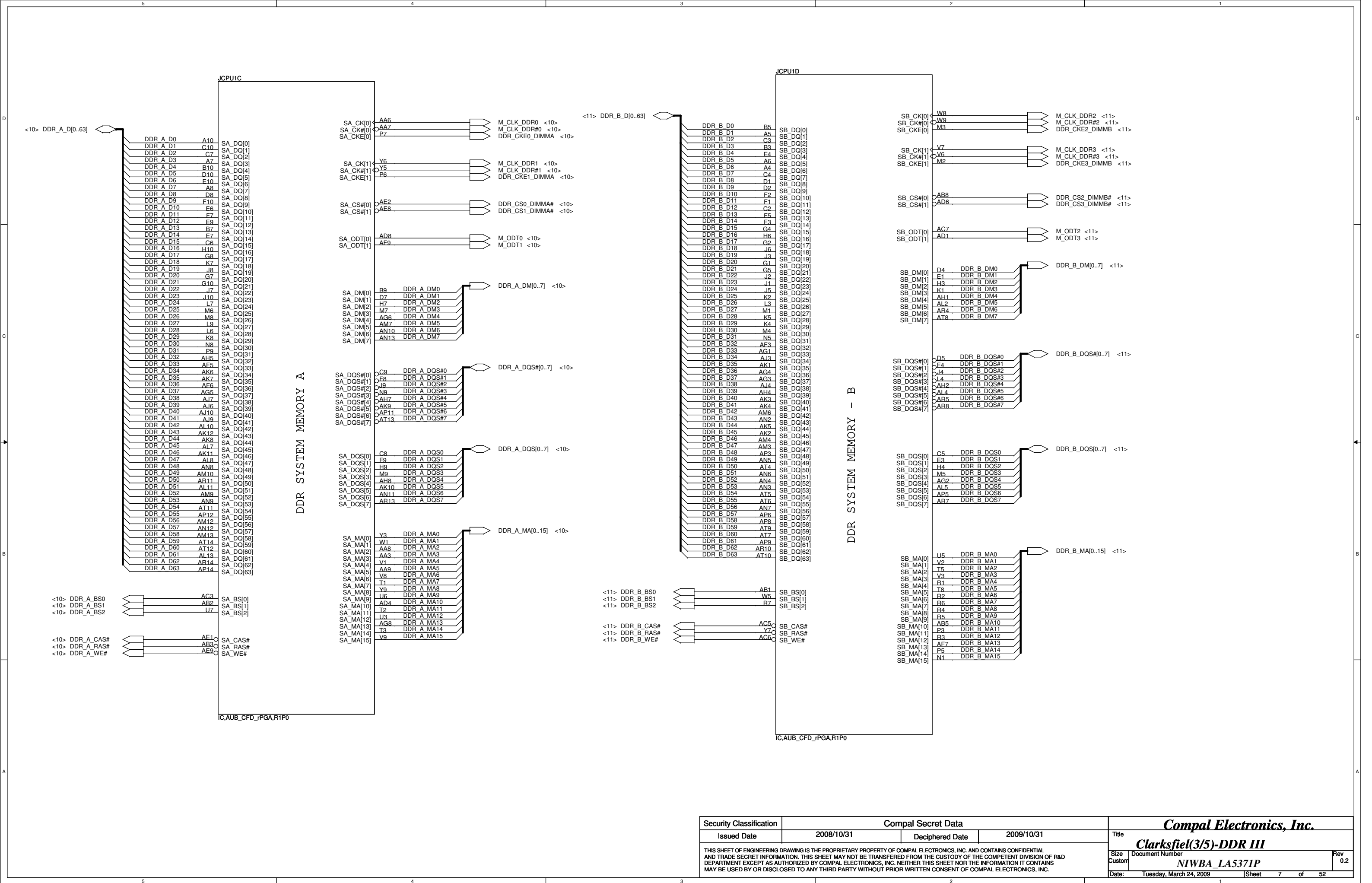


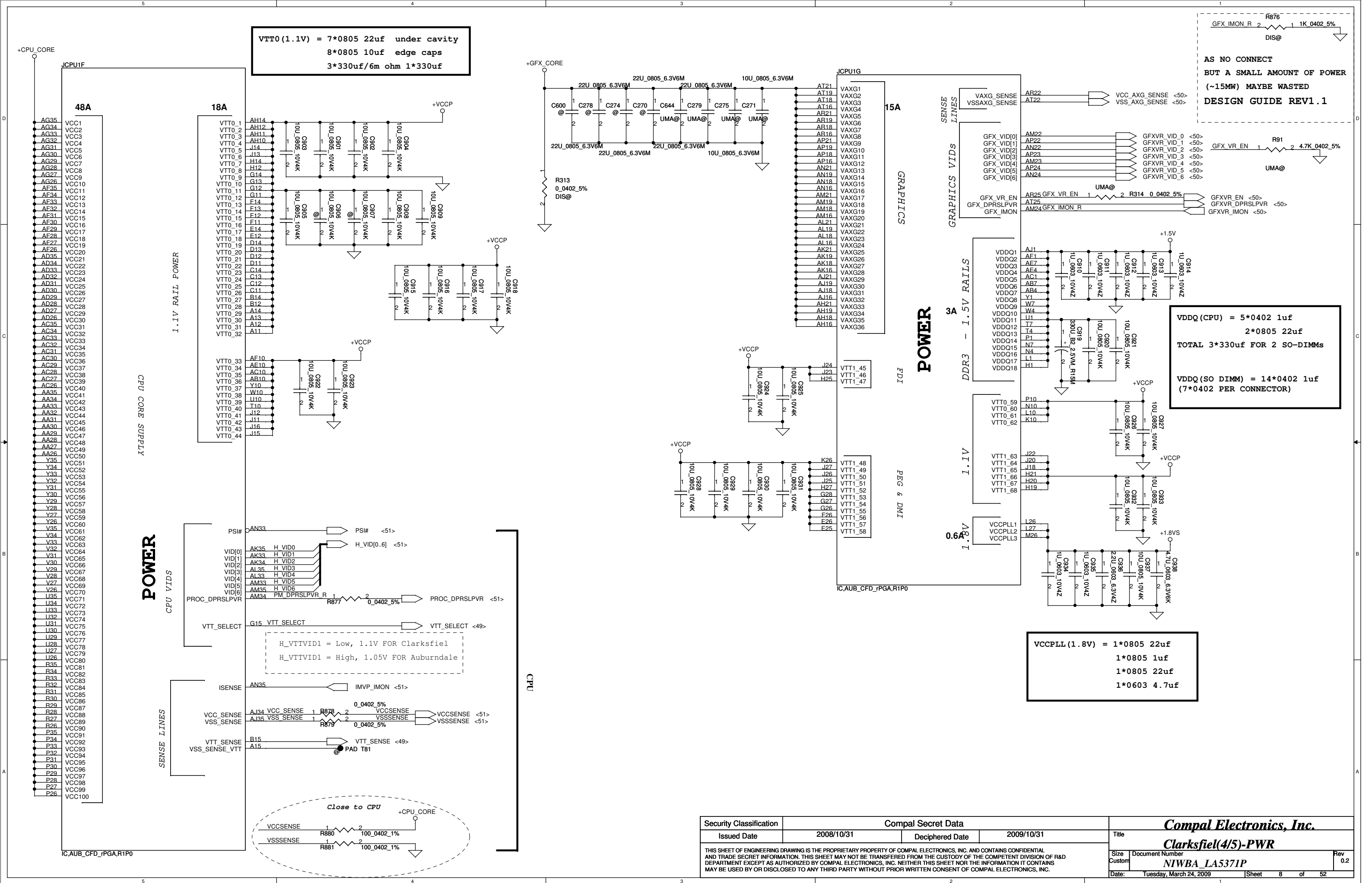
Layout rule : 10mil width trace
length < 0.5", spacing 20mil



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VTT0(1.1V) = 7*0805 22uf under cavity
8*0805 10uf edge caps
3*330uf/6m ohm 1*330uf

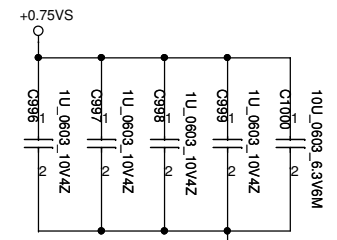
AS NO CONNECT
BUT A SMALL AMOUNT OF POWER
(~15MW) MAYBE WASTED
DESIGN GUIDE REV1.1

VDDQ(CPU) = 5*0402 1uf
2*0805 22uf
TOTAL 3*330uf FOR 2 SO-DIMMs

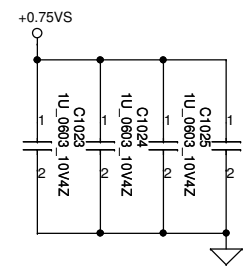
VDDQ(SO DIMM) = 14*0402 1uf
(7*0402 PER CONNECTOR)

VCCPLL(1.8V) = 1*0805 22uf
1*0805 1uf
1*0805 22uf
1*0603 4.7uf

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Size	Document Number	Rev		0.2	
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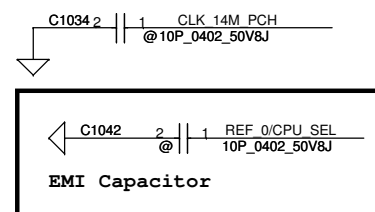
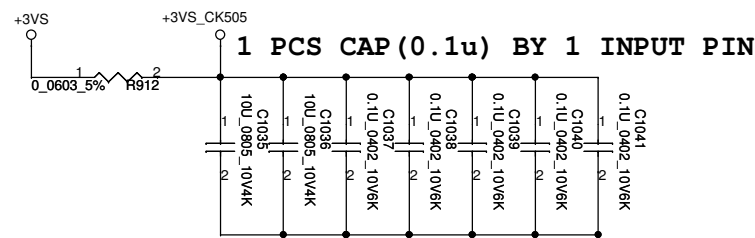
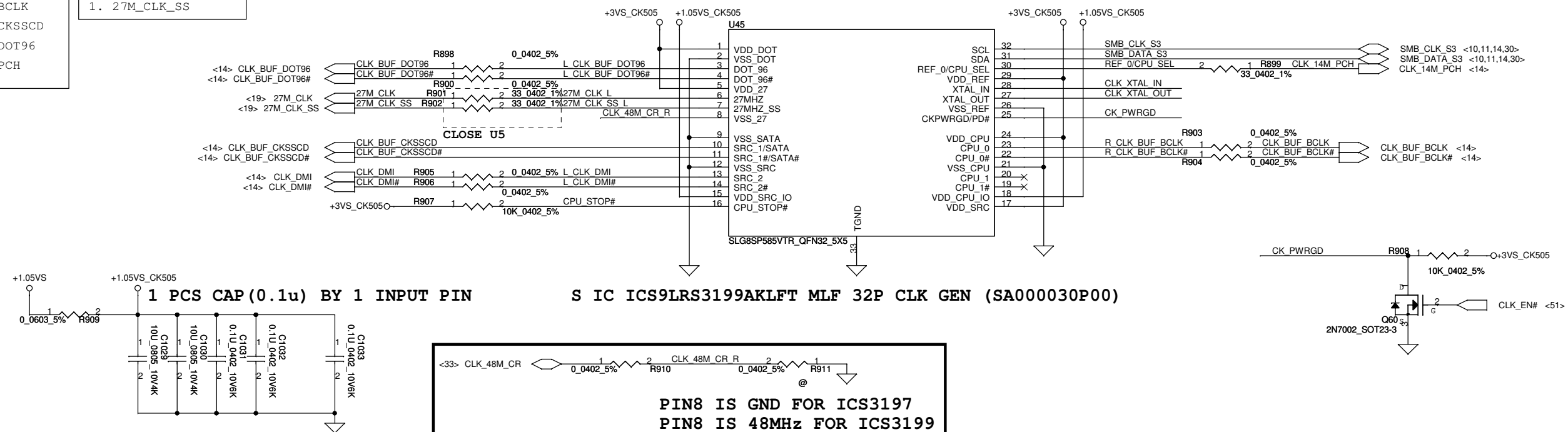
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Issued Date	2008/10/31	Deciphered Date	2009/10/31			
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				Document Number		
				Date:		
				NIWBA LA5371P		
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CLK GEN TO PCH

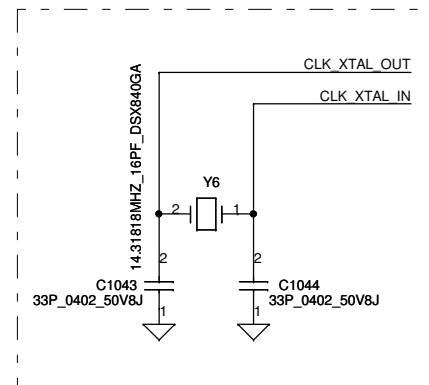
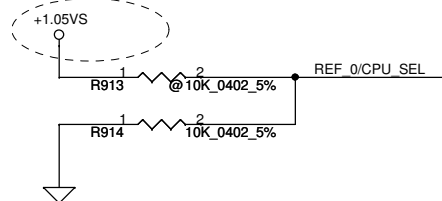
1. CLK_DMI
2. CLK_BUF_BCLK
3. CLK_BUF_CKSSCD
4. CLK_BUF_DOT96
5. CLK_14M_PCH

CLK GEN TO VGA

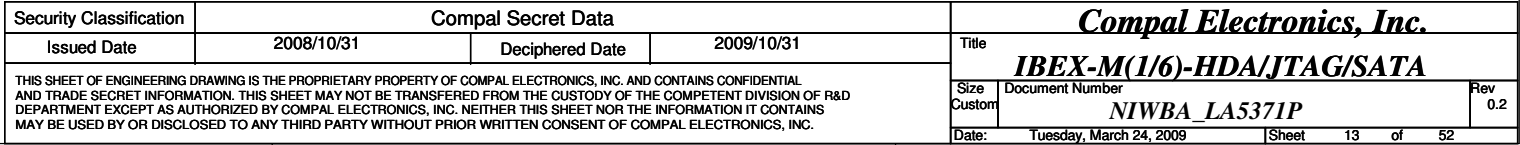
1. 27M_CLK
1. 27M_CLK_SS



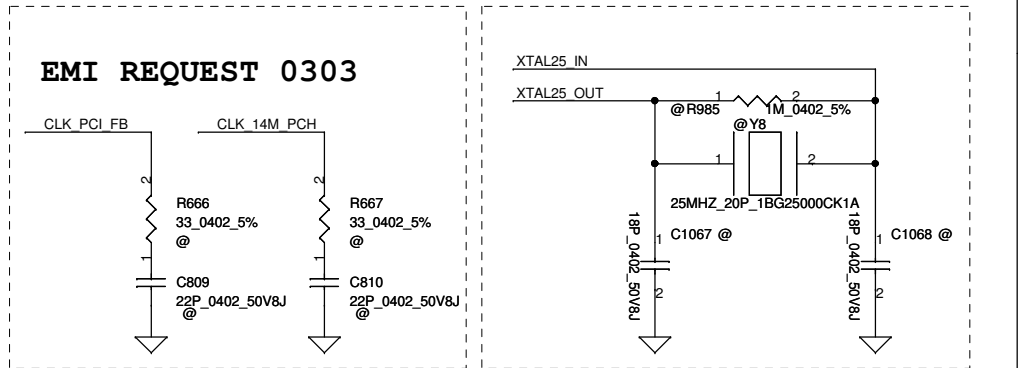
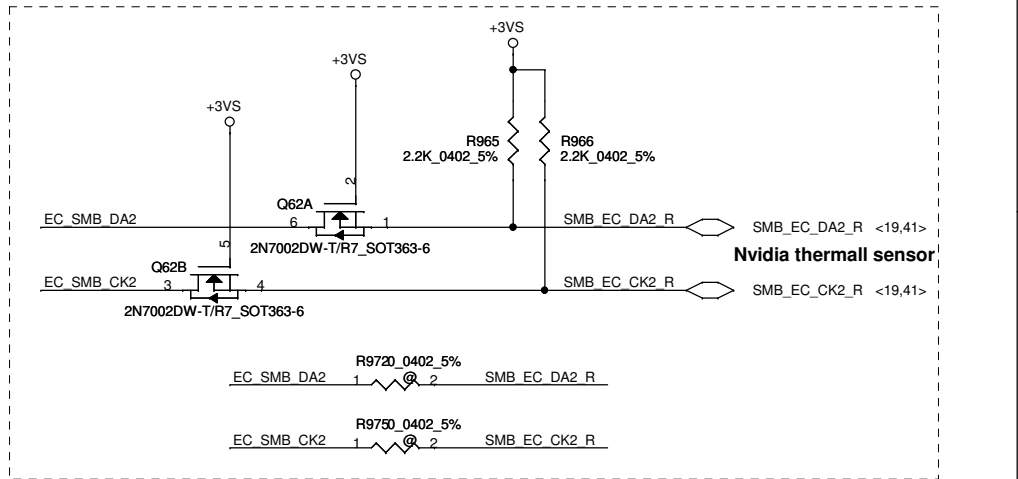
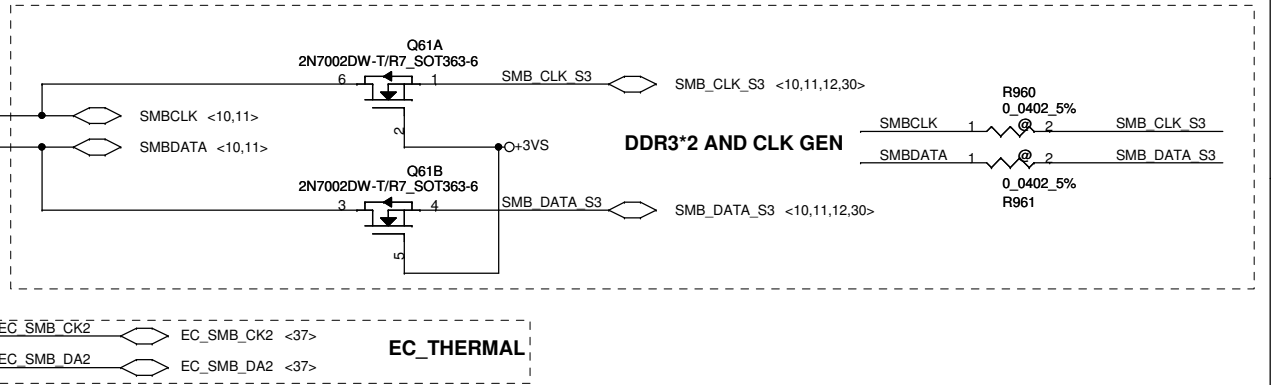
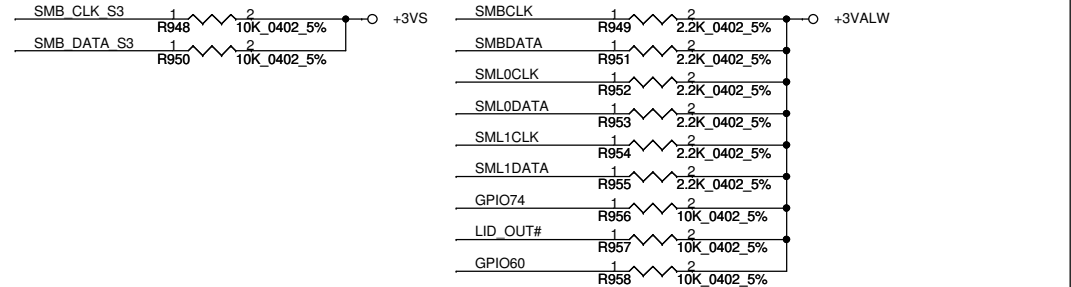
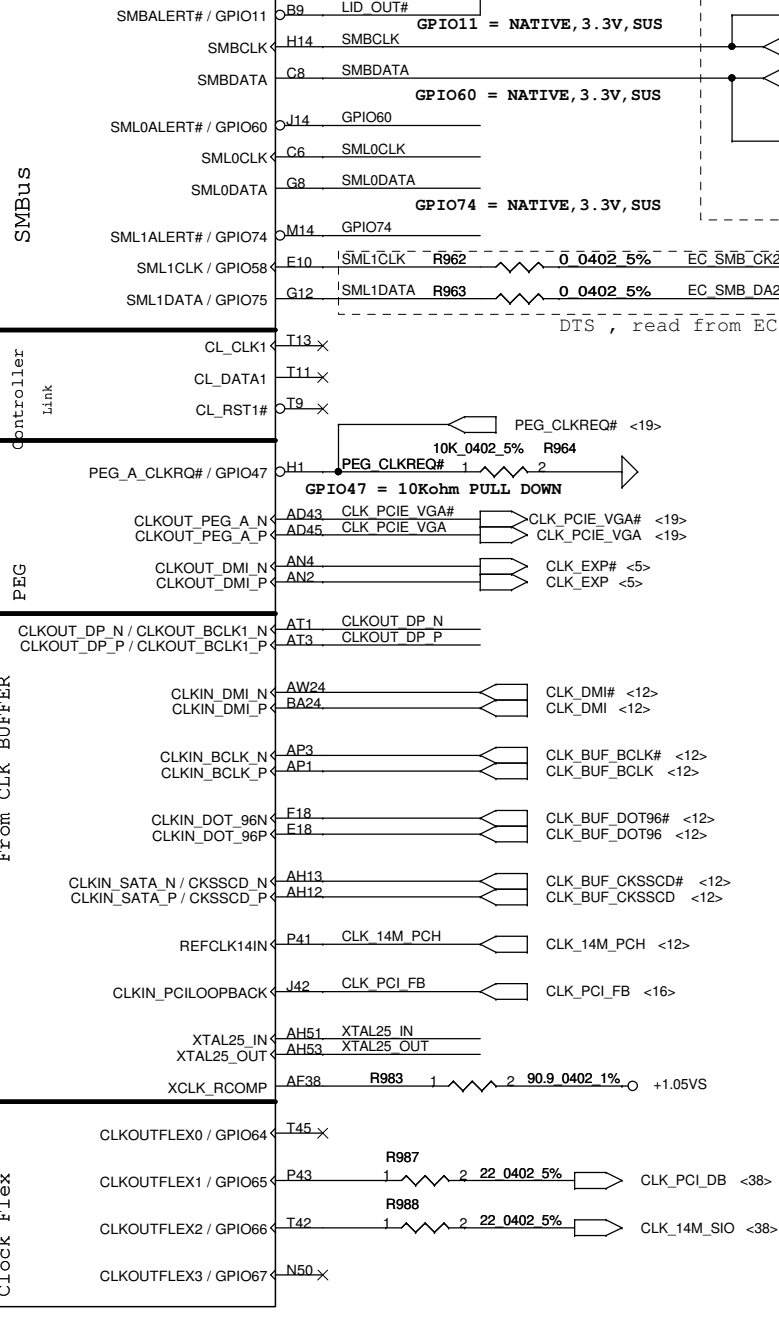
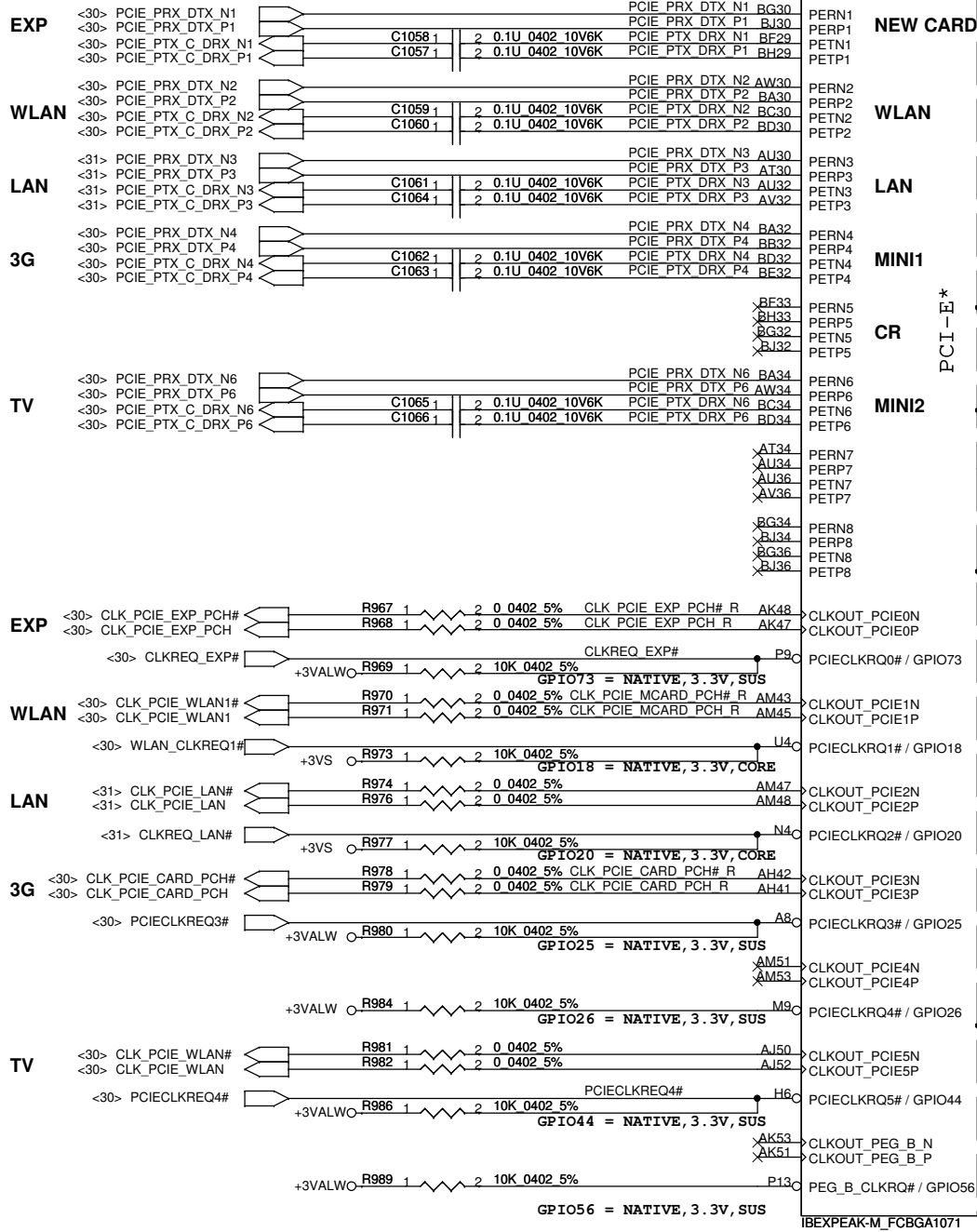
PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz



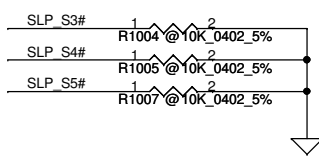
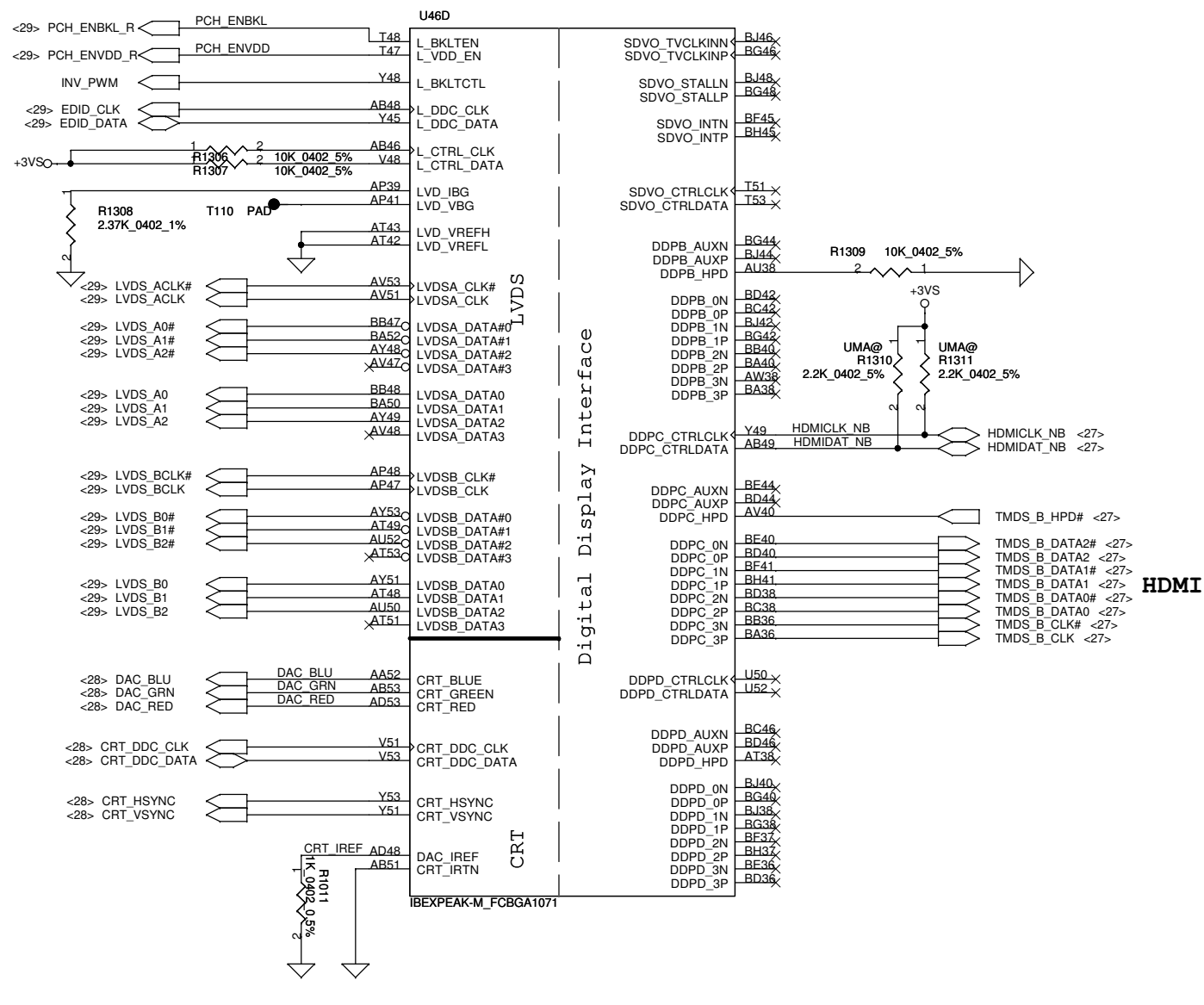
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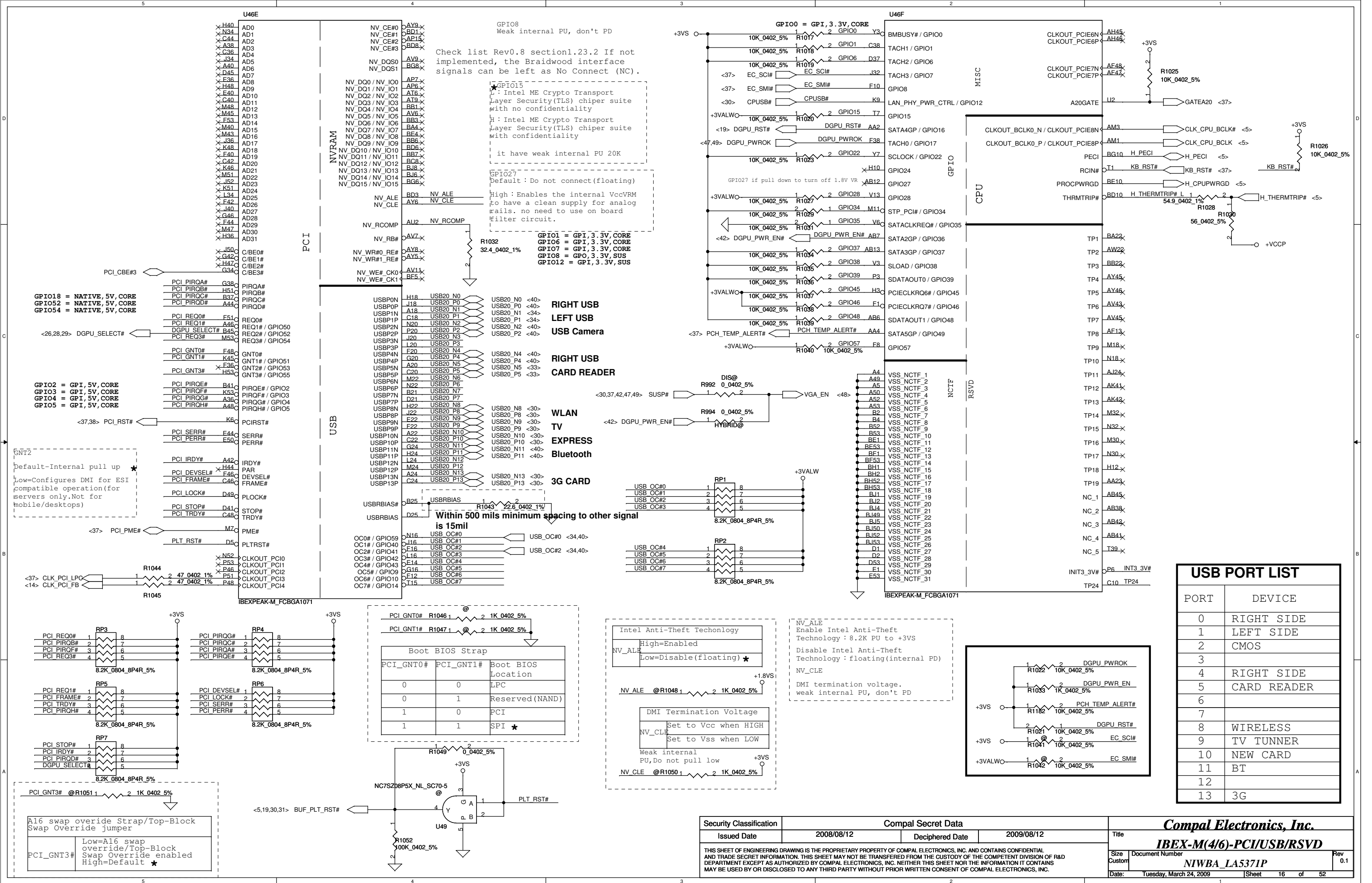
PCIe PORT LIST	
PORT	DEVICE
1	NEW CARD
2	WLAN
3	LAN
4	3G
5	X
6	TV TUNNER
7	X
8	X

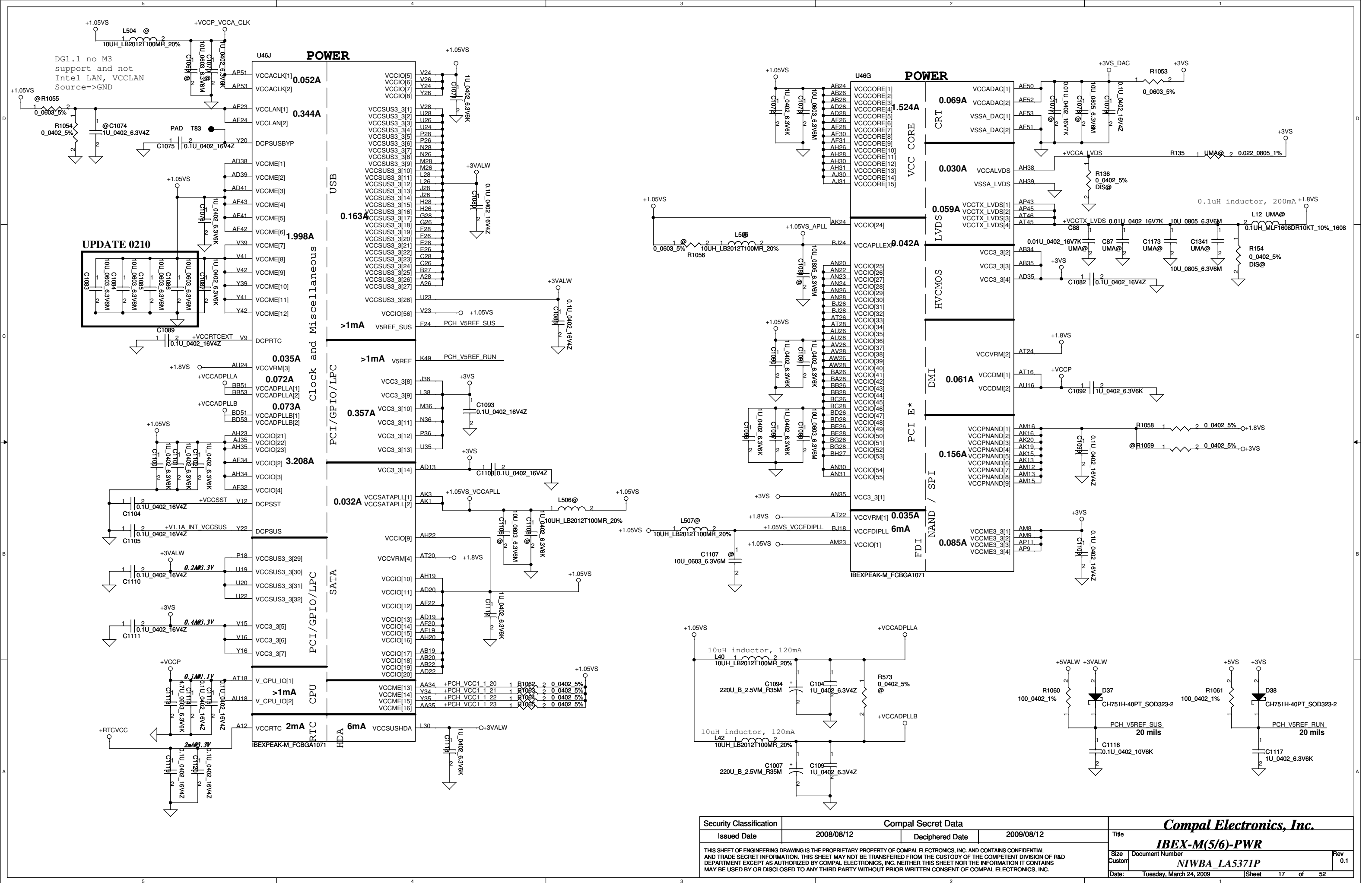


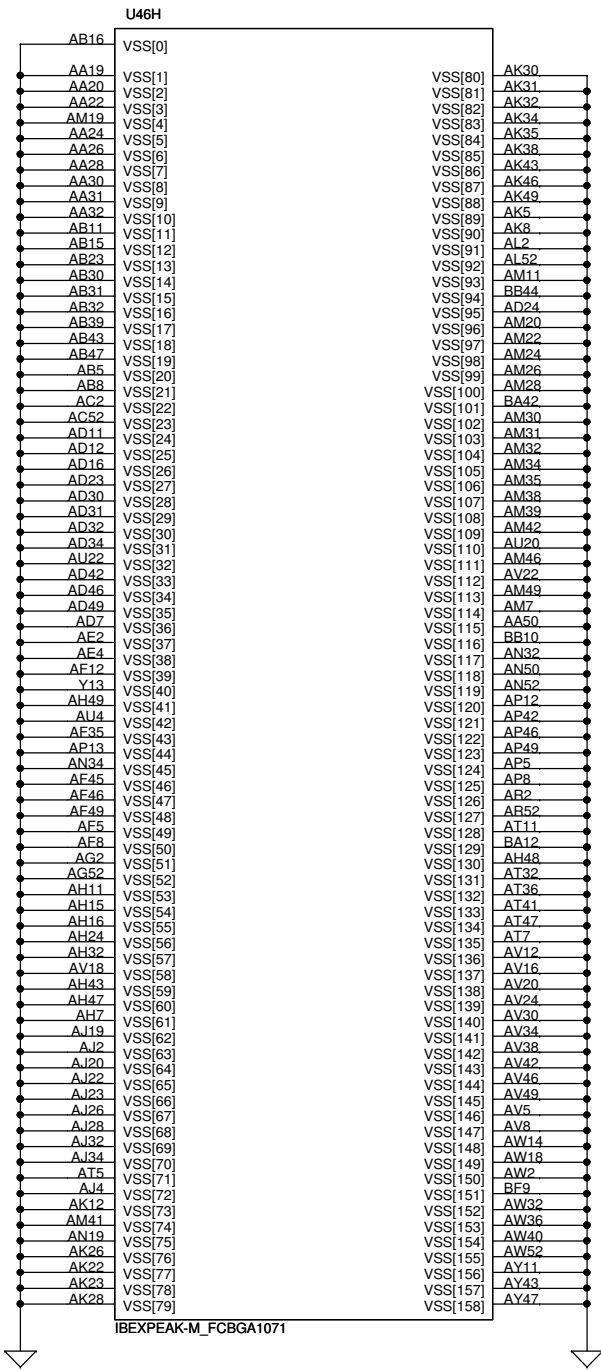
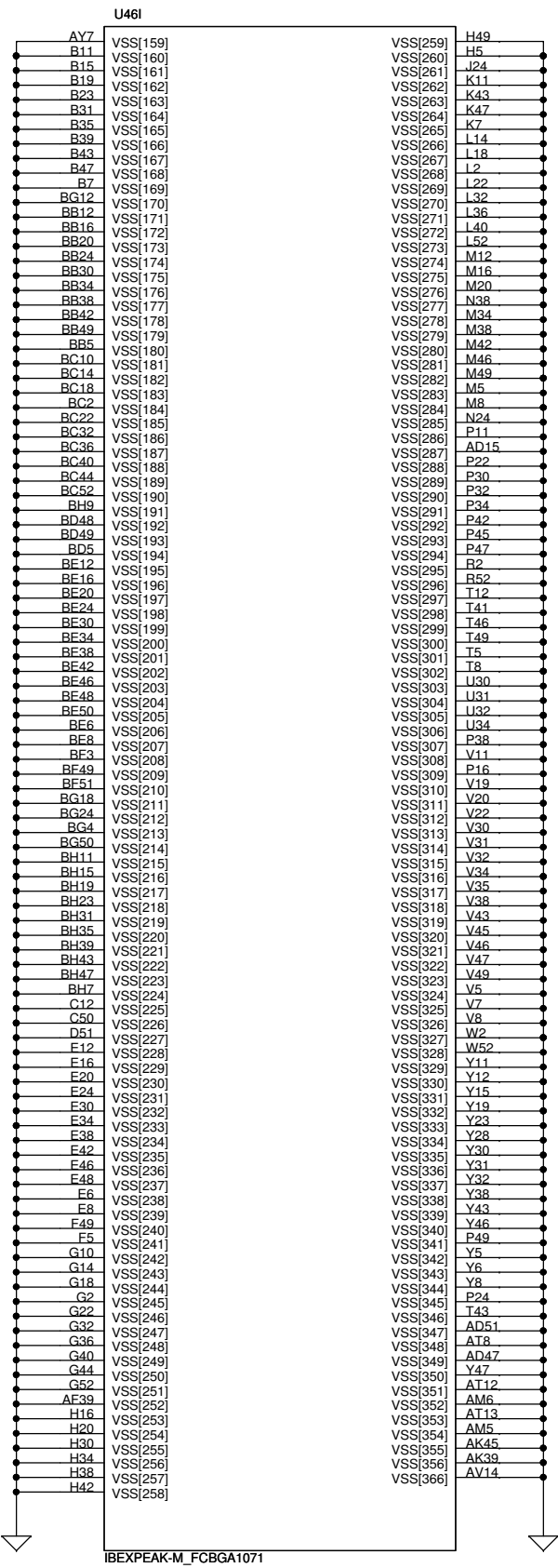
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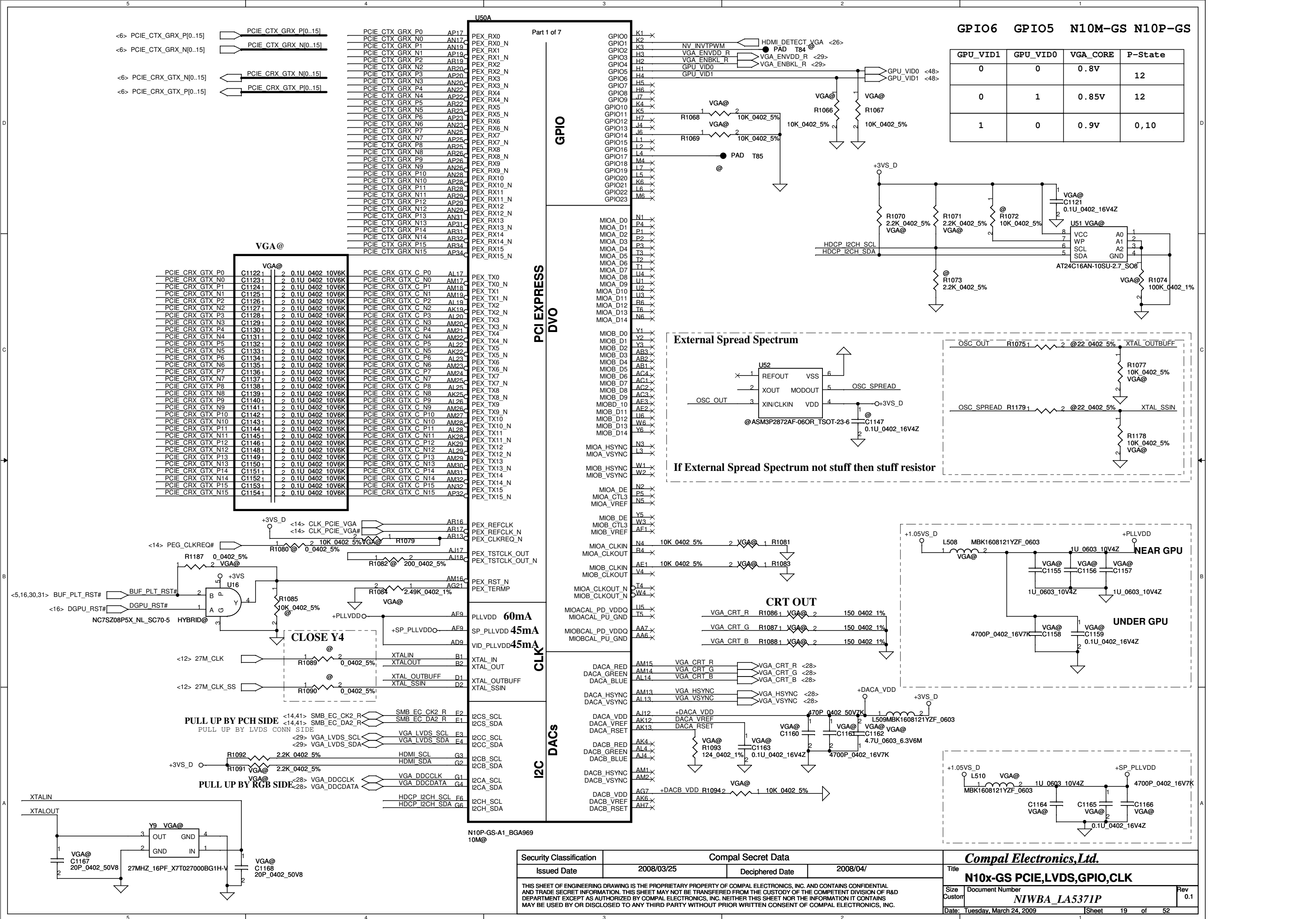
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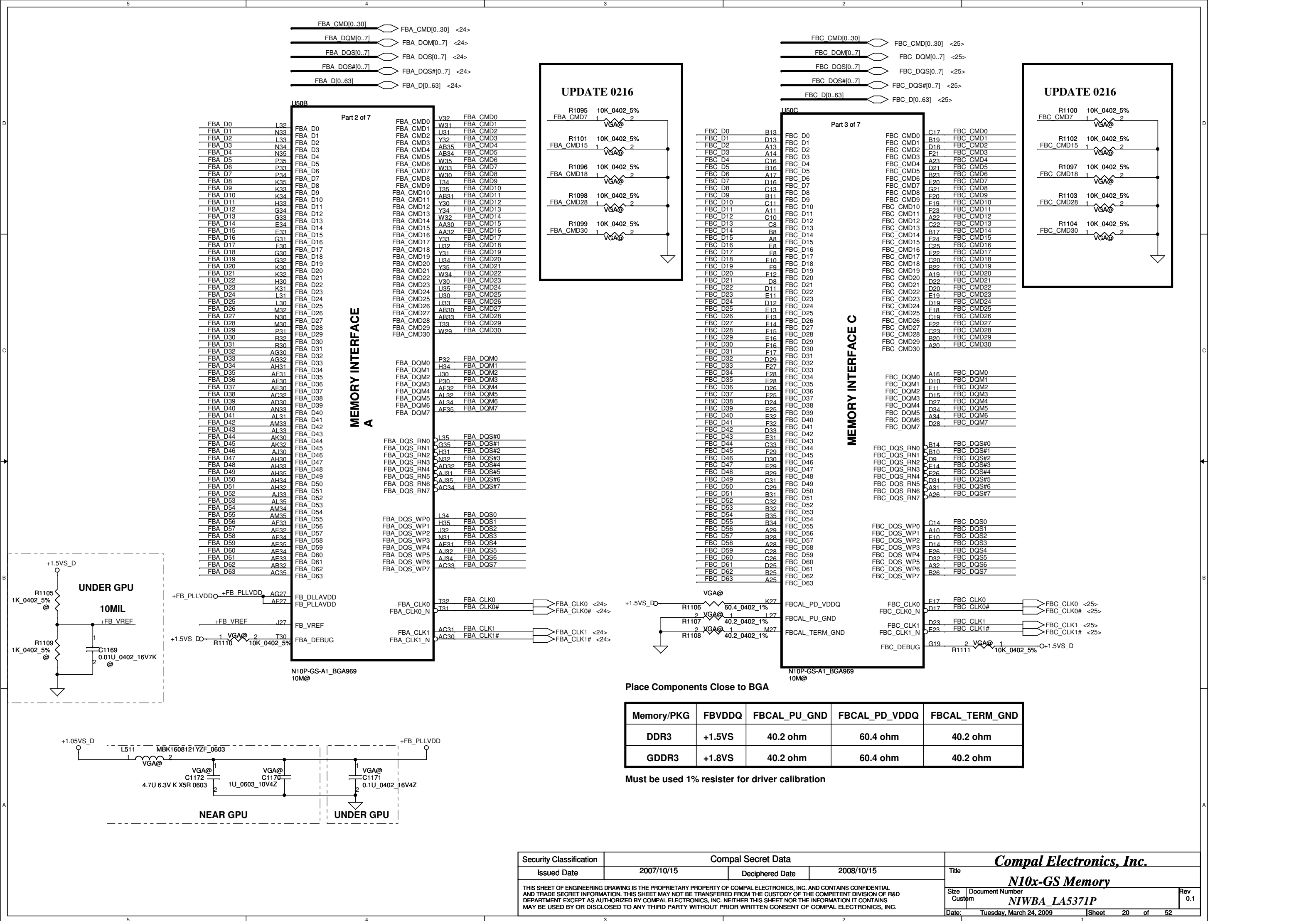


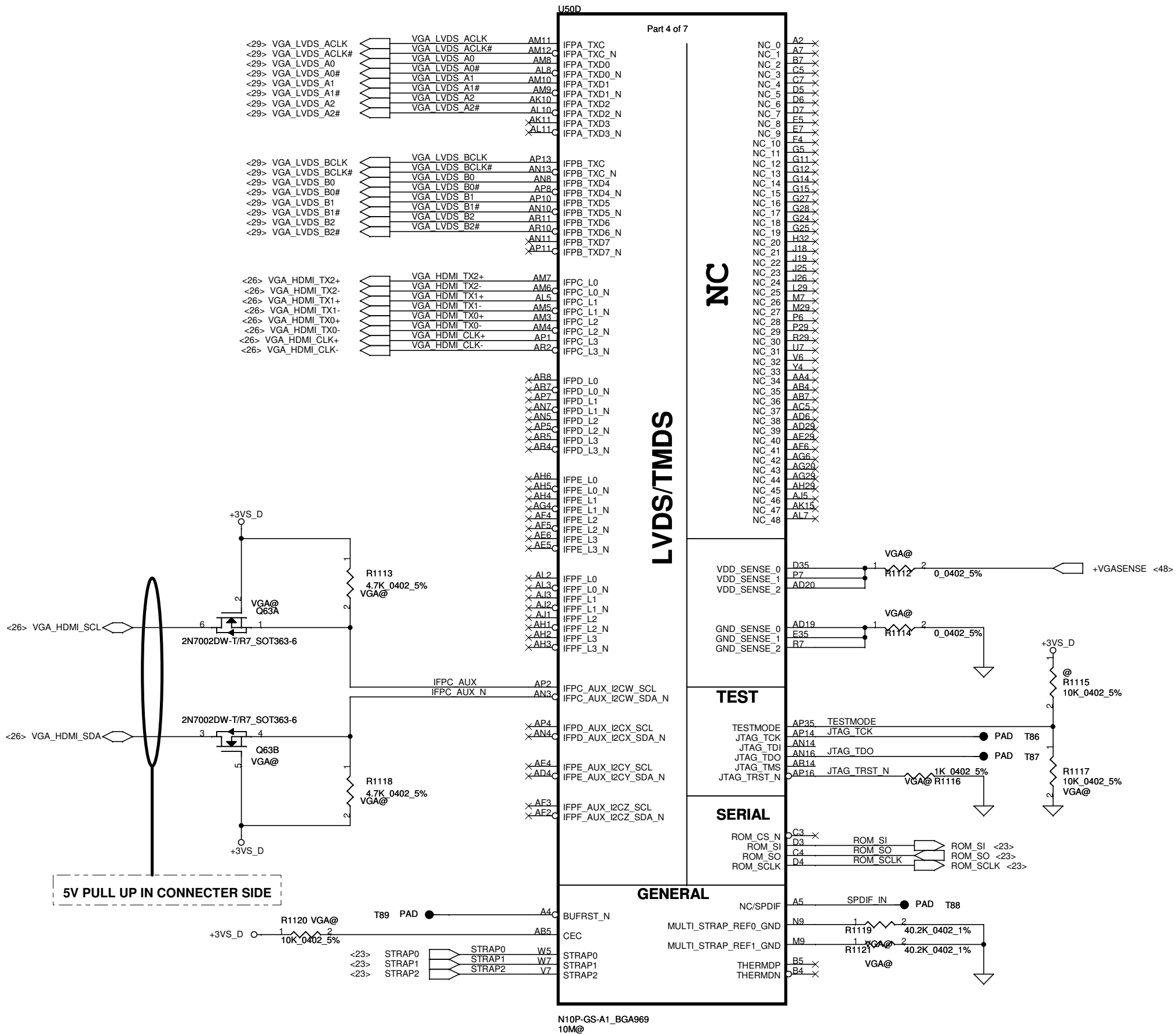




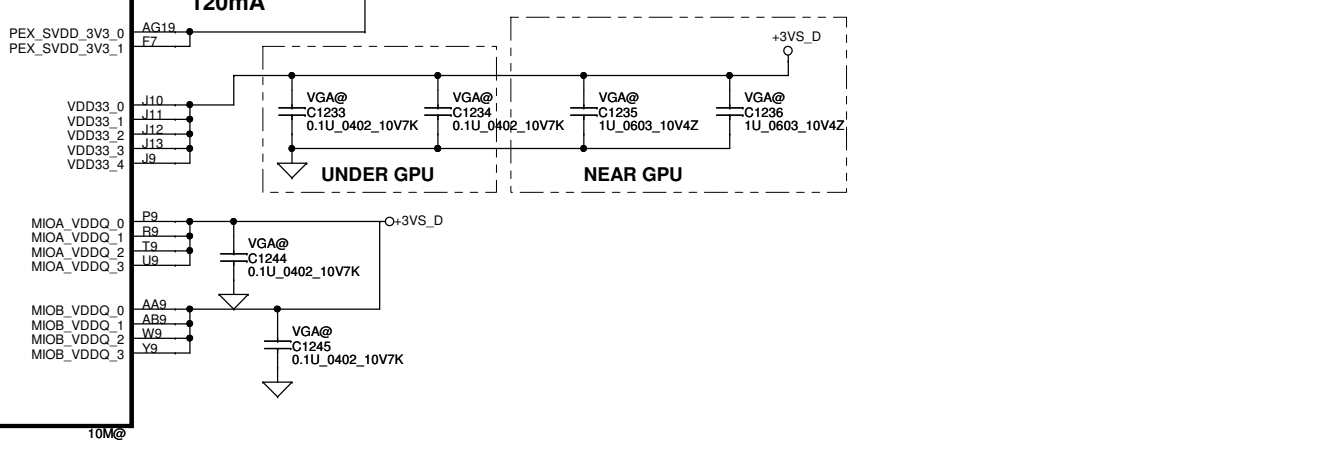
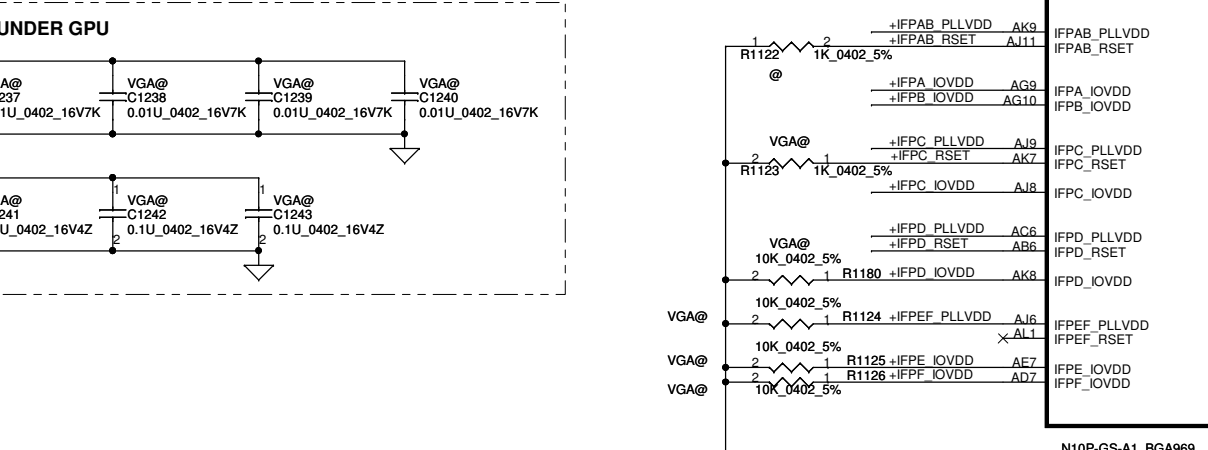
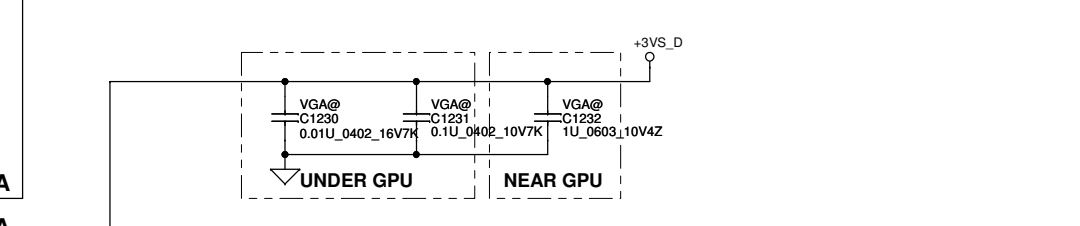
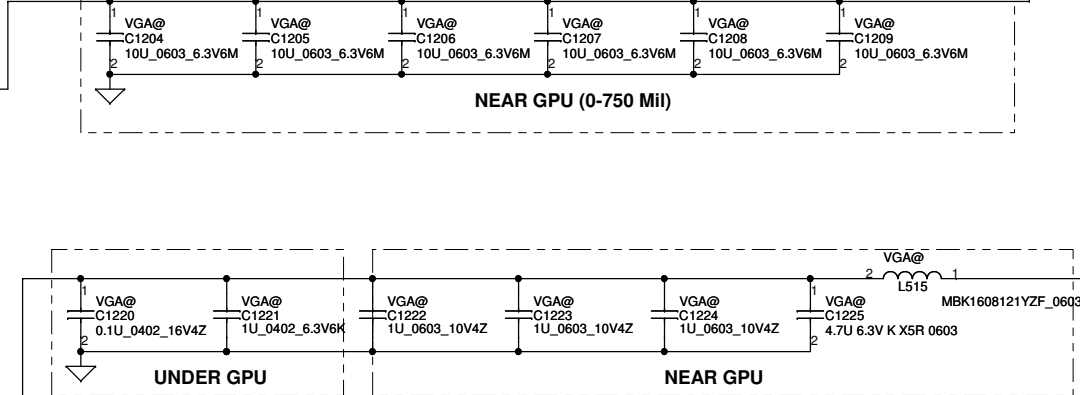
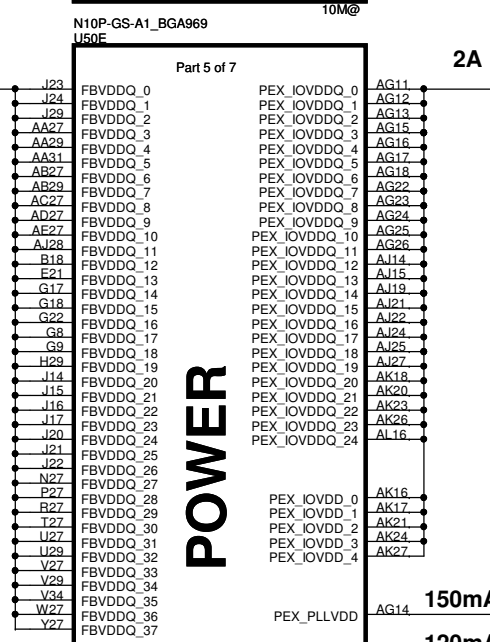
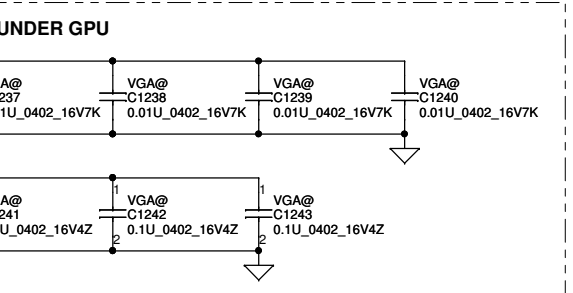
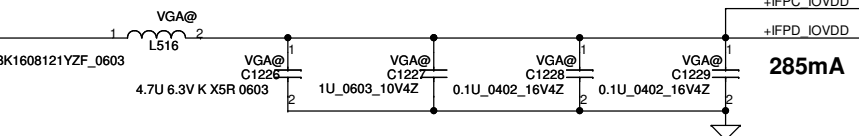
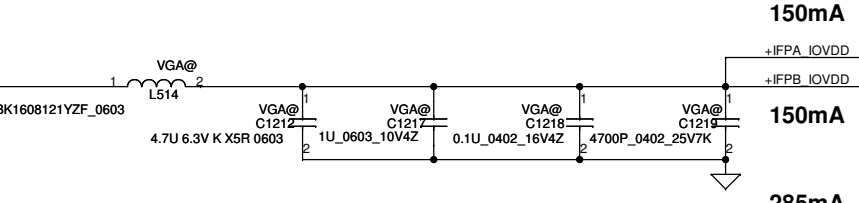
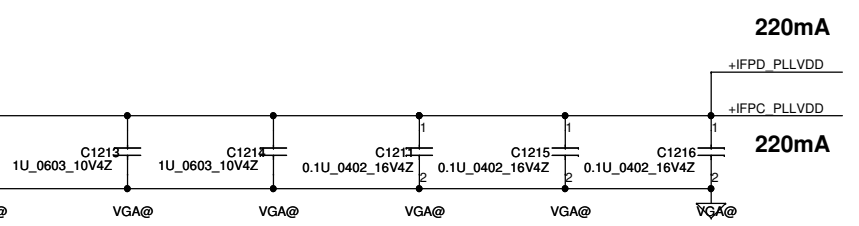
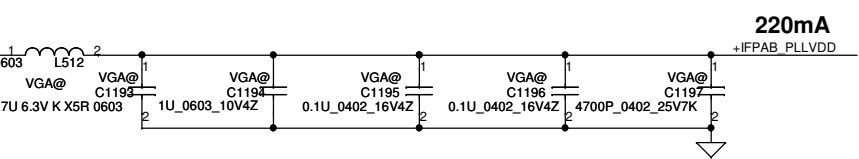
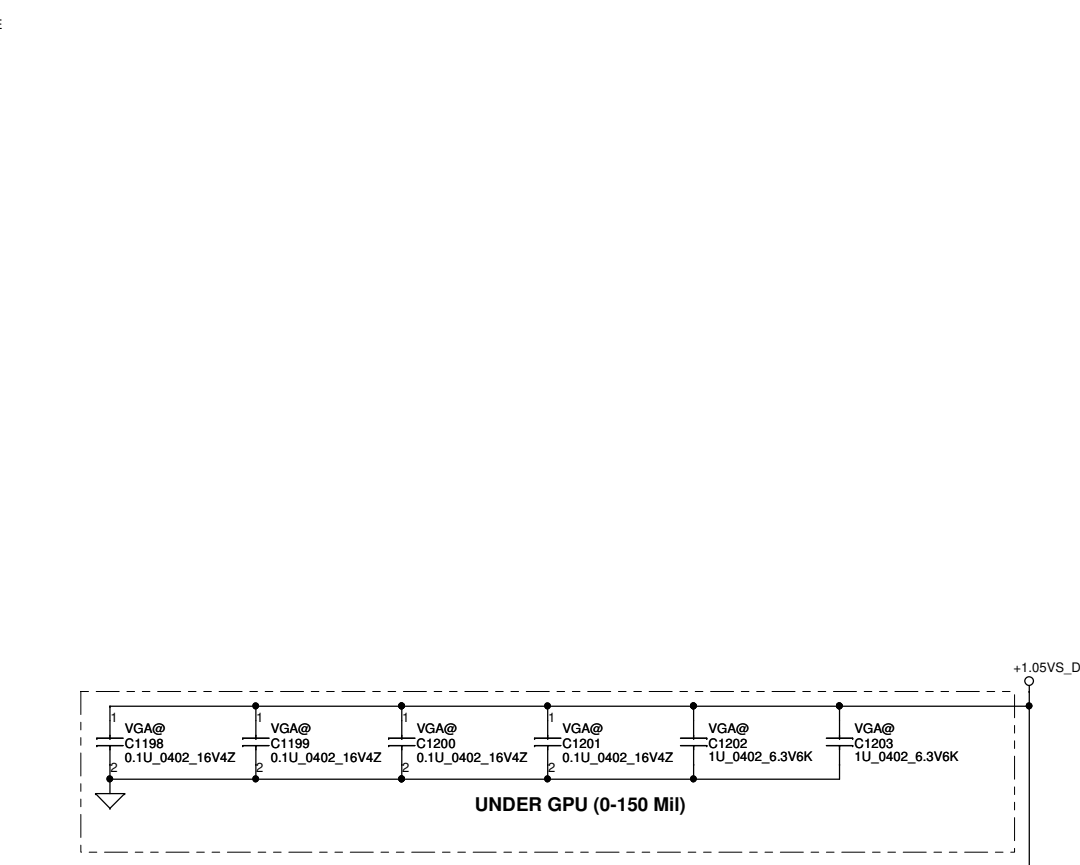
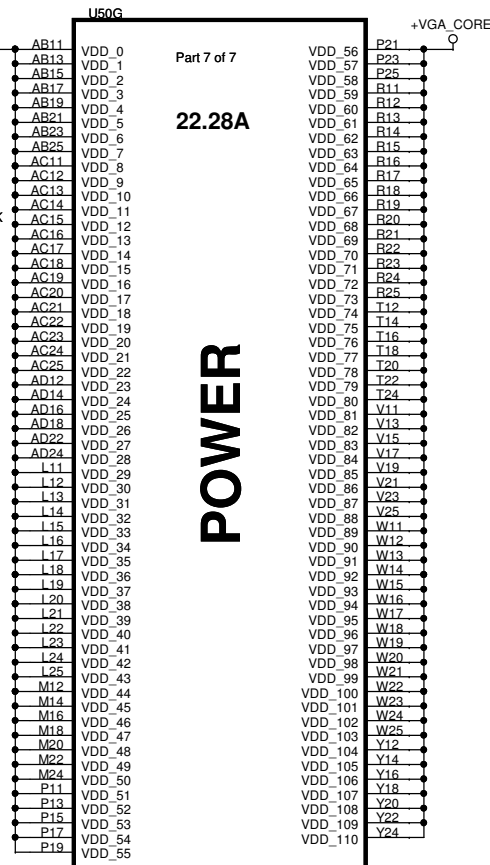
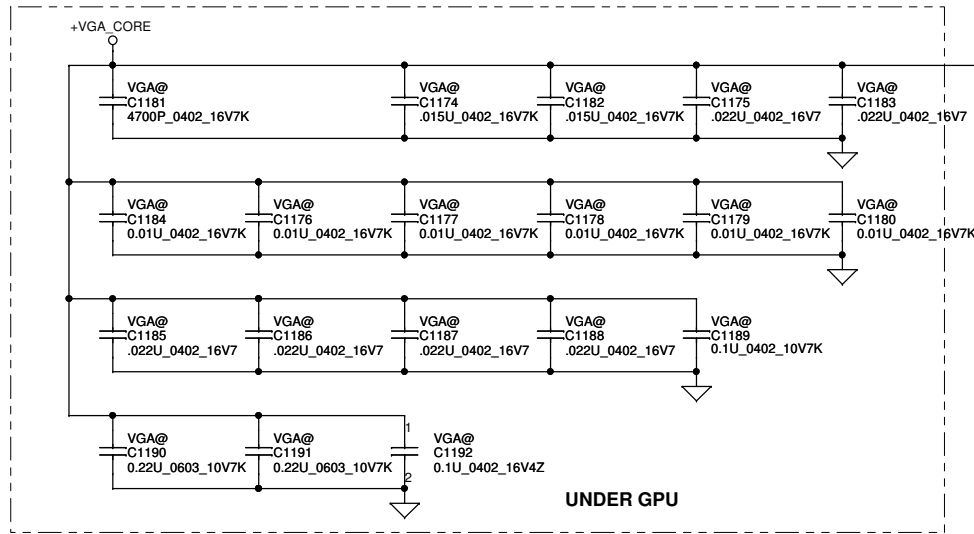
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2008/10/31	Deciphered Date	2009/10/31	Title IBEX-M(6/6)-GND	
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				Date: Tuesday, March 24, 2009	Sheet 18 of 52



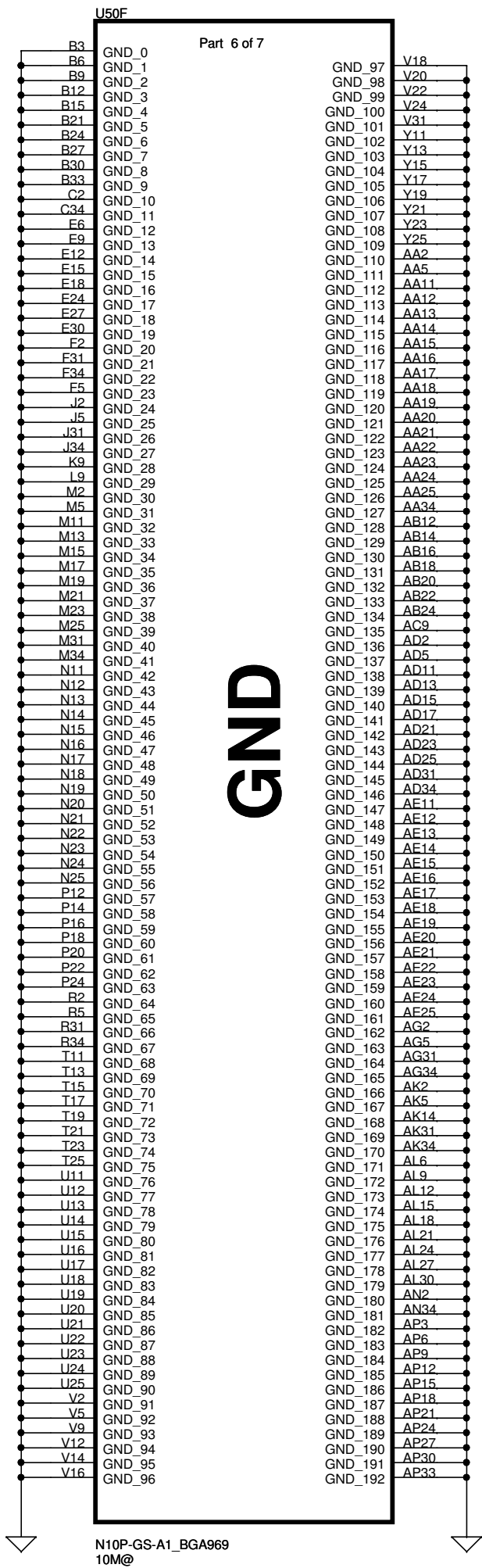




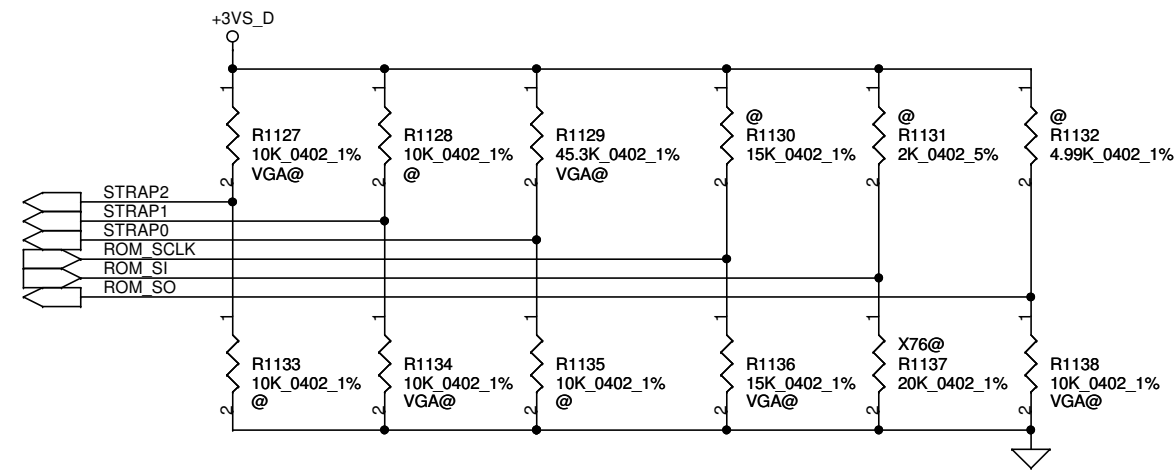
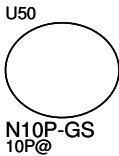
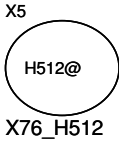
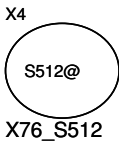
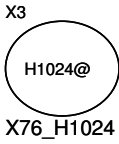
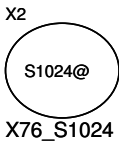
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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				Size Custom	Document Number NIWBA_LA5371P Rev 0.1
				Date: Tuesday, March 24, 2009	Sheet 21 of 52



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2007/10/15		2008/10/15		Title	
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Size		Document Number		Rev	
C		NIWBA_LA5371P		0.1	
Date:		Tuesday, March 24, 2009		Sheet	
		22		of	
		52			



<21> STRAP2
<21> STRAP1
<21> STRAP0
<21> ROM_SCLK
<21> ROM_SI
<21> ROM_SO



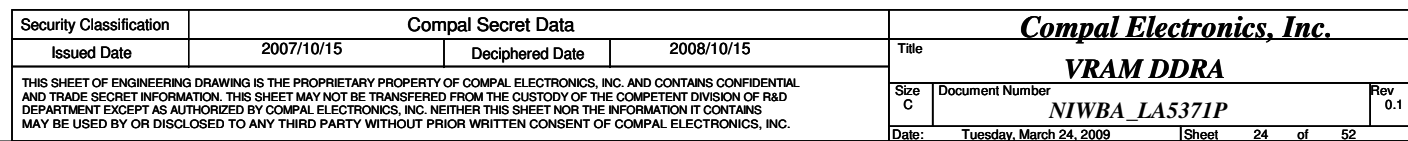
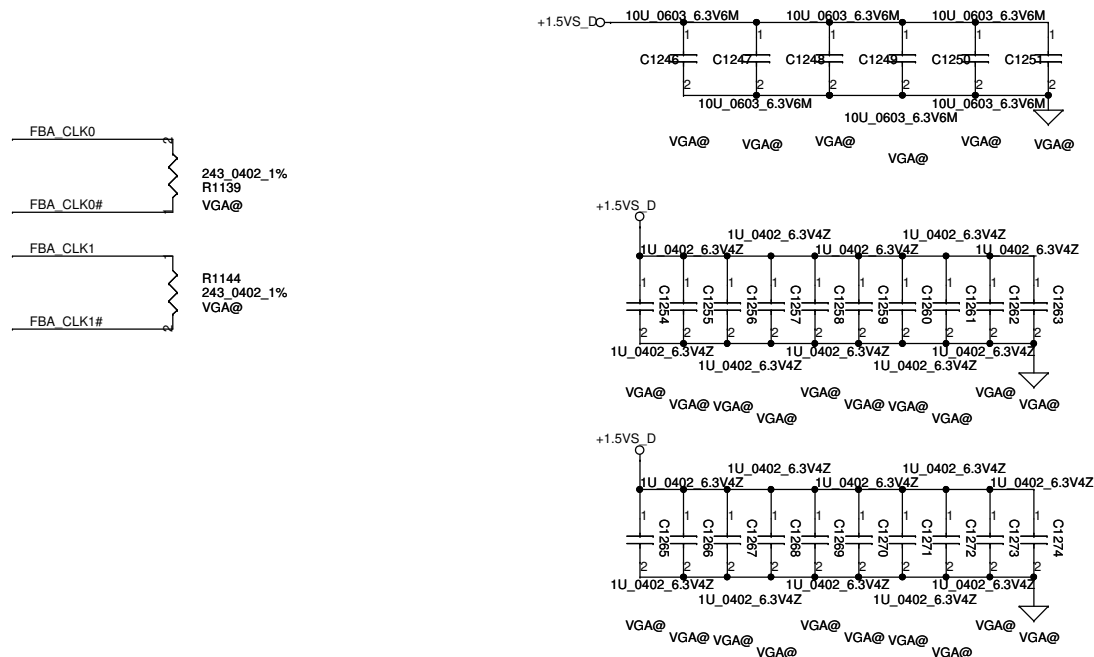
GB1 Family GPU Strap Options

		GPU DEVID	RAM_CFG	GPU DEVID				
GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0	
N10P-GS (0xA34)	Samsung	64Mx16	PD 10K	PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K

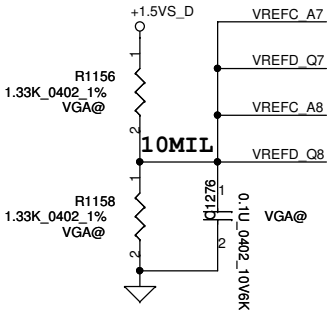
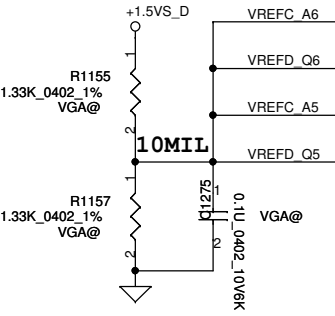
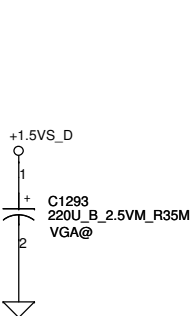
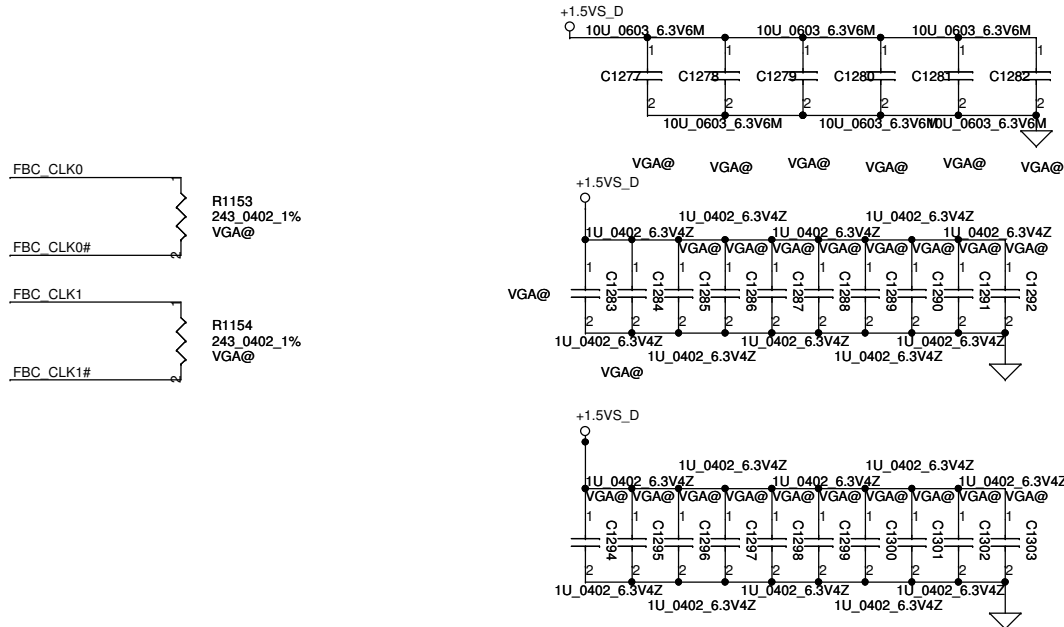
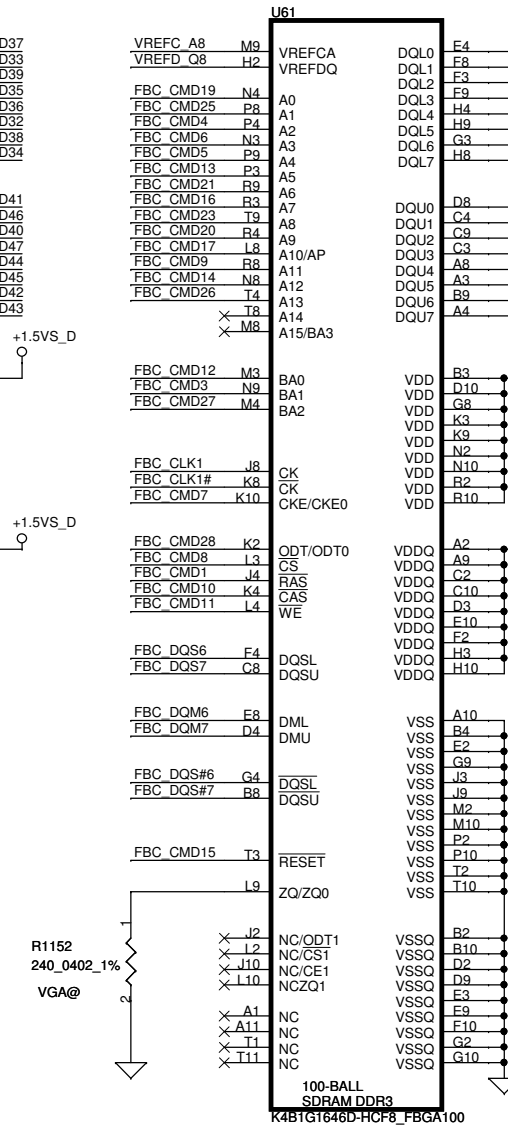
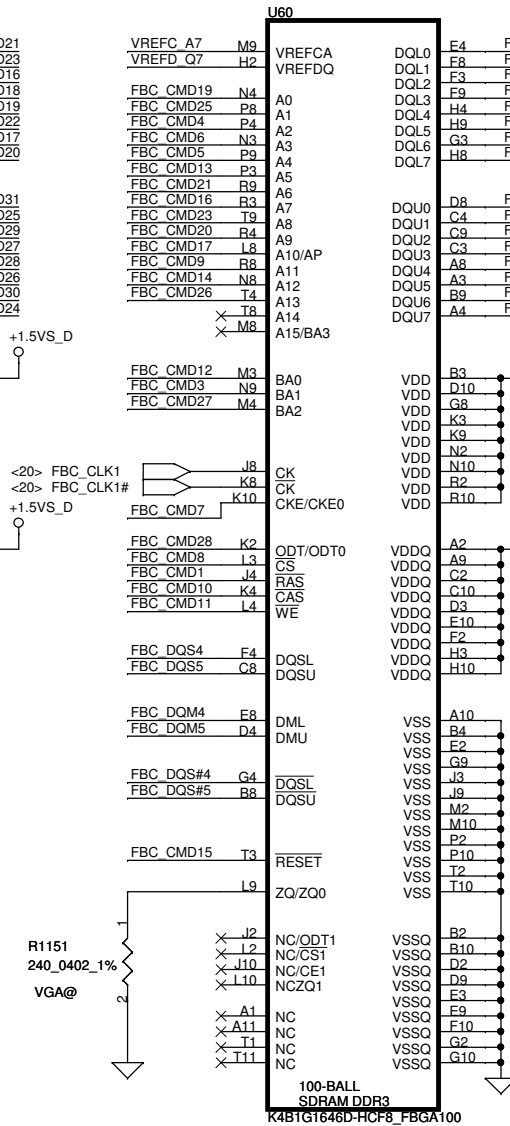
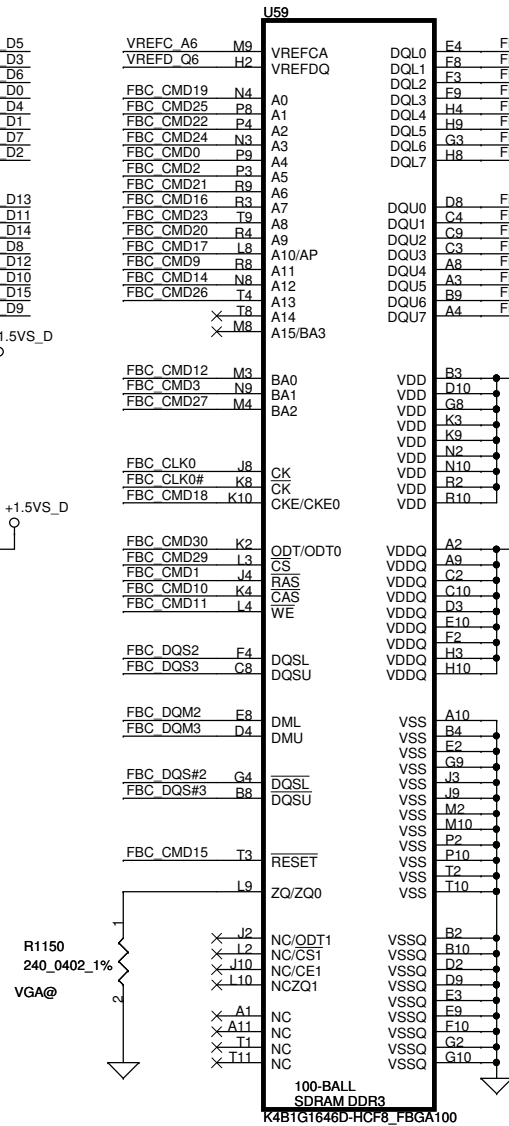
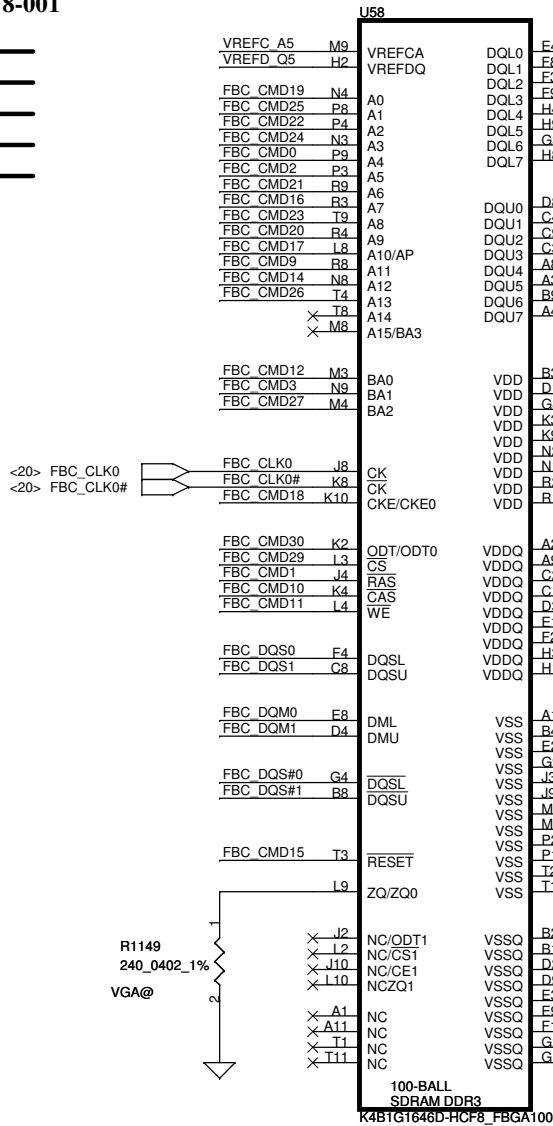
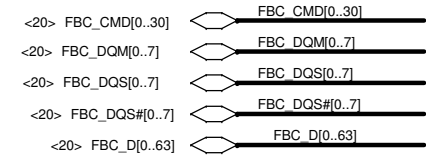
GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0	
N10M-GS (0xA74)	Samsung	64Mx16	PD 10K	PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K

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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title N10x-GS GND & STRAP	
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<20> FBA_CMD[0..30]		FBA_CMD[0..30]
<20> FBA_DQM[0..7]		FBA_DQM[0..7]
<20> FBA_DQS[0..7]		FBA_DQS[0..7]
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<20> FBA_D[0..63]		FBA_D[0..63]

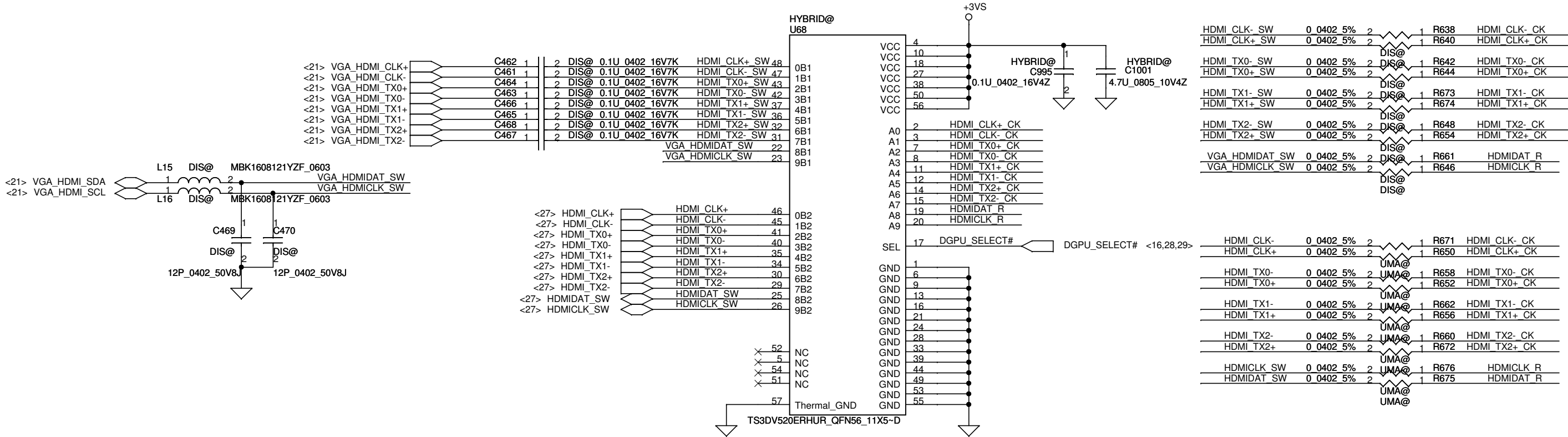


N10x 40nm DDR3 MAPPING
NVIDIA DOCUMENT FOR DA-3978-001

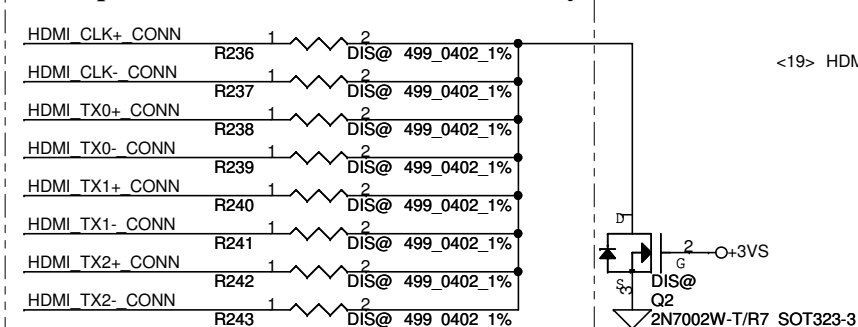


Security Classification		Compal Secret Data		Title VRAM DDRA NIWBA_LA5371P	
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				Date: Tuesday, March 24, 2009	Sheet 25 of 52

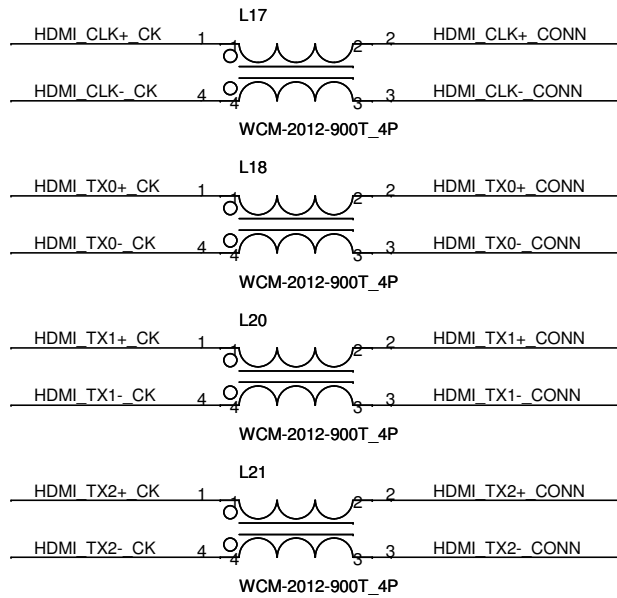
HDMI switch1



TMDS pull down (500ohm) resistors G9x only

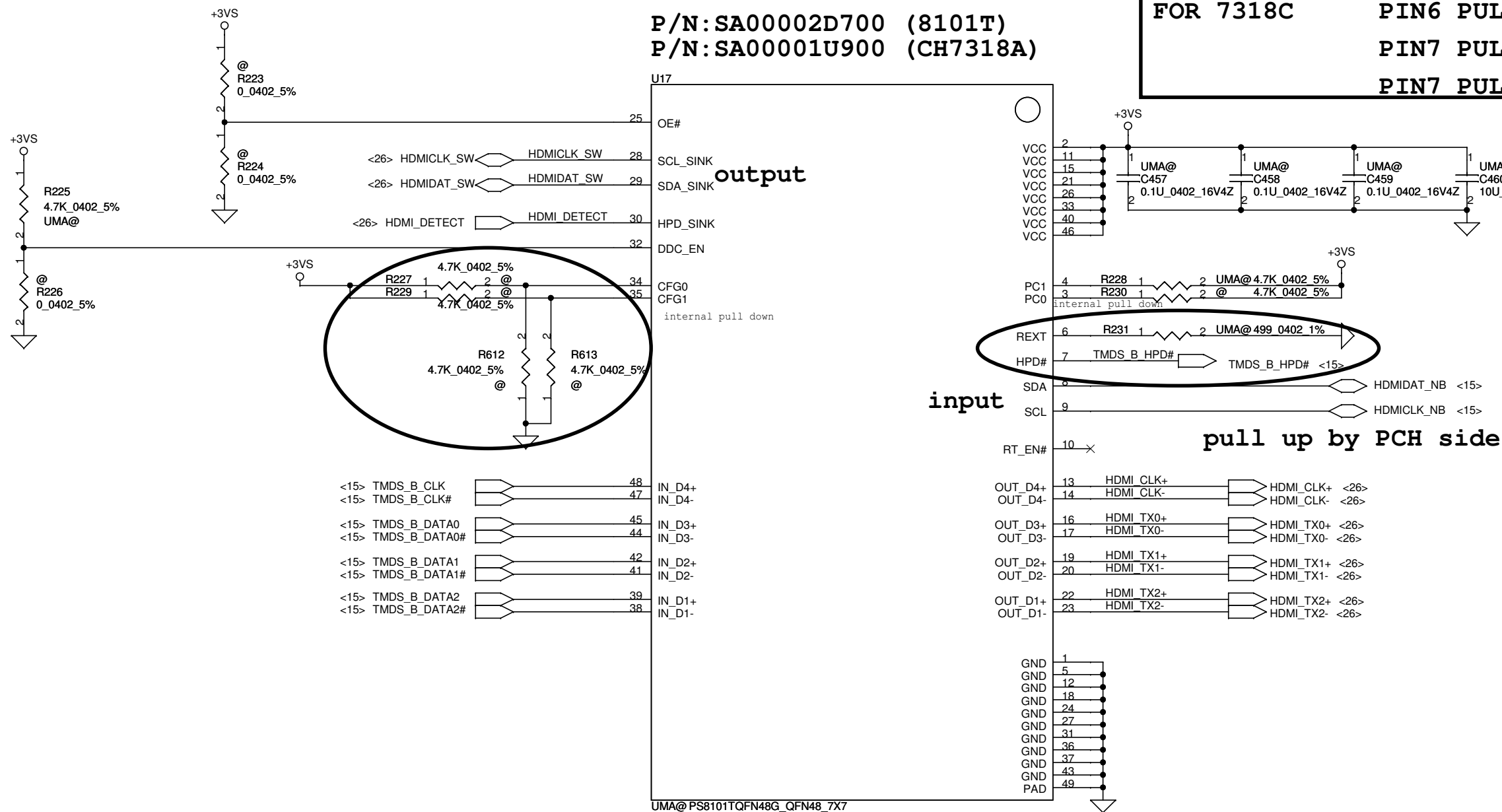


NEAR CONNECT

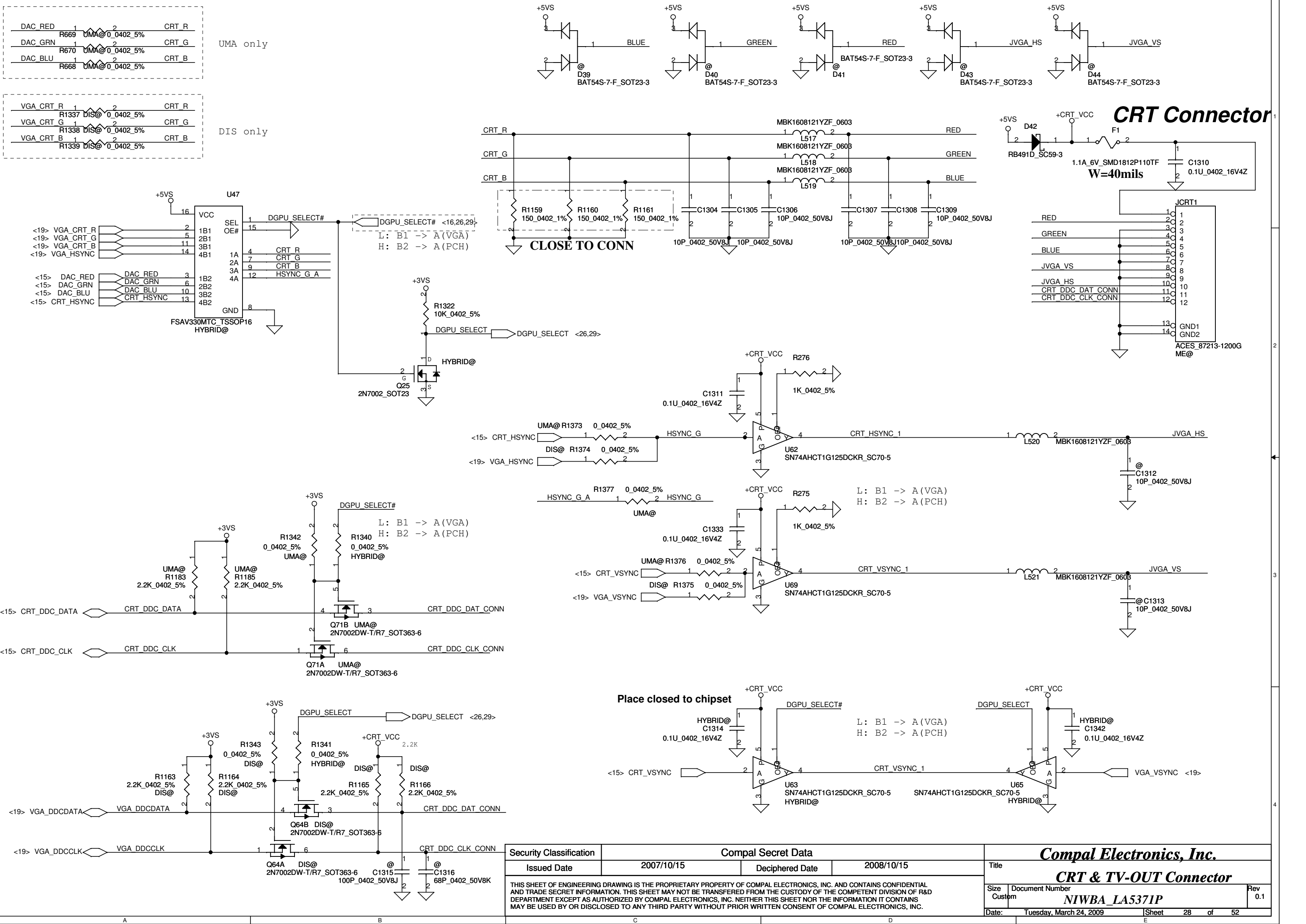


HDMI_CLK+_CK	R251	1	@	2	0	0402	5%	HDMI_CLK+_CONN
HDMI_CLK-_CK	R252	1	@	2	0	0402	5%	HDMI_CLK-_CONN
HDMI_TX0+_CK	R253	1	@	2	0	0402	5%	HDMI_TX0+_CONN
HDMI_TX0-_CK	R254	1	@	2	0	0402	5%	HDMI_TX0-_CONN
HDMI_TX1+_CK	R255	1	@	2	0	0402	5%	HDMI_TX1+_CONN
HDMI_TX1-_CK	R256	1	@	2	0	0402	5%	HDMI_TX1-_CONN
HDMI_TX2+_CK	R257	1	@	2	0	0402	5%	HDMI_TX2+_CONN
HDMI_TX2-_CK	R258	1	@	2	0	0402	5%	HDMI_TX2-_CONN

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Issued Date		2008/03/25	Deciphered Date	2008/04/		
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				Size	Document Number	Rev
				Custom	KIWB1/B2_LA4601P	0.1
				Date:	Tuesday, March 24, 2009	Sheet

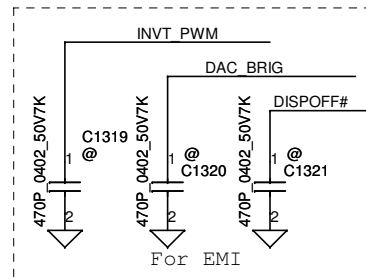
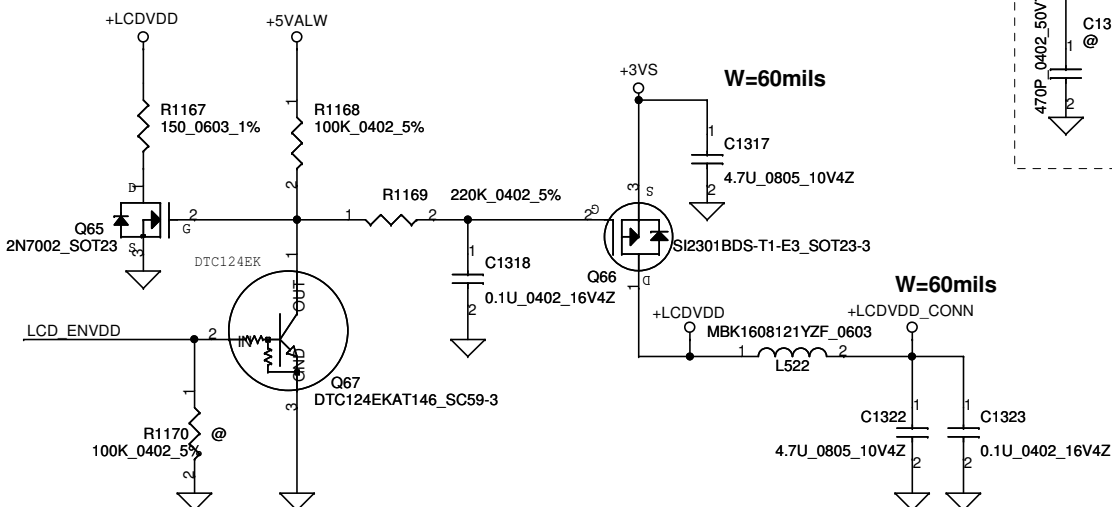


Security Classification		Compal Secret Data		Compal Electronics,Ltd.	
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	
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				Size	Rev
				Custom	0.1
Date: Tuesday, March 24, 2009				Sheet	27 of 52

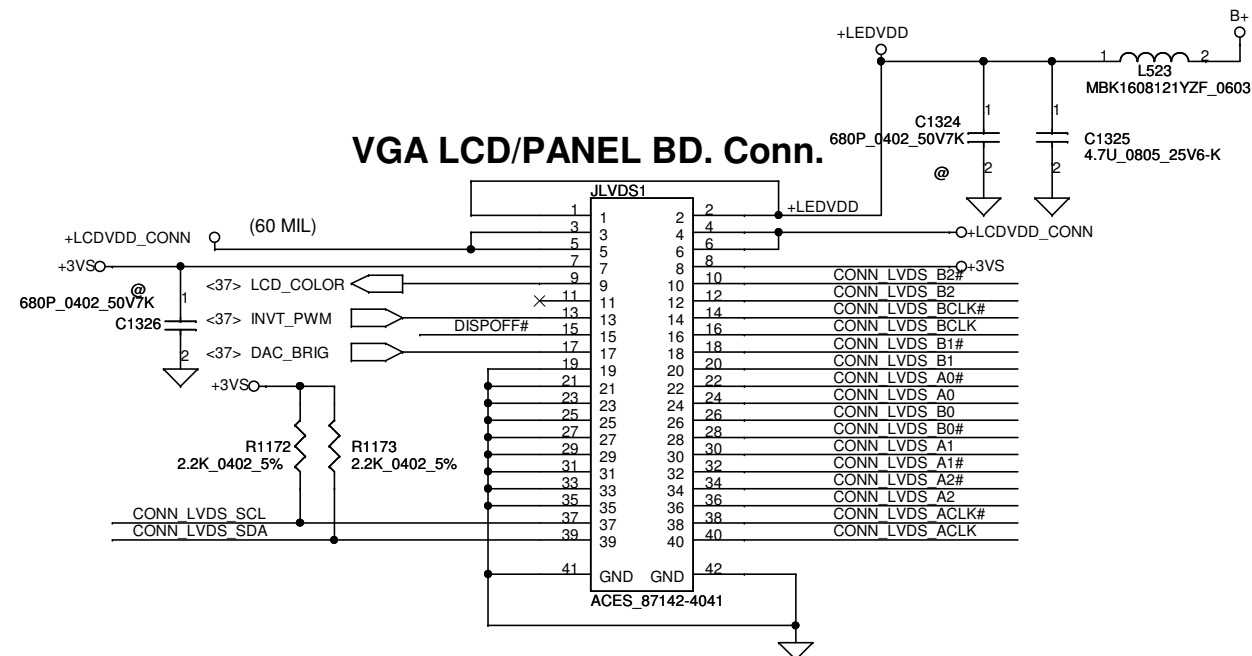


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Issued Date		2007/10/15	Deciphered Date	2008/10/15		
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				Size	Document Number	Rev
				Custom	NIWBA_LA5371P	0.1
				Date: Tuesday, March 24, 2009 Sheet 28 of 52		

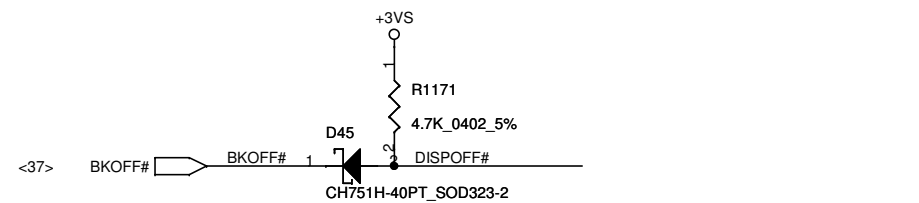
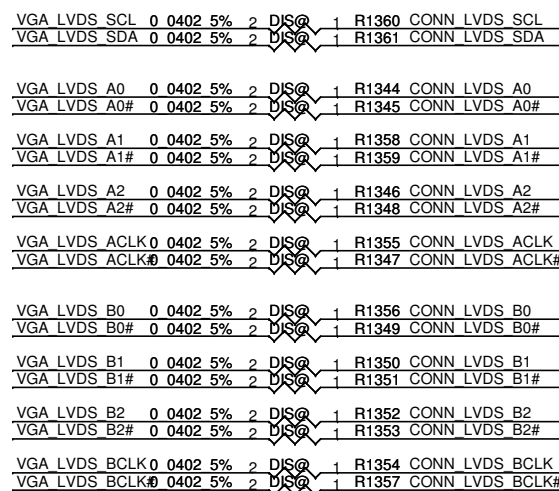
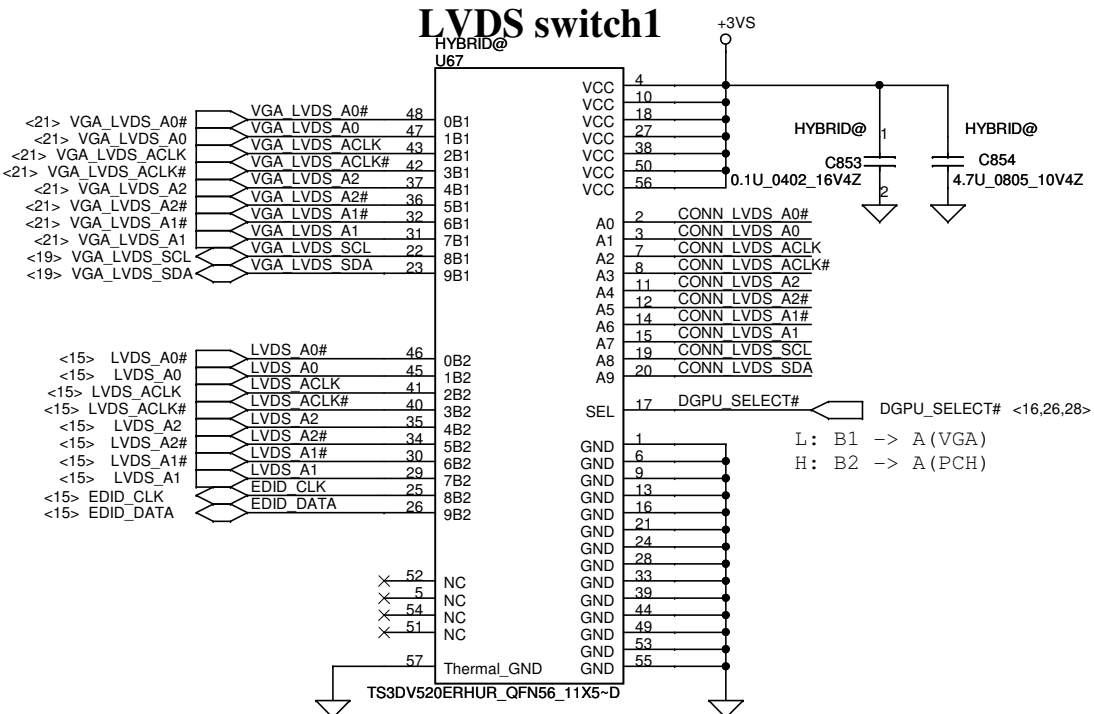
LCD POWER CIRCUIT



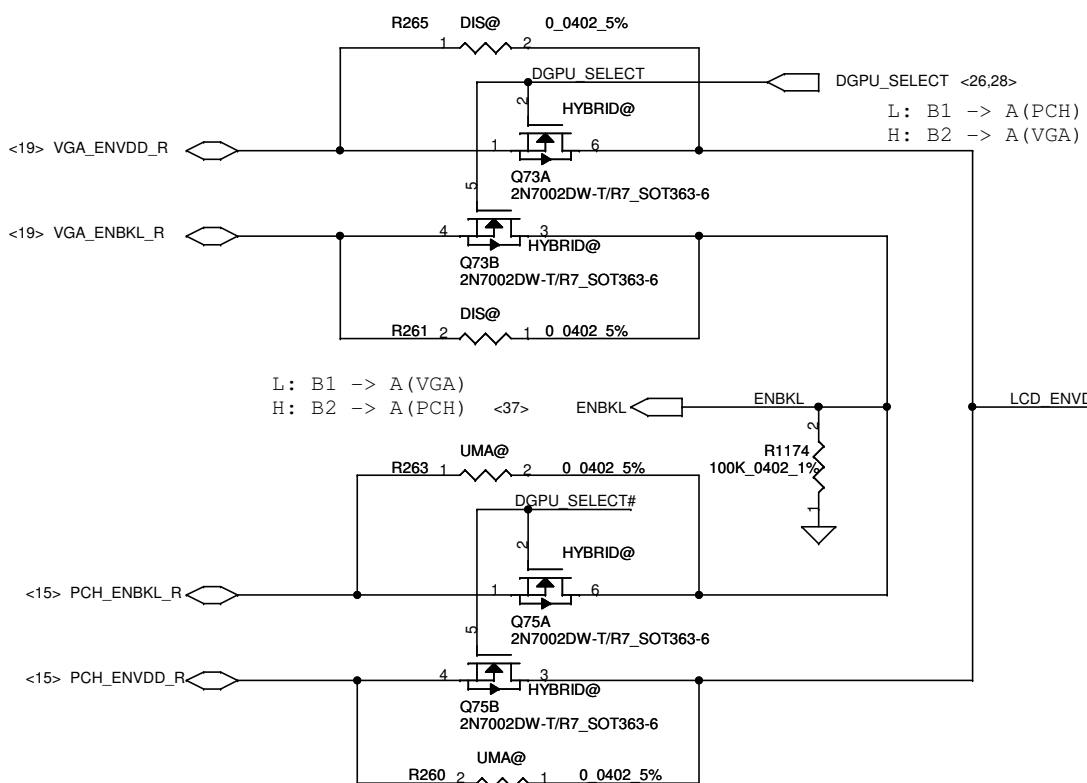
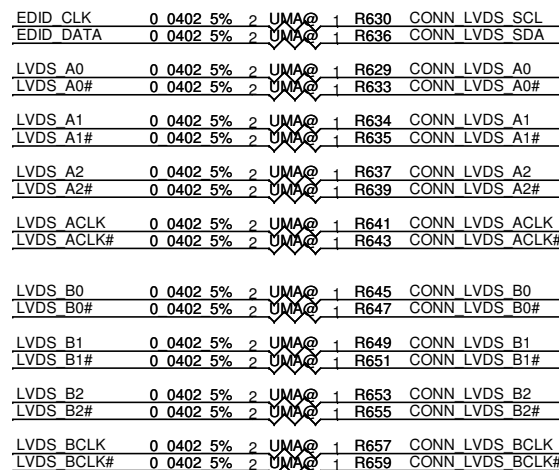
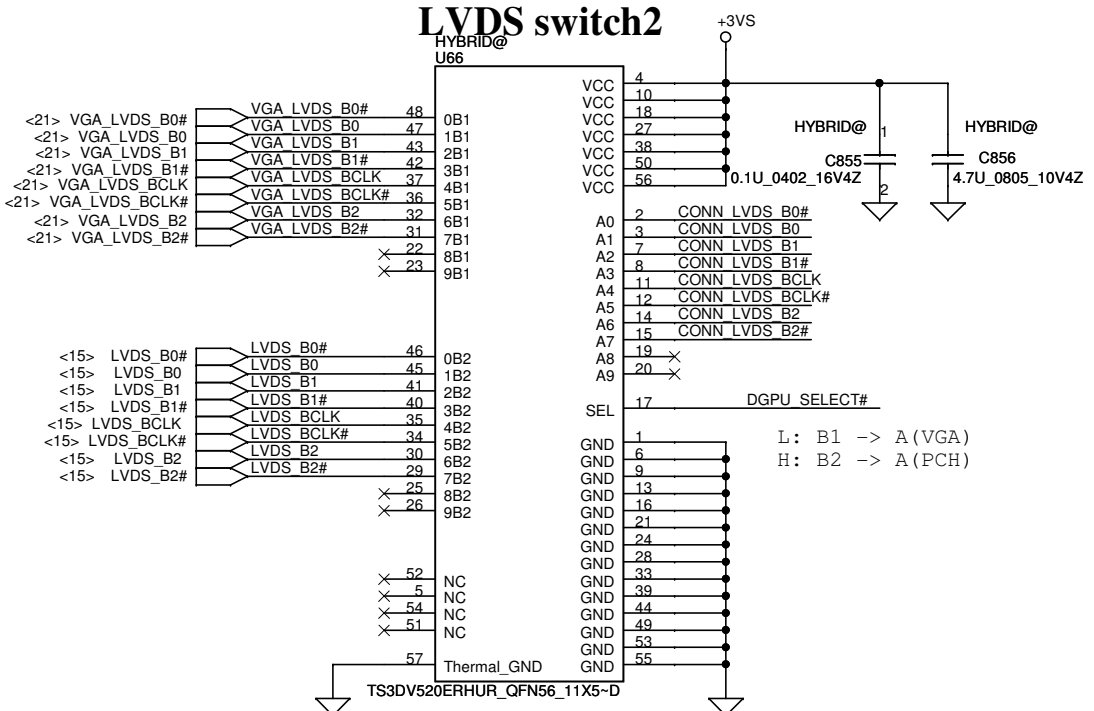
VGA LCD/PANEL BD. Conn.



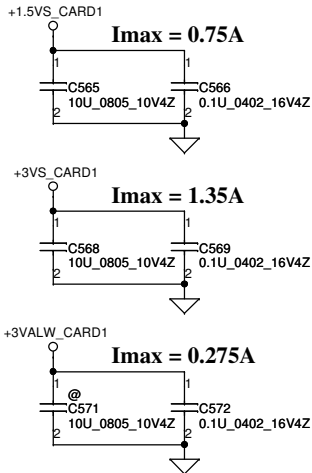
LVDS switch1



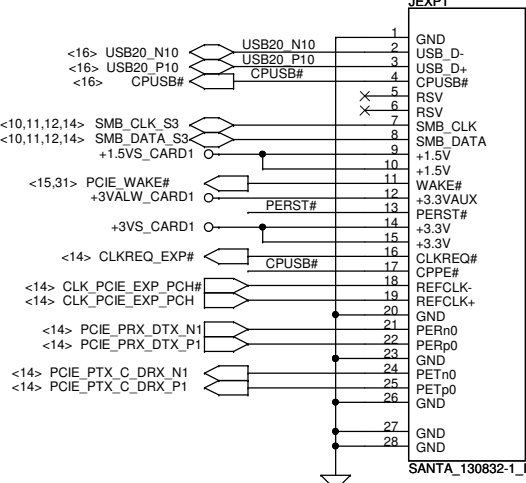
LVDS switch2



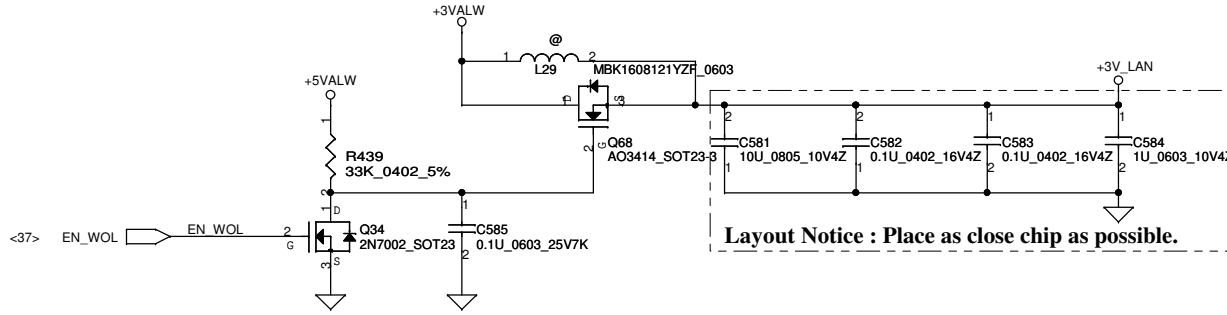
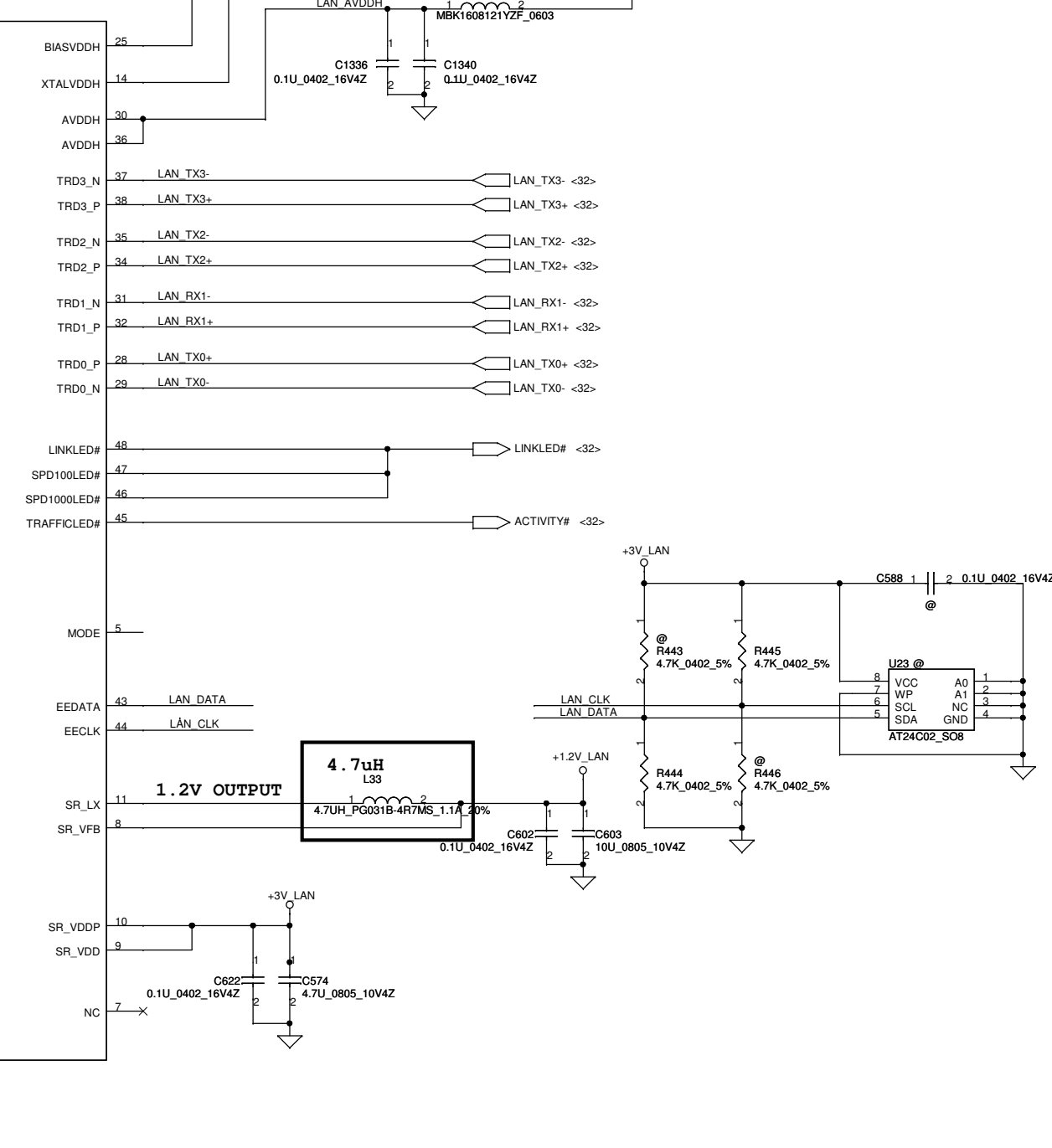
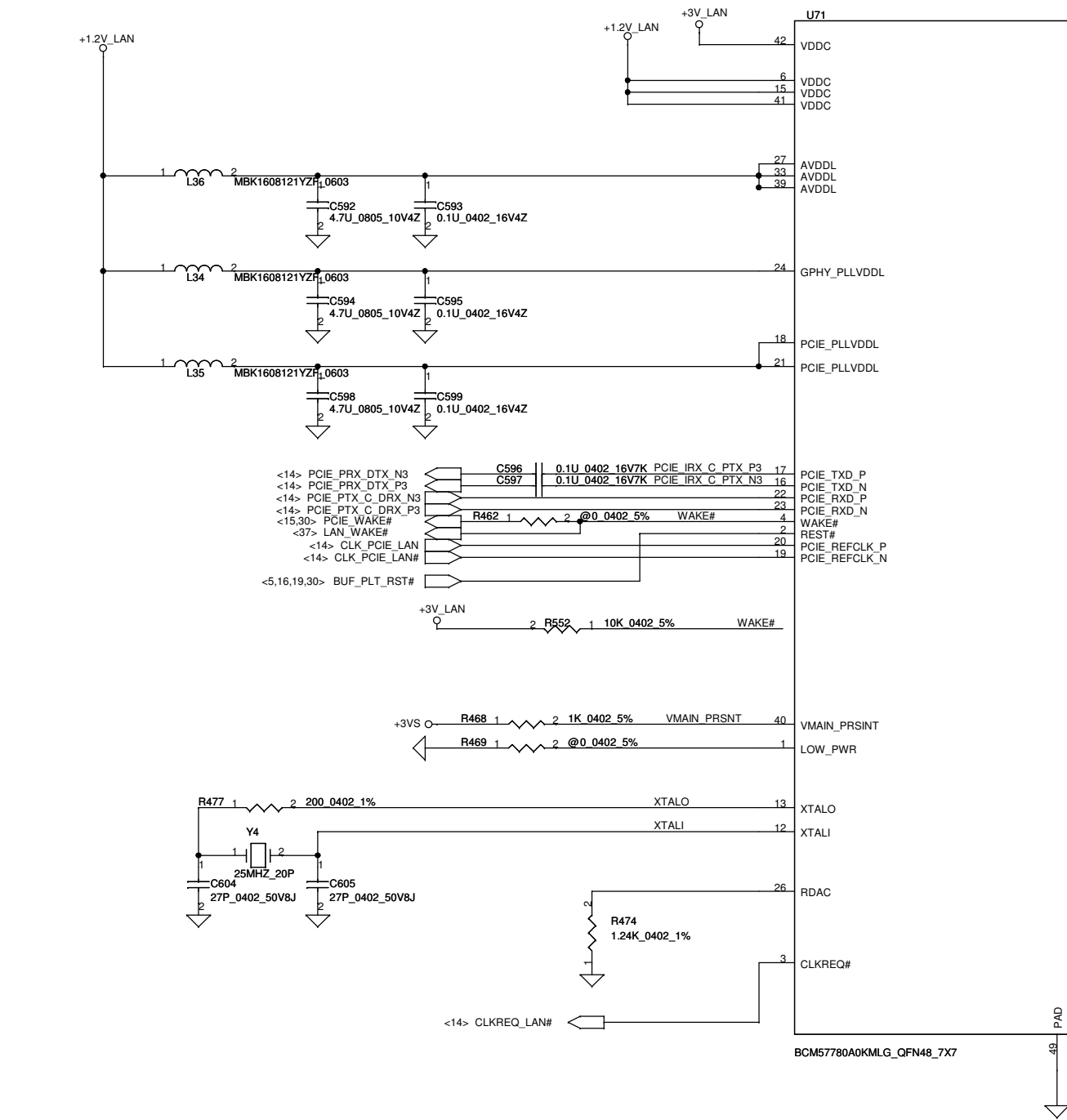
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>		
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title <i>LVDS & DVI Connector</i>		
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				Date	Tuesday, March 24, 2009	Sheet 29 of 52

Mini-Express Card(Slot 1-TV TUNNER) 4.0mm high

5.6mm high

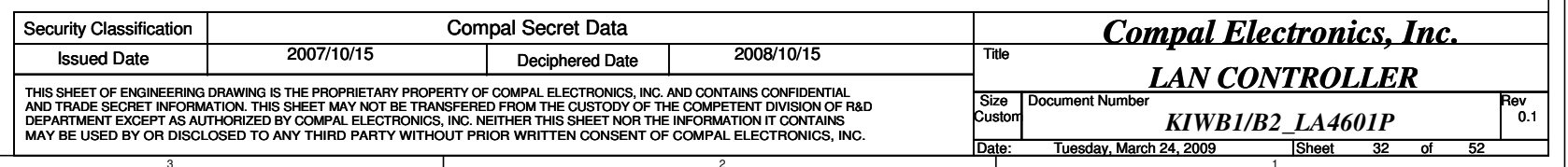


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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	Mini-Card/3G/FeliCa/BT
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				NIWBA_LAS371P	
				Date:	Tuesday, March 24, 2009
				Sheet	30 of 52

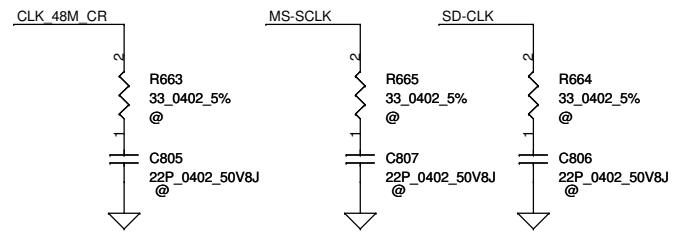
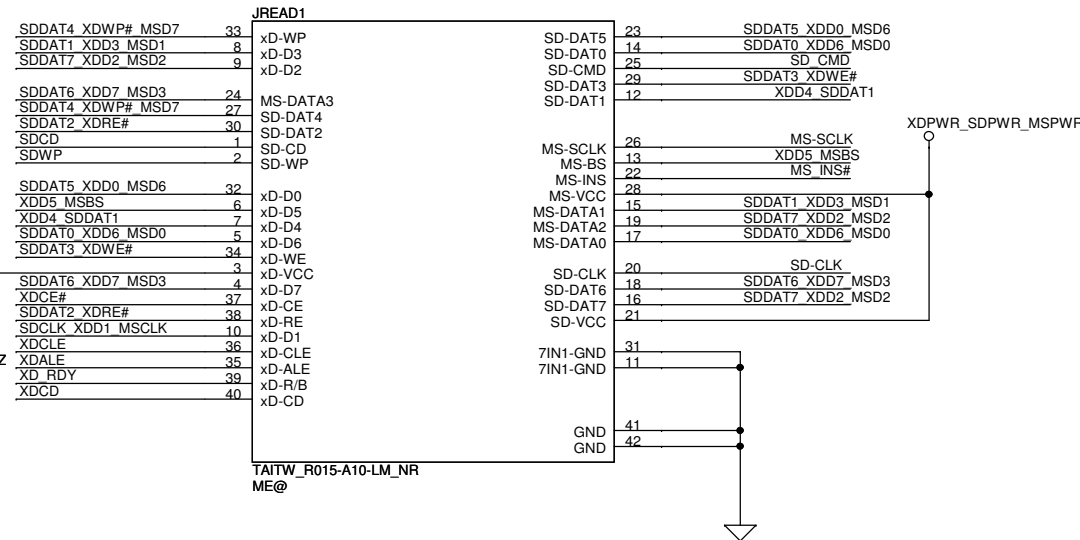
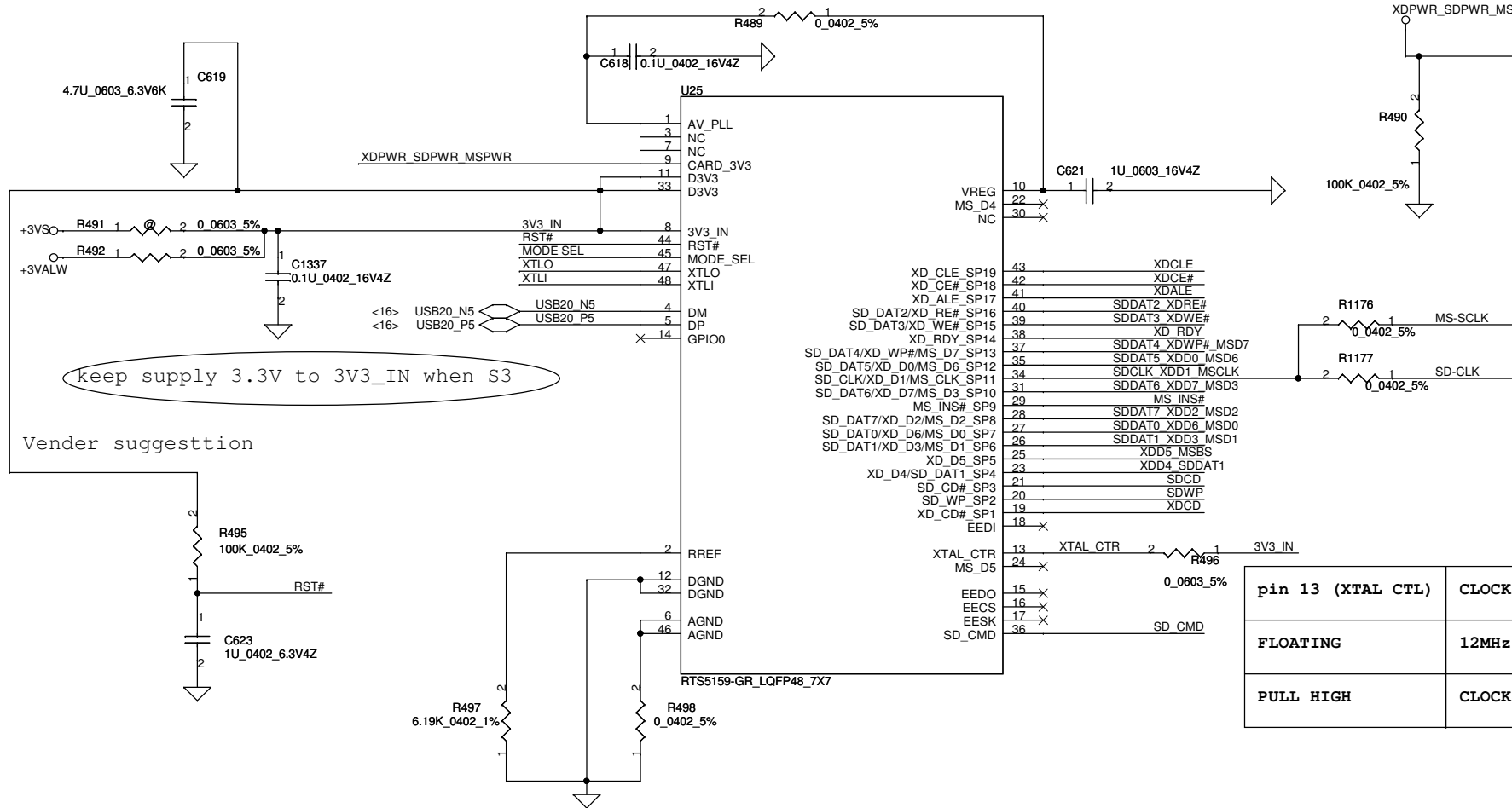


Layout Notice : Place as close chip as possible.

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2008/03/25		2008/04/		Title	
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				Document Number	
				NIWBA_LA5371P	
				Rev	
				0.1	
Date: Tuesday, March 24, 2009		Sheet		31 of 52	

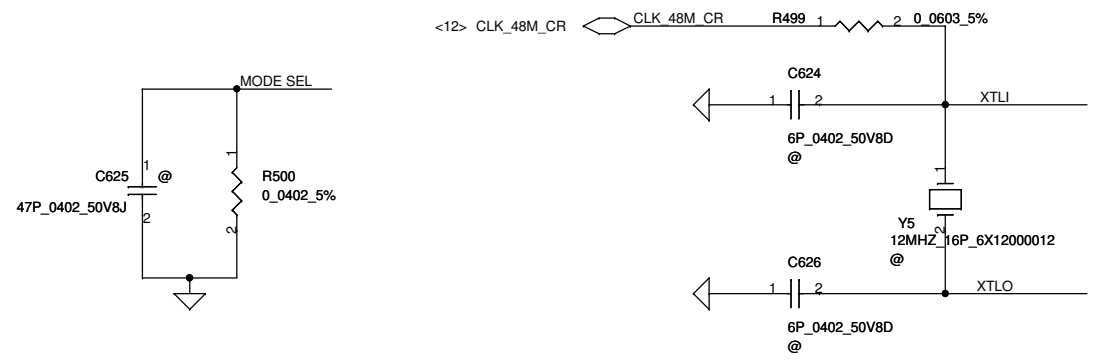


0513 : CARD_3V3 旁路電阻 100K change to 4.7u CAP==>預留
0521 : change C79 form 4.7u to 0.1u, add R47 100K ohm,
change C526 form 1u to 4.7u

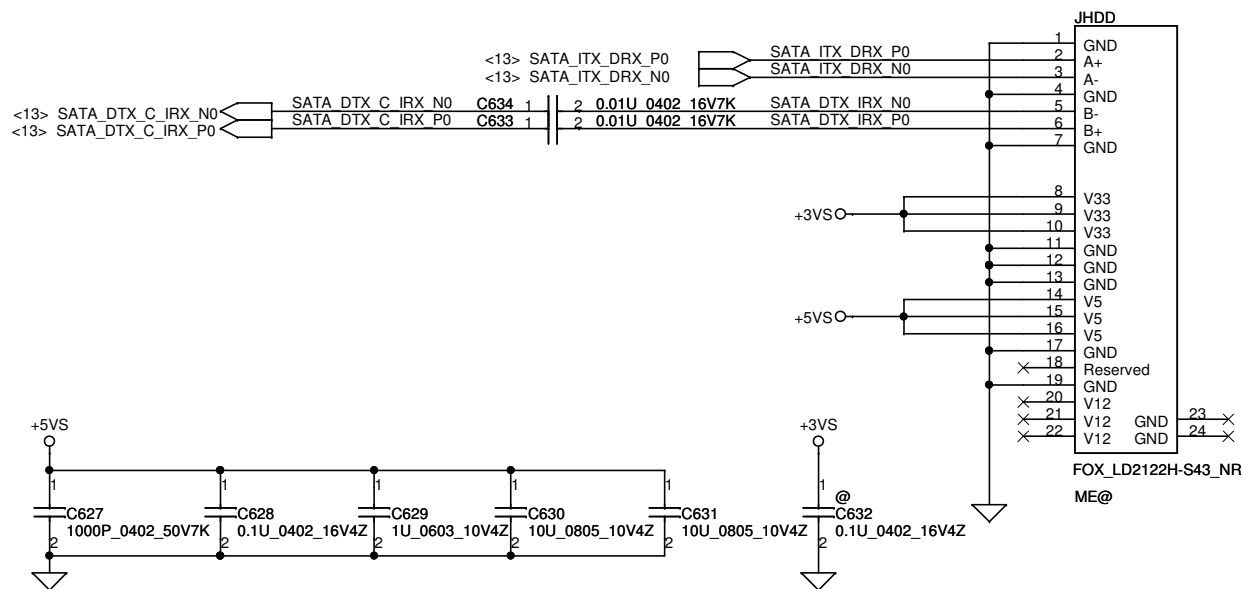


pin 13 (XTAL CTL)	CLOCK SOURCE	REMARK
FLOATING	12MHz CRYSTAL INPUT	
PULL HIGH	CLOCK GENERATOR'S 48MHZ INPUT	INPUT TO PIN48

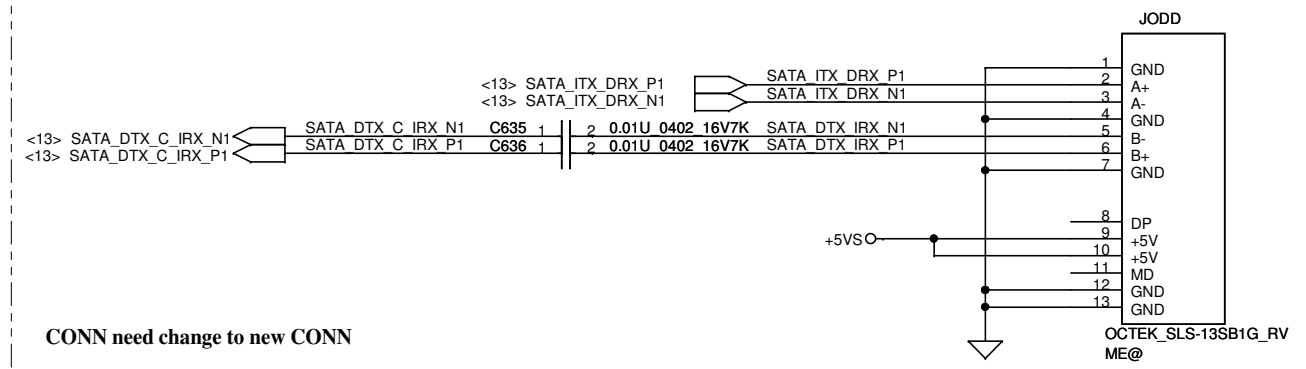
MCLK and SDCLK 該二電阻是預留給EMI solution使用, (但請靠近RTS5158E側).
將SD_DAT1 連接到RTS5158E的pin23



SATA HDD Conn.

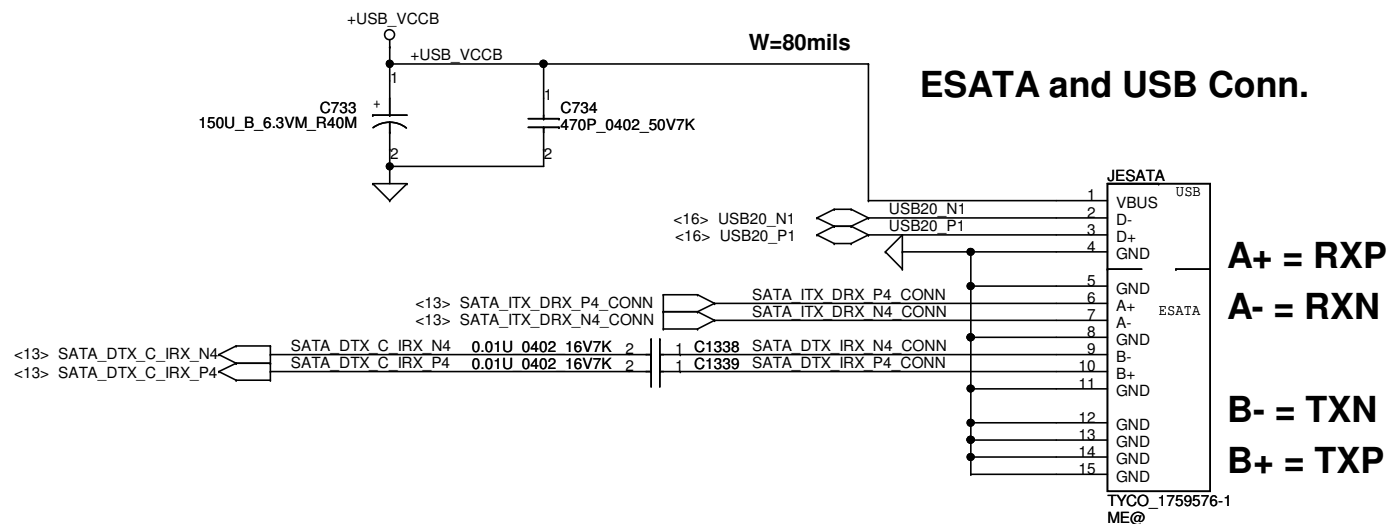


SATA ODD Conn.



CONN need change to new CONN

ESATA and USB Conn.



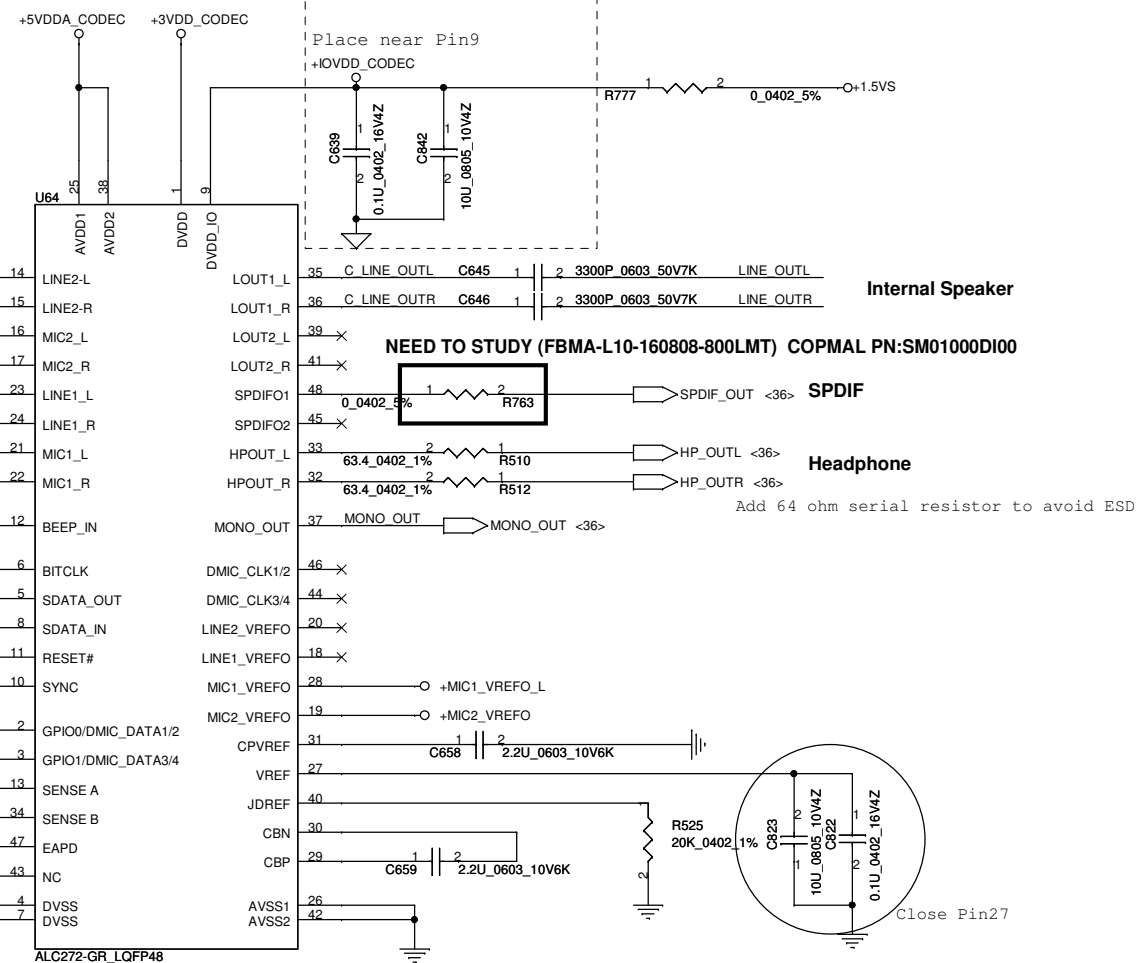
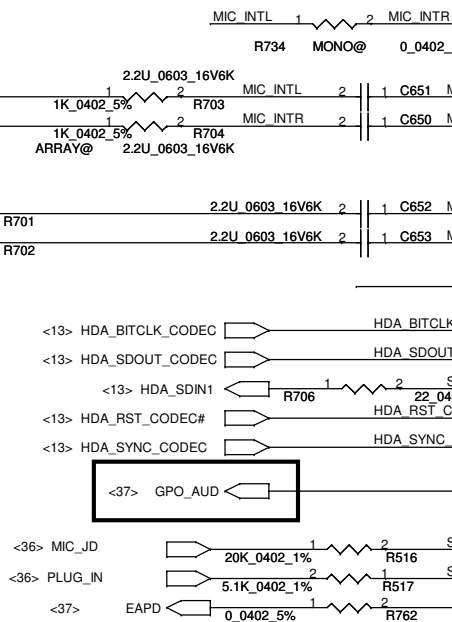
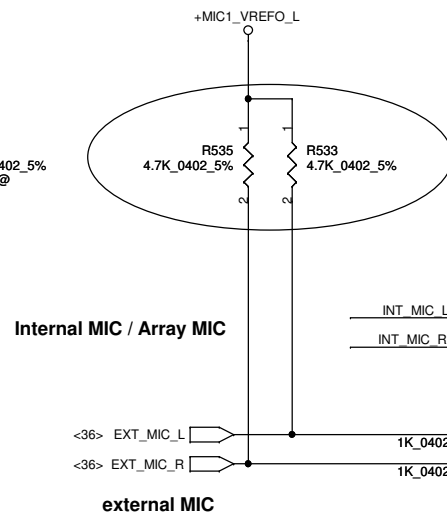
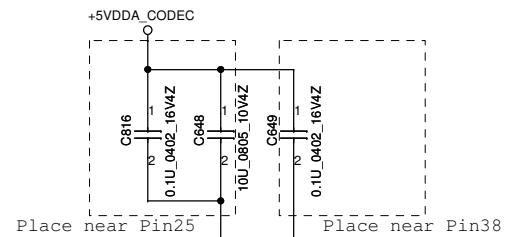
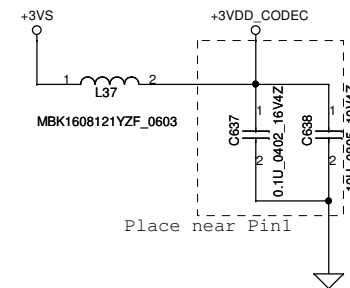
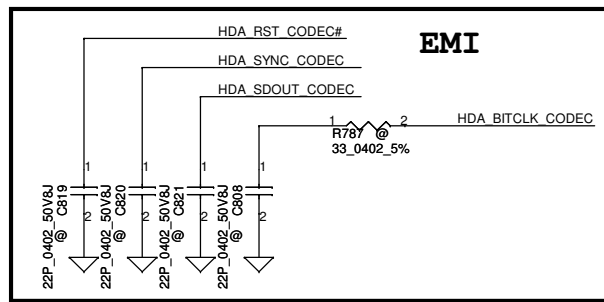
A+ = RXP

A- = RXN

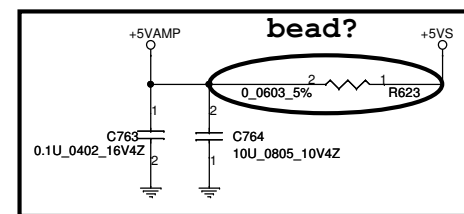
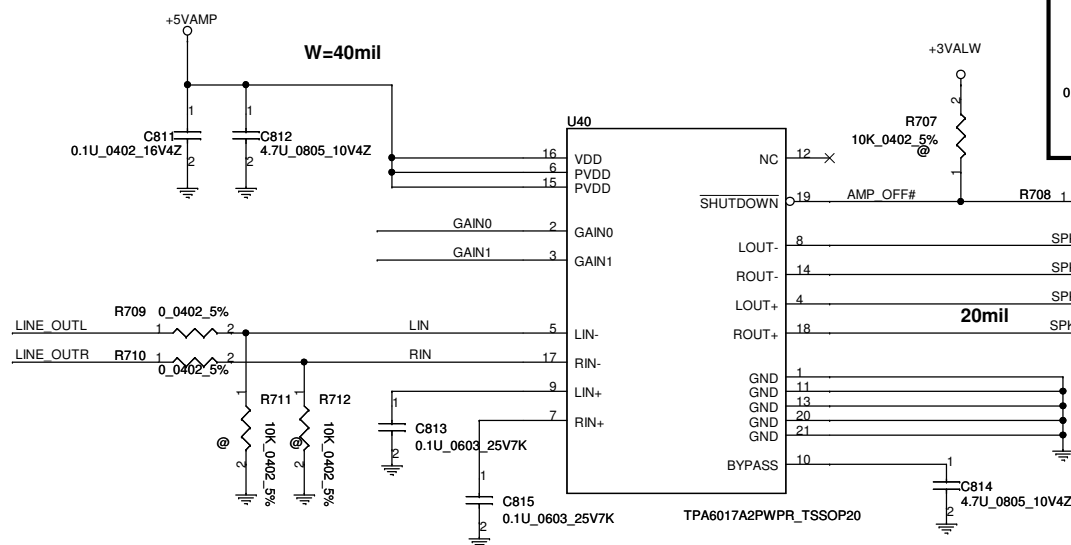
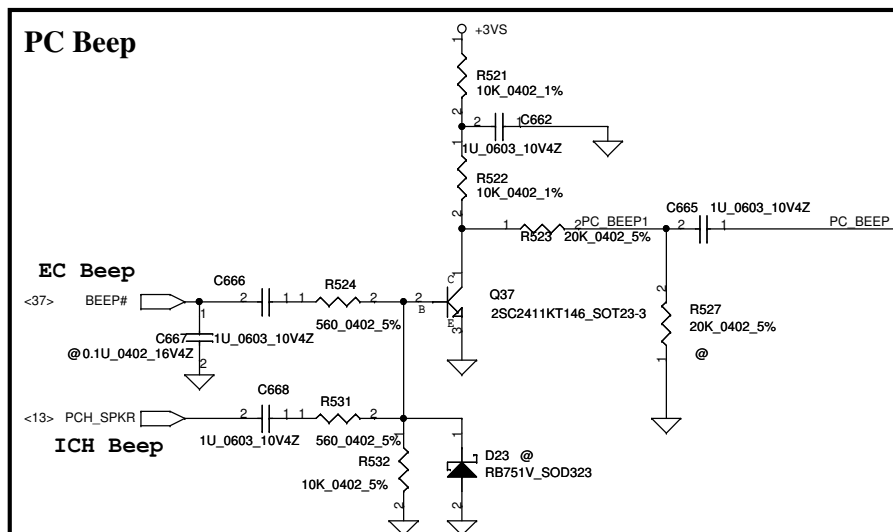
B- = TXN

B+ = TXP

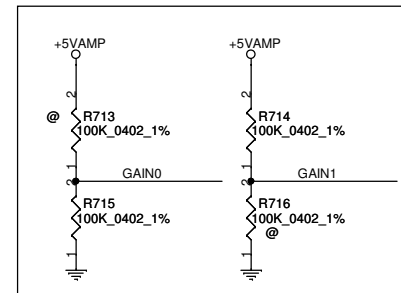
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	HDD & ODD Connector	
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				NIWBA_LA5371P	
Date: Tuesday, March 24, 2009				Sheet	34 of 52



```
MIC Sense
R516 place near pin13
Capless HP Sense
R517 place near pin34
```



GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



EMI 20080826

20mil

JSPK1

Signal	Pin	Label	Pin	Label
WOOFER-	L43	1	FBMA-L10-160808-121LMT	2P
WOOFER+	L44	1	FBMA-L10-160808-121LMT	2P
SPK_R1-	L45	1	FBMA-L10-160808-121LMT	2P
SPK_R2+	L46	1	FBMA-L10-160808-121LMT	2P
SPK_L1-	L47	1	FBMA-L10-160808-121LMT	2P
SPK_L2+	L48	1	FBMA-L10-160808-121LMT	2P

WO-

WO+

SPK_R1- CONN

SPK_R2+ CONN

SPK_L1- CONN

SPK_L2+ CONN

1

2

3

4

5

6

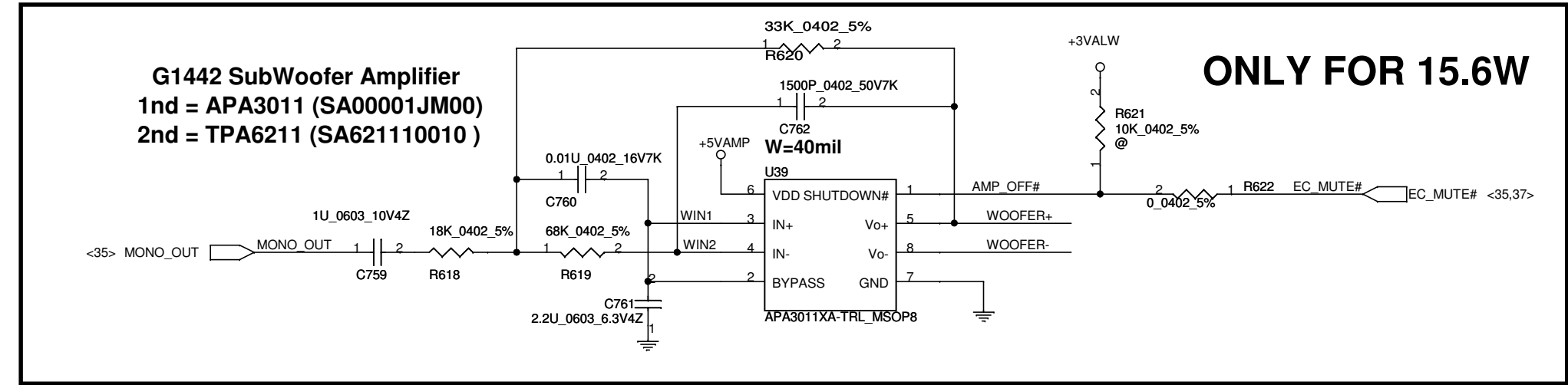
5 G1

6 G2

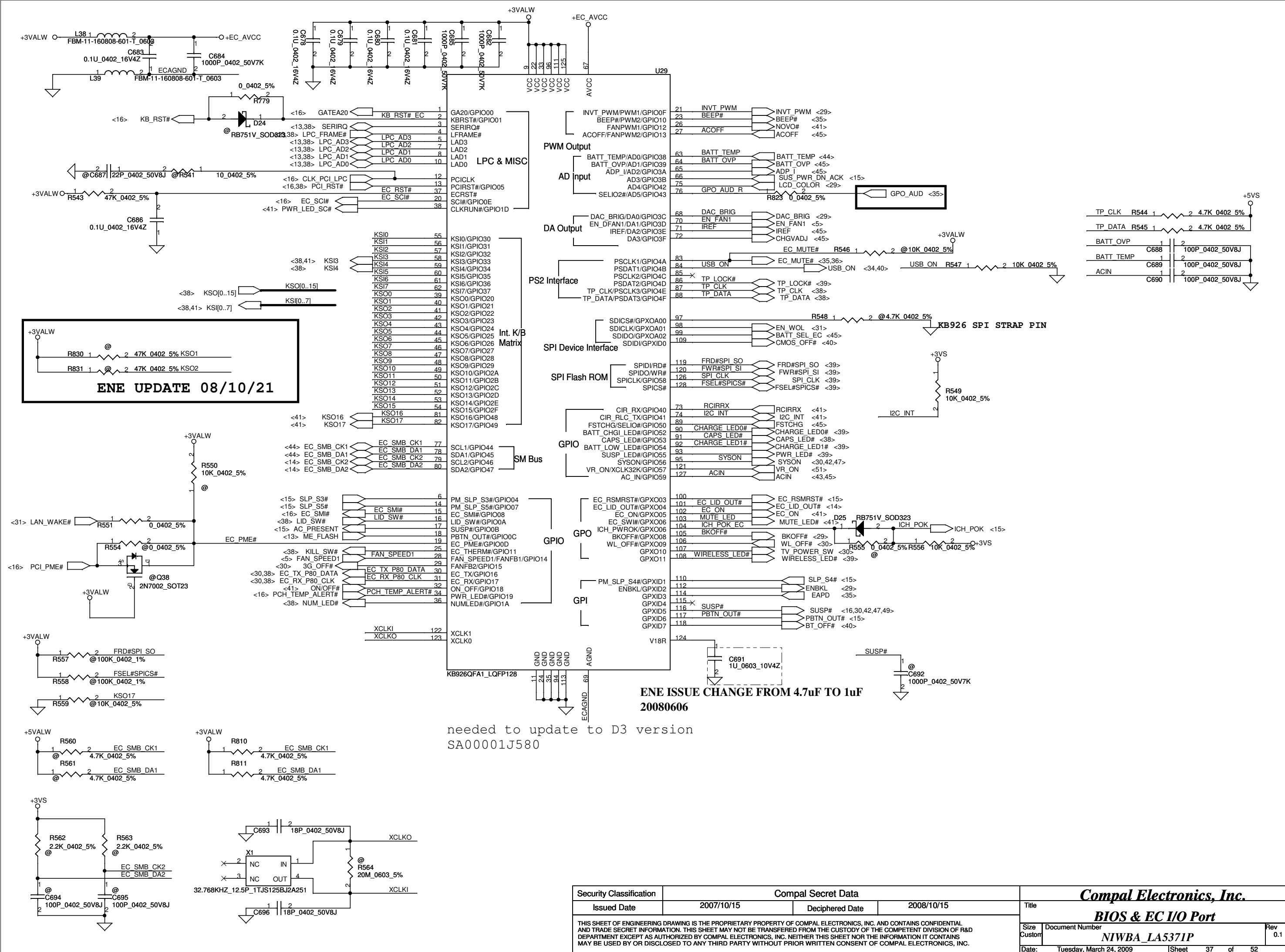
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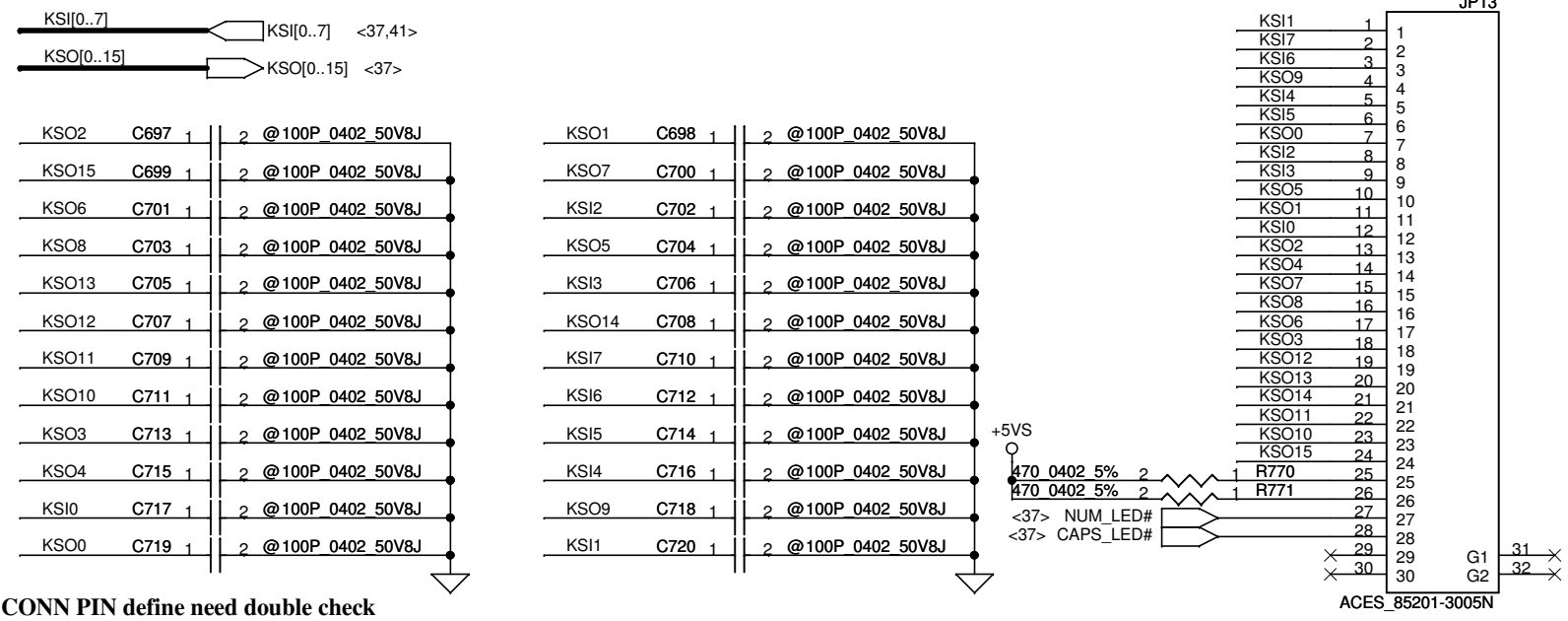
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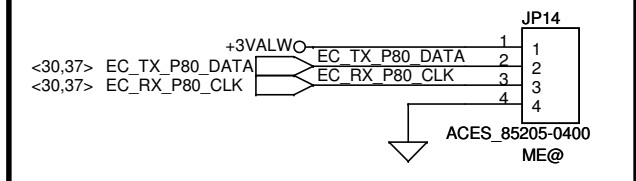
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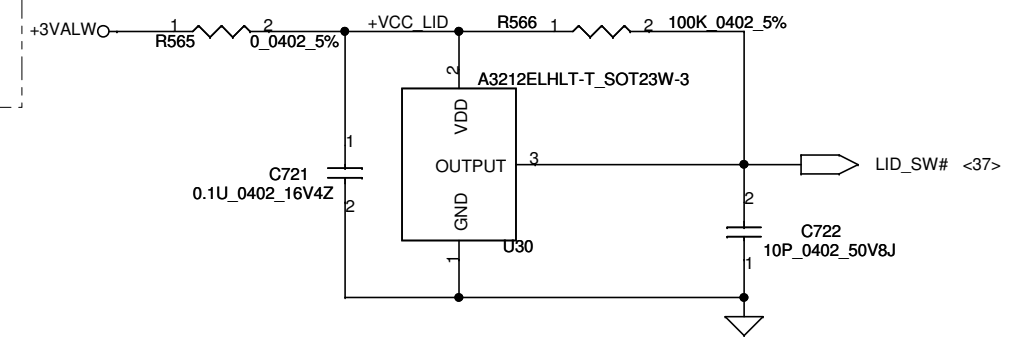
INT_KBD Conn.



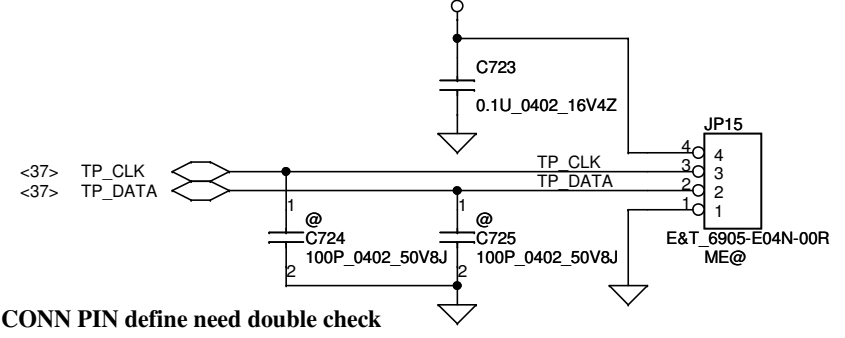
EC DEBUG PORT



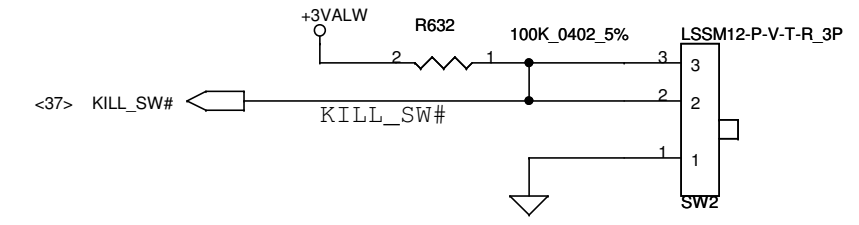
Lid Switch



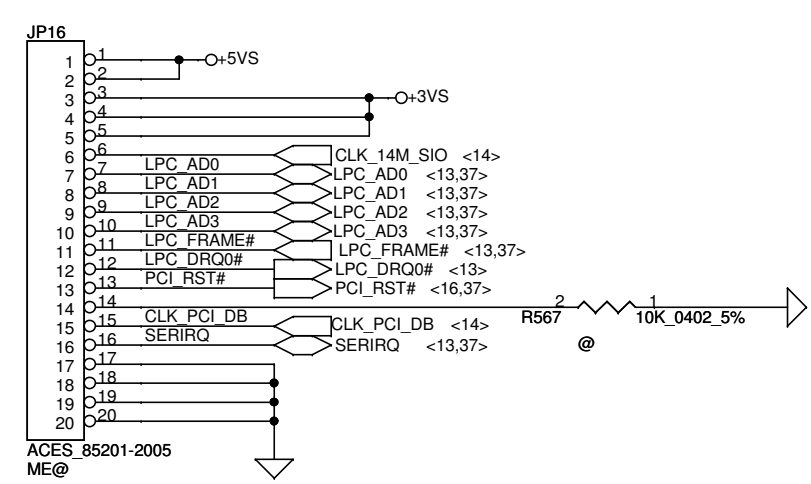
To TP/B Conn.



Kill Switch

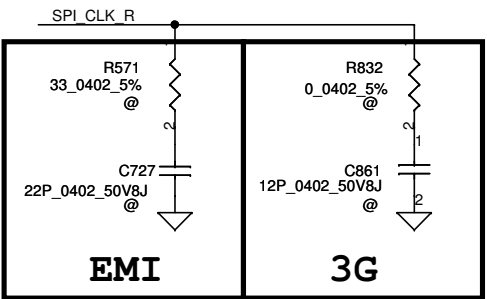
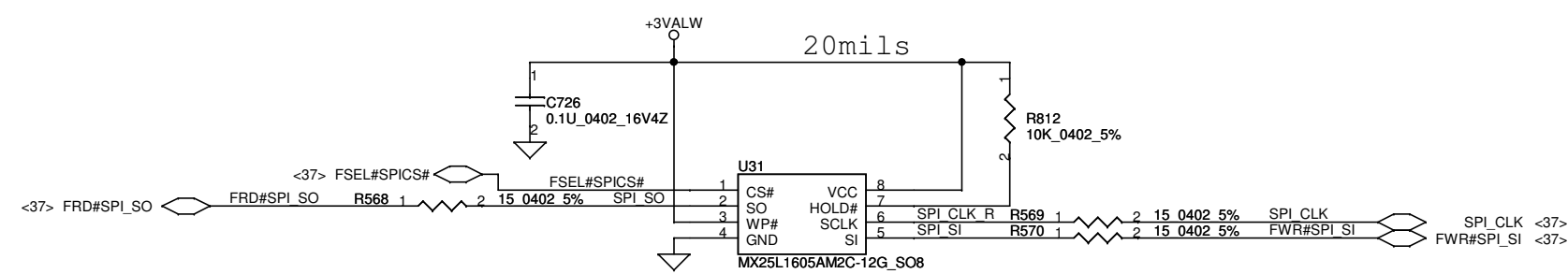


FOR LPC SIO DEBUG PORT



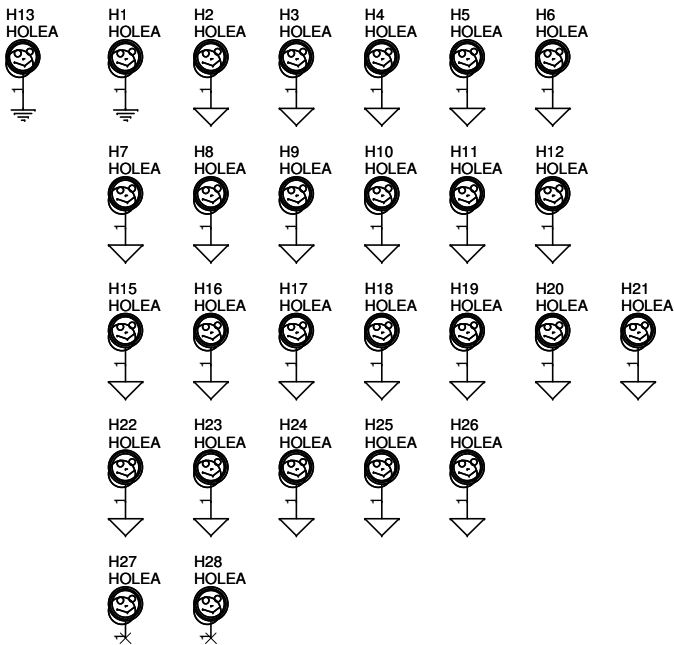
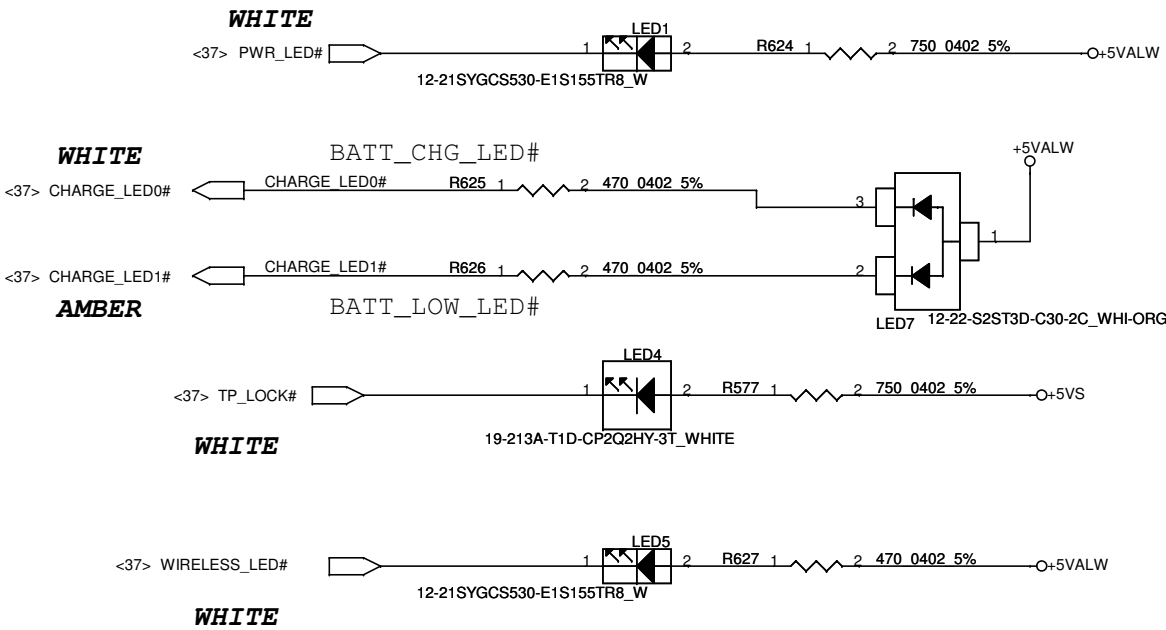
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						Size		Document Number		Rev	
				B		KIWB1/B2_LA4601P		0.1			
Date:		Tuesday, March 24, 2009				Sheet		38 of 52			
		3				2		1			

FOR EC 16M SPI ROM

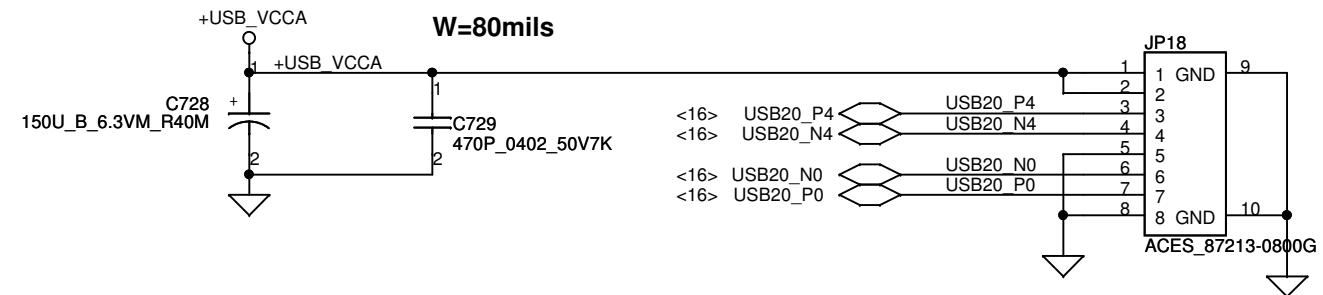
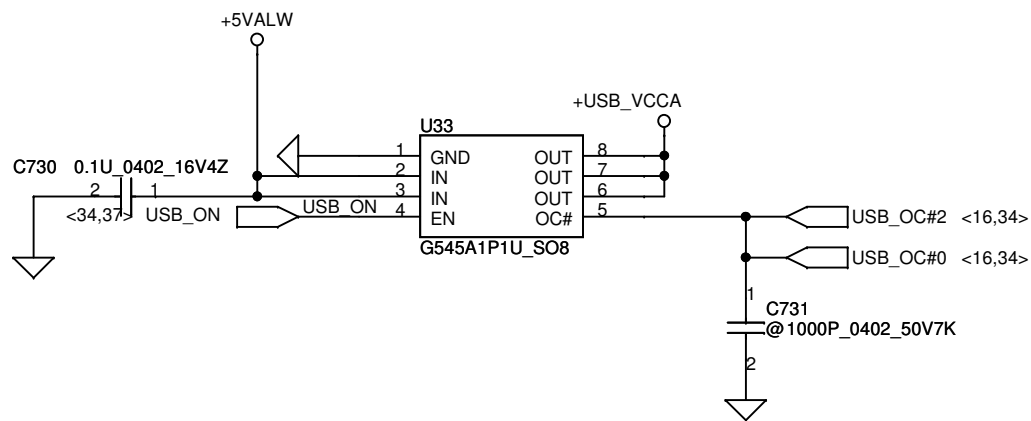


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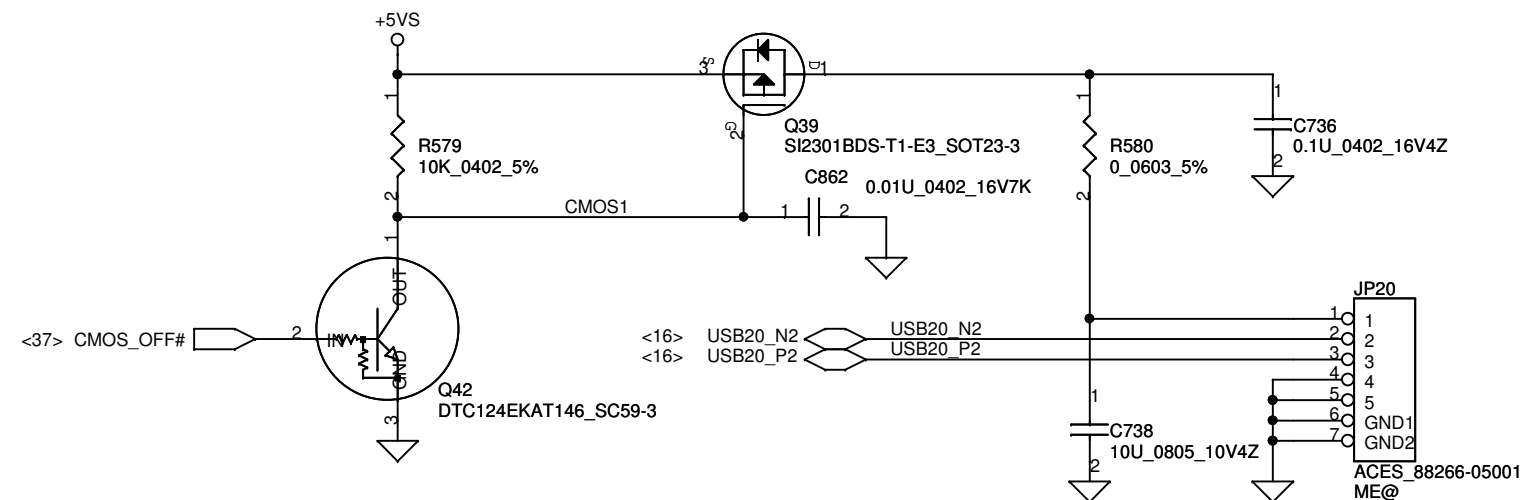
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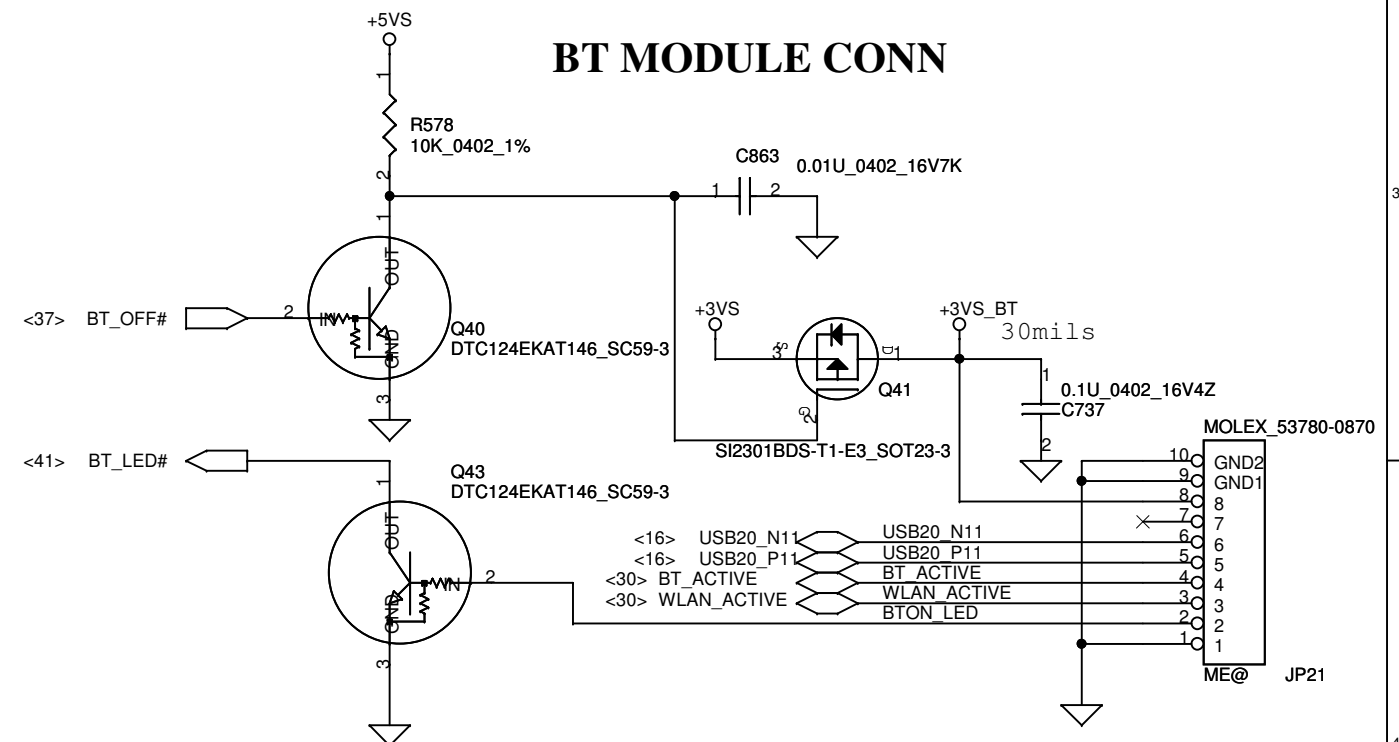
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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				Size B	Rev 0.1
				Document Number	NIWBA_LA5371P
				Date:	Tuesday, March 24, 2009
				Sheet	39 of 52



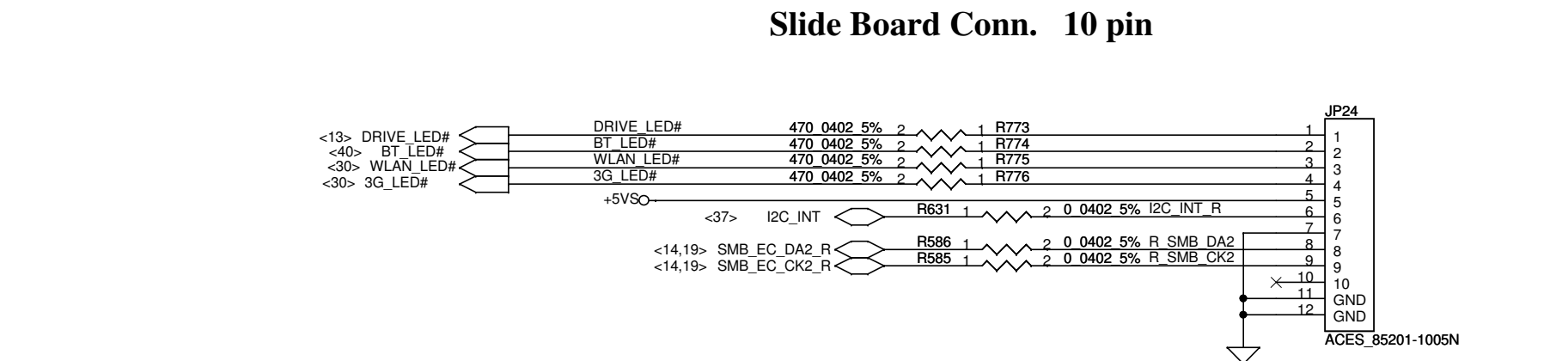
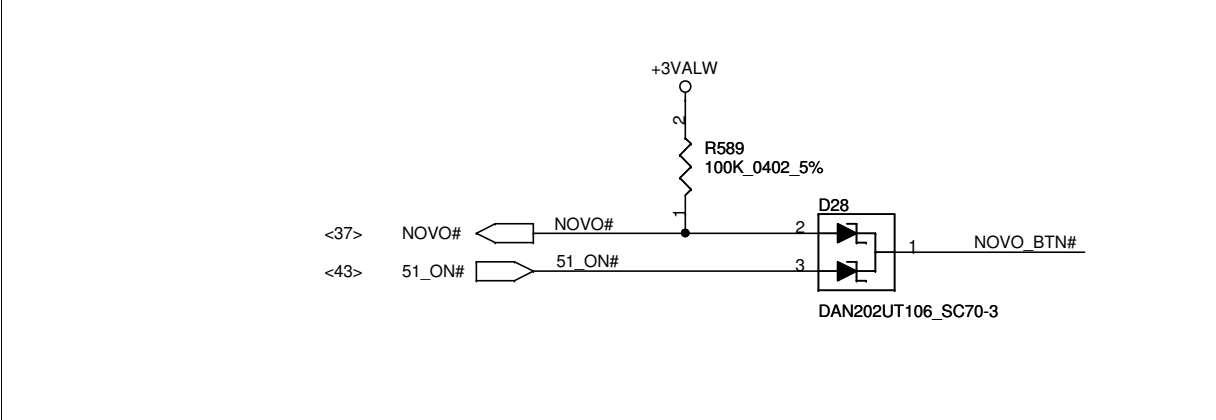
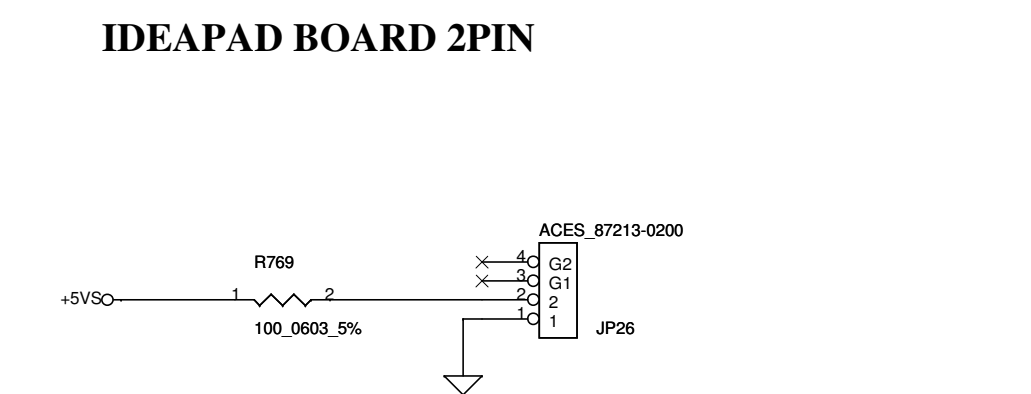
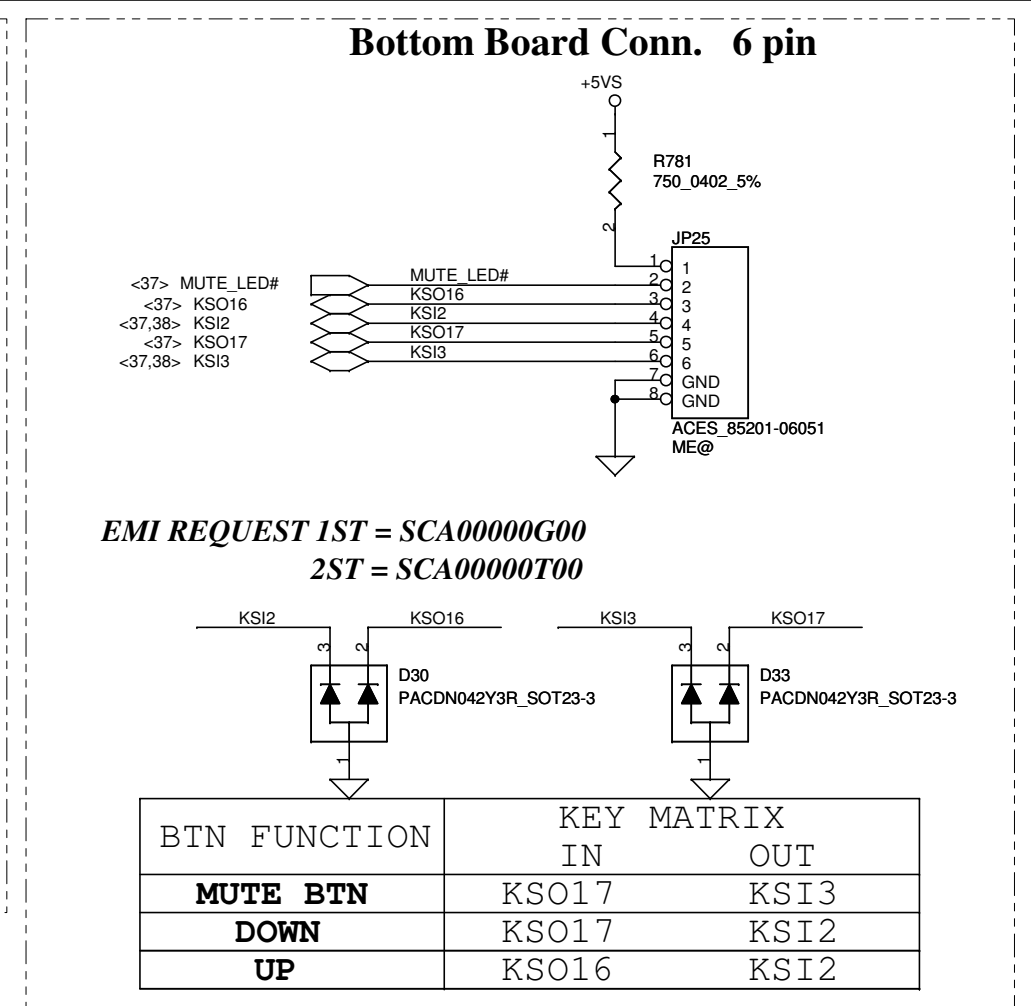
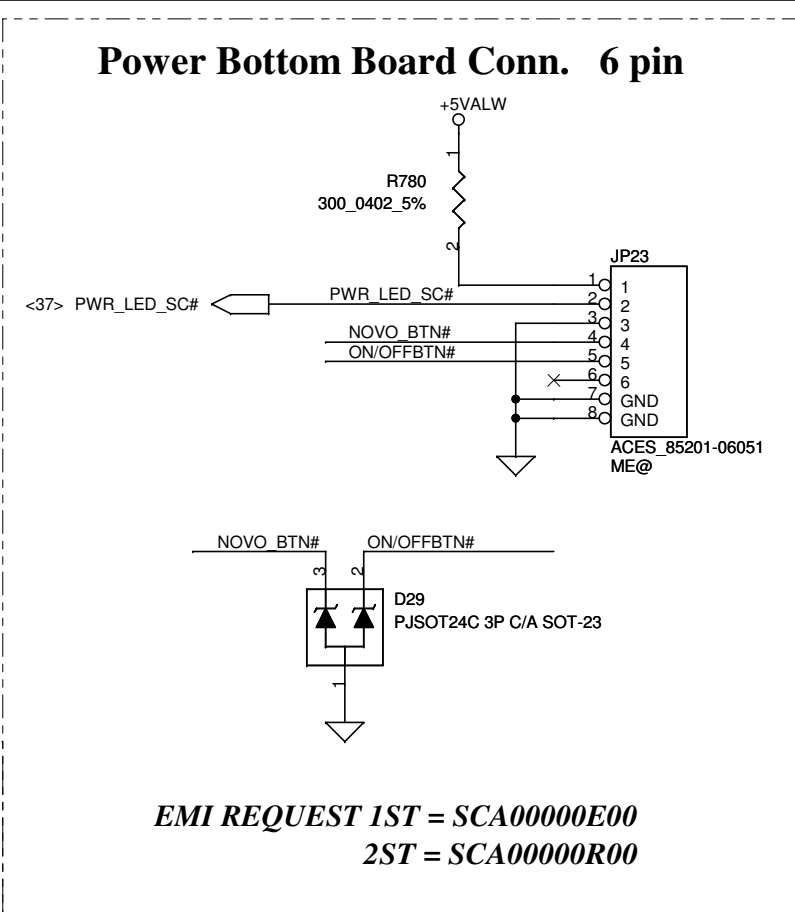
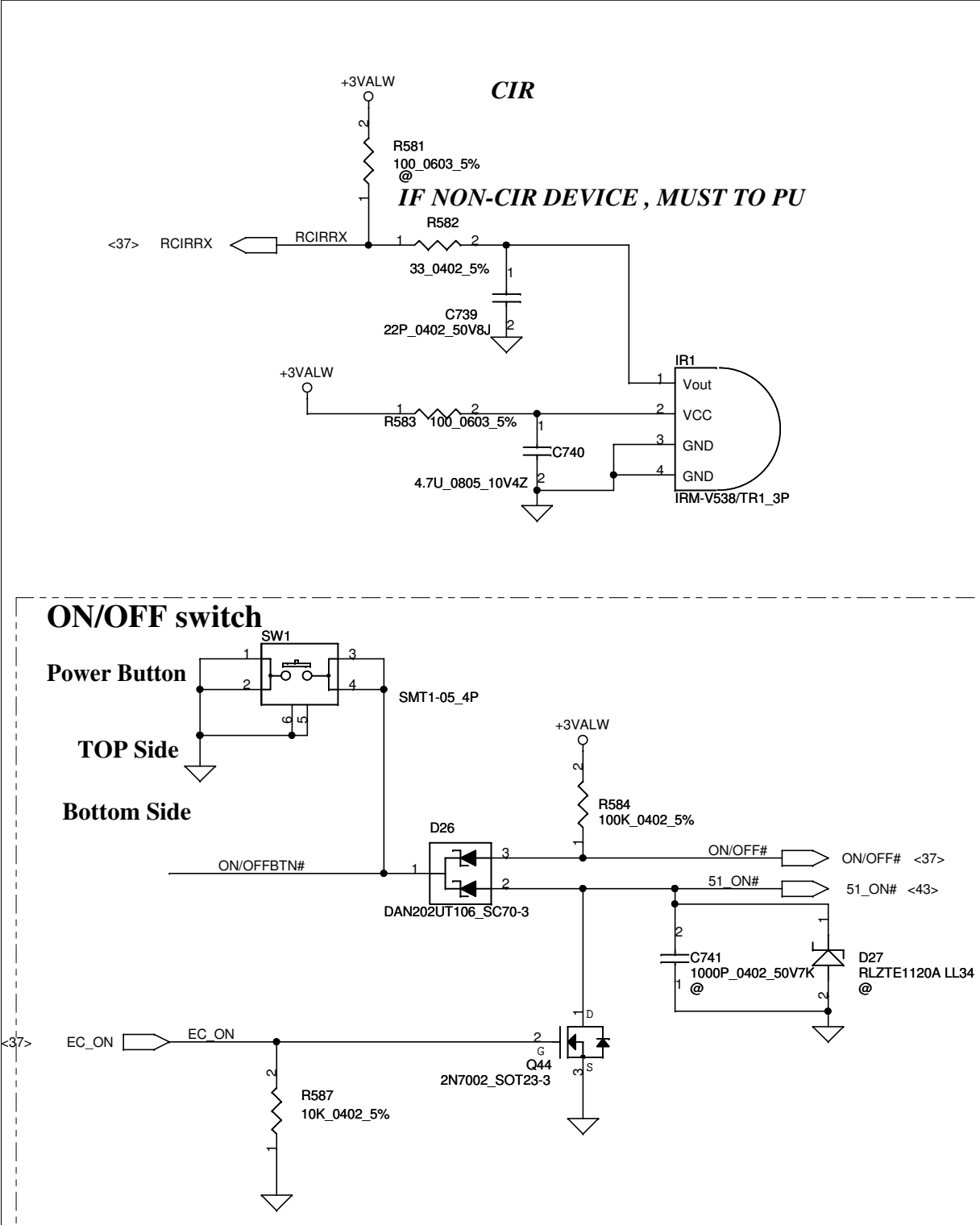
CMOS Camera Conn



BT MODULE CONN

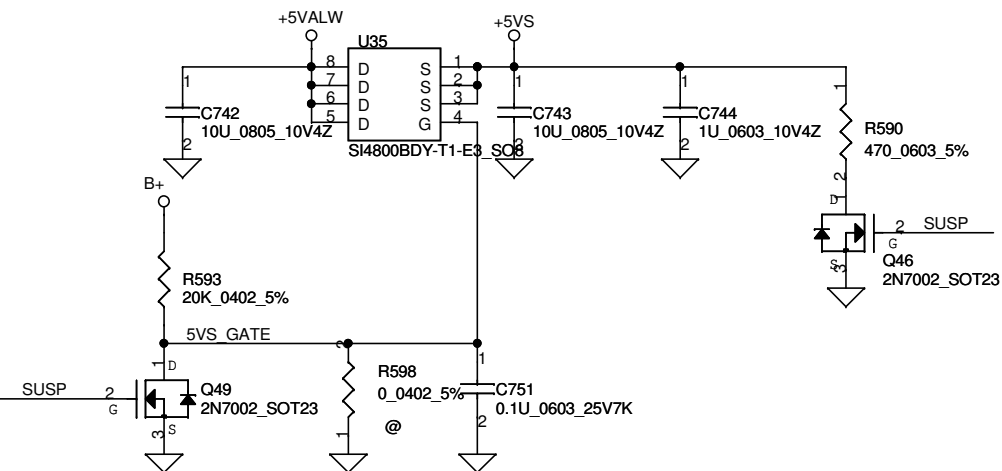


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		NIWBA_LA5371P			0.1
Date:		Tuesday, March 24, 2009		Sheet	40 of 52

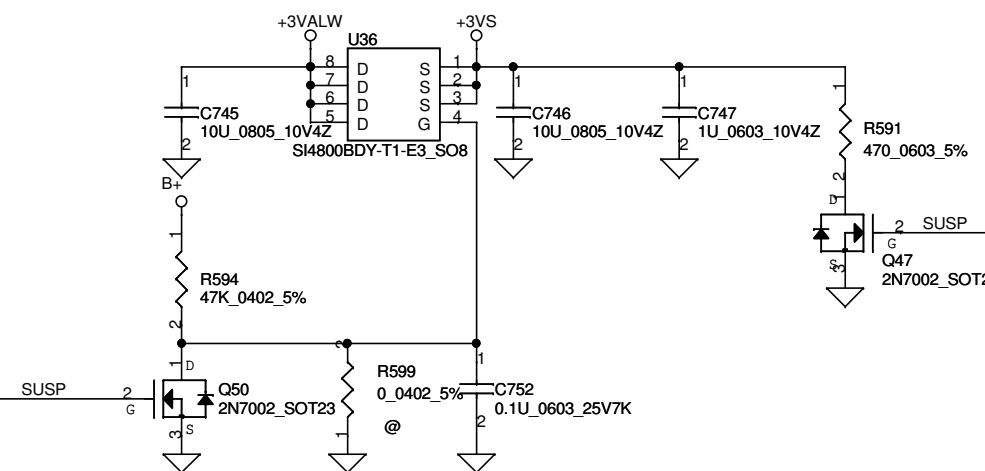


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				Size Custom	Rev 0.1
				Date: Tuesday, March 24, 2009	Sheet 41 of 52

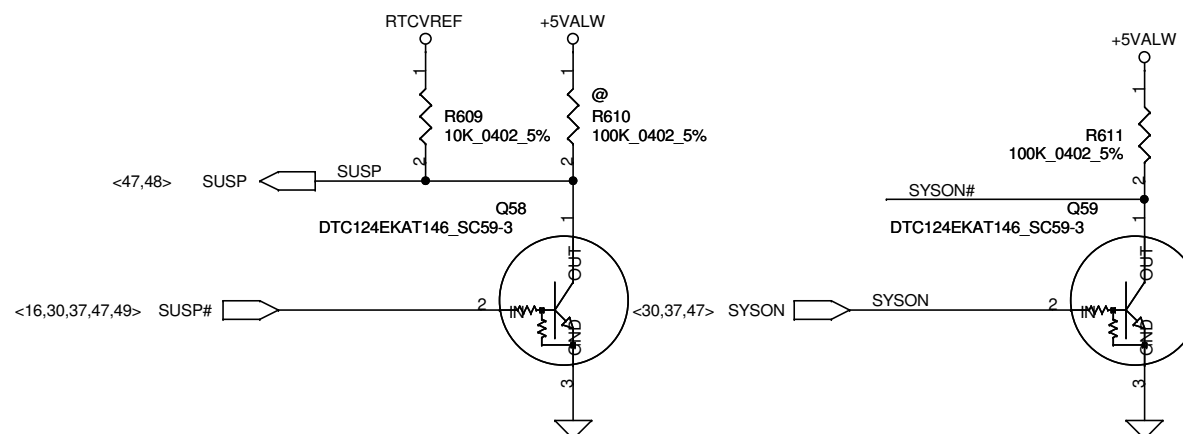
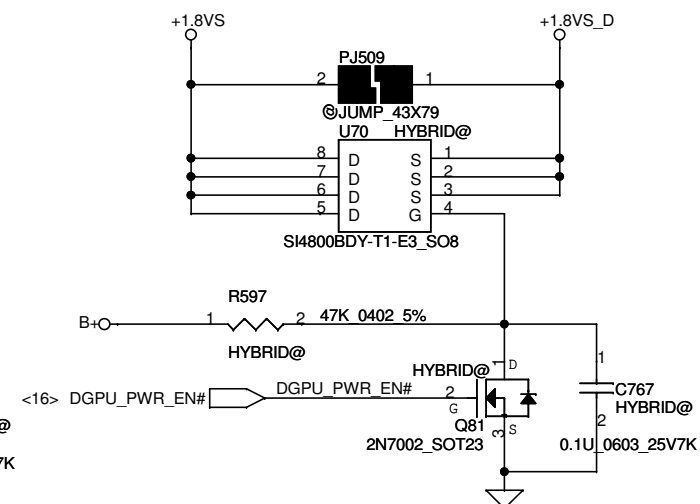
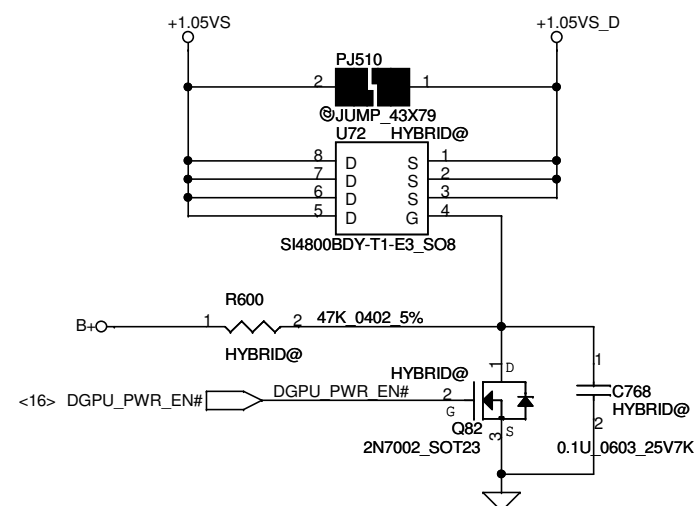
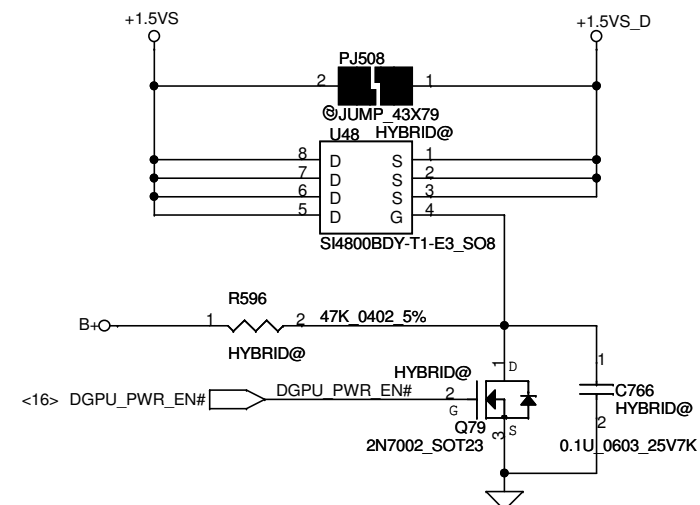
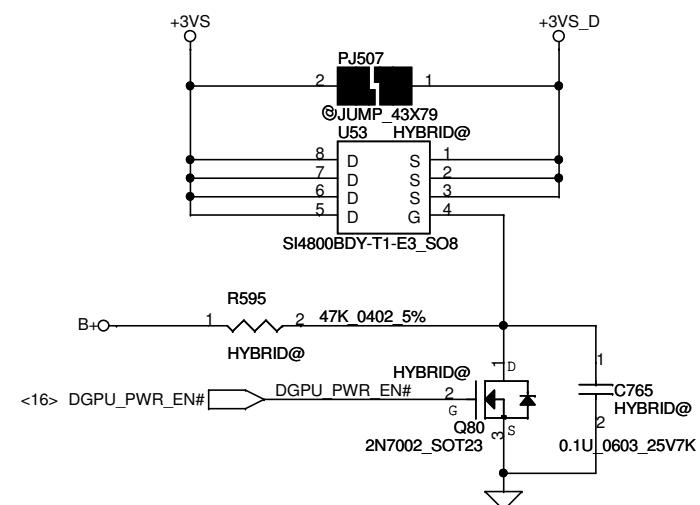
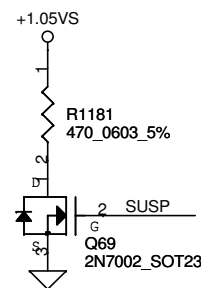
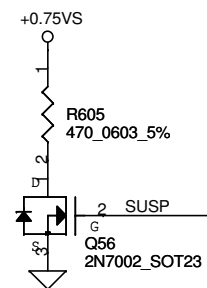
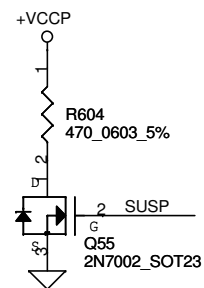
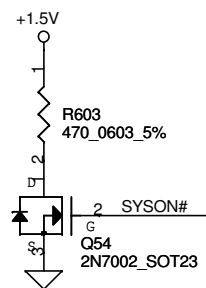
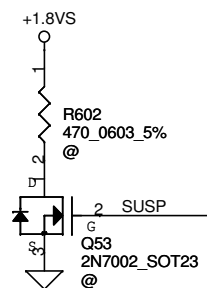
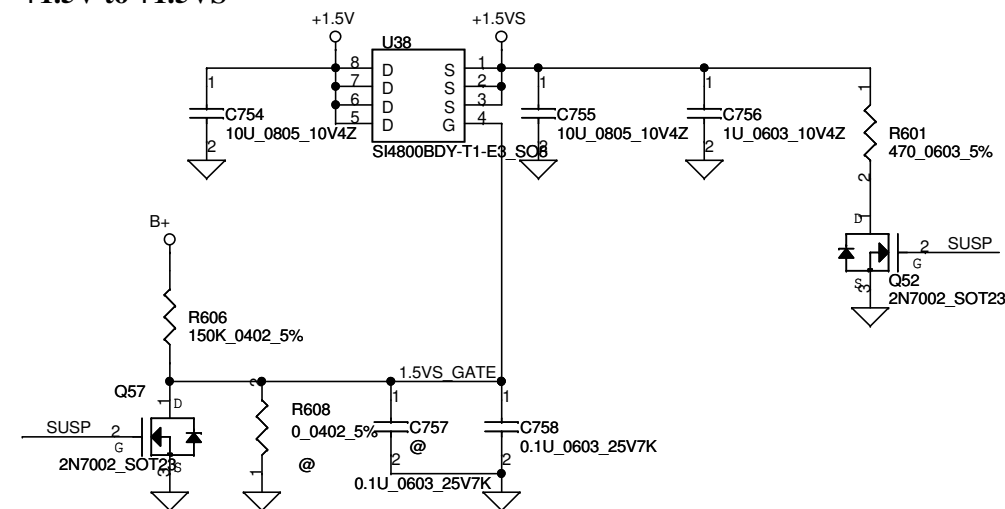
+5VALW TO +5VS



+3VALW TO +3VS

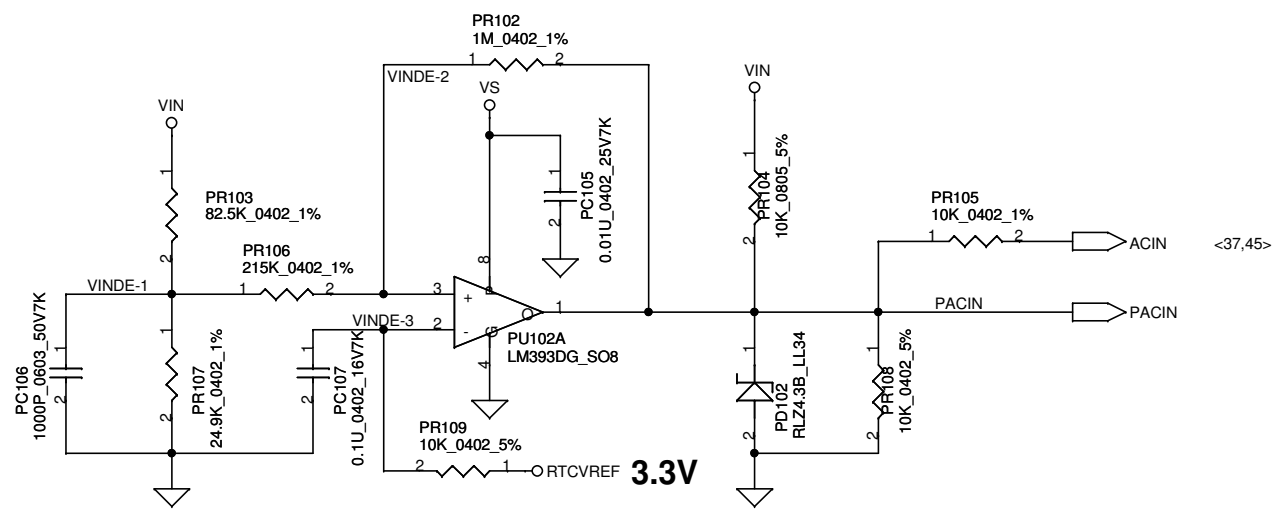
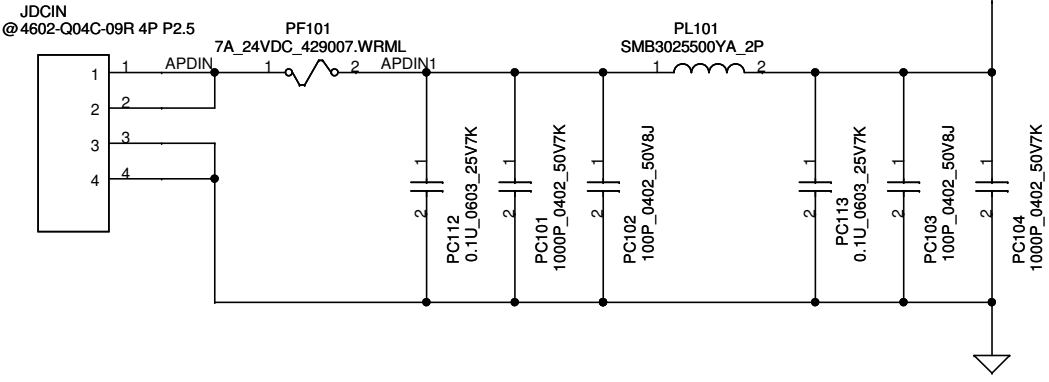


+1.5V to +1.5VS



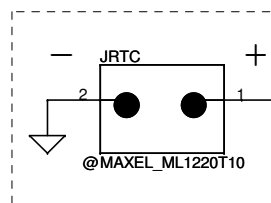
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				Size Custom	Document Number <i>NIWBA_LA5371P</i>			Rev 0.1	
				Date:	Tuesday, March 24, 2009		Sheet	42	of

DC030006J00

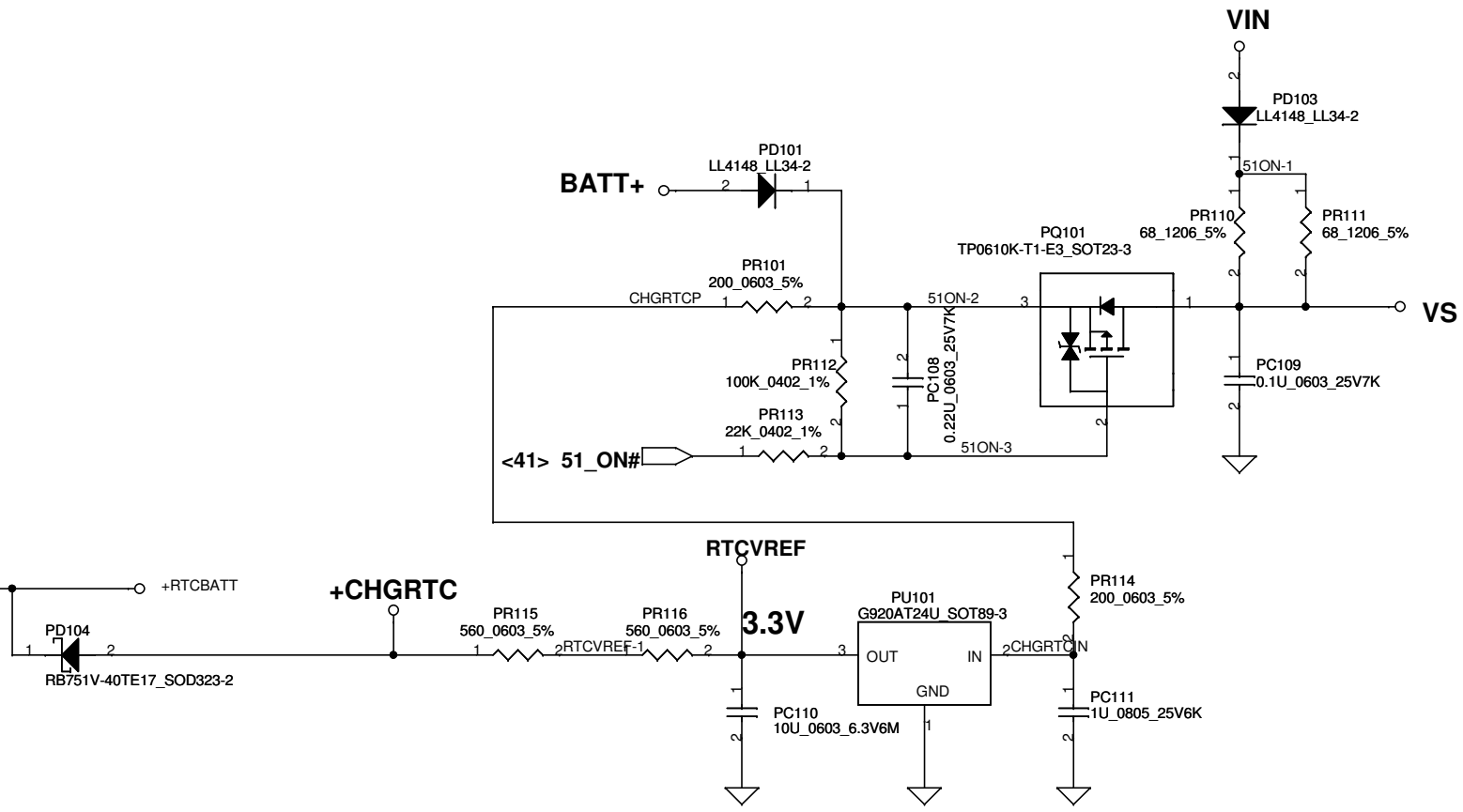


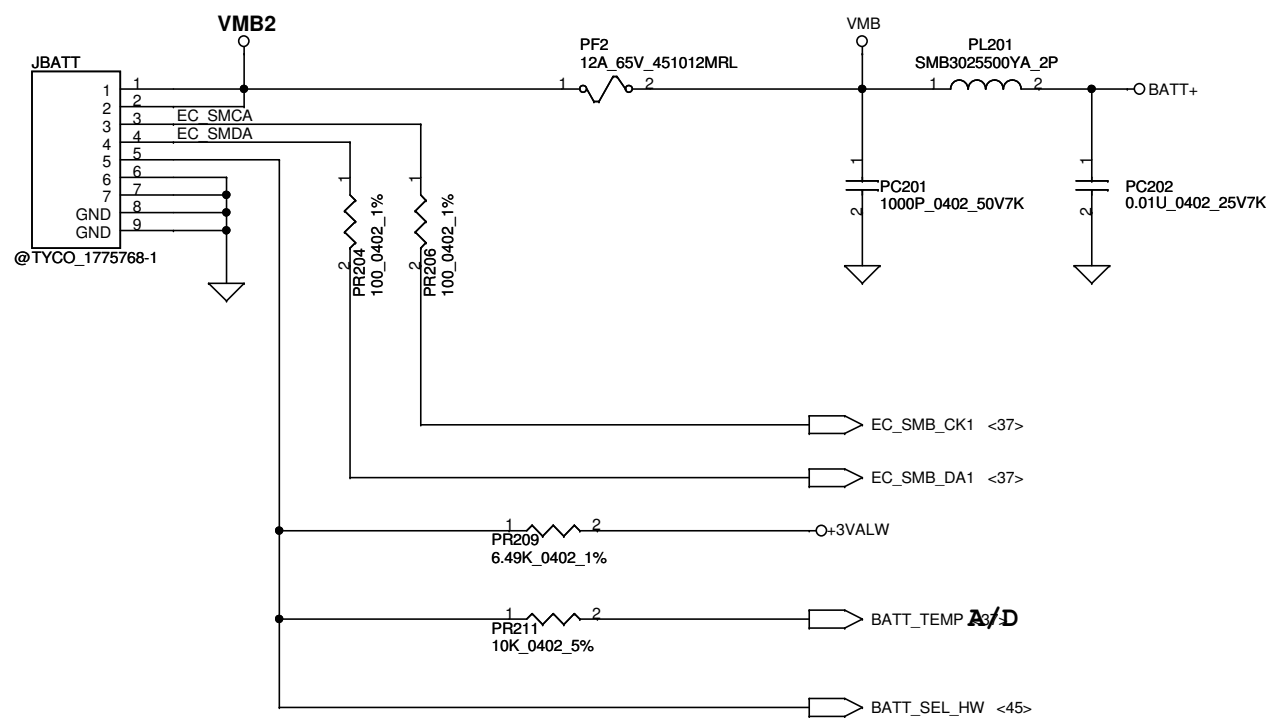
Vin Detector			
High	18.135	17.566	17.011
Low	14.866	14.355	14.063

RTC Battery

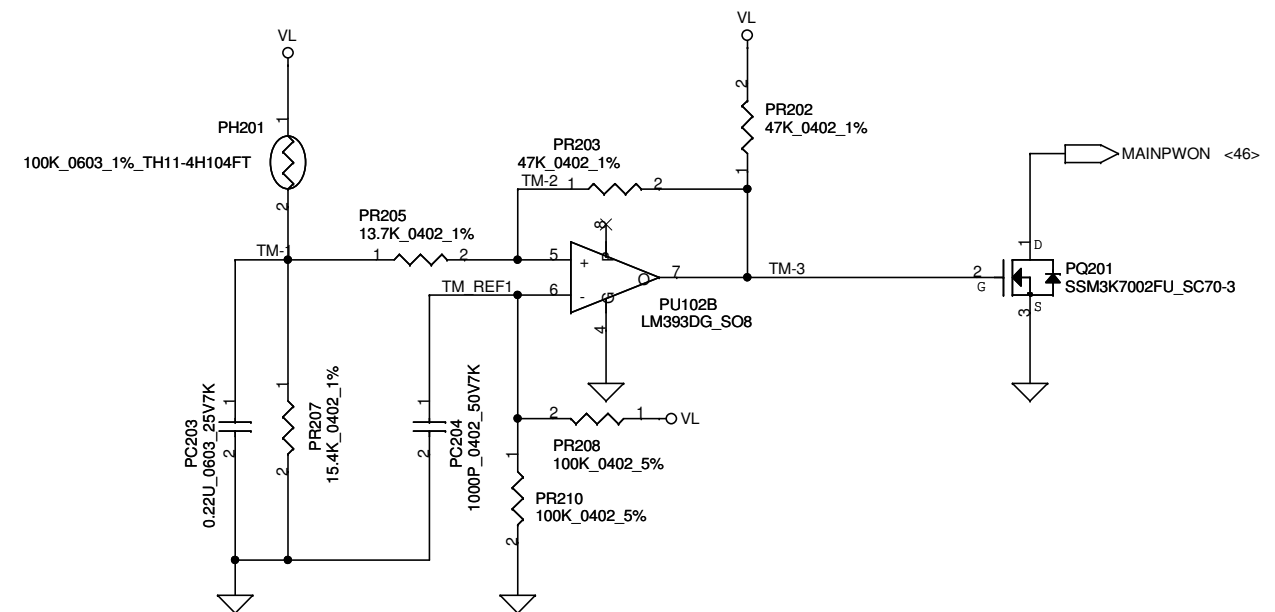


SP093MX0000

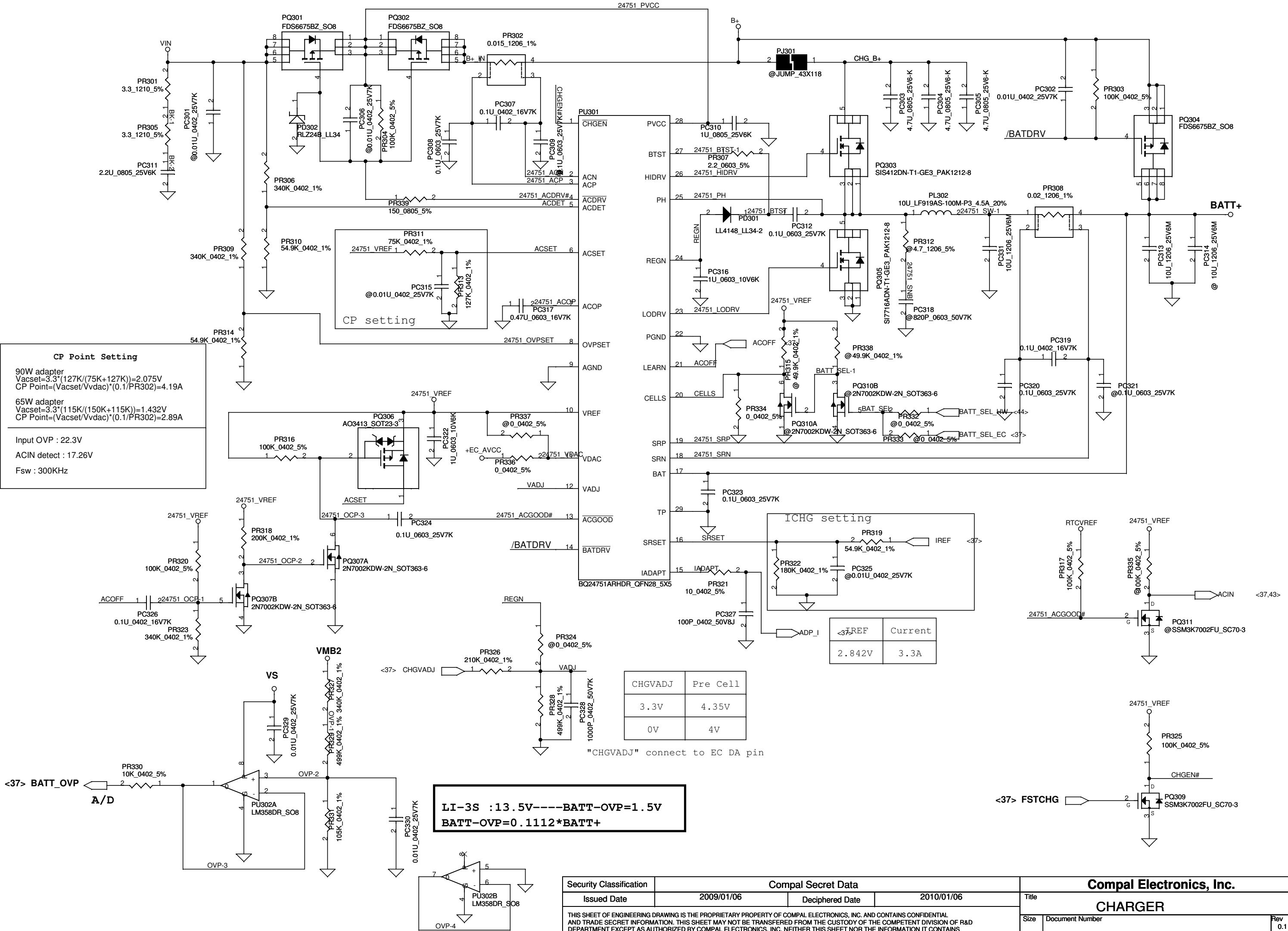


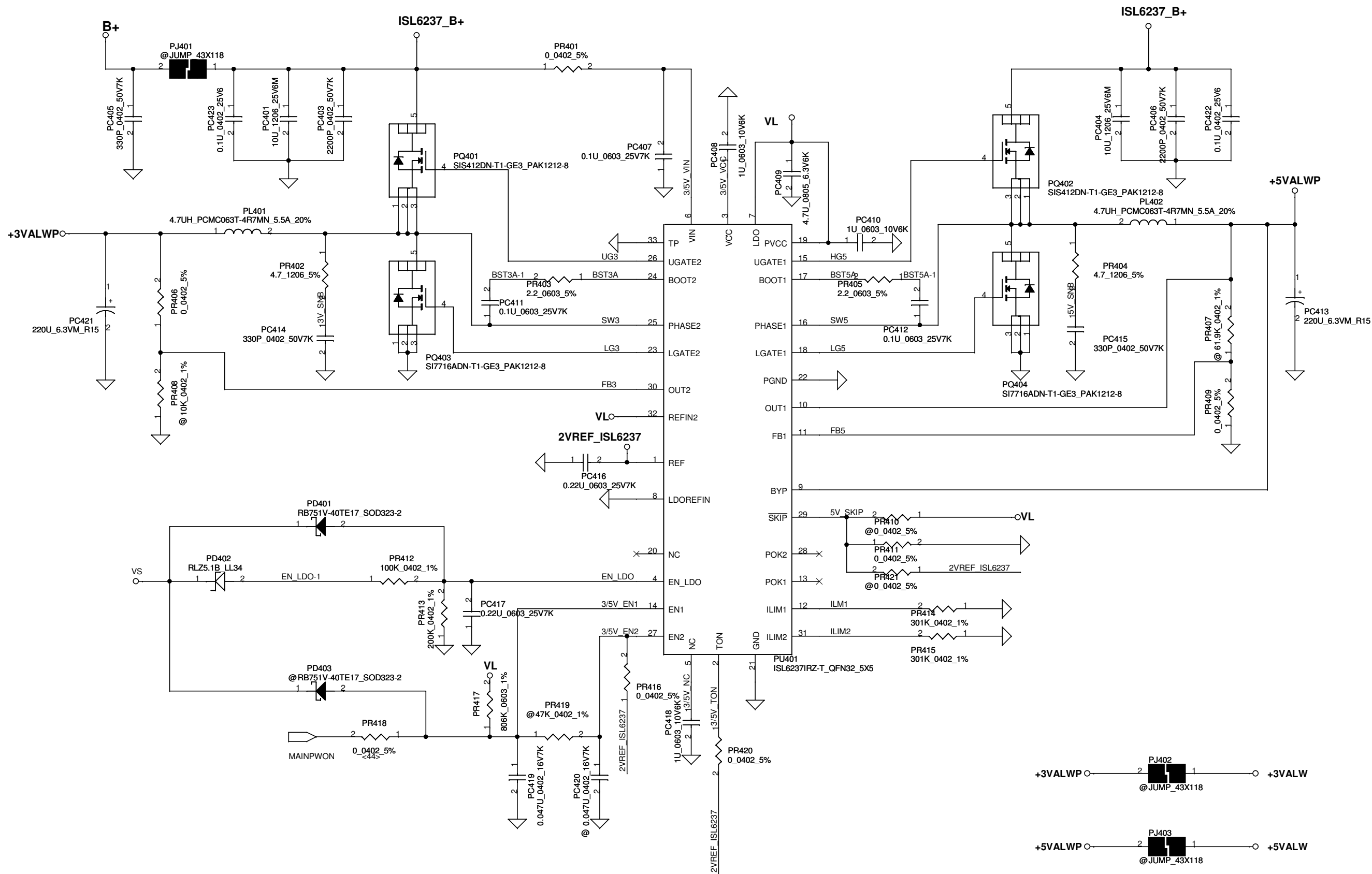


PH1 under CPU botten side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C

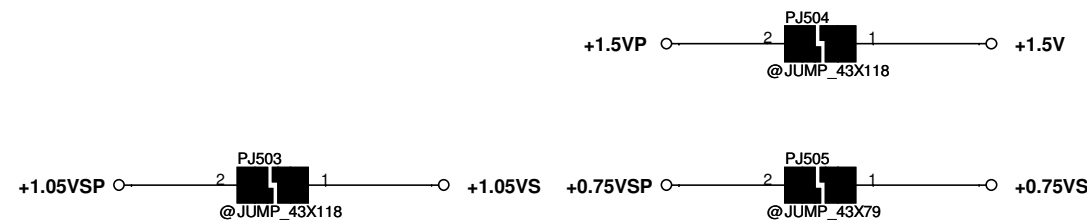
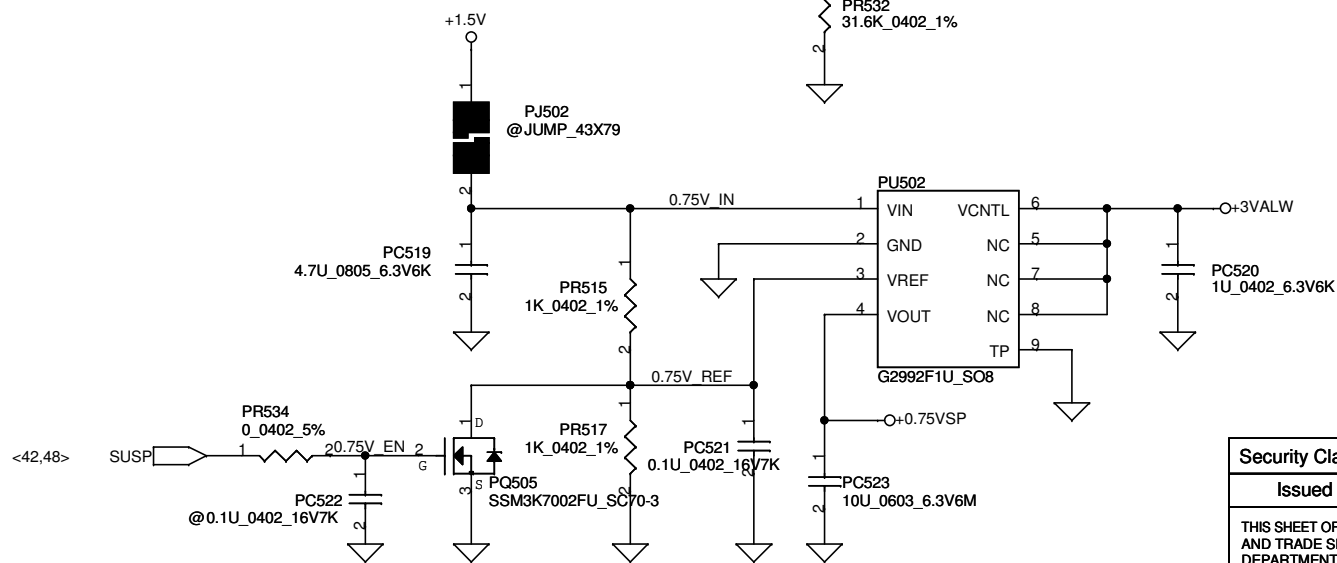
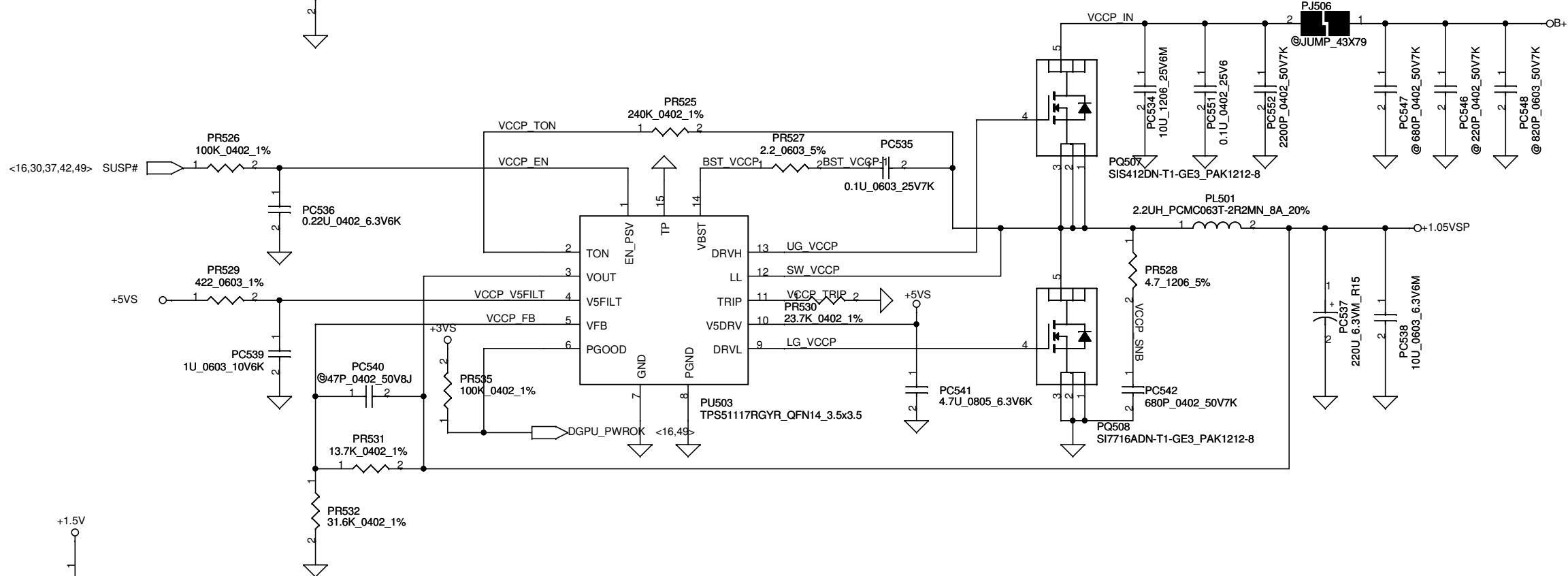
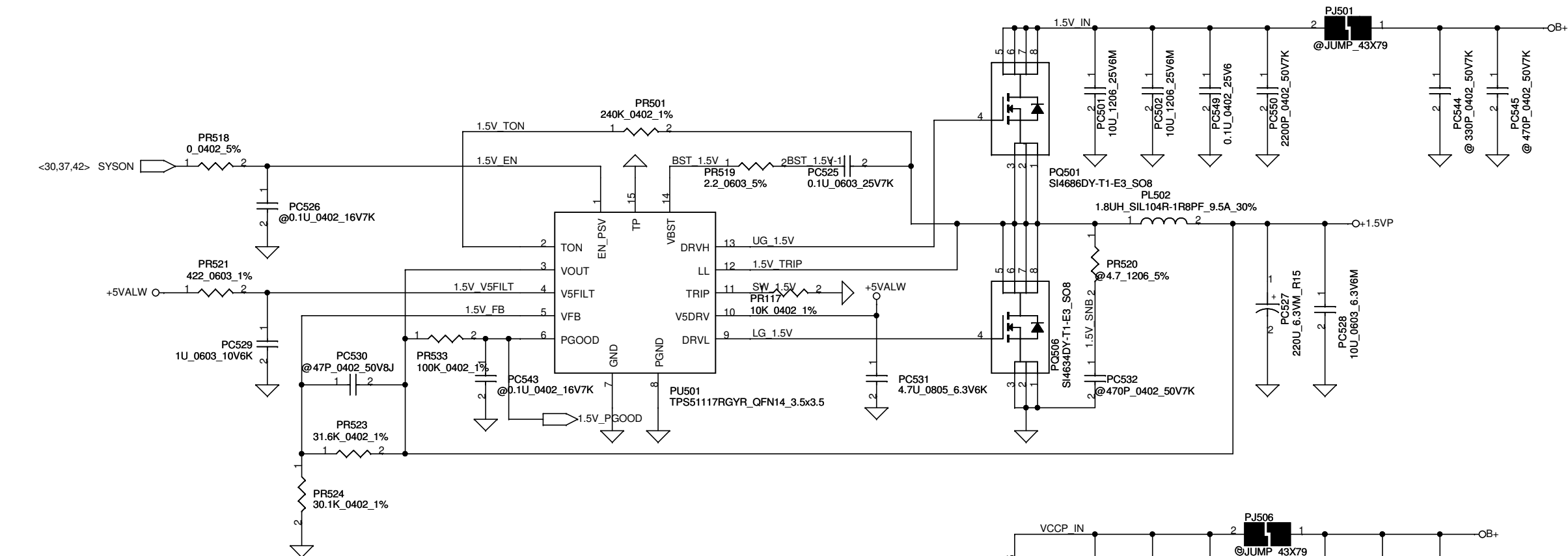


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				Rev	0.1
Date: Tuesday, March 24, 2009				Sheet	44 of 52

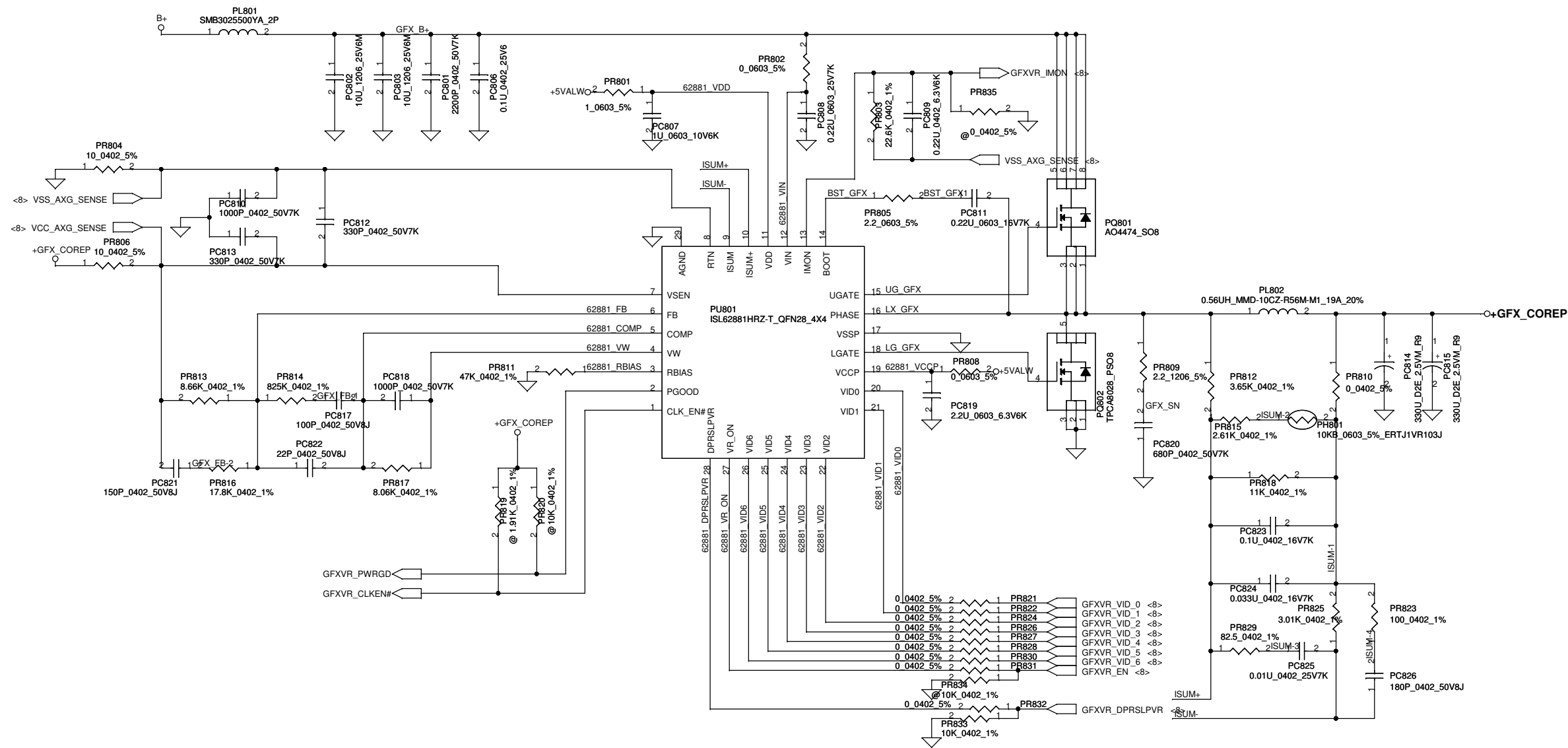




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				Custom	Rev 0.1
				Date:	Tuesday, March 24, 2009
				Sheet	46 of 52

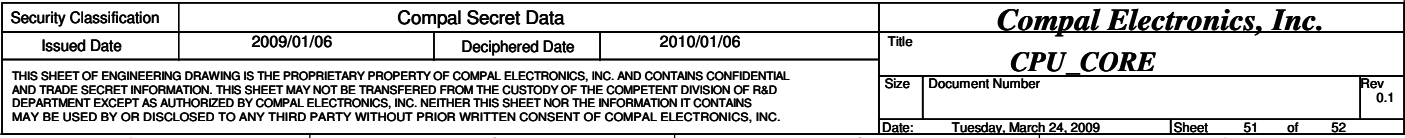


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