

Compal Confidential

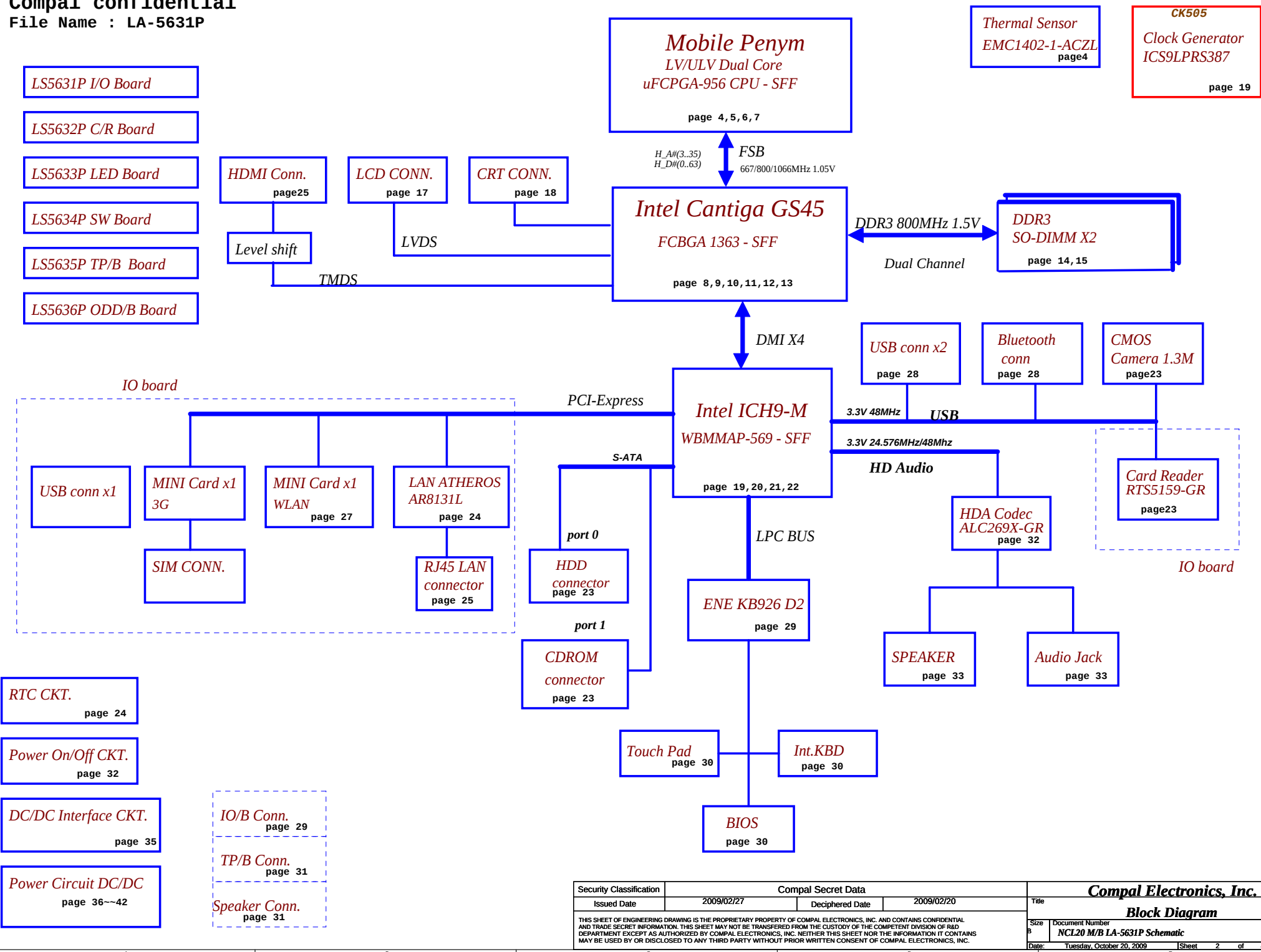
NCL20 ULV M/B Schematics Document

Intel Penryn Processor with Cantiga SFF + DDRIII + ICH9M SFF

2009-10-08

REV: 0.4

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
		ON	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+0.75V	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b

EC SM Bus2 address

ICH9M SMBUS Address

Device	HEX	Address
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (ICS9LPRS387, SLG8SP556V)	D2	1 1 0 1 0 0 1 0

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure

PCIE table

PCIE port1	3G Card
PCIE port2	Wireless Card
PCIE port3	GLAN
PCIE port4	
PCIE port5	
PCIE port6	

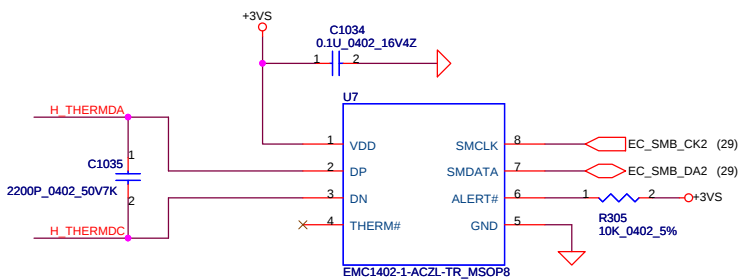
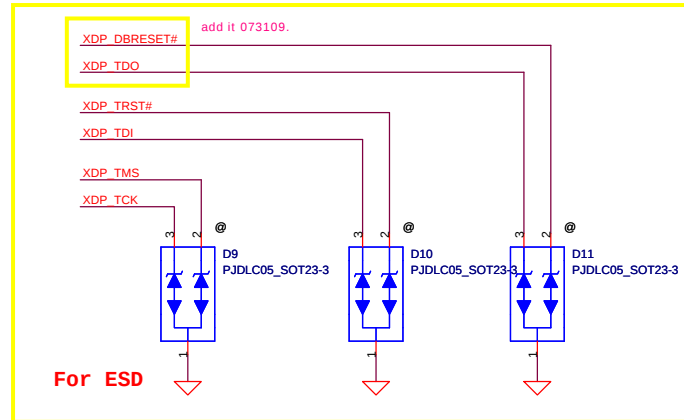
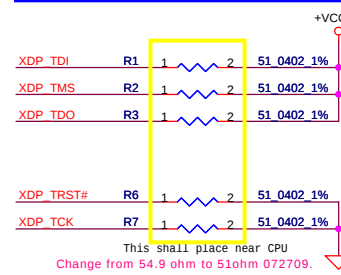
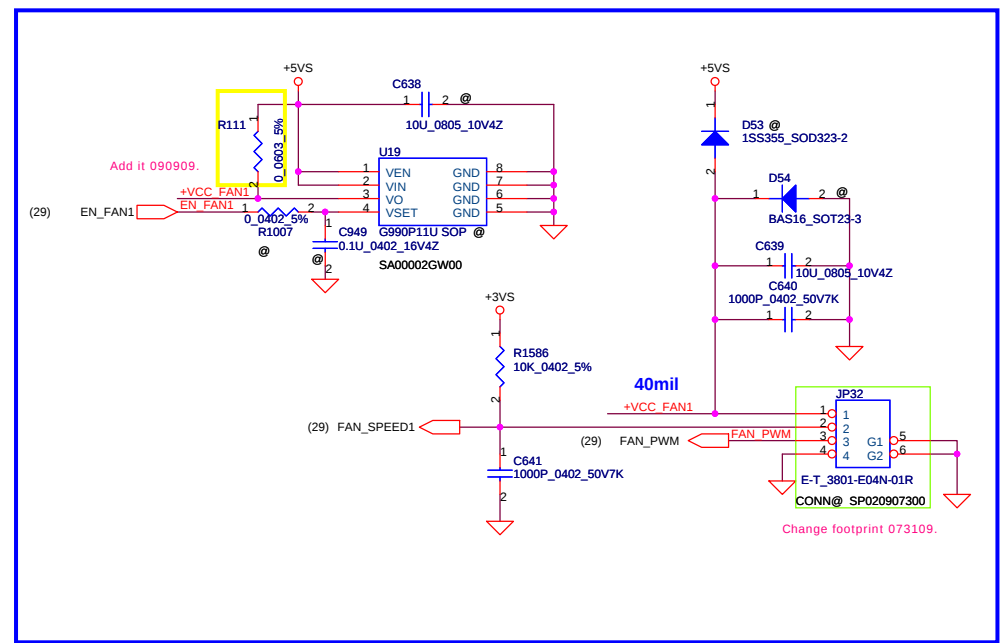
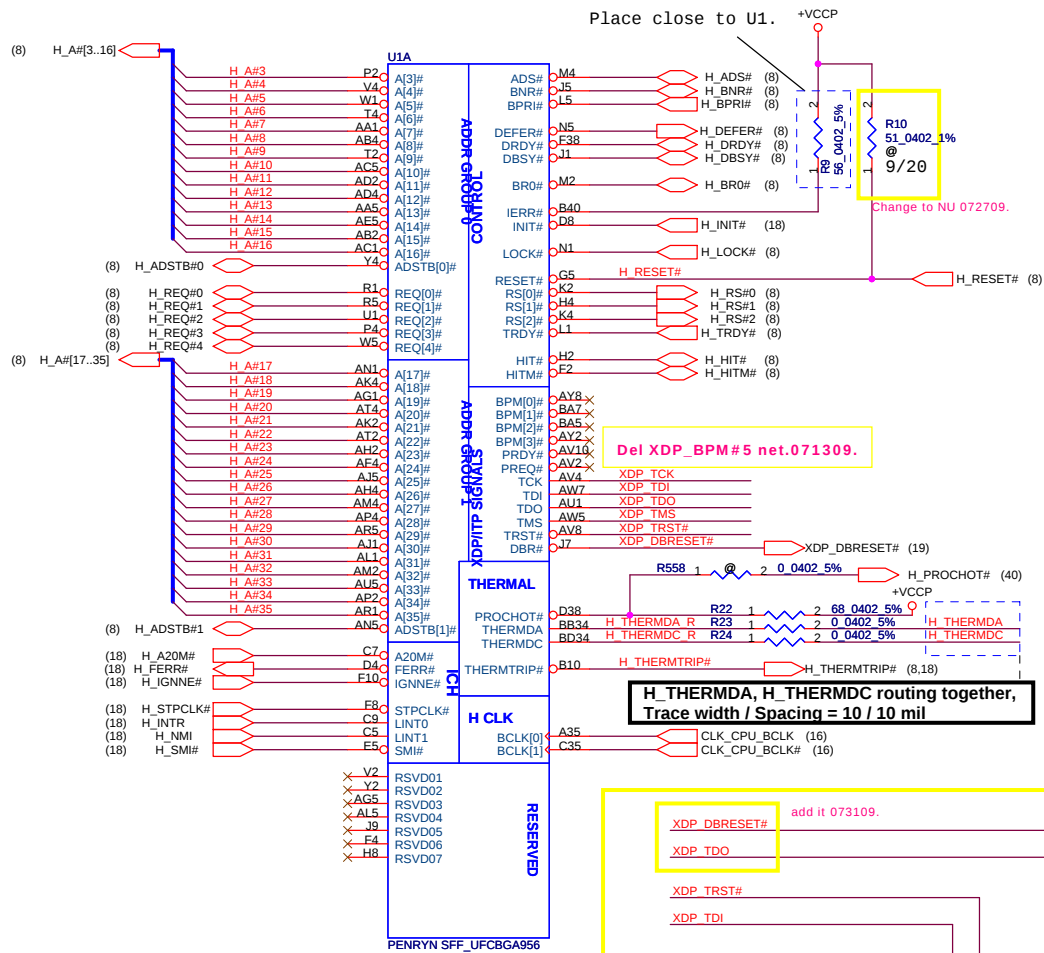
SATA table

SATA port0	HDD
SATA port1	ODD
SATA port2	
SATA port3	
SATA port4	
SATA port5	

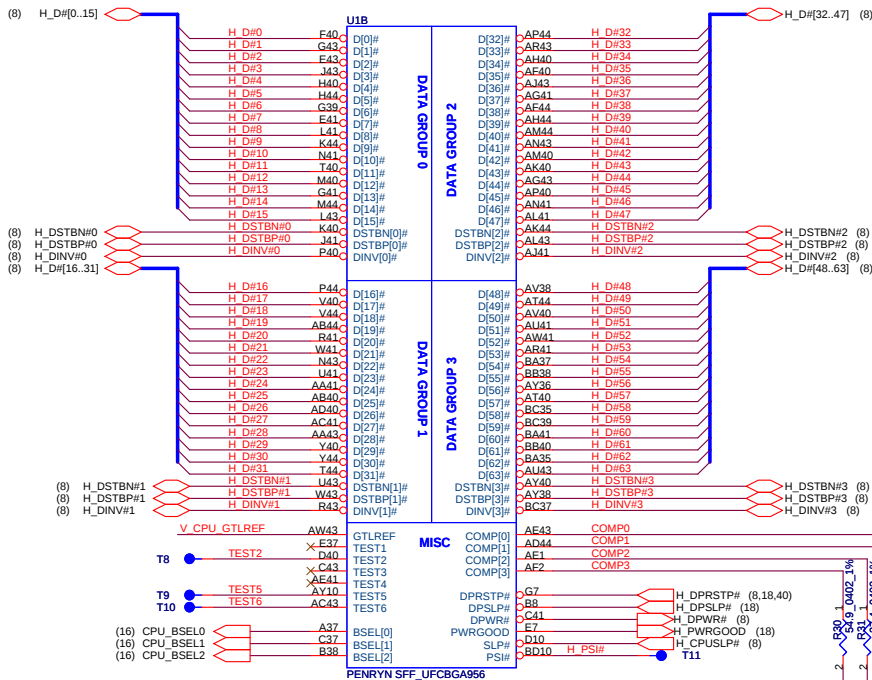
USB table

EHCI1	UHCI1	Port0	MB USB Conn1.
		Port1	MB USB Conn2.
	UHCI2	Port2	sub board
		Port3	WLAN
EHCI2	UHCI3	Port4	Card Reader
		Port5	3G
	UHCI4	Port6	BT
		Port7	CMOS Camera
	UHCI5	Port8	
		Port9	
	UHCI6	Port10	
		Port11	





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								Penryn (1/3) & FAN			
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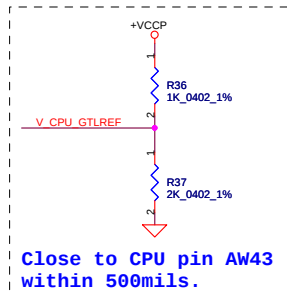


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

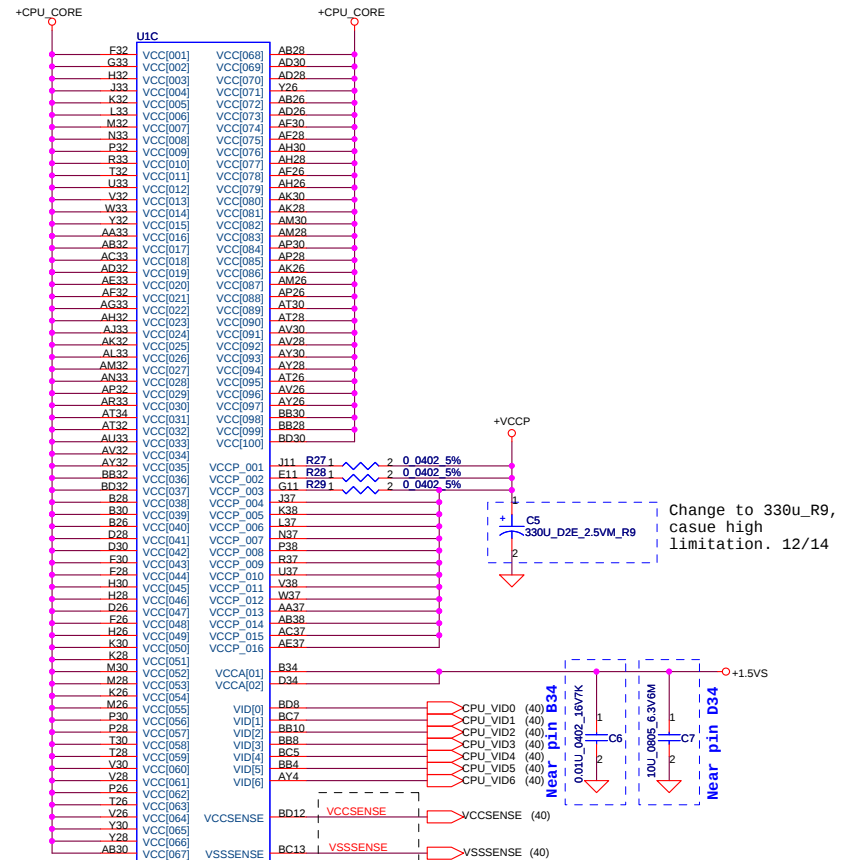
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Cause CPU core power change to 1 phase, and not need support the pin, leave it as TP. 10/02

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

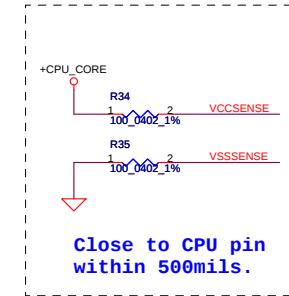


Close to CPU pin AW43 within 500mils.



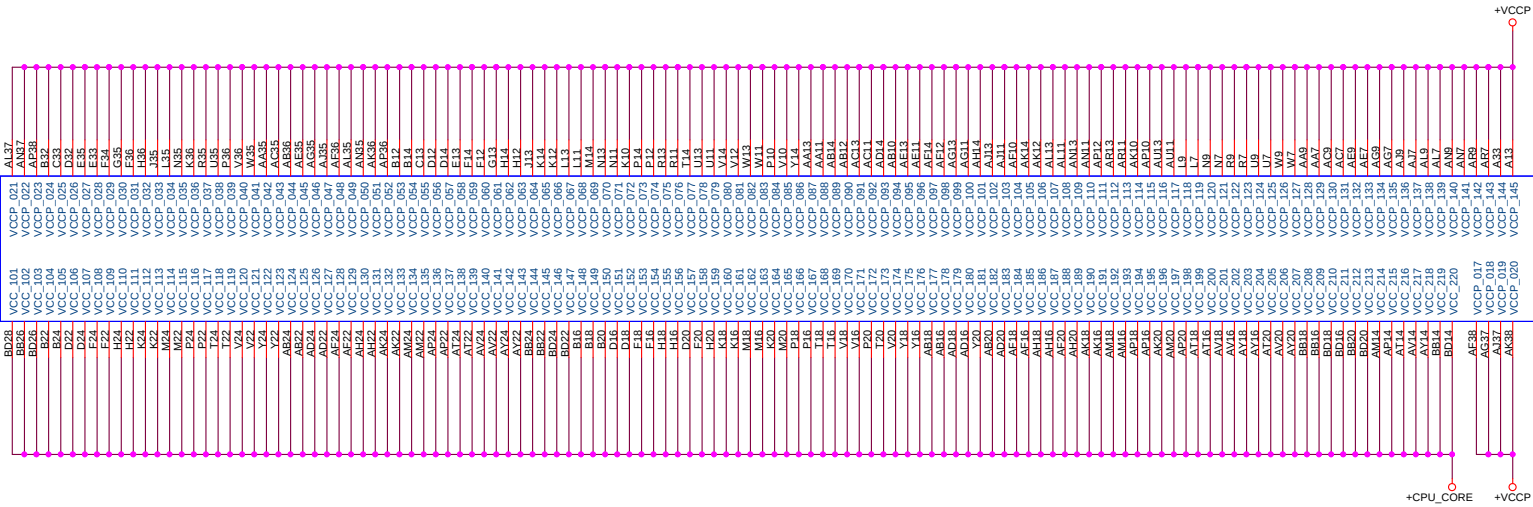
Change to 330u_R9, casue high limitation. 12/14

Length match within 25 mils. The trace width/space/other is 20/7/25.

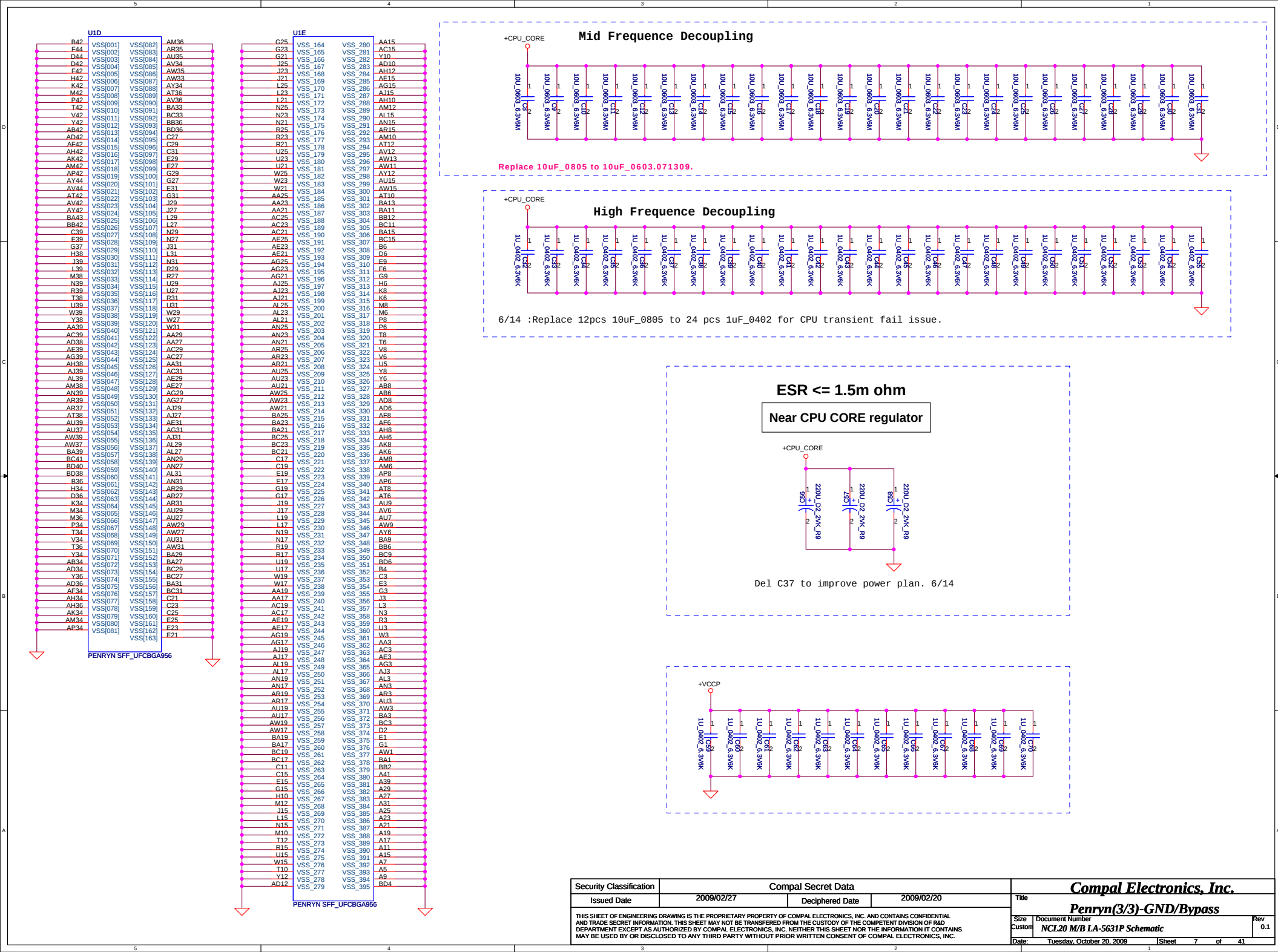


Close to CPU pin within 500mils.

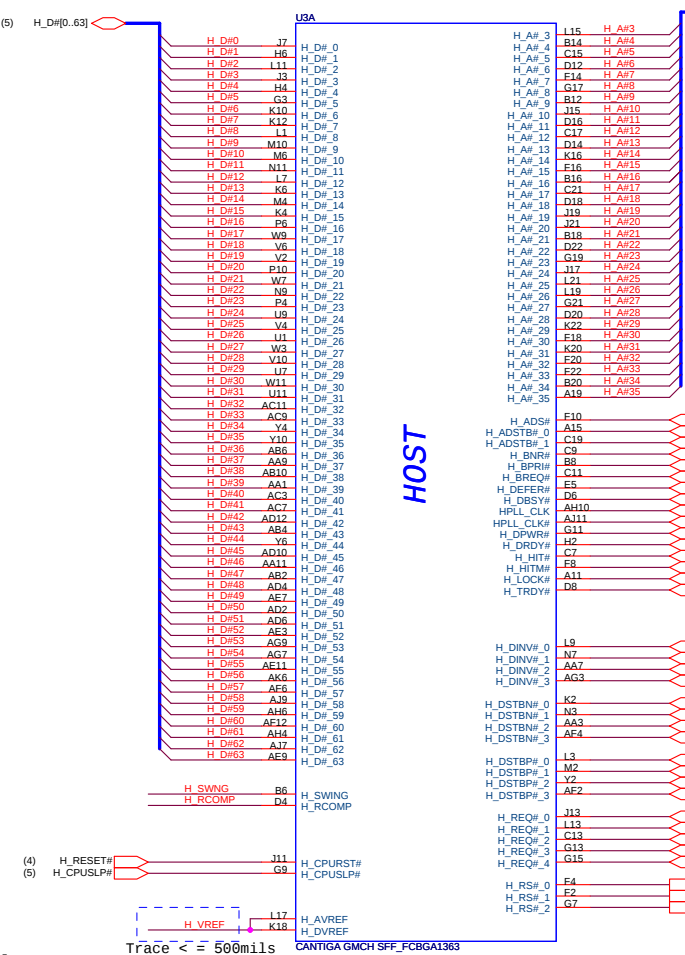
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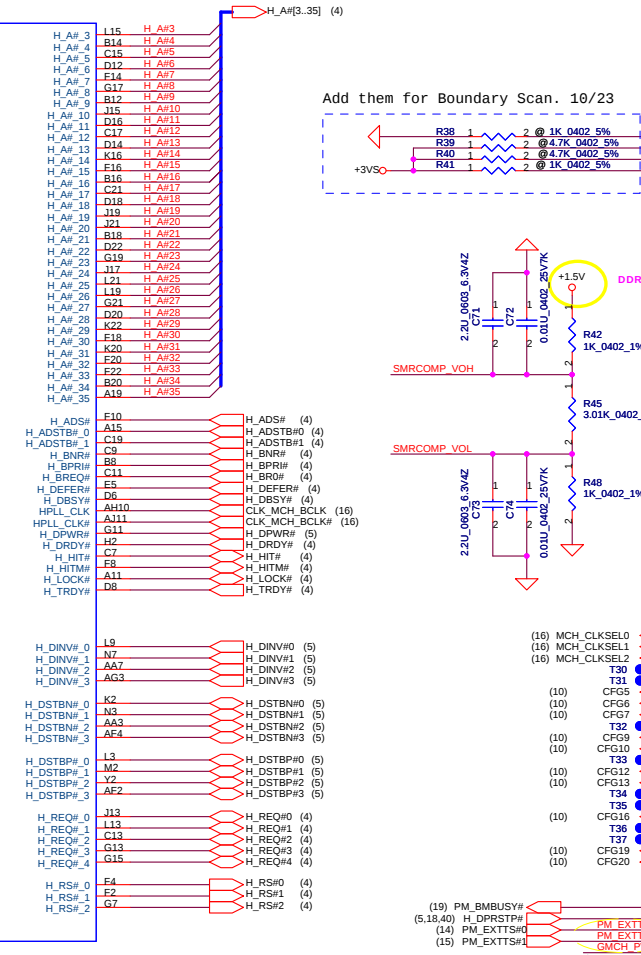
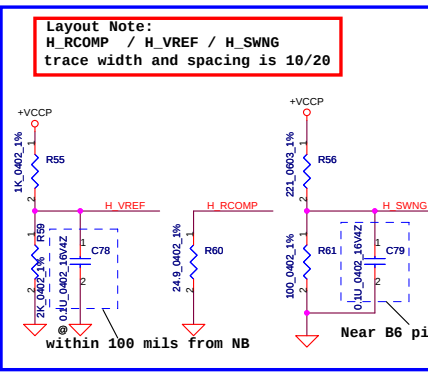
UIF
PENRYN SFF_UFCBGA956



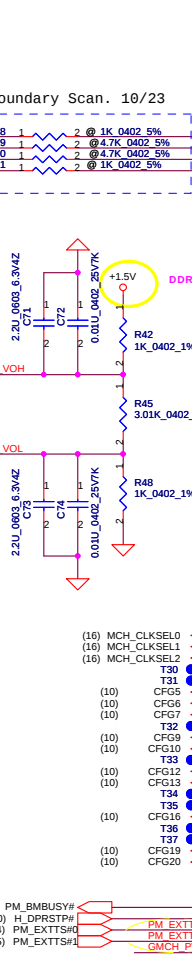
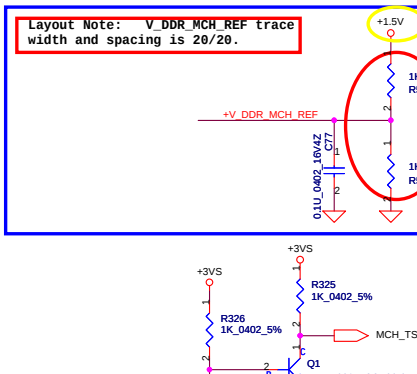
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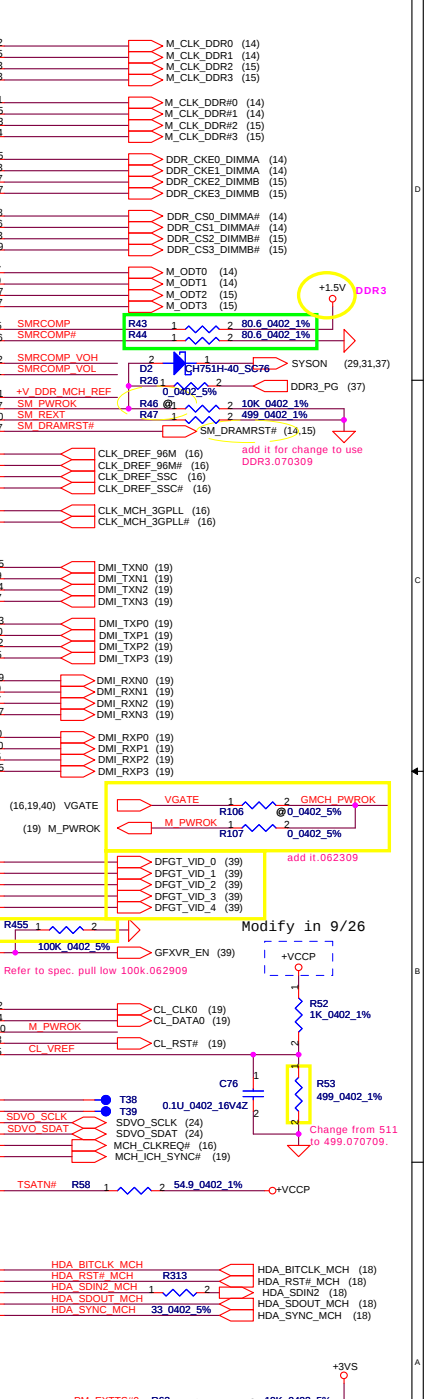
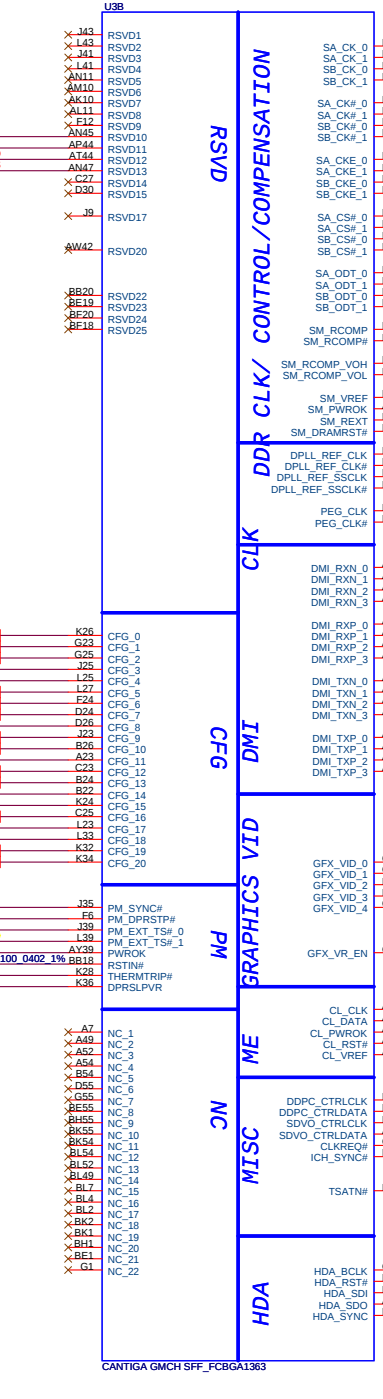
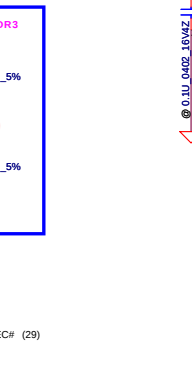
layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces



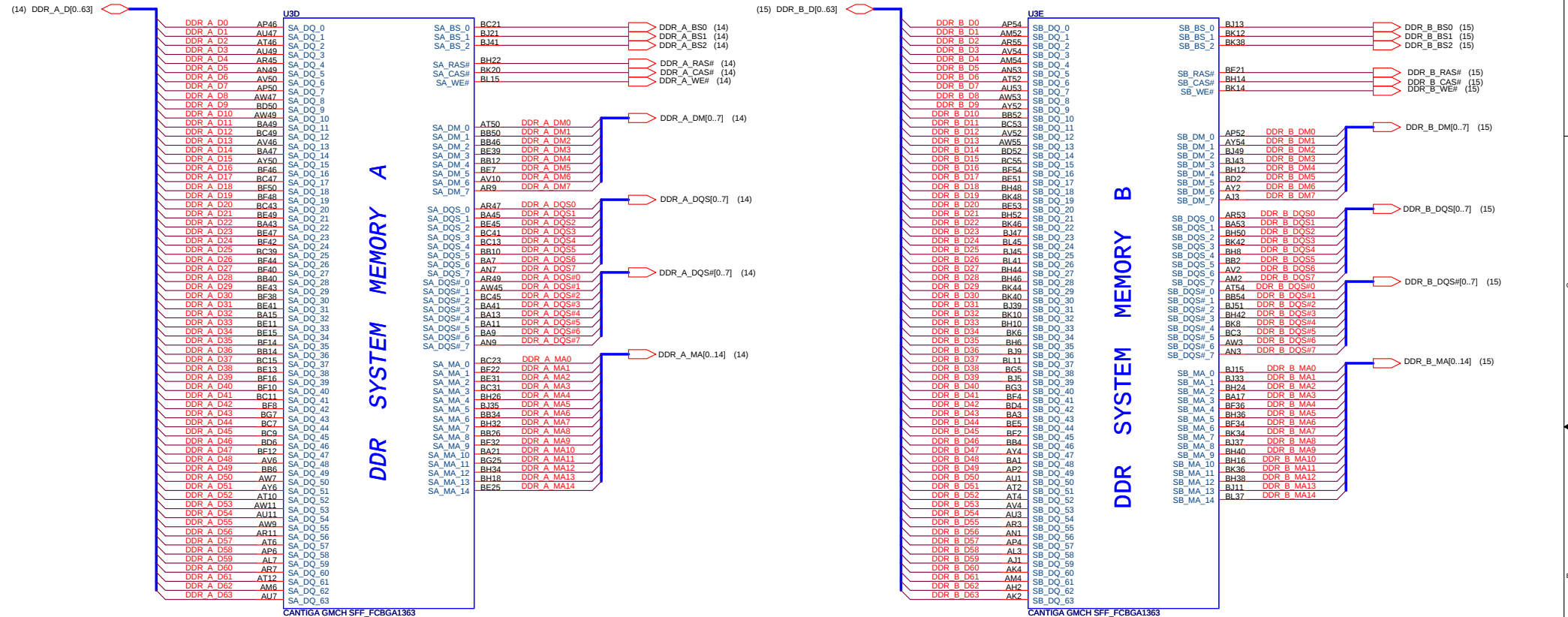
layout note:
Place them close to U4 pin BC51.

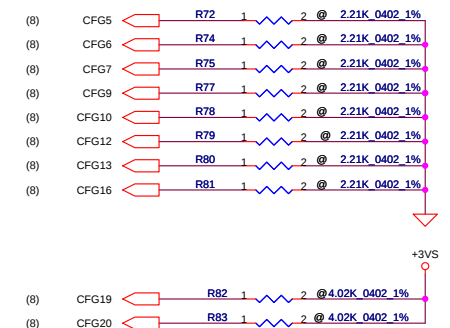
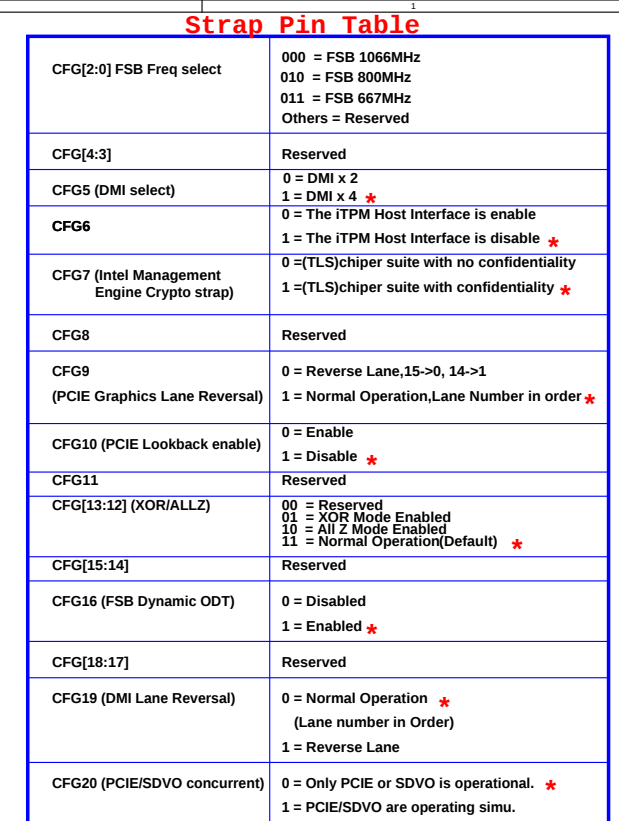


layout note:
Add R428 in 9/26



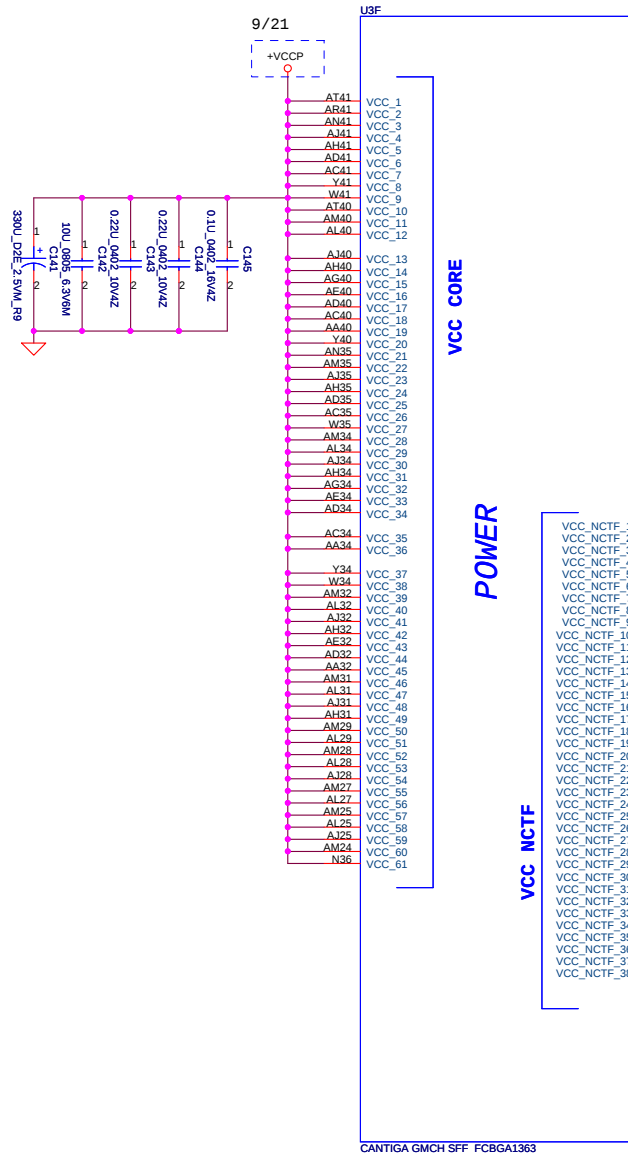
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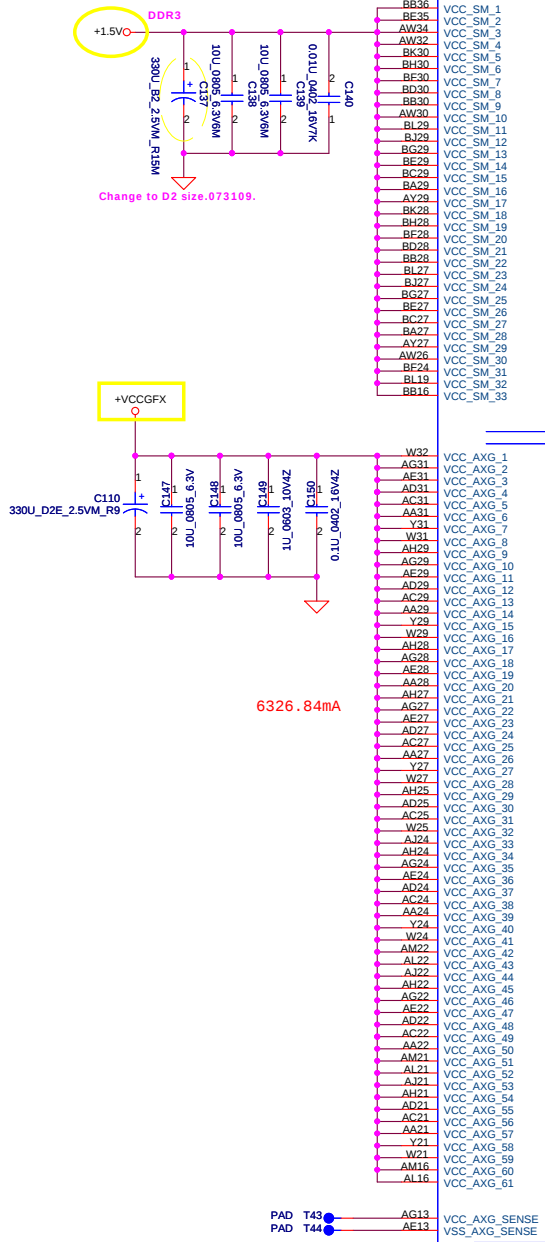


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Extnal Graphic: 1210.34mA
Integrated Graphic: 1930.4mA

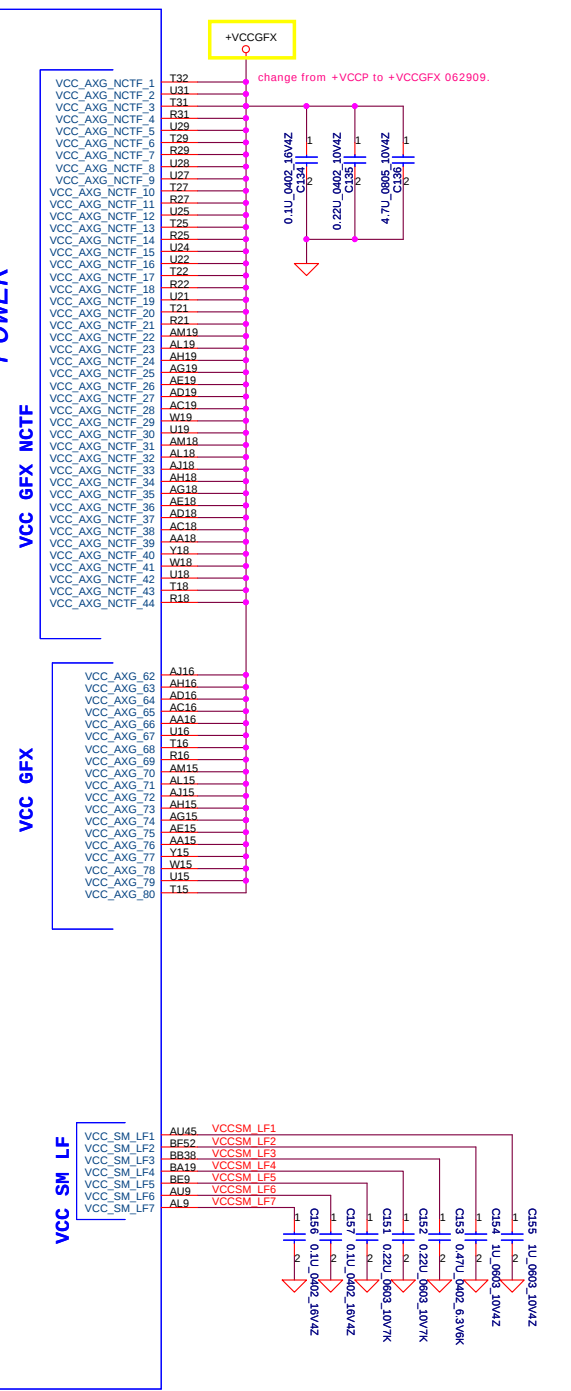


CANTIGA GMCH SFF_FCBGA1363

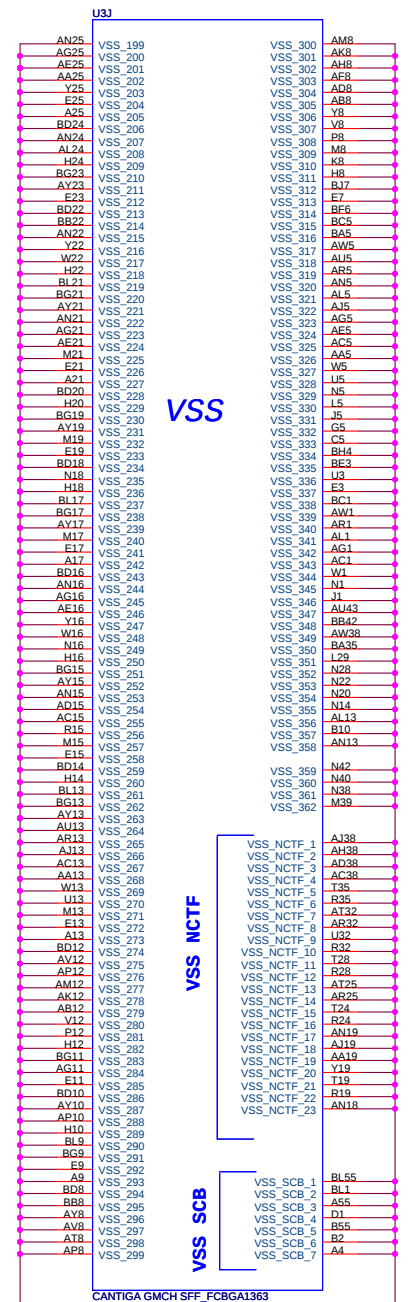
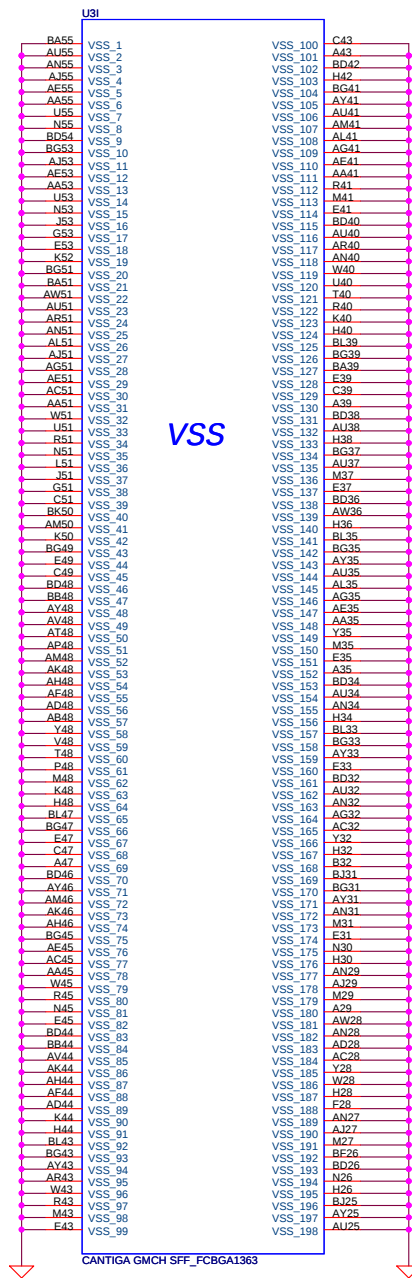


PAD T43 AG13 VCC_AGG_SENSE
PAD T44 AE13 VSS_AGG_SENSE

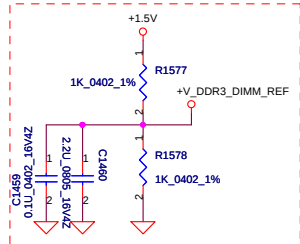
CANTIGA GMCH SFF_FCBGA1363



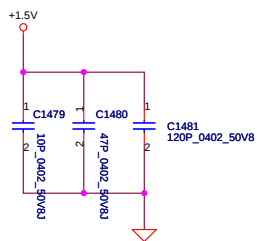
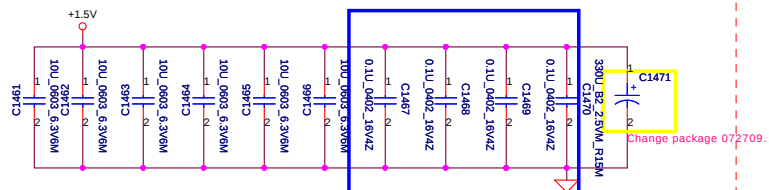
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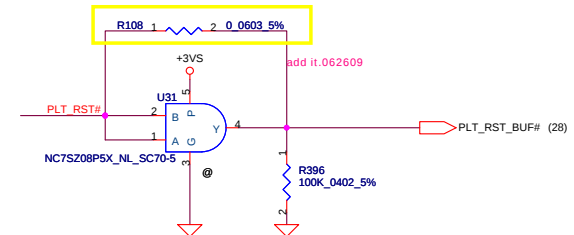
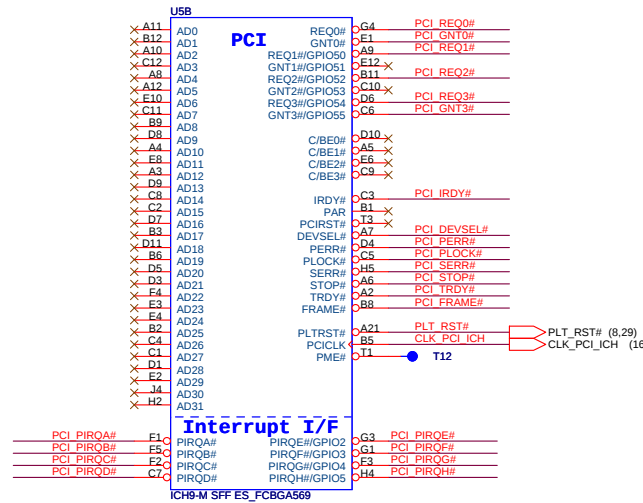
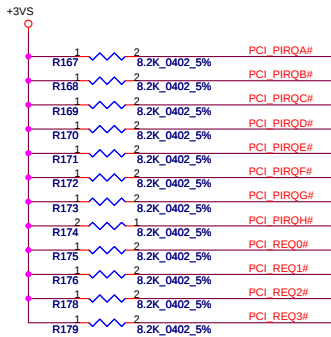
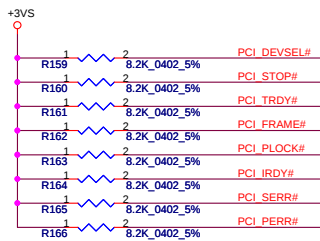


Layout Note: Place these 4 Caps near Command and Control signals of DIMMA - - - - -

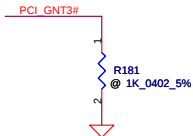


DDR3 SO-DIMM A REVERSE

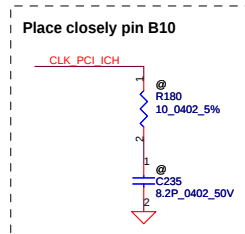
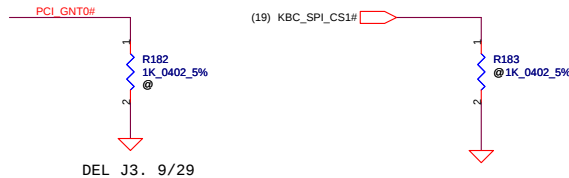
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				DDRIII-SODIMM SLOT1	
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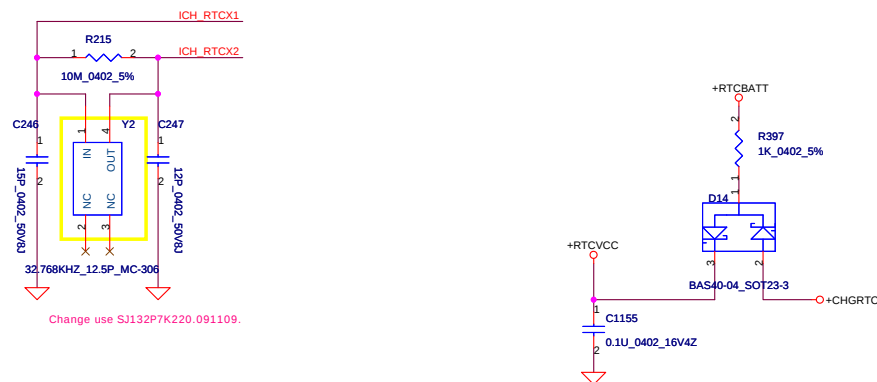
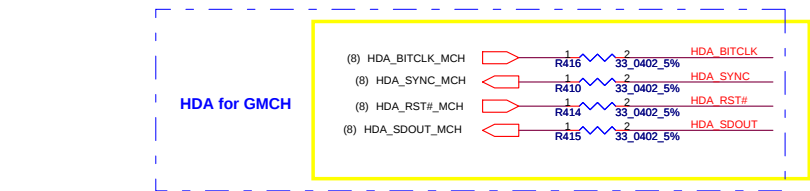
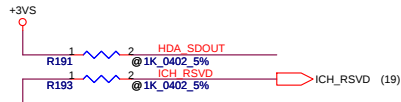


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *

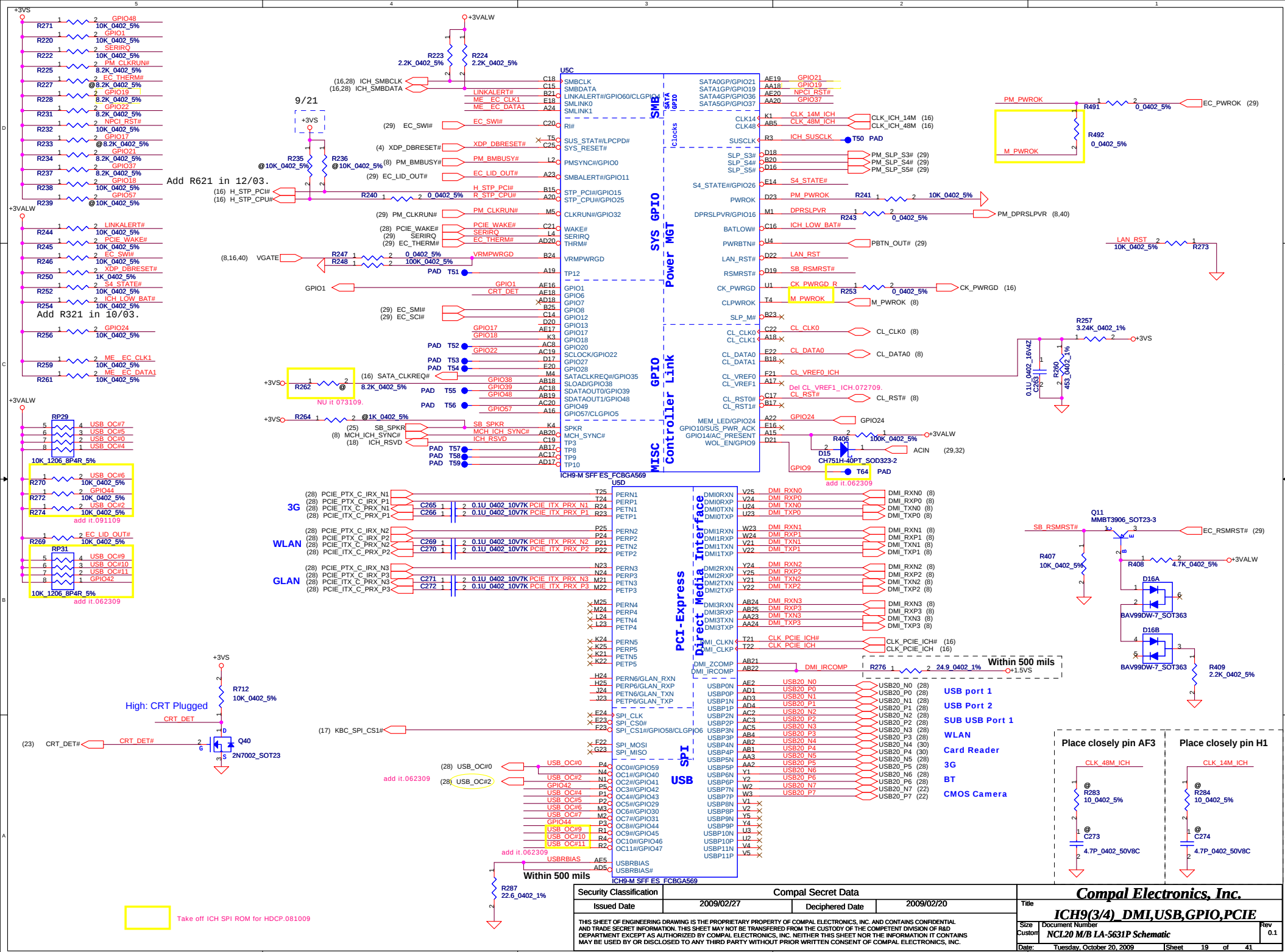


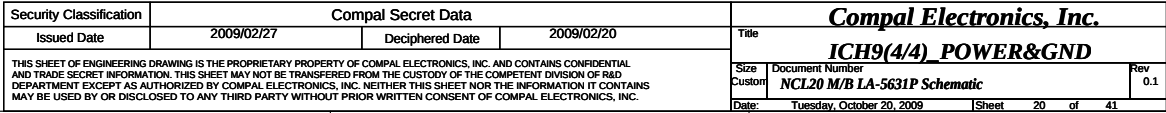
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

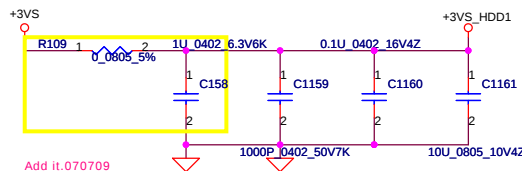
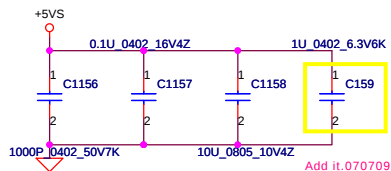




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				Document Number NCL20 M/B LAN-563P1 Schematic	
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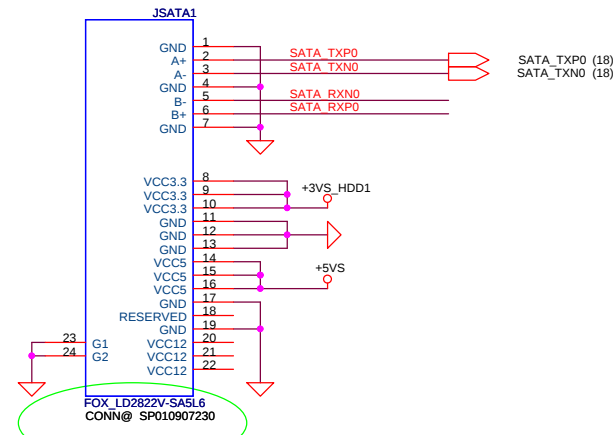
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SATA_RXN0_C 1 2 C1162 0.01U_0402_16V7K SATA_RXN0

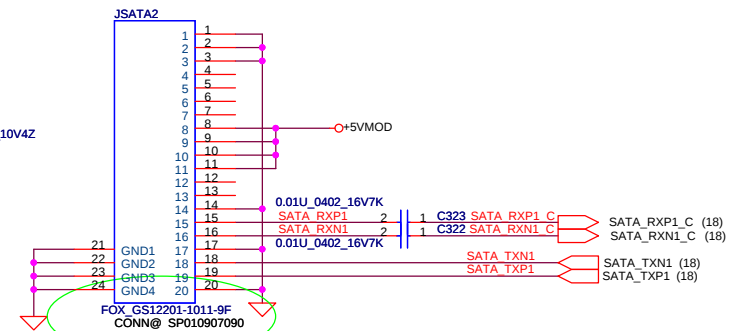
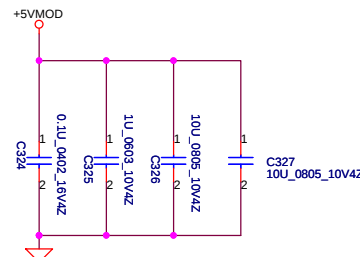
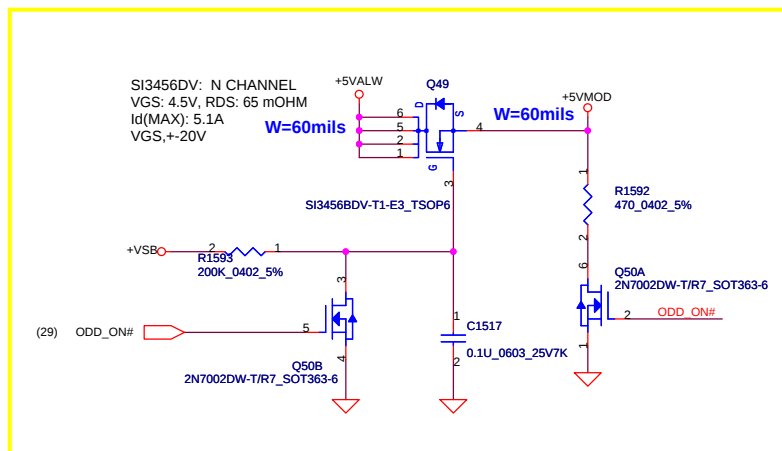
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SATA_RXP0_C 1 2 C1163 0.01U_0402_16V7K SATA_RXP0

SATA HDD Conn.



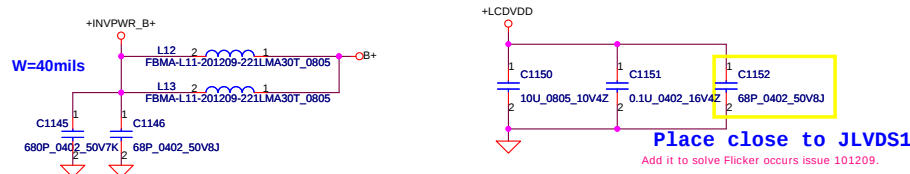
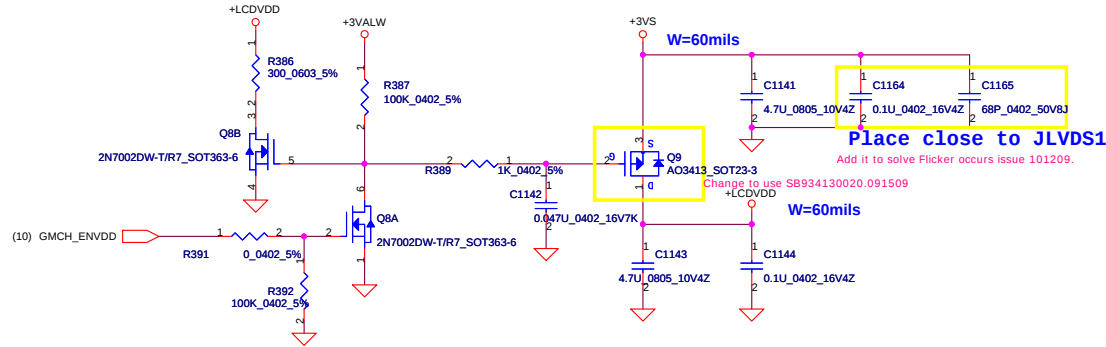
CD-ROM Connector



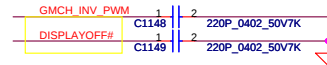
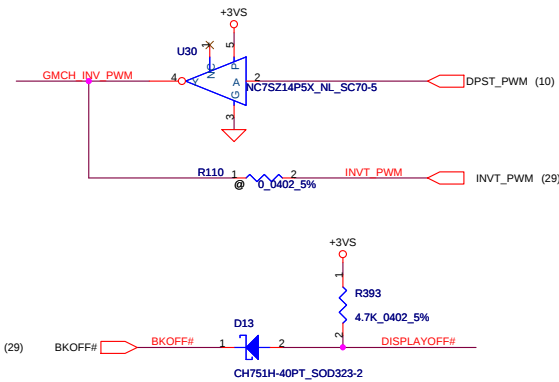
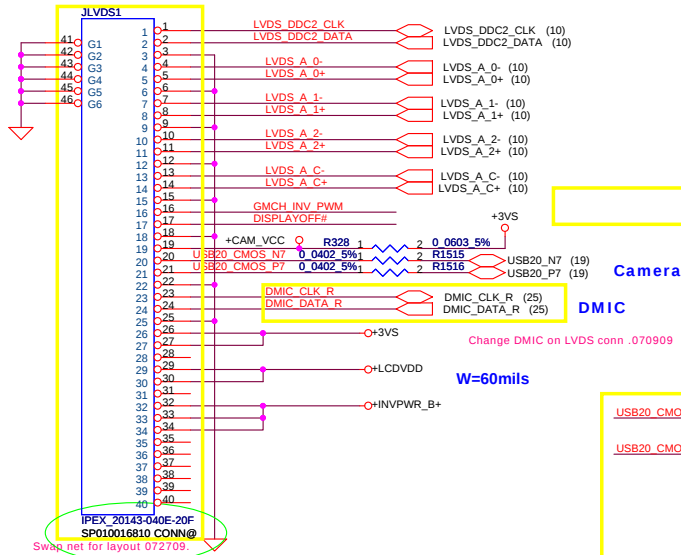
Add it for ODD button.072109.

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						Size		Document Number		Rev	
						Custom		NCL20 M/B LA-5631P Schematic		0.1	
						Date:		Tuesday, October 20, 2009		Sheet 21 of 41	

LCD POWER CIRCUIT



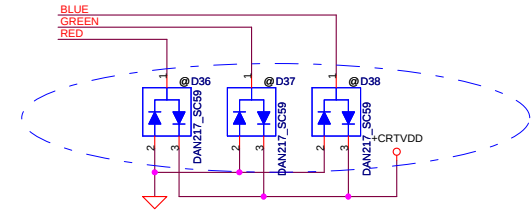
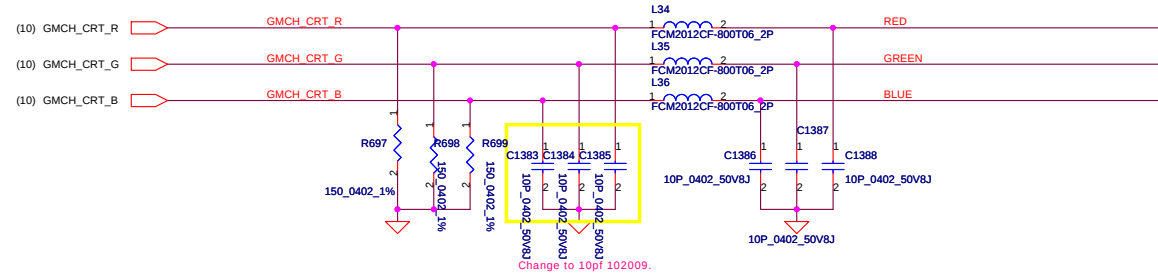
LVDS and USB CAM connector



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				Size	Document Number	Rev
				Custom	NCL20 M/B LA-5631P Schematic	0.1
Date:		Tuesday, October 20, 2009		Sheet	22 of 41	

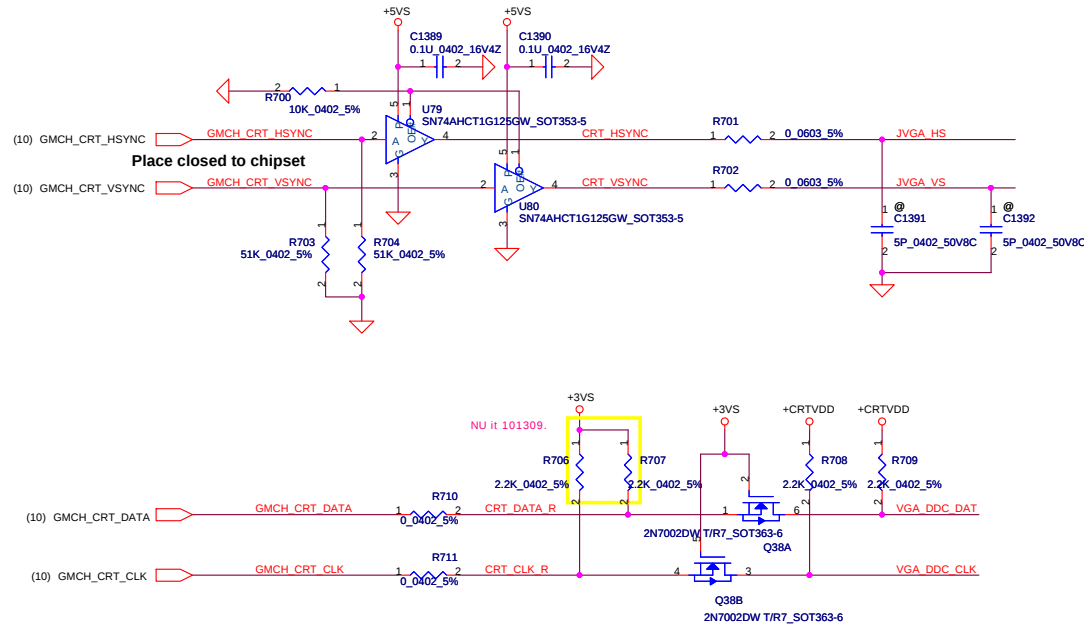
NOTE: L : A-->B1
H: A-->B2

Place closed to chipset

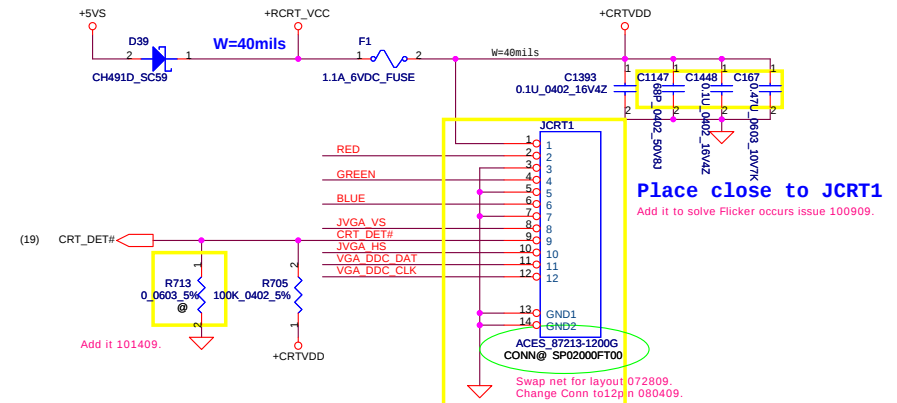


Place close to JCRT1

Place closed to chipset



CRT PORT

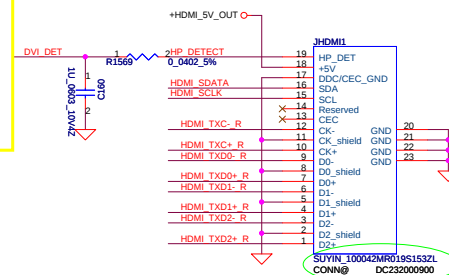
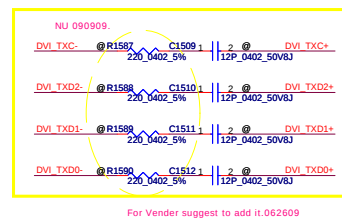
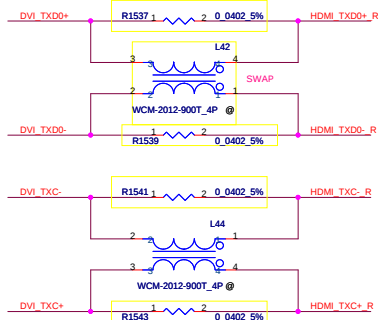
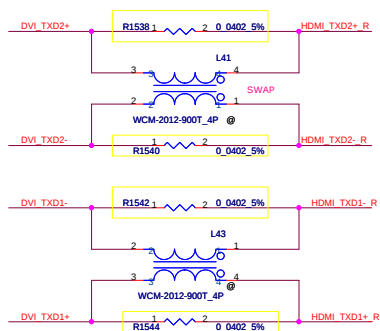
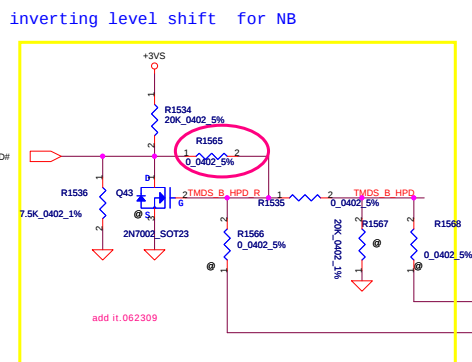
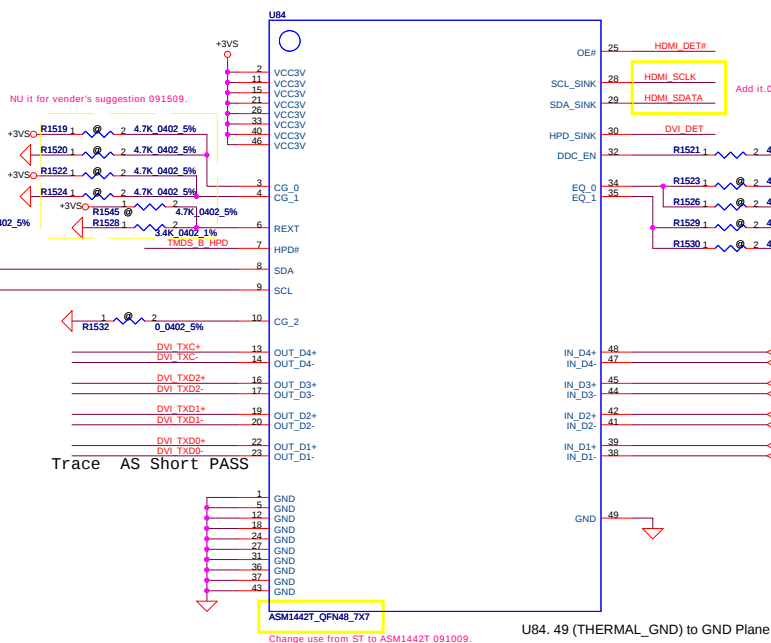
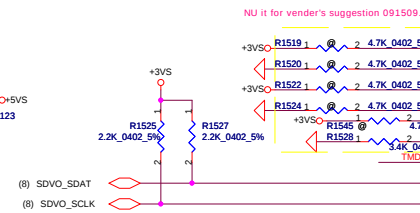
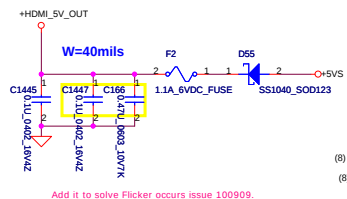


Place close to JCRT1

Add it to solve Flicker occurs issue 100909.

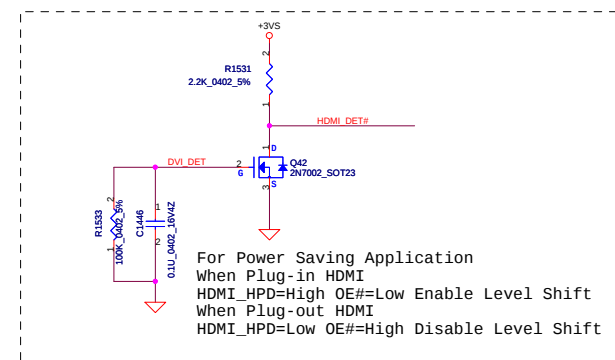
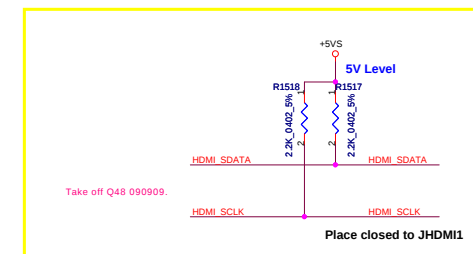
ACES_87213-1200G
CONN@ SP02000FT00
Swap net for layout 072809.
Change Conn to 12pin 080409.

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EQ_1	EQ_0	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB

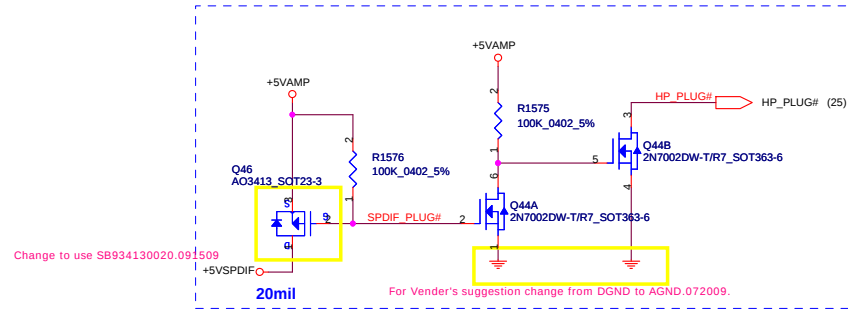
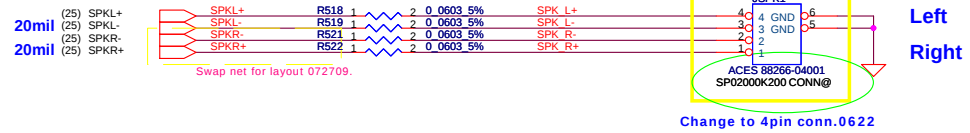
	PC_2	PC_1	PC_0	Swing	Pre-amp	Slew-rate	
★	0	0	0	450	0	0	
	0	0	1	420	0	-3dB	Shortest trace
	0	1	0	450	0	-3dB	Shortest trace
	0	1	1	460	0	-4dB	
	1	0	0	340	0	0	
	1	0	1	400	2dB	0	Longest trace
	1	1	0	400	2dB	0	Longest trace
	1	1	1	420	0	0	



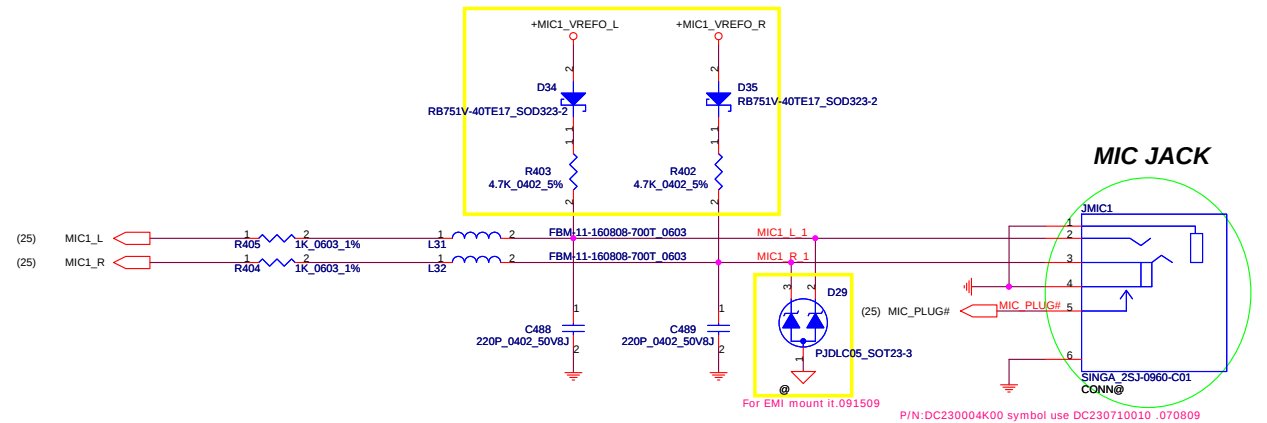
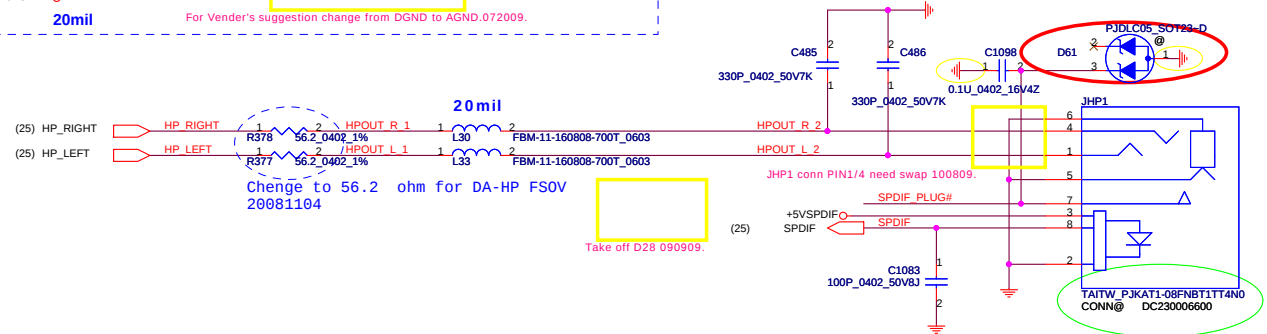
HDMI Connector

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				2007/09/29	
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				HDMI	
				Size	Document Number
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Int. Speaker Conn.

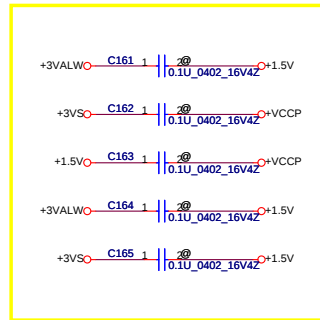
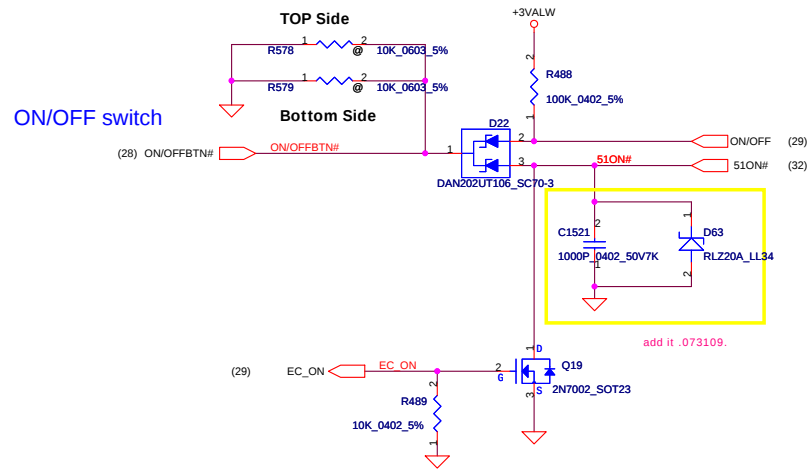


LINE Out/Headphone Out

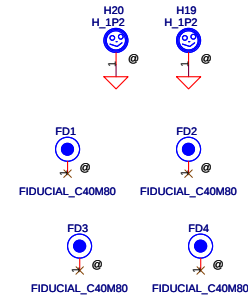
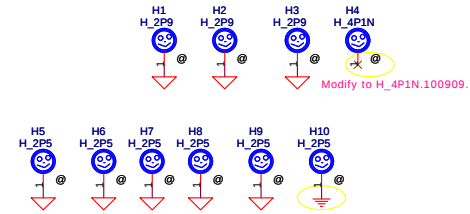


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Issued Date				Deciphered Date				Title			
2009/02/27				2010/01/21				Amplifier & Audio Jack			
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								NCL20 M/B LA-5631P Schematic			
								Date: Wednesday, October 21, 2009			
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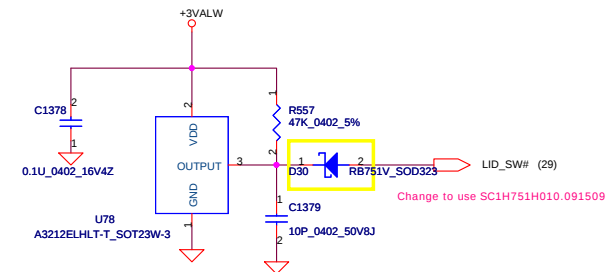
Power Button Logic



For EMI to add it.091109.

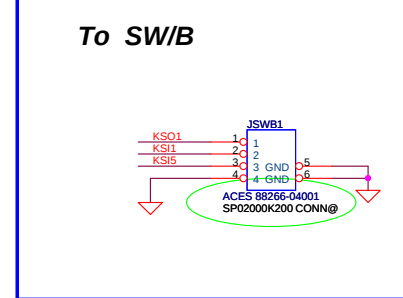
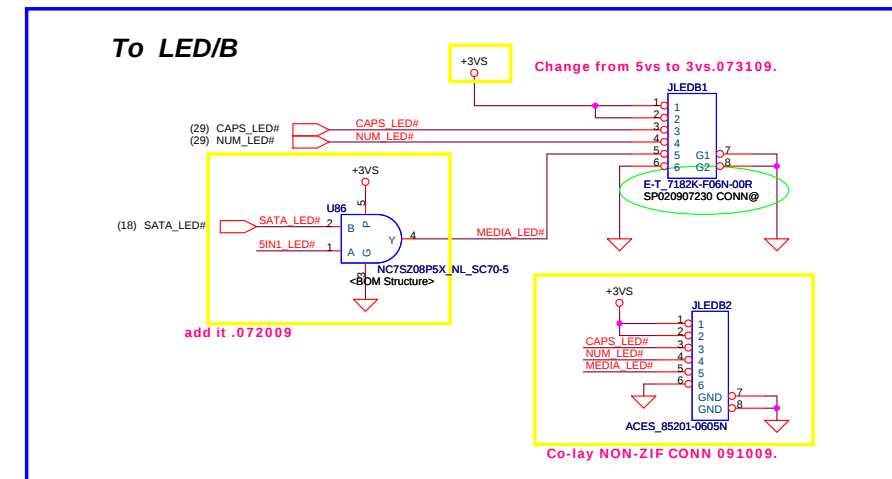
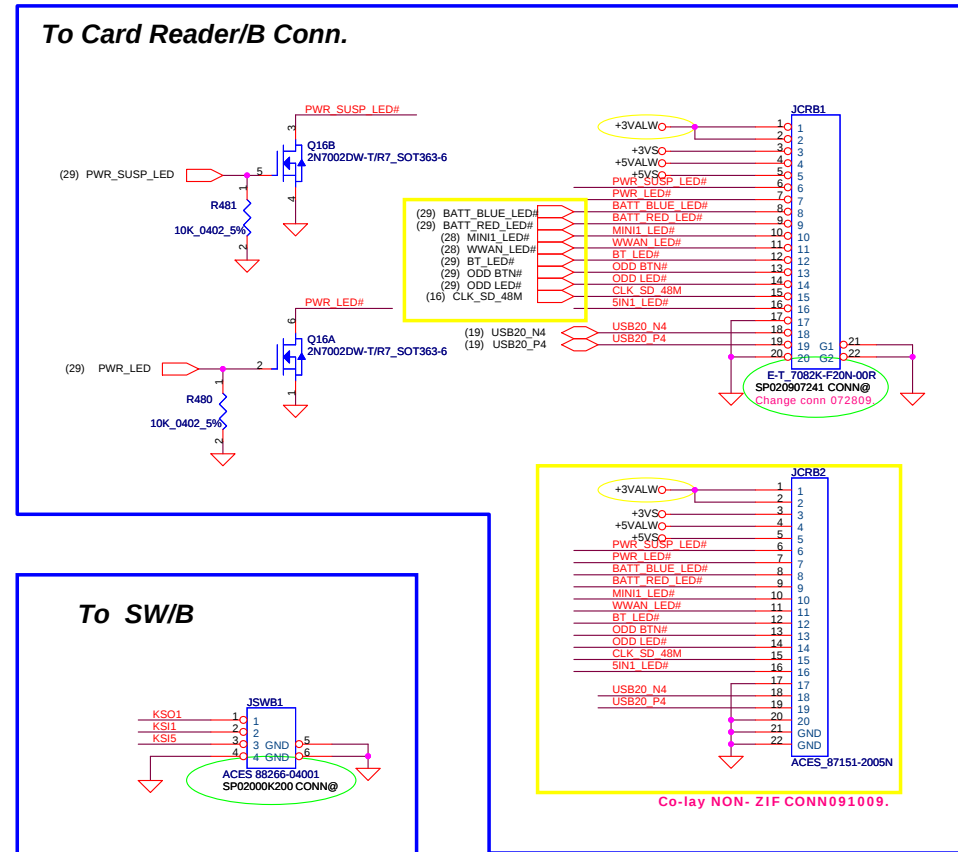
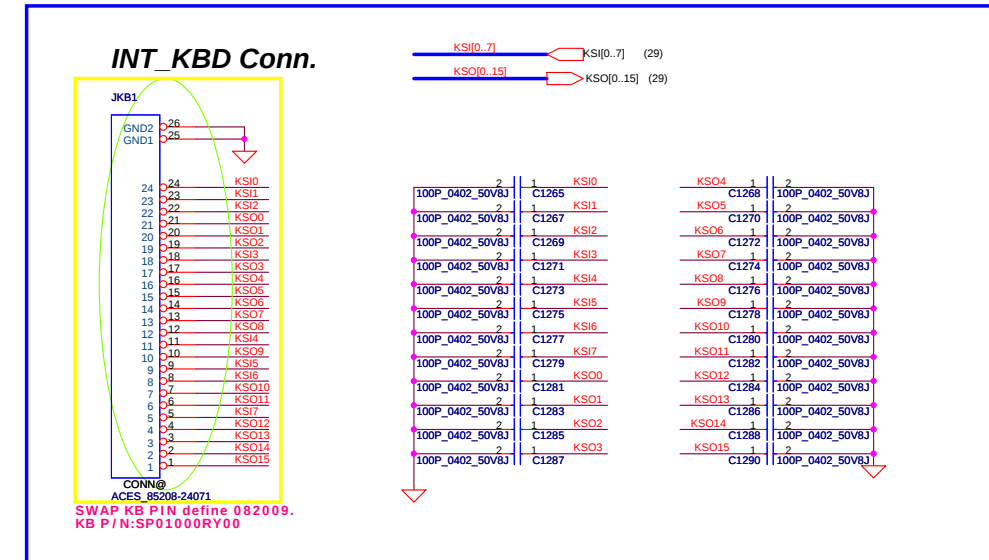
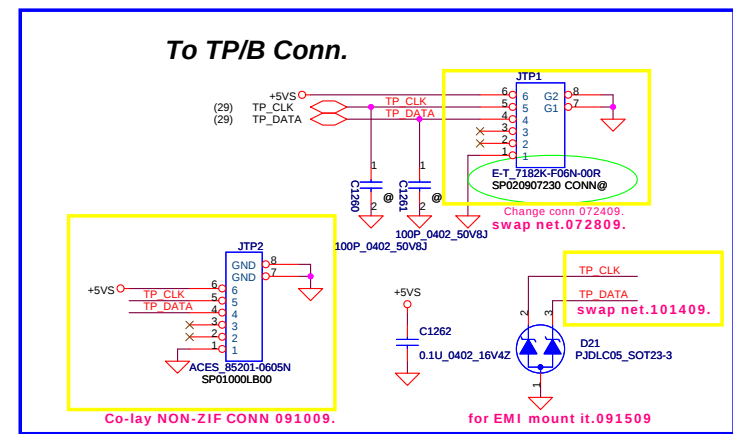
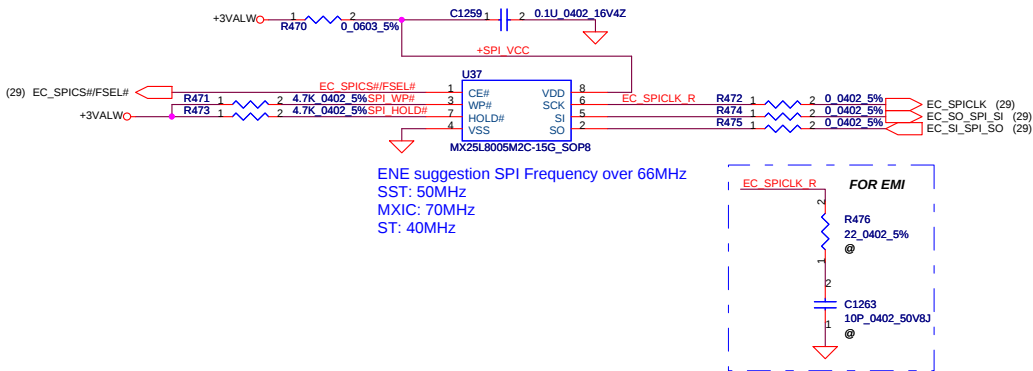


Lid Switch (Hall Effect Switch)



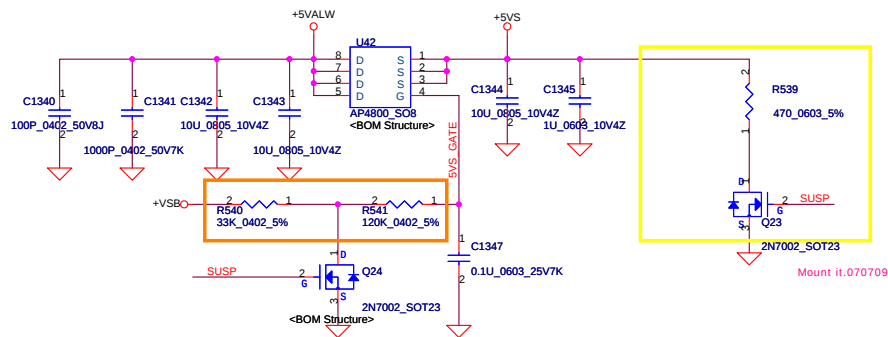
Change to use SC1H751H010.091509

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2009/01/22				2009/11/20				PWR ON/OFF & Screw Hole			
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								0.1			
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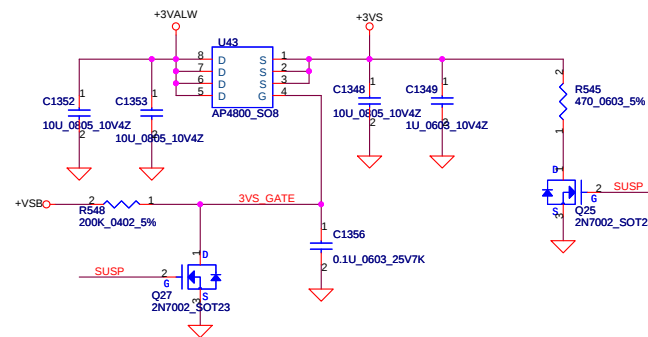


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Size	B	Document Number	NCL20 M/B LA-5631P Schematic			Rev
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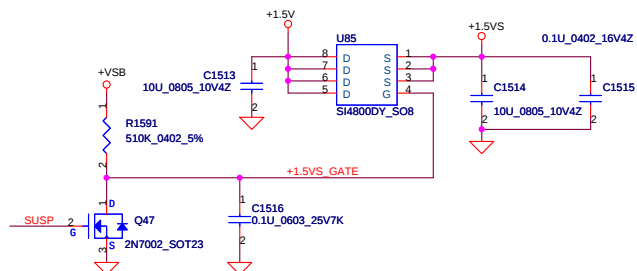
+5VALW TO +5VS



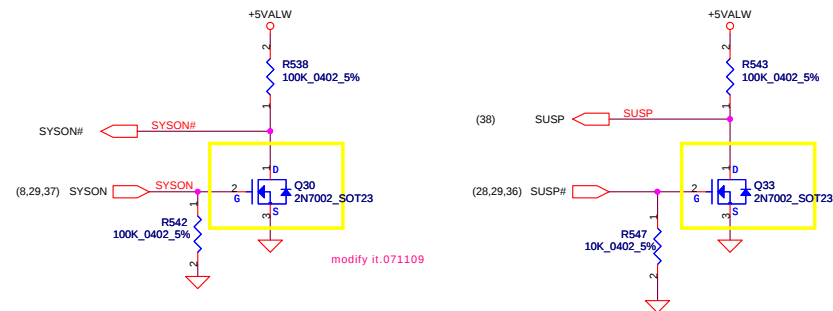
+3VALW TO +3VS



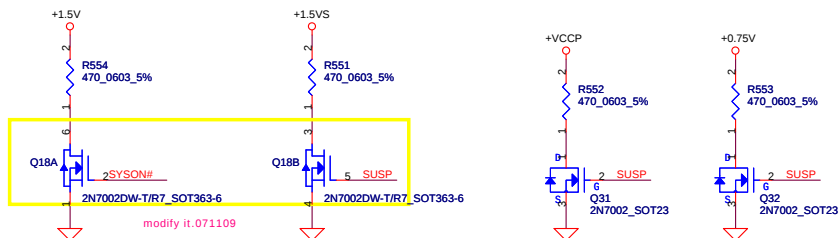
+1.5V to +1.5VS Transfer



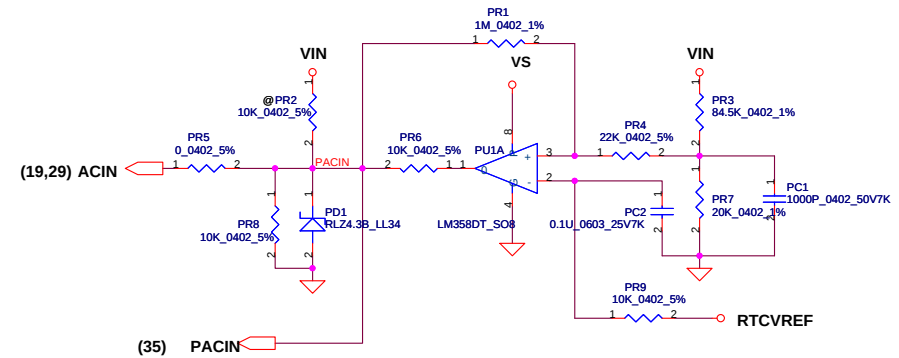
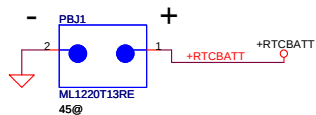
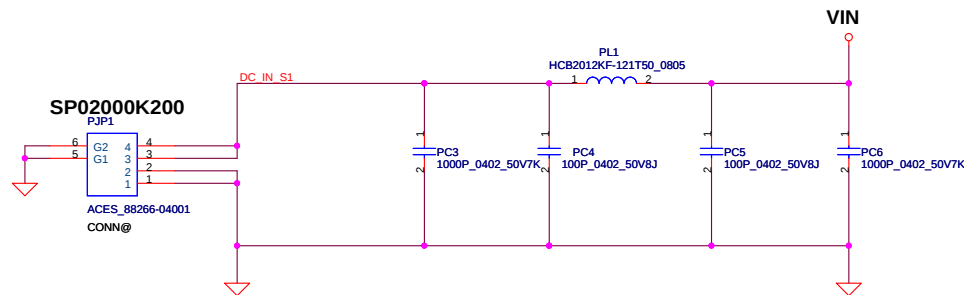
add it.070709



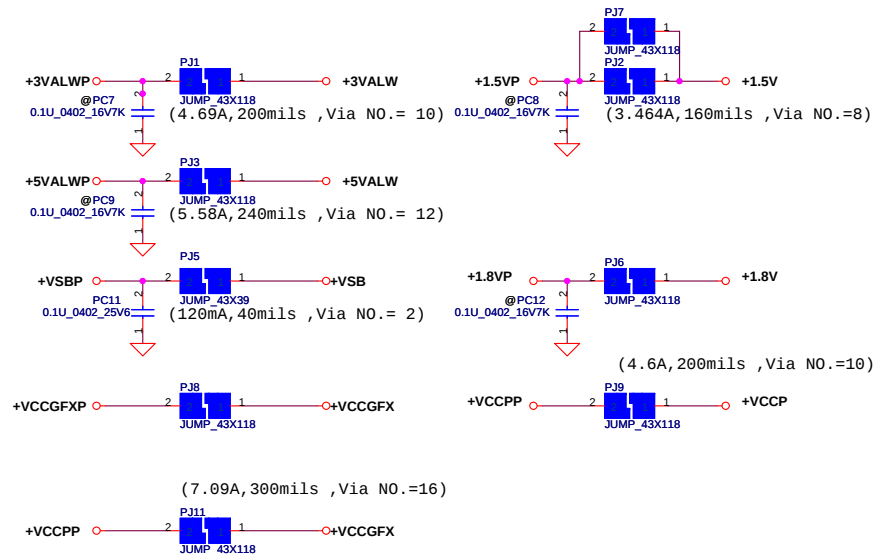
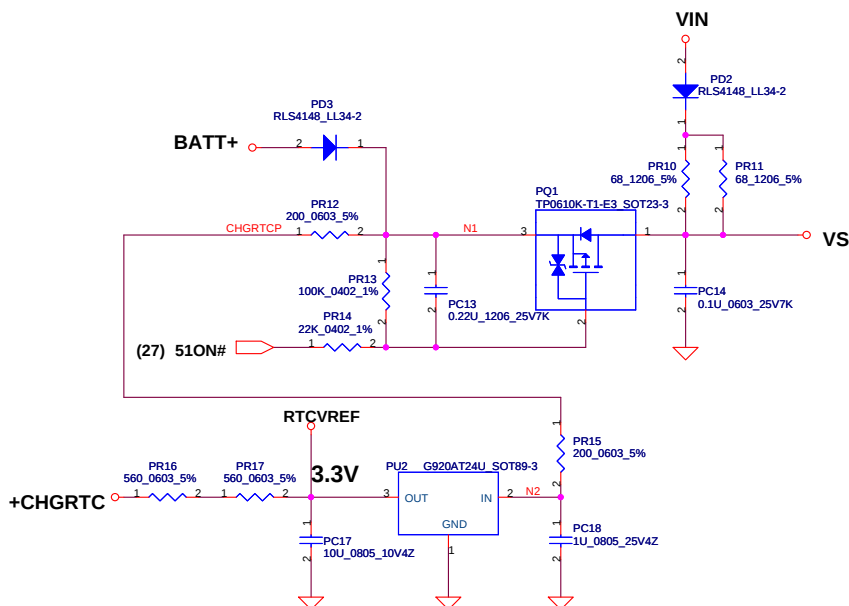
Discharge circuit



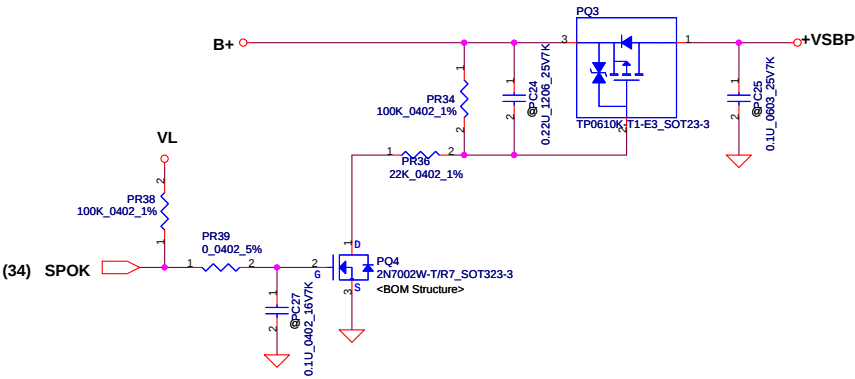
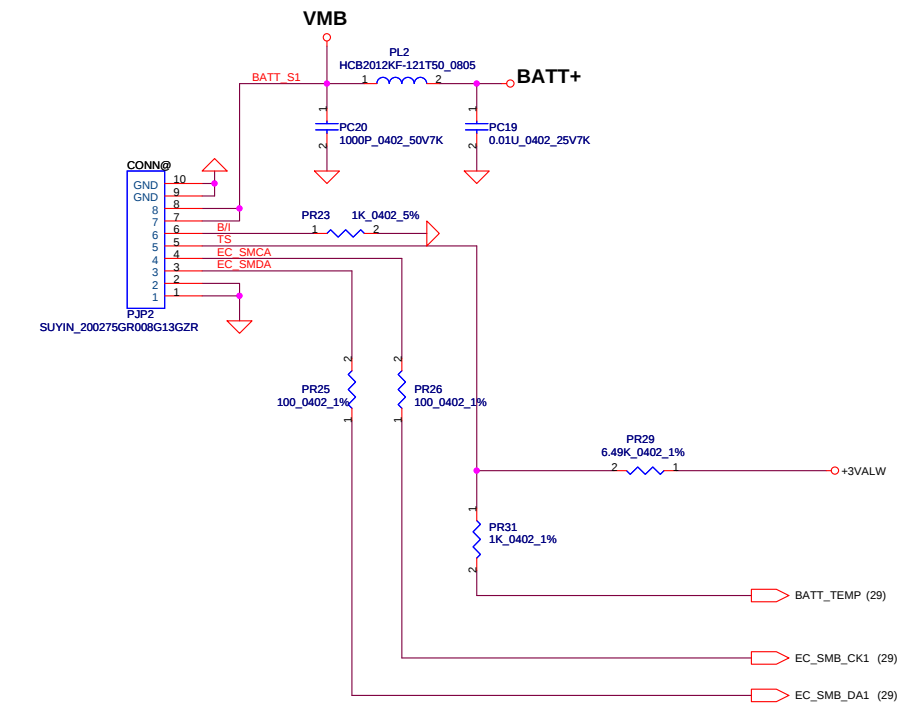
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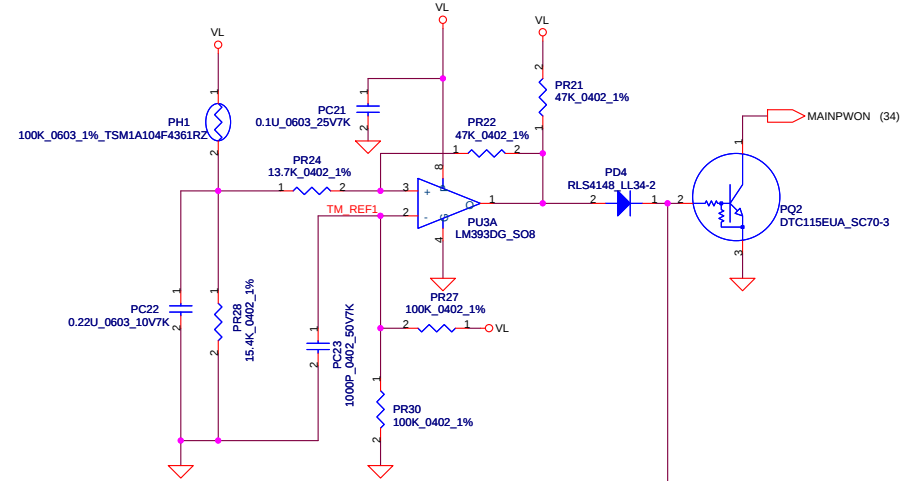
Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



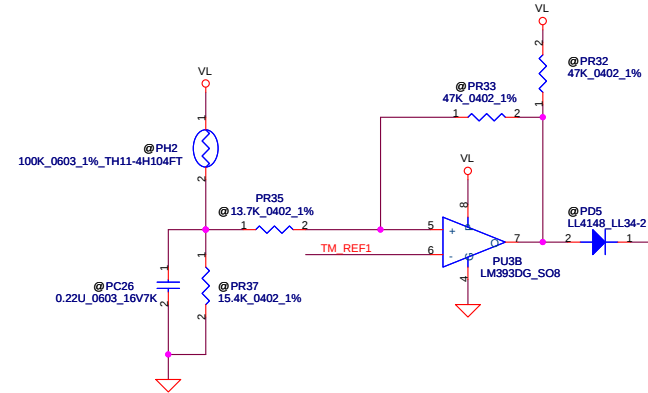
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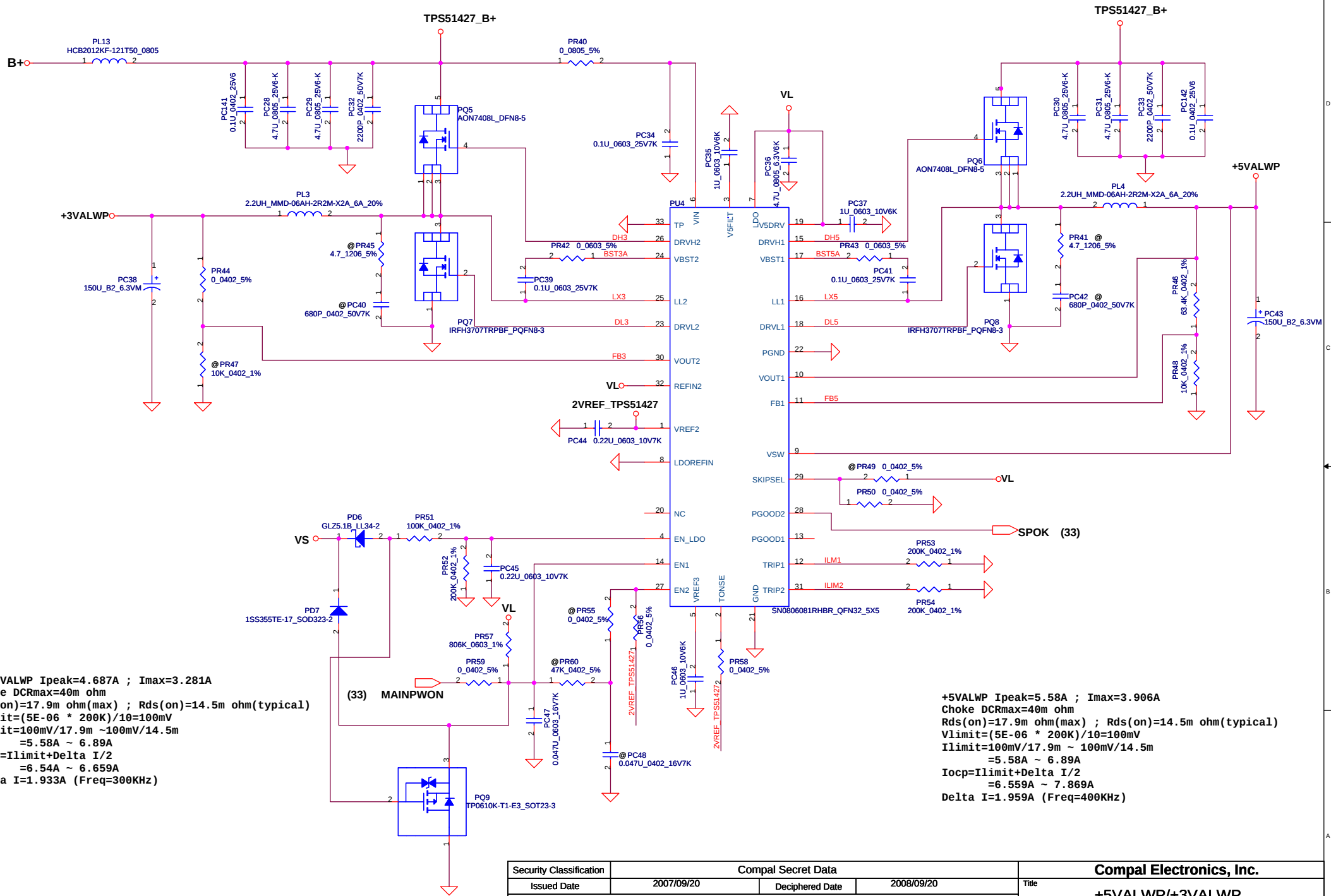
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C



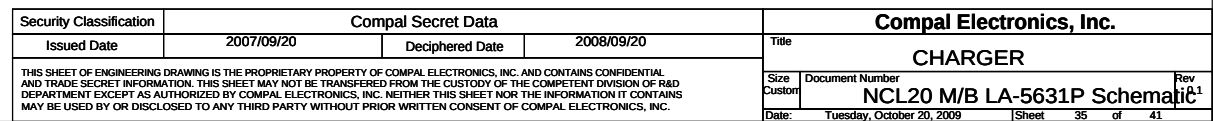
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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	
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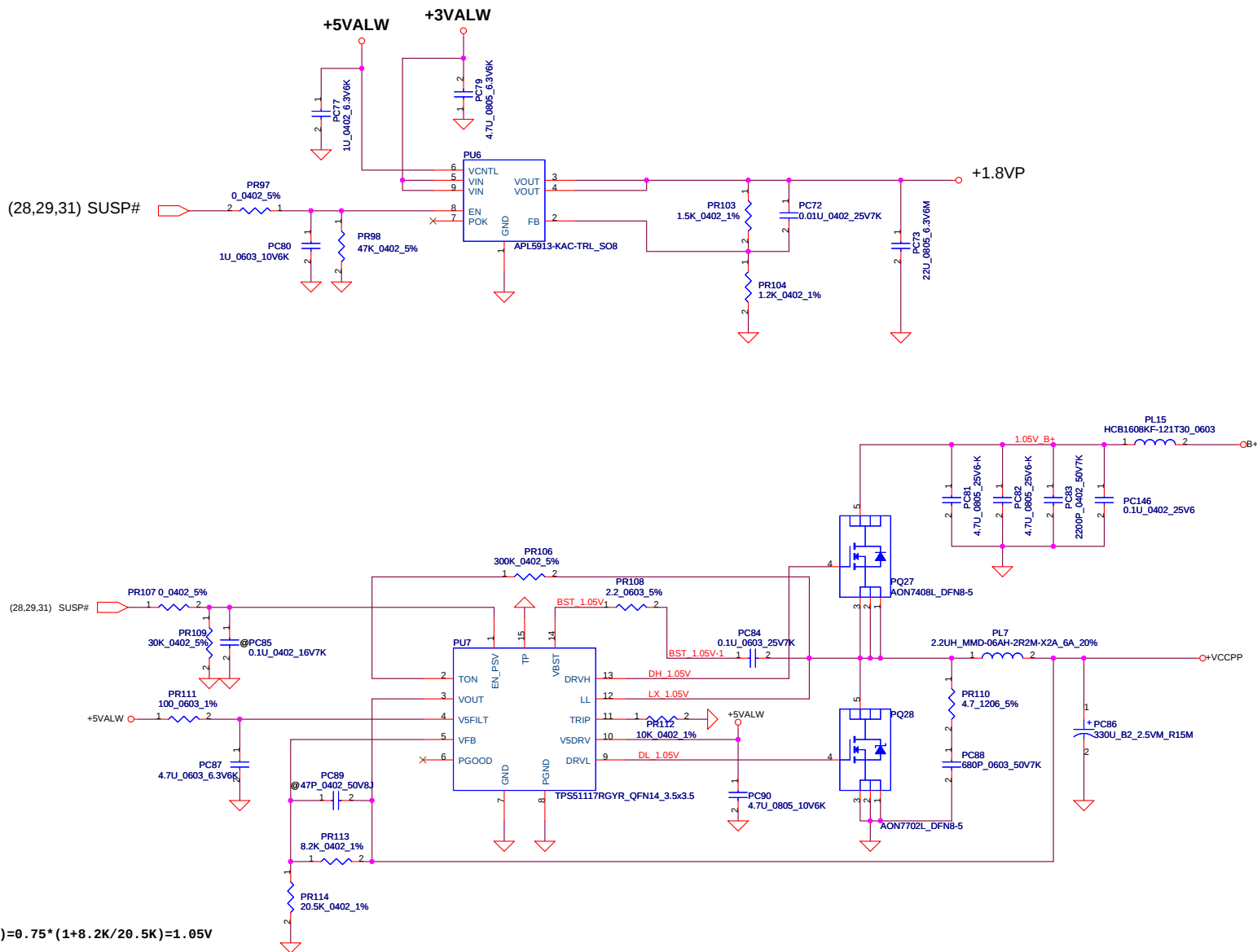


+3.3VALWP Ipeak=4.687A ; Imax=3.281A
Choke DCRmax=40m ohm
Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)
Vlimit=(5E-06 * 200K)/10=100mV
Ilimit=100mV/17.9m ~100mV/14.5m
=5.58A ~ 6.89A
Iocp=Ilimit+Delta I/2
=6.54A ~ 6.659A
Delta I=1.933A (Freq=300KHz)

+5VALWP Ipeak=5.58A ; Imax=3.906A
Choke DCRmax=40m ohm
Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)
Vlimit=(5E-06 * 200K)/10=100mV
Ilimit=100mV/17.9m ~ 100mV/14.5m
=5.58A ~ 6.89A
Iocp=Ilimit+Delta I/2
=6.559A ~ 7.869A
Delta I=1.959A (Freq=400KHz)

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<Vo=1.05V> VFB=0.75V

Vo=VFB*(1+PR113/PR114)=0.75*(1+8.2K/20.5K)=1.05V

Fsw=261KHz

Cout ESR=15m ohm Rdson(max)=17.9m Rdson(min)=14.5m

Ipeak=5A, Imax=5A, Iocp=6A

Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=1.72A

=>1/2DeltaI=0.86A

Vtrip=Rtrip*10uA=12K*10uA=0.12V

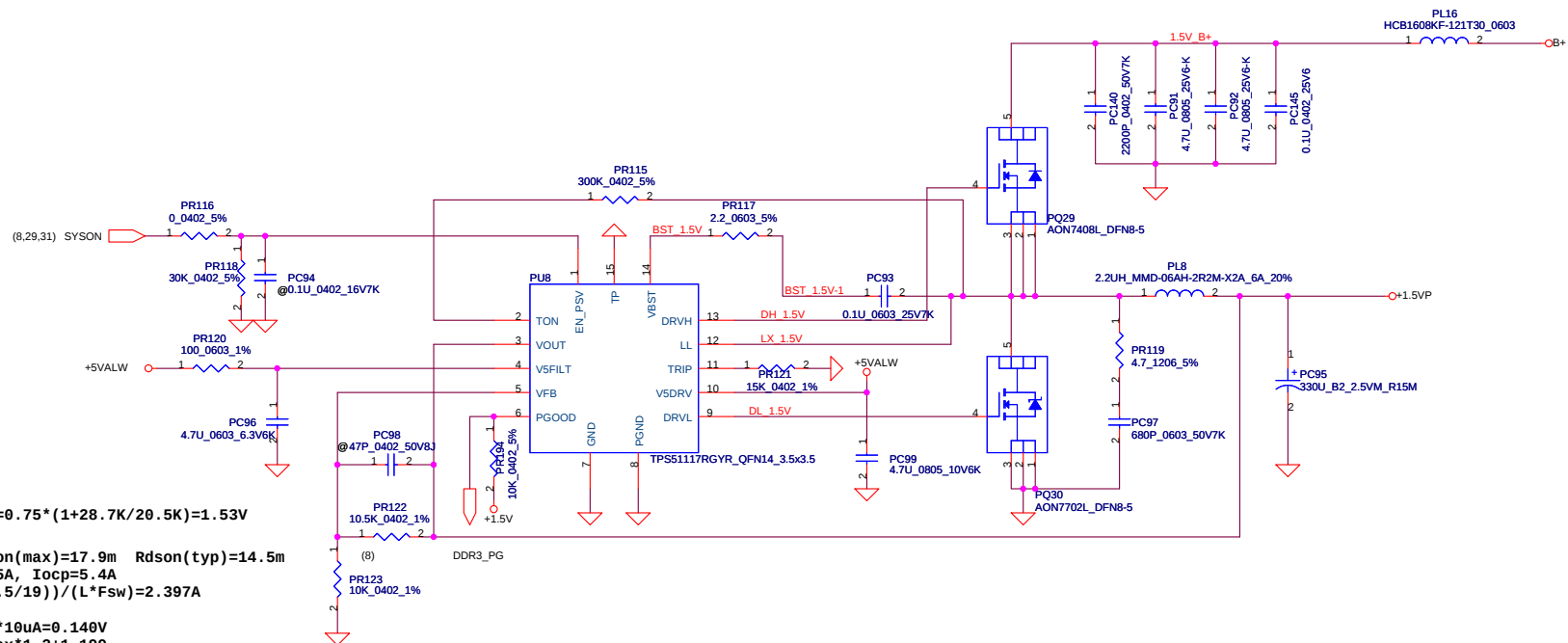
Iocpmin=Vtrip/Rdsonmax*1.2+0.86

=0.12/(0.0179*1.2)+0.86=6.446A

Iocpmax=(0.12/(0.0145*1.2))+0.86=7.756A

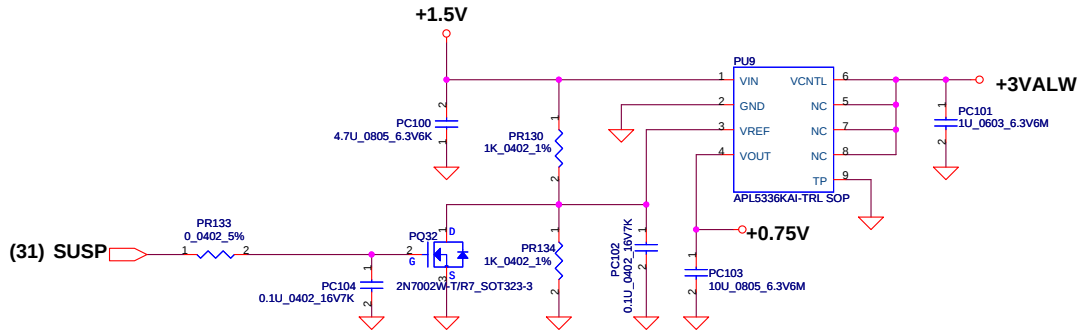
Iocp=6.446A~7.756A

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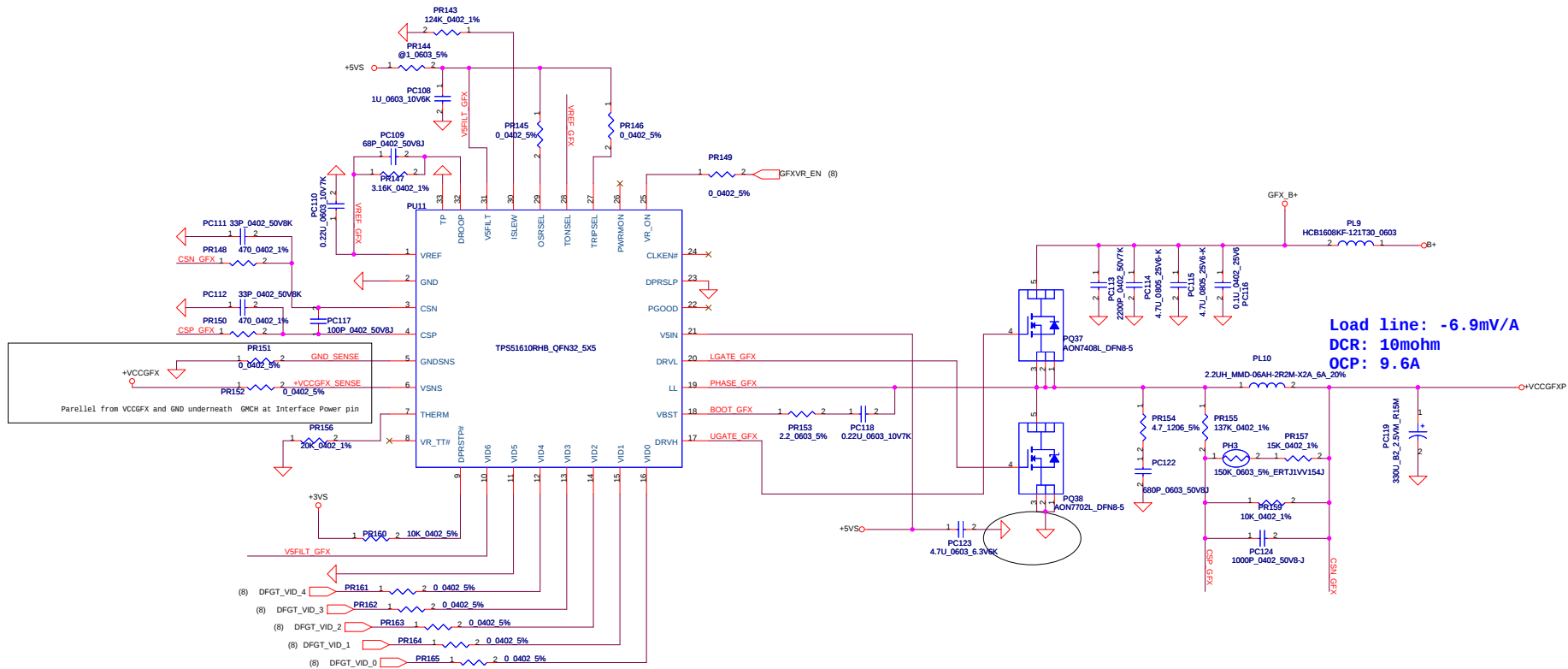
$V_o = 1.5V$ $V_{FB} = 0.75V$
 $V_o = V_{FB} * (1 + PR91/PR92) = 0.75 * (1 + 28.7K/20.5K) = 1.53V$
 $F_{sw} = 262KHz$
 $C_{out} ESR = 15m \text{ ohm}$ $R_{dson(max)} = 17.9m$ $R_{dson(typ)} = 14.5m$
 $I_{peak} = 4.5A$, $I_{max} = 3.15A$, $I_{ocp} = 5.4A$
 $\Delta I = ((19 - 1.5) * (1.5/19)) / (L * F_{sw}) = 2.397A$
 $\Rightarrow 1/2 \Delta I = 1.199A$
 $V_{trip} = R_{trip} * I_{ocp} = 14K * 10uA = 0.140V$
 $I_{ocpmin} = V_{trip} / R_{dsonmax} * 1.2 + 1.199$
 $= 0.140 / (0.0179 * 1.2) + 1.199 = 7.717A$
 $I_{ocpmax} = (0.140 / (0.0145 * 1.2)) + 1.199A = 9.245A$
 $I_{ocp} = 7.717A - 9.245A$

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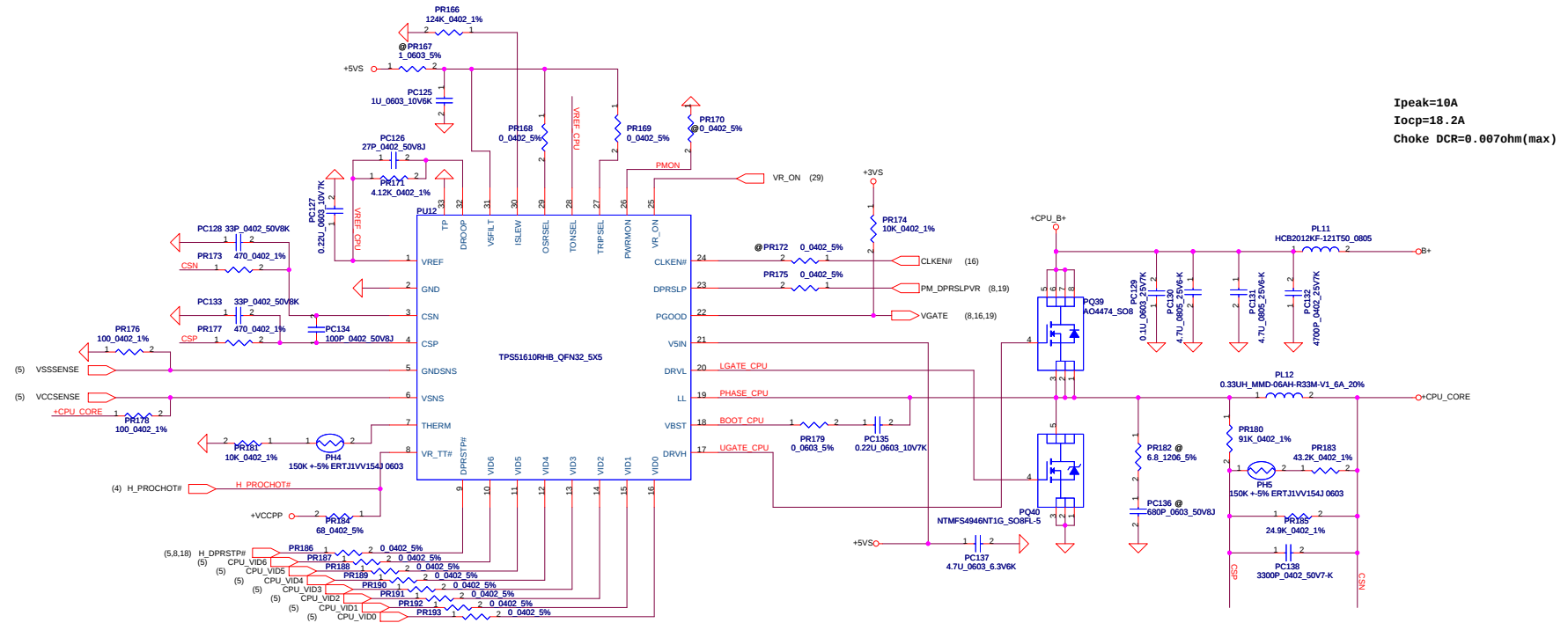


Ipeak=1A, Imax=0.7A

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change PR121 to 18K	modify 1.5VP OCP to 12A	0.2	44	Change PR121 to 18K	08/23	EVT2
2	Change GFXVCCP OCP	Change GFXVCCP OCP to 9.1A	0.2	46	Change PR147 PR155 PH3 PR157 PR159 PC124	08/23	EVT2
3	Improve VCCP Efficiency	Decrease L/S DCR value to 11m ohm	0.3	43	Change PQ28 from IRE3707 to AON7702L	09/16	DVT
4	Change VCCP OCP	Change VCCP OCP to 6.8A~8.4A	0.3	43	Change PR112 from 12K to 10K	09/16	DVT
5	Delete 0.75V enable signal	Delete 0.75V enable signal(reserve)	0.3	45	Delete PR131	09/16	DVT
6	Change GFXVCCP OCP	Change GFXVCCP OCP to 9.1A	0.3	46	Change PR147 PR155 PH3 PR157 PR159 PC124	09/16	DVT
7	Change PR121 to 15K	modify 1.5VP OCP to 10A	0.3	44	Change PR121 to 15K	09/16	DVT
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