

ZZZ1

LA-6001P

DAZ0CG00100

Compal Confidential

NBLB3/5 Schematics Document

Intel Clarksfield Processor with DDRIII + Ibex HM55

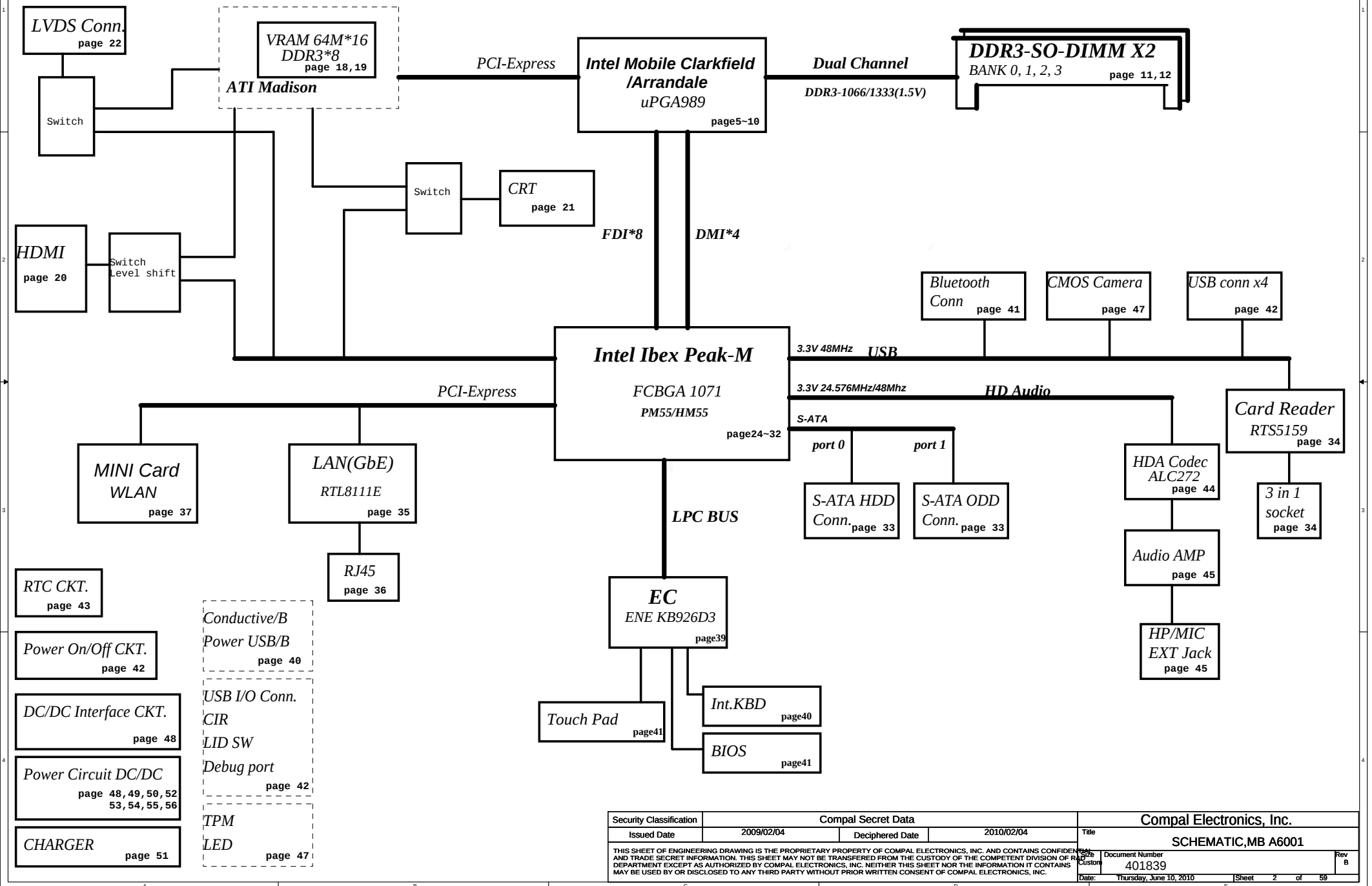
2010-04-28

REV:1.0

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				Custom	401839	B
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File Name : LA-6001P(Madison)

Clock Gen.
SLG8SP587
9LRS3199AKLFT
page23

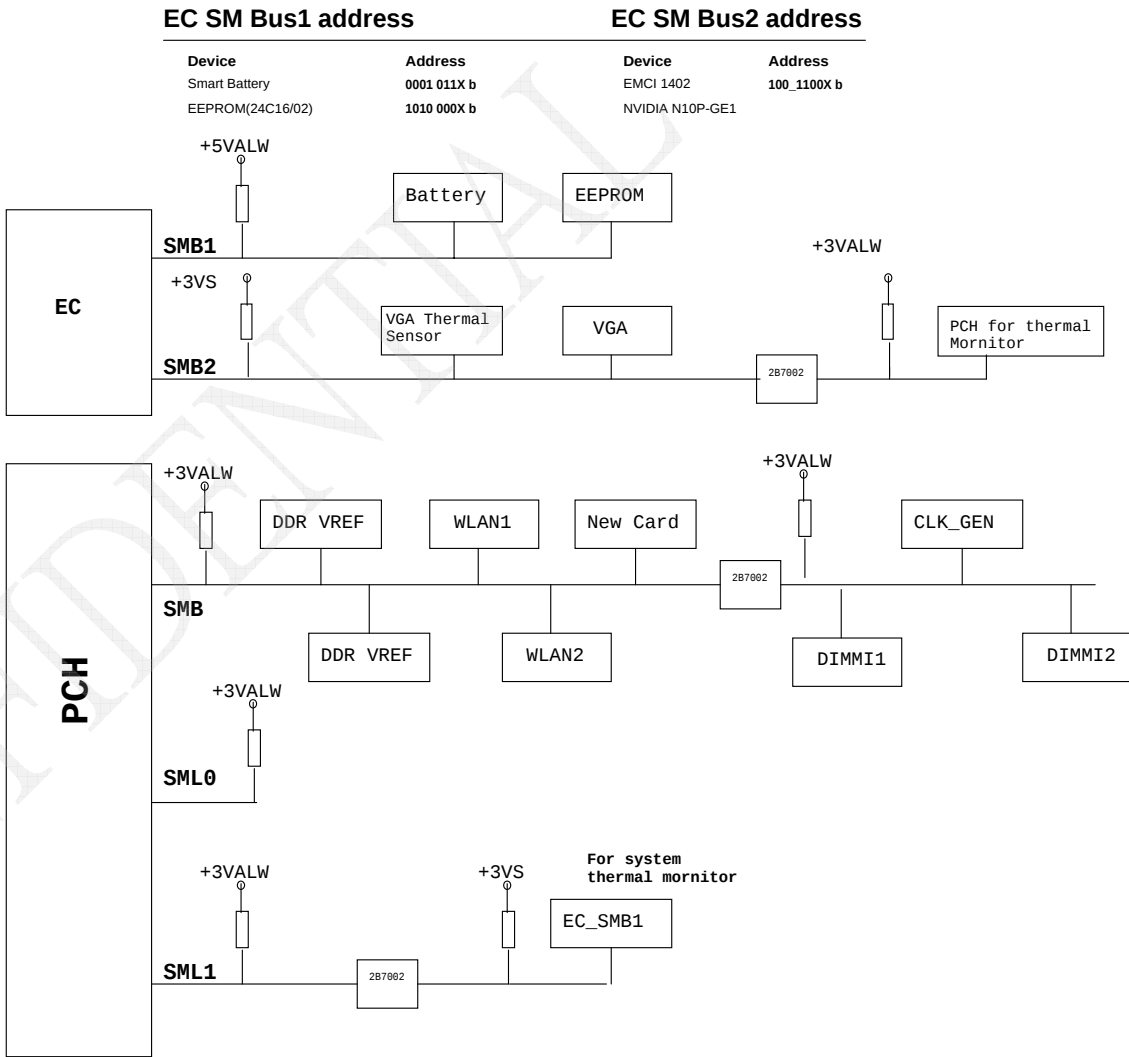


DDR3 Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS +1.1VS_VTT +1.5VS_VRAM
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

GPIO PIN Define

	ID3	ID2	ID1	ID0
NBLB2(1100)	R358	R361	R766	R765
Reserve (1101)	X	X	X	X
Reserve (1110)	X	X	X	X
Reserve (1111)	X	X	X	X
NBLB1 (0000)	R353	R350	R766	R765
Reserve(0001)	X	X	X	X
Reserve(0010)	X	X	X	X
Reserve(0011)	X	X	X	X
Reserve(0100)	X	X	X	X
Reserve(0101)	X	X	X	X
Reserve (0110)	X	X	X	X
Reserve (0111)	X	X	X	X
Reserve (1000)	X	X	X	X
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Reserve (1010)	X	X	X	X
Reserve (1011)	X	X	X	X



VGA (Madison)

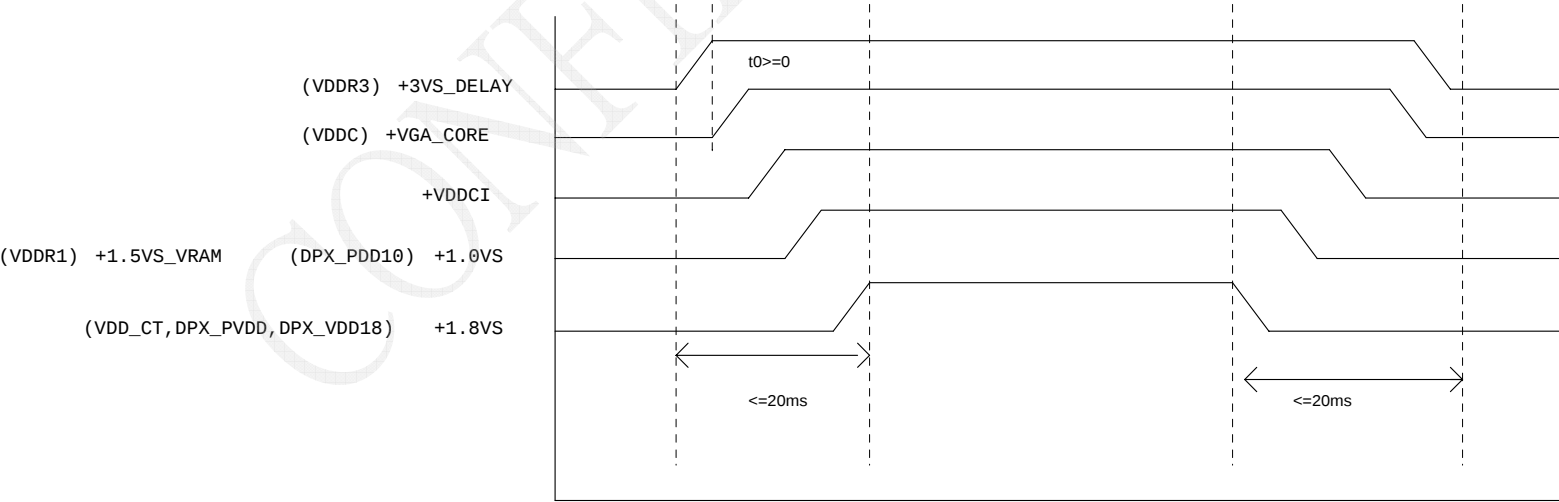
State \ power plane	+1.8VS +1.5VS_VRAM	+3VS_DELAY +VGA_CORE +1.1VS
S0	0	0
S1	0	0
S3	X	X
S5 S4/AC	X	X
S5 S4/ Battery only	X	X
S5 S4/AC & Battery don't exist	X	X

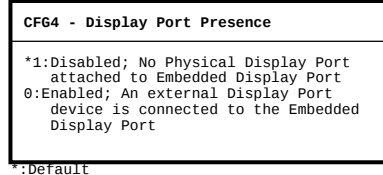
POWER UP/DOWN Sequence

47132_madison_ds_nda_1.04

Madison sequence

- Power-Up/Down Sequence
Madison has the following requirements with regards to power supply sequencing to avoid damaging the ASIC.
- 1, All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.
 - 2, VDDR3 should ramp-up before or simultaneously with VDDC.
 - 3, For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.
 - 4, The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.
 - 5, VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)
 - 6, For power-down, reversing the ramp-up sequence is recommended.





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SA_ODT[0] AD8
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SA_DM[3] M7
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IC:AUB_CFD_rPGA,R0P9
CONN@

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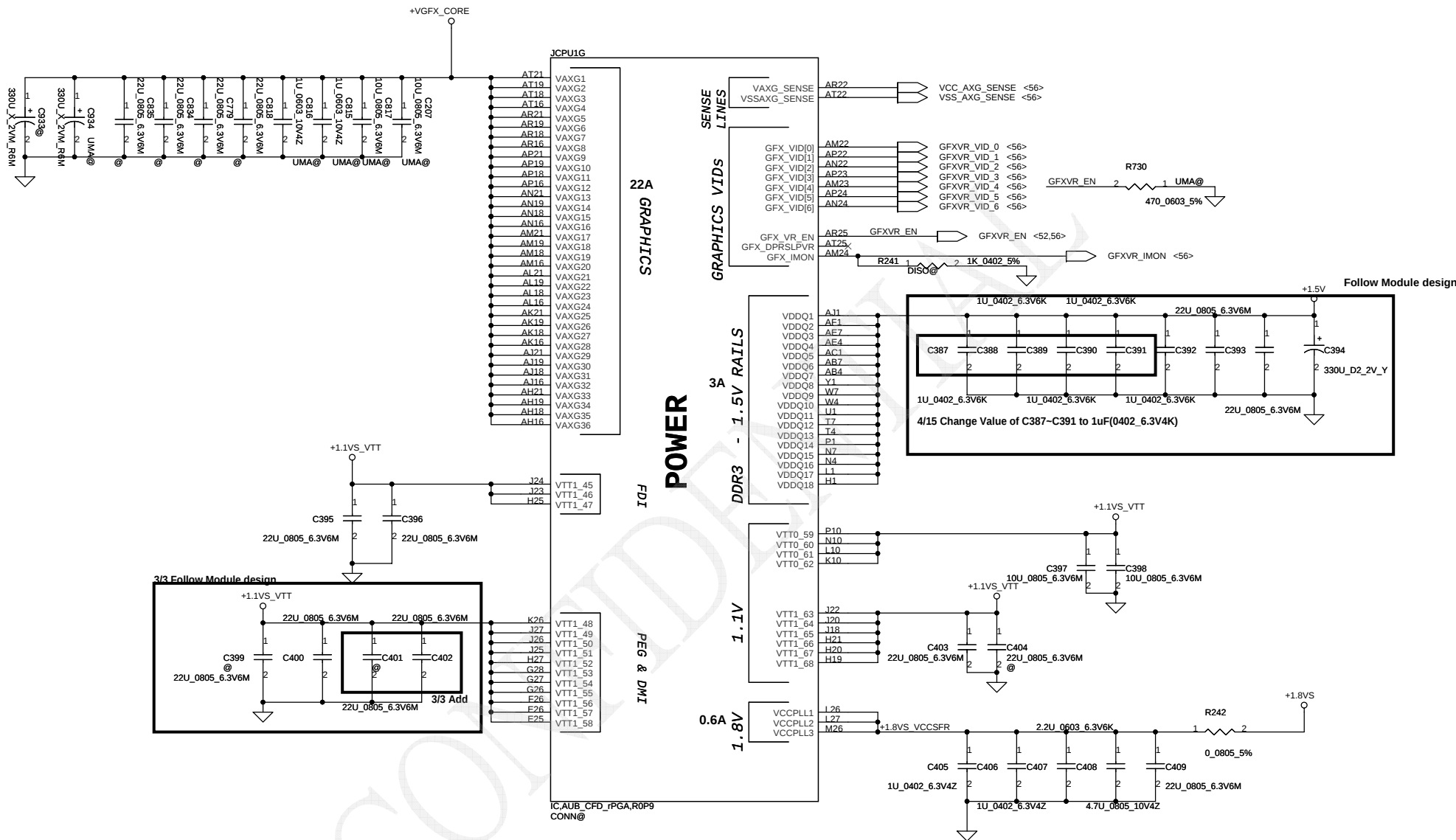
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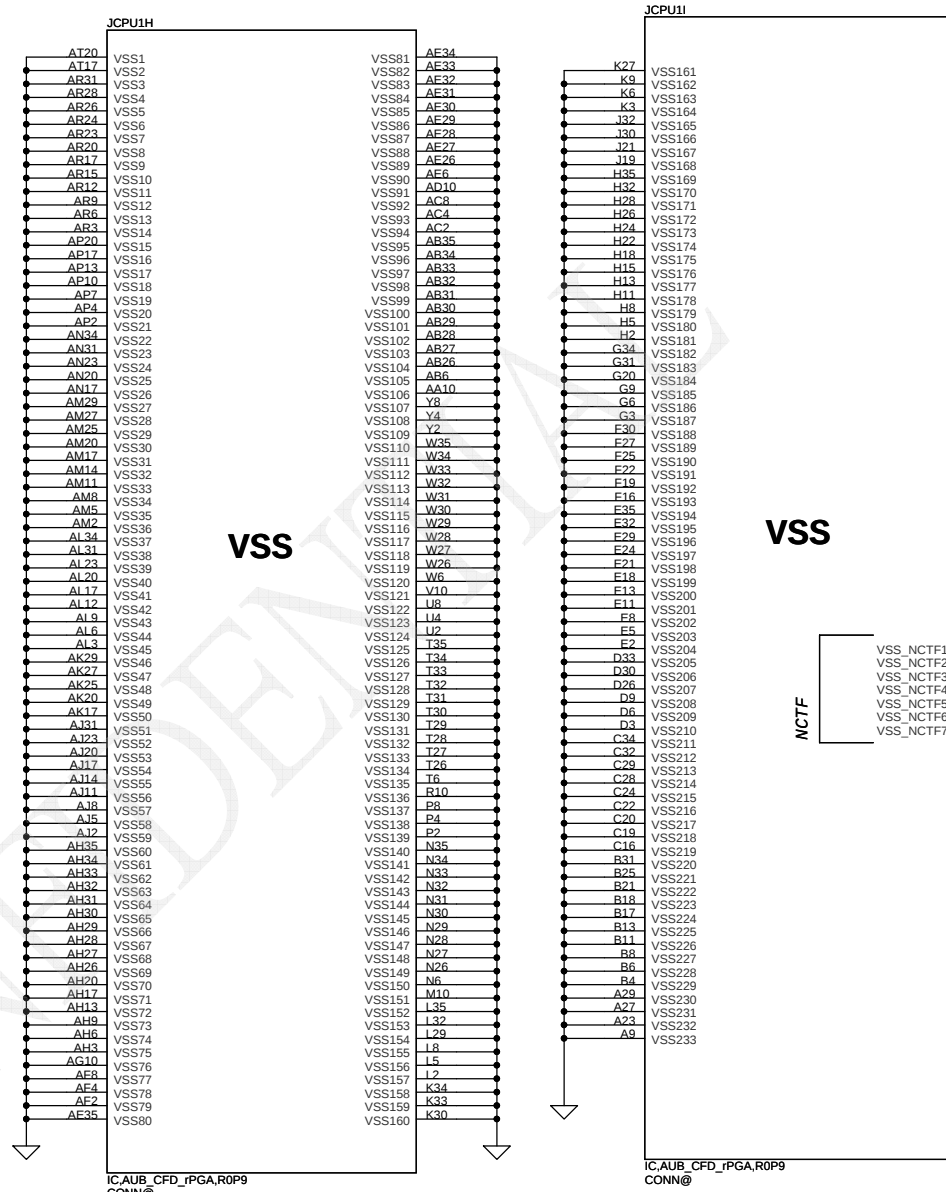
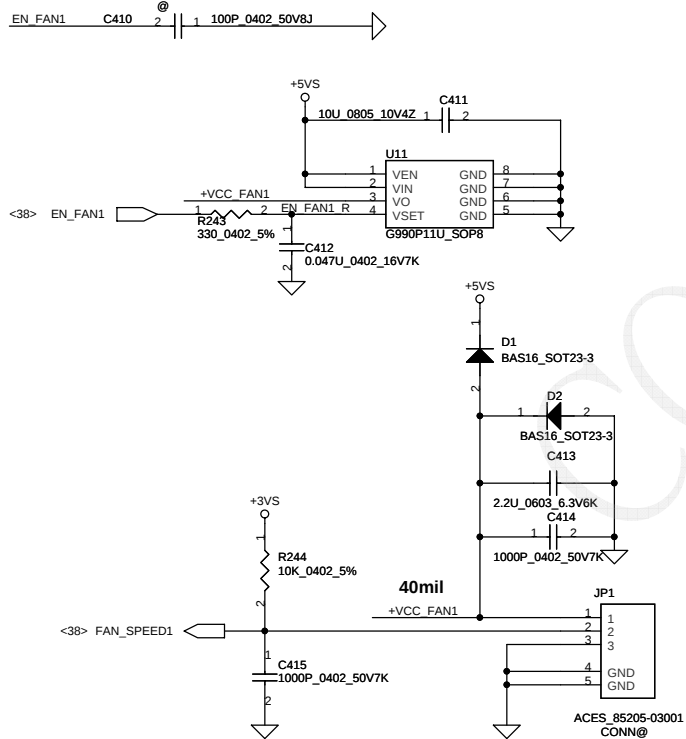
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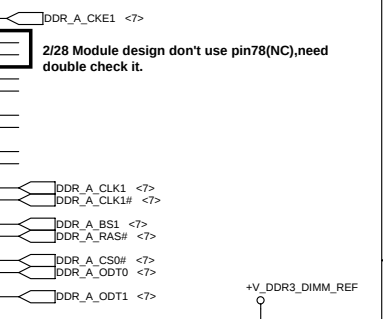
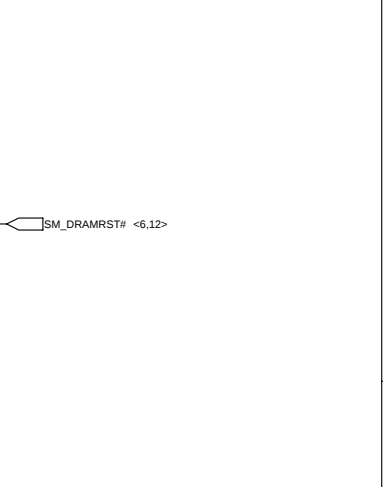


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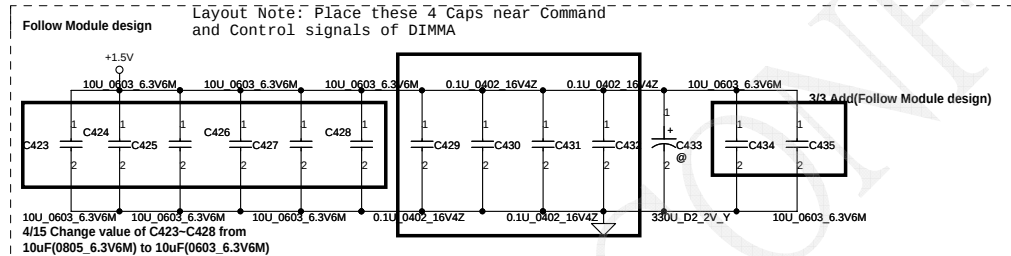
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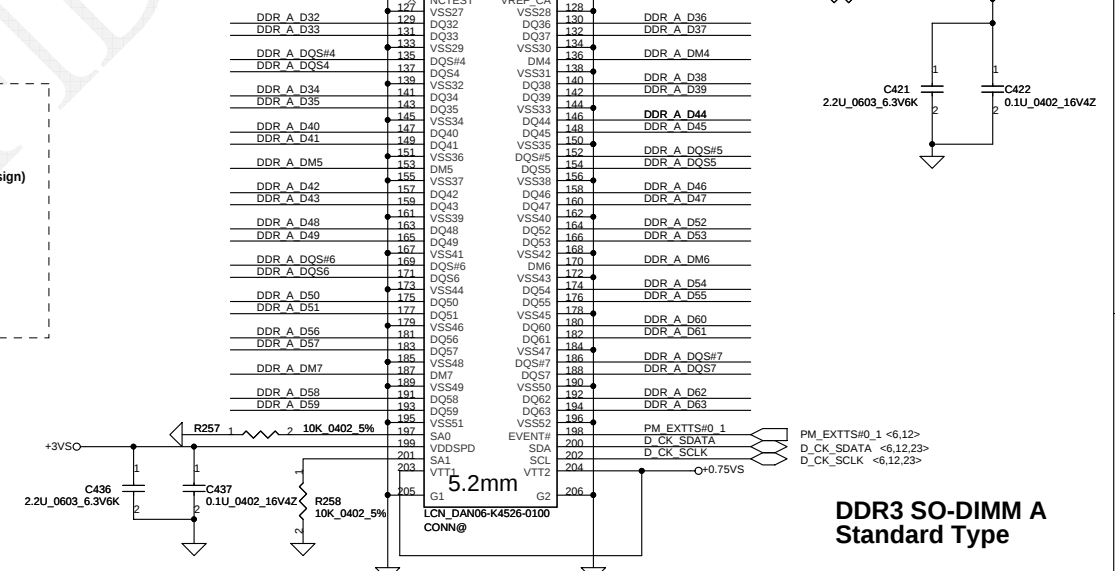
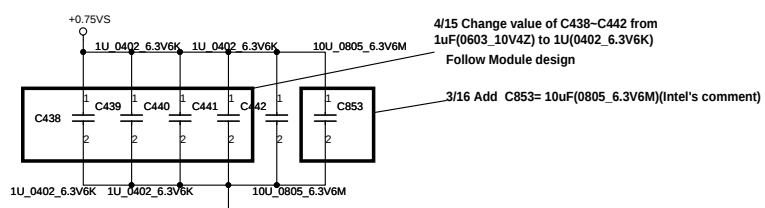
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				Date	Thursday, June 10, 2010
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Layout Note:
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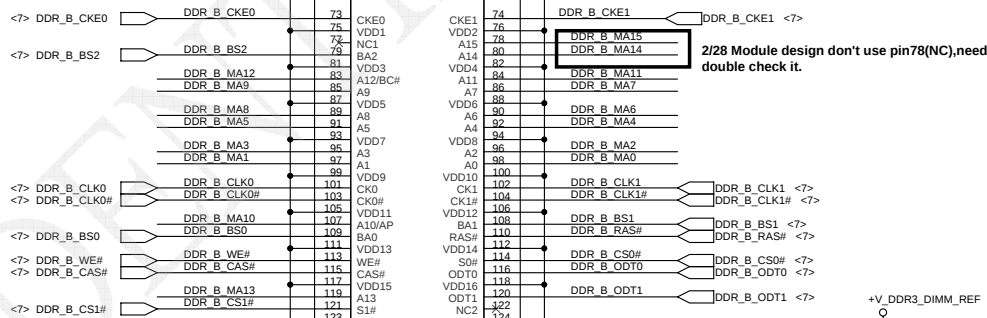
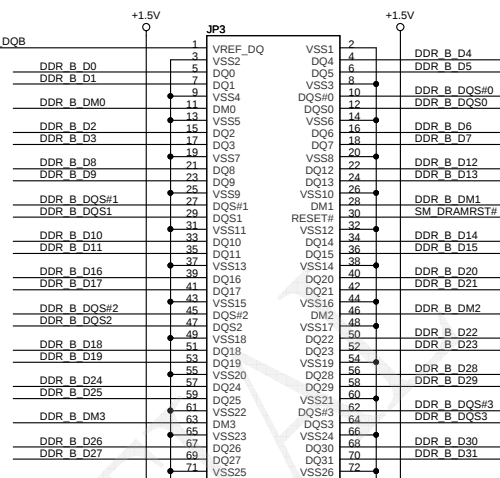
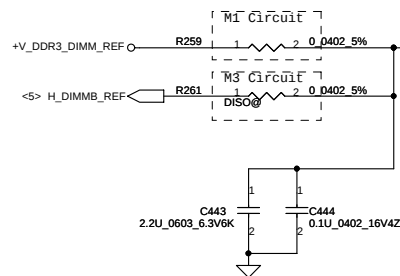
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				Docu- ment Number		
				401839		
				Rev B		
				Date: Thursday, June 10, 2010		
				Sheet 11 of 59		

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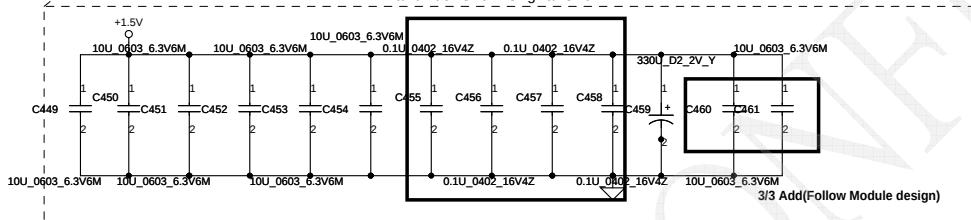
2098/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details



2/28 Module design don't use pin78(NC), need double check it.

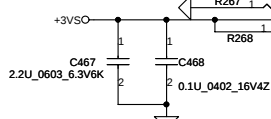
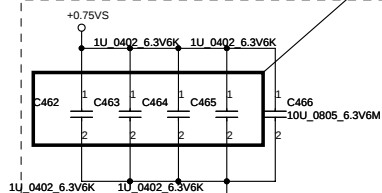
Layout Note:
Place near JP3

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



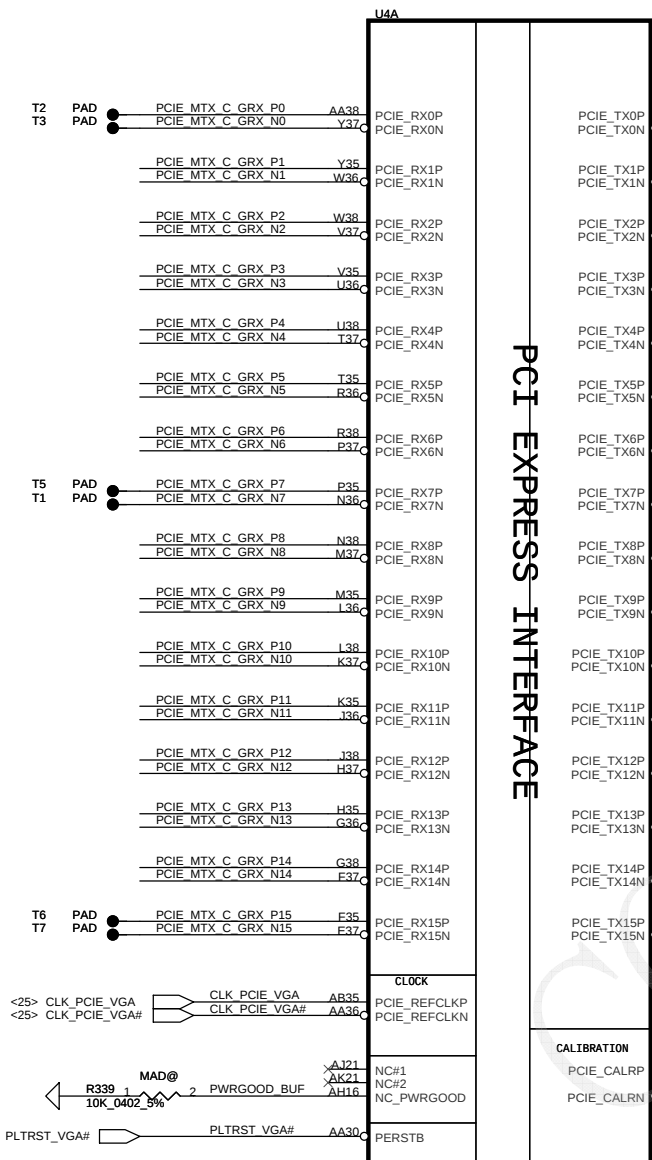
Layout Note:
Place near JP3.203 & JP3.204

4/15 Change value of C462-C465 from 1uF(0603_10V4Z) to 1U(0402_6.3V6K)
Follow Module design



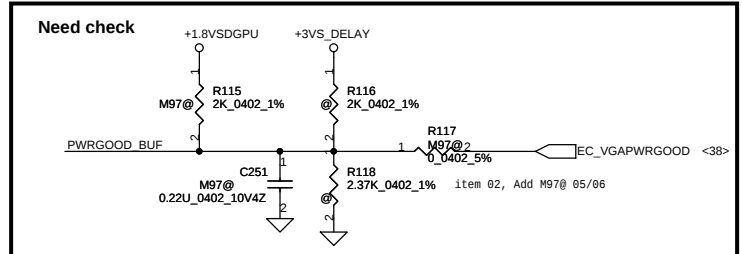
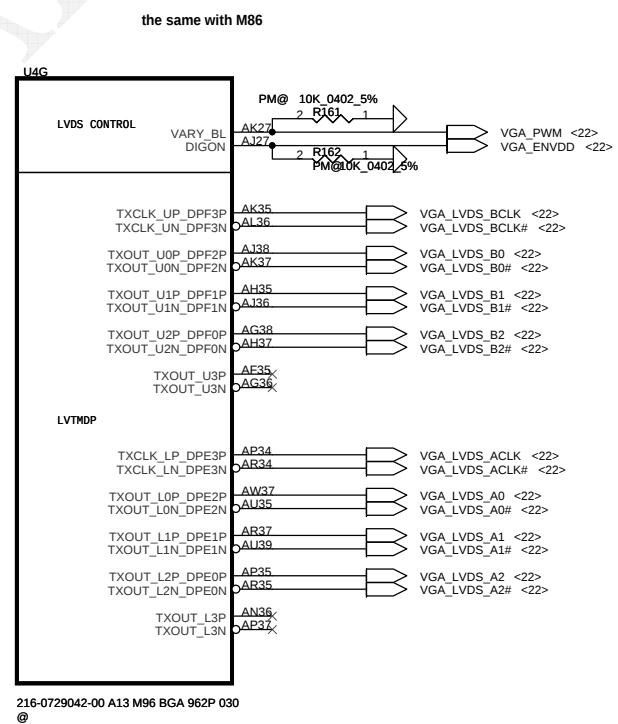
DDR3 SO-DIMM B
Standard Type

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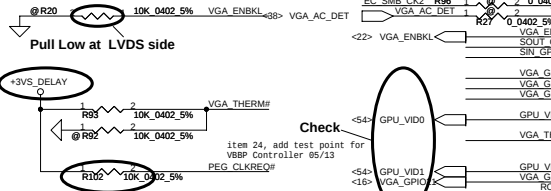
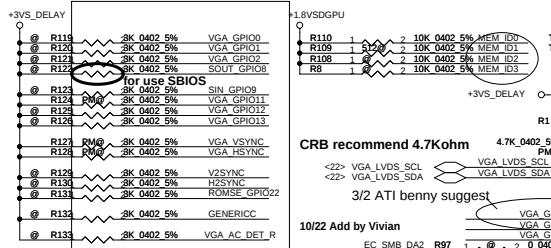
<S> PCIE_MTX_C_GRX_N[0..15] PCIE MTX C GRX N[0..15]
<S> PCIE_MTX_C_GRX_P[0..15] PCIE MTX C GRX P[0..15]
<S> PCIE_GTX_C_MRX_N[0..15] PCIE GTX C MRX N[0..15]
<S> PCIE_GTX_C_MRX_P[0..15] PCIE GTX C MRX P[0..15]

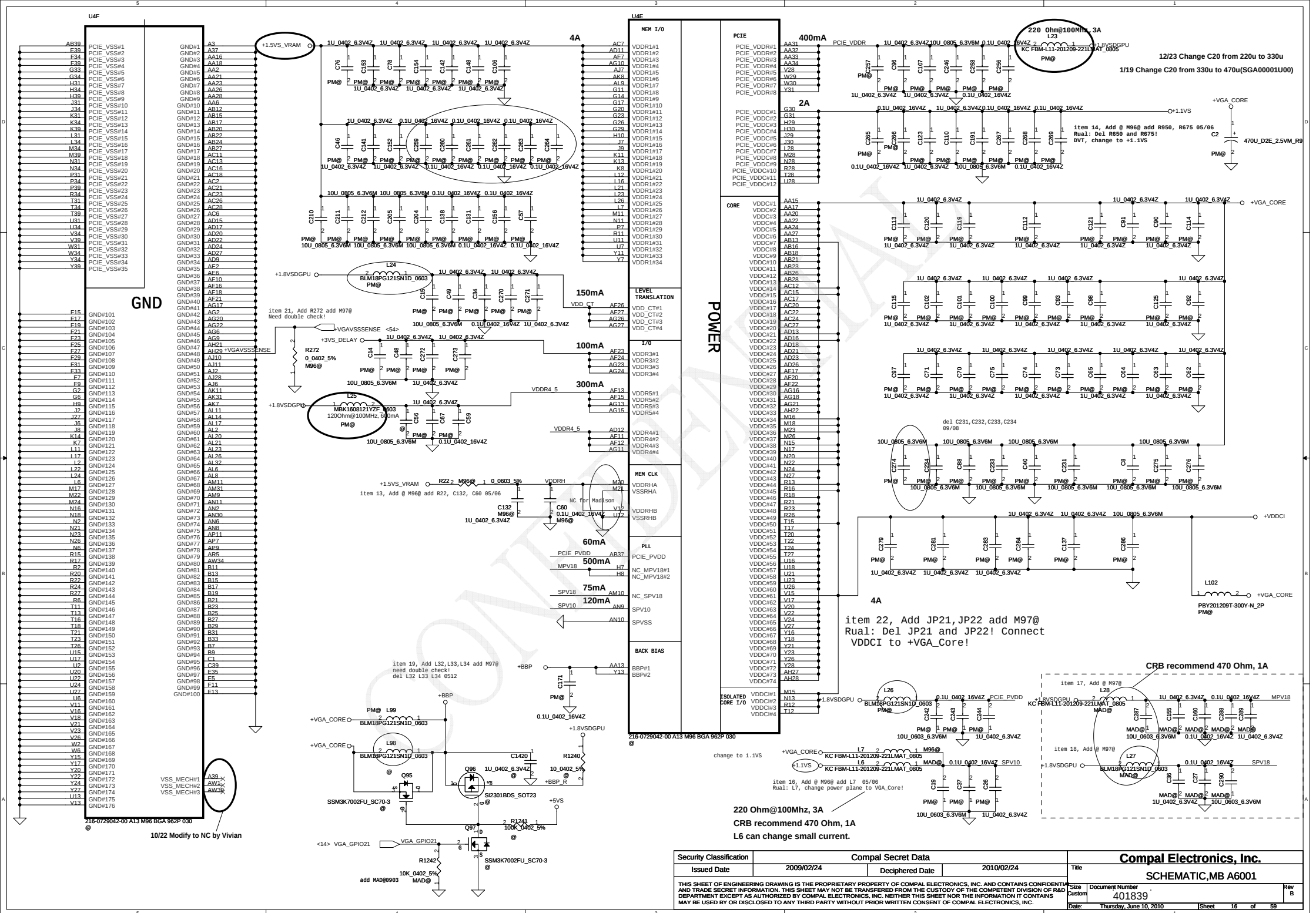
U4
SA00002UQ50
216-0729042 A13 M96-M2 FCBGA962 0FA M96@
U4
SA00003M320
216-0772000 A11 MADISON PRO 030 MADVGA@
U4
SA00003MC20
216-0774007 A11 PARK XT M2 962P 030 PARKVGA@

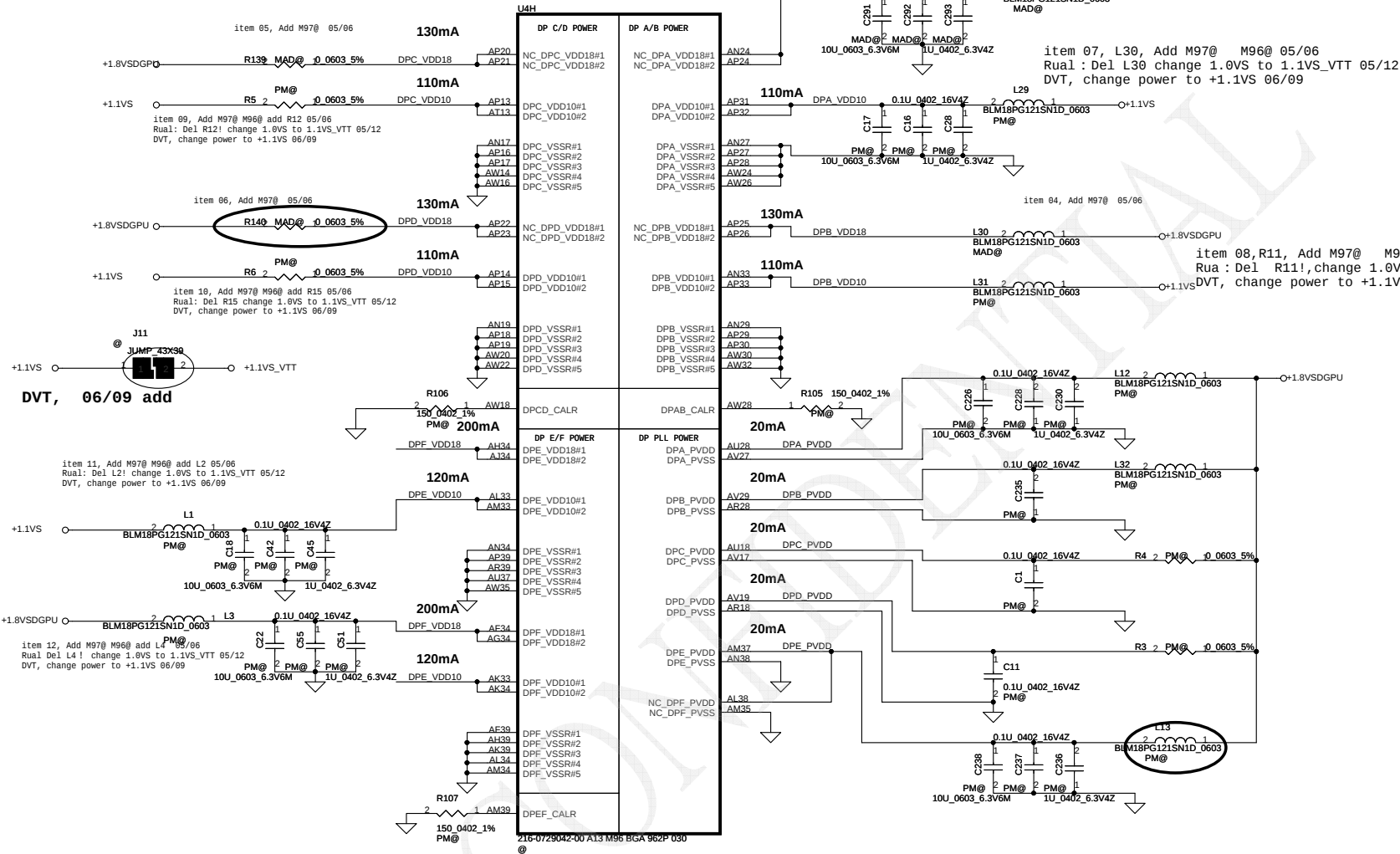


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				Date: Thursday, June 10, 2010	Sheet 13 of 59

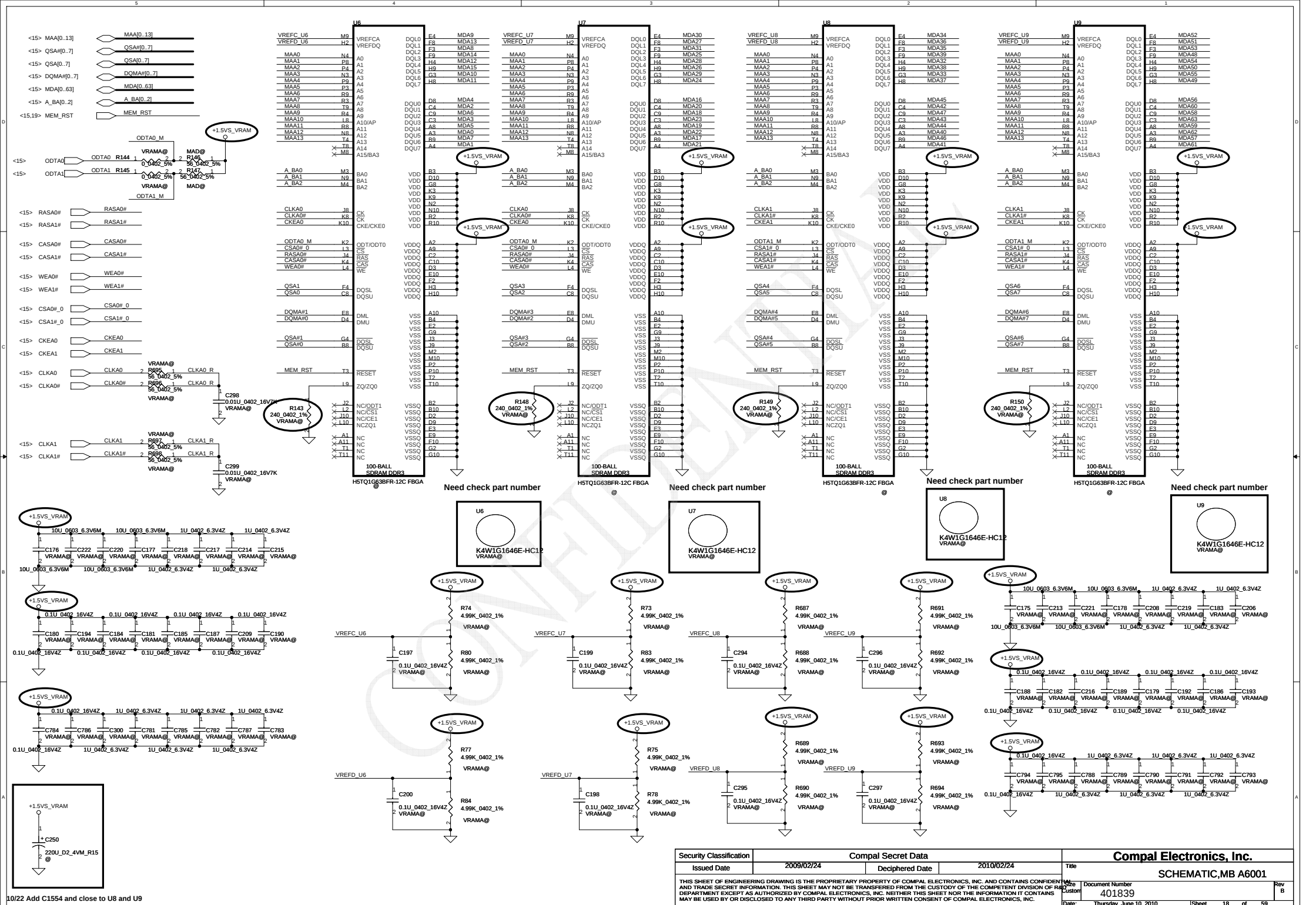
Strap Name	Pin Straps description	Default Value
TX_PWRS_EN#	GPIO0 Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN#	GPIO1 PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	0
BIF_GEN2_EN	GPIO2 0: Advertises the PCI-E device as 2.5 GT/s capable at power-on 1: Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
GPIO23 GPIO21	Reserved	0
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11 a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22 Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC 00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	1
GENERICC H2SYNC	Reserved	0
VIP_DEVICE STRAP_EN	V2SYNC Reserved	0

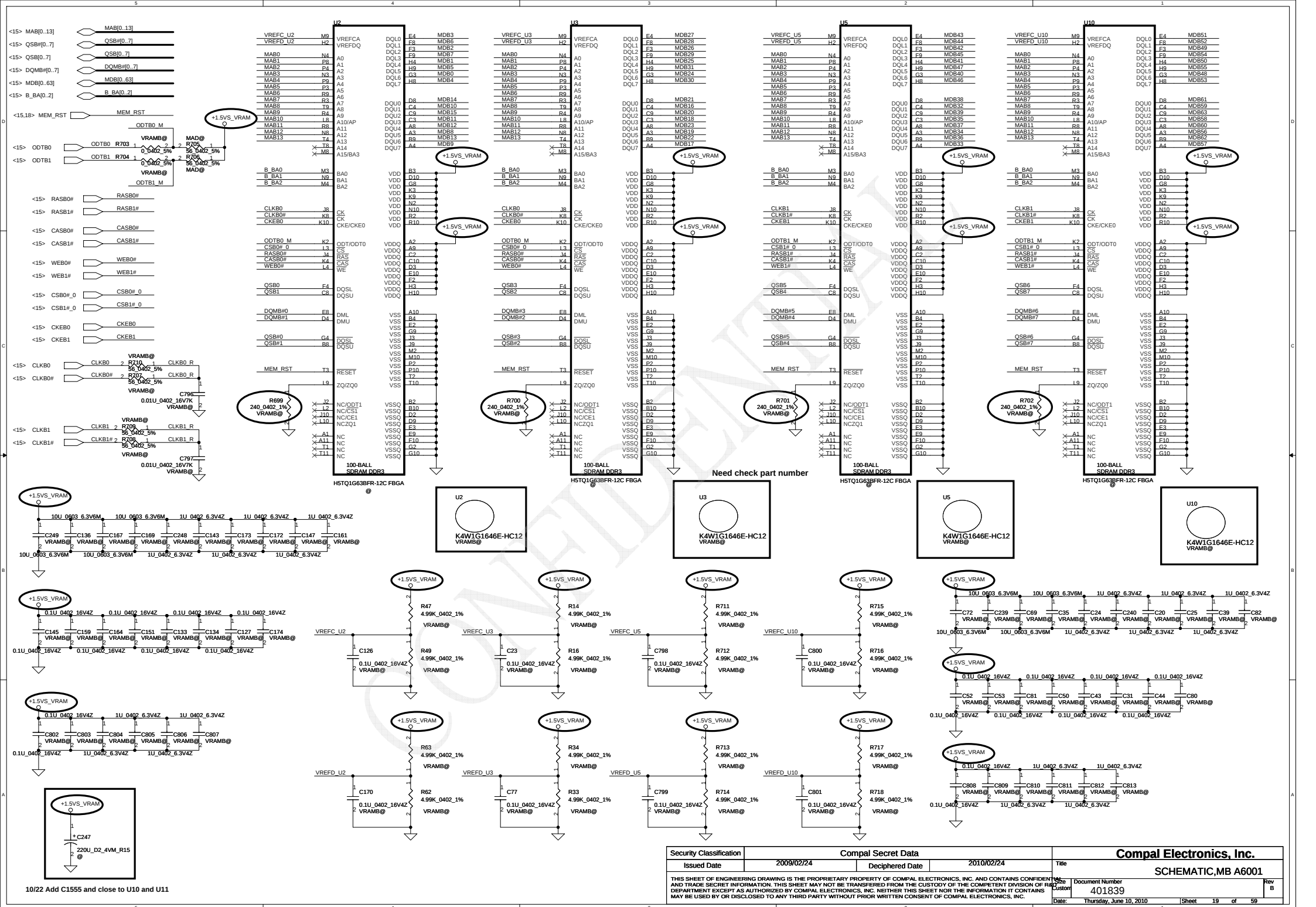




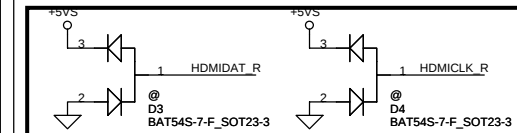
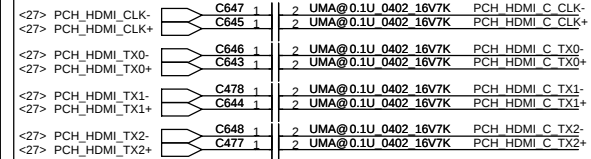
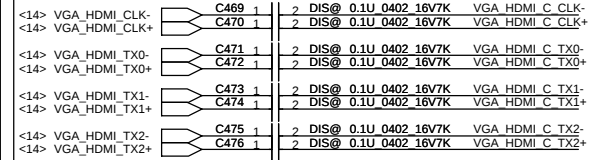


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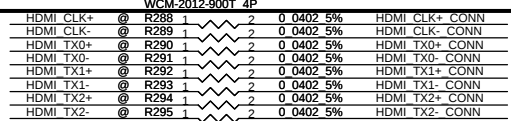
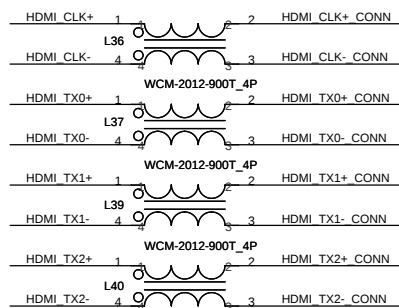
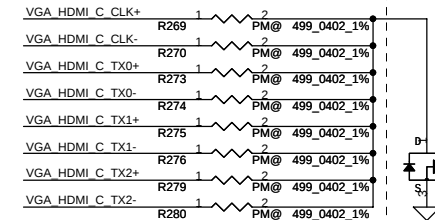




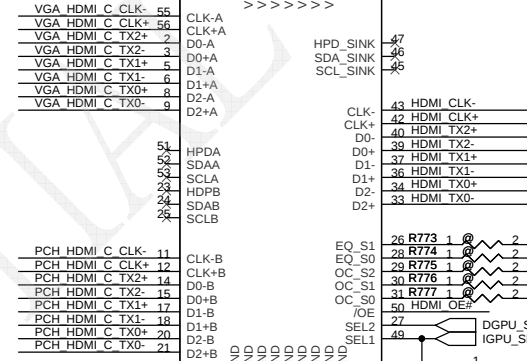
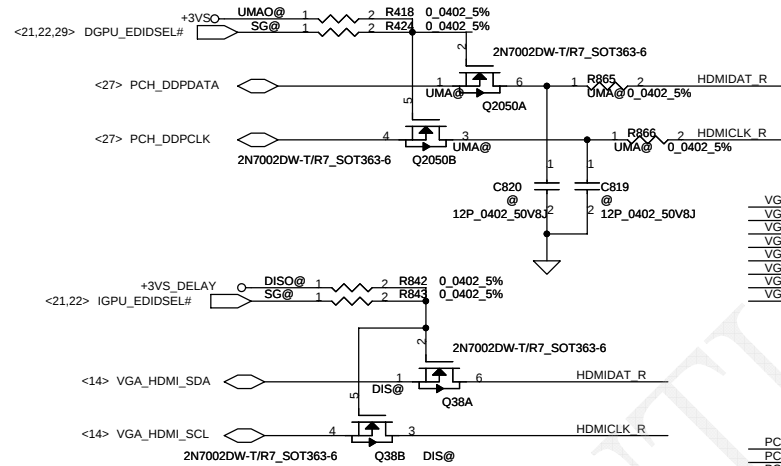
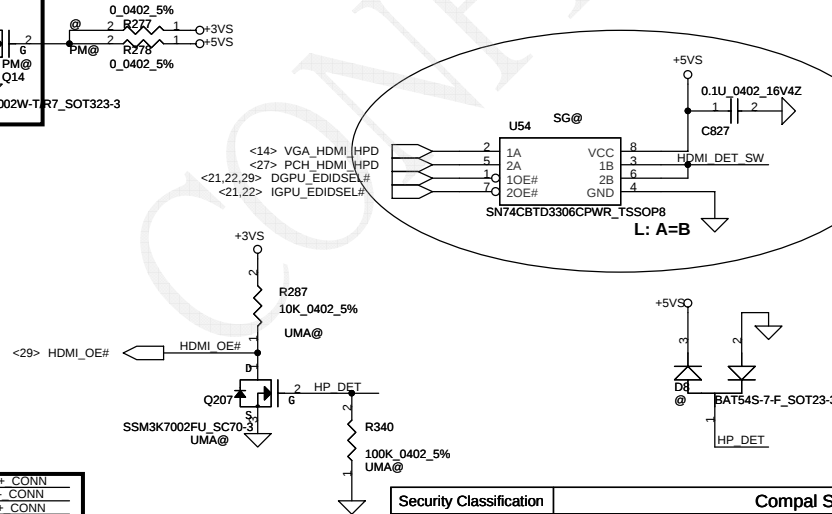
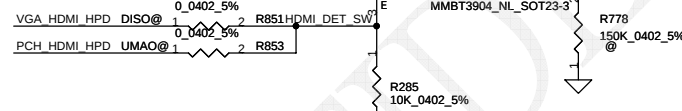
have the pull high on PCH/VGA side



TMDS pull down (500ohm) resistors G9x only

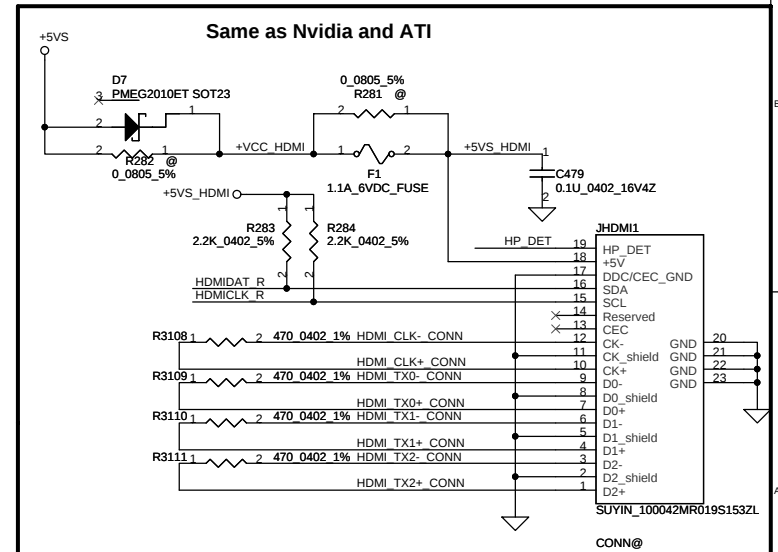


DVT, change HDMI detec 06/09



DGPU_SELECT#
L: 0 -> Y(Madison)
H: 1 -> Y(PCH)

OE--SEL1--SEL2--Result
1---X---X---Hi-Z
0---1---X---A active
0---0---1---B active
0---0---0---B all port dis



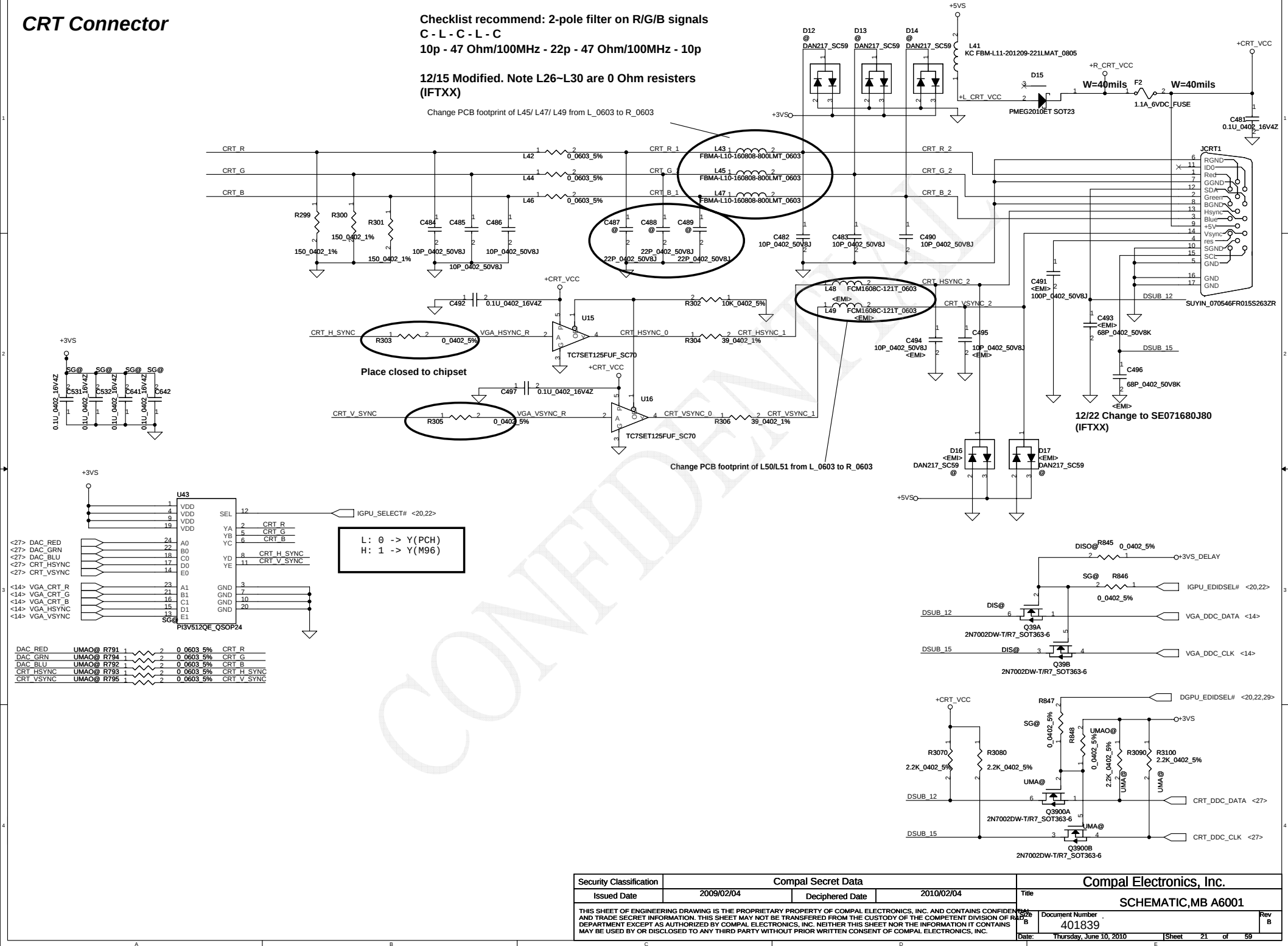
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CRT Connector

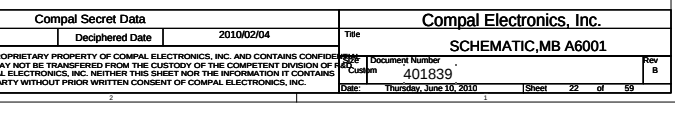
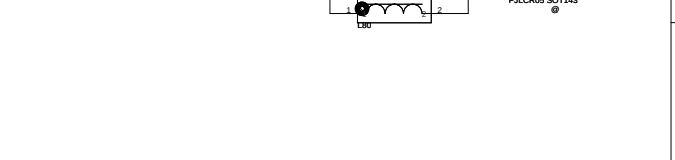
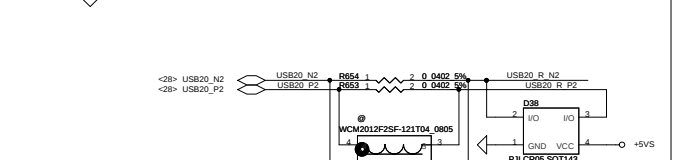
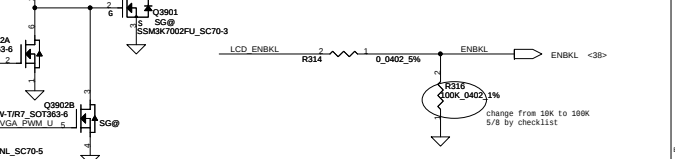
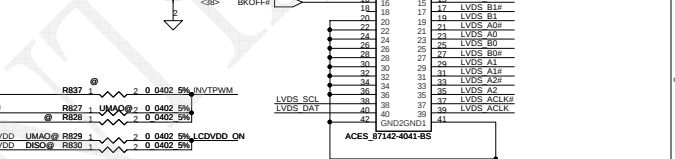
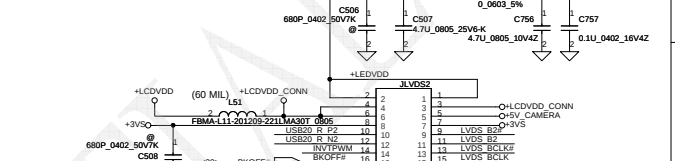
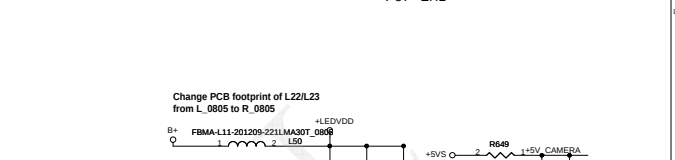
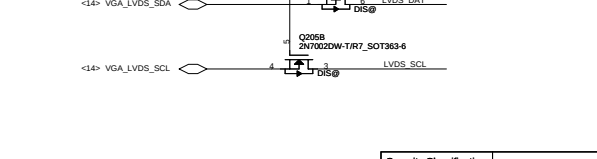
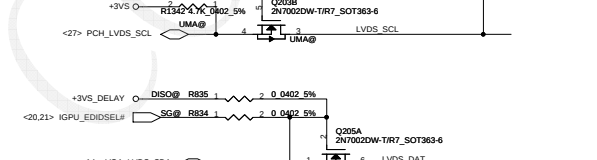
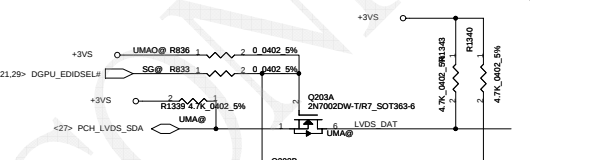
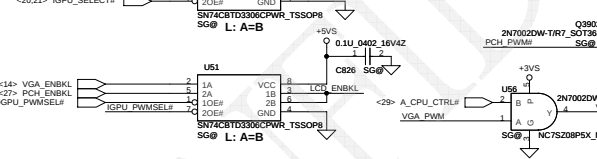
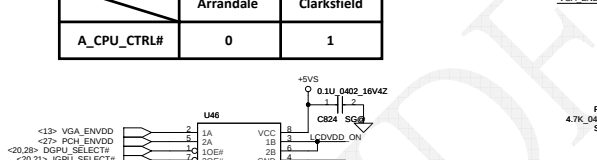
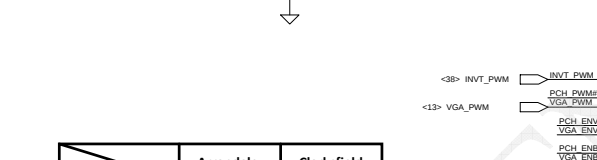
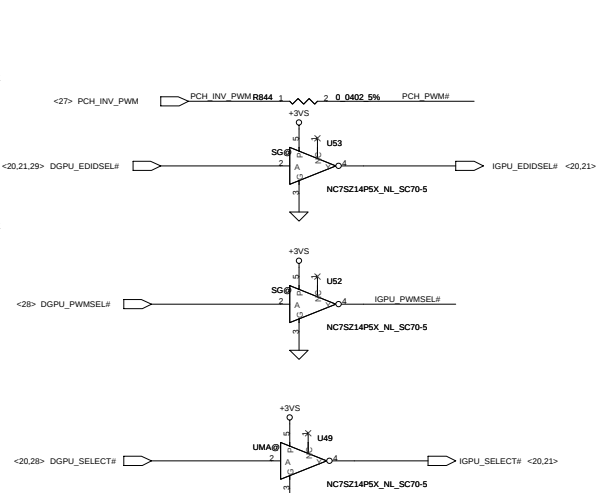
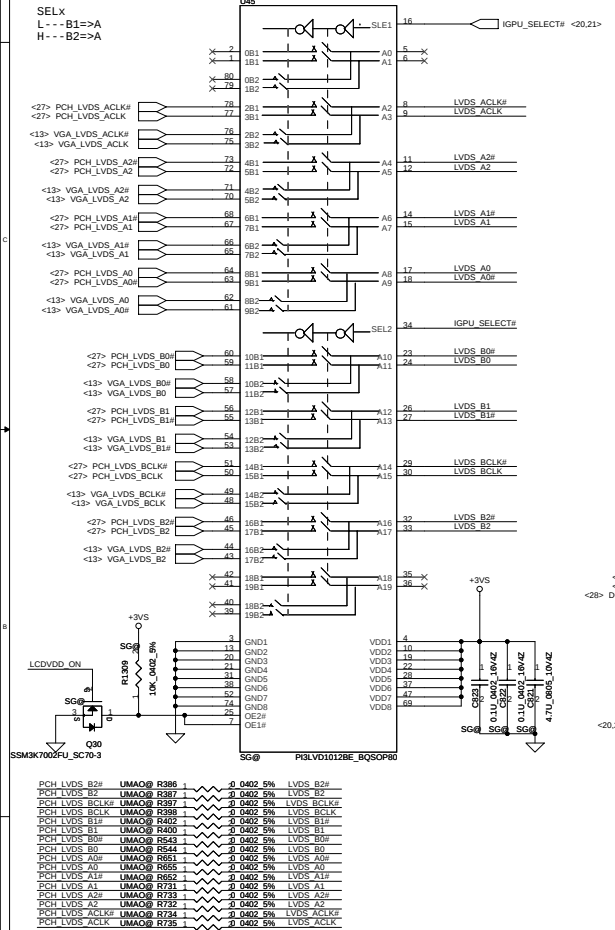
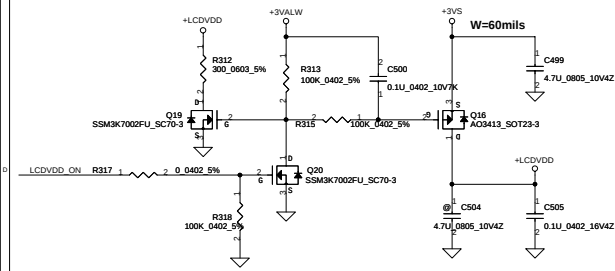
Checklist recommend: 2-pole filter on R/G/B signals
C - L - C - L - C
10p - 47 Ohm/100MHz - 22p - 47 Ohm/100MHz - 10p

12/15 Modified. Note L26~L30 are 0 Ohm resistors (IFTXX)

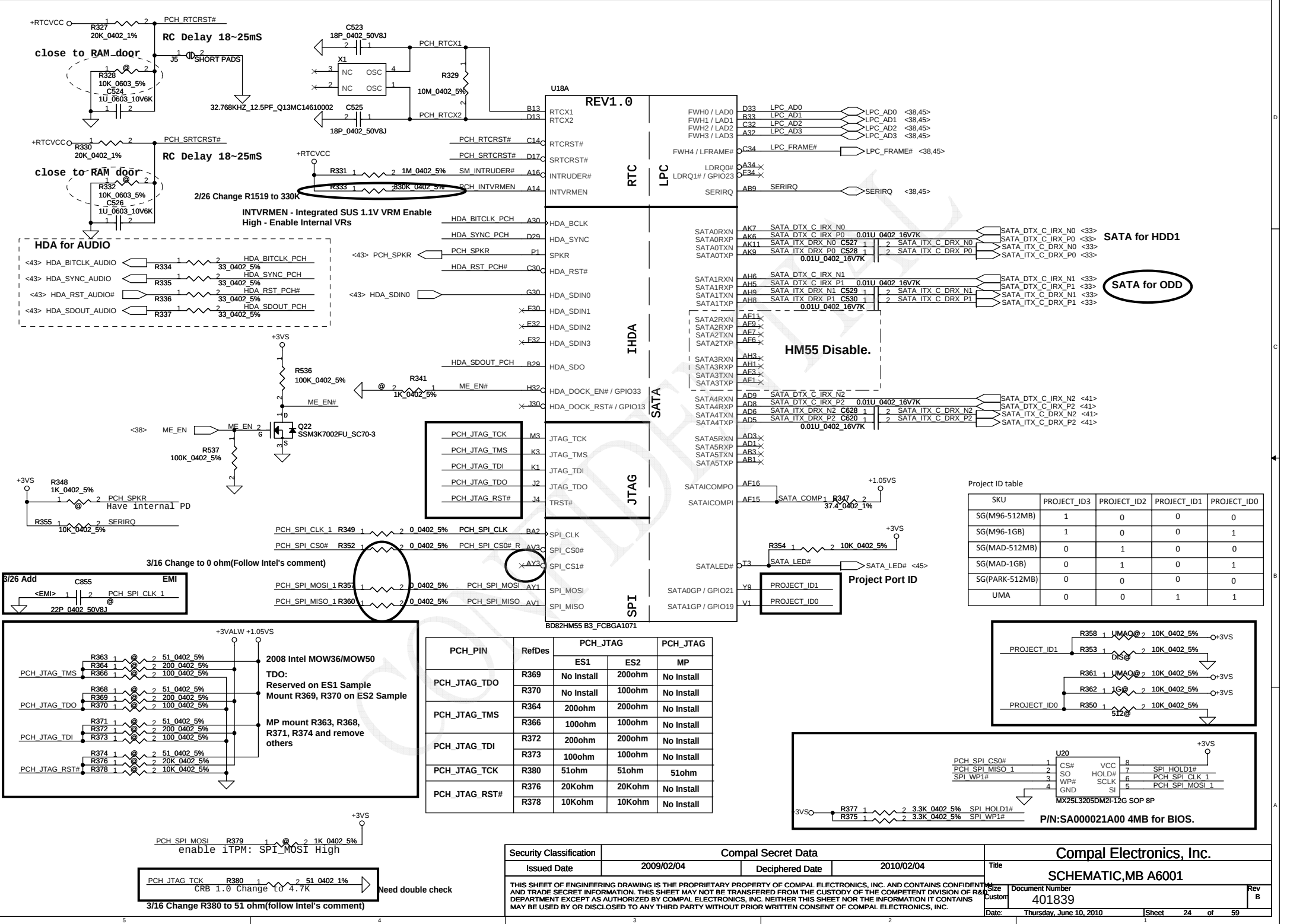
Change PCB footprint of L45/ L47/ L49 from L_0603 to R_0603



LCD POWER CIRCUIT



	Arrandale	Clarkfield
A_CPU_CTRL#	0	1



For Wireless LAN

For PCIE LAN

For Wireless LAN

For PCIE LAN

REV1.0

PCI-E*

From CLK BUFFER

CLKOUT FLEX

Project ID		
ID1	ID0	Project
0	0	Future
0	1	JV

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1. Connect Directly EXPRESS CARD, MINI12
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP

3/16 Add by Vivian(follow Intel's comment)

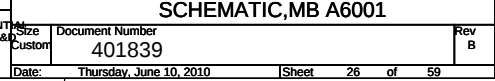
2/28 Follow Module design Rev1.0

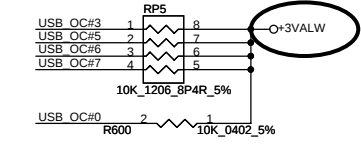
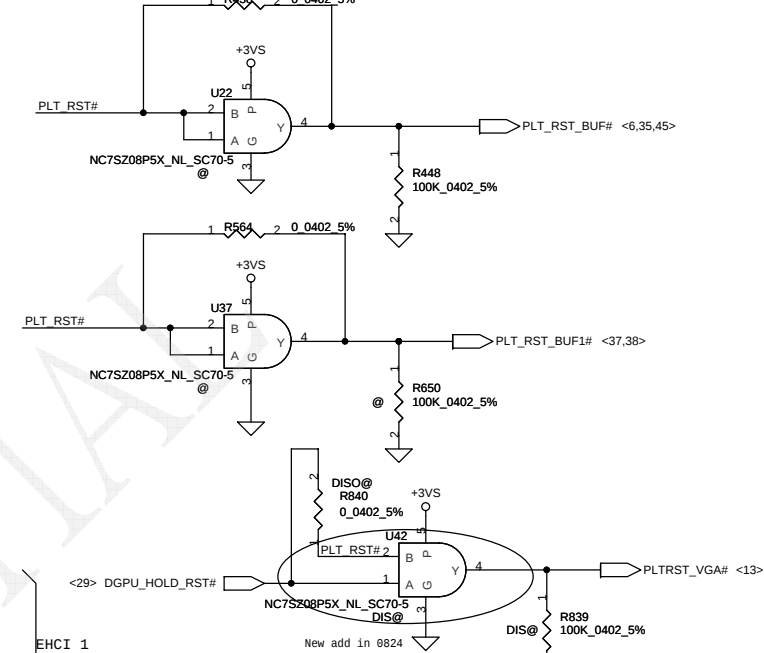
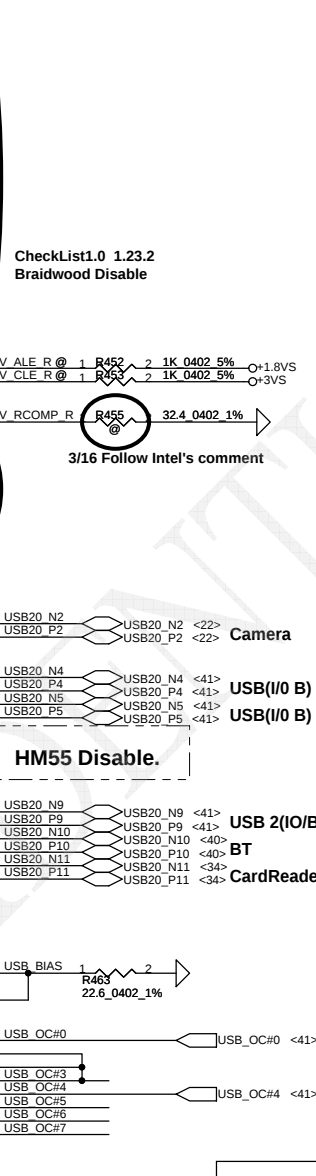
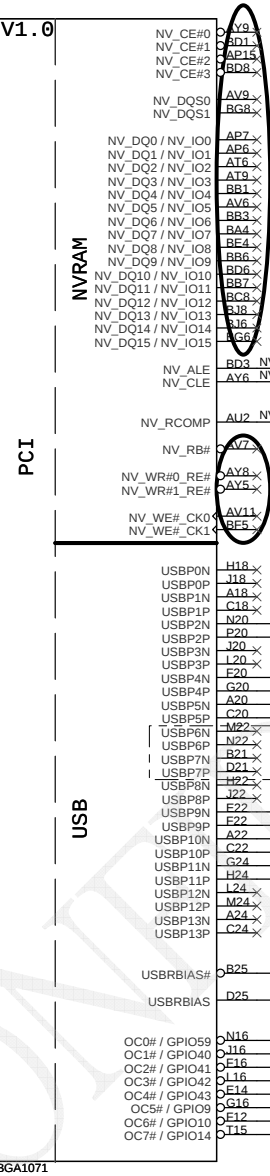
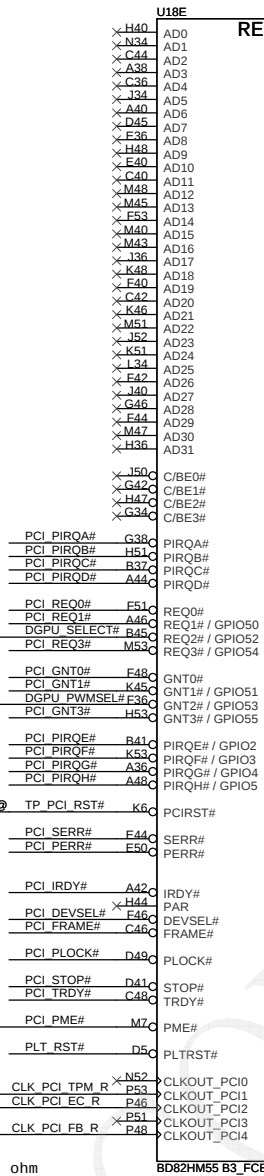
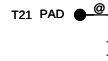
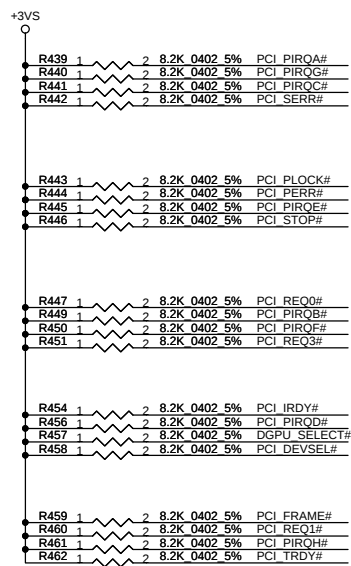
Buffer Mode check is need or not

3/20 Remove by Vivian

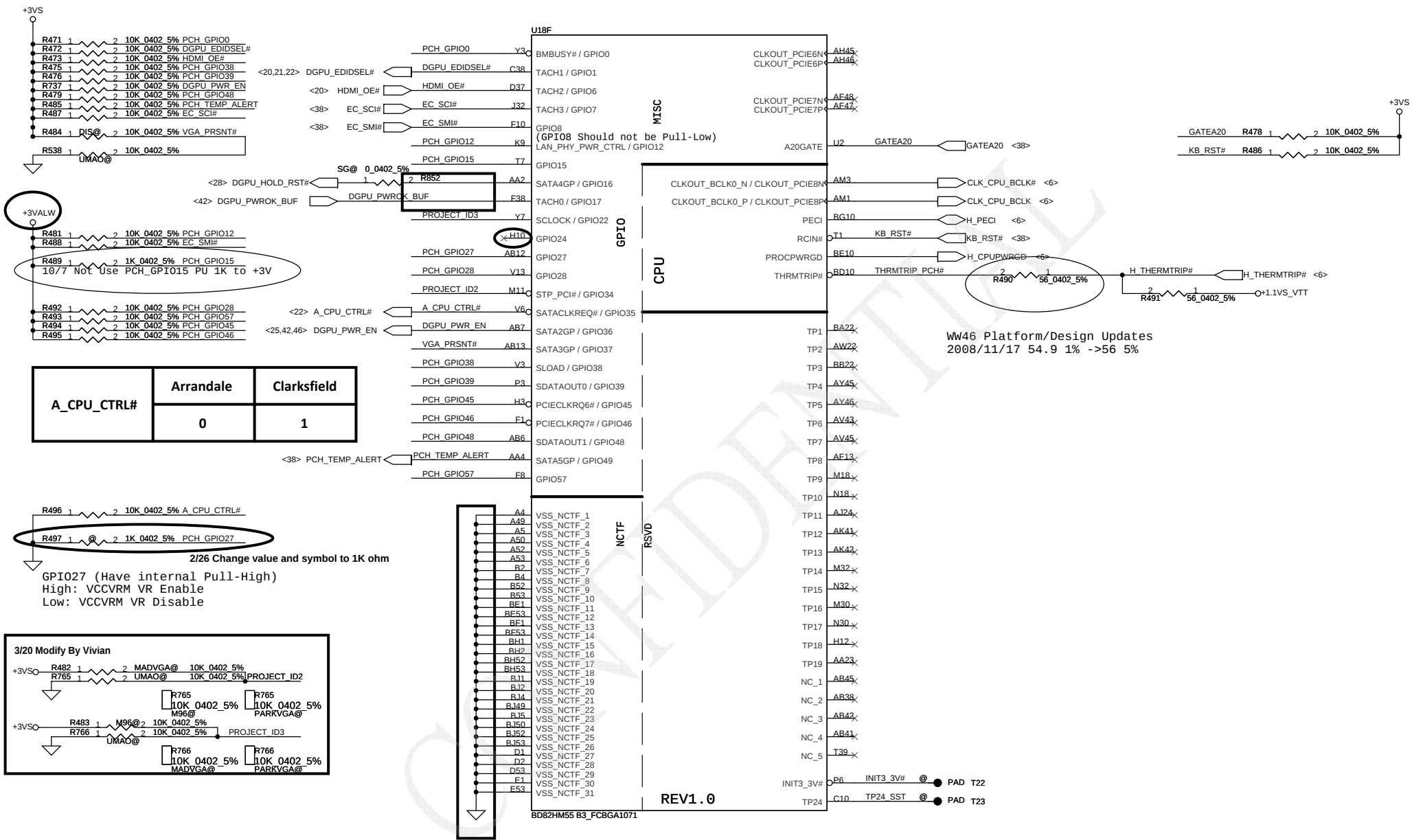
3/16 Change R408/R409 to 2.2K ohm(follow Intel's comment)

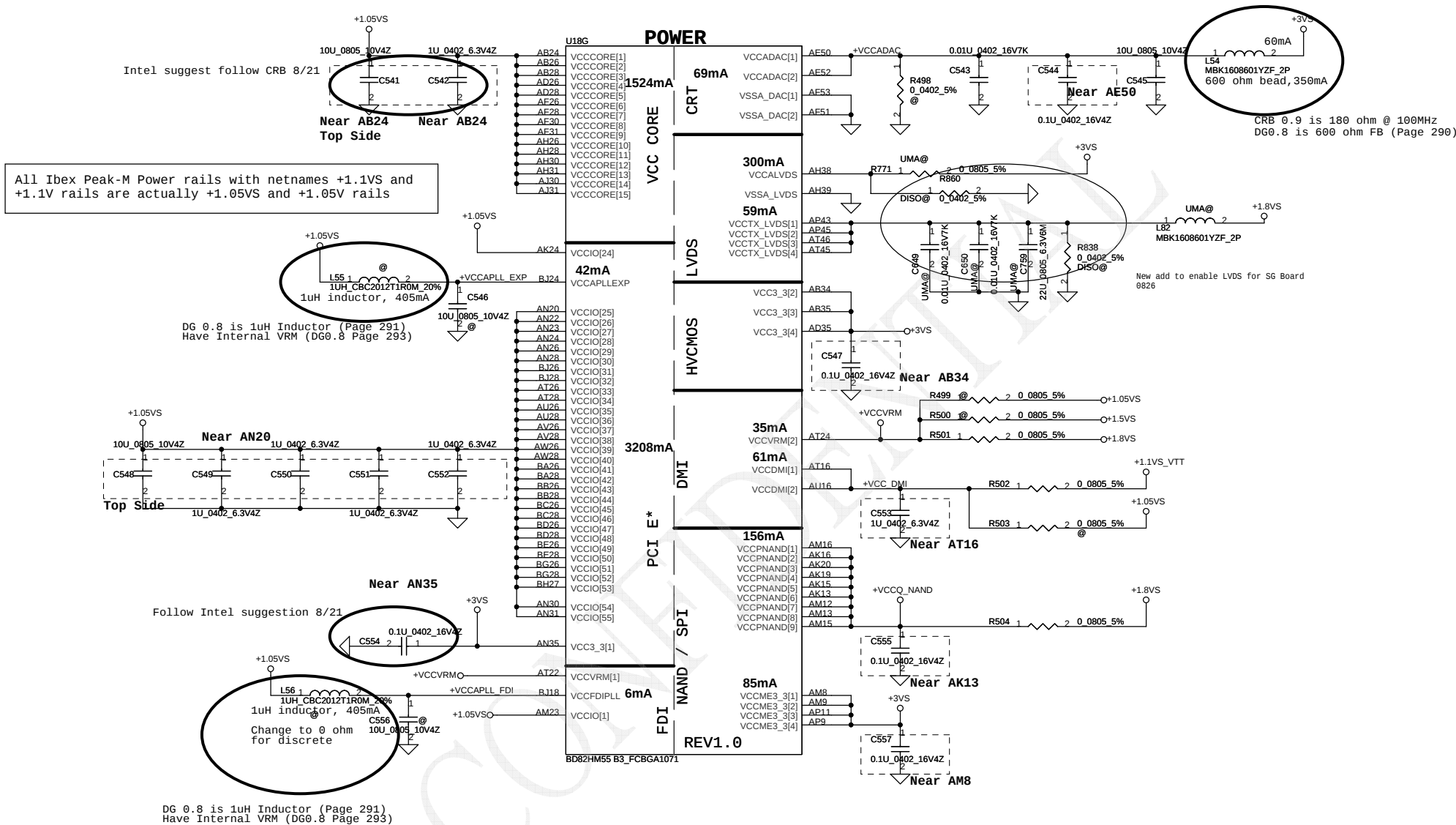
3/16 Add R761/R762 to 2.2K ohm(follow Intel's comment)



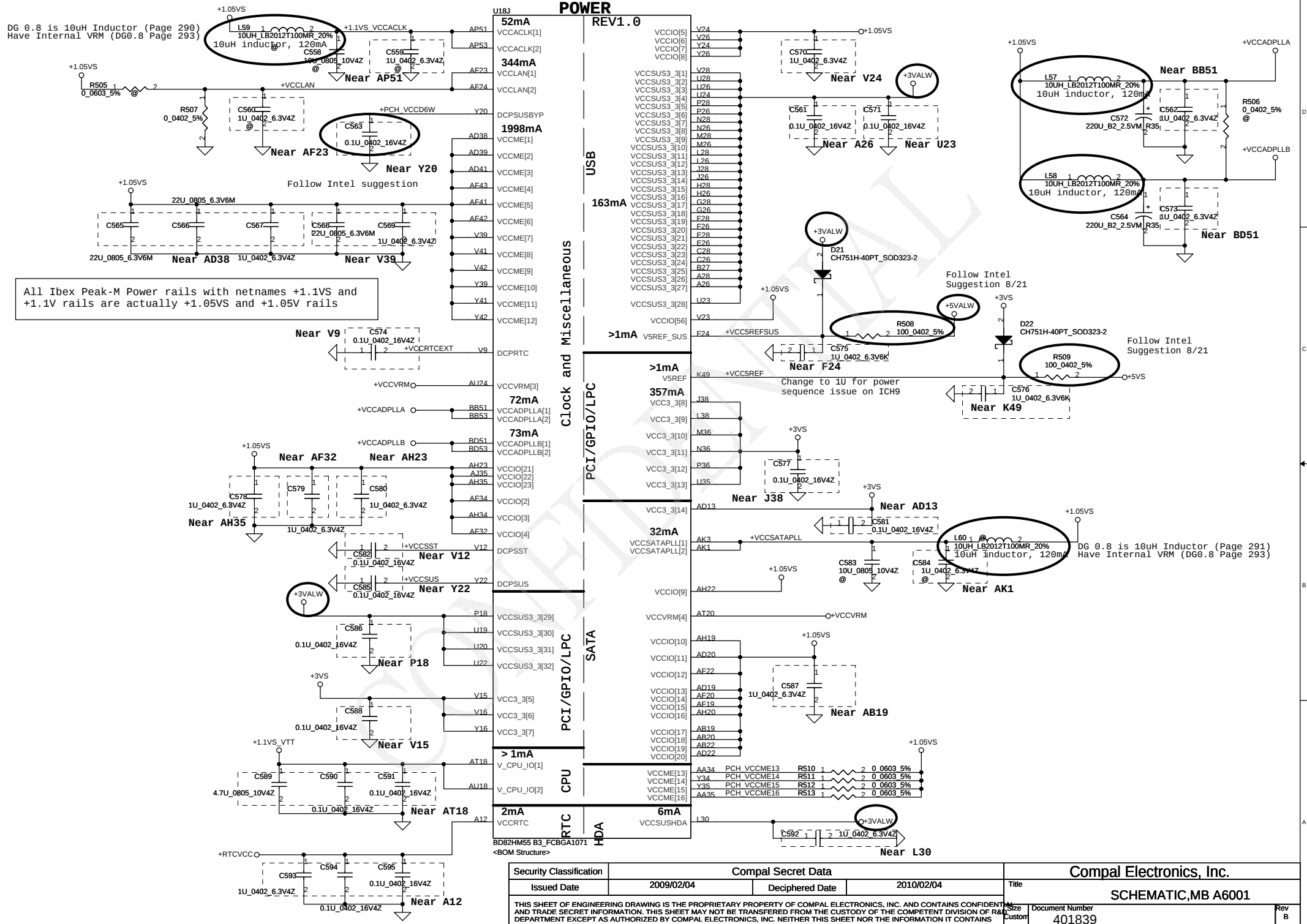


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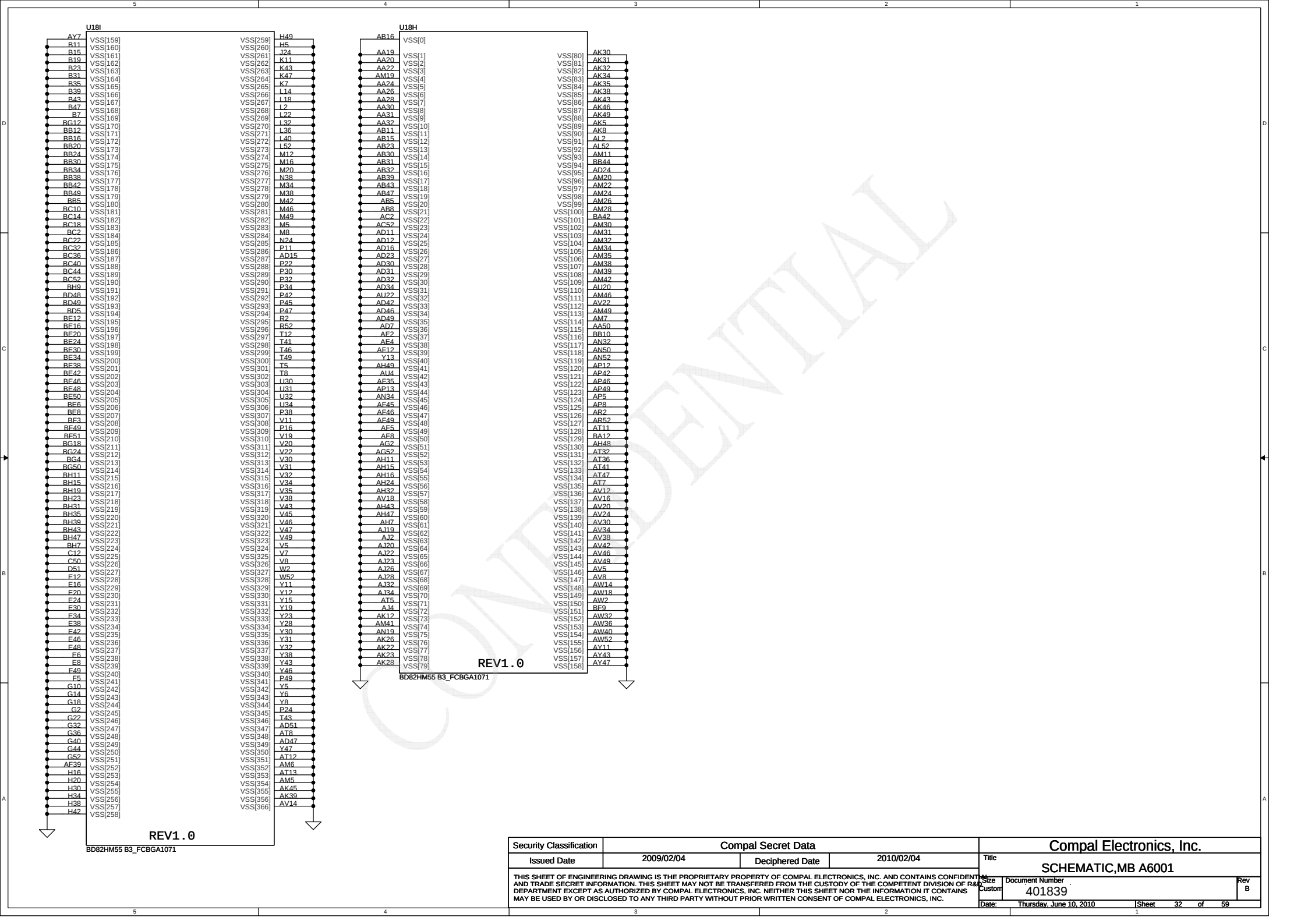




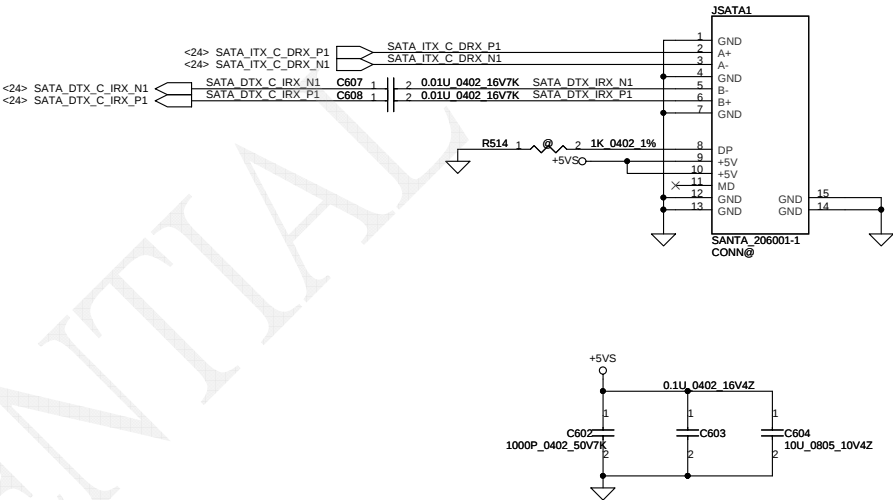
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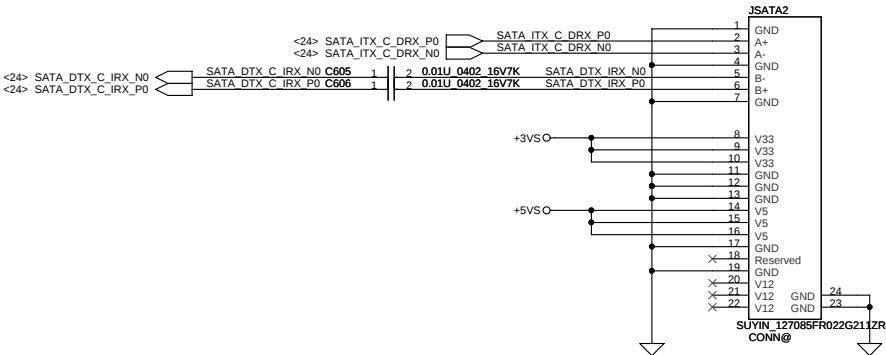
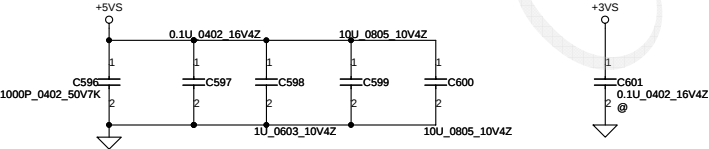
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				Date:	Thursday, June 10, 2010	Sheet 31 of 59



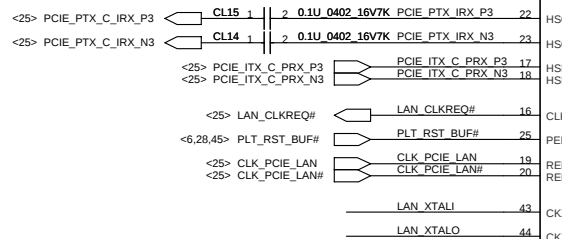
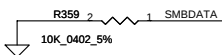
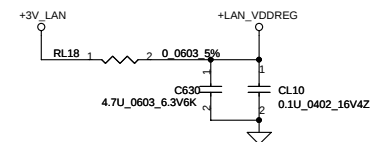
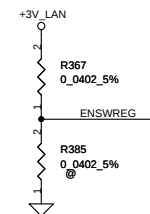
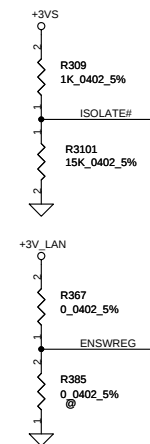
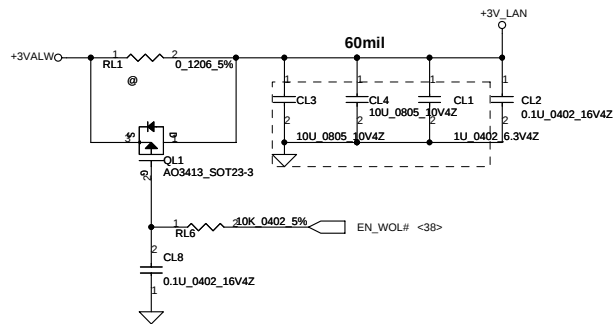
SATA ODD Conn.



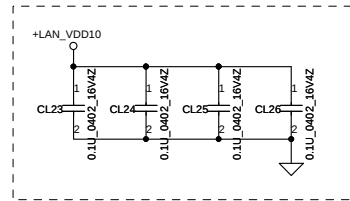
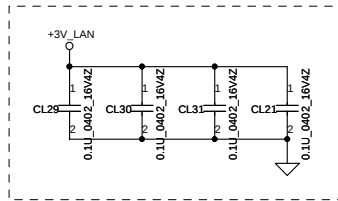
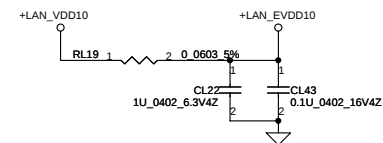
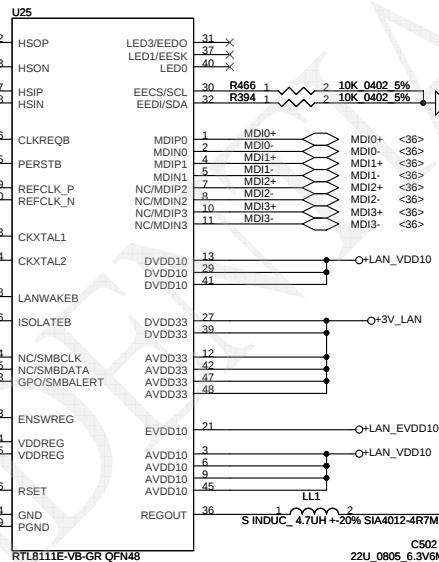
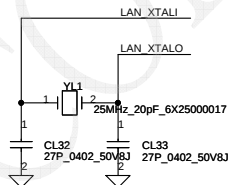
SATA HDD Conn.



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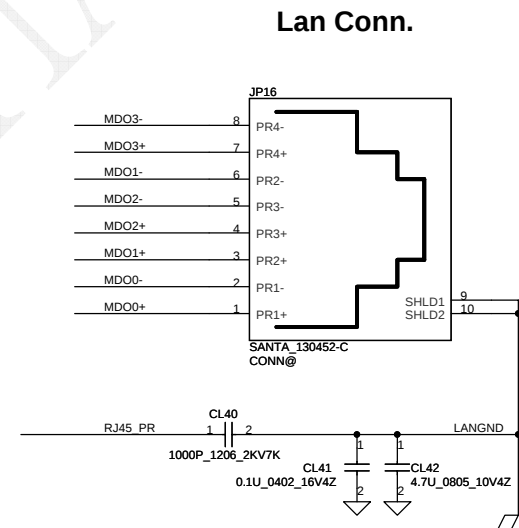
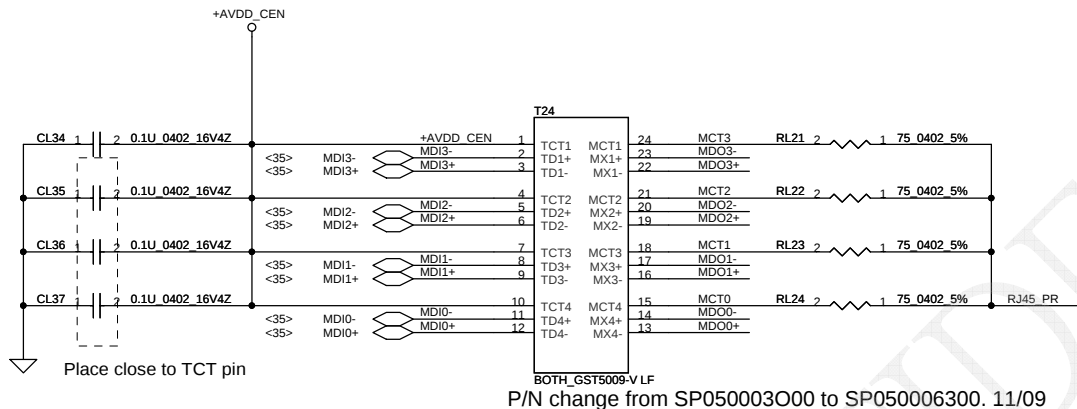


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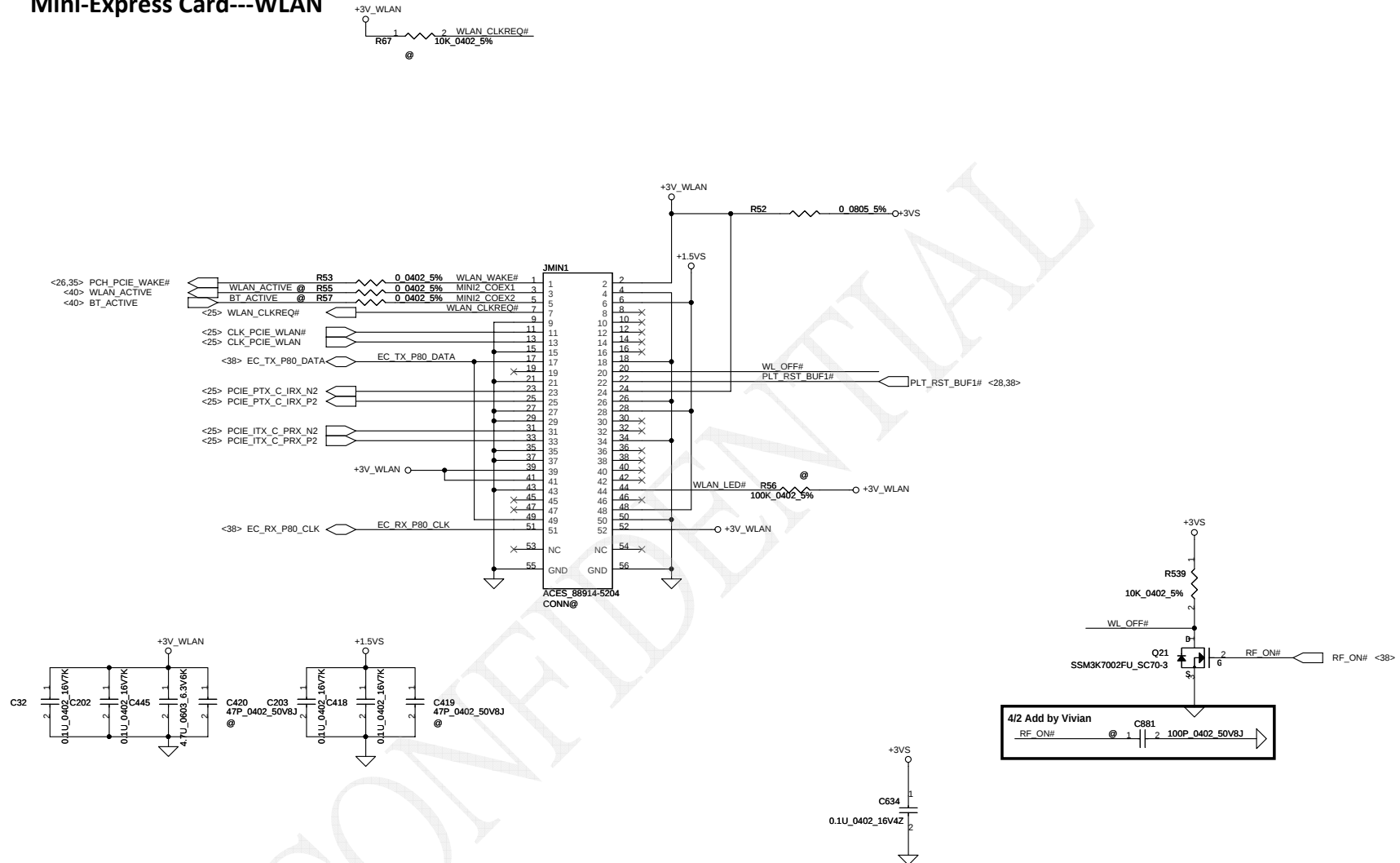
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Compal Electronics, Inc.
SCHEMATIC,MB A6001

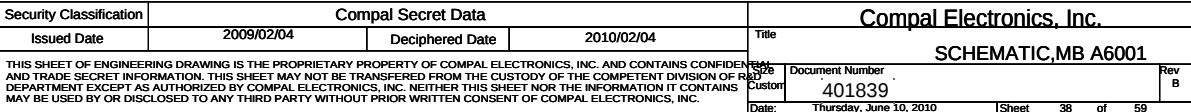


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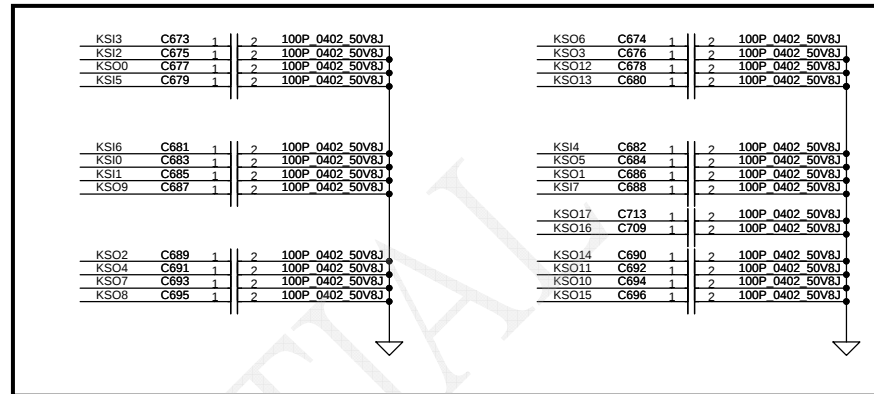
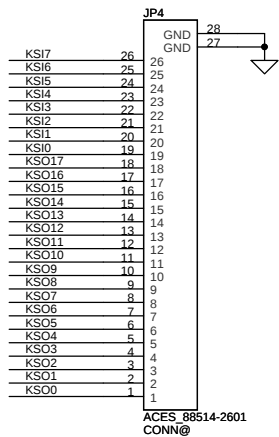
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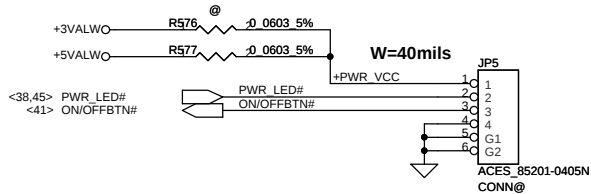
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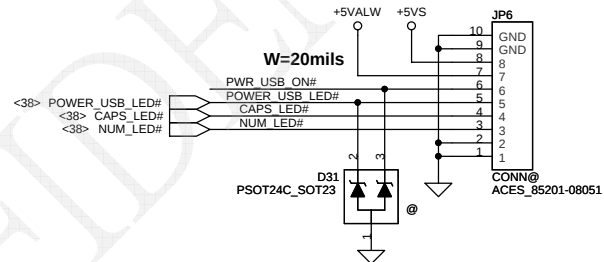
INT_KBD Conn.



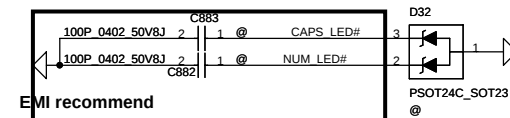
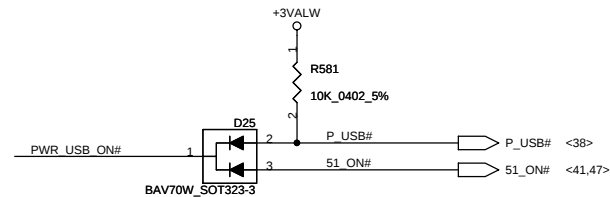
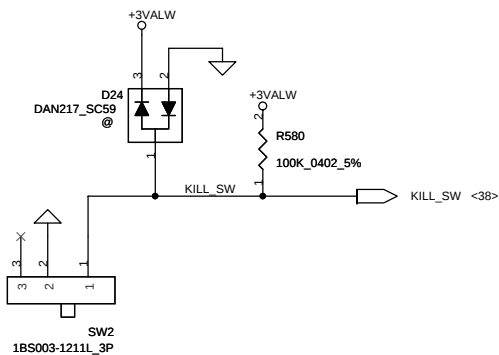
Power BTN Board Conn



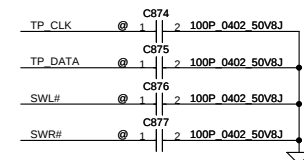
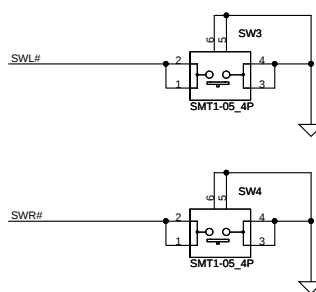
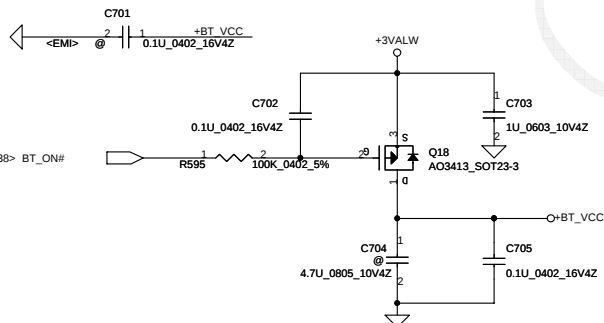
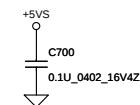
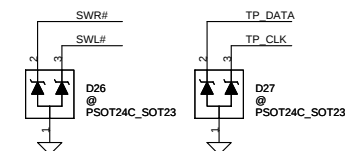
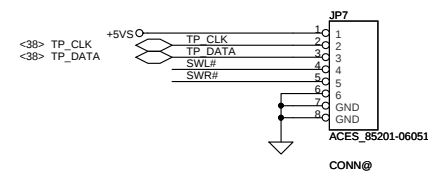
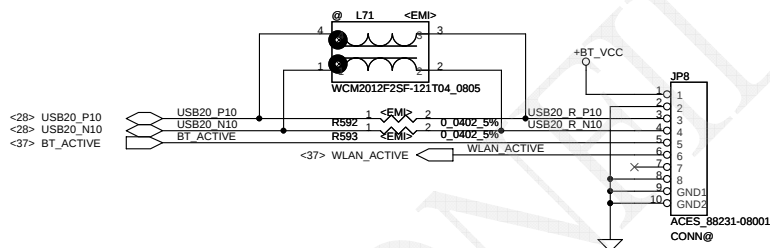
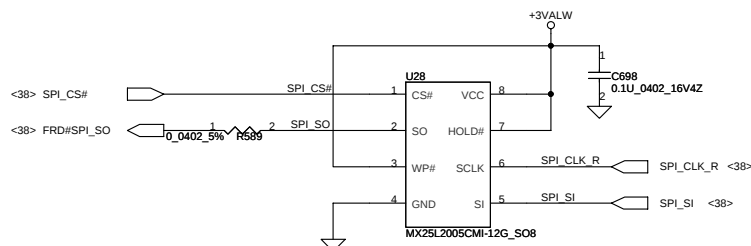
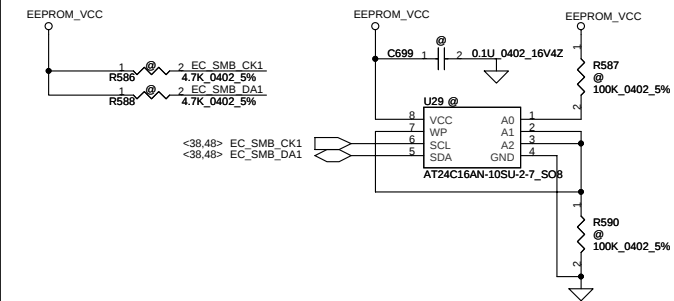
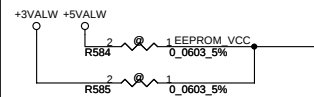
Function board conn



Kill SWITCH



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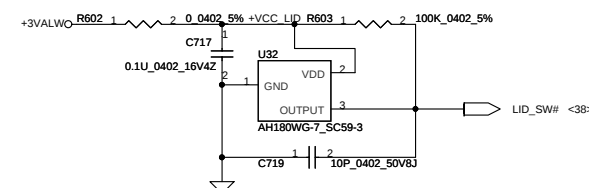
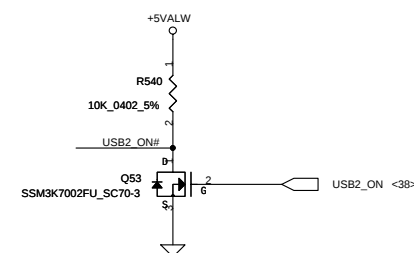
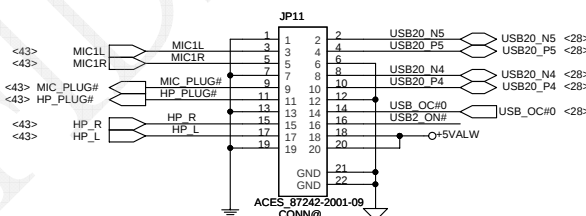
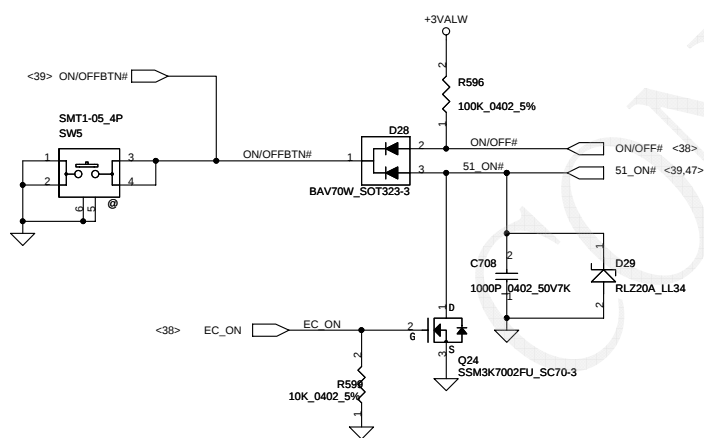
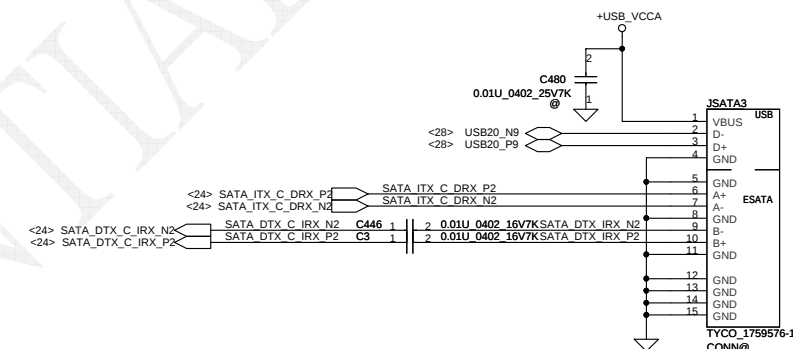
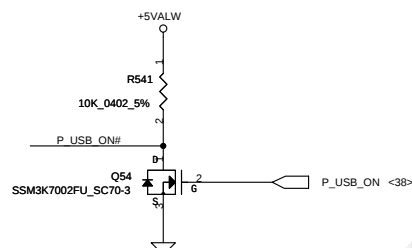
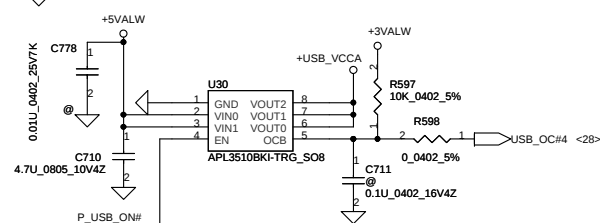
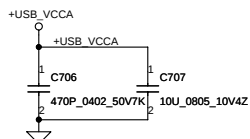


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APL3510 □□□-□□□
APL3511

Assembly Material
Handling Code
Temperature Range
Package Code
Output Current/EN Function

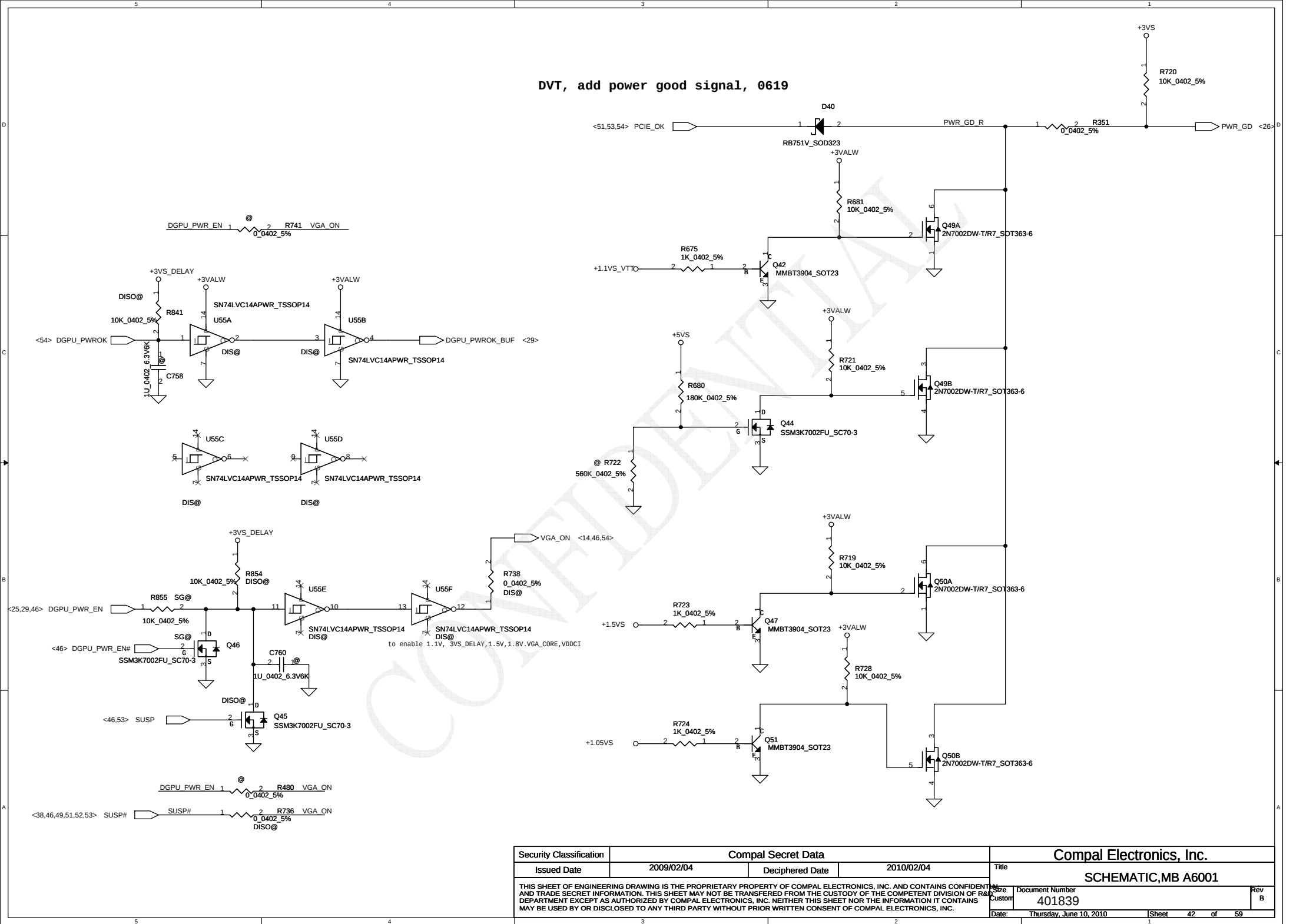
Package Code
K : SOP-8 X : MSOP-8 B : SOT-23-5
Operating Ambient Temperature Range
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Output Current/EN Function
A : 2A/Active High B : 2A/Active Low
C : 1A/Active High D : 1A/Active Low
Assembly Material
G : Halogen and Lead Free Device



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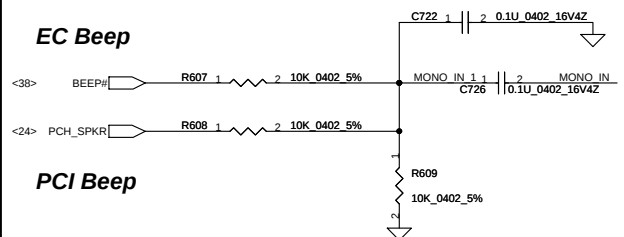
Compal Electronics, Inc.
SCHEMATIC, MB A6001

DVT, add power good signal, 0619

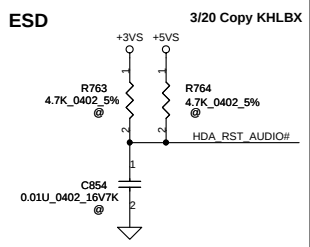
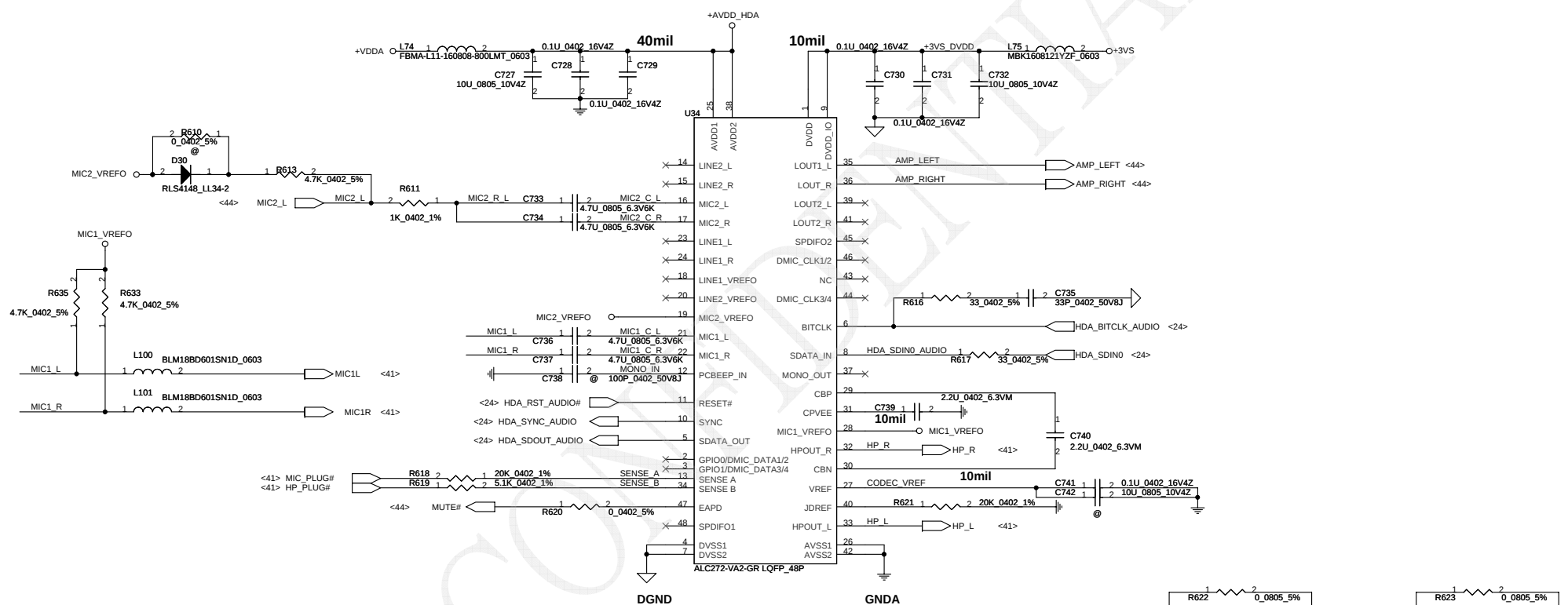


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EC Beep

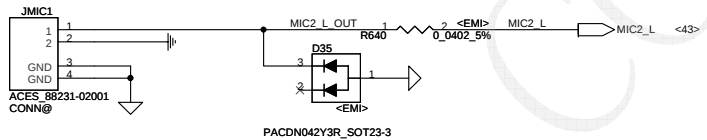
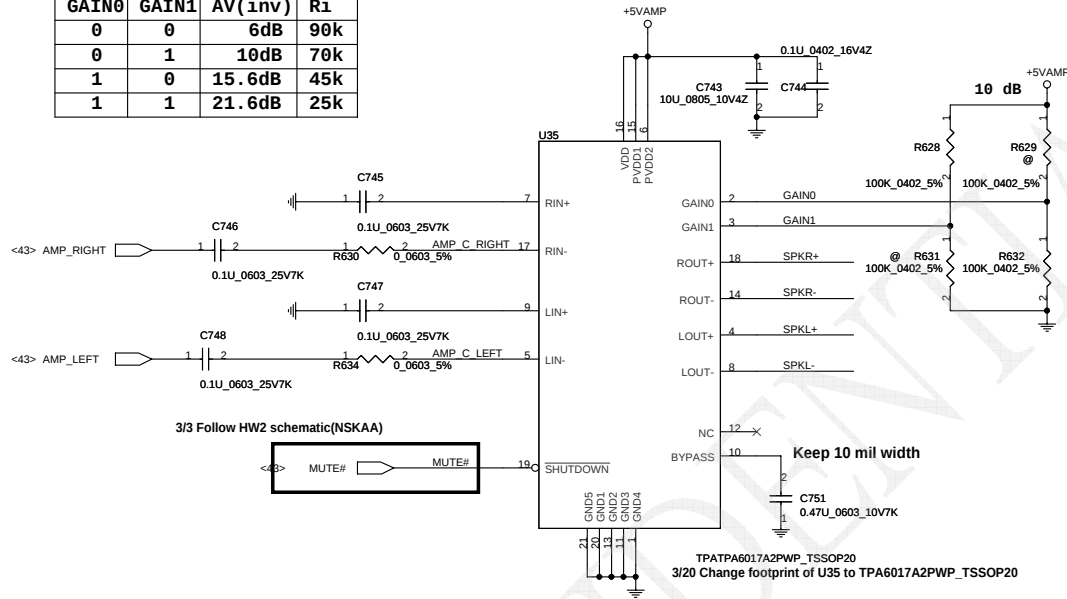


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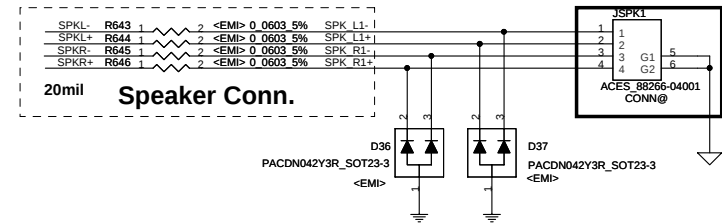


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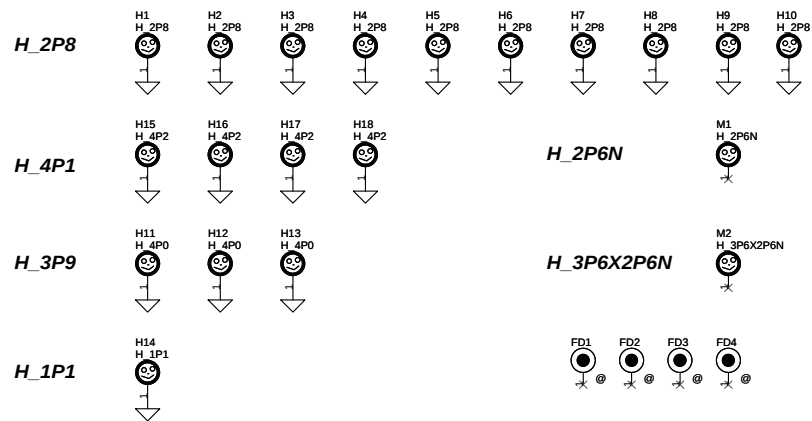
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0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k



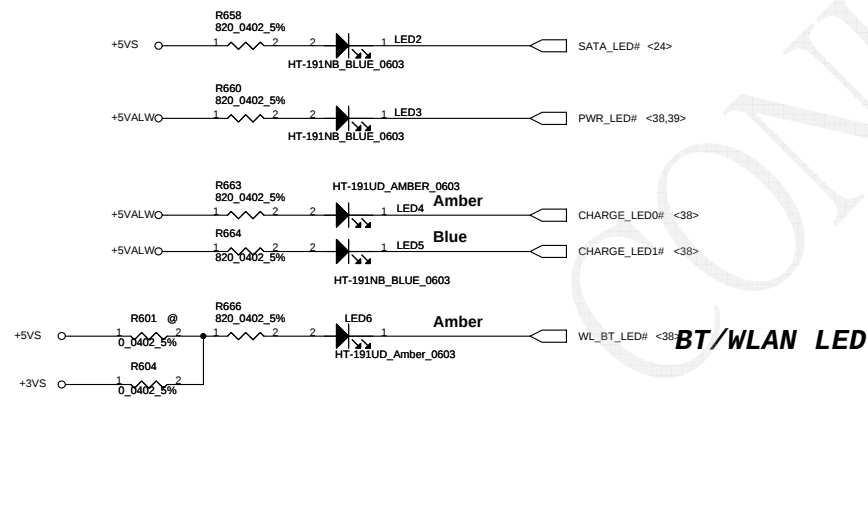
Int. Speaker Conn.



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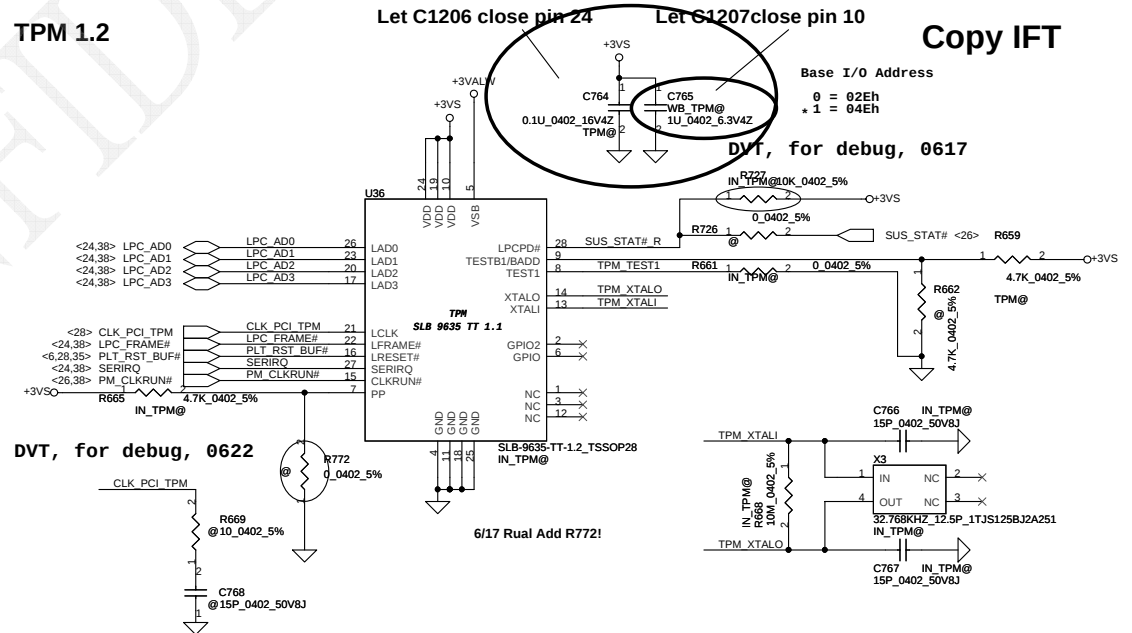


LED



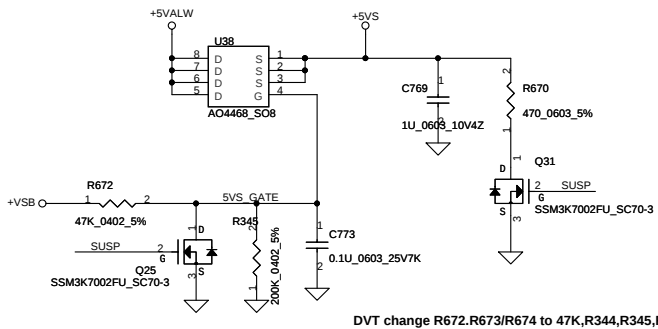
BT/WLAN LED

TPM 1.2



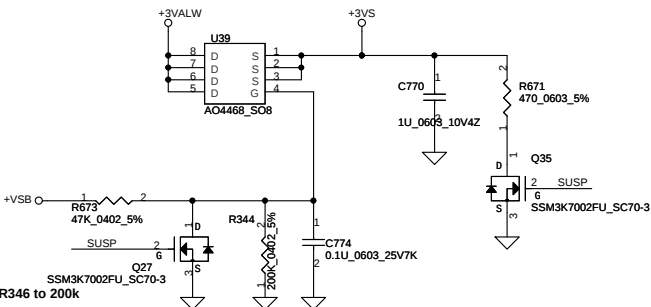
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+5VALW TO +5VS

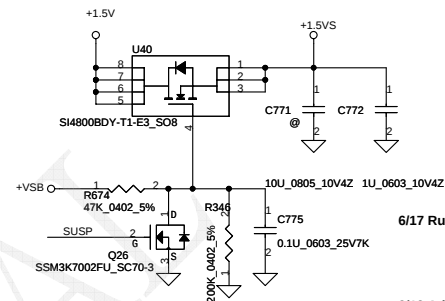


6/17 Rual Add R345!

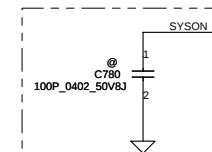
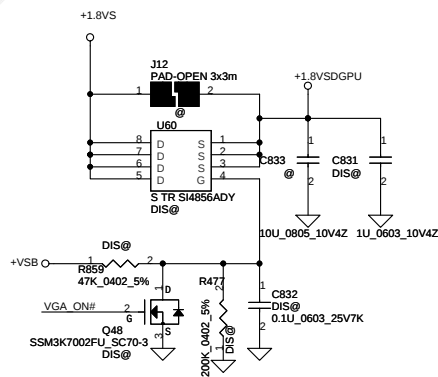
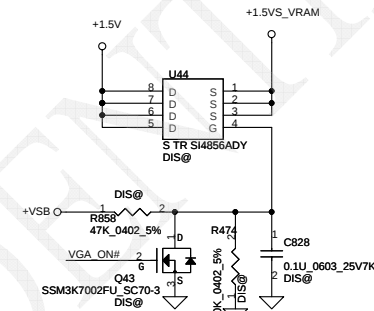
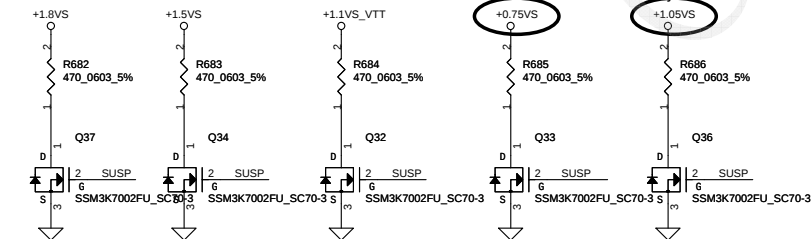
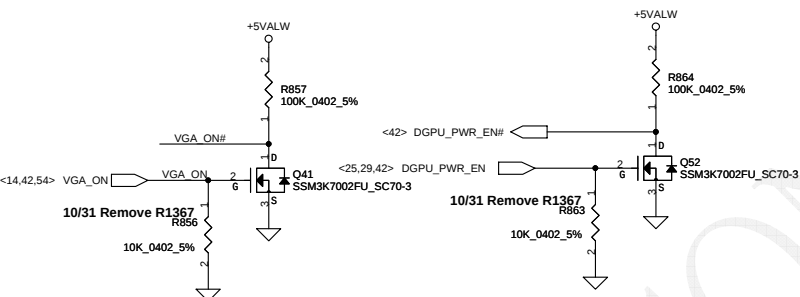
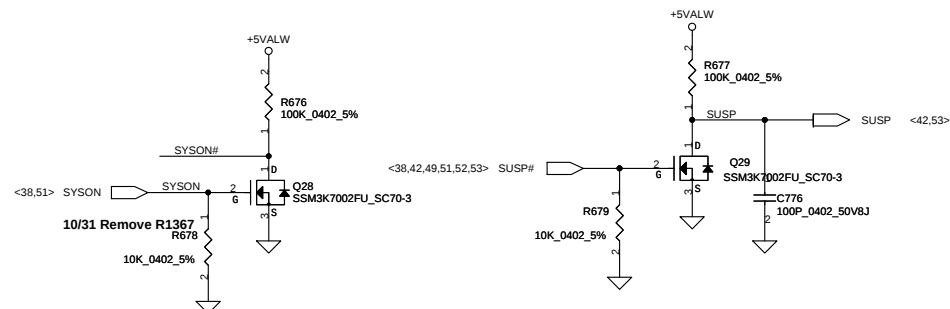
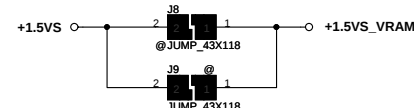
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+1.5V TO +1.5VS

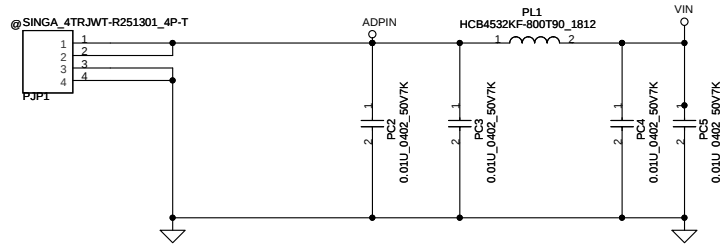


3/12 Add by Vivian



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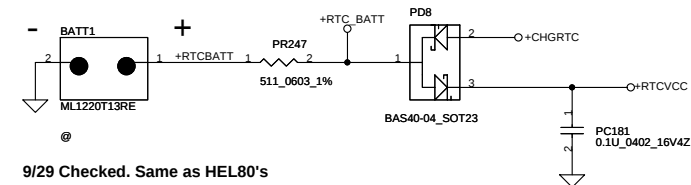
DC301008L00



RTC Battery

Change BATT1 P/N : SP093PA0200 (Panasonic)
SP093MX0000 (MAXELL)

9/29 modified to follow ISKAA



9/29 Checked. Same as HEL80's

Reserve another location

BOM structure comment

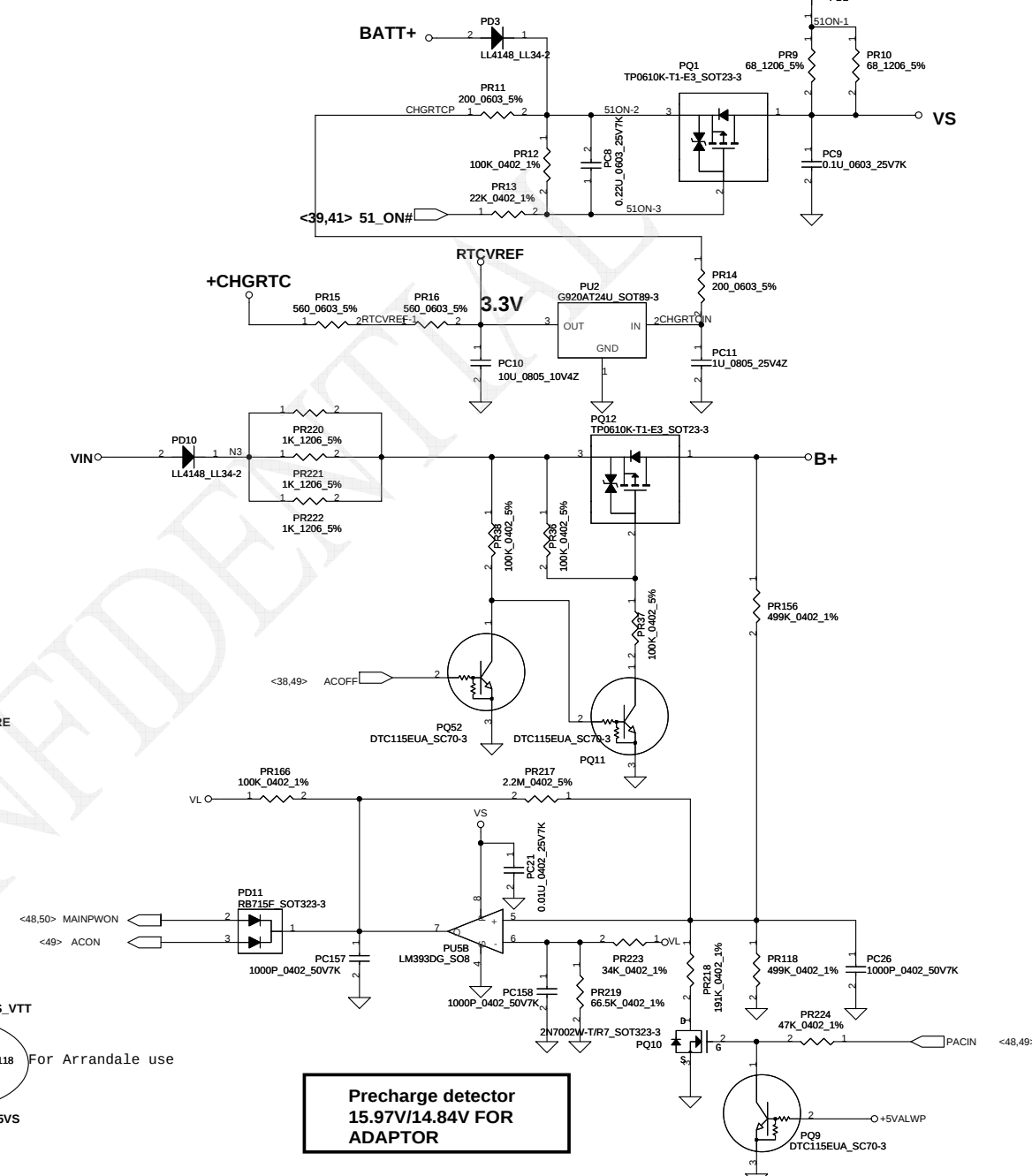
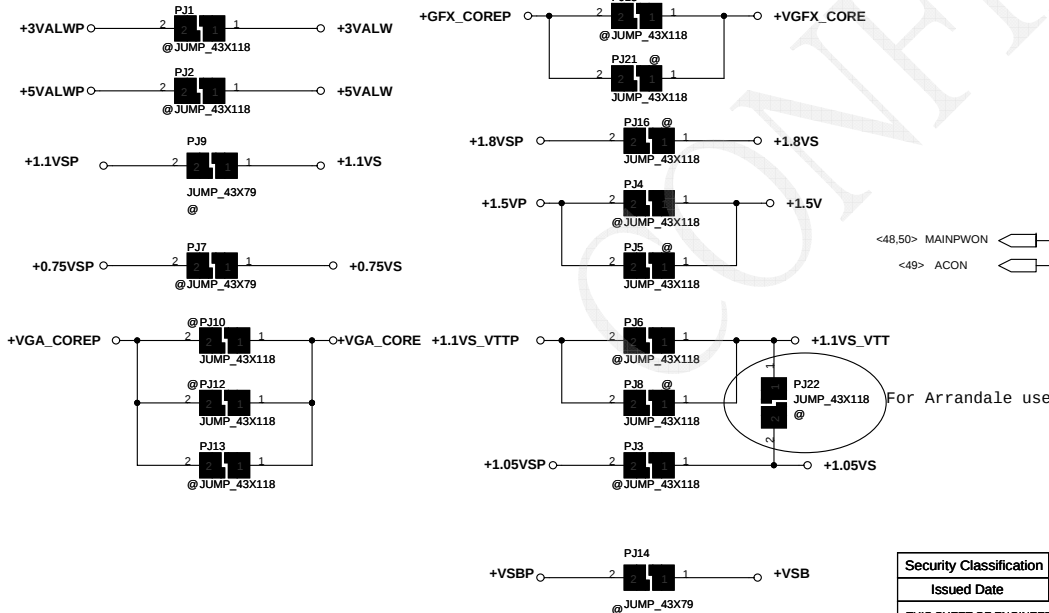
@ ==>unpop

UMA@==>UMA sku only

DIS@==>DIS sku only

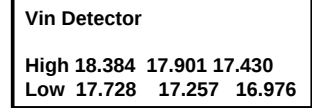
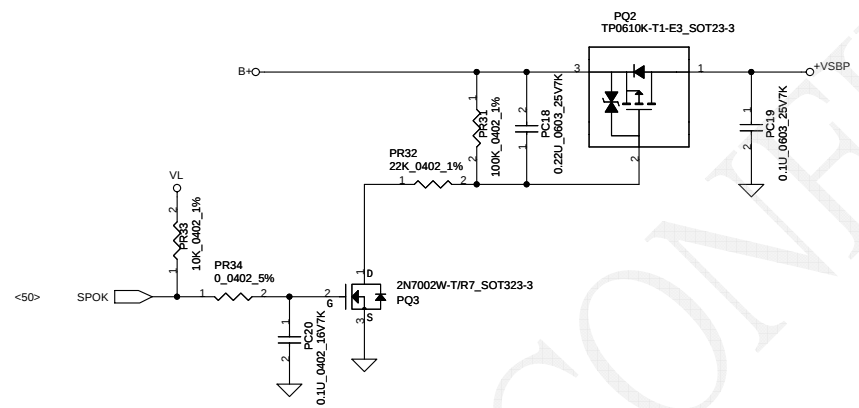
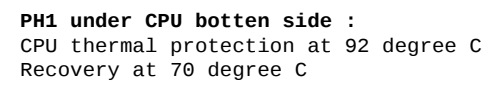
06/24 Rual remove BATT2!

SP093MX0000

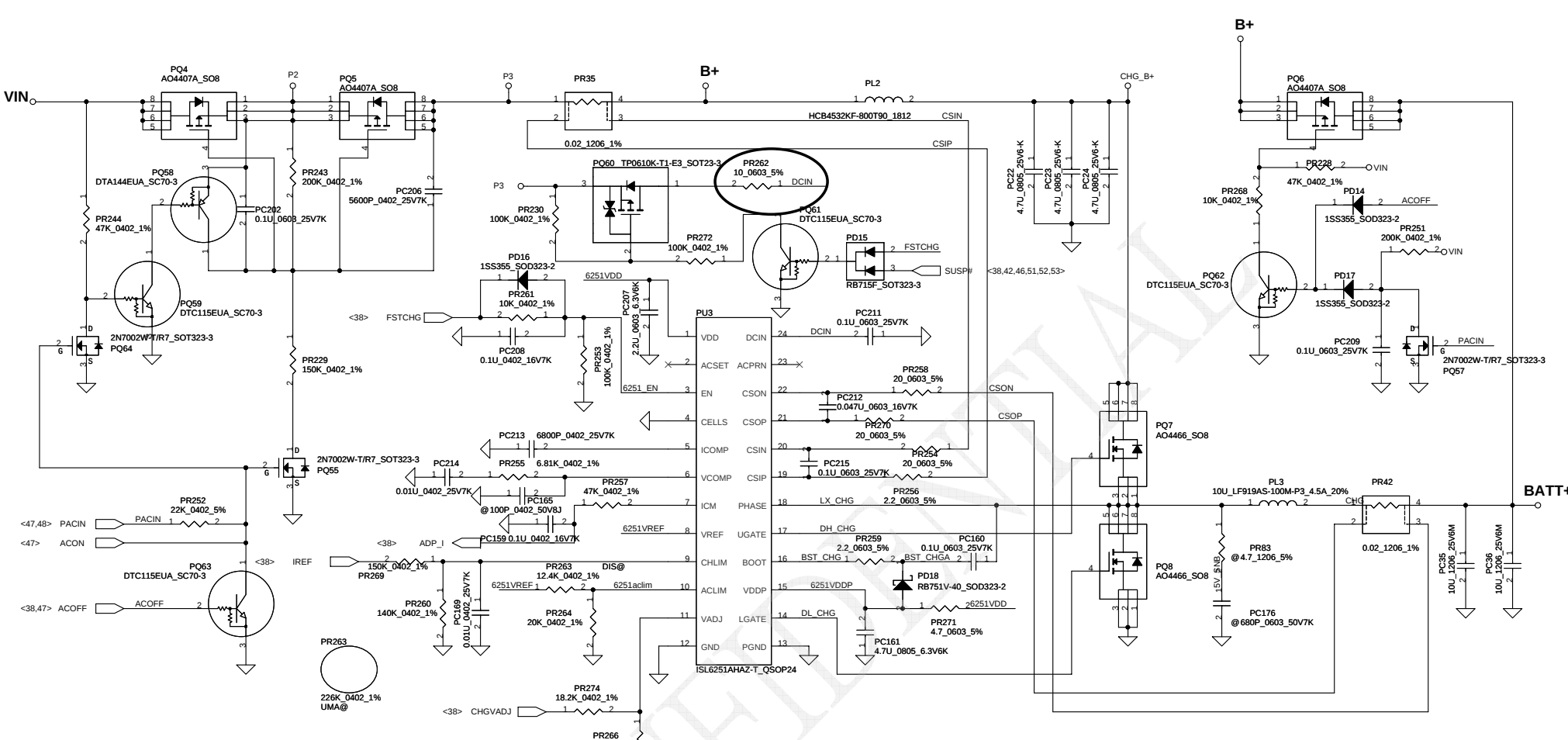


Precharge detector
15.97V/14.84V FOR
ADAPTOR

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"CHGVADJ" connect to EC DA pin

PR263
12.4K SD00000A380(DIS)
226K SD034226380(UMA)

Iada=0~4.74A(90W) CP= 85%*Iada; CP=4.02A

CP mode
Vac11m=2.39*(20K/(152K/(20K/(152K+12.4K/(152K)))=1.44966V
Iinput=(1/0.02)*((0.05*Vac1m)/2.39+0.05)
where Vac1m=1.44966V, Iinput=4.02A

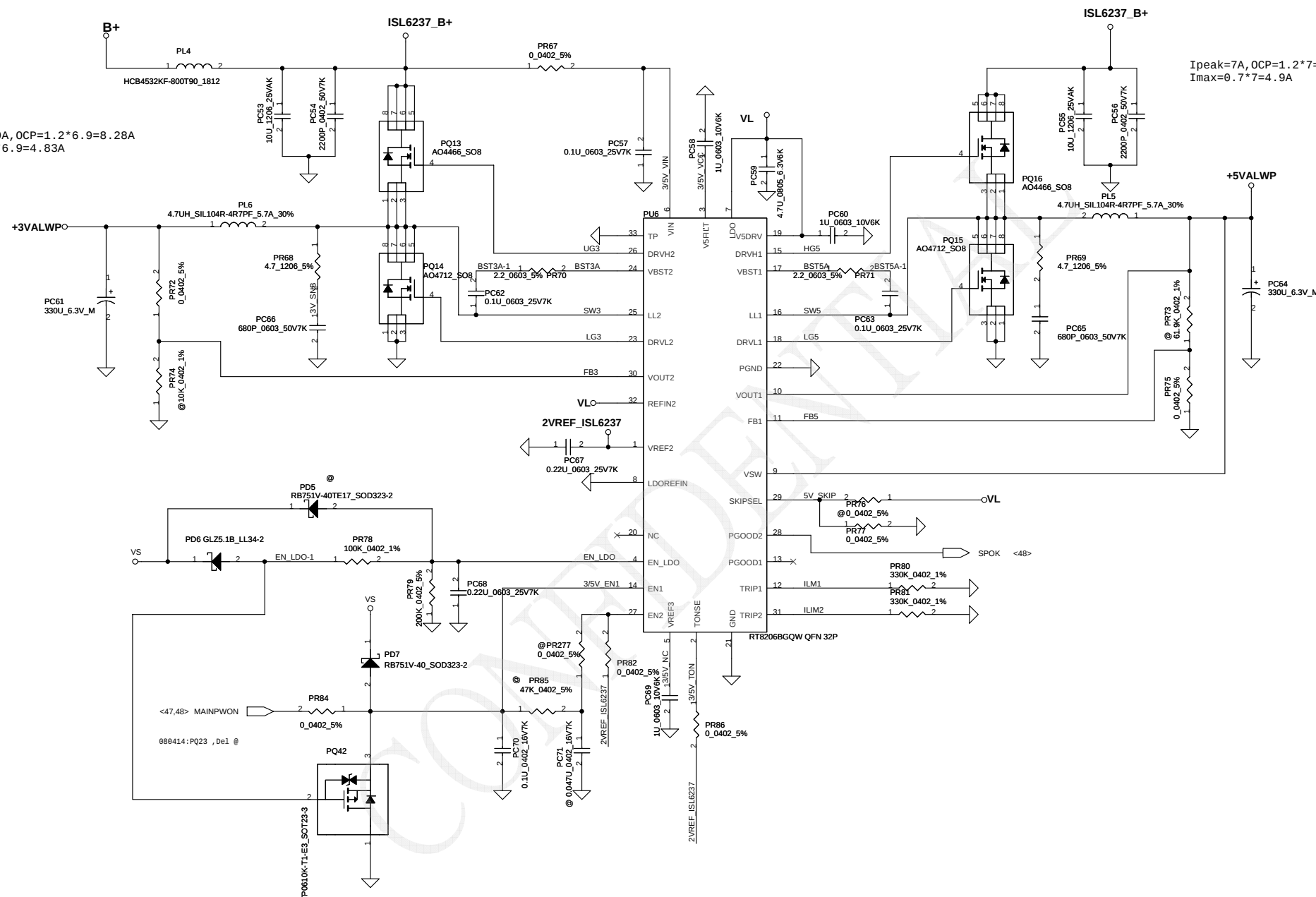
CC=0.5A~3.64A(0.7C)
IREF=2.42V (4.8AH)
2.62V (5.2AH)
IREF=0.4V~2.62V

CHGVADJ=	
Vcell	CHGVADJ
4V	0V
4.2V	1.854V
4.35V	3.12V

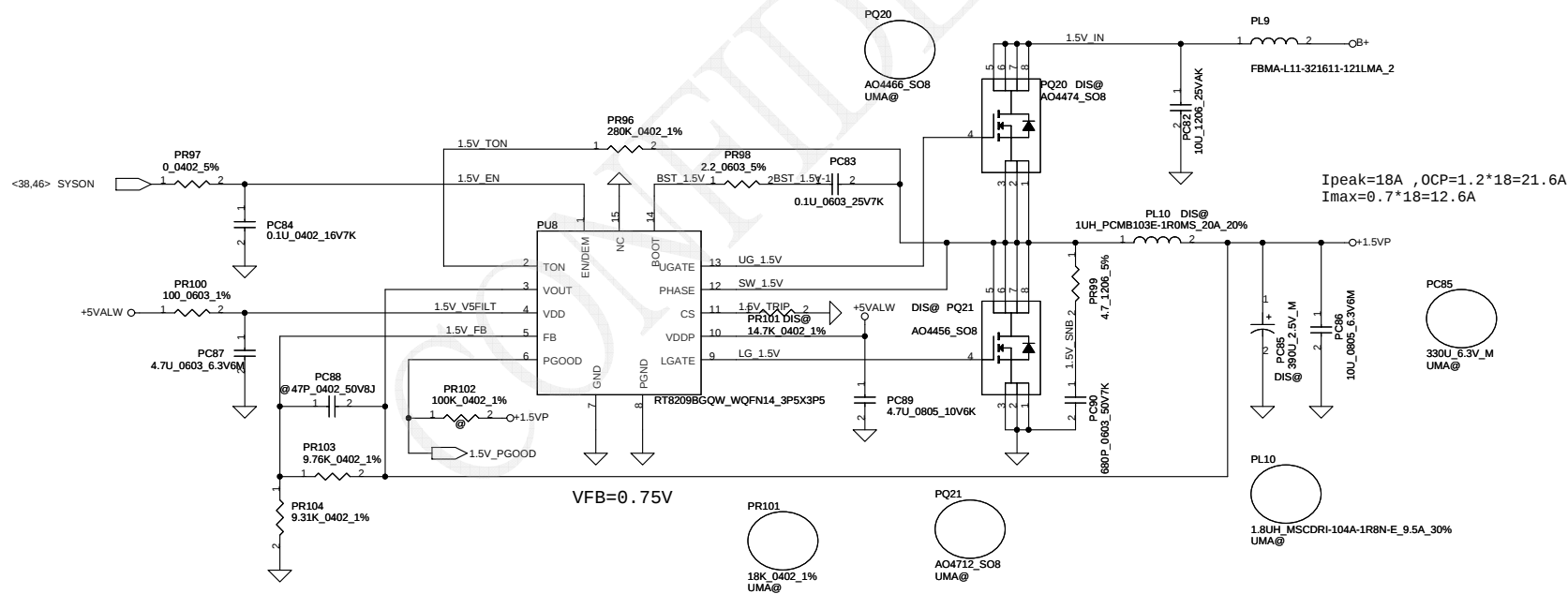
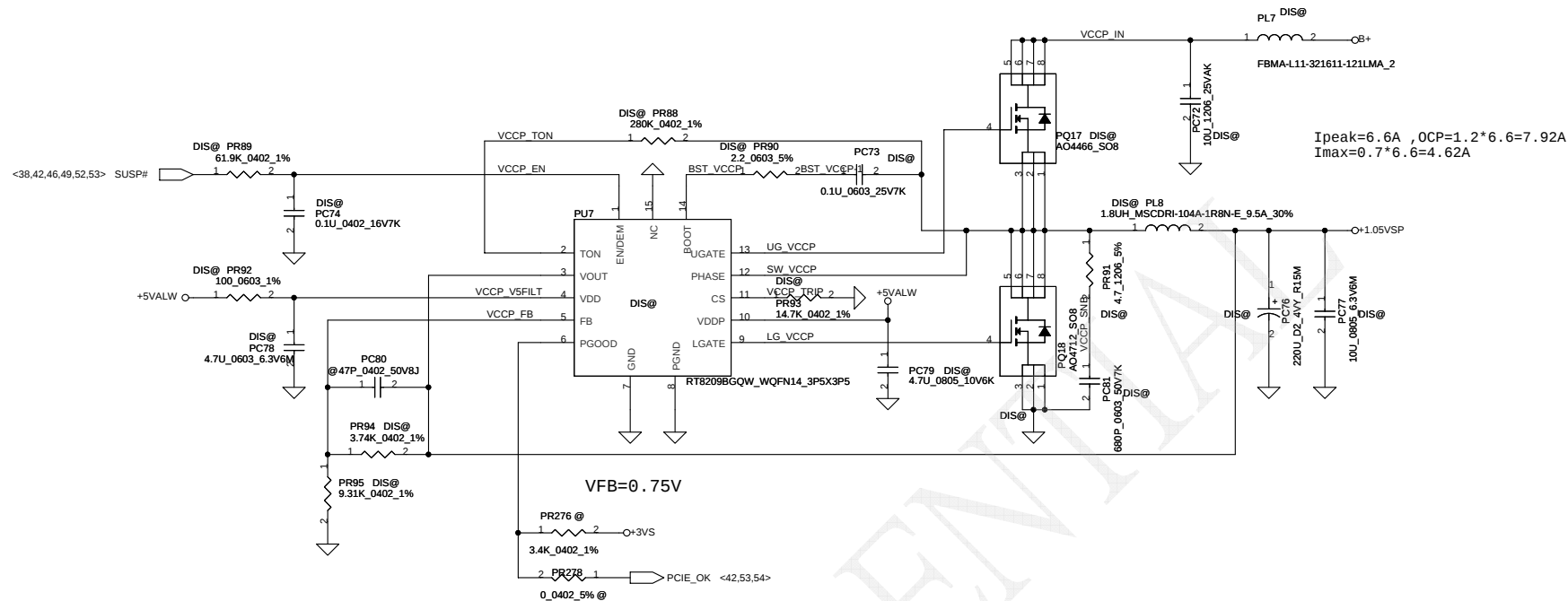
CELLS	VDD	GND	Float
CELL number	4	3	2

Ipeak=6.9A, OCP=1.2*6.9=8.28A
Imax=0.7*6.9=4.83A

Ipeak=7A, OCP=1.2*7=8.4A
Imax=0.7*7=4.9A



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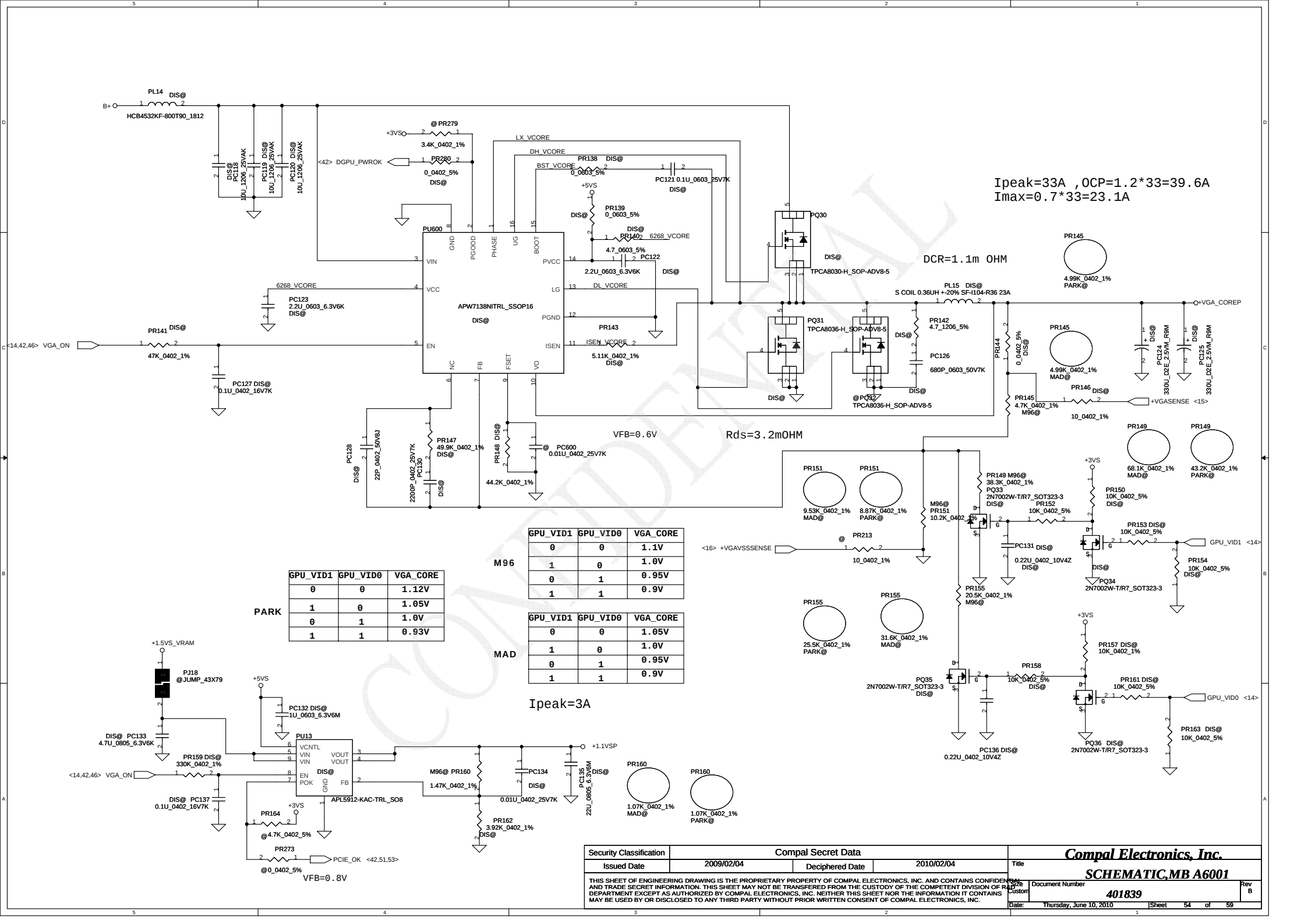


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1



Ipeak=33A ,OCP=1.2*33=39.6A
Imax=0.7*33=23.1A

DCR=1.1m OHM

VFB=0.6V

Rds=3.2mOHM

GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.12V
1	0	1.05V
0	1	1.0V
1	1	0.93V

PARK

GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.1V
1	0	1.0V
0	1	0.95V
1	1	0.9V

M96

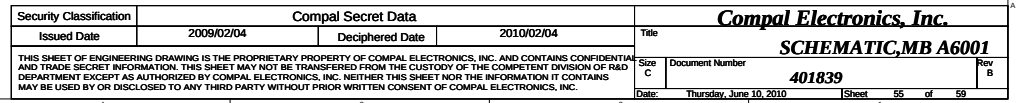
GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.05V
1	0	1.0V
0	1	0.95V
1	1	0.9V

MAD

Ipeak=3A

VFB=0.8V

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dy
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	can't use PWM to control brightness.	use PCH to control brightness in all SKU.	0.2	22	remove U47, R861,C825; U48; add R844, R827	01/30	DVT
2	Cost down	Cost down	0.2	23	Change Y6 from SJ100002600 to SJ114P3M730	01/30	DVT
3	Cost down	Cost down	0.2	20,21	change D7 and D15 to SCS00003H00	01/30	DVT
4	Cost down	Cost down	0.2	22	delete D18 , change R311 from 4.7K to 10K and pull down to GND.	01/30	DVT
5	Cost down	Cost down	0.2	22,40	change Q16&Q18 from SB923010020 to SB934130000 (A03413)	01/30	DVT
6	Cost down	Cost down	0.2		delete C433, C404;C852; C851;C401;C399; C364	01/30	DVT
7	Cost down	Cost down	0.2	9,30	Change R242;R501;R502;R504 from SD00000S000 to SD002000080 (0805 0ohm)		
8	Cost down	Cost down	0.2		delete C339;C336;C334		
9	Cost down	Cost down	0.2	38	delete crystal for EC		DVT
10	Cost down	Cost down	0.2	35	change YL1 from SJ100003300 to SJ125P0M200		DVT
11	Cost down	Cost down	0.2	35	change QL1 from SB000005X80 to SB934130000 (A03413)		DVT
12	Cost down	Cost down	0.2	41	change U30 from SA005280110 to SA000039E00		DVT
13	Cost down	Cost down	0.2	39,41	change D25&D28 from SC2N202U010 to SC600000B00		DVT
14	EMI Reserved.	EMI Reserved.	0.2	20	Add R865 and R866 on HDMI DDC signals for EMI		DVT
15	EMI&ESD Reserved.	EMI&ESD Reserved.	0.2	39	add D31, D32 and c838.		DVT
16		株y! n%?0 = ""	0.2	22		2/8	DVT
17		? ? n% ? h %-01/30					DVT
18		P? 統y! n%?0 =					
19		"" 0 !					
20							
21							
22							
23							

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Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	ADD PQ64 in BOM	BOM STRUCTURE ERROR	0.1	51	Delete error bom structure	11/12	EVT
2	Battery OTP set	Battery OTP set	0.1	50	Change pr27 from 10k to 33.2k (sd034332280)	11/12	EVT
3	For material EOL issue	For material EOL issue	0.1	51	change pq4,pq5,pq6 from ao4407 to ao4407a (sb00000d100)	11/12	EVT
4	PH801 part number change	PH801 part number change	0.1	58	change ph801 from sl200000581 to sl200000500	11/18	EVT
5	output voltage unstable	output voltage unstable	0.1	55	change pc129,pc147 from 4.7u to 22u(se000000i10)	11/18	EVT
6	for material shortage issue	for material shortage issue	0.1	51	change pc22,pc23,pc24 from se142475k80 to se000006r80	11/19	EVT
7	For +3valw&5valw enable singal rising time delay	For +3valw&5valw enable singal rising time delay	0.1	52	change pr23 from 100k to 806k(sd014806380)	11/25	EVT
8	cost down	cost down	0.1	52	del pr830(sd034300080)	11/25	EVT
9	Not need	cost down	0.1	50	del pr22(sd034100180)	12/08	DVT
10	cost down	cost down	0.1	53	change pl11 from 2.2u to 1.8u(sh000008u80)	12/18	DVT
11	cost down	cost down	0.1	49	del pr225,pr226,pr265,pc175	12/24	DVT
12	cost down	cost down	0.1	56	change pq801 from si4686 to tpca8030 (sb00000h100)	12/26	DVT
13	cost down	cost down	0.1	49	change pr35 from 1206 size to 2512 size (sd000001f00)	12/26	DVT
14	pl3 temperature is too hot when charge	pl3 temperature is too hot when charge	0.1	49	change pl3 from sh00000e300 to sh162100m10	12/26	DVT
15	cost down	cost down	0.1	51	change pq20 from ao4474 to ao4466 (sb00000cg00) UMA	12/26	DVT
16	cost down	cost down	0.1	51	change pq21 from ao4456 to ao4712 (sb00000aj00)UMA	12/26	DVT
17	cost down	cost down	0.1	51	change pl10 from 1.0u to 1.8u (sh000008u80)UMA	12/26	DVT
18	cost down	cost down	0.1	51	change pc85 from 390u to 330u (sf000001g00)UMA	12/26	DVT
19	cost down	cost down	0.1	48, 49	change pq3 ,pq10,pq55,pq57,pq64 to sb000006800	01/21	DVT
20	for material shortage issue	for material shortage issue	0.1	56	change pq31 ,pq26,pq44,pq38,pq802 to sb00000hr00	01/21	DVT
21	for material shortage issue	for material shortage issue	0.1	47	change pd2 ,pd3,pd10 to sc100001y80	01/21	DVT
22	for material shortage issue	for material shortage issue	0.1	49	change pd7 ,pd18,pd20 to scs00000z00	01/21	DVT
23	for material shortage issue	for material shortage issue	0.1	48	change pd1 to sc400001200	01/21	DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	for material shortage issue	for material shortage issue	0.1	50	change pd6 to sc400001300	01/21	DVT
2	for material shortage issue	for material shortage issue	0.1	49	change pd11,PD15 to scsh715f080	01/21	DVT
3	for material shortage issue	for material shortage issue	0.1	51	change pl17,pl19,pl15,pl802 to sh000005680	01/21	DVT
4	cost down	cost down	0.1	56	change pl16 to sm010020720	01/21	DVT
5	Change 1.1vsp power level from 1.0v to 1.1v	vga chip change from madison to M96	0.1	54	change pr160 from 1.07k to 1.47k(sd000009480)	1/29	DVT
6	ME interface	ME interface	0.1	49	change pr35 from 2512 size to 1206 size	1/29	DVT
7	OCP SETTING	OCP SETTING	0.1	52	change pr125 from 3.74k to 5.11k in UMA sku, change pr125 from 3.74k to 4.02k in DIS sku	2/2	DVT
8	OCP SETTING	OCP SETTING	0.1	51	change pr101 from 12.7k to 18k in UMA sku, change pr125 from 12.7k to 14.7k in DIS sku	2/2	DVT
9	TPCA8036(PQ38,PQ44) have OTP risk in Clarksfield SKU	TPCA8036(PQ38,PQ44) have OTP risk in Clarksfield SKU	0.1	55	change pq38,pq44from TPCA8036 to TPCA8028 in DIS sku	2/4	DVT
10	For madison voltage level change	For madison voltage level change	0.1	54	change pr151 from 10.2k to 9.53k(sd034953180)	2/5	DVT
11	For madison voltage level change	For madison voltage level change	0.1	54	change pr155 from 20.5k to 31.6k(sd034316280)	2/5	DVT
12	For madison voltage level change	For madison voltage level change	0.1	54	change pr149 from 38.3k to 68.1k(sd034681280)	2/5	DVT
13	For madison voltage level change	For madison voltage level change	0.1	54	change pr145 from 4.7k to 4.99k(sd034499180)	2/5	DVT
14	HW sequency request	HW sequency request	0.1	53	change pr199 from 200k to 150k for M96 VGA chip(sd034150380)	2/23	DVT
15	HW sequency request	HW sequency request	0.1	53	change pc177 from 0.22u to 0.1u for M96 VGA chip(se076104k80)	2/23	DVT
16	H_vttpwrgd glitch issue	H_vttpwrgd glitch issue	0.1	52	change PU500 pin14 pull high voltage from +5vs to +5valw	3/22	PVT
17	fix ki for all 030 project	fix ki for all 030 project	0.1	49	change pr269 from 80.6k to 150k(sd034150380) change pr260 from 100k to 140k(sd034140380)	3/29	PVT
18	fix kv for all 030 project	fix kv for all 030 project	0.1	49	change pr274 from 15.4k to 18.2k(sd034182280)	3/29	PVT
19	for IMON setting	for IMON setting	0.1	55	change pr55 from 4.53k to 5.36k, pc174 from 0.1u to 0.068u in UMA SKU	04/1	PVT
20	for RPM frequency setting	for RPM frequency setting	0.1	55	change pr174 from 47.5k to 69.8k,	04/1	PVT
21			0.1	47		01/21	DVT
22			0.1			01/21	DVT
23			0.1			01/21	DVT

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