Compal confidential

HGL30/HGL31 Schematics Document

Mobile Yonah uFCPGA with Intel 945GM/PM+ICH7-M

LA-3241P
REV:1.0
2006/4/28

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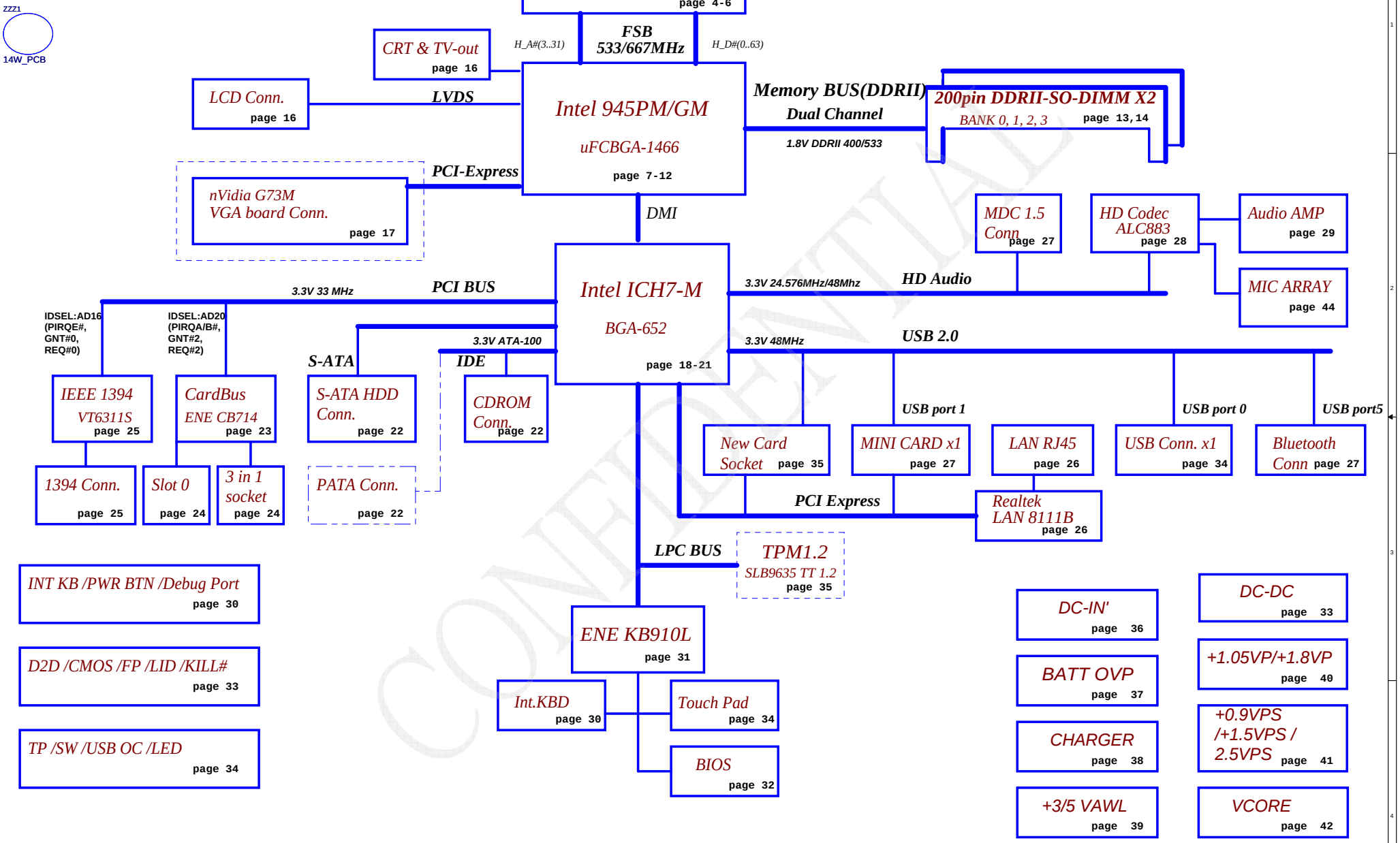
Model Name : HGL30
File Name : LA-3241P



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Voltage Rails

State \ power plane	+B LDO3 LDO5	+5VALW +3VALW	+1.8V +5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.2VS +VGA_CORE +0.9VS +CPU_CORE +VCCP
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

O MEANS ON
X MEANS OFF

S3 : STR
S4 : STD
S5 : SOFT OFF

SKU ID Table

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

SKU ID	HEL30/31 SKU
* 0	HEL30 SKU
1	HEL31 SKU
2	TEST MODE
3	
4	
5	
6	
7	

BOM Structure

MARK	FUNCTION
@	NC FOR ALL
UMA@	Internal 945GM
VGA@	External G7xM
TPM@	TPM1.2
VP1020@	MIC ARRAY
1394@	1394
SATA@	SATA HDD
ONEMIC@	ONE MIC
IOMP@	IOMP
PATA@	PATA HDD
APA@	HP out from AMP
HPA@	HP out from HP AMP
HP@	HP out from CODEC

USB PORT LIST

PORT	DEVICE
0	LEFT SIDE
1	BLUE TOOTH
2	RIGHT SIDE
3	CMOS
4	RIGHT SIDE
5	FINGER PRINTER
6	NEW CARD
7	

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/B
1394	AD16	0	PIRQE

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

EC SM Bus2 address

Device	Address
ADM1032	1001 100X b
EEPROM(24C02)	1010 000X b

ICH7 SM Bus address

Device	Address
Clock Generator (SLG8LP465VTR)	1101 001Xb
DDRII DIMM0	1010 000Xb
DDRII DIMM1	1010 010Xb

+3VALW	KB910L SB RTL8110SBL/CL	mA 160mA
+CPU_CORE	CPU	36A
+VCCP	CPU NB	2.5A 9.8A (14.7A)
+5VS	EXPRESS CARD HDD ODD MDC APA2066 TPA0211 AD1986 USB PORT * 6	1A 1.5A 1.8A 300mA 1A mA 70mA 3A
+3VS	NB EXPRESS CARD CLK_GEN LCDVCC VGA CARD (G7XM) SB R5C832 BIOS ROM KB910L CB1410	480mA 1A 200mA 1A 655mA 680mA mA 15mA 200mA mA
+2.5VS	VGA CARD (G7XM) NB	130mA (143mA)
+1.8V	DDR2_DIMM NB (667Mhz)	8A 3.1A
+1.8VS	GDDR2 VGA CARD (G7XM)	6A 4.06A
+0.9VREF	DDR2_DIMM	10mA
+0.9VS	GDDR2 DDR2_DIMM	1A 2A
+1.5V	SB	40mA
+1.5VS	NB SB MiniCard EXPRESS CARD VGA CARD (G7XM)	8.9A(13.8A) 3.8A 1A 0.65A 2A

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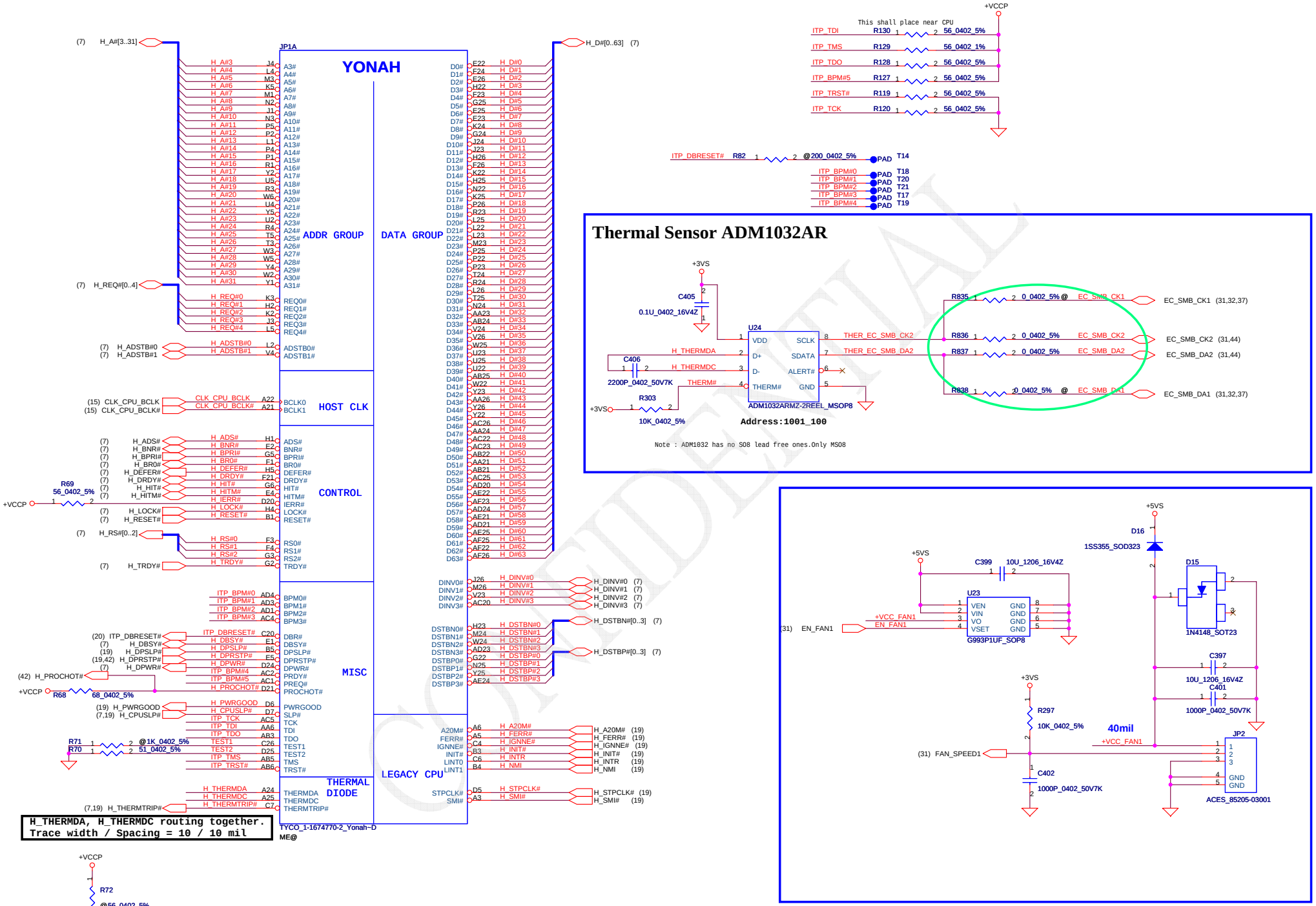

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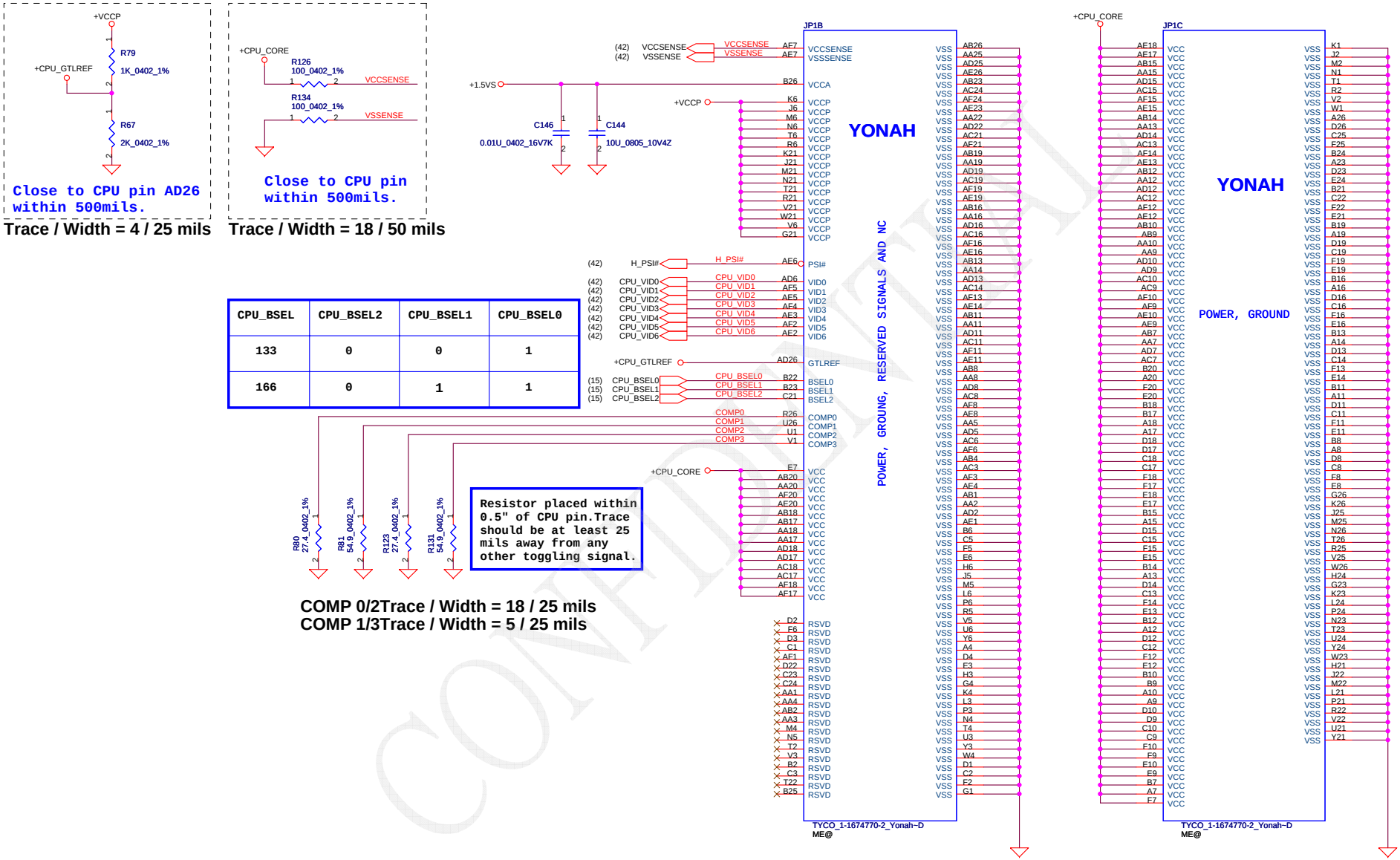

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

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3/29:from 22uF change to 10uF

+CPU_CORE

Place these capacitors on L8 (North side,Secondary Layer)

C411 10U_0805_6.3V6M, C417 10U_0805_6.3V6M, C175 10U_0805_6.3V6M, C193 10U_0805_6.3V6M, C443 10U_0805_6.3V6M, C191 10U_0805_6.3V6M, C206 10U_0805_6.3V6M, C208 10U_0805_6.3V6M

+CPU_CORE

Place these capacitors on L8 (North side,Secondary Layer)

C416 10U_0805_6.3V6M, C212 10U_0805_6.3V6M, C437 10U_0805_6.3V6M, C201 10U_0805_6.3V6M, C409 10U_0805_6.3V6M, C211 10U_0805_6.3V6M, C189 10U_0805_6.3V6M, C438 10U_0805_6.3V6M

+CPU_CORE

Place these capacitors on L8 (Sorth side,Secondary Layer)

C207 10U_0805_6.3V6M, C192 10U_0805_6.3V6M, C428 10U_0805_6.3V6M, C412 10U_0805_6.3V6M, C195 10U_0805_6.3V6M, C427 10U_0805_6.3V6M, C204 10U_0805_6.3V6M, C199 10U_0805_6.3V6M

+CPU_CORE

Place these capacitors on L8 (Sorth side,Secondary Layer)

C174 10U_0805_6.3V6M, C188 10U_0805_6.3V6M, C442 10U_0805_6.3V6M, C196 10U_0805_6.3V6M, C202 10U_0805_6.3V6M, C200 10U_0805_6.3V6M, C410 10U_0805_6.3V6M, C205 10U_0805_6.3V6M

Mid Frequence Decoupling

+CPU_CORE

South Side Secondary

C414 330U_D2E_2.5VM_R9, C198 330U_D2E_2.5VM_R9, C197 330U_D2E_2.5VM_R9, C431 330U_D2E_2.5VM_R9, C413 330U_D2E_2.5VM_R9, C415 330U_D2E_2.5VM_R9

North Side Secondary

ESR <= 1.5m ohm
Capacitor > 1980uF

+VCCP

C131 220U_D2_2VMR15

C209 0.1U_0402_16V4Z, C176 0.1U_0402_16V4Z, C178 0.1U_0402_16V4Z, C177 0.1U_0402_16V4Z, C210 0.1U_0402_16V4Z, C213 0.1U_0402_16V4Z

Place these inside socket cavity on L8 (North side Secondary)

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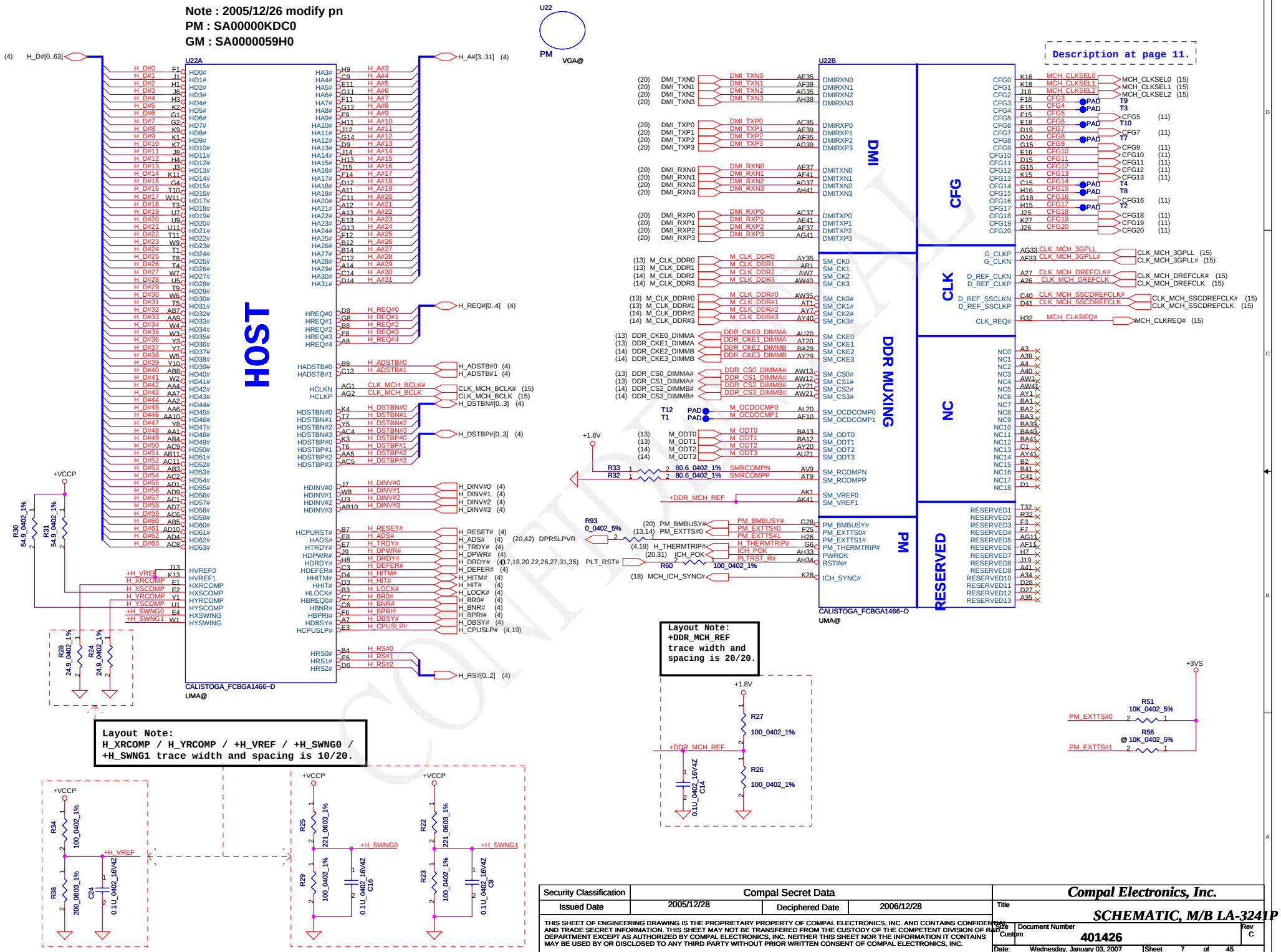
Note : 2005/12/26 modify pn
PM : SA00000KDC0
GM : SA0000059H0



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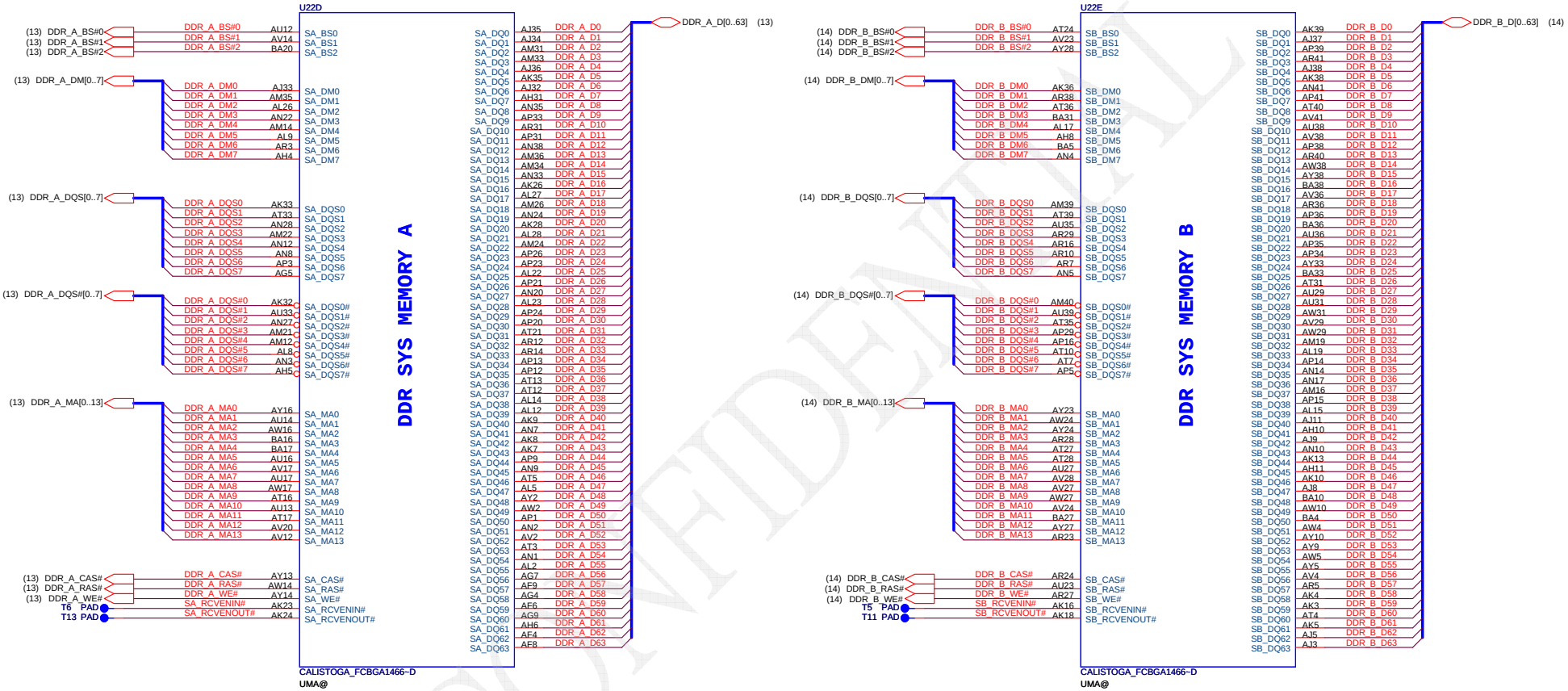

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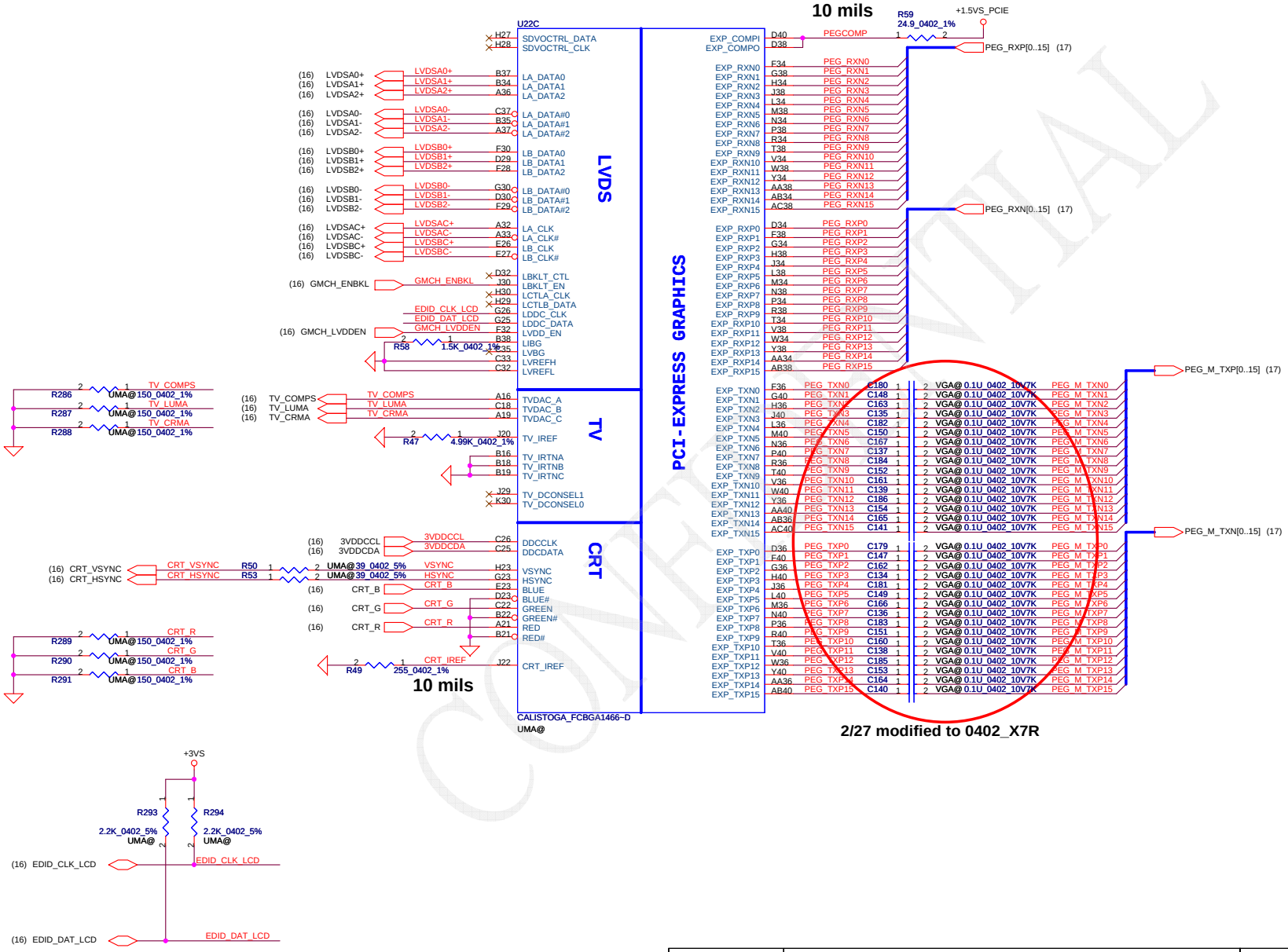

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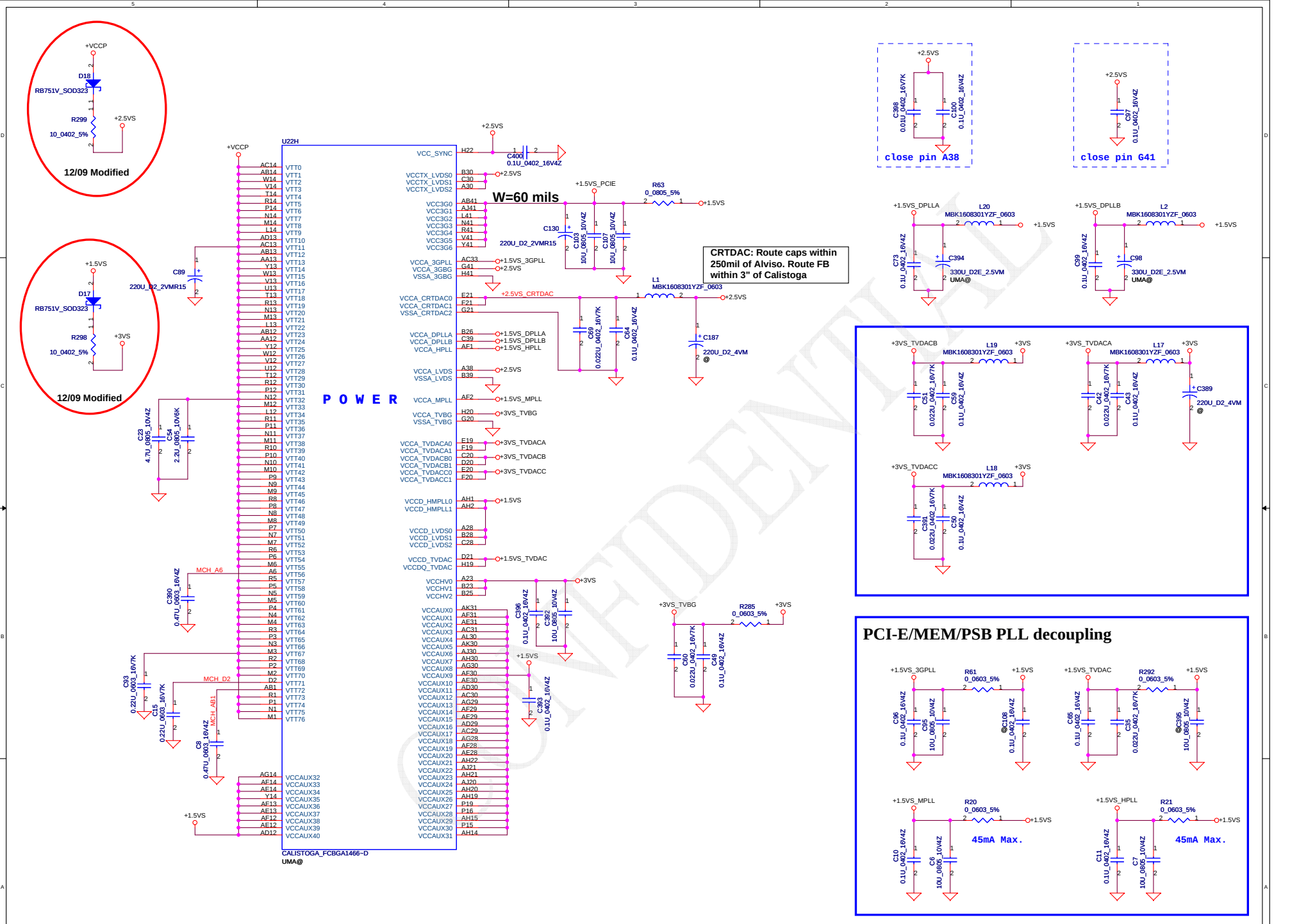

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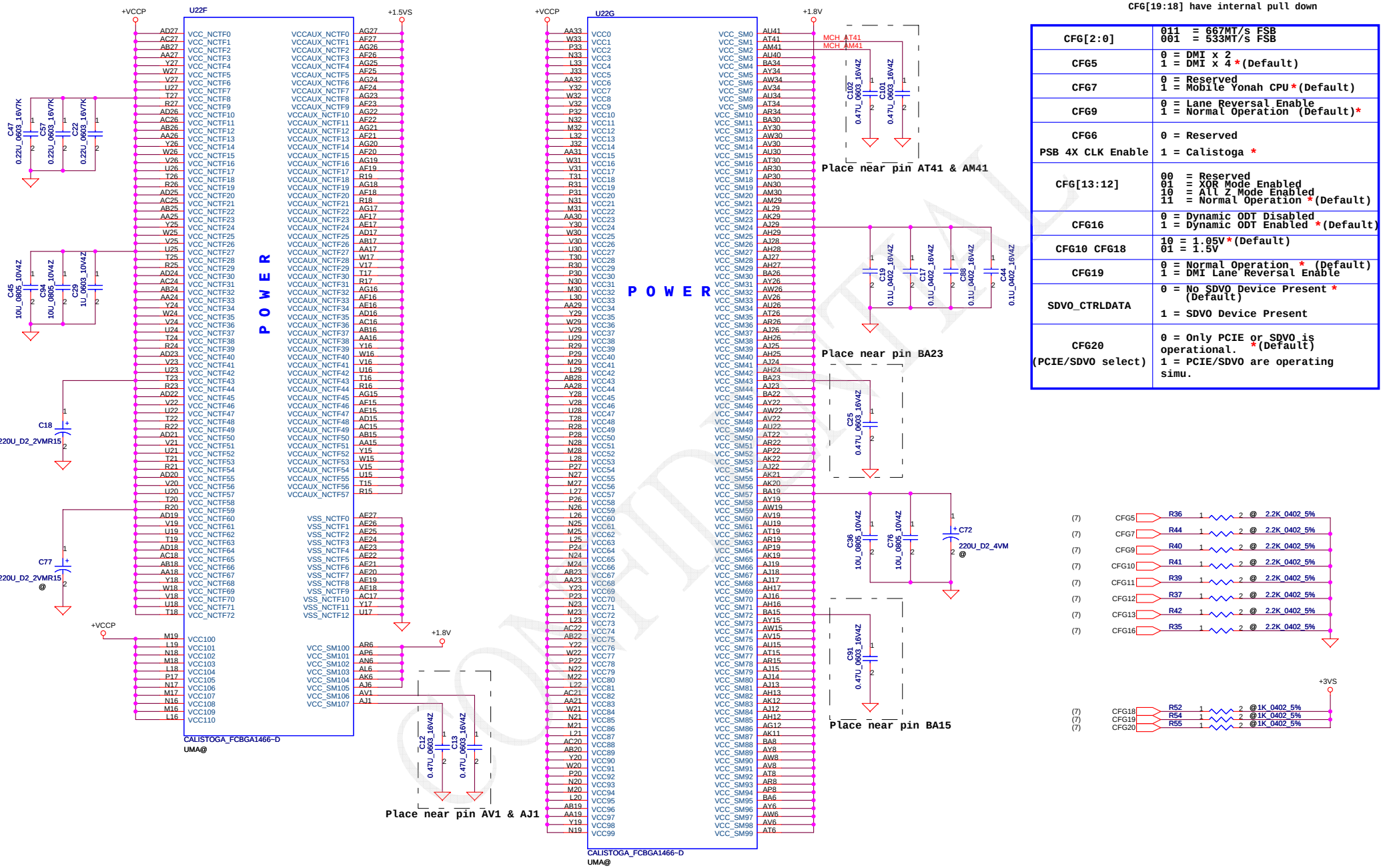
Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6 PSB 4X CLK Enable	0 = Reserved 1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V *(Default) 01 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



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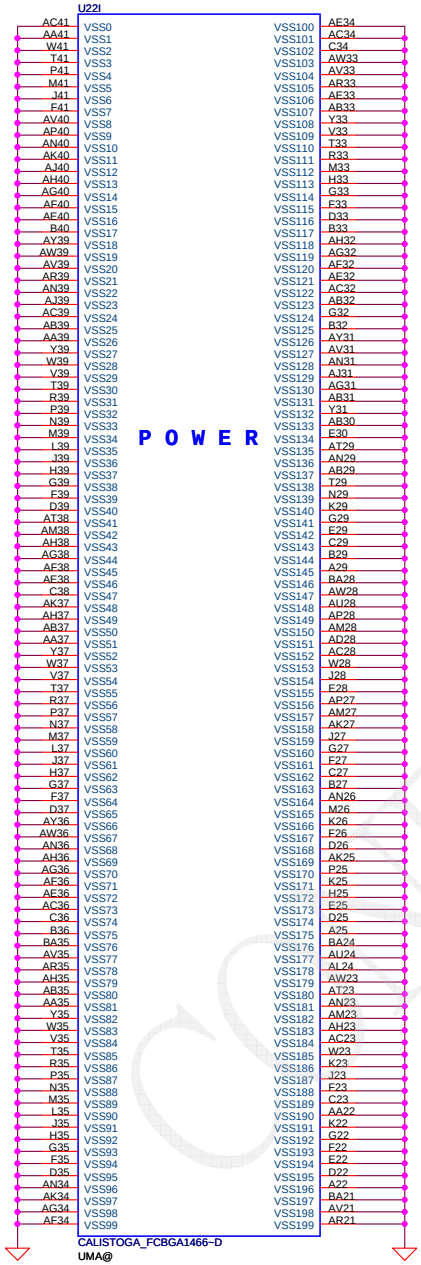

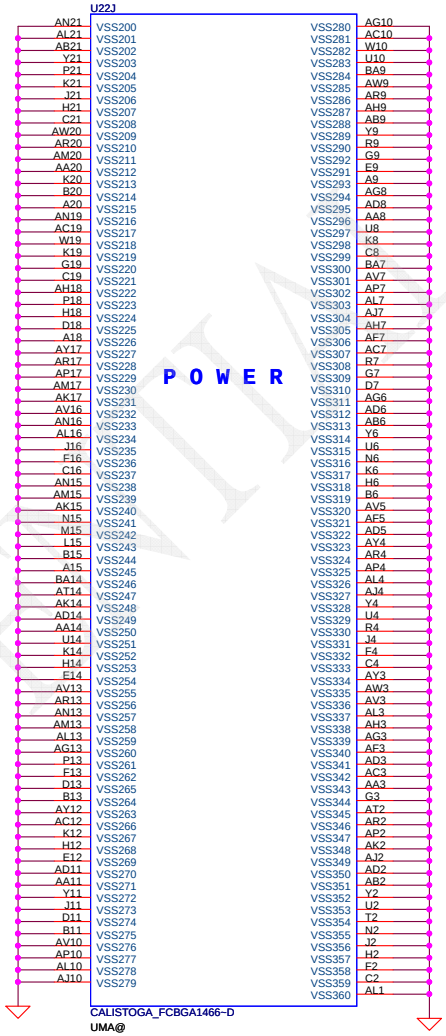

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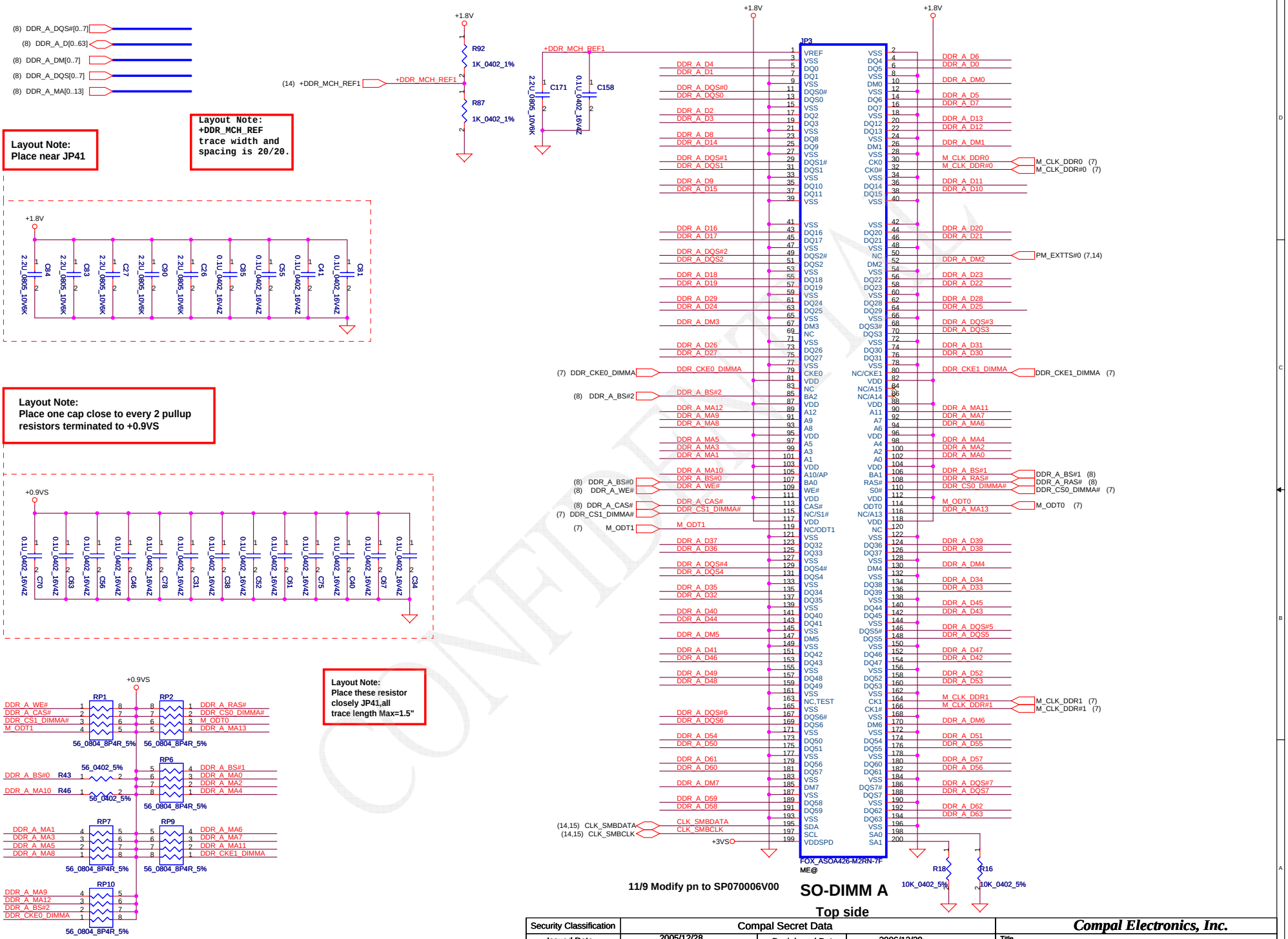

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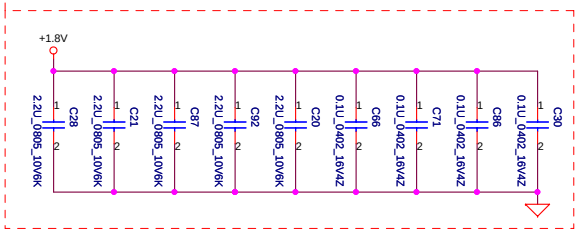
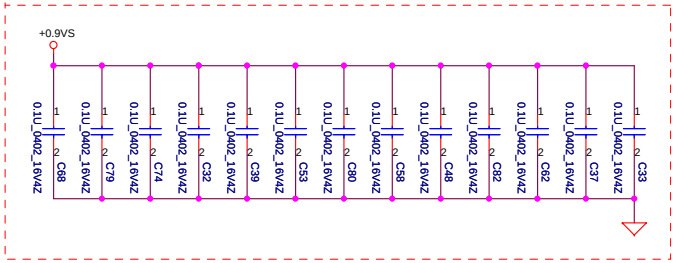
(8) DDR_B_DQS#[0..7]
(8) DDR_B_D[0..63]
(8) DDR_B_DM[0..7]
(8) DDR_B_DQS[0..7]
(8) DDR_B_MA[0..13]

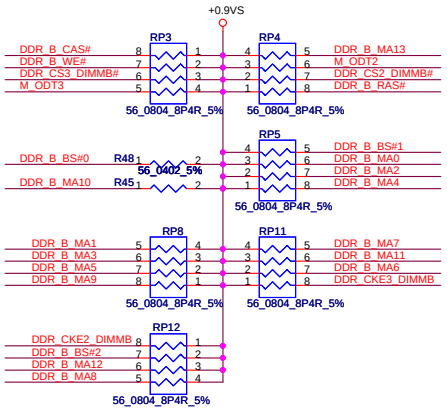
Layout Note:
Place near JP42

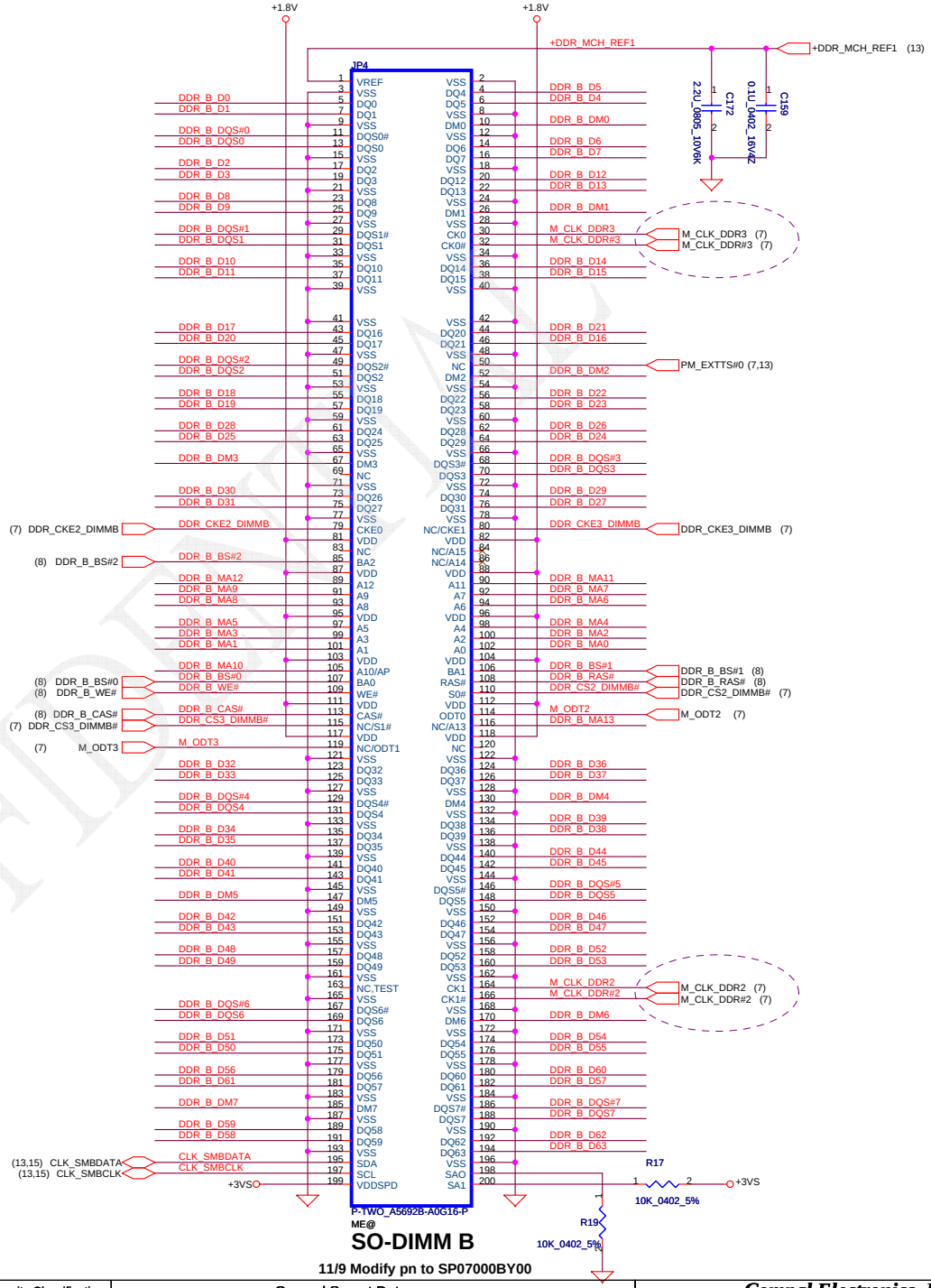


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP42,all trace length Max=1.5"





11/9 Modify pn to SP07000BY00

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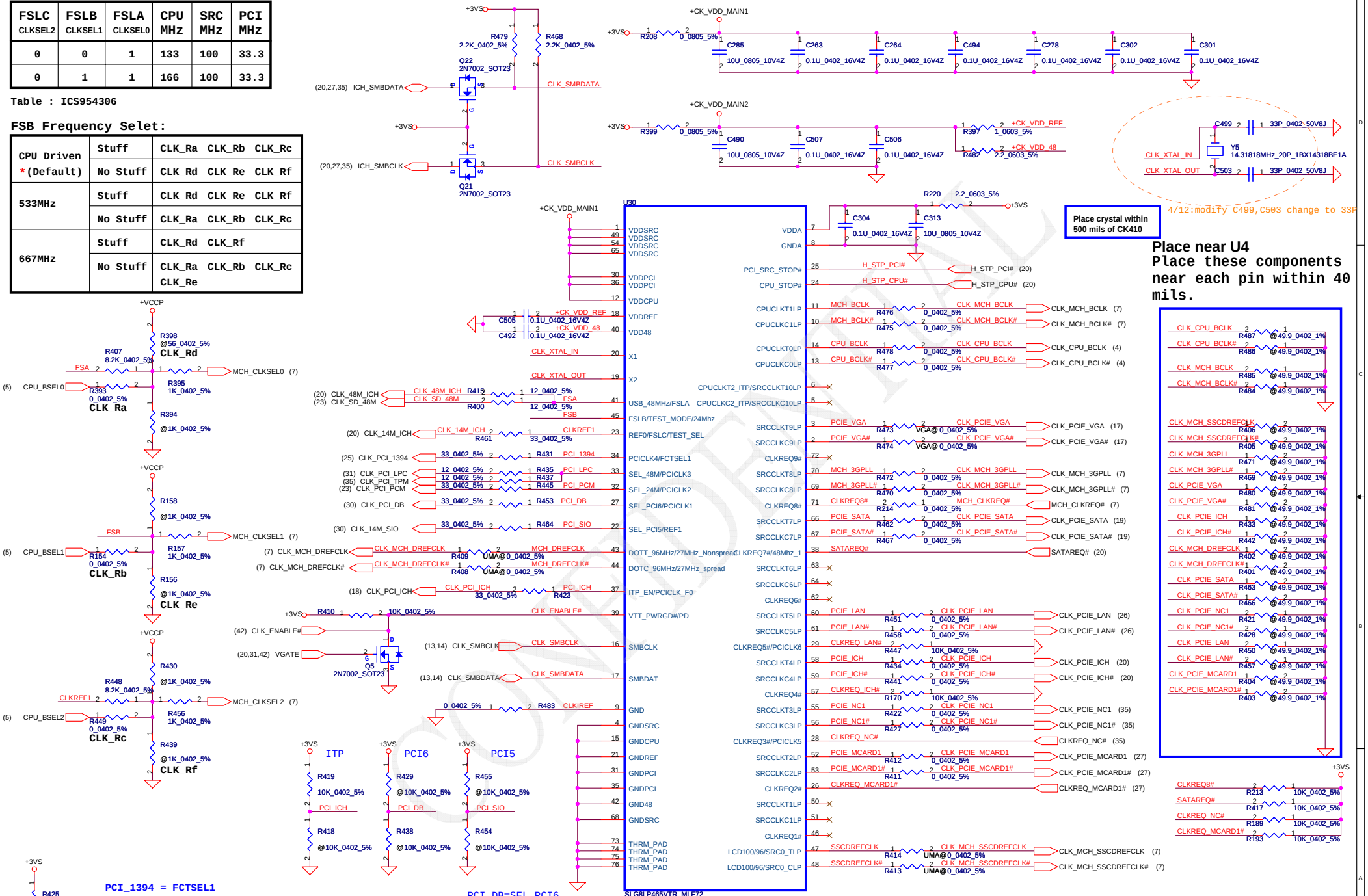
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS954306

FSB Frequency Selet:

CPU Driven *(Default)	Stuff	CLK_Ra CLK_Rb CLK_Rc
	No Stuff	CLK_Rd CLK_Re CLK_Rf
533MHz	Stuff	CLK_Rd CLK_Re CLK_Rf
	No Stuff	CLK_Ra CLK_Rb CLK_Rc
667MHz	Stuff	CLK_Rd CLK_Rf
	No Stuff	CLK_Ra CLK_Rb CLK_Rc CLK_Re



FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0	DOT96T	DOT96C	96/100M_T	96/100M_C
1	27Mout	27MSSout	SRCT0	SRCC0

PCI_DB	PIN27
0	CLKREQ5
1	PCICLK6

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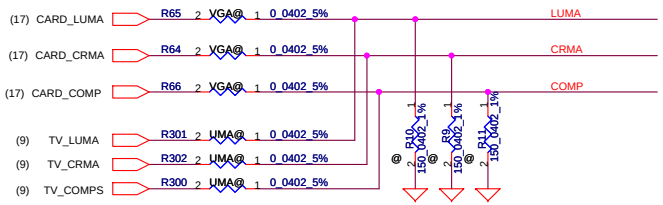
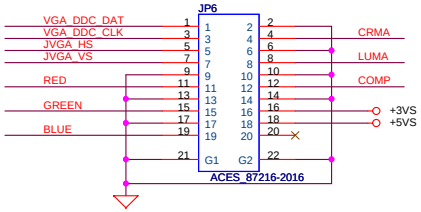
TV-OUT Conn.

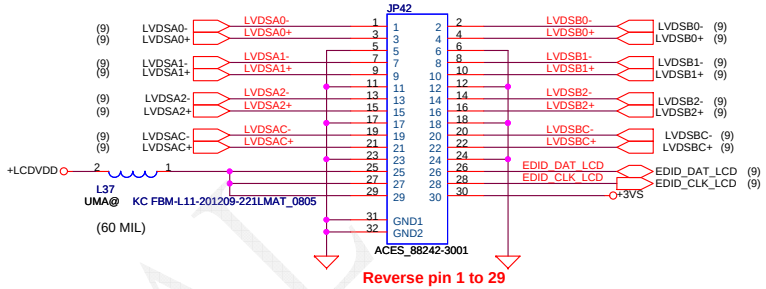


Pop when with internal graphics

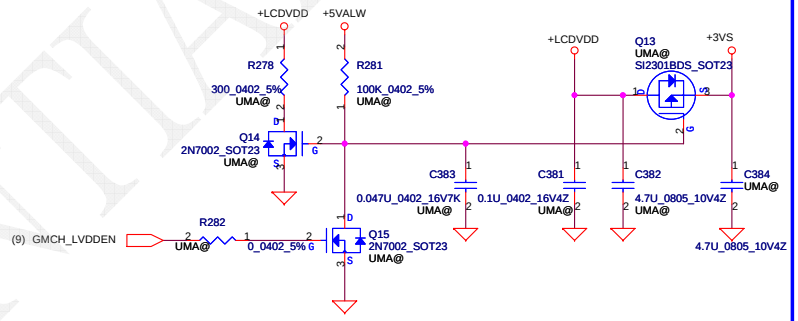
VGA I/O PORT Conn.



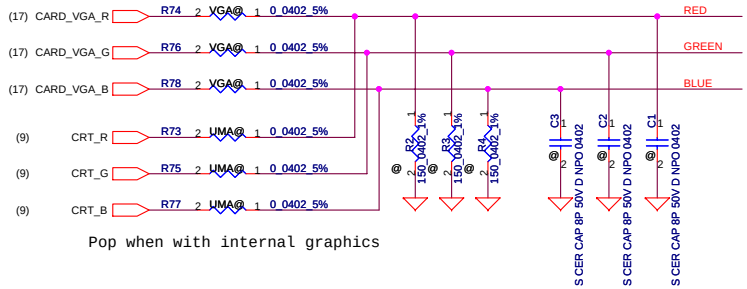
UMA LCD / PANEL Conn.



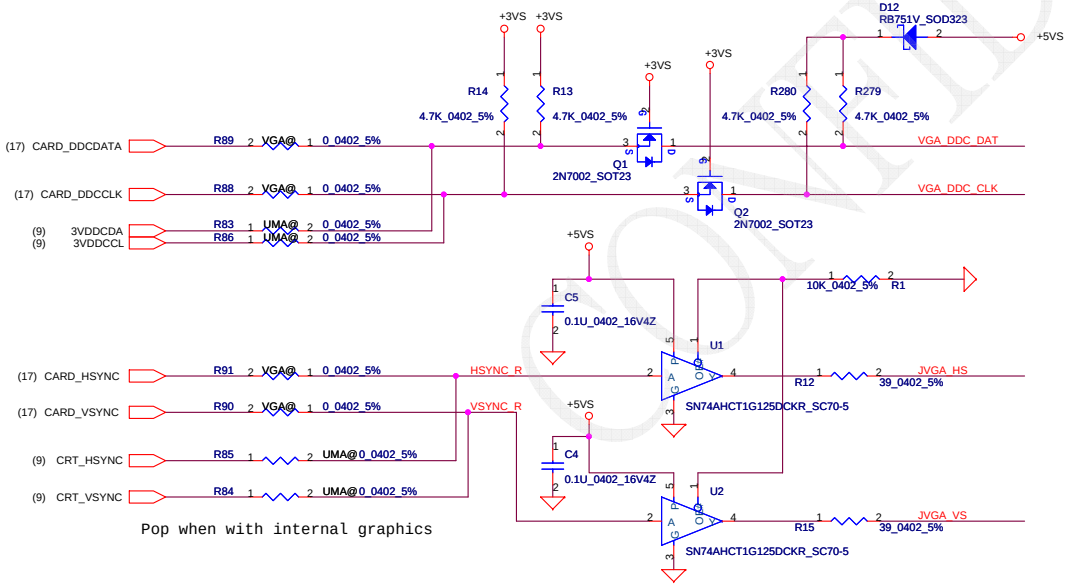
Reverse pin 1 to 29



CRT Conn.

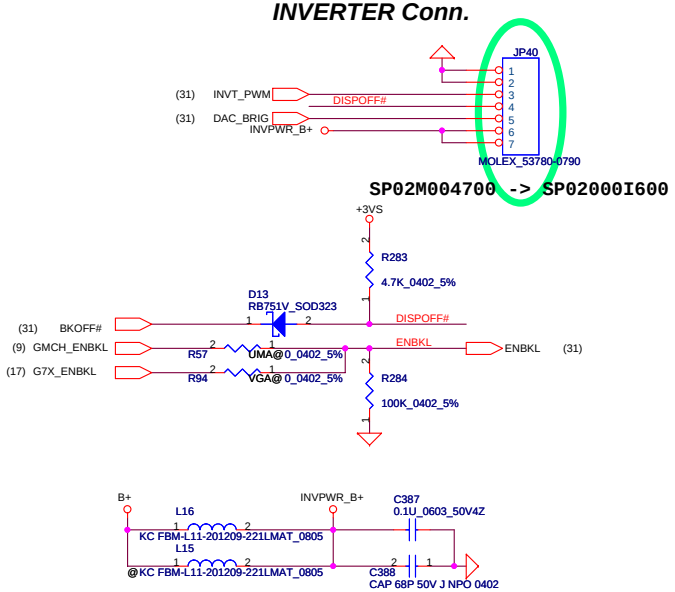


Pop when with internal graphics



Pop when with internal graphics

INVERTER Conn.



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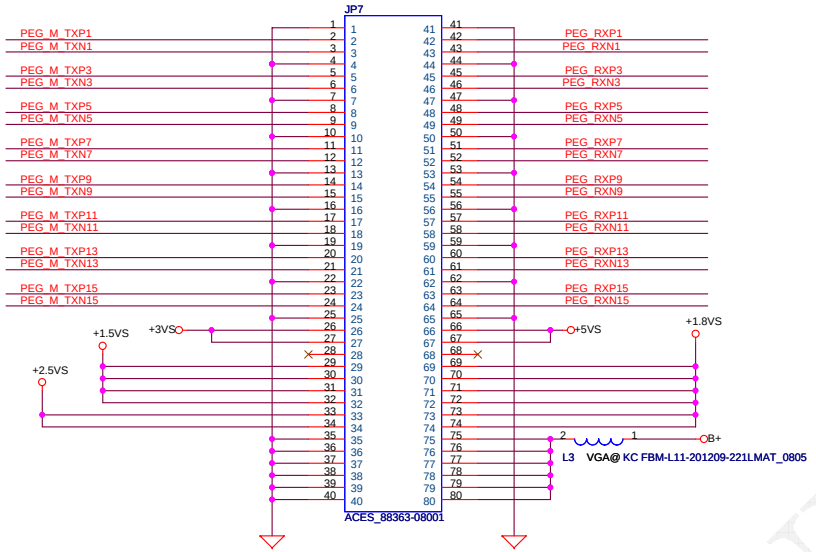
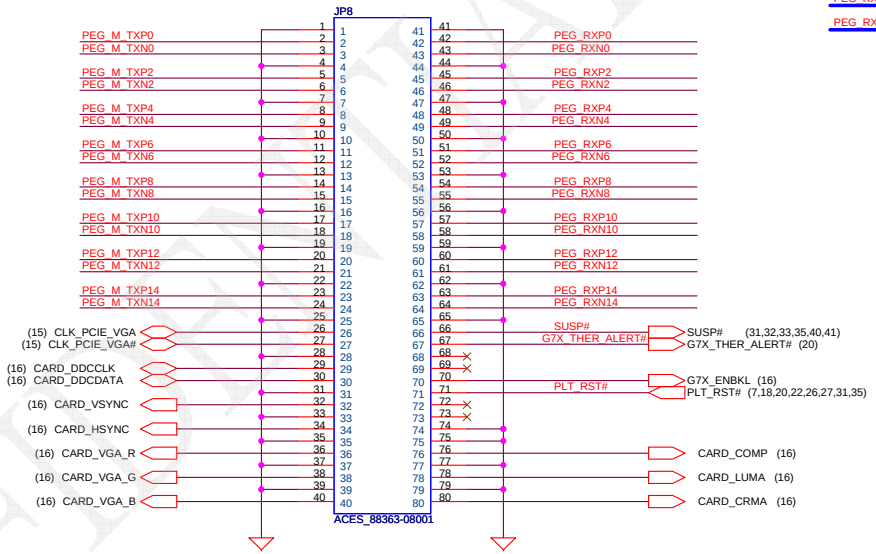
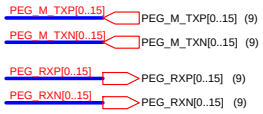
MAX. 4.06A @ 1.8V

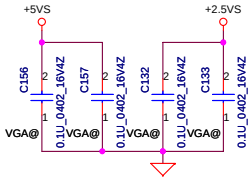
MAX. 130mA @ 2.5V

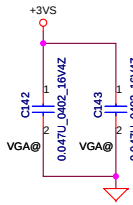
MAX. 655mA @ 3.3V











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Custom	401426	C

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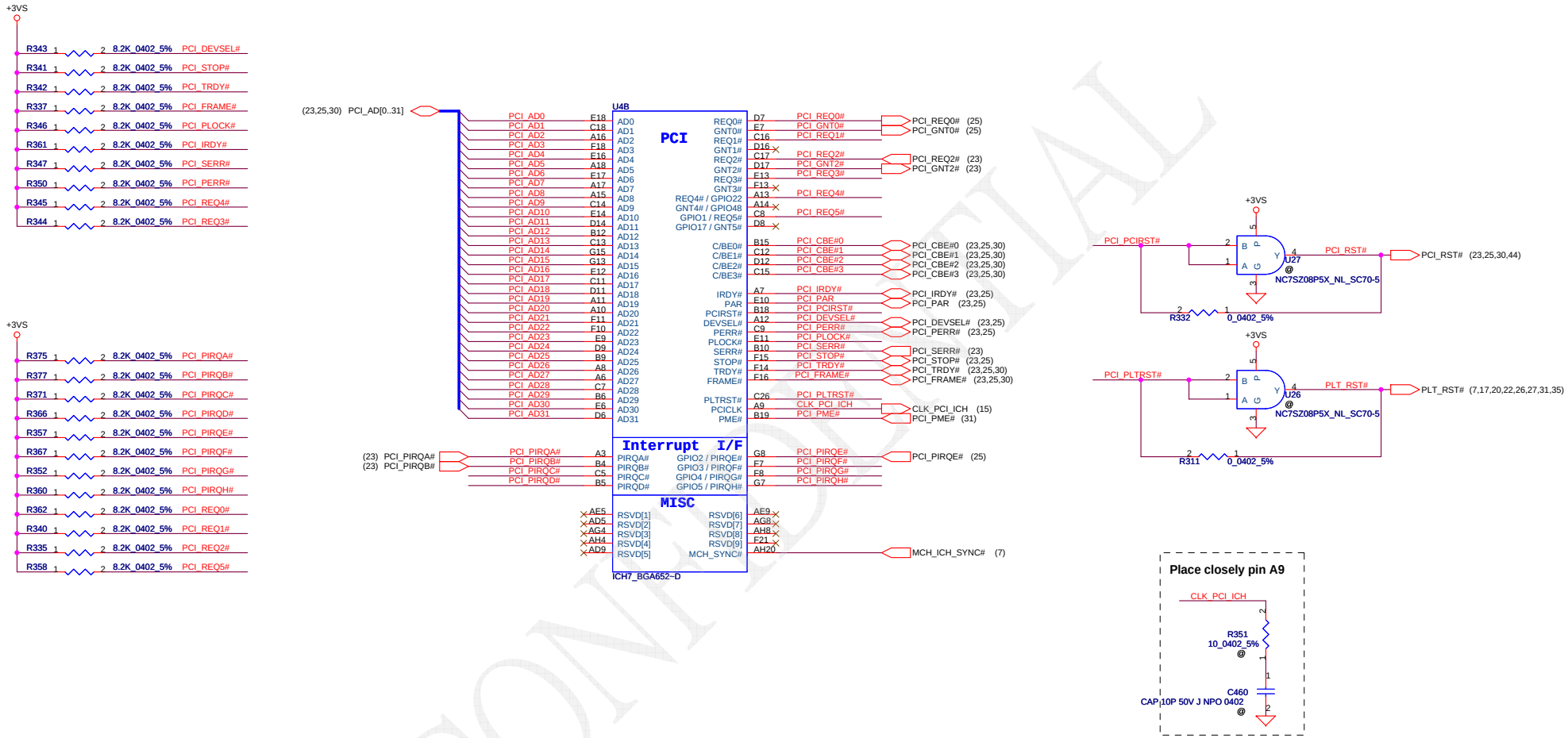

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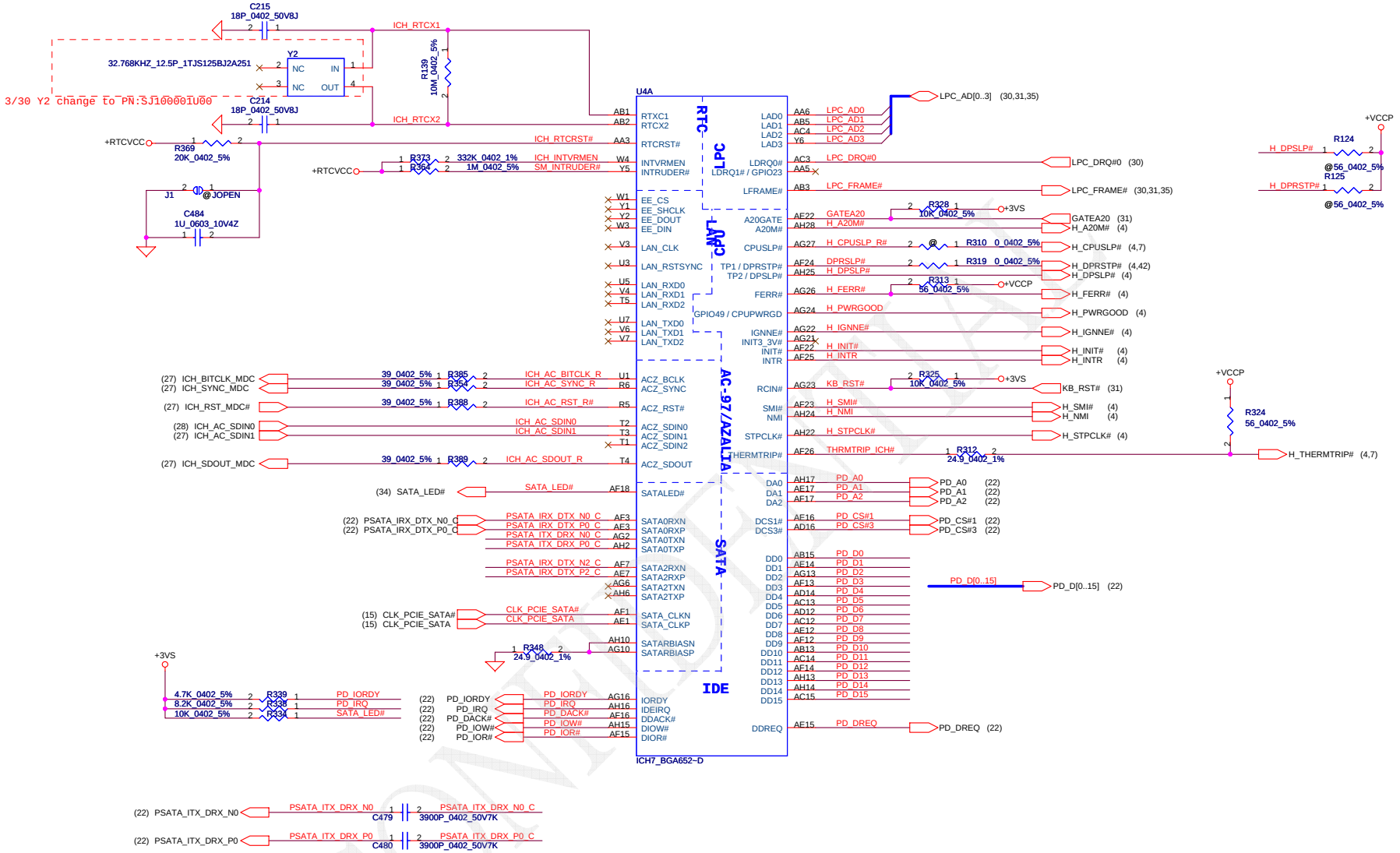

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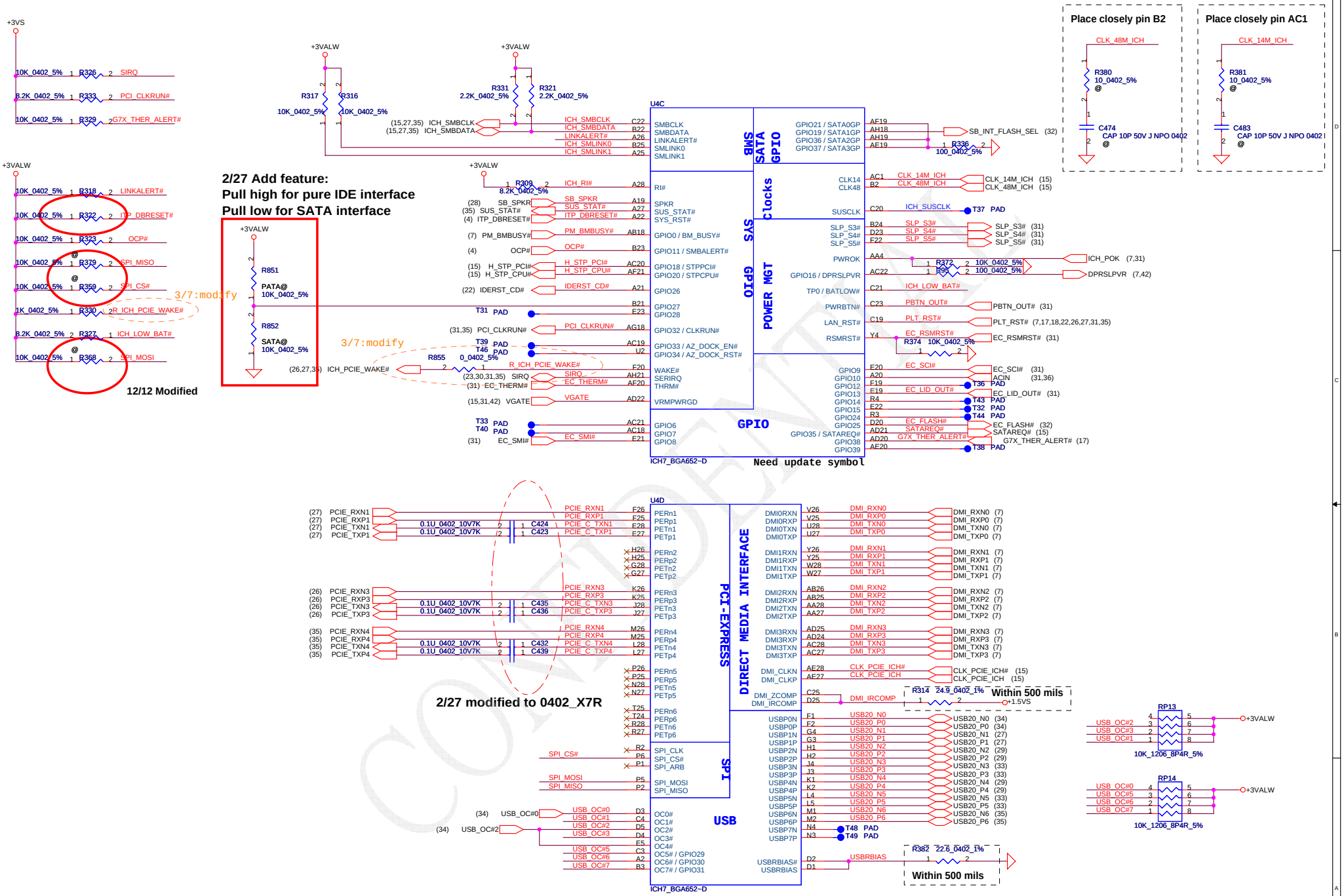

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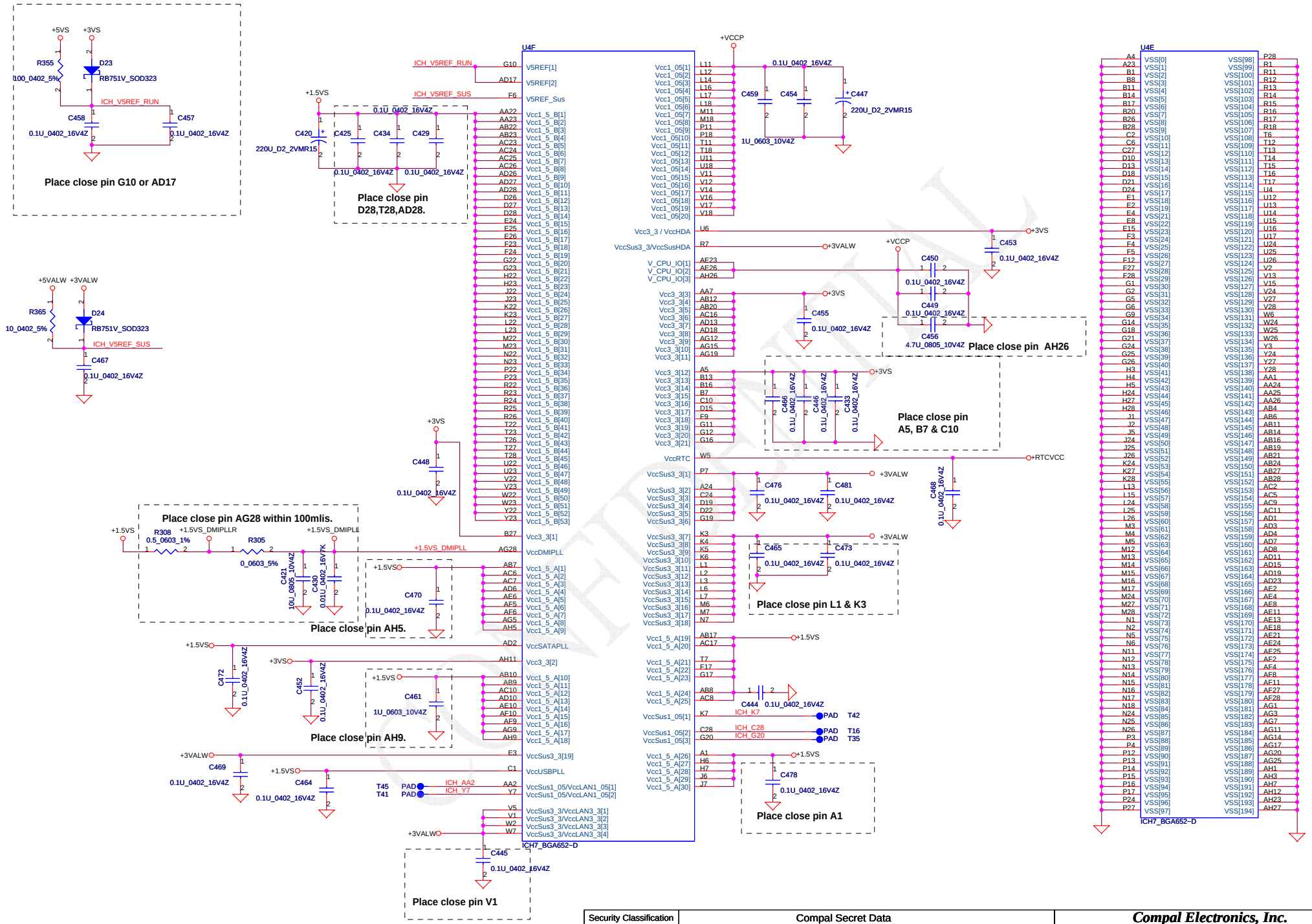

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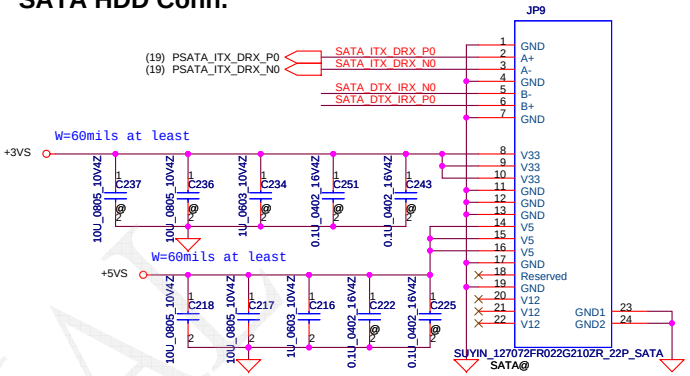
2005/11/4 Modified library pn:DC010003J00

SATA HDD Conn.

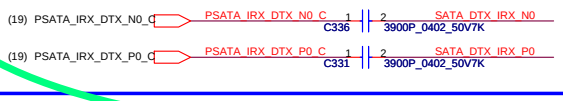
Main SATA +5V Default

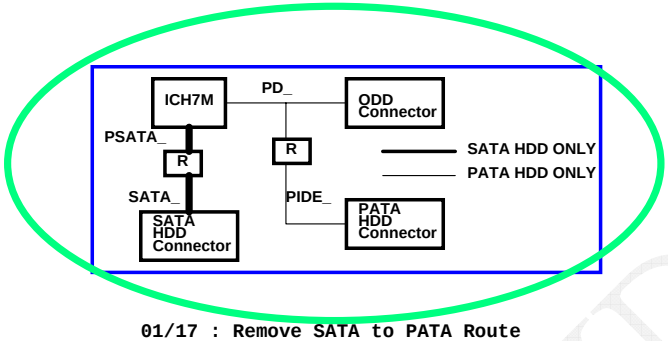


Place closed to 3811

2005/09/04

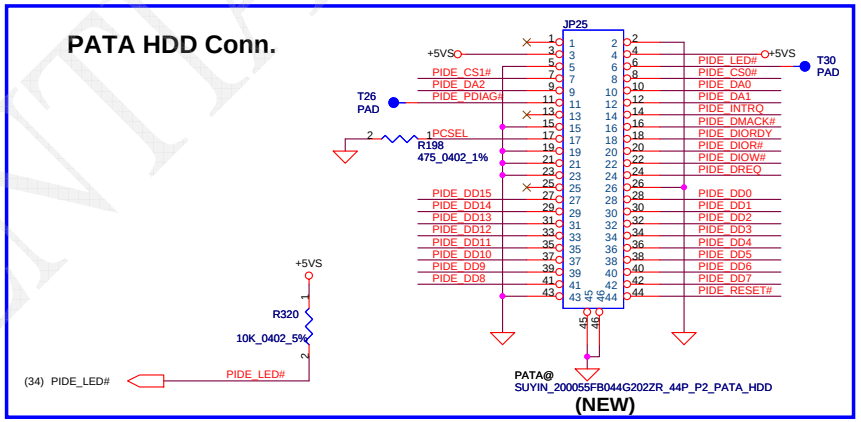
01/18 : Remove RP15,RP16





01/17 : Remove SATA to PATA Route

PATA HDD Conn.

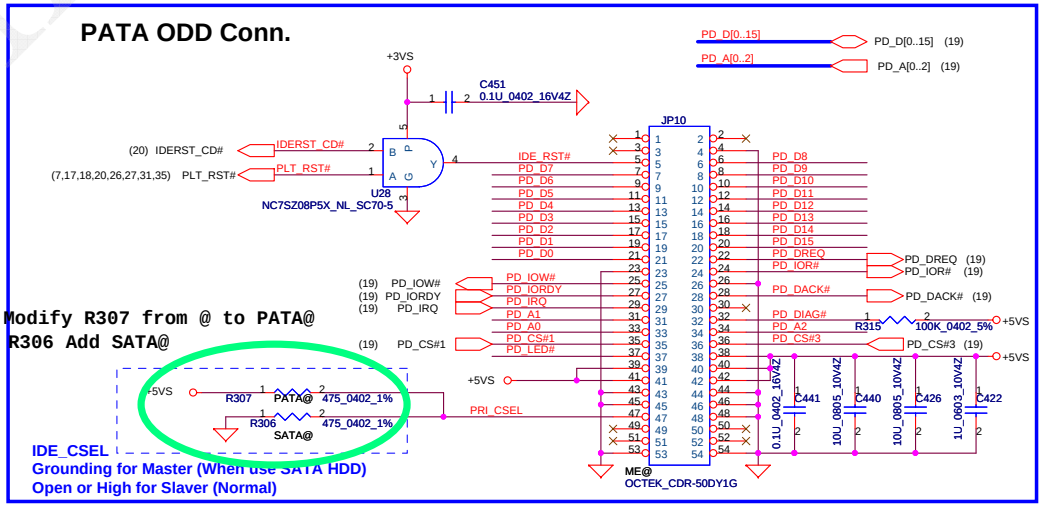


(NEW)

PD_D2	R194	PATA@	0_0402_5%	PIDE_DD2
PD_D12	R199	PATA@	0_0402_5%	PIDE_DD12
PD_D3	R205	PATA@	0_0402_5%	PIDE_DD3
PD_D11	R210	PATA@	0_0402_5%	PIDE_DD11
PD_D4	R215	PATA@	0_0402_5%	PIDE_DD4
PD_D10	R217	PATA@	0_0402_5%	PIDE_DD10
PD_D5	R218	PATA@	0_0402_5%	PIDE_DD5
PD_D9	R222	PATA@	0_0402_5%	PIDE_DD9
PD_D6	R225	PATA@	0_0402_5%	PIDE_DD6
PD_D8	R227	PATA@	0_0402_5%	PIDE_DD8
PD_D7	R231	PATA@	0_0402_5%	PIDE_DD7
IDE_RST#	R241	PATA@	0_0402_5%	PIDE_RESET#
PD_D0	R177	PATA@	0_0402_5%	PIDE_DD0
PD_D14	R176	PATA@	0_0402_5%	PIDE_DD14
PD_D1	R175	PATA@	0_0402_5%	PIDE_DD1
PD_D13	R190	PATA@	0_0402_5%	PIDE_DD13
PD_IOR#	R181	PATA@	0_0402_5%	PIDE_DIOR#
PD_IOW#	R180	PATA@	0_0402_5%	PIDE_DIOW#
PD_DREQ	R179	PATA@	0_0402_5%	PIDE_DREQ
PD_D15	R178	PATA@	0_0402_5%	PIDE_DD15
PD_A1	R185	PATA@	0_0402_5%	PIDE_DA1
PD_IRQ	R184	PATA@	0_0402_5%	PIDE_INTRQ
PD_DACK#	R183	PATA@	0_0402_5%	PIDE_DMACK#
PD_IORDY	R182	PATA@	0_0402_5%	PIDE_DIORDY
PD_CS#3	R207	PATA@	0_0402_5%	PIDE_CS1#
PD_CS#1	R203	PATA@	0_0402_5%	PIDE_CS0#
PD_A2	R187	PATA@	0_0402_5%	PIDE_DA2
PD_A0	R186	PATA@	0_0402_5%	PIDE_DA0
PD_DIAG#	R169	PATA@	0_0402_5%	PIDE_PDIAG#

PD_LED# — R853 — PATA@ — 0_0402_5% — PIDE_LED#

PATA ODD Conn.



01/17 : Modify R307 from @ to PATA@
R306 Add SATA@

IDE_CSEL
Grounding for Master (When use SATA HDD)
Open or High for Slaver (Normal)

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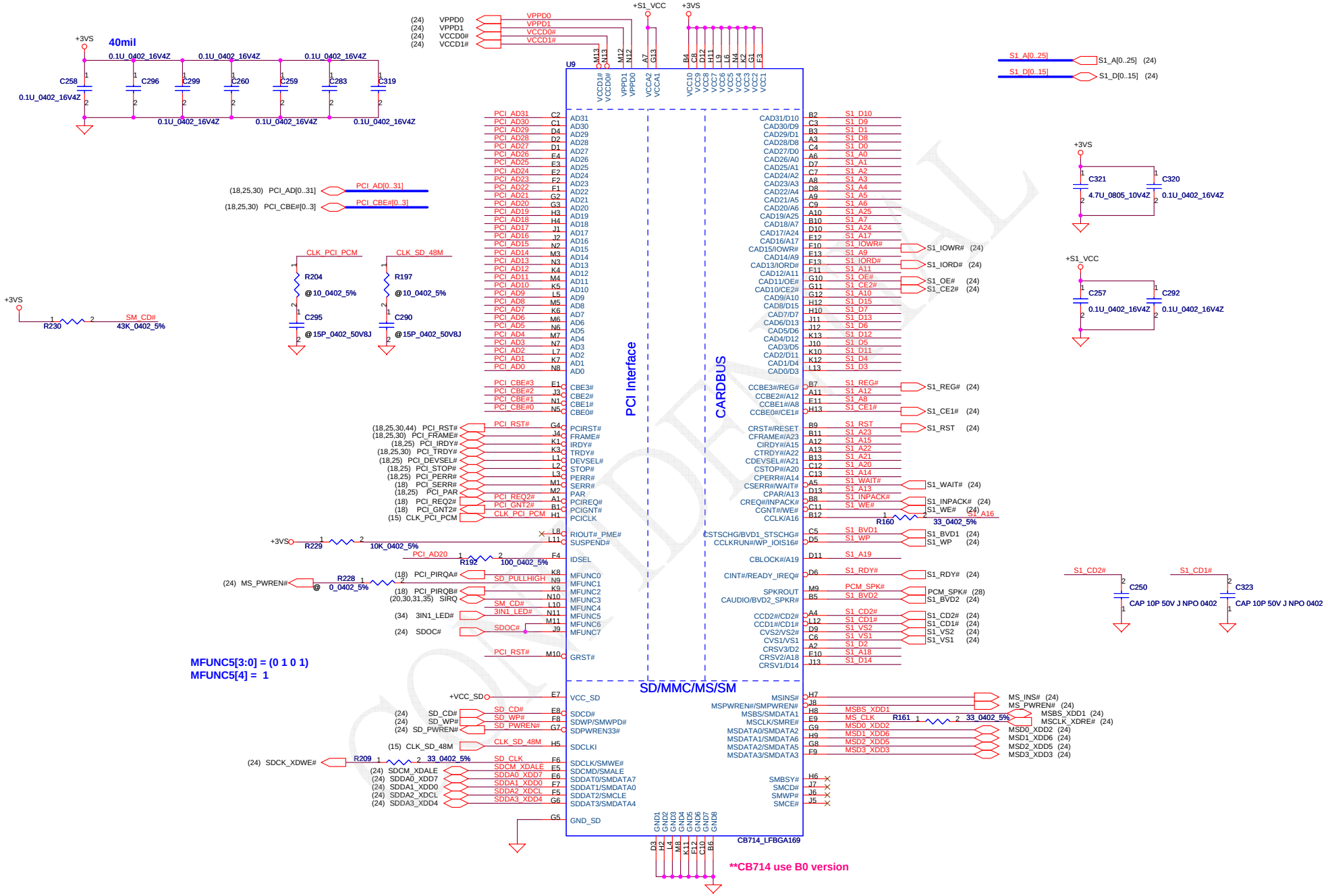

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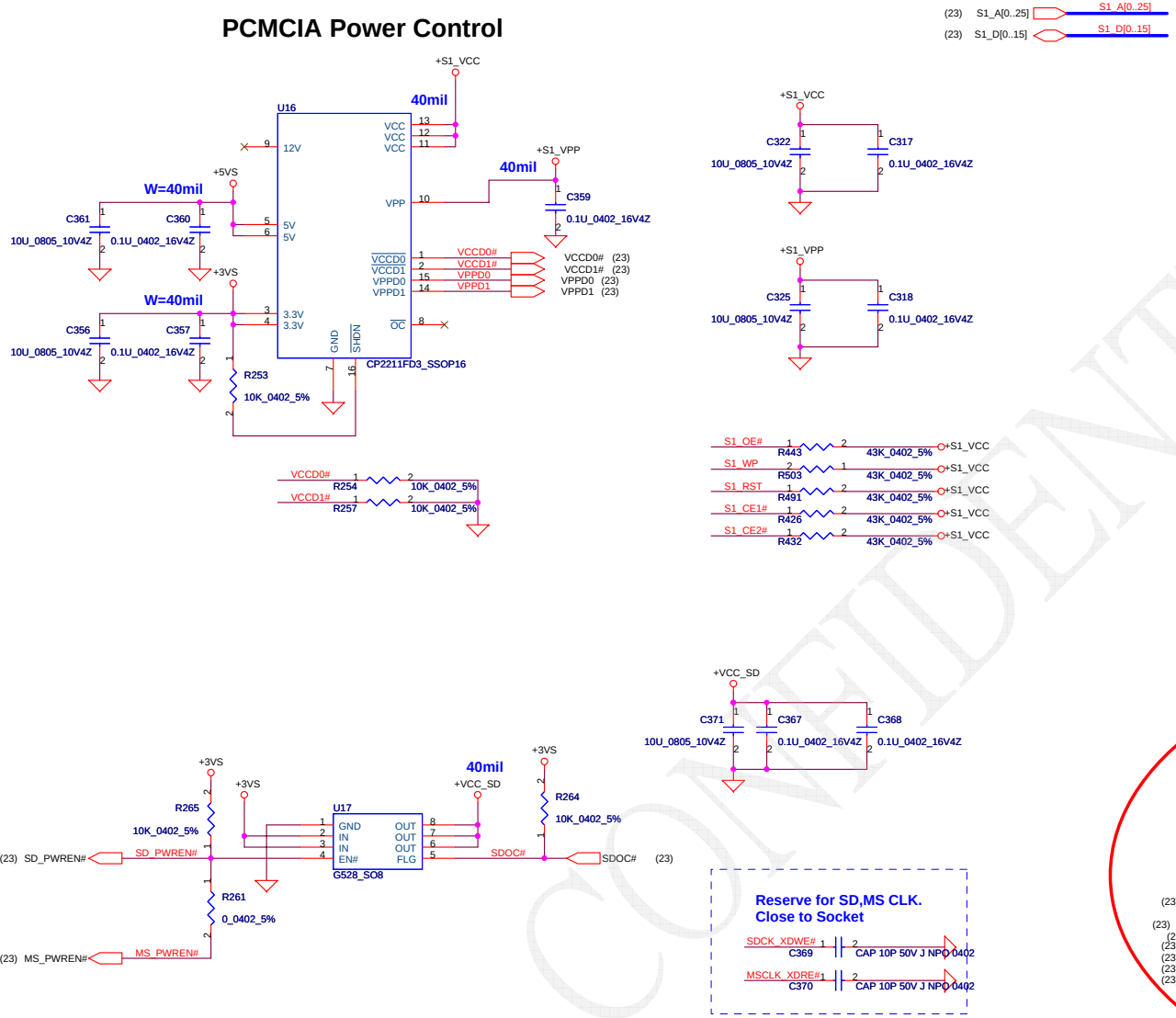
PCMCIA Socket

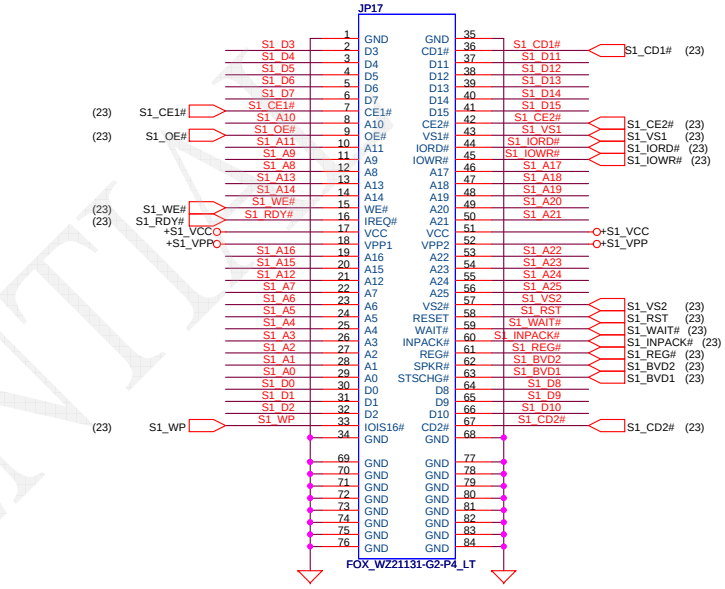
Note : 11/10 modify library to meet spec

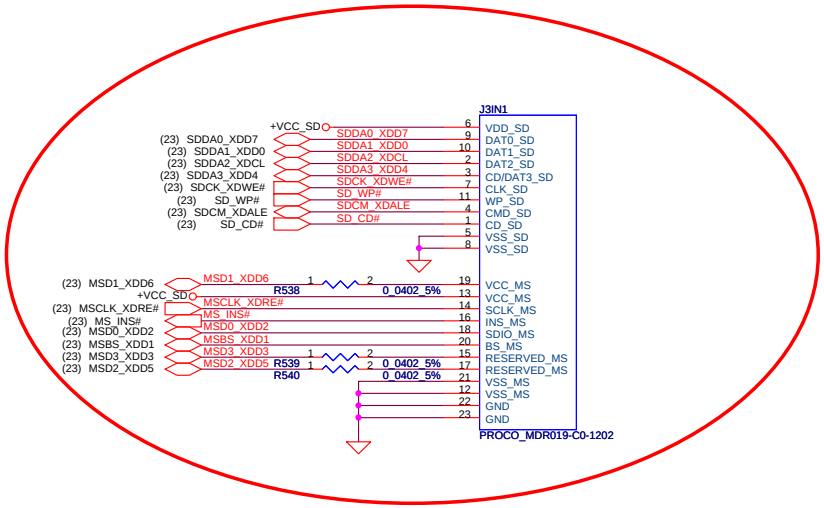
pn: SP01000IC00

11/14 modify footprint to FOX_1CA41521-TC2-4F_68P_LT

PCMCIA Power Control







12/20 modified

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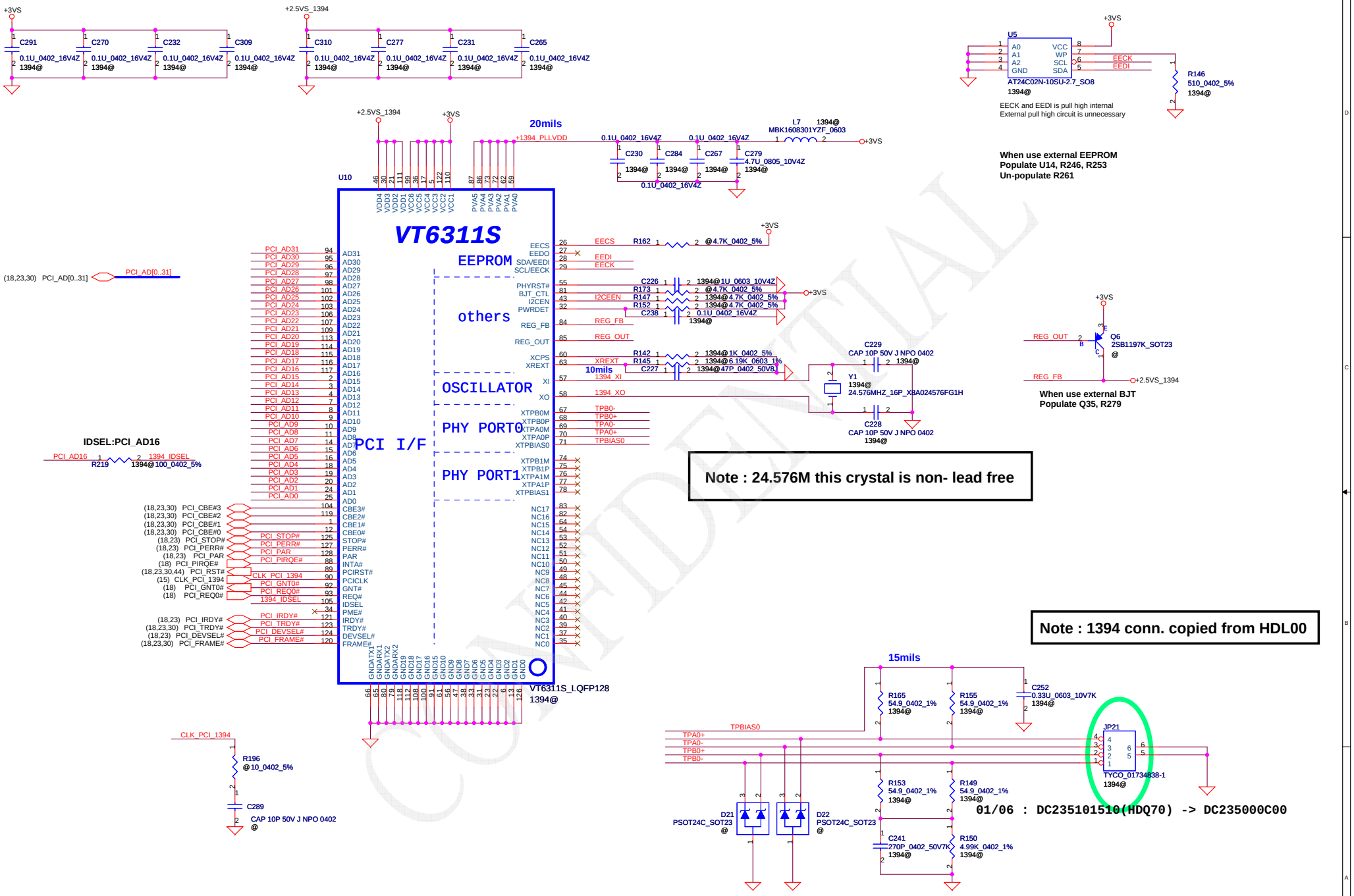

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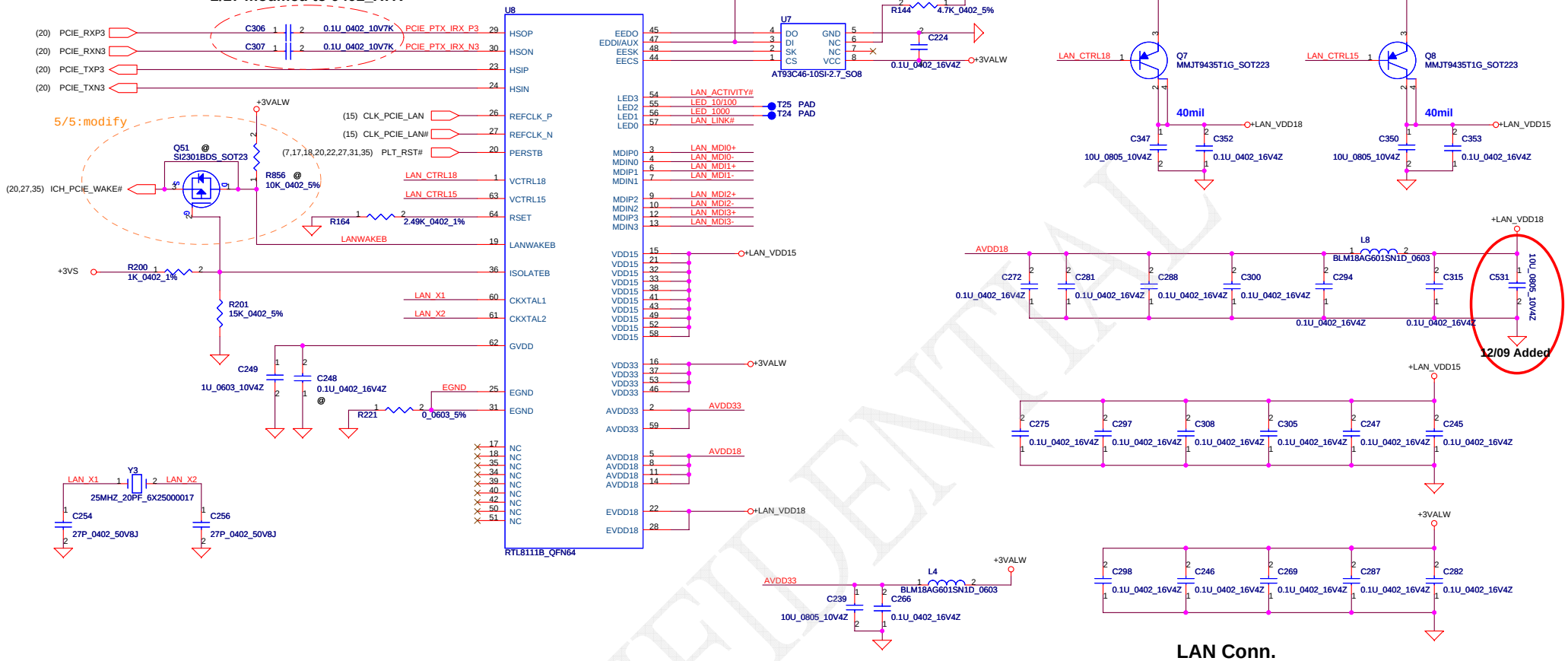
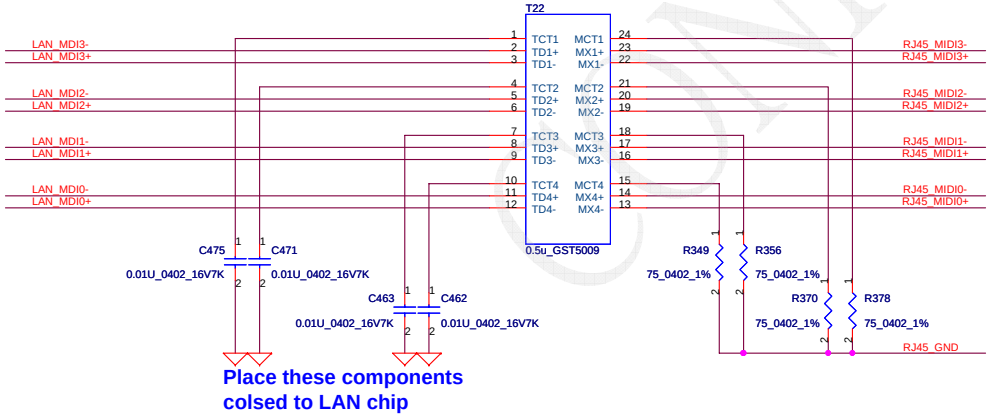
PN : SA00000TL00 (QFN64 Lead Free)

2/27 modified to 0402_X7R

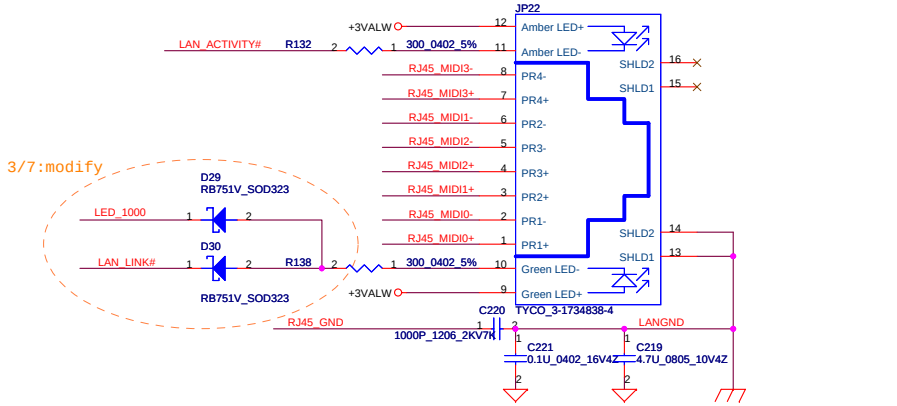


GbE Transformer: GST5009 (SP050005610) MY



LAN Conn.

01/06 : DC234103600(HAZ00) -> DC234001A00



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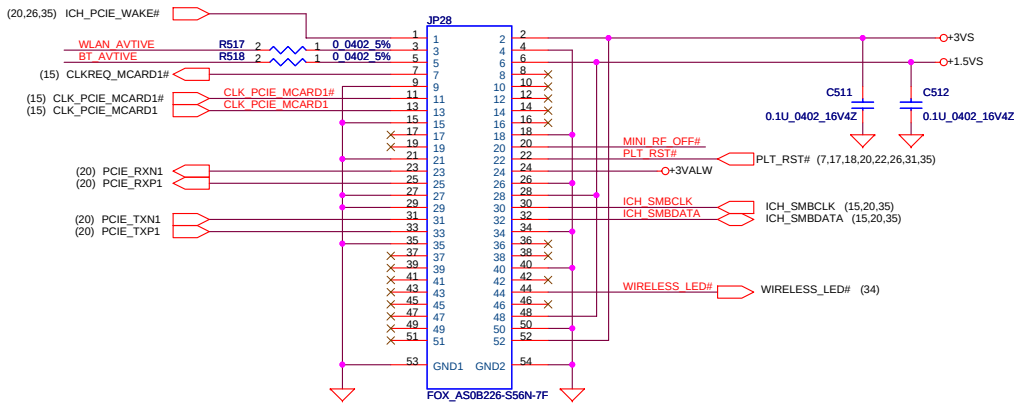
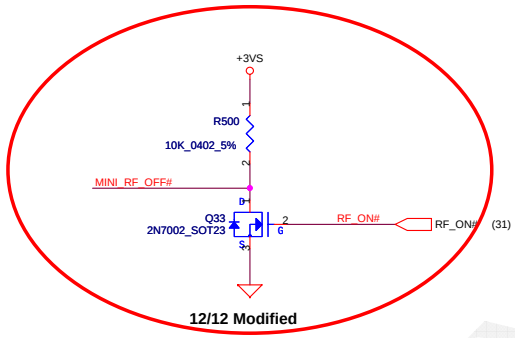
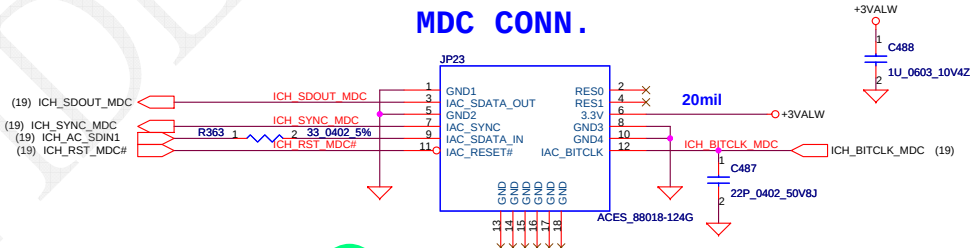
Mini-Express Card(Slot 1-WLAN)





MDC CONN.

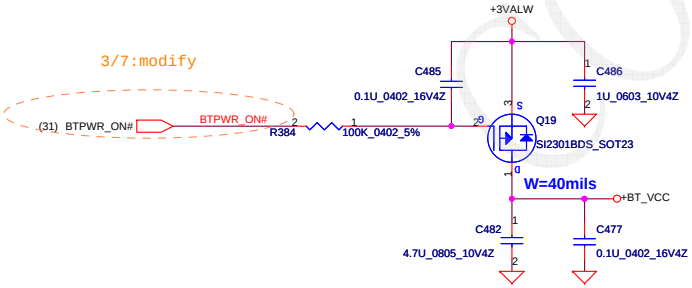


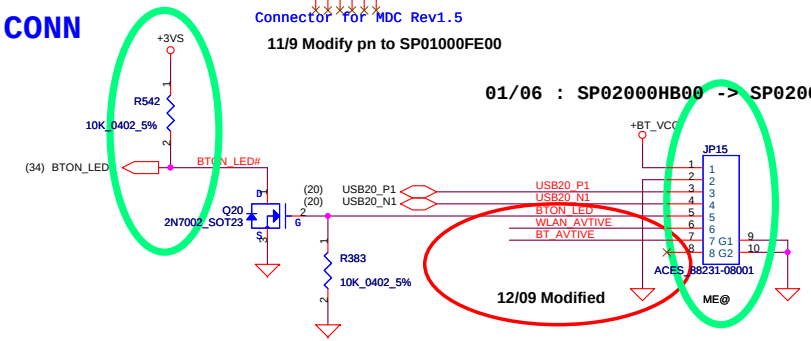
Connector for MDC Rev1.5

11/9 Modify pn to SP01000FE00

01/06 : SP02000HB00 -> SP02000HC00

BT MODULE CONN





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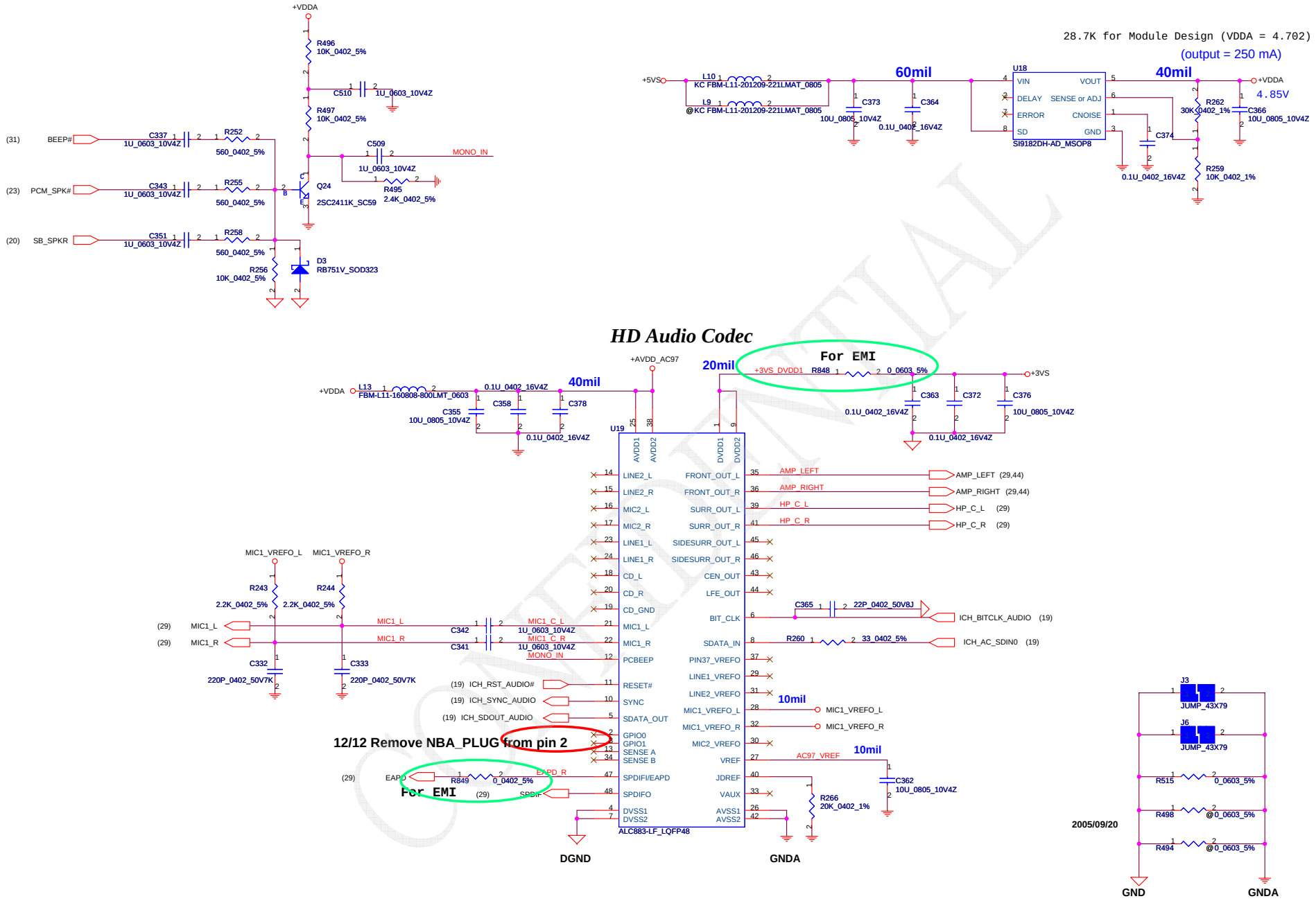

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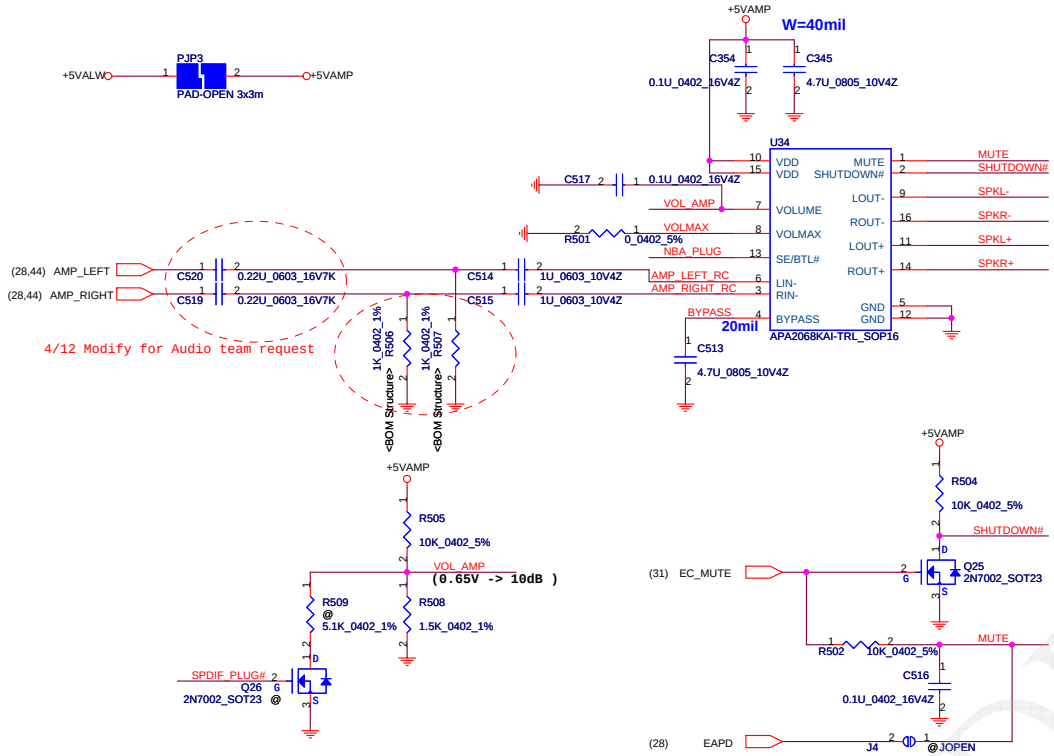
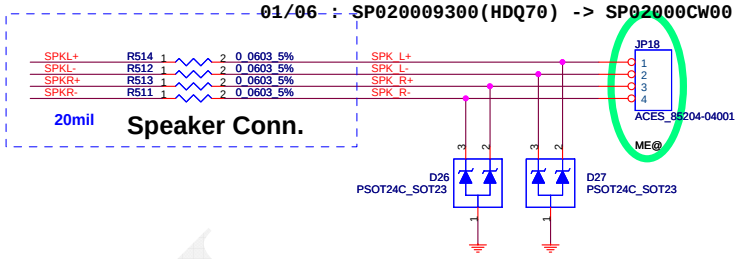
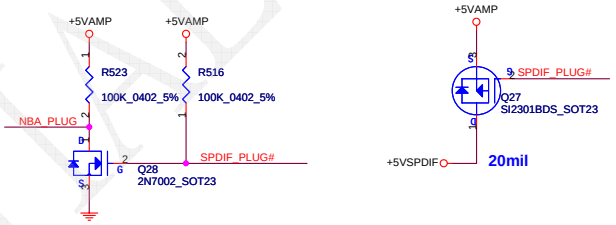




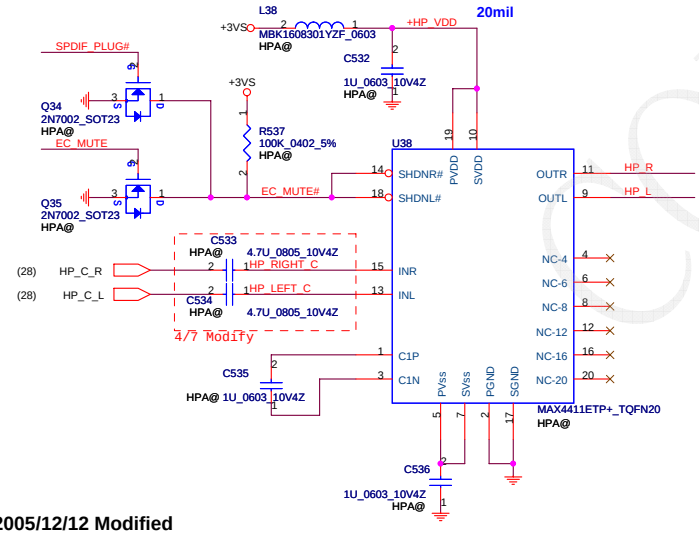


	SPDIF_PLUG#	NBA_PLUG
Un-Plug	H	L
HP_Plug_In	L	H
SPDIF_Plug_In	L	H

HEAD PHONE AMP

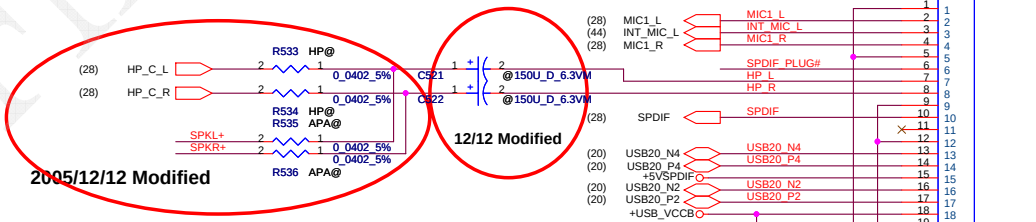
HPF Fc = 338Hz

R=1K, C=0.22U for HBQ60



2005/12/12 Modified

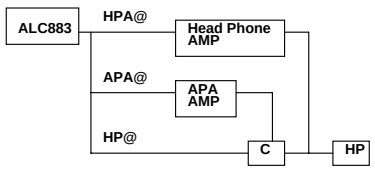
Audio Jack/USB Conn.



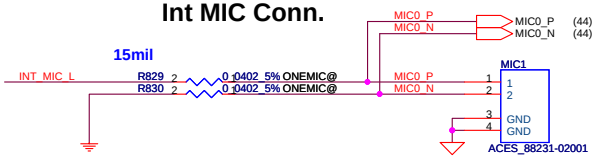
11/10 Modify pn to SP02000BJ00

2005/12/12 Modified

BOM Structure



Int MIC Conn.



PN : SP02000EZ00

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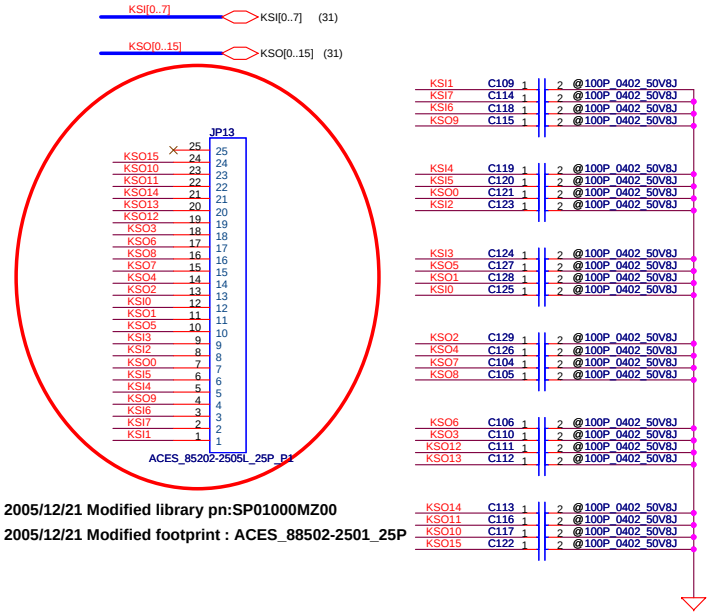
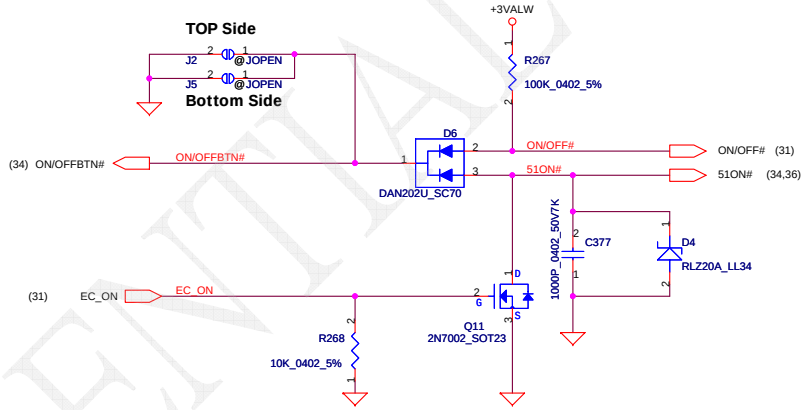
INT_KBD CONN.(TYPE "D" KB)

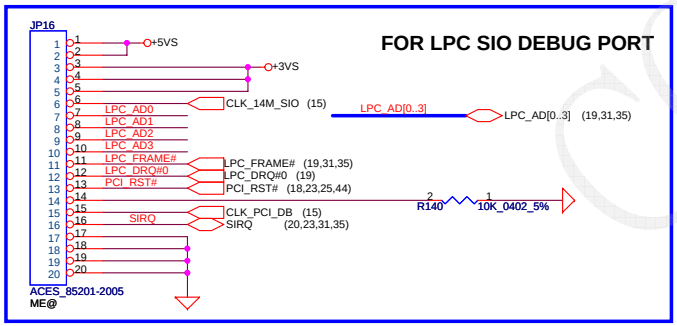


2005/12/21 Modified library pn:SP01000MZ00

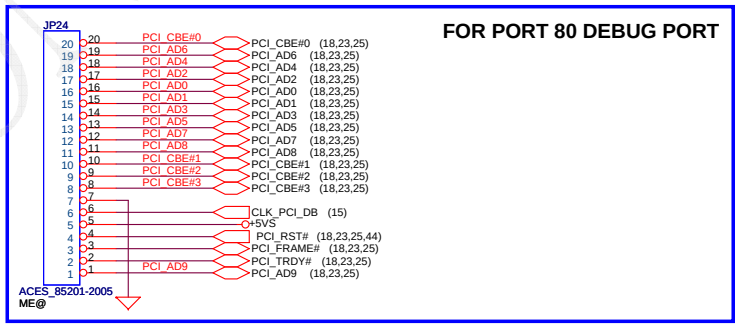
2005/12/21 Modified footprint : ACES_88502-2501_25P

Power BTN





Not lead free



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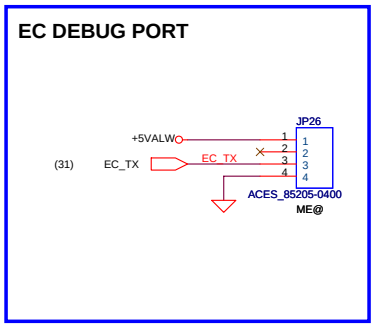

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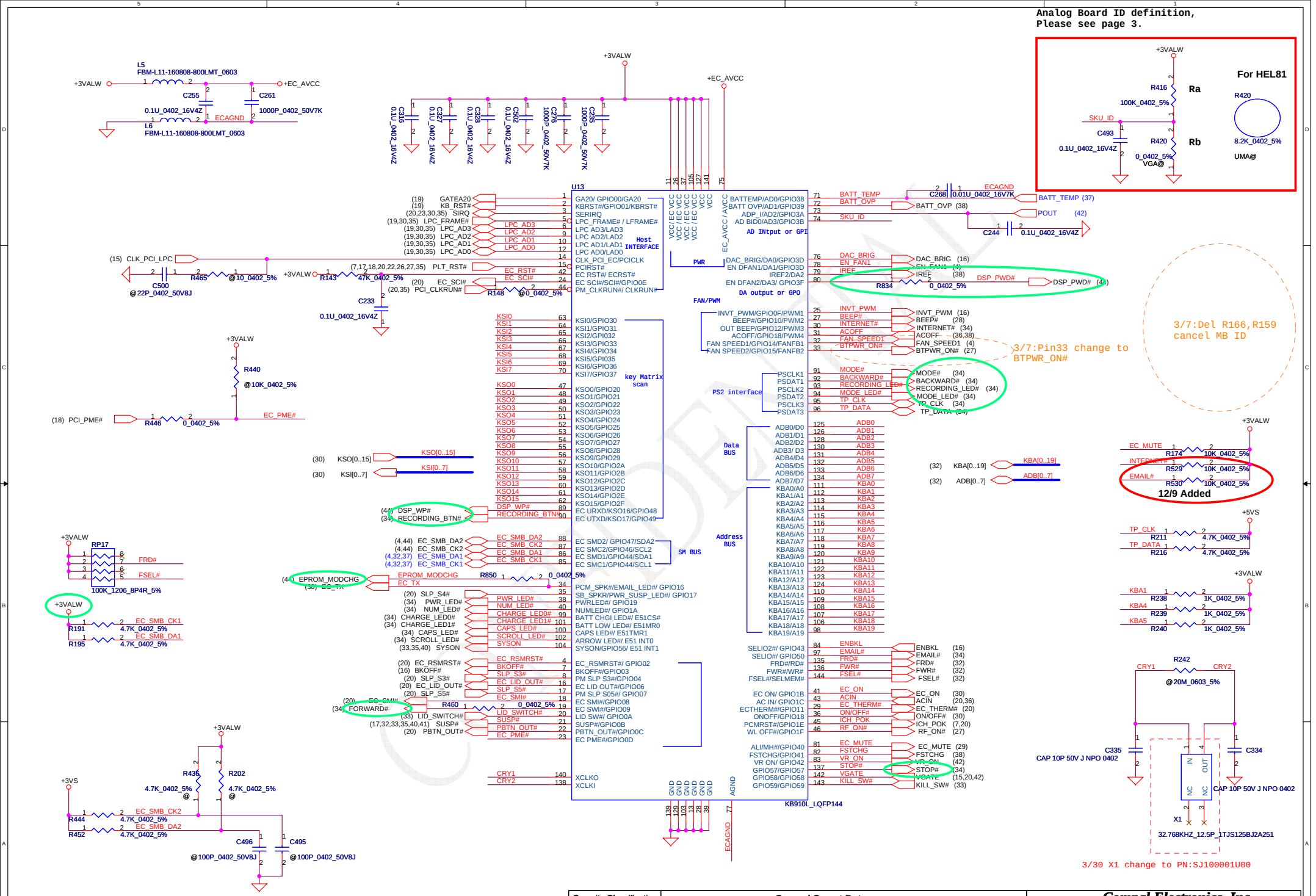
Analog Board ID definition,
Please see page 3.



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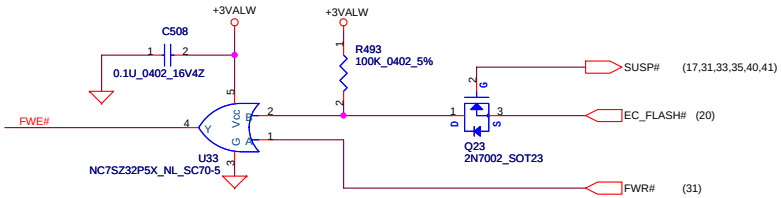
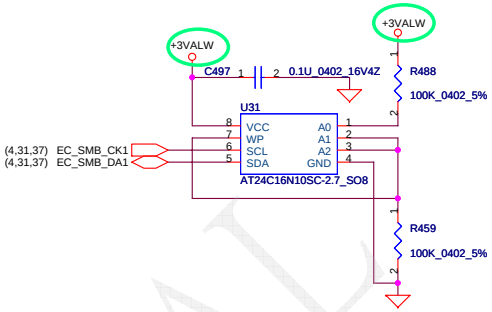
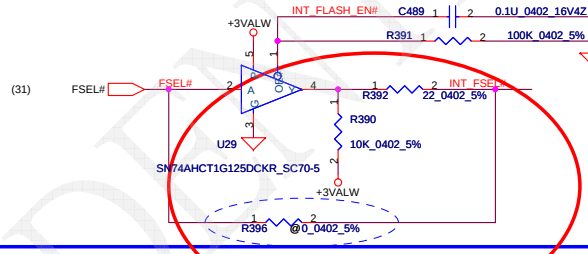




FOR DEBUG ONLY



12/9 Modified BOM Structure

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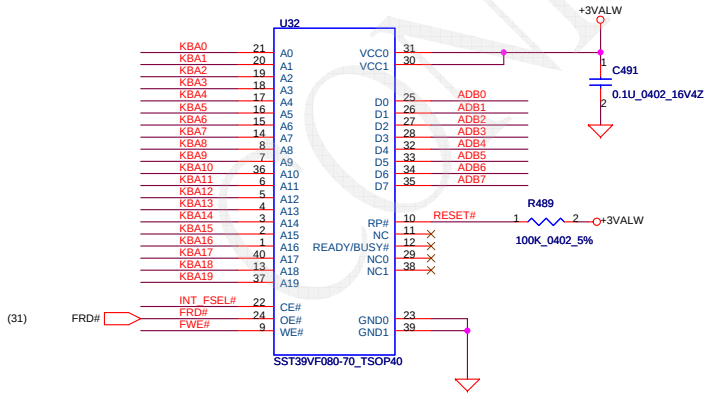
(31) KBA[0..19] — KBA[0..19]

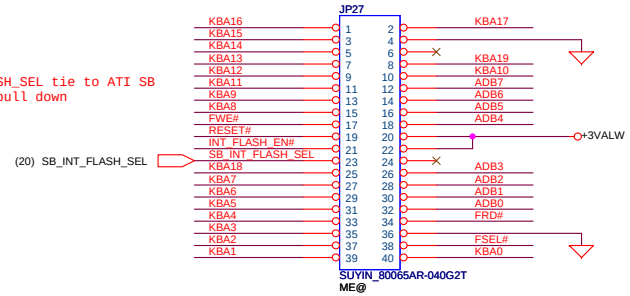
(31) ADB[0..7] — ADB[0..7]

1MB Flash ROM



1MB ROM Socket

SB_INT_FLASH_SEL tie to ATI SB GPIO1 and pull down



Not Lead Free

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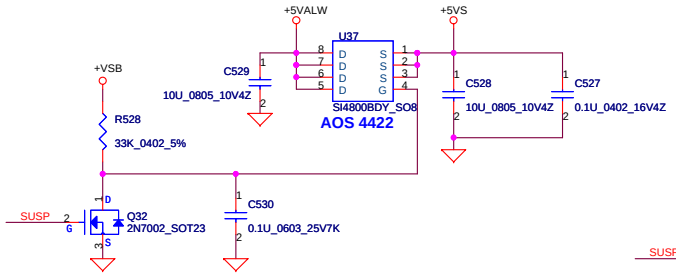
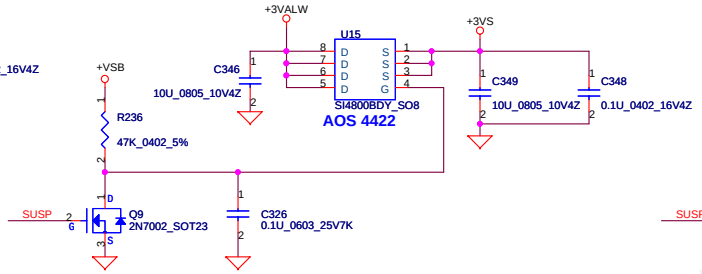
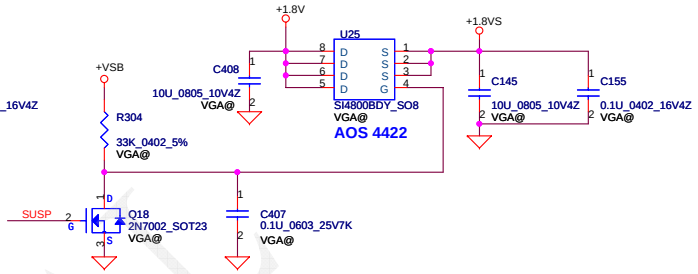
+5VALW to +5VS Transfer

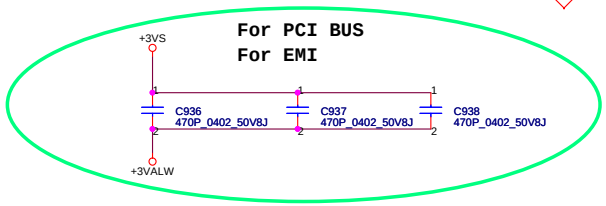


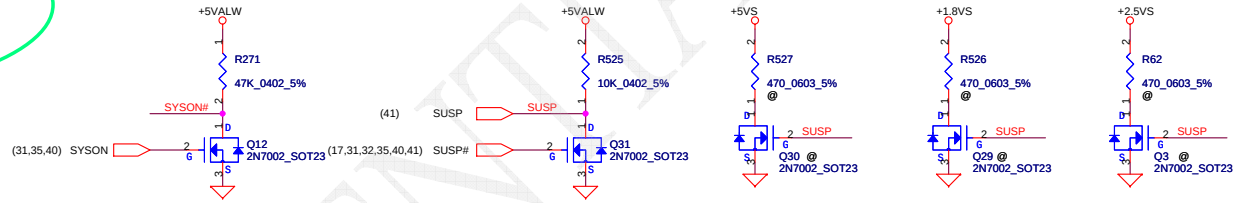
+3VALW to +3VS Transfer



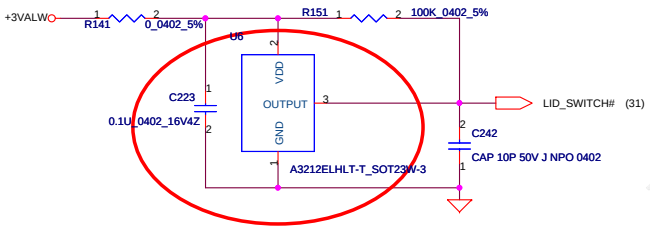
+1.8V to +1.8VS Transfer





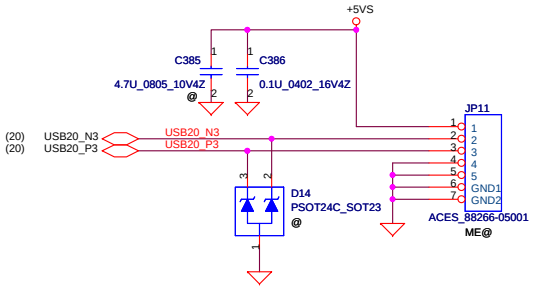


LID Switch

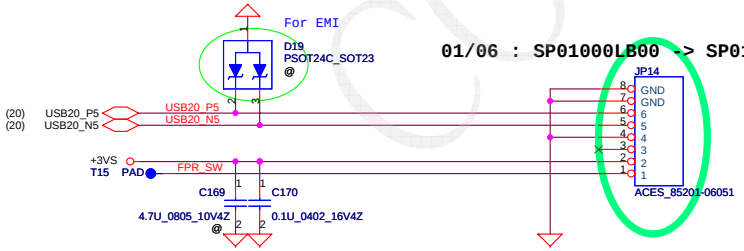


12/9 Change to SA032120010

CMOS Camera Conn

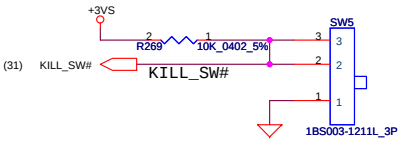


Finger Print board + MP3 Module CONN.



ACES

Kill Switch



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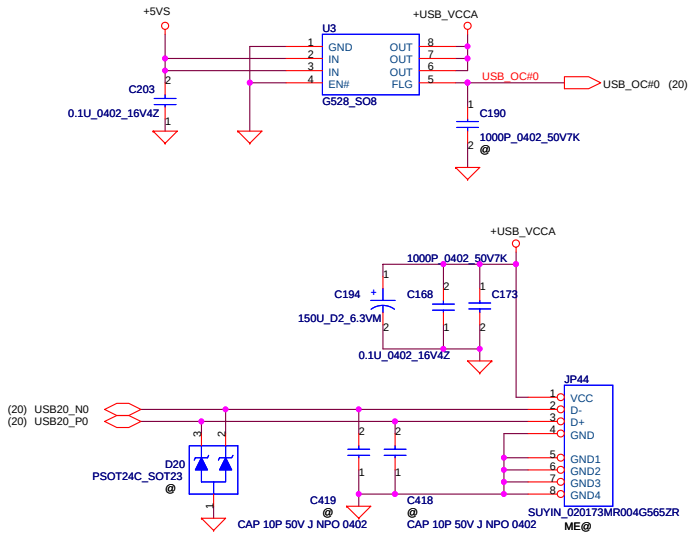
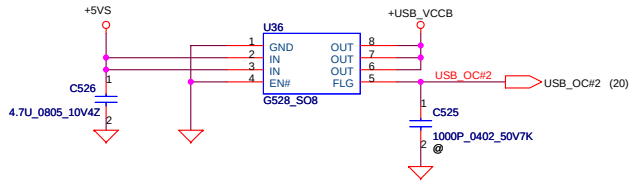
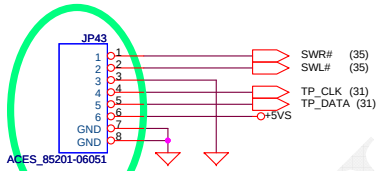
USB Port

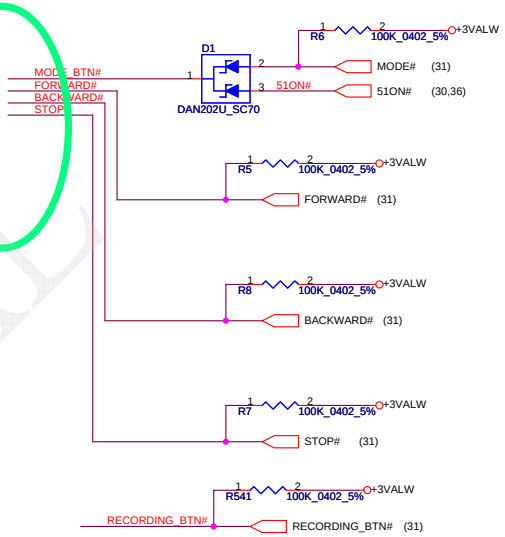


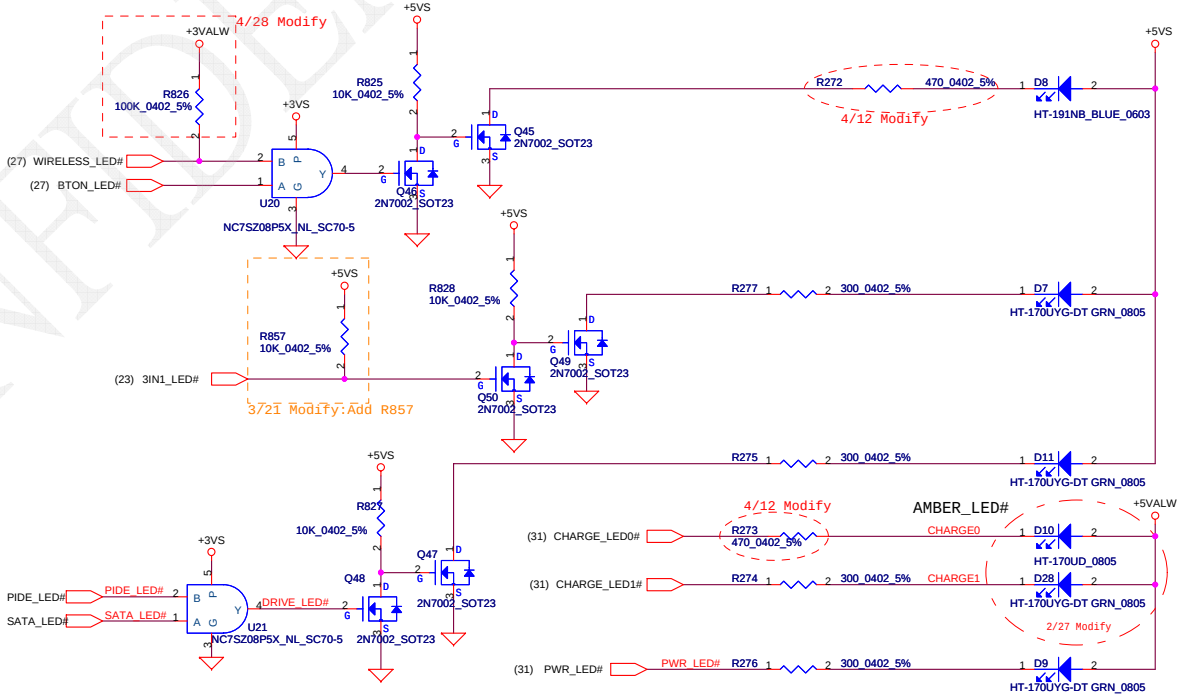


T/P Board

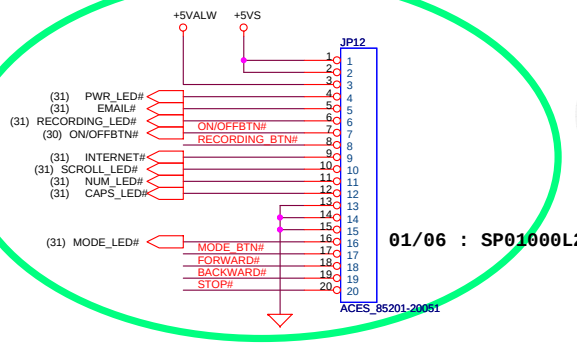


01/06 : SP01000LB00 -> SP01000B000





Switch Board CONN.



01/06 : SP01000L200 -> SP010008210

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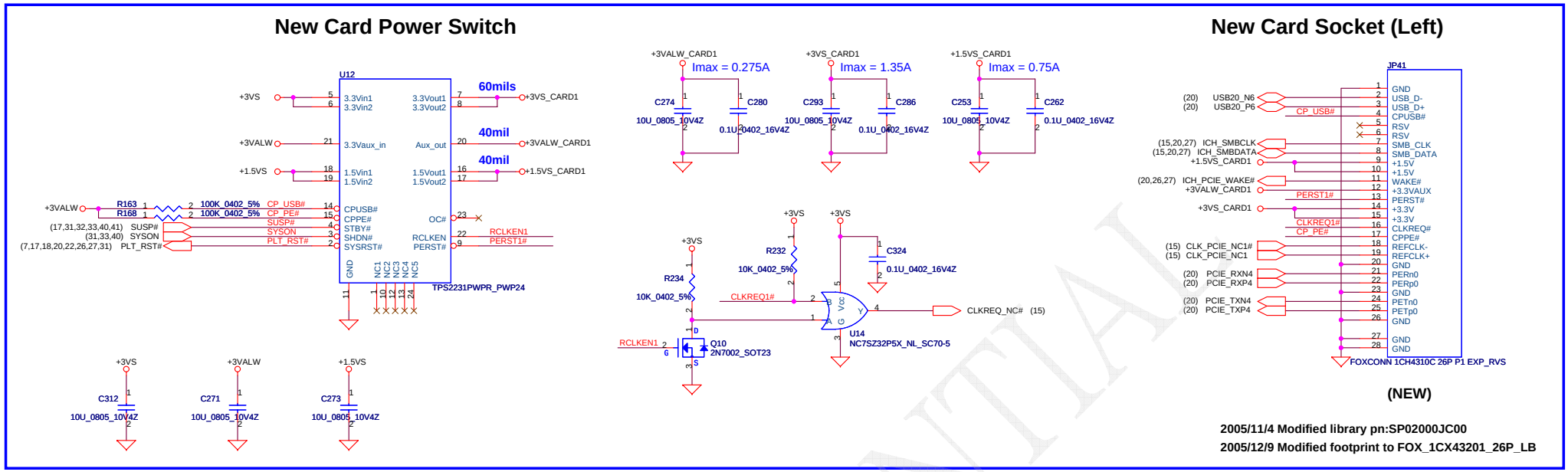

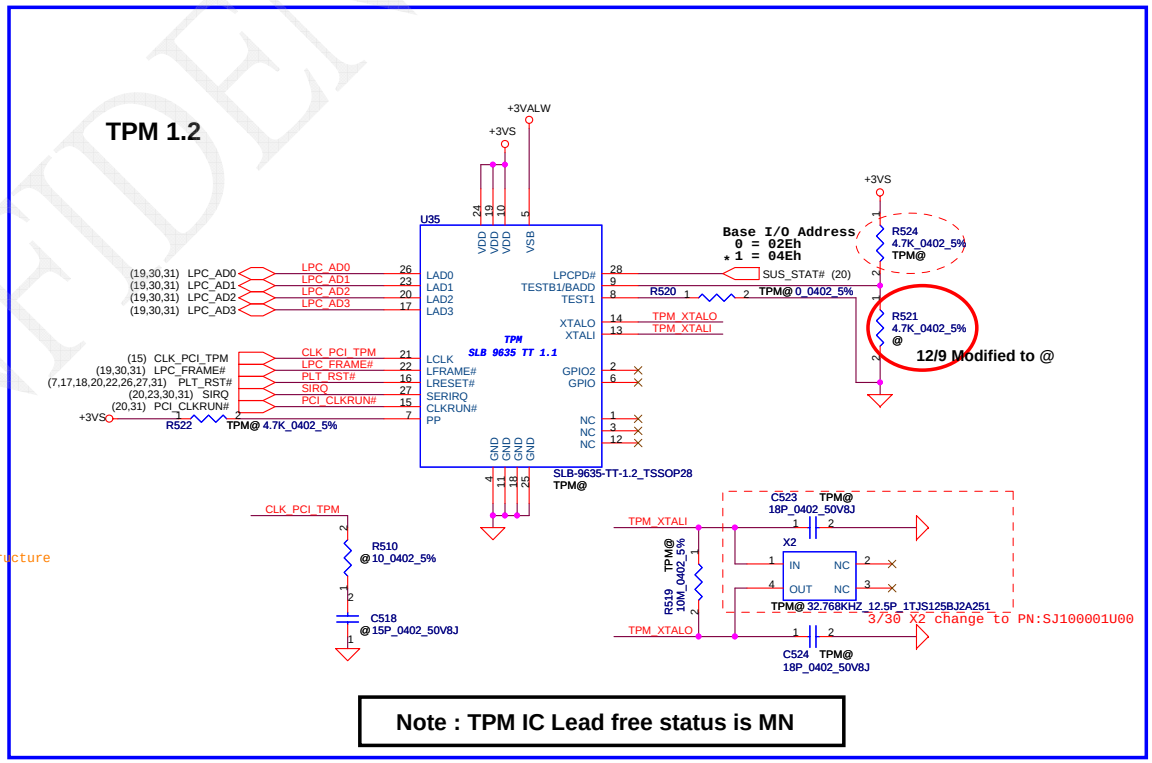

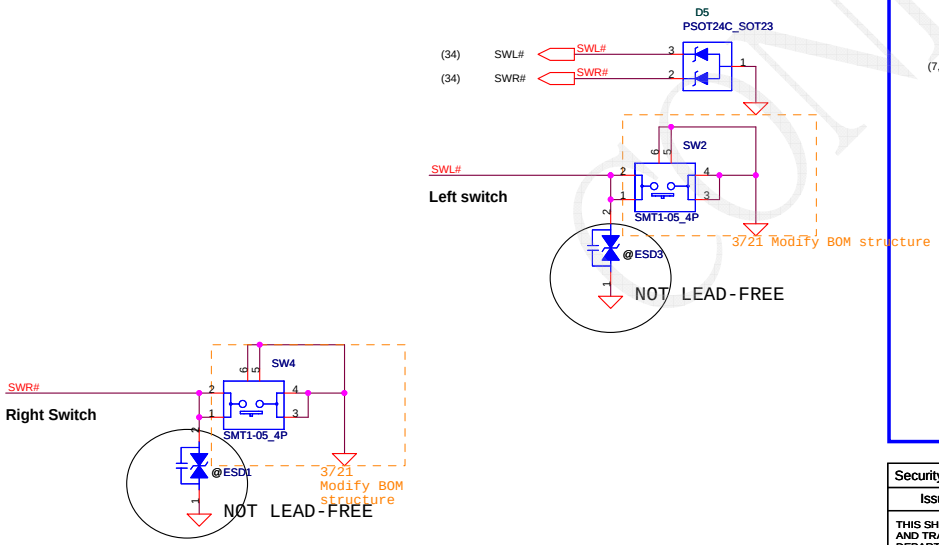

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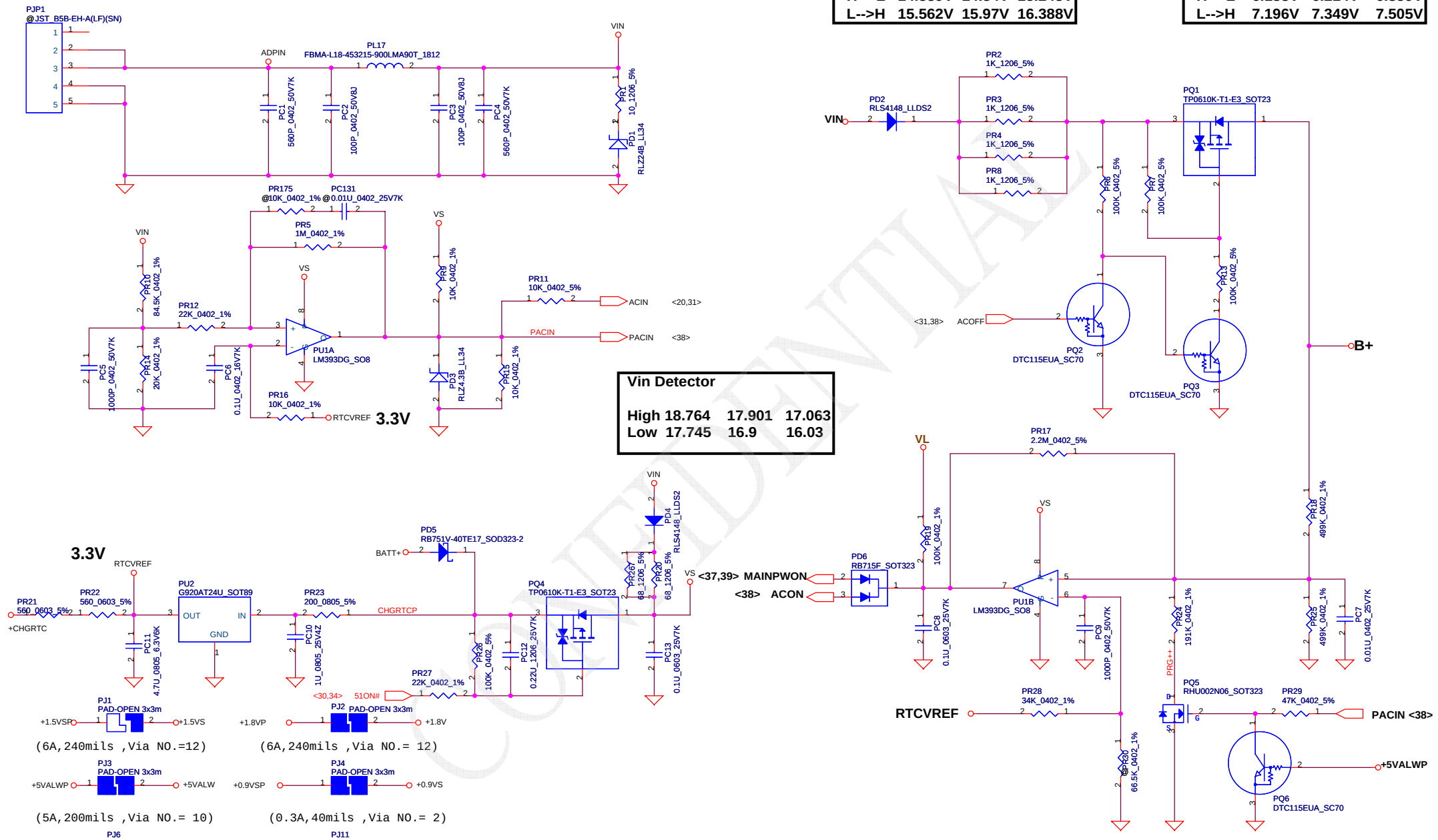
ACIN

Precharge detector	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



Vin Detector

High	18.764	17.901	17.063
Low	17.745	16.9	16.03

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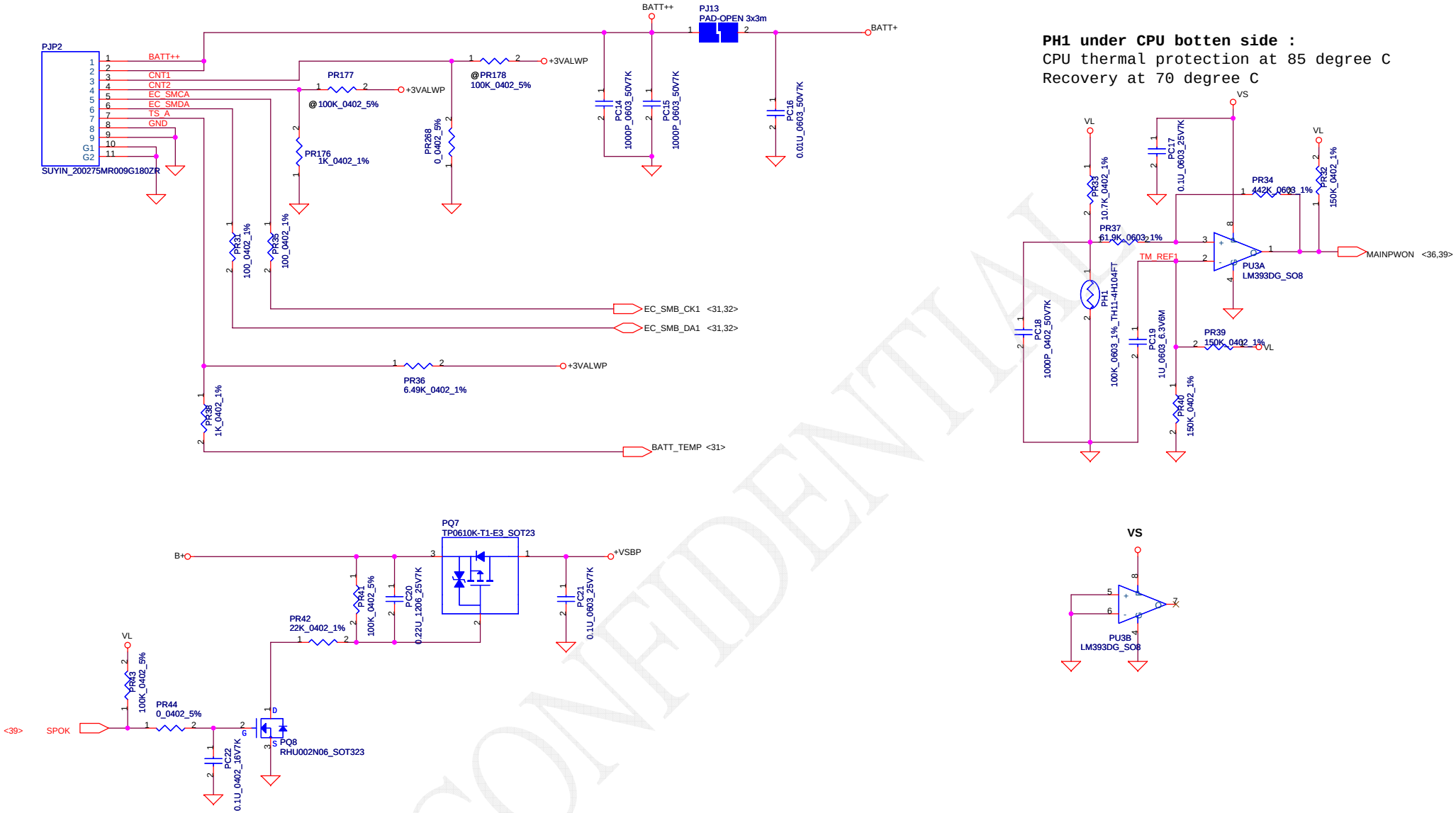

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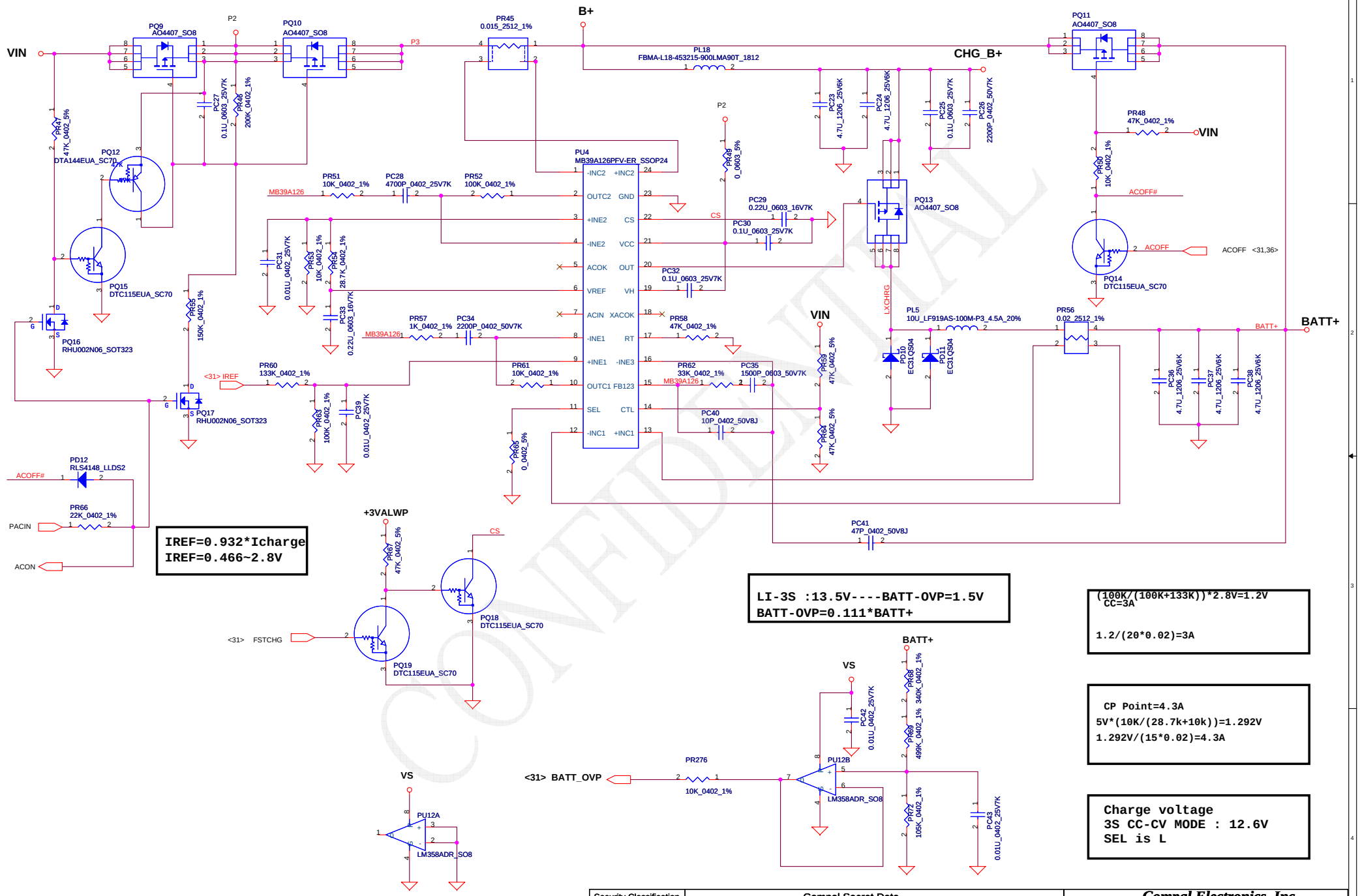
75W PR45=0.02_2512_1% PR54=23.7K_0402_1% Iadp=0~3.71A
90W PR45=0.15_2512_1% PR54=28.7K_0402_1% Iadp=0~4.3A

Fosc=14100/Rt=14100/47=300KHz

Charger



IREF=0.932*Icharge
IREF=0.466~2.8V

LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.111*BATT+

(100K/(100K+133K))*2.8V=1.2V
CC=3A

1.2/(20*0.02)=3A

CP Point=4.3A
5V*(10K/(28.7k+10k))=1.292V
1.292V/(15*0.02)=4.3A

Charge voltage
3S CC-CV MODE : 12.6V
SEL is L

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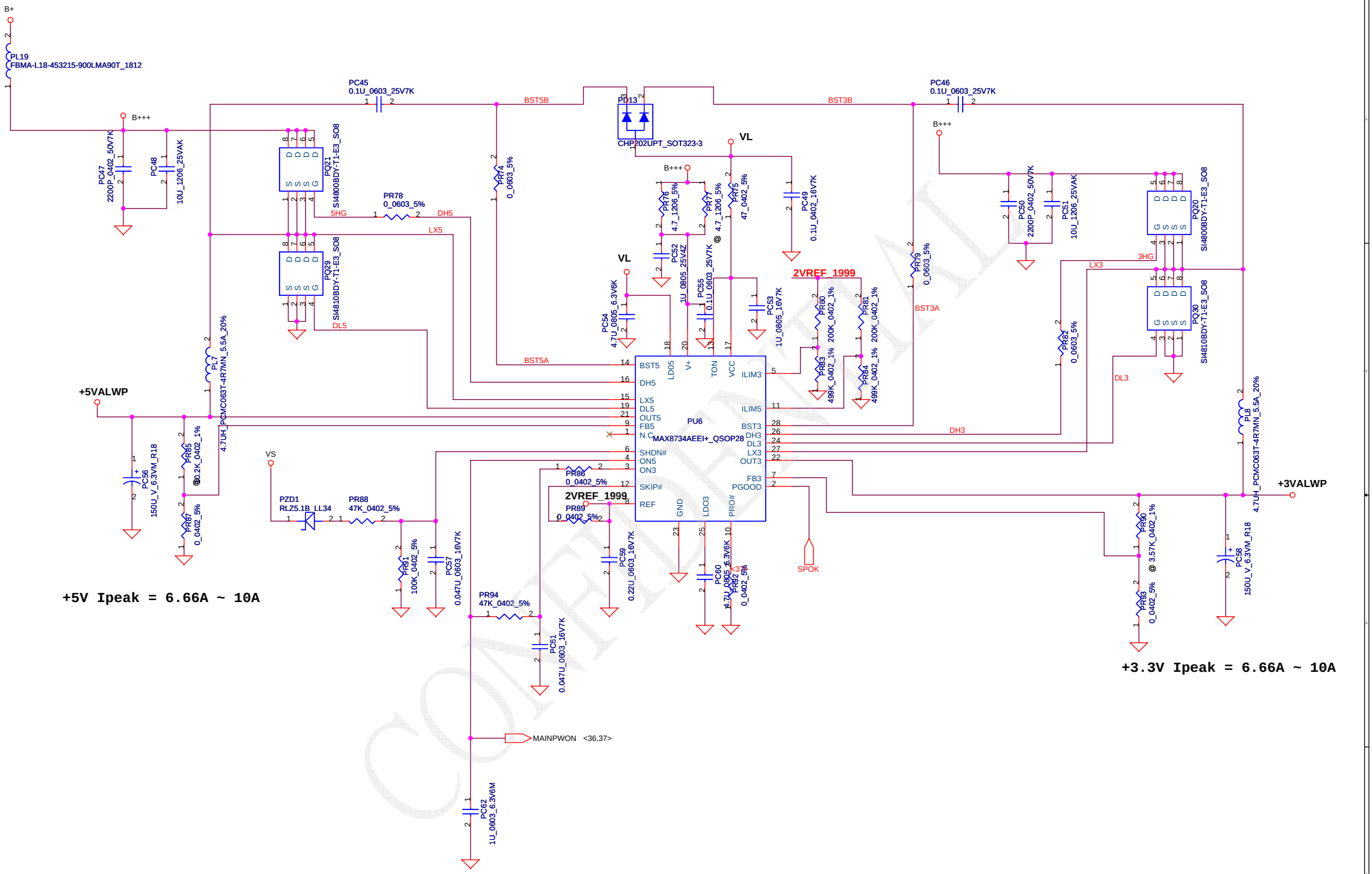

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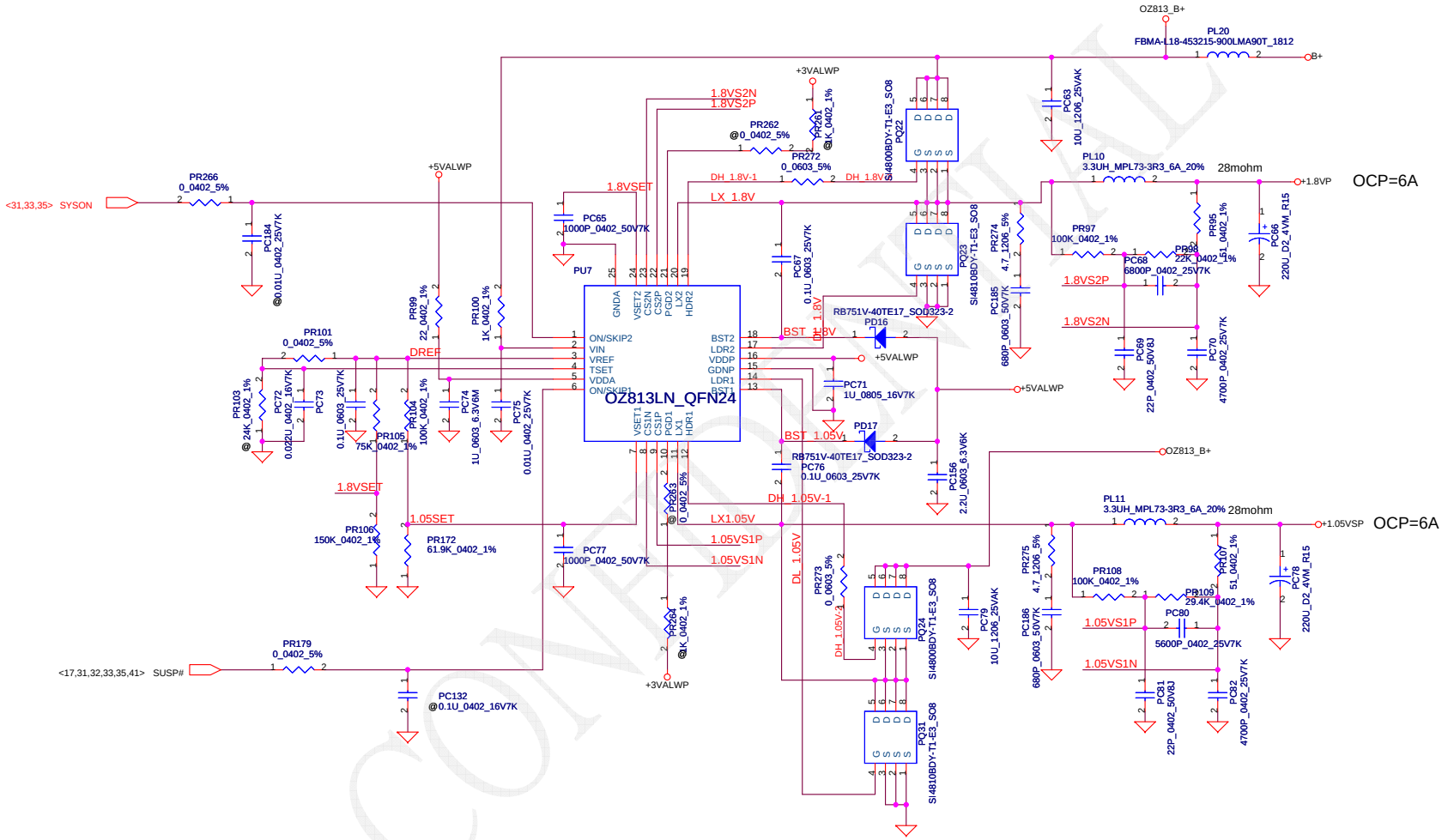

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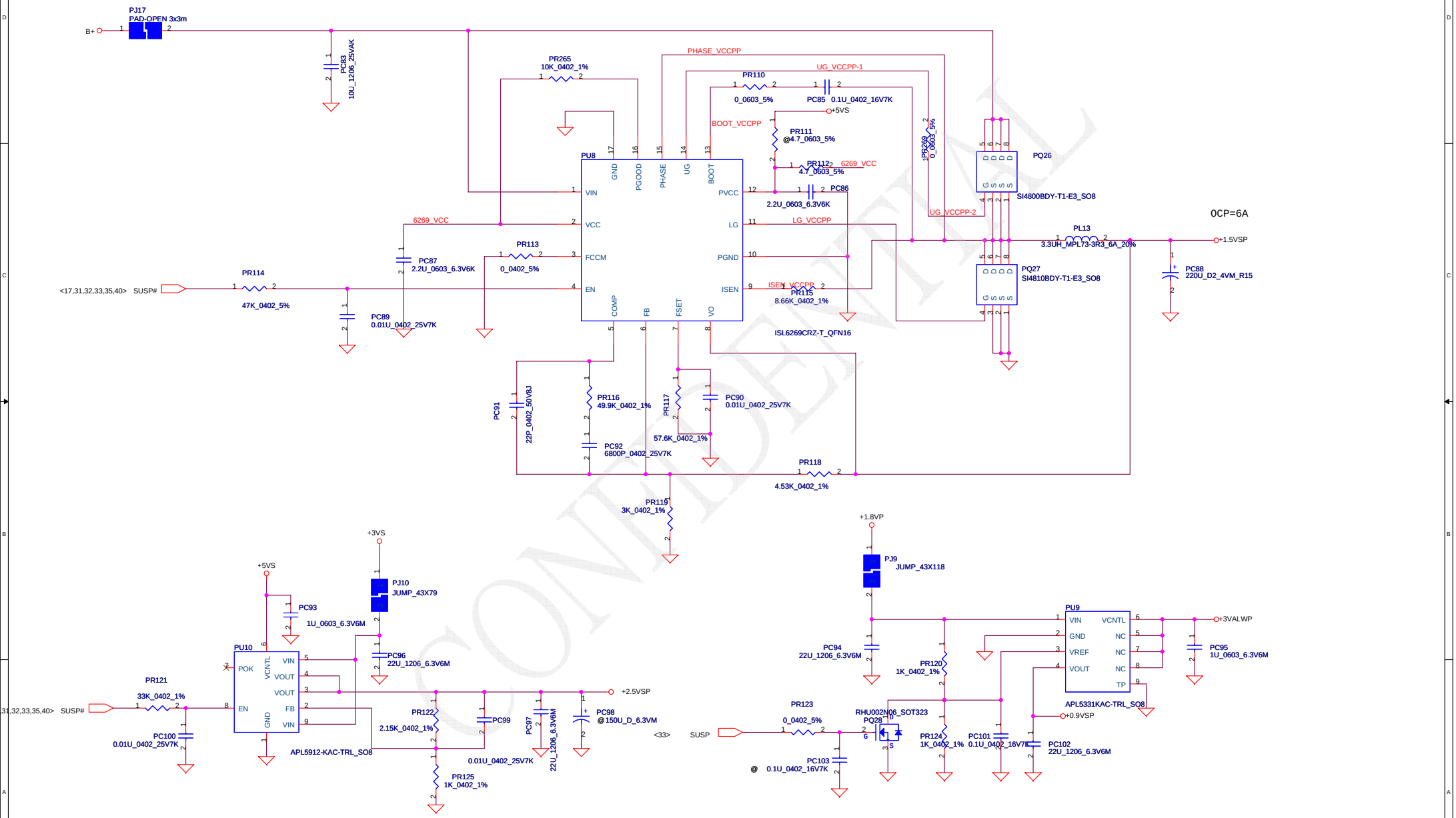

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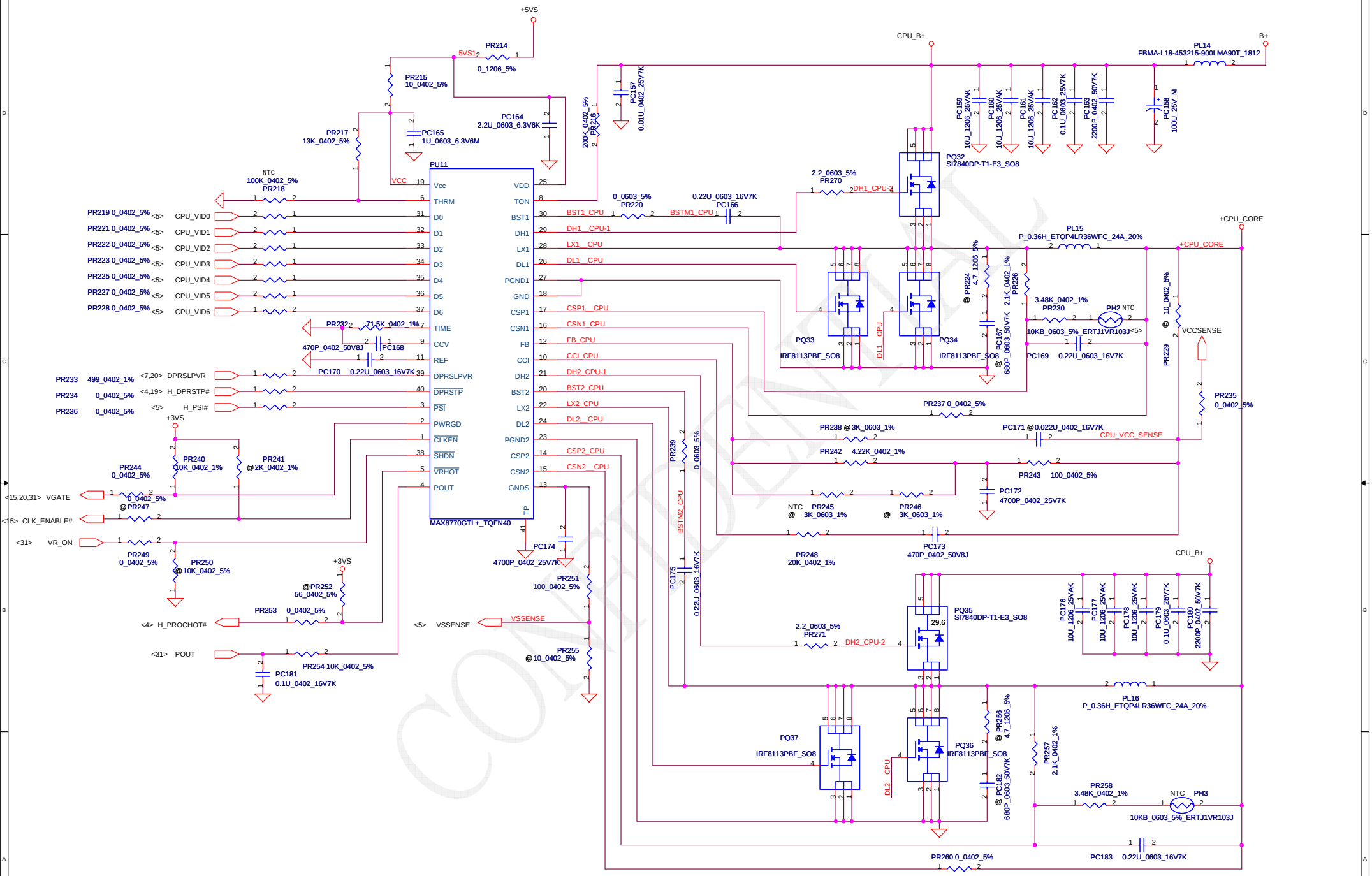

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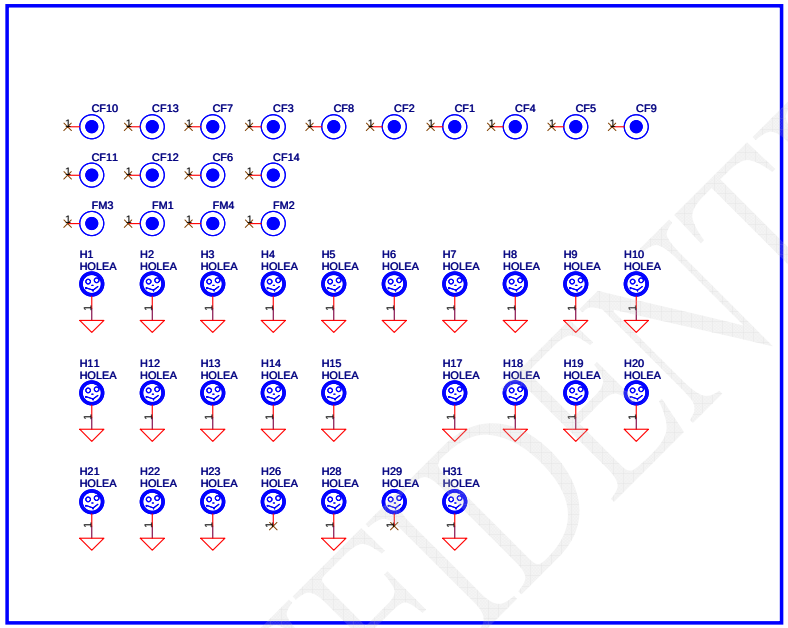


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01/19 : Modify
H8-------------->H_S315D118
H17.H22.H23----->H_C315D146
H10------------->H_S315D146
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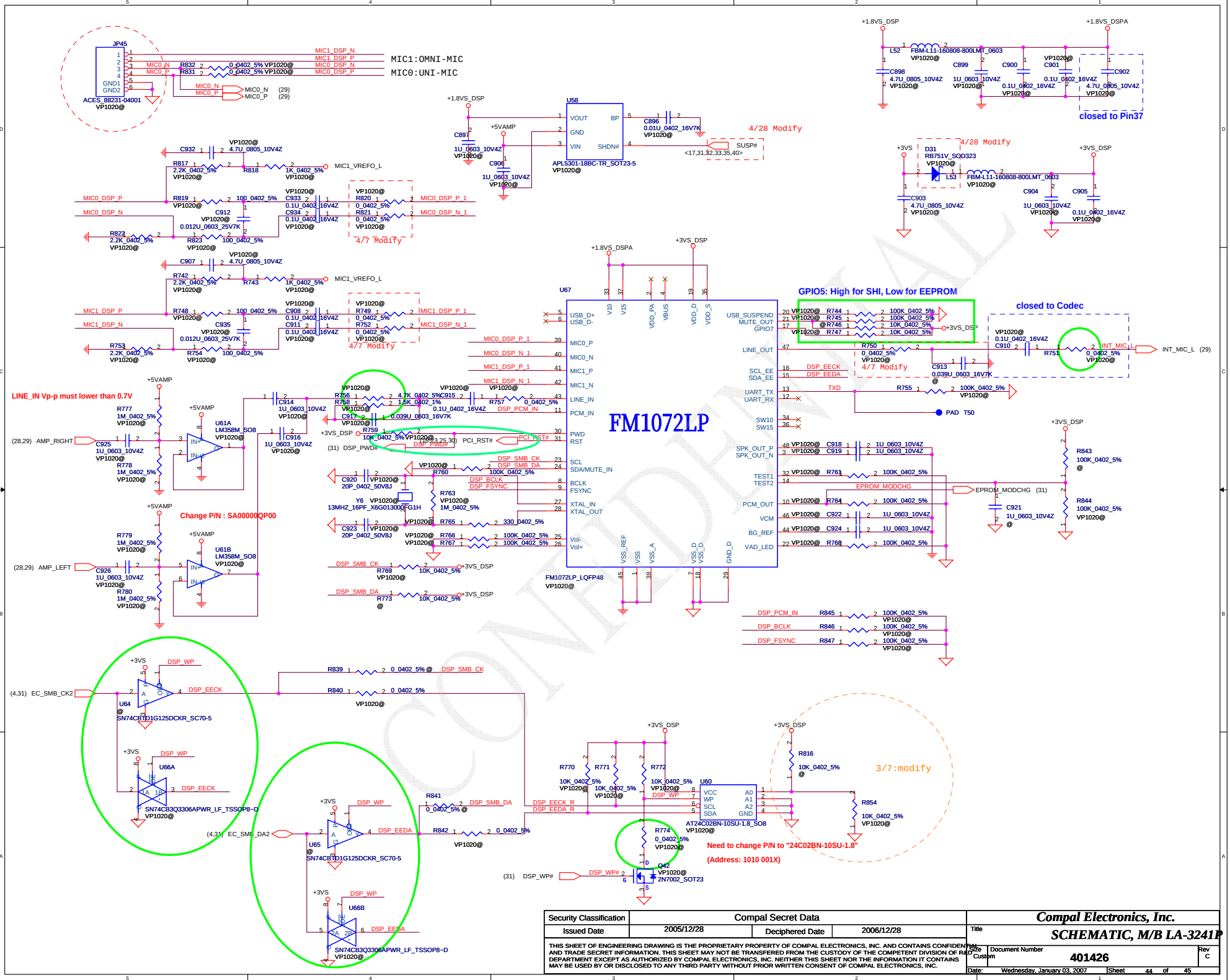

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DVT

page	Reason for change	Modify list
42	Vss_ sense feedback	PC174 change 1000P to 4700p
42	Vcc_ sense resistance	PR235 change 100 ohm to 0 ohm
42	load line	PR242 change 3.65K ohm to 4.22K
42	Vcc_ sense resistance (H.W. had pull-high)	Delete PR229
36	Prevent PACIN Low	PR11 change 0 ohm to 10K ohm
42	Heavy load unstable	change PQ33,PQ34,PQ36,PQ37 from AO4410 to IRF8113

PVT

page	Reason for change	Modify list
36	Battery and Adapter in sequence	PD4 Pin2 voltage change VS to VIN
38	Battery and Adapter in sequence	Add PR276 between PU12 pin 7 and BATT_OVP.
42	For EMI	Change High side gate resister 0ohm to 2.2ohm
42	For EMI	Change boost resister 2.2ohm to 0ohm
38	Delete sunbber for EMI	Delete PR256_4.7ohm,PR224_4.7ohm, PC182_680pf,PC167_680pf
38	Reduce delay time for EC	Delete PR175_10K, PC131_0.01uF

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