

Model NAME : VAUB0
PCB NO : LA-9941P
DAA0006W000

BOM P/N : TBD

Dell/Compal Confidential

Schematic Document

Phantom (Shark Bay)

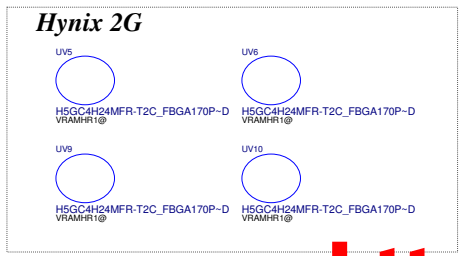
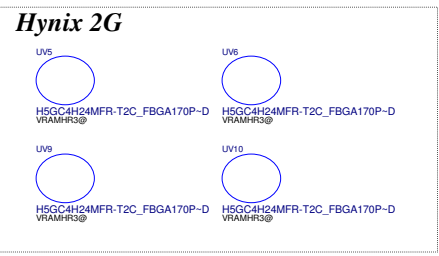
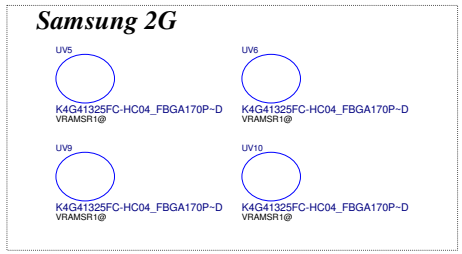
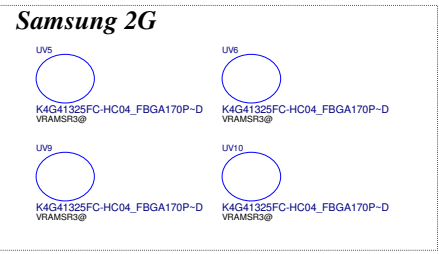
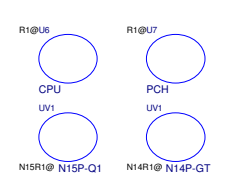
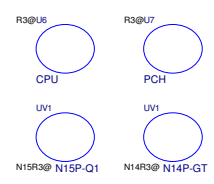
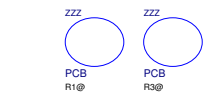
Haswell (BGA) + Lynx Point

DISCRETE VGA N14P (optimus) --- Testarossa
DISCRETE VGA N15P (optimus) --- Testarossa-P

2013-01-02

Rev: 0.1 (X00)

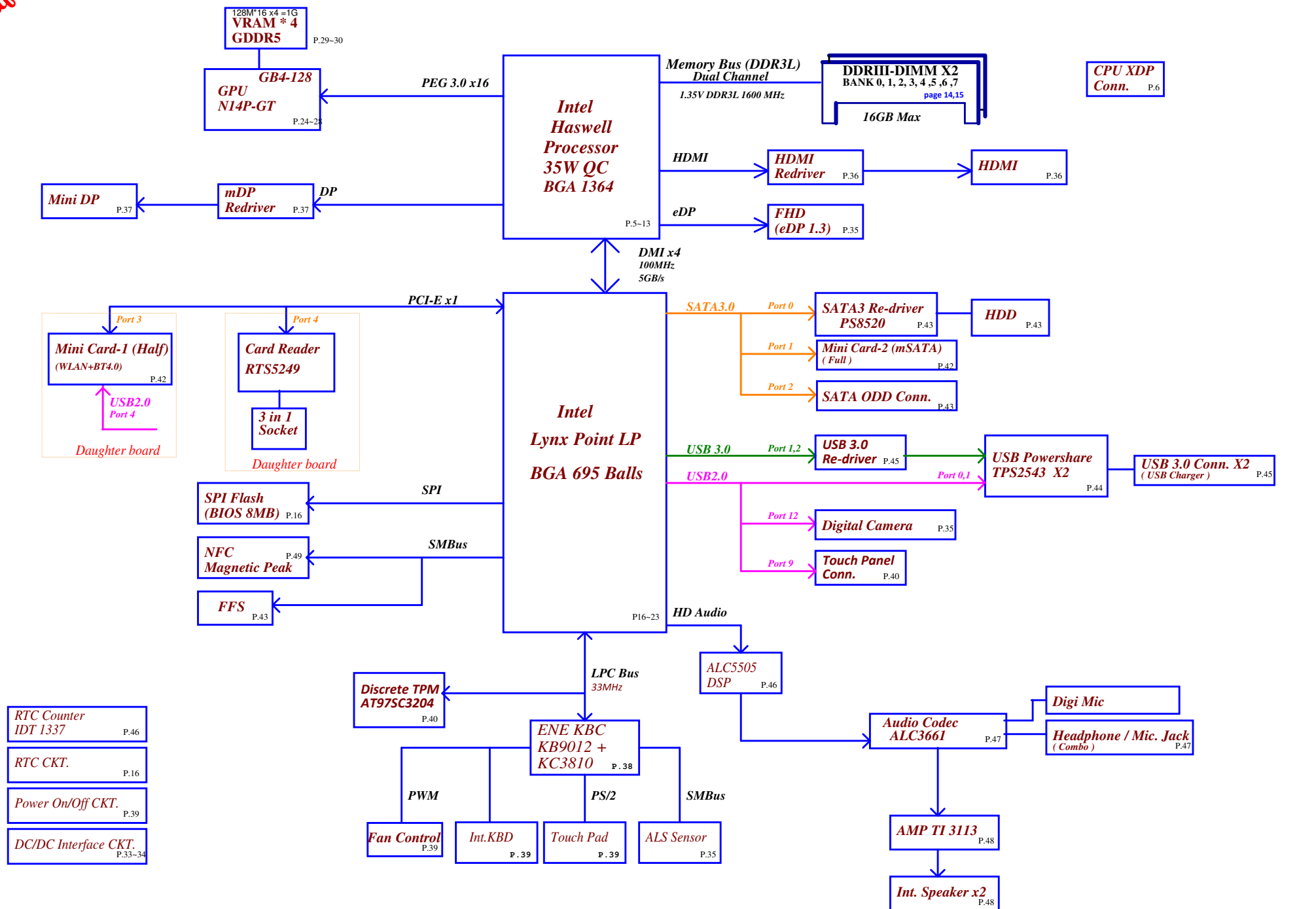
@ : Nopop Component
CONN@ : Connector Component
TPM@ : TPM function
DSP@ : DSP function
N14@ : DGPU N14P-GT
N15@ : DGPU N15P-Q1



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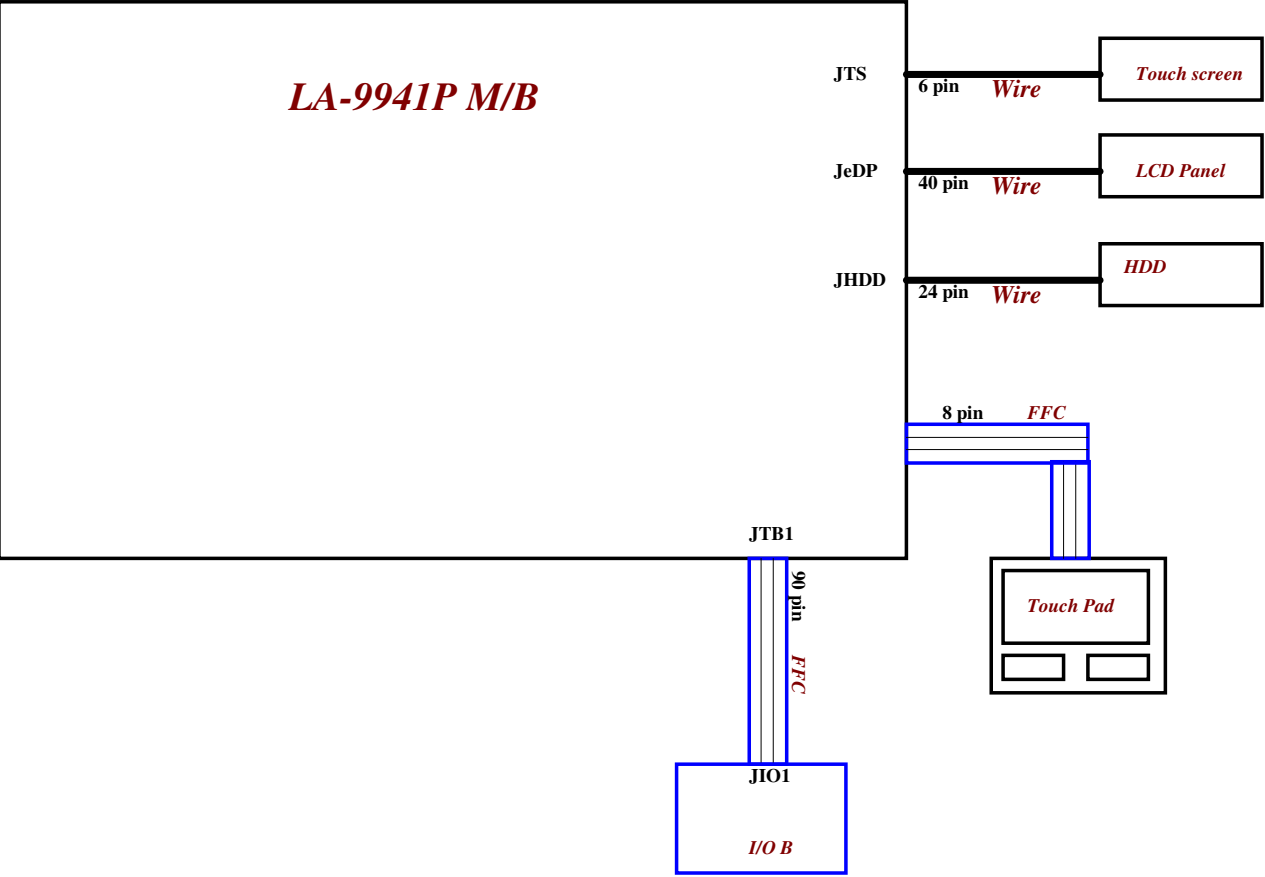
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Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb		Board ID	PCB Revision	
0	0		0	DIS 0.1	
1	12K +/- 1%		1	DIS 0.2	
2	15K +/- 1%		2	DIS 0.3	
3	20K +/- 1%		3	DIS 0.4	
4	27K +/- 1%		4	DIS 0.5	
5	33K +/- 1%		5	DIS 1.0	
6	43K +/- 1%		6	DIS-P 0.2	
7	56K +/- 1%		7	DIS-P 0.3	
8	75K +/- 1%		8	DIS-P 0.4	
9	100K +/- 1%		9	DIS-P 1.0	
10	130K +/- 1%		10	UMA 0.2	
11	160K +/- 1%		11	UMA 0.3	
12	200K +/- 1%		12	UMA 0.4	
13	240K +/- 1%		13	UMA 1.0	
14	270K +/- 1%		14		
15	330K +/- 1%		15		
16	430K +/- 1%		16		
17	560K +/- 1%		17		
18	750K +/- 1%		18		
19	NC		19		

PCI EXPRESS	DESTINATION
Lane 1	None
Lane 2	None
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

SATA	DESTINATION
SATA0	HDD
SATA1	SSD
SATA2	None
SATA3	None
SATA4	None
SATA5	None

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

PCH	USB PORT#	DESTINATION
	0	USB Conn 1 (Power share)
	1	USB Conn 3 (Power share)
	2	USB Conn 2 (Power share)
	3	USB Conn 4 (Power share)
	4	JMINI1 (WLAN)
	5	None
	6	None
	7	None
	8	None
	9	Touch screen
	10	None
	11	None
	12	CAMERA
	13	None

USB3	DESTINATION
1	USB Conn 1 (Power share)
2	USB Conn 3 (Power share)
3	USB Conn 2 (Power share)
4	USB Conn 4 (Power share)

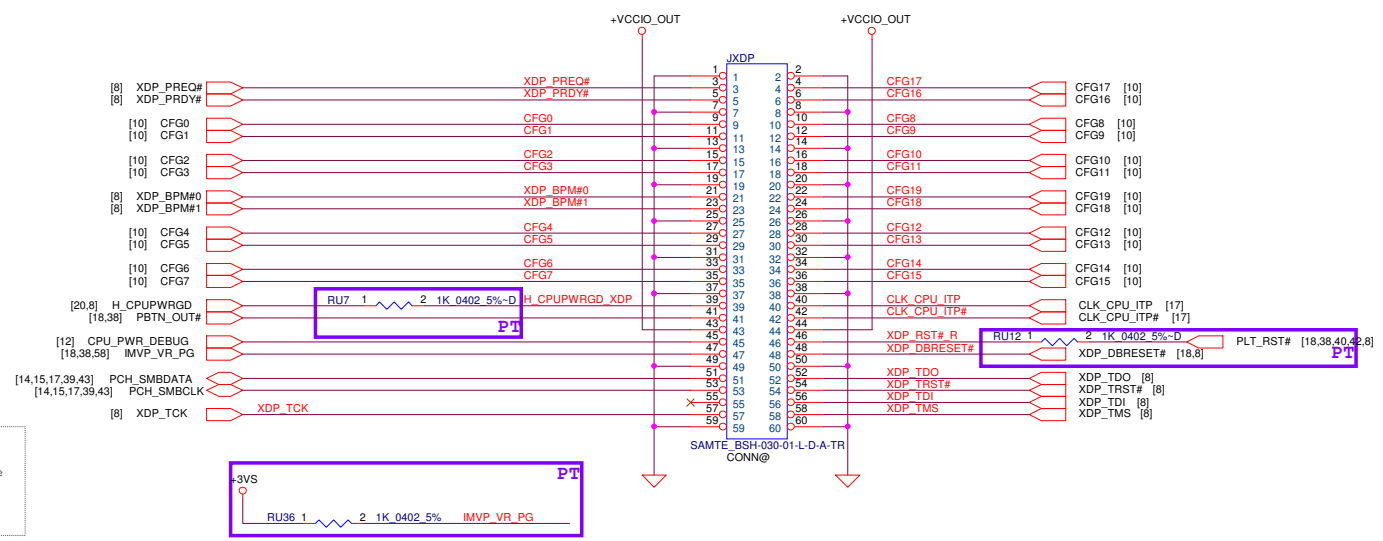
CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	CLK_PCI_TPM
	CLKOUT_PCIE1	None	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :

 : means Digital Ground
 : means Analog Ground

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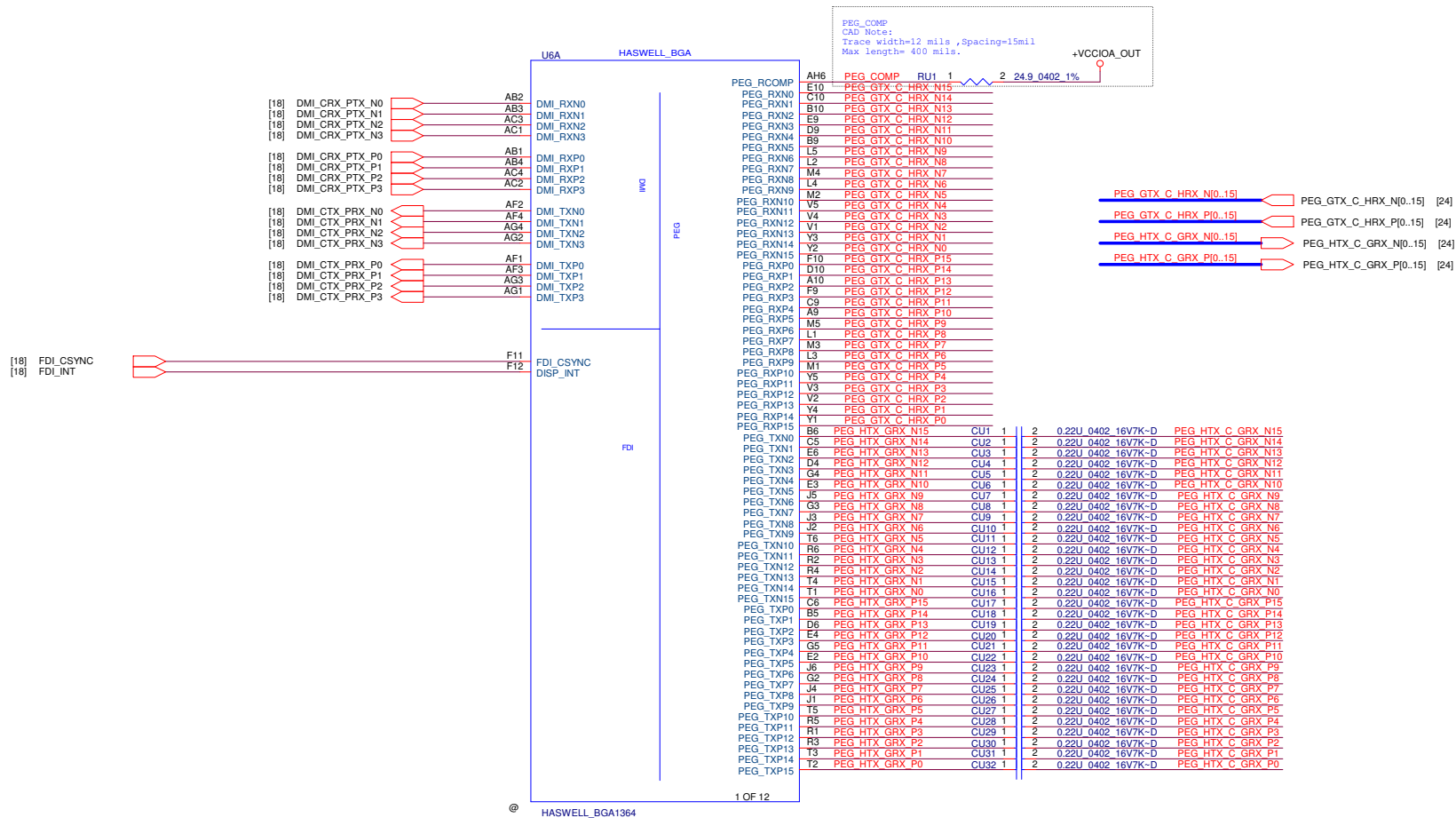
XDP CONN



The resistor for HOOK2 should be placed such that the stub is very small on CFG0 net

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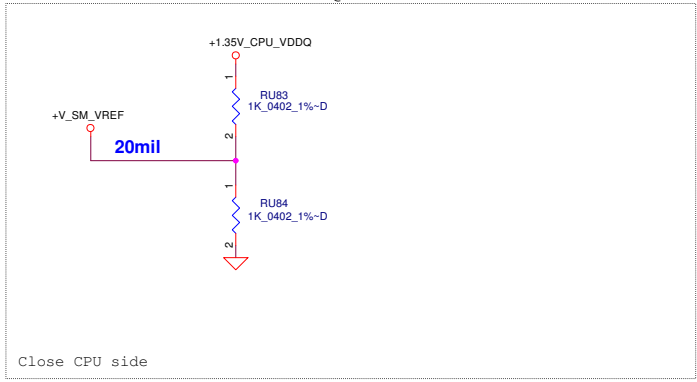
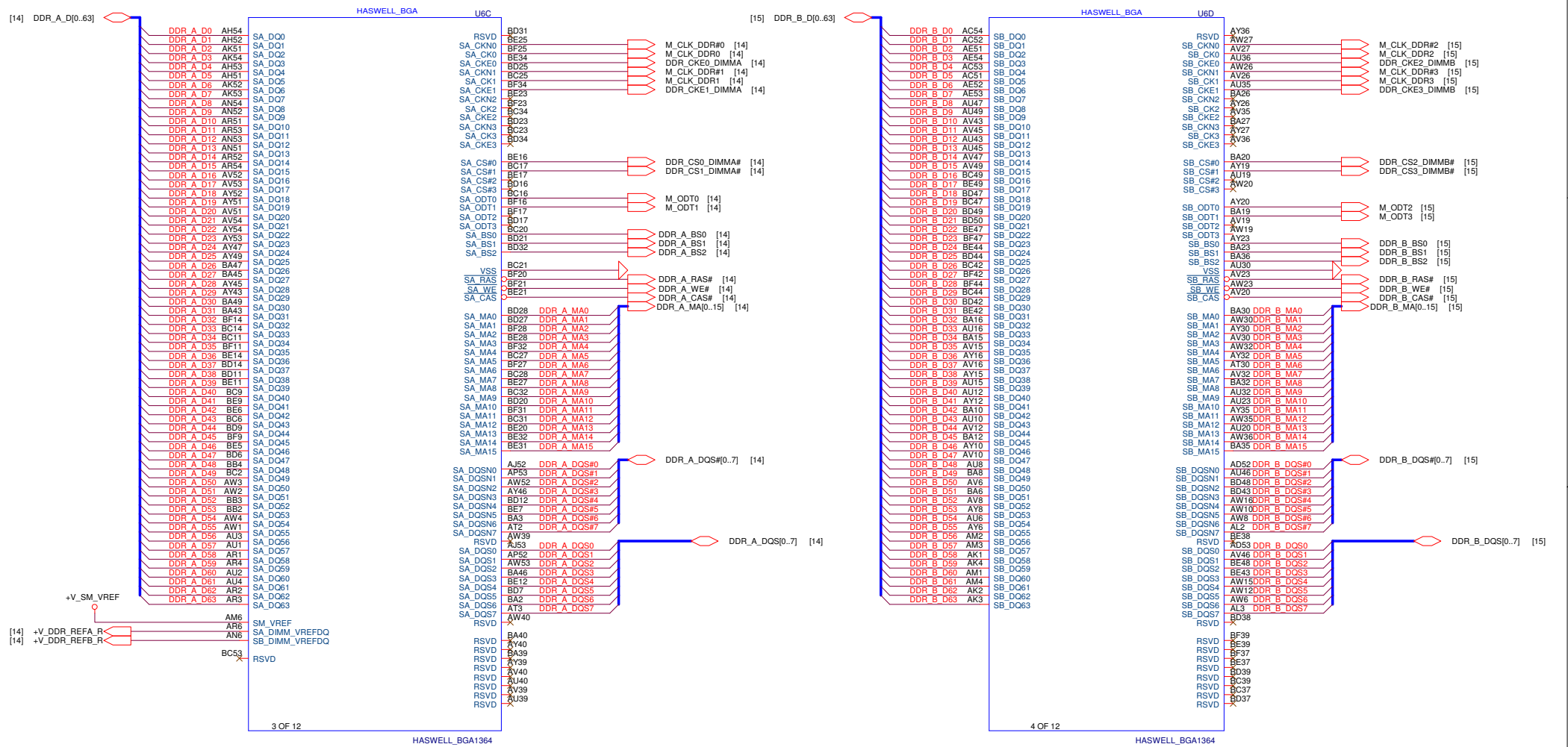
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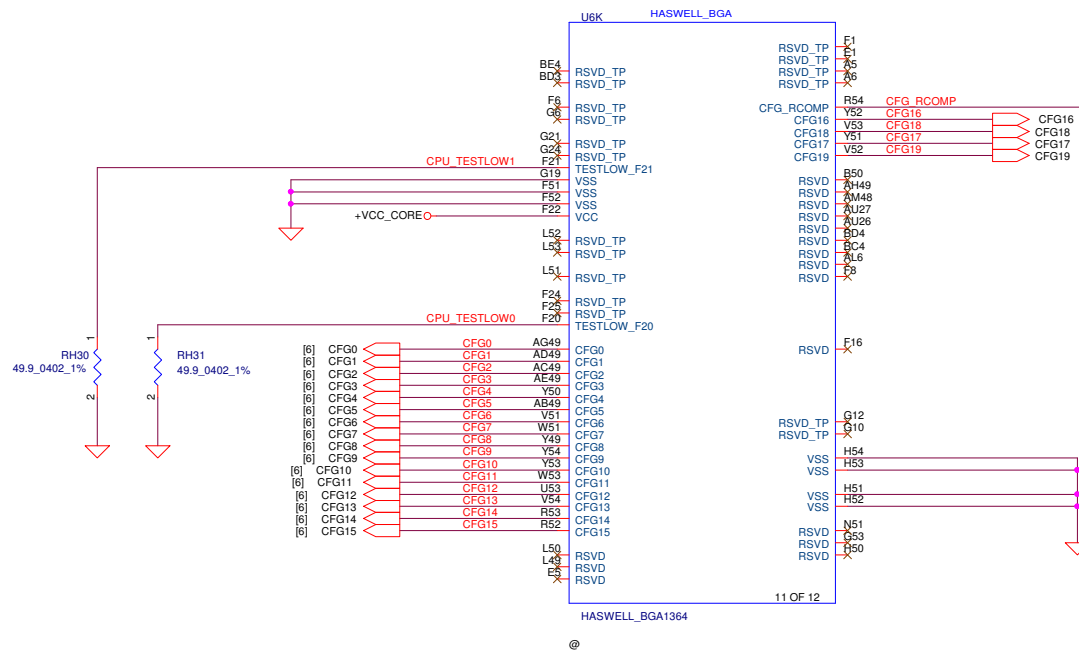
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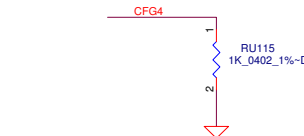
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Date: Tuesday, September 03, 2013				Sheet 9	of 62

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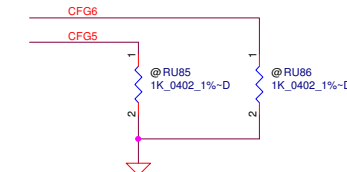
CFG Straps for Processor



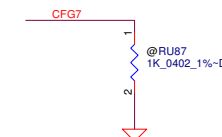
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



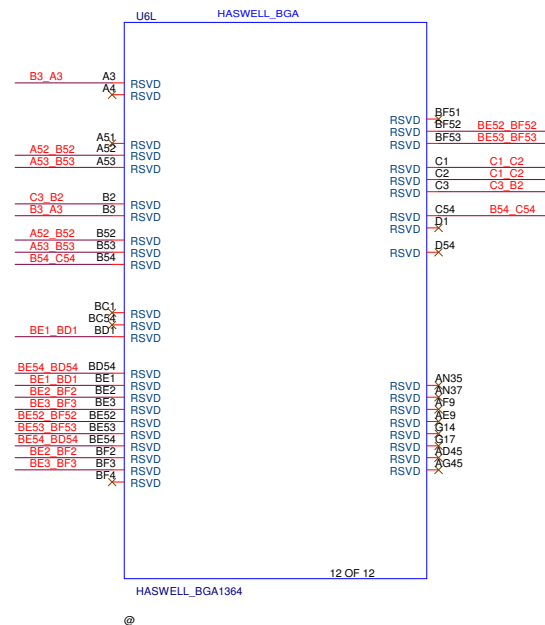
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



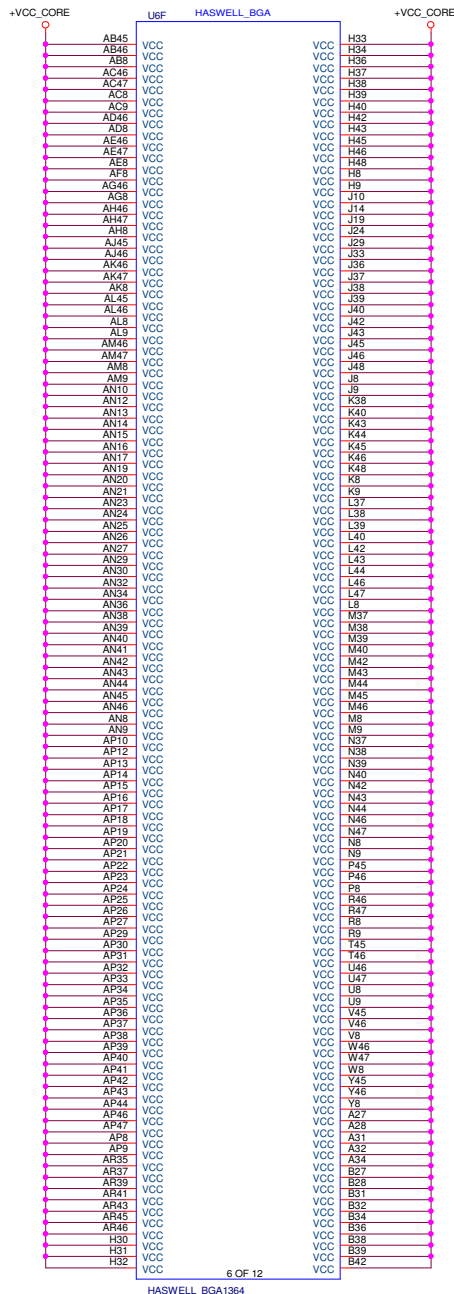
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



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55A



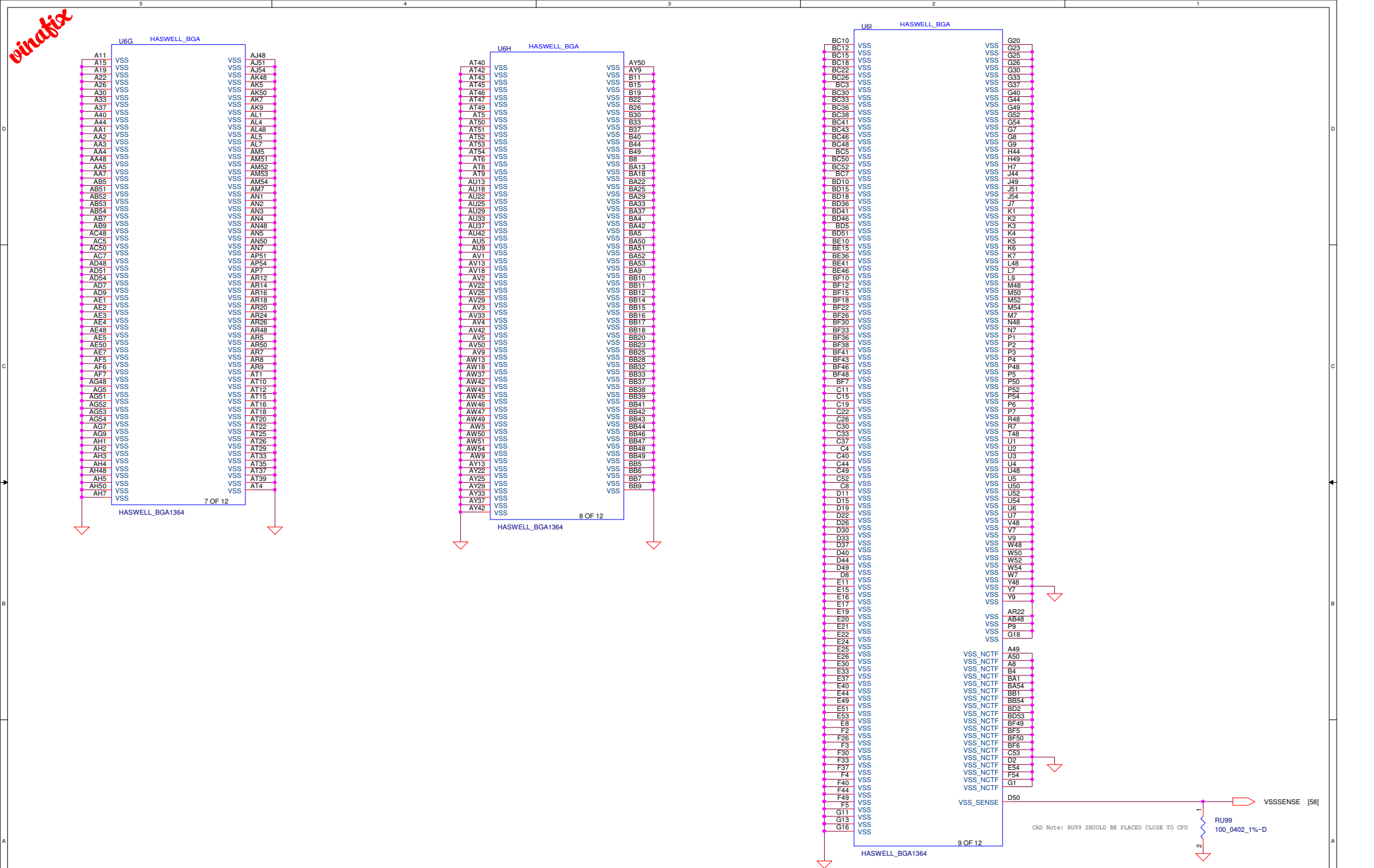
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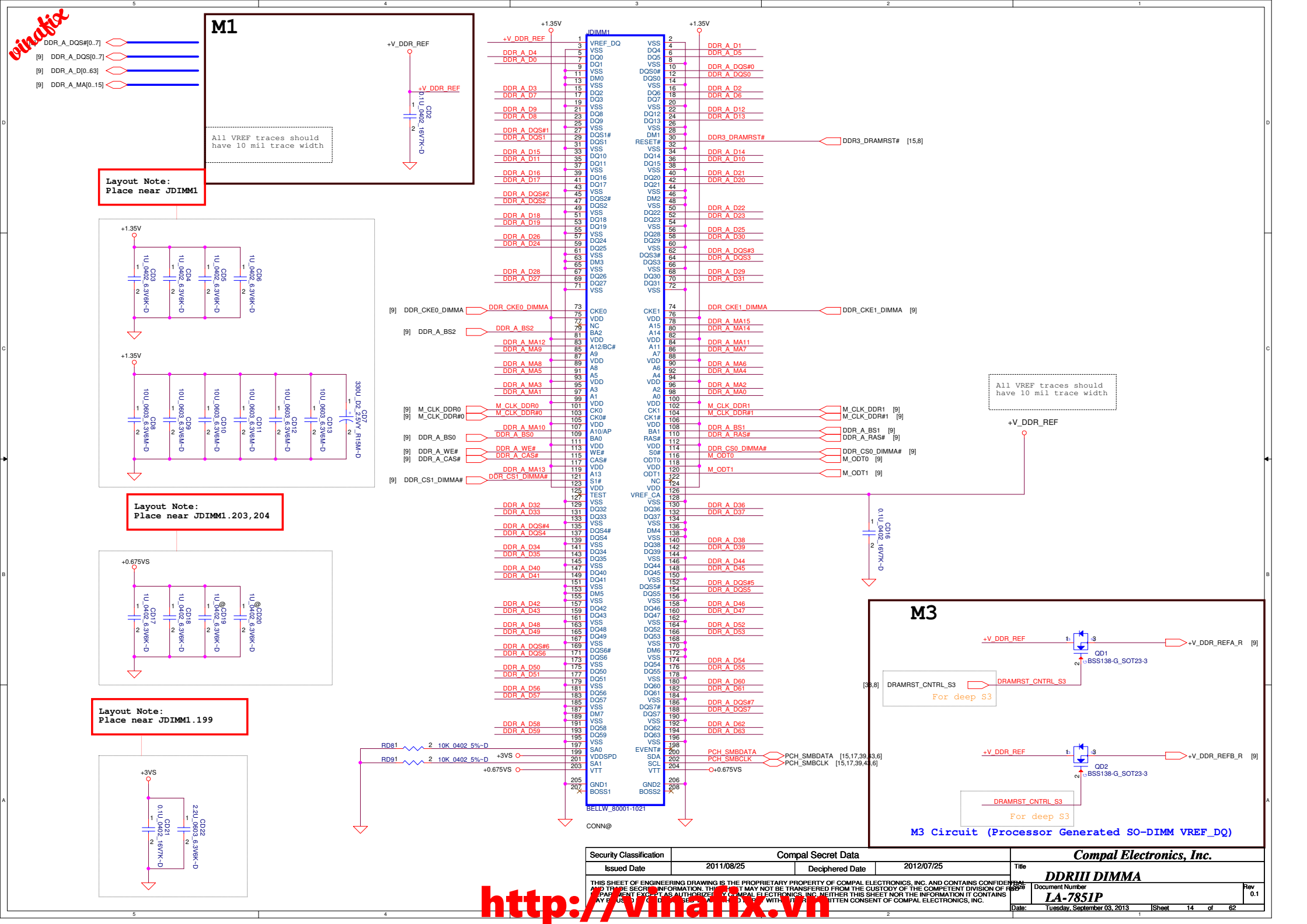


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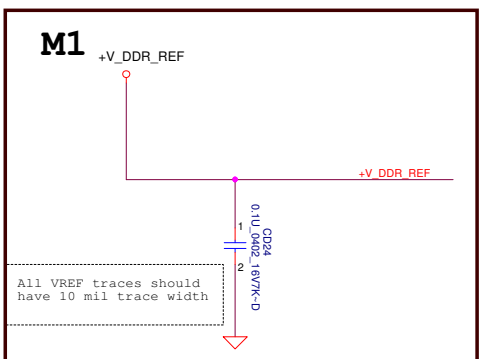


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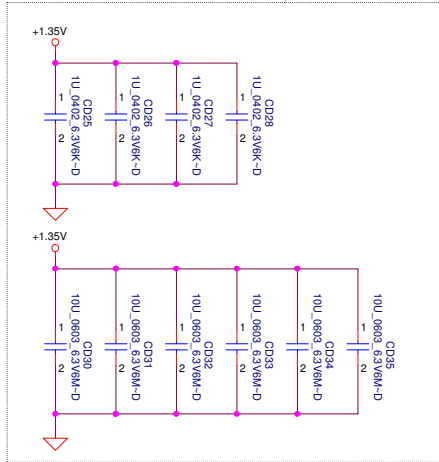
<http://vinafix.vn>



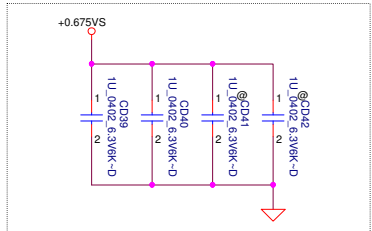
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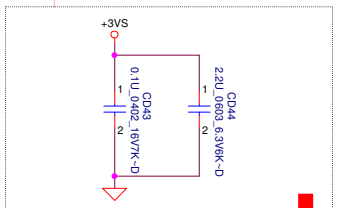
Layout Note:
Place near JDIMMB



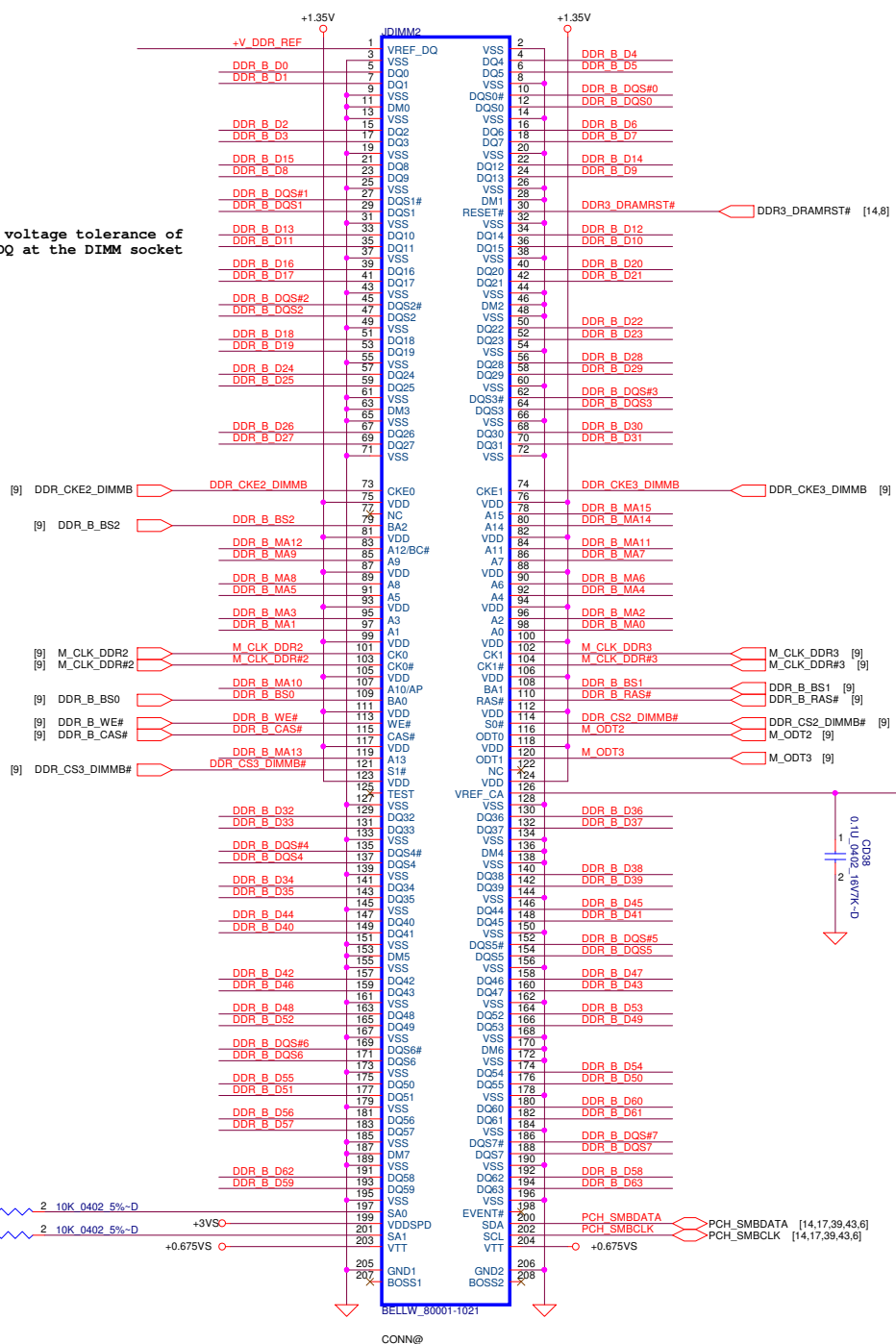
Layout Note:
Place near JDIMMB.203,204



Layout Note:
Place near JDIMMB.199

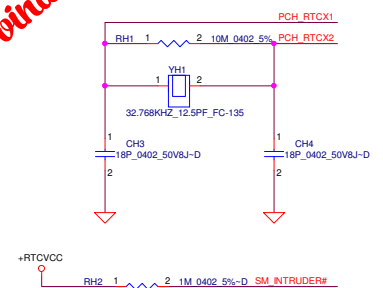


Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



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				Document Number		LA-7851P	
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PCH Strap PIN

INTVRMEN Integrated 1.05V VRM Enable/Disable

+RTCVCC

RH13 1 2 330K 0402 5% PCH_INTVRMEN

@RH16 1 2 330K 0402 5% PCH_INTVRMEN

★ H : Integrated VRM enable
L : Integrated VRM disable

SPKR No Reboot

+3VS

@RH17 1 2 1K 0402 5%-D HDA_SPKR

★ LOW=Default
HIGH=No Reboot

If the signal is sampled high, this indicate that the system is strapped to the "No Reboot" mode

HDA_SYNC On-Die PLL Voltage Regulator Voltage Select

+3V_PCH

@RH32 1 2 1K 0402 5%-D HDA_SYNC

★ This signal has a weak internal pull-down
On Die PLL VR is supplied by 1.5V when sampled high
1.8V when sampled low
Needs to be pulled High for Huron River platform

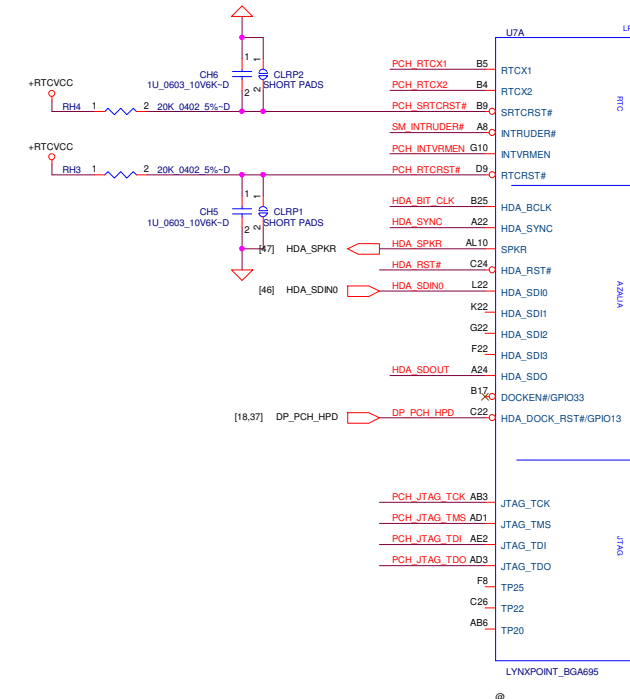
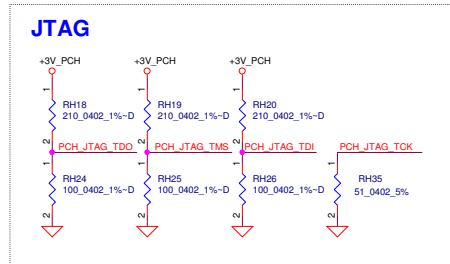
HDA_SDO Flash Descriptor Security Override/Intel ME Debug Mode

+3V_PCH

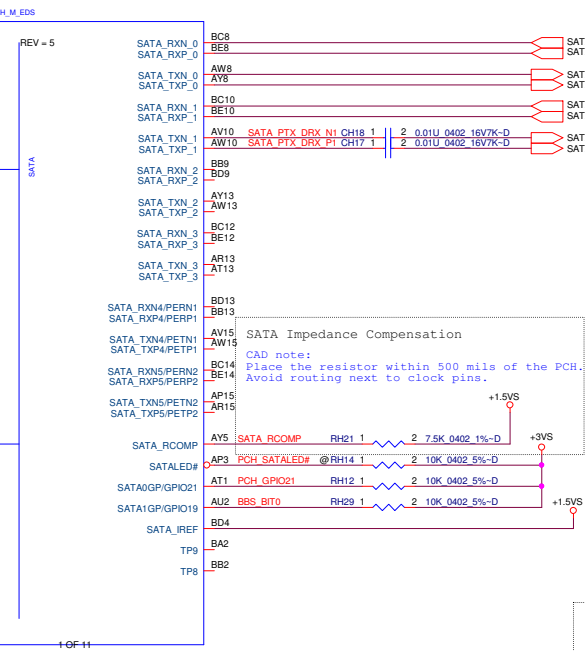
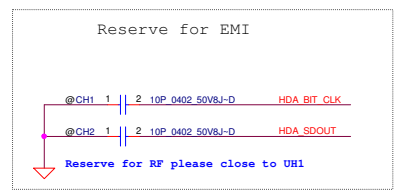
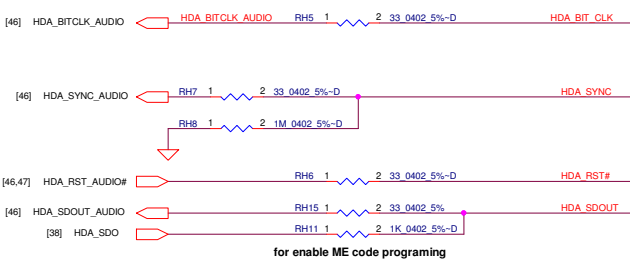
@RH23 1 2 1K 0402 5%-D HDA_SDO

★ Low = Disabled
High = Enabled

ME debug mode , this signal has a weak internal PD
L=>security measures defined in the Flash Descriptor will be in effect (default)
H=>Flash Descriptor Security will be overridden



HD Audio



RTC Battery



Boot BIOS Strap

@RH245 1 2 1K 0402 5%-D BBS_BIT0

@RH244 1 2 1K 0402 5%-D BBS_BIT1 [18]

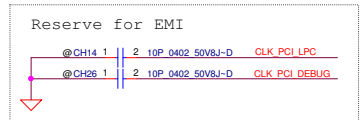
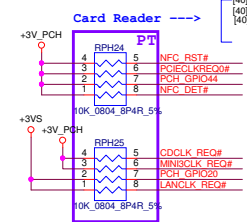
GPIO19 => BBS_BIT0
GPIO51 => BBS_BIT1

Boot BIOS Strap		
BBS_BIT[1]	BBS_BIT[0]	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

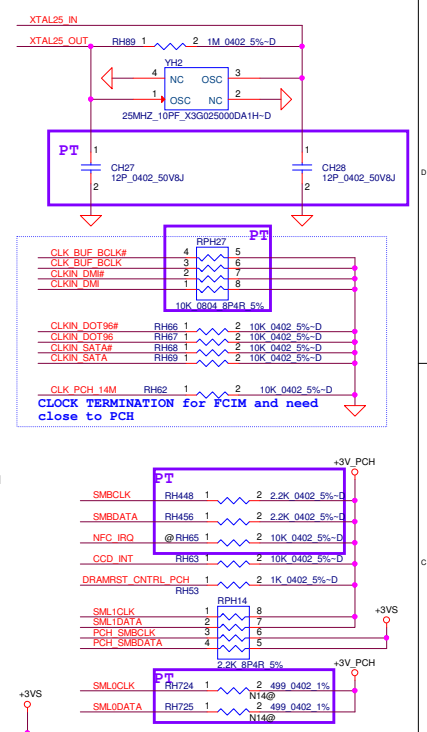
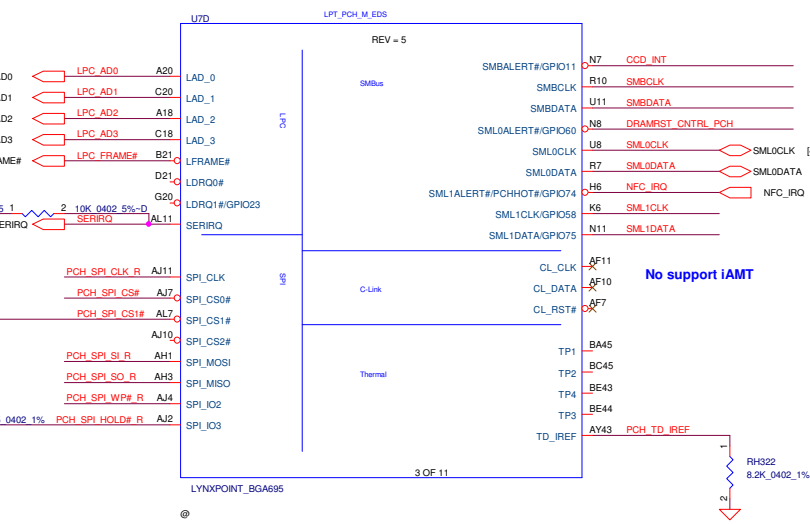
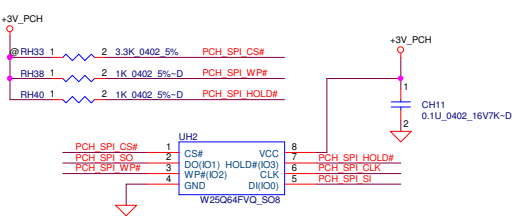
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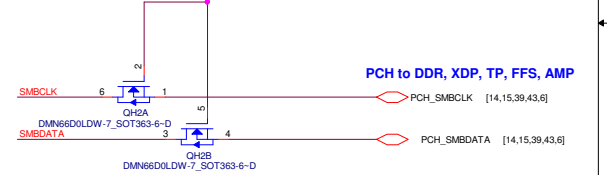
MiniWLAN (Mini Card 1)---->



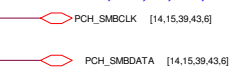
SPI ROM FOR ME (8MByte)



PCH to NFC

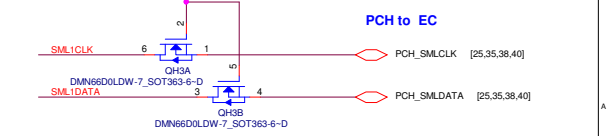


PCH to DDR, XDP, TP, FFS, AMP



No support iAMT

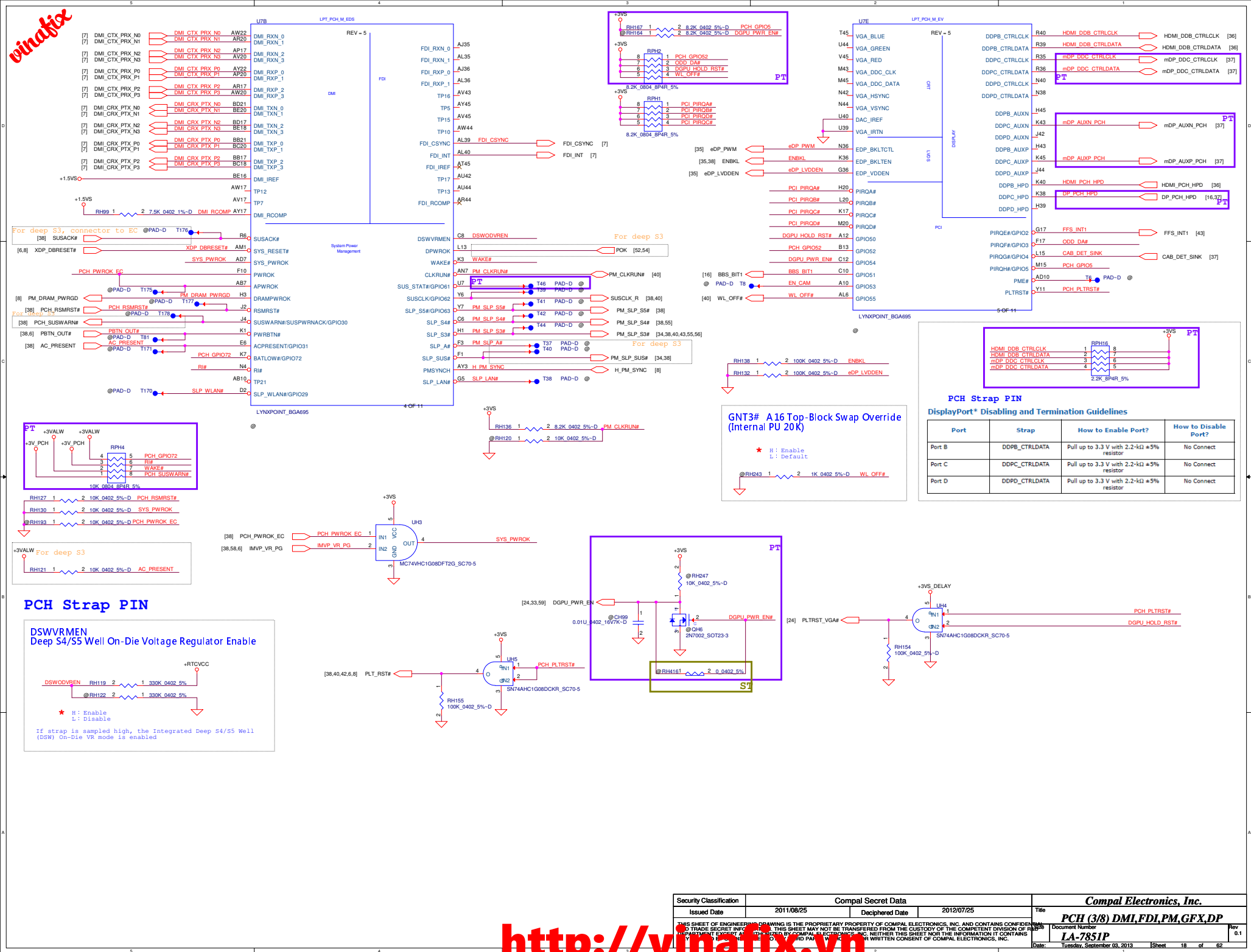
PCH to EC



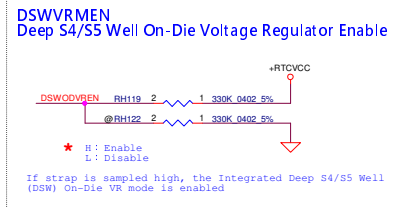
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		Date	Tuesday, September 17, 2013
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PCH Strap PIN



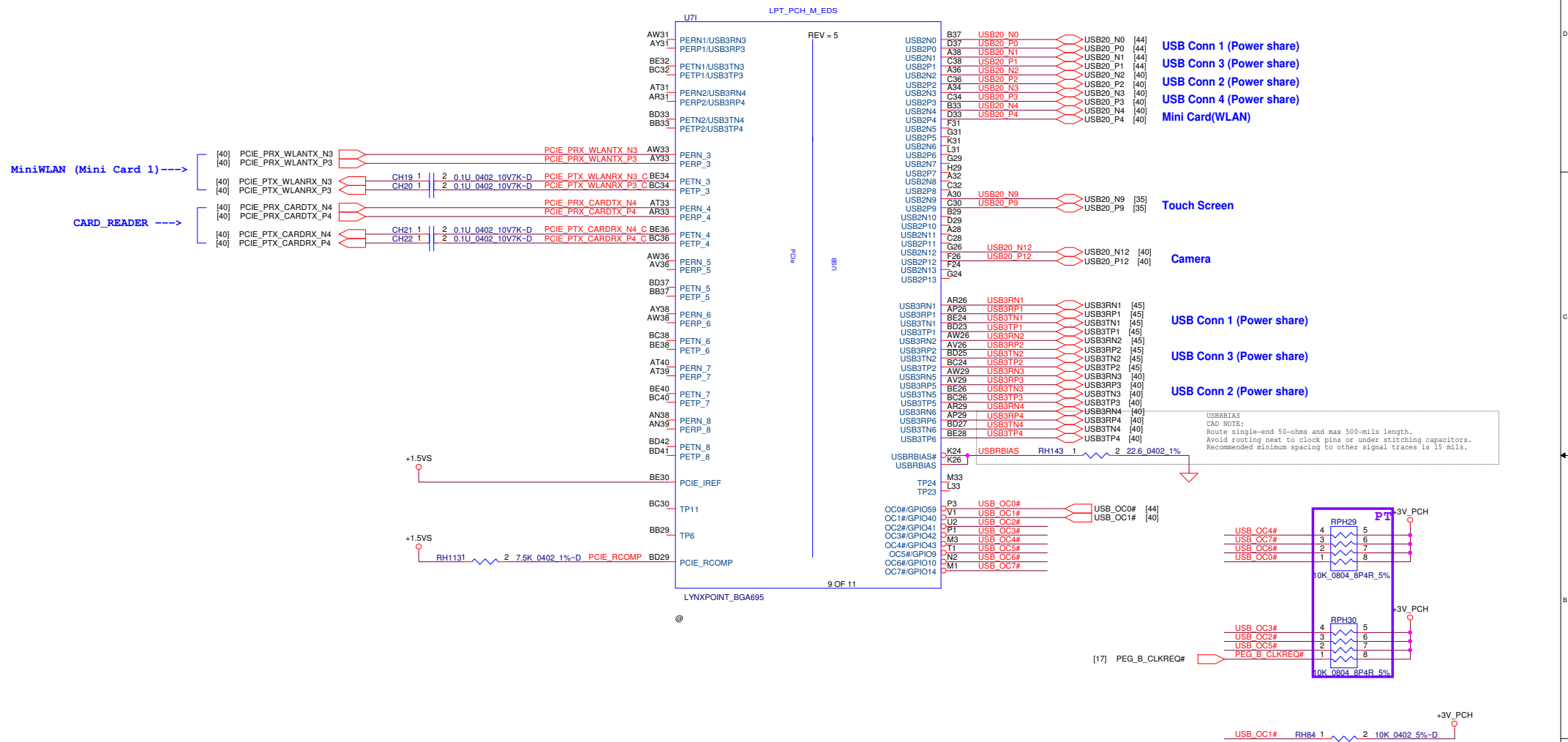
PCH Strap PIN

DisplayPort* Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k Ω $\pm$ 5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k Ω $\pm$ 5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k Ω $\pm$ 5% resistor	No Connect

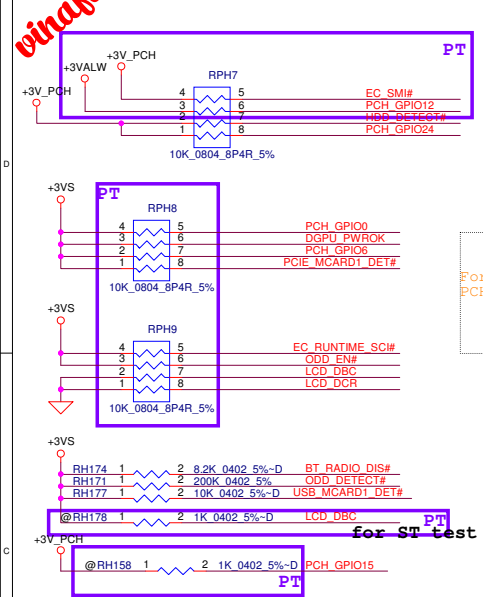
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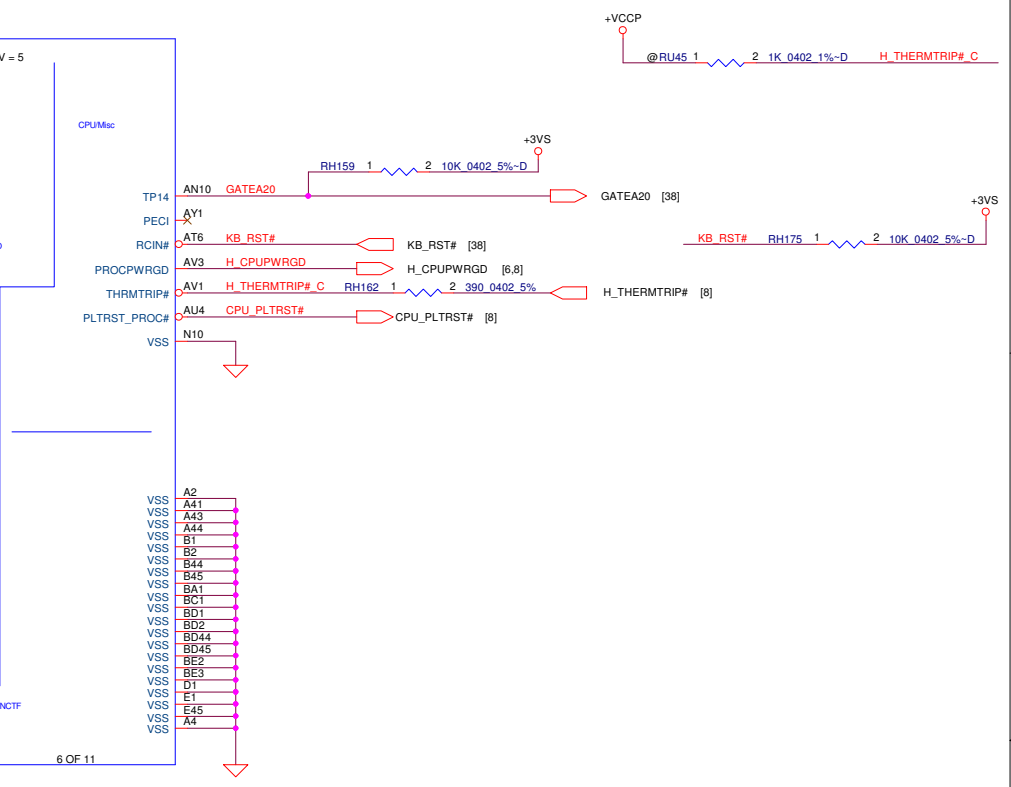
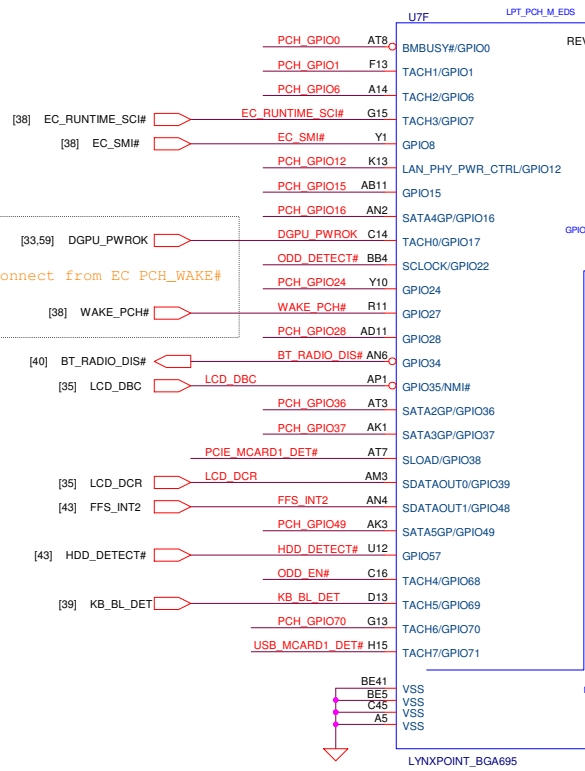


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For deep S3,
PCH_GPIO27 connect from EC PCH_WAKE#



PCH Strap PIN

GPIO37 TLS Confidentiality

Low - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
High - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

★

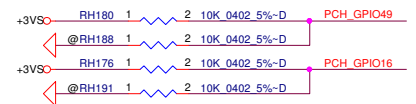
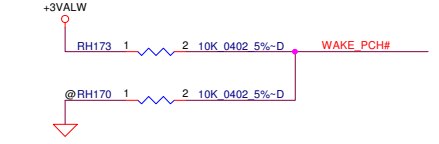
GPIO28 On-Die PLL Voltage Regulator

This signal has a weak internal pull up

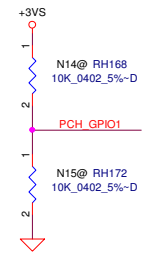
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

SATA2GP/GPIO36 Reserved

When Unused as GPIO or SATA*GP -
Use 8.2K-10K pull-down to ground



config	GPIO16,GPIO49
★ USB X4,PCIEX8,SATAX6	11
USB X6,PCIEX8,SATAX4	01



DGPU Board ID Optional

PCH_GPIO1
N14P
1 = N14P-GT 0 = N15P

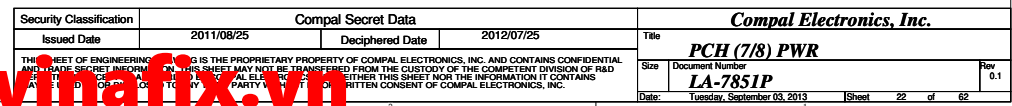
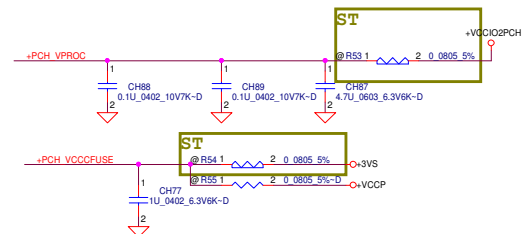
PCH_GPIO70

DIS	1
UMA	0

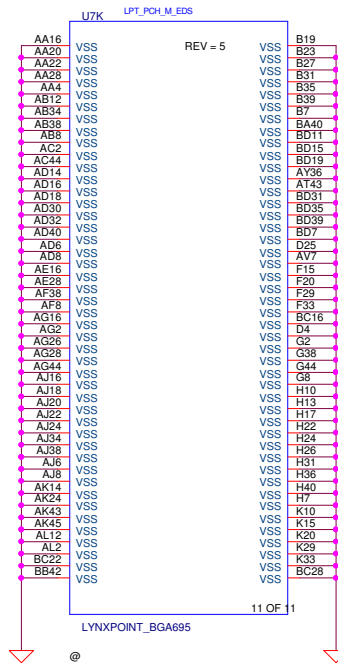
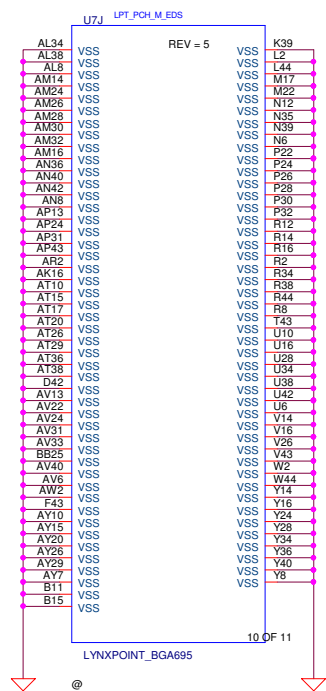
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Issued Date		2011/08/25		Deciphered Date	
2012/07/25				Title	
				PCH (6/8) PWR	
				Size	
				Document Number	
				LA-7851P	
				Date: Tuesday, September 03, 2013	
				Sheet 21 of 62	

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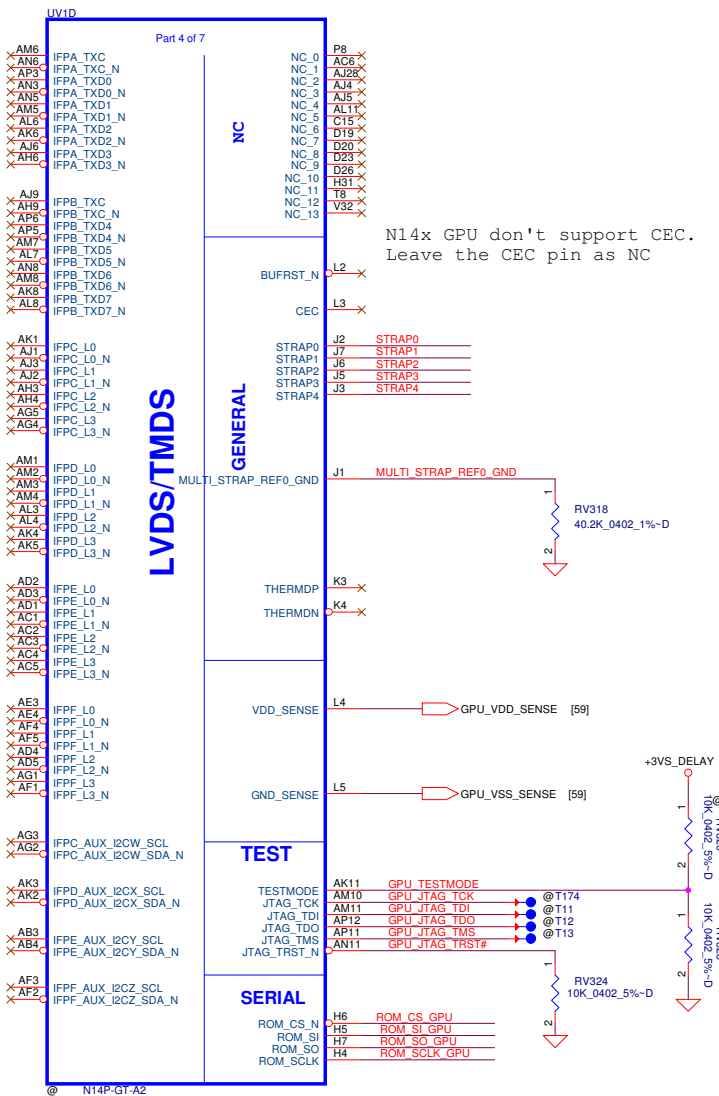
vinafix



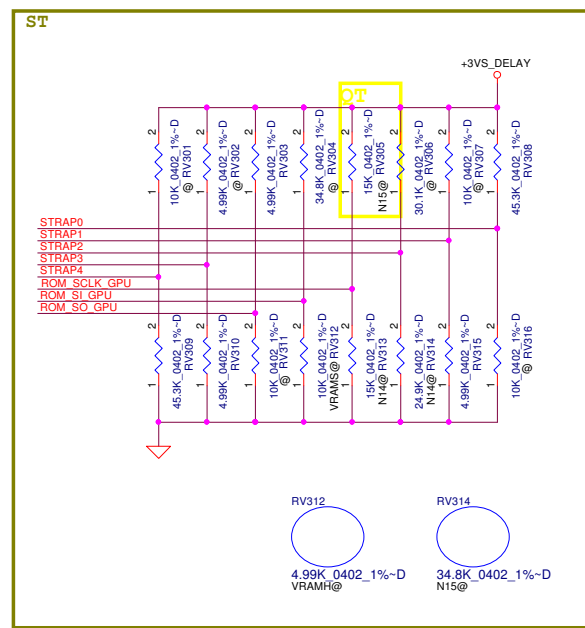
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Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	PCH (8/8) VSS
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				Date	Tuesday, September 03, 2013
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				Rev	0.1

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Straps

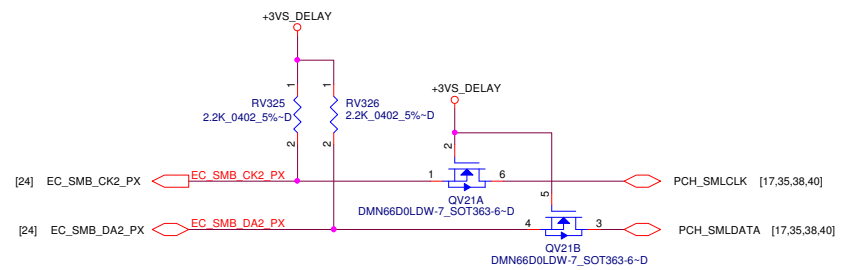
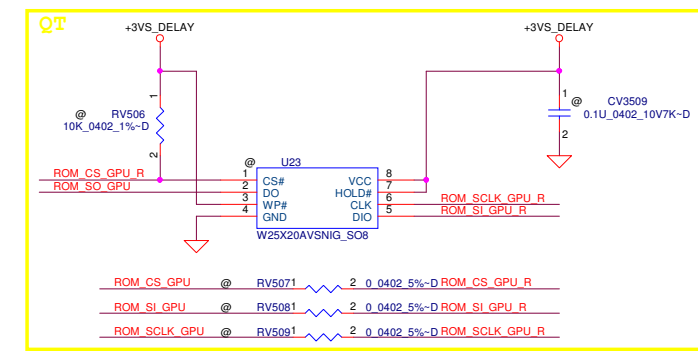


	N14P-GT	N15P-Q1
ROM SCL	PD 15K	PU 15K
ROM SI	PD 10K	
ROM SO	PU 5K	
STRAP[0]	PU 45K	
STRAP[1]	PD 5K	
STRAP[2]	PD 24.9K	PD 35K
STRAP[3]	PD 5K	
STRAP[4]	PD 45K	

Change to PU35K in N15 for use ext ROM

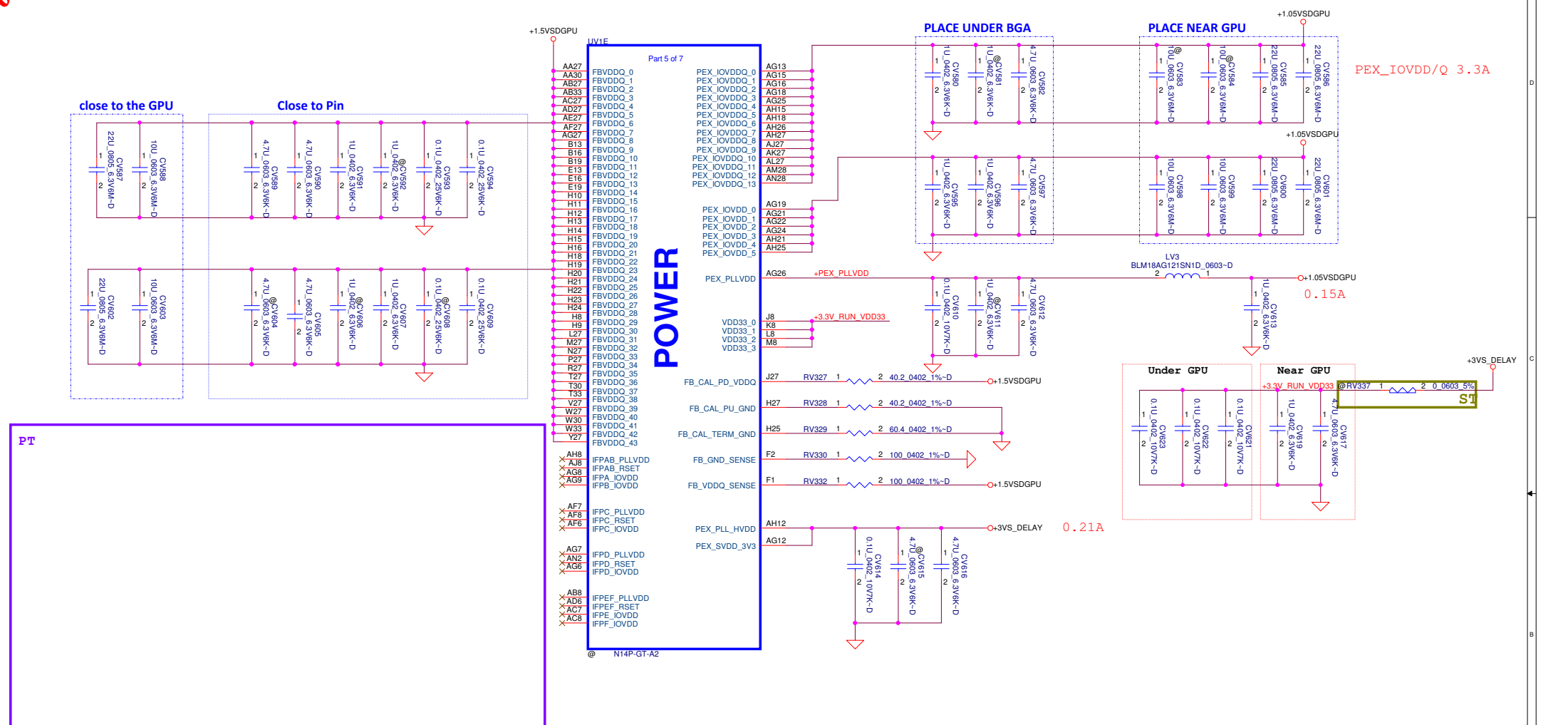
Hynix "0". ROM_SI=PD 5K ohm Samsung"1". ROM_SI=PD 10K ohm

SPI ROM for N14E-GL (2M bit/256K byte)



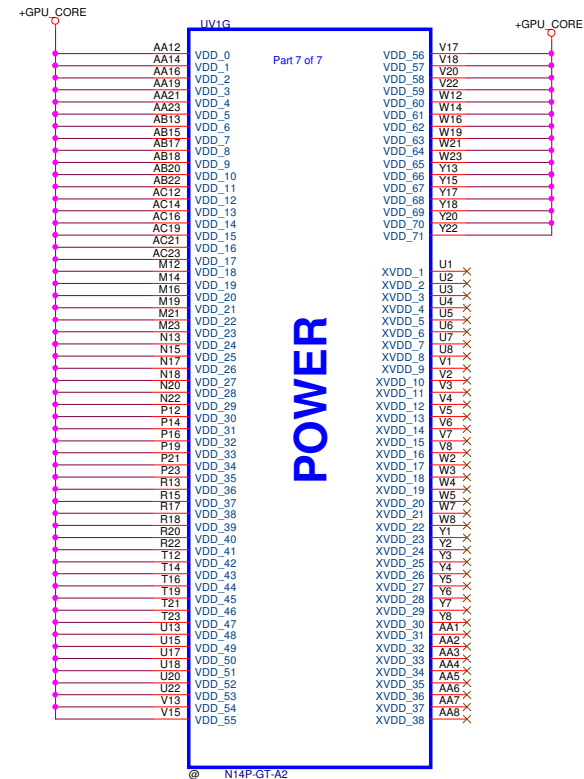
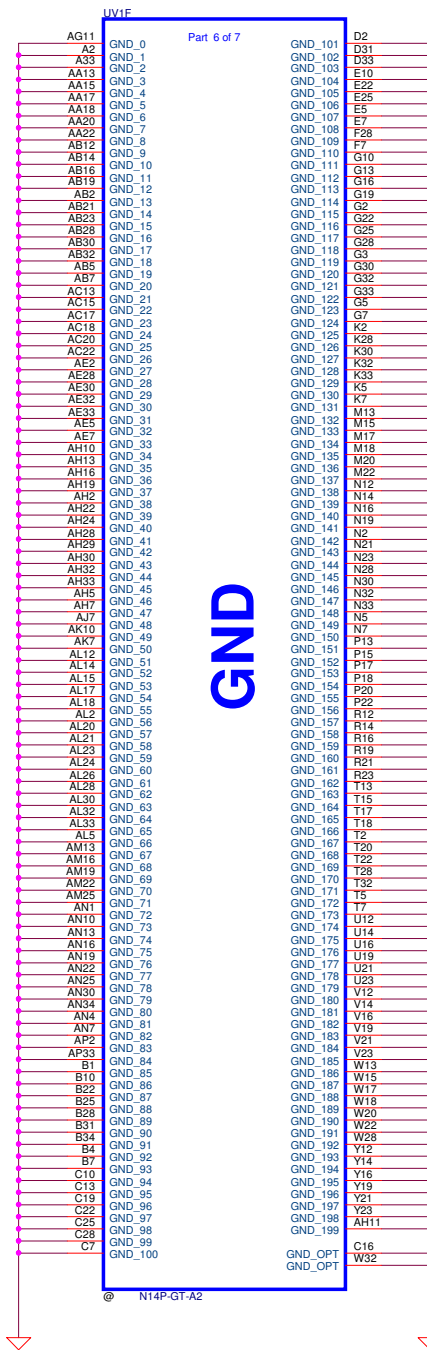
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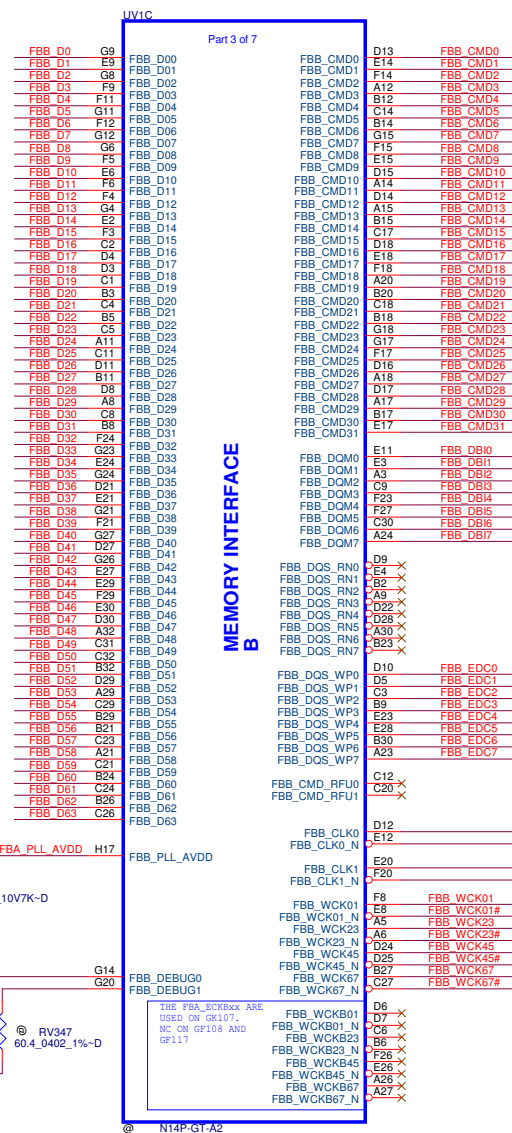
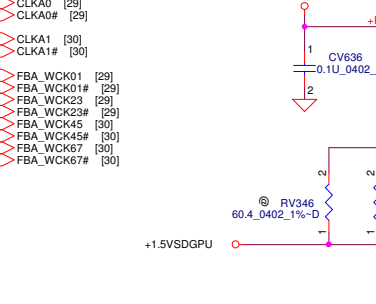
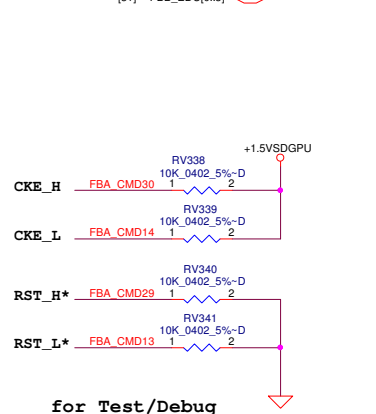
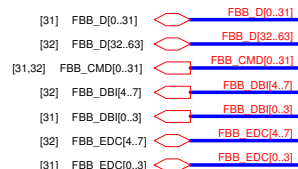
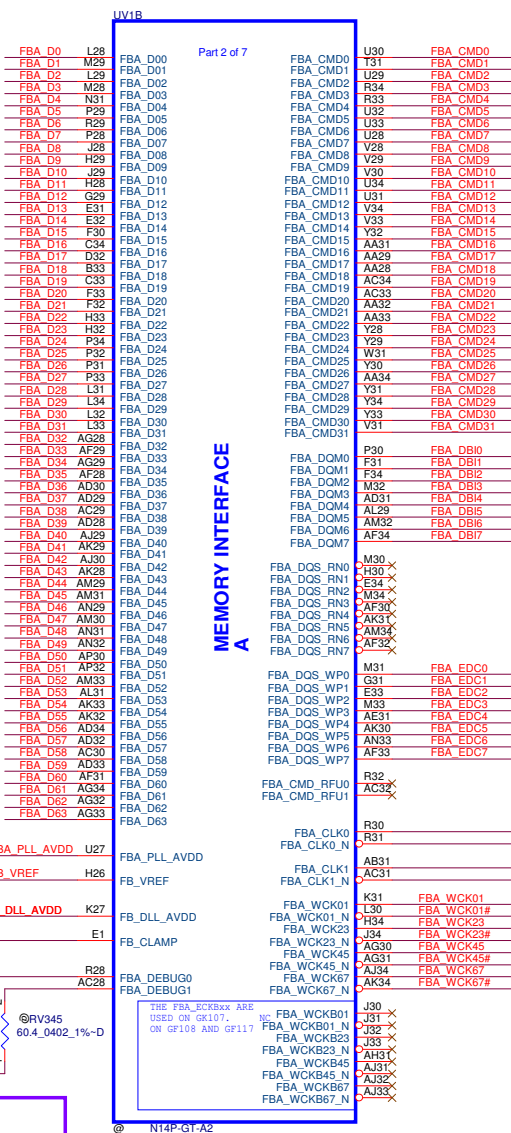
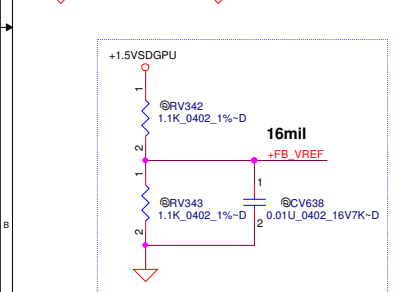
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				Document Number		Rev 0.1	
				Date: Tuesday, September 03, 2013		Sheet 27 of 62	

Figure 1: Schematic representation of the FBA model. The diagram shows a metabolic network with various reactions and their associated fluxes. The reactions are listed on the left, and the fluxes are shown on the right. The reactions are: [29] FBA_D[0..31], [30] FBA_D[32..63], [29,30] FBA_CMD[0..31], [30] FBA_DB[4..7], [29] FBA_DB[0..3], [30] FBA_EDC[4..7], and [29] FBA_EDC[0..3]. The fluxes are represented by blue arrows pointing to the right, with labels: FBA_D[0..31], FBA_D[32..63], FBA_CMD[0..31], FBA_DB[4..7], FBA_DB[0..3], FBA_EDC[4..7], and FBA_EDC[0..3].

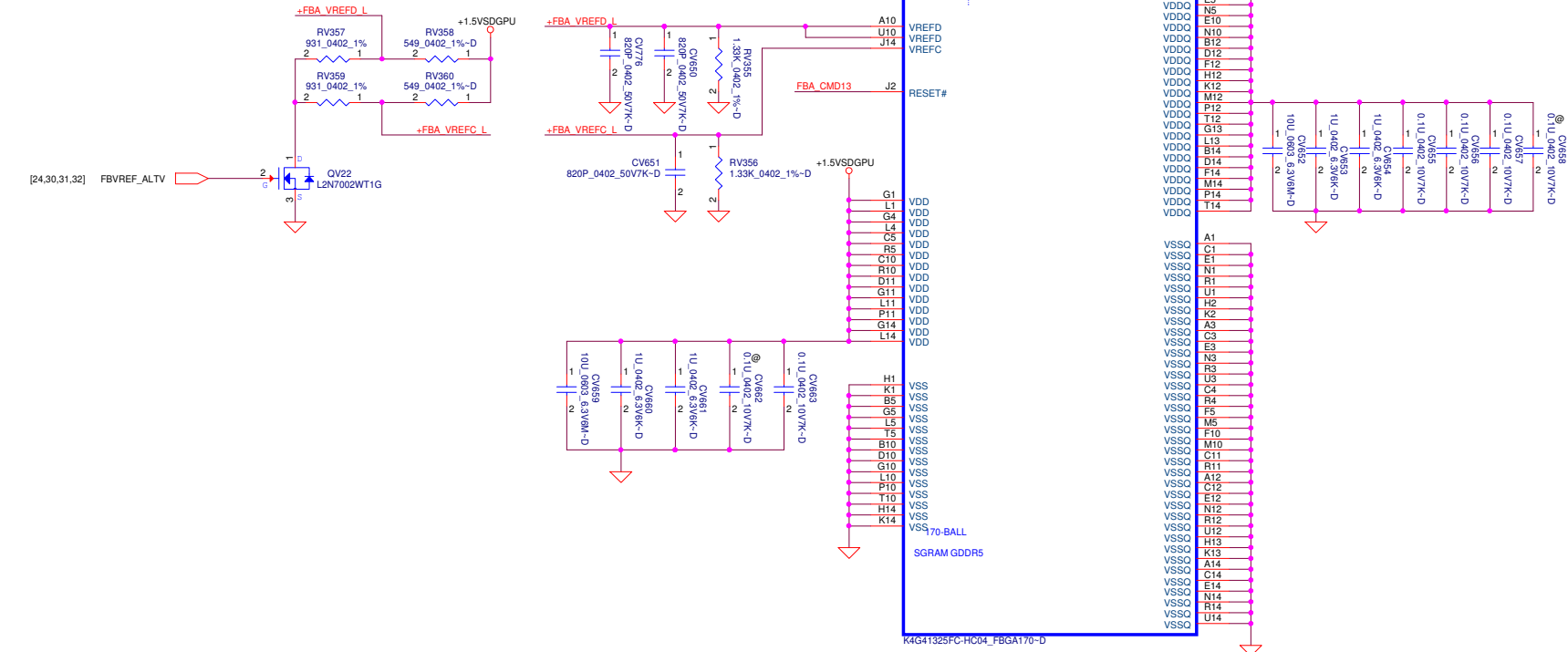


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Memory Partition A - Lower 32 bits

Table 46. GDDR5 Mode H Mapping

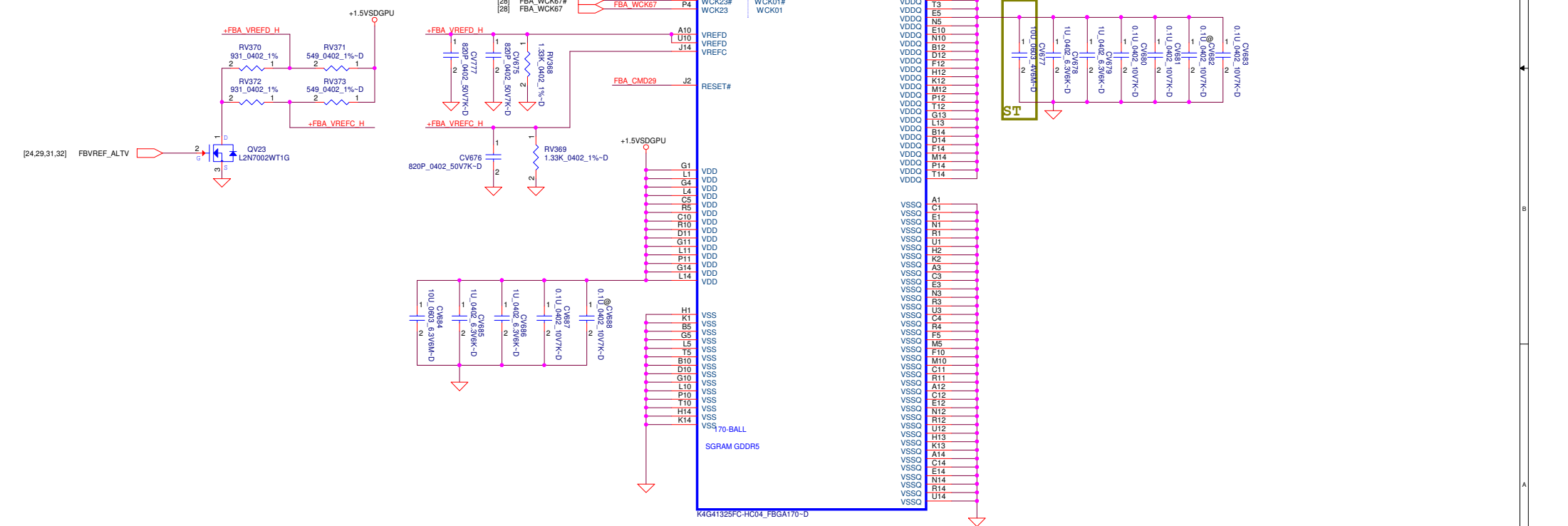
GB2-64, GB4-128	Channel 0 0...31	GB2-64, GB4-128	Channel 1 32...63
CMD0	C5*	CMD16	C5*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	AB1*	CMD24	AB1*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	R5T*	CMD29	R5T*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*



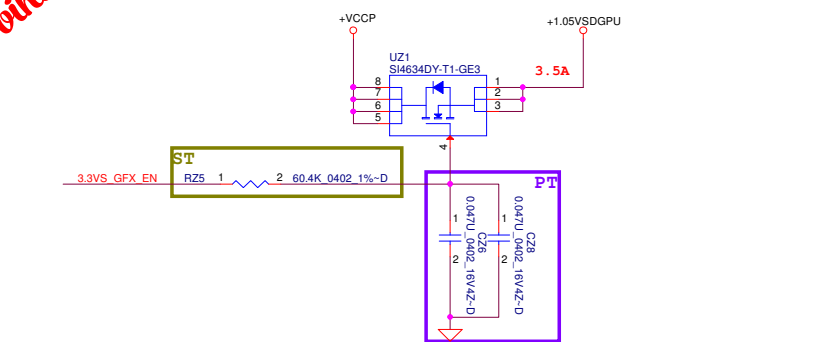
Memory Partition A - Upper 32 bits

Table 46. GDDR5 Mode H Mapping

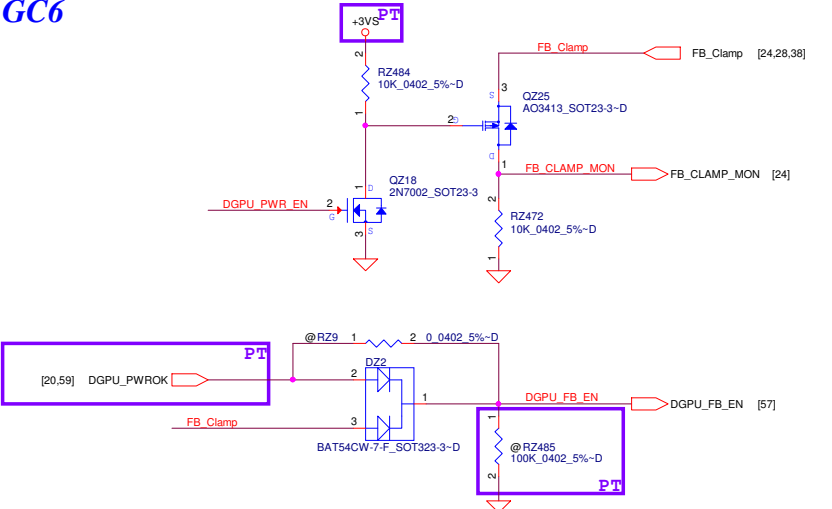
GB2-64, GB4-128	Channel 0 0...31	GB2-64, GB4-128	Channel 1 32...63
CMD0	C5*	CMD16	C5*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	AB1*	CMD24	AB1*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*



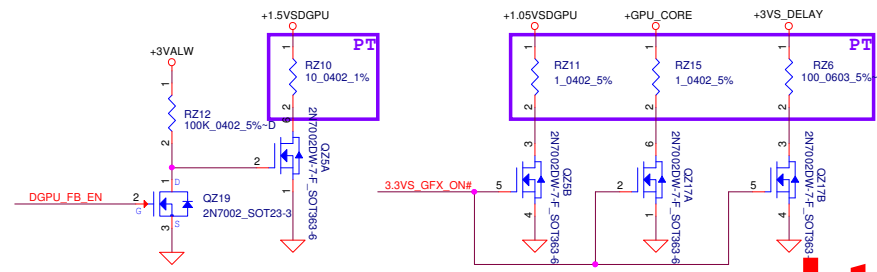
+1.4VS to +1.05VSDGPU



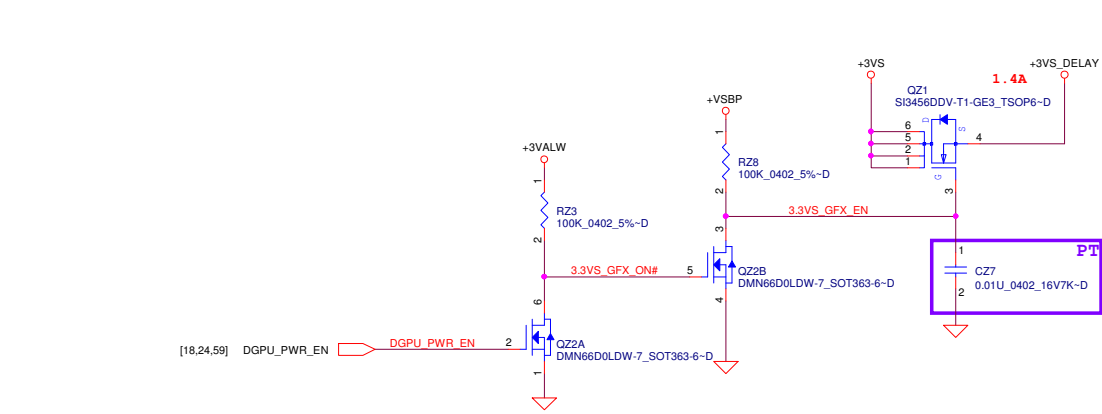
GC6



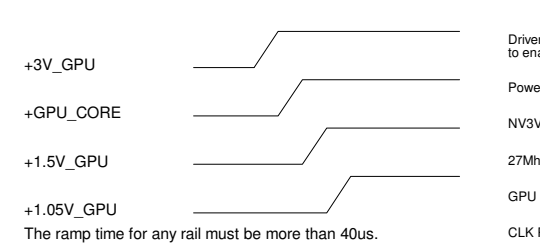
Discharge



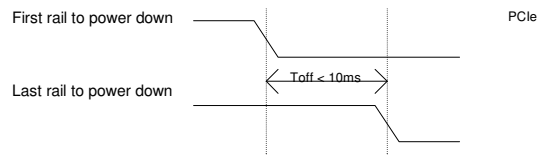
+3VS to +3VS_DELAY



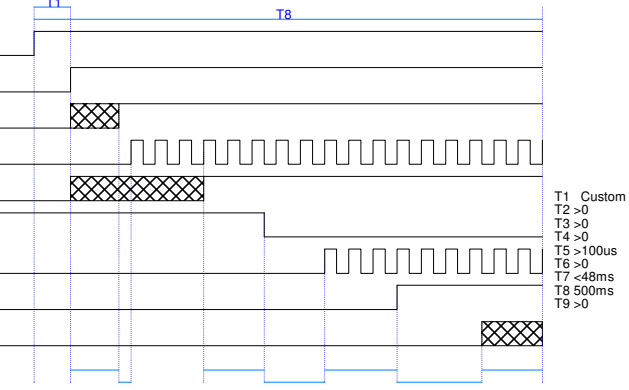
GPU Power Up Power Rail Sequence



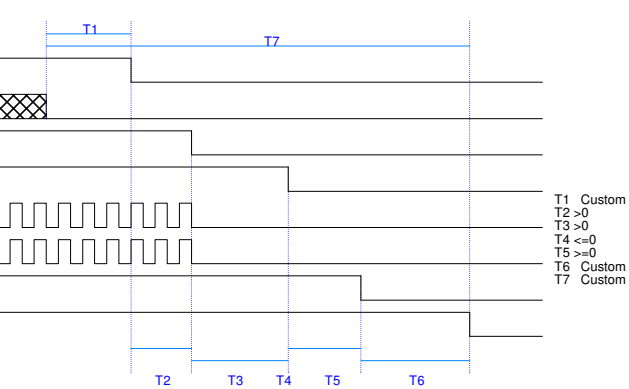
GPU Power Down Sequence



GPU Power Up Sub-system Sequence



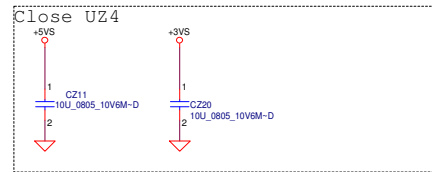
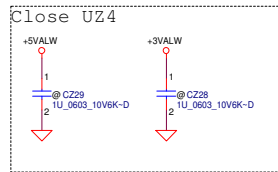
GPU Power Down Sub-system Sequence



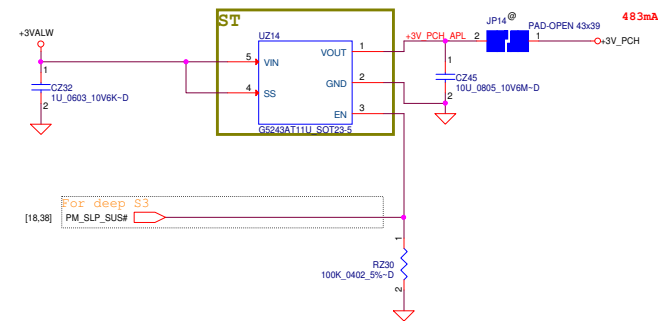
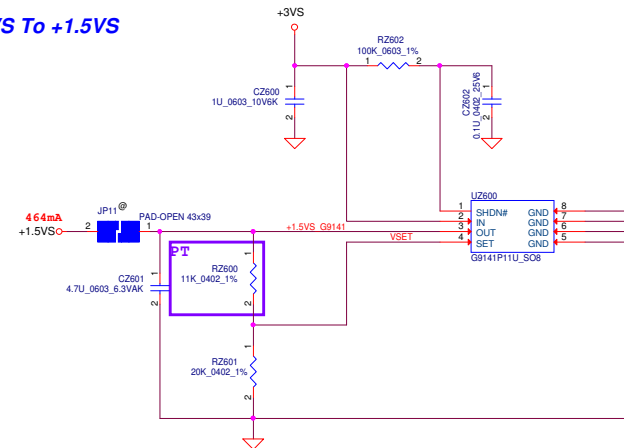
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Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	Block Diagram
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+5V
+3V
vinak



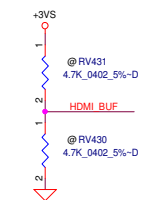
8



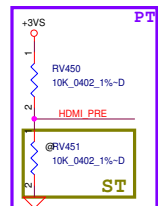
1

LCD backlight PWR CTRL

Touch Screen



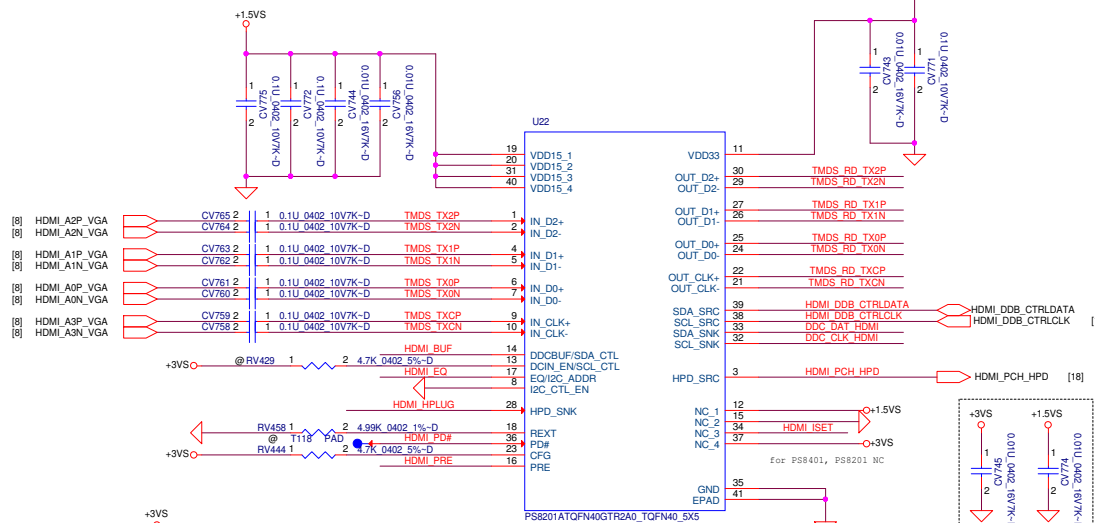
Enable active DDC buffer;
Internal pull down at ~150kΩ, 3.3V I/O
L: default, passive DDC pass-through
H: active DDC buffer with internal pull up 2.36K resistor
M: active DDC buffer without internal pull up resistor



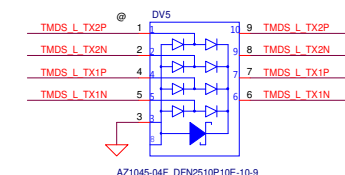
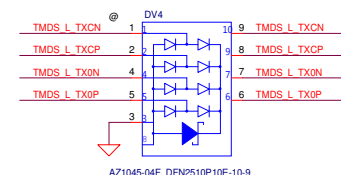
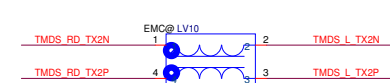
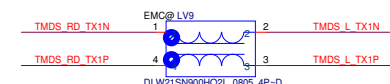
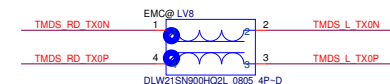
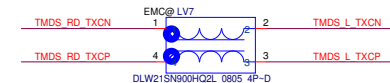
Output pre-emphasis setting;
Internal pull down at ~150kΩ, 3.3V I/O.
L: no pre-emphasis
H: 1.6dB pre-emphasis
M: 3.0dB pre-emphasis



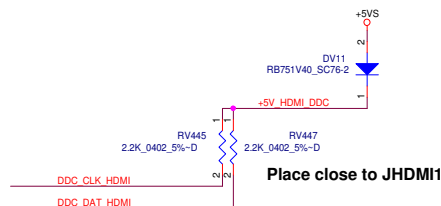
Receiver equalization setting;
Internal pull down at ~150kΩ, 3.3V I/O.
L: programmable EQ for channel loss up to 5.3dB
H: programmable EQ for channel loss up to 10dB
M: programmable EQ for channel loss up to 14dB



PS8201A --- SA00005PJ00
PS8401A --- SA00005CW10

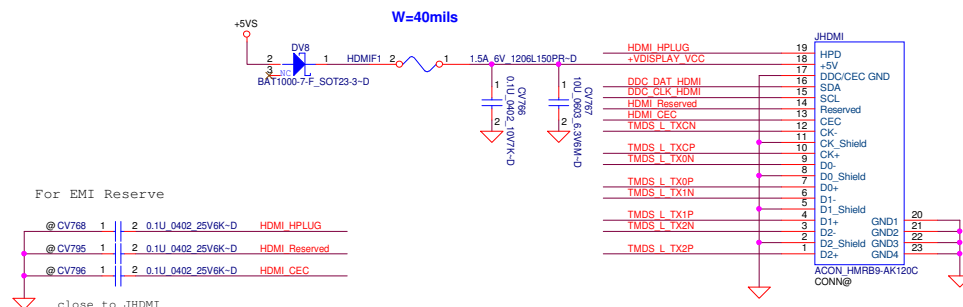


HDMI DDC

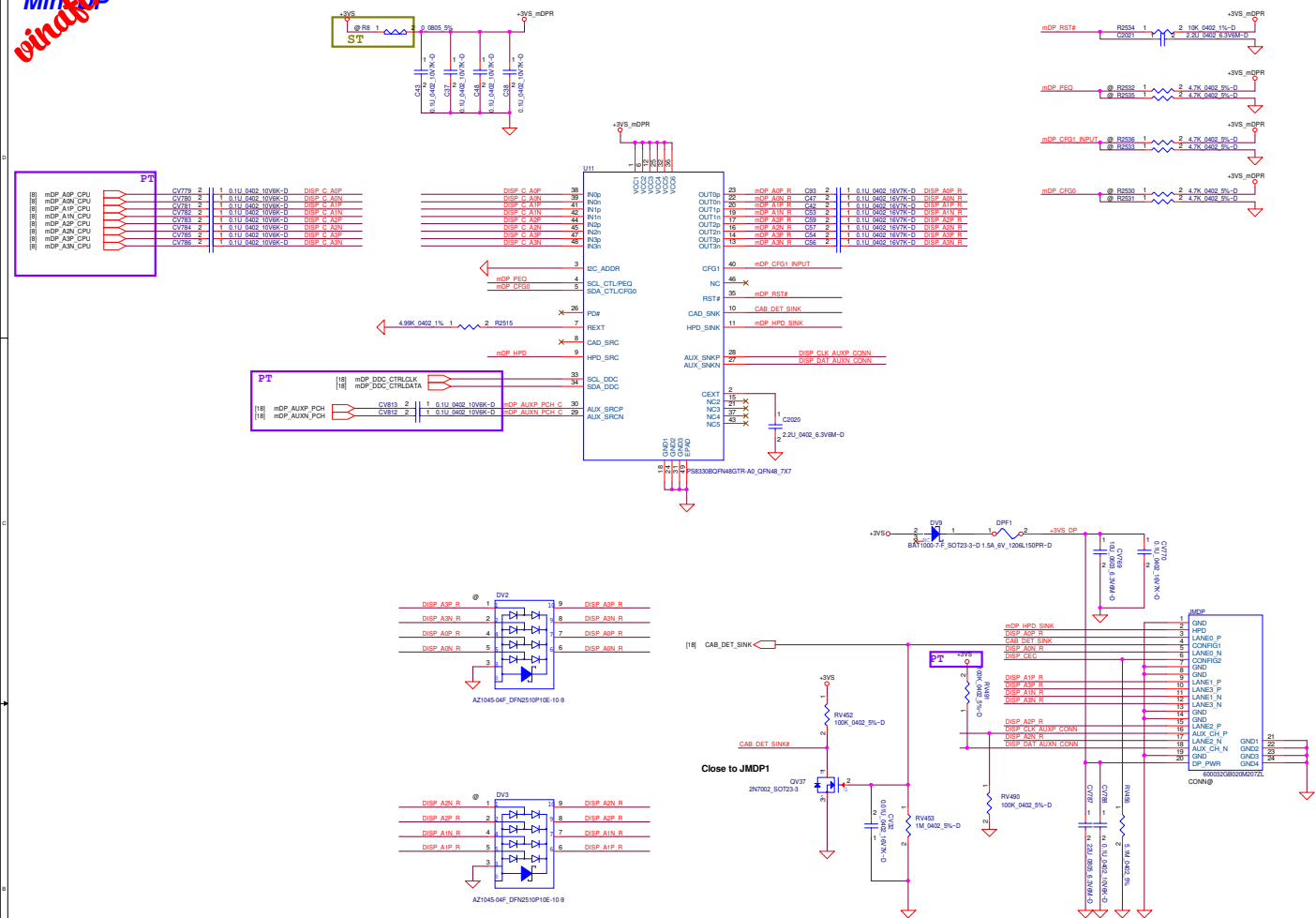


Place close to JHDMI1

HDMI conn



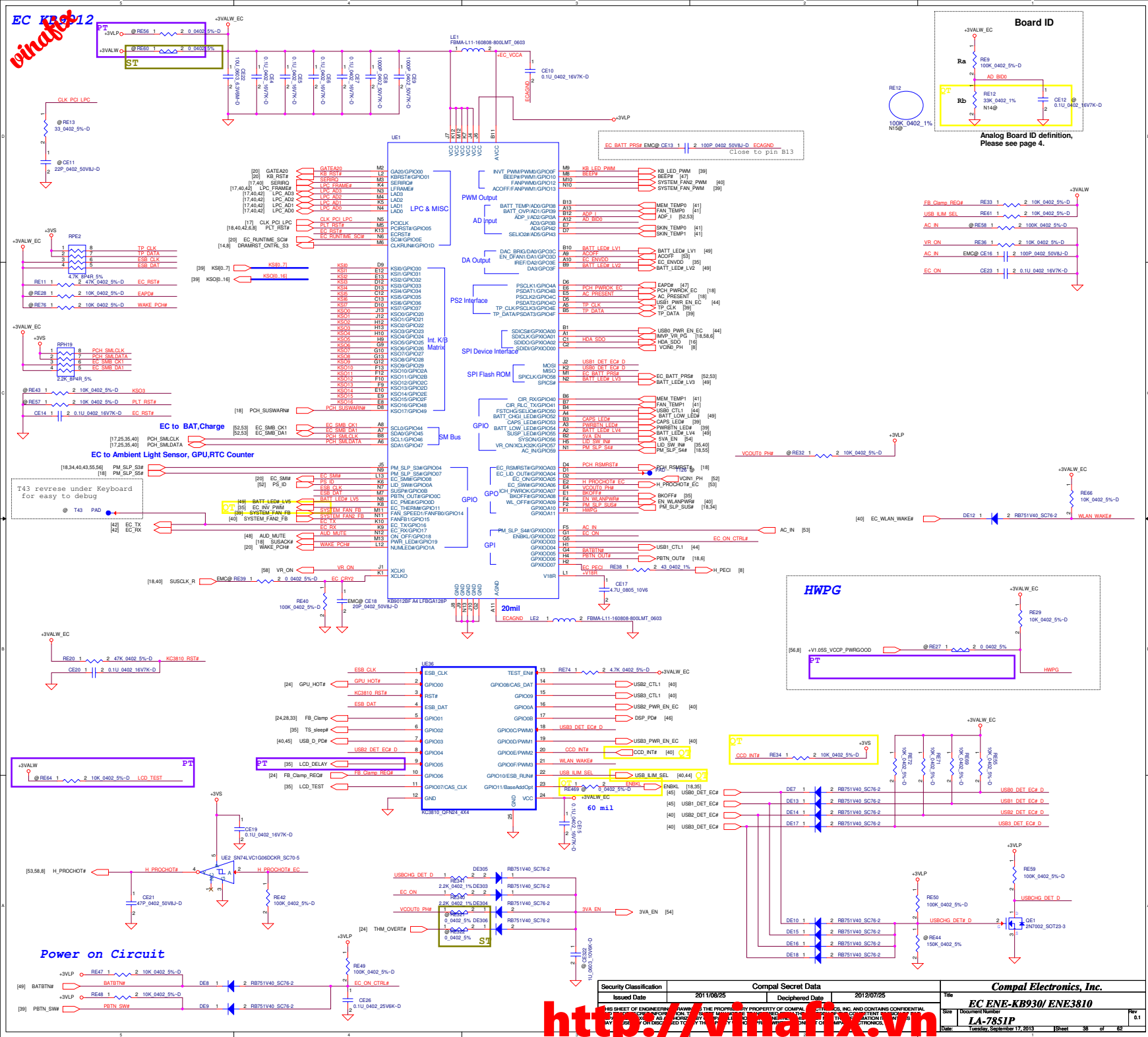
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Issued Date		Deciphered Date		HDMI	
2011/08/25		2012/07/25		LA-7851P	
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Custom		Document Number		0.1	
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DDC Dongle SW for DP

DP HPD to PCH (iGPU)

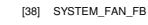
DP HPD for DGPU output (Optimus)



Power



PWM FAN



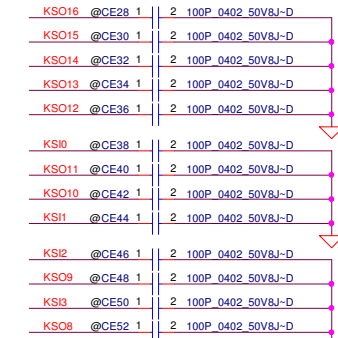
Touch pad



INT_KBD CONN

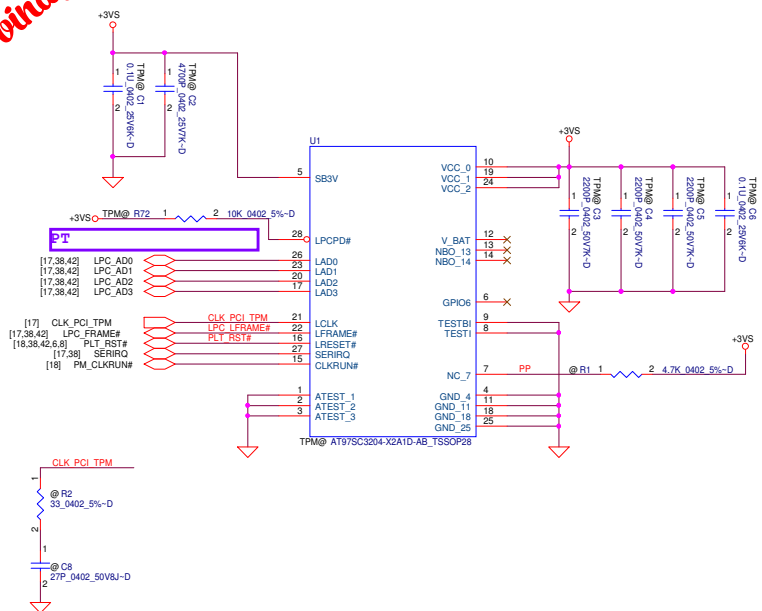


Keyboard back light

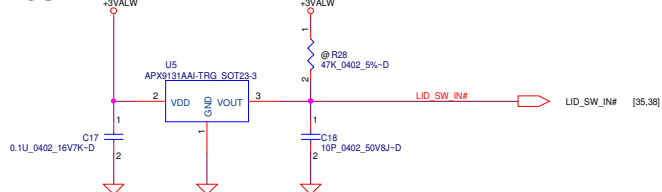


Security Classification		Compal Secret Data		Compal Electronics, Inc. SW/TP/SCREW	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	
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				Document Number LA-7851P	0.1
Date: Tuesday, September 03, 2013				Sheet	39 of 62

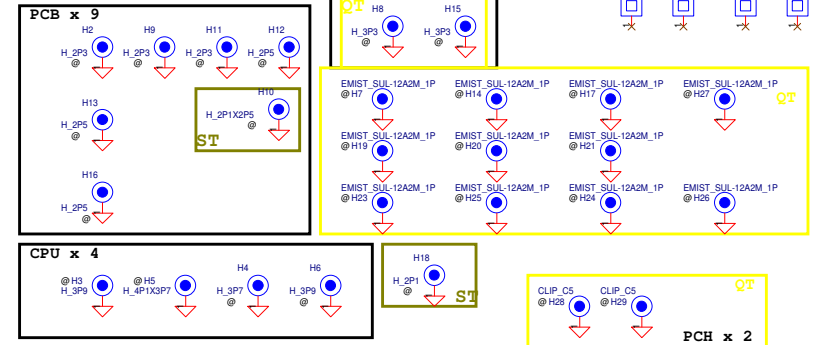
ATMEL TPM



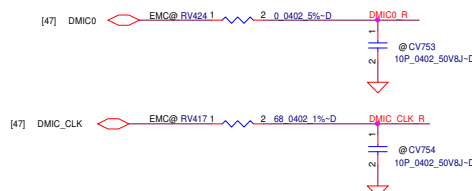
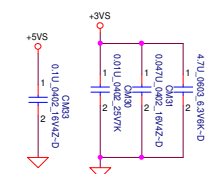
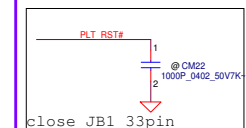
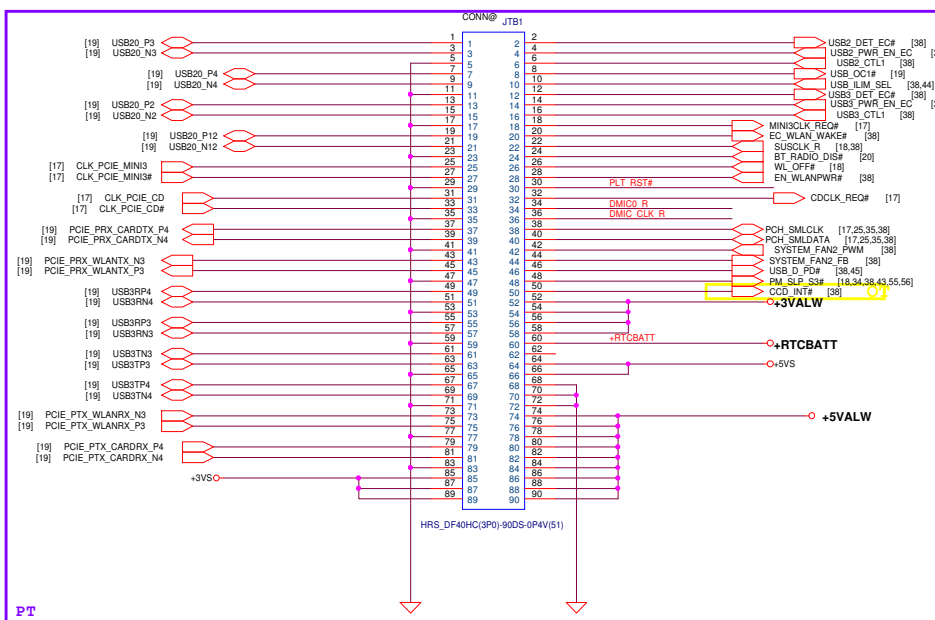
Lid Switch



Screw Hole



M/B to D/B conn.



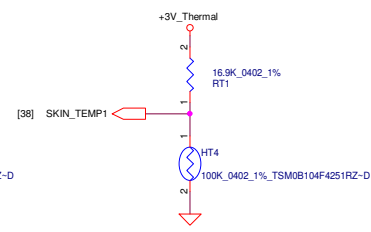
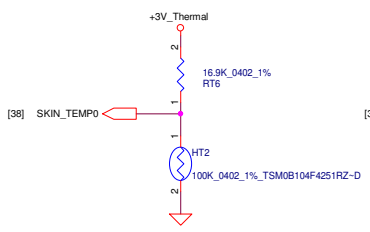
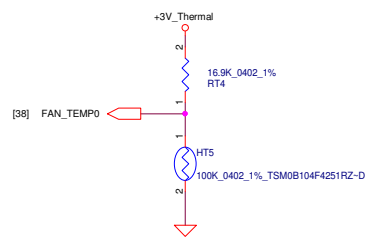
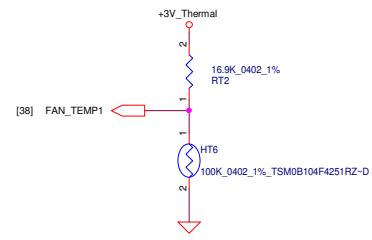
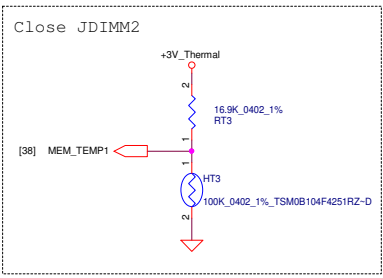
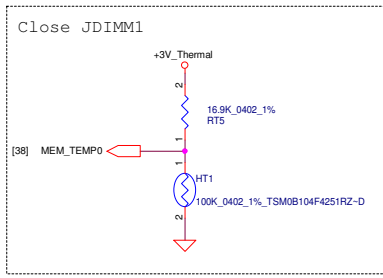
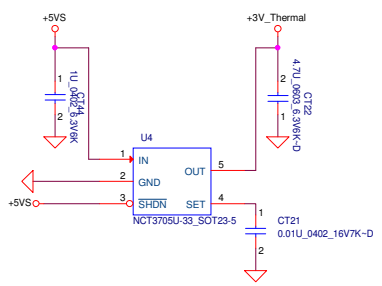
Wedcam PWR CTRL



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				LA-7851P	
Date: Thursday, September 05, 2013				Sheet	40 of 62

<http://vinafix.vn>

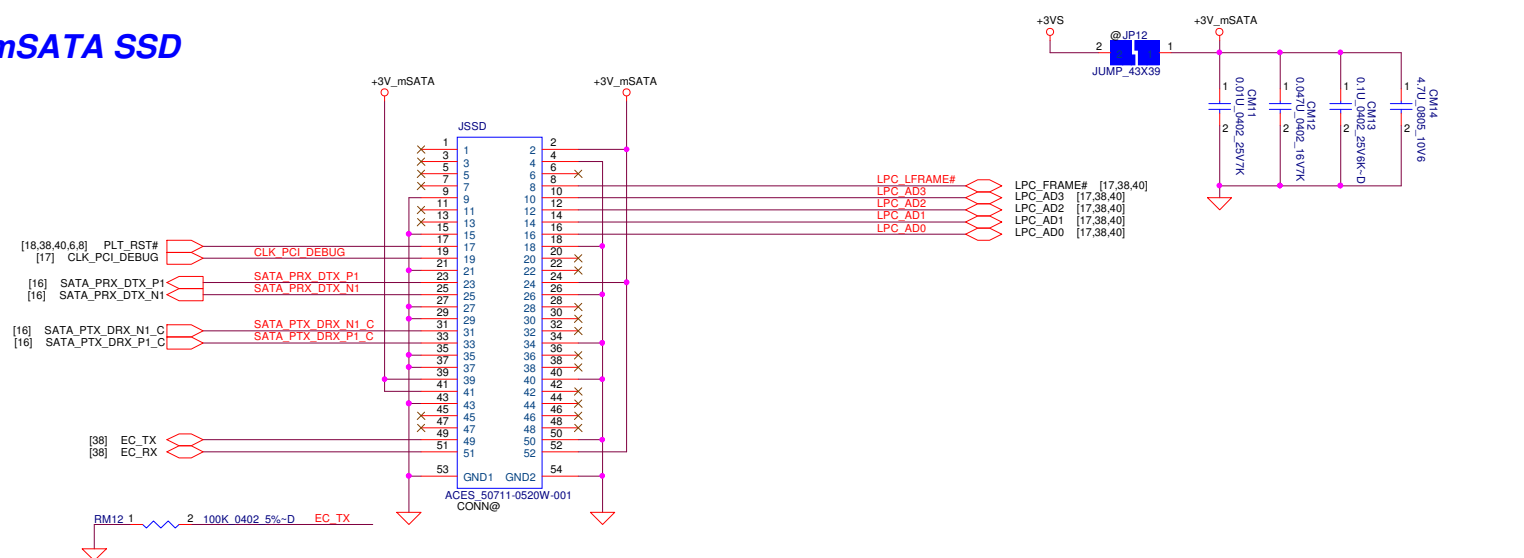
winfix Thermal sensor



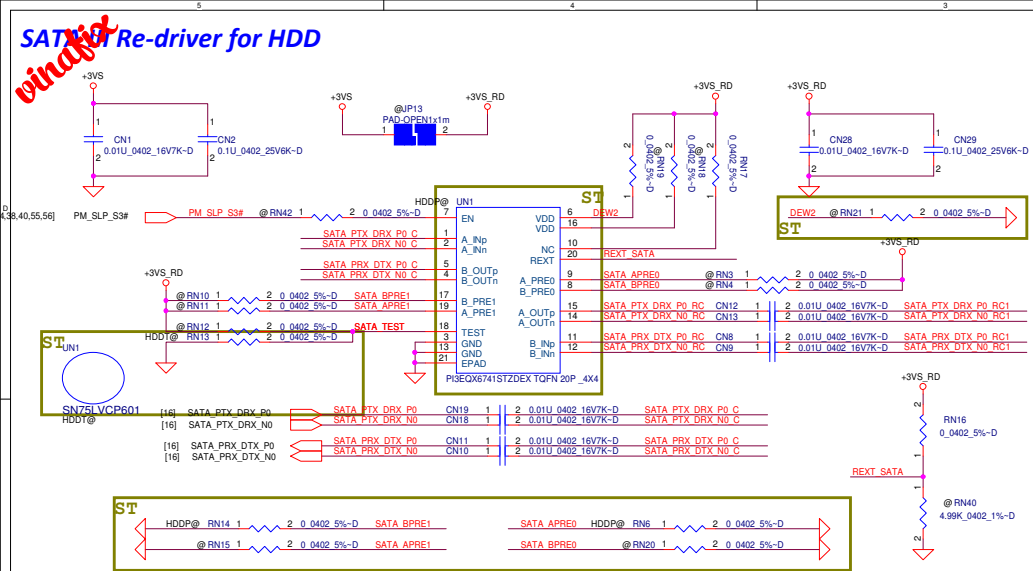
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Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title
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Size	Document Number	Rev		
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Date:	Tuesday, September 03, 2013	Sheet	41	of 62

Pin#	Assignment	Description	Pin#	Assignment	Description
1	N/A	N/A	27	GND	Return Current Path
2	+3.3V	3.3V source	28	N/A	N/A
3	N/A	N/A	29	GND	Return Current Path
4	GND	Return Current Path	30	N/A	N/A
5	N/A	N/A	31	-A (port 1)	SATA Differential Rx- based on SSD
6	N/A	N/A	32	N/A	N/A
7	N/A	N/A	33	+A (port 1)	SATA Differential Rx+ based on SSD
8	N/A	N/A	34	GND	Return Current Path
9	GND	Return Current Path	35	GND	Return Current Path
10	N/A	N/A	36	Reserved	No Connect
11	N/A	N/A	37	GND	Return Current Path
12	N/A	N/A	38	Reserved	No Connect
13	N/A	N/A	39	+3.3V	3.3V Source
14	N/A	N/A	40	GND	Return Current Path
15	GND	Return Current Path	41	+3.3V	3.3V Source
16	N/A	N/A	42	N/A	N/A
17	N/A	N/A	43	N/A	N/A
18	GND	Return Current Path	44	N/A	N/A
19	N/A	N/A	45	Reserved	N/A
20	N/A	N/A	46	N/A	N/A
21	GND	Return Current Path	47	Reserved	N/A
22	N/A	N/A	48	N/A	N/A
23	+B(port 1)	SATA Differential	49	DAVSSG	Device Activity / Disable Staggered Spin-up
24	+3.3V	3.3V Source	50	GND	Return Current Path
25	-B(port 1)	SATA Differential	51	Presence Detection	Shall be pulled to GND by device
26	GND	Return Current Path	52	+3.3V	3.3V Source

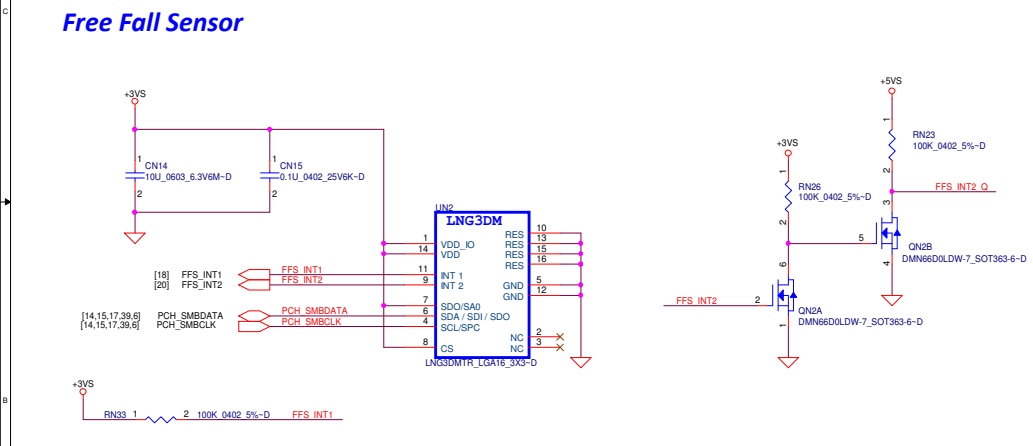
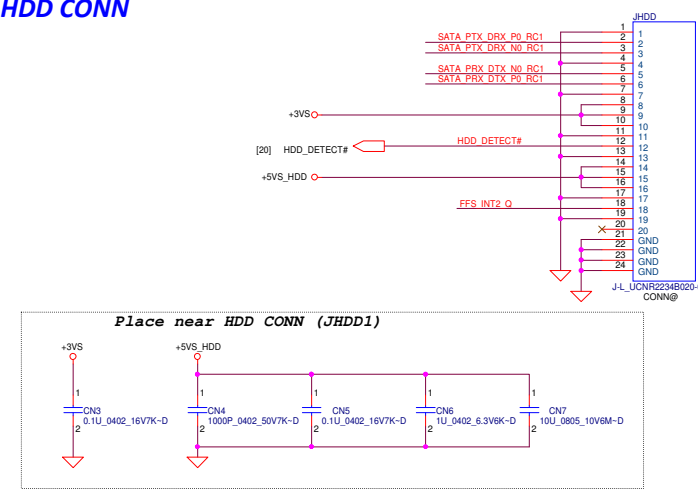
mSATA SSD



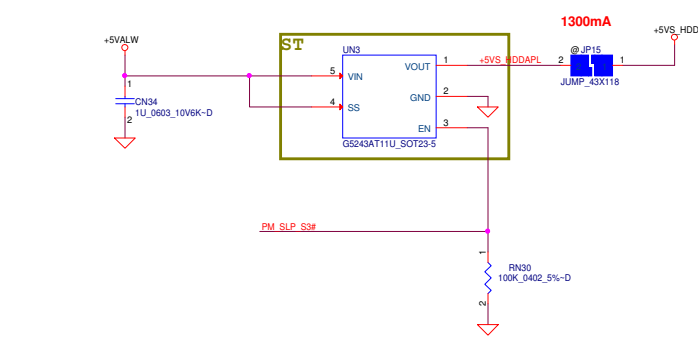
Security Classification		Compal Secret Data		Compal Electronics, Inc. WLAN/WWAN/SIM/BT	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	
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HDD CONN

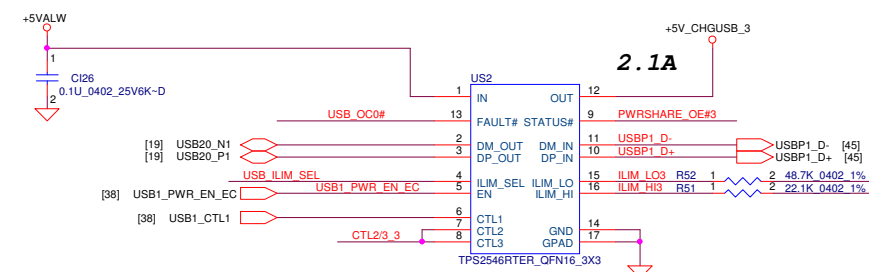
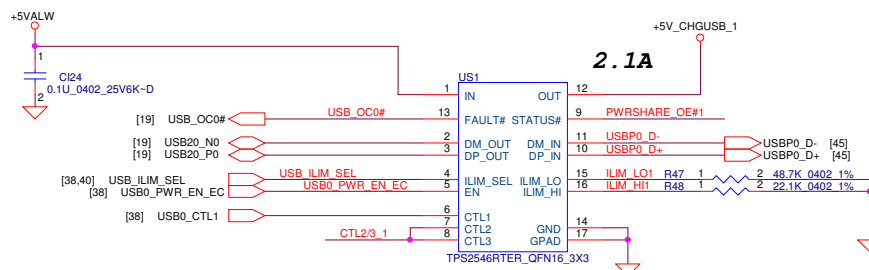
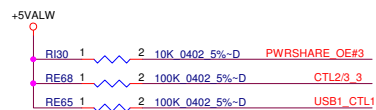
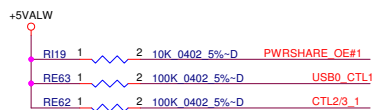


HDD power control for AOAC



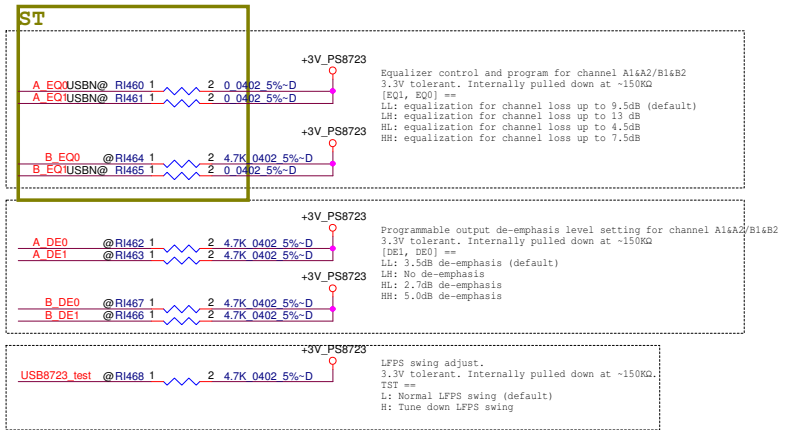
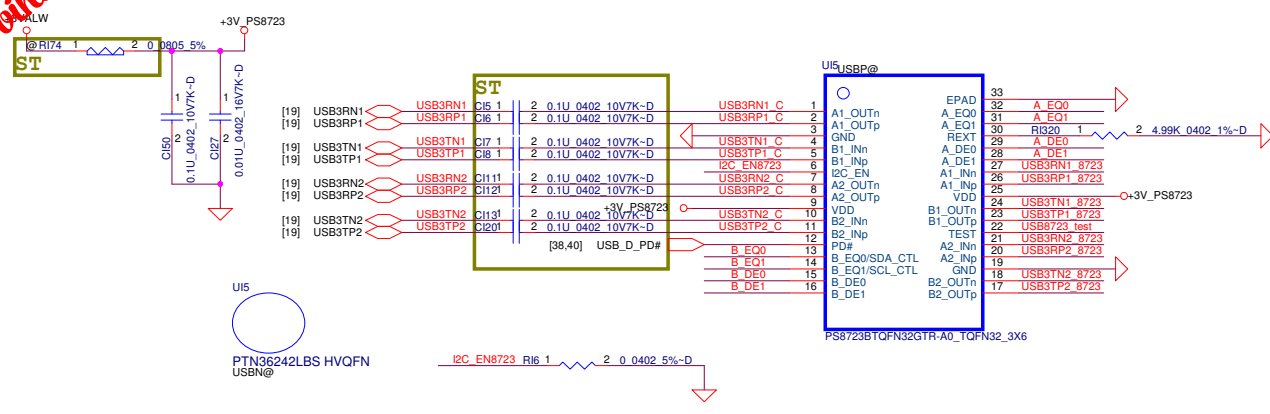
<http://vinafix.vn>

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Size	Document Number	Rev		
Custom	LA-7851P	0.1		
Date:	Tuesday, September 03, 2013	Sheet	43	of 62

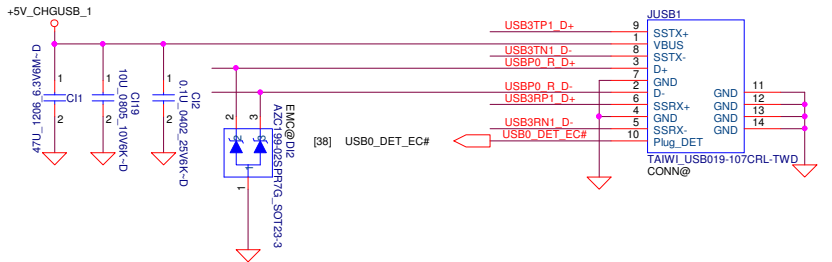
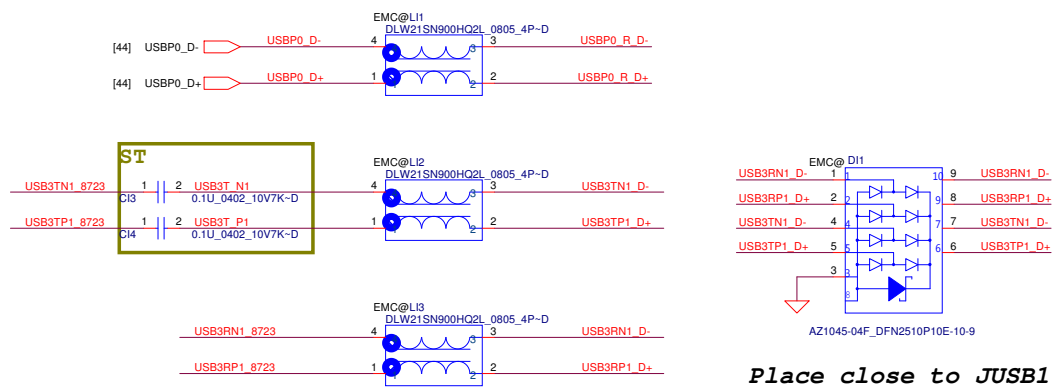


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Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	USB Powershare	
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				LA-7851P		0.1
				Date: Tuesday, September 03, 2013		Sheet 44 of 62

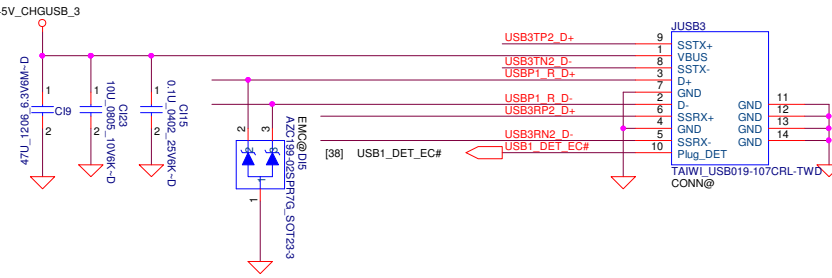
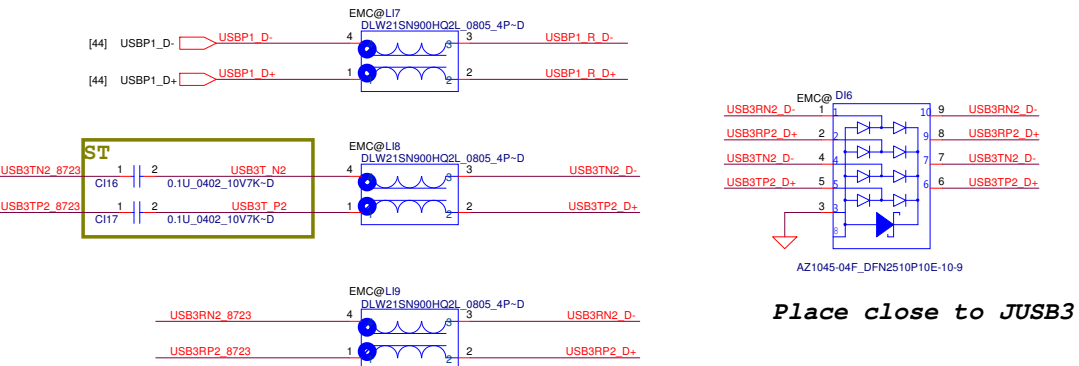
USB3.0 Re-driver



USB3.0 / USB2.0 Port1



USB3.0 / USB2.0 Port3



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Issued Date		2011/08/25		Deciphered Date		2012/07/25	
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				Document Number		LA-7851P	
				Date:		Tuesday, September 03, 2013	
				Sheet		45 of 62	
				Rev		0.1	

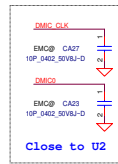
http://vinafix.vn



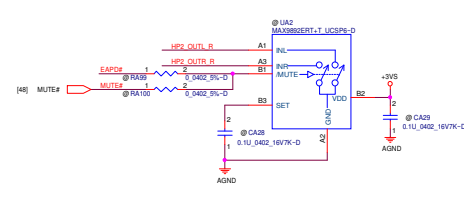
Deciphered Date 2012/01/25

RTC *runner/Green Clock*

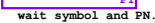
<http://vinafix.vn>



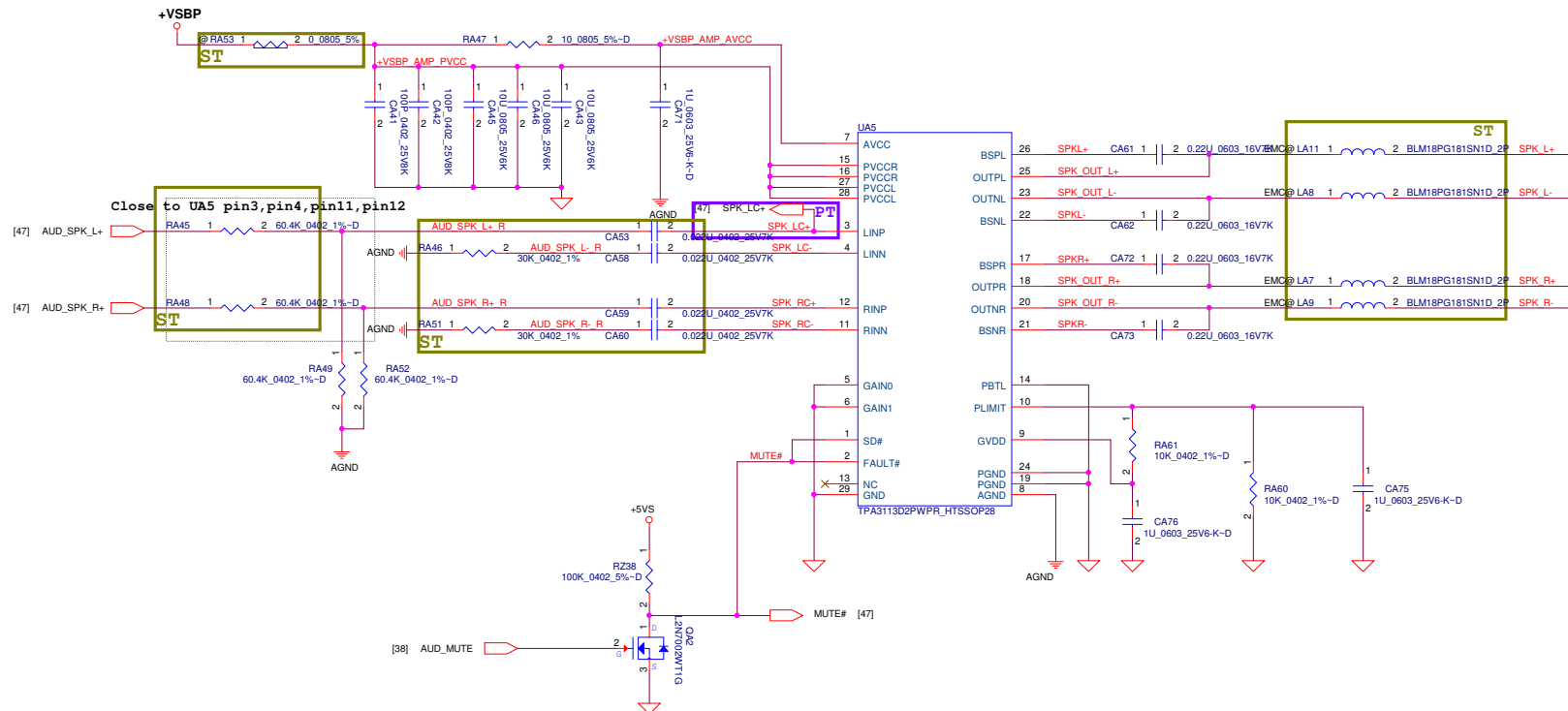
For De-pop noise



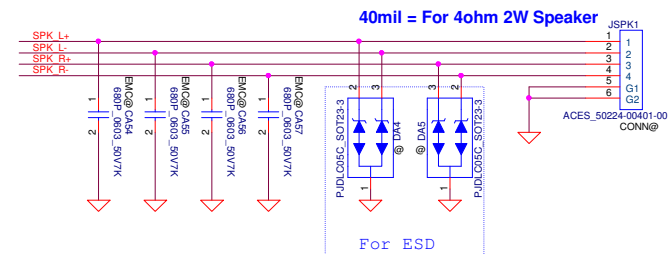
HeadPhone / Mic. combo JACK



Security Classification	Compul Secret Data		Compul Electronics, Inc.	
Issued Date	2011/06/25	Deciphered Date	2012/07/25	Title
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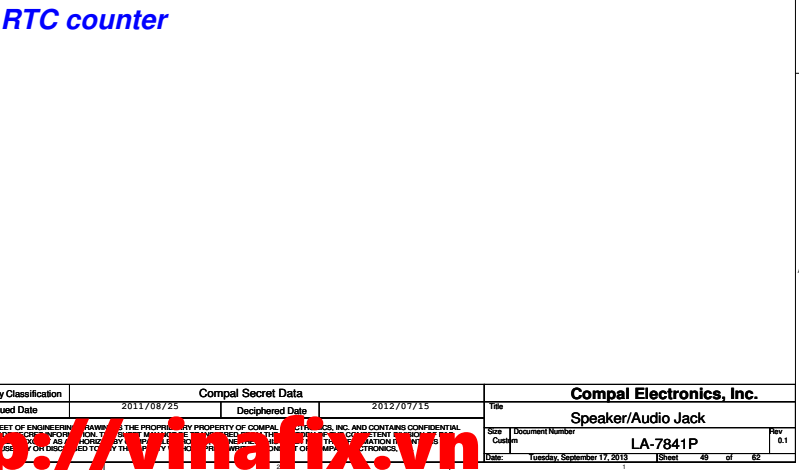
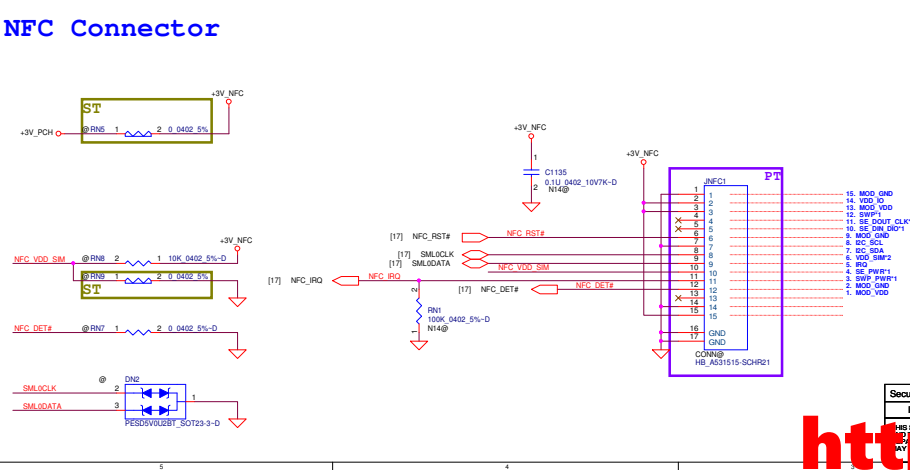
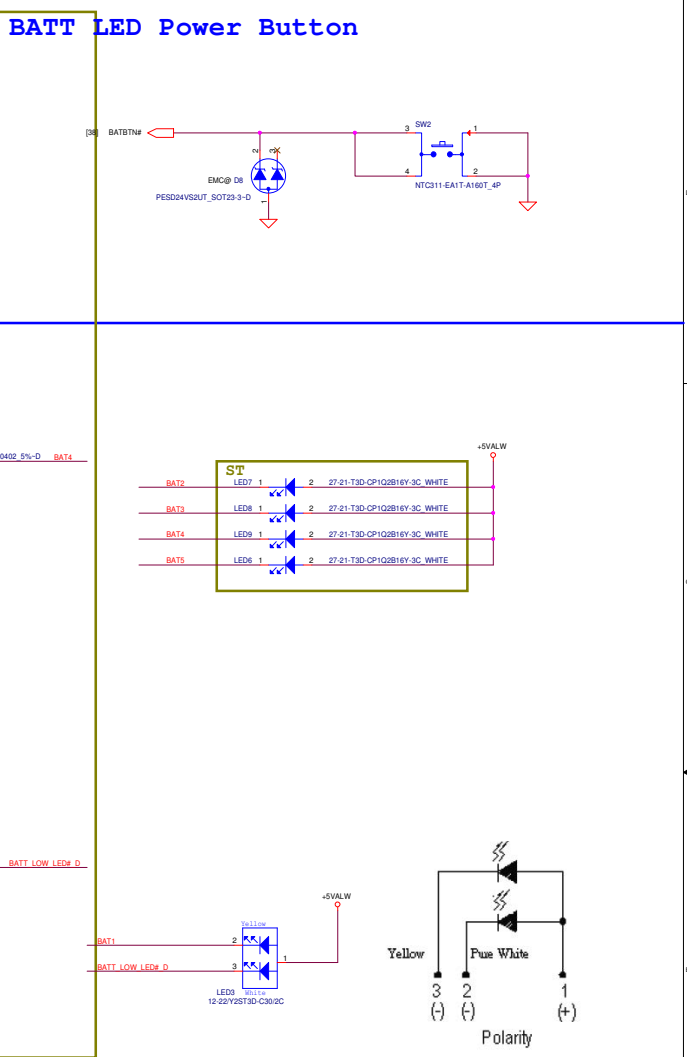
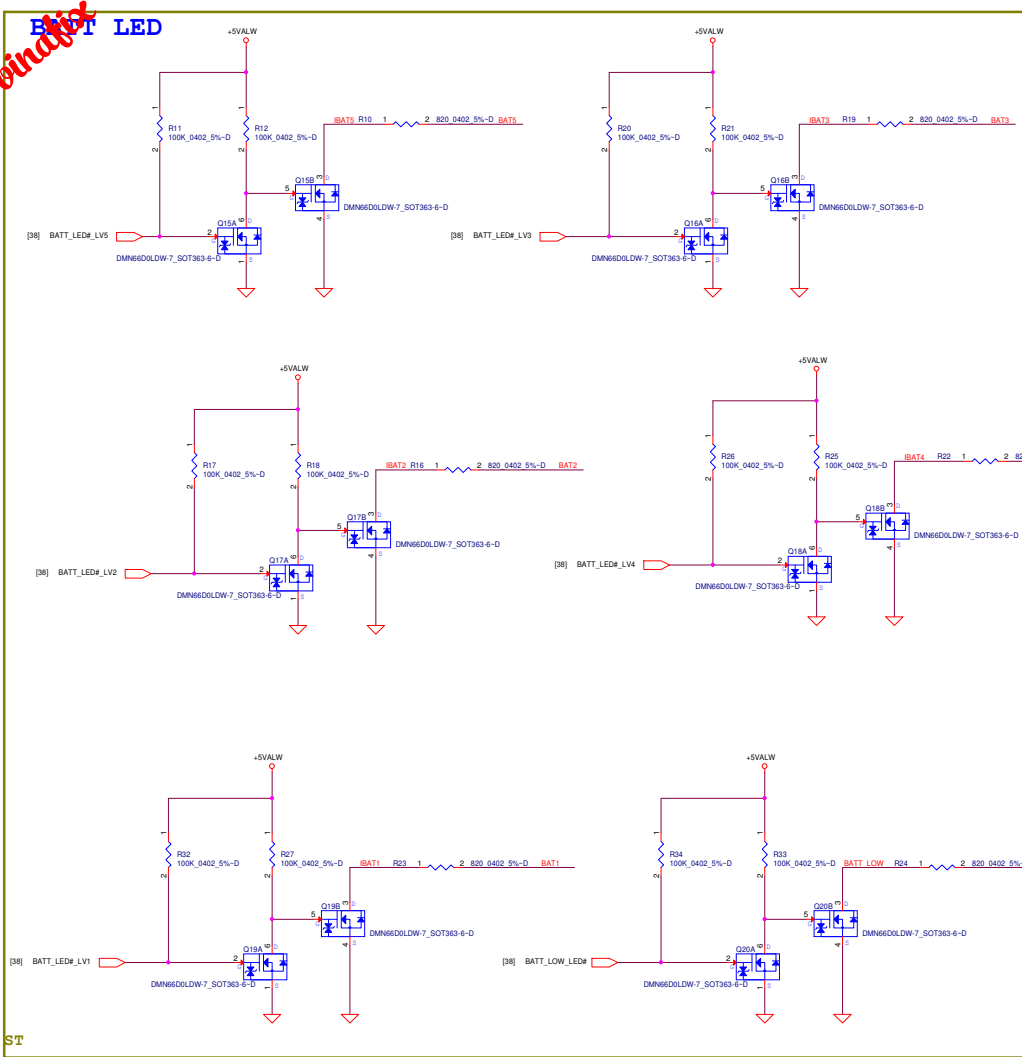


Int. Speaker Conn.



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Issued Date	2011/08/25	Deciphered Date	2012/07/21	Title	Speaker/Audio Jack
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http://vinafix.vn				Date	Tuesday, September 03, 2013
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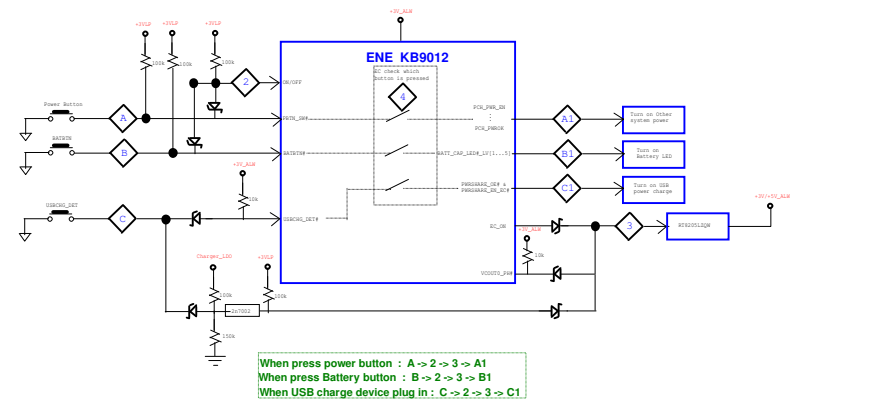
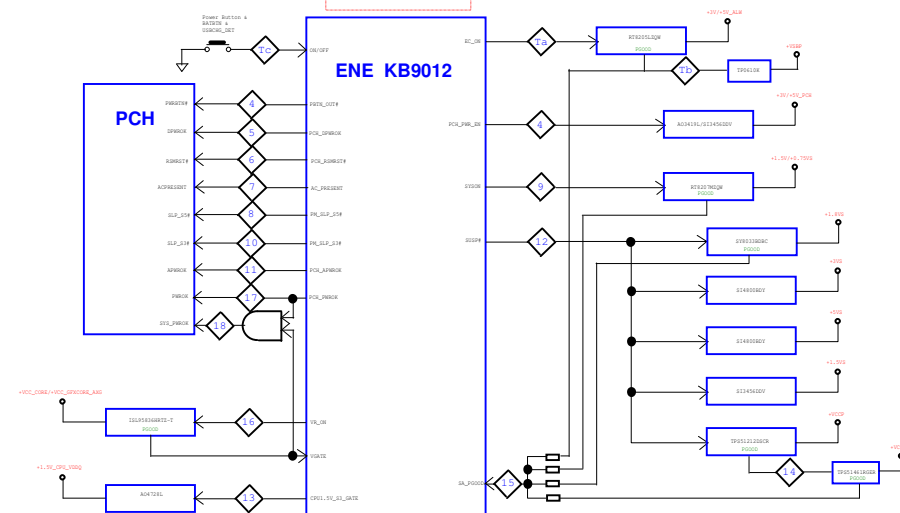
winafix



<http://winafix.vn>

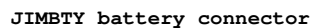
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Issued Date	2011/08/25	Deciphered Date	2012/07/15	Doc Number	LA-7841P
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Module	REV	Change List	From	To
vinafix	1	Initial release	1.0	1.0
	2	Initial release	1.0	1.0
	3	Initial release	1.0	1.0
	4	Initial release	1.0	1.0
	5	Initial release	1.0	1.0
vinafix	6	Initial release	1.0	1.0
	7	Initial release	1.0	1.0
	8	Initial release	1.0	1.0
	9	Initial release	1.0	1.0
	10	Initial release	1.0	1.0
vinafix	11	Initial release	1.0	1.0
	12	Initial release	1.0	1.0
	13	Initial release	1.0	1.0
	14	Initial release	1.0	1.0
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vinafix	16	Initial release	1.0	1.0
	17	Initial release	1.0	1.0
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vinafix	21	Initial release	1.0	1.0
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vinafix	26	Initial release	1.0	1.0
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vinafix	31	Initial release	1.0	1.0
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vinafix	41	Initial release	1.0	1.0
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	45	Initial release	1.0	1.0
vinafix	46	Initial release	1.0	1.0
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vinafix	56	Initial release	1.0	1.0
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vinafix	61	Initial release	1.0	1.0
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vinafix	96	Initial release	1.0	1.0
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	99	Initial release	1.0	1.0
	100	Initial release	1.0	1.0



<http://vinafix.vn>

CONN@ ADP100
ACES 50290-00701-001



**SMART
Battery:**
01.BAT+
02.BAT+
03.BAT+
04.BAT+
05.CLK_SMB
06.DAT_SMB
07.BATT_PRS
08.SYS_PRS
09.GND
10.GND
11.GND
12.GND

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Title **PWR-DCIN / BATT CONN / OTP**

Size	Document Number
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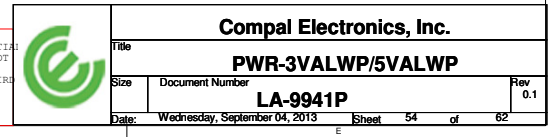
LA-9941P

Rev	
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http://vinafix.vn



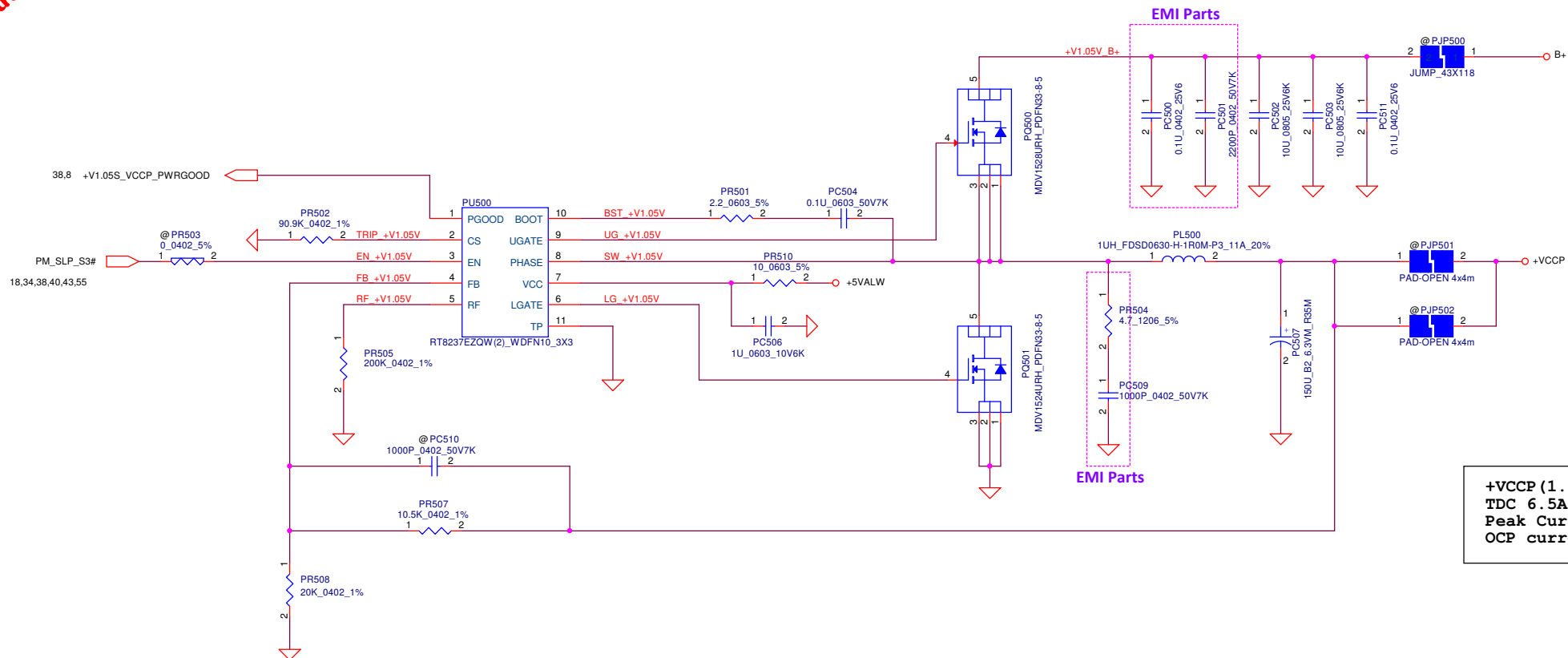
1.35Volt +/- 5%
TDC 7.2A
Peak Current 10.2A
OCP current 12.2A

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.1A



Compal Electronics, Inc.			
Title +1.35V MEN/+0.675V DDR VTT			
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vinafix



+VCCP (1.05V)
TDC 6.5A
Peak Current 9.2A
OCP current 11.1A

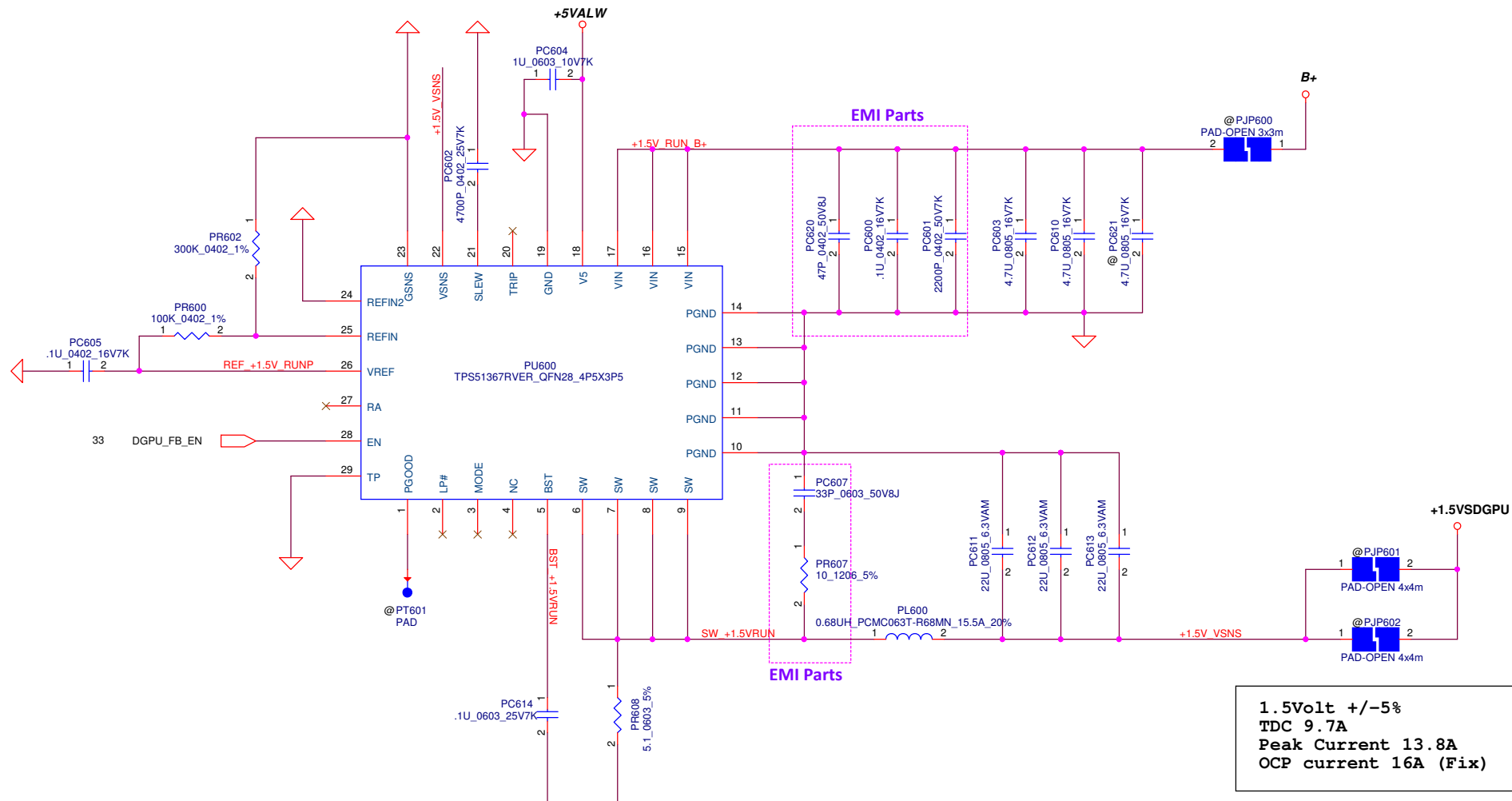
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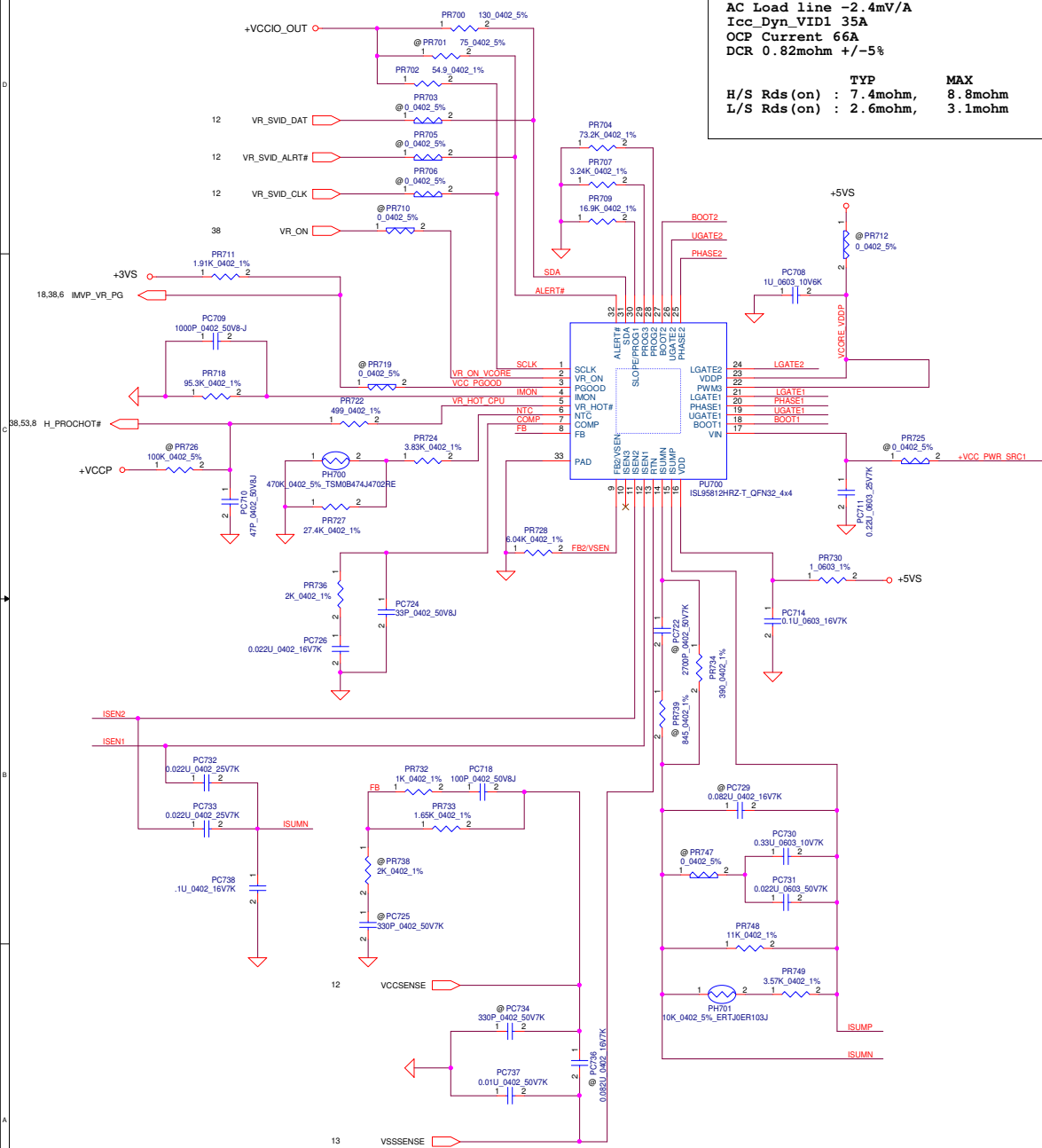


Compal Electronics, Inc.			
Title		PWR +1.5VRUN	
Size	Document Number		Rev
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Date:	Wednesday, September 04, 2013	Sheet	57 of 62

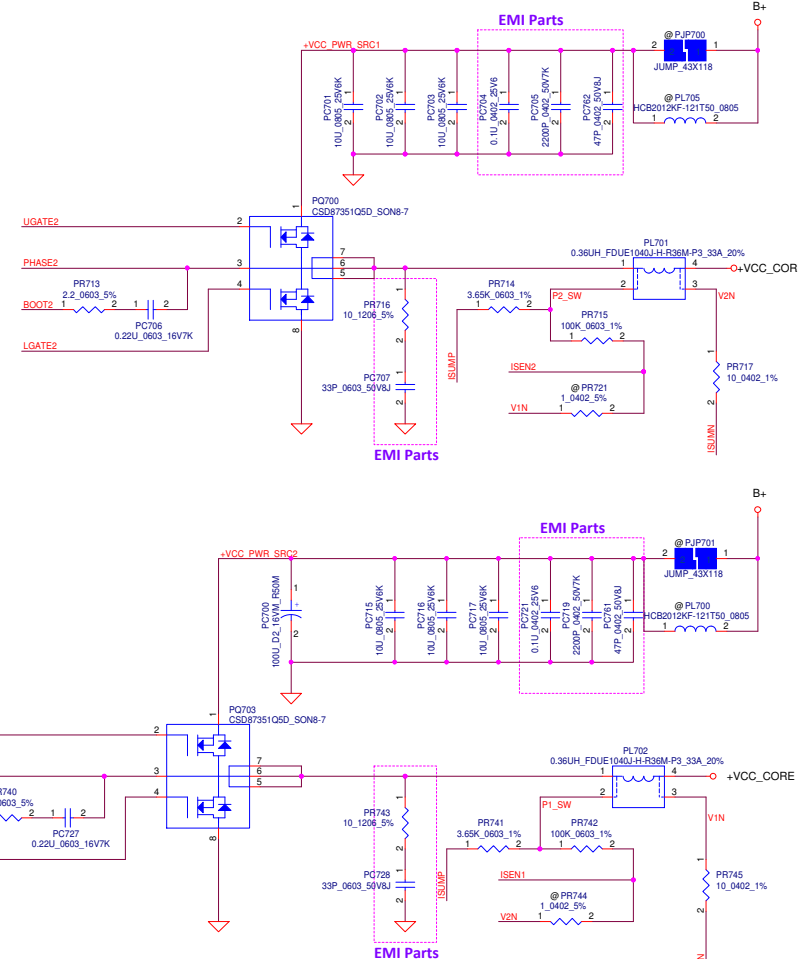
vinafix

VCC_core (Base on PDDG rev 1.0)(1.8V)
TDC 21A
TDC PL2 (40Sec):26A
Peak Current 55A
DC Load line -1.5mV/A
AC Load line -2.4mV/A
Icc_Dyn_VID1 35A
OCP Current 66A
DCR 0.82mohm +/-5%

H/S Rds(on) : 7.4mohm, 8.8mohm
L/S Rds(on) : 2.6mohm, 3.1mohm



Local sense put on HW site

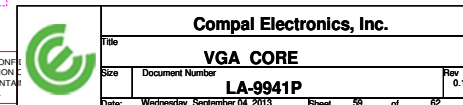


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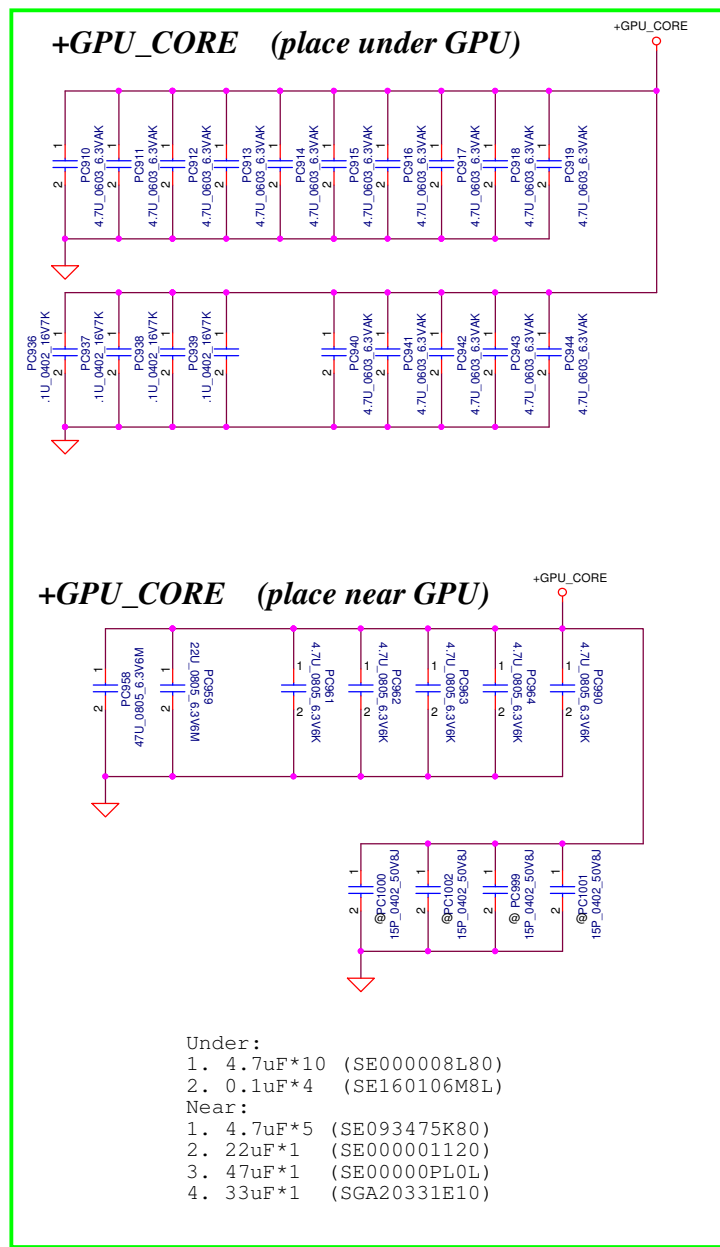
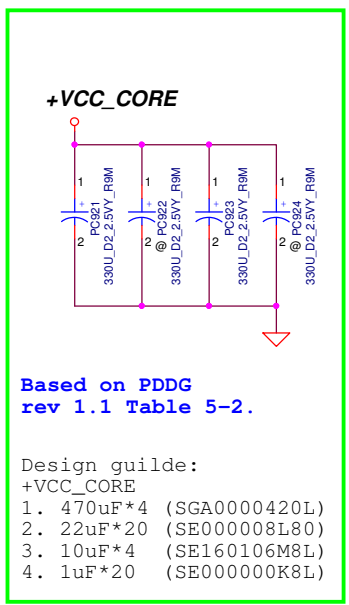
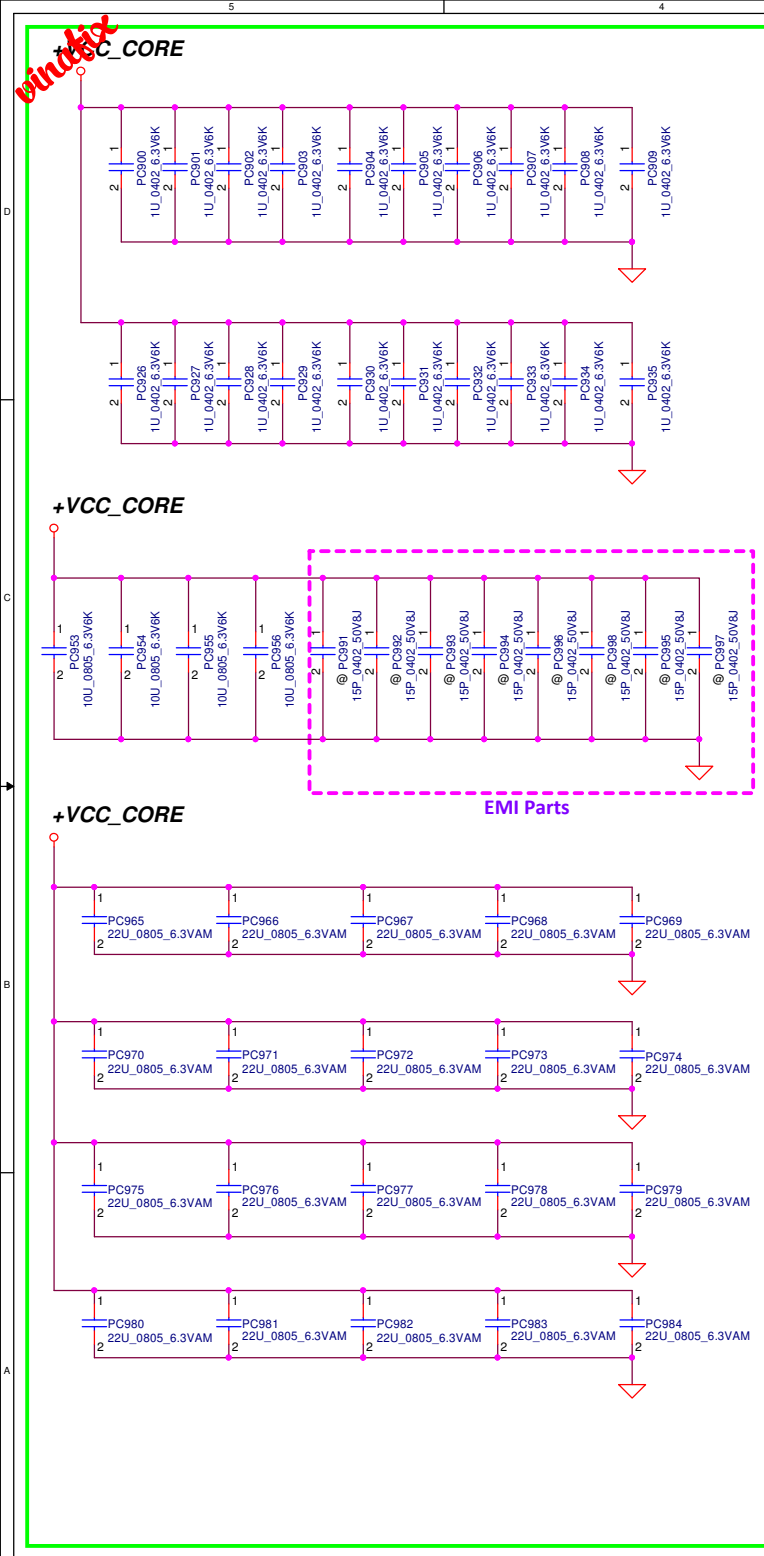
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Compal Electronics, Inc.	
+VCC CORE	
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	TYP	MAX
H/S Rds (on) :	7.4mohm	8.1mohm
L/S Rds (on) :	2.6mohm	3.1mohm



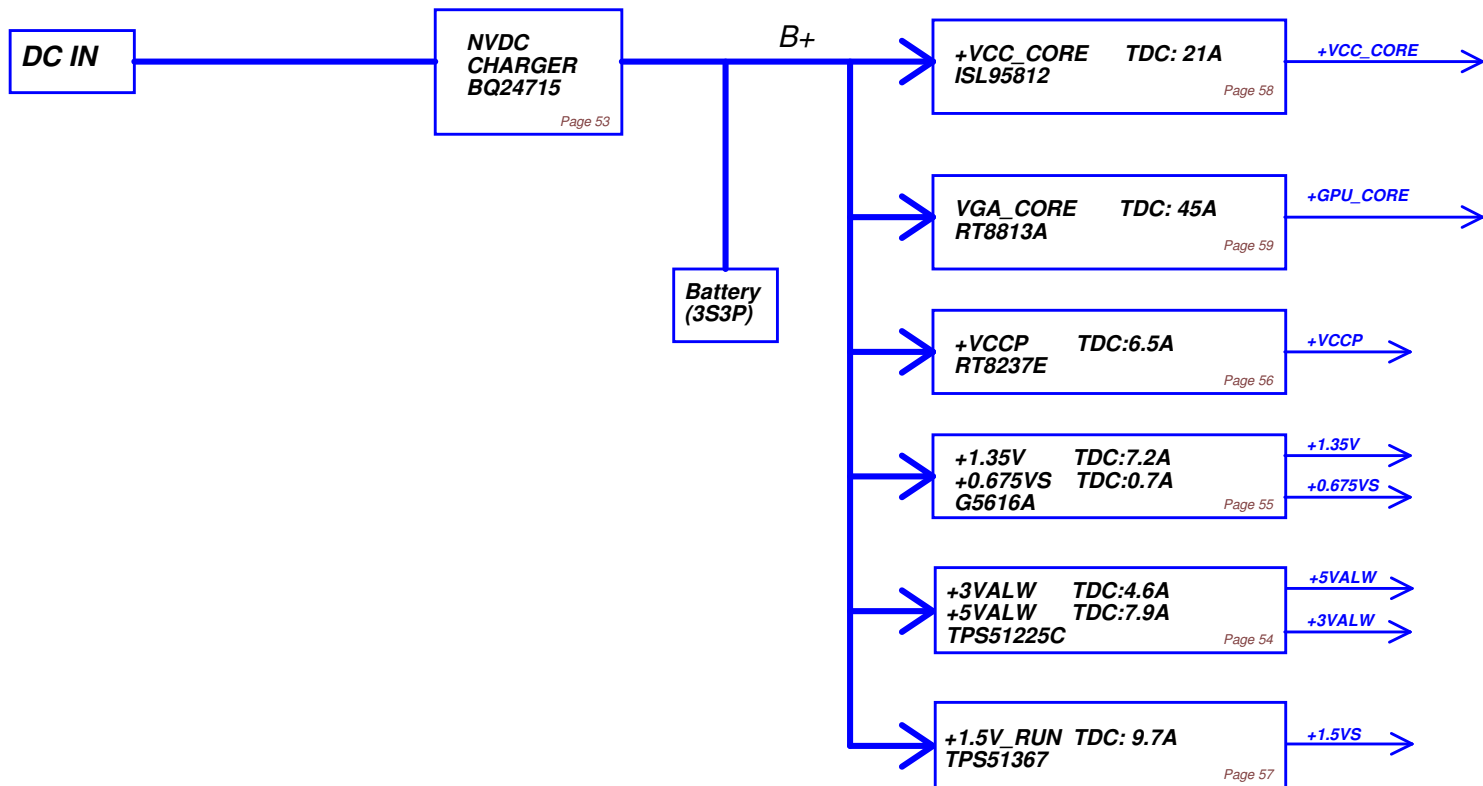
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	Title			
	POWER BLOCK DIAGRAM			
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[AC in]

[Battery only, AC absent]

EC pay attention timing

Discrete Power On Sequence

[AC in]

[Battery only, AC absent]

ITEM	Measure Point	Time
Ta	B+	To
Tb	ACIN	To
Tc	+3VLP	To
Td	EC_ON	To
Te	+5VALW	To
Tf	+3VALW	To
Tg	+VSBP	To
Tg	PBTN_SW#	Low pulse width

ITEM	Measure Point	Time
Ta	B+	To
Tb	ACIN	To
Tc	PBTN_SW#	Low pulse width
Td	EC_ON	To
Te	+3VLP	To
Tf	+5VALW	To
Tg	+3VALW	To
Tg	+VSBP	To

ITEM	Measure Point	Time
T1	PBTN_SW#	To
T2	PCH_PWR_EN	To
T3	+3V_PCH	To
T4	PCH_DPWRK	To
T5	PCH_RSMRST#	To
T6	SUSCLK	To
T7	AC_PRESENT	To
T8	PBTN_OUT#	To
T9	PM_SLP_S4#	To
T10	WLAN_EN	To
T11	PM_SLP_S4#	To
T12	SYSON	To
T13	+1.5V	To
T14	PM_SLP_S4#	To
T15	PM_SLP_S3#	To
T16	SUSP#	To
T17	SUSP#	To
T18	SUSP#	To
T19	SUSP#	To
T20	+1.8VS	To
T21	SUSP#	To
T22	+VCCP	To
T23	+VCCP	To
T24	+VCCSA	To
T25	SA_PGOOD	To
T26	CPU1.5V_S3_GATE	To
T27	CPU1.5V_S3_GATE	To
T28	CPU1.5V_S3_GATE	To
T29	+0.75VSP	To
T30	HWP	To
T31	HWP	To
T32	PCH_PWRK	To
T33	PM_DRAM_PWRGD	To
T34	VR_ON	To
T35	H_CUPWRGD	To
T36	+VCC_CORE	To
T37	VGATE	To
T38	SYS_PWRK	To
T39	SUSP#	To
T40	DGPU_PWREN	To
T41	DGPU_PWREN	To
T42	DGPU_PWREN	To
T43	DGPU_PWREN	To

GPU power on sequence

