

Compal confidential

Schematics Document

Calypso 13.3"

Mobile AMD S1G2 CPU with ATI RS780M(NB) & SB700(SB) core logic

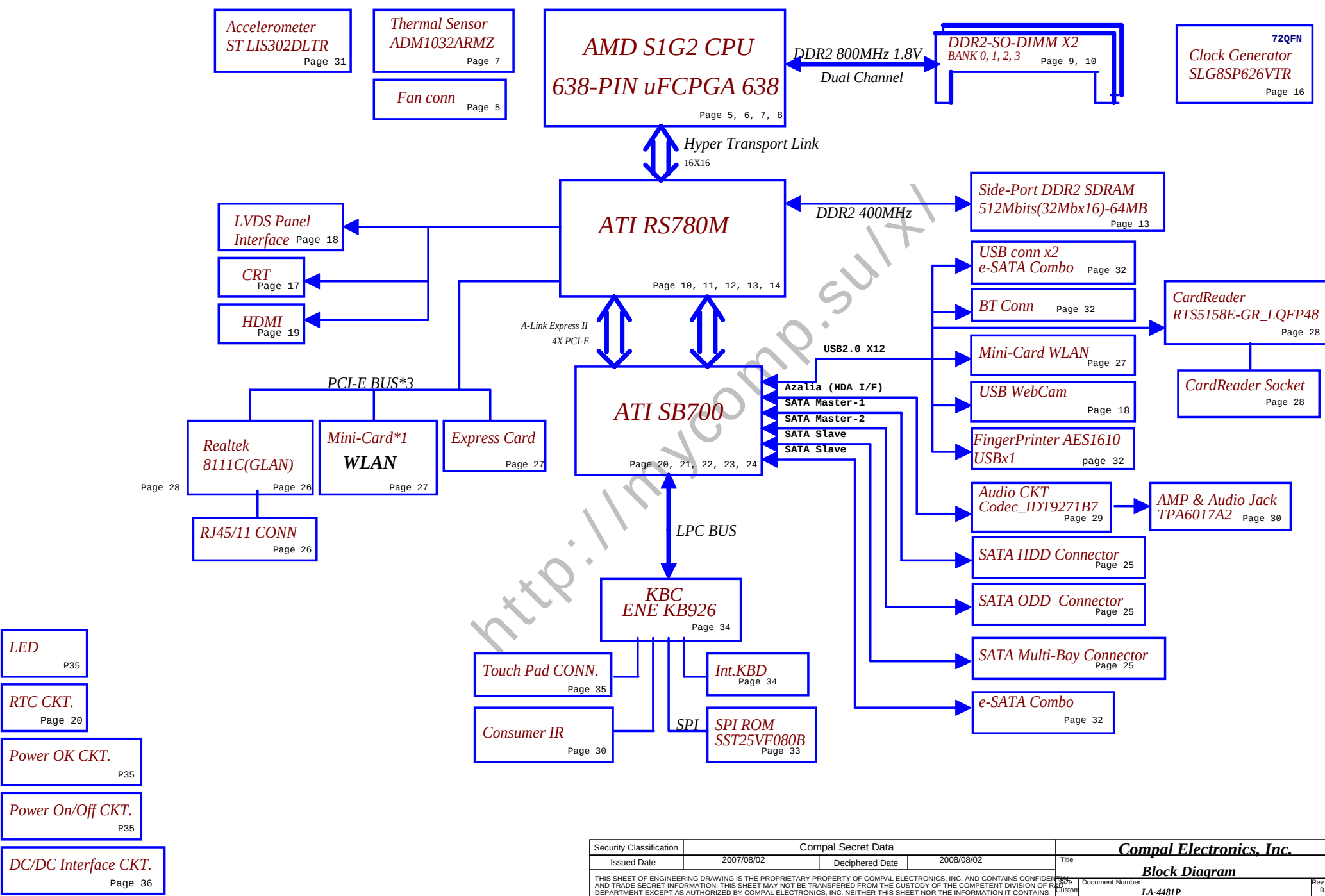
2008-09-04

LA-4481P REV:0.4



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Consumer AMD 13.3" UMA - Sally



Voltage Rails

0 MEANS ON X MEANS OFF

power plane				+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +VGA_CORE +2.5VS +1.8VS +1.2VS +0.9VGA
State	+B	+5VALW +3VALW	+1.8V	
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

EC SM Bus1 address

EC SM Bus2 address

Device	HEX	Address	Device	HEX	Address
Smart Battery	16H	0001 011X b	CPU	98H	1001 100X b
24C16	A0H	1010 000X b	ADI1032-2 CPU	9AH	1001 101X b

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

Layout Notes

UMA@ : means for RS780M.
Please see VGA@ as no install. No support RX780M.

11/14 update

 : Question Area Mark.(Wait check)

USB assignment:

USB-0 Right side
 USB-1 Right side
 USB-2 Left side(with ESATA)
 USB-3 Dock
 USB-4 Camera
 USB-5 WLAN
 USB-6 Bluetooth
 USB-7 Finger Printer
 USB-8 MiniCard(WWAN/TV)
 USB-9 Express card
 USB-10 X
 USB-11 X

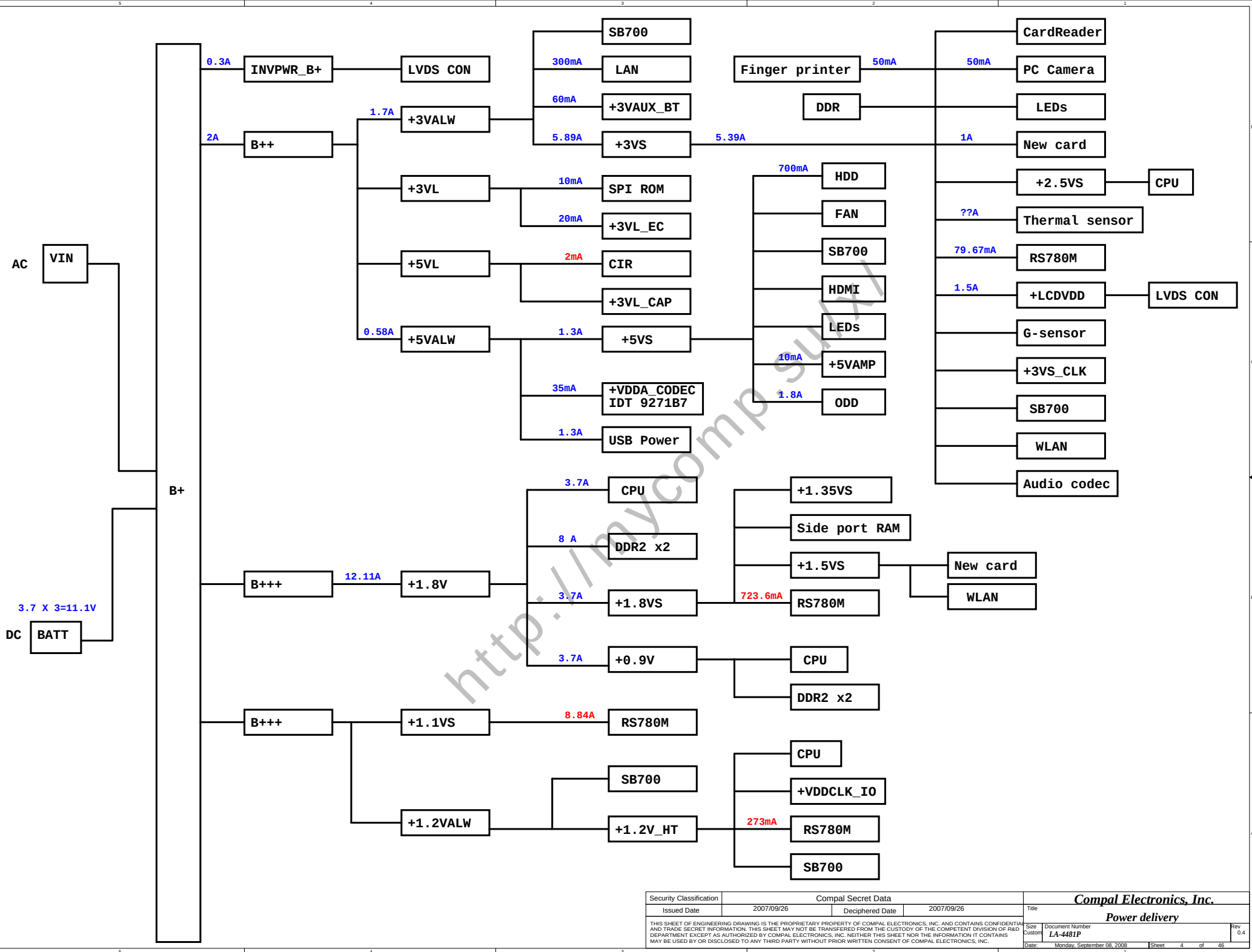
PCIe assignment:

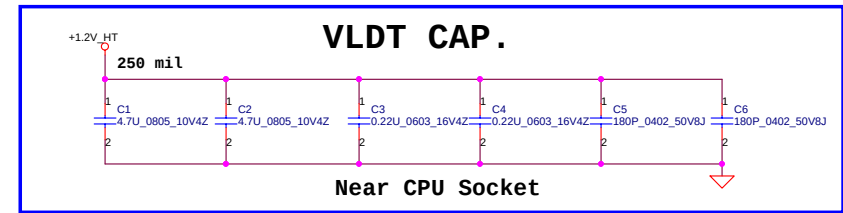
PCIe-1 TV tuner/WWAN/Robeson
 PCIe-2 X
 PCIe-3 WLAN
 PCIe-4 New Card
 PCIe-5 Card reader
 PCIe-6 GLAN (Marvell)

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR CPU & ADM1832	SODIMM I / II	CLK CHIP	MINI_CARD Slot 2	LCD	HDMI	G-Sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X
I2C_CLK I2C_DATA	RS780M	X	X	X	X	X	X	X	V	X	X
DDC_CLK0 DDC_DATA0	RS780M	X	X	X	X	X	X	X	X	V	X
DDC_CLK1 DDC_DATA1	RS780M	X	X	X	X	X	X	X	X	X	X
SCL0 SDA0	SB700	X	X	X	X	V	V	X	X	X	X
SCL1 SDA1	SB700	X	X	X	X	X	X	V	X	X	X
SCL2 SDA2	SB700	X	X	X	X	X	X	X	X	X	V
SCL3 SDA3	SB700	X	X	X	X	X	X	X	X	X	X

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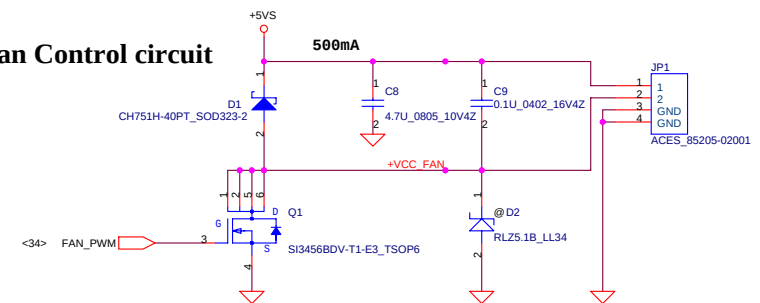
<11> H_CADIP[0..15] H_CADIP[0..15]
 <11> H_CADIN[0..15] H_CADIN[0..15]

H_CADOP[0..15] H_CADOP[0..15] <11>
 H_CADON[0..15] H_CADON[0..15] <11>

If VLDT is connected only on one side, one 4.7uF cap should be added to the island side.

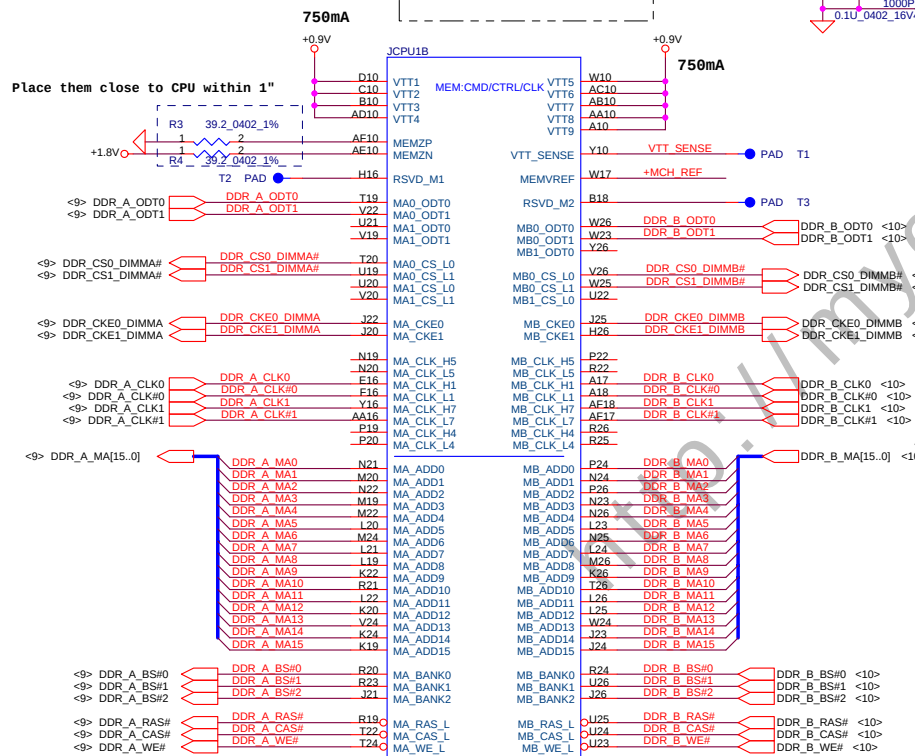
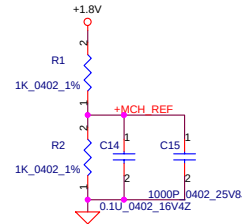
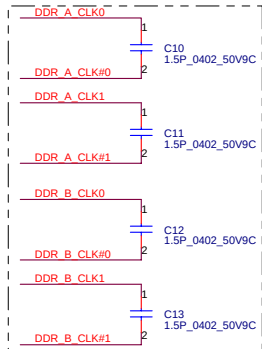
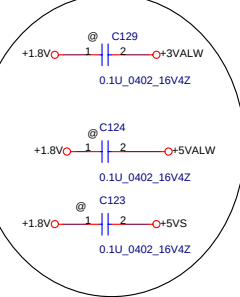


PWM Fan Control circuit



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**PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH**



Athlon 64 S1 Processor Socket

The diagram illustrates the internal architecture of a DDR memory controller, showing the connection between the controller's internal blocks and external DDR memory modules.

Internal Blocks:

- JCPUIFC:** The central interface block, divided into two main sections:
 - Top Section (DDR_B [0:63.0]):** Contains a large array of internal data paths (e.g., D0, D1, D2, ..., D63) and control signals (e.g., C11, C12, C13, ..., C16).
 - Bottom Section (DDR_B_DM [7..0]):** Contains a smaller array of internal data paths (e.g., D0, D1, D2, ..., D6) and control signals (e.g., C12, C13, C14, ..., C16).
- MEMDATA:** The memory data interface block, which receives data from the JCPUIFC and outputs it to the memory modules.

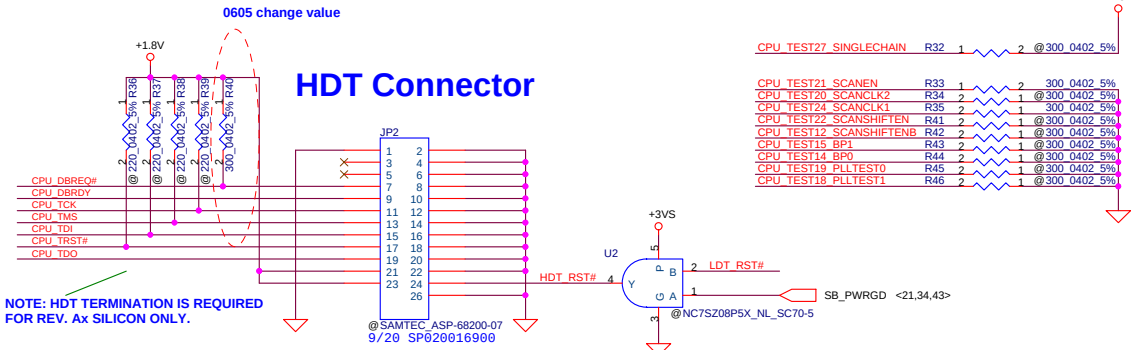
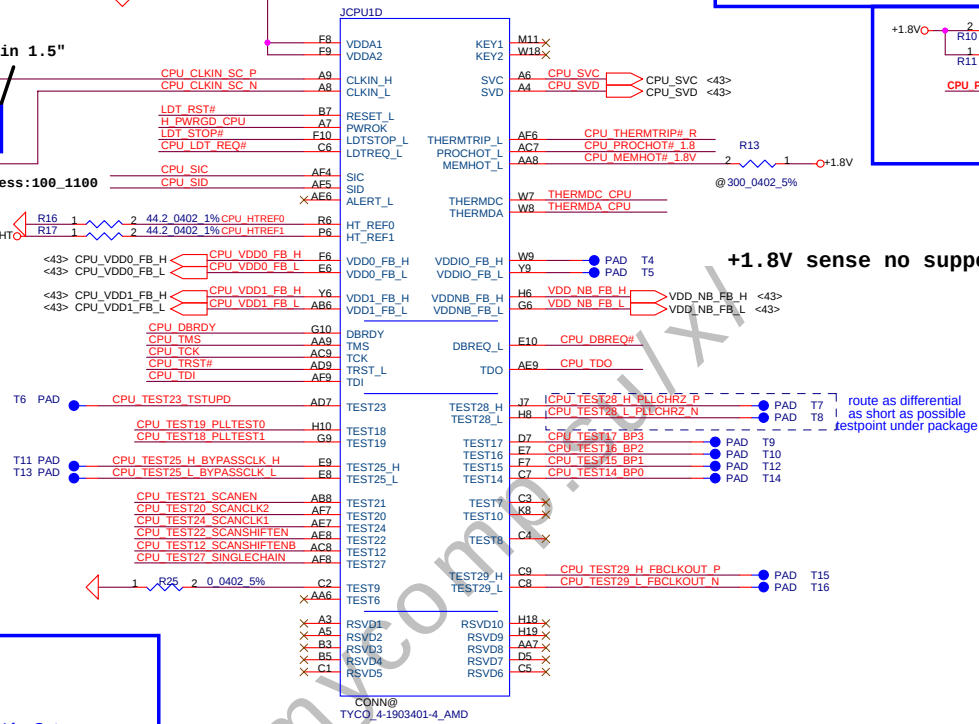
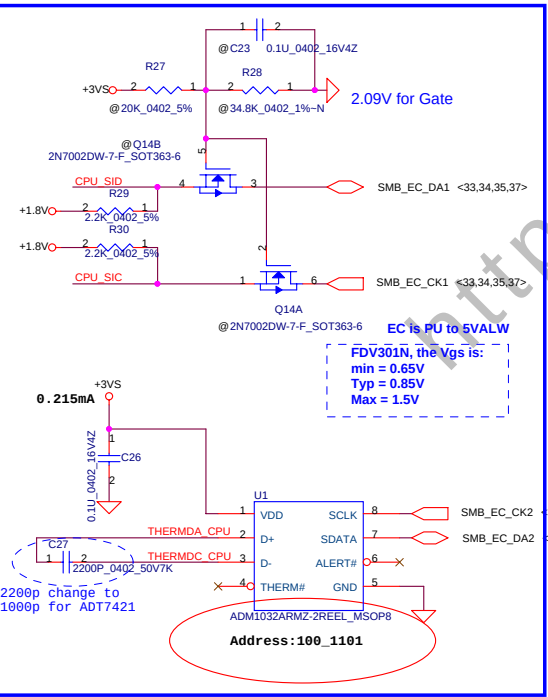
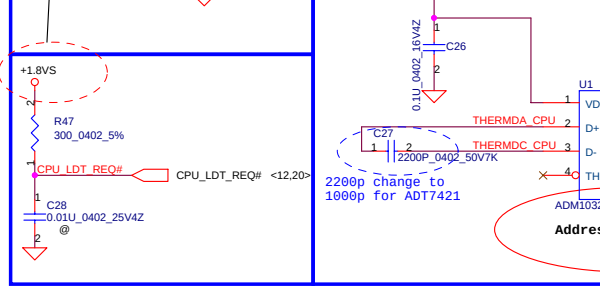
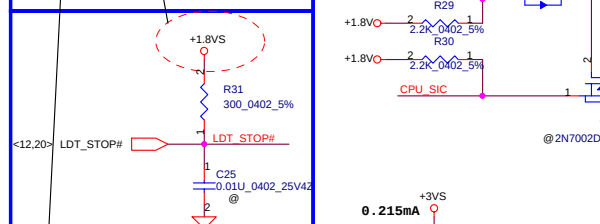
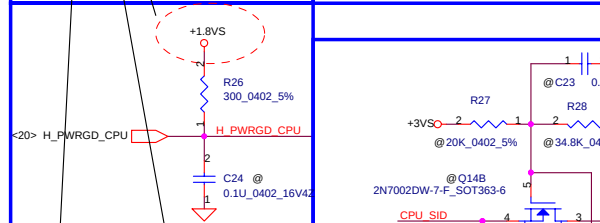
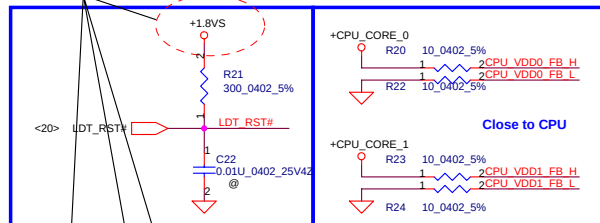
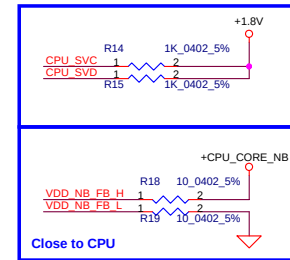
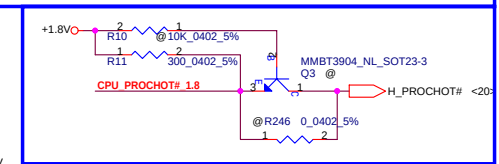
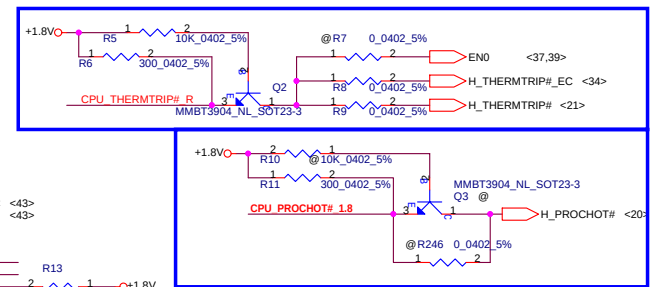
External Connections:

- DDR_B [0:63.0]:** The main data bus, connected to the JCPUIFC and MEMDATA blocks. It includes signals for data (DQ), data strobe (DQS), data mask (DQM), and data sense in (DQSI).
- DDR_B_DM [7..0]:** The data mask bus, connected to the JCPUIFC and MEMDATA blocks. It includes signals for data mask (DQM) and data sense in (DQSI).
- DDR_A [0:63.0]:** The main data bus, connected to the JCPUIFC and MEMDATA blocks. It includes signals for data (DQ), data strobe (DQS), data mask (DQM), and data sense in (DQSI).
- DDR_A_DM [7..0]:** The data mask bus, connected to the JCPUIFC and MEMDATA blocks. It includes signals for data mask (DQM) and data sense in (DQSI).

The diagram shows the internal structure of the controller, including the JCPUIFC and MEMDATA blocks, and their connections to the external DDR memory modules. The diagram is divided into two main sections: the top section for DDR_B [0:63.0] and the bottom section for DDR_B_DM [7..0].

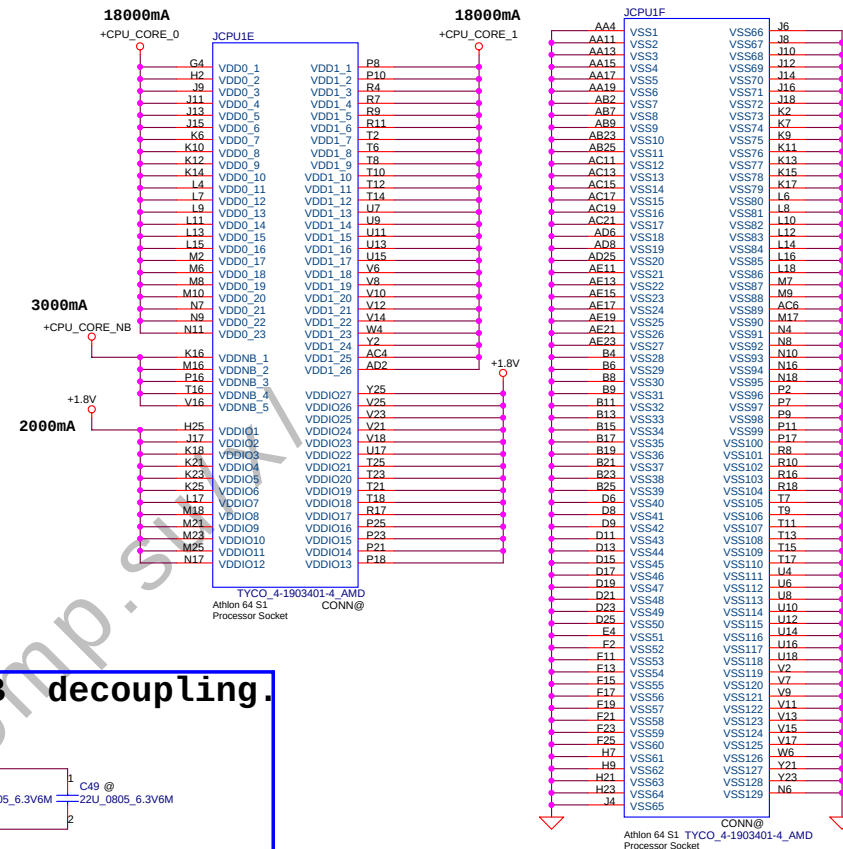
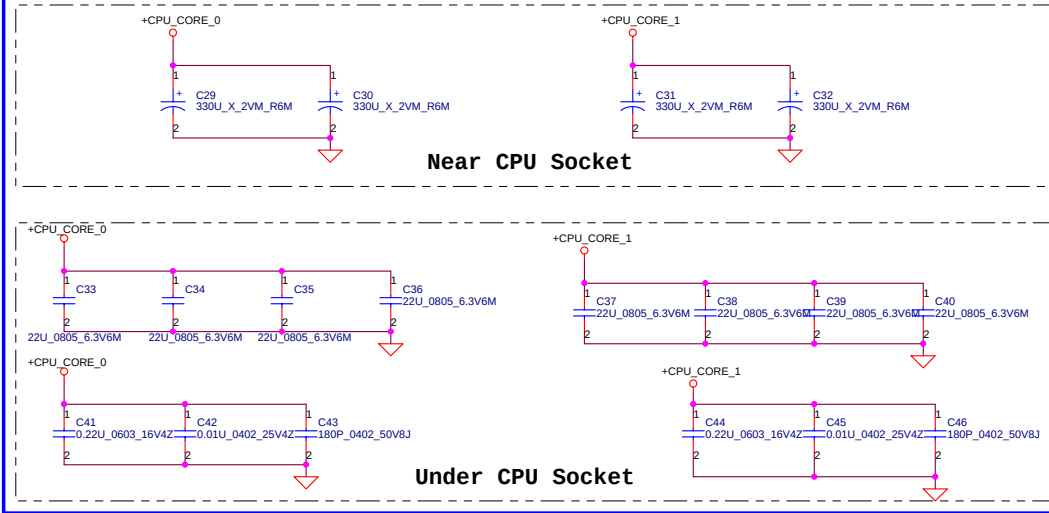
Athlon 64 S1 TYCO_4-1903401-4_AMD
Processor Socket CONN@

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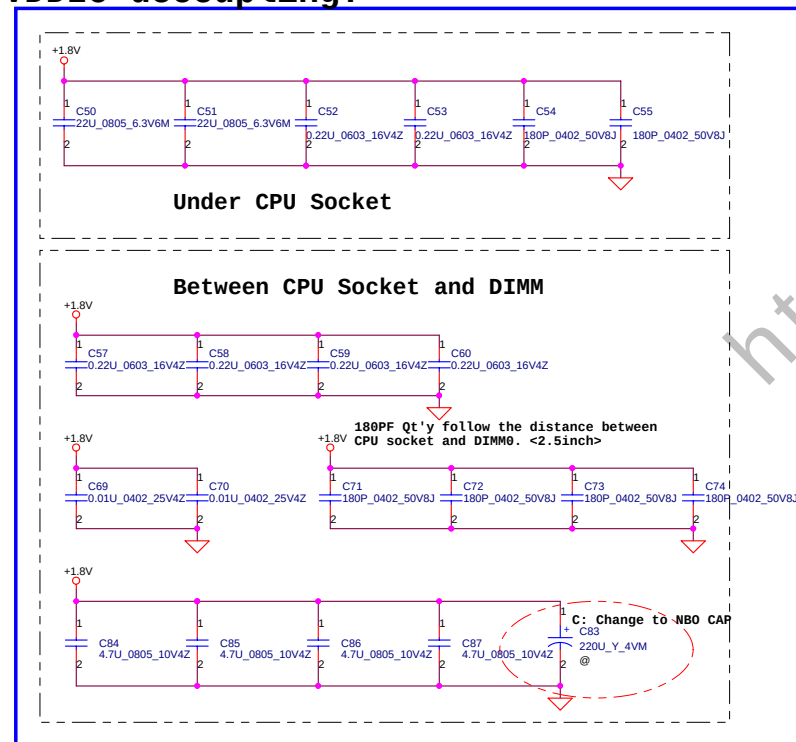


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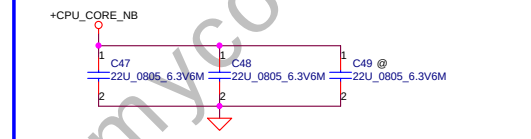
VDD(+CPU_CORE) decoupling.



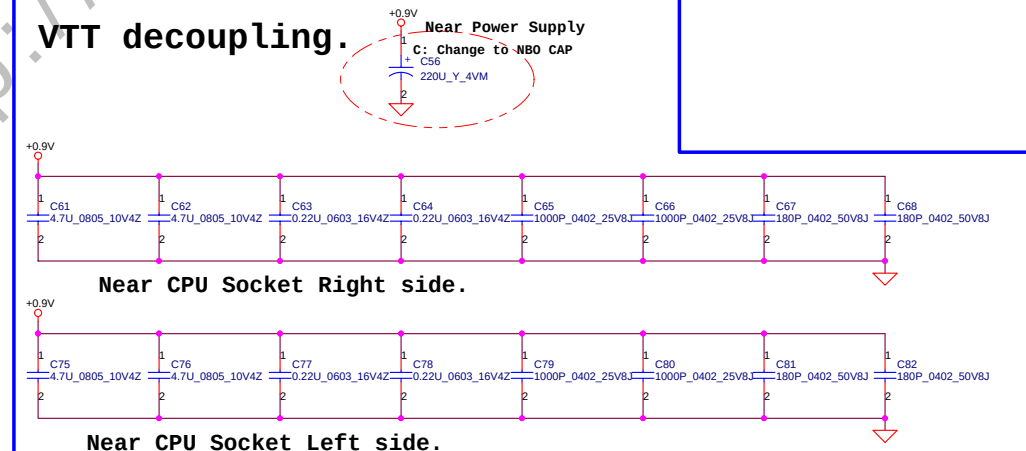
VDDIO decoupling.



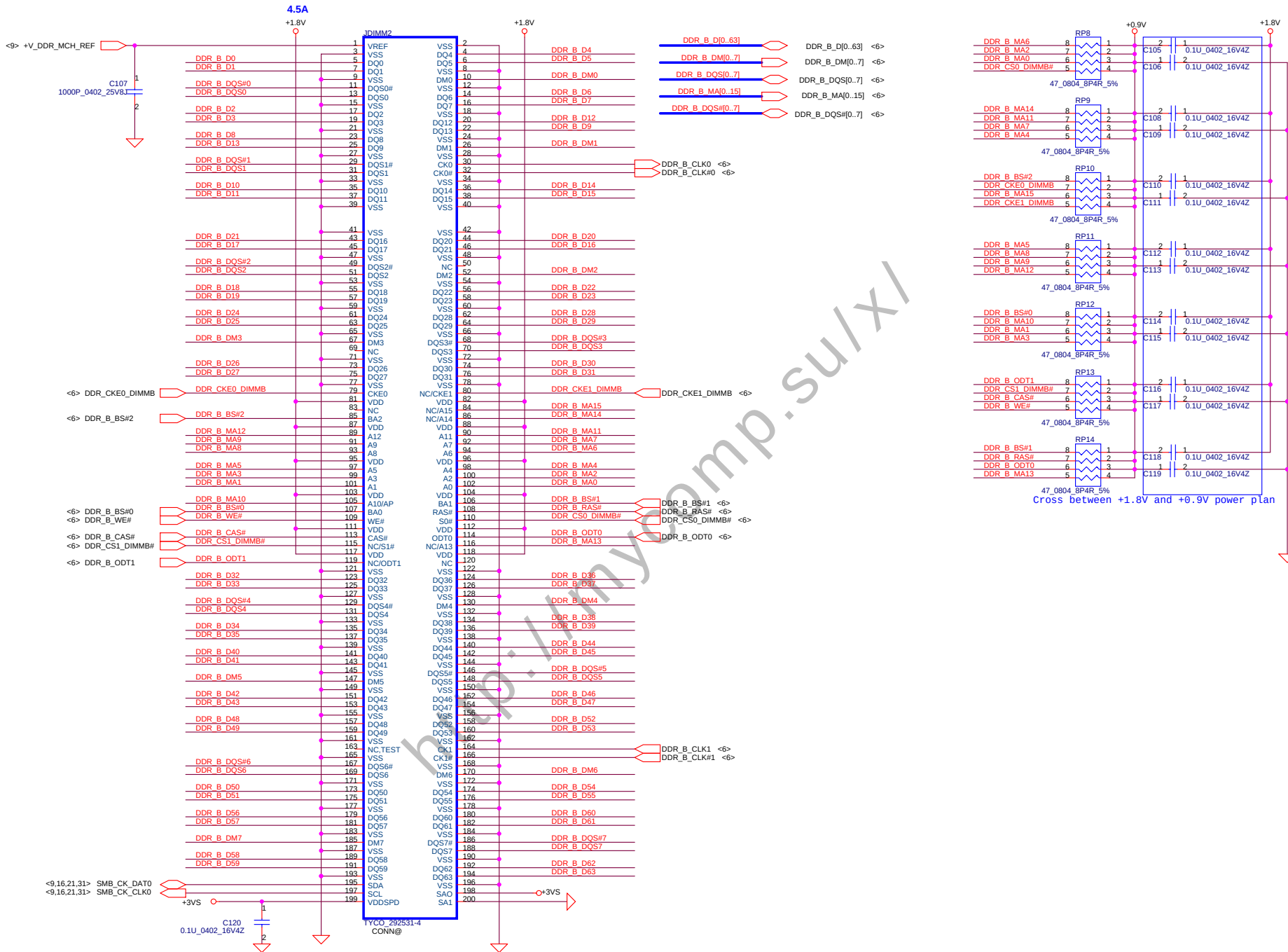
+CPU_CORE_NB decoupling.



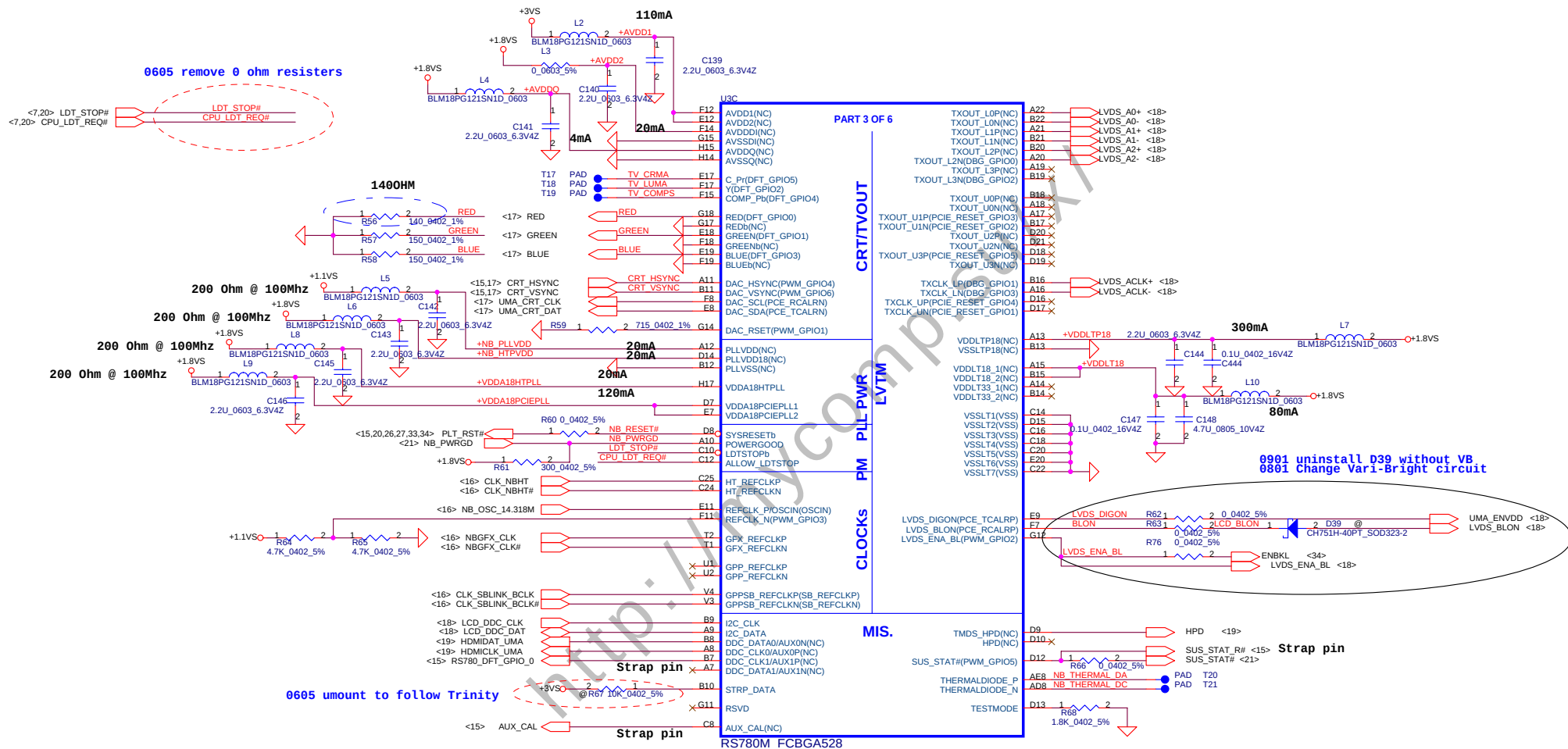
VTT decoupling.



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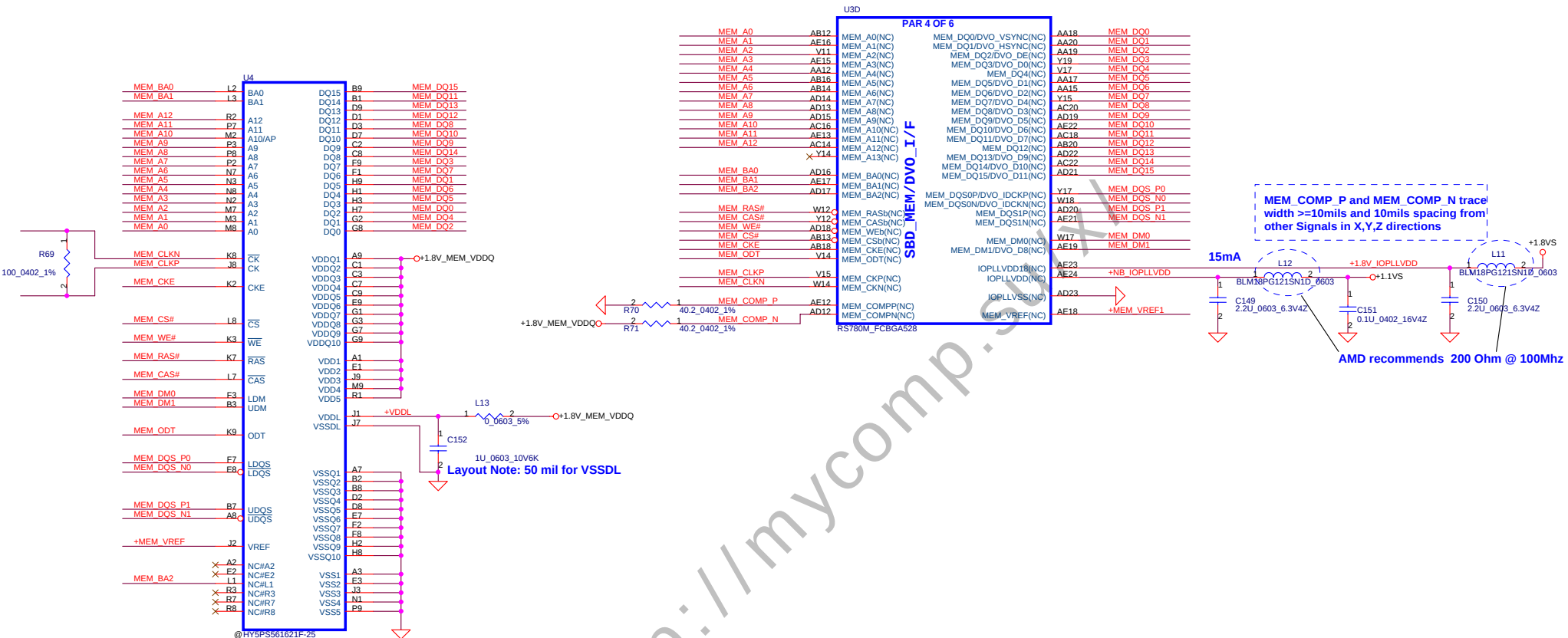


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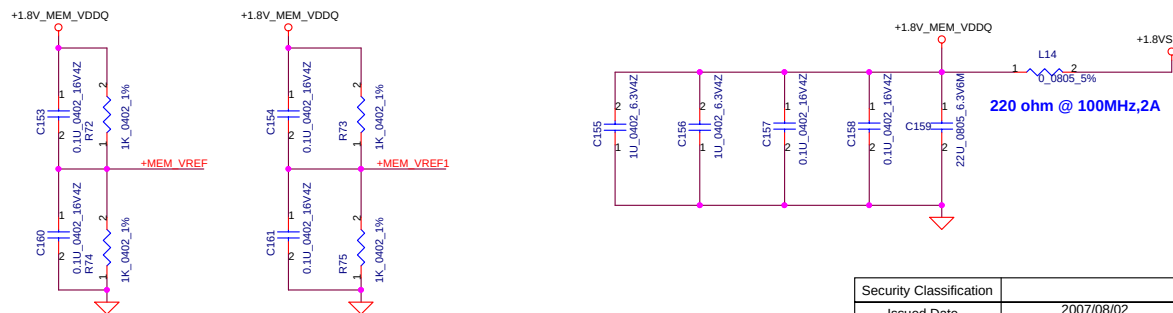


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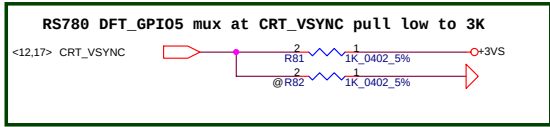
Side-Port DDR2 SDRAM
512Mbits(32Mbx16)-64MB



Side Port disable,VREF need connect to +1.8VS for DDR2



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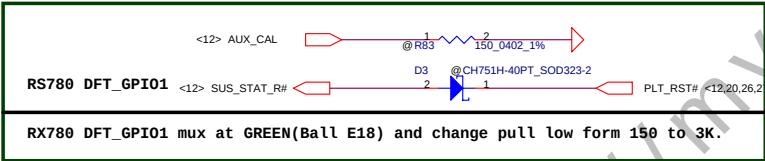
DFT_GPI05:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

1 : Disable (RS740) Disable (RX780, RS780)

0 : Enable (Rs740) Enable (RX780, RS780)

PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#



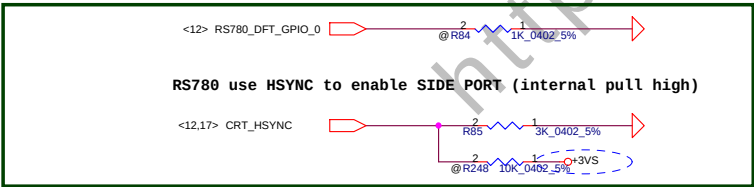
DFT_GPI01: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values

0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS740/RX780: DFT_GPI01 RS780:SUS_STAT



DFT_GPI00: STRAP_DEBUG_BUS_PCIE_ENABLEb

RX780: Enables the Test Debug Bus using PCIE bus

1 : Disable (Can still be enabled using nbcfg register access)

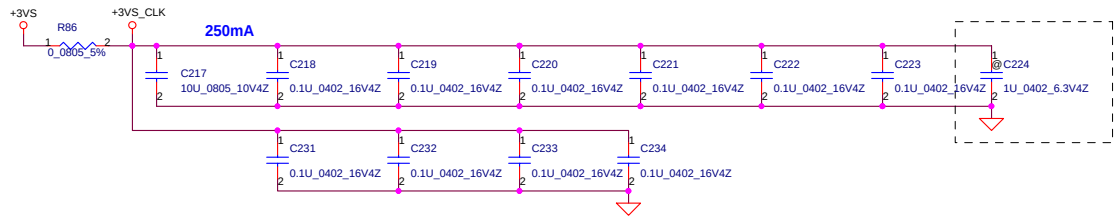
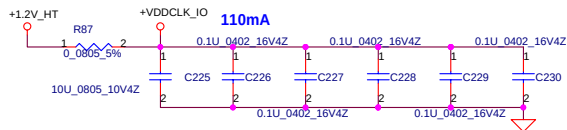
0 : Enable

RS740/RS780: Enables Side port memory (RS780 use HSYNC#)

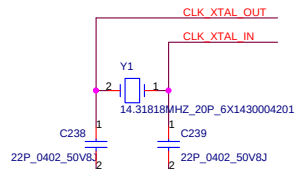
1. Disable (RS740/RS780)

0 : Enable (RS740/RS780)

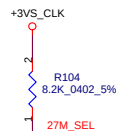
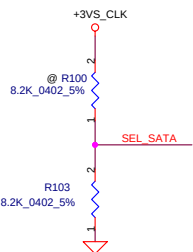
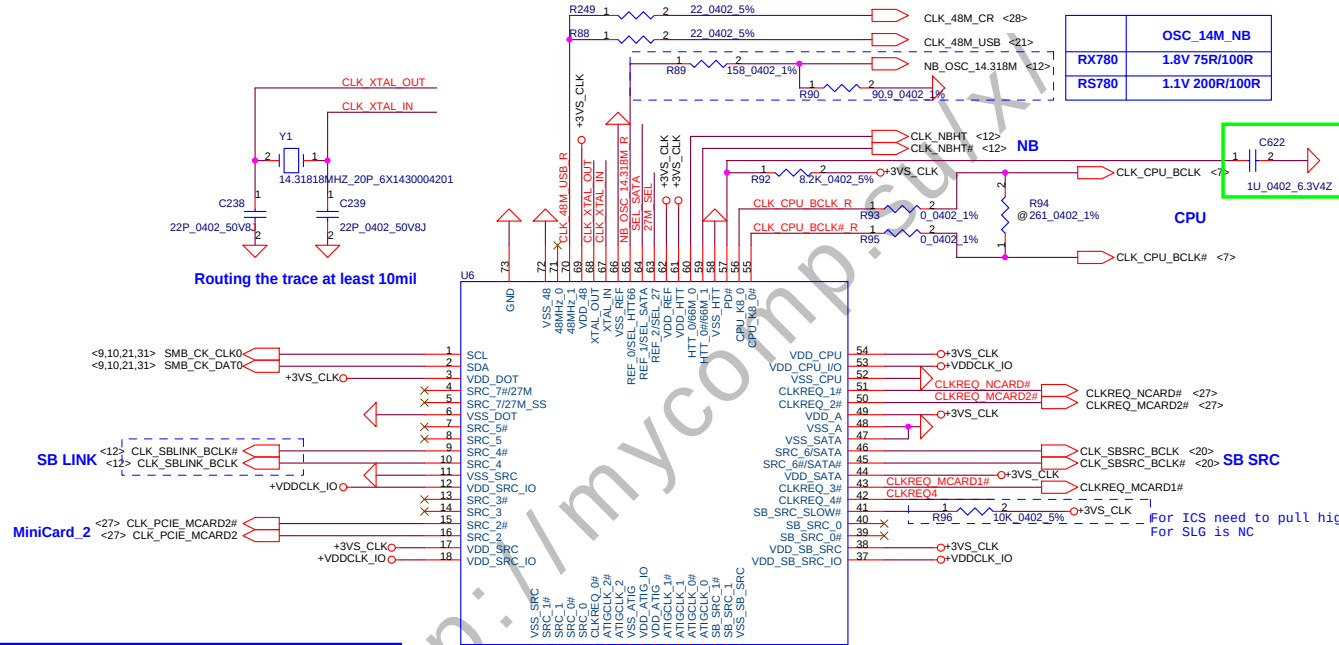
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EMI Caps for single end clock.



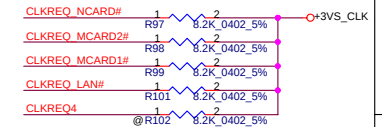
Routing the trace at least 10mil



SEL_SATA	1	configure as SATA output
	0	configure as normal SRC(SRC. 6) output
		* default

Use voltage divider resistor R379 & R380 to pull low

NB_OSC_14.318M	1	configure as single-ended 66MHz output
	0	configure as differential 100MHz output
		* default

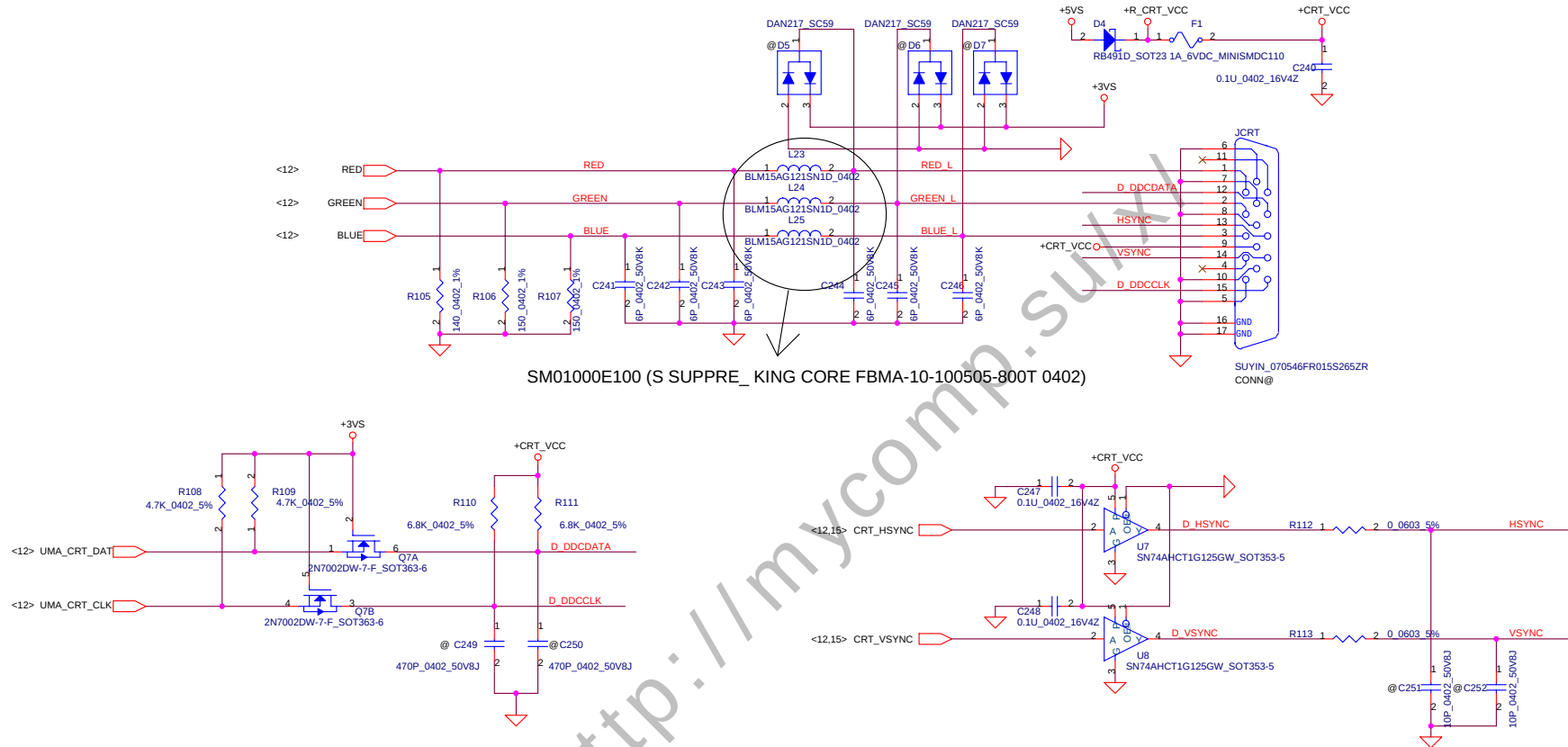


NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*

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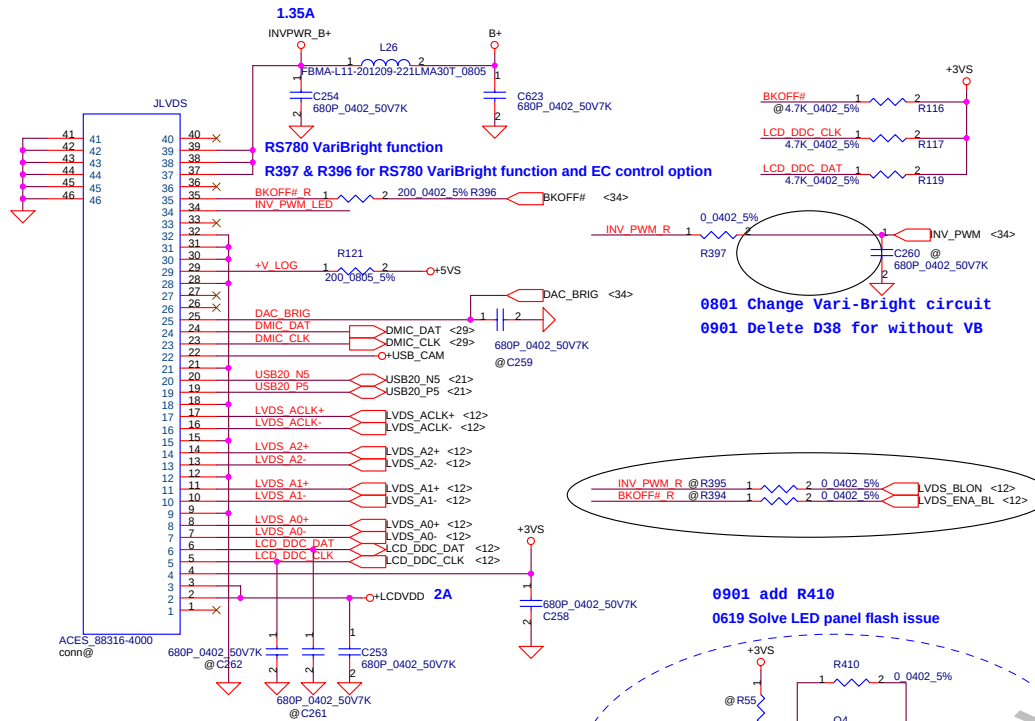
CRT CONNECTOR



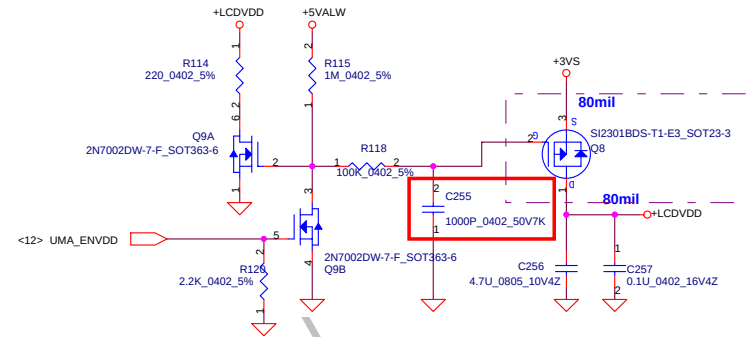
SM01000E100 (S SUPPRE_KING CORE FBMA-10-100505-800T 0402)

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Issued Date	2007/08/02	Deciphered Date	2008/08/02	Title	CRT Connector
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				Date	Monday, September 08, 2008
				Sheet	17 of 46
				Rev	0.4

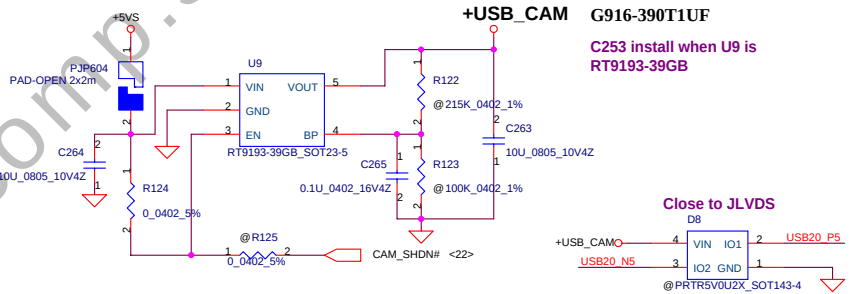
LVDS CONN



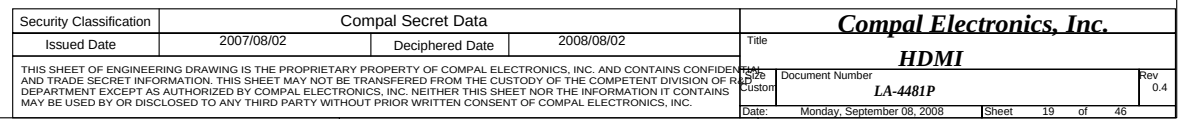
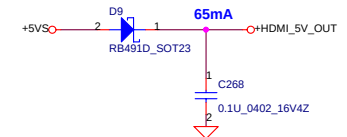
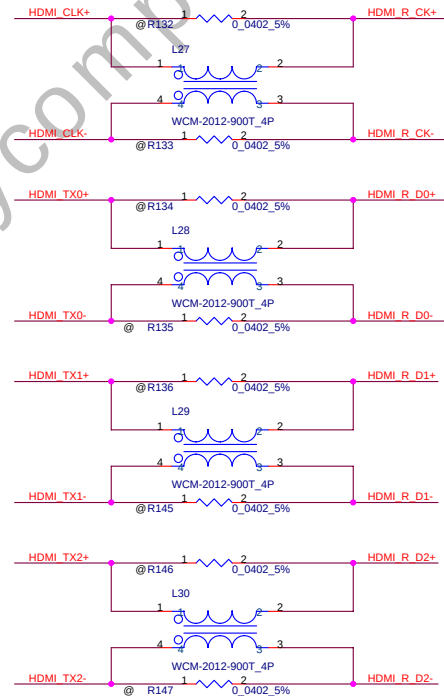
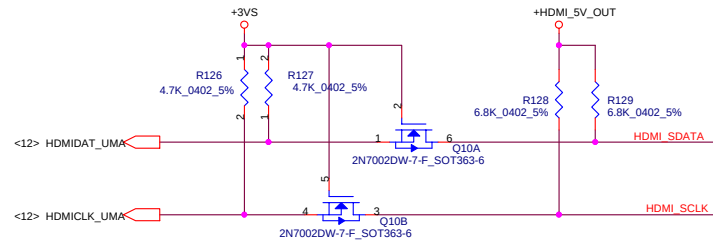
LVDS PWR circuit

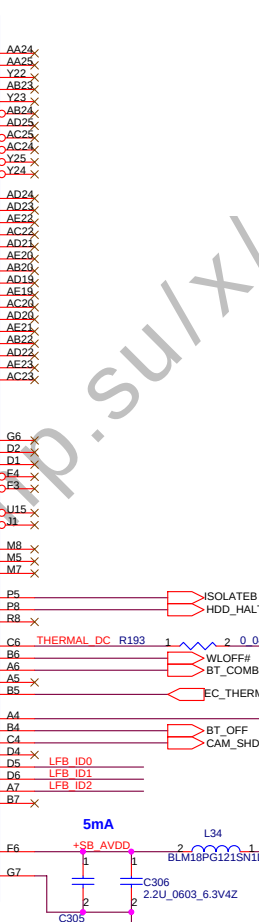
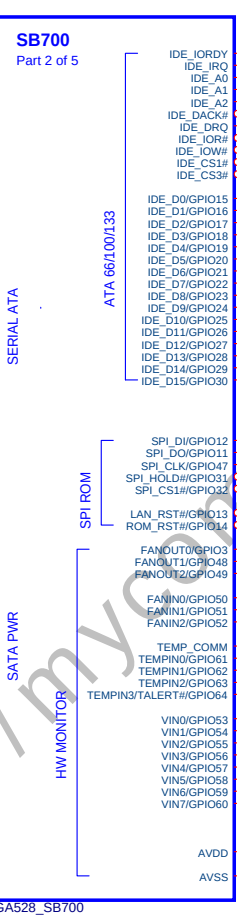
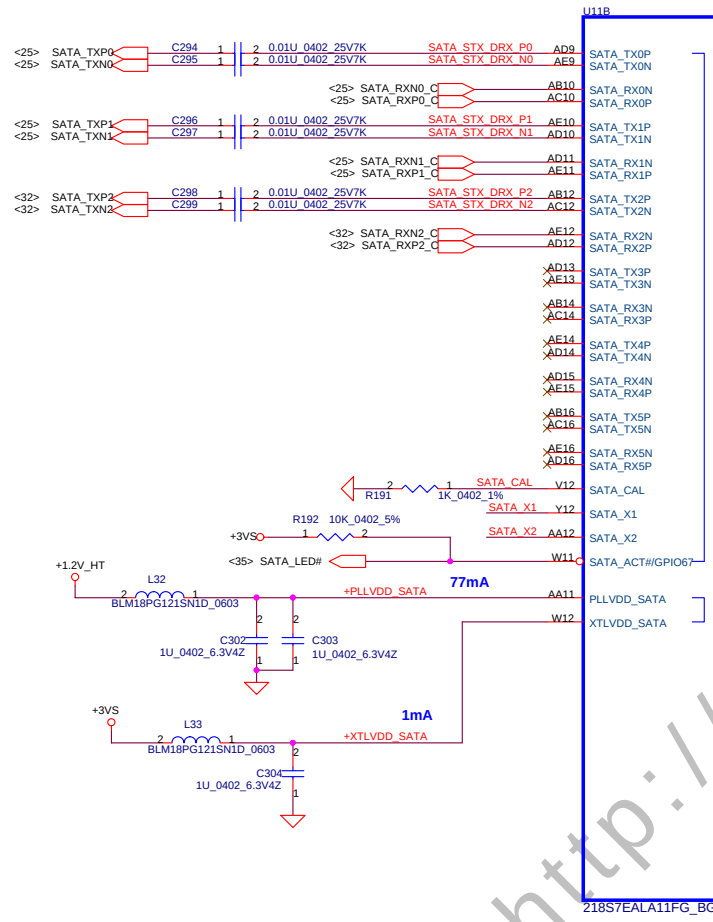
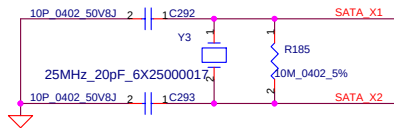


Camera PWR circuit



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Issued Date	2007/08/02	Deciphered Date	2008/08/02	Title LA-481P	
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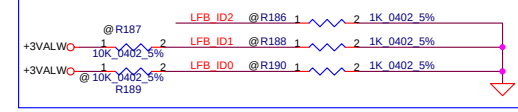


Local Frame Buffer Strapping List

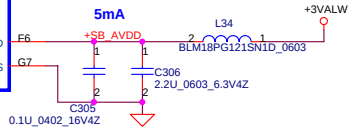
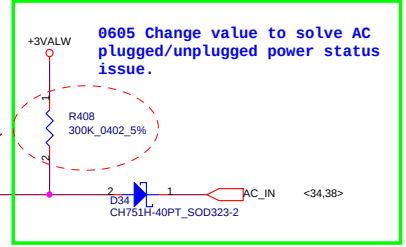
Copy from Becks.

	LFB_ID2	LFB_ID1	LFB_ID0
Hynix	0	0	0
Qimonda	0	0	1
Samsung	0	1	0

LFB_ID0 to LFB_ID2 got internal PU 10K to S5.



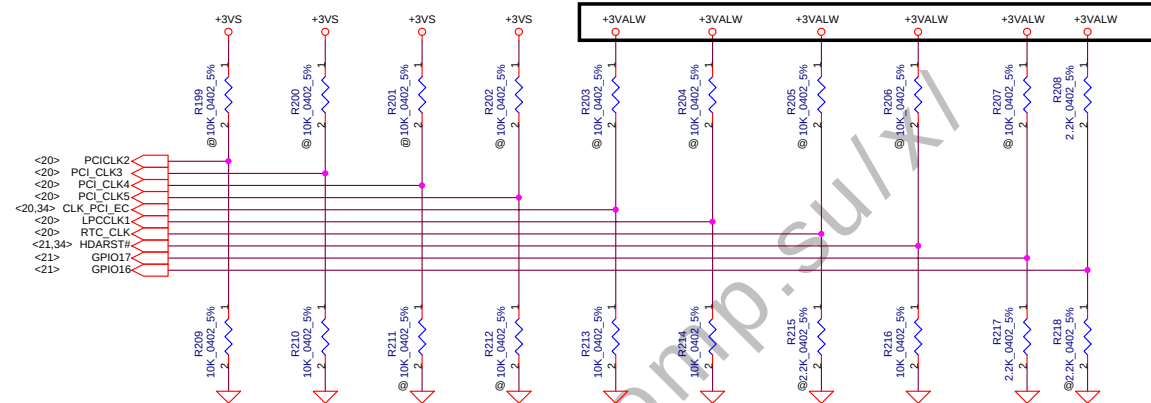
0605 Change value to solve AC plugged/unplugged power status issue.



REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

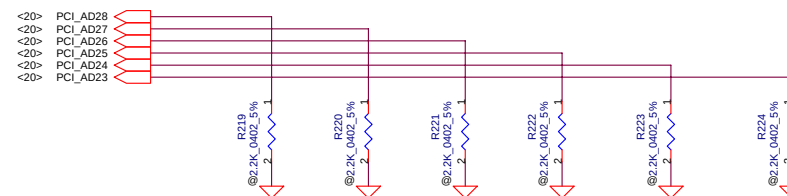
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	AZ_RST_CD#	LPC_CLK1	RTC_CLK	LPC_CLK0	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	



DEBUG STRAPS

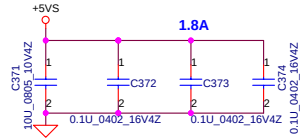
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

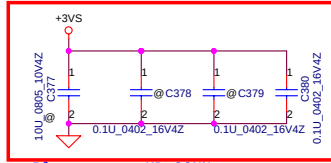


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Issued Date	2007/08/02	Deciphered Date	2008/08/02	SB700 STRAPS	
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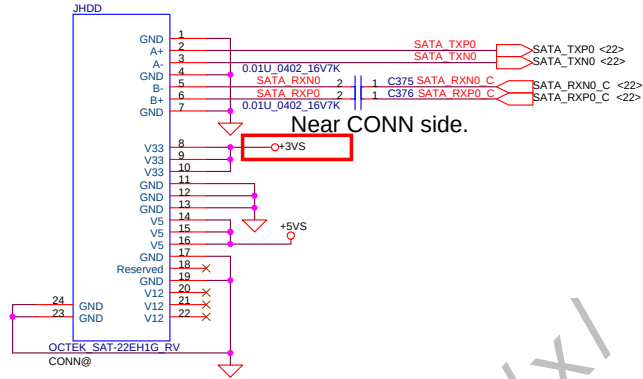
HDD Connector



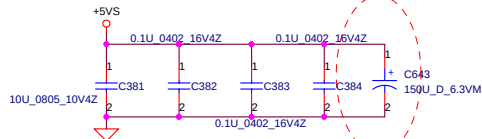
Place near HD CONN



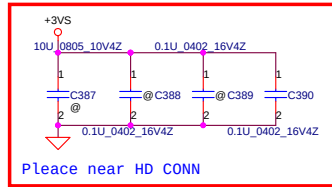
Place near HD CONN



0605 add 150uF Cap to solve hot-plug

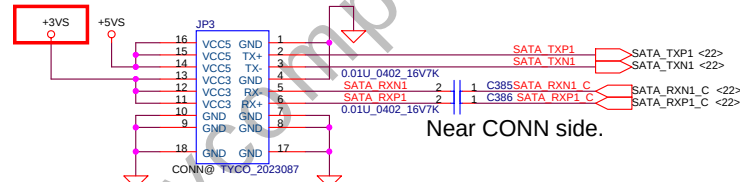


Place near HD CONN



Place near HD CONN

Multi-Bay Connector-option



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Issued Date	2007/08/02	Deciphered Date	2008/08/02	HDD/CDROM	
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+1.5VS Max 0.5A +1.5VS WL



1000

U16

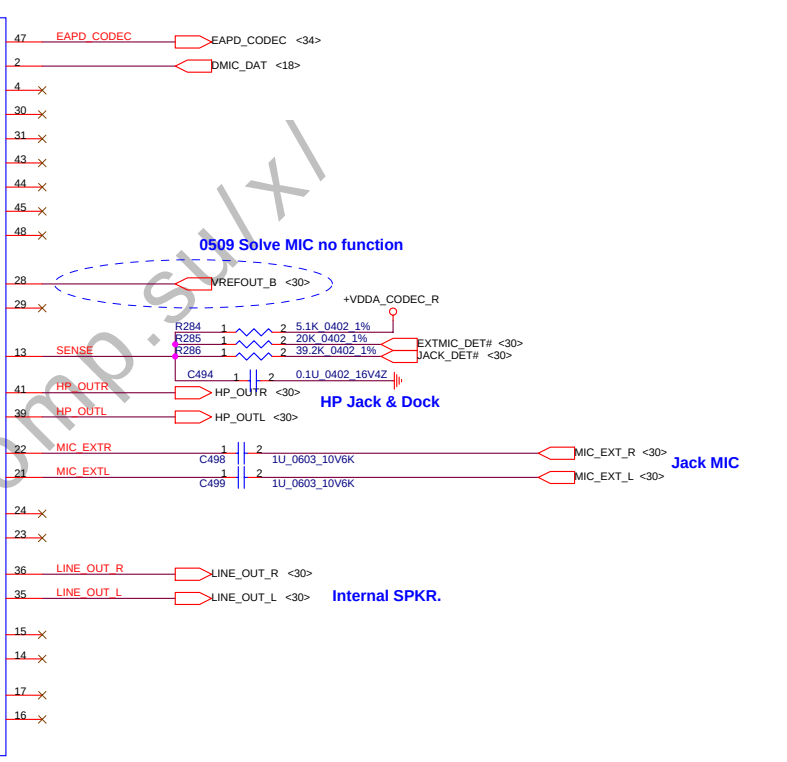
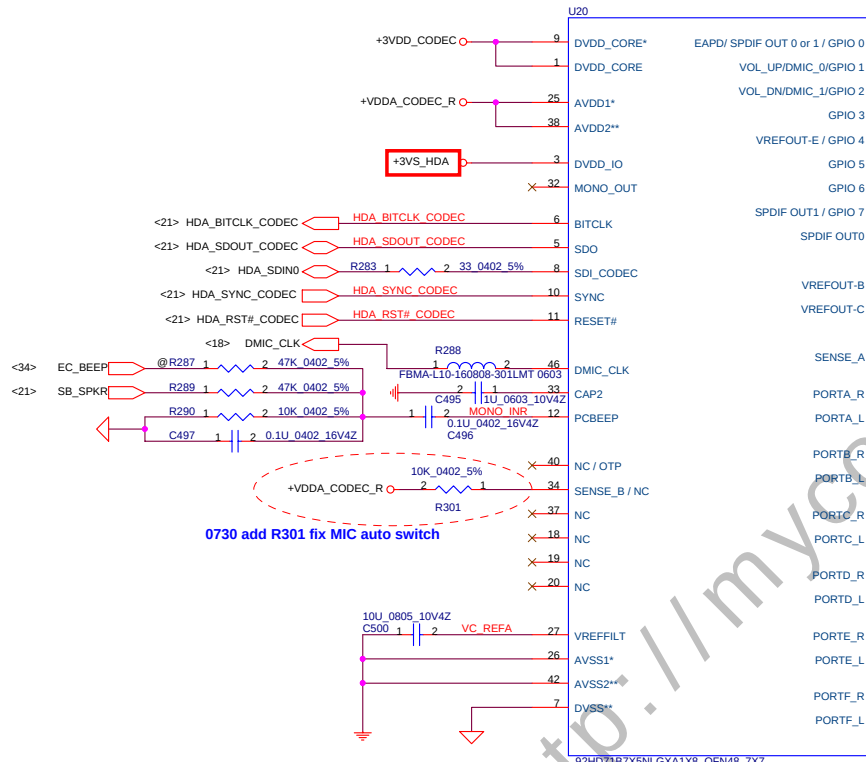
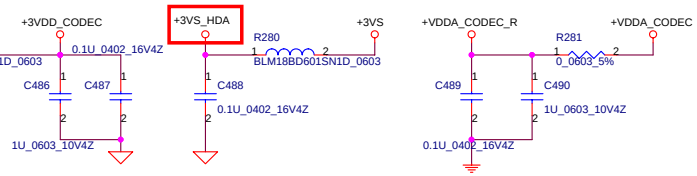
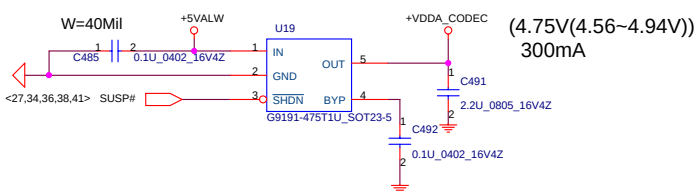


1000

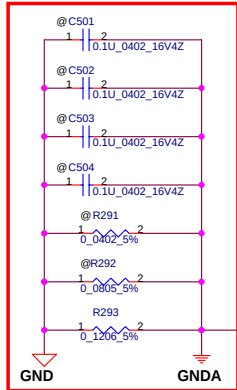


C	D	E
---	---	---

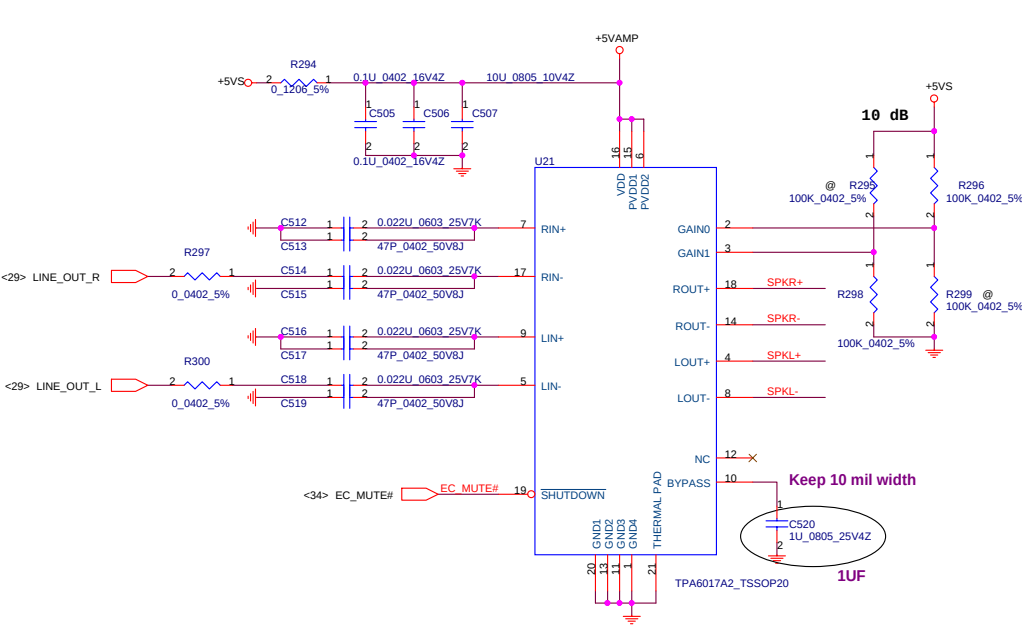
CODEC POWER



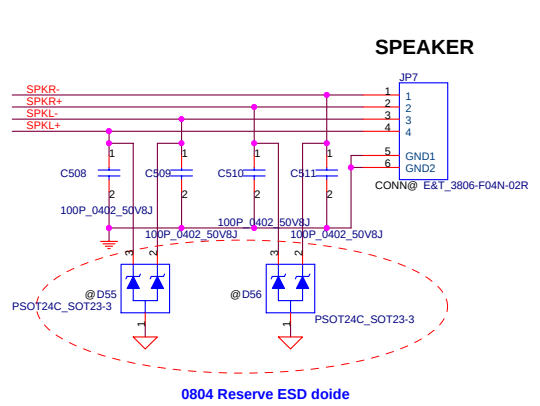
SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K



Use an 80mil to connection or place a 1206 resistor under CODEC with double vias.

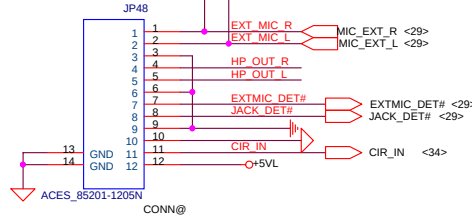
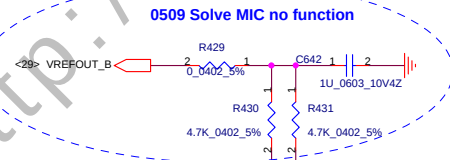
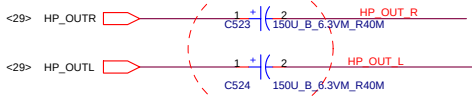


GAIN0	GAIN1	Av(inv)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

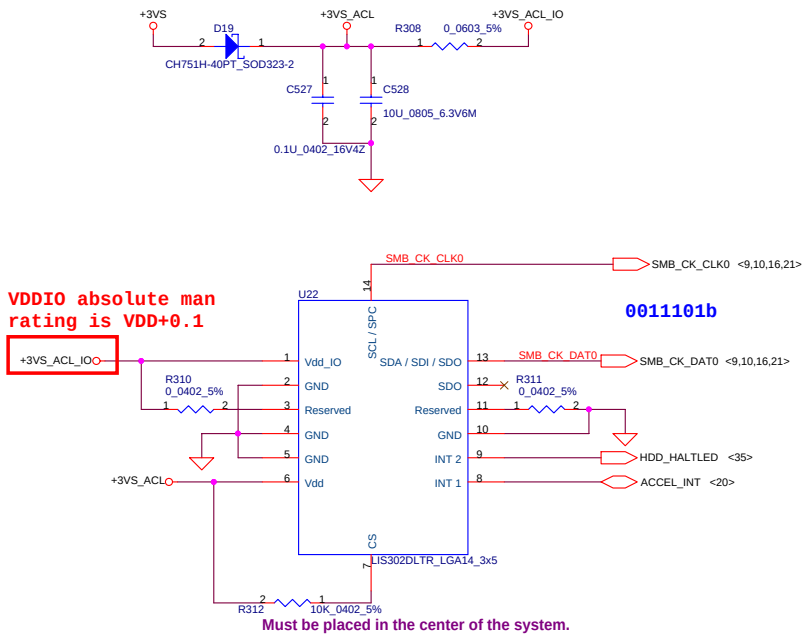


0605 Remove Transistors.

0605 change Cap size to solve DFB issue.

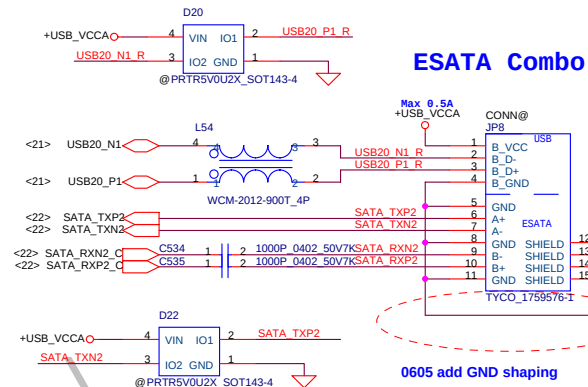
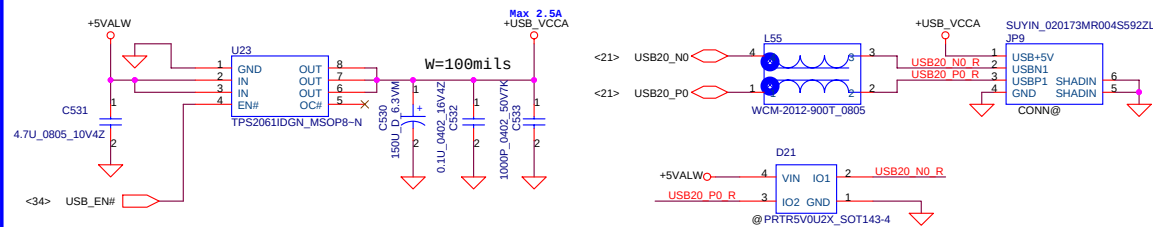


ACCELEROMETER

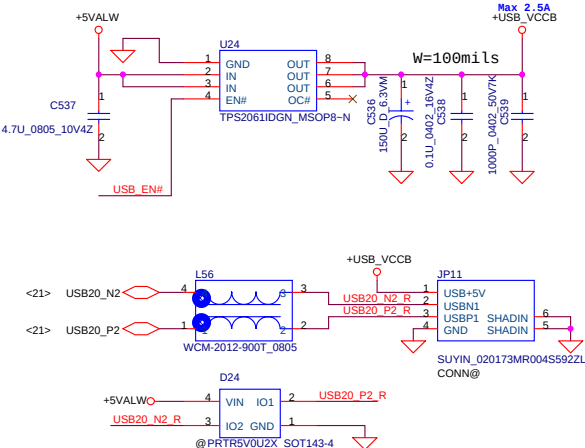


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Issued Date	2007/08/02	Deciphered Date	2008/08/02	Accelerometer	
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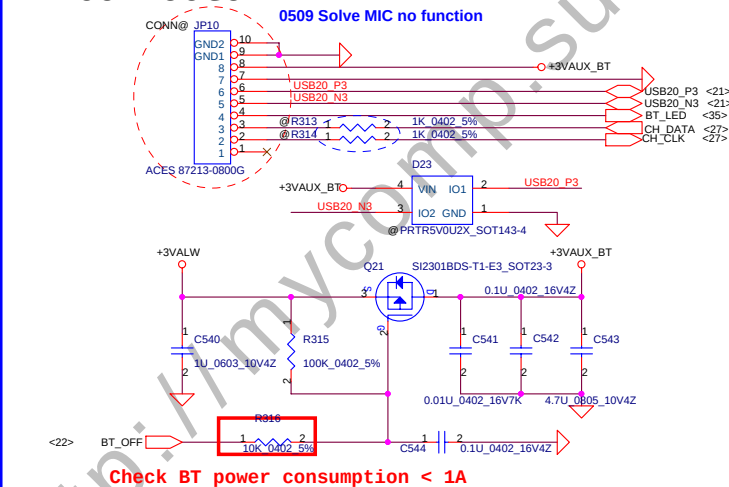
E-SATA Combo & USB-1



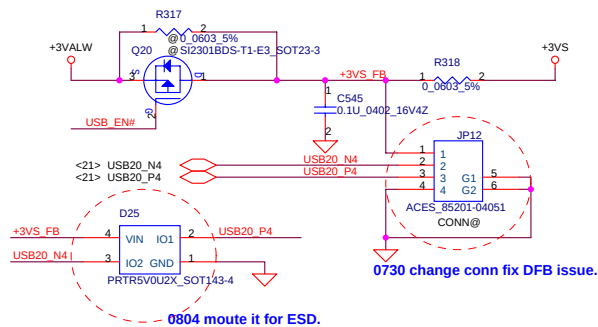
USB-3



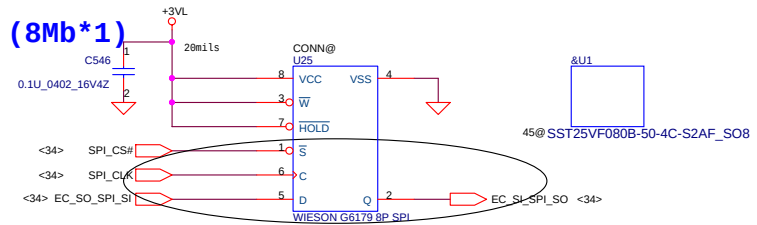
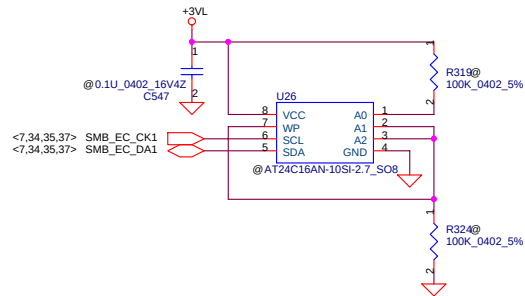
BT Connector



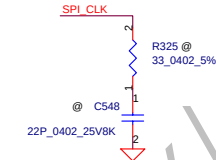
Finger printer



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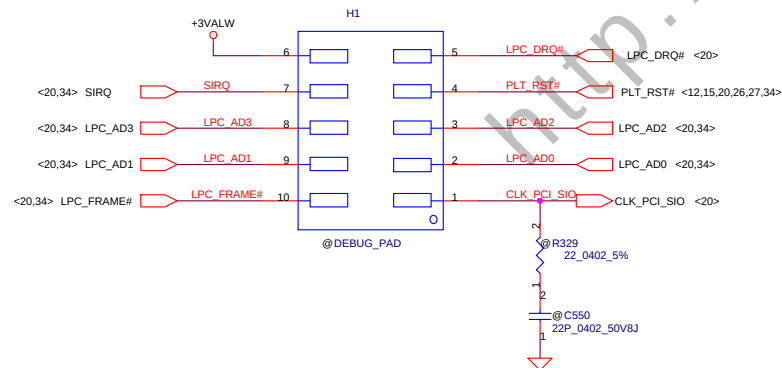


0605 remove 0 ohm resistors

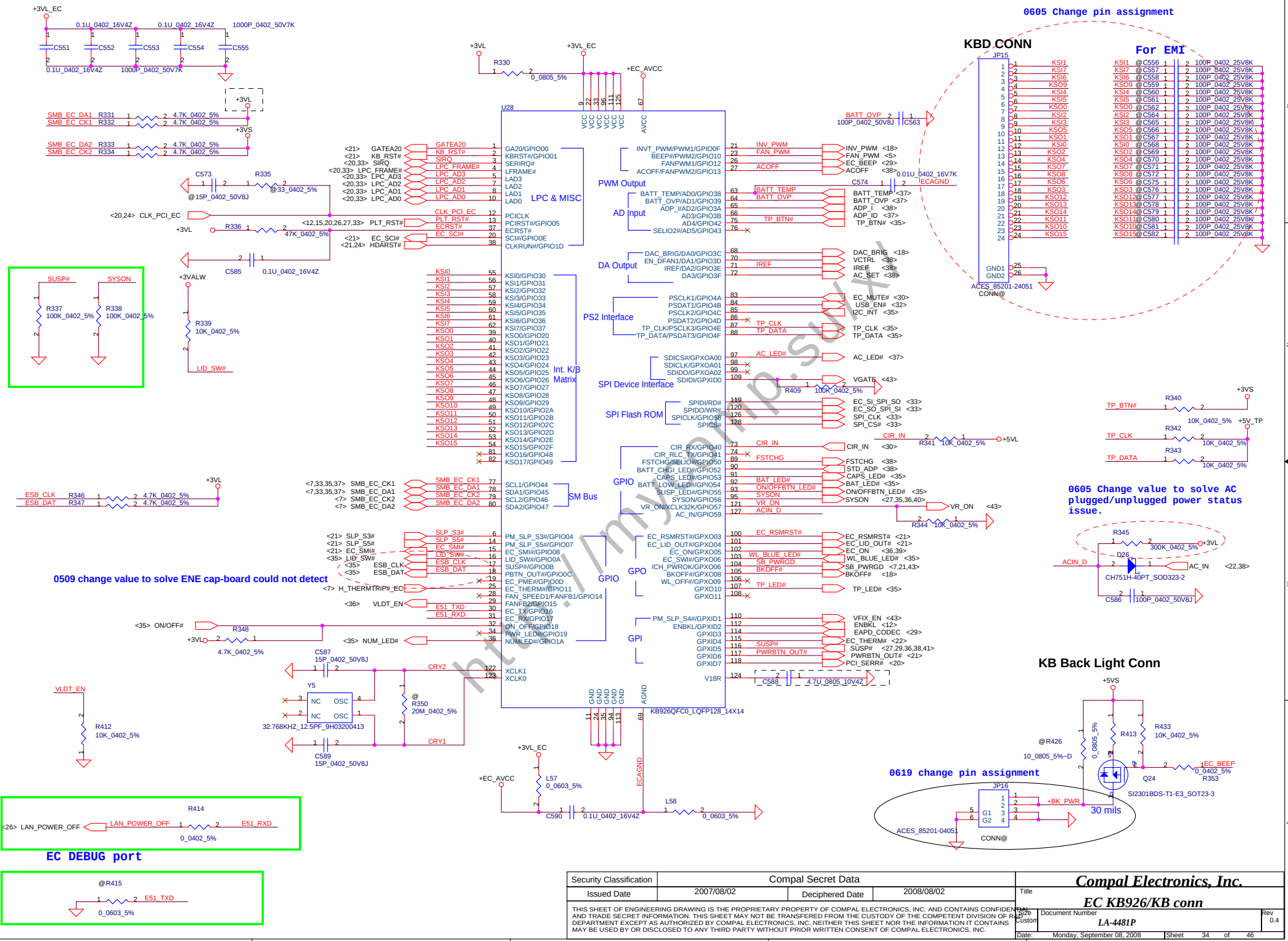


0605 Remove LPC debug connector

LPC Debug Port

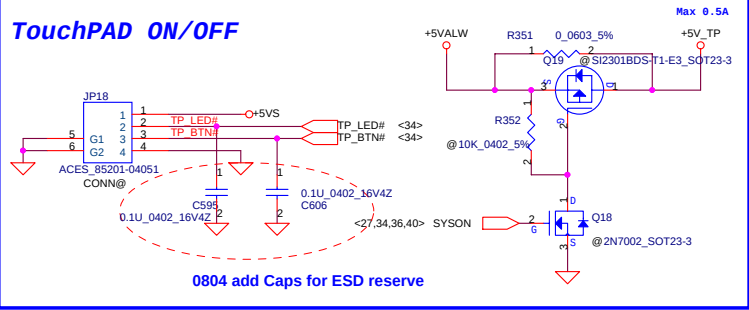


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2007/08/02				2008/08/02				BIOS ROM/Debug Tool			
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				Monday, September 08, 2008				0.4			
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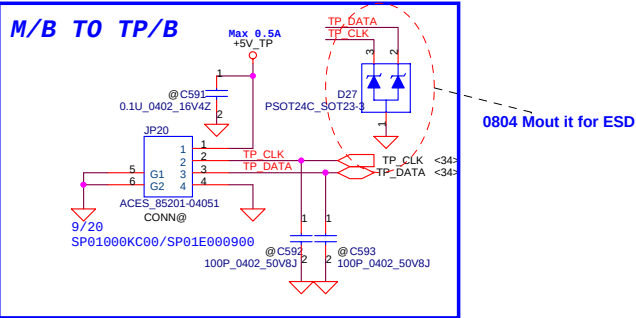


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Issued Date	2007/08/02	Deciphered Date	2008/08/02	Compal Electronics, Inc.	
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				LA-4481P	0.4
				Date: Monday, September 08, 2008	Sheet 34 of 46

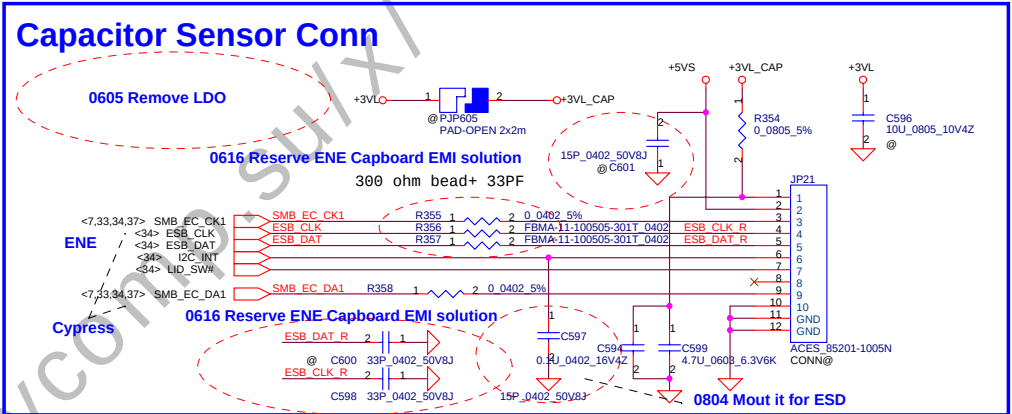
TouchPAD ON/OFF



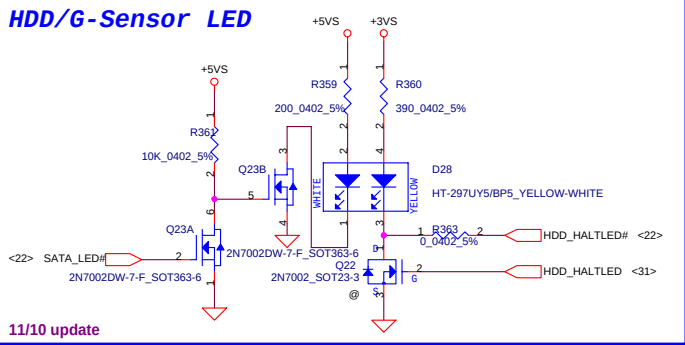
M/B TO TP/B



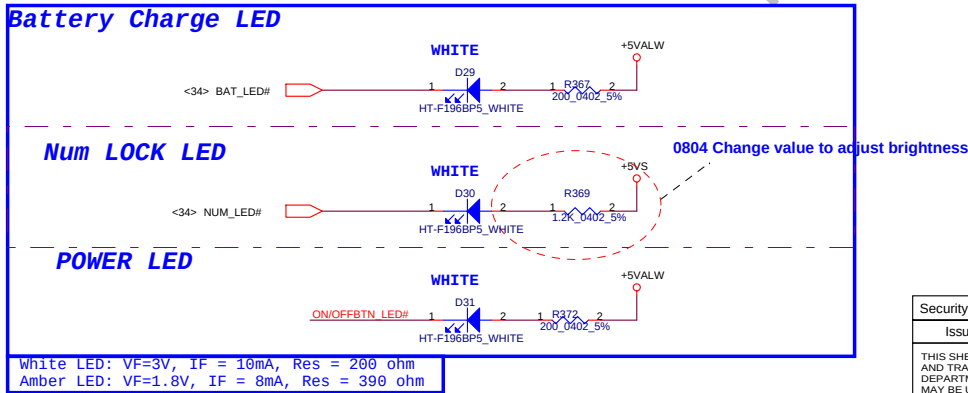
Capacitor Sensor Conn



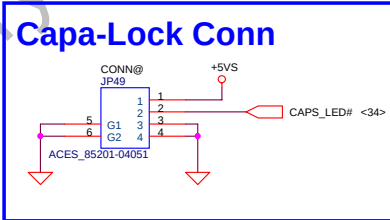
HDD/G-Sensor LED



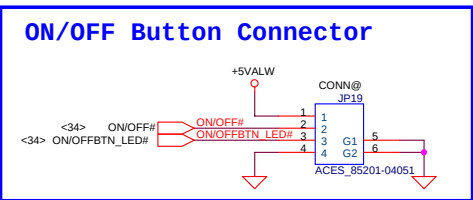
Battery Charge LED



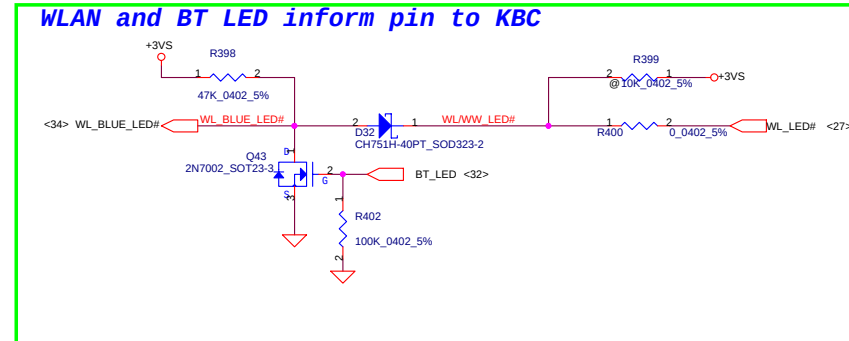
Capa-Lock Conn



ON/OFF Button Connector

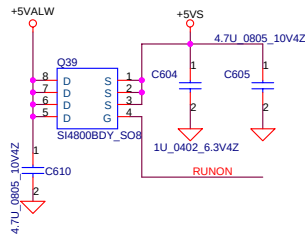


WLAN and BT LED inform pin to KBC

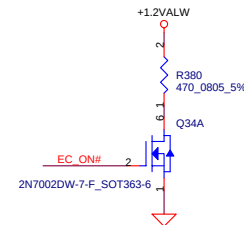
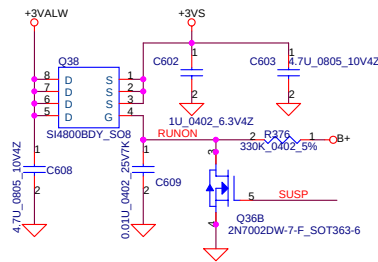


Security Classification				Compal Secret Data				Title			
Issued Date				2007/08/02				Deciphered Date			
2007/08/02				2008/08/02				TP,MDC,ON/OFF,S/W,LED,Reed			
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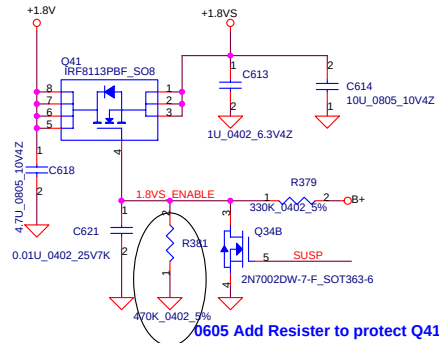
+5VALW TO +5VS



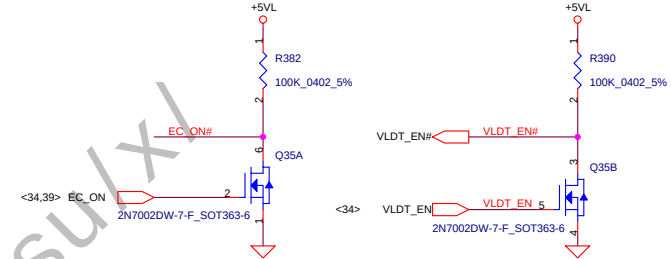
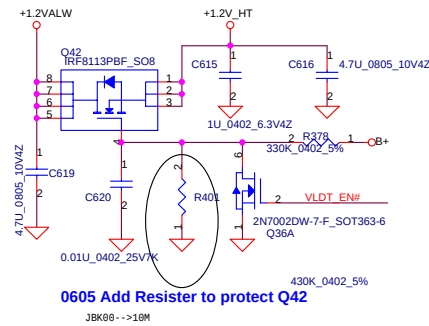
+3VALW TO +3VS



+1.8V TO +1.8VS

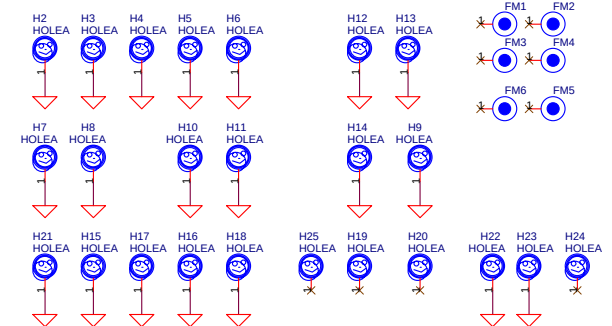
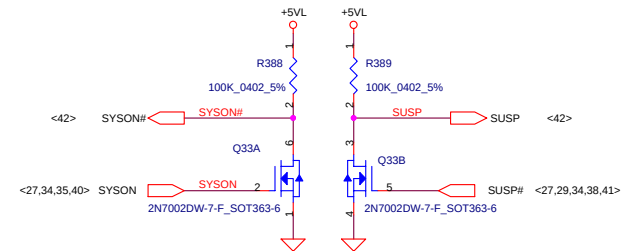
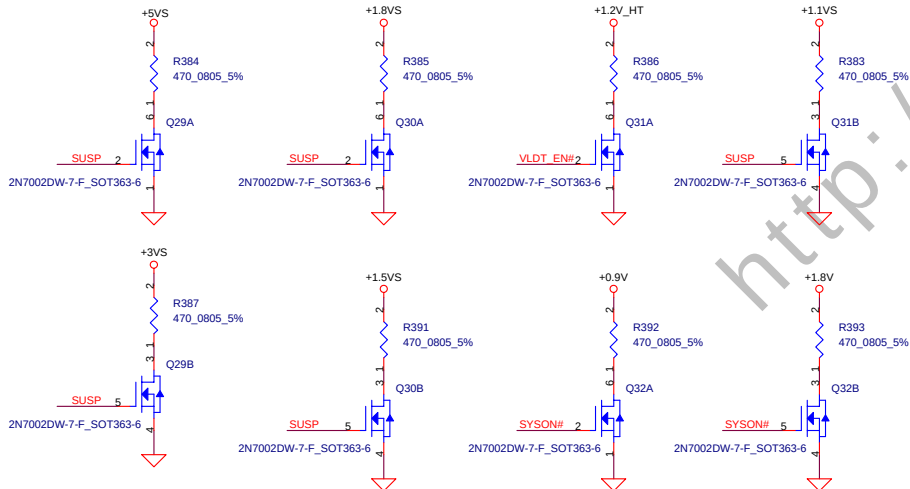


+1.2VALW TO +1.2V_HT



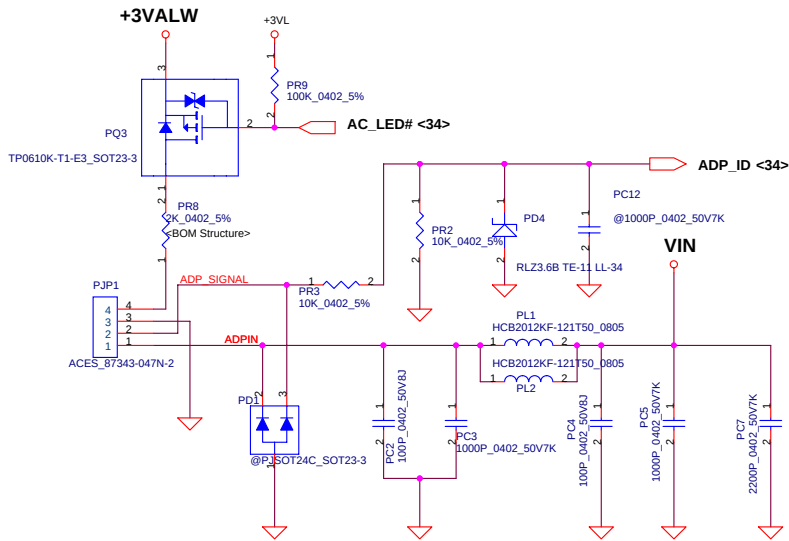
Discharge circuit

JBK00 --> 759K

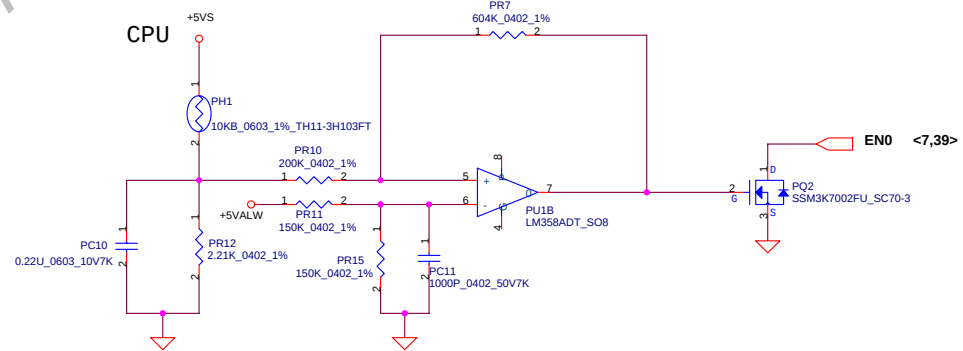
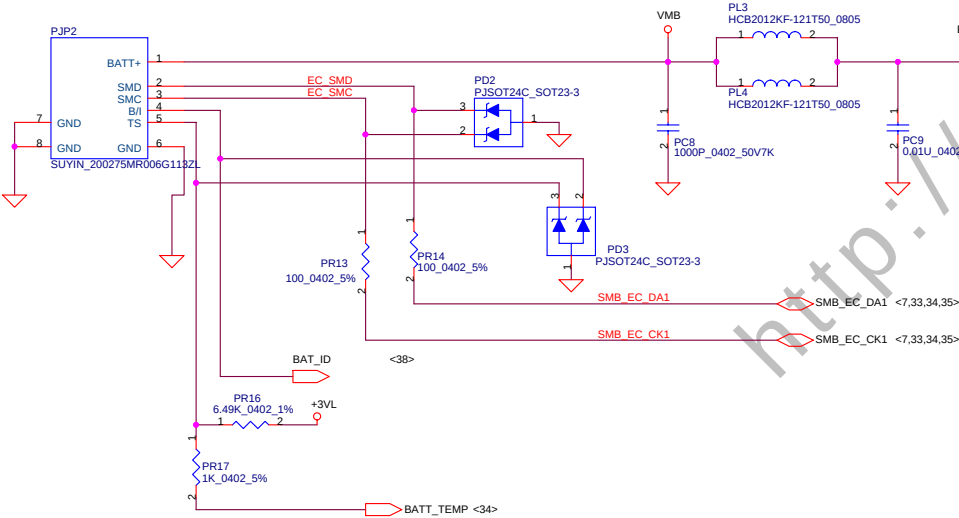
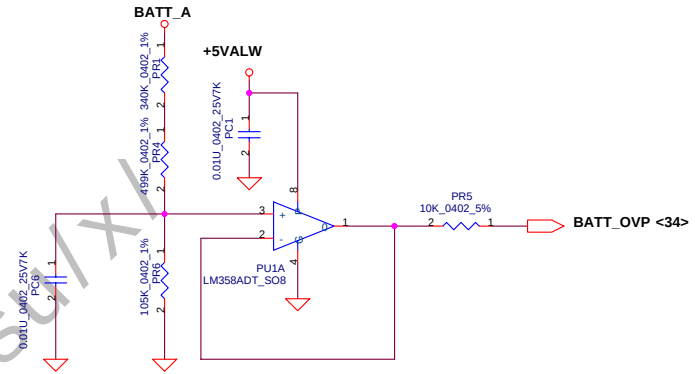


Security Classification				Compal Secret Data				Title			
Issued Date				2007/08/02				Deciphered Date			
2007/08/02				2008/08/02				2008/08/02			
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LA-4481P				0.4				Date: Monday, September 08, 2008			
Sheet				36				of			
46				E							

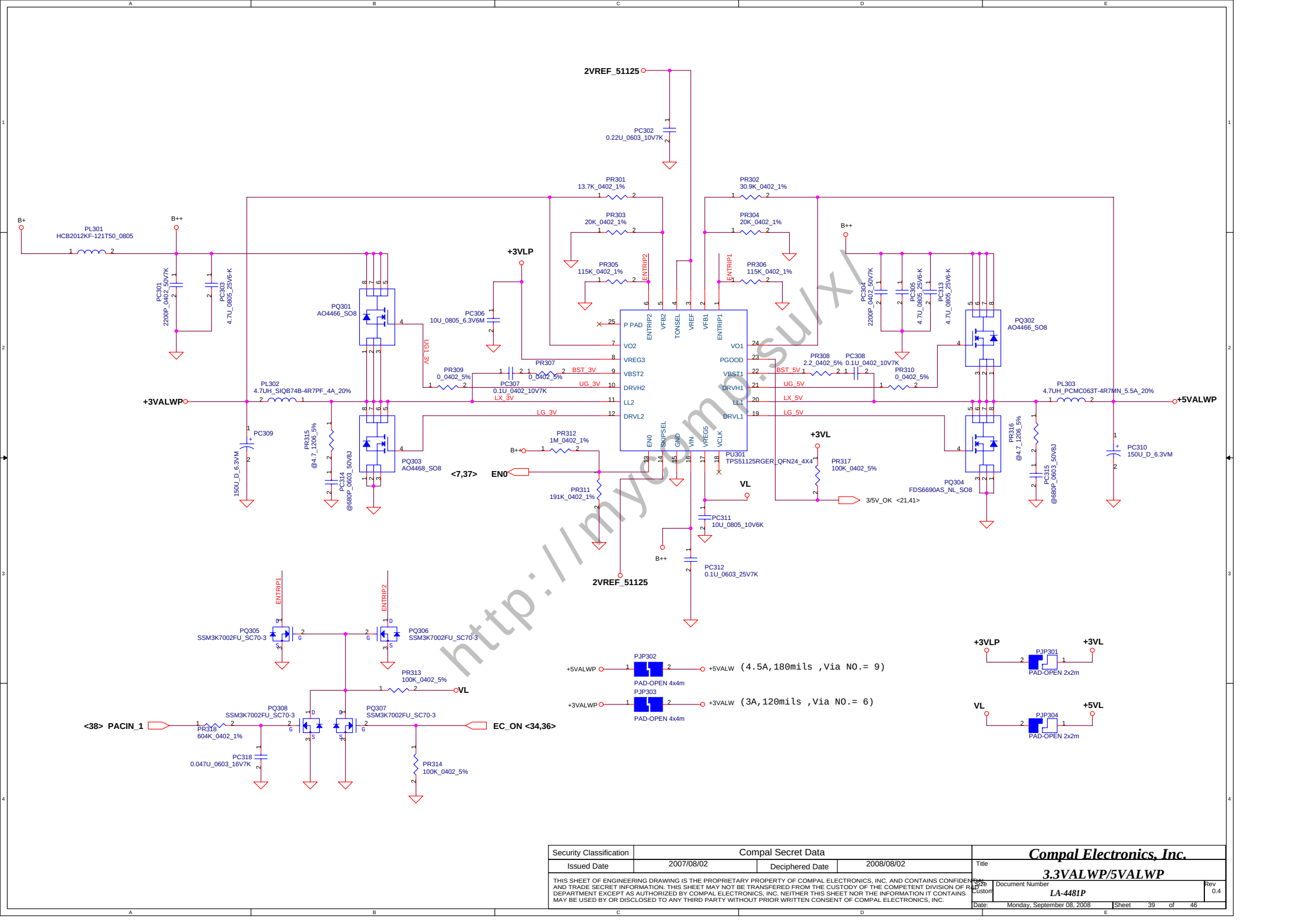
BATT1
45@CR2032 RTC BATTERY



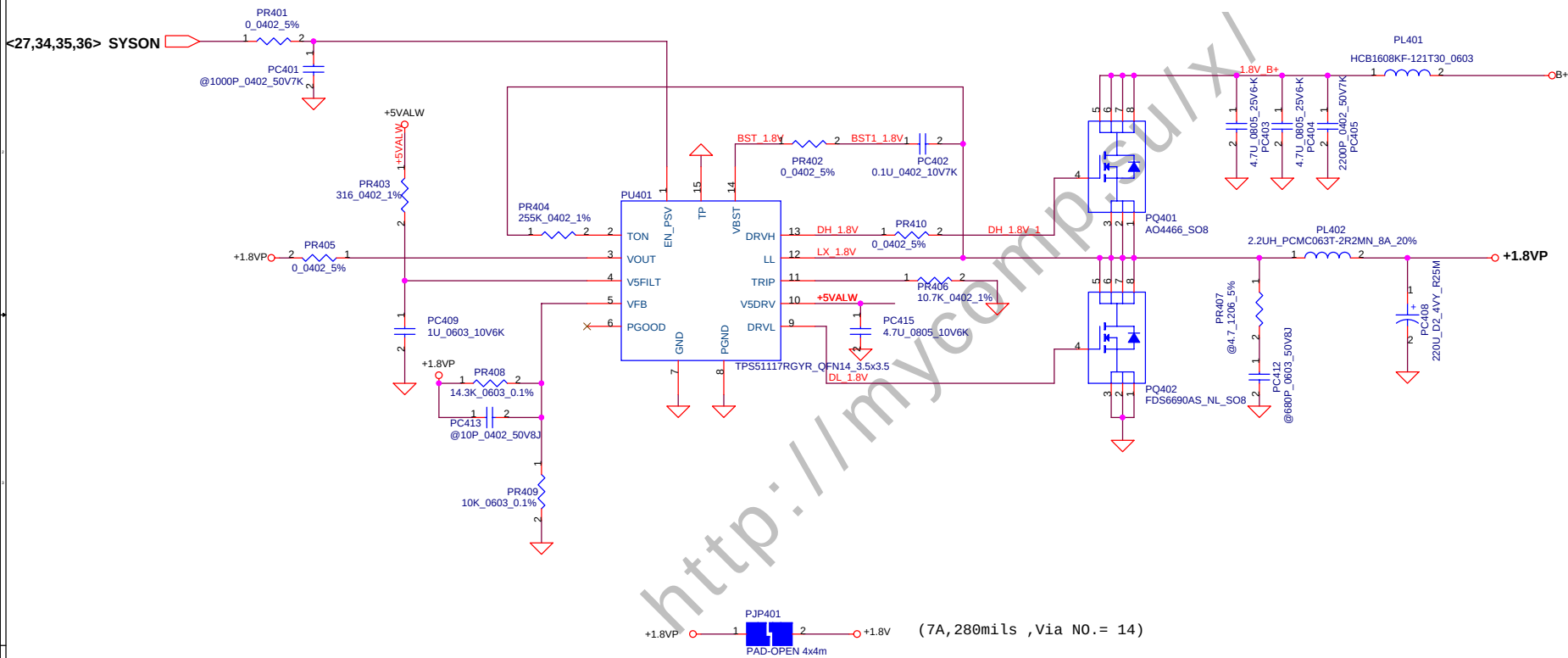
PH1 under CPU bottom side :
CPU thermal protection at 95 +-3 degree C



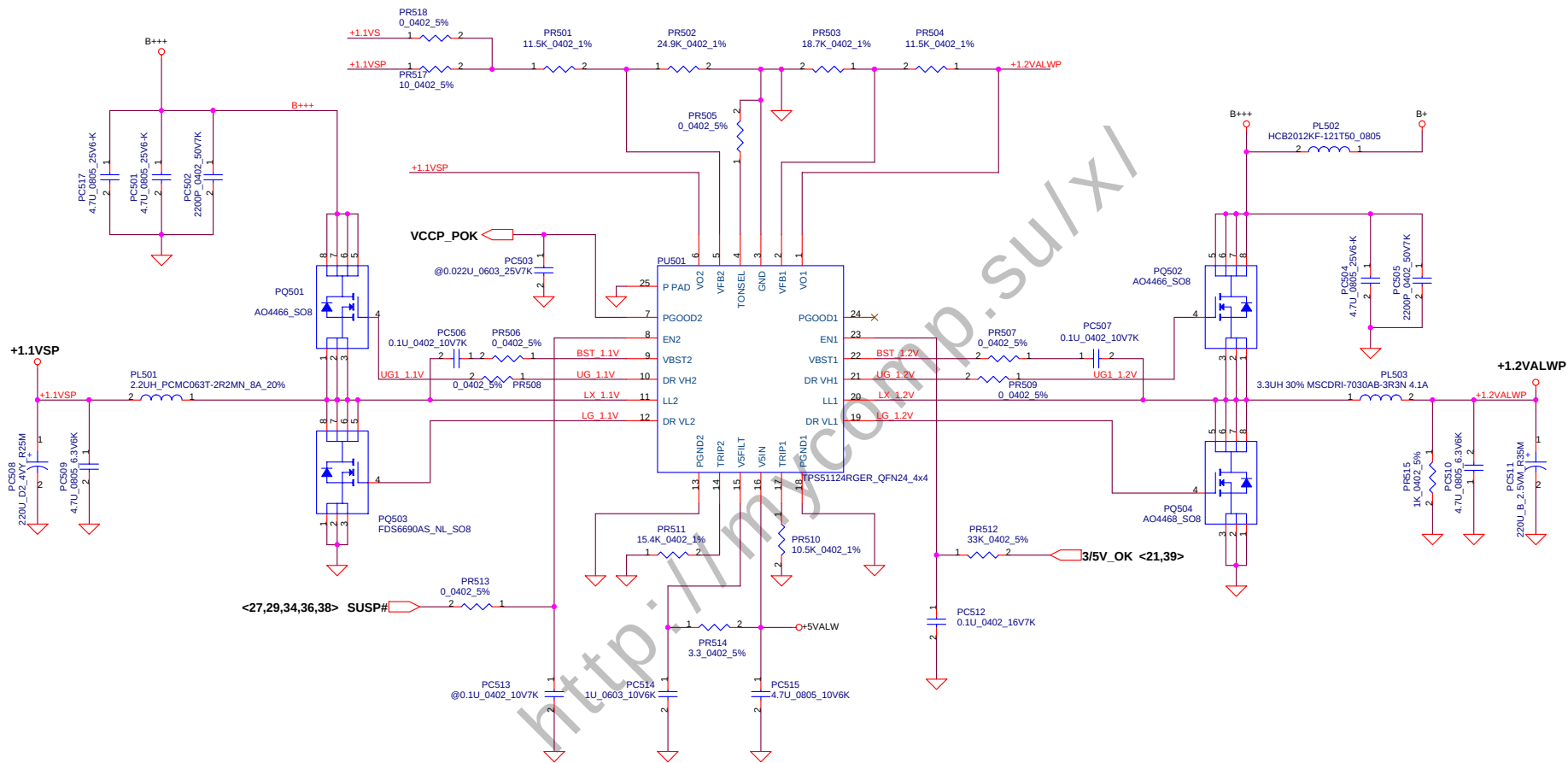
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	DC Connector/CPU_OTP	
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				Date: Monday, September 08, 2008	Sheet 37 of 46



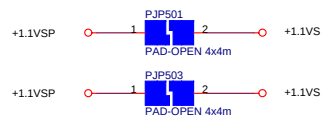
Security Classification	Compal Secret Data			Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	3.3VALWP/5VALWP	
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Issued Date	2007/05/29	Deciphered Date	2008/05/29	Title	1.8VP
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				Rev	0.4
				Date:	Monday, September 08, 2008
				Sheet	40 of 46



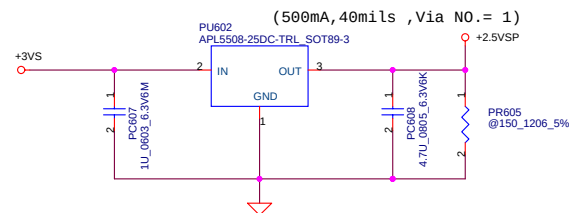
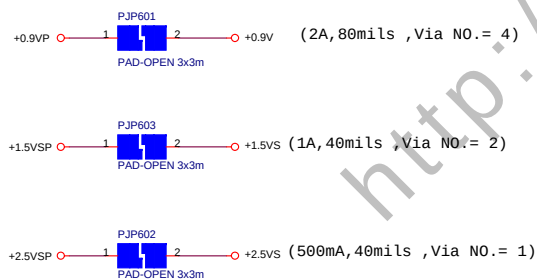
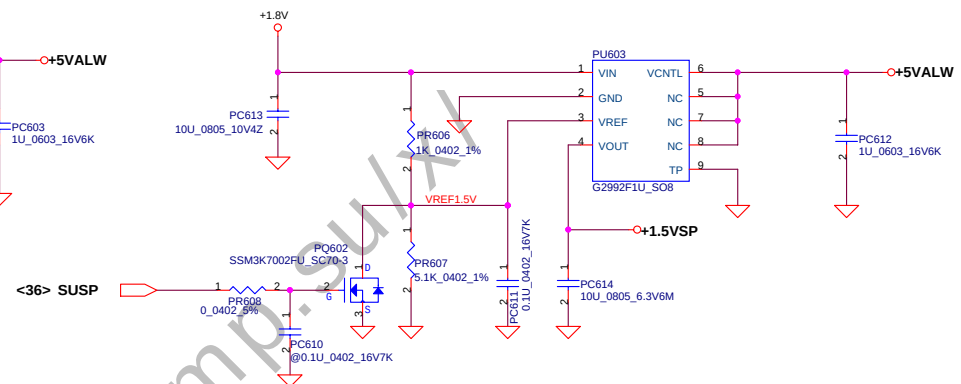
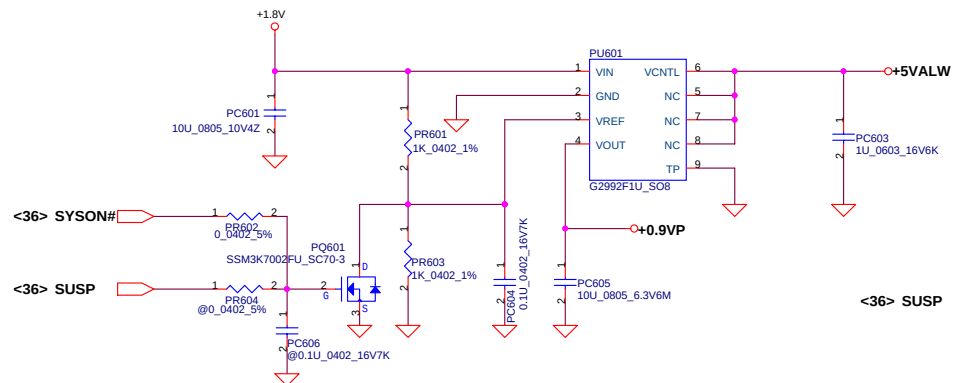
(6A,240mils ,Via N0.=12)



(4A,160mils ,Via N0.=8)



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						Document Number		LA-4481P		Rev	
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						Document Number		LA-4481P		Rev	
						Date: Monday, September 08, 2008		Sheet 42 of 46		0.4	

Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	DC Connector /CPU_OTP	2008/05/21	PWR	HW request	PR8 change the value from 100 to 2K.	0.2
2	38	Charger	2008/05/21	PWR	PWR request, solve inrush current.	Modify PR102 footprint and PQ101,PQ103 change from AM4835 to SI4835BDY, PQ103 change from AM4835 to FDS6675BZ, PC106 change from 0.22u to 0.47u,	0.2
3	39	3.3VALWP/5VALWP	2008/05/21	PWR	PWR request, modify OCP	PR305 change the value from 140K to 95.3K, PR306 change the value from 133K to 105K, PC318 change the value from 0.022u to 0.047u.	0.2
4	40	1.8VP	2008/05/21	PWR	PWR request, modify OCP.	PR406 change the value from 15.4K to 10.7K.	0.2
5	41	1.1VSP/1.2VALWP	2008/05/21	PWR	For PWR request, prevent leakage power and modify OCP.	Add PR515 1k_0402_5%, PR511 change the value from 18.2K to 15.4K, PR510 change the value from 17.8K to 10.5K.	0.2
6	42	CPU_CORE	2008/05/21	PWR	PWR request	Modify PC206 change the footprint from 0603 to 0402, PR207 change the value from 15.4K to 14K.	0.2
7	38	Charger	2008/06/04	PWR	HP request	Add 4 cell schematic, add net name BATT_A.	0.2
8	37	DC Connector /CPU_OTP	2008/06/12	PWR	Thermal request, prevent PH1 will OTP on TPD.L.	PR12 change the value from 2.55K to 2.21K.	0.2
9	38	Charger	2008/06/18	PWR	PWR request	Add PC133 220P_0402, PR147 change the value from 100K_0402_5% to 470K_0402_1%.	0.2
10	39	3.3VALWP/5VALWP	2008/07/21	PWR	PWR request	Add PR311 191K_0402_1%, PR312 1M_0402_1%.	0.2
11	38	Charger	2008/07/28	PWR	PWR request	Add 4 cell one shoot schematic, add net name PACIN_2	0.3
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Item	Fixed Issue and change item	PAGE	Modify List	M.B. Ver.
<2008.05.09>	1 Fix Audio MIC no function and follow Ripley schematics	30	Add R429, R430, R431, C642	0.2
	2 Fix ENE cap-board could not detect	34	Remove R410 & R411 & C627	0.2
	3 Fix BT no function and follow Ripley schematics	32	change BT pin assignment	0.2
<2008.06.05>	1 change power rail to solve +3vs leakage	07	LDT_RST# & H_PWRGD CPU & LDT_STOP# & CPU_LDT_REQ# change power rail to +1.8VS	0.2
	2 Remove 0 ohm resisters at LDT_STOP# & CPU_LDT_REQ#	12	Remove R54 & R55 (0 ohm)	0.2
	3 Remove 0 ohm resisters at NB_PWRGD	21	Remove R164 (0 ohm)	0.2
	4 Change value to solve AC plugged/unplugged power status issue.	22	Change R408 to 300k ohm	0.2
	5 add 150uF Cap to solve hot-plug for Multi-bay ODD	25	Add C643 150uF	0.2
	6 Remove HP switch Transisters and change Cap size to solve DFB issue.	30	Change C523 & C524 size and remove Q16, Q17, Q24...	0.2
	7 Remove LPC debug connector	33	Remove JP14	0.2
	8 Remove 0 ohm resisters at SPI ROM	33	Remove R320-323 (0 ohm)	0.2
	9 add GND shaping at E-SATA	32	Add E-SATA GND shaping	0.2
	10 Change Keyboard pin assignment to follow Ripley design	34	change pin assignment (follow Ripley)	0.2
	11 Change value to solve AC plugged/unplugged power status issue.	34	change R345 to 300Kohm	0.2
	12 Add Keyboard backlight control circuit	34	add Q24, R426	0.2
	13 Remove Cap-sensor baord power LDO	35	remove U29....	0.2
	14 Add Resister to protect Q42, Q41	36	Add R381 & R401	0.2
<2008.06.16>	1 Add and reserve EMI soultion for ENE cap-board	35	Add C600, C601 and Change R356, R357 size to 300ohm bead	0.2
<2008.06.19>	1 Solve LED panel flash issue when AC IN	18	Add Q4 and R54	0.2
<2008.07.30>	2 change KB backlight connector pin assignment	34	pin1 & 2 (Power), pin3 & 4 (GND) swapped	0.2
	1 Fix external and internal MIC auto switch issue	29	add R301 and pull up +VDDA_CODEC_R	0.3
	2 change FPR connector to fix Assy DFB issue.	32	change pin count from 6 pins to 4 pins	0.3
<2008.08.01>	1 Vari-Bright design change for EC & RS780 common use	18, 12	Add D38, D39, R76	0.3
<2008.08.04>	1 Reserve Caps to protect ESD	35	Add C595, C606	0.3
	2 Change R value for LED brightness	28	Change R276 value to 1.2Kohm	0.3
	3 Fix OTS#0392705 (WLAN Slot Pin 24 is tied to different power than pins 2, 52, 39 and 41)	27	Unmount R245 and install R244	0.3
	4 Reserve ESD diode to protect SPK	30	Add D55, D56	0.3
	5 Fix FPR ESD issue	32	Install D25	0.3
	6 Reserve Cap to protect T/P ON/OFF	35	Add C595, C606	0.3
	7 0804 Change value to adjust LED brightness	35	Change R369 value to 1.2kohm	0.3
	8 Install Cap to fix ESD issue	35	Install C597	0.3
<2008.09.04>	1 Remove Varibright function	12, 18	Uninstall D39, Delete D38	0.4
	2 Fix SMT DFX issue	28	Change D16 footprint	0.4
	3 Follow Vendor suggestion to change CR_LED#	28	Change power rail from+5VS to +3vs	0.4
	4 Reserve R for protect LED panel flash control	18	Add R410	0.4
	5			0.4
	6			0.4

Calypso power sequence

