

Compal Confidential

Model Name : QILE1 & QILE2
File Name : LA-8131P, LA-8132P
BOM P/N:

QILE1:
4319GG39L01 : SMT MB A8131 QILE1 DIS-N13P
4319GG39L02 : SMT MB A8131 QILE1 DIS GPU-N13M
4319GG39L03 : SMT MB A8131 QILE1 UMA

QILE2:
4319GJ39L01 : SMT MB A8133 QILE2 DIS-N13P
4319GJ39L02 : SMT MB A8133 QILE2 DIS GPU-N13M
4319GJ39L03 : SMT MB A8133 QILE2 UMA

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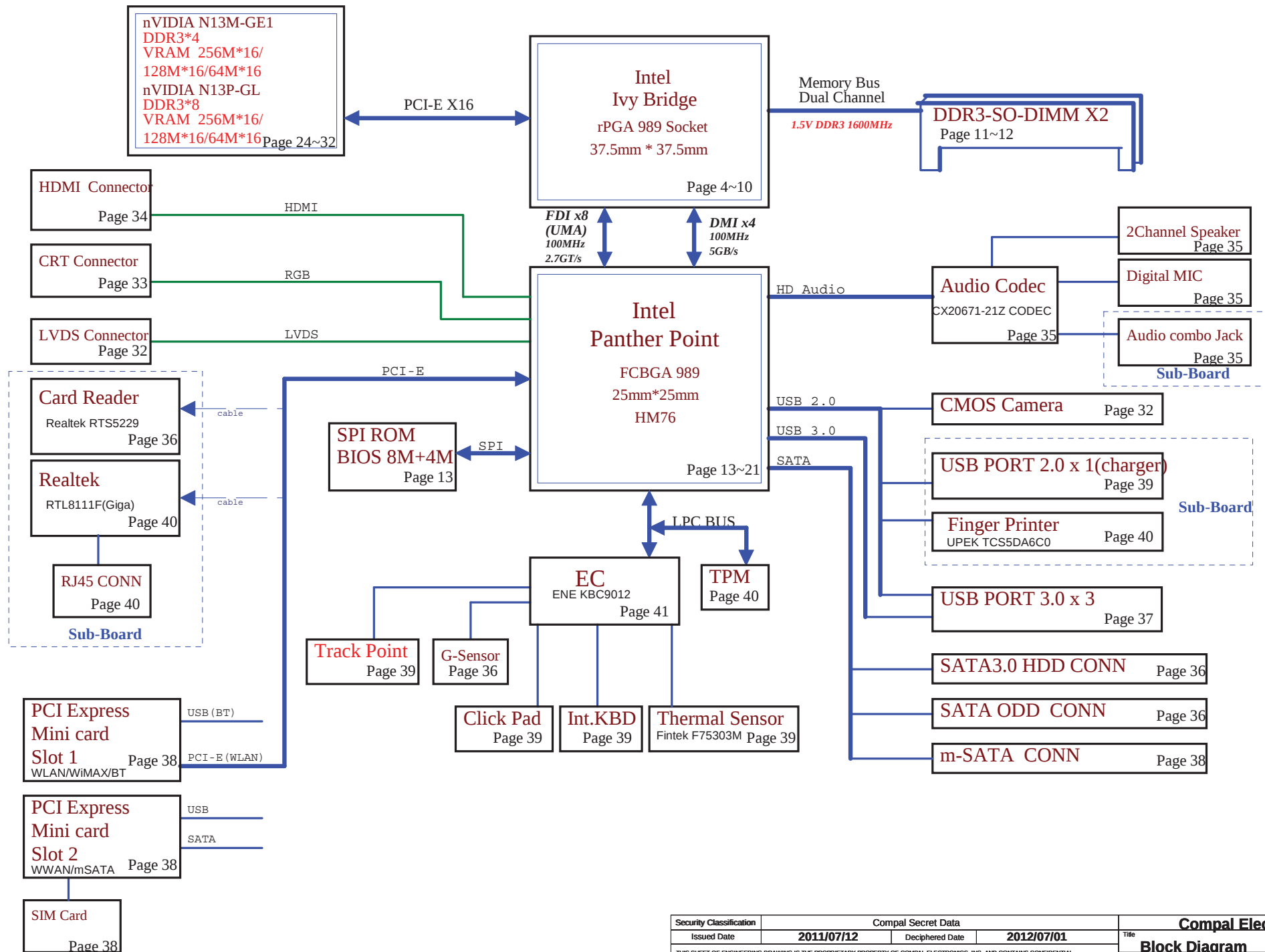
M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH
GPU nVIDIA N13M-GE1 / N13P-GL

2011-12-20

REV:0.6

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	Cover Sheet
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				Date Friday, January 06, 2012	Rev 0.6
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Voltage Rails

power plane	State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS	+3VM +1.05VM
S0		○	○	○	○	○ M3 Supported
S3		○	○	○	✗	○ M3 Supported
S5 S4/AC		○	○	✗	✗	○ M3 Supported
S5 S4/ Battery only		✗	✗	✗	✗	
S5 S4/AC & Battery don't exist		✗	✗	✗	✗	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	0.6
6	
7	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor Fintek F75303M	1001 101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

USB Port Table

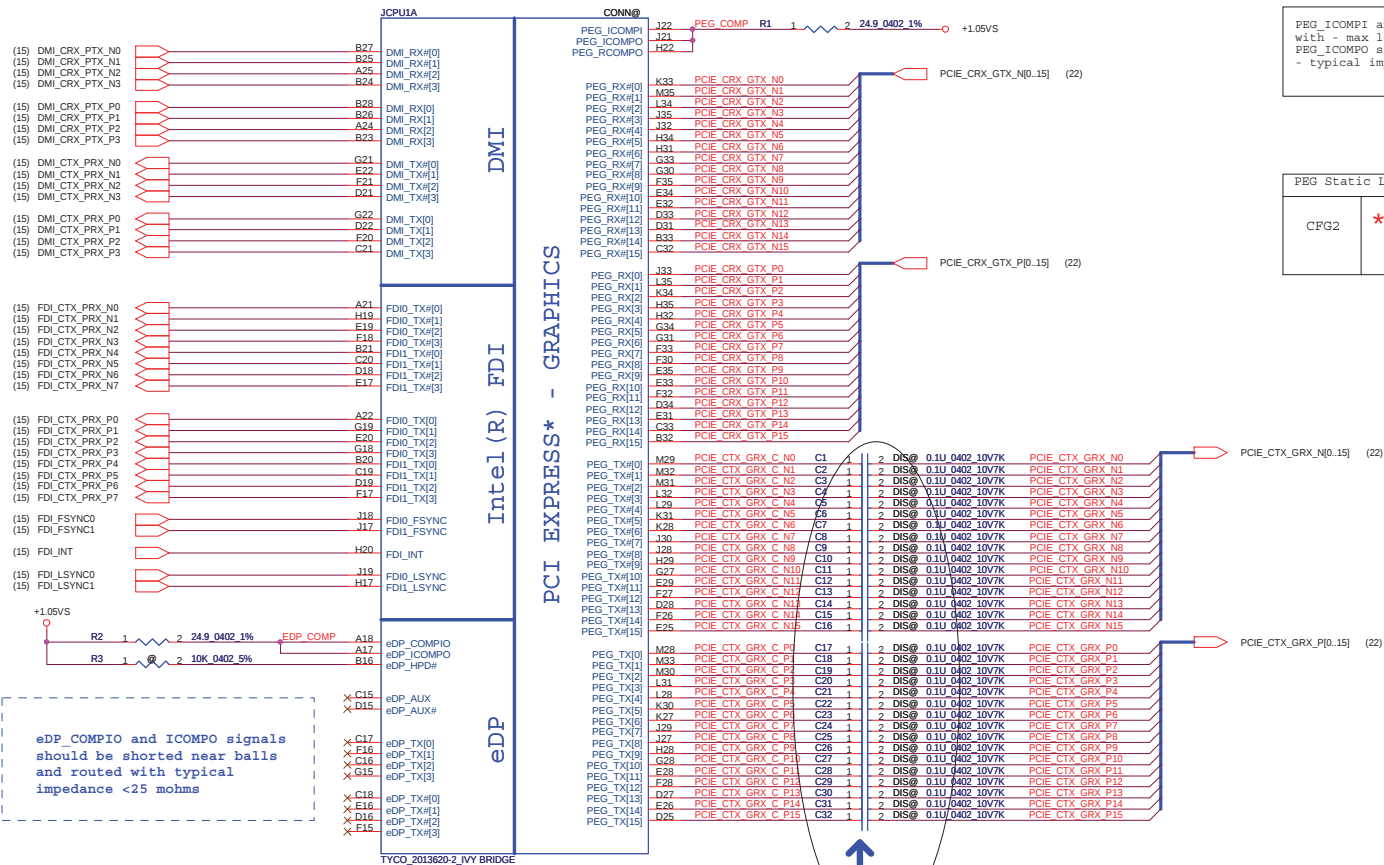
	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	
		1	USB 3.0 Port (Left Side)
	UHCI1	2	USB 3.0 Port (Left Side)
		3	USB 3.0 Port (Left Side)
	UHCI2	4	
		5	Camera
EHCI2	UHCI3	6	
		7	
	UHCI4	8	
		9	USB Port (Right Side)
	UHCI5	10	Mini Card(WLAN/BT)
		11	EPR
	UHCI6	12	Mini Card(WWAN)
		13	Blue Tooth

BOM Structure Table

BTO Item	BOM Structure
Connector	CONN@
45 LEVEL	45@
Unpop	@
nVidia	DIS@
INTEL DD3 M3	M3@
SIM Card Slot	3G@
Intel UMA	UMA@
VRAM Option	X76@
Intel SBA	SBA@
Intel AOAC	AOAC@
TPM	TPM@
GPU N13M	N13M@
GPU N13P	N13MP

SMBUS Control Table

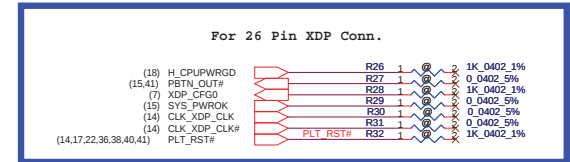
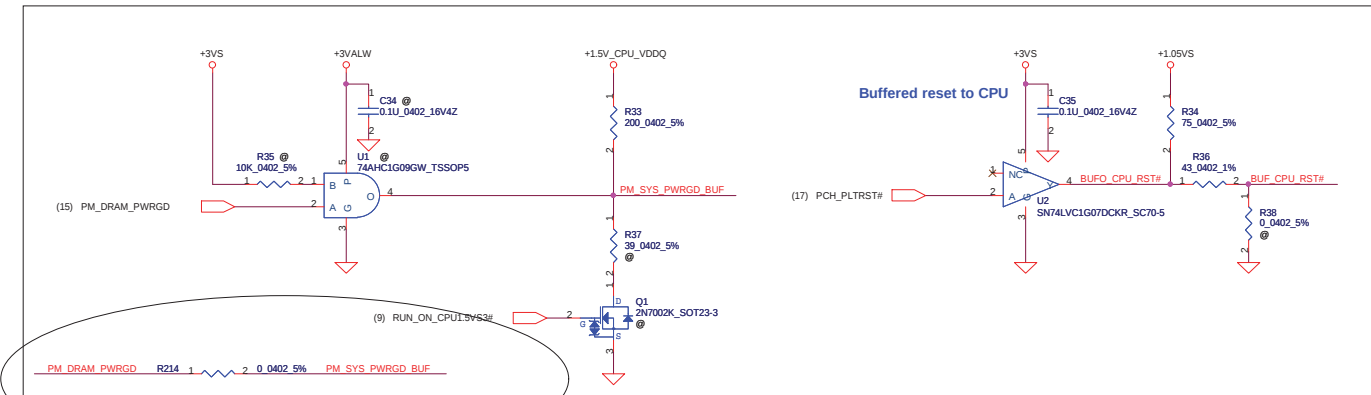
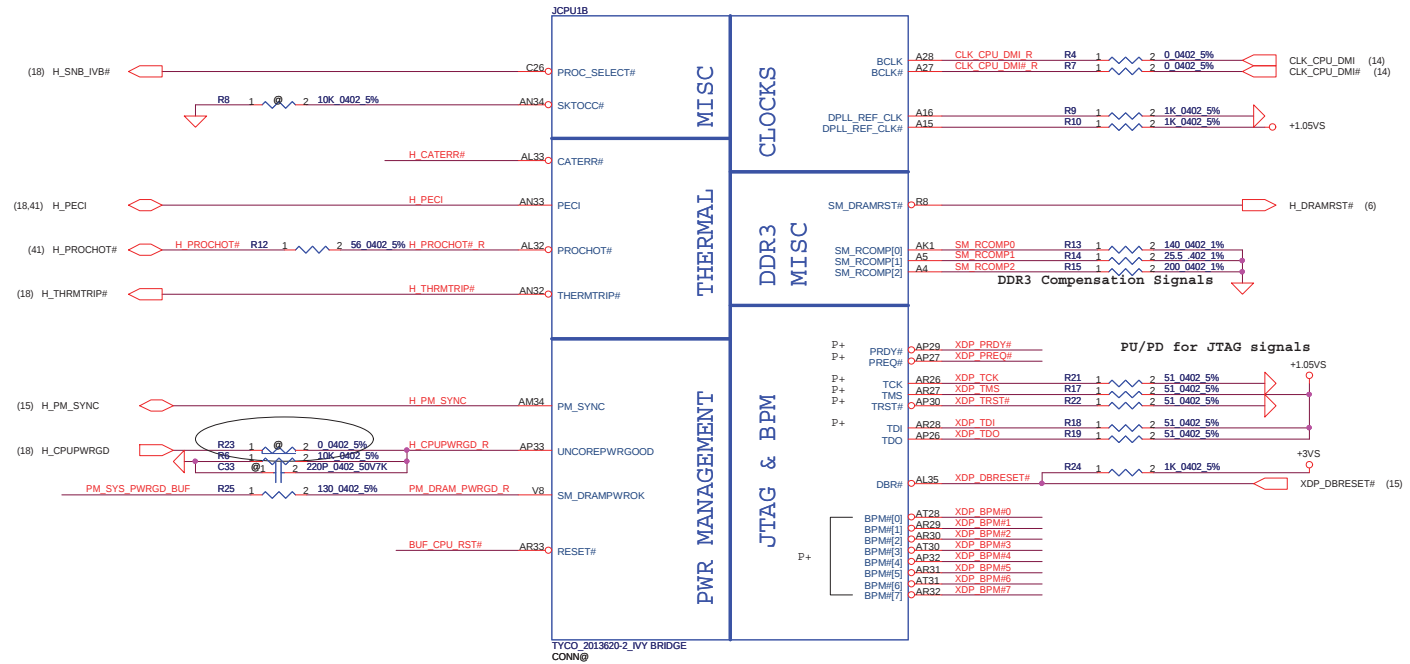
	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	✗	✓	✗	✗	✗	✗	✗
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	✗	✗	✗	✗	✗	✗	✓
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	✗	✗	✗	✓	✓	✗	✗
SMBDATA	+3VALW				+3VS	+3VS		
SMLOCLK	PCH	✗	✗	✗	✗	✗	✗	✗
SML0DATA	+3VALW							
SML1CLK	PCH	✓	✗	✓	✗	✗	✓	✗
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

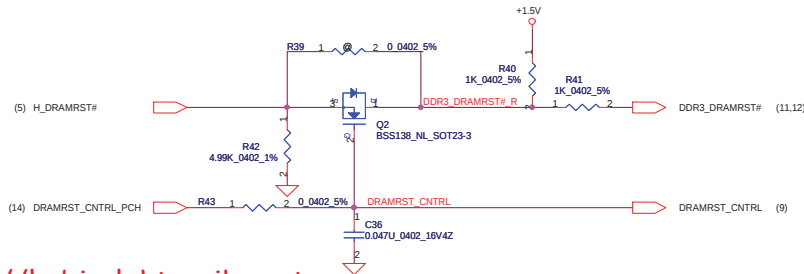
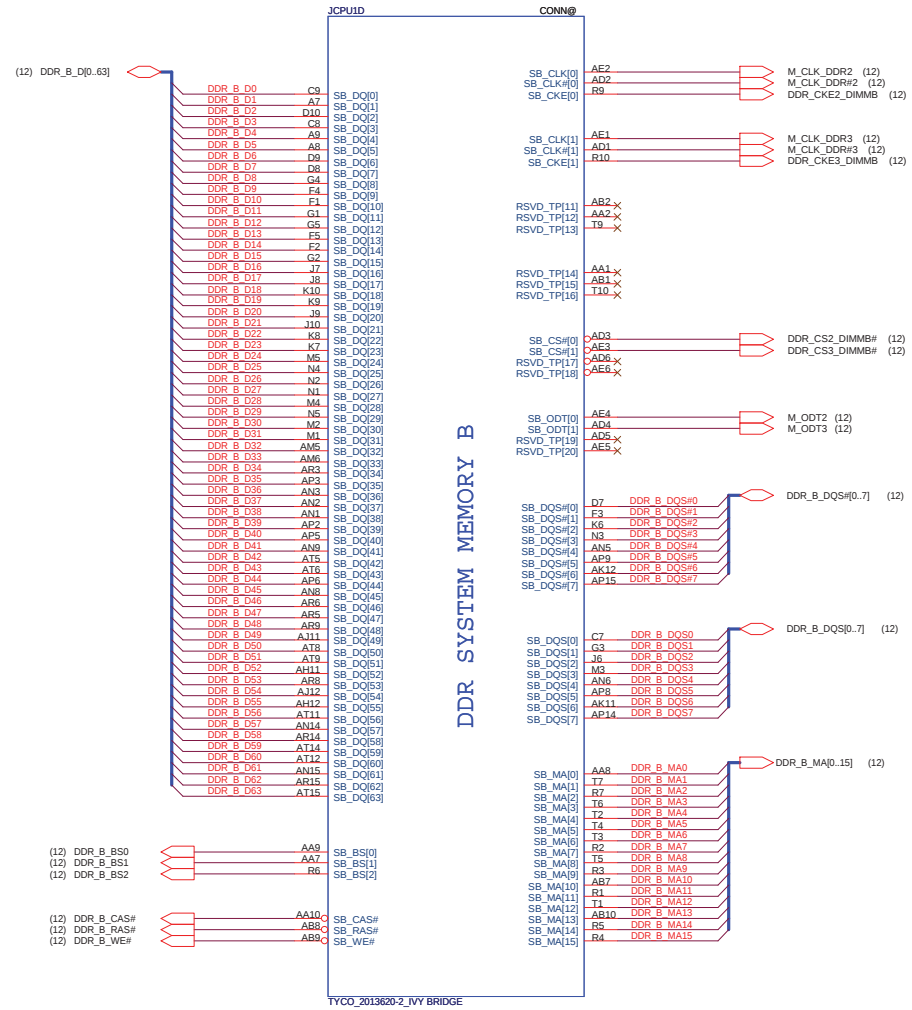
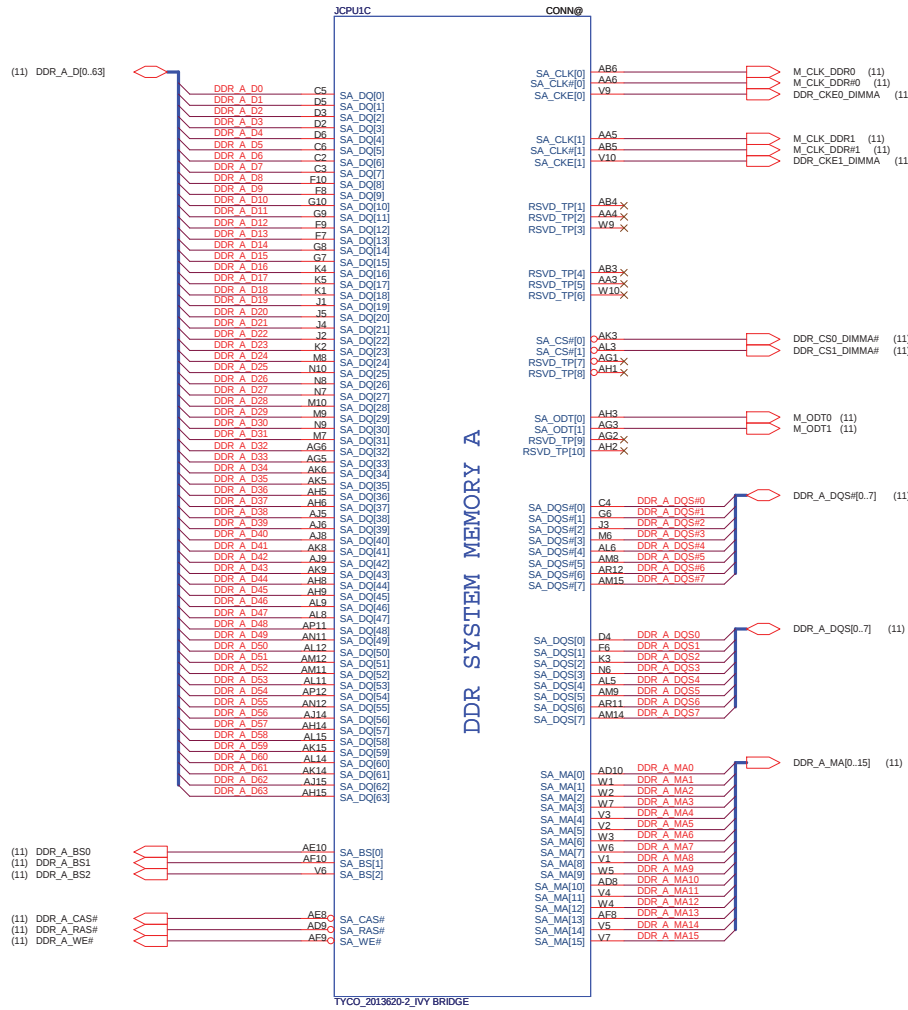


PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

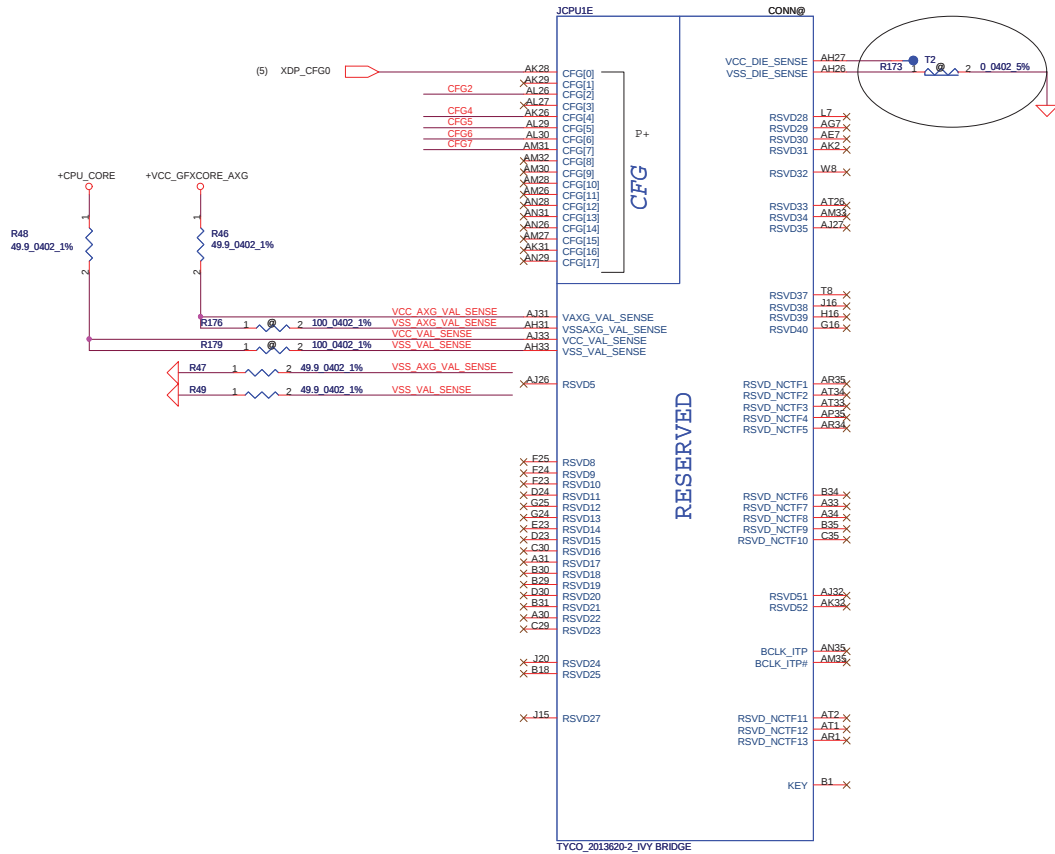
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	★ 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
------	--

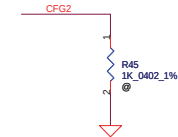




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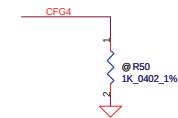


CFG Straps for Processor



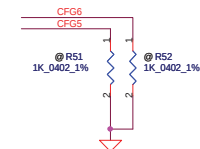
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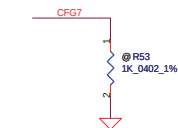
Display Port Presence Strap

CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
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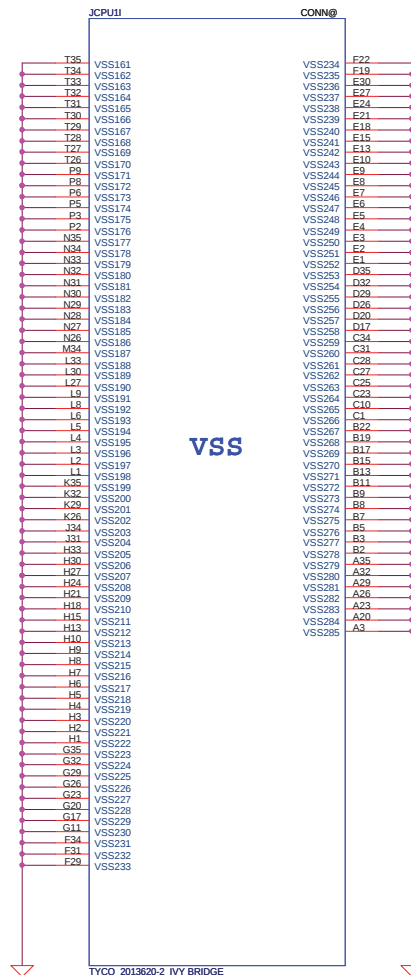
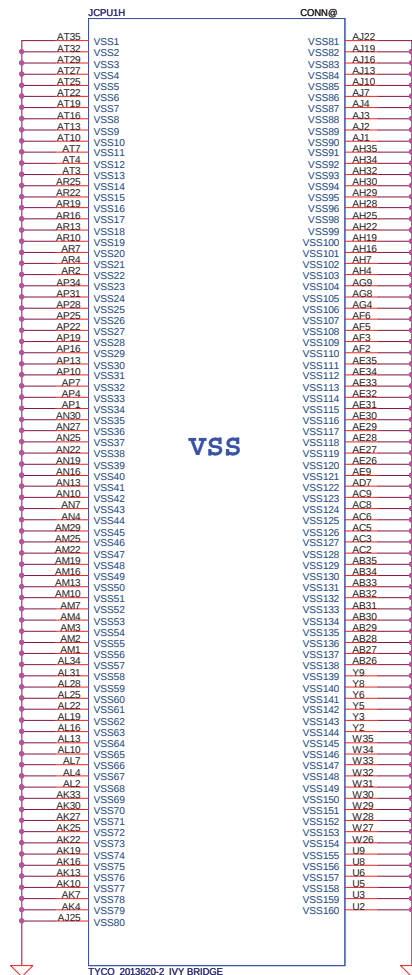
PCIe Port Bifurcation Straps

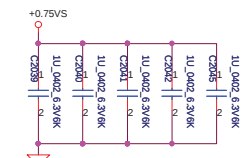
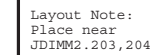
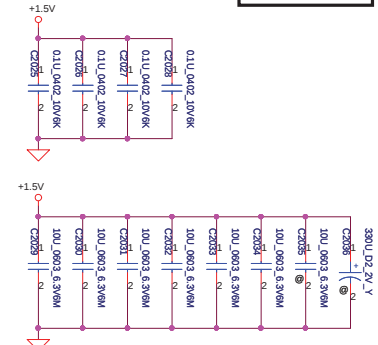
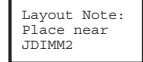
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
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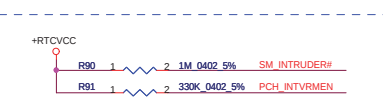
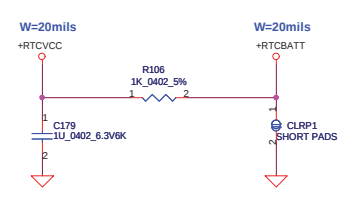
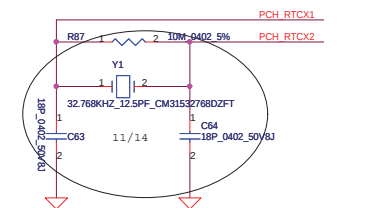


PEG DEFER TRAINING

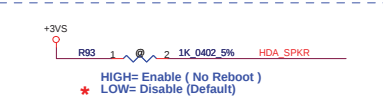
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
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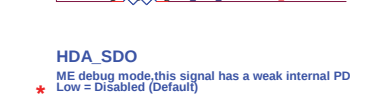




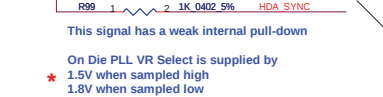
INTVRMEN
★ H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)



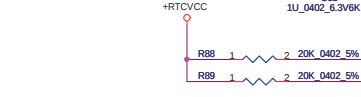
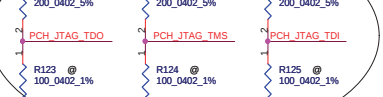
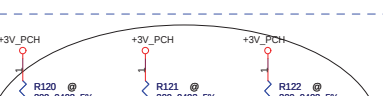
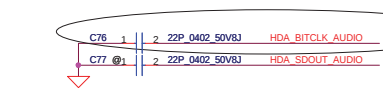
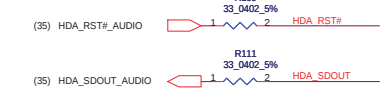
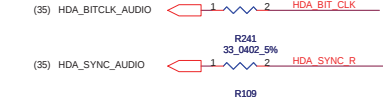
HDA SPKR
★ HIGH= Enable (No Reboot)
★ LOW= Disable (Default)



HDA SDO
★ ME debug mode, this signal has a weak internal PD
Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Override]



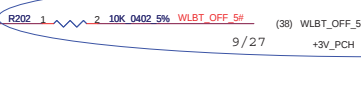
HDA SYNC
★ On Die PLL VR Select is supplied by 1.5V when sampled high
1.8V when sampled low
Needs to be pulled High for Huron River platform



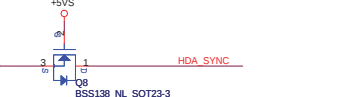
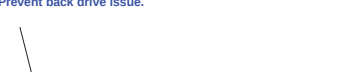
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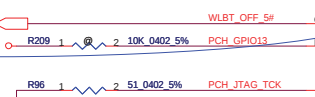
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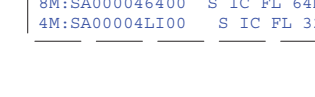
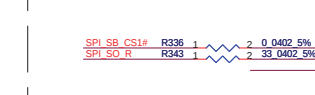
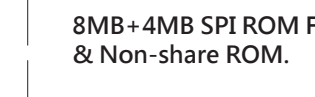
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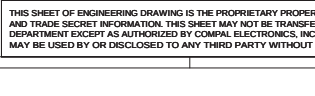
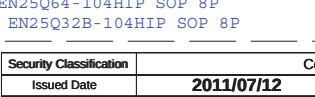
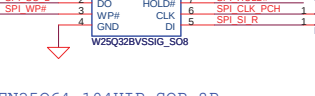
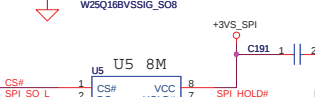
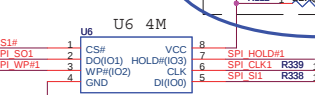
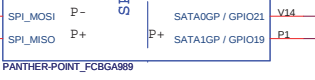
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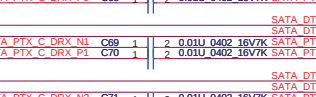
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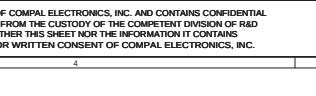
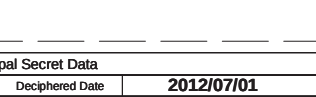
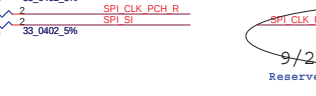
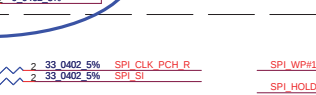
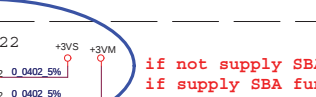
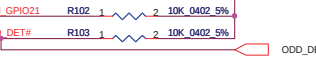
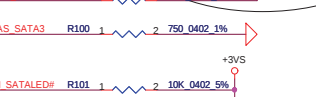
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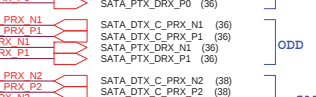
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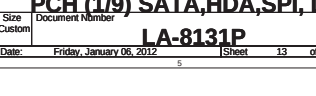
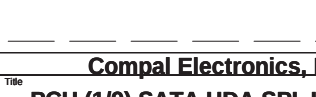
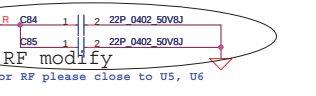
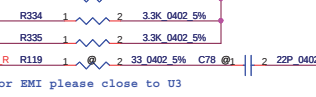
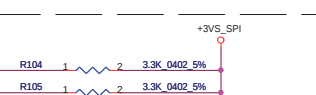
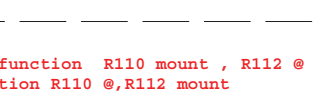
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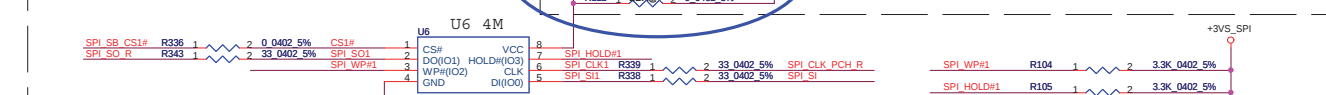
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8MB+4MB SPI ROM FOR 5M ME(SBA) & Non-share ROM.



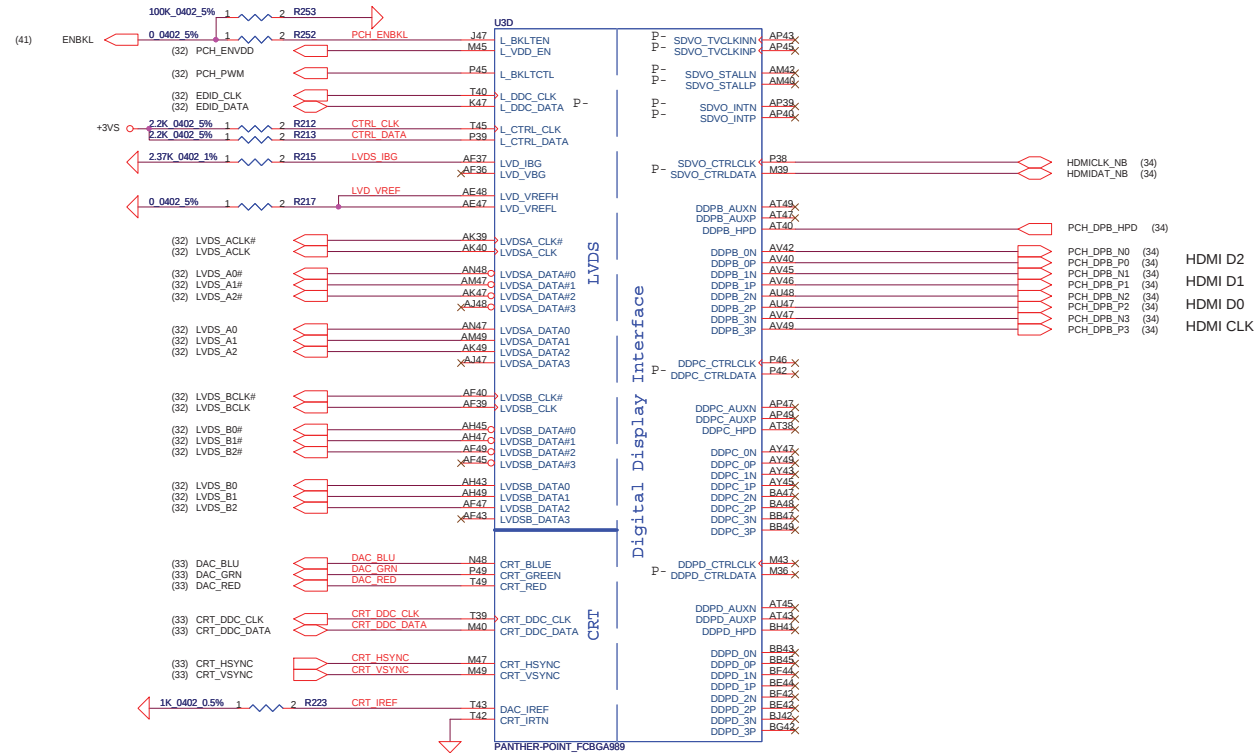
if not supply SBA function R110 mount , R112 @
if supply SBA function R110 @, R112 mount



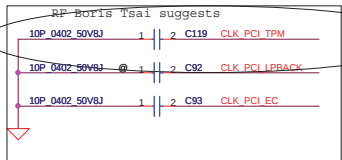
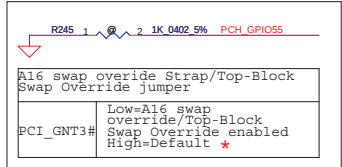
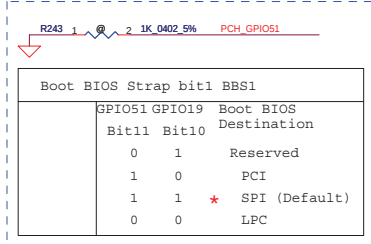
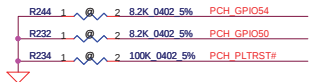
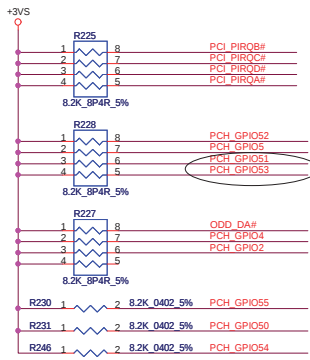
Reserve for EMI please close to U3
Reserve for RF please close to U5, U6

8M:SA000046400 S IC FL 64M EN25Q64-104HIP SOP 8P
4M:SA00004LI00 S IC FL 32M EN25Q32B-104HIP SOP 8P

Security Classification		Compal Secret Data		Title	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Rev	06
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Date:		Friday, January 06, 2012		Sheet 13 of 58	



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	PCH (4/9) LVDS,CRT,DP,HDMI
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				Date: Friday, January 06, 2012	Sheet 16 of 58



- (37) USB3_RX1_N
- (37) USB3_RX2_N
- (37) USB3_RX3_N
- (37) USB3_RX1_P
- (37) USB3_RX2_P
- (37) USB3_RX3_P
- (37) USB3_TX1_N
- (37) USB3_TX2_N
- (37) USB3_TX3_N
- (37) USB3_TX1_P
- (37) USB3_TX2_P
- (37) USB3_TX3_P

- (22) DGPU_HOLD_RST#
- (51) NVDD_PWR_EN
- (22,24) DGPU_PWR_EN

- (38) ST_DET#
- (38) ODD_DA#
- (41) PCI_PME#
- (5) PCH_PLTRST#

- (14) CLK_PCL_LPBACK
- (41) CLK_PCL_EC
- (38,40) CLK_PCL_DB
- (40) CLK_PCL_TPM

- (14) CLK_PCL_LPBACK
- (41) CLK_PCL_EC
- (38,40) CLK_PCL_DB
- (40) CLK_PCL_TPM

- (14) CLK_PCL_LPBACK
- (41) CLK_PCL_EC
- (38,40) CLK_PCL_DB
- (40) CLK_PCL_TPM

- (14) CLK_PCL_LPBACK
- (41) CLK_PCL_EC
- (38,40) CLK_PCL_DB
- (40) CLK_PCL_TPM

- (14) CLK_PCL_LPBACK
- (41) CLK_PCL_EC
- (38,40) CLK_PCL_DB
- (40) CLK_PCL_TPM

- (14) CLK_PCL_LPBACK
- (41) CLK_PCL_EC
- (38,40) CLK_PCL_DB
- (40) CLK_PCL_TPM

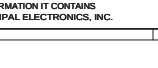
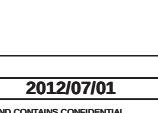
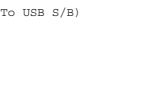
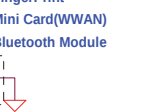
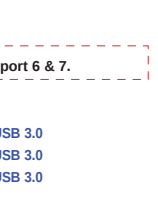
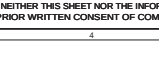
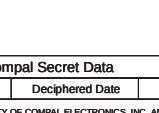
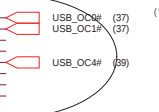
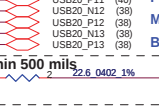
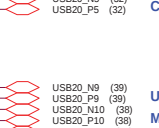
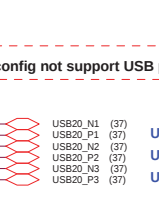
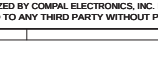
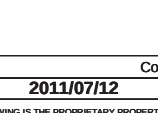
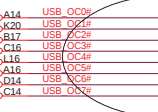
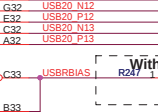
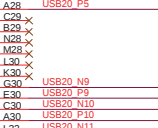
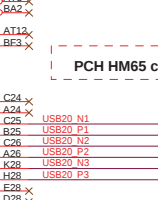
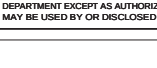
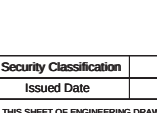
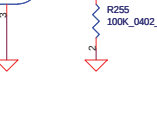
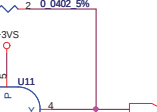
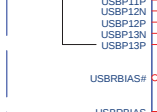
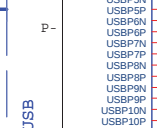
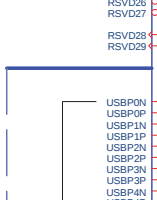
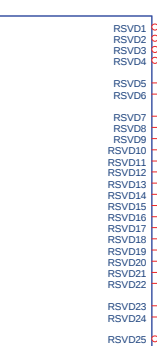
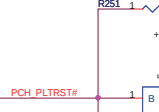
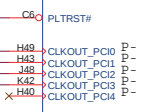
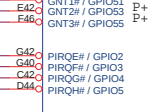
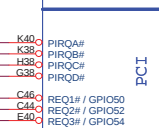
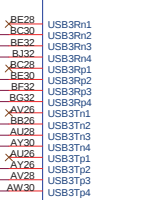
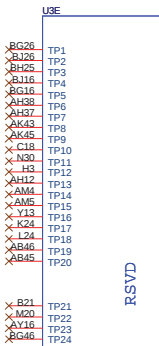
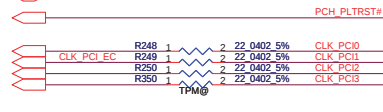
- (14) CLK_PCL_LPBACK
- (41) CLK_PCL_EC
- (38,40) CLK_PCL_DB
- (40) CLK_PCL_TPM

- (14) CLK_PCL_LPBACK
- (41) CLK_PCL_EC
- (38,40) CLK_PCL_DB
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- (41) CLK_PCL_EC
- (38,40) CLK_PCL_DB
- (40) CLK_PCL_TPM

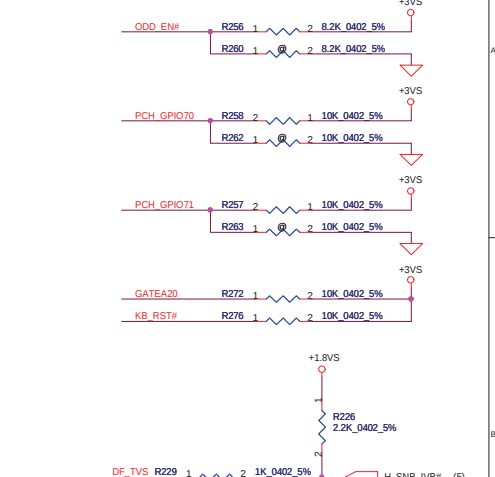
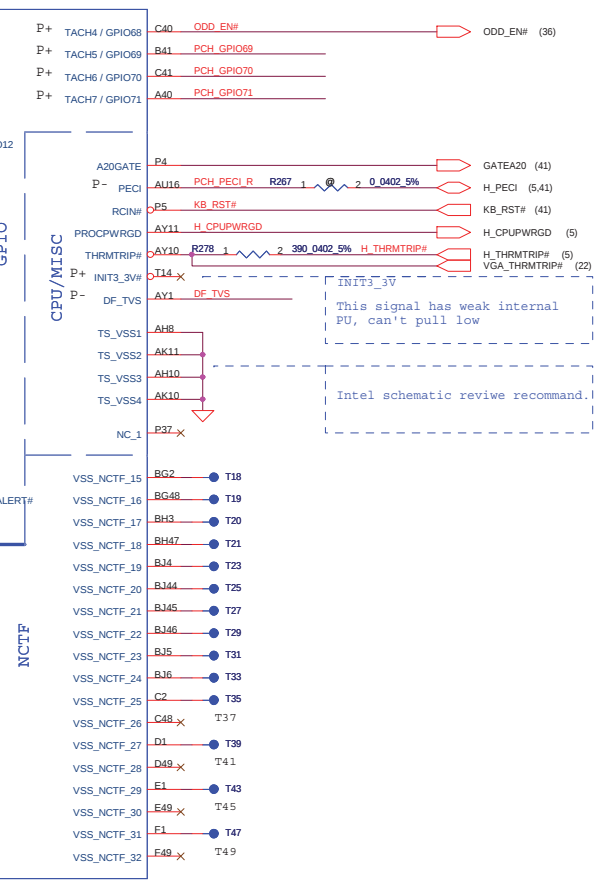
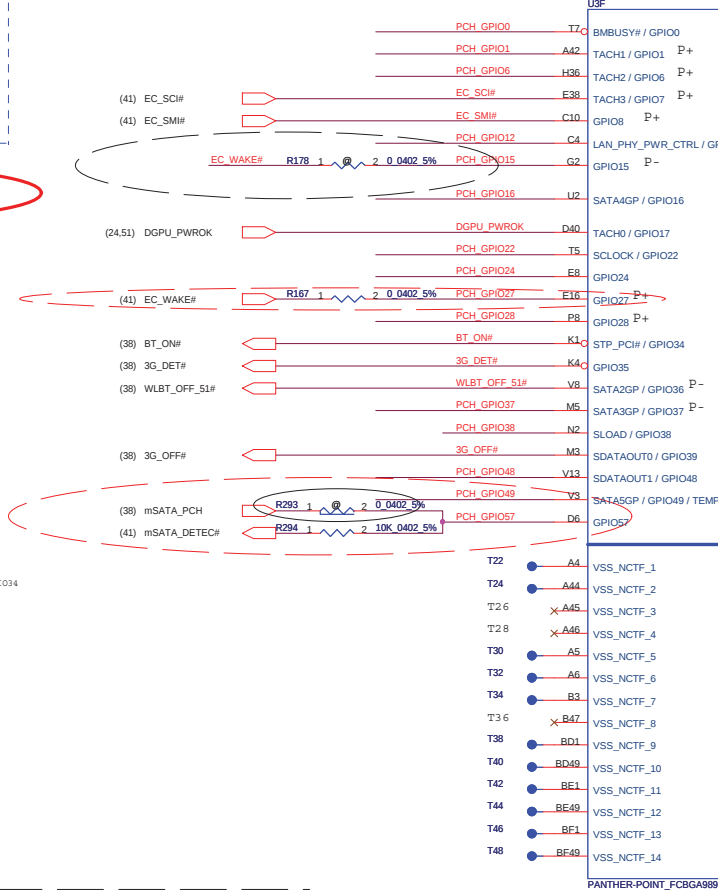
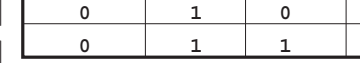
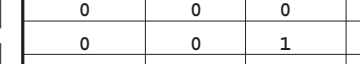
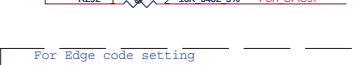
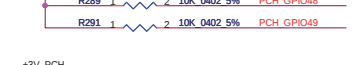
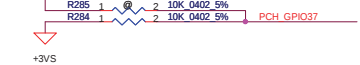
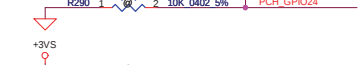
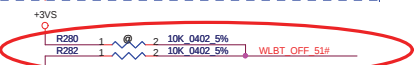
- (14) CLK_PCL_LPBACK
- (41) CLK_PCL_EC
- (38,40) CLK_PCL_DB
- (40) CLK_PCL_TPM



GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable



GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

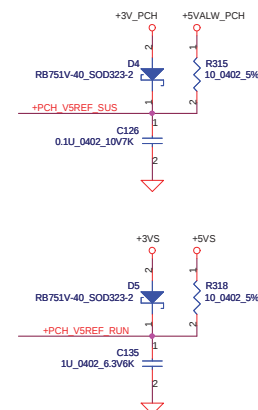


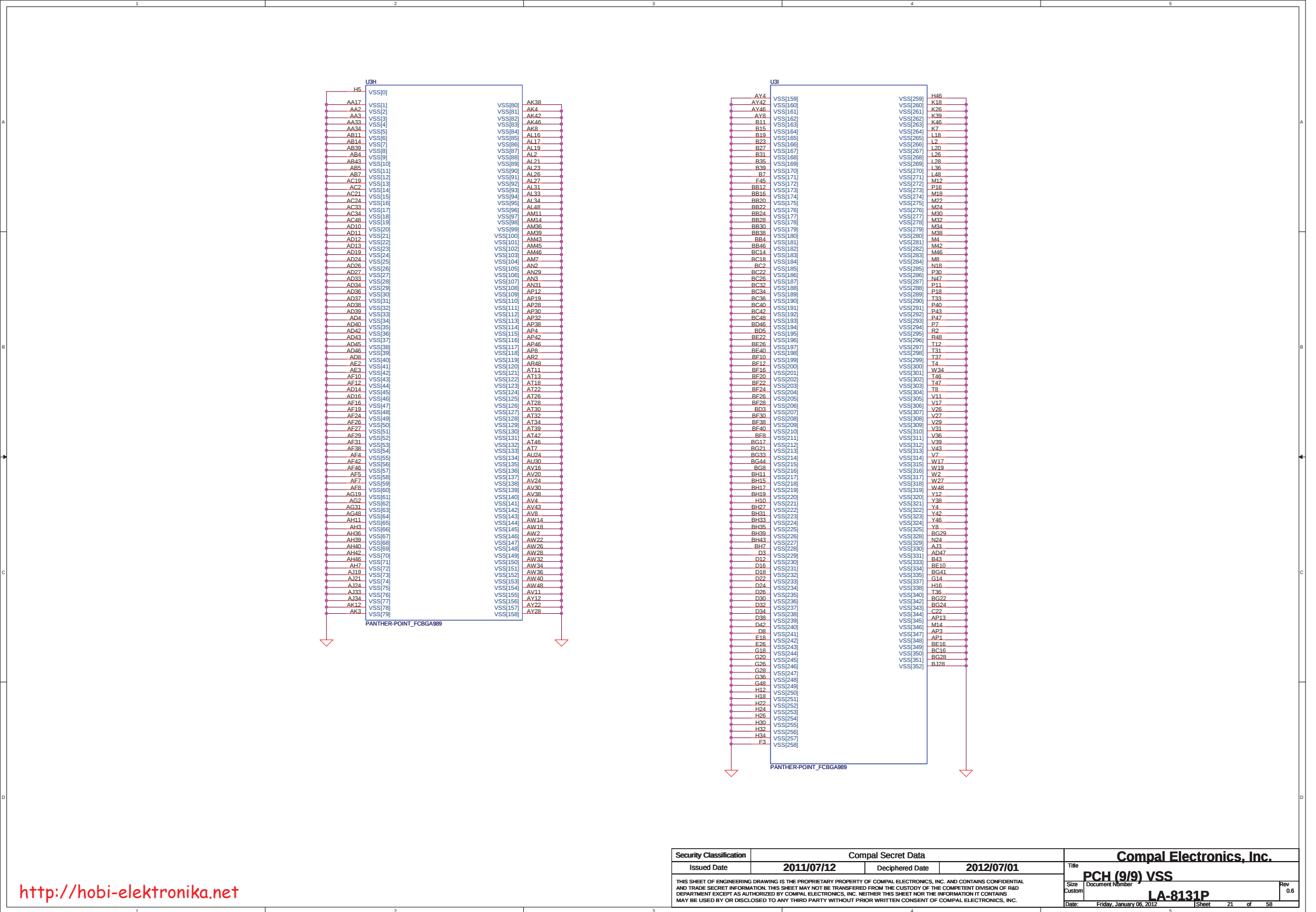
DMI Termination Voltage	
nv_cle	Set to Vcc when HIGH Set to Vss when LOW

For Edge code setting

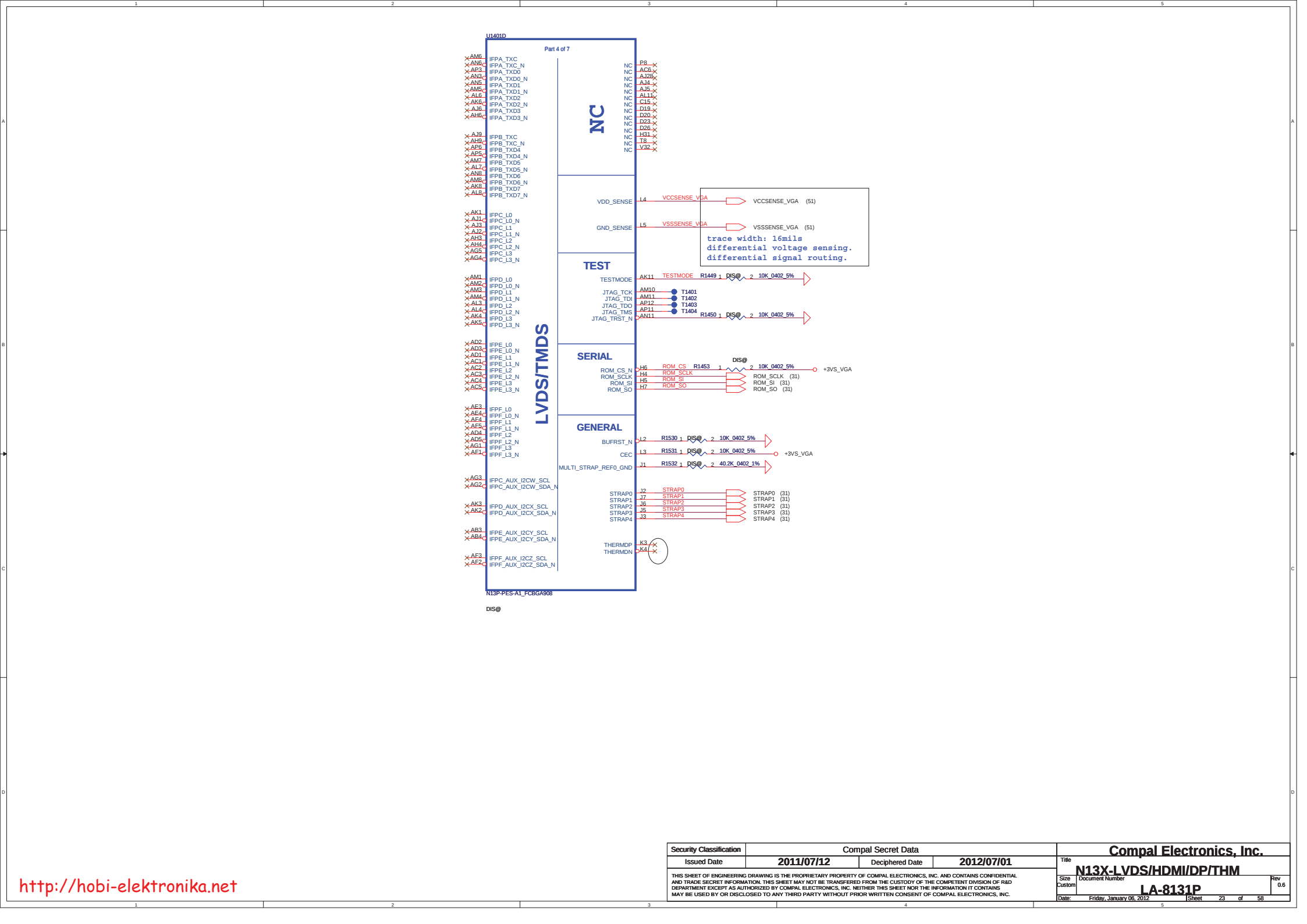
PCH_GPIO69	PCH_GPIO38	PCH_GPIO67	Function
0	0	0	Optimus
0	0	1	Reserved
0	1	0	DIS
0	1	1	UMA

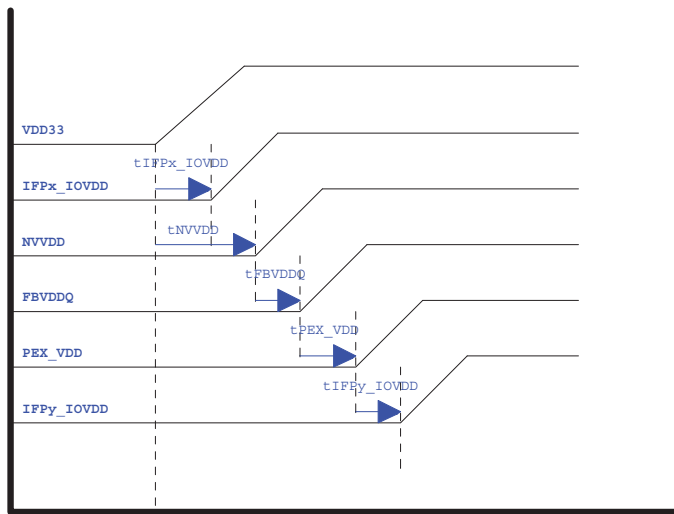
http://hobi-elektronika.net



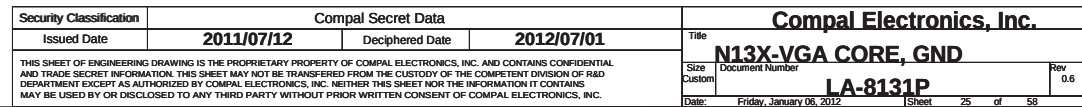






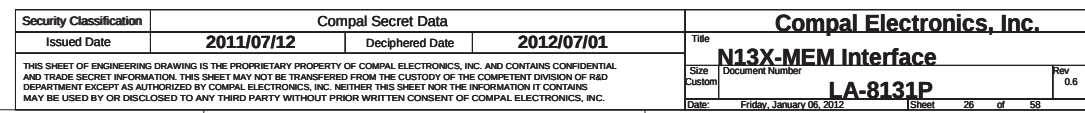
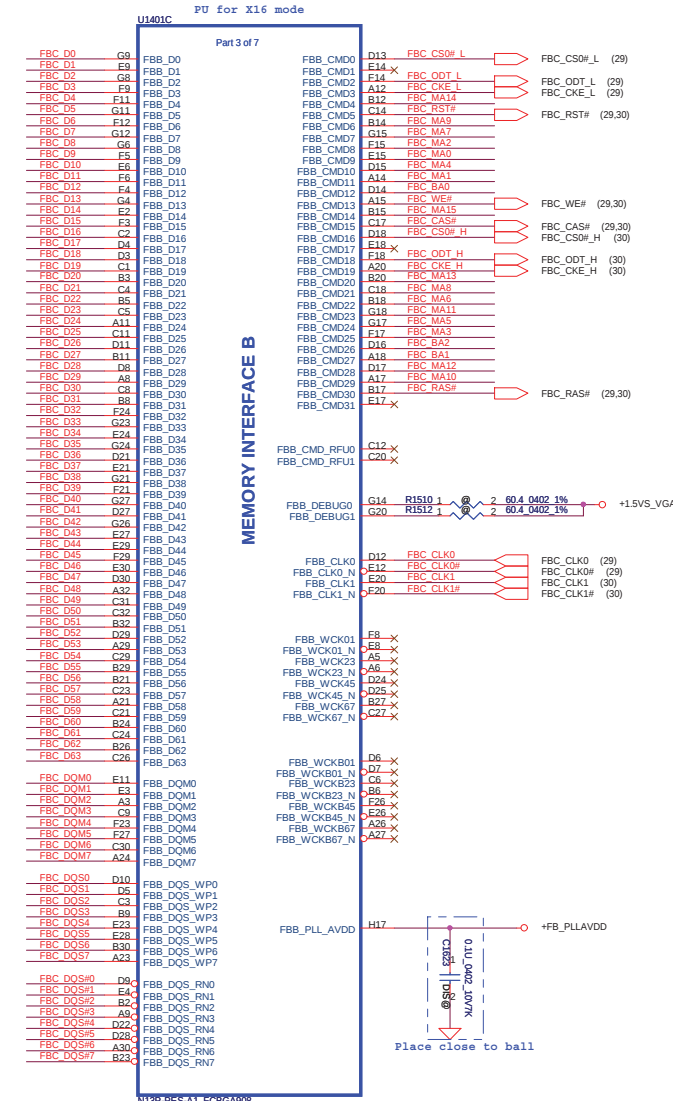


X=A and B
Y=C, D, E and F



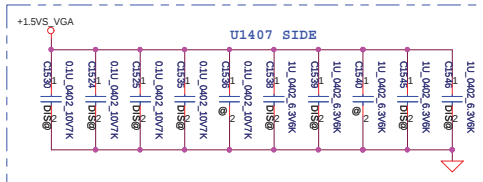
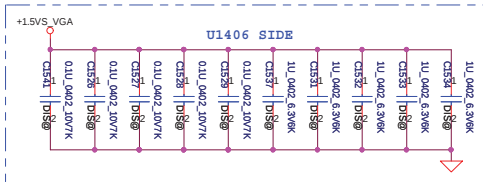
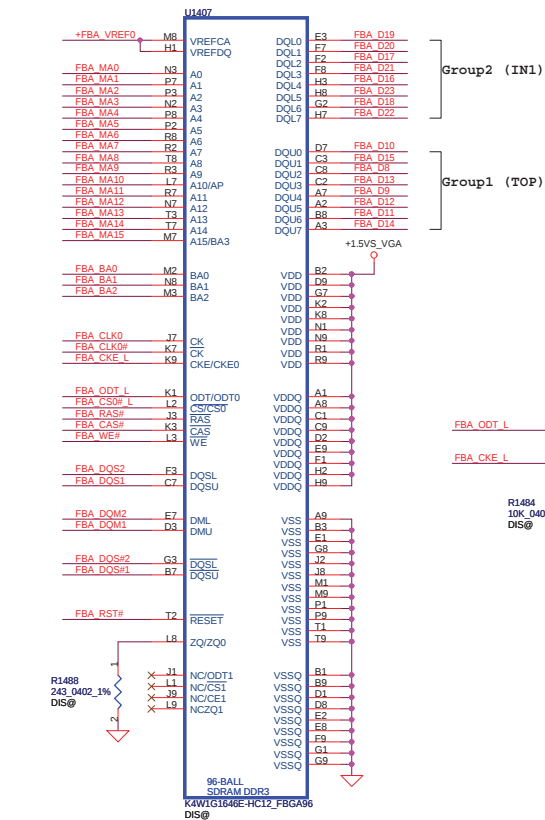
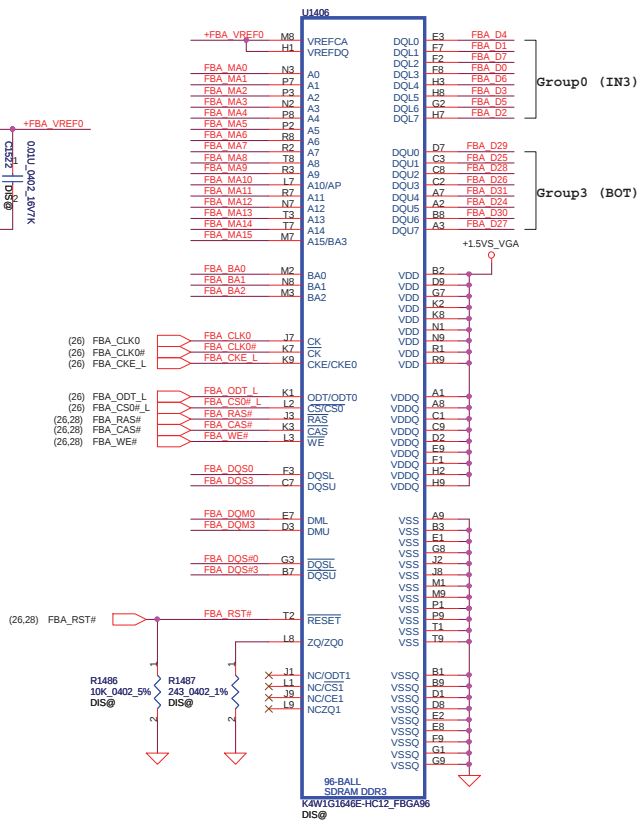


	DATA Bus	
Address	0...31	32...63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

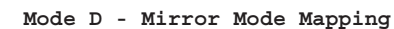
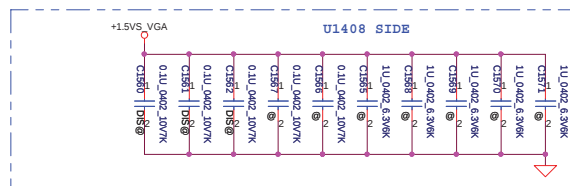
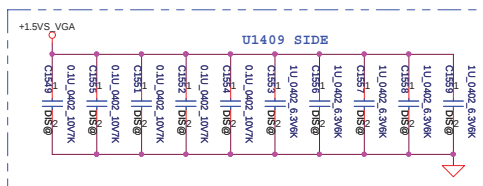


Memory Partition A - Lower 32 bits

- FBA_MA[15..0] (26,28)
- FBA_BA[2..0] (26,28)
- FBA_D[0..63] (26,28)
- FBA_DQM[7..0] (26,28)
- FBA_DQS[7..0] (26,28)
- FBA_DQS# [7..0] (26,28)

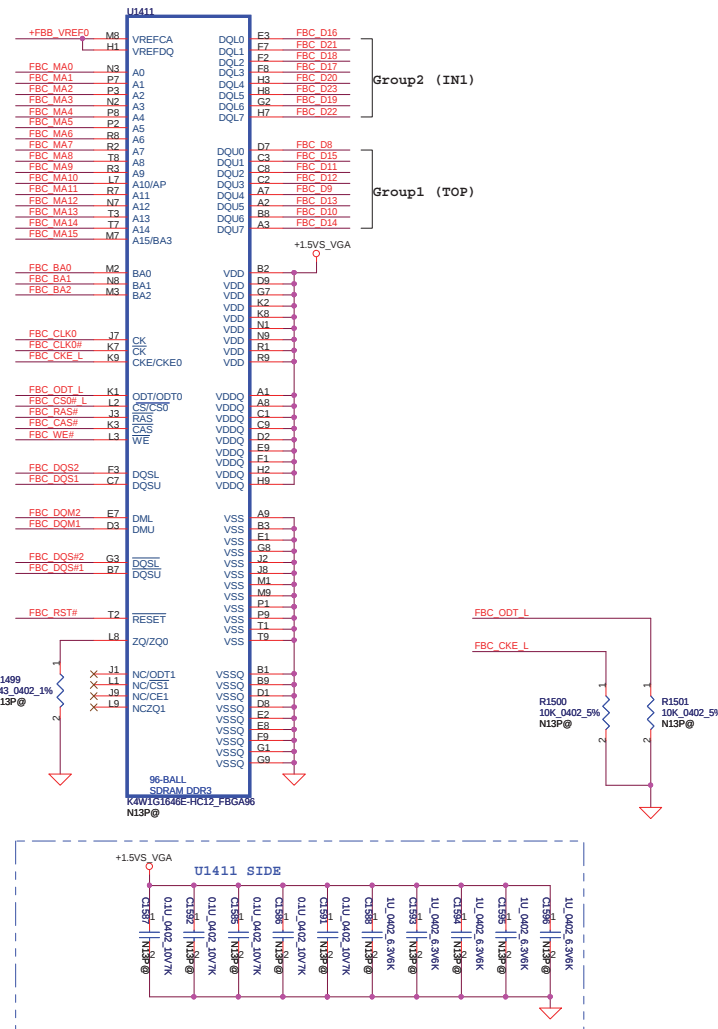
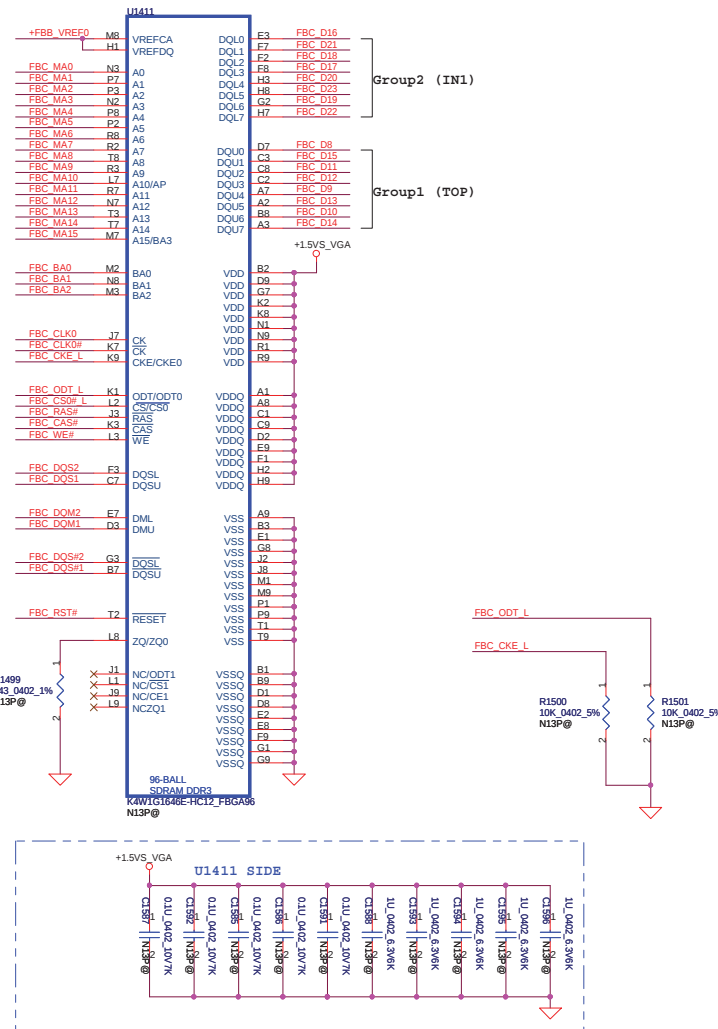


<http://hobi-elektronika.net>



	DATA Bus	
Address	0...31	32...63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

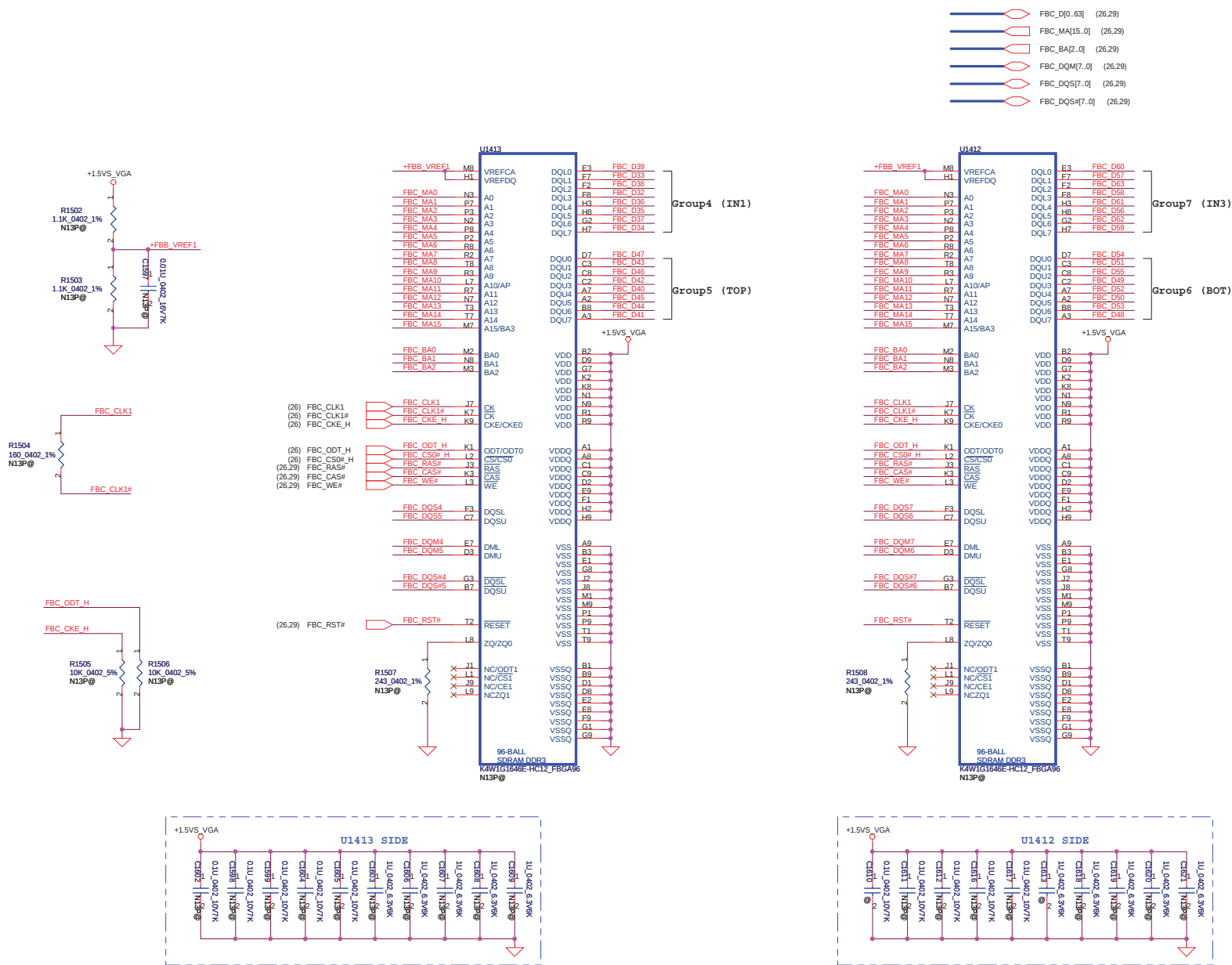
<http://hobi-elektronika.net>



	DATA Bus	
Address	0...31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

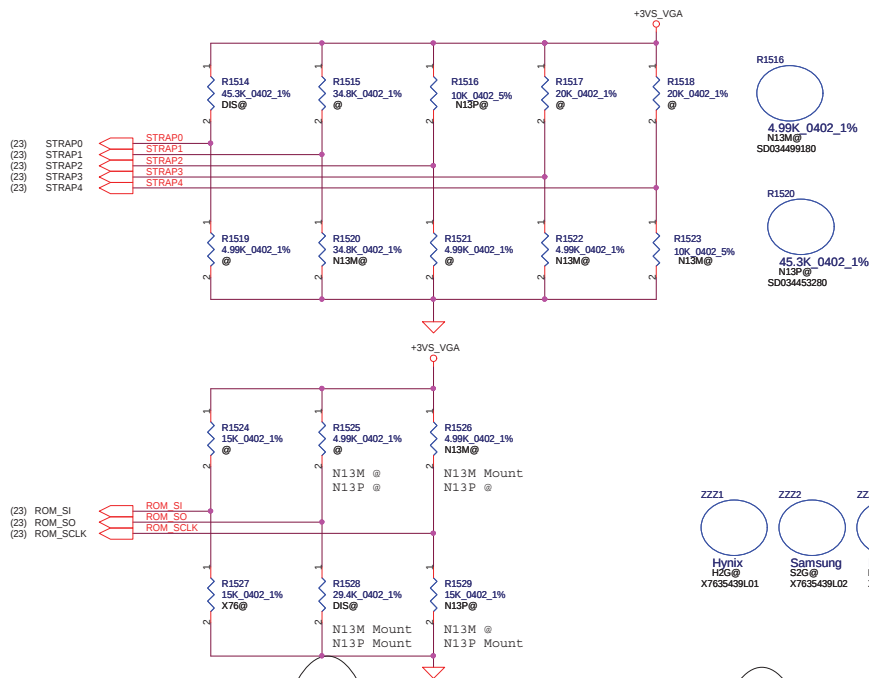
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	N13X-VRAM C Lower	
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				Custom	LA-8131P	0.6
				Date:	Friday, January 06, 2012	Sheet

Memory Partition C - Upper 32 bits



Mode D - Mirror Mode Mapping

DATA Bus	
Address	0..31 32..63
FBx_CMD0	CS0#_L
FBx_CMD1	
FBx_CMD2	ODT_L
FBx_CMD3	CKE_L
FBx_CMD4	A14 A14
FBx_CMD5	RST RST
FBx_CMD6	A9 A9
FBx_CMD7	A7 A7
FBx_CMD8	A2 A2
FBx_CMD9	A0 A0
FBx_CMD10	A4 A4
FBx_CMD11	A1 A1
FBx_CMD12	BA0 BA0
FBx_CMD13	WE# WE#
FBx_CMD14	A15 A15
FBx_CMD15	CAS# CAS#
FBx_CMD16	CS0#_H
FBx_CMD17	
FBx_CMD18	ODT_H
FBx_CMD19	CKE_H
FBx_CMD20	A13 A13
FBx_CMD21	A8 A8
FBx_CMD22	A6 A6
FBx_CMD23	A11 A11
FBx_CMD24	A5 A5
FBx_CMD25	A3 A3
FBx_CMD26	BA2 BA2
FBx_CMD27	BA1 BA1
FBx_CMD28	A12 A12
FBx_CMD29	A10 A10
FBx_CMD30	RAS# RAS#



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

USER Straps	
User[3:0]	
1000-1100	Customer defined

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

GPU	FB Memory gDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GL	Samsung 900MHz	K4W1G1646G-BC11	PD 10K	PD 15K	PD 20K	PU 45K	PD 45K	PU 10K	NC	NC
		64Mx16						PU 45K(ES)		
	Hynix 900MHz	H5TQ1G63DFR-11C	PD 10K	PD 15K	PD 15K	PU 45K	PD 45K	PU 10K	NC	NC
		64Mx16						PU 45K(ES)		
	Samsung 900MHz	K4W2G1646C-HC11	PD 10K	PD 15K	PD 45K	PU 45K	PD 45K	PU 10K	NC	NC
		128Mx16						PU 45K(ES)		
	Hynix 900MHz	H5TQ2G63BFR-11C	PD 10K	PD 15K	PD 35K	PU 45K	PD 45K	PU 10K	NC	NC
		128Mx16						PU 45K(ES)		

GPU	FB Memory gDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13M-GE1	Samsung 900MHz	K4W1G1646G-BC11	PD 30K	PU 5K	PD 20K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
		64Mx16								
	Hynix 900MHz	H5TQ1G63DFR-11C	PD 30K	PU 5K	PD 15K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
		64Mx16								
	Samsung 900MHz	K4W2G1646C-HC11	PD 30K	PU 5K	PD 45K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
		128Mx16								
	Hynix 900MHz	H5TQ2G63BFR-11C	PD 30K	PU 5K	PD 35K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
		128Mx16								

9/27
from 15K to 5K

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				Sheet 31 of 58	LA-8131P



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10



11

(16) DAC_RED
(16) DAC_GRN
(16) DAC_BLU

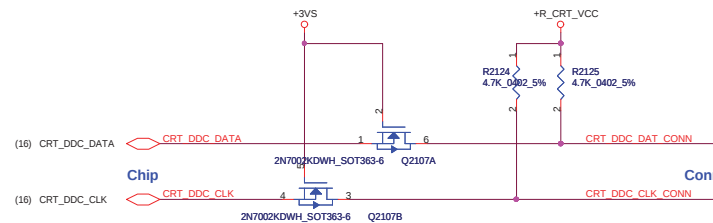
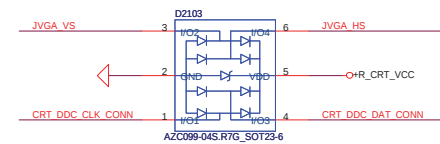
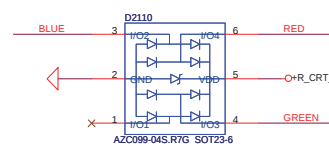
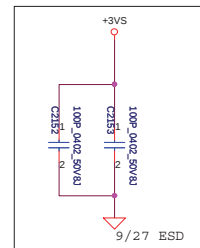
DAC_RED
DAC_GRN
DAC_BLU

(16) CRT_HSYNC

CRT_HSYNC

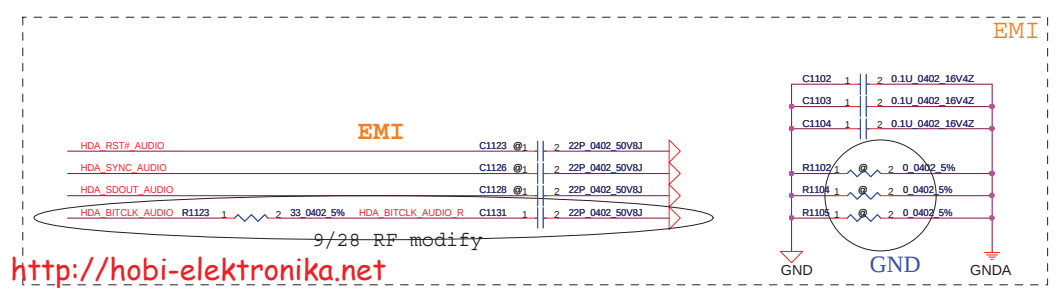
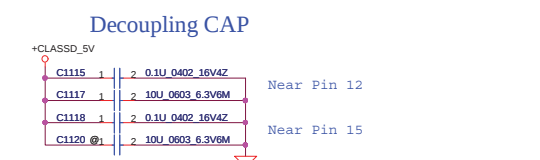
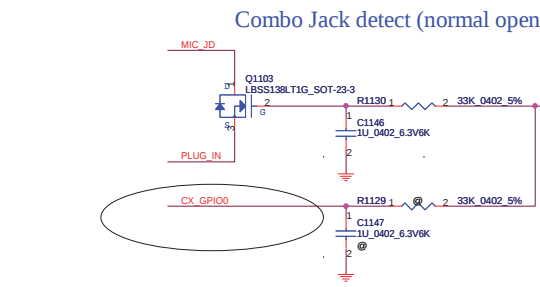
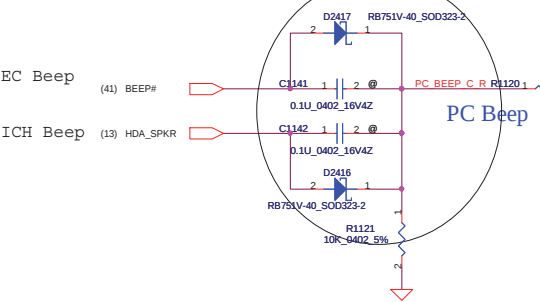
(16) CRT_VSYNC

CRT_VSYNC



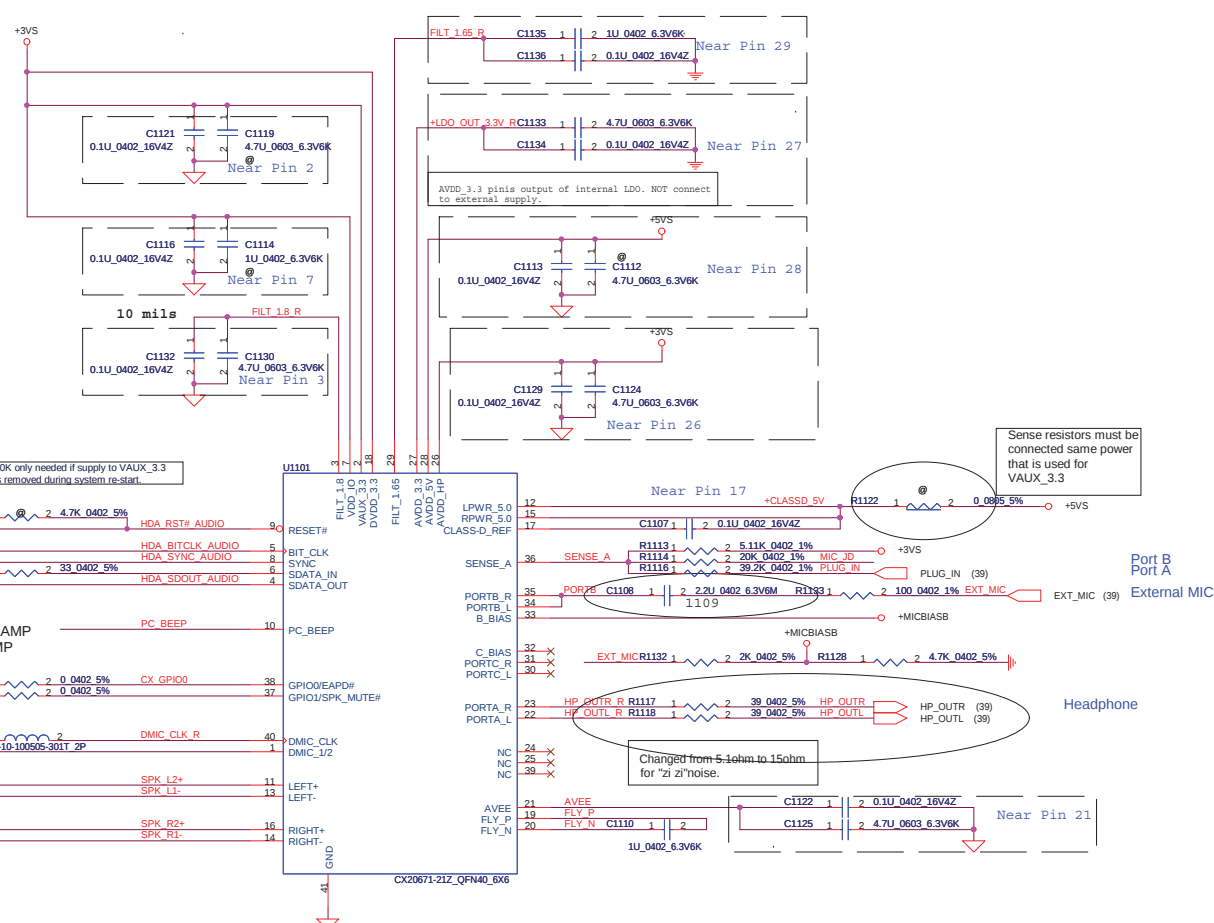
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				Document Number	LA-8131P
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				Rev	0.6

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



Layout Note: Path from +5VS to Pin12, Pin15 must be very low resistance (<0.01 ohms)

To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 & VDD_IO pins must be powered by a rail that is not removed unless AC power is removed. *DSH paget2 has more detail.



Internal Speaker

SP02000N010
SP02000SM10

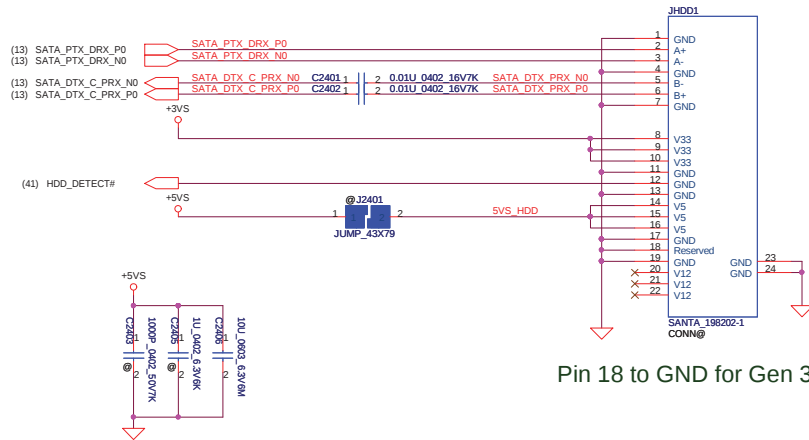
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EMI

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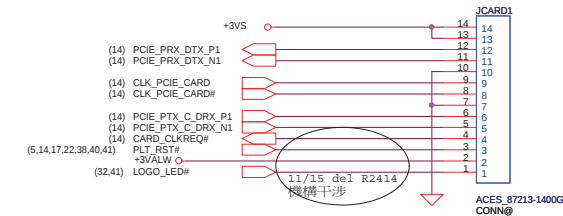
SATA HDD CONN.

PN:DC010004C00



Card Reader CONN.

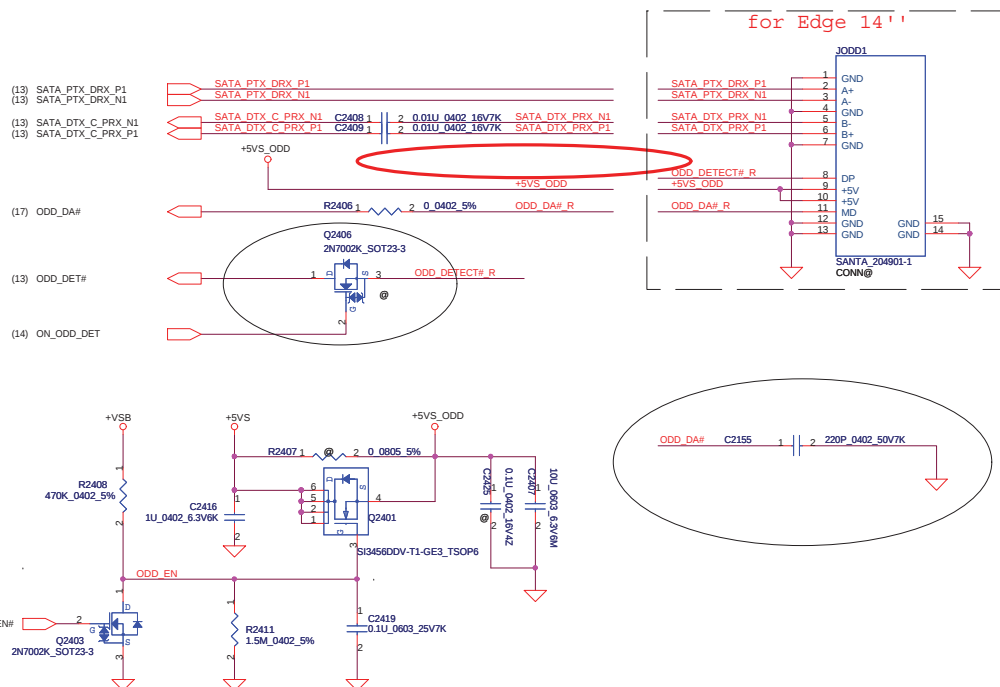
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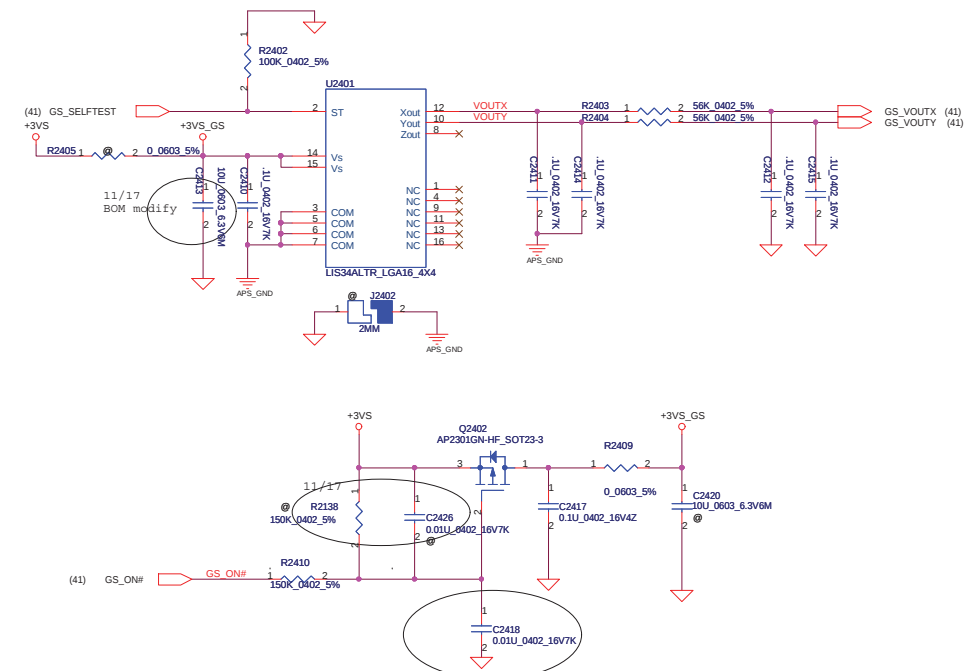
10/06
change PN to SP02000H810
footprint: ACES_87213-1400G_14P

SATA ODD CONN.

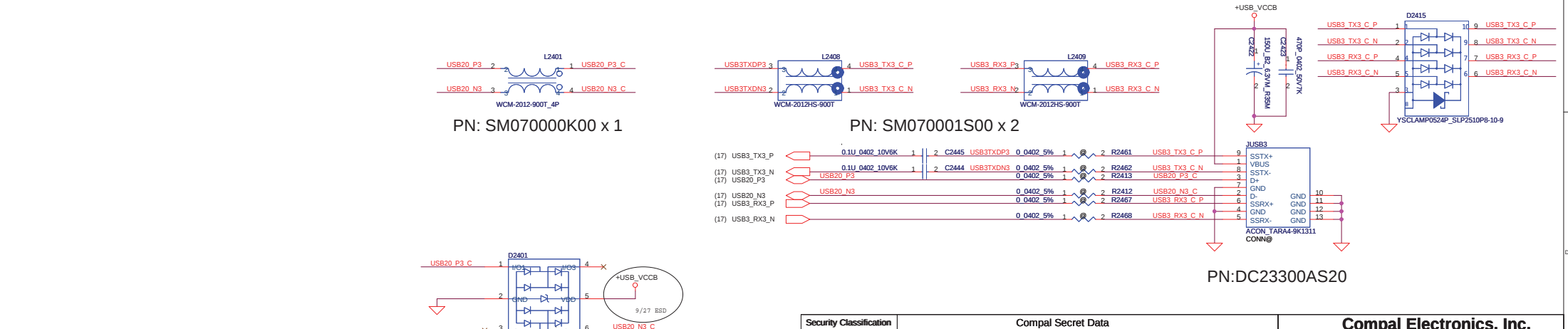
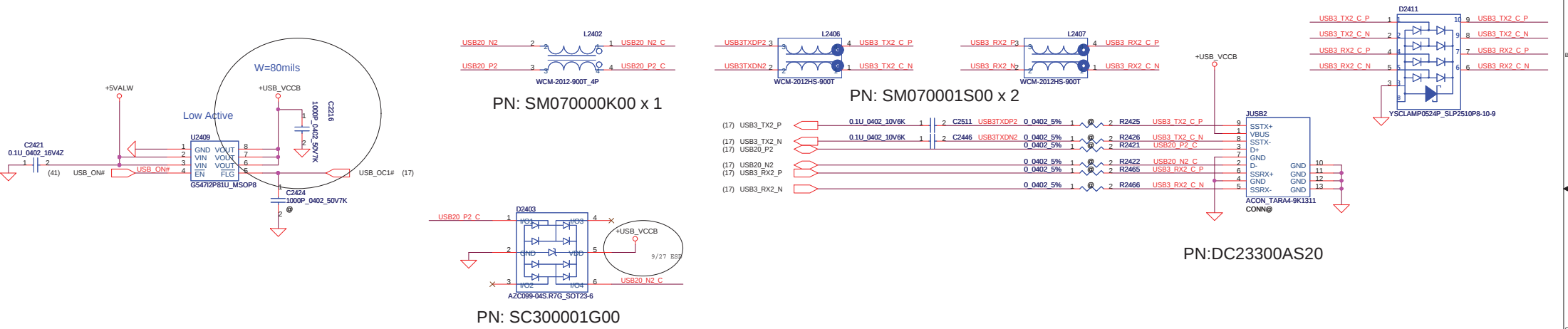
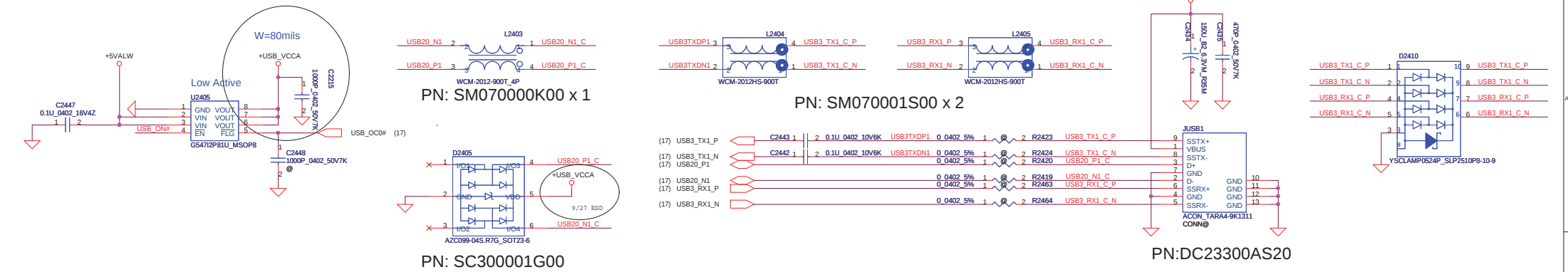
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APS G-Sensor



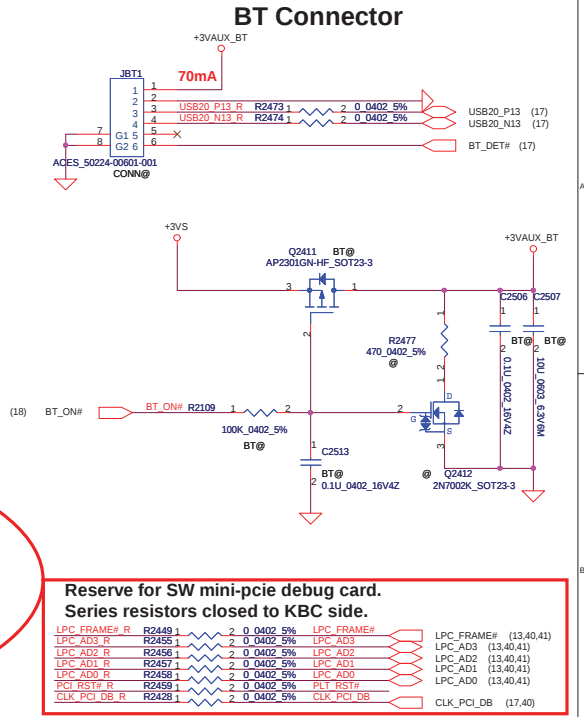
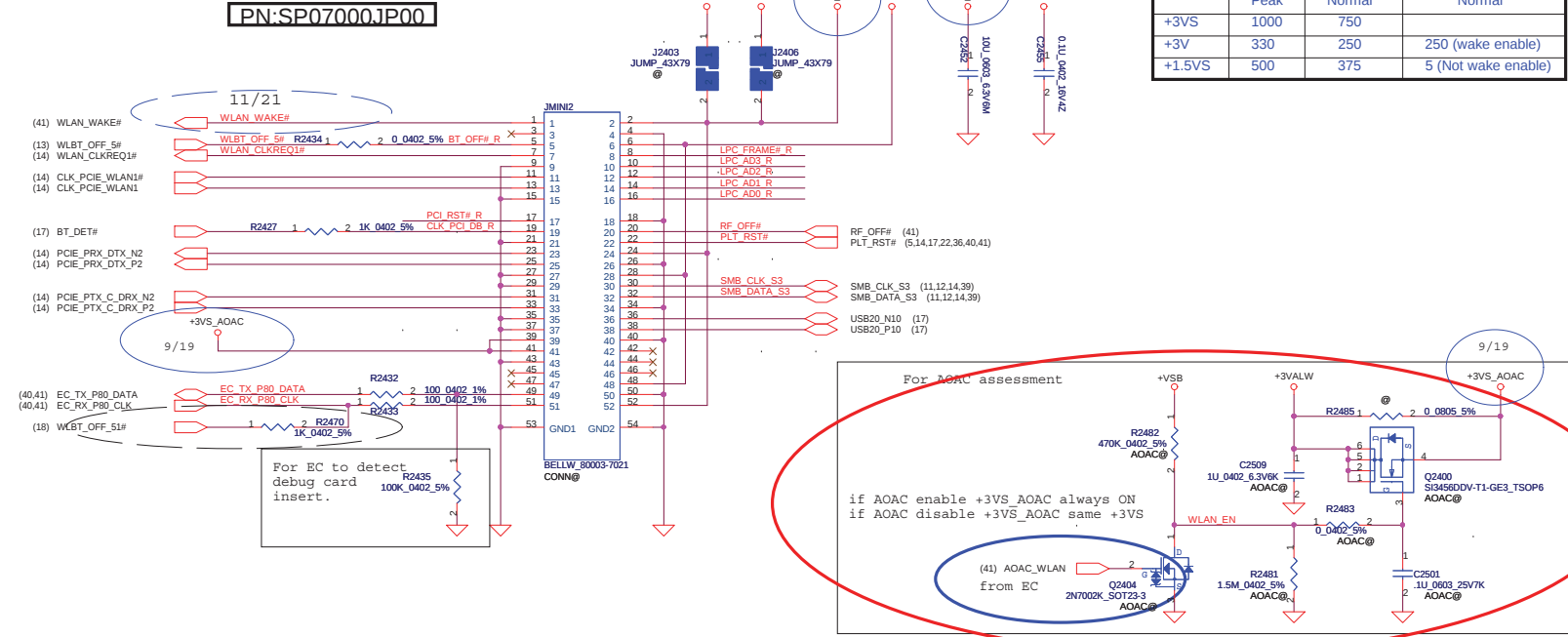
USB 3.0 Conn.



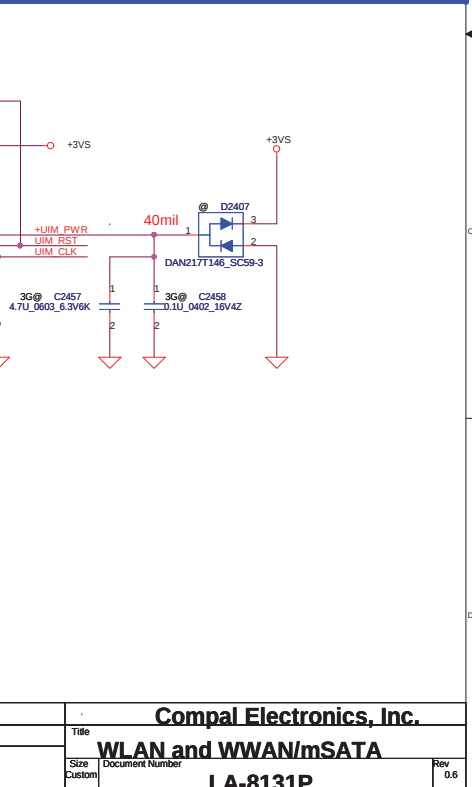
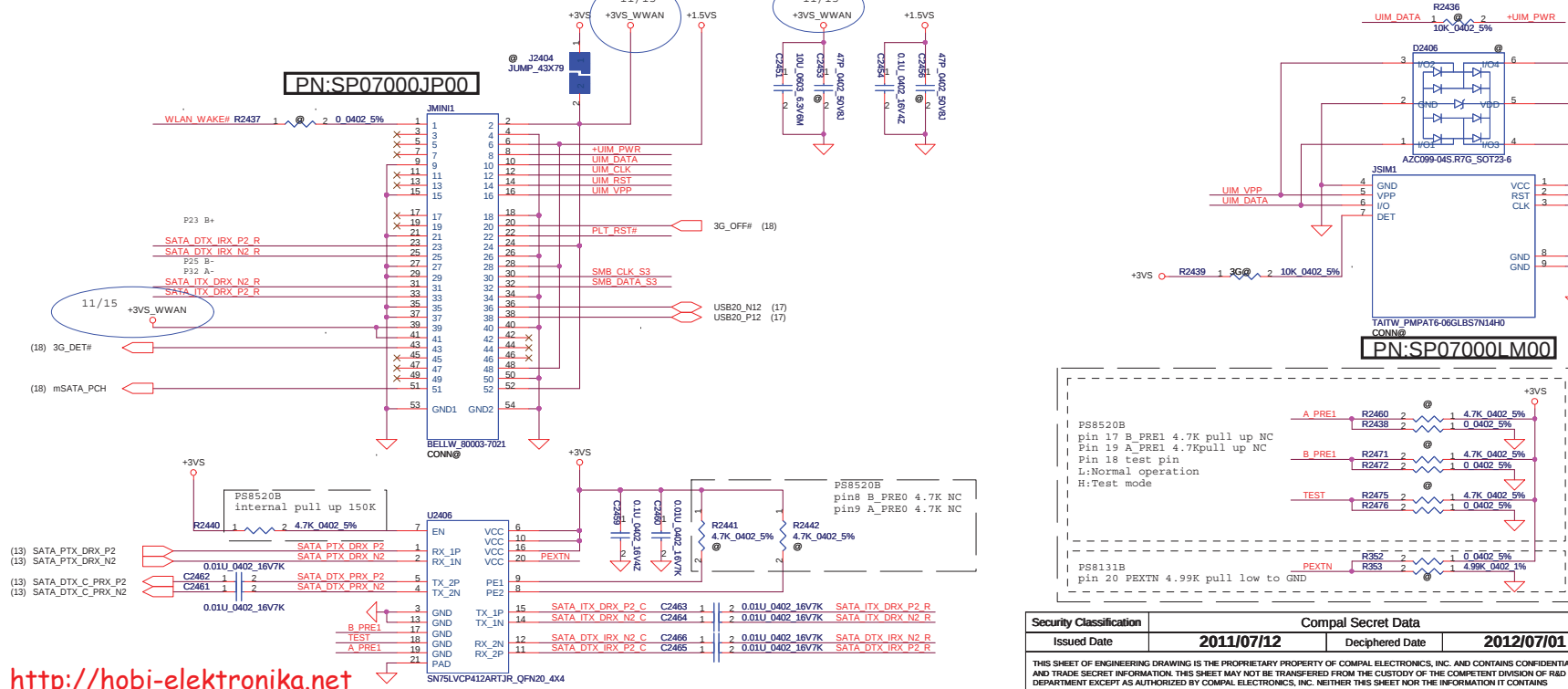
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				Custom	LA-8131P
				Date	Friday, January 06, 2012
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Mini-Express Card for WLAN/WiMAX(Half)

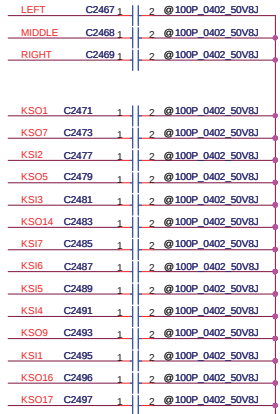
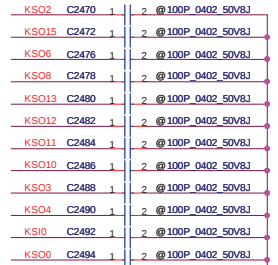
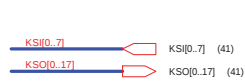
Mini-Express Card(WLAN/WiMAX)



Mini-Express Card for WWAN/mSATA(Full)

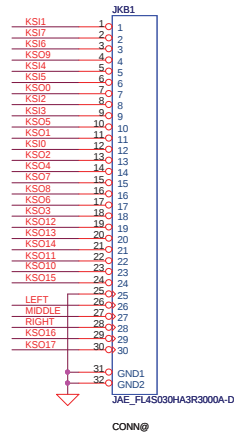


INT_KBD Conn.



M1(Left BUTTON)
M2(Center BUTTON)
M3(Right BUTTON)

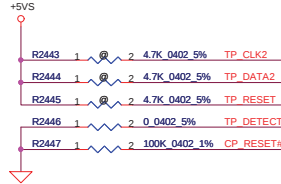
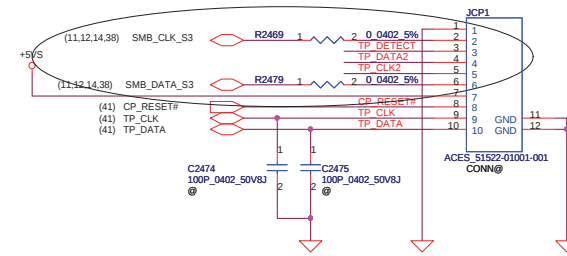
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CONN@

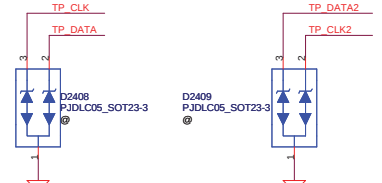
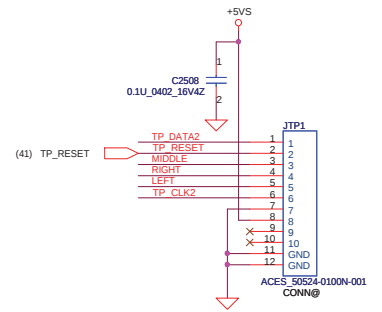
Click pad

PN:SP01001AL00



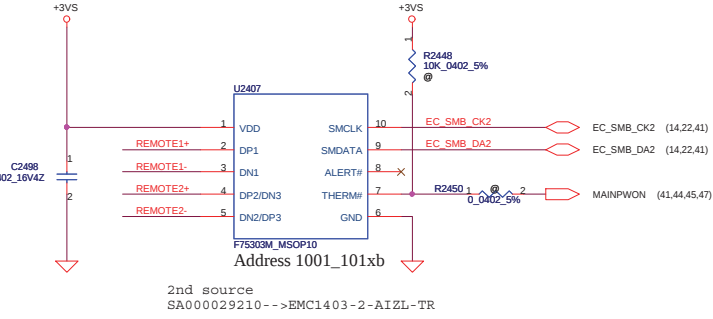
Track point

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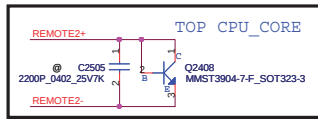
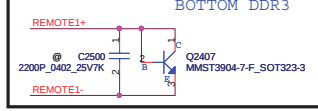
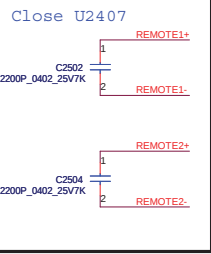


PN: SCA00000U10 X 2

Fintek thermal sensor placed near by TOP DDR3

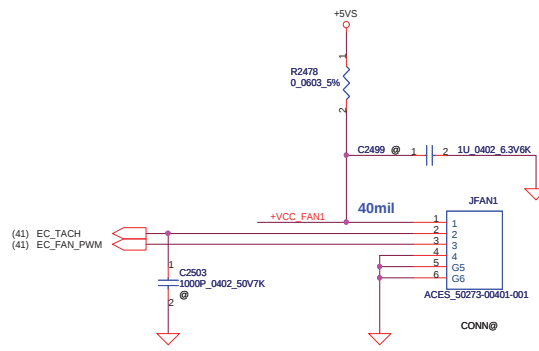


2nd source
SA000029210-->EMC1403-2-AIZL-TR



REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

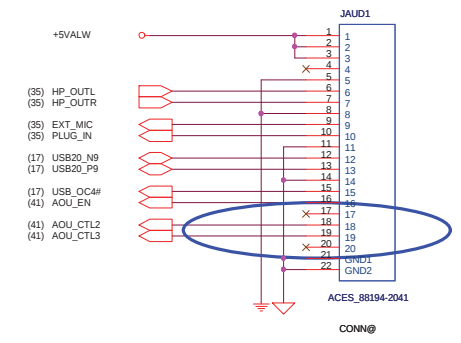
FAN CONN.



PN:SP02000U900

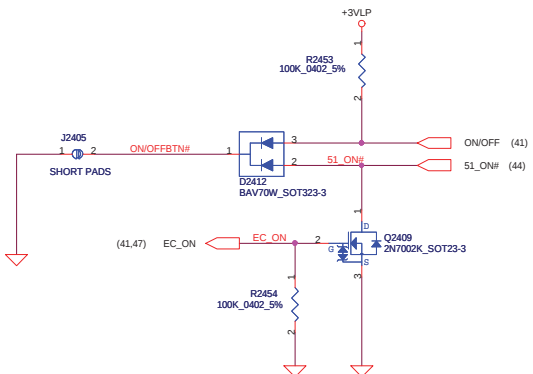
Audio Board

PN:SP011108040

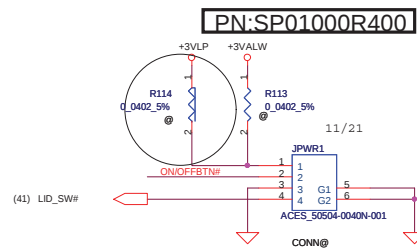


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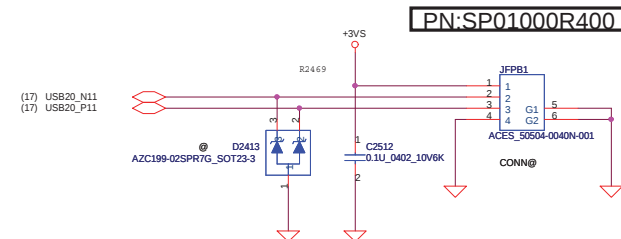
Power Button



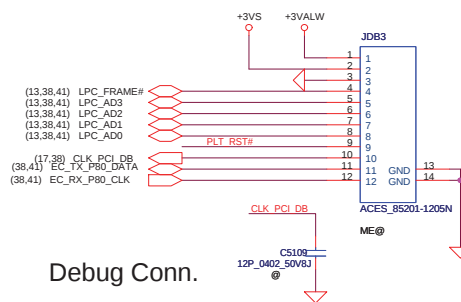
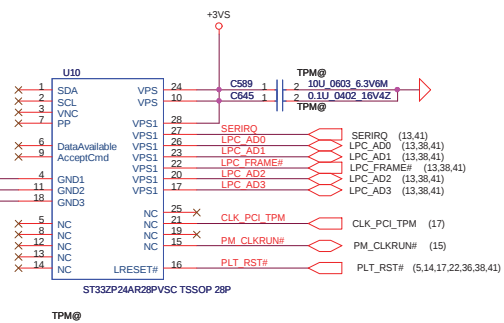
Power Button CONN.



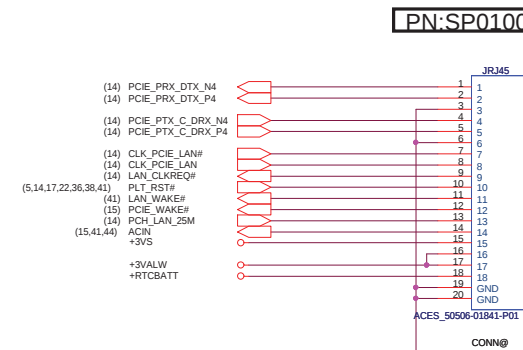
Finger Print Board



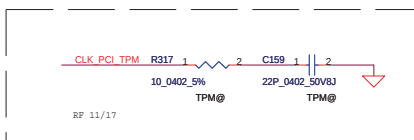
TPM



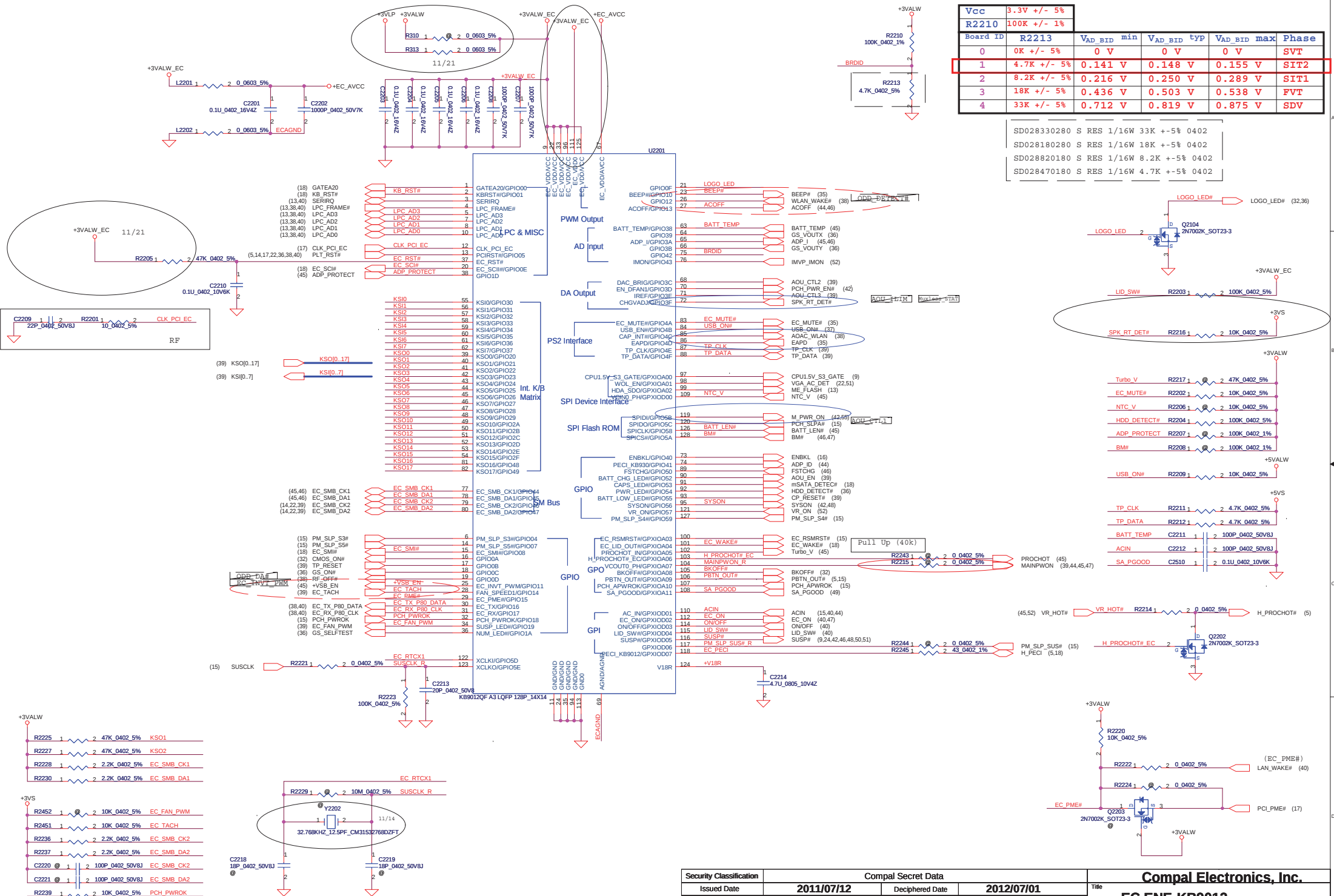
RJ45 Board



Debug Conn.



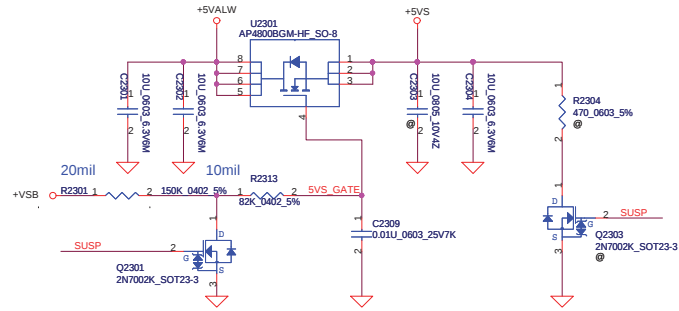
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	PWR Button/Power OK/RJ45
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				Custom	0.1
				Date:	Tuesday, January 10, 2012
				Sheet	40 of 58



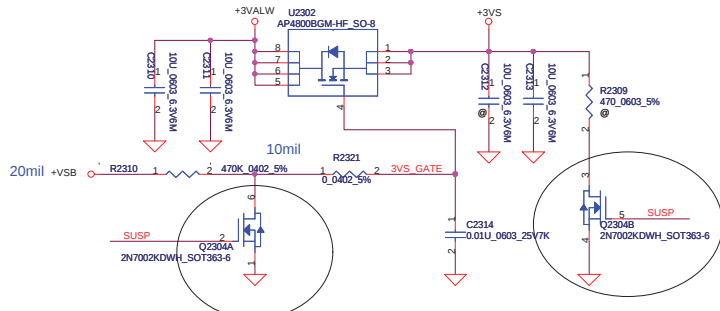
Vcc		3.3V +/- 5%			
R2210		100K +/- 1%			
Board ID	R2213	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SVT
1	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	SIT2
2	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	SIT1
3	18K +/- 5%	0.436 V	0.503 V	0.538 V	FVT
4	33K +/- 5%	0.712 V	0.819 V	0.875 V	SDV

SD028330280	S	RES	1/16W	33K	+/-5%	0402
SD028180280	S	RES	1/16W	18K	+/-5%	0402
SD028820180	S	RES	1/16W	8.2K	+/-5%	0402
SD028470180	S	RES	1/16W	4.7K	+/-5%	0402

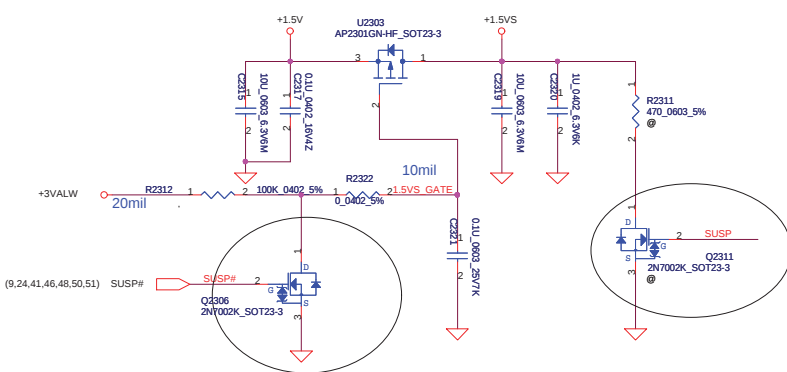
+5VALW TO +5VS



+3VALW TO +3VS

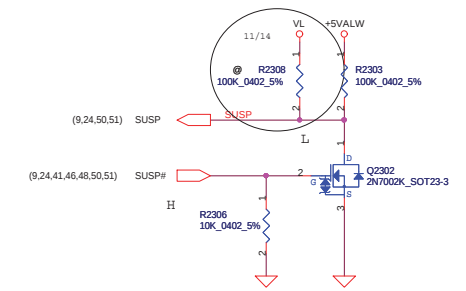
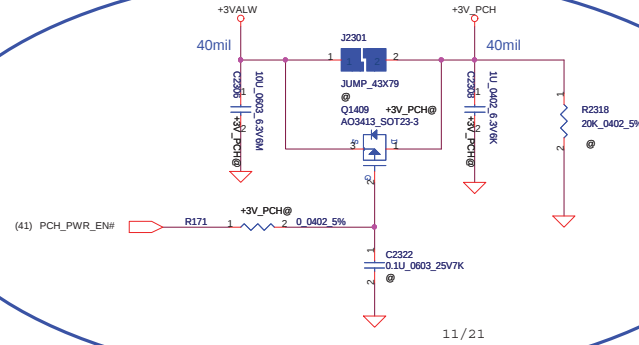


+1.5V to +1.5VS

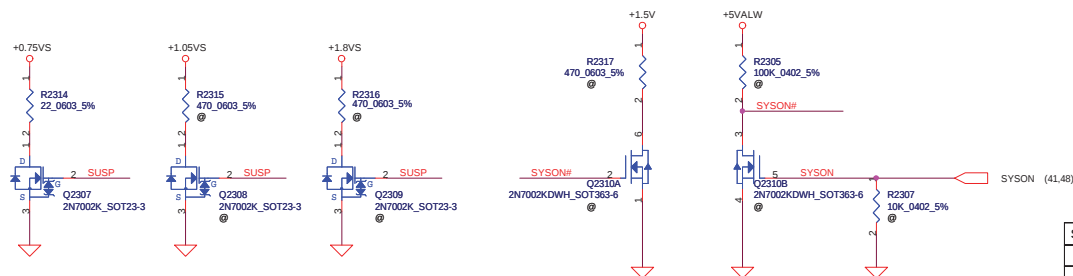
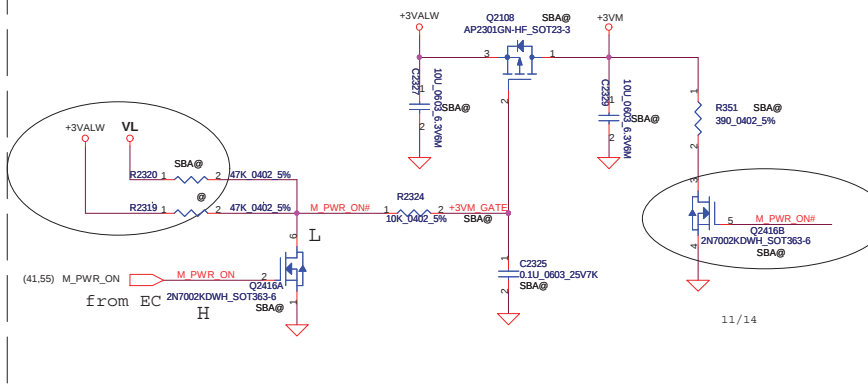


+3VALW TO +3VALW(PCH AUX Power)

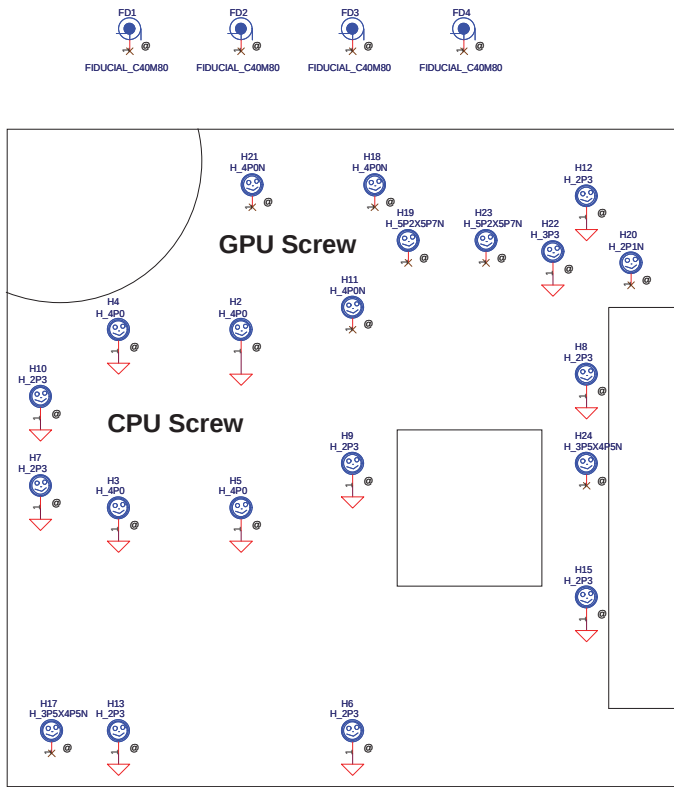
Short J2301 for PCH VCCSUS3.3



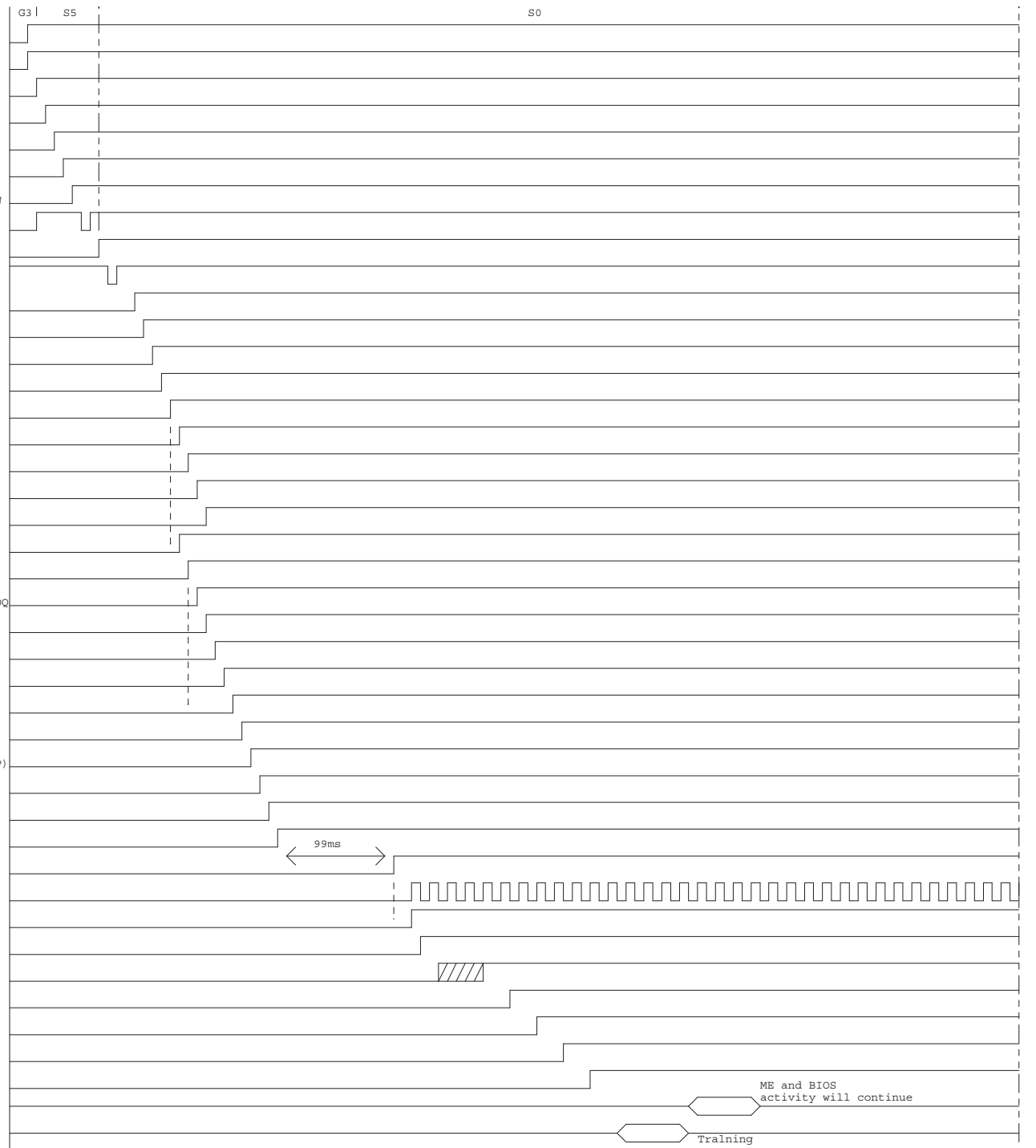
FOR SBA Function POWER(always mount)

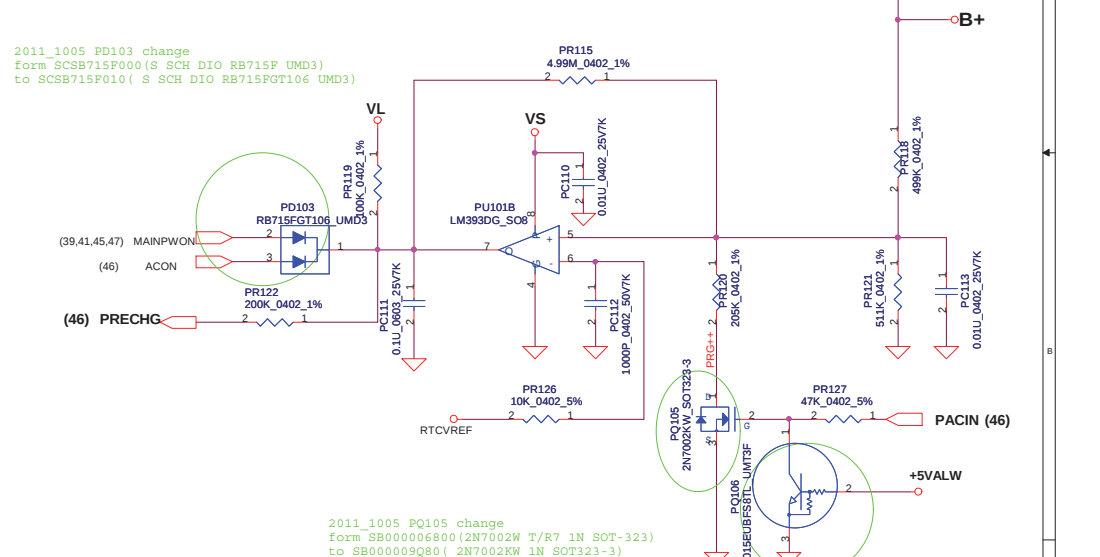
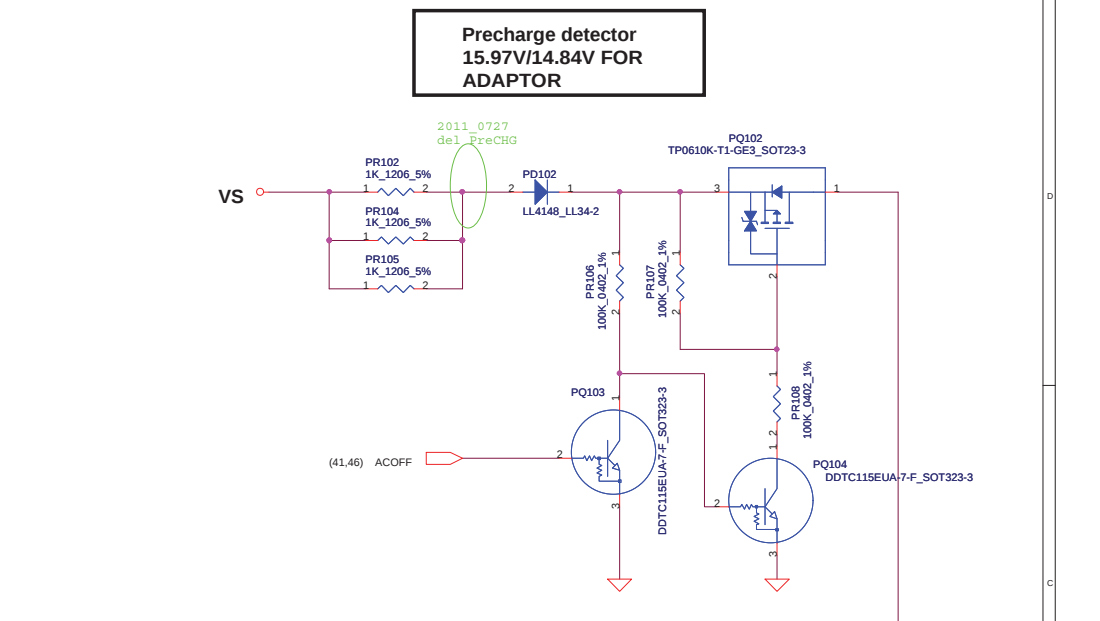
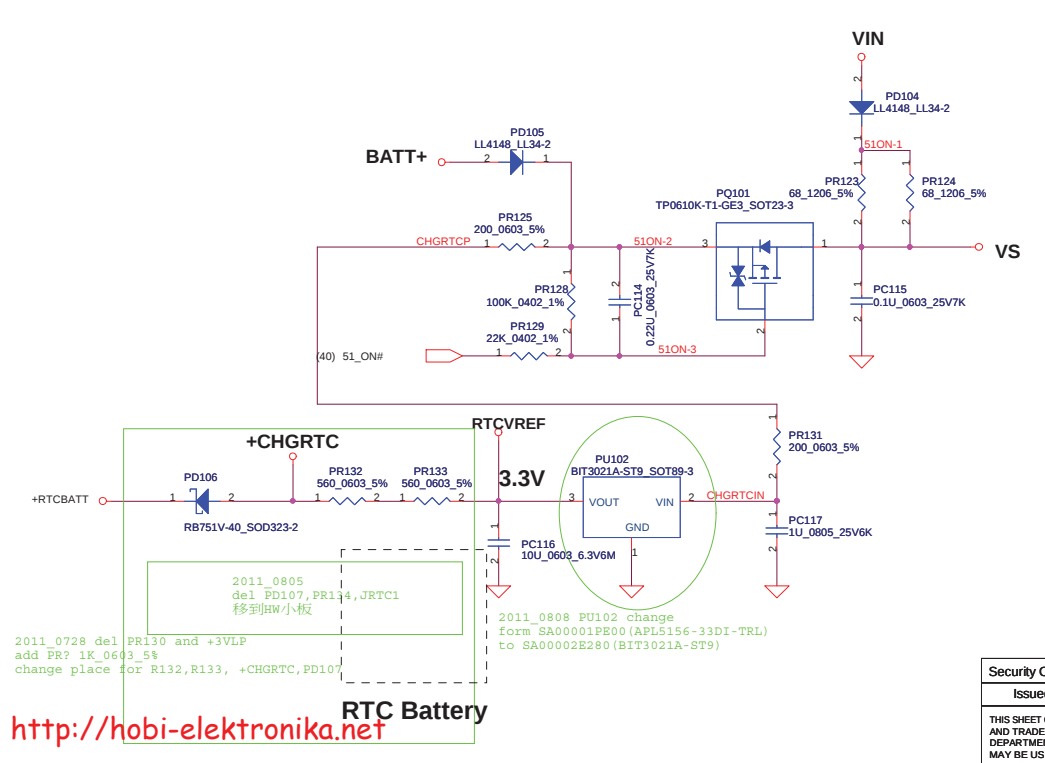
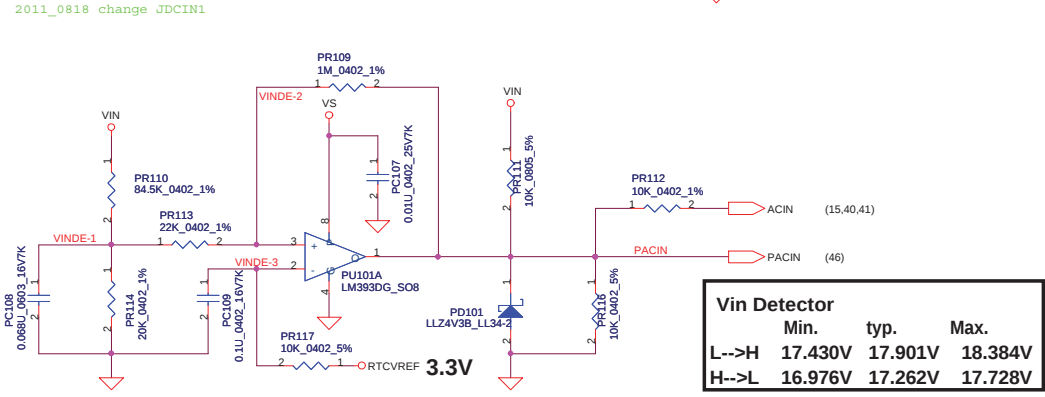
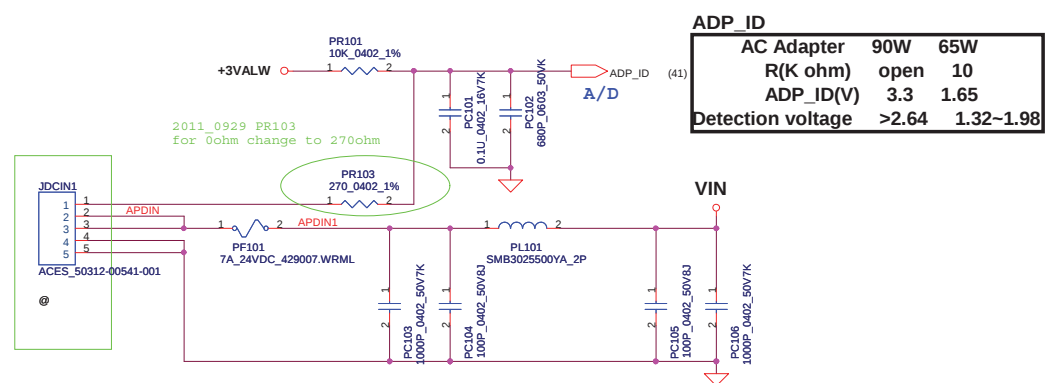


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Title		Compal Electronics, Inc.	
Size		DC Interface	
Document Number		LA-8131P	
Date		Tuesday, January 10, 2012	
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RTC
RTCRST
EC_111 pin
EC_ON
MAINPWON
+5VALW
+3VALW/VCCDSW
ON/OFF#
EC_RSMRST#
PBTN_OUT#
SLP_S5#
SLP_S4#
SYSON
SYSON
PCH_SLPA#
M_PWR_ON
+3VM
+1.05VM
PCH_APWROK
SLP_S3#
SUSP#
+1.5V_CPU_VDDQ
+1.8VS
+5VS
+3VS
+1.5VS
+0.75VS
+V1.05VS (VCCP)
+VCCSA
SA_PGOOD
VR_ON
PCH_POK
PCH_CLKOUT
DRAMPWROK
H_CPUPWRGD
CPU_VID
CPU_CORE
VGATE
SYS_PWROK
BUF_PLT_RST#
SPI
DMI



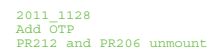


ACIN

Precharge detector			
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector			
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V



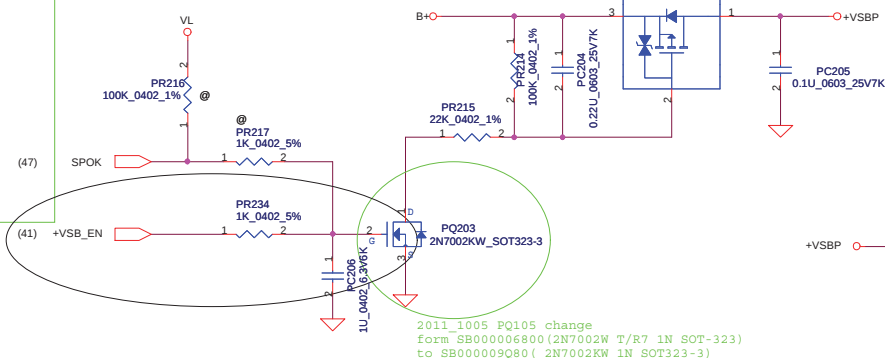
For KB930 --> Keep PU201 circuit
($V_{th} = 1.25V$)

For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211, PO201, PR208, PR212



2011_0808
PR227,PQ206
change place

```
2011_1005
PH201 form SL200000V00
100K +-1% NCP15WF104F03RC 0402
change to SL200000U00
100K +-1% TSM0B104F4251RZ 0402
```



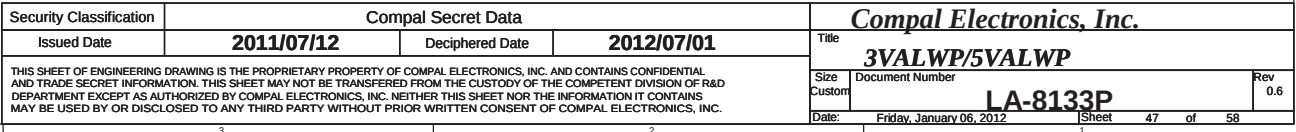
2011_1005 PQ105 change
form SB000006800(2N7002W T/R7 1N SOT-323)
to SB000009080(2N7002KW 1N SOT323-3)

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Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title		
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				Custom	LA-8133P	0.6
				Date:	Tuesday, January 10, 2012	Sheet 45 of 58

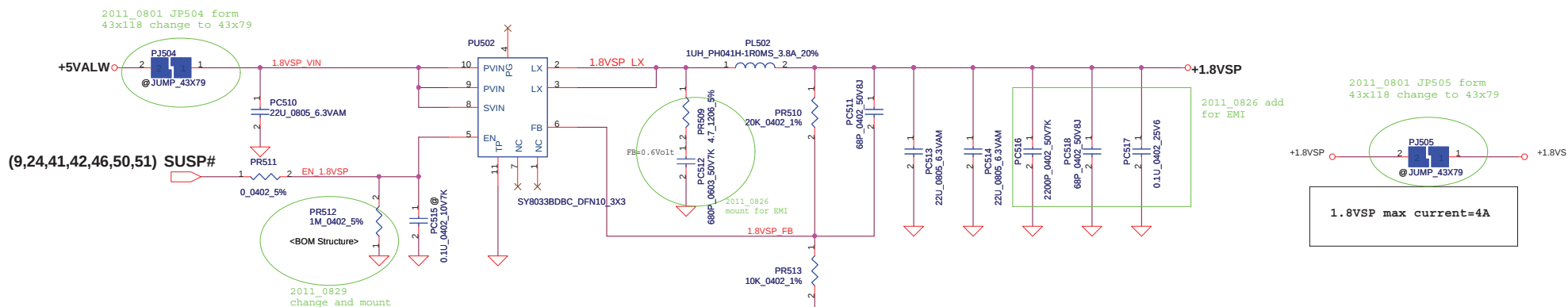
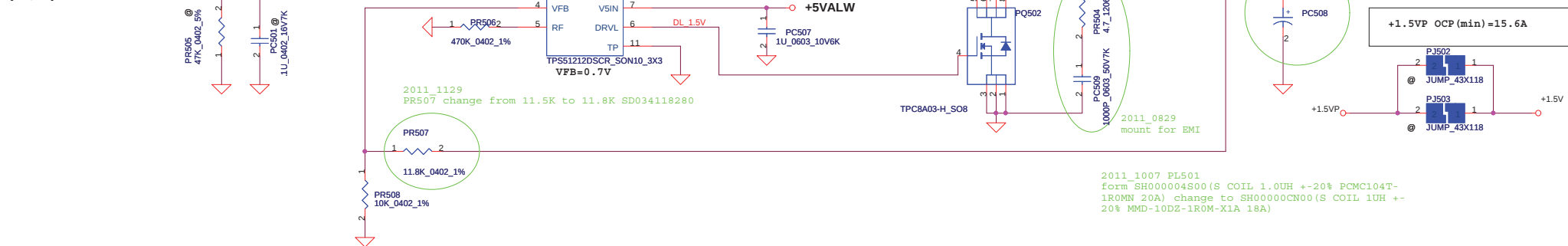


Date:	Friday, January 06, 2012	Sheet	46	of	58
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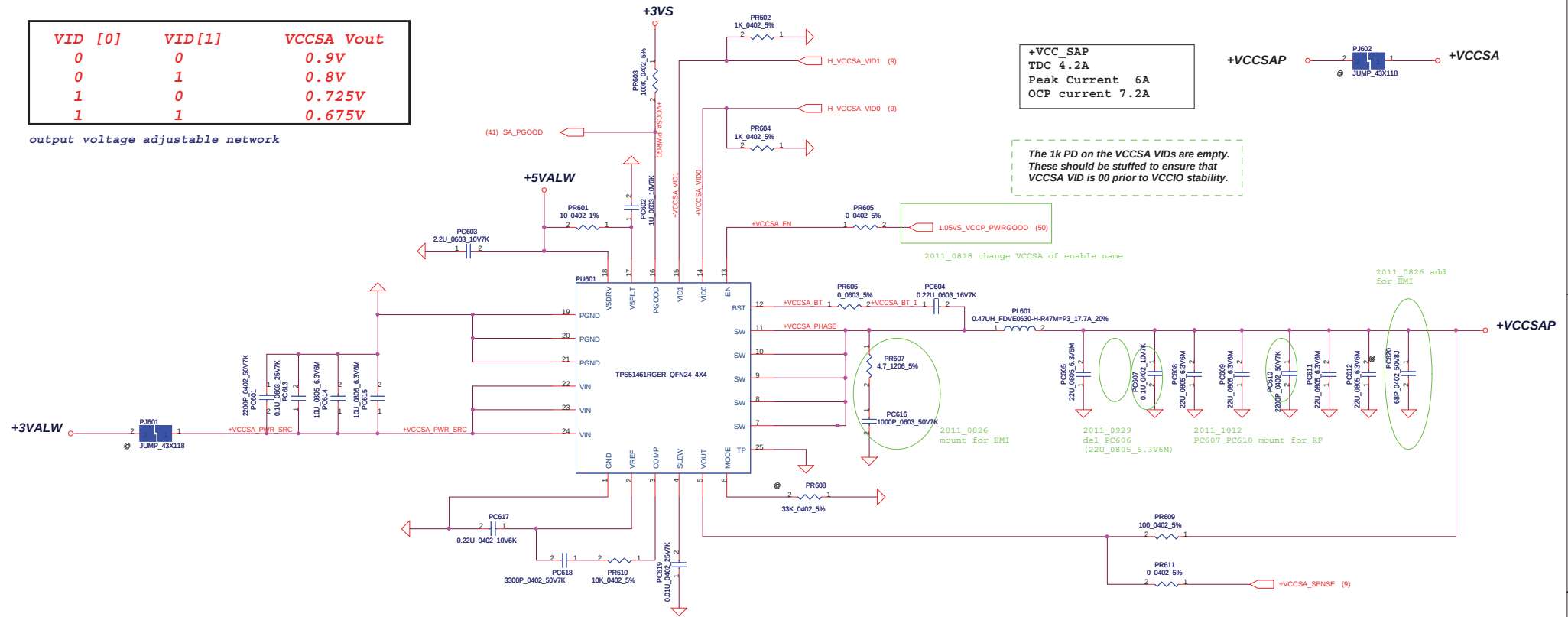
(41,42) SYSON



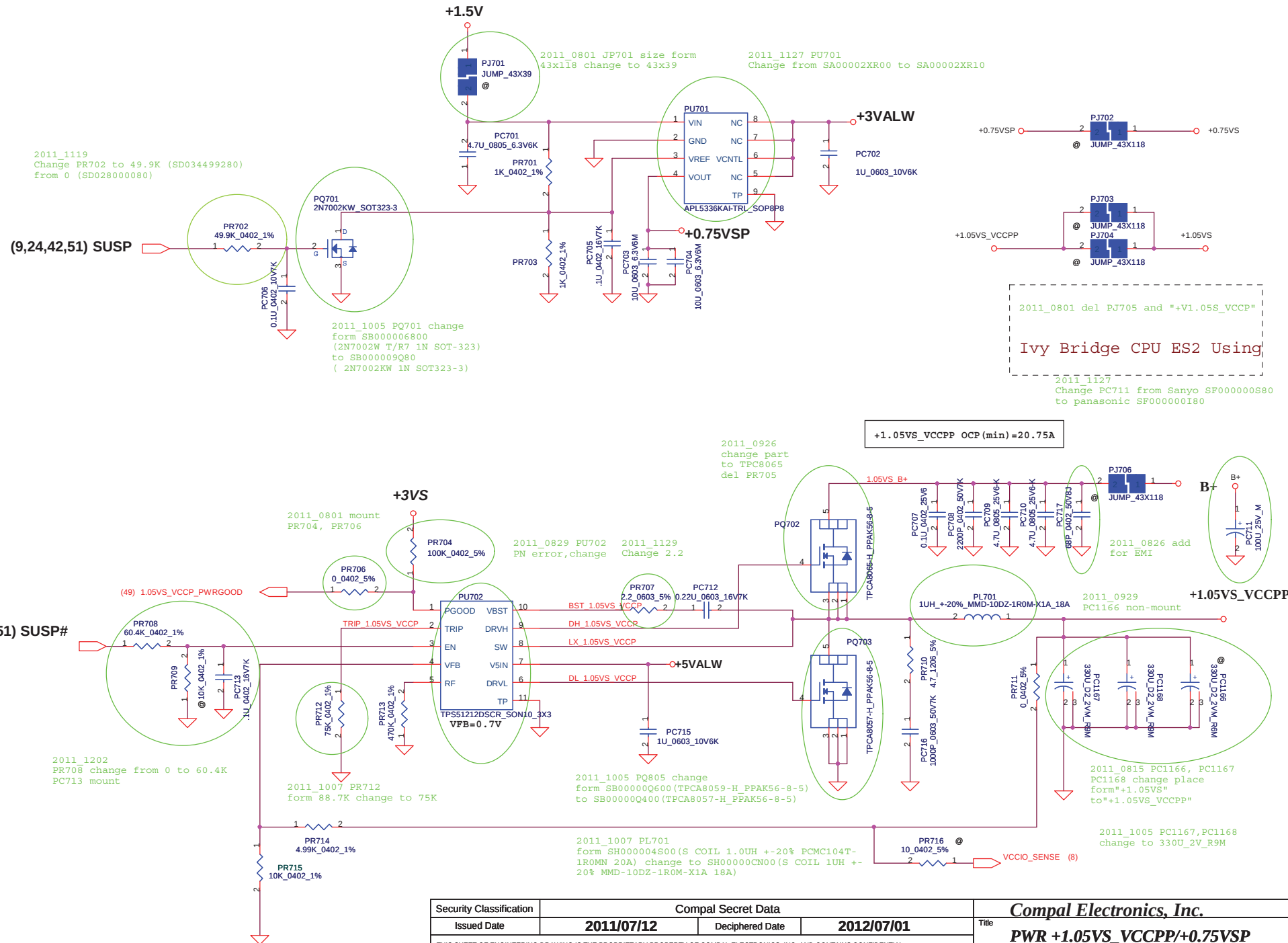
Security Classification		Compal Secret Data		Compal Electronics, Inc.				
Issued Date	2011/07/12	Deciphered Date	2012/07/01					
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				PWR-+1.5VP/+1.8VSP				
				Size	Document Number		Rev	
				Custom	LA-8133P		0.6	
				Date:	Friday, January 06, 2012		Sheet	48

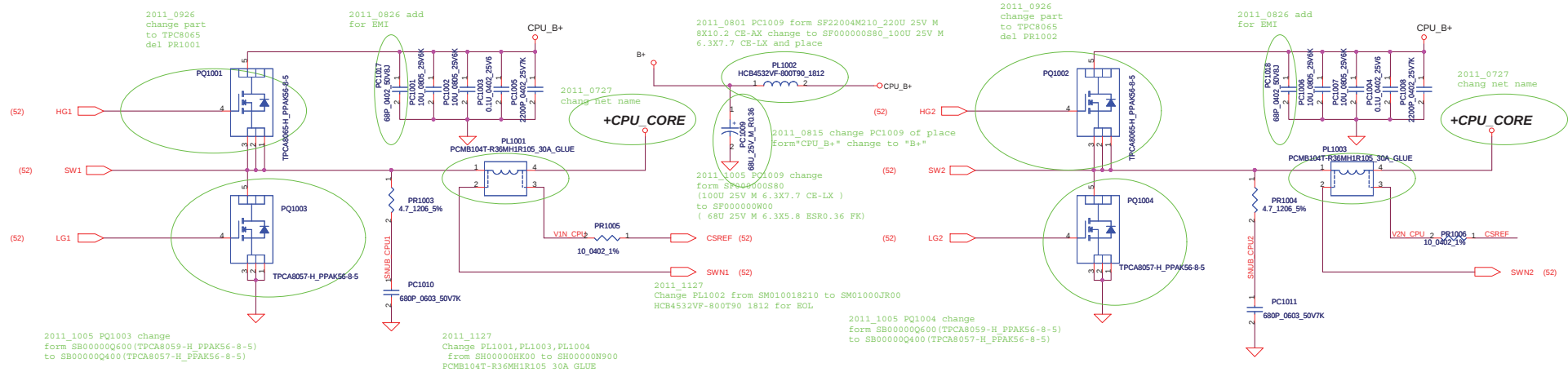
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network



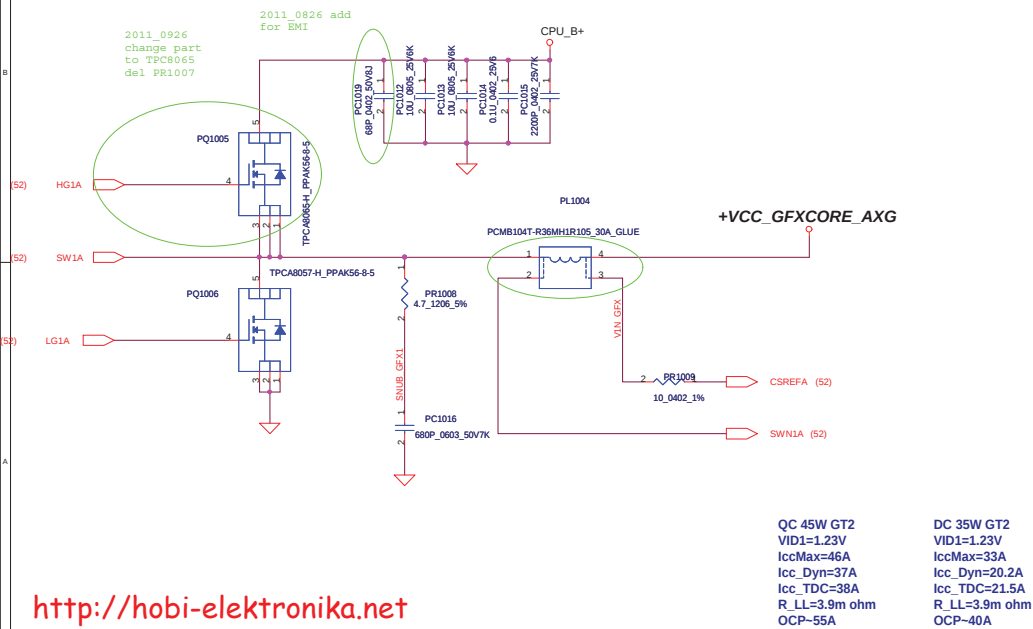
2011_0801 del +V1.05S_VCCPP circuit



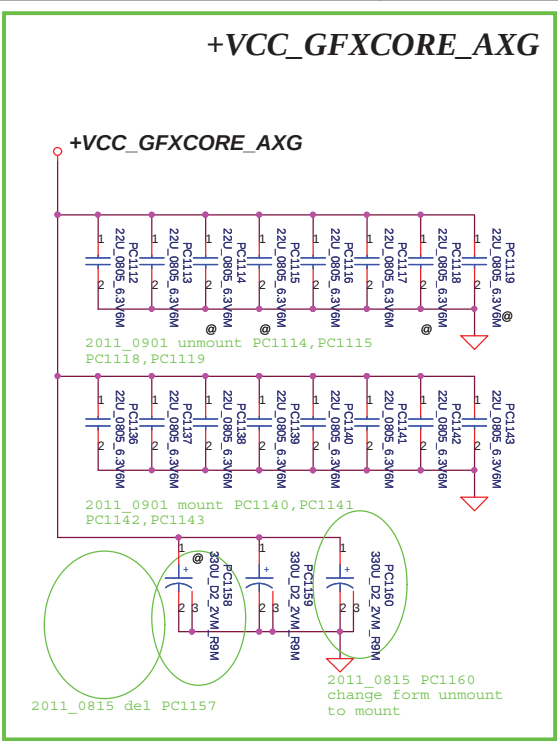
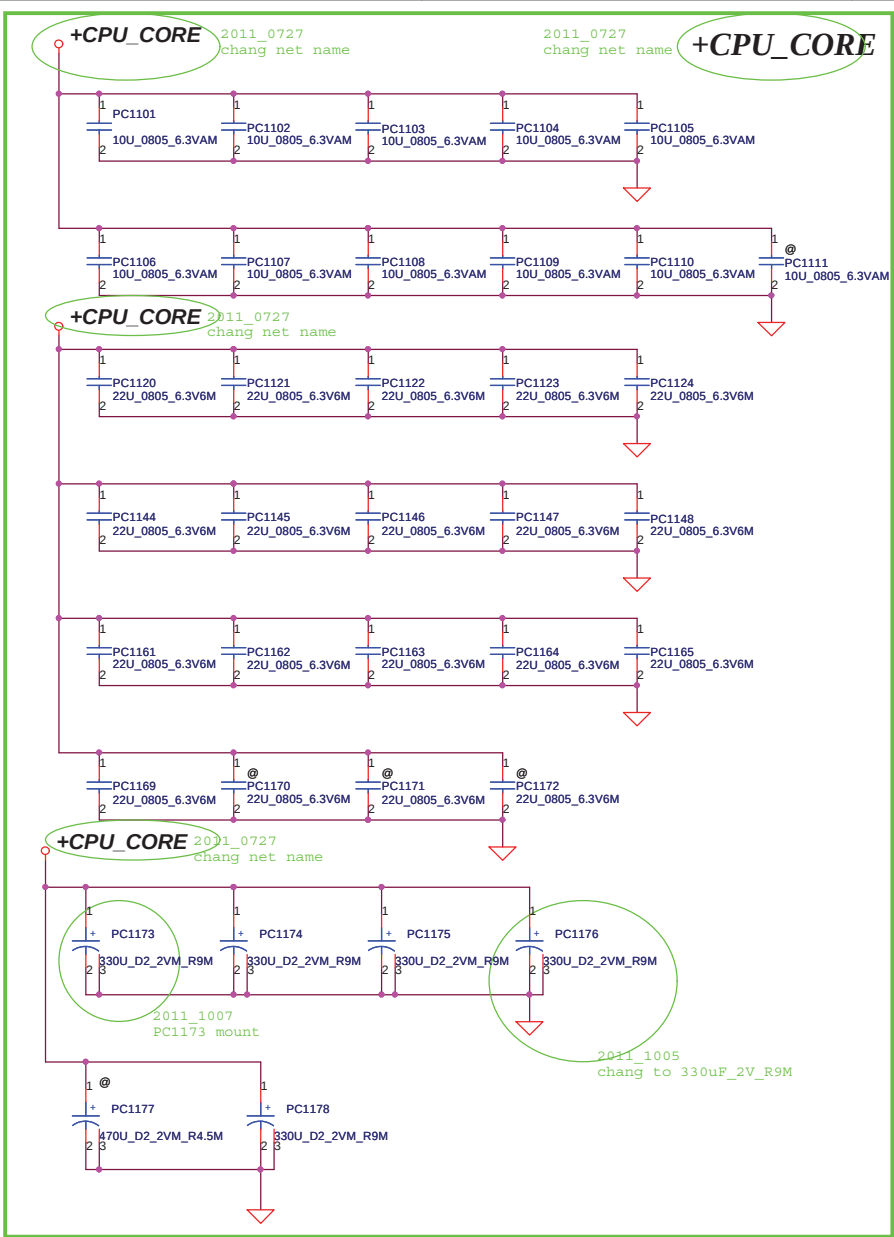


QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP=110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP=65A

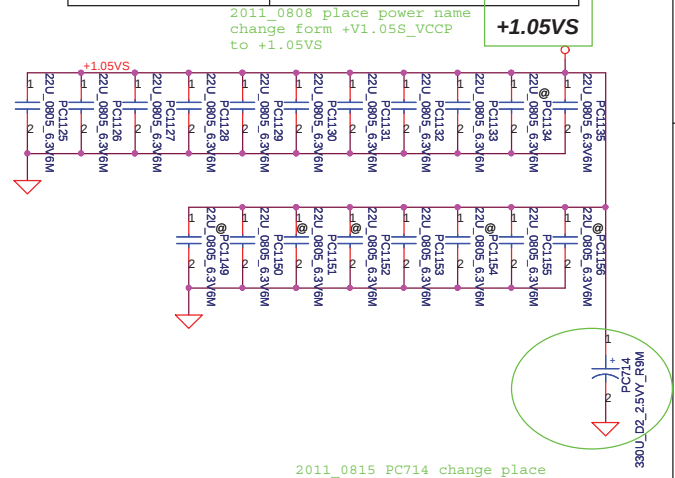


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Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

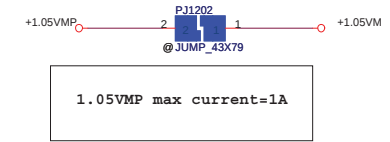
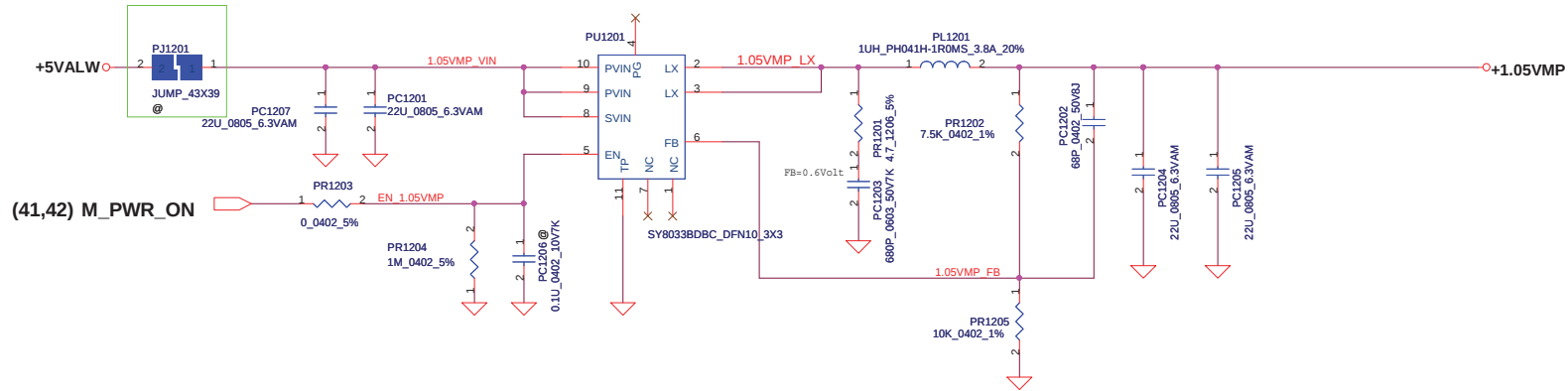


2011_0815 PC714 change place form "+1.05VS_VCCPP" to "+1.05VS"

2011_1005 PC714 change to 330uF_2V_R9M

2011_1007 PC714 form SGA00001Q802 (S POLY C 330U 2V M X LESR6M SX H1.9) change to SGA00002680 (330U_D2_2.5VY_R9M)

2011_0923 JUMP form 43X79 change to 43X79



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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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Version Change List (P.I.R. List)

Phase	Date	No.	BOM	Sch	Layout	Description	function
	2011/09/13	No1		V	V	Add C2325,C2326,C2327,C2328,C2329,R2319,R2324,Q2312	Add SBA function (+3VM) power
	2011/09/15	No2		V		Del Q2305	Del SYSYON#
	2011/09/15	No3		V		Add EC pin 119(M_PWR_ON) for SBA function	Add SBA function
	2011/09/15	No4		V		Add EC pin 120(PCH_SLP#) from PCH to EC for SBA function	Add SBA function
	2011/09/15	No5		V		Add EC pin72 (Muxless_STAT) for GPU STAT	Add Muxless_STAT function
	2011/09/15	No6		V		Del PR310, PR311, PR312, PR313, net name:"H_PROCHOT#", +3VALW.	PWR-CHARGER-BQ24727
	2011/09/15	No7	V			mount PC832	
	2011/09/15	No8		V	V	Add R2482,Q2404,C2509,R2481,R2485,Q2400,R2483,C2501	AOAC Function
	2011/09/15	No9		V	V	change net name BT_OFF# to BT_ON# and change PCH EN GPIO from GPIO34 to GPIO36 R280 from @ to mount,R282 from mount to @	BT Function
	2011/09/15	No10		V	V	change net name(Mini-Express) from BT_OFF# to WLBT_OFF# PCH EN GPIO change to GPIO34	BT Function
	2011/09/19	No11		V	V	change +3VS WLAN net name to +3VS_AOAC change +3VS_WWAN net name to +3VS_AOAC	AOAC Function
	2011/09/19	No12		V	V	Del R1010 for LVDS CONN plug high voltage	LVDS CONN
	2011/09/19	No13		V	V	R1102,R1104,R1105 from @ to mount fix MIC(ECR97236)issue	MIC function
	2011/09/19	No14		V	V	Add R2470 for 80 port function	80 port function
	2011/09/19	No15		V	V	Del R2476 Add Q2405	BT Function
	2011/09/20	No16		V	V	Add power schematic 9/15 again modify RF PC423, PC425, PC519, PC620, PC717, PC873, PC874, PC8124, PC1018, PC1019, PC422, PC516, PC517 modify POWER在VGA的PWM IC 加的零件PR869, PR870	
	2011/09/22	No17		V	V	Add U10,C589,C645 for TPM function	TPM function
	2011/09/22	No18		V	V	Add R110,R112 for SPI POWER choose(SBA function)	
	2011/09/23	No19		V	V	modify power page 44-57(PJ1201 JUMP form 43X79 change to 43X79)	
	2011/09/26	No20		V	V	change CPU footprint from TYCO 2013620-2 989P-T to TYCO 2013620-2 989P-T-A39 change PCH footprint from PANTHER-POINT_FCBGA_989P-T to PANTHER-POINT_FCBGA_989P-T-A39 change GPU footprint N13P-PES-A1_FCBGA_908P to N13P-PES-A1_FCBGA_908P-A39 change VRAM footprint K4W1G1646E-HC12_FBGA_96P to K4W1G1646E-HC12_FBGA_96P-A39	
	2011/09/26	No21		V	V	change PCH_GPIO24(R288) pull up to +3V_PCH	
	2011/09/26	No22		V		change P18 (R311,R330,R286,R329) for UMA and Optimus memon	
	2011/09/26	No23		V		change net name PCH_THRMTRIP#_R to VGA_THRMTRIP#	
	2011/09/26	No24		V	V	PQ702 change to TPC8065,Del PR705 PQ1001,PQ1002,PQ1005 change to T0C8065,Del PR1001,PR1002,PR1007	
	2011/09/26	No25		V	V	p43 change Q2304 dual channel 2n7002 to single channel Q2304,Q2305(Q2305 @) p43 change Q2306 dual channel 2n7002 to single channel Q2306,Q2311(Q2311 @)	
	2011/09/27	No27	V			modify EC Board ID R2213 to 18K	
	2011/09/27	No28		V	V	net name CX_GPIO0 connect to U1101 pin 38	
	2011/09/27	No29		V	V	Add C2152,C2153,D2113 for ESD	
	2011/09/27	No30		V	V	change NVIDIA N13W ROM_SCLK from 15K PU to 5K PU	
	2011/09/27	No31		V	V	change ESD part D2401,D2403,D2405 power from +5VALW to +USB VCCA	
	2011/09/27	No32		V	V	Add C2108 for GPU_CLKREQA	
	2011/09/27	No33				Add Q2406 , modify R2401,Change PCH_GPIO19 to ODD_DET#,for zero power ODD	
	2011/09/27	No34				change WLBT_OFF# to PCH_GPIO34	
	2011/09/27	No35				change PCH_GPIO34 to WLBT_OFF#(mini card pin5)	
	2011/09/27	No36				change BT_ON# connect to WLBT_OFF#(mini card pin51)	
	2011/09/28	No37				C76 , R1123 , c1131 , R2201,C2209 C84,C85 from @ to mount for RF team	
	2011/09/29	No38				R1529 change to 15K	
	2011/09/29	No39				Add CONN JDB3 fo debug	
	2011/09/29	No40				Add R2460,R2438,R2471,R2472,R2475,R2476 for PS8520B	
	2011/09/29	No41				change D2403 ,D2401 power to +USB_VCCB,and del D2403 ,D2401,D2405 Pin3 net	
	2011/09/29	No42				change power schematic del PC606 (22U_0805_6.3V6M) PR855.1 net change form +VGA_CORE to +VGA_COREP PR827 mount change to @ (non-mount) PR839 for 47Kohm change to 147Kohm PR103 for 0ohm change to 270ohm PC1166 non-mount,PC1173 non-mount,PC1158 non-mount	
	2011/09/29	No43					
	2011/09/29	No44				Add Q2313,C2305,C2306,C2307,C2308,R2318,R2320,R2320,C2322 for +3V_PCH change CRT CONN to DC061109231(footprint pin modify) Add PR954,PR955	
	2011/09/29	No45				Add H16,H27 change Q2304,Q2305 to Q2304 modify PTH H11,H18 ,H21 Del T10 for SUS_STAT(SLP_S3# 走不出来)	
	2011/10/04	No46				reserve R352,R353 for SATA re-drive PS-8131B change net name from WLBT_OFF to WLBT_OFF_5# modify PCH_GPIO34 connect to BT_ON# for BT module modify PCH_GPIO36 from BT_ON# connect to WLBT_OFF_51# for mini card BT combo module changr Q2301 to 2N7002	
	2011/10/05	No47				Del R2469,T49,T45,T41,T37,T36,T28,T26 for ME 限高0 changer power net +3VS_FP to +3VS update power schematics P44-P57	
	2011/10/06	No48				change Q1202 part to SB0000007H10. change JCARD1 PN to SP020000H810 footprint: ACES_87213-1400G_14P change some CONN part NO. for ME CONN list Add D2416	

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				Document Number	Rev
				LA-8133P	0.6
				Drawn	Check
				Fiddev, January 05, 2012	Sheet 58 of 58