Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM+ICH9-M core logic

2009-02-16

REV:1.0

機密 等級 硬體二部 產出人員 產出日期 解密日期

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

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Title: *Cover Sheet*

Size: Custom | Document Number: *Montevina UMA* | Rev: 0.1

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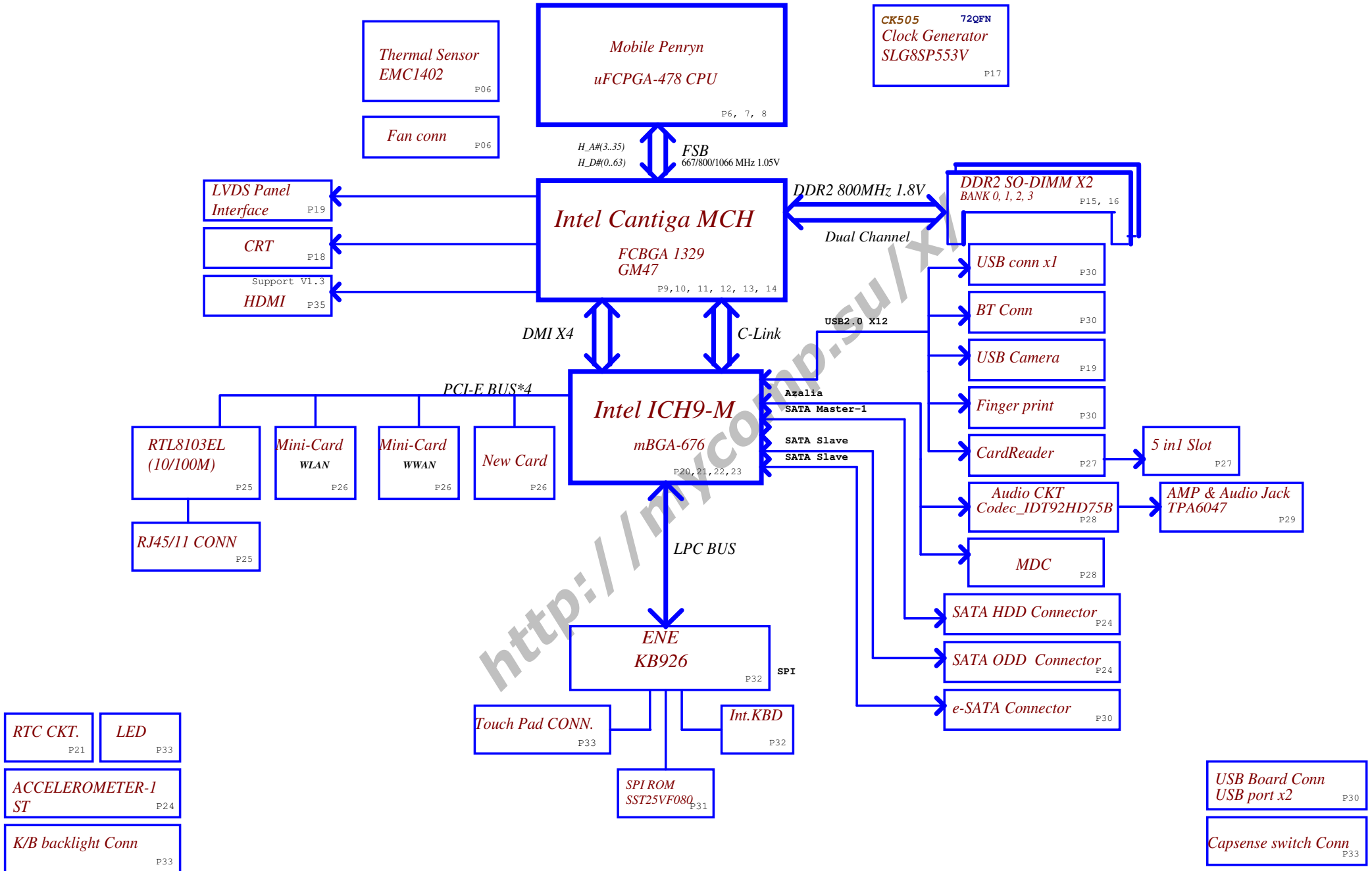
Montevina Consumer UMA



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Title: Block Diagram			
Size: Custom	Document Number: Montevina UMA		Rev: 0.1
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Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +2.5VS +1.8V
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
DEBUG@ :	means just reserve for debug.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
ESATA @ :	means just reserve for ESATA
GS @ :	means just reserve for G sensor
FP @ :	means just reserve for Finger Print
Multi @ :	means just reserve for Multi Bay
NewC@ :	means just reserve for New card
Main@ :	means just reserve for Main stream
OPP@ :	means just reserve for OPP
2MiniC@ :	means just reserve for 2nd Mini card slot
PA @ :	means just reserve for PA
PR @ :	means just reserve for PR

USB assignment:

USB-0	Right side(with eSATA)
USB-1	Left side
USB-2	Left side
USB-3	Cardreader
USB-4	Camera
USB-5	WLAN
USB-6	Bluetooth
USB-7	Finger Printer
USB-8	MiniCard(WWAN/TV)
USB-9	Express card
USB-10	X
USB-11	X

PCIe assignment:

PCIe-1	WWAN
PCIe-2	X
PCIe-3	WLAN
PCIe-4	GLAN (Realtek)
PCIe-5	X
PCIe-6	New Card

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X	V	V
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V	X	X	X

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Title: Notes List

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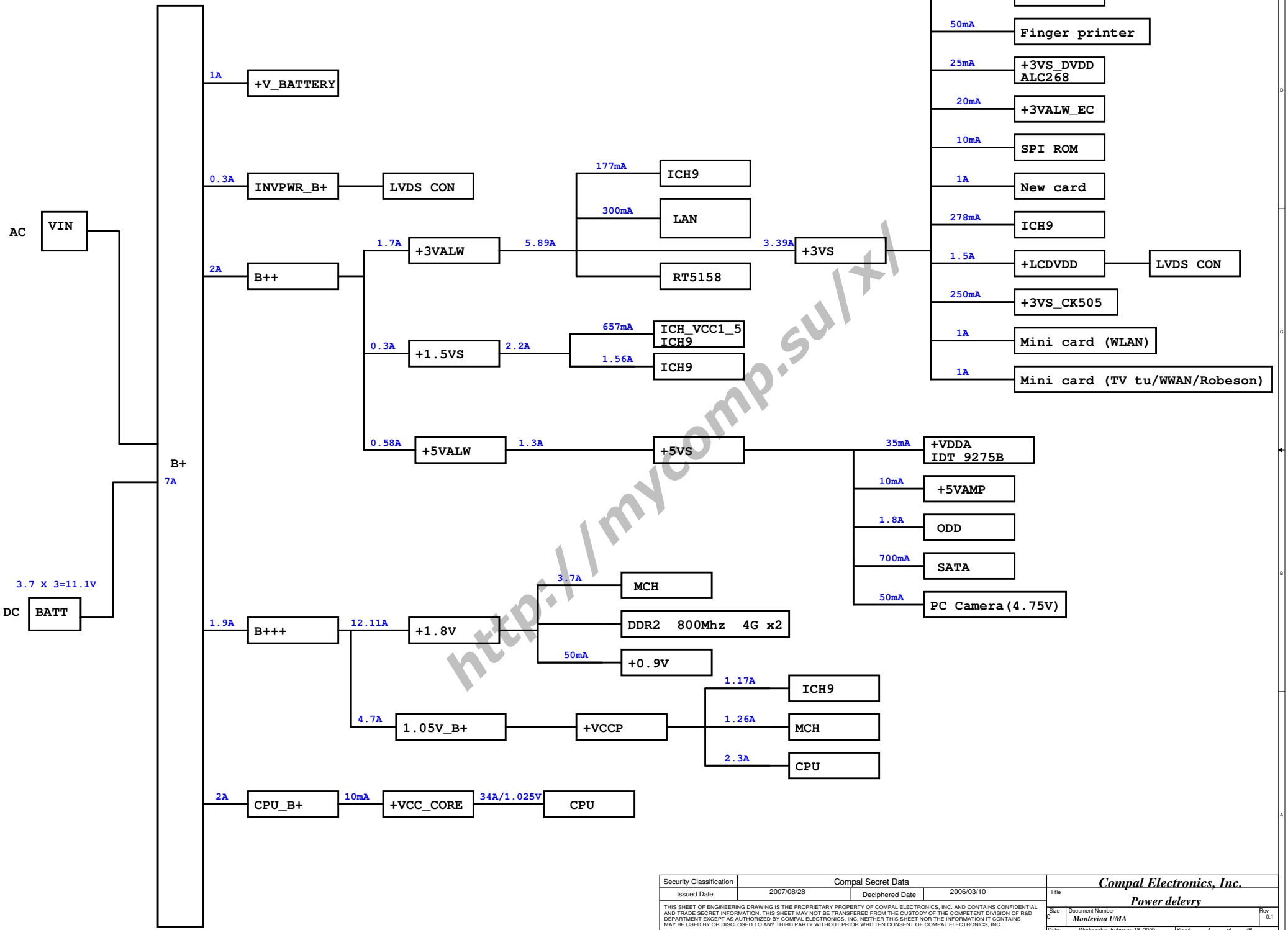

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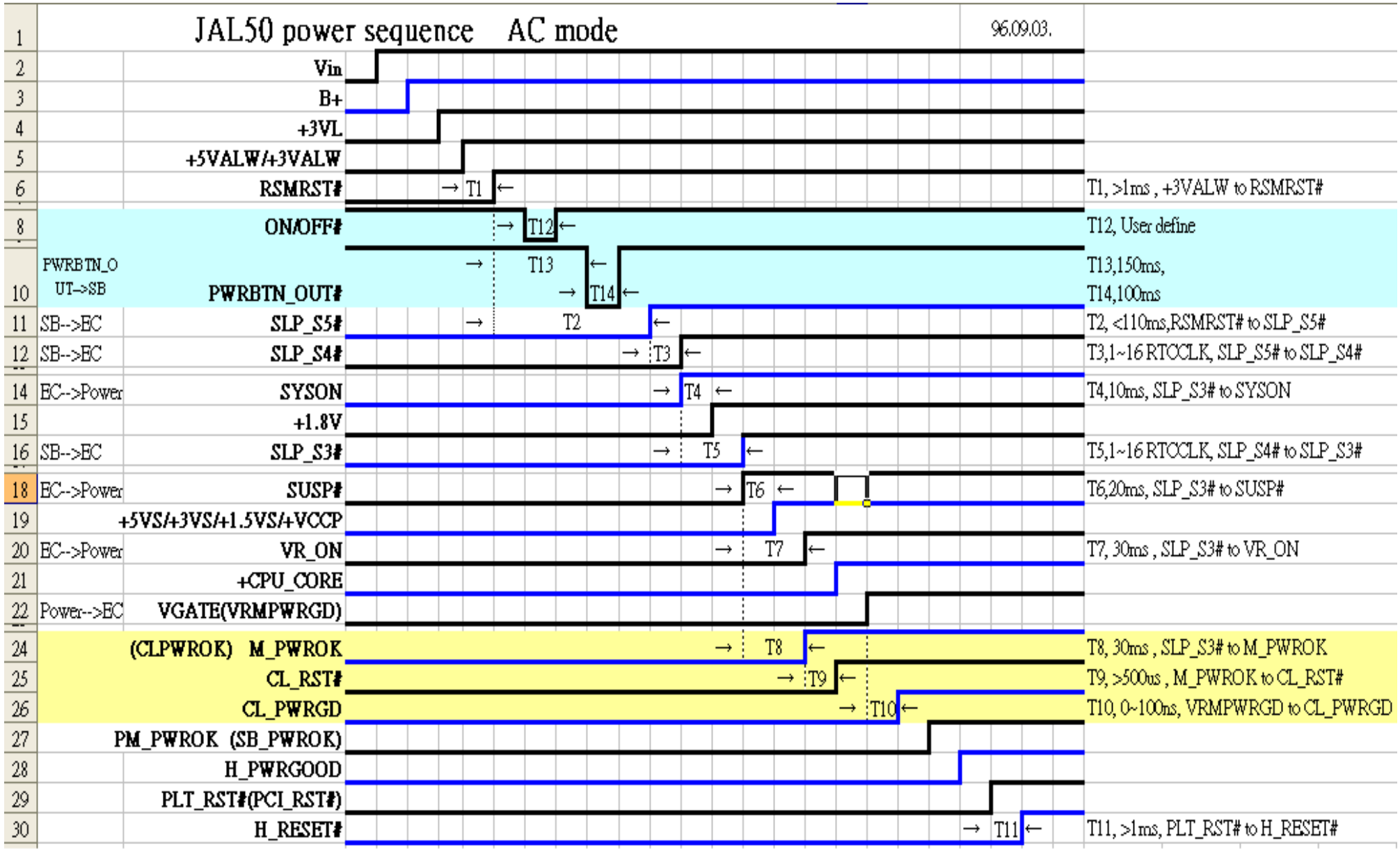

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Title: Notes List		
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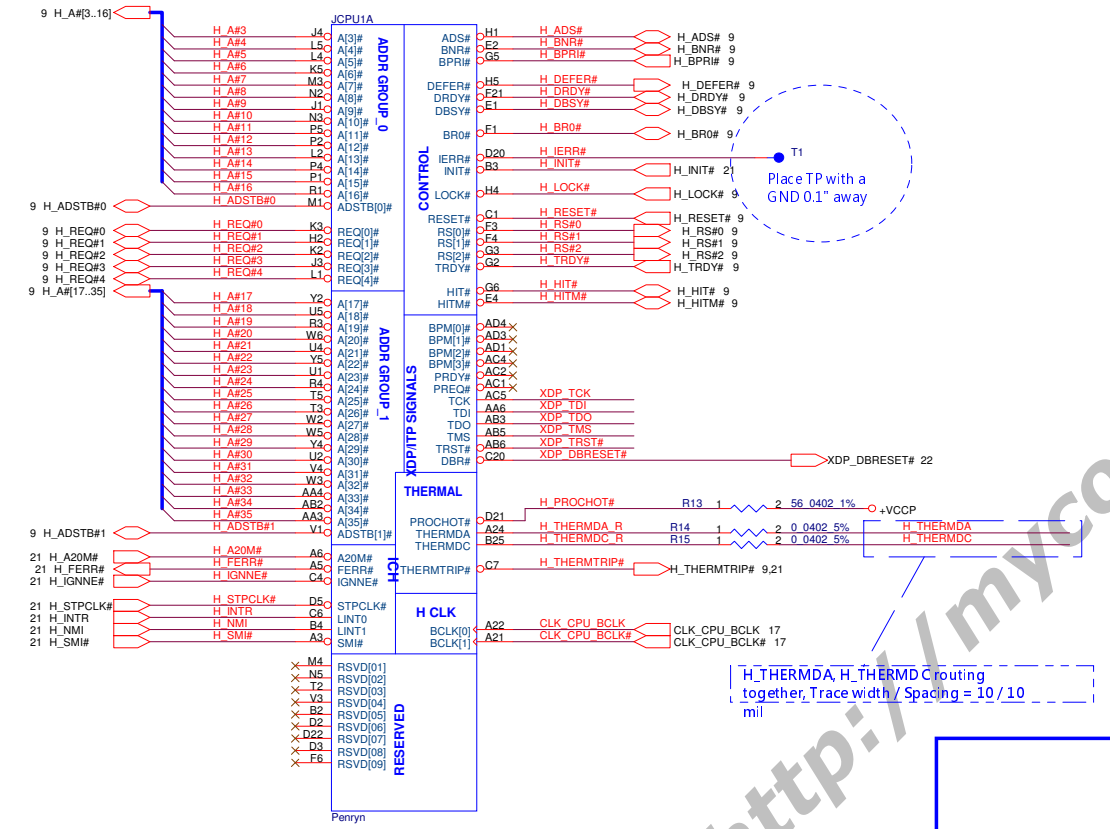
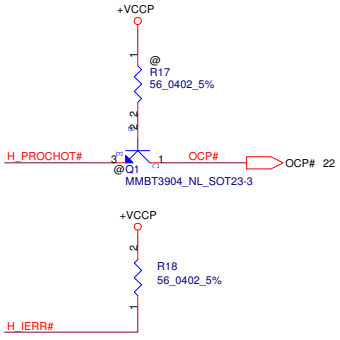
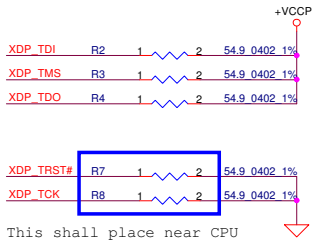
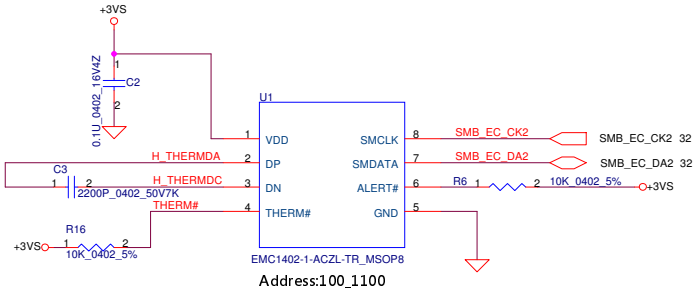




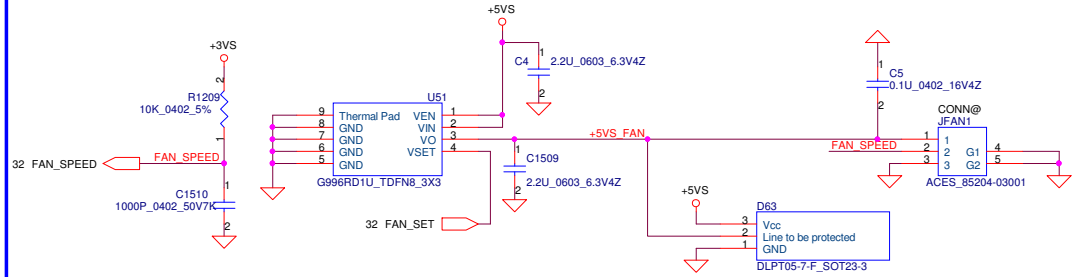
ITP-XDP Connector





Fan Control circuit

SI-1 Change to voltage control circuit



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Title	Compal Electronics, Inc.		
	Penryn(1/3)-AGTL+/ITP-XDP		
Size: Custom	Document Number: Montevina UMA		Rev: 0.1
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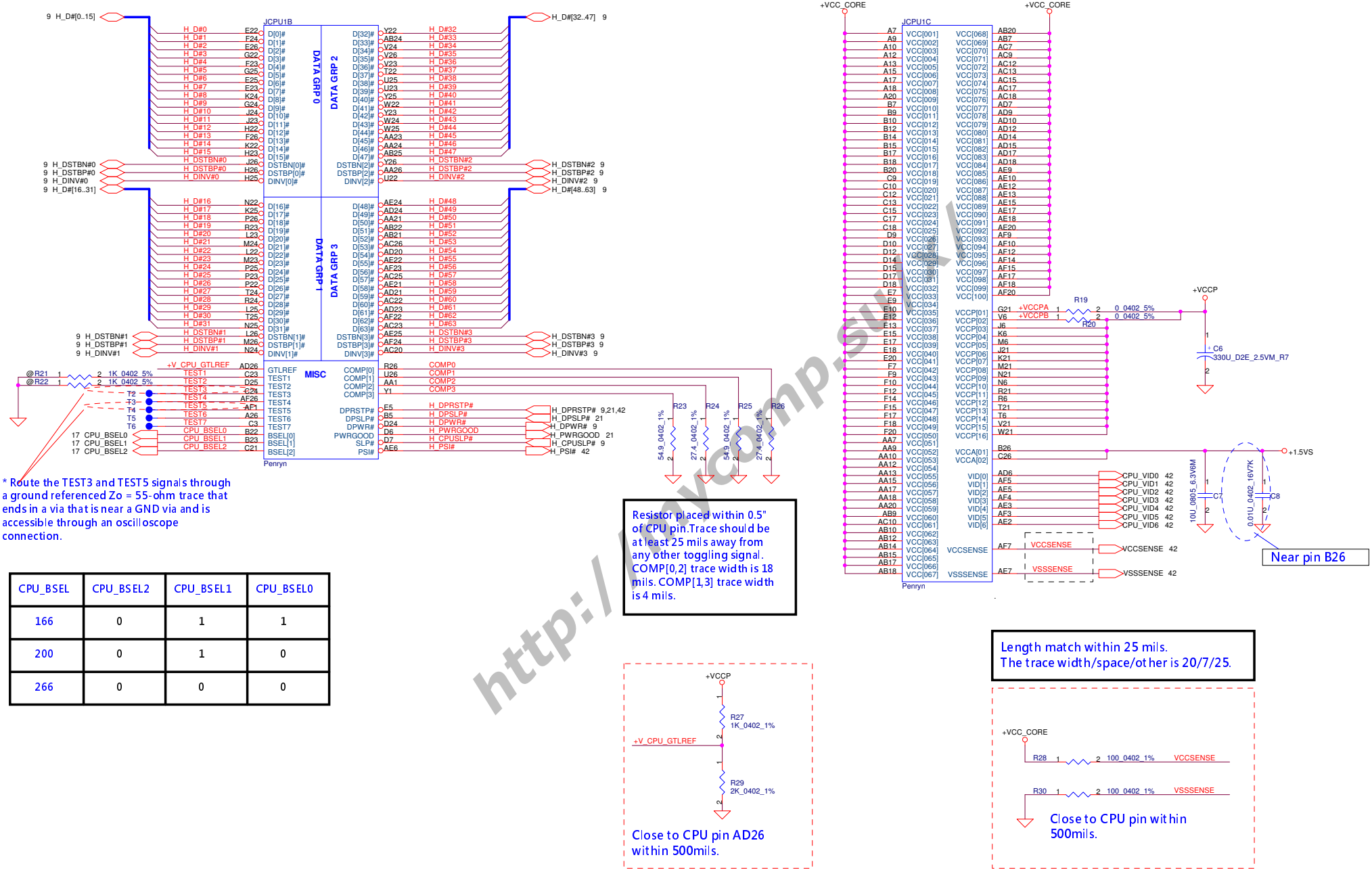

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: Penryn(2/3)-AGTL+/ITP-XDP

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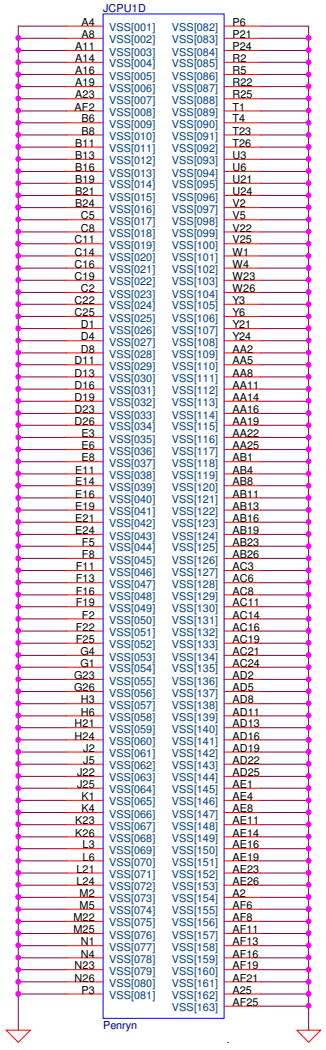
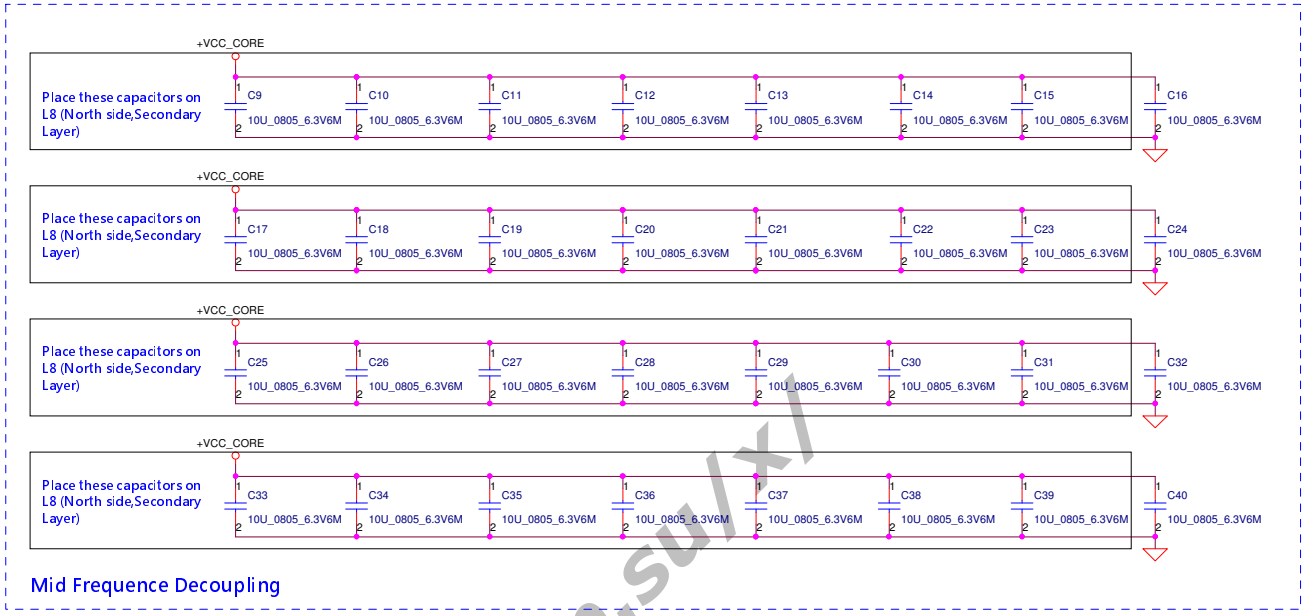
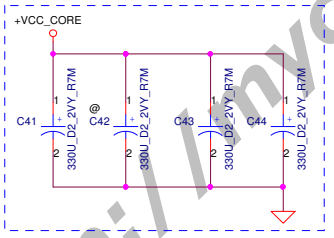
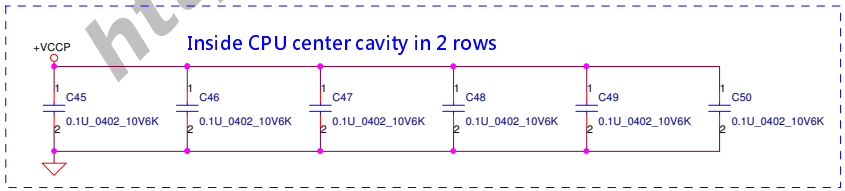




Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF





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Compal Electronics, Inc.

Title: Penryn(3/3)-AGTL+/ITP-XDP

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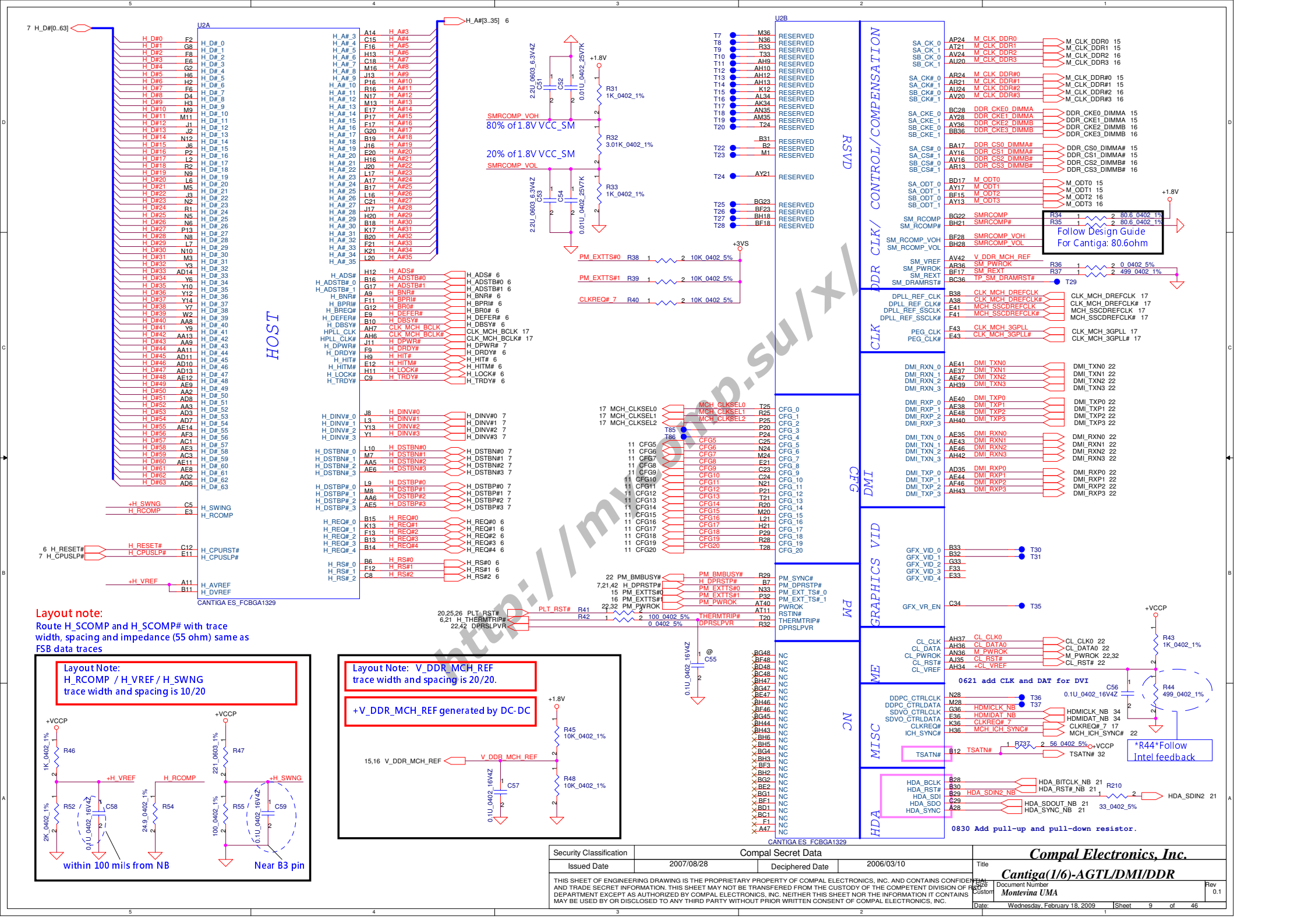

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Title	Compal Electronics, Inc.		
	Cantiga(1/6)-AGTL/DMI/DDR		
Size: Custom	Document Number: Montevina UMA		Rev: 0.1
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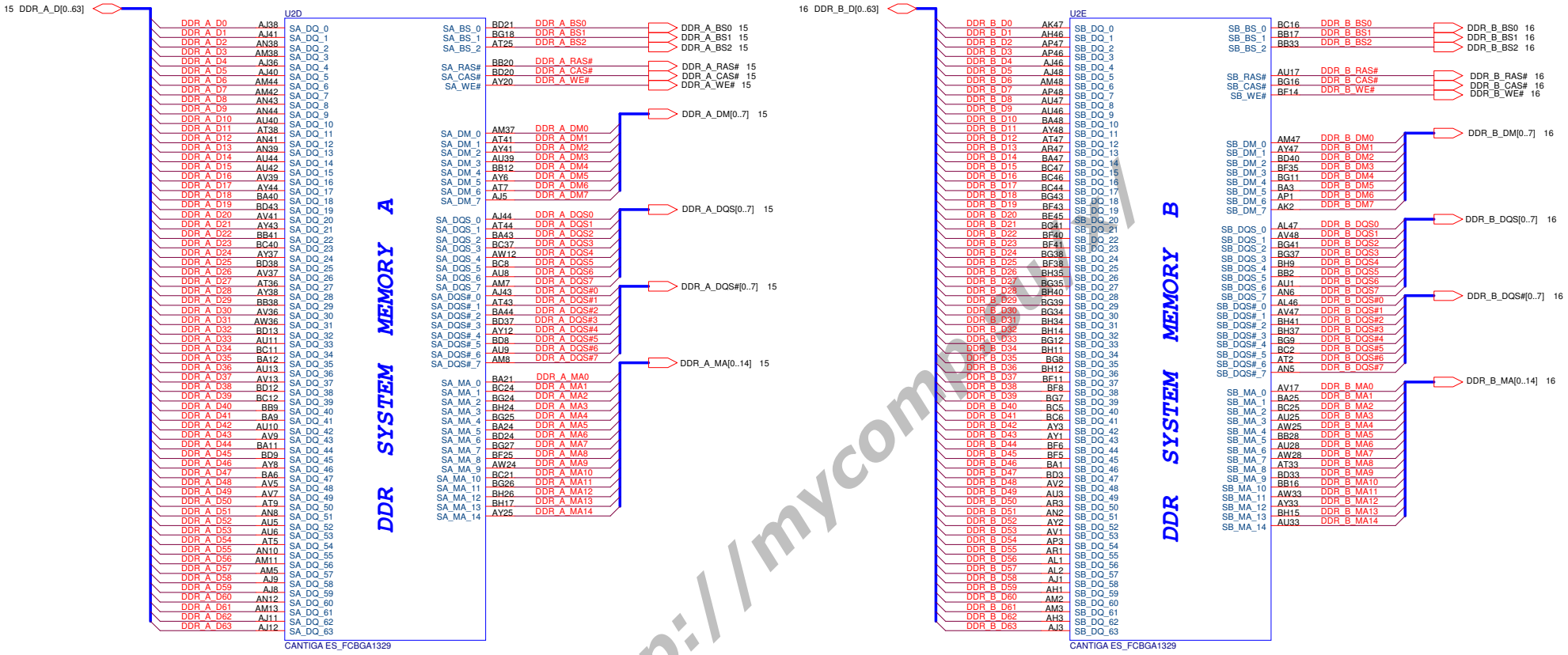

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Compal Electronics, Inc.

Title: **Cantiga(2/6)-DDR2 A/B CH**

Size: Custom	Document Number: *Montevina UMA*	Rev: 0.1
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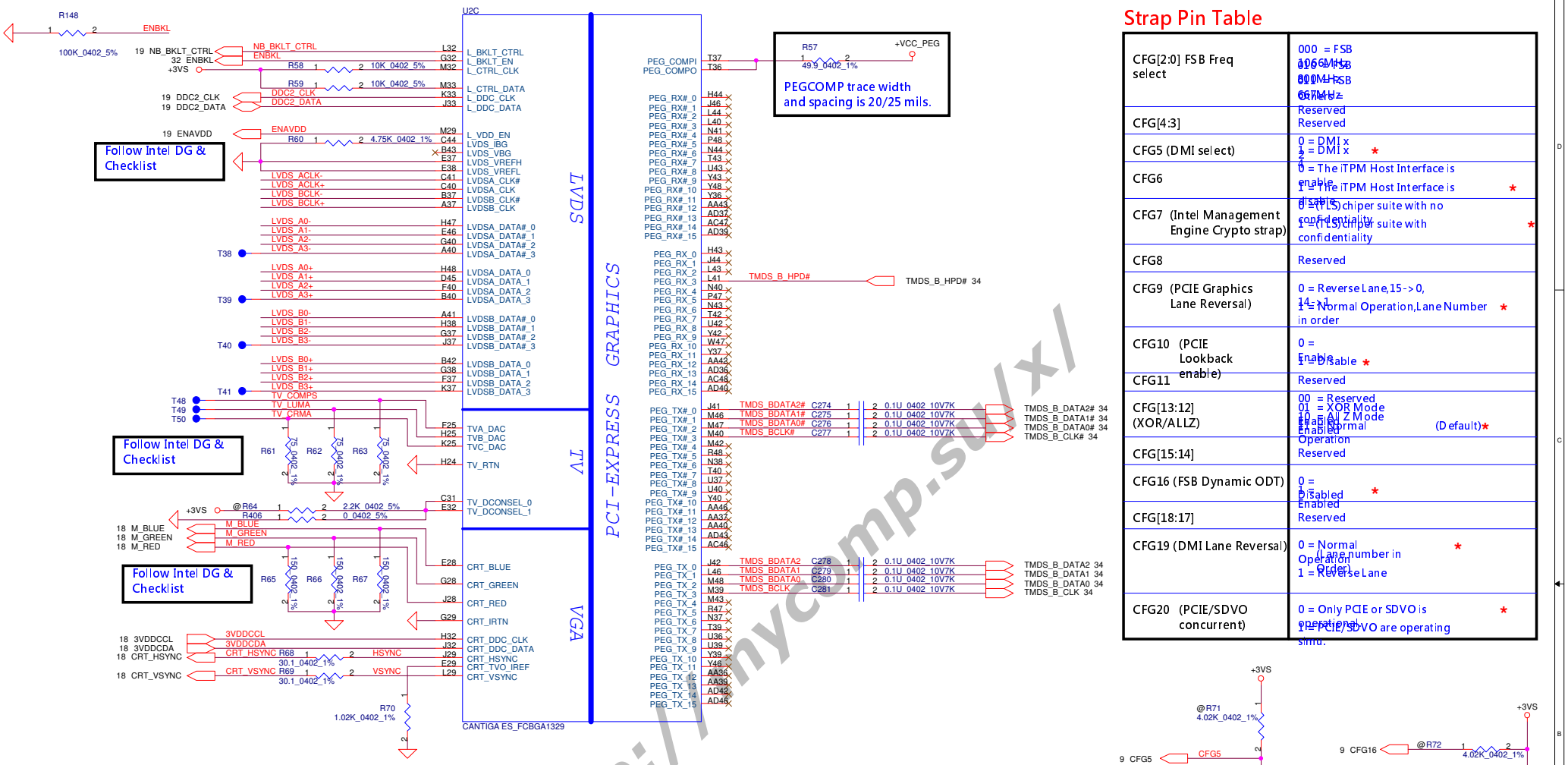
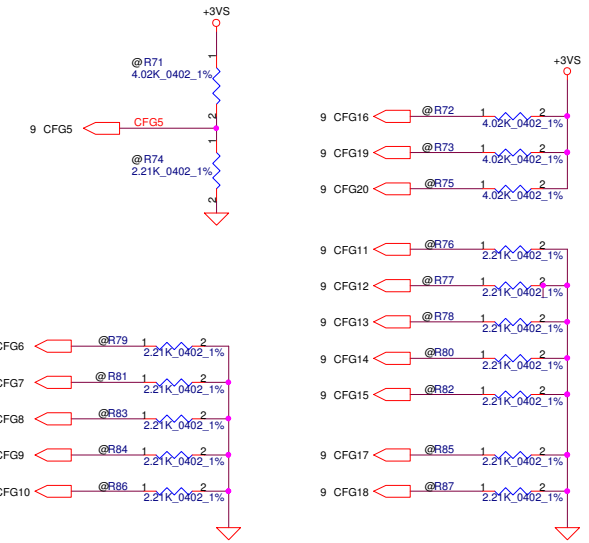
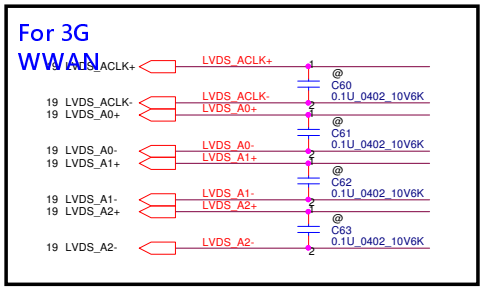


Strap Pin Table

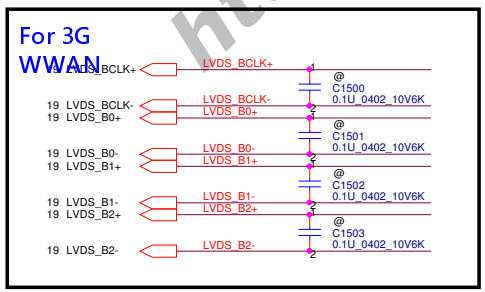
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 001 = FSB 800MHz 010 = FSB 667MHz 011 = FSB 533MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chiper suite with no confidentiality 1 = (TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode 10 = ALL Z Mode 11 = Normal (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) 1 = Reverse Lane *
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. 1 = PCIE/SDVO are operating simu. *



For 3G WWAN



For 3G WWAN



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Compal Electronics, Inc.	
Title	Cantiga(3/6)-VGA/LVDS/TV
Size: Custom	Document Number: Montevina UMA
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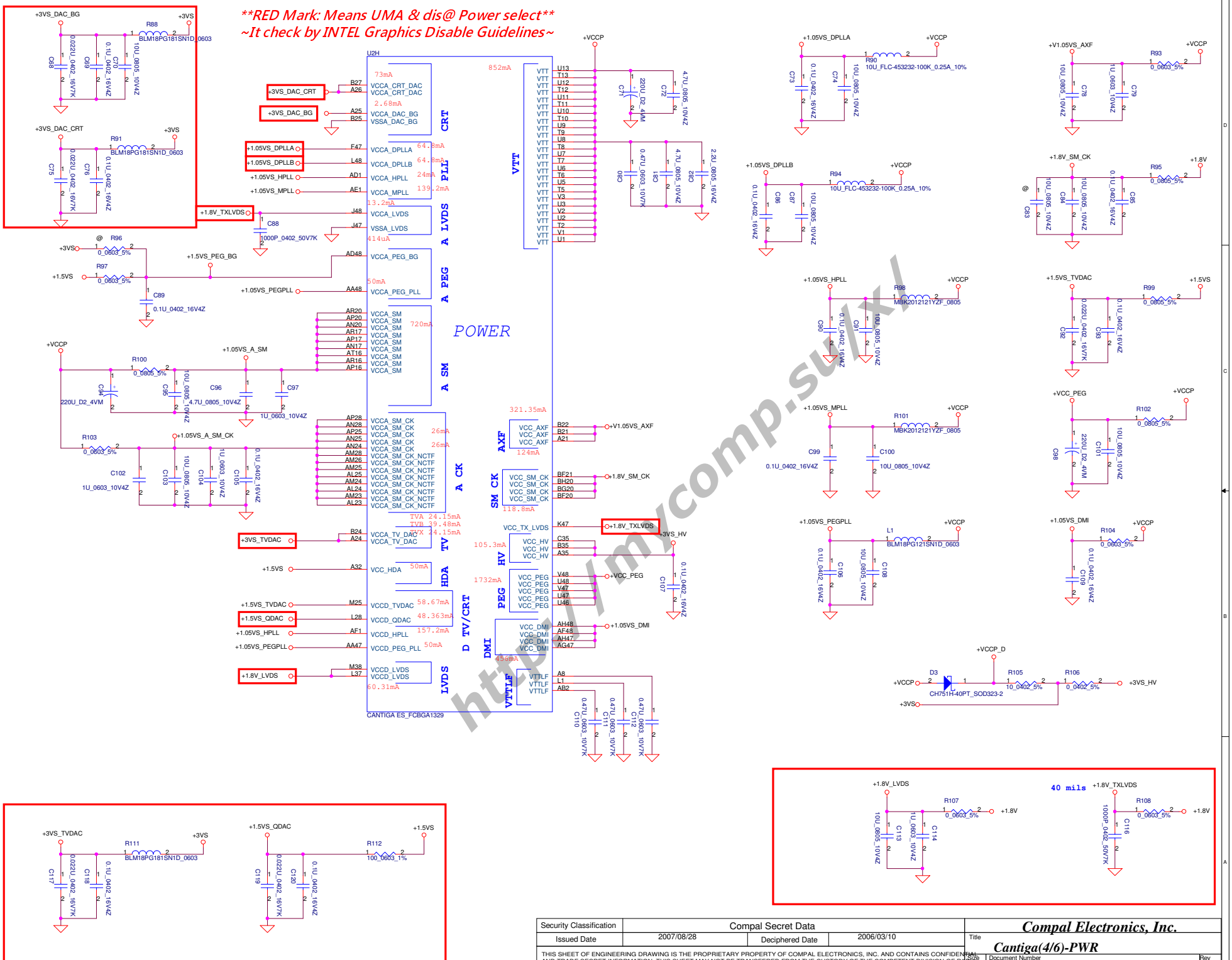

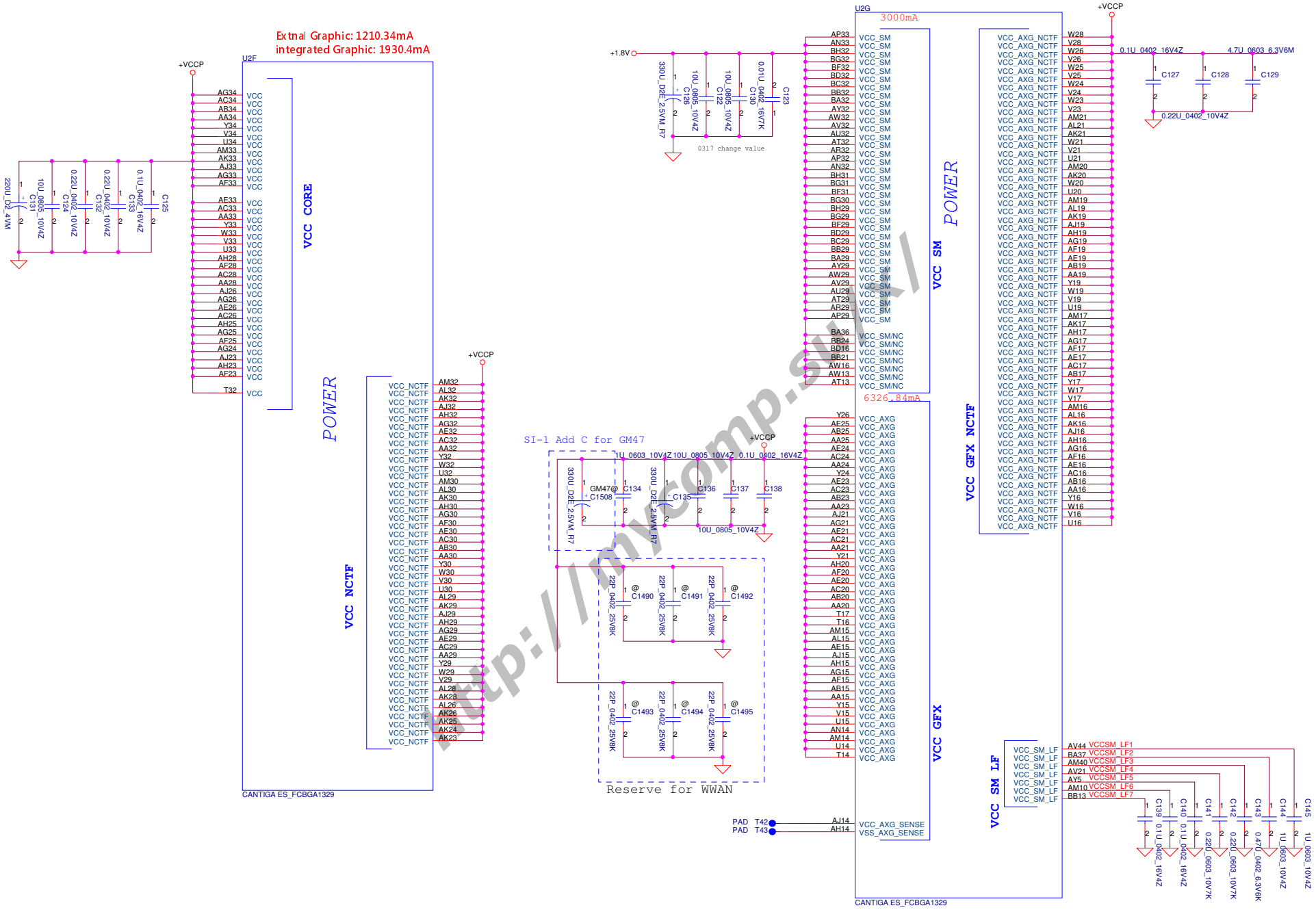

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Compal Electronics, Inc.			
Title: Cantiga(5/6)-PWR/GND			
Size: Custom	Document Number: Montevina UMA		Rev: 0.1
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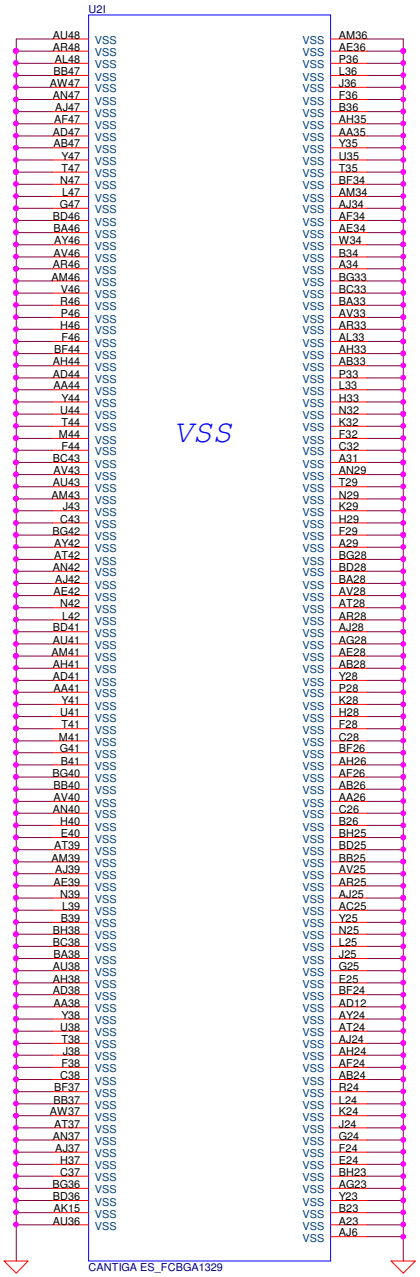

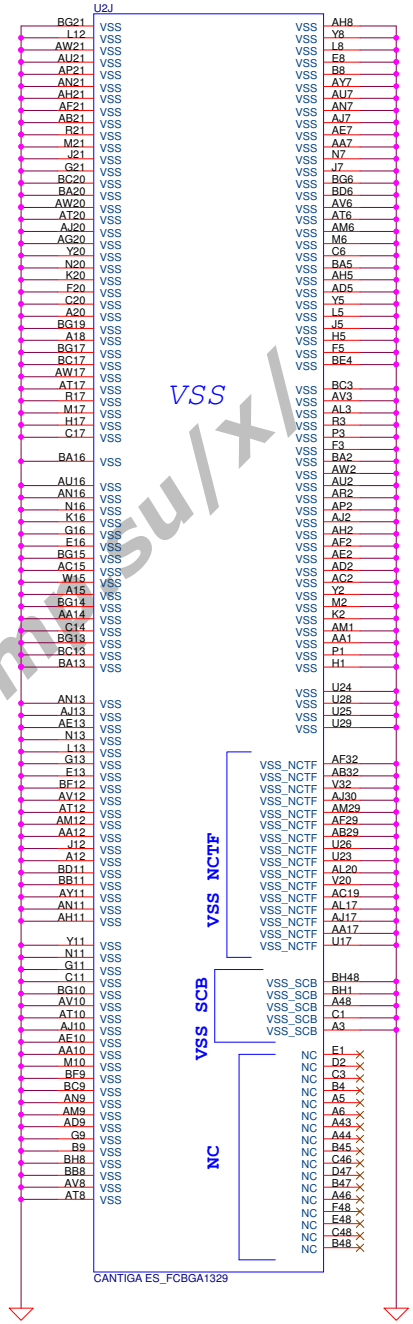

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Title: **Cantiga(6/6)-PWR/GND**

Size: Custom	Document Number: *Montevina UMA*	Rev: 0.1
Date: Wednesday, February 18, 2009	Sheet 14 of 46	

10 DDR_A_DQS#[0..7]
10 DDR_A_D[0..63]
10 DDR_A_DM[0..7]
10 DDR_A_DQS[0..7]
10 DDR_A_MA[0..14]

Layout Note:
Place near
JP3

+1.8V
2.2U_0805_16V4Z C152
2.2U_0805_16V4Z C147
2.2U_0805_16V4Z C153
2.2U_0805_16V4Z C154
2.2U_0805_16V4Z C155
0.1U_0402_16V4Z C156
0.1U_0402_16V4Z C148
0.1U_0402_16V4Z C149
0.1U_0402_16V4Z C157
330U_D2E_2.5VM_R7 C150

Layout Note:
Place one cap close to every 2
pullup
resistors terminated to +0.9VS

+0.9V
0.1U_0402_16V4Z C158
0.1U_0402_16V4Z C159
0.1U_0402_16V4Z C160
0.1U_0402_16V4Z C161
0.1U_0402_16V4Z C162
0.1U_0402_16V4Z C163
0.1U_0402_16V4Z C164
0.1U_0402_16V4Z C165
0.1U_0402_16V4Z C166
0.1U_0402_16V4Z C167
0.1U_0402_16V4Z C168
0.1U_0402_16V4Z C169
0.1U_0402_16V4Z C170

Layout Note:
Place these resistor
closely JP3,all
trace length Max= 1.5"

+0.9V
RP29 56_8P4R_0.05
DDR_A_BS2
DDR_CKE0_DIMMA
DDR_A_MA12
DDR_A_MA9
DDR_A_MA14
DDR_CKE1_DIMMA
DDR_A_MA6
DDR_A_MA7
RP30 56_8P4R_0.05
RP31 56_8P4R_0.05
DDR_A_MA8
DDR_A_MA5
DDR_A_MA1
DDR_A_MA3
DDR_A_MA2
DDR_A_MA4
DDR_A_BS1
DDR_A_MA0
RP32 56_8P4R_0.05
RP33 56_8P4R_0.05
DDR_A_BS0
DDR_A_MA10
DDR_A_CAS#
DDR_A_WE#
DDR_A_MA13
M_ODT0
DDR_CS0_DIMMA#
DDR_A_RAS#
RP34 56_8P4R_0.05
+0.9V
56_0404_4P2R_5%
RP11
DDR_CS1_DIMMA#
M_ODT1
DDR_A_MA11
R117 56_0402_5%

+1.8V
V_DDR_MCH_REF
V_DDR_MCH_REF 9,16
2.2U_0805_16V4Z C146
0.1U_0402_16V4Z C151
JDIMM1
FOX_ASOA426-M4R-1F
CONN@
SO-DIMM A

DDR_A_D4
DDR_A_D1
DDR_A_DQS#0
DDR_A_DQS0
DDR_A_D2
DDR_A_D3
DDR_A_D8
DDR_A_D9
DDR_A_DQS#1
DDR_A_DQS1
DDR_A_D11
DDR_A_D10
DDR_A_D16
DDR_A_D17
DDR_A_DQS#2
DDR_A_DQS2
DDR_A_D18
DDR_A_D19
DDR_A_D29
DDR_A_D24
DDR_A_DM3
DDR_A_D26
DDR_A_D27
9 DDR_CKE0_DIMMA
10 DDR_A_BS2
DDR_A_MA12
DDR_A_MA9
DDR_A_MA8
DDR_A_MA5
DDR_A_MA3
DDR_A_MA1
DDR_A_MA10
10 DDR_A_BS0
10 DDR_A_WE#
DDR_A_WE#
10 DDR_A_CAS#
9 DDR_CS1_DIMMA#
DDR_A_CAS#
DDR_CS1_DIMMA#
9 M_ODT1
M_ODT1
DDR_A_D37
DDR_A_D36
DDR_A_DQS#4
DDR_A_DQS4
DDR_A_D39
DDR_A_D38
DDR_A_D45
DDR_A_D44
DDR_A_DM5
DDR_A_D47
DDR_A_D46
DDR_A_D49
DDR_A_D48
DDR_A_DQS#6
DDR_A_DQS6
DDR_A_D54
DDR_A_D50
DDR_A_D61
DDR_A_D60
DDR_A_DM7
DDR_A_D59
DDR_A_D58
16,17,24 CLK_SMBDATA
16,17,24 CLK_SMBCLK
+3VSO
CLK_SMBDATA
CLK_SMBCLK
2.2U_0603_6.3V4Z C171
0.1U_0402_16V4Z C172

DDR_A_D5
DDR_A_D0
DDR_A_DM0
DDR_A_D6
DDR_A_D7
DDR_A_D13
DDR_A_D12
DDR_A_DM1
M_CLK_DDR0
M_CLK_DDR#0
DDR_A_D15
DDR_A_D14
DDR_A_D20
DDR_A_D21
PM_EXTTS#0 9
DDR_A_DM2
DDR_A_D23
DDR_A_D22
DDR_A_D28
DDR_A_D25
DDR_A_DQS#3
DDR_A_DQS3
DDR_A_D31
DDR_A_D30
DDR_CKE1_DIMMA
DDR_A_MA14
DDR_A_MA11
DDR_A_MA7
DDR_A_MA6
DDR_A_MA4
DDR_A_MA2
DDR_A_MA0
DDR_A_BS1
DDR_A_RAS#
DDR_CS0_DIMMA#
M_ODT0
DDR_A_MA13
DDR_A_D32
DDR_A_D33
DDR_A_DM4
DDR_A_D34
DDR_A_D35
DDR_A_D40
DDR_A_D41
DDR_A_DQS#5
DDR_A_DQS5
DDR_A_D43
DDR_A_D42
DDR_A_D52
DDR_A_D53
M_CLK_DDR1
M_CLK_DDR#1
DDR_A_DM6
DDR_A_D51
DDR_A_D55
DDR_A_D57
DDR_A_D56
DDR_A_DQS#7
DDR_A_DQS7
DDR_A_D62
DDR_A_D63
R115 10K_0402_5%
R116 10K_0402_5%

M_CLK_DDR0 9
M_CLK_DDR#0 9
M_CLK_DDR1 9
M_CLK_DDR#1 9
DDR_CKE1_DIMMA 9
DDR_A_BS1 10
DDR_A_RAS# 10
DDR_CS0_DIMMA# 9
M_ODT0 9

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: DDRII-SODIMM SLOT1

Size: Custom | Document Number: Montevina UMA | Rev: 0.1

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10 DDR_B_DQS#[0..7]
10 DDR_B_D[0..63]
10 DDR_B_DM[0..7]
10 DDR_B_DQS[0..7]
10 DDR_B_MA[0..14]

Layout Note:
Place near
JP10

Layout Note:
Place one cap close to every 2
pullup
resistors terminated to +0.9VS

Layout Note:
Place these resistor
closely JP3,all
trace length Max = 1.5"

V_DDR_MCH_REF
V_DDR_MCH_REF 9,15

JDIMM2

DDR_CKE2_DIMMB 9
DDR_BS2 10
DDR_B_BS0 10
DDR_B_WE# 10
DDR_CAS# 10
DDR_CS3_DIMMB# 9
M_ODT3 9
CLK_SMBDATA 15,17,24
CLK_SMBCLK 15,17,24
+3VS

M_CLK_DDR2 9
M_CLK_DDR#2 9
PM_EXTTS#1 9
DDR_CKE3_DIMMB 9
DDR_B_BS1 10
DDR_B_RAS# 10
DDR_CS2_DIMMB# 9
M_ODT2 9
M_CLK_DDR3 9
M_CLK_DDR#3 9

0612 add

FOX_AS0A426-N8RN-7F
@RNN@

SO-DIMM B

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

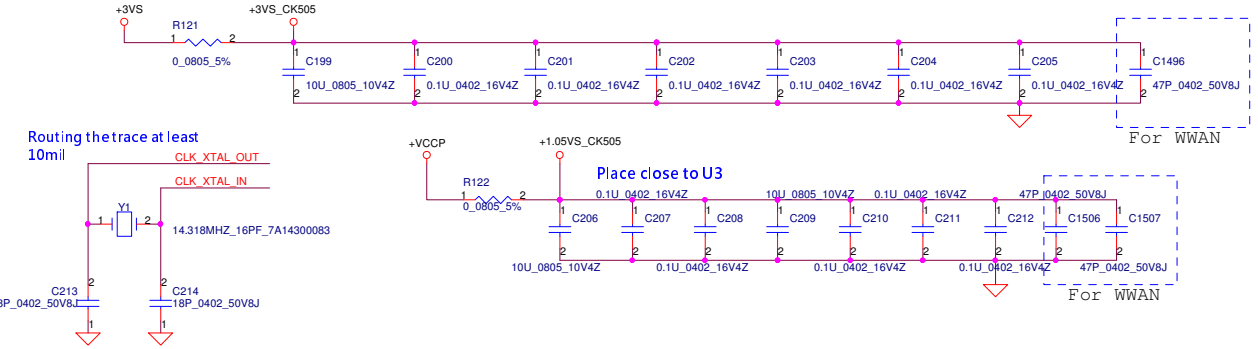
Compal Electronics, Inc.

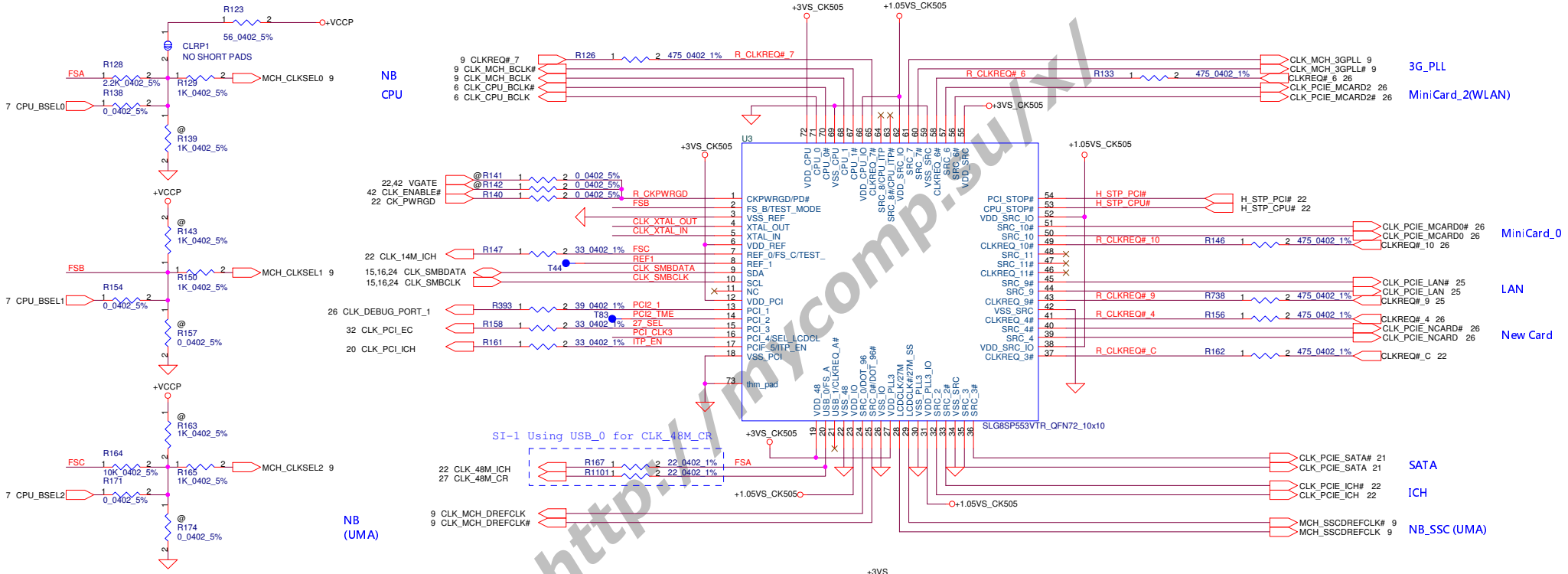
Title: DDRII-SODIMM SLOT2

Size: B | Document Number: Montevina UMA | Rev: 0.1

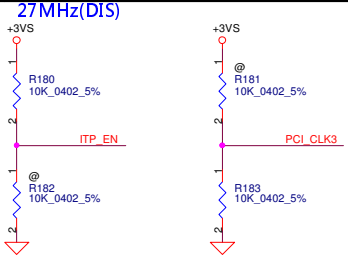
Date: Wednesday, February 18, 2009 | Sheet 16 of 46

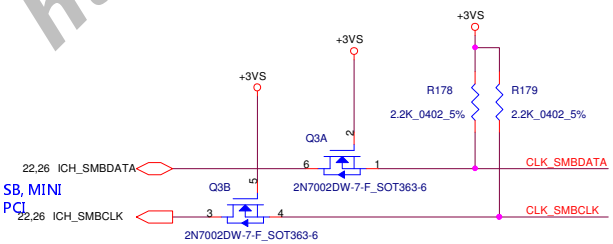
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

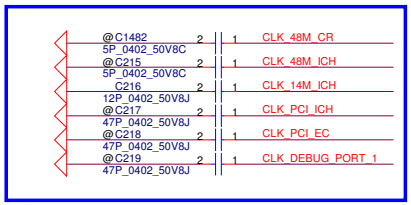




ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
PCI_CLK3	0 = Enable DOT96 & SRC1(UMA)/SRC0 & 27MHz(DIS) 1 = Enable







Install C217,C218,C219 for WWAN noise

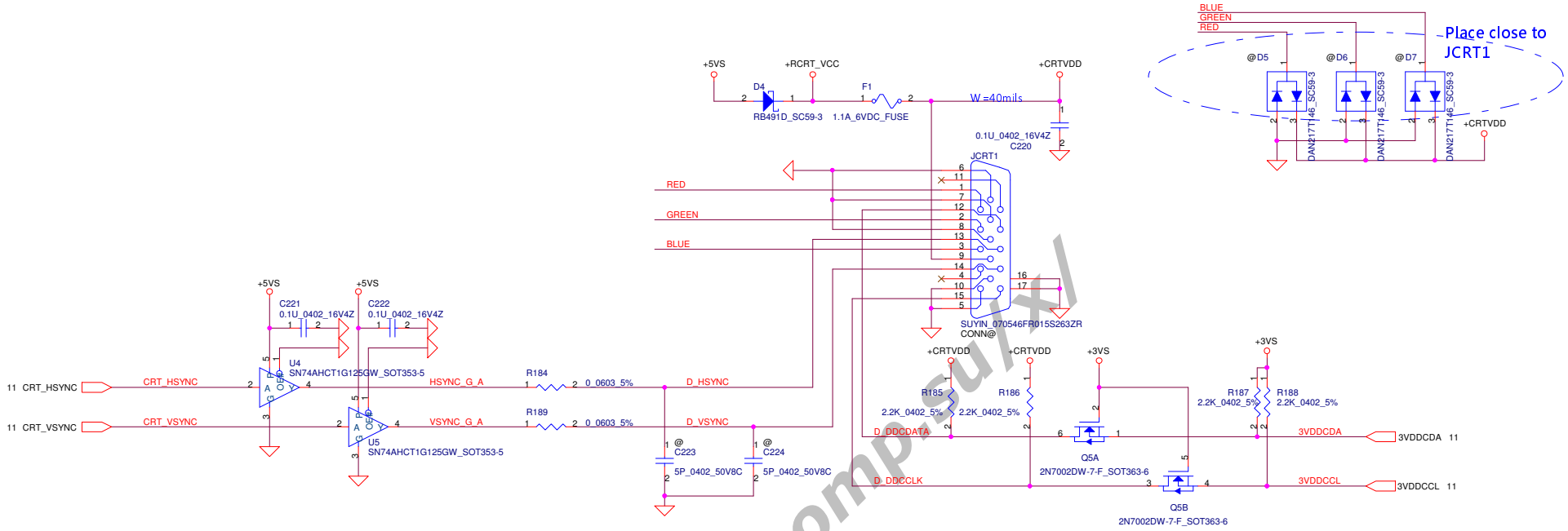
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.

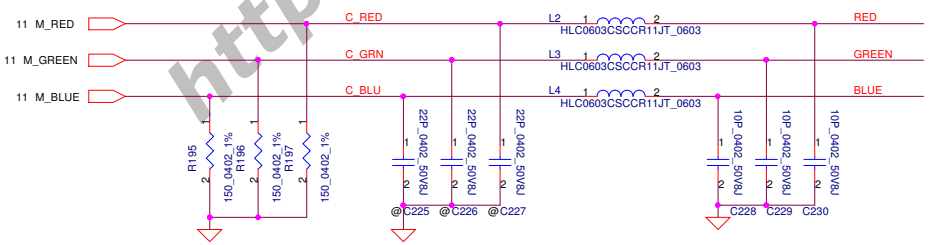
Title: Clock Generator CK505

Size: Document Number: Montevina UMA — Rev: 0.1

Date: Wednesday, February 18, 2009 — Sheet 17 of 46



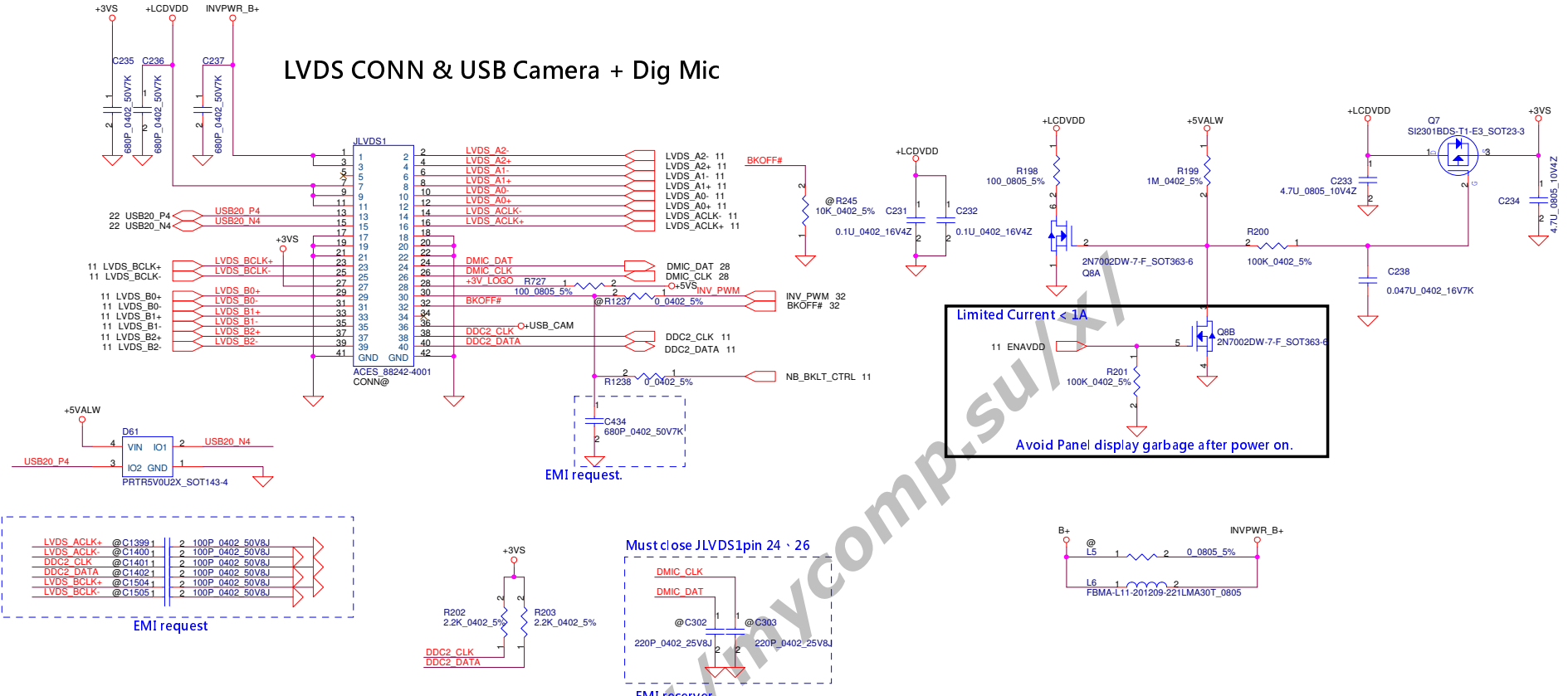
CRT Termination/EMI Filter



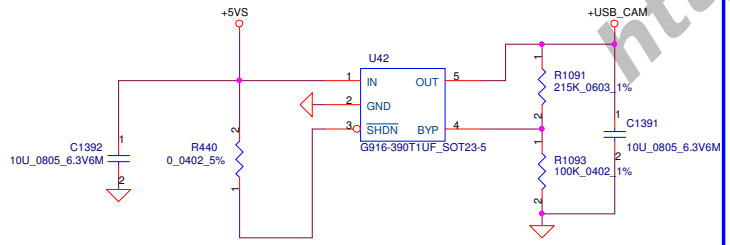
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: CRT Connector			
Size: C	Document Number: Montevina UMA		Rev: 0.1
Date: Wednesday, February 18, 2009	Sheet 18 of 46		

LVDS CONN & USB Camera + Dig Mic



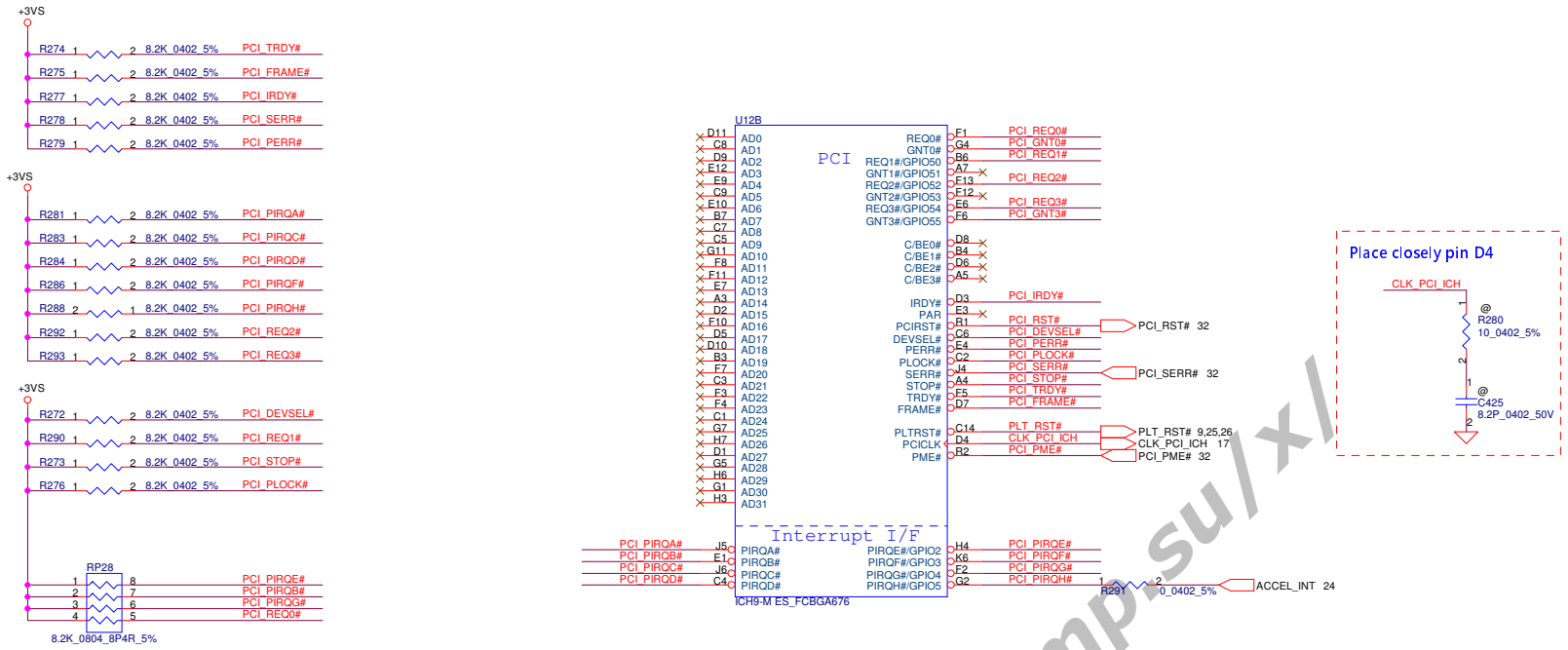
USB Camera



+USB_CAM is +3.9VS, R1091:215K; R1093:100Kohm +USB_CAM=1.25(1+R1091/R1093)

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: LCD CONN.			
Size: B	Document Number: Montevina UMA		Rev: 0.1
Date: Wednesday, February 18, 2009	Sheet 19 of 46		



A16 swap override Strap

PCI_GNT3#	Low= A16 swap override Enble High= Default*

PCI_GNT3# @R294 1 2 1K_0402_5%

Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

22 SPI_CS1#_R SPI_CS1#_R @R295 1 2 1K_0402_5%
+3VALW
PCI_GNT0# @R296 1 2 1K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.

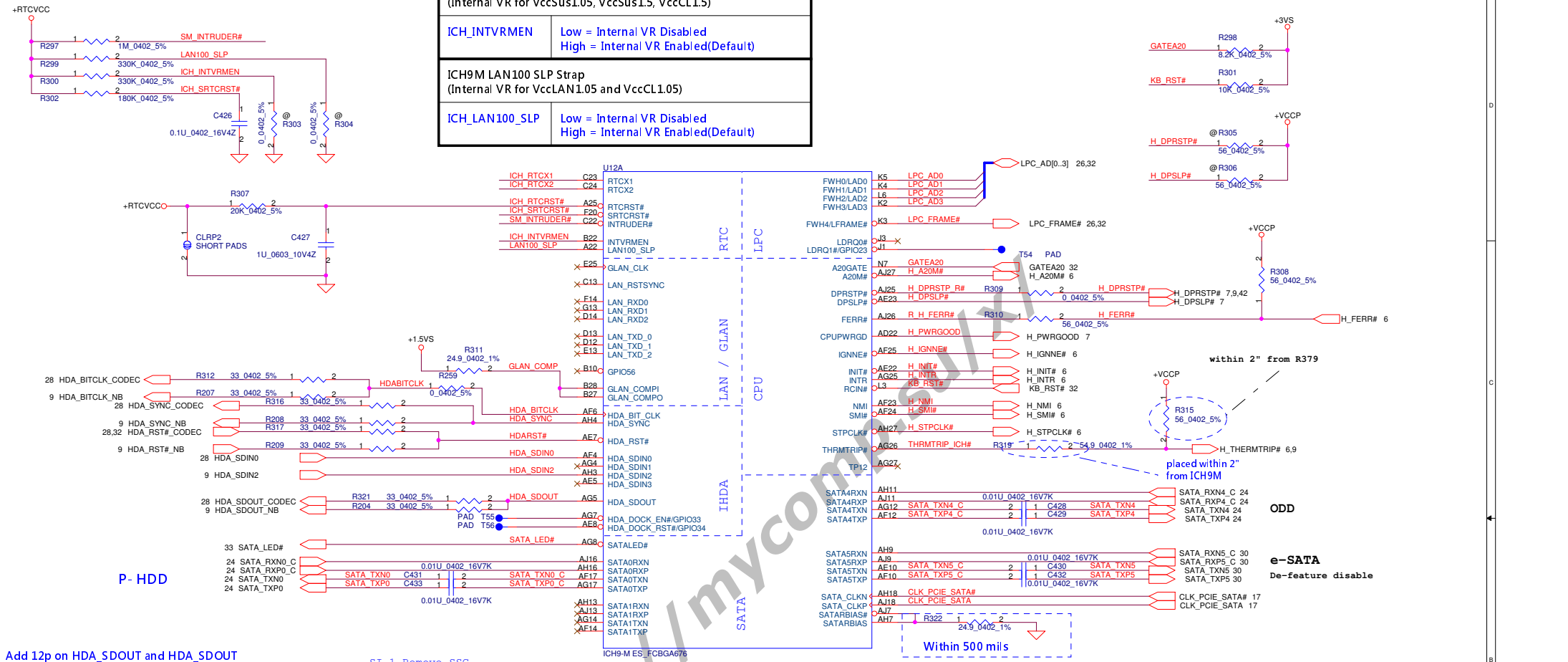
Title: ICH9(1/4)-PCI/INT

Size: A3 | Document Number: Montevina UMA | Rev: 0.1

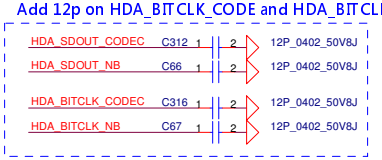
Date: Wednesday, February 18, 2009 | Sheet 20 of 46

ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH9M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



Add 12p on HDA_SDOUT and HDA_SDOUT
Add 12p on HDA_BITCLK_CODE and HDA_BITCLK_NB

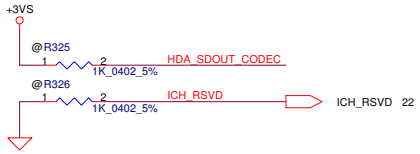


SI-1 Remove SSC

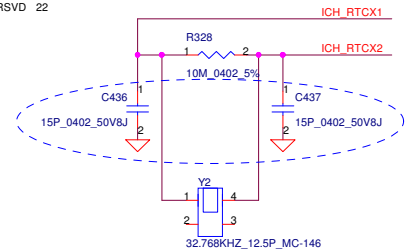
Reserve SSC for EMI

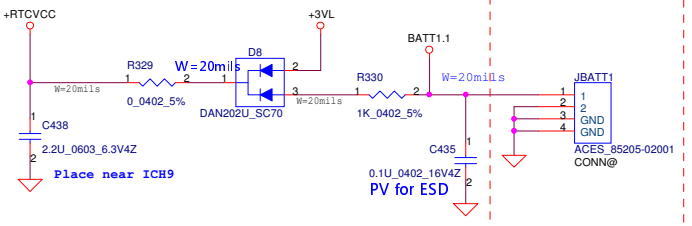
Reserve cap on HDA_BITCLK for WWAN noise issue

XOR CHAIN ENTRANCE STRAP:RSVD



ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	





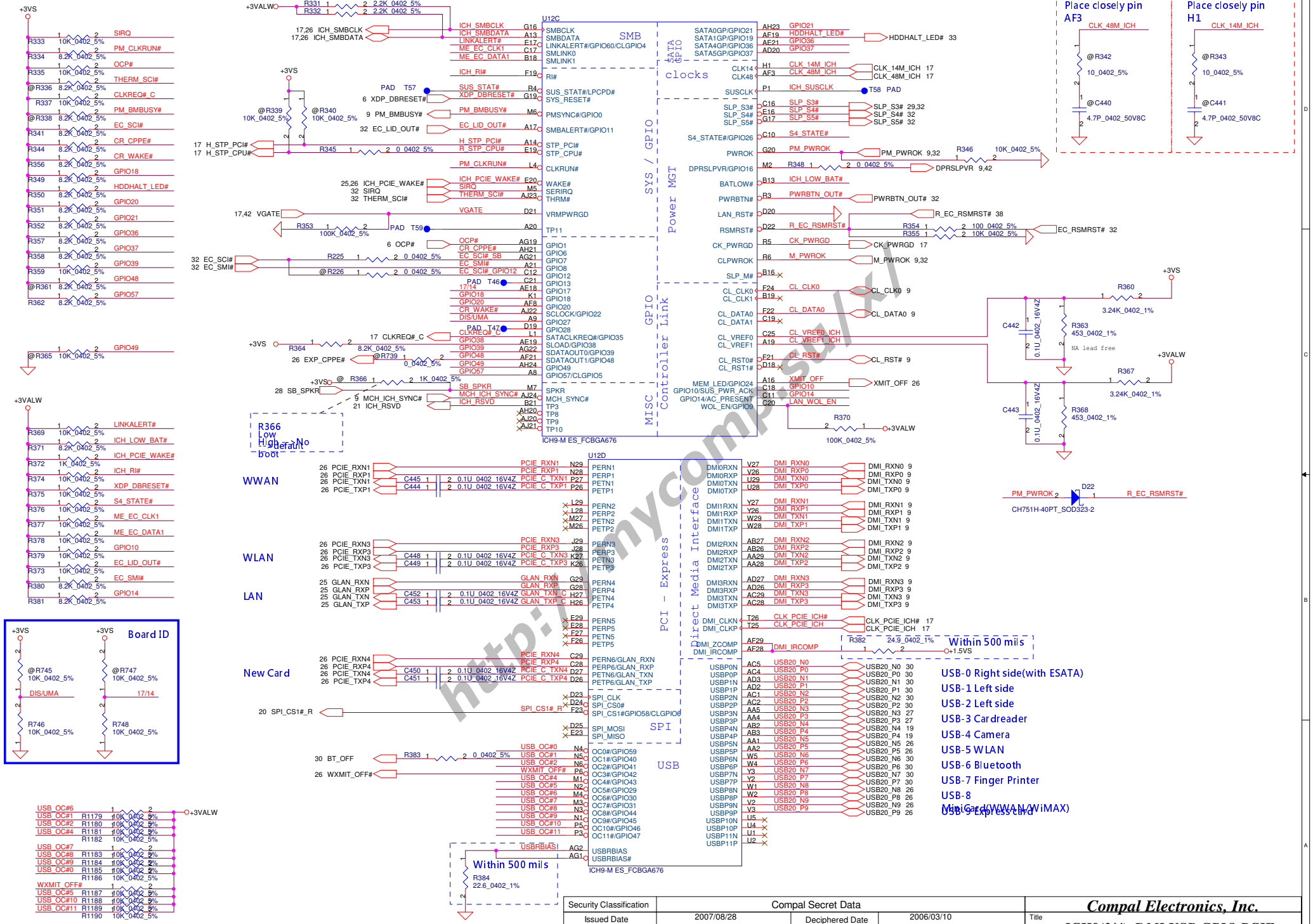
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: ICH9(2/4)_LAN,HD,IDE,LPC

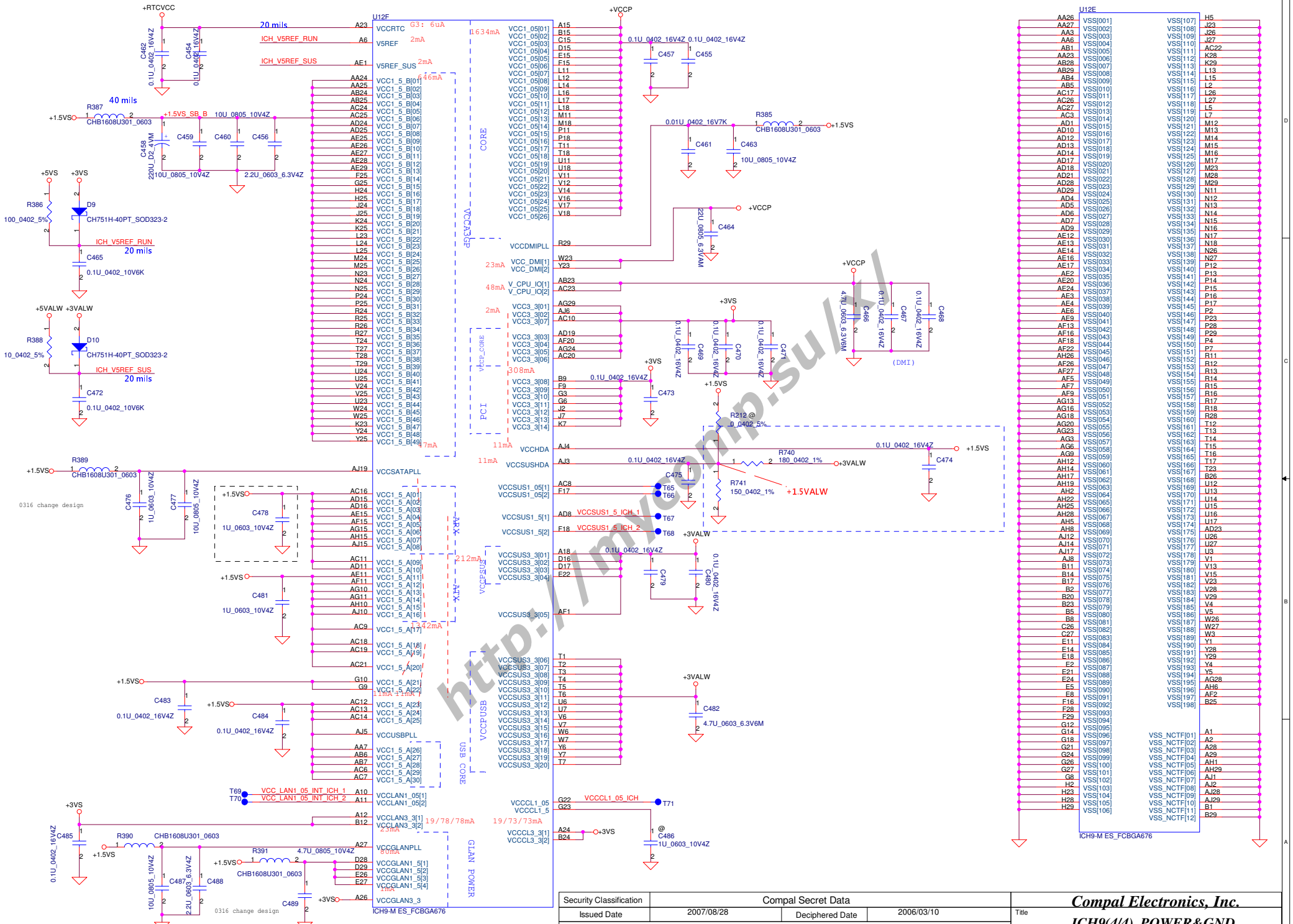
Size: Custom | Document Number: Montevina UMA | Rev: 0.1

Date: Wednesday, February 18, 2009 | Sheet 21 of 46

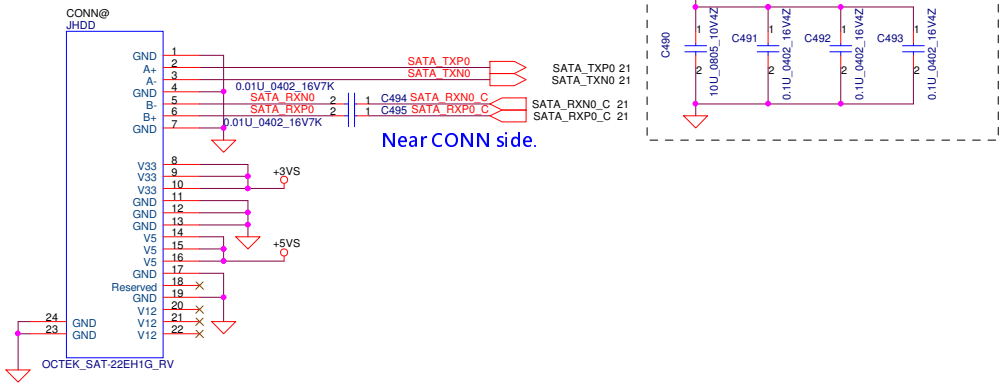


Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

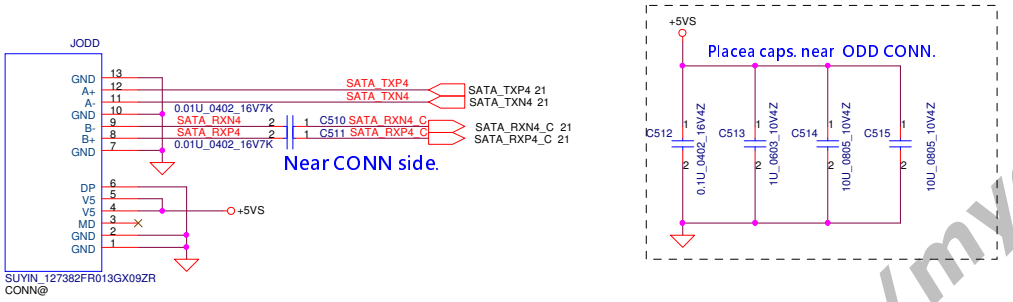
Compal Electronics, Inc.			
Title	ICH9(3/4)_DMI,USB,GPIO,PCIE		
Size: Custom	Document Number: Montevina UMA		Rev: 0.1
Date: Wednesday, February 18, 2009	Sheet 22 of 46		



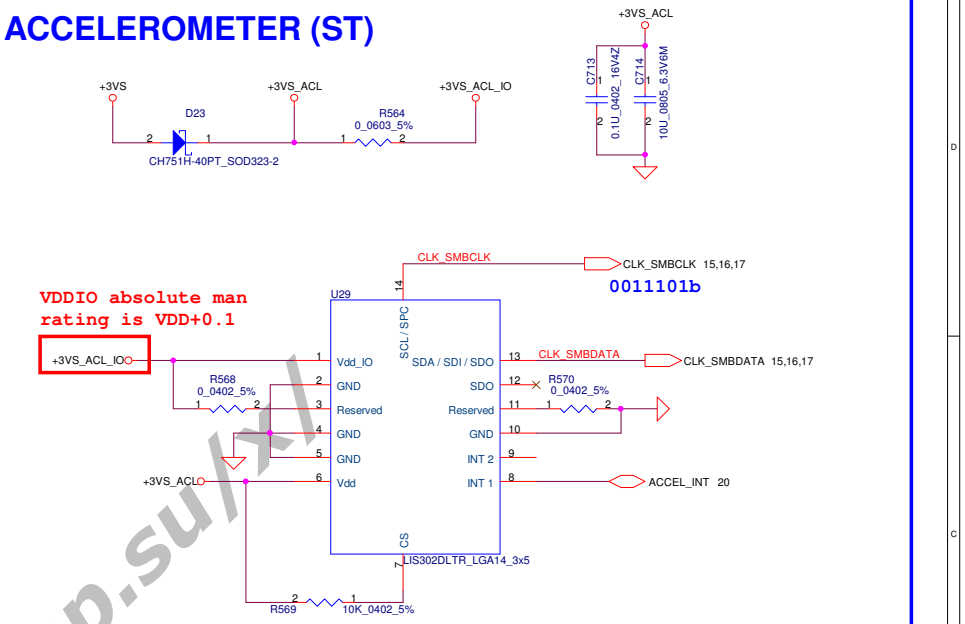
HDD Connector



CD-ROM Connector



ACCELEROMETER (ST)



PA@ ZZZ PCB-MB

PR@ ZZZ PCB-MB

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

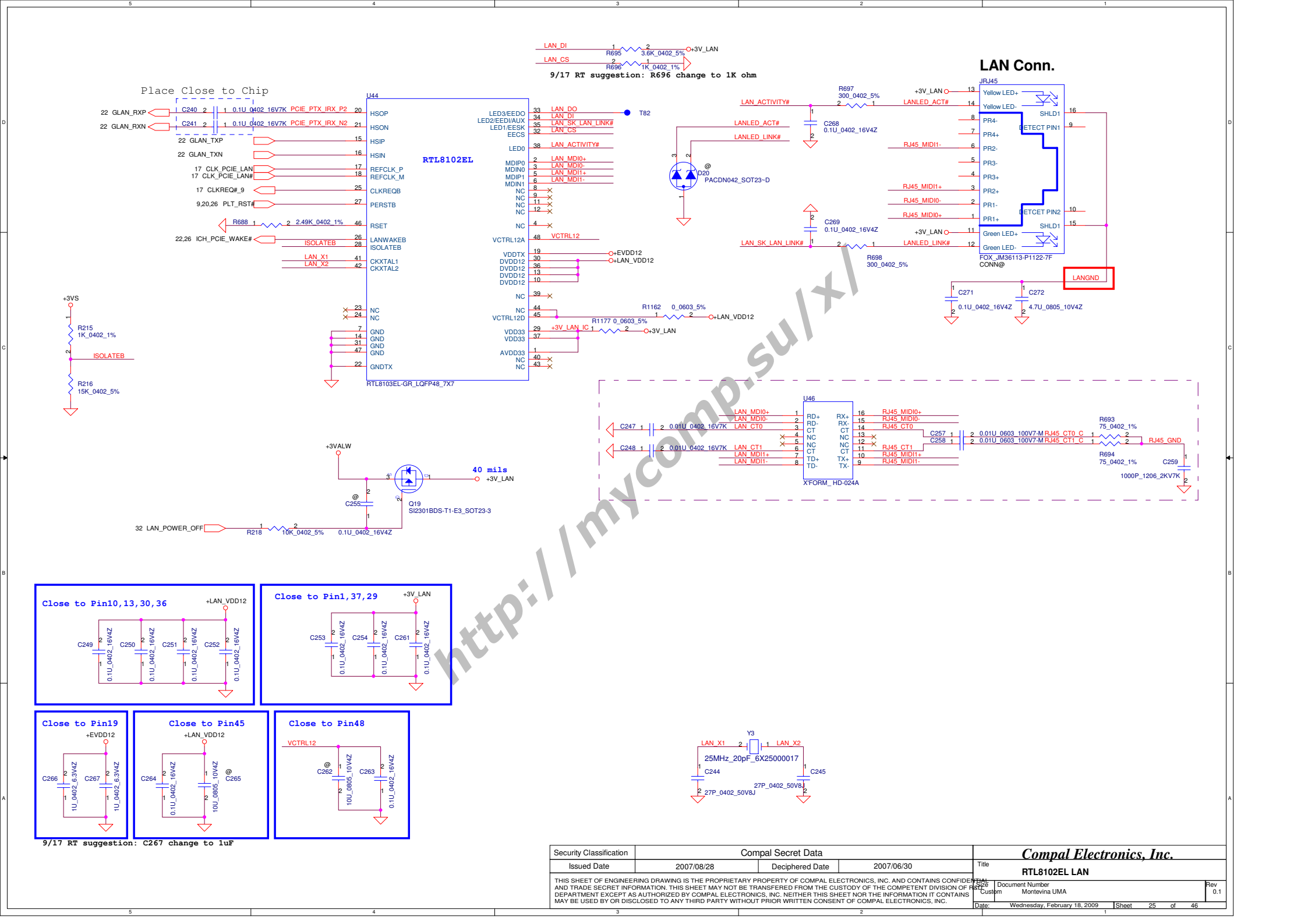
Compal Electronics, Inc.

Title: HDD & CDROM

Size: Custom | Document Number: Montevina UMA | Rev: 0.1

Date: Wednesday, February 18, 2009 | Sheet 24 of 46

LAN Conn.



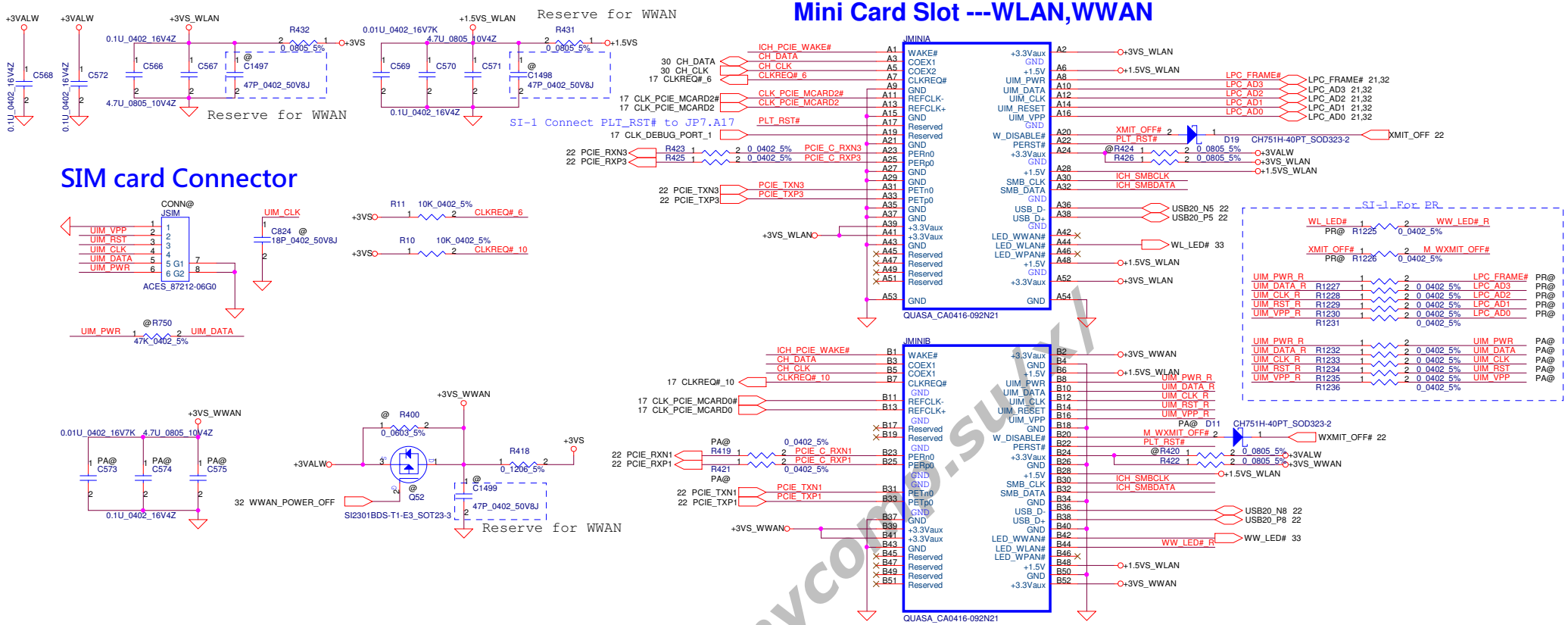
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2007/06/30

Compal Electronics, Inc.

Title: **RTL8102EL LAN**

Size: C26 Custom	Document Number: Montevina UMA	Rev: 0.1
Date: Wednesday, February 18, 2009	Sheet 25 of 46	

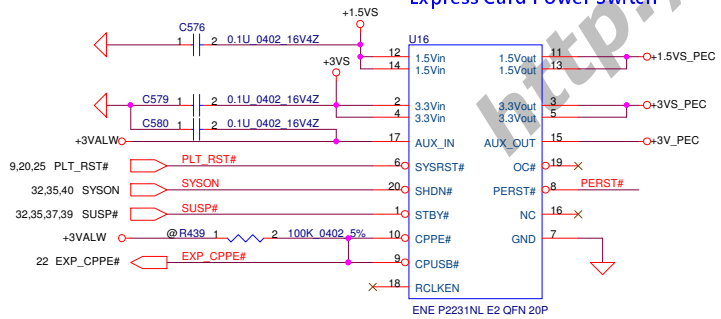
Mini Card Slot ---WLAN,WWAN



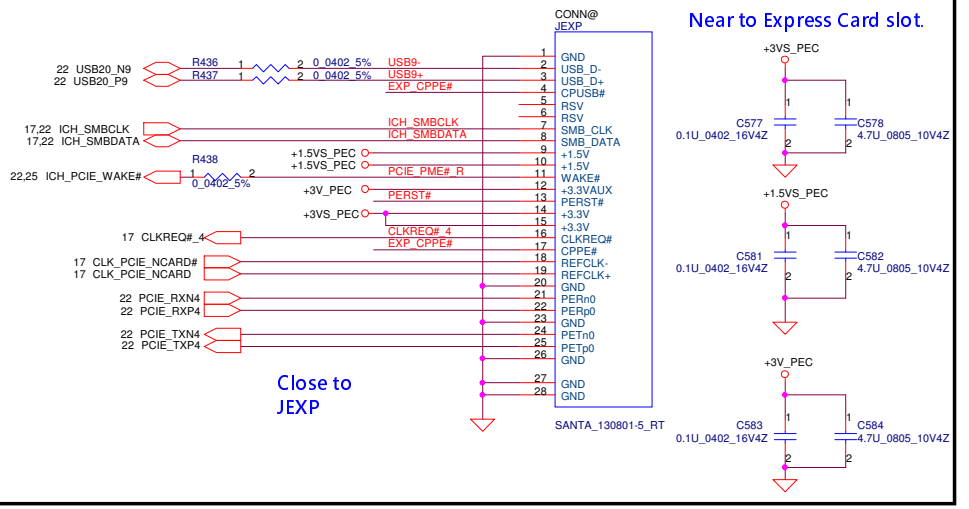
SIM card Connector

New Card

Express Card Power Switch

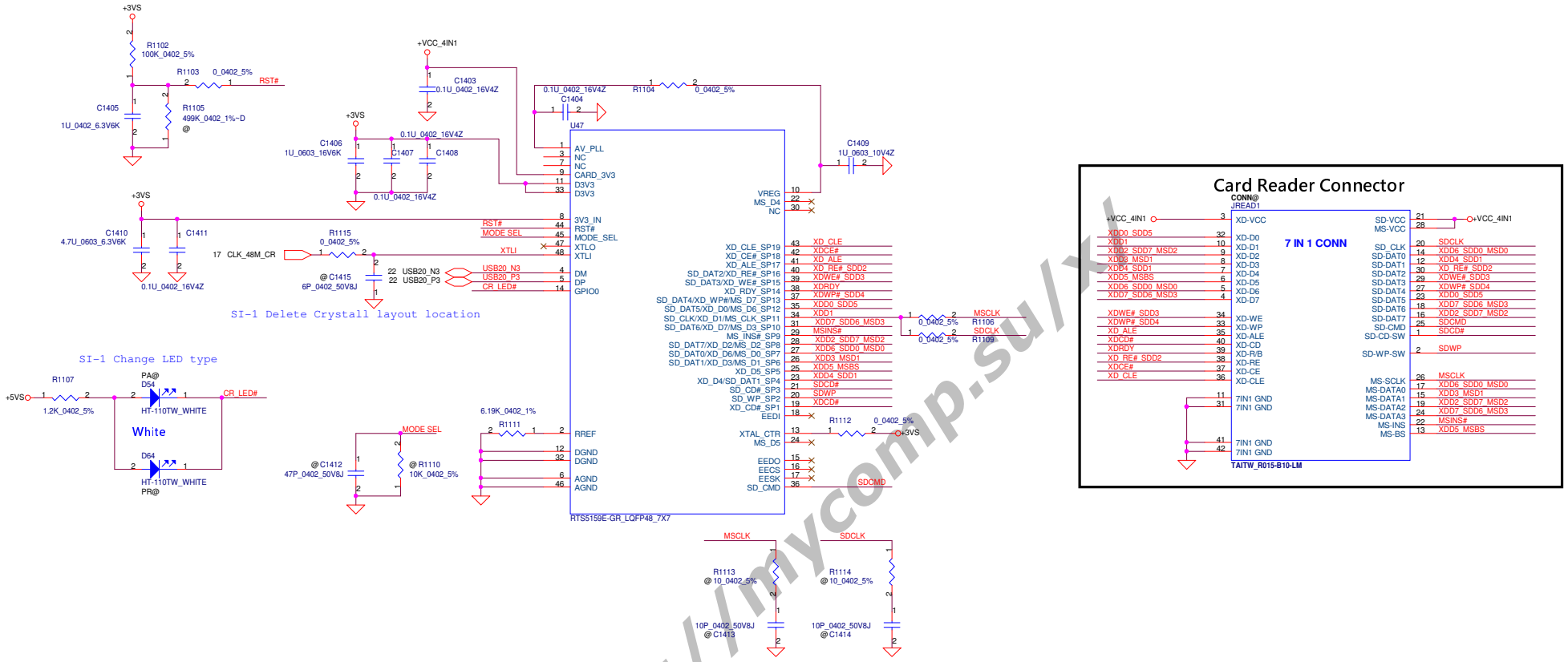


internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title	WLAN, WWAN, New Card		
Size	Document Number	Montevina UMA	Rev 0.1
Date: Wednesday, February 18, 2009	Sheet 26 of 46		



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/10/06

Compal Electronics, Inc.

Title: **USB CardReader&CONN**

Size	Document Number	Rev
Custom	Montevina UMA	0.1

Date: Wednesday, February 18, 2009 | Sheet 27 of 46

CODEC POWER

(4.75V(4.56~4.94V)) 300mA

SI-1 Delete CODEC POWER IC

+VDDA_CODEC

R1122 0_0603_5%

+VDDA_CODEC_R

C1422 0.1U_0402_16V7K

C1423 1U_0603_10V4Z

R1123 BLM18BD601SN1D_0603

+3VS

+3VS_HDA

C1424 0.1U_0402_16V7K

C1425 1U_0603_10V4Z

C1426 10U_0805_10V4Z

U49

DVDD_LV

DVDD_CORE

AVDD

SENSE_A

SENSE_B

PORT_A_L

PORT_A_R

PORT_B_L

PORT_B_R

VREFOUT_B

PORT_C_L

PORT_C_R

VREFOUT_C

PORT_D_L

PORT_D_R

PORT_E_L

PORT_E_R

PC_BEEP/MONO

CAP2

VREFFILT

AVSS

TPAD

DVSS

92HD75B1X5NLGXYAX8 QFN 32P 1.5V CODEC

HDA_BITCLK_CODEC

HDA_SDIN0

HDA_SDOUT_CODEC

HDA_SYNC_CODEC

HDA_RST#_CODEC

HDA_BITCLK

HDA_SDI

HDA_SDO

HDA_SYNC

HDA_RST#

33_0402_5%

R1130

SPDIF_OUT_0

SPDIF_OUT_1/GPIO7

EAPD/GPIO0/SPDIF_OUT 0 or 1

EAPD_CODEC

DMIC_CLK

DMIC0/GPIO1

DMIC_CLK

DMIC_DAT

R1132 22_0603_1%

R1178 0_0603_5%

SENSEA

R1128 100K_0402_5%

@C1428 1000P_0402_50V7K

+VDDA_CODEC_R

R1124 2.49K_0402_1%

R1125 39.2K_0402_1%

R1126 20K_0402_1%

C1429 1000P_0402_50V7K

HP_DET# 29

EXTMIC_DET# 29

HP_IN_L

HP_IN_R

HP_IN_L 29

HP_IN_R 29

HP Jack

C1430 2.2U_0603_6.3V6K

C1431 2.2U_0603_6.3V6K

MIC_EXTL

MIC_EXTR

MIC_EXT_L

MIC_EXT_R

MIC_EXT_L 29

MIC_EXT_R 29

Jack MIC

MIC_INL

MIC_INR

C1432 2.2U_0603_6.3V6K

MIC_IN_L

MIC_IN_L 29

Internal MIC

LINE_OUT_L

LINE_OUT_R

LINE_OUT_L 29

LINE_OUT_R 29

Internal SPKR.

C1433 2.2U_0603_6.3V6K

MIC_IN_R

MIC_IN_R 29

MONO_INR

0.1U_0402_16V7K

C1434

MONO_IN

R1133 47K_0402_5%

R1134 10K_0402_5%

+VDDA_CODEC

C1435 0.1U_0402_16V7K

R1135 10K_0402_5%

C1459 0.1U_0402_16V7K

22 SB_SPKR

Q10A 2N7002DW-7-F_SOT363-6

Q10B 2N7002DW-7-F_SOT363-6

C1436 10U_0805_10V4Z

C1437 1U_0603_10V4Z

PV-1 ESD request

+1.5VS

R1239 4.7K_0402_5%

HDA_RST#_CODEC

C1516 0.01U_0402_16V7K

SI-1 For EMI request

19 DMIC_CLK

19 DMIC_DAT

PV-1 For EMI

MIC_EXTL

MIC_EXTR

D58 PSOT24C_SOT23-3

R1116 0_0402_5%

VREFOUT_B

C1418 1U_0603_10V4Z

R1118 4.7K_0402_5%

R1119 4.7K_0402_5%

MIC_EXT_R

MIC_EXT_L

R1117 1K_0402_5%

VREFOUT_C

C1419 1U_0603_10V4Z

R1120 4.7K_0402_5%

R1121 4.7K_0402_5%

MIC_IN_R

MIC_IN_L

C1478 1000P_0402_50V7K

C1479 1000P_0402_50V7K

C1480 1000P_0402_50V7K

C1481 1000P_0402_50V7K

R1174 0_0402_5%

R1175 0_1206_5%

R1176 0_1206_5%

GNDA 29

GND

GNDA

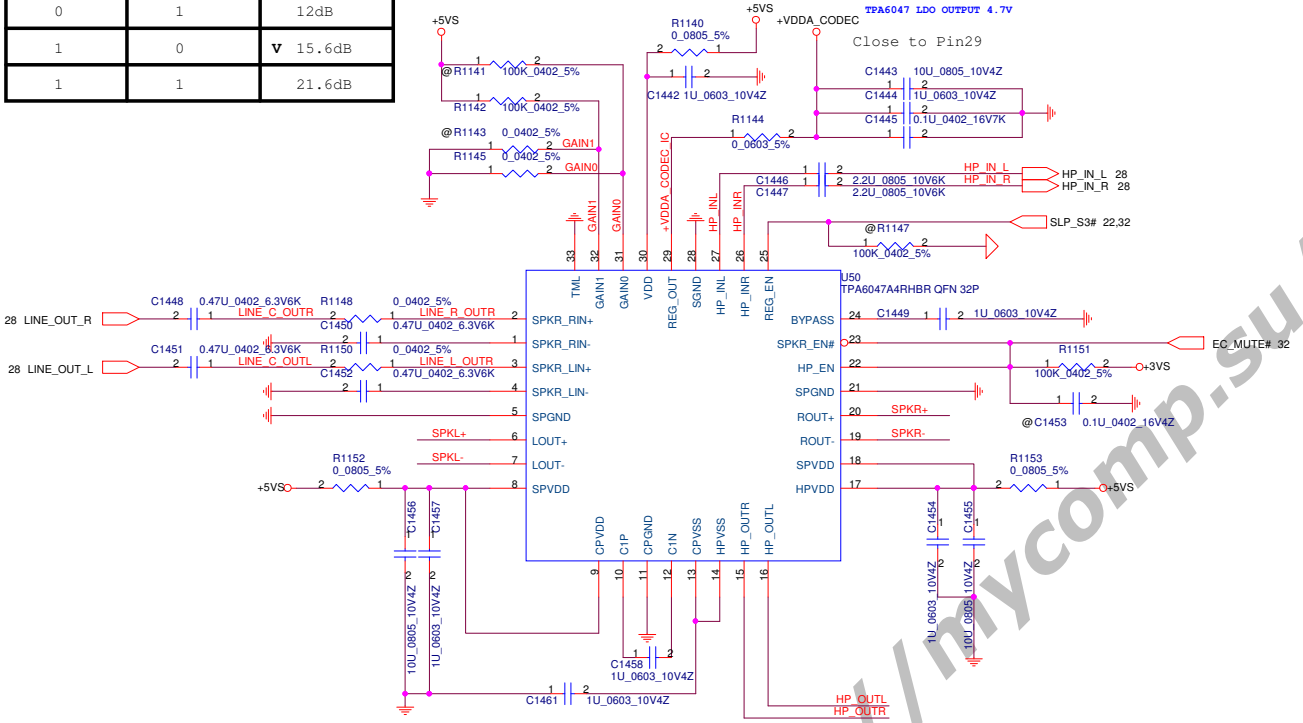
090212 For PC Beep Noise

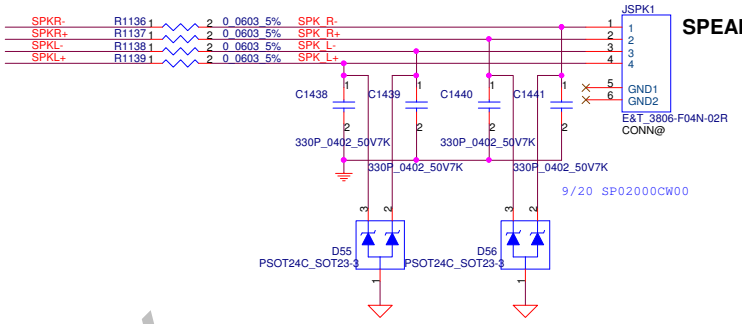
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

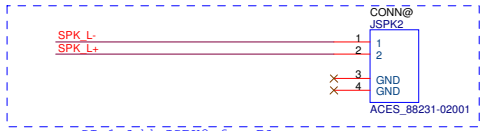
Title	Codec_IDT9275B		
Size: Custom	Document Number: Montevina UMA		Rev: 0.1
Date: Wednesday, February 18, 2009	Sheet 28 of 46		

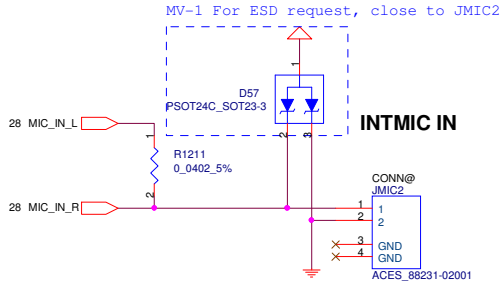
AMP. FOR INTERNAL SPEAKER

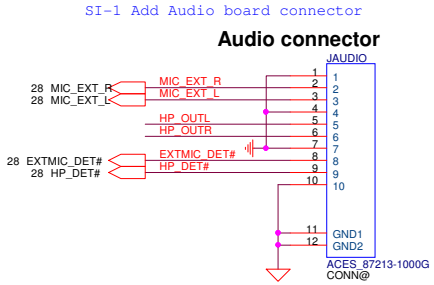
GAIN1	GAIN0	Av(inv)
0	0	10dB
0	1	12dB
1	0	15.6dB
1	1	21.6dB

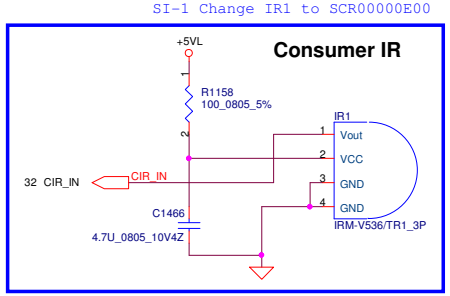








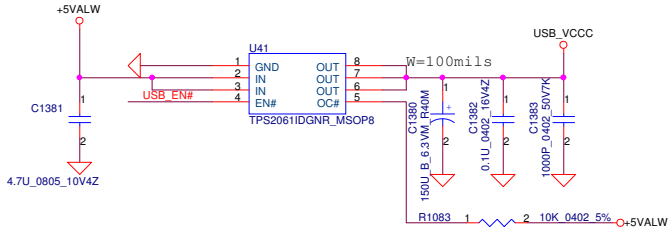




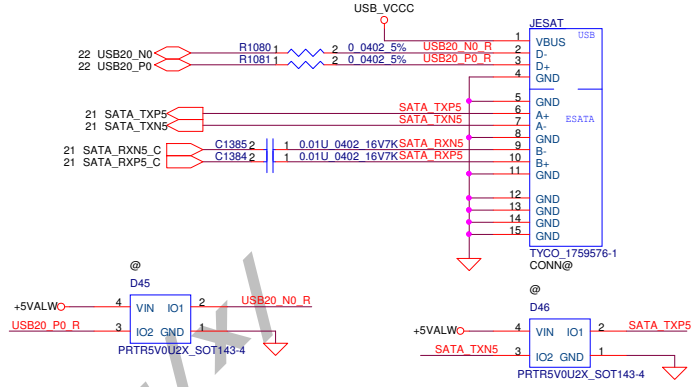
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Title	AMP & Audio Jack		
Size: Custom	Document Number: Montevina UMA		Rev: 0.1
Date: Wednesday, February 18, 2009	Sheet 29 of 46		

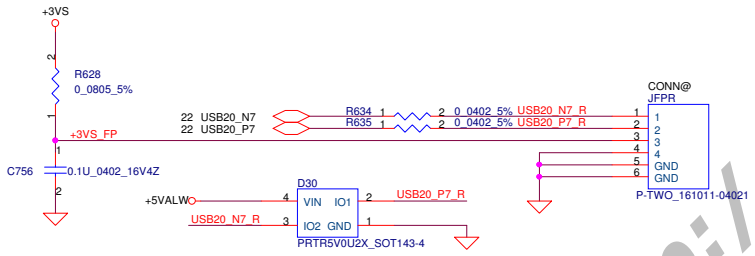
Right side USB Power Switch



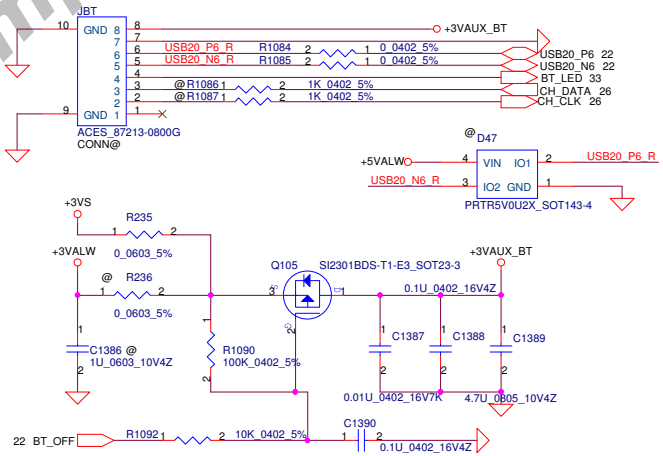
Right side ESATA/USB combination Connector



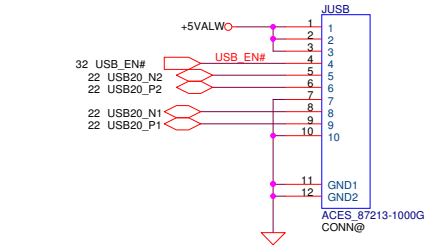
Finger printer



BT Connector



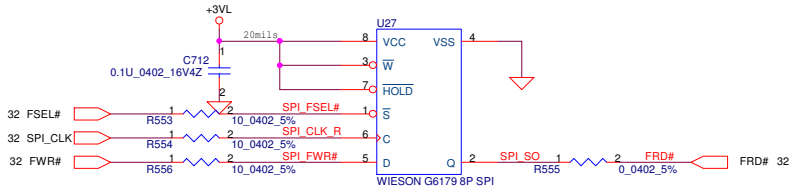
USB cable connector for Right side



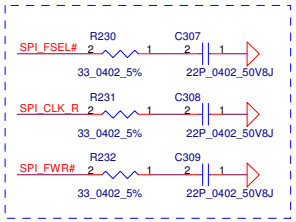
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: USB, BT, eSATA			
Size:	Document Number: Montevina UMA		Rev: 0.1
Date: Wednesday, February 18, 2009	Sheet 30 of 46		

SPI ROM



SP07000F500 S SOCKET WIESON G6179-100000 8P SPIFLASH
WIESO_G6179-100000_8P



EMI request

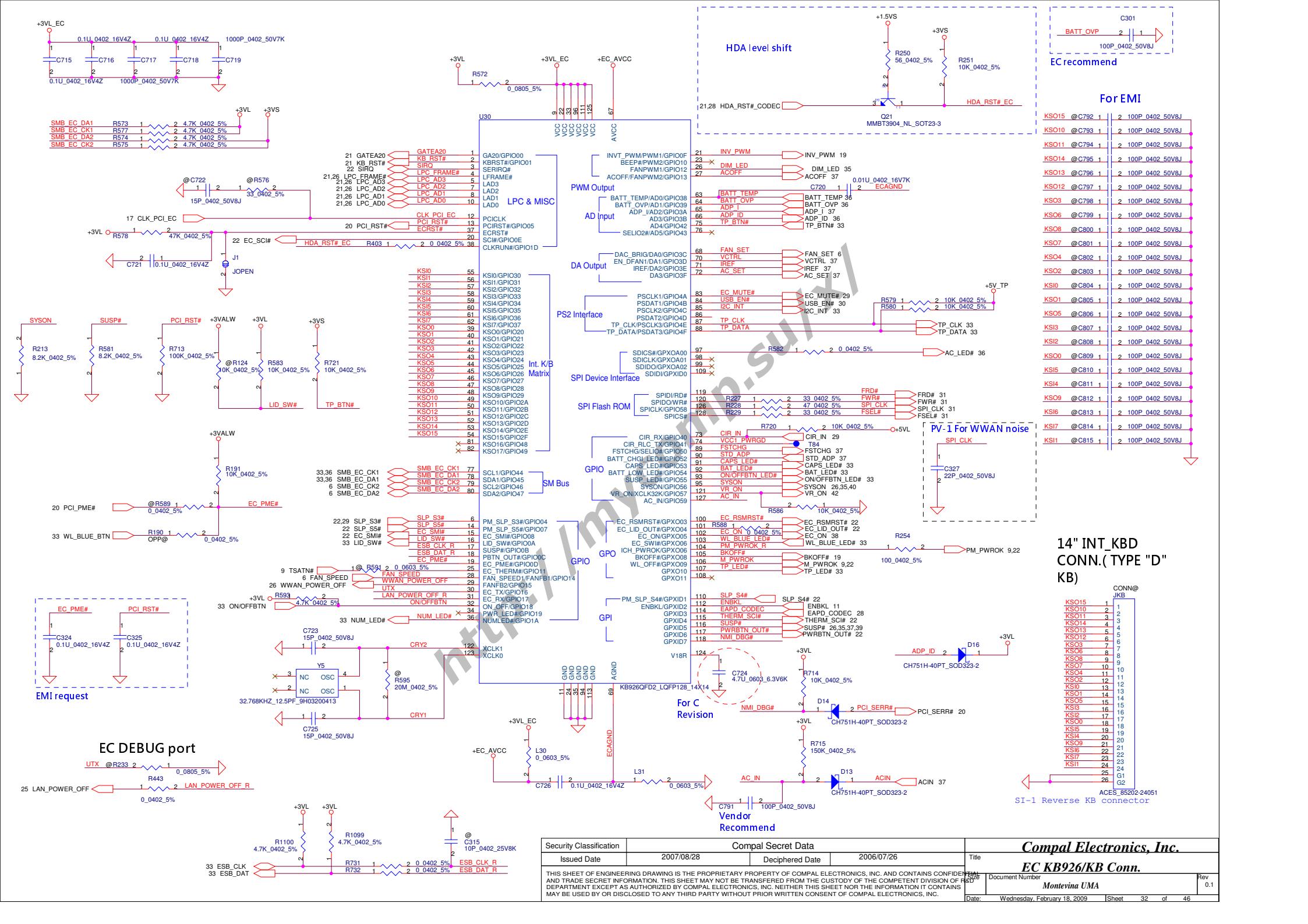
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **BIOS ROM**

Size: B26 | Document Number: *Montevina UMA* | Rev: 0.1

Date: Wednesday, February 18, 2009 | Sheet 31 of 46


U30
KB926QFD2_LQFP128_14X14
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
Int. K/B Matrix
SM Bus
GPIO
GPO
GPI
HDA level shift
Q21
MMBT3904_NL_SOT23-3
EC recommend
For EMI
PV-1 For WWAN noise
14" INT_KBD CONN.(TYPE "D" KB)
CONN@ JKB
ACES_85202-24051
SI-1 Reverse KB connector
EMI request
EC DEBUG port
For C Revision
Vendor Recommend
32.768KHZ_12.5PF_9H03200413
CH751H-40PT_SOD323-2
Security Classification
Compal Secret Data
Issued Date
2007/08/28
Deciphered Date
2006/07/26
Compal Electronics, Inc.
EC KB926/KB Conn.
Document Number
Montevina UMA
Rev
0.1
Date:
Wednesday, February 18, 2009
Sheet
32
of
46

SI-1 Delete SW2

Power Button
for debug only

MV-1 For ESD request, close to JTPSW

TP_LED#
TP_BTN#
+5VS
D65 SM05_SOT23
D66 SM05_SOT23

System LED Conn

White
AMBER

+5VALW
+5VS
+3VS
32 BAT_LED#
21 SATA_LED#
22 HDDHALT_LED#
ON/OFFBTN_LED#
CONN@ JLED
ACES_87213-0800G

Caps-Lock Conn

CONN@ JCAP
+5VS
CAPS_LED# 32
P-TWO_161011-04021

Keyboard backlight Conn

+5VS_LED
R205 0_0805_5%
CONN@ JKBL
GND
GND
P-TWO_161011-04021

T/P Board (Inculde T/P_ON/OFF)

CONN@ JTPSW
TP_LED#
TP_BTN#
+5VS
TP_LED# 32
TP_BTN# 32
GND
GND
P-TWO_161011-04021

SI-1 Change Cap board power rail to +3VL

SWITCH BOARD.

+3VL
+5VALW
ENE@ C326 33P_0402_50V8K
ESB_CLK_CAP
R51 0_0805_5% Main@
R53 0_0805_5% OPP@
4.7U_0603_6.3V6K
C313
Cypress@ R729 0_0402_5%
Cypress@ R730 0_0402_5%
32,36 SMB_EC_CK1
32,36 SMB_EC_DA1
32 WL_BLUE_BTN
OPP@ R151 0_0402_5%
WL_BLUE_LED# OPP@ R1191 0_0402_5%
+5VS
JCSB_CONN@
32 ON/OFFBTN_LED#
32 ESB_CLK
32 ESB_DAT
32 I2C_INT
+5VALW
32 LID_SW#
32 ON/OFFBTN
ENE@ R56 FBMA-11-100505-801T 0402
R149 FBMA-11-100505-801T 0402
ESB_CLK_CAP
ESB_DAT_CAP
ENE@ Close to JP59
main@ R169 1.8K_0402_5%
R238 1K_0402_1%
GND
GND
P-TWO_161021-10021
32 NUM_LED#
R1192 0_0402_5% OPP@
C1518 0.1U_0402_16V4Z
@D60 SM05_SOT23
MV-1 For ESD request, close to JCSB

T/P Board Conn

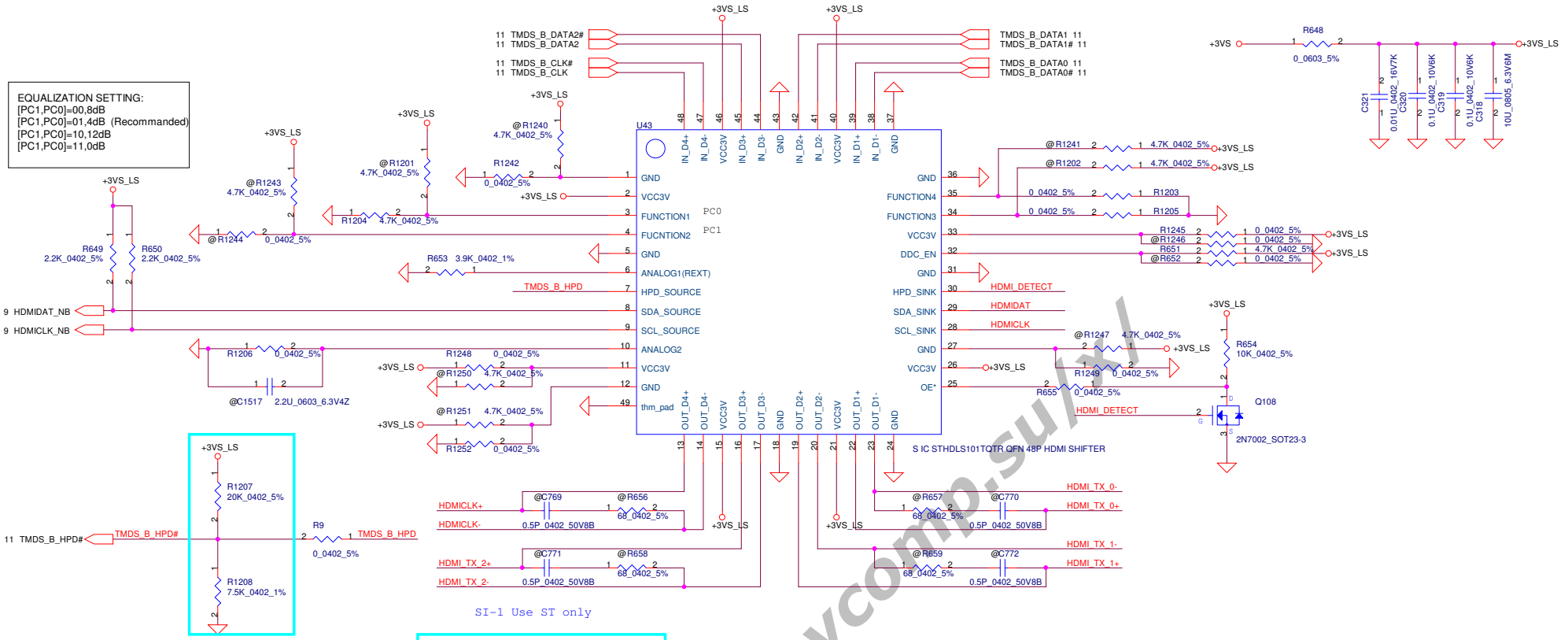
TP_DATA
TP_CLK
D28 SM05_SOT23
+5VALW
+5V_TP
R691 0_0603_5%
+5V_TP
C729 0.1U_0402_16V4Z
+5V_TP
D67 SM05_SOT23
CONN@ JTP
TP_CLK
TP_DATA
TP_CLK 32
TP_DATA 32
GND
GND
P-TWO_161011-04021
@C730 100P_0402_50V8J
@C731 100P_0402_50V8J
MV-1 For ESD request, close to JTP

Mini card LED

+3VS
R193 10K_0402_5%
WL_BLUE_LED# 32
Q11 2N7002_SOT23-3
30 BT_LED
R716 100K_0402_5%
D24
26 WL_LED#
26 WW_LED#
WL_BLUE_LED#
PSOT24C_SOT23-3

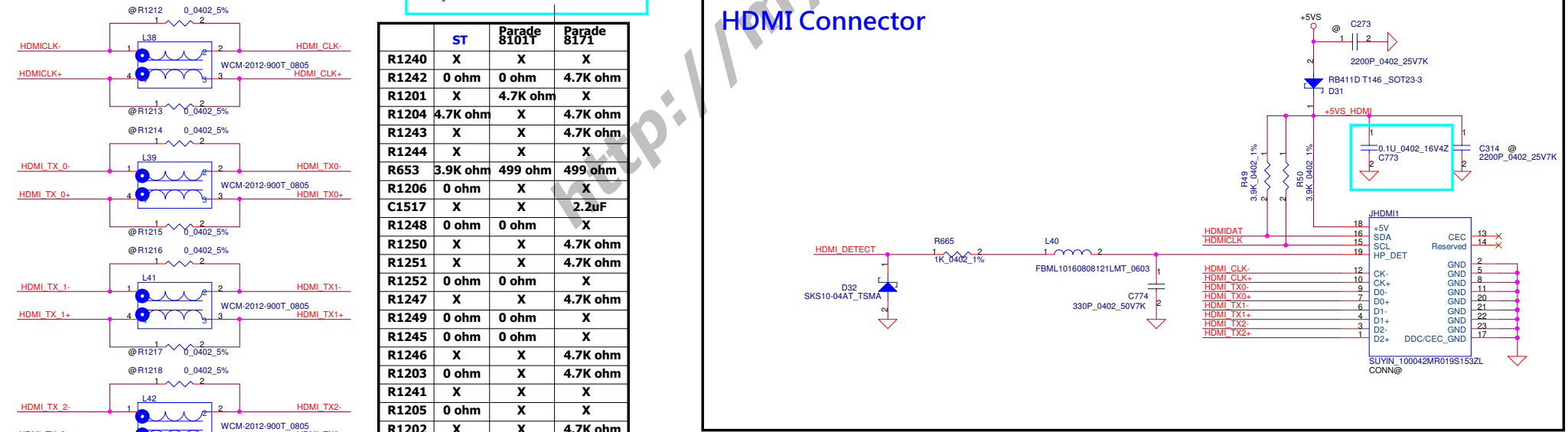
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Title	Compal Electronics, Inc.		
	KBD, ON/OFF, SW, CIR		
Size	Document Number	Montevina UMA	Rev 0.1
Date: Wednesday, February 18, 2009	Sheet 33 of 46		



To option use ST or Parade

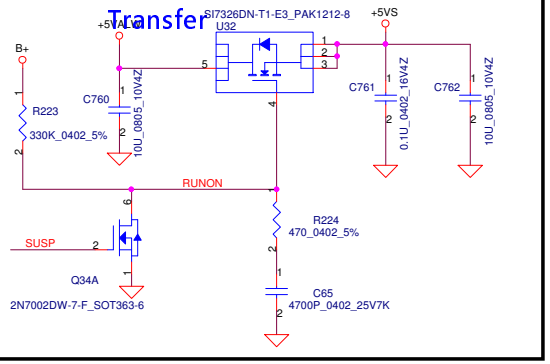
	ST	Parade 8101T	Parade 8171
R1240	X	X	X
R1242	0 ohm	0 ohm	4.7K ohm
R1201	X	4.7K ohm	X
R1204	4.7K ohm	X	4.7K ohm
R1243	X	X	4.7K ohm
R1244	X	X	X
R653	3.9K ohm	499 ohm	499 ohm
R1206	0 ohm	X	X
C1517	X	X	2.2uF
R1248	0 ohm	0 ohm	X
R1250	X	X	4.7K ohm
R1251	X	X	4.7K ohm
R1252	0 ohm	0 ohm	X
R1247	X	X	4.7K ohm
R1249	0 ohm	0 ohm	X
R1245	0 ohm	0 ohm	X
R1246	X	X	4.7K ohm
R1203	0 ohm	X	4.7K ohm
R1241	X	X	X
R1205	0 ohm	X	X
R1202	X	X	4.7K ohm
C773	0.1uF	1uF	1uF
R1207	V	X	X
R1208	V	X	X



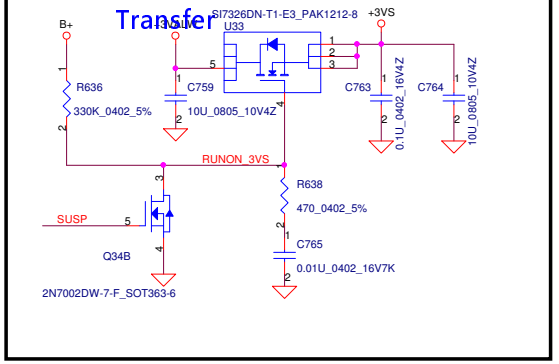
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.	
Title: HDMI LS & Conn.	
Size: Custom	Document Number: Montevina UMA
Rev: 0.1	
Date: Wednesday, February 18, 2009	Sheet 34 of 46

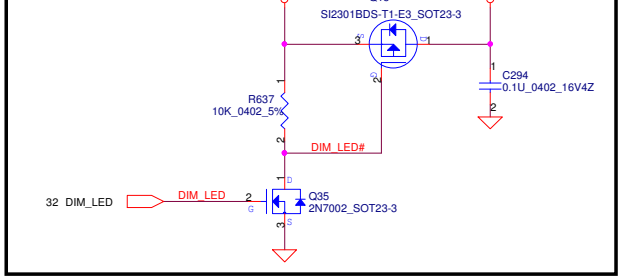
+5VALW to +5VS Transfer



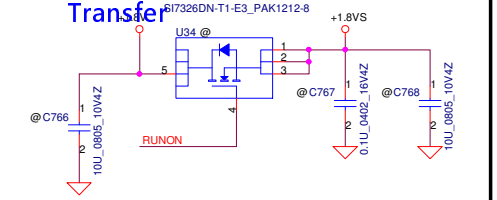
+3VALW to +3VS Transfer

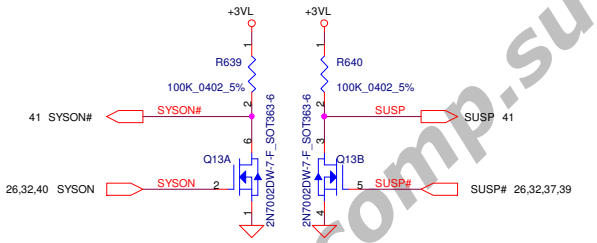


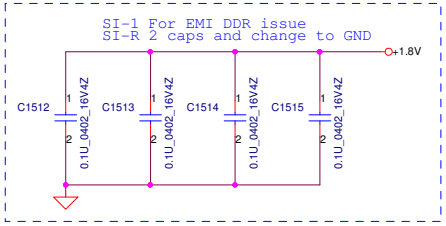
DIM LED



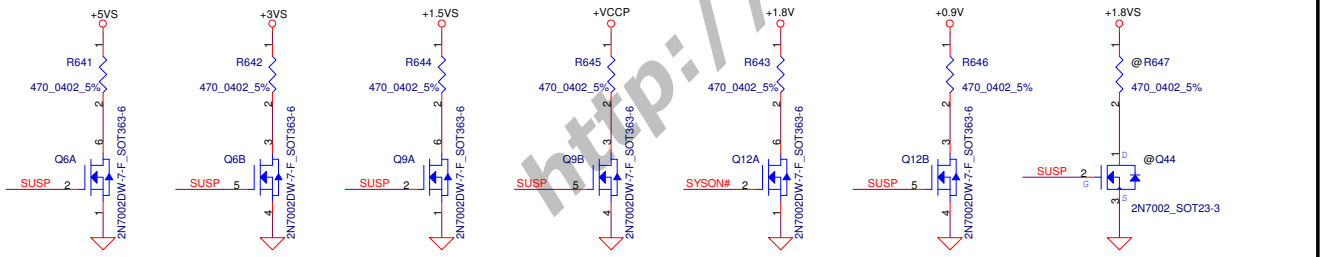
+1.8V to +1.8VS Transfer

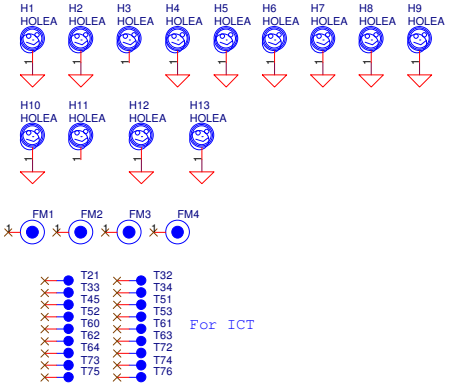






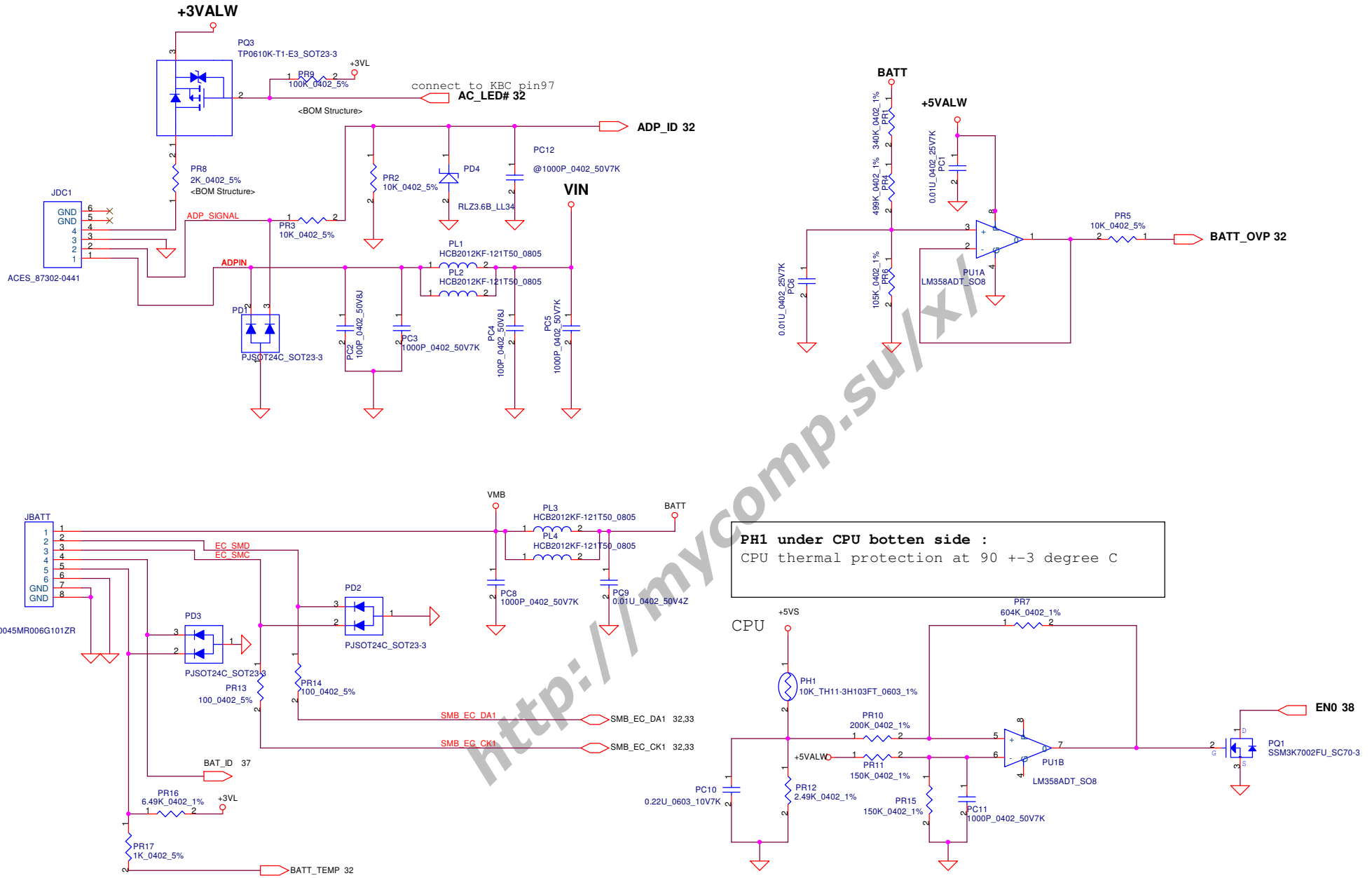
Discharge circuit





Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title	DC/DC Interface		
Size	Document Number	Montevina UMA	Rev 0.1
Date: Wednesday, February 18, 2009	Sheet 35 of 46		



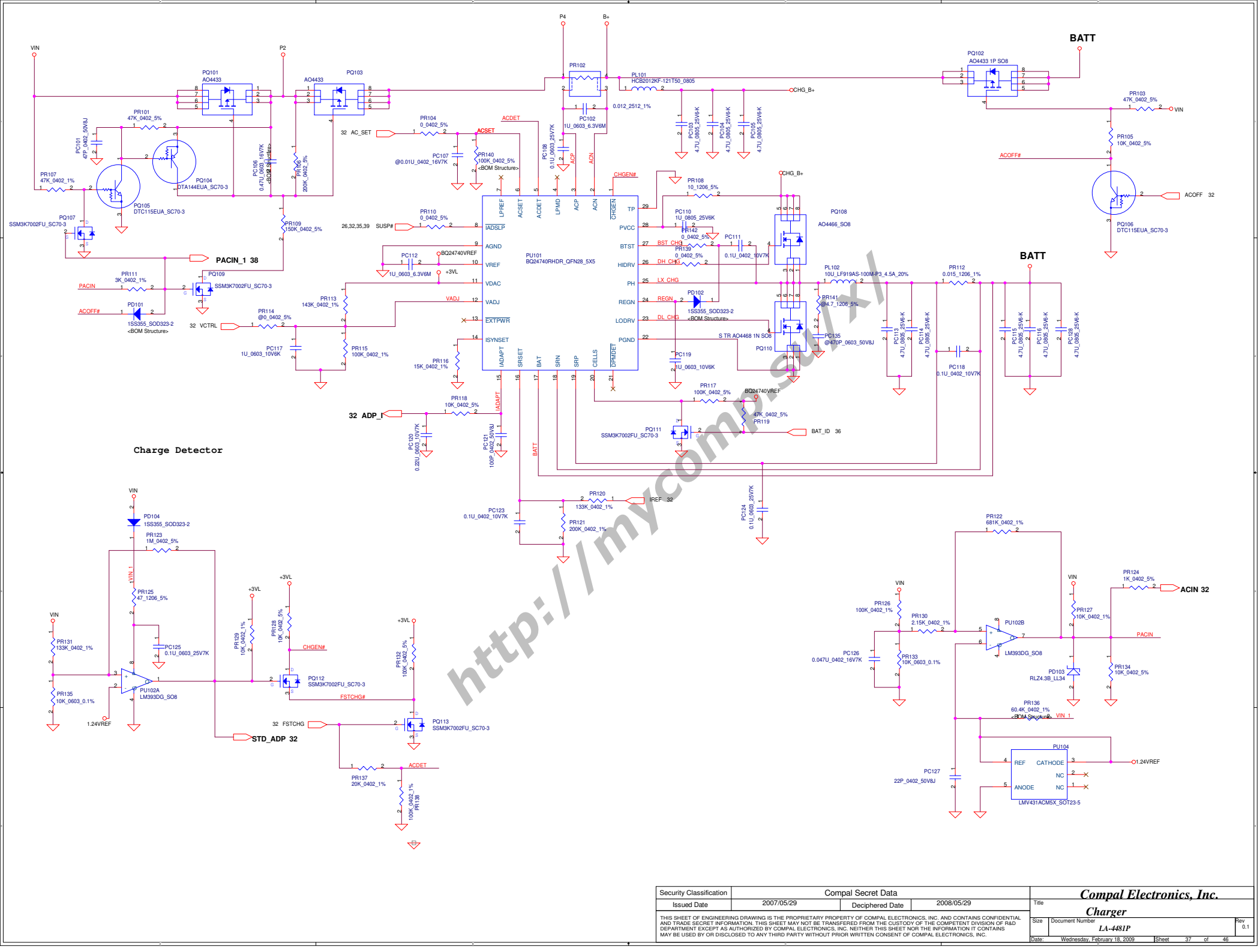
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **DC Connector/CPU_OTP**

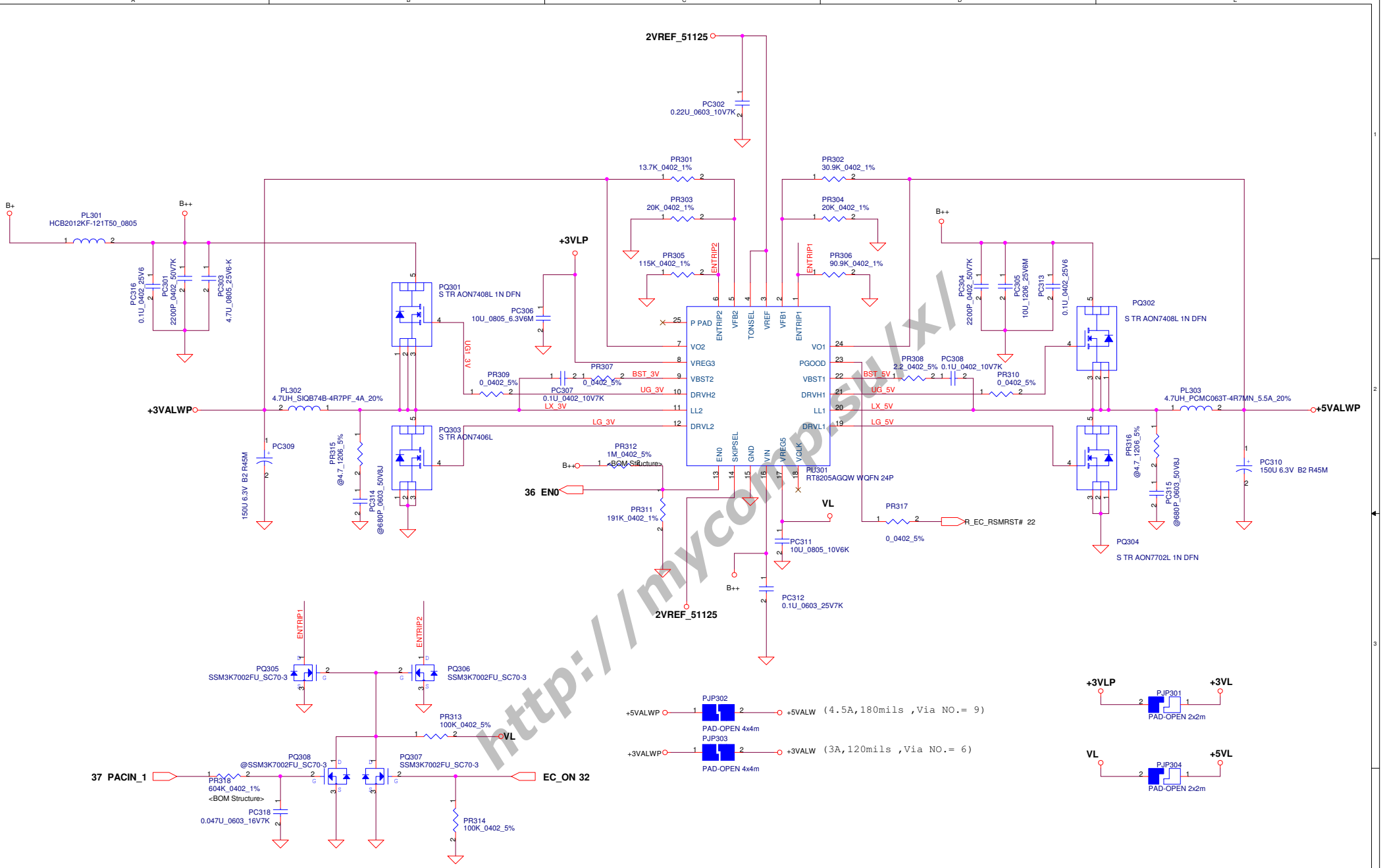
Size	Document Number	Rev
	Montevina Consumer Discrete	0.1

Date: Wednesday, February 18, 2009 | Sheet 36 of 46



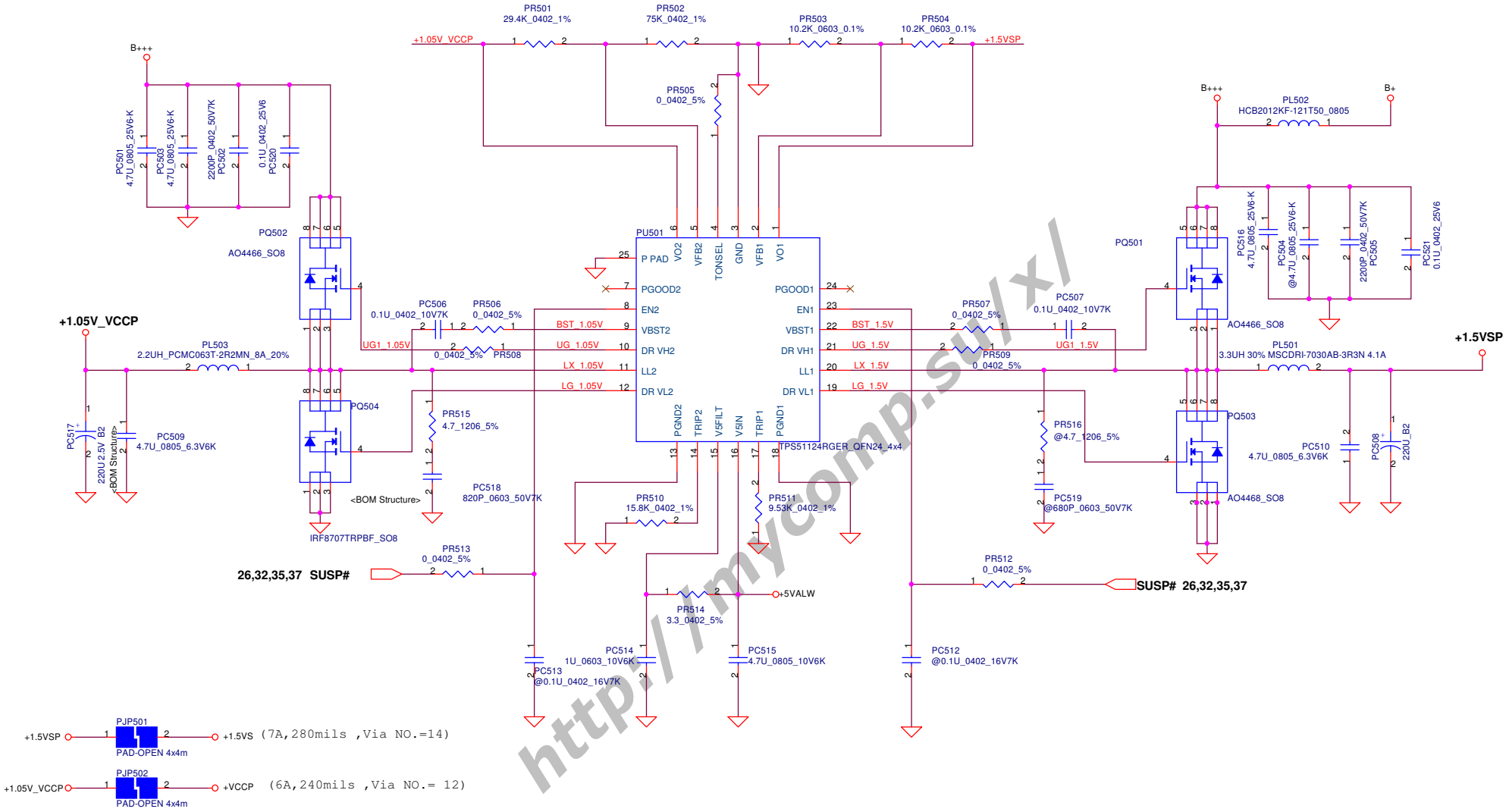
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.			
Title: Charger			
Size	Document Number: LA-4481P		Rev: 0.1
Date: Wednesday, February 18, 2009	Sheet 37 of 46		



Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.			
Title	3.3VALWP/5VALWP		
Size: Custom	Document Number: LA-4481P		Rev: 0.1
Date: Wednesday, February 18, 2009	Sheet 38 of 46		



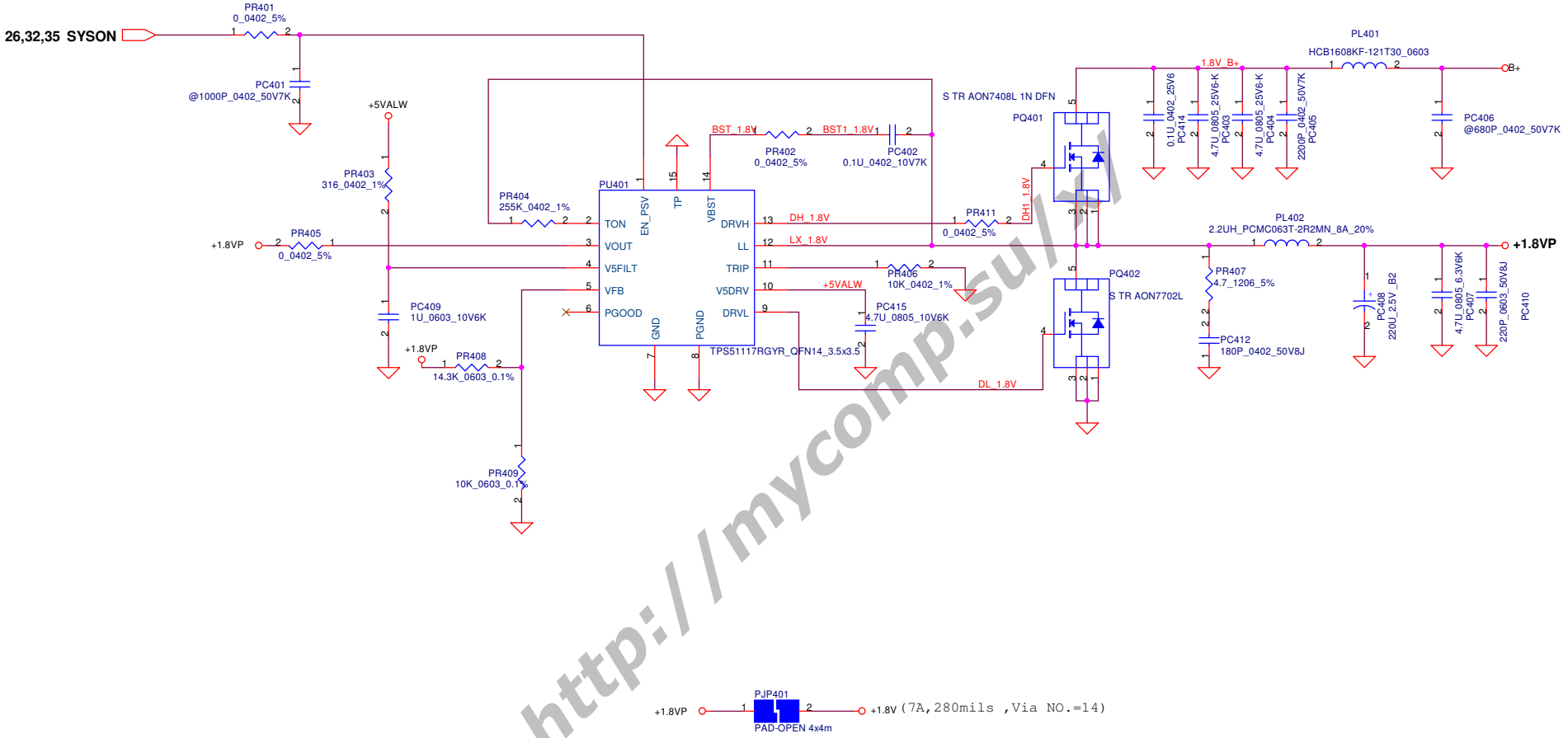
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **1.5VP/1.05V_VCCP**

Size	Document Number	Rev
	Montevina Consumer Discrete	0.1

Date: Wednesday, February 18, 2009 | Sheet 39 of 46



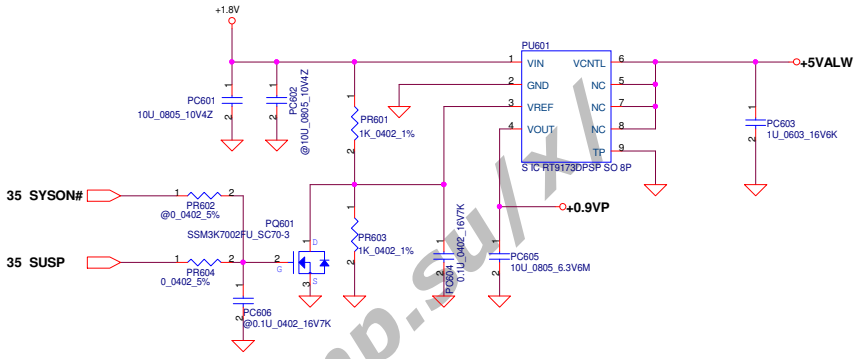
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **+1.8VP**

Size	Document Number	Rev
	Montevina Consumer Discrete	0.1

Date: Wednesday, February 18, 2009 | Sheet 40 of 46



(2A,80mils ,Via NO.= 4)

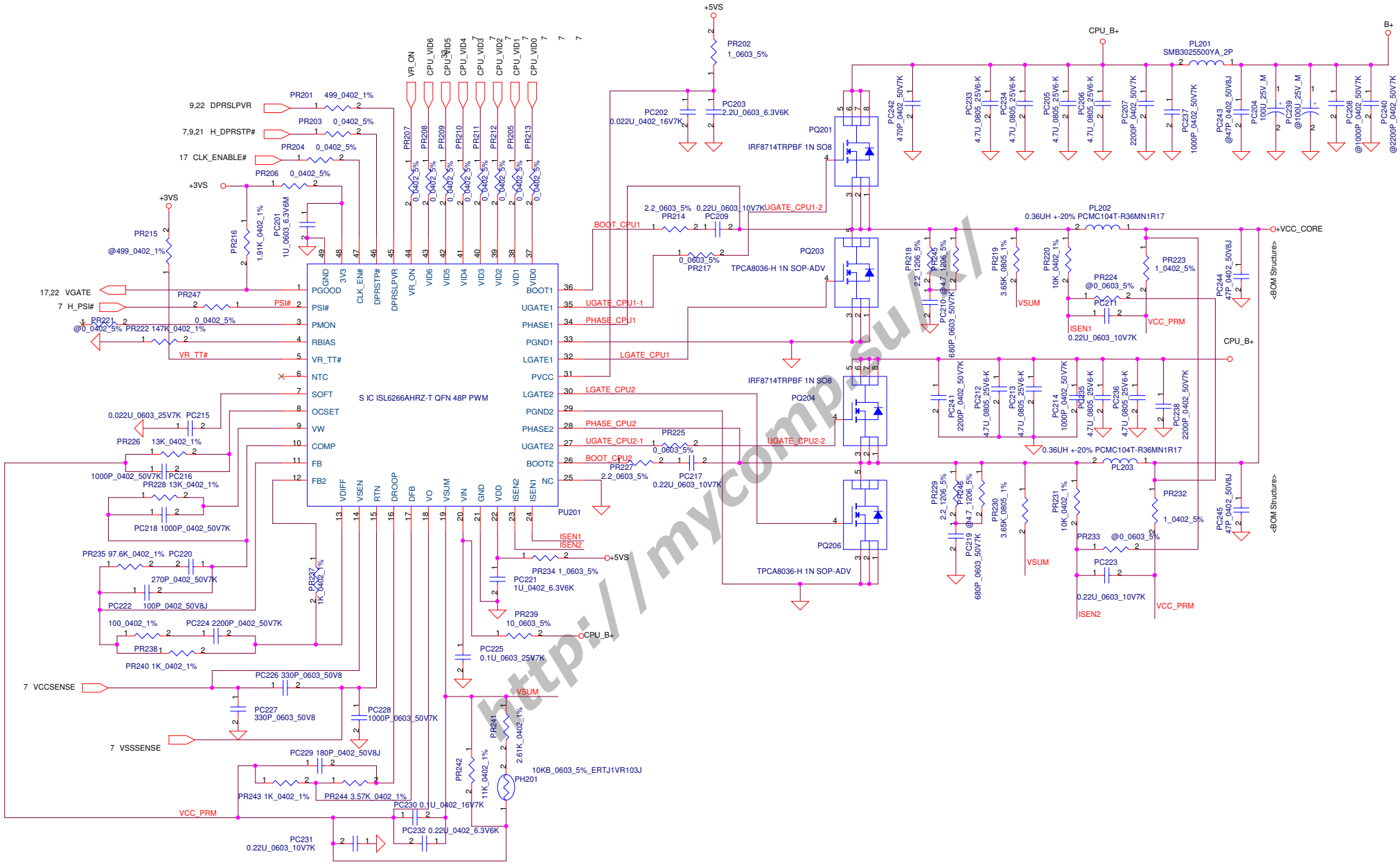
Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: **0.9VP**

Size | Document Number: **Montevina Consumer Discrete** | Rev: 0.1

Date: Wednesday, February 18, 2009 | Sheet 41 of 46



Compal Electronics, Inc.	
Title	+CPU_CORE
Size	Document Number
Date: Wednesday, February 18, 2009	Sheet 42 of 46
Rev	0.1

Version Change List (P. I. R. List) for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.		
Title: Power Changed-List History-1		
Size: Custom	Document Number: LA-4111P	Rev: 0.1
Date: Wednesday, February 18, 2009	Sheet 43 of 46	

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	CardReader clock issue	17	Using USB_0 for CLK_48M_CR	2008/10/08	SI-1
2	Debug Card issue	26	Connect PLT_RST# to JP7.A17	2008/10/08	SI-1
3	SMT issue	29	Change IR1 to SCR00000E00	2008/10/08	SI-1
4	Add Audio board	29	Add JAUDIO for audio board	2008/10/08	SI-1
5	SW2 is for DB1 debug	33	Delete SW2	2008/10/08	SI-1
6	Cap board issue	33	Change Cap board power rail to +3VL	2008/10/08	SI-1
7	Support GM47	13	Add C1503 for GM47	2008/10/08	SI-1
8	Change FAN control circuit to voltage control	6	Add U51,D63	2008/10/08	SI-1
9	Delete HDA SSC	21	Remove U8 for layout spacing	2008/10/08	SI-1
10	For PR mini card connector	26	Add R1225 -- R1236	2008/10/08	SI-1
11	PA/PR CardReader LED	27	D54 for PA, D64 for PR	2008/10/08	SI-1
12	EMI request	28	Change R1132 to bead	2008/10/08	SI-1
13	Use audio board	29	Add audio board connector, change MIC to 2pin and add SPK connector	2008/10/08	SI-1
14	Change JFPR to 6 pin connector	30	Add Q109, C1518, R1210	2008/10/08	SI-1
15	EMI request	35	Add C1512 -- C1517	2008/10/08	SI-1
16	Change JFPR to 4 pin connector	30	Delete Q109, C1518, R1210	2008/11/21	SI-R
17	Delete resistor for Debug card	26	Delete R1220-R1224	2008/11/21	SI-R
18	EMI request	35	Delete C1516,C1517 and connect to GND	2008/11/21	SI-R
19	For Intel DPST	19	Add R1237,R1238	2008/11/25	SI-R
20	EMI and WWAN request	17 21 28	Install C217, C218, C219, C435, C312, C316, C66, C67, C1478, C1479, C1480, C1481, D58, C1516, R1239, C327	2008/12/18	PV-1
21	Audio board connector	29	Change pin define	2008/12/18	PV-1
22	ST and Parade level shift	34	Add R for Parade	2008/12/18	PV-1
23	ESD request	33	Add C1518,D65,D66,D67	2008/1/19	MV-1
24	ESD/ EMI request	17 25 28 32 30	C217-C219, D5-D7, D45-D47, D20, C792-C815 no stuff	2008/2/13	MV-1
25	AUDIO issue	29	C1446, C1447 change to 0805 size	2008/2/13	MV-1
26	PC Beep issue	28	change to analog GND and add separate diode	2008/2/13	MV-1
27					
28					

Compal Electronics, Inc.

Title: PIR

Size: C | Document Number: Montevina UMA | Rev: 0.1

Date: Wednesday, February 18, 2009 | Sheet 44 of 46

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
29					
30					
31					
32					
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Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: PIR 2			
Size: C	Document Number: Montevina UMA		Rev: 0.1
Date: Wednesday, February 18, 2009	Sheet 45 of 46		

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
57					
58					
59					
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84					

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: HW PIR 3			
Size: D	Document Number: Montevina UMA		Rev: 0.1
Date: Wednesday, February 18, 2009	Sheet 46 of 46		