

11/03 Add DC-IN Cable P/N : DC301009N00

12/04 Change PJP1 to JDCIN1

11/18 Change PCB P/N from DA60000G300 to DA60000G200

02/26 Change LA-6101P P/N from DA60000G200 to DA60000G210

02/26 Add DAZ P/N and other small board P/N

02/26 Change DAZ P/N from DAZ0D9001001 to DAZ0D900101

Compal Confidential

NAU00 LA-6101P Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M

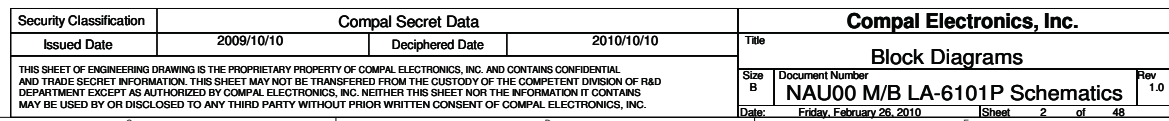
SV M/B

2010-03-09

Rev : 1.0

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Model Name : NAU00
File Name : LA-6101P



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for PCH	ON	ON	ON
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5V	5V power rail for PCH	ON	ON	ON
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
ISL90727	0101 1100b
ISL90728	0111 1100b

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

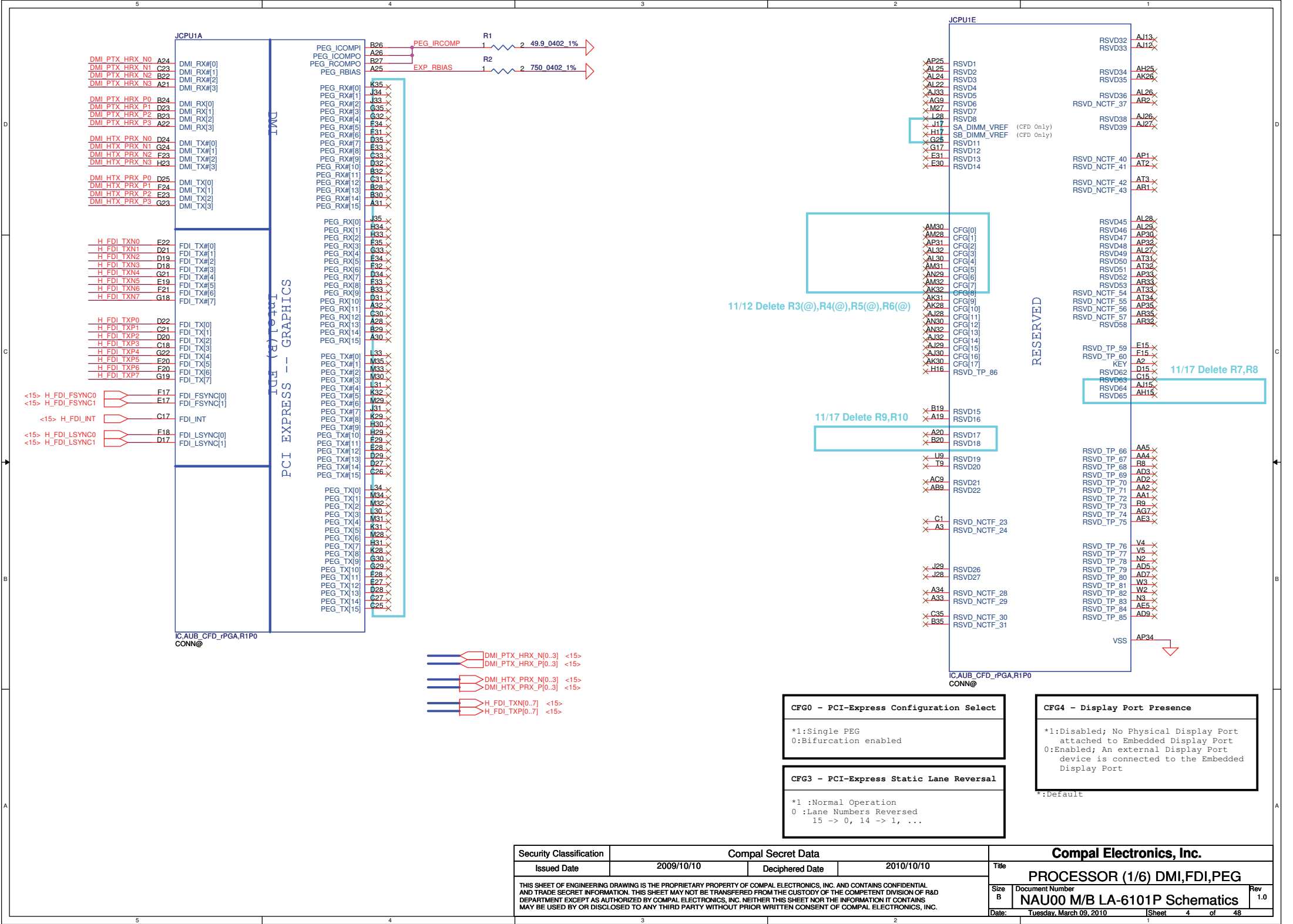
Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
* 0	0.1
1	
2	
3	
4	
5	
6	
7	

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CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bitfurcation enabled

CFG3 - PCI-Express Static Lane Reversal

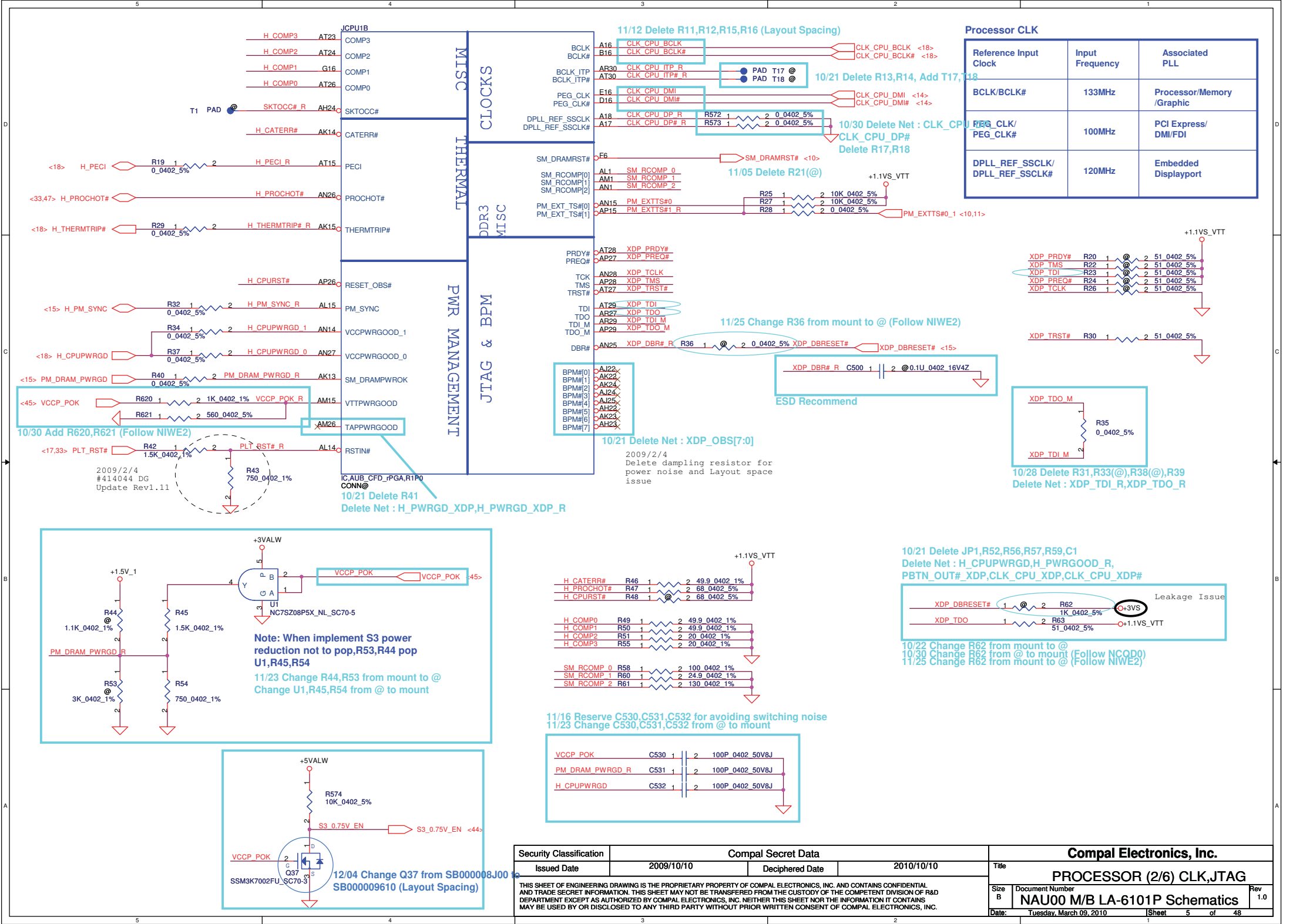
*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

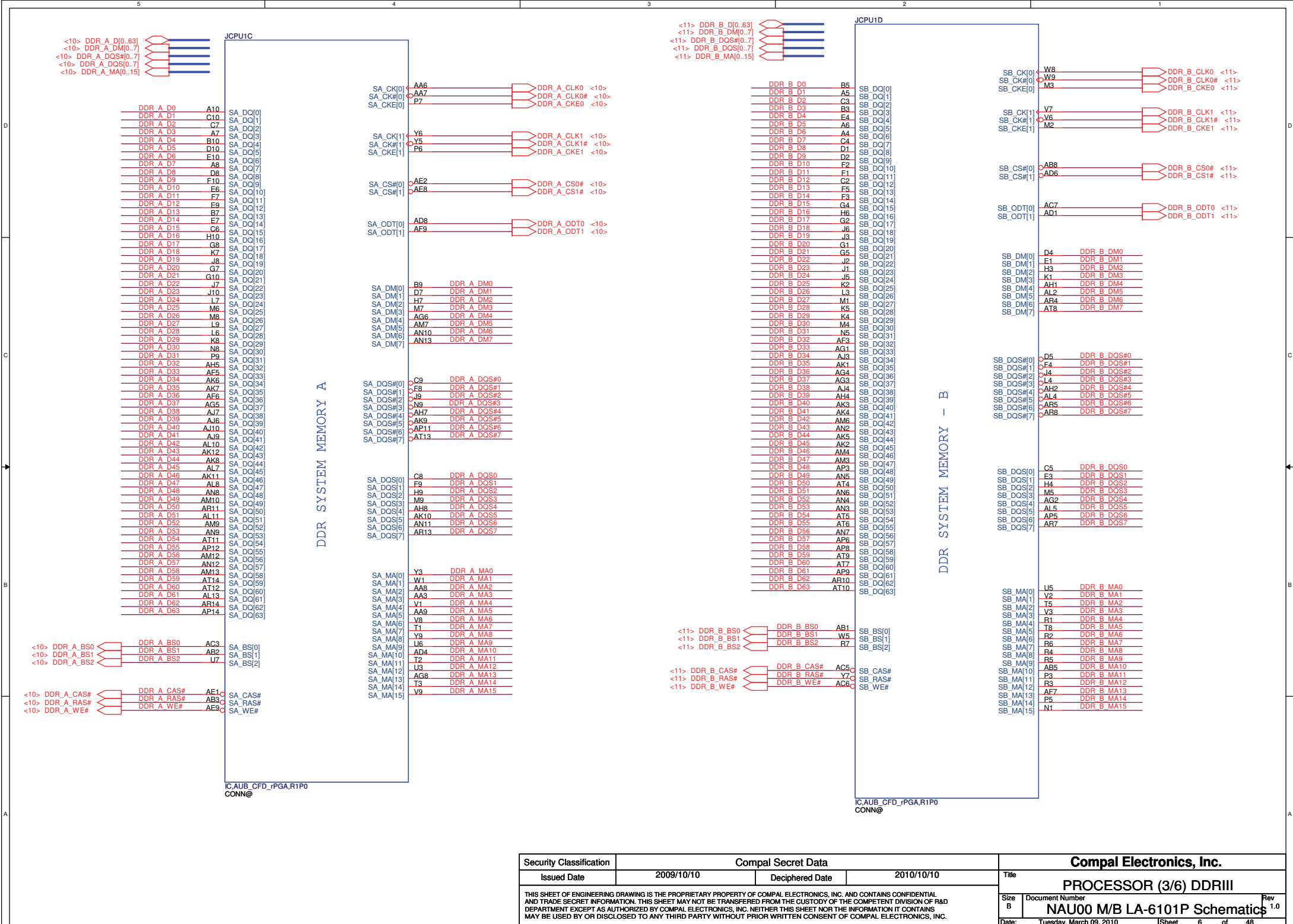
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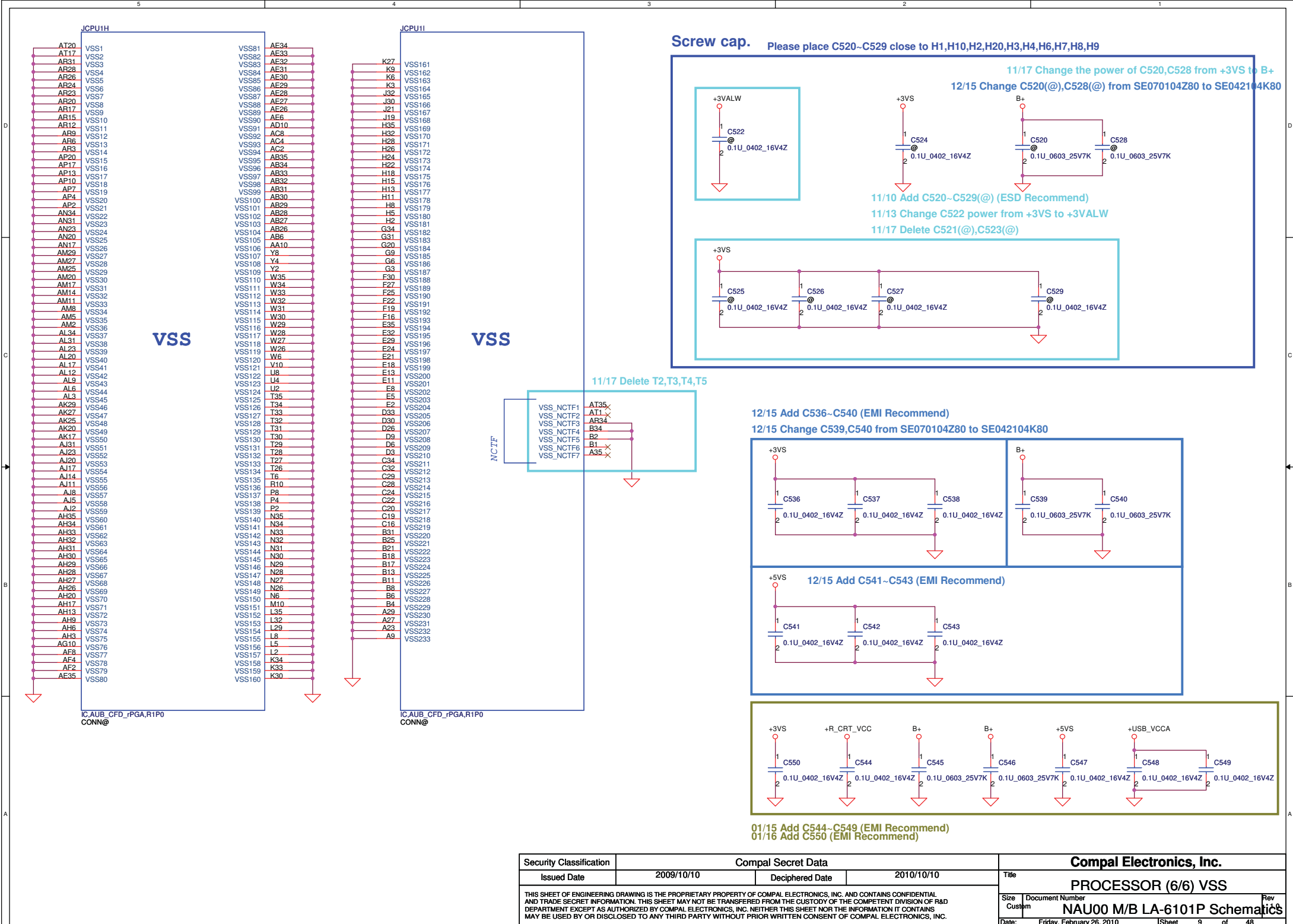
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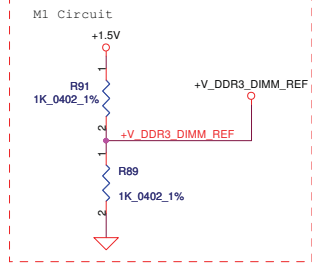
Processor CLK		
Reference Input Clock	Input Frequency	Associated PLL
BCLK/BCLK#	133MHz	Processor/Memory /Graphic
PEG_CLK/ PEG_CLK#	100MHz	PCI Express/ DMI/FDI
DPLL_REF_SSCLK/ DPLL_REF_SSCLK#	120MHz	Embedded Displayport

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								PROCESSOR (2/6) CLK,JTAG	
Size B		Document Number						Rev 1.0	
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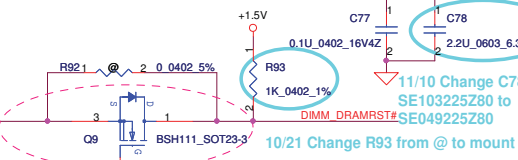
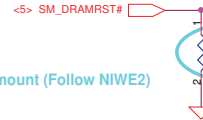
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2009/04/13
For Arrandale, it should be use M1 Circuit
For Clarksfield, it should be use M3 Circuit
DG V1.52

<6> DDR_A_DQS#[0..7]
<6> DDR_A_D[0..63]
<6> DDR_A_DM[0..7]
<6> DDR_A_DQS[0..7]
<6> DDR_A_MA[0..15]

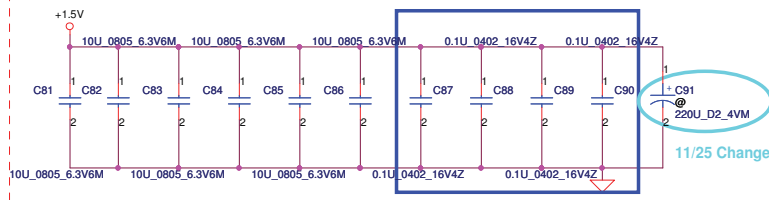
11/05 Change R94 from @ to mount (Follow NIWE2)



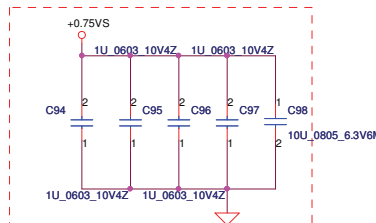
10/22 Add C502 at RST_GATE
(Intel 425302_Calpella_S3PowerReduction_WhitePaper_Rev1.0)
11/09 Change C502 from 0.047uF to 0.1uF
11/23 Change R92 from mount to @
Change Q9 from @ to mount

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA



Layout Note:
Place near JDIMM1.203 & JDIMM1.204



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DDR3 SO-DIMM A
Standard Type
H = 4.0mm

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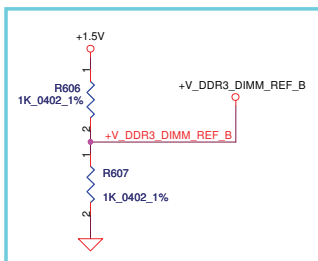
2009/04/13
For Arrandale, it should be use M1 Circuit
For Clarksfield, it should be use M3 Circuit
DG V1.52

+V_DDR3_DIMM_REF_B

M1 Circuit

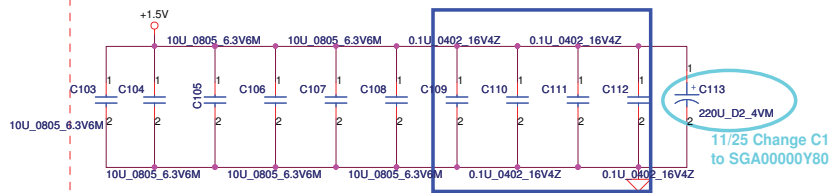
C99

11/10 Change C99 from
SE103225Z80 to
SE049225Z80



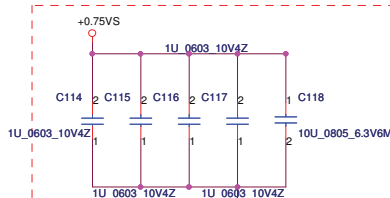
Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA



11/25 Change C113 from SGA20331E10
to SGA00000Y80

Layout Note:
Place near JDIMM2.203 & JDIMM2.204

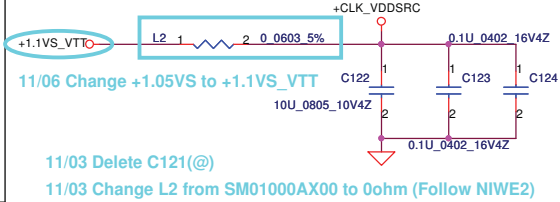


DDR3 SO-DIMM B
Standard Type

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								DDRIII-SODIMM SLOT2	
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								Rev 1.0	

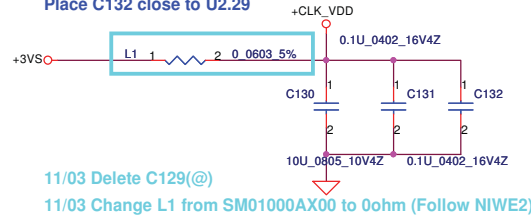
Layout note:

Place C122 close to L2
Place C123 close to U2.15
Place C124 close to U2.18



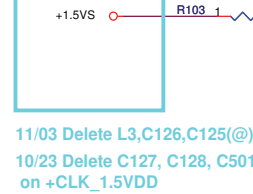
Layout note:

Place C130 close to L1
Place C131 close to U2.5
Place C132 close to U2.29



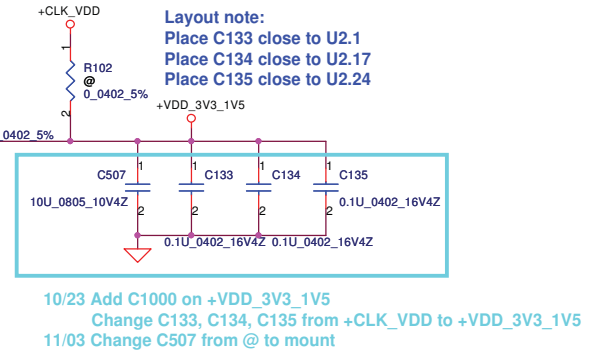
Layout note:

Place C507 close to R103



Layout note:

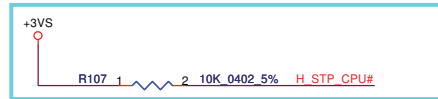
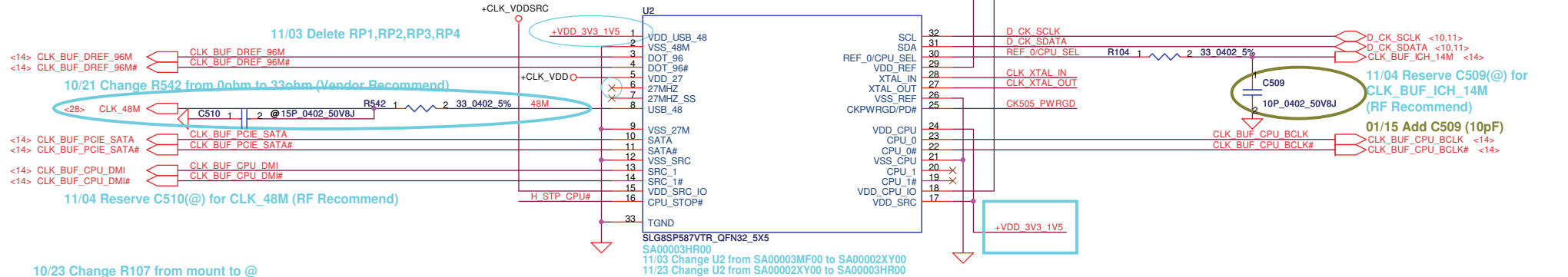
Place C133 close to U2.1
Place C134 close to U2.17
Place C135 close to U2.24



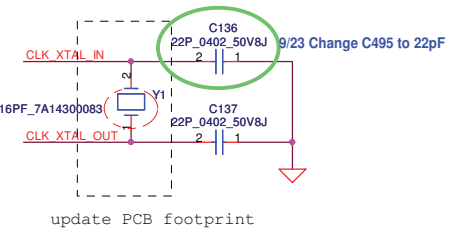
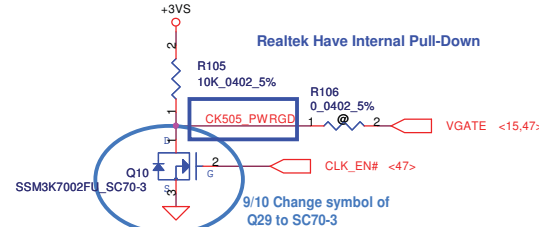
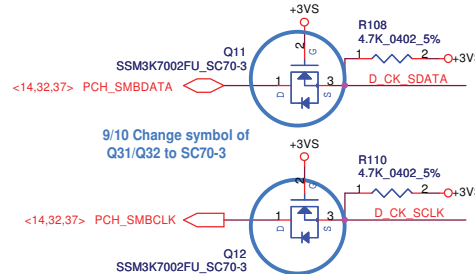
Type	R102	R103
Standard	Mount	@
Low Power	@	Mount

10/23 Change U2 Pin1,17,24
Net Name to +VDD_3V3_1V5

Clock Generator

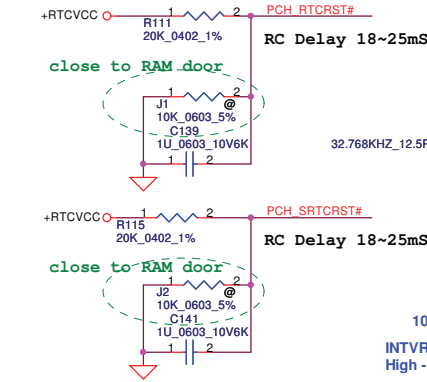


PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

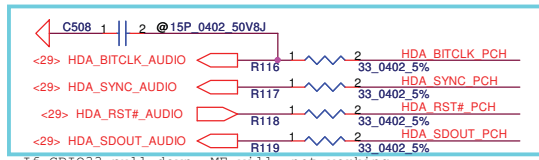


Security Classification				Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title		Clock Generator (CK505)	
2009/10/10		2010/10/10		Size		Document Number	
				Customer		NAU00 M/B LA-6101P Schematics	
				Date		Tuesday, March 09, 2010	
				Sheet		12 of 48	

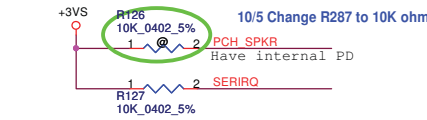
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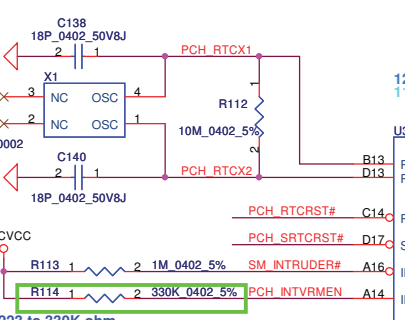
HDA for AUDIO 11/04 Reserve C508(@) for BITCLK (RF Recommend)



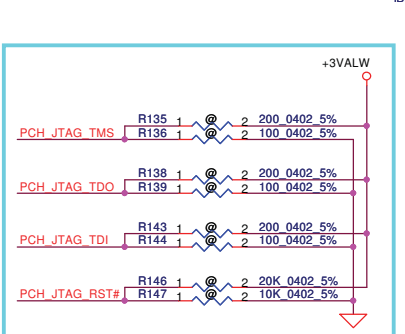
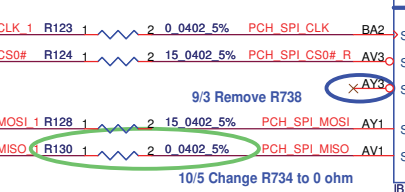
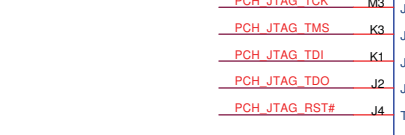
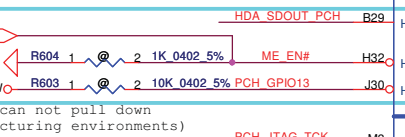
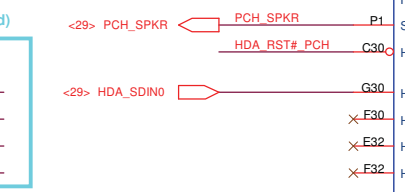
11/10 Delete Q13,R120,R121 (Follow NIWE2)



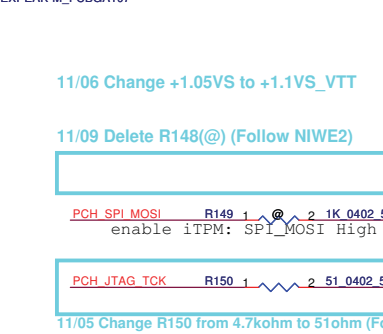
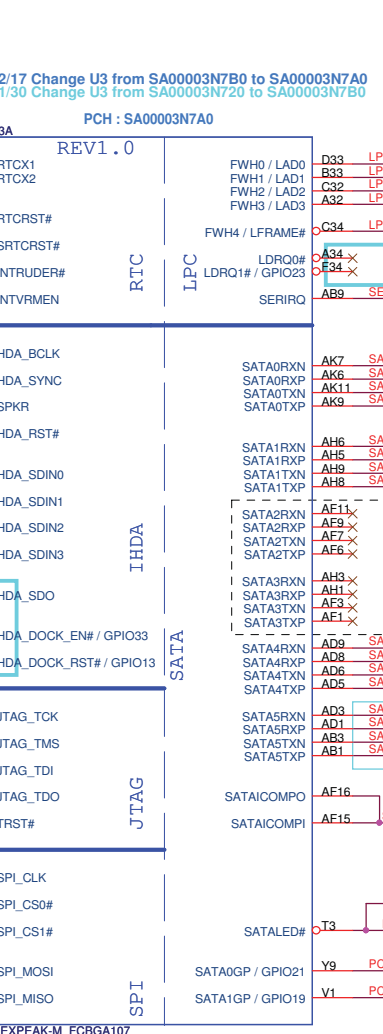
PCH Pin	RefDes	PCH JTAG Pre-Production		PCH JTAG Production
		ES1	ES2	★ MP
PCH_JTAG_TDO	R138	No Install	200ohm	No Install
	R139	No Install	100ohm	No Install
PCH_JTAG_TMS	R135	200ohm	200ohm	No Install
	R136	100ohm	100ohm	No Install
PCH_JTAG_TDI	R143	200ohm	200ohm	No Install
	R144	100ohm	100ohm	No Install
PCH_JTAG_TCK	R150	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R146	20Kohm	20Kohm	No Install
	R147	10Kohm	10Kohm	No Install



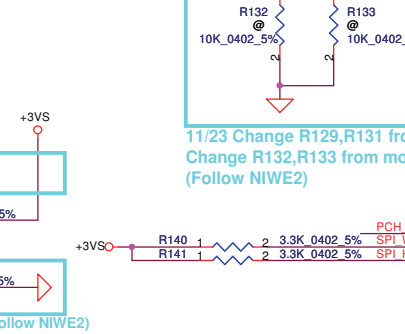
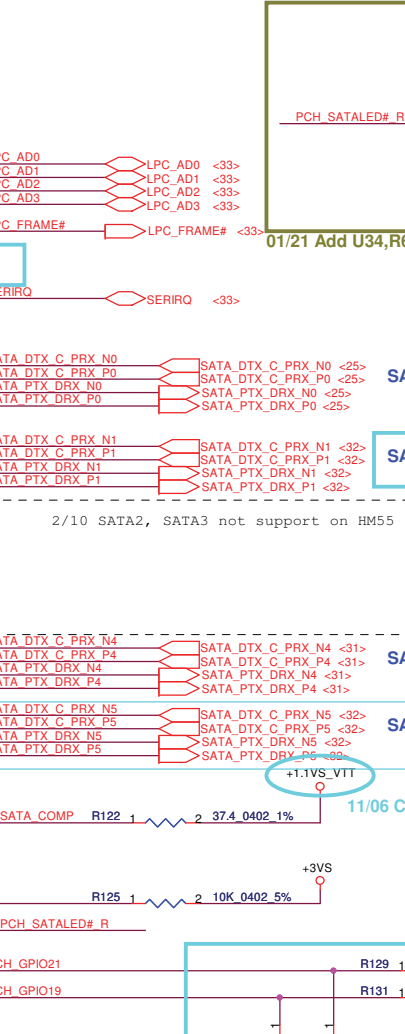
10/5 Change R223 to 330K ohm
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs



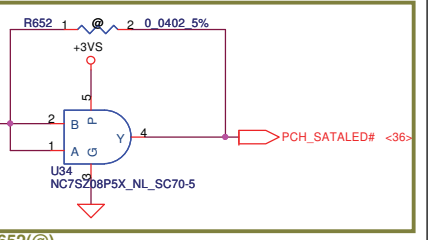
11/05 Change R135,R136,R138,R139,R143,R144,R146,R147 from mount to @ (Follow NIWE2)
11/10 Delete R134(@),R137(@),R142(@),R145(@)



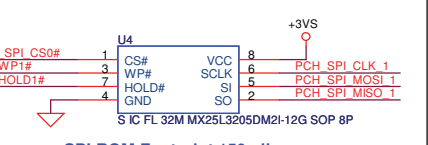
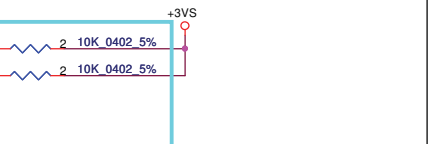
11/05 Change R150 from 4.7kohm to 51ohm (Follow NIWE2)



11/05 Change R150 from 4.7kohm to 51ohm (Follow NIWE2)



01/21 Add U34,R652(@)

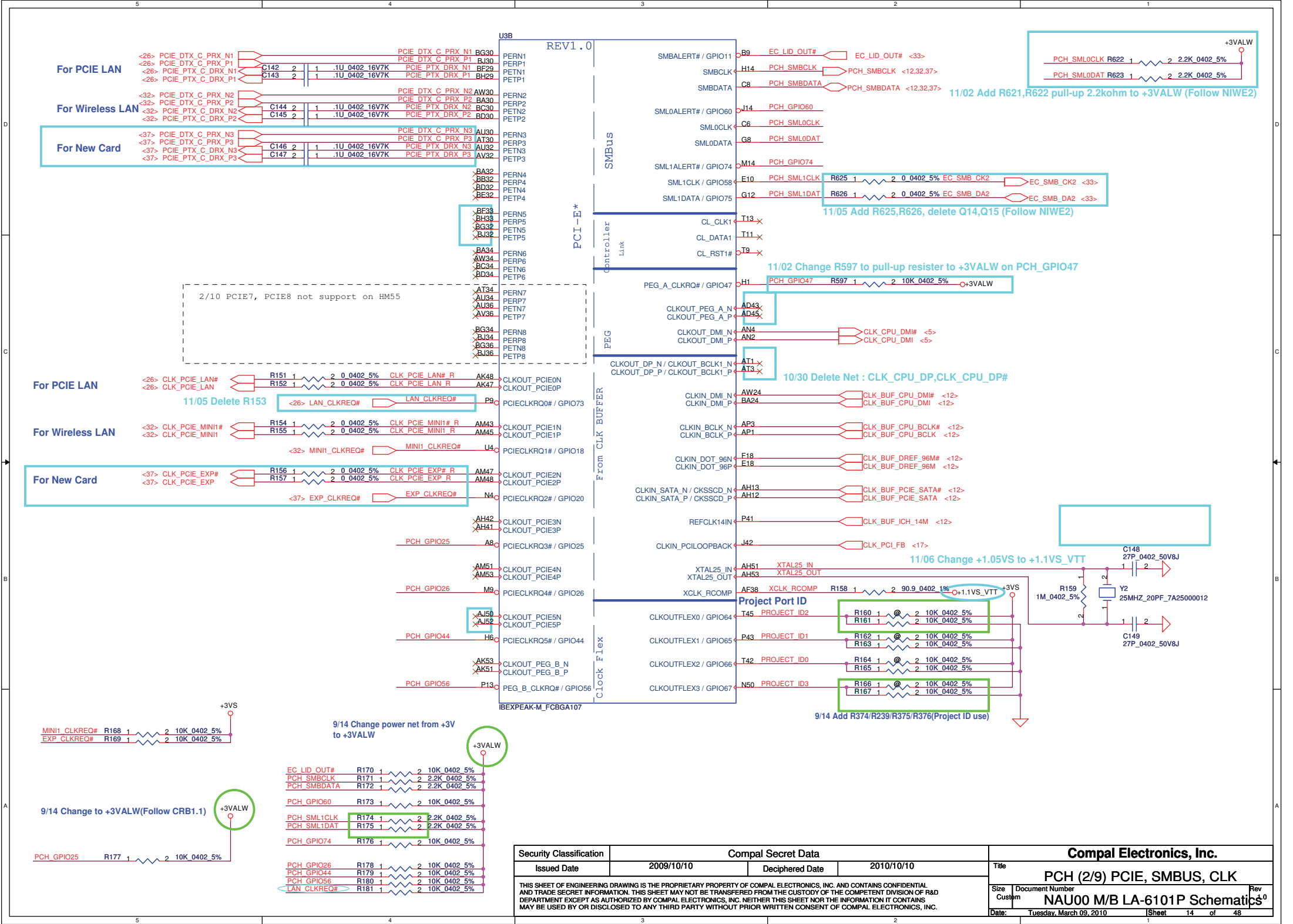


11/06 Change +1.05VS to +1.1VS_VTT

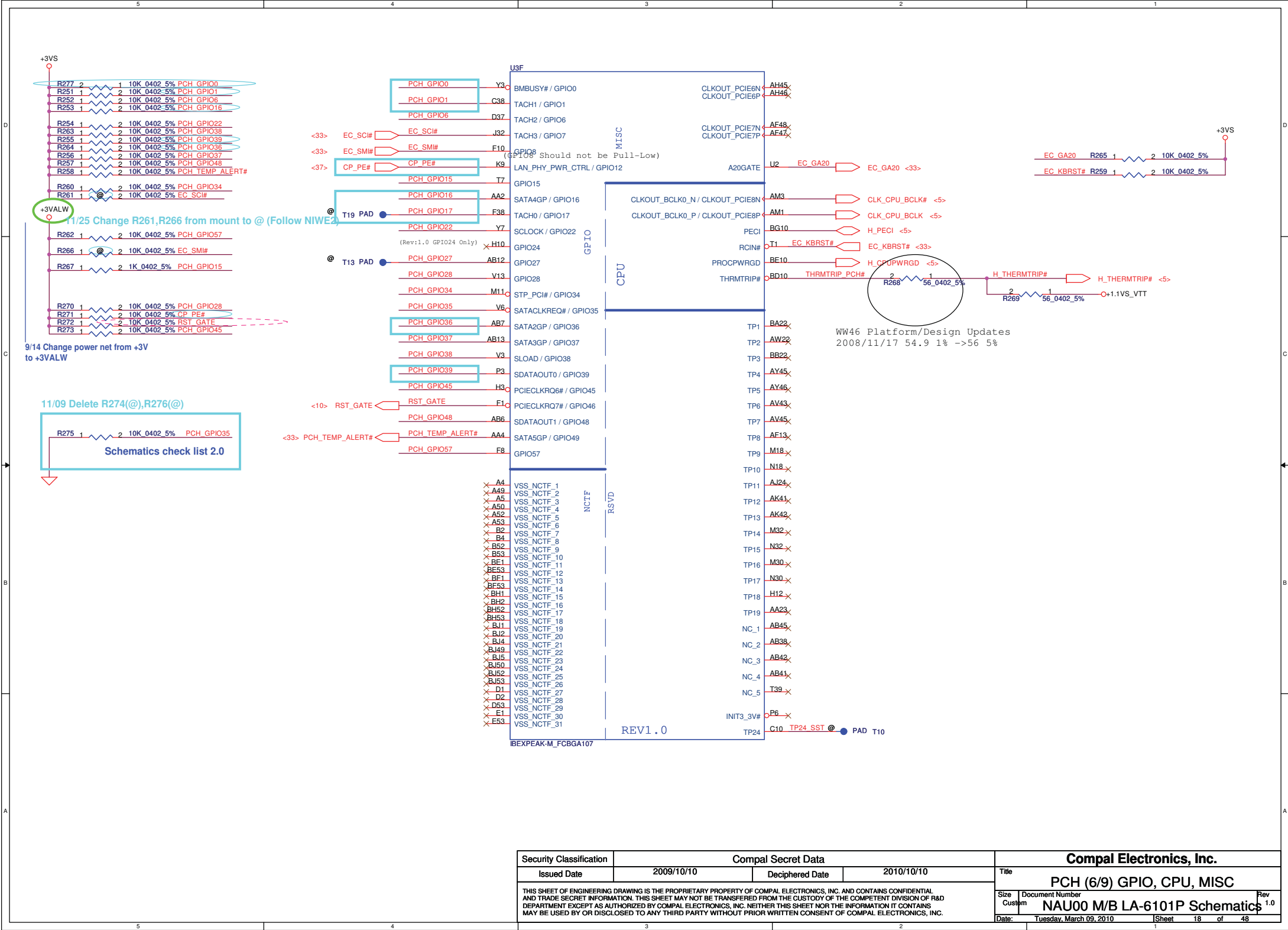
11/06 Change +1.05VS to +1.1VS_VTT

11/06 Change +1.05VS to +1.1VS_VTT

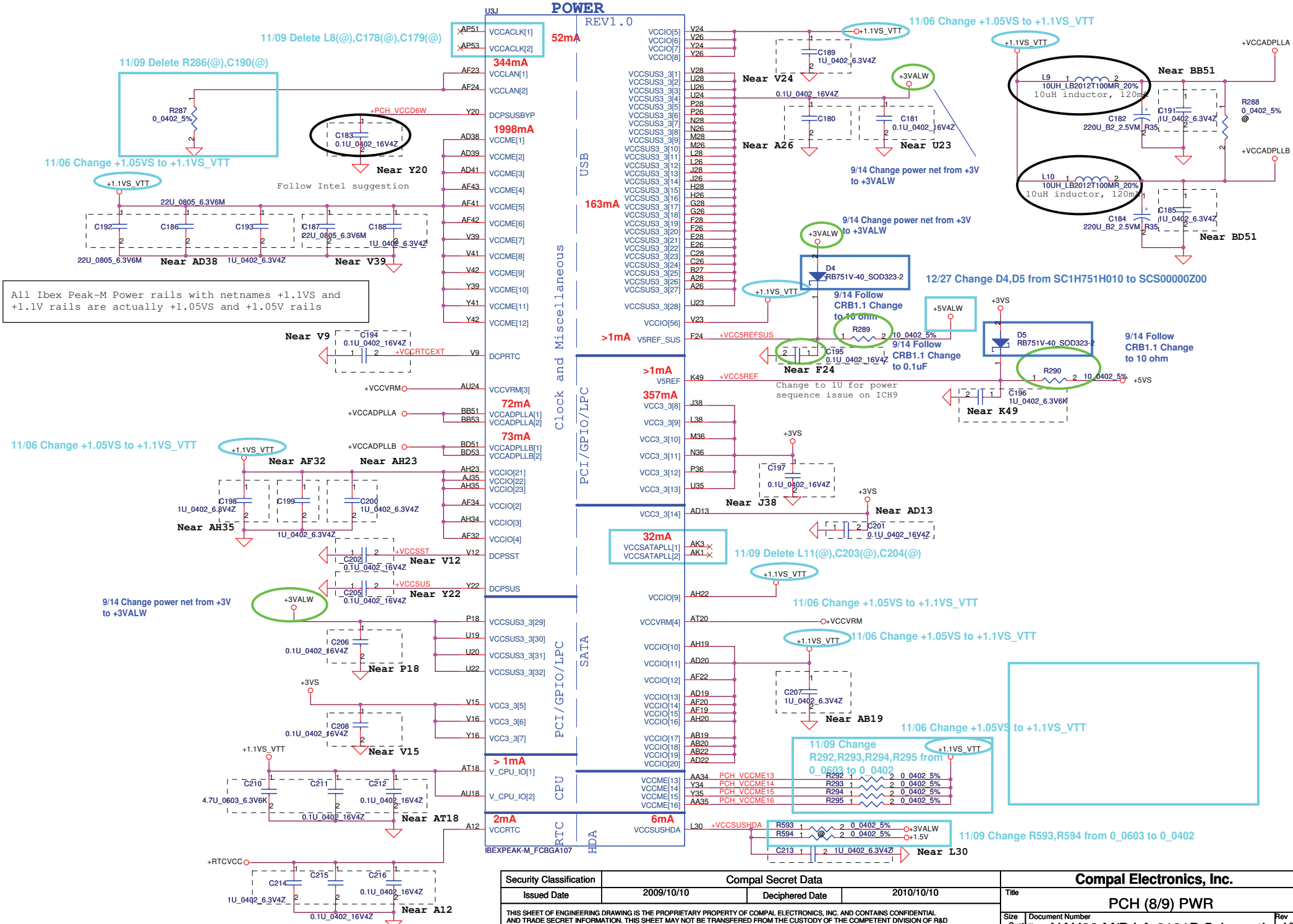
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Issued Date		2009/10/10		Deciphered Date		2010/10/10		Title				
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								Size	Document Number			Rev
									NAU00 M/B LA-6101P Schematics			0
								Date:	Tuesday, March 09, 2010		Sheet	13



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Size	Custom	Document Number	NAU00 M/B LA-6101P Schematics	Rev	0
Date	Tuesday, March 09, 2010	Sheet	14	of	48

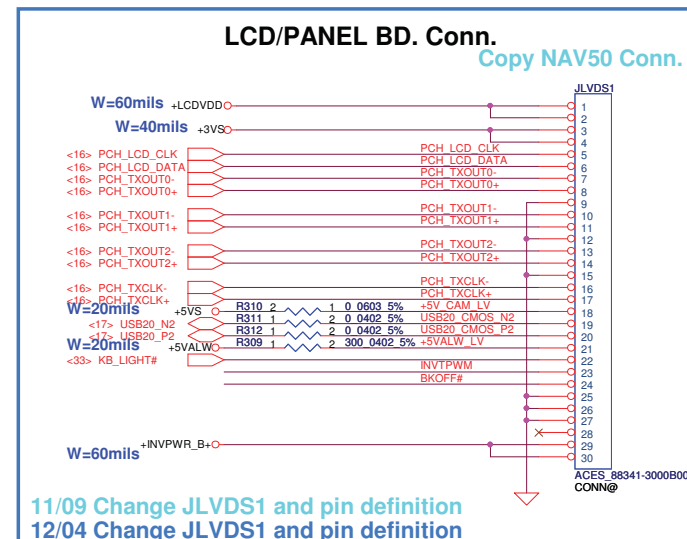
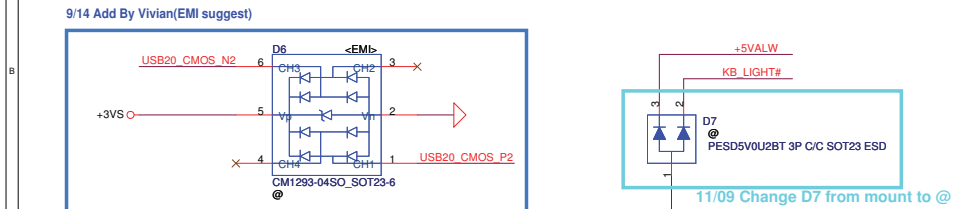
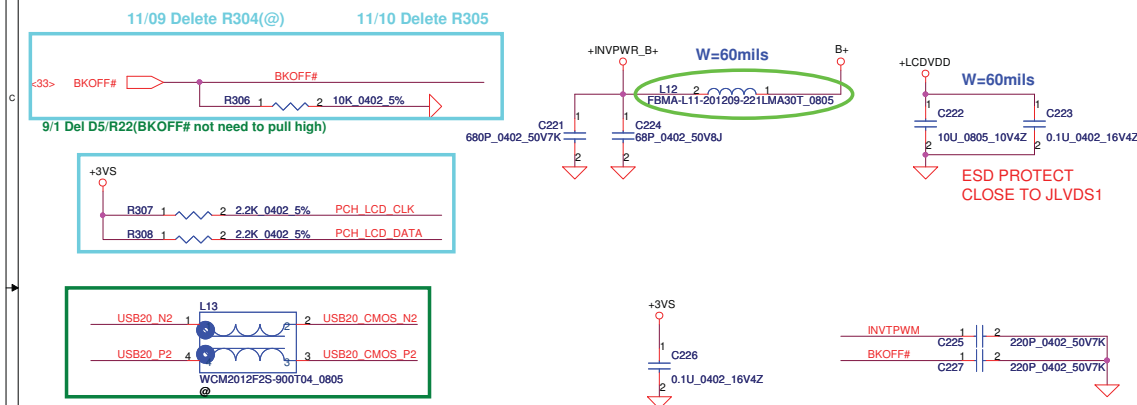
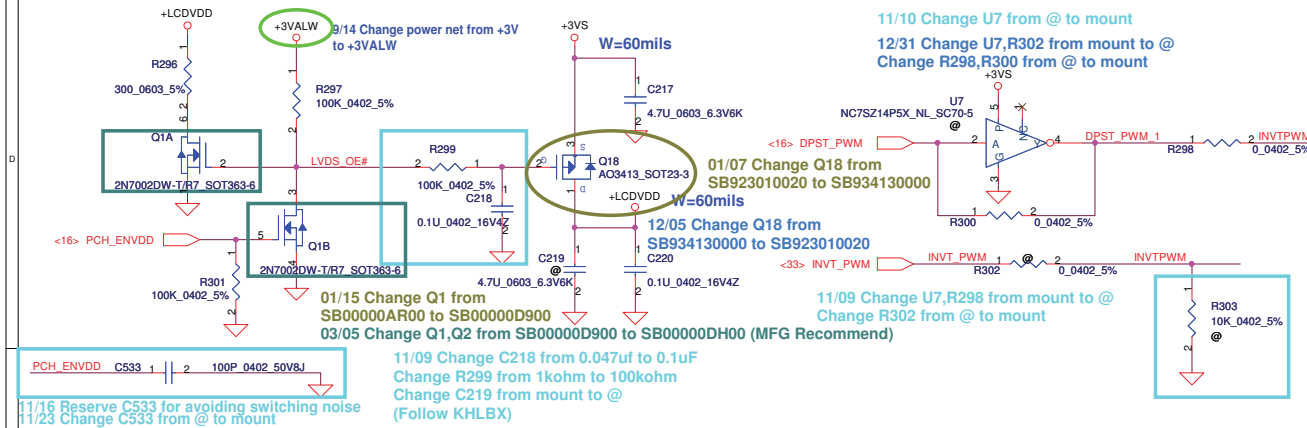


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				Custom	1.0
				NAU00 M/B LA-6101P Schematics	
Date:		Tuesday, March 09, 2010		Sheet	18 of 48



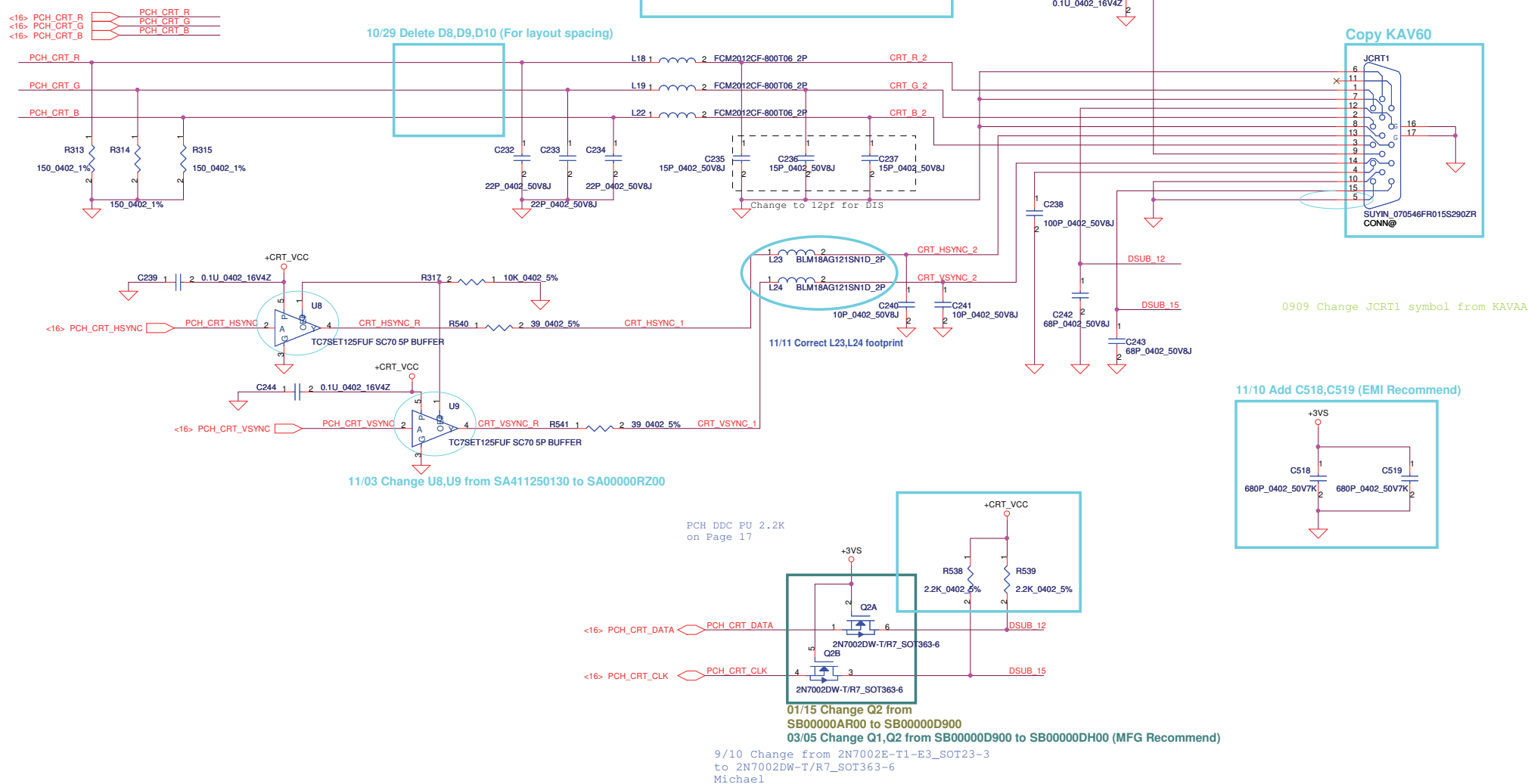
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Size	Document Number	NAU00 M/B LA-6101P Schematics		Rev	1.0
Date:	Friday, February 26, 2010	Sheet	20	of 48	

LCD POWER CIRCUIT

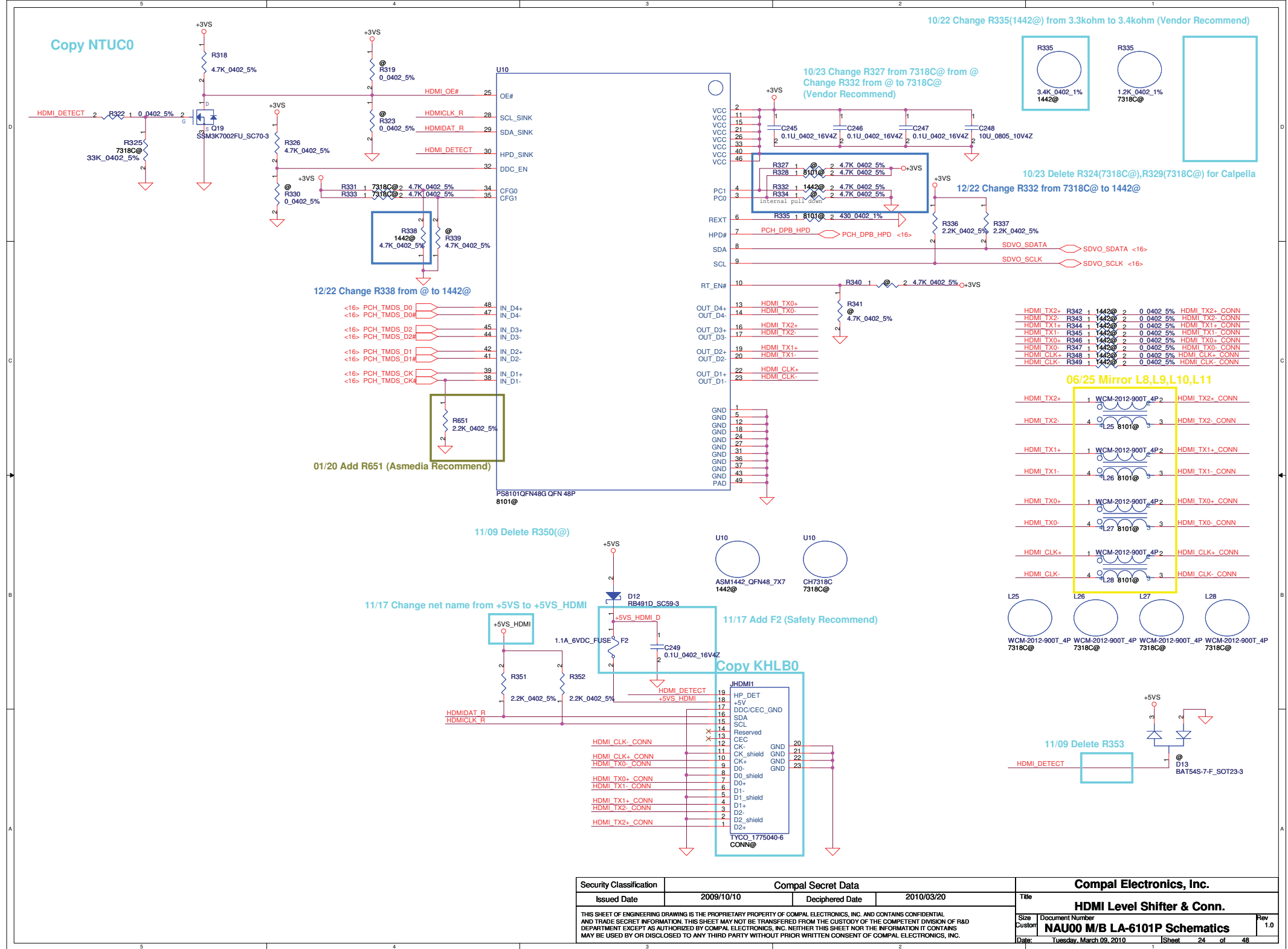


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				Custom	4.0
				Document Number NAU00 M/B LA-6101P Schematics	
Date:	Tuesday, March 09, 2010	Sheet	22	of	48

CRT Connector



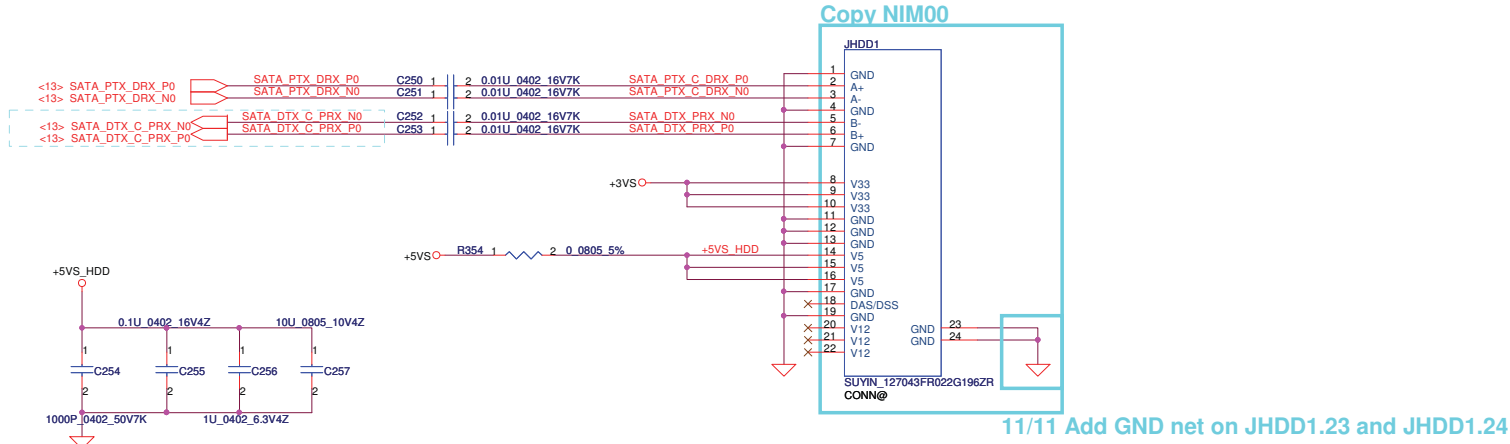
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/10/10	Deciphered Date	2010/10/10	Title	CRT Connector
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				Date: Tuesday, March 09, 2010	Sheet 23 of 48



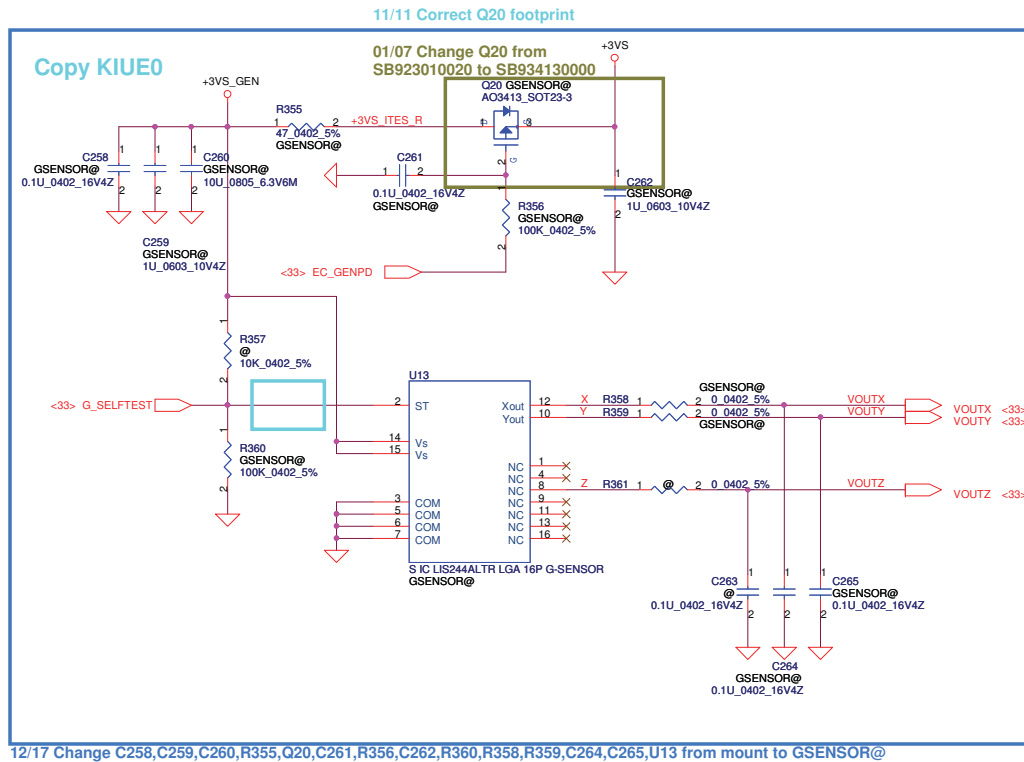
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THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
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HDD

SATA HDD Conn.

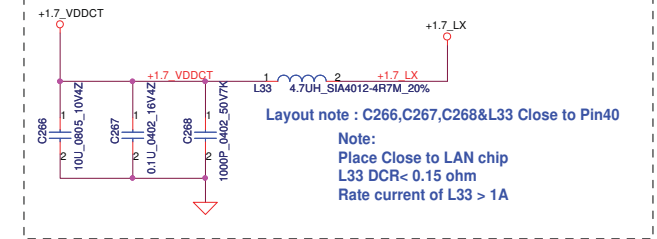
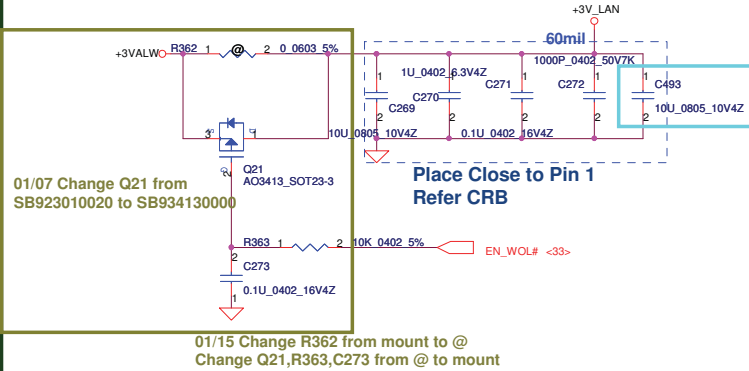


G-Sensor

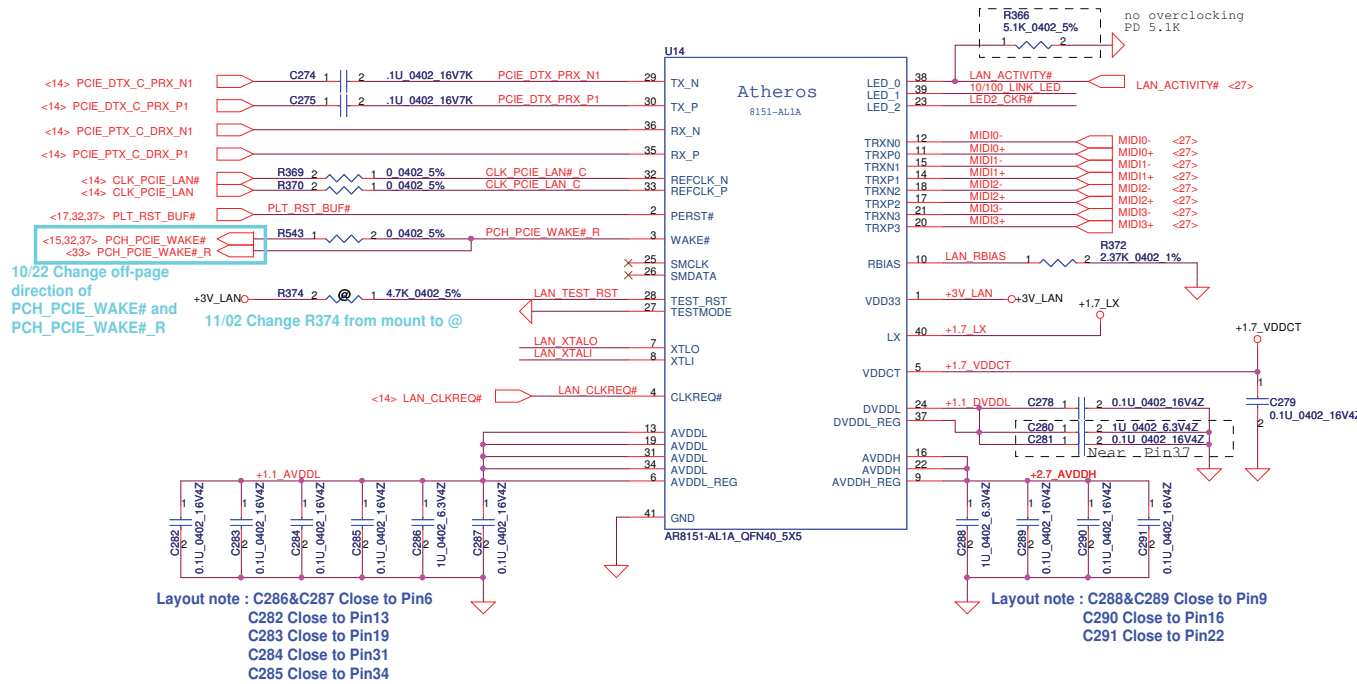
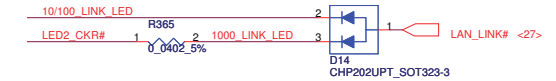


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				HDD Conn/G-Sensor	
				Date:	Rev
				Tuesday, March 09, 2010	1.0
				Sheet	of
				25	48

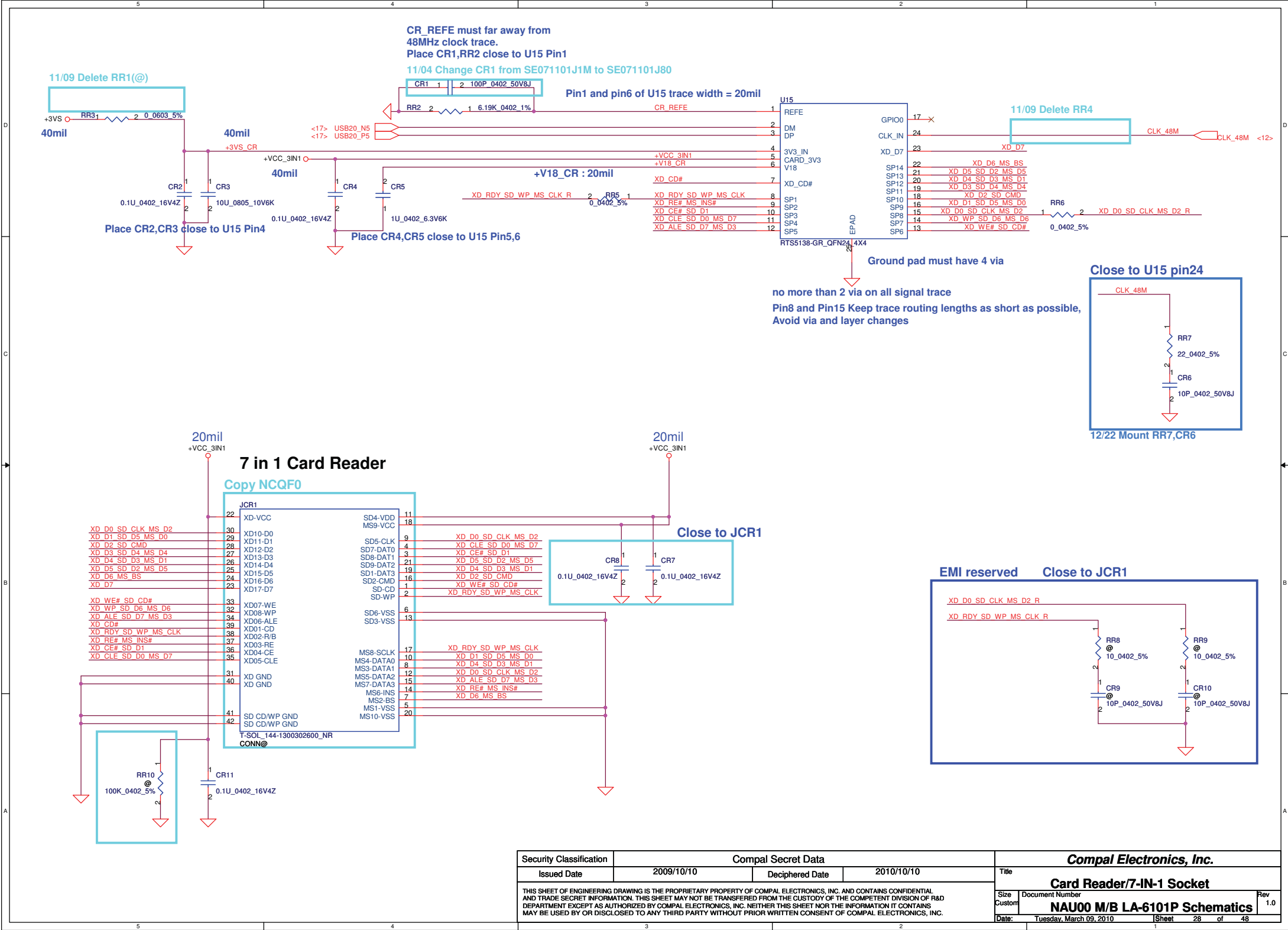
LAN Power Circuit & Refer NTUC0



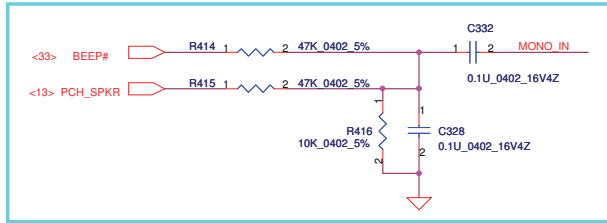
10/22 Remove R364



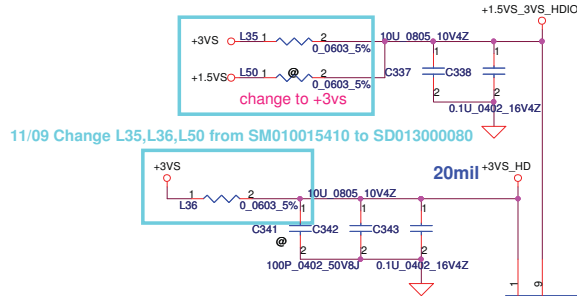
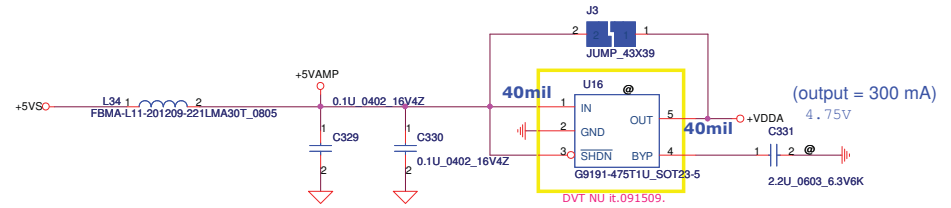
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				Date Tuesday, March 08, 2010	Rev 1.0
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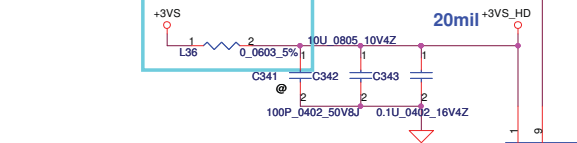
10/29 Follow NTUC0



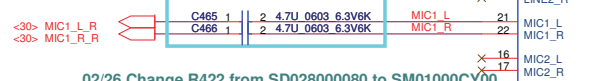
10/29 Delete C333,C334,D15,Q22,R411,R412,R413
Change R414,R415 from 560ohm to 47kohm
Change C332,C328 from 1uF to 0.1uF



11/09 Change L35,L36,L50 from SM010015410 to SD013000080

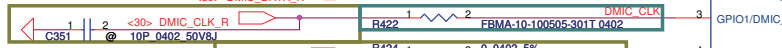


11/10 Change R465,R466 from SE053475Z80 to SE107475M80 (Realtek Recommend)



02/26 Change R422 from SD028000080 to SM01000CY00

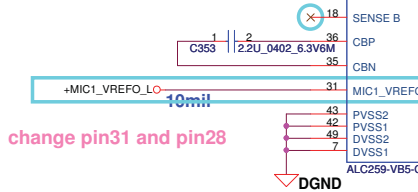
01/07 Change C351.2 from R422.2 to R422.1



01/07 Add R648(@) to +HD_AVDD (Realtek Recommend)

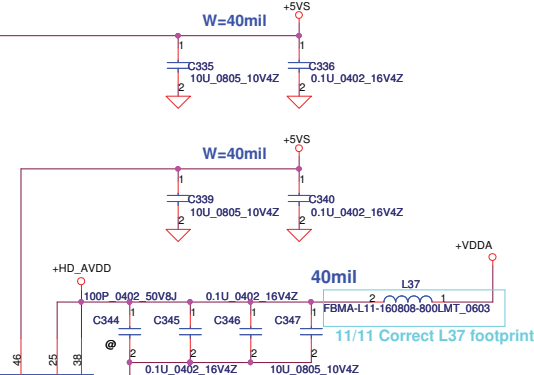


10/30 Change C352 GND from AGND to GND

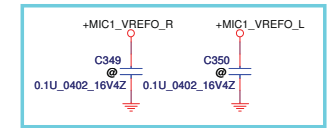
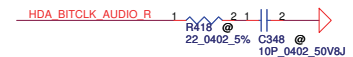


change pin31 and pin28

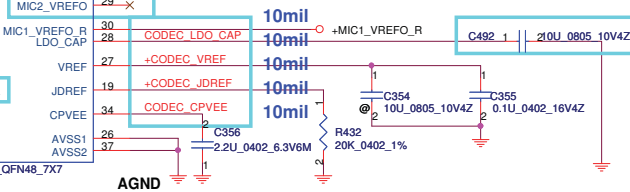
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 32, 33)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 48)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 20)
	5.1K	PORT-H (PIN 47)



11/11 Correct L37 footprint



11/05 Add net name : CODEC_LDO_CAP,+CODEC_VREF,+CODEC_JDREF,CODEC_CPVEE



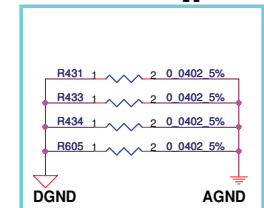
10/21 Change U17 to SA00003QR00 Symbol

03/04 Change U17 from SA00003QR00 to SA00003QR10

11/02 Change R429,R430,R431,R433,R434,R605 from 0_0603 to 0_0402 (Layout Spacing)

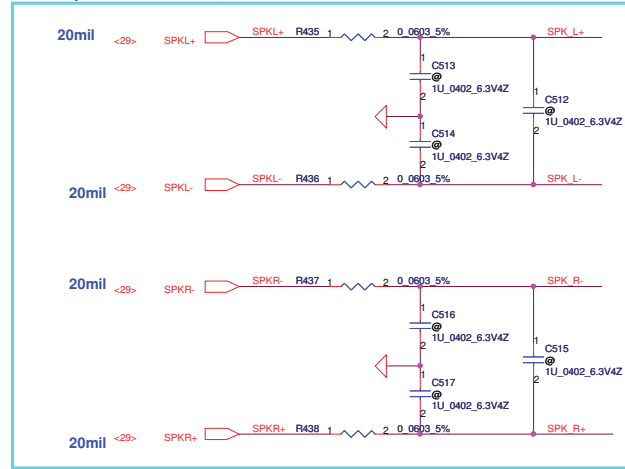
11/17 Delete R429,R430

DGND To AGND Bypass

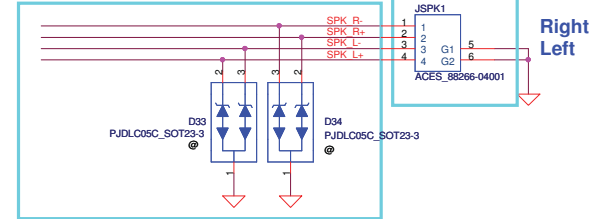


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2009/10/10				2010/10/10				Title			
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								Customer			
								NXXXX M/B LA-6101P Schematics			
								Date			
								Tuesday, March 09, 2010			
								Sheet			
								29			
								of			
								1.0			

11/11 Change R435~R438 from SM010012010 to SD013000080
 11/10 Add C512~C517(@) for EMI (Follow Realtek CRB)
 Please place R435~R438,C512~C517 close to U17



Int. Speaker Conn.

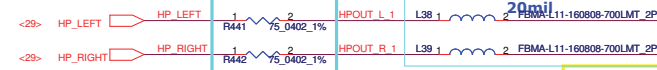


11/18 Change the pin definition of JSPK1 (Audio Recommend)
 11/18 Swap D33

Copy KTV00

Right
Left

10/29 Change R441,R442 from 56ohm to 75ohm (Follow Realtek CRB)

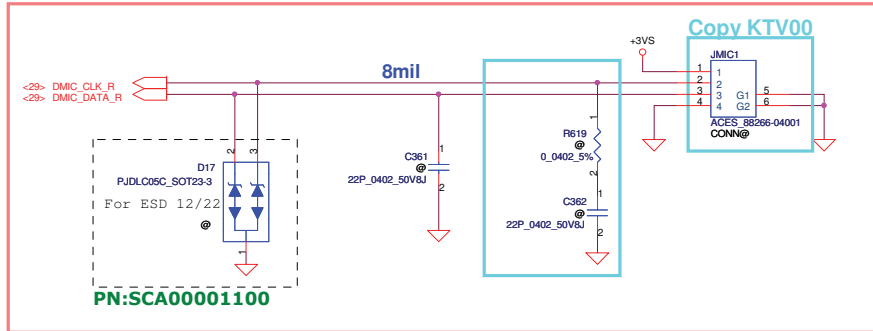


11/11 Correct L38,L39,L40,L41 footprint

Take off D28 090909.

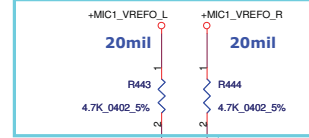
Headphone Out

Copy NIUR1



Copy KTV00

10/29 Short D18,D19 (Follow Realtek CRB)
 10/29 Change R443,R444 location



MIC JACK

Copy NIUR1

01/07 Change GND to GNDA

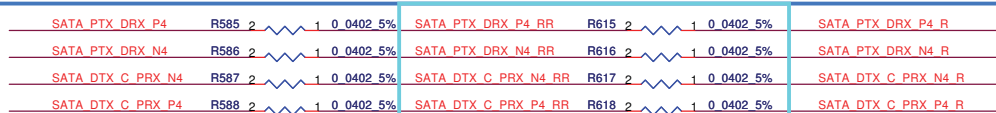
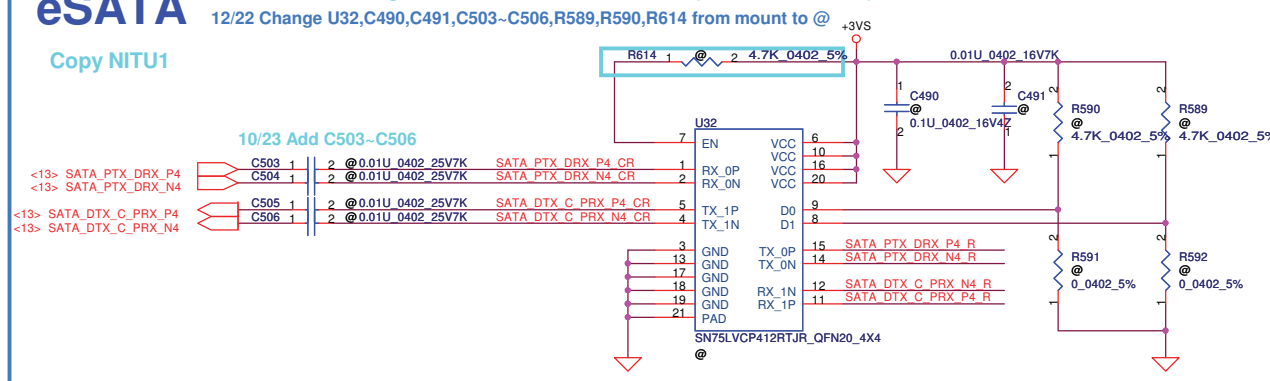
11/11 Correct D20 footprint

01/07 Change GND to GNDA

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Size	Customer	Document Number	Rev	1.0
NXXXX M/B LA-6101P Schematics		Date: Tuesday, March 08, 2010	Sheet	30 of 48

Copy NITU1

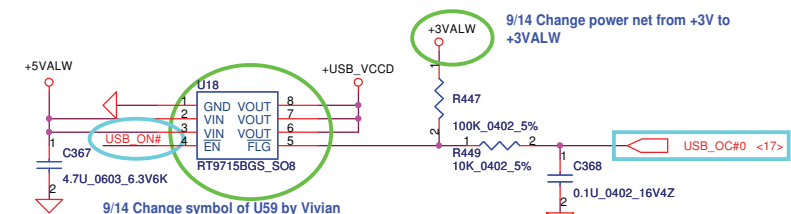
12/22 Change U32,C490,C491,C503~C506,R589,R590,R614 from mount to @



12/22 Change R585~R588,R615~R618 from @ to mount

TI:D0 D1					SN75LVCP412	
EN	BA	BB			CHANNEL 0	CHANNEL 1
0	X	X			Low-power	Low-power
1	0	0			0dB	0dB
1	1	0			2.5dB pre-emphasis	0dB
1	0	1			0dB	2.5dB pre-emphasis
1	1	1			2.5dB pre-emphasis	2.5dB pre-emphasis

(Default)



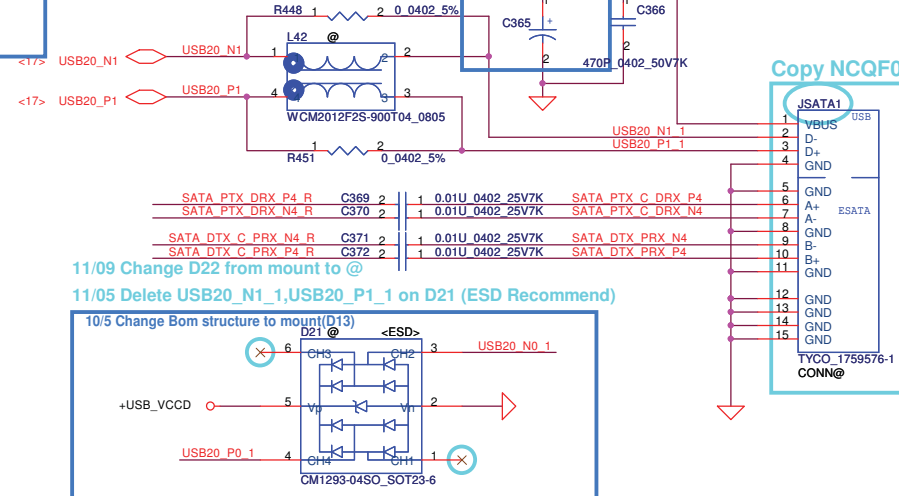
11/25 Change L42 from @ to mount

(EMI Recommend)

Change R451,R448 from @ to mount

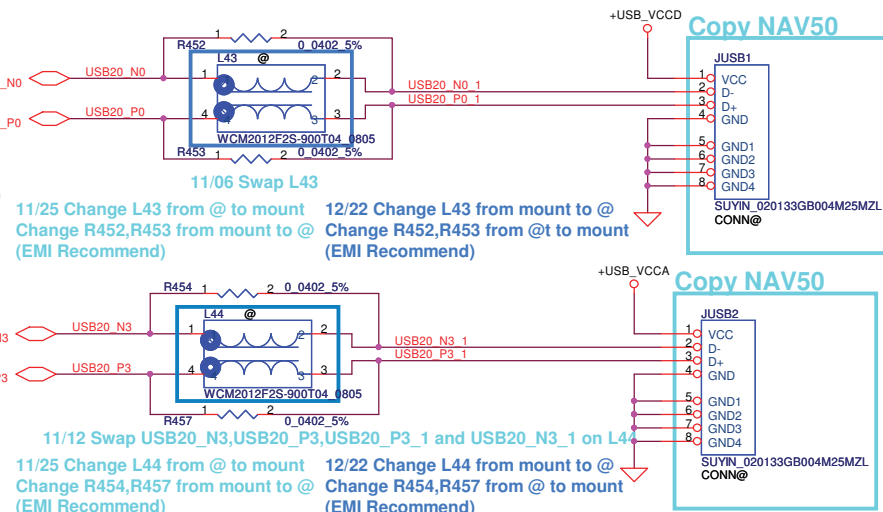
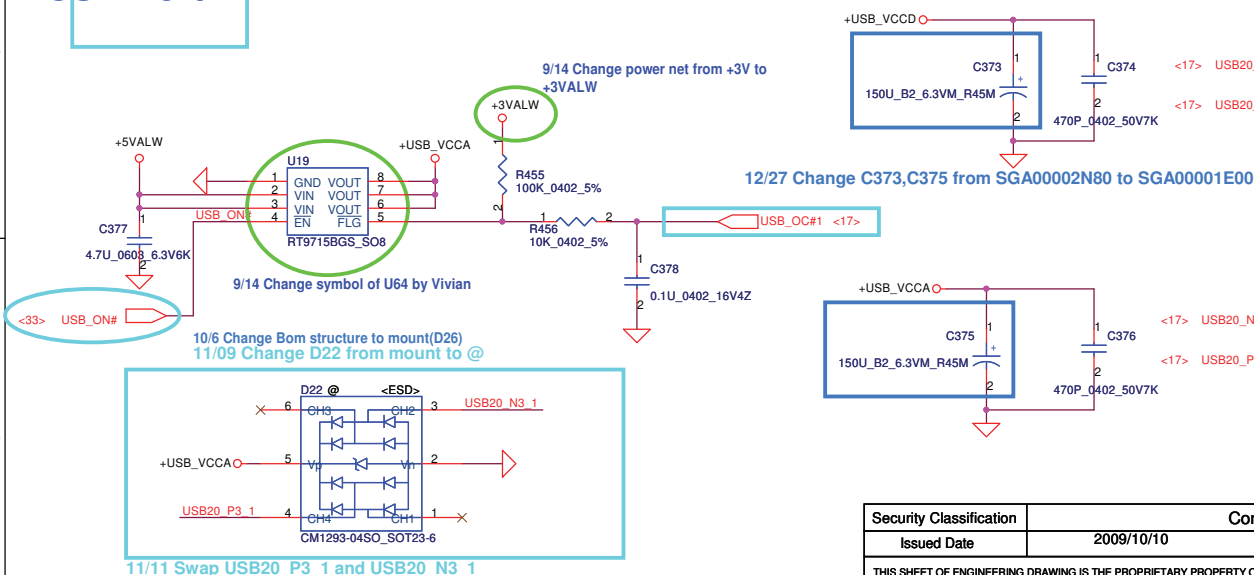
R448 1 2 0.04

12/27 Change C365 from SGA00002N80 to SGA00001E00



Copy NCQF0

USB Port



CA Copy NAV50

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				Size	Document Number	Rev
				Custm	NAU00 M/B LA-6101P Schematics	1.0
Date:	Tuesday, March 09, 2010	Sheet	31	of	48	

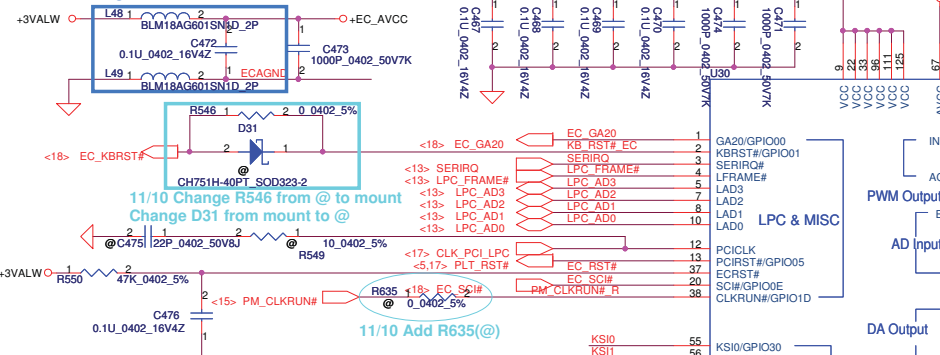
A

A

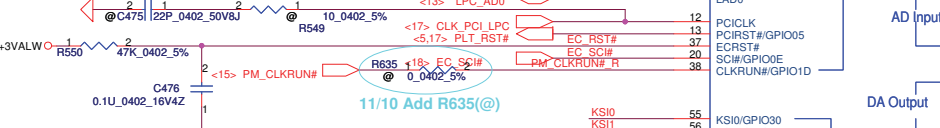


5	4	3	2	1
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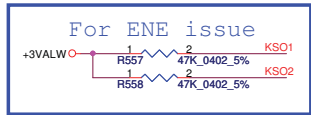
12/05 Change L48,L49 from SM010016810 to SM010005500



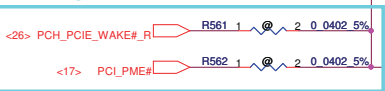
11/10 Change R546 from @ to mount Change D31 from mount to @



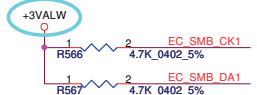
11/10 Add R635(@)



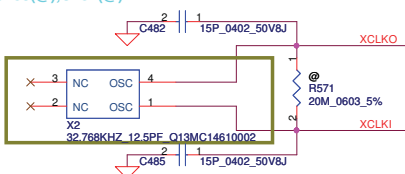
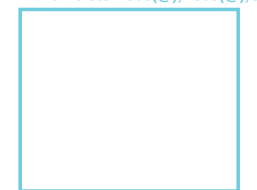
10/22 Change R561 from mount to @ Change R562 from @ to mount 11/10 Change R562 from mount to @



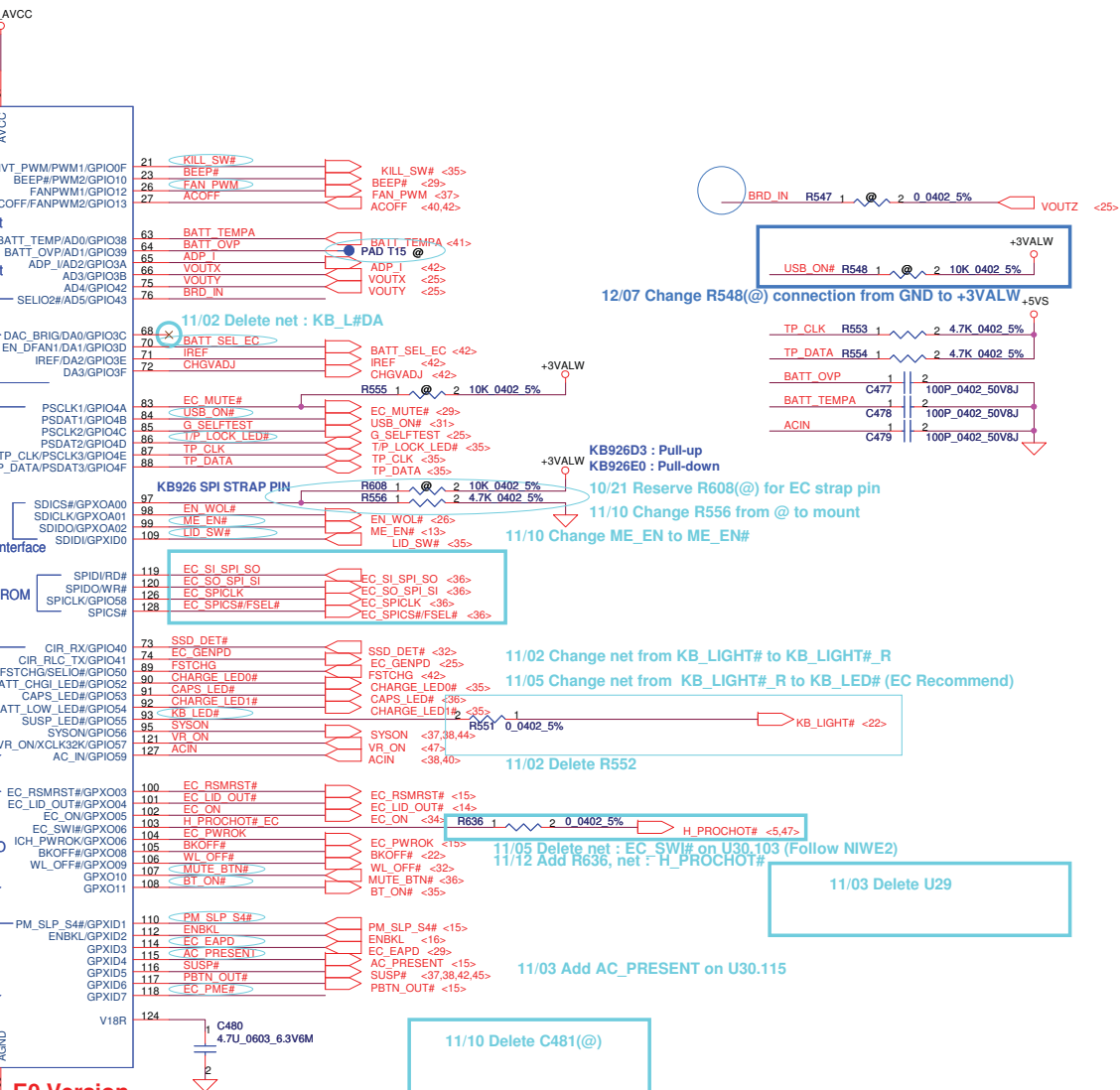
11/05 Change the power of R566,R567 from +5VALW to +3VALW (Follow NIWE2)



11/03 Change R568,R569 from 2.7kohm to 2.2kohm 11/05 Change R568,R569 from mount to @ (Follow NIWE2) 11/10 Delete R568(@),R569(@),C483(@),C484(@)



01/11 Change X2 from SJ100003M00 to SJ132P7KW10 (Cost down)



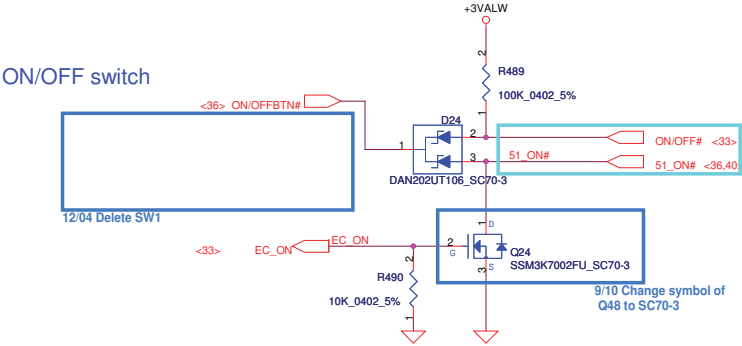
E0 Version SA00001J5A0

10/21 Change U30 from SA00001J580 to SA00001J5A0

11/02 Delete U31,Q36,R570

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Date:		Tuesday, March 09, 2010		Sheet	33 of 48

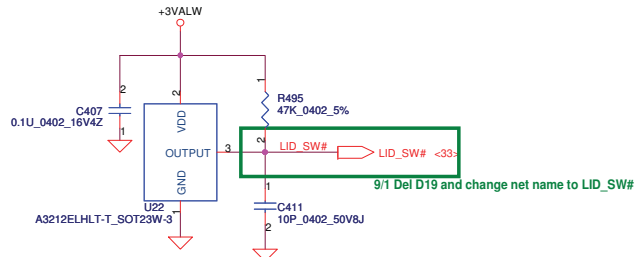
Power Button



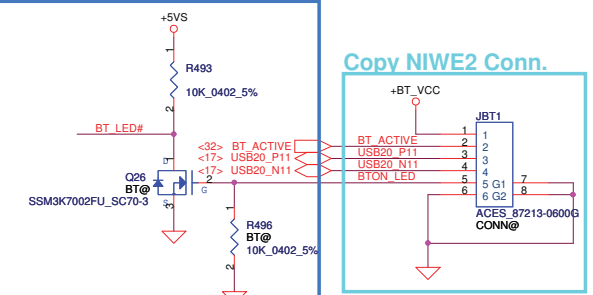
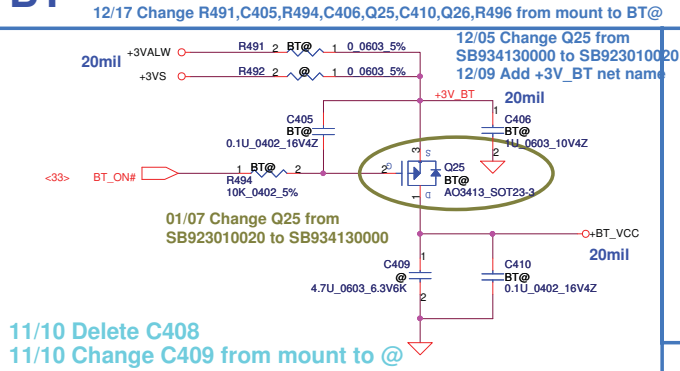
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Lid Switch

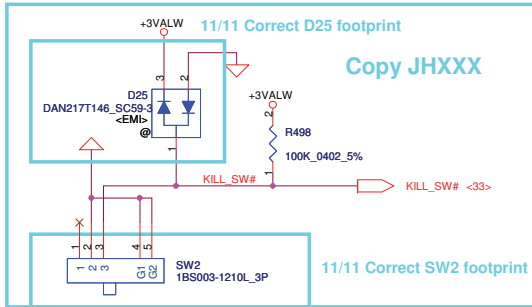
(Hall Effect Switch)



BT

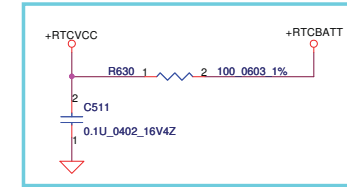


KILL Switch

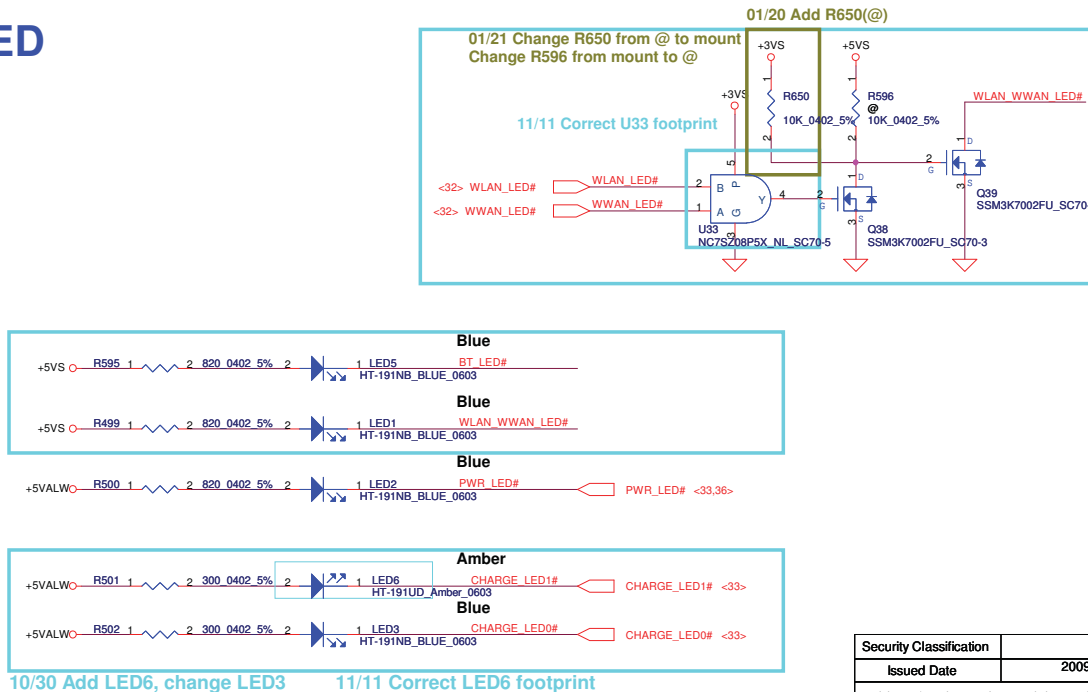


RTC

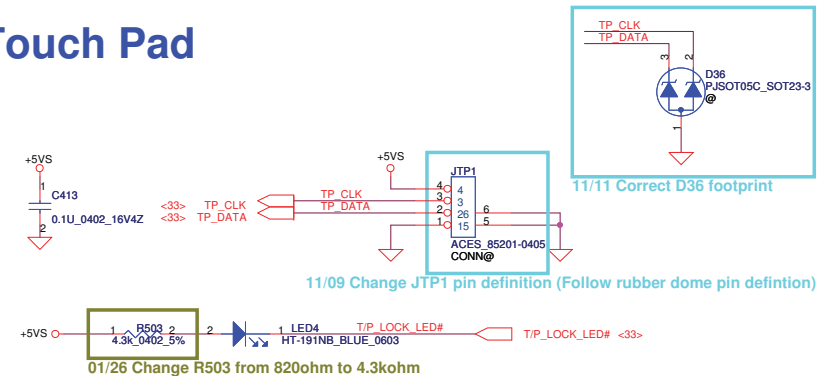
11/10 Delete D26,C412,R497, Add R630,C511 (Follow NIWE2)



LED

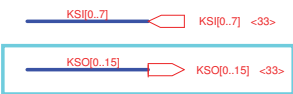


Touch Pad

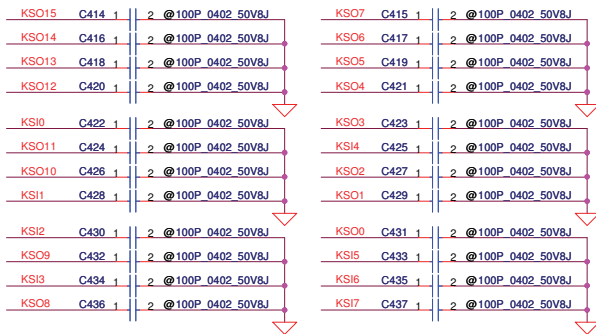
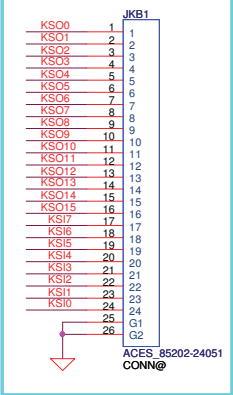


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				NAU00 M/B LA-6101P Schematics	Rev 1.0
				Date	Sheet
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INT_KBD Conn.



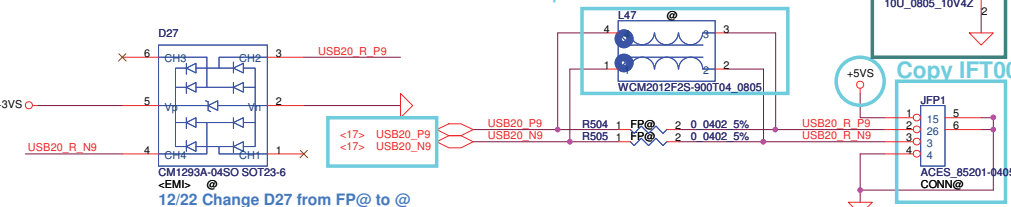
Copy KIUE0



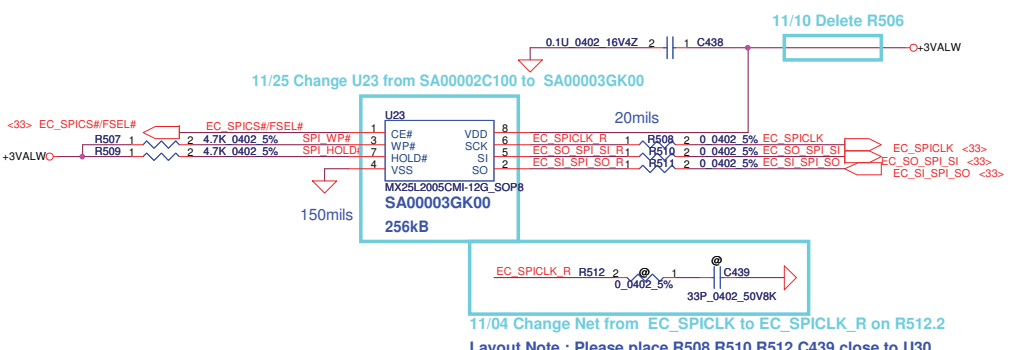
03/02 Add C555 (10uF) for FP power

FingerPrint/B Conn.

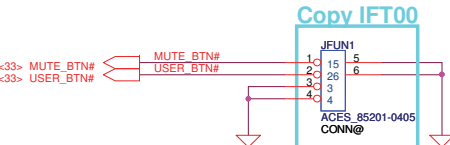
12/17 Change D27,R504,R505 from mount to FP@
10/28 Change Net from USB20_N10,USB20_P10,USB20_R_P10,USB20_R_N10 to USB20_N9,USB20_P9,USB20_R_P9,USB20_R_N9
11/11 Correct L47 footprint



EC SPI ROM

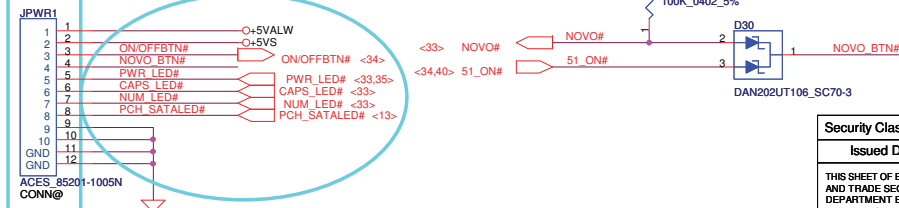


Function/B Conn.



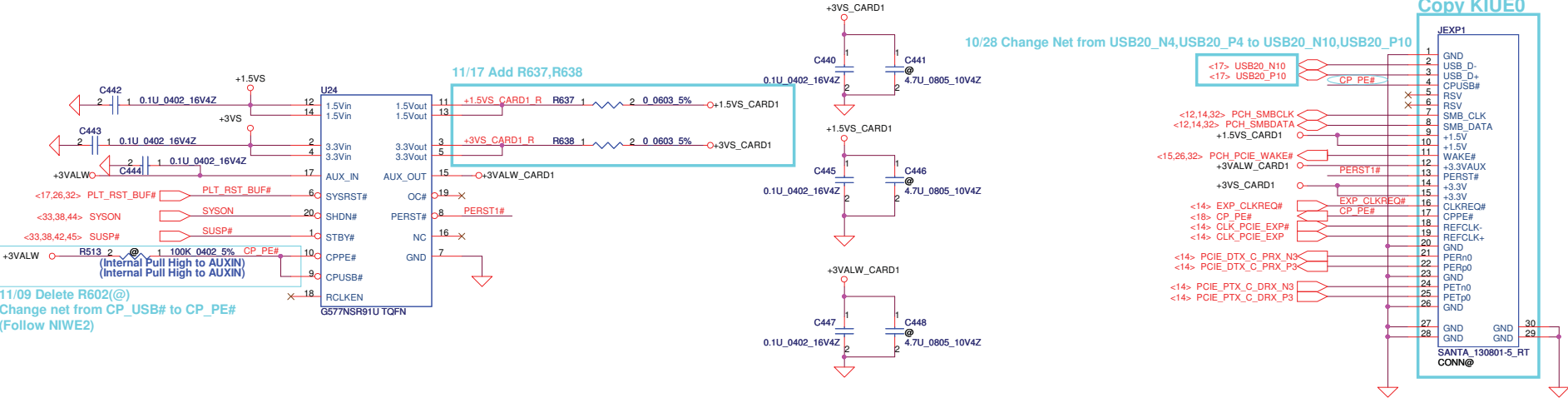
Power/B Conn.

Copy KSW01

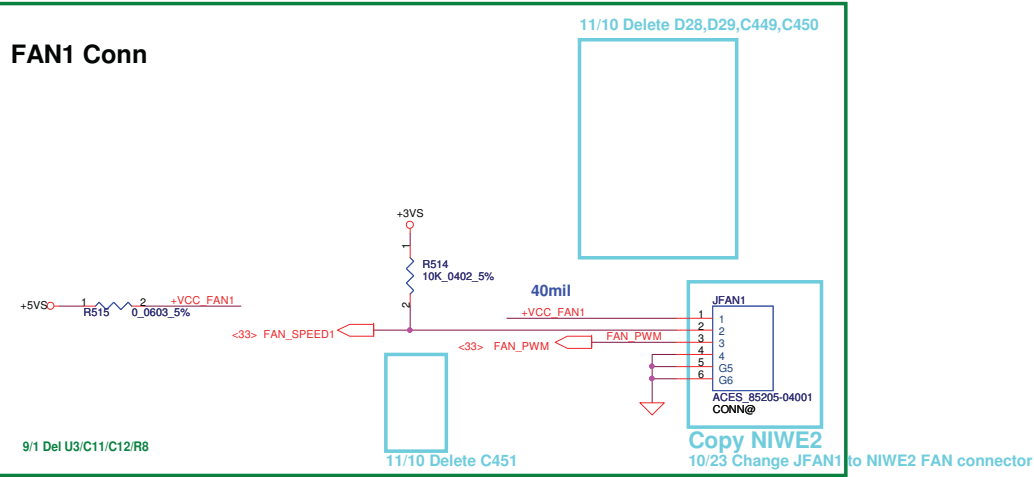


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New Card Power Switch



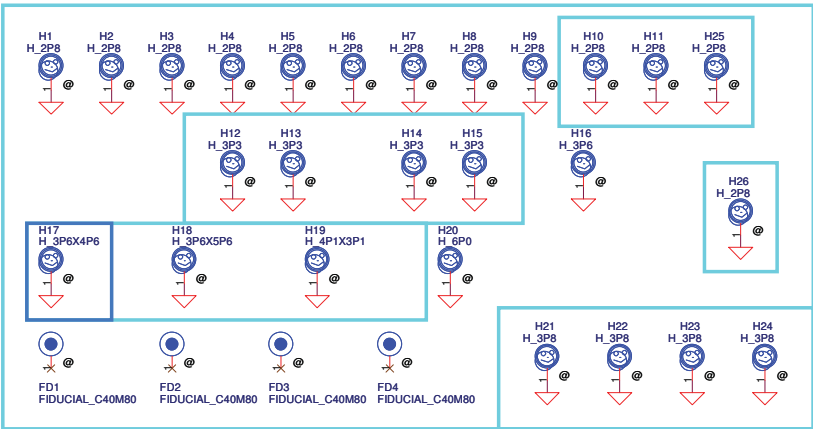
FAN1 Conn



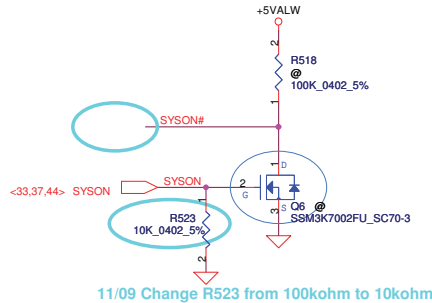
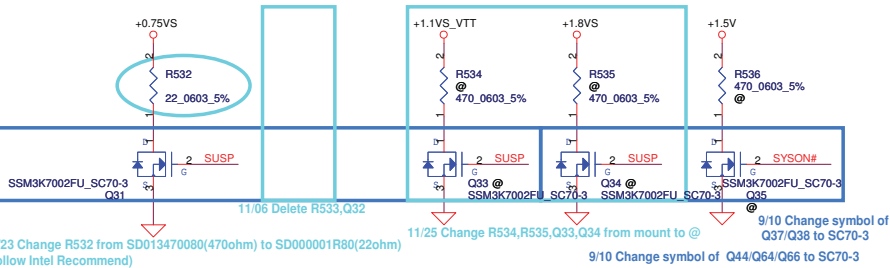
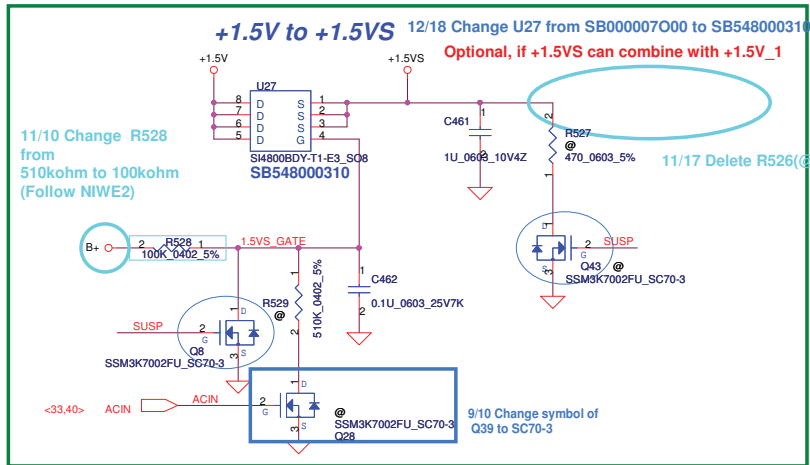
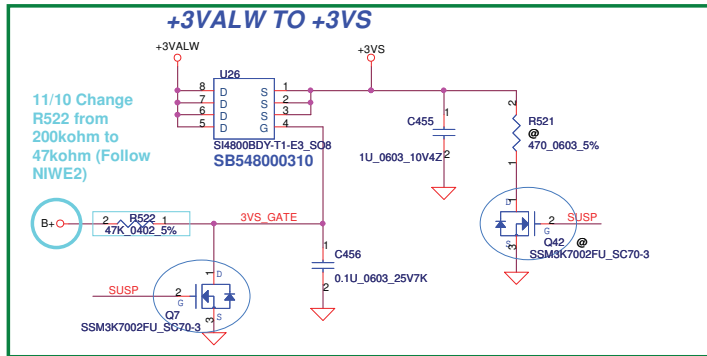
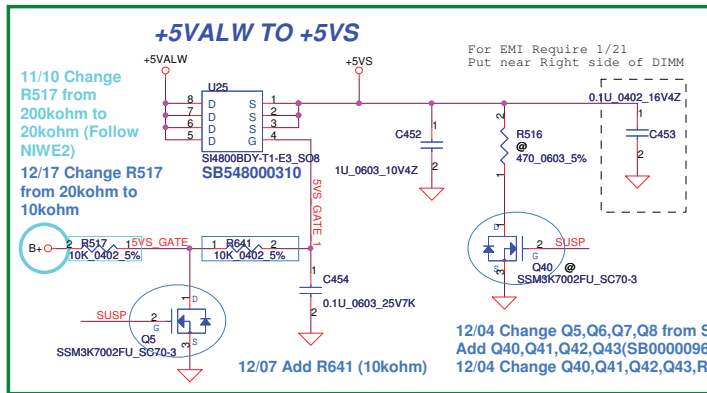
12/10 Change H17 from H_3P6X5P6 to H_3P6X4P6

11/14 Add H26 H_2P8

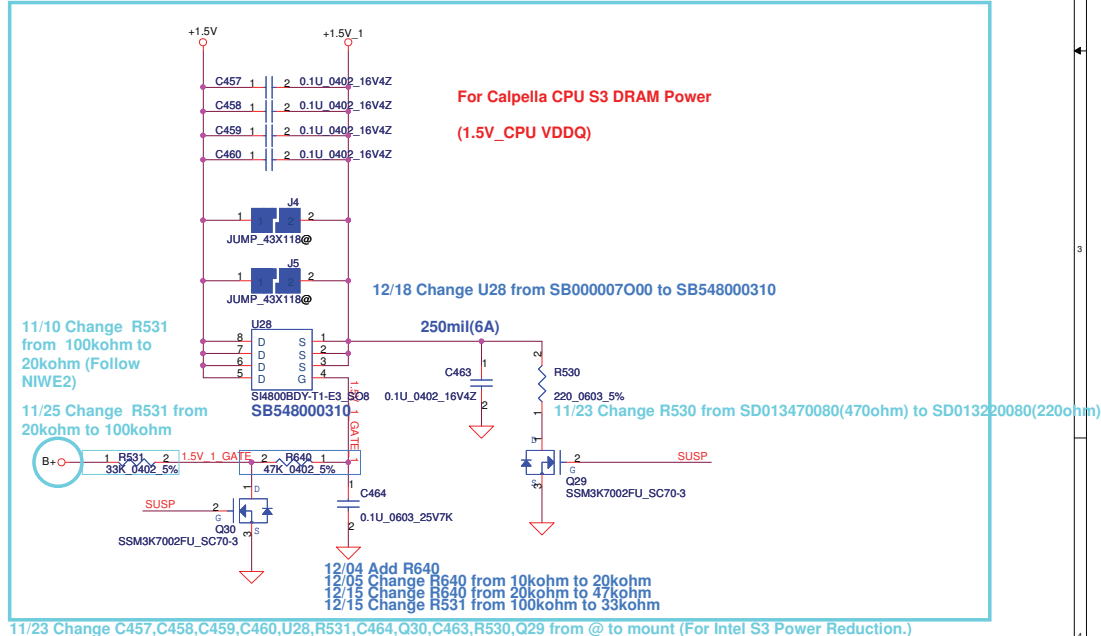
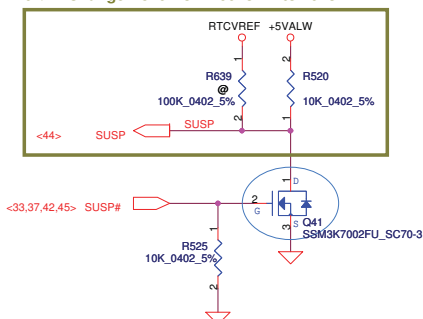
11/11 Change H12-H15 to H_3P3



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Size B	Document Number	NAU00 M/B LA-6101P Schematics		Rev	1.0
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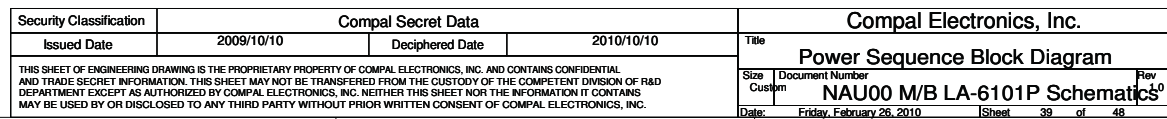


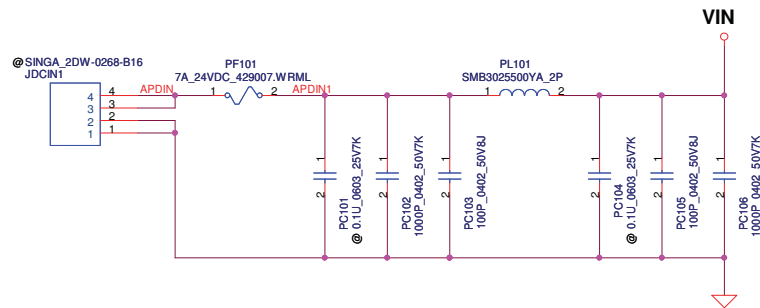
12/04 Add R639, Change R520 from mount to @
01/21 Change R520 from @ to mount
Change R639 from mount to @
01/21 Change R520 from 100kohm to 10kohm



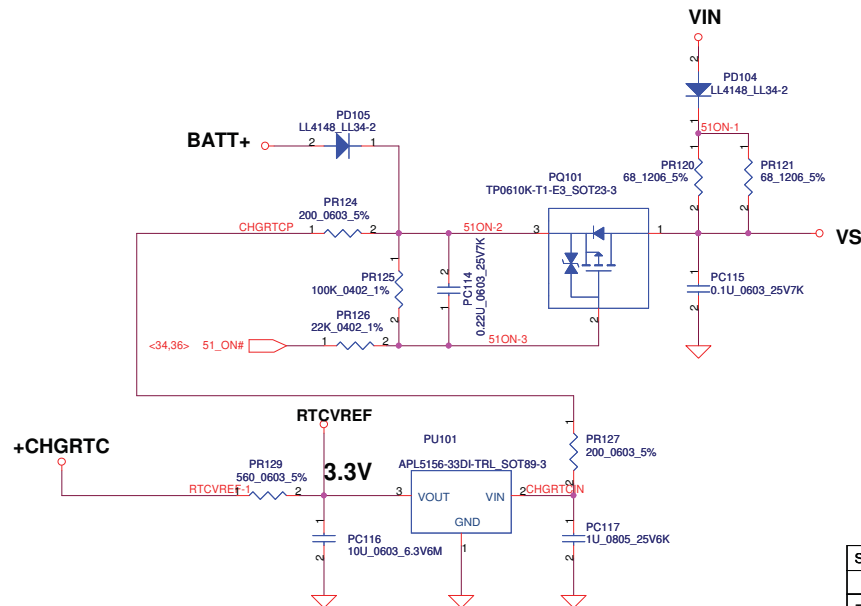
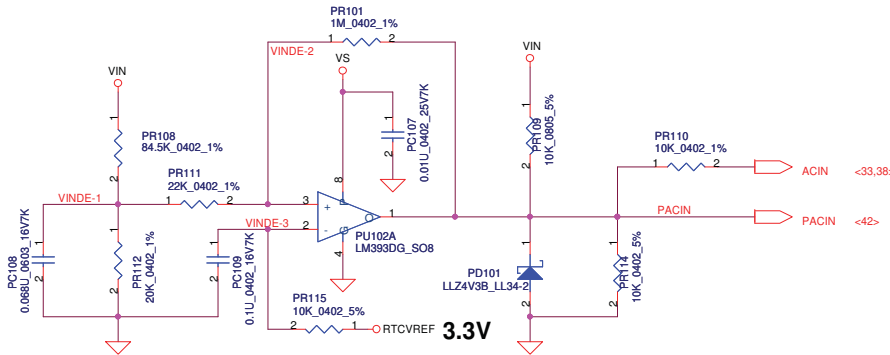
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						Size B	Document Number			NAU00 M/B LA-6101P Schematics		Rev 1.0
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MODEL NAME: *KBLA0 Power Sequence Block Diagram*
PCB NAME: *LA4811P*
REVISION:
DATE: *2008/12/04*





Vin Detector			
	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V

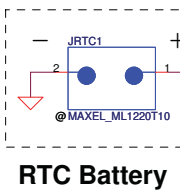
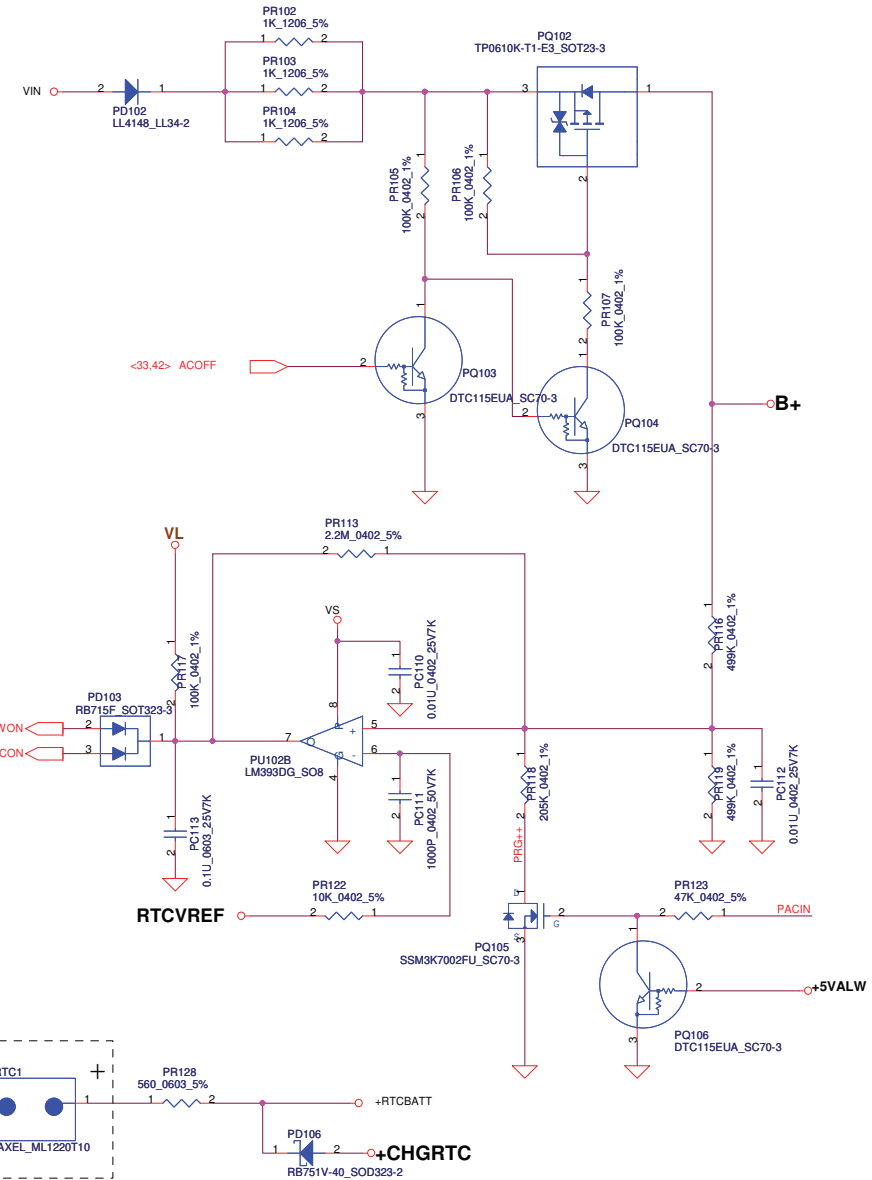


ACIN

Precharge detector			
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

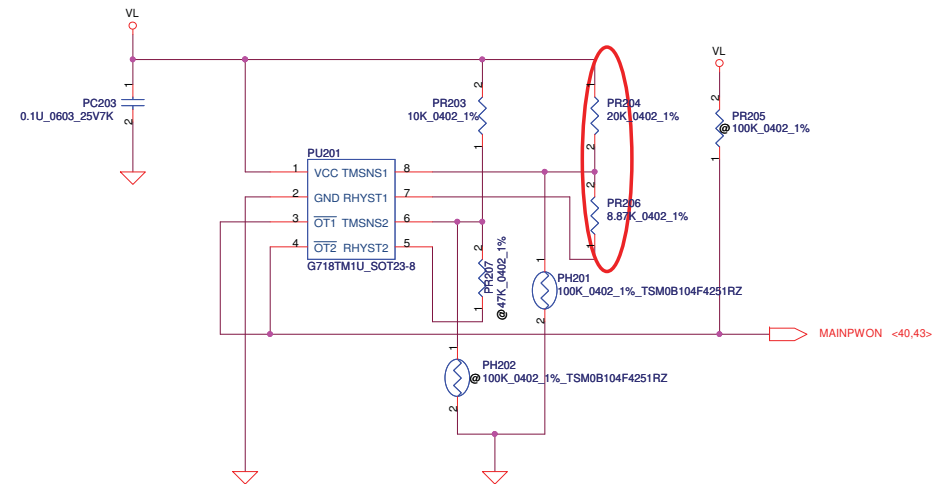
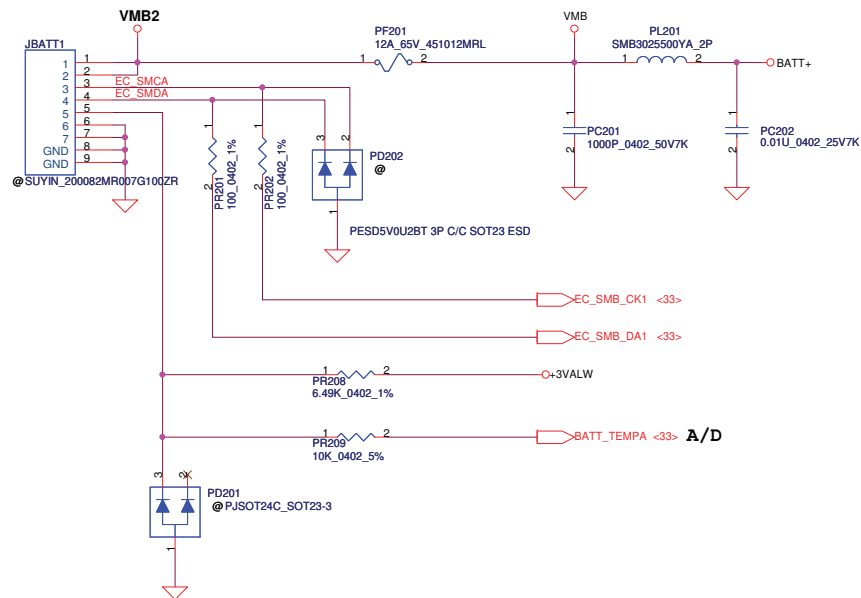
BATT ONLY

Precharge detector			
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

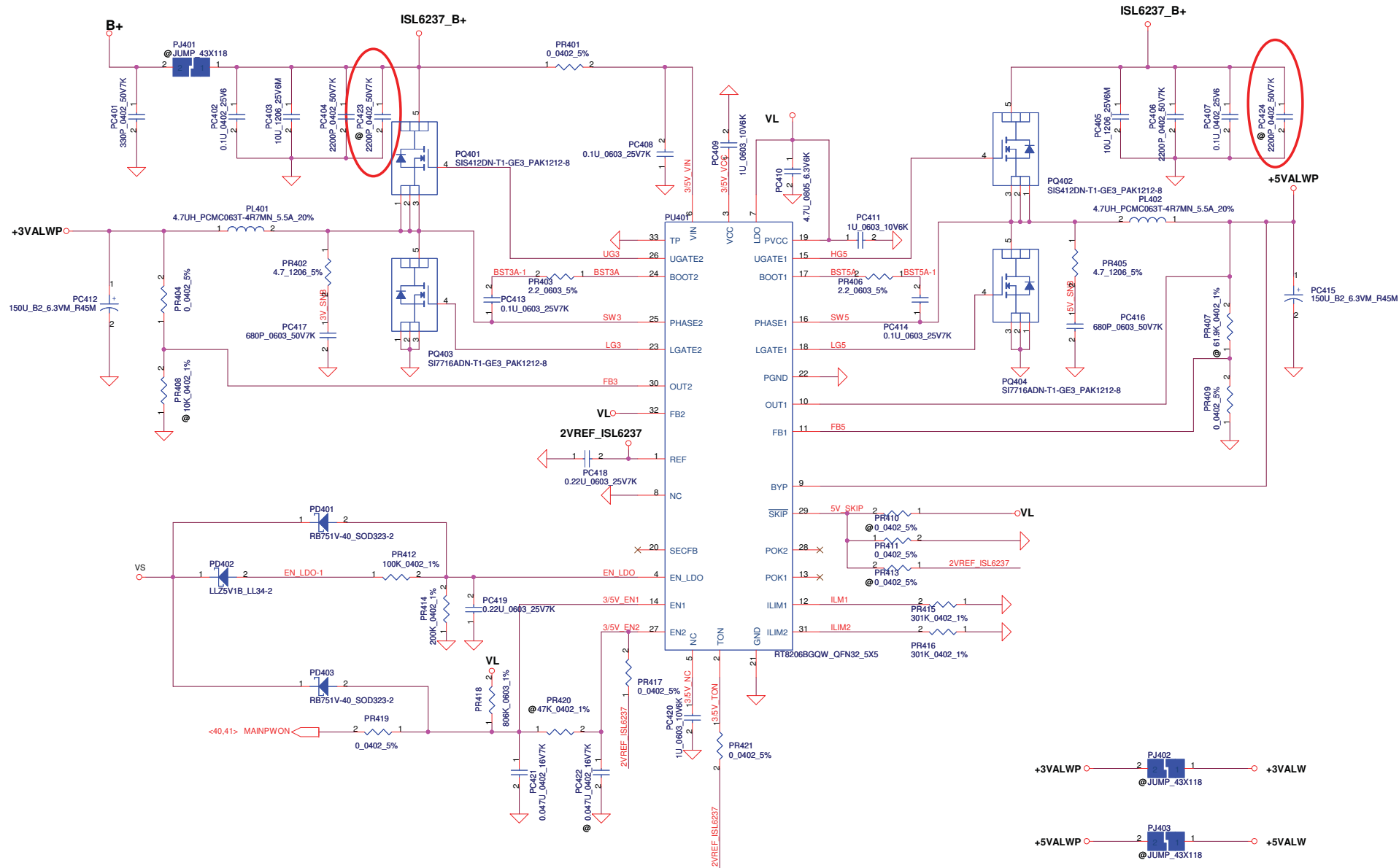


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Deciphered Date				2010/01/06				DCIN & DETECTOR			
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Date				Tuesday, March 09, 2010				Sheet			
40				48				0.1			

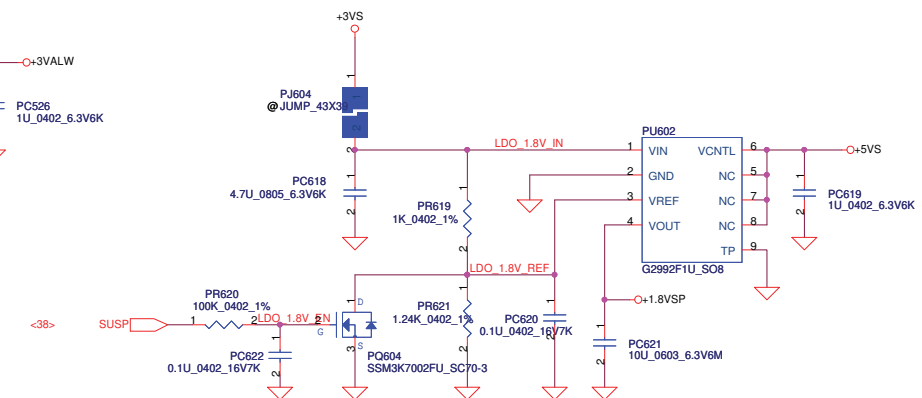
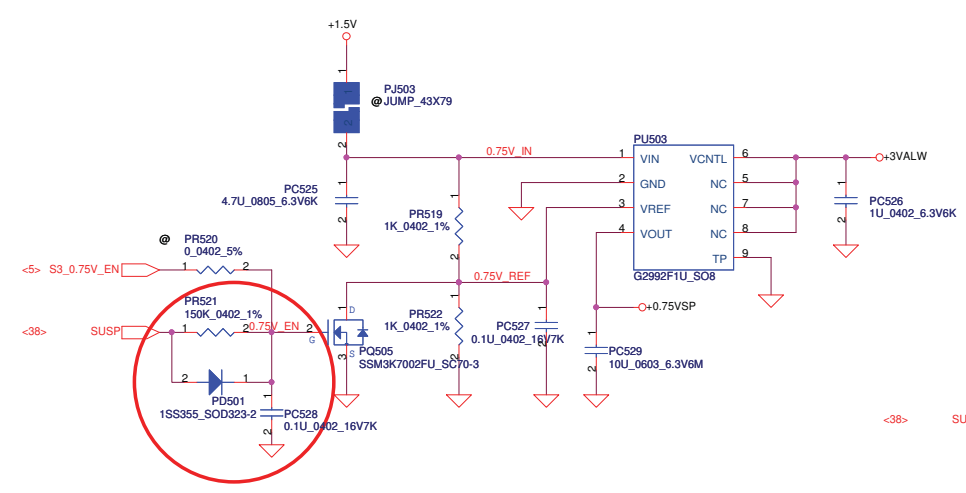
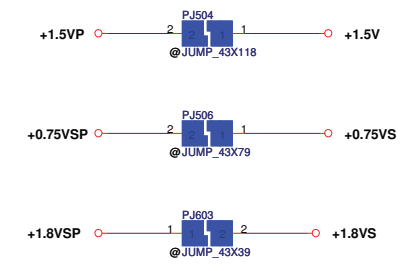
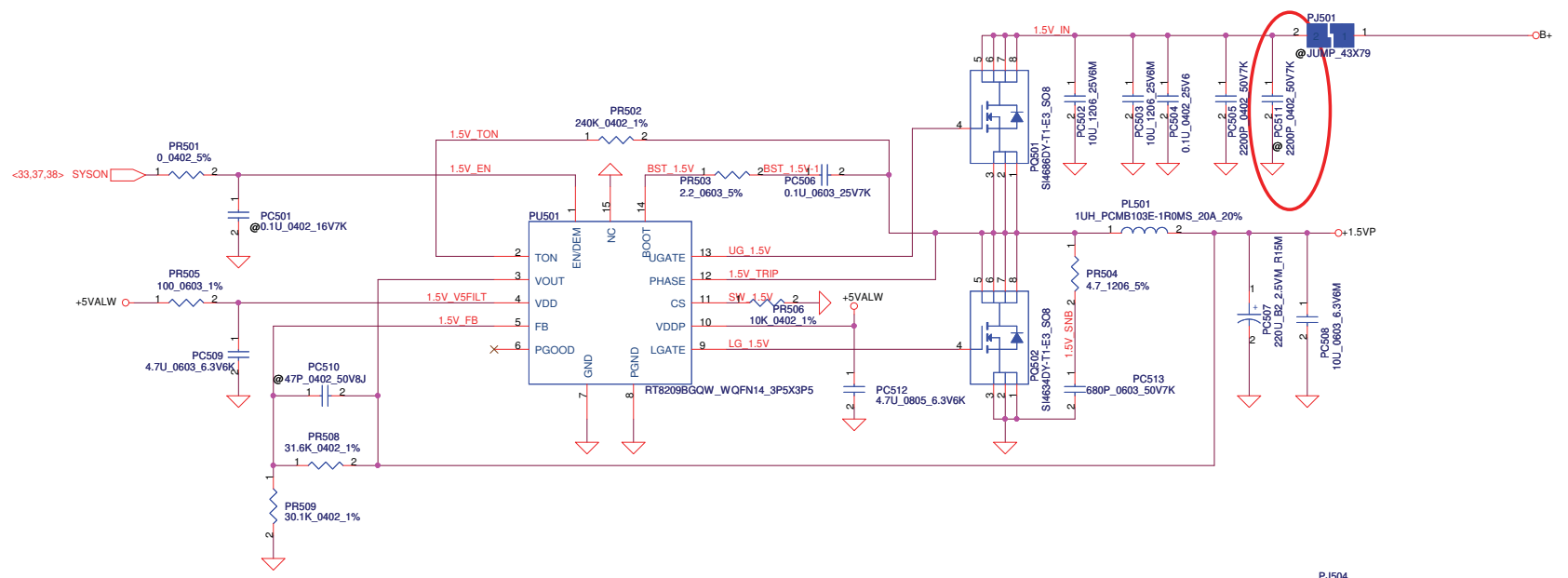
PH1 under CPU botten side :
 CPU thermal protection at 95 degree C
 Recovery at 56 degree C



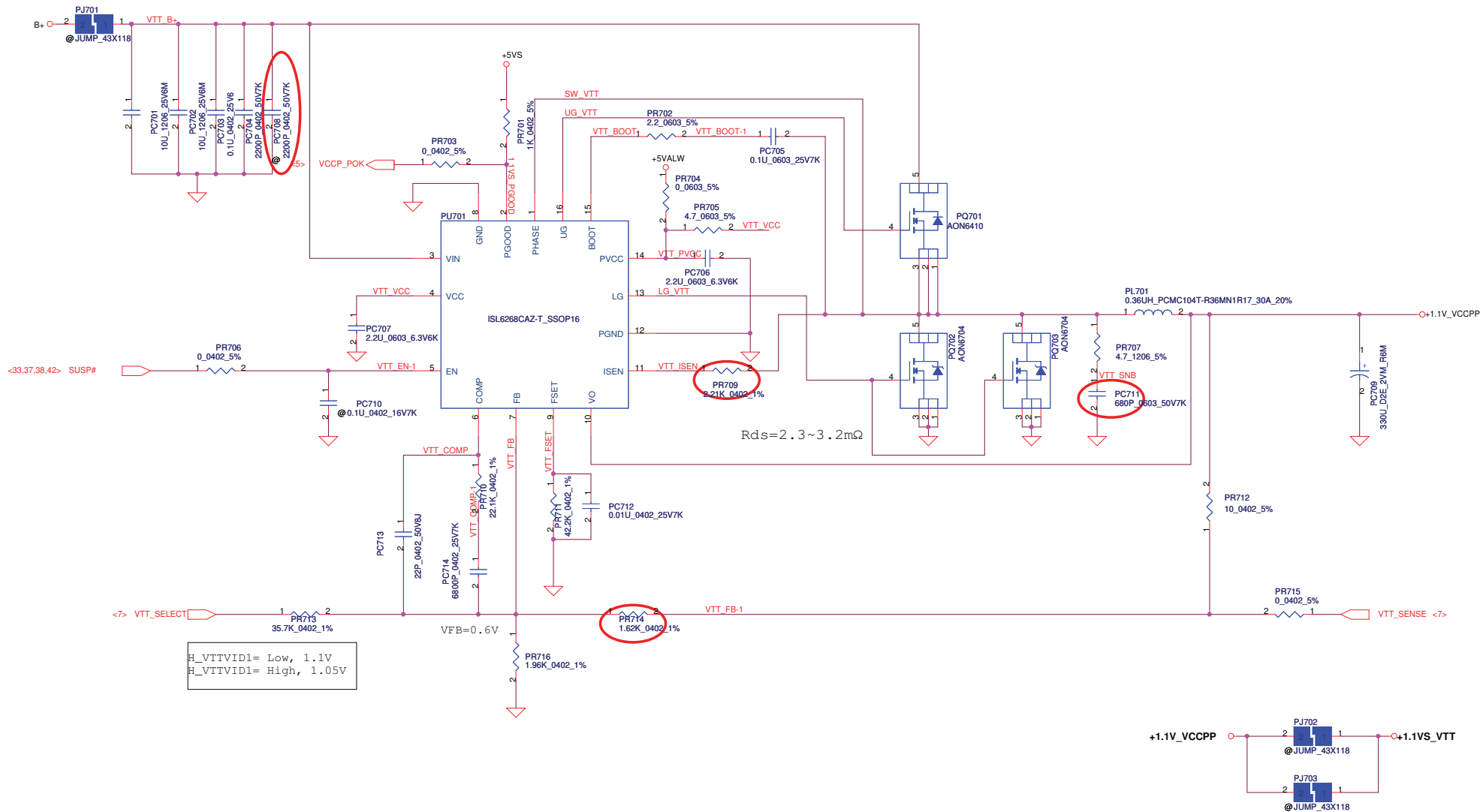
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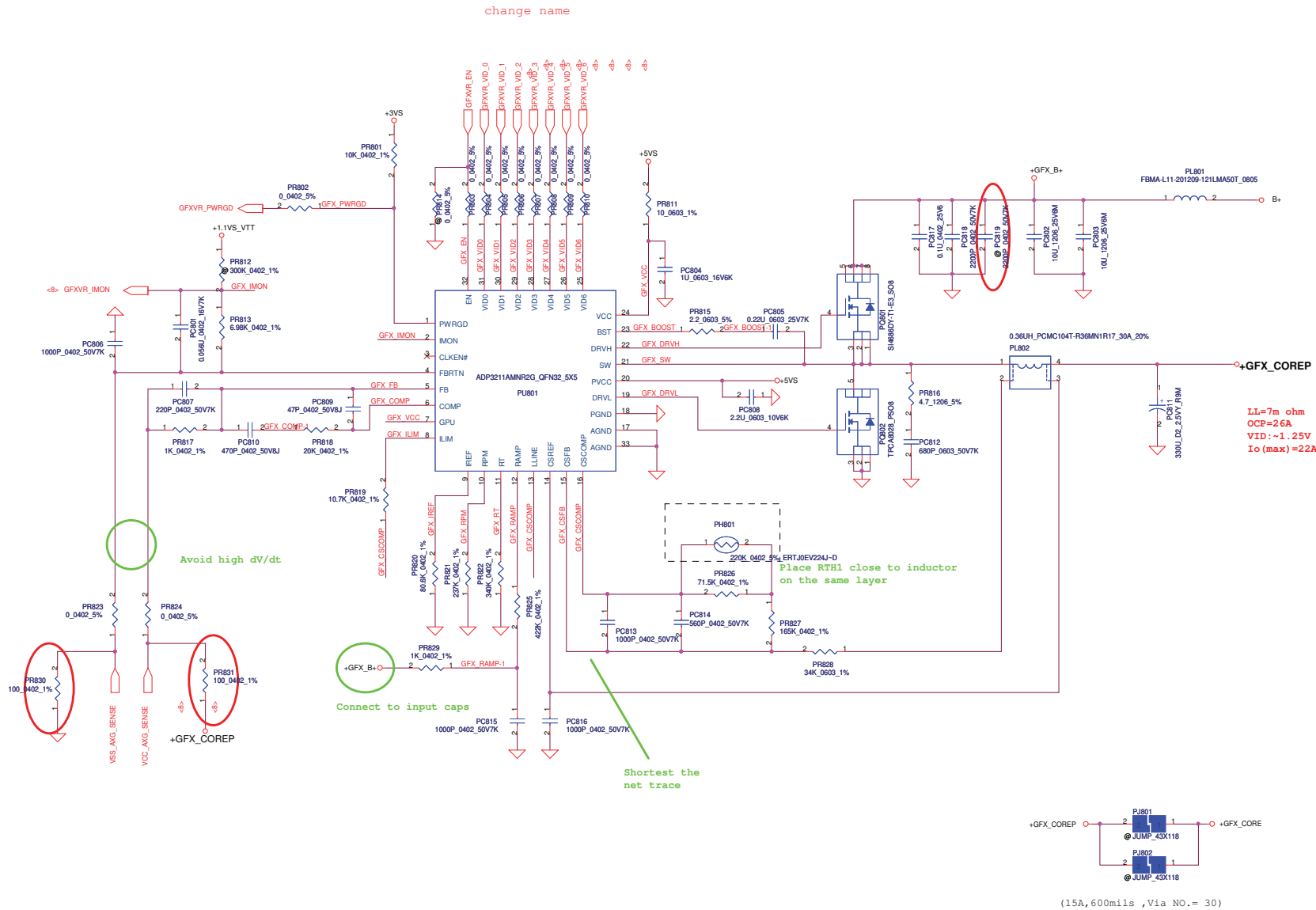
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				Custom	0.1
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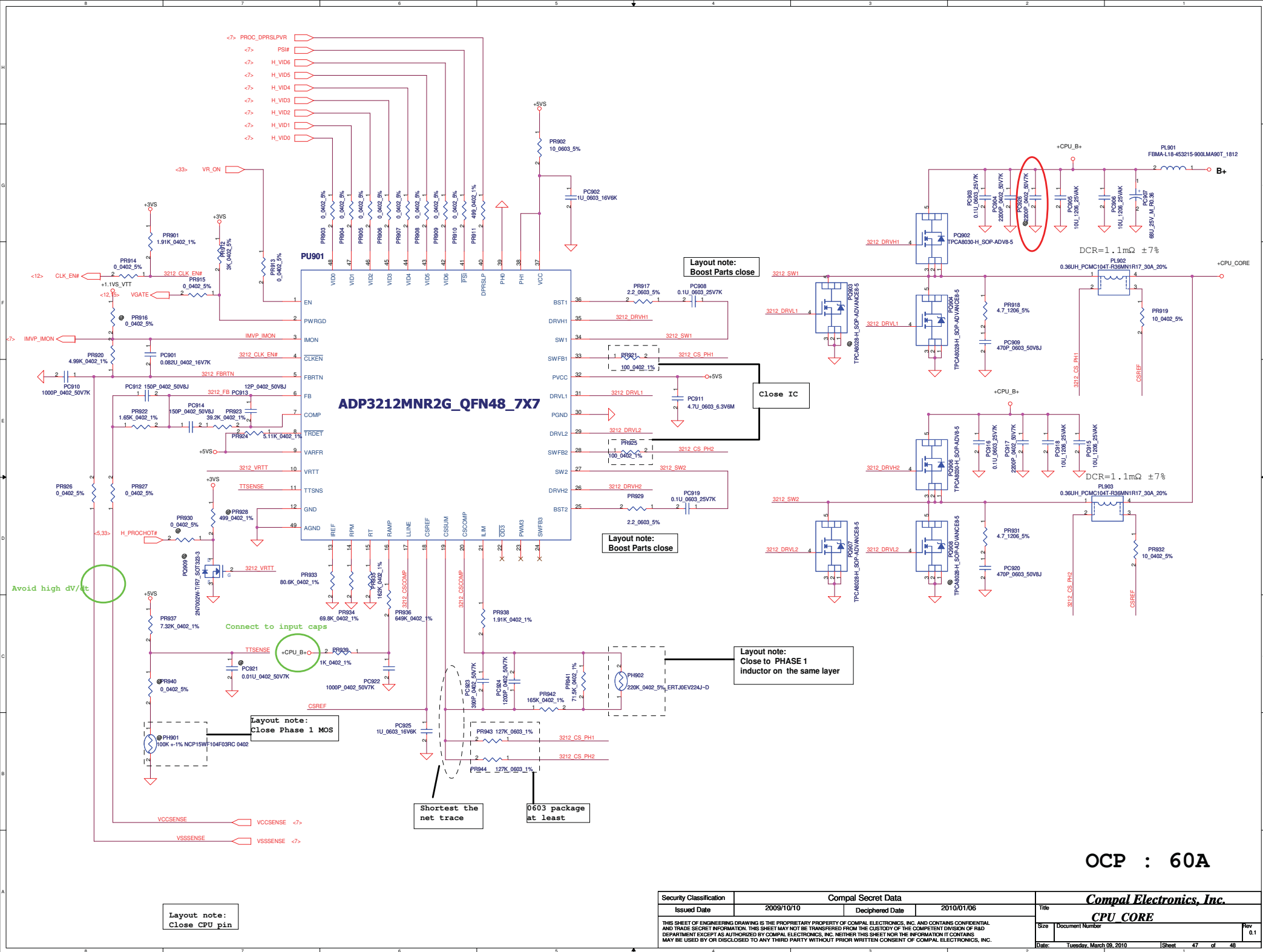


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2009/10/10		2010/01/06		CPU CORE	
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Version change list (P.I.R. List)

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for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	For ESD	P41	Add PD202	2009.11.5	EVT
2	For HW request remove +1.05V's JUMP	P41	Remove +1.05V's JUMP	2009.11.6	EVT
3	Because limited high is not enough.	P47	Change PC907 from 220uF to 68uF	2009.11.6	EVT
4	Add PR830,PR831 for GFX_CORE sence.	P46	Add PR830,PR831 for GFX_CORE sence.	2009.11.17	EVT
5	Change Battery connent footprint.	P41	Change Battery connent footprint.	2009.11.17	EVT
6	Change PR521 from 0ohm to 150Kohm. Add PC528 on BOM.	P44	HW request	2009.11.25	EVT
7	Add PD501.	P44	HW request	2009.12.16	DVT
8	Reserve Cap. on B+ for RF.		RF request	2010.1.15	PVT
9	Change PR204 from 21.5Kohm to 20Kohm. Change PR206 from 9.76Kohm to 8.87Kohm.	P41	Thermal team request to change OTP temp. change from 92 degree to 95 degree.	2010.1.22	PVT
10					
11					
12					
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				Document Number NAU00 M/B LA-6101P Schematics	
				Rev 0.1	
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