

VFKAA

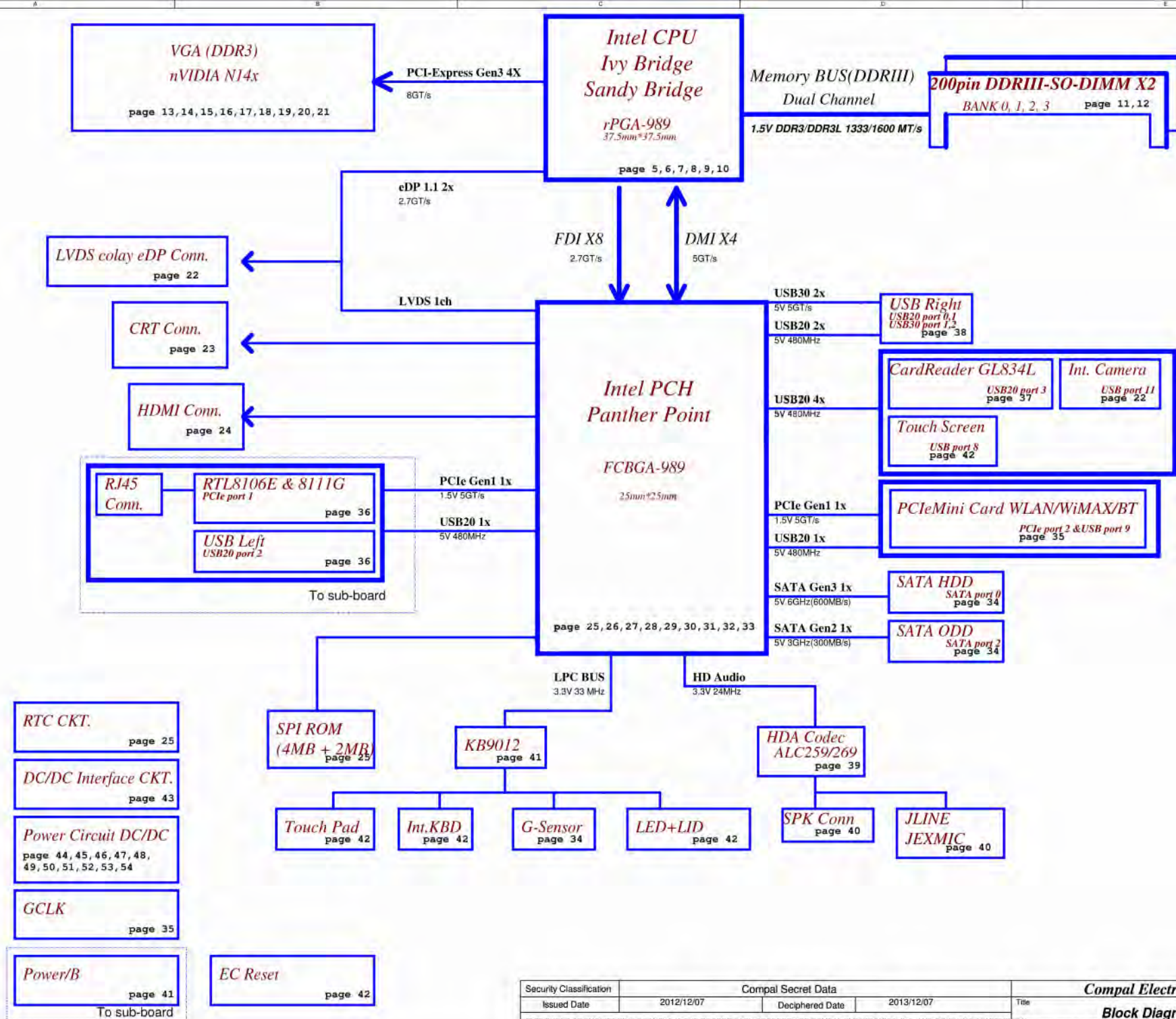
Rosetta 10FG

LA-9863P REV 1.0 Schematics

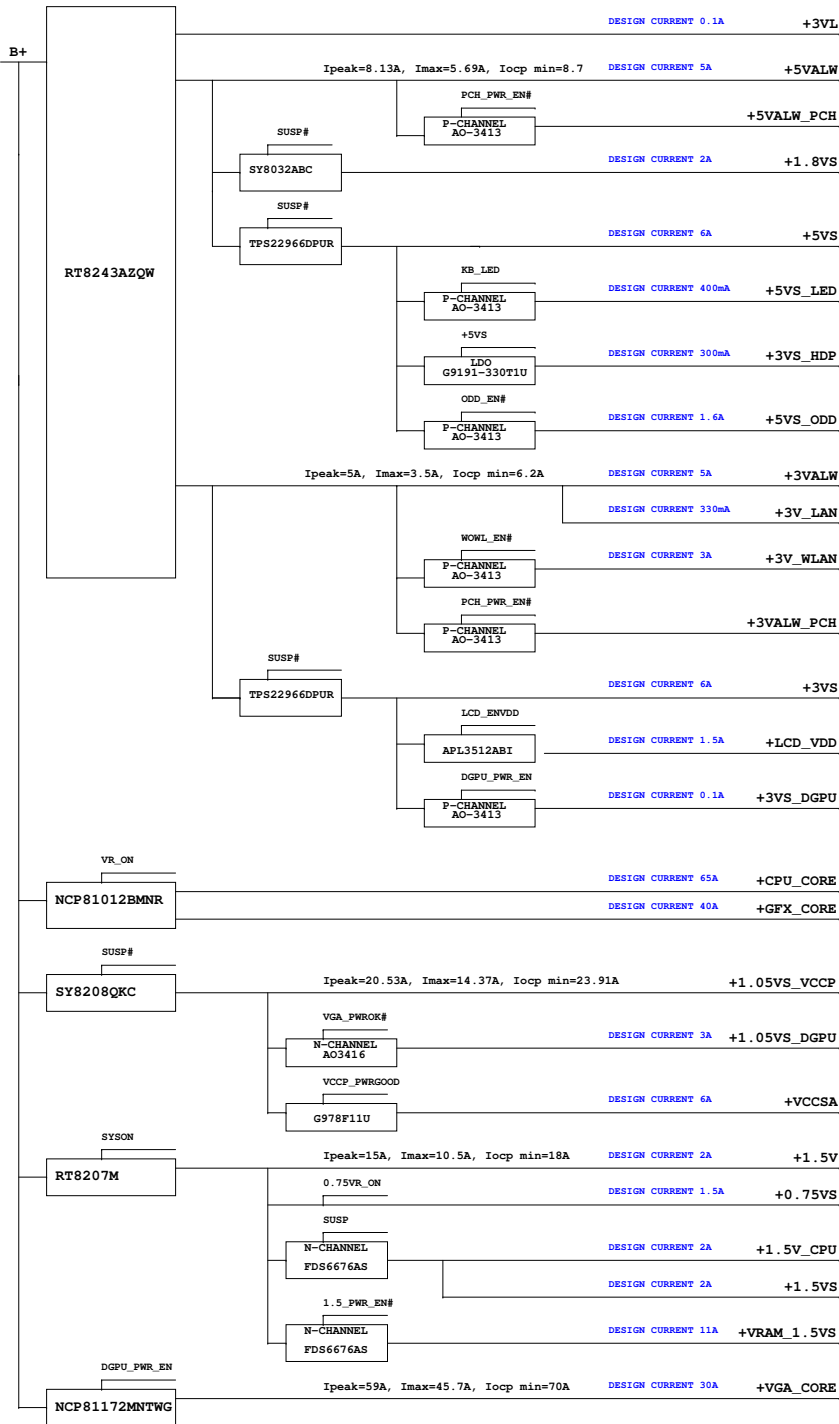
Intel Processor(Ivy Bridge / Sandy Bridge)
PCH(Panther Point)

2013-01-14 Rev 1.0

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Issued Date	2012/12/07	Deciphered Date	2013/12/07	Title	Power Tree
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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW	+1. 5V	+5VS +3VS +1. 8VS +1. 5VS +1. 05VS +0. 75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1. 5VS +3VS_DGPU +1. 05VS_DGPU
	S0	O	O	O	O	O
	S1	O	O	O	O	O
	S3	O	O	O	O	X
	S5 S4/AC	O	O	O	X	X
	S5 S4/ Battery only	O	O	O	X	X
	S5 S4/AC & Battery don't exist	O	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	WLAN/WIMAX		
+3VS	Touch Pad	2C H	0010 1100 b

EC SM Bus1 Address

EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b	+3VS	NVIDIA GPU	9E H	1001 1010 b
+3VL	USB S&C 14640	35 H	0011 0101 b	+3VS	G-Sensor	40 H	0100 0000 b

BTO Option Table

Function	SKU	PCH		GPU		VRAM	EC		ISPD
description	Optimus	Panther Point		N14M-GL	N14P-GV2	Dual Rank	EC		HDMI Logo
explain	Optimus	HM76	HM70	N14M-GL	N14P-GV2	Dual Rank	KB9012	NPCE885N	HDMI Logo
BTO	OPT@	HM76R1@	HM70R1@	N14MGL@	N14PGV2@	DRANK@	9012@	885@	HDMI45@
		HM76R3@	HM70R3@	N14MGLR1@	N14PGV2R1@				
				N14MGLR3@	N14PGV2R3@				

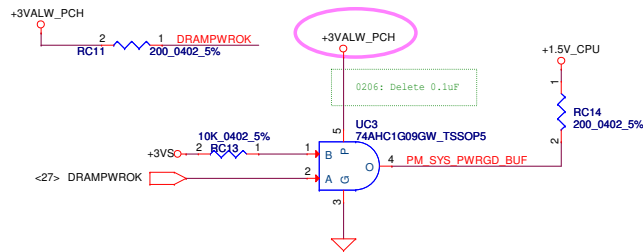
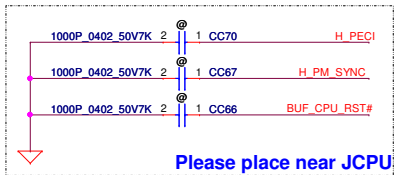
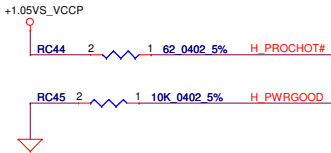
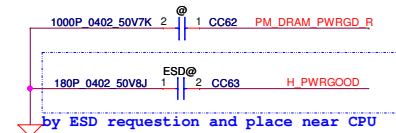
Function	LVDS-eDP		Camera & Mic	USB S&C		CRT		Touch Screen
description	LVDS-eDP		Camera & Mic	14640	14641	CRT		Touch Screen
explain	LVDS	eDP	Camera & Mic	14640	14641	w/ CRT		Touch Screen
BTO	LVDS@	IEDP@	CAM_EMI@	14640@	14641@	CRT@	CRT_EMI@	TOUCH_EMI@

Function	WOWL		G-SENSOR	ZPODD		GCLK		VRAM SKU for GV2	
description	WOWL		G-SENSOR	ZPODD		GCLK	non-GCLK	Single Rank	Dual Rank
explain	w/	w/o	G-SENSOR	w/	w/o	GCLK	non-GCLK	Single Rank	Dual Rank
BTO	WOWL@	NOWOWL@	GSENSOR@	ZPODD@	NONZP@	GCLK@	NOGCLK@	GVSR@	GVDR@

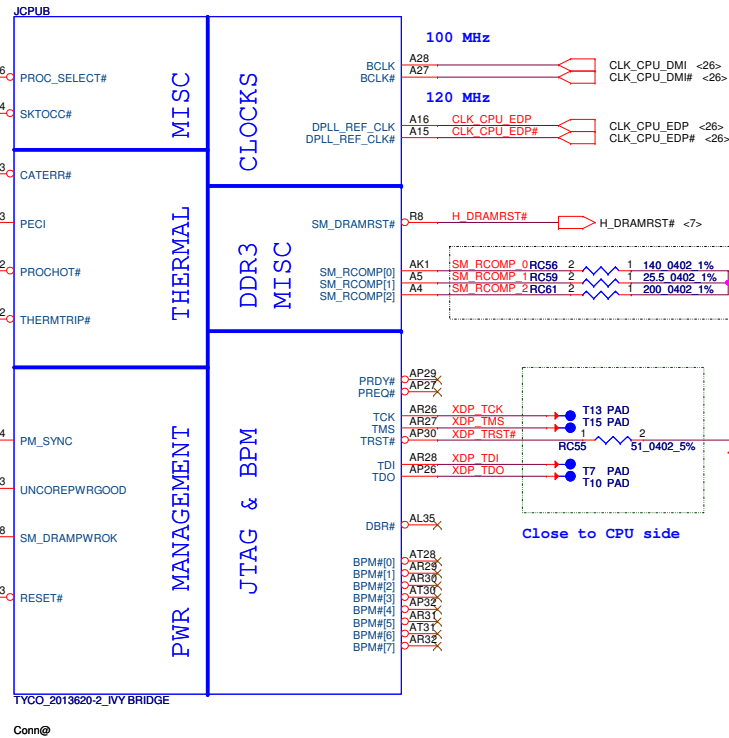
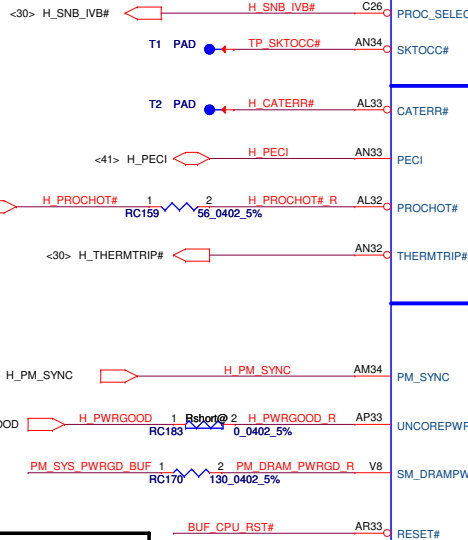
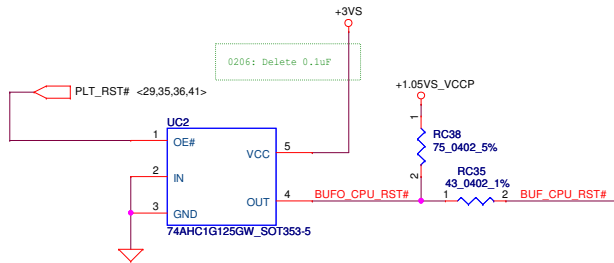
Function	Sleep & Music		KB Light	EMI/ESD part	
description	Sleep & Music		KB Light	EMI/ESD part	
explain	w/ S&M	w/o S&M	KB Light	EMI/ESD part	
BTO	269@	259@	KBL@	EMI@	ESD@

STATE	SIGNAL		
	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

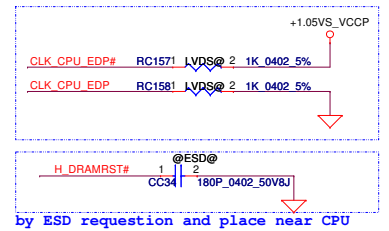
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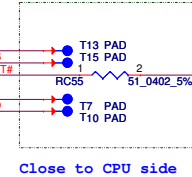
Buffered Reset to CPU



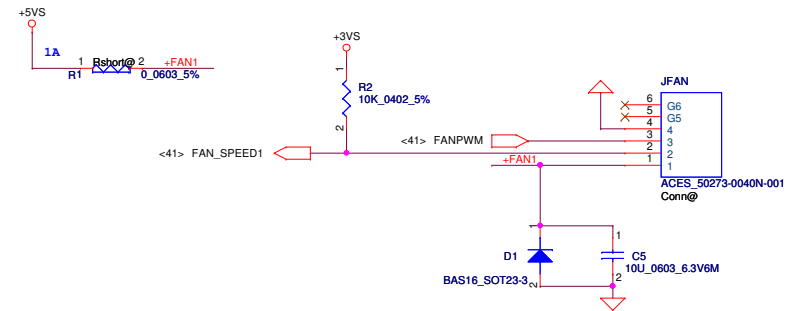
Stuff R41 and R42 if do not support eDP



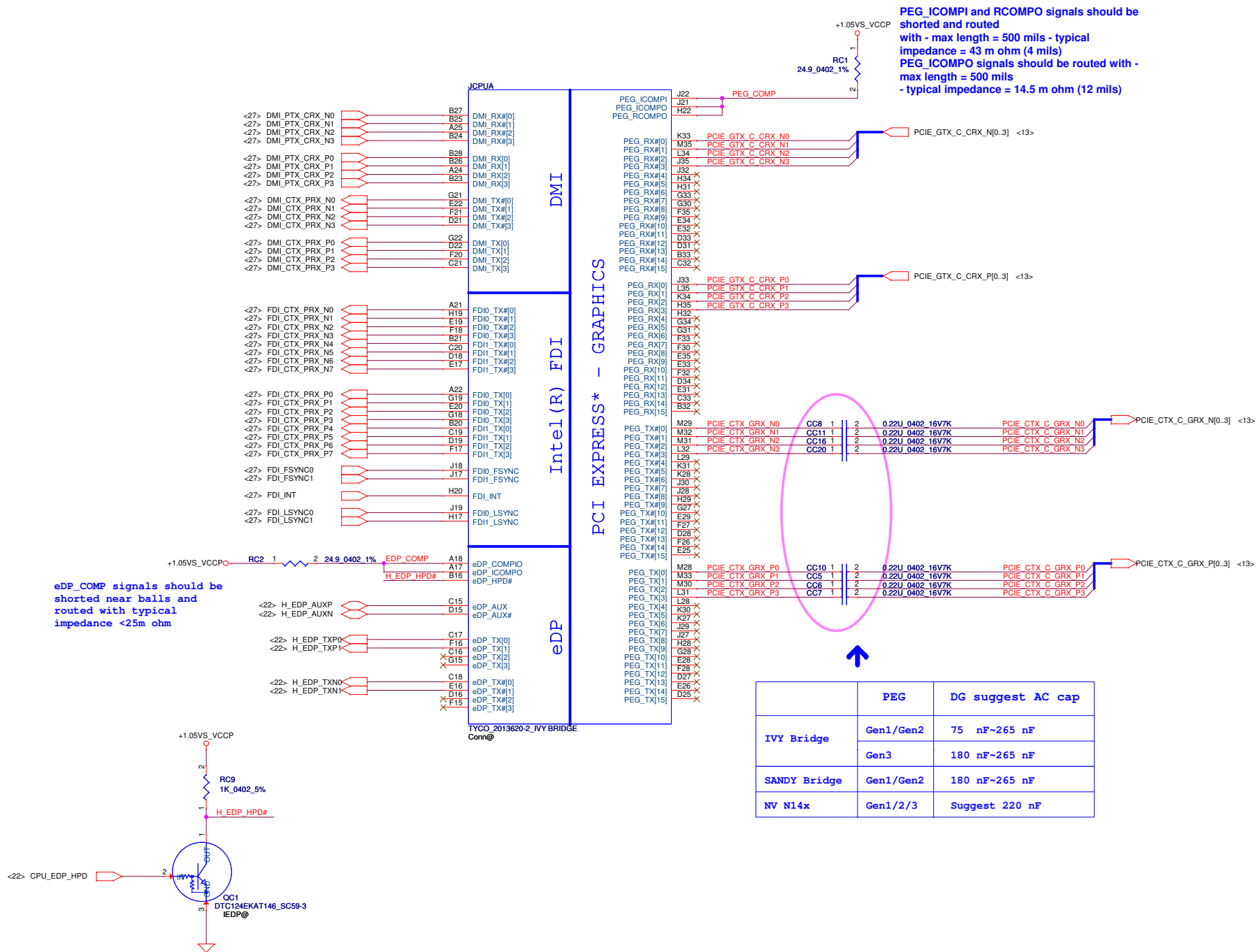
DDR3 Compensation Signals
Layout Note: Place these
resistors near Processor



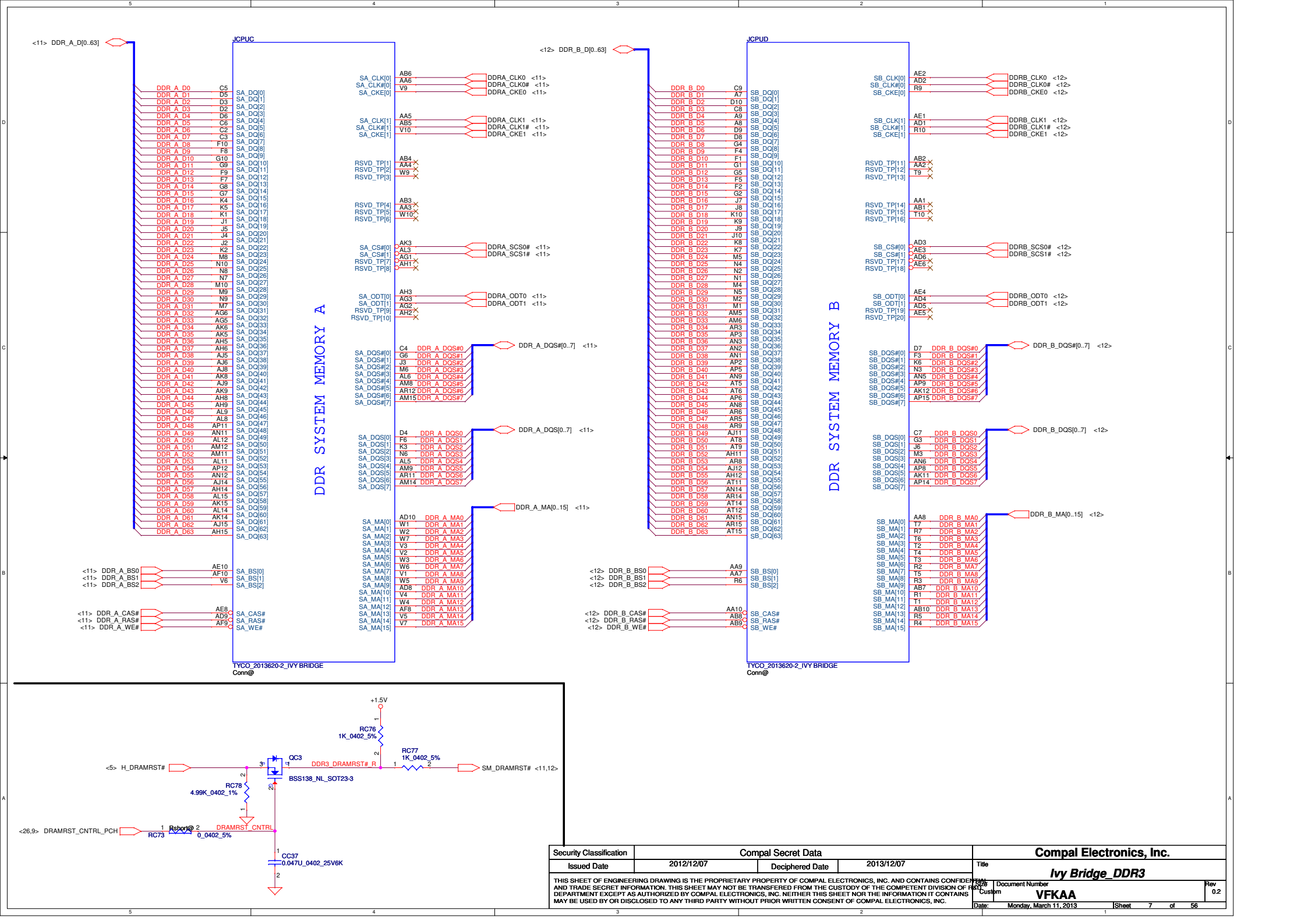
FAN Control Circuit

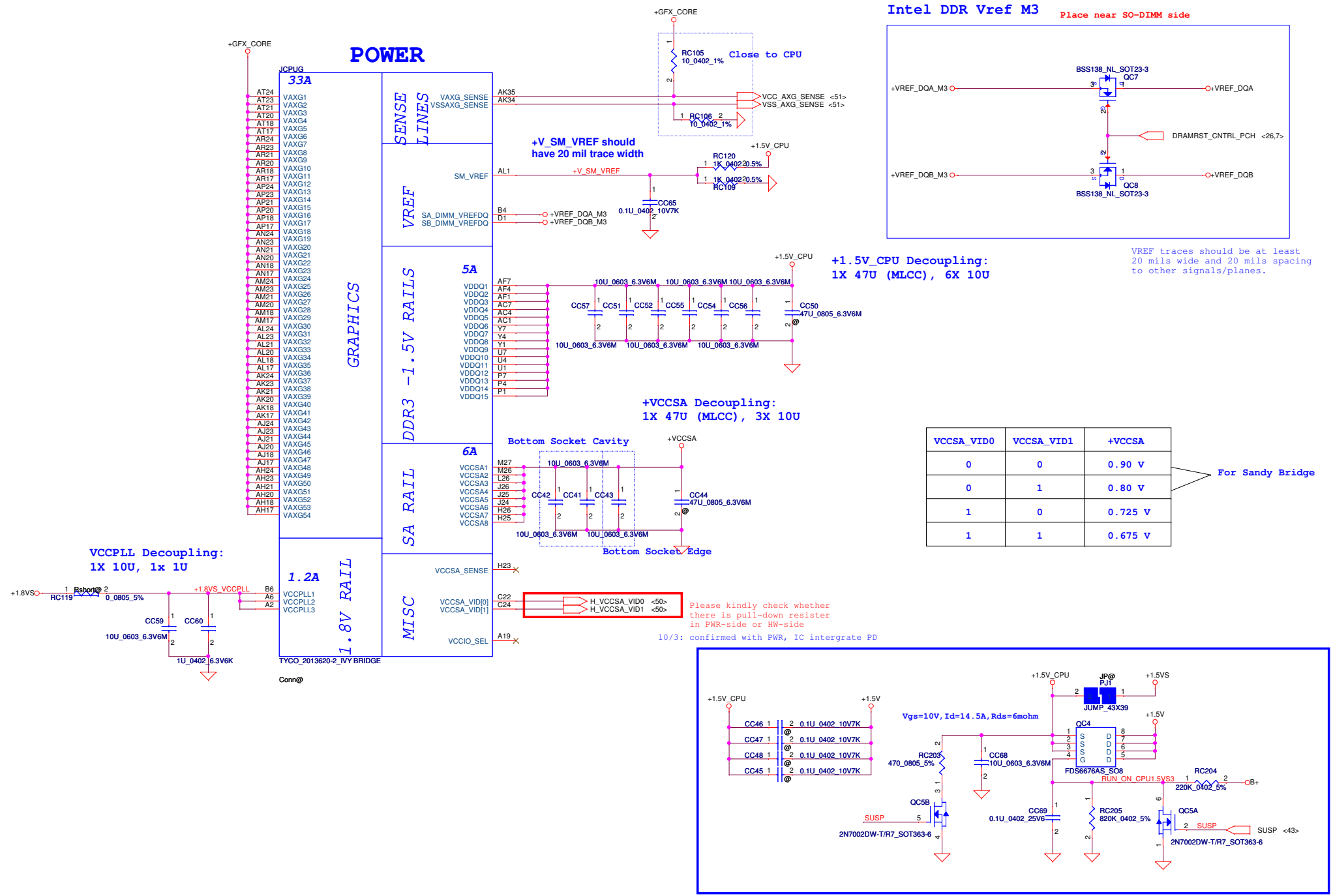


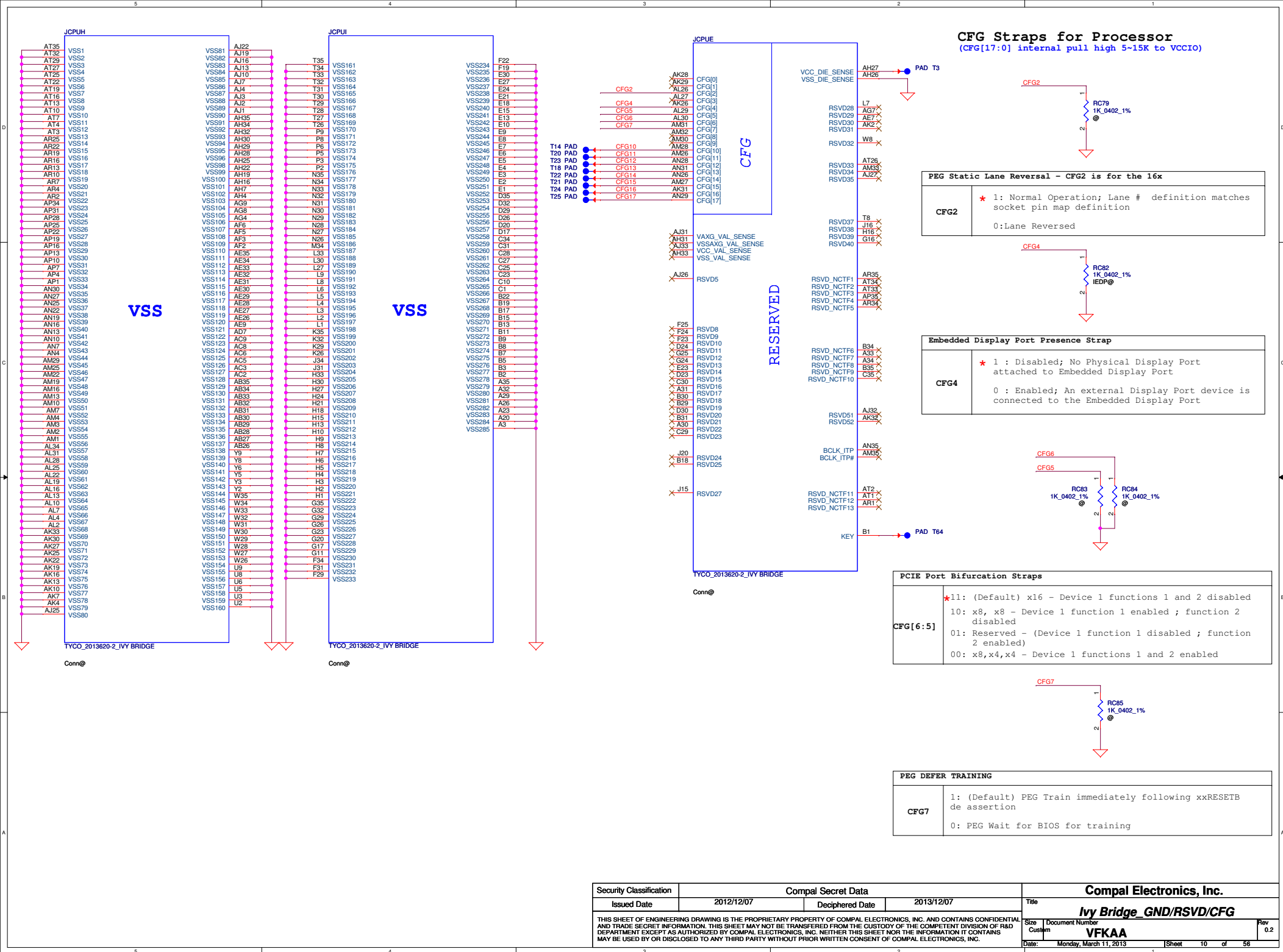
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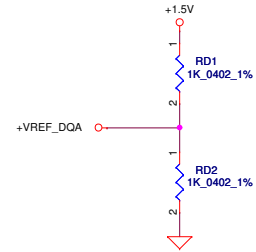
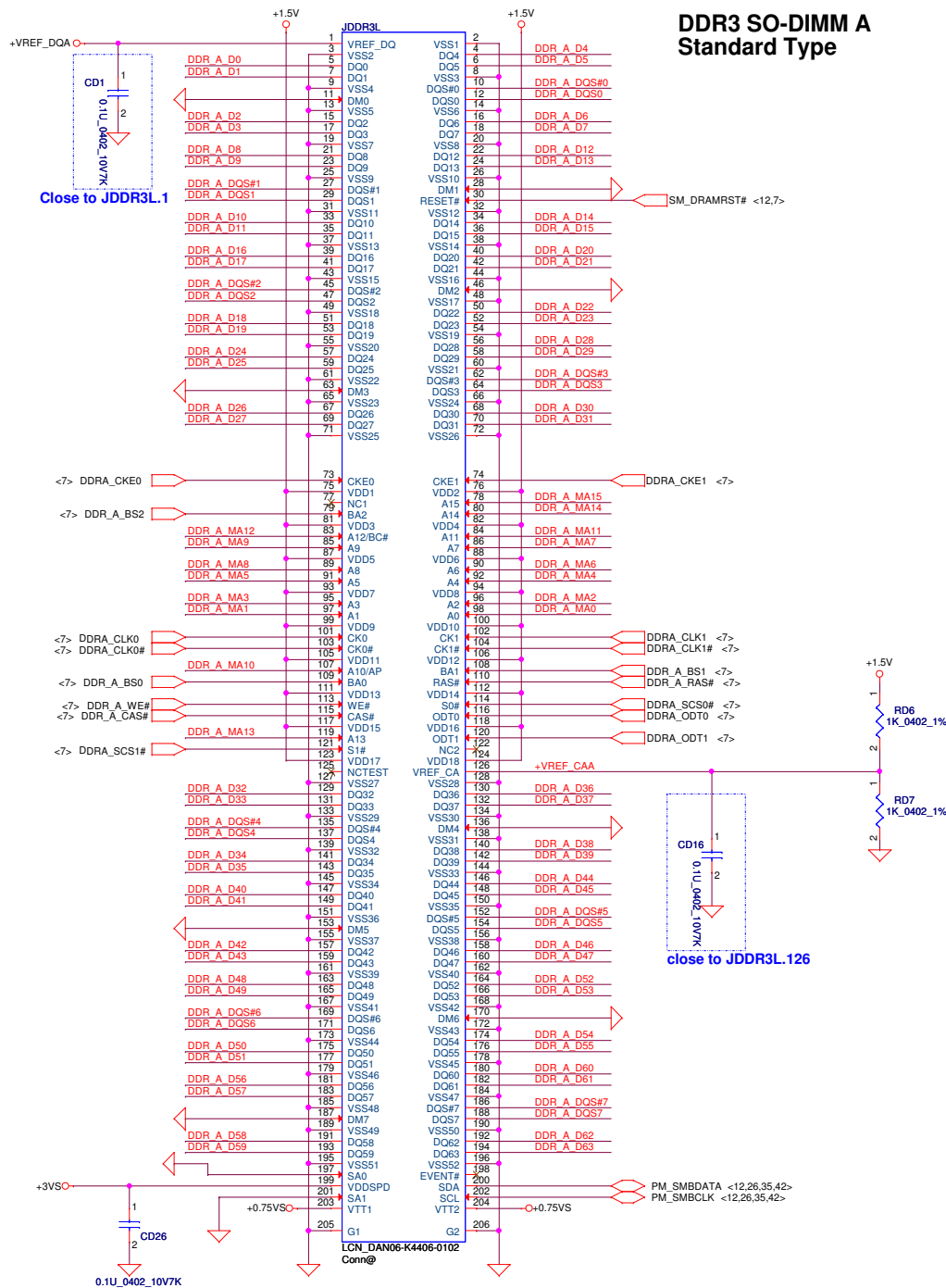
	PEG	DG suggest AC cap
IVY Bridge	Gen1/Gen2	75 nF~265 nF
	Gen3	180 nF~265 nF
SANDY Bridge	Gen1/Gen2	180 nF~265 nF
NV N14x	Gen1/2/3	Suggest 220 nF







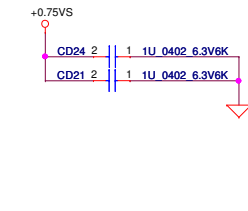
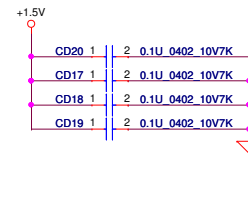
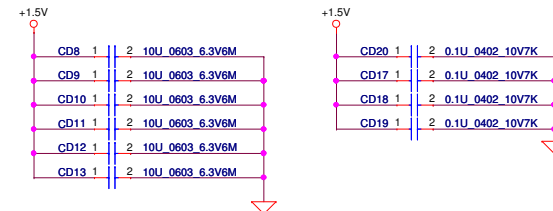
DDR3 SO-DIMM A Standard Type



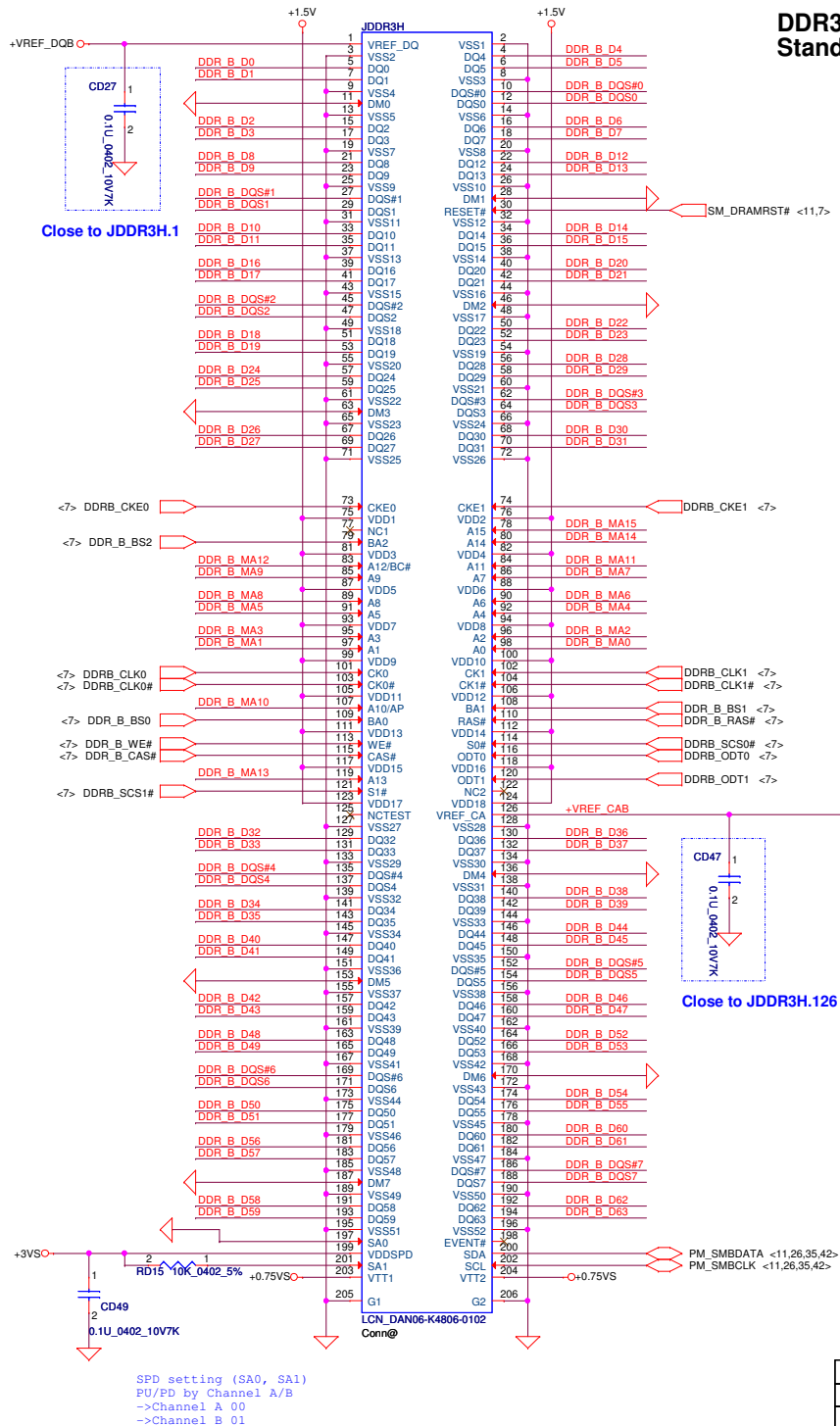
Layout Note:
Place near JDDR L

Layout Note: Place these 4 Caps near
Command and Control signals of DIMMA

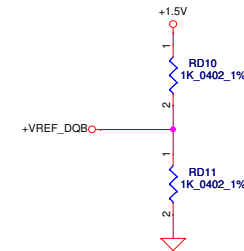
Layout Note:
Place near JDDR L.203 and 204



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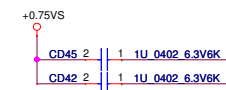
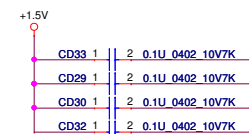
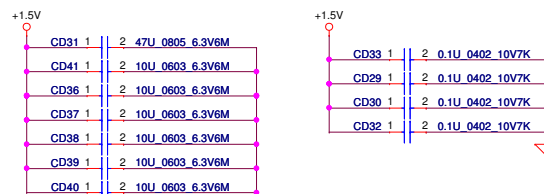
DDR_B_DQS#[0..7] <7>
DDR_B_DQS#[0..7] <7>
DDR_B_D[0..63] <7>
DDR_B_MA[0..15] <7>



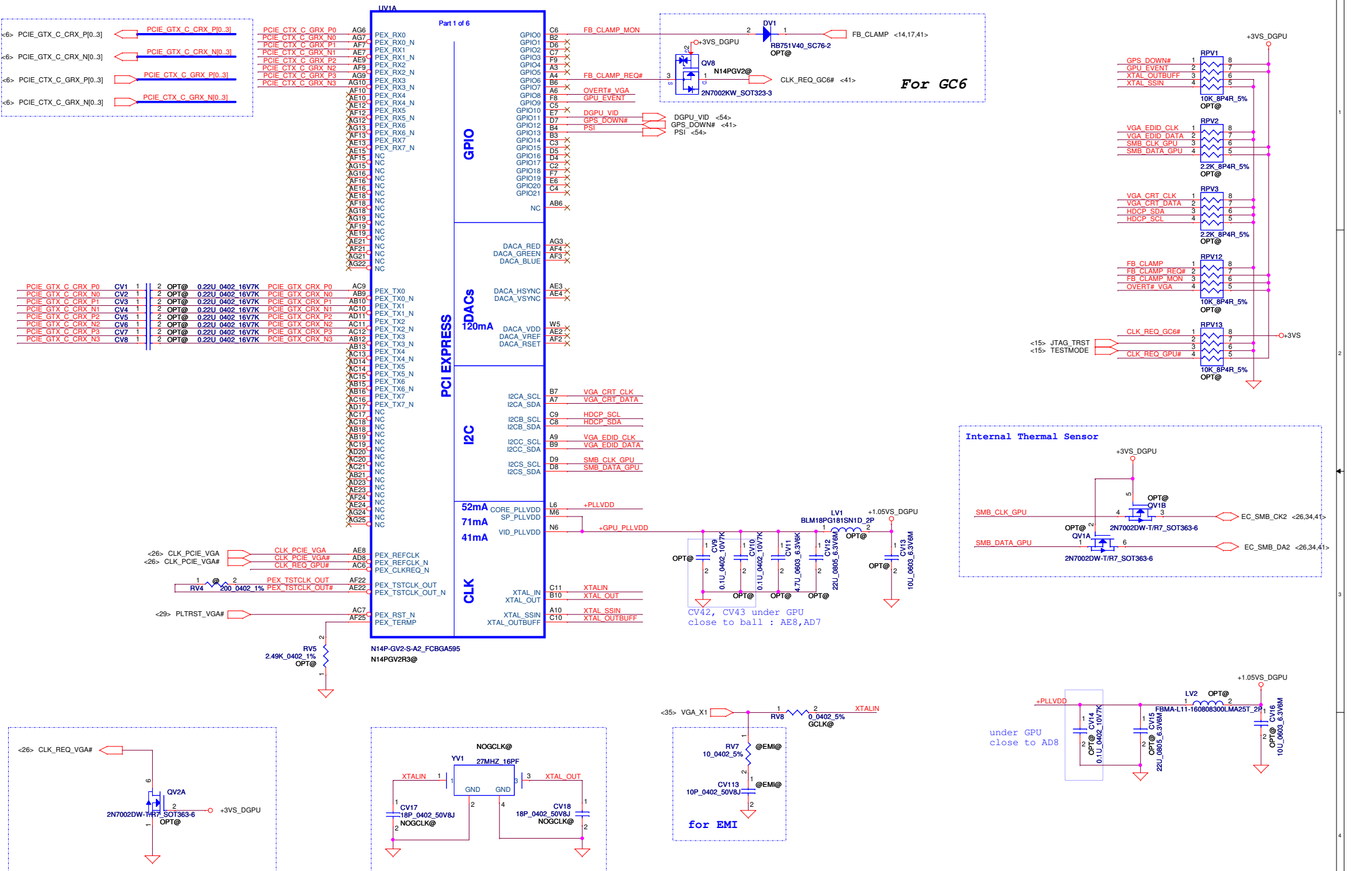
Layout Note:
Place near JDDRH

Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB

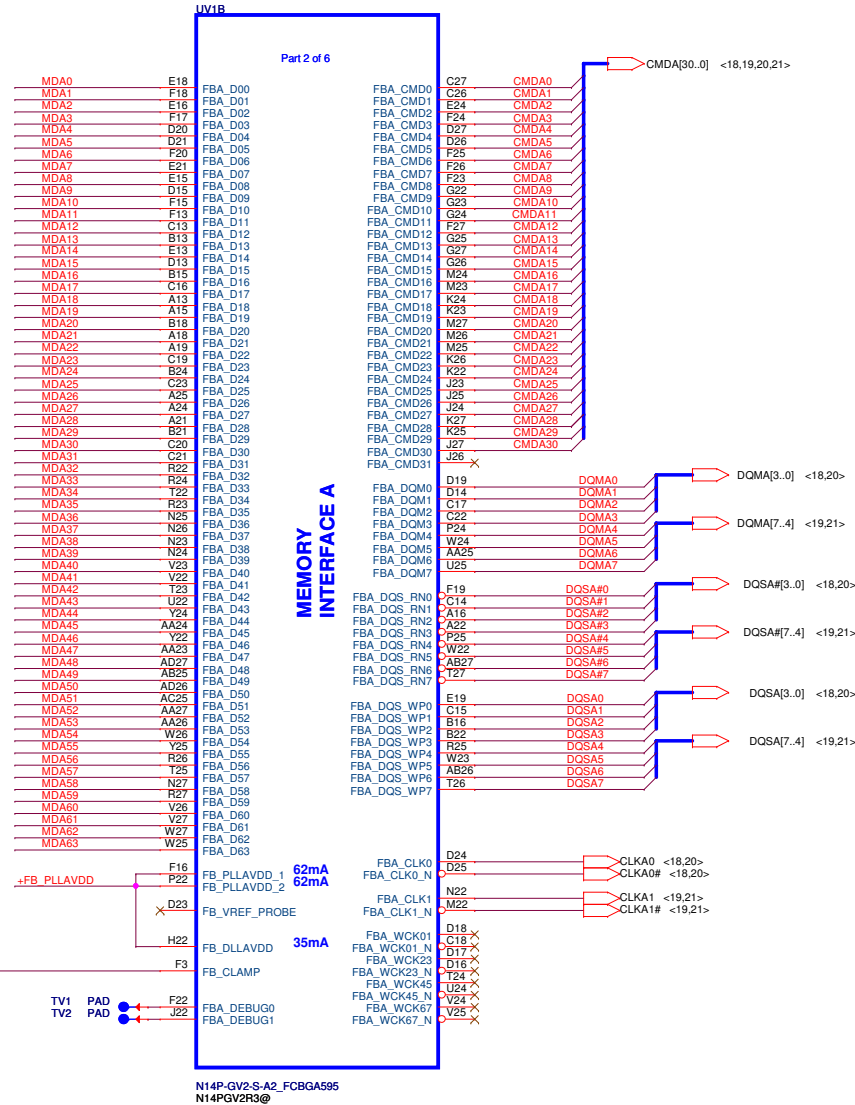
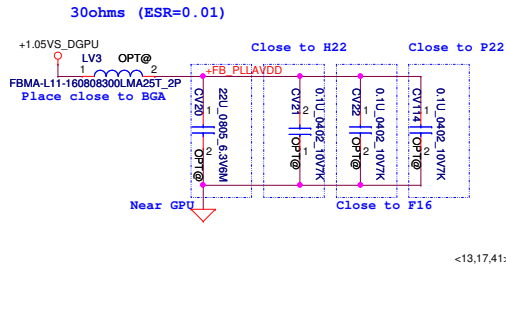
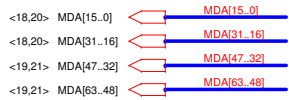
Layout Note:
Place near JDDRH.203 and 204

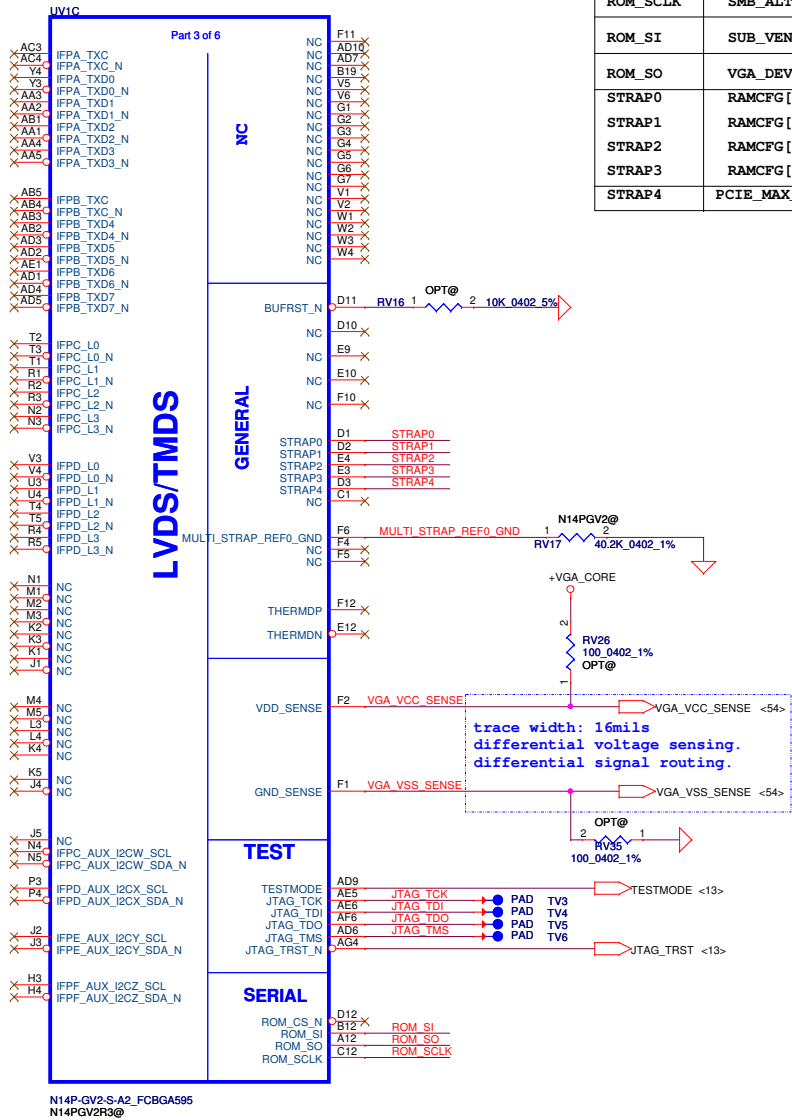


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VRAM Interface





N14P-GV2-S-A2_FCBGA595
N14PGV2R3@

BINARY STRAPS (for N14M-GL)

Strap Pin	Strap Mapping	
ROM_SCLK	SMB_ALT_ADDR	PD 10k
ROM_SI	SUB_VENDOR	PU 10k if VBIOS ROM exists PD 10k if no VBIOS ROM
ROM_SO	VGA_DEVICE	PD 10k (no display)
STRAP0	RAMCFG[0]	
STRAP1	RAMCFG[1]	Refer to RVL
STRAP2	RAMCFG[2]	
STRAP3	RAMCFG[3]	
STRAP4	PCIE_MAX_SPEED	PD 10k

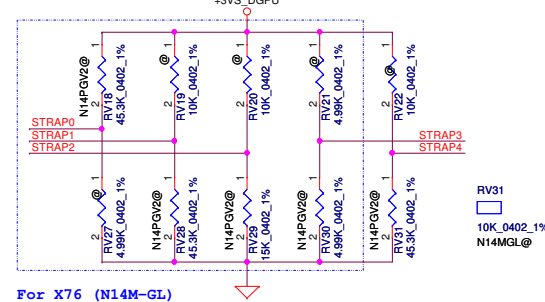
MULTI LEVEL STRAPS (for N14P-GV2)

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_DGPU	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_DGPU	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

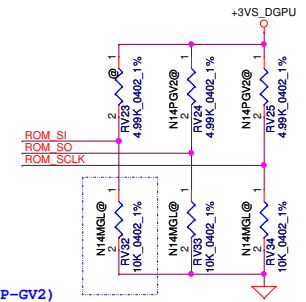
SKU	Device ID	biit5 to bit0
N14P-GV2	0x1292	010010
N14M-GL	0x1140	000000

Resistor Values	Pull-up to +3VS_DGPU	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

MULTI LEVEL STRAPS



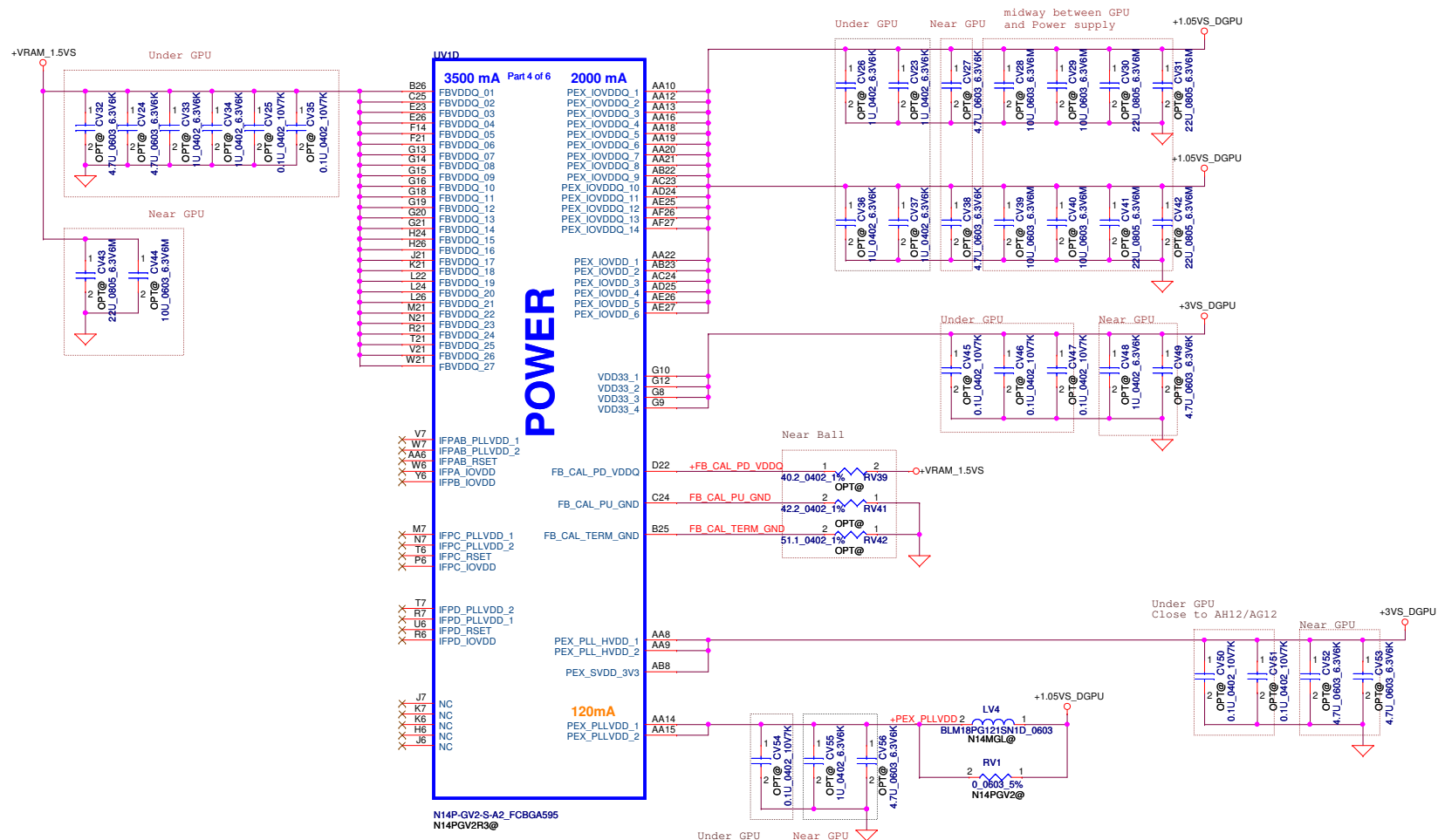
For X76 (N14P-GV2)



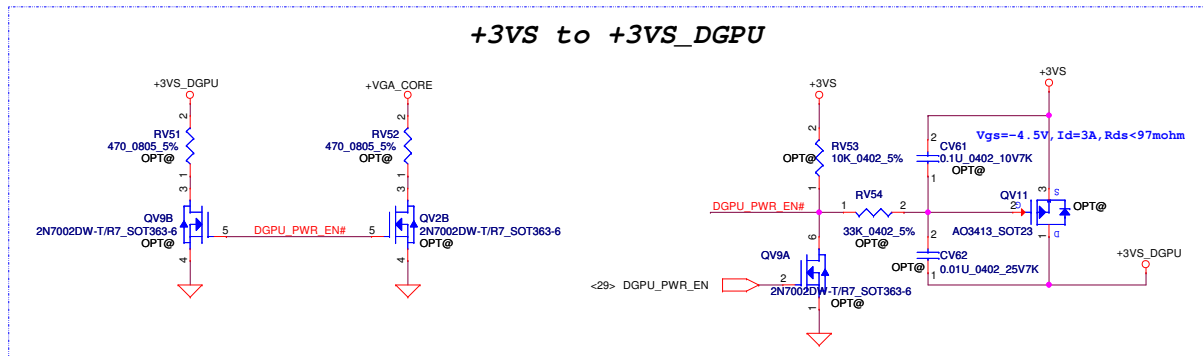
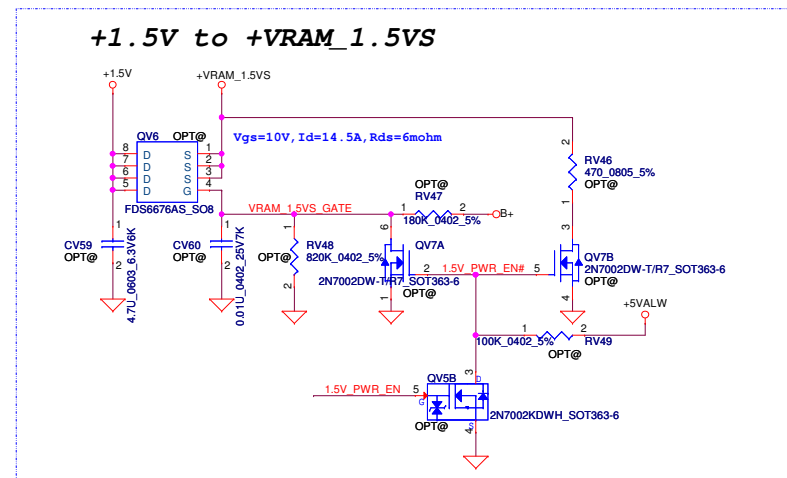
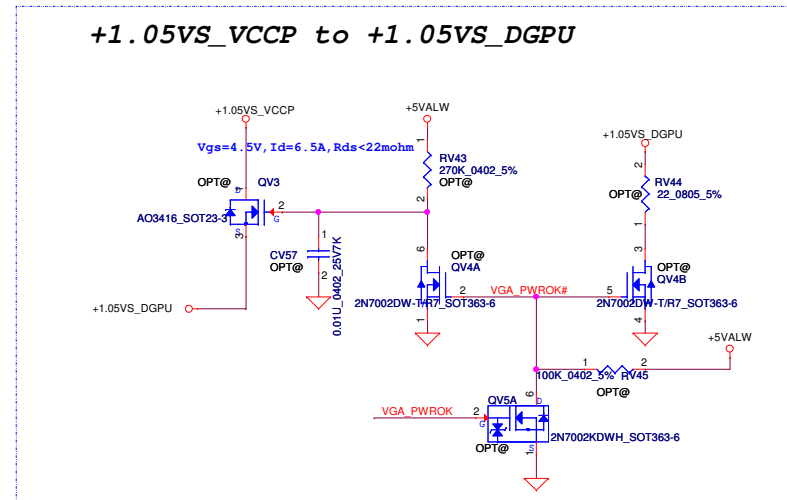
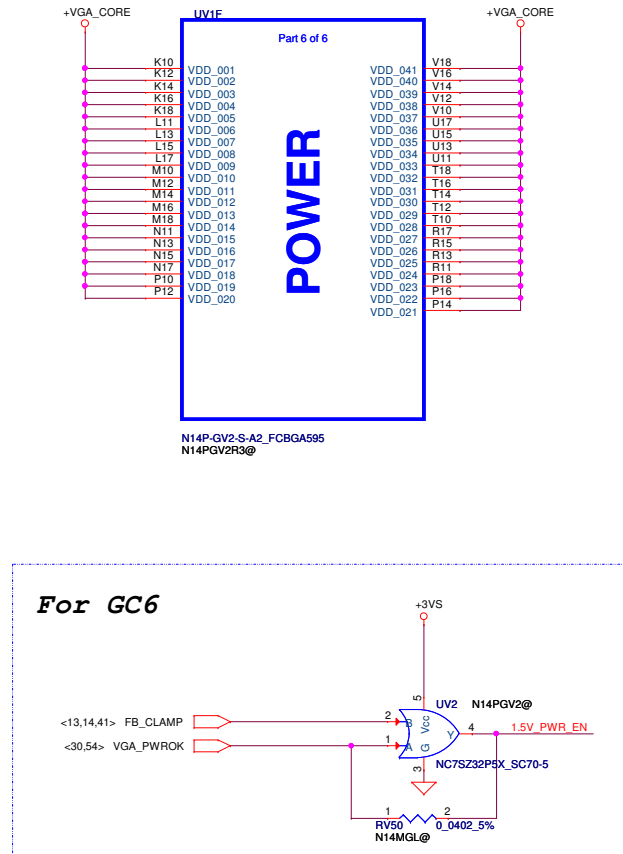
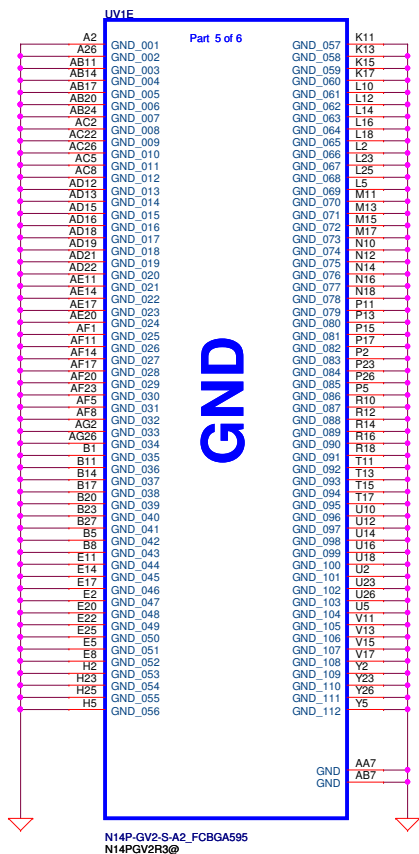
GPU	FB Memory gDDR3				ROM_SI	
N14P-GV2	1 2 8 M x 1 6	Samsung	900MHz	K4W2G1646E-BC11	PD 45.3K	
			1GHz	K4W2G1646E-BC1A		
		Hynix	900MHz	H5TQ2G63DFR-11C	PD 34.8K	
			1GHz	H5TQ2G63DFR-N0C		
		Micron	900MHz	MT41K128M16JT-107G	PD 30K	
		2 5 6 M x 1 6	Samsung	900MHz	K4W4G1646B-HC11	PD 20K
			Micron	900MHz	MT41K256M16HA-107G	PD 10K

GPU	FB Memory gDDR3			STRAP [3:0]
N14M-GL	1 2 8 M x 1 6	Samsung	900MHz K4W2G1646E-BC11	0101
			1GHz K4W2G1646E-BC1A	
		Hynix	900MHz H5TQ2G63DFR-11C	0110
			1GHz H5TQ2G63DFR-N0C	
		Micron	900MHz MT41K128M16JT-107G	0001
		2 5 6 M x 1 6	Samsung	900MHz K4W4G1646B-HC11
	Micron		900MHz MT41K256M16HA-107G	1101

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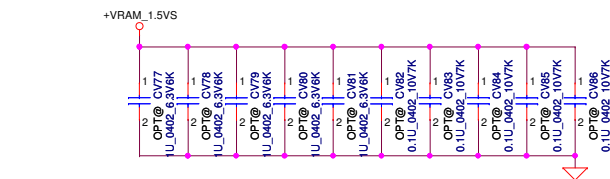
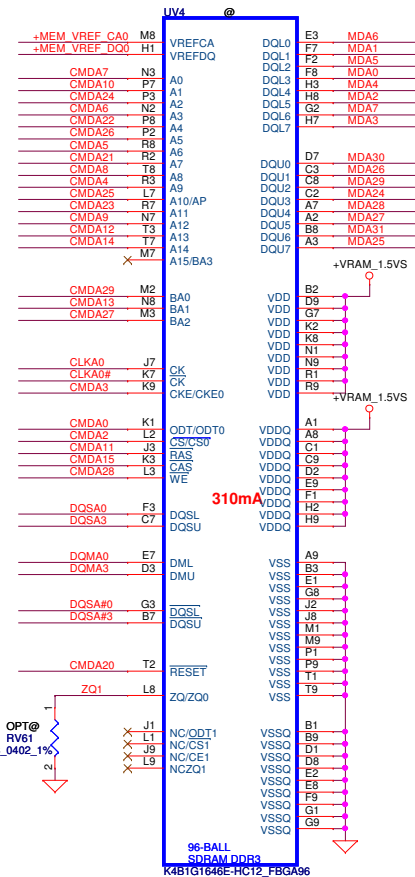
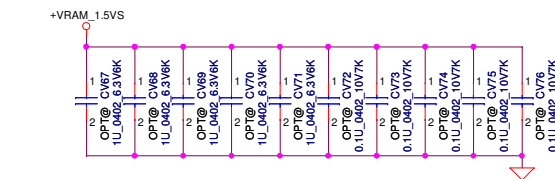
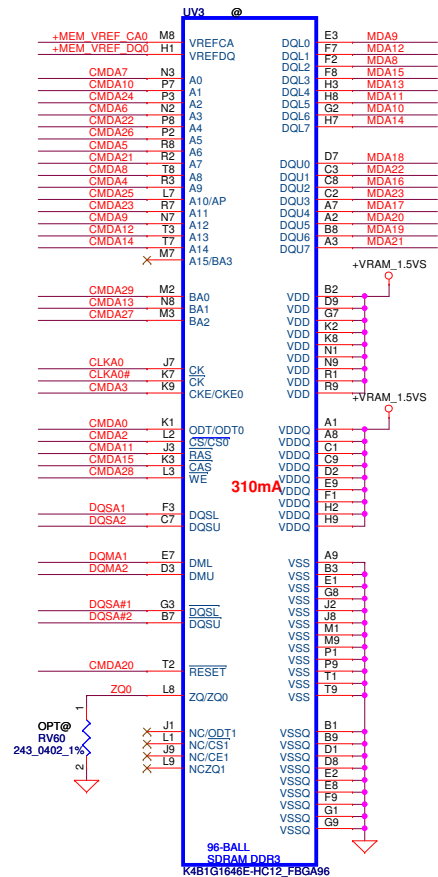
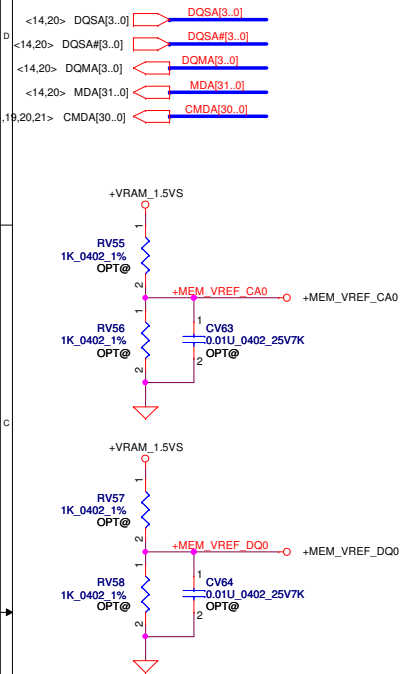


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Issued Date	2012/12/07	Deciphered Date	2013/12/07	VGA N14x POWER	
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Date: Monday, March 11, 2013				Sheet	16 of 56

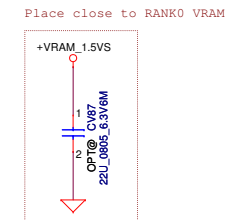
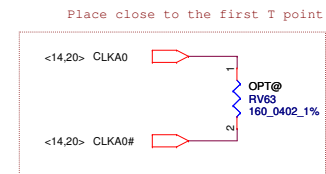


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Issued Date	2012/12/07	Deciphered Date	2013/12/07	Title
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				0.2
				Date: Monday, March 11, 2013
				Sheet 17 of 56

VRAM DDR3 Chips

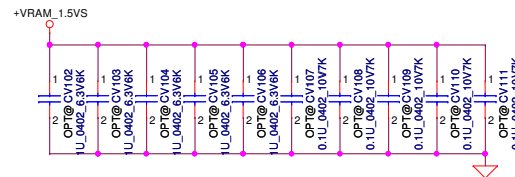
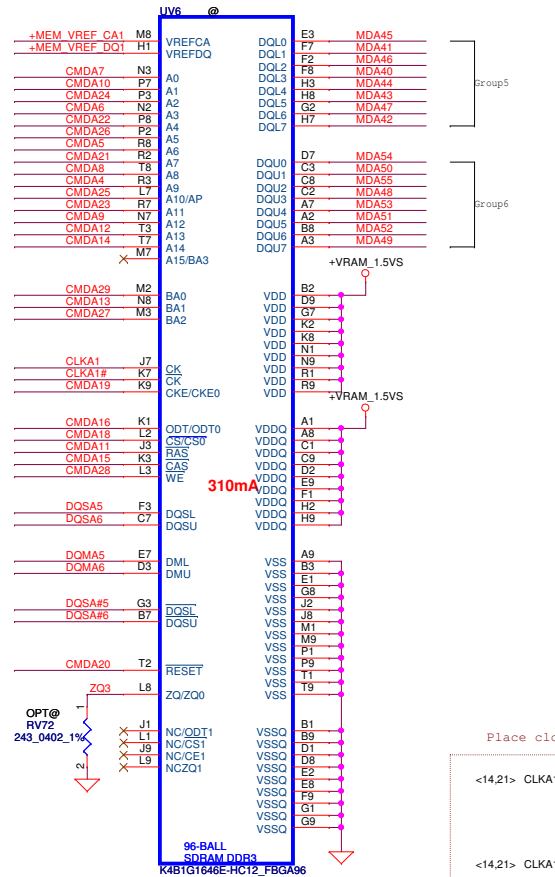
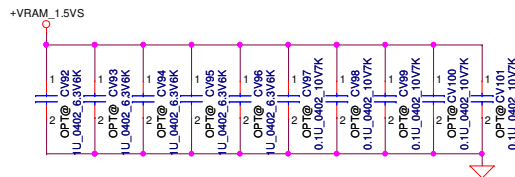
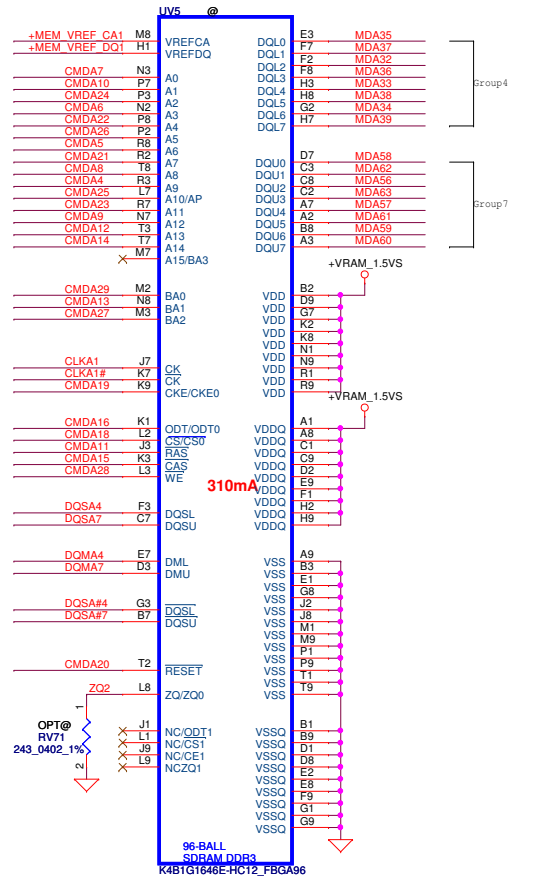
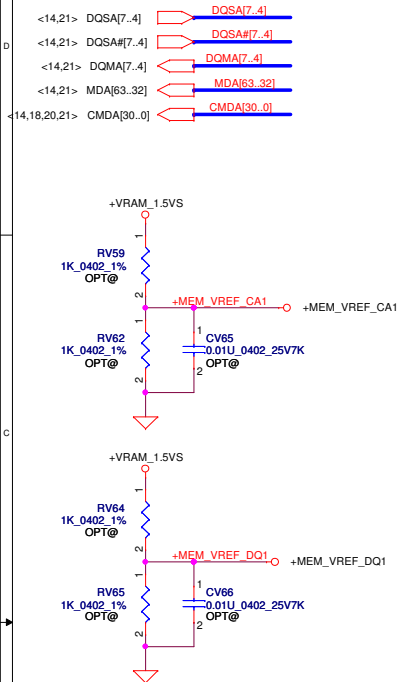


Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

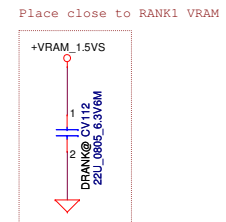
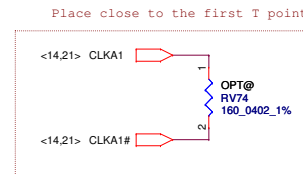


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/12/07	Deciphered Date	2013/12/07	Title	VGA N14x VRAM RANK 0L	
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				Date: Monday, March 11, 2013	Sheet	18 of 56

RANK 0 [63...32]

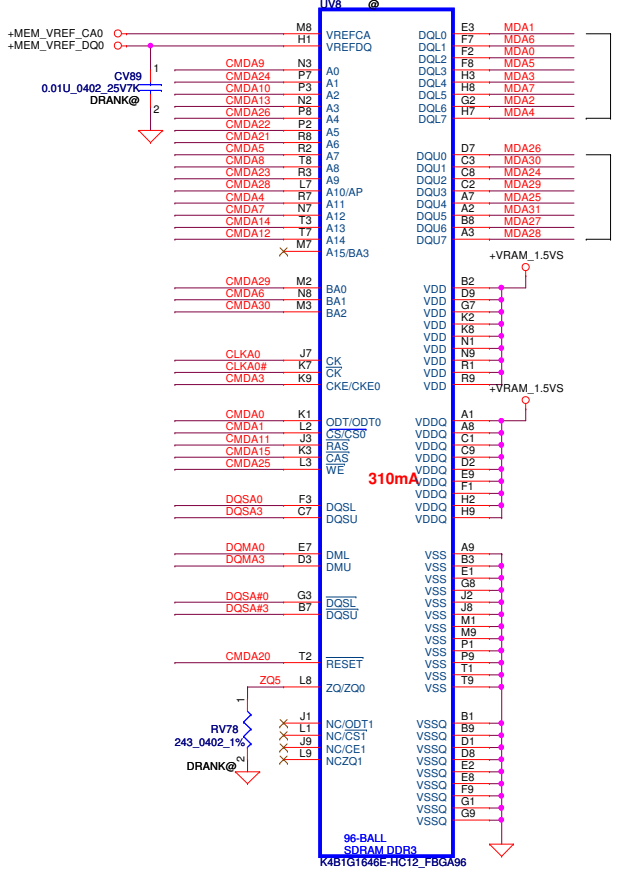
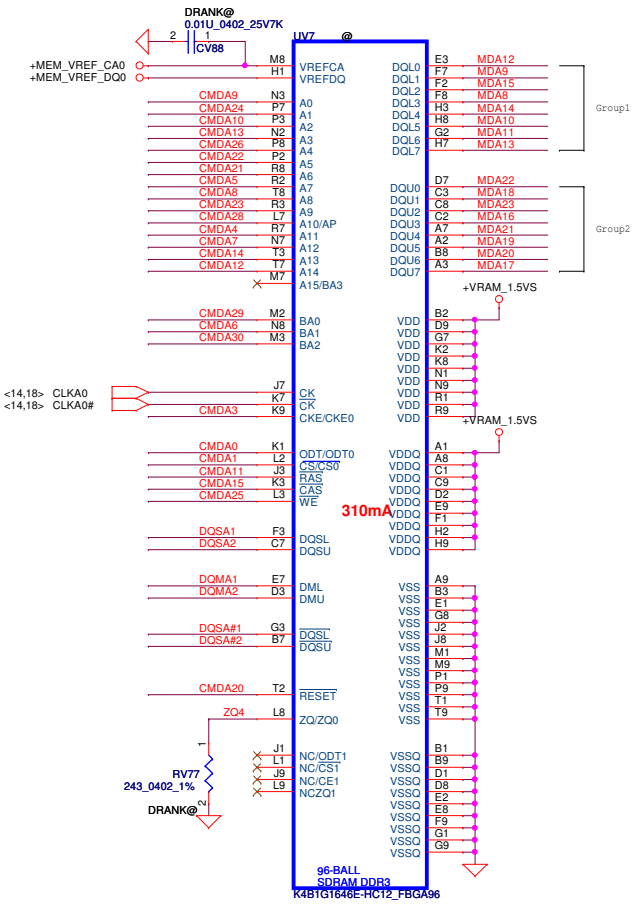
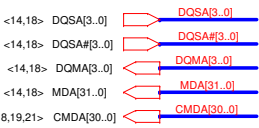


Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2



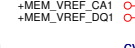
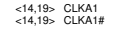
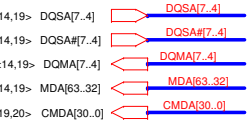
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Issued Date	2012/12/07	Deciphered Date	2013/12/07	Title	VGA N14x VRAM RANK 0H
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				Document Number	
				Date:	Monday, March 11, 2013
				Sheet	19 of 56
				Rev	0.2

RANK 1 [31...0]
VRAM DDR3 Chips



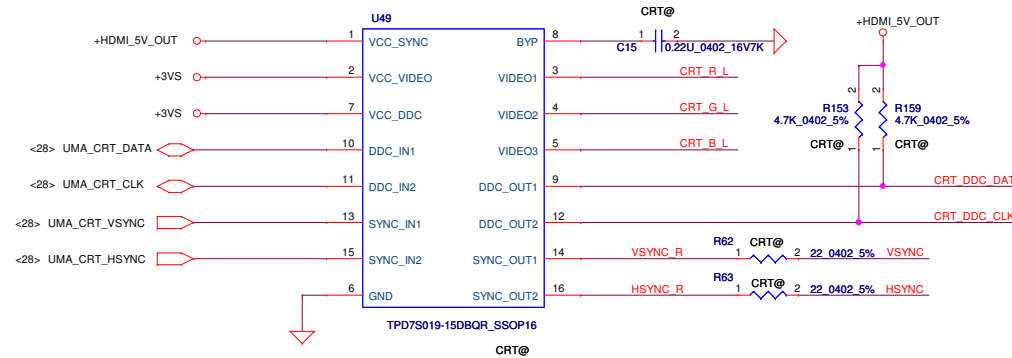
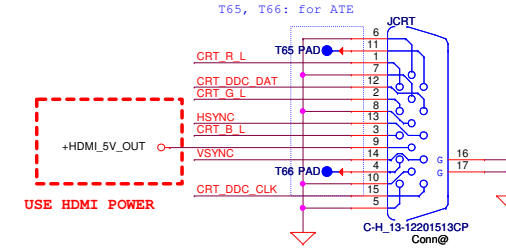
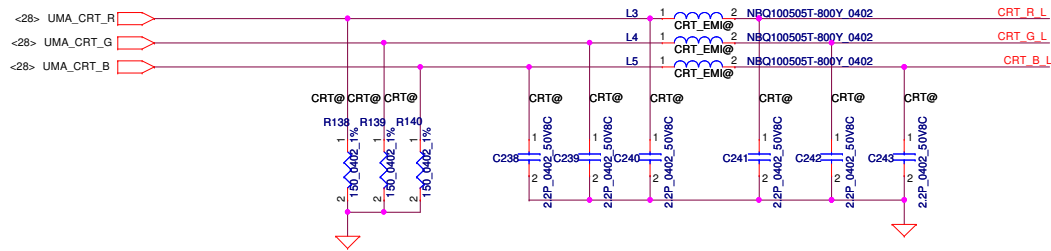
Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17			CS1#	
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

14,19> DQSA[7..4] → DQSA[7..4]
 14,19> DQSA#[7..4] → DQSA#[7..4]
 14,19> DQMA[7..4] → DQMA[7..4]
 14,19> MDA[63..32] ← MDA[63..32]
 19,20> CMDA[30..0] ← CMDA[30..0]

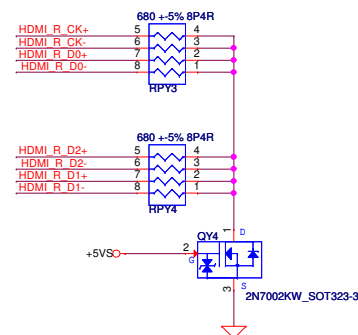
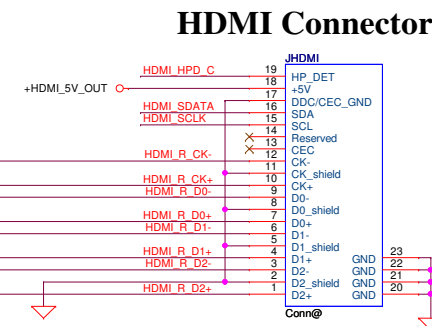
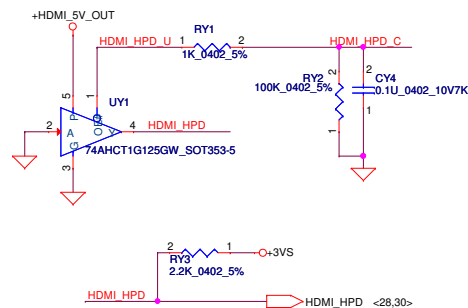
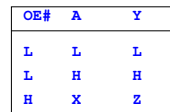


Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

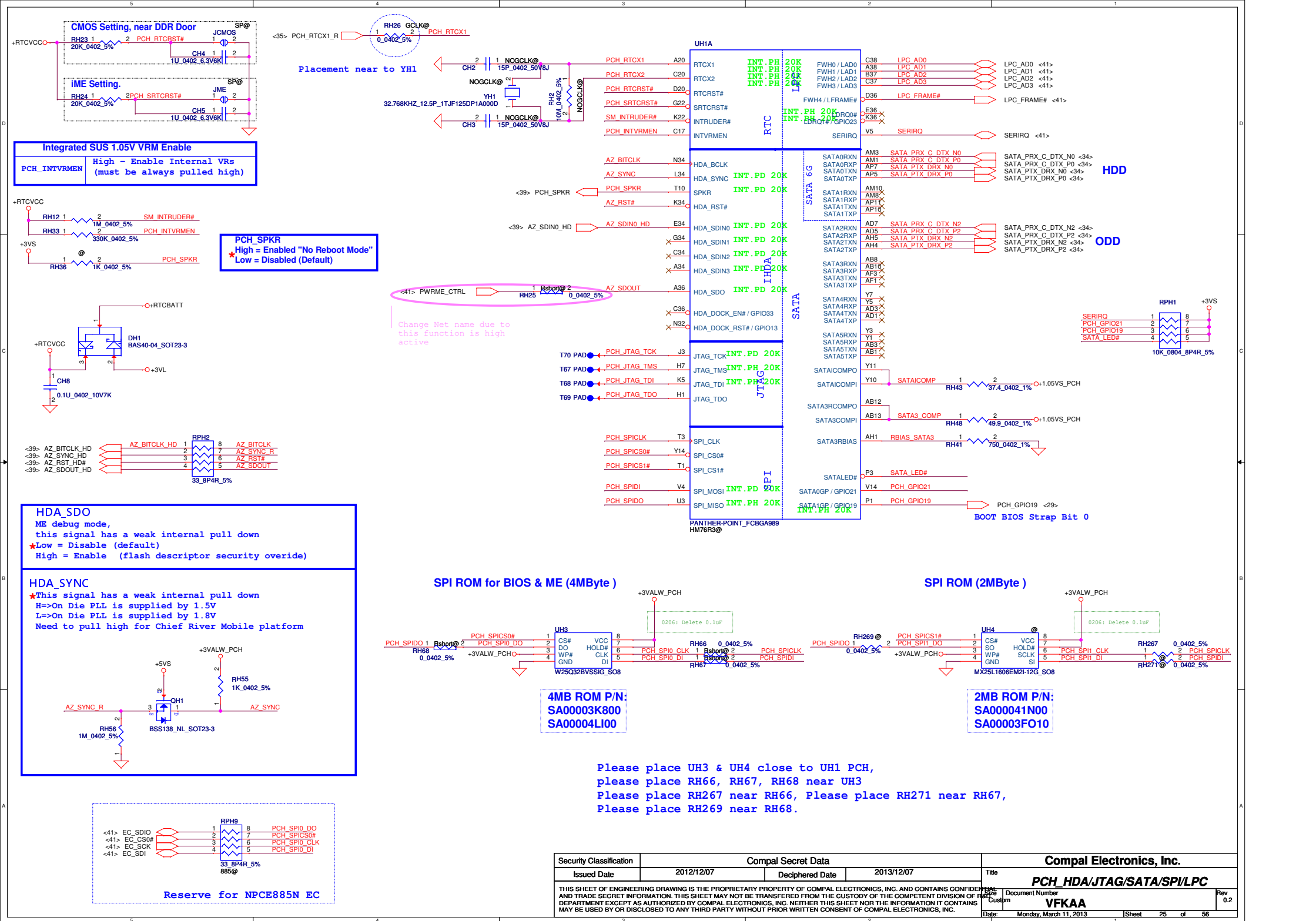
CRT CONNECTOR

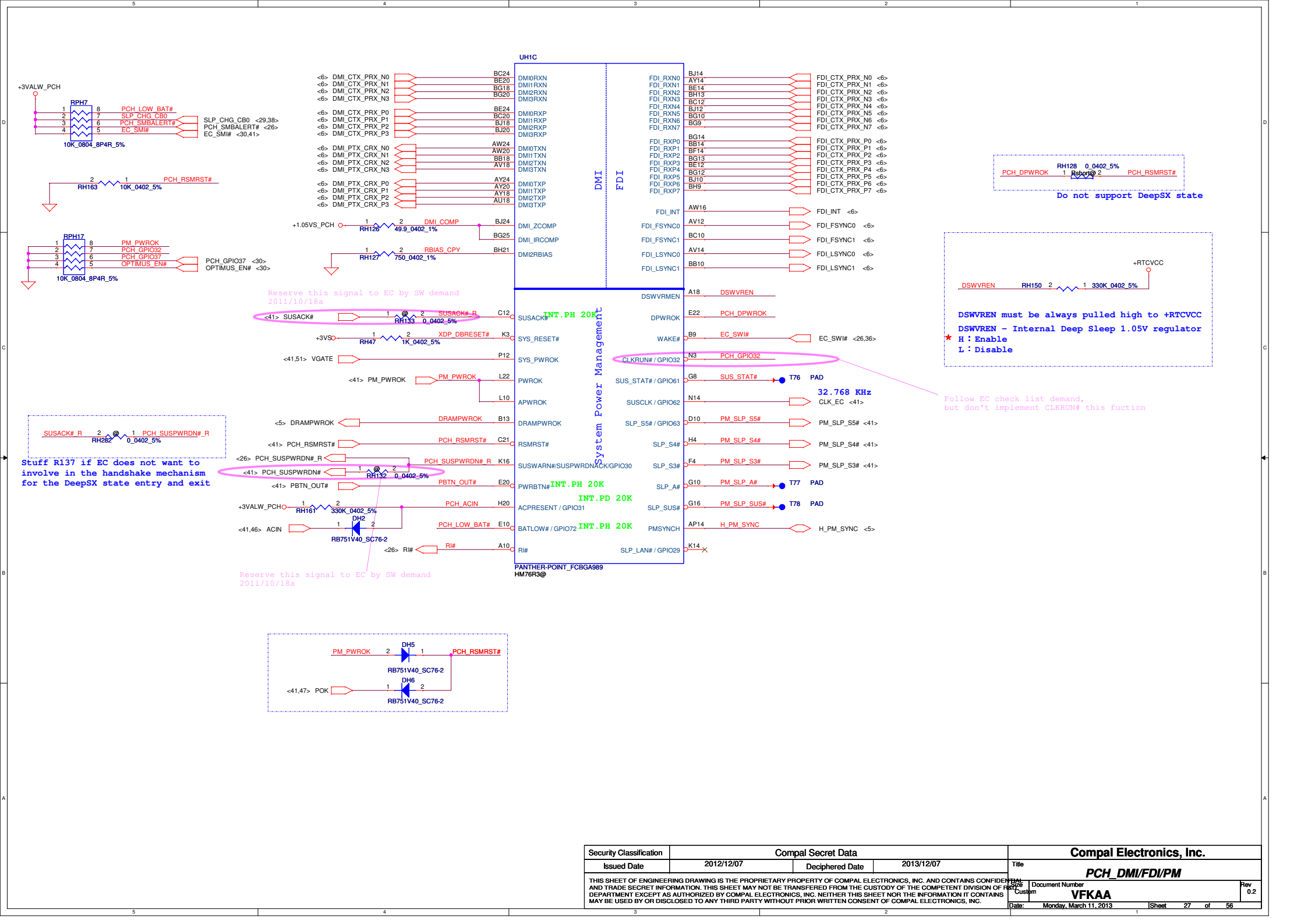


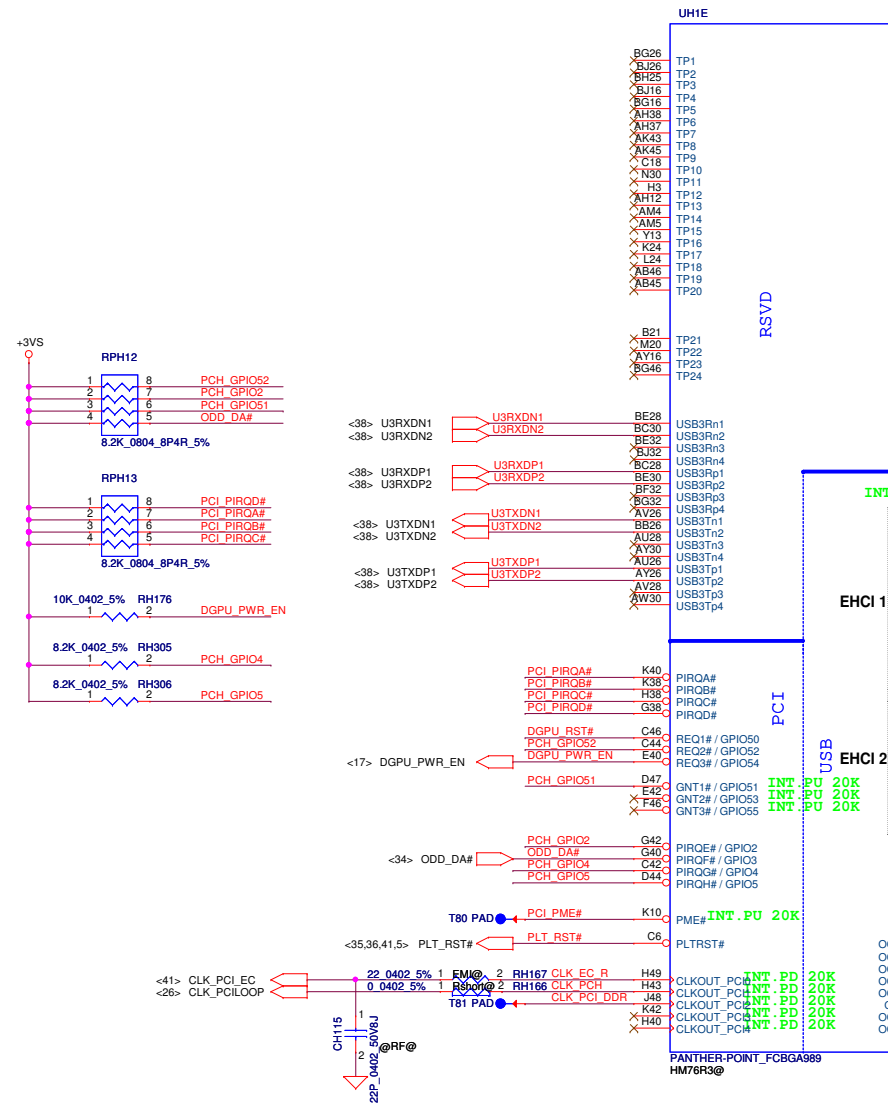
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2012/12/07	Deciphered Date	2013/12/07	Title	CRT		
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				Date:	Monday, March 11, 2013	Sheet	23 of 56



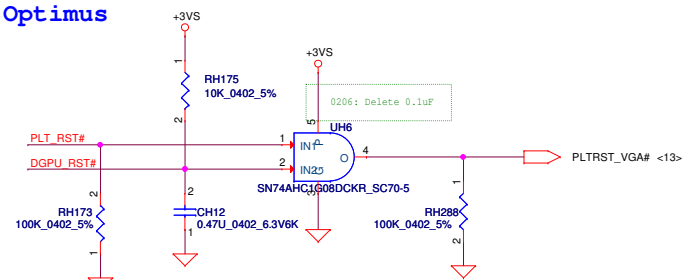
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Date:	Monday, March 11, 2013



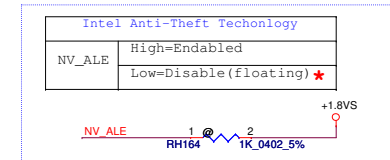




For Optimus

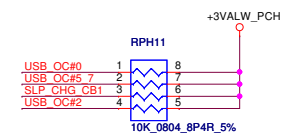


Note: HM70 only enable
USB port 0, 1, 2, 3, 8, 9, 10, 11



USB-Right1
USB-Right2
USB-Left
CardReader
Touch Screen
BT
Int. Camera

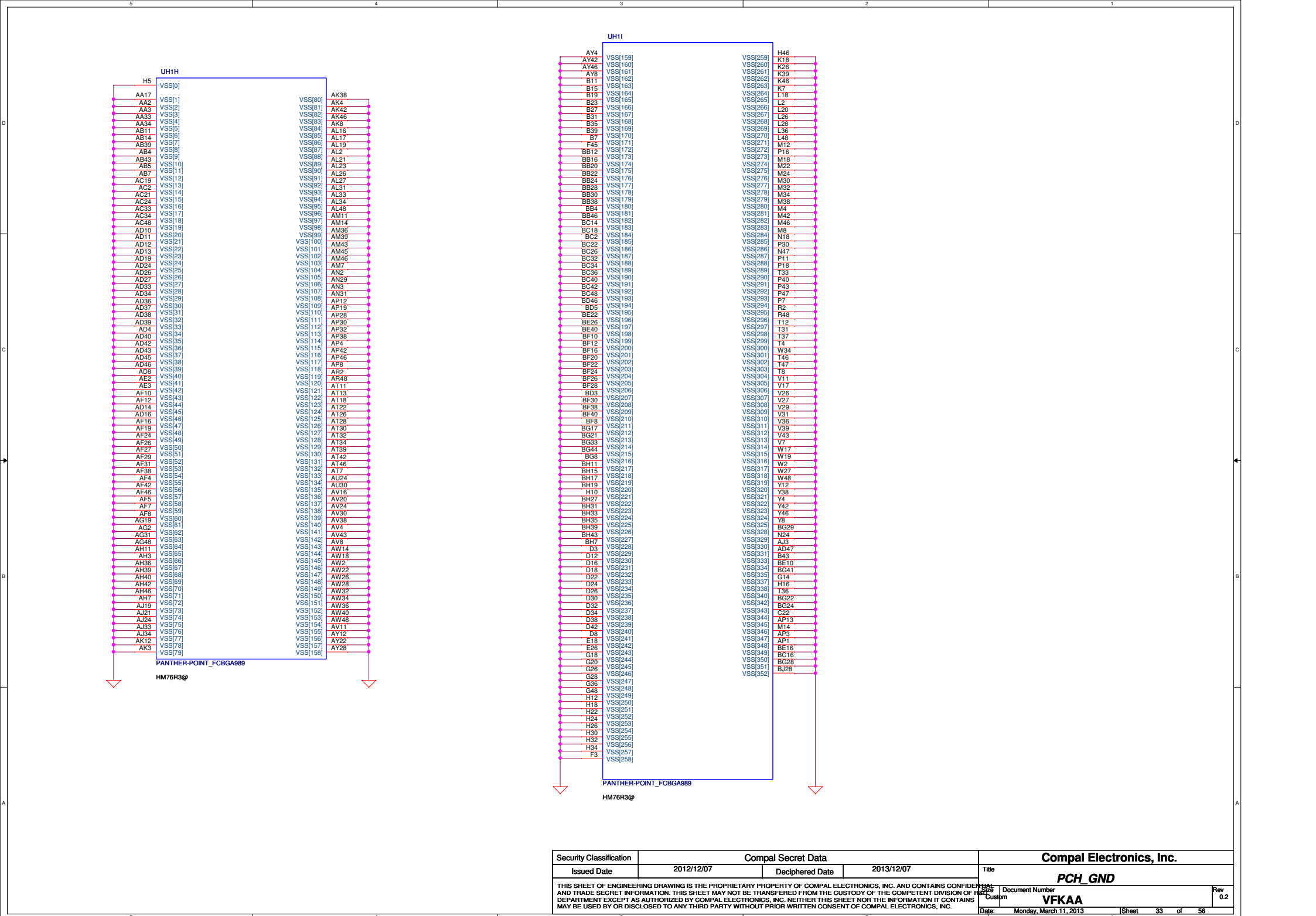
Within 500 mils



Boot BIOS Strap		
PCH_GPIO51	PCH_GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI ★

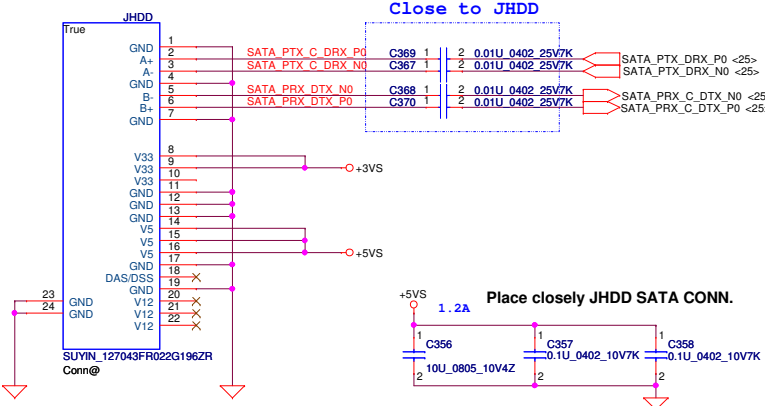
A16 Swap Override Strap	
WL_OFF#	
★	Low= A16 swap override Enable High= A16 swap override Disable

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				Deciphered Date				2013/12/07			
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				Date				Monday, March 11, 2013			
				Sheet				29 of 56			

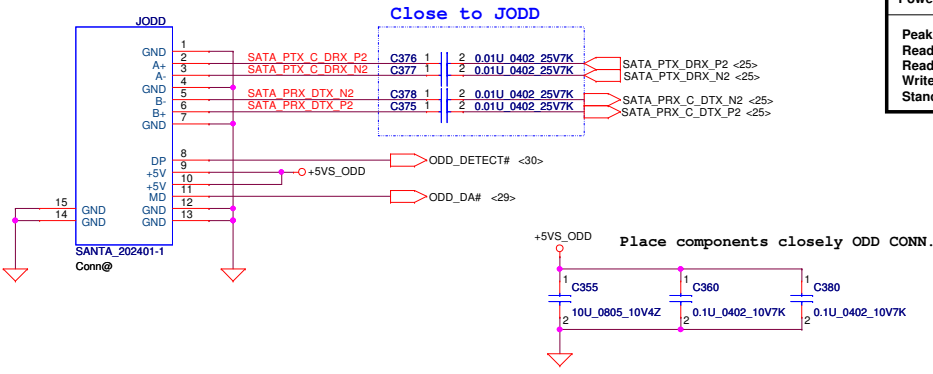


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				Date	Monday, March 11, 2013
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SATA HDD Conn.

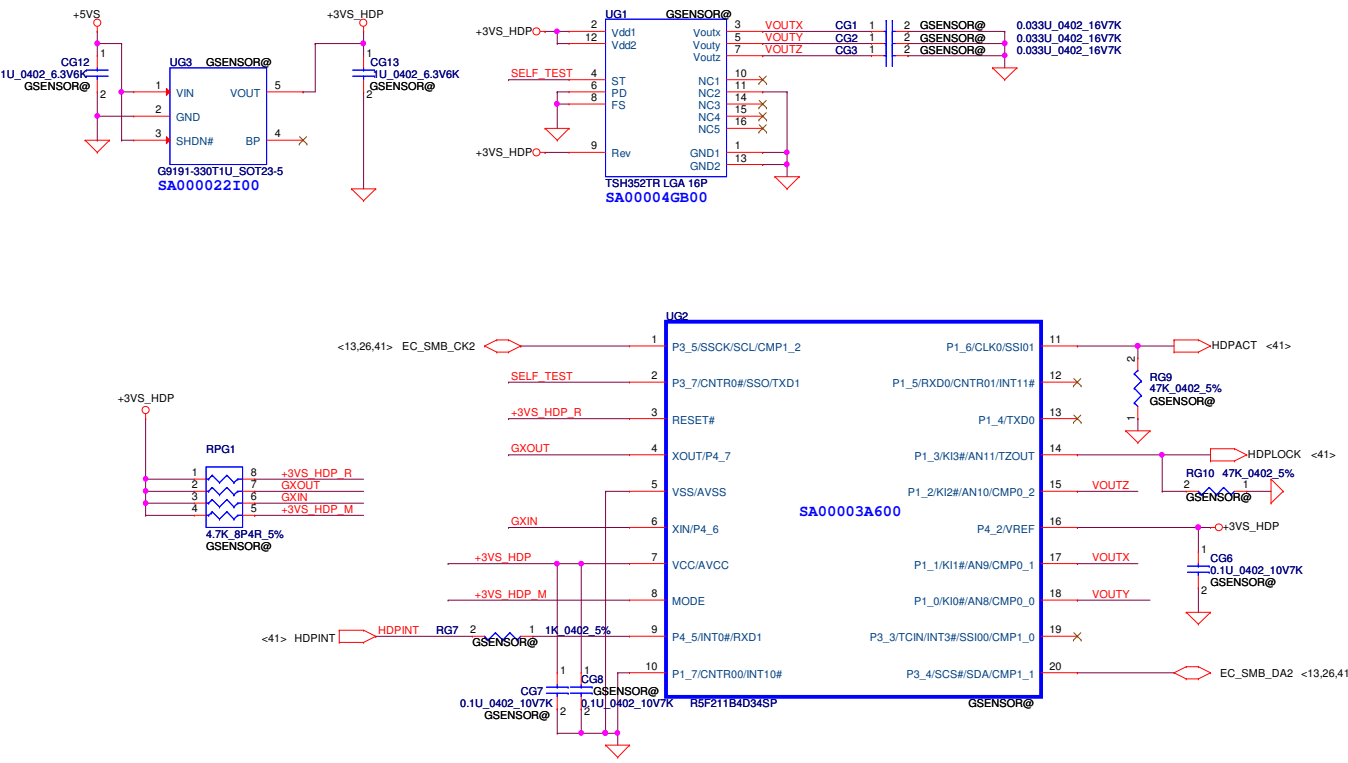


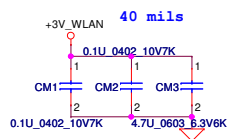
SATA ODD Conn



Power Consumption	
Peak	1800 mA
Read (CD)	1100 mA
Read (DVD)	950 mA
Write	1300 mA
Standby	20mA

G-Sensor



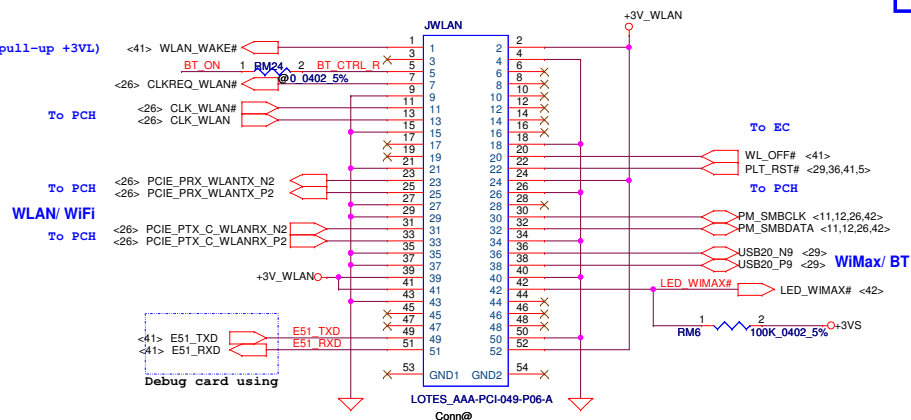
Slot 1 Half PCIe Mini Card-WLAN

	BT on module Enable	BT on module Disable
BT_ON	H	L

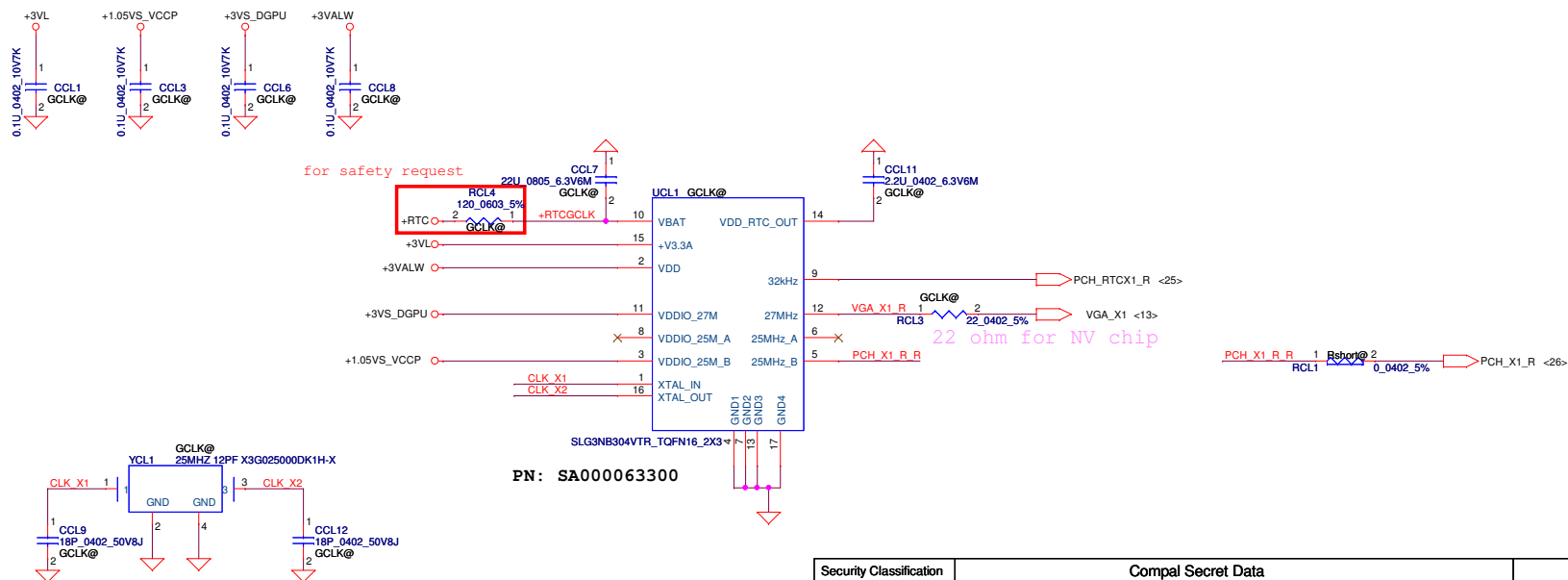
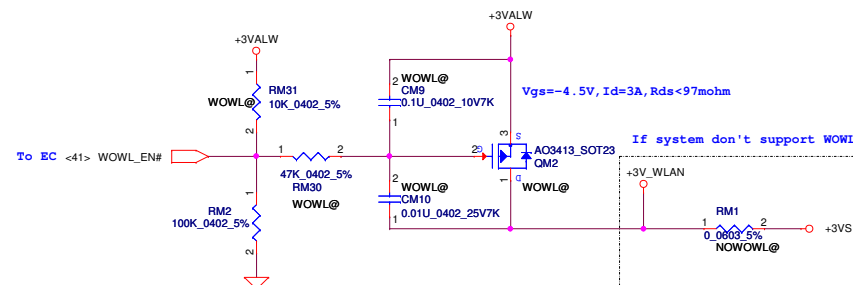
From EC

<41> BT_ON  BT_ON 1 RM27 2 E51_RXD
1K_0402 5%

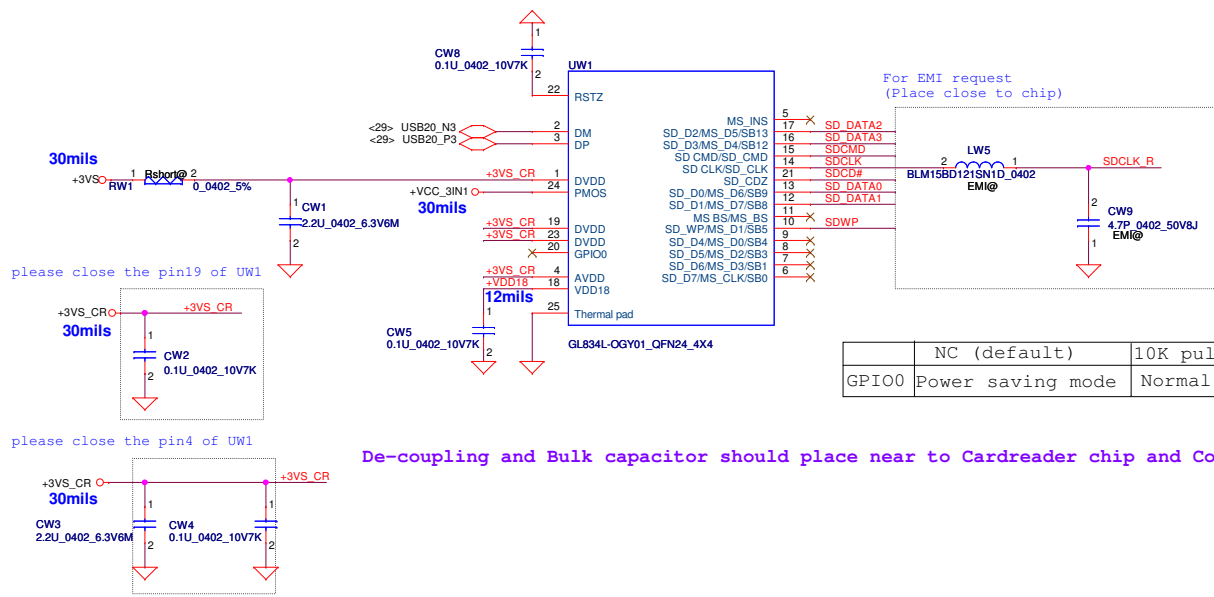
For isolate BT_ON and
Compal Debug Card.



+3VALW TO +3V WLAN for WOWL

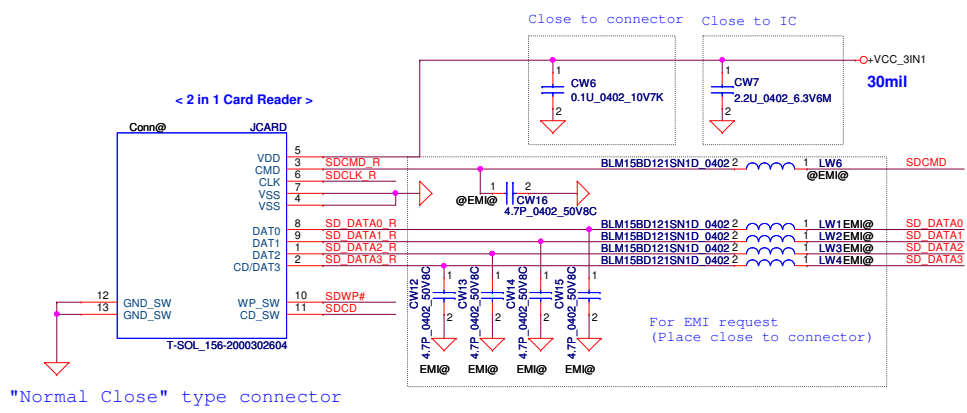


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								Date:		Monday, March 11, 2013	
								Rev		0.2	

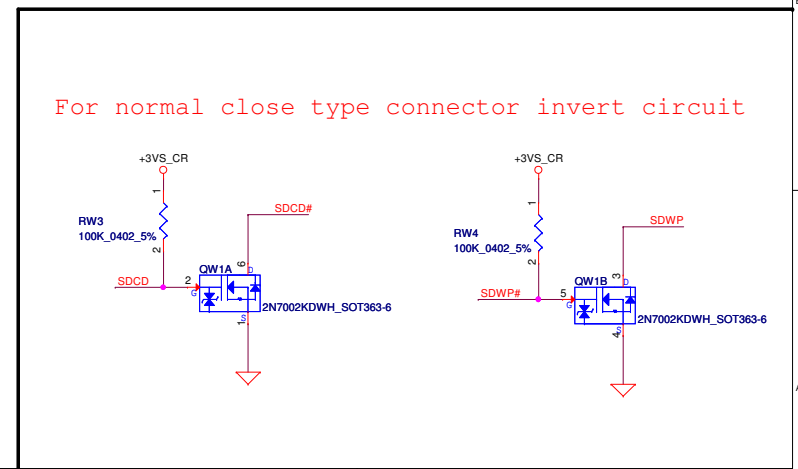


	NC (default)	10K pull down
GPI00	Power saving mode	Normal mode

De-coupling and Bulk capacitor should place near to Cardreader chip and Combo Socket

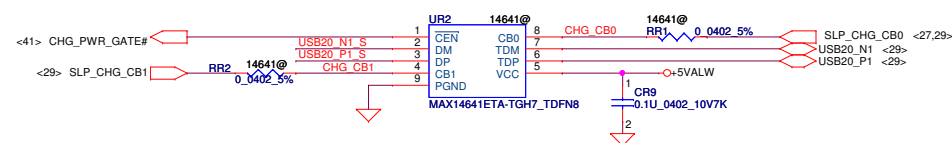


	CD_SW	WP_SW	
Card Uninsertion	Close	Protect disable	Protect Enable
		Close	Close
Card Insertion	Open	Open	Close

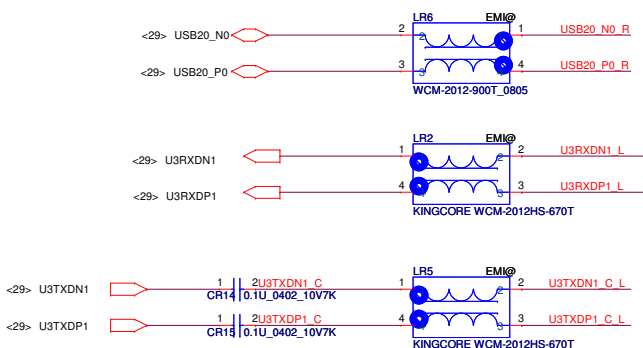


USB Sleep & Charge

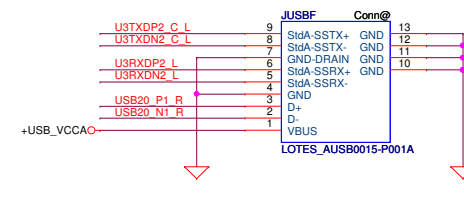
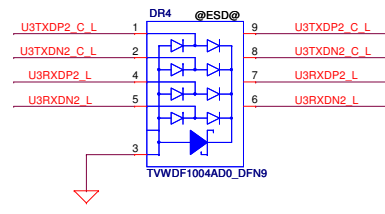
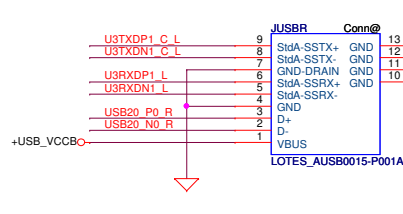
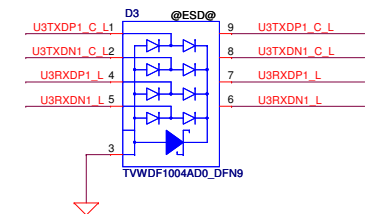
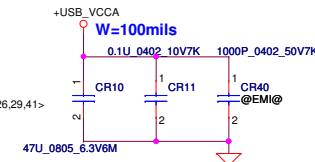
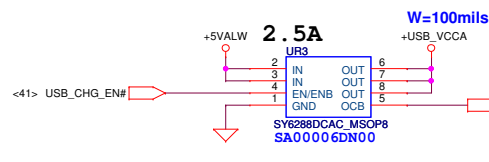
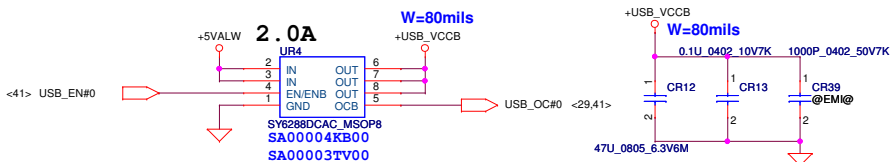
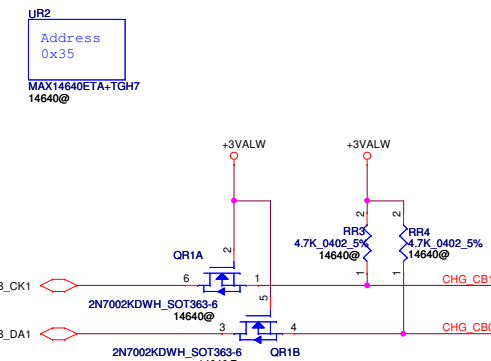
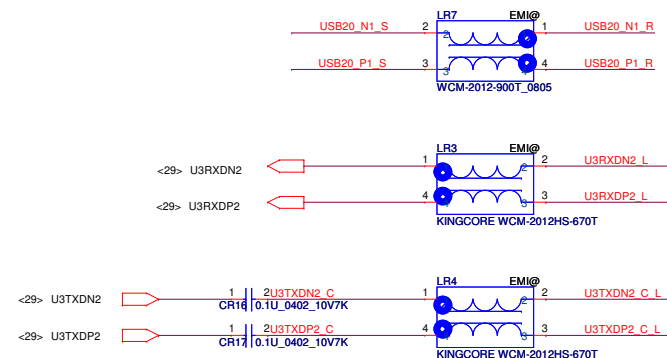
State table for MAX14641			
CB0	CB1	Mode	STATUS
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.



Right rear USB3.0 Conn.



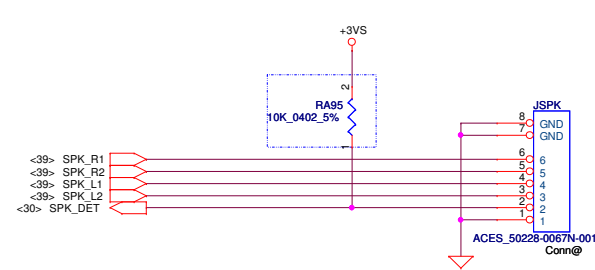
Right front USB3.0 Conn. (Support S&C function)



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Date: Monday, March 11, 2013				Sheet	38 of 56

SPK Conn.

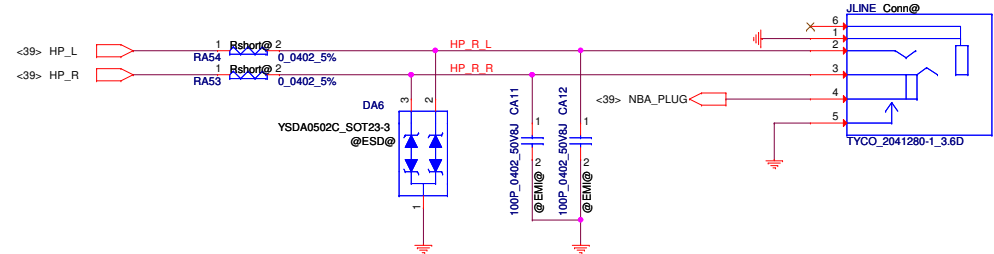
For common design,
pull-high resistor should be placed at connector side.



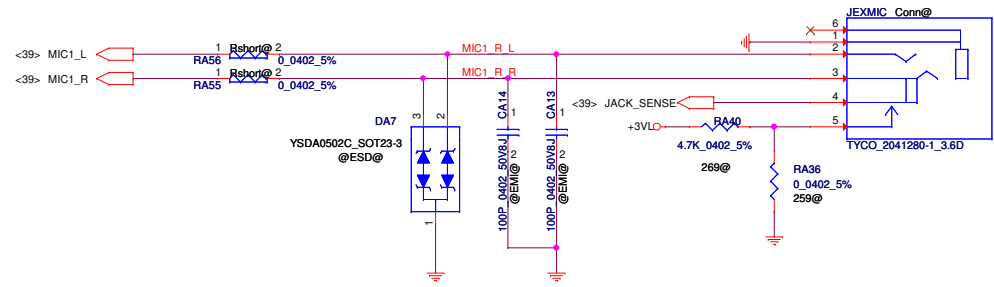
SM_DET (GPIO48)	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	269@
0		Non Harman	259@

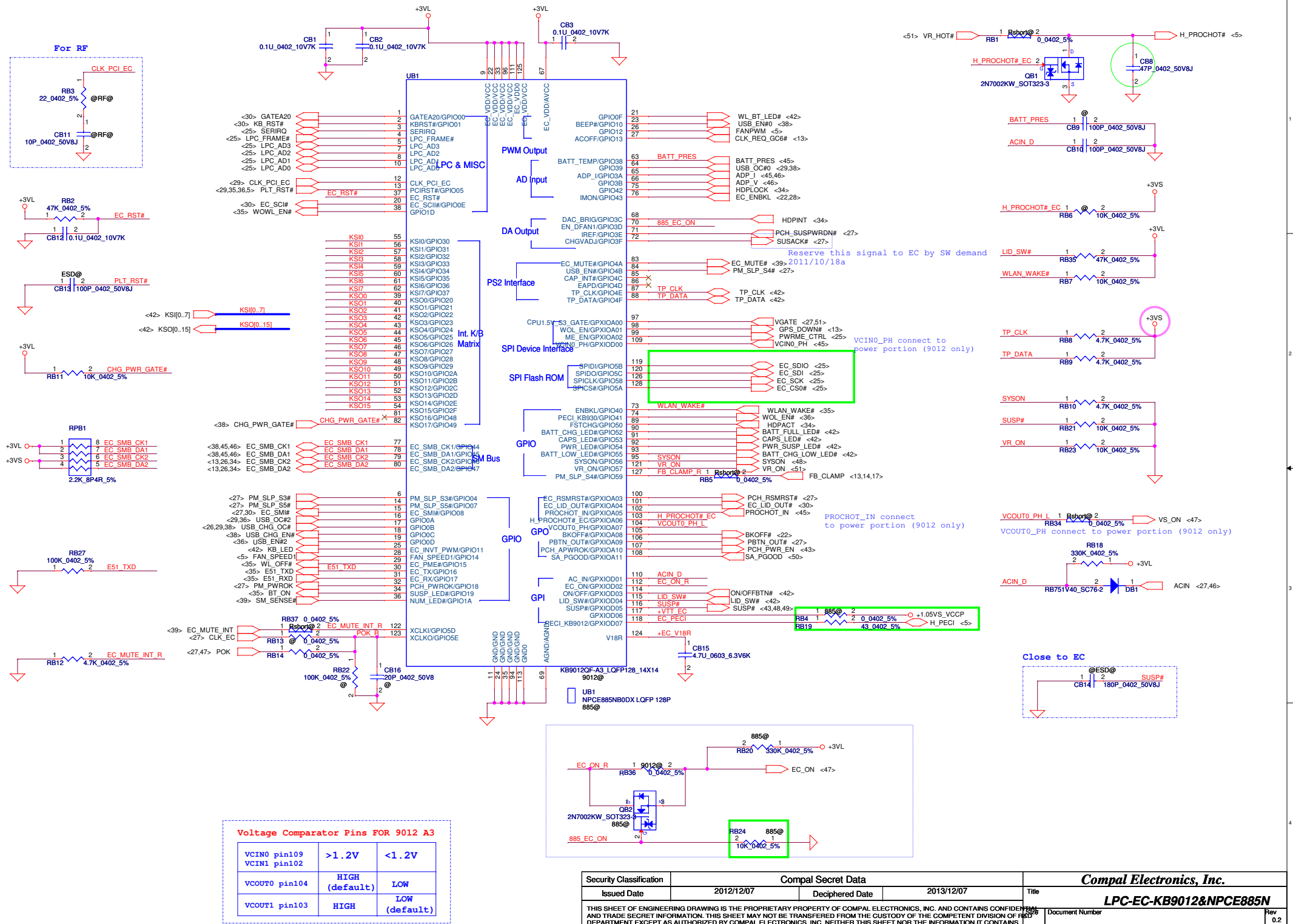
Non-Harman detection		
SPK_DET (GPIO70)	0	ONKYO
	1	Non-Brand

HeadPhone/LINE Out JACK



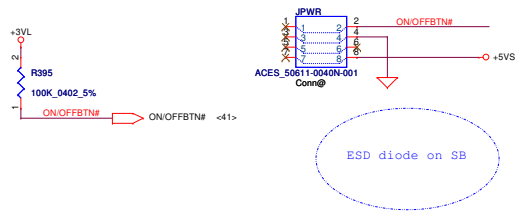
MIC/LINE IN JACK



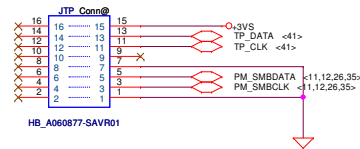


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				Date:	Monday, March 11, 2013	Sheet 41 of 56

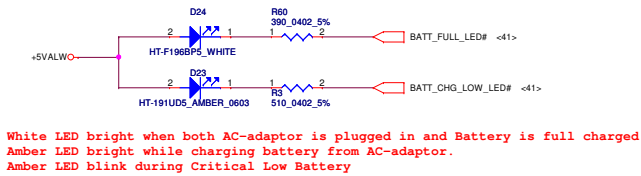
Power Button Conn.



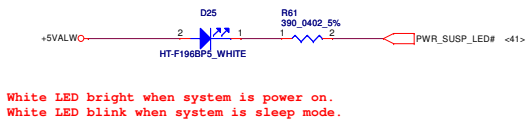
Touchpad Connector



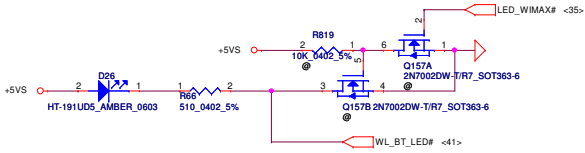
BATT CHARGE /FULL LED



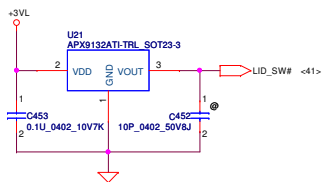
POWER LED



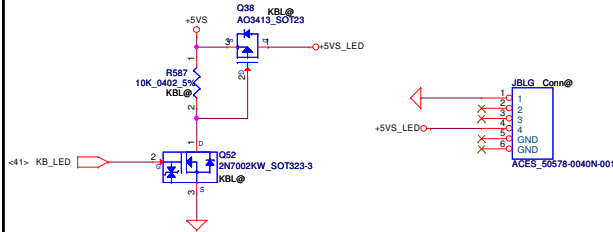
WLAN/WiMAX LED



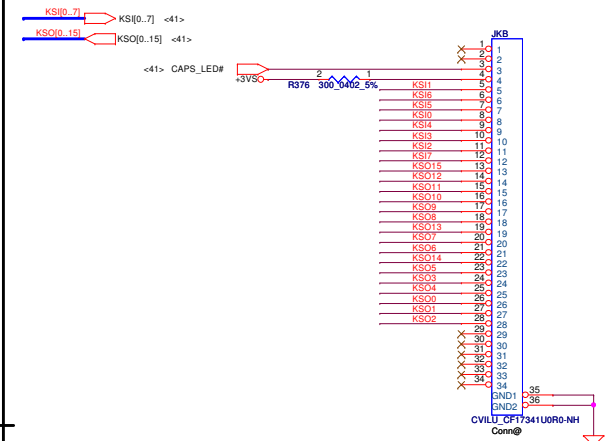
Lid SW



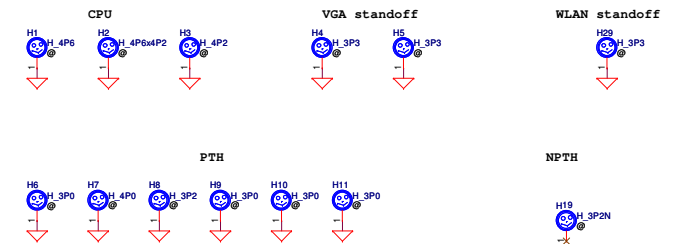
Keyboard LED



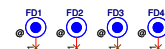
KEYBOARD CONN.



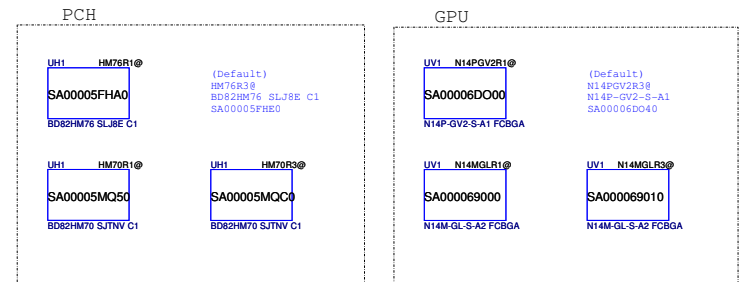
Screw Hole



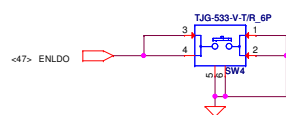
PCB Federal Mark PAD



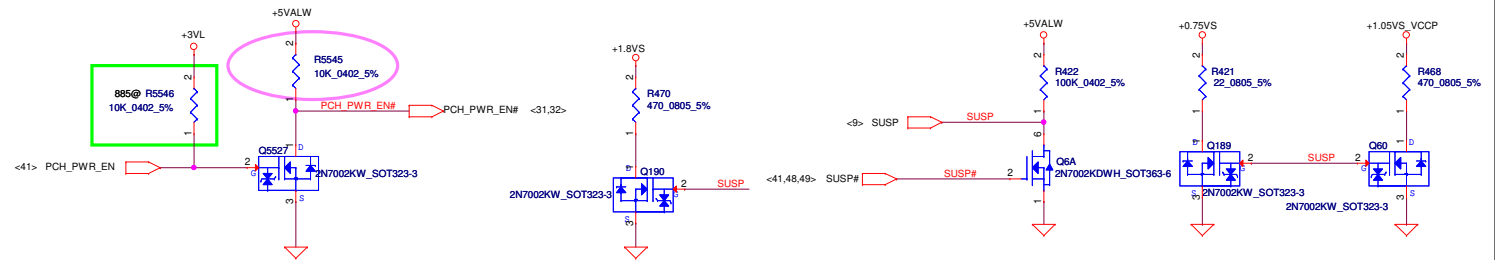
ISPD



EC Reset



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TP/ISPD/KB/LED/Screw VFKAA				Date: Monday, March 11, 2013 Sheet 42 of 56



<4B,50> VCCP_PWRGOOD

1 2

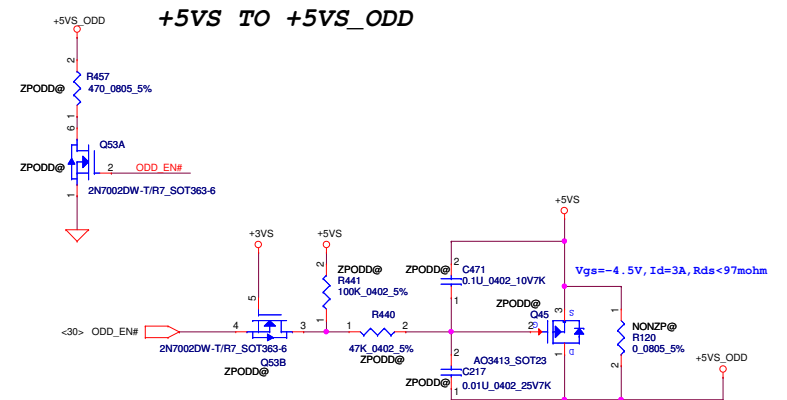
R15B 220K_0402_5%

0.75VR_EN

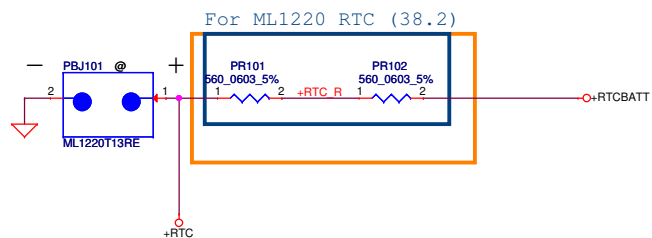
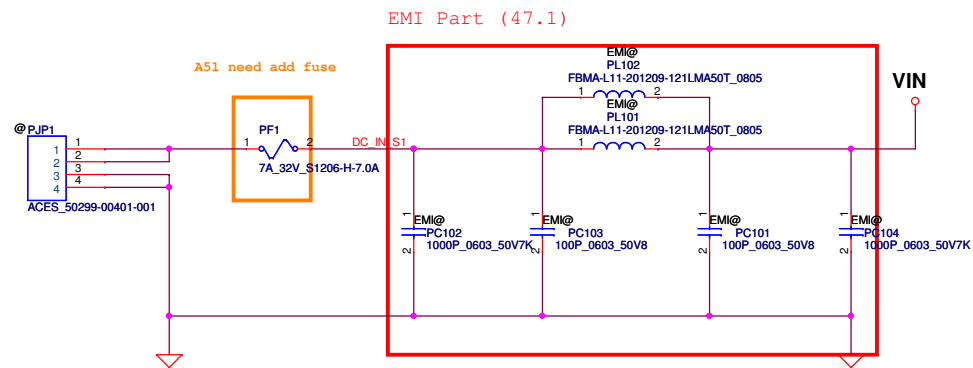
0.75VR_EN <4B>

SUSP 5

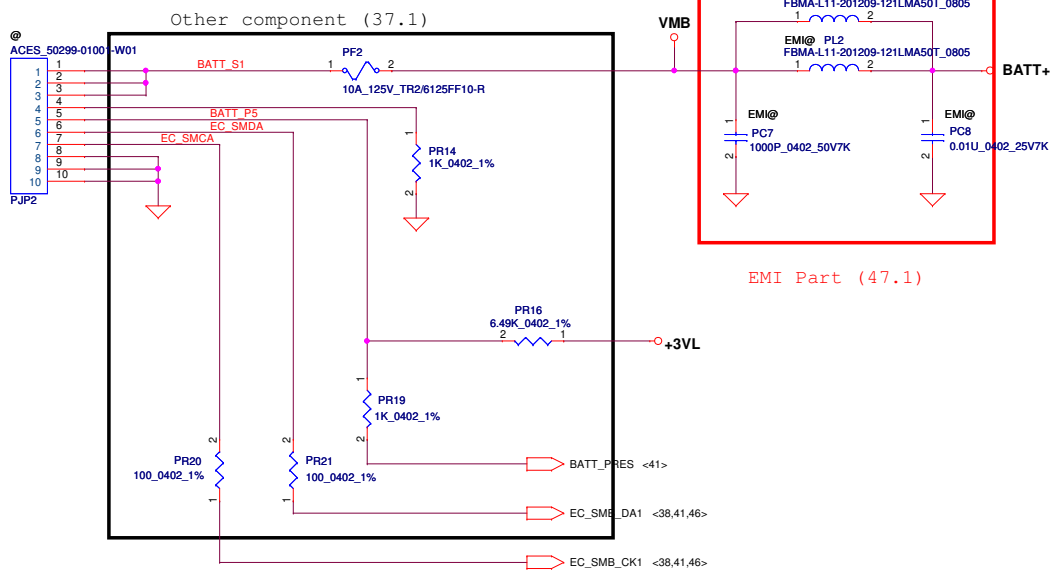
Q6B 2N7002KDW_H_SOT363-6



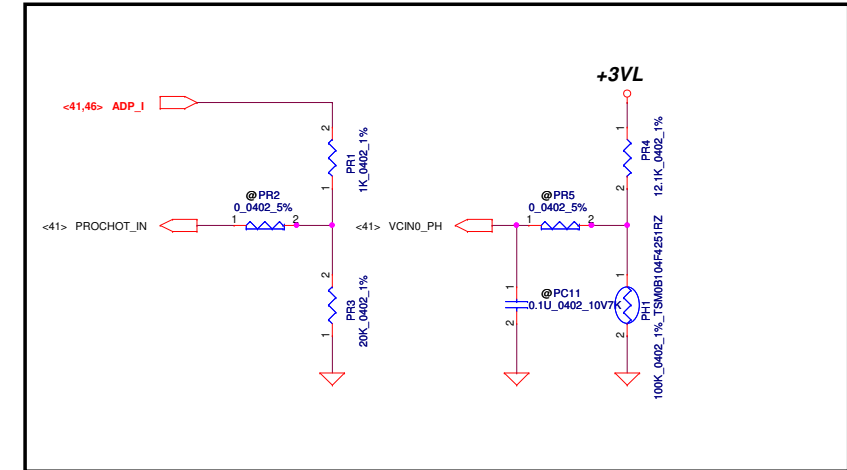
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/12/07	Deciphered Date	2013/12/07	Title	DC-DC INTERFACE	
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Issued Date	2012/09/24	Deciphered Date	2013/09/24	Title	DCIN/PRECHARGE
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OTP (39.7)



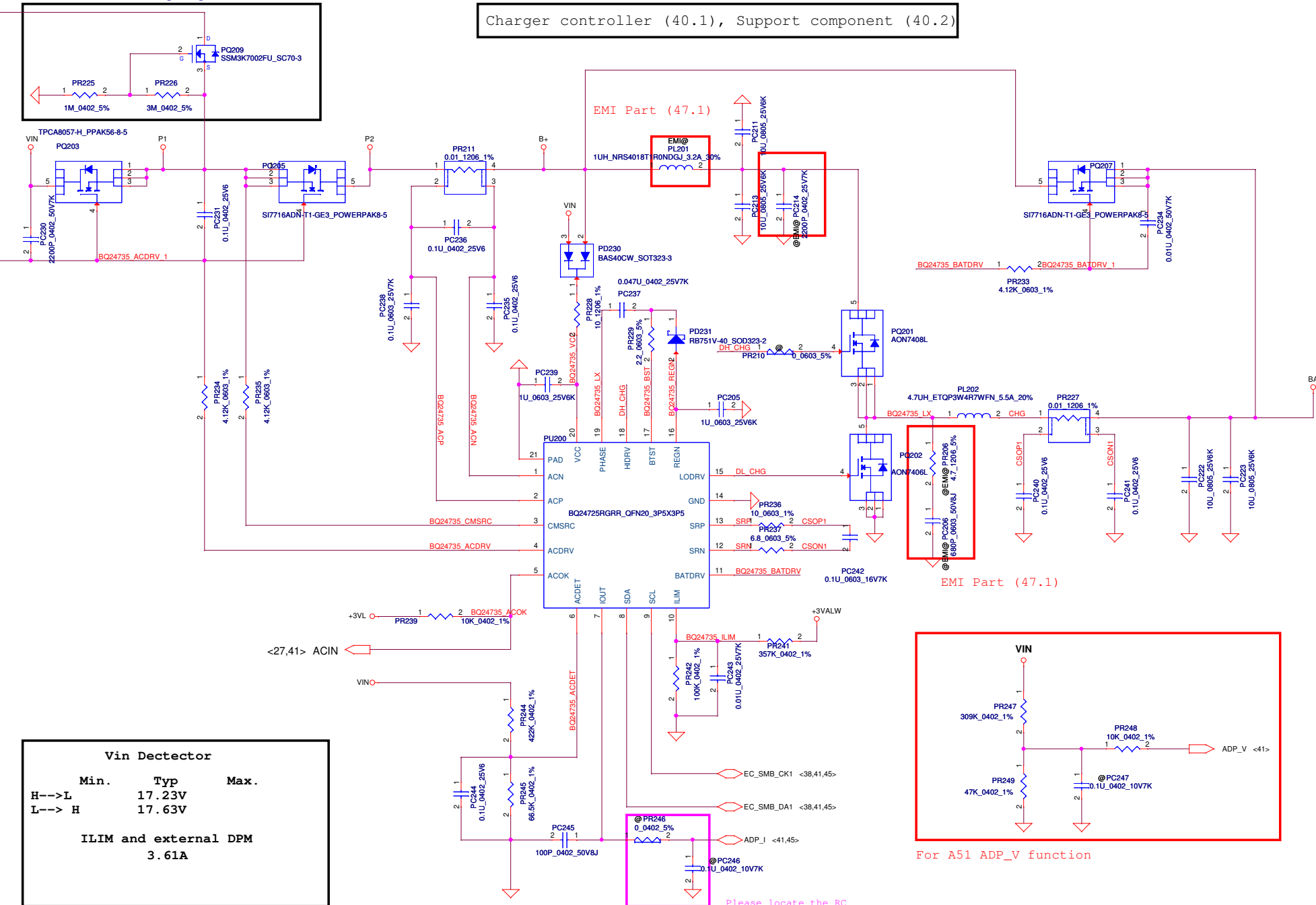
PH1 under CPU bottom side :
CPU thermal protection at 93 $\pm$ 3 degree C
Recovery at 56 $\pm$ 3 degree C

	Initial	Protect	Recovery
65W	0.75V	0.752V	0.626V
75W	0.9V	0.902V	0.722V

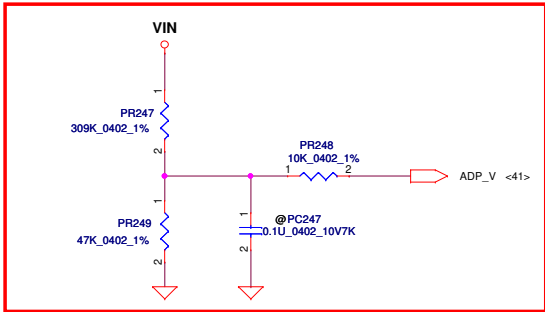
	Initial	Protect	Recovery
CPU OTP	65W	93 C	56 C

for reverse input protection

Charger controller (40.1), Support component (40.2)



Vin Detector			
Min.	Typ	Max.	
H-->L	17.23V		
L-->H	17.63V		
ILIM and external DPM			
3.61A			



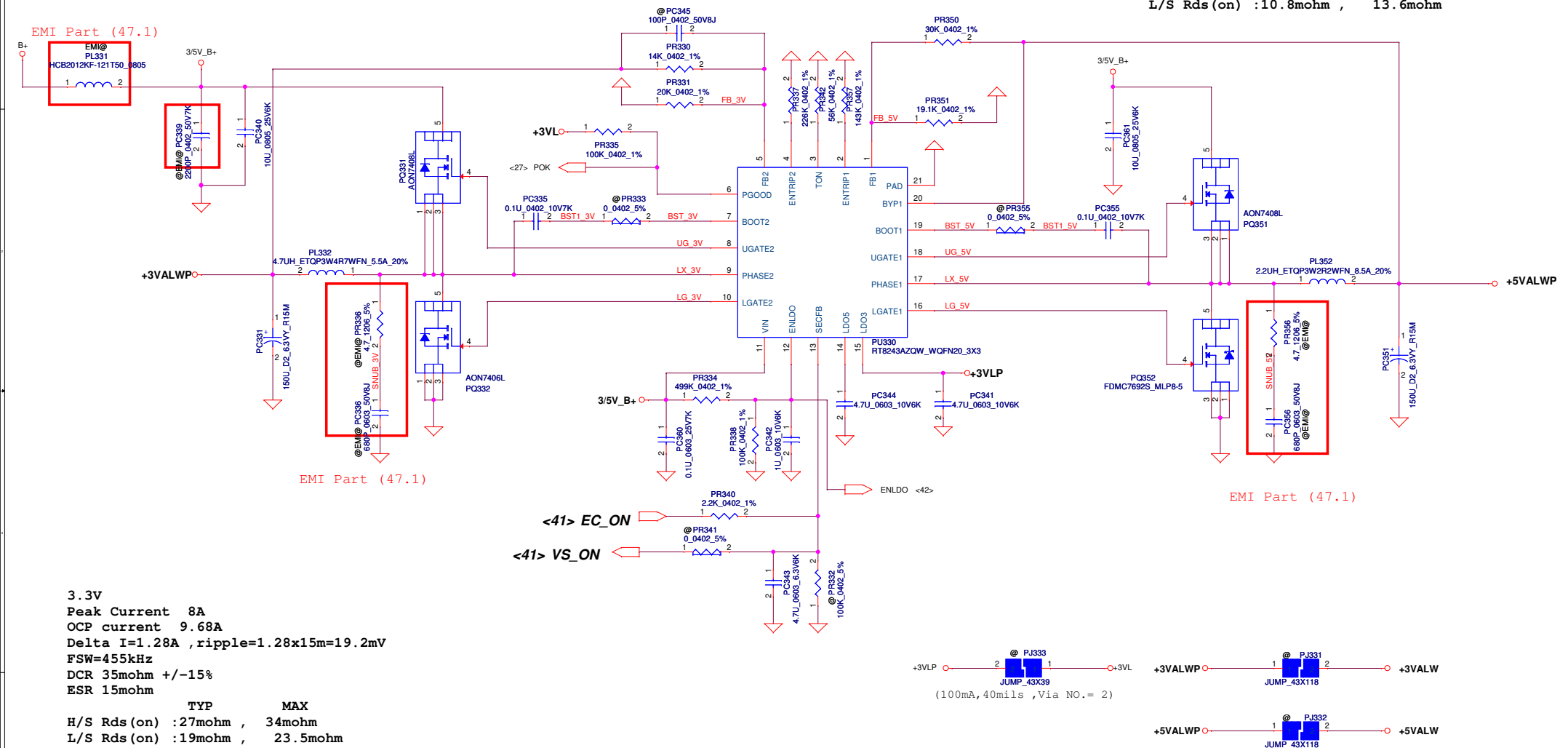
For A51 ADP_V function

Please locate the RC
Near EC chip
2011-02-22

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				Custom	VFKAA
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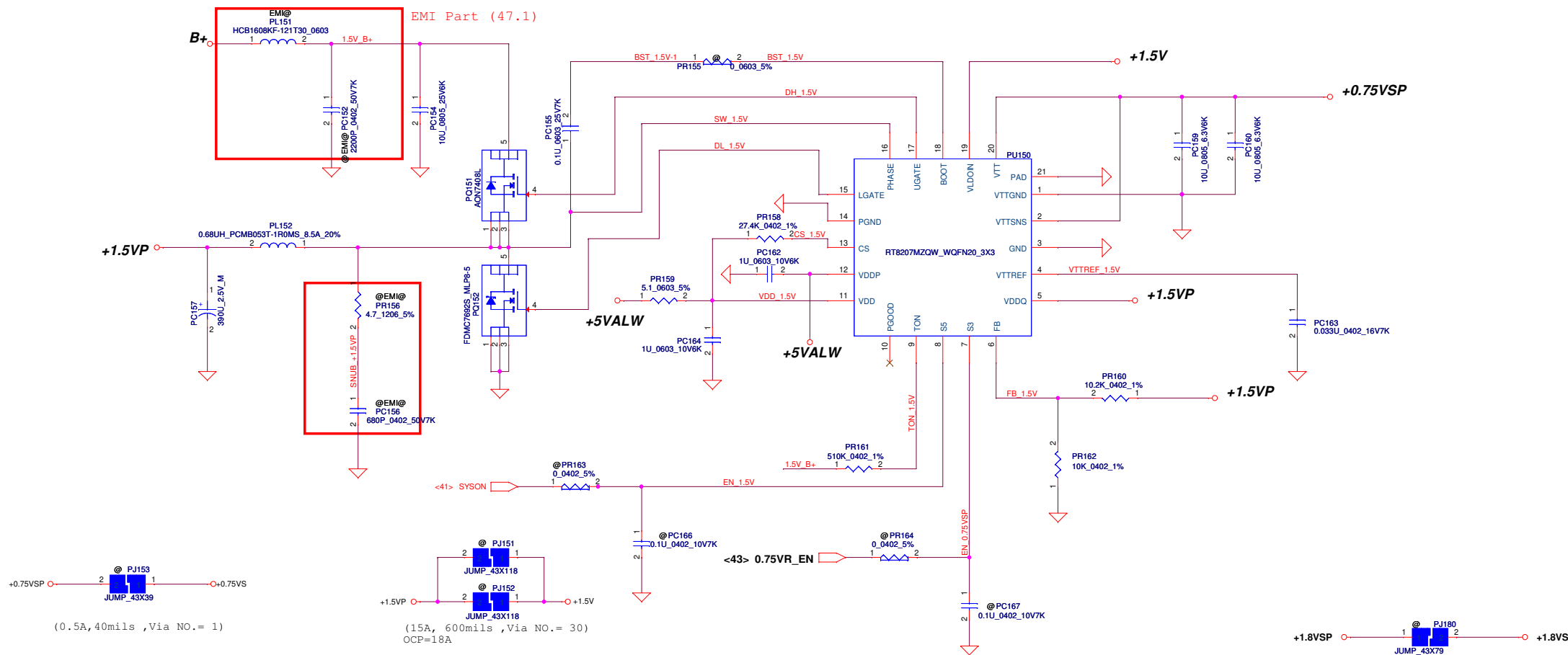
5V
Peak Current 10A
OCP current 12.03A
FSW=390kHz
Delta I=4.29A, ripple=4.29*17m=72.93mV
DCR 15.5mohm+/-15%
ESR 17mohm

	TYP	MAX
H/S Rds(on)	:27mohm	34mohm
L/S Rds(on)	:10.8mohm	13.6mohm



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				Custom	VFKAA	0.1	
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DDR controller (35.3), Support component (35.4)

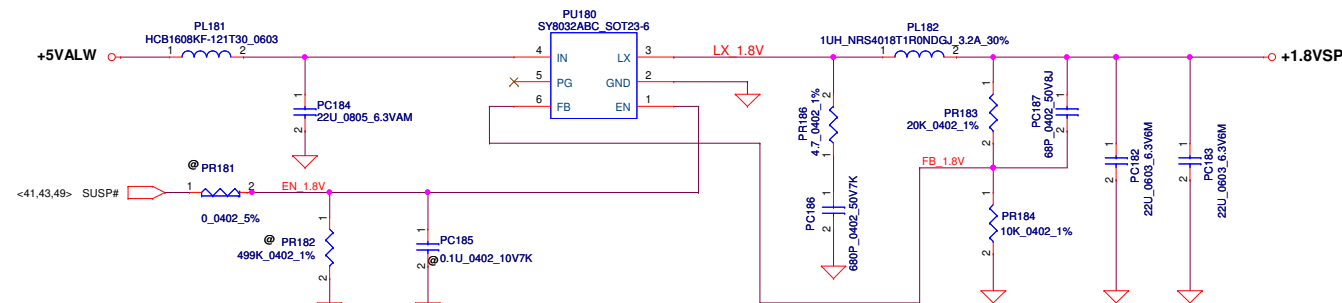


1.5V	
Peak Current	16.8A
OCF current	20 A
FSW=495kHz	
DCR 13mohm	
ESR 9mohm	
	TYP
H/S Rds (on)	:27mohm ,
L/S Rds (on)	:10.8mohm ,
	MAX
	34mohm
	13.6mohm

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

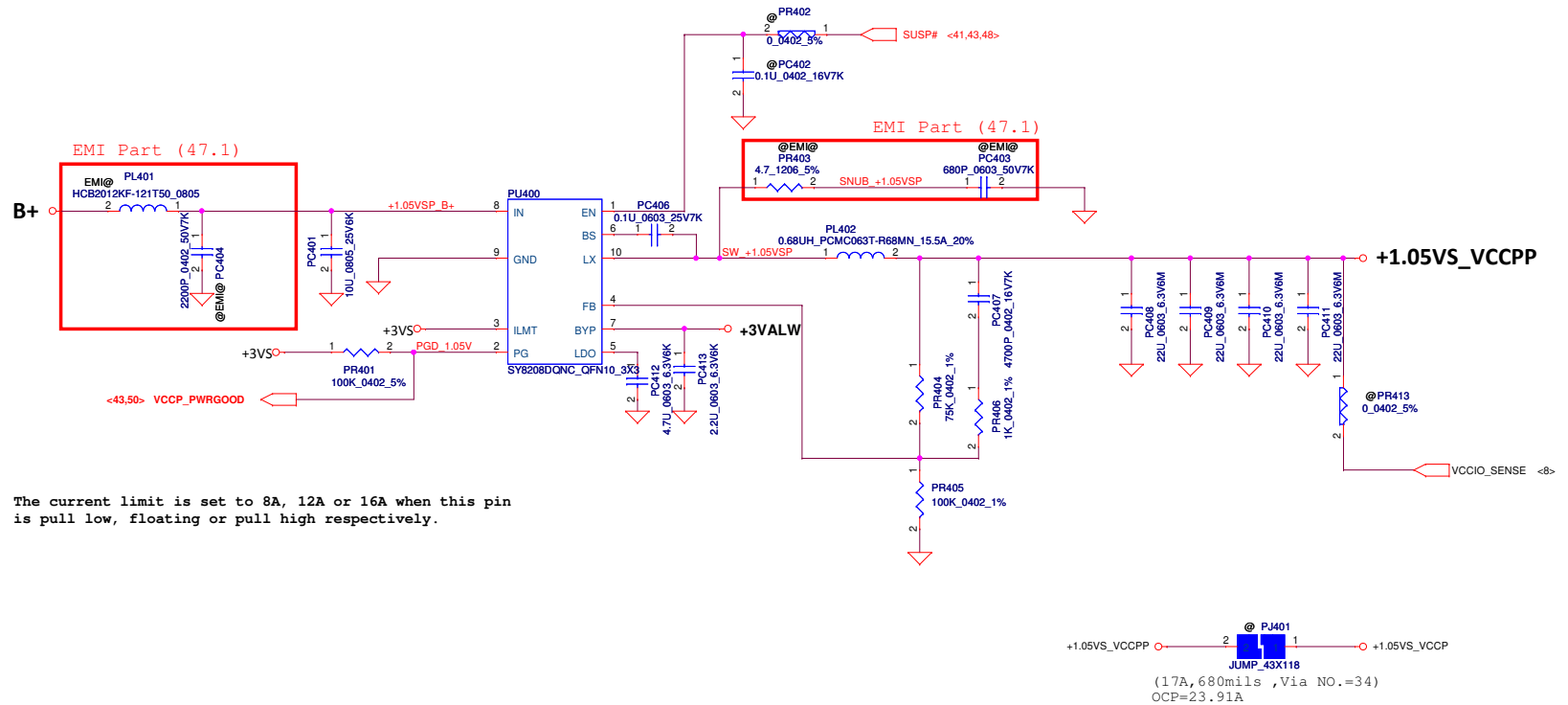
Note: S3 - sleep ; S5 - power off

1.8VS controller (35.15), Support component (35.16)



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				Size	Document Number	Rev	
				Custom	VFKAA	0.	
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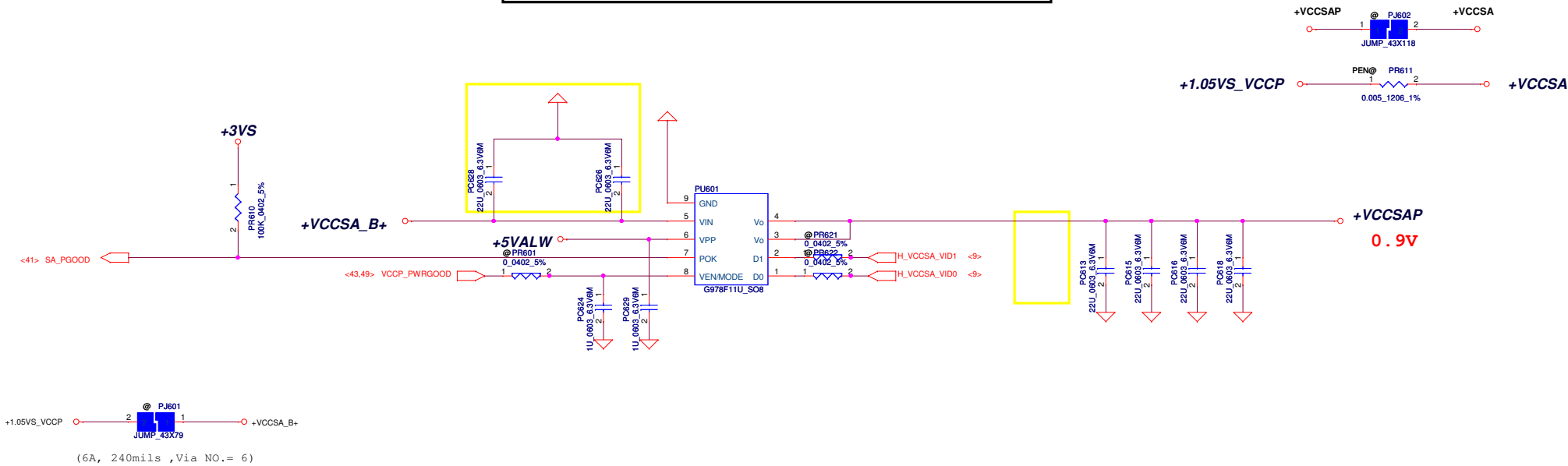
1.05VCCP controller (35.5), Support component (35.6)



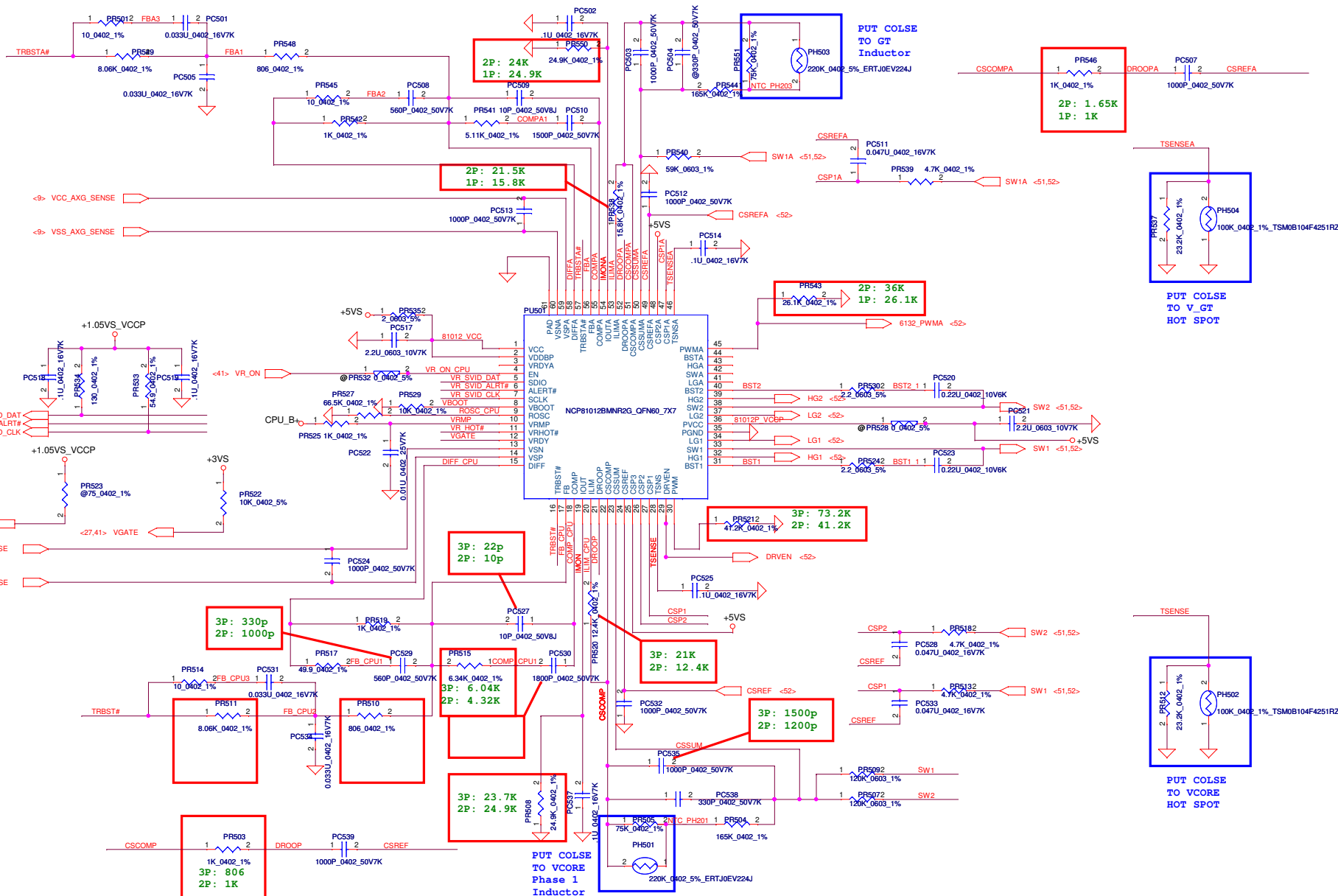
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Issued Date	2012/09/24	Deciphered Date	2013/09/24	Title	+1.05VS VCCP	
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VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

VCCSA controller (35.17), Support component (35.18)

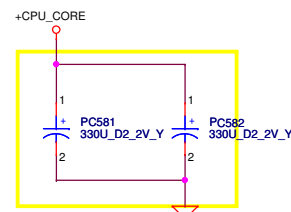
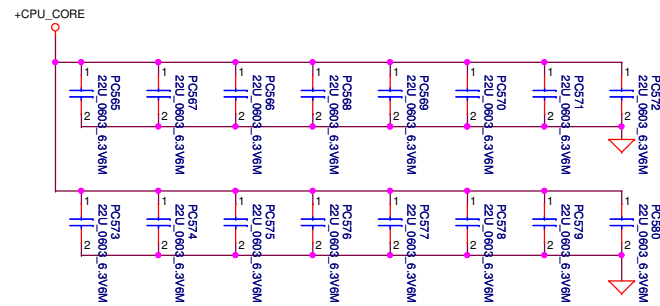
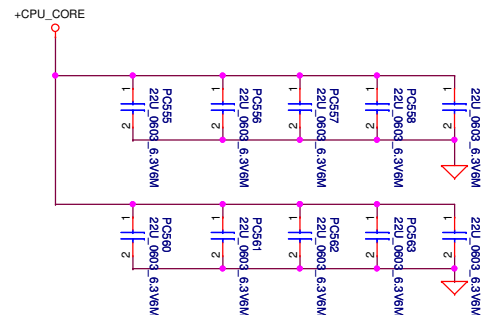
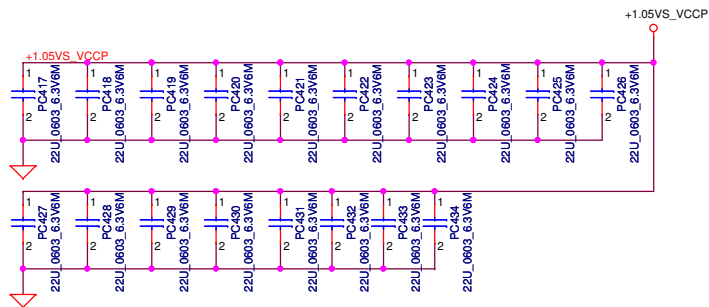
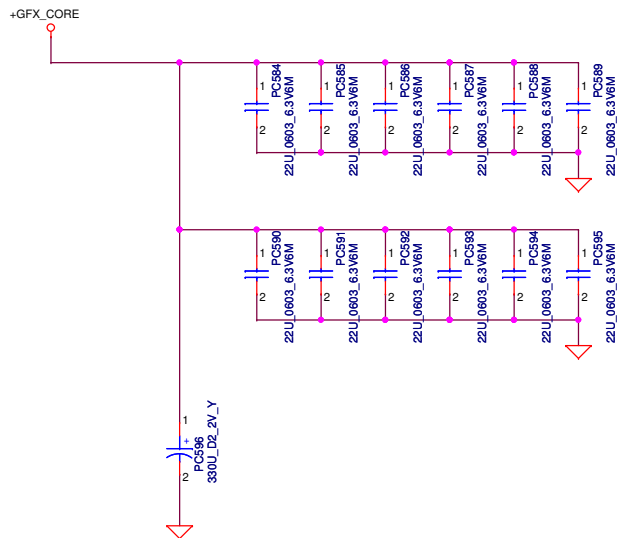


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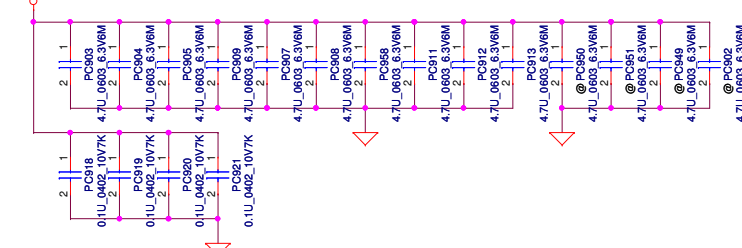
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> PWR-CPU_CORE	
Issued Date	2012/09/24	Deciphered Date	2013/09/24	Title	
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CPU_CORE output cap (36.4)
GFX_CORE output cap (36.5)
VCCP output cap (36.6)

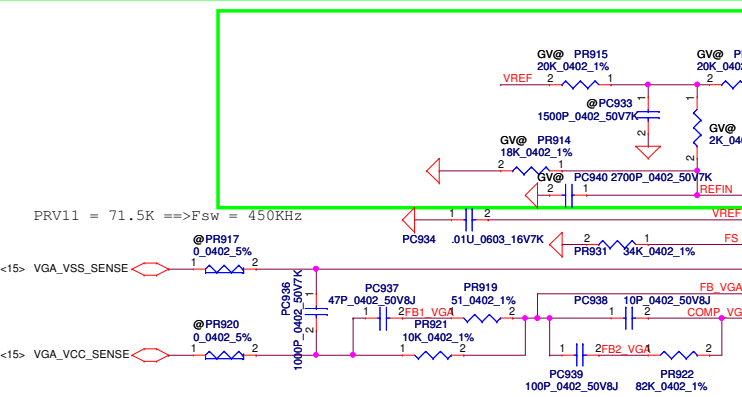
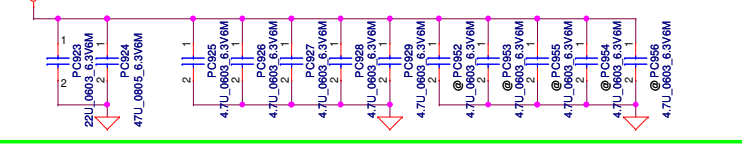


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+VGA_CORE Under VGA Core GB4-128 package



+VGA_CORE Near VGA Core

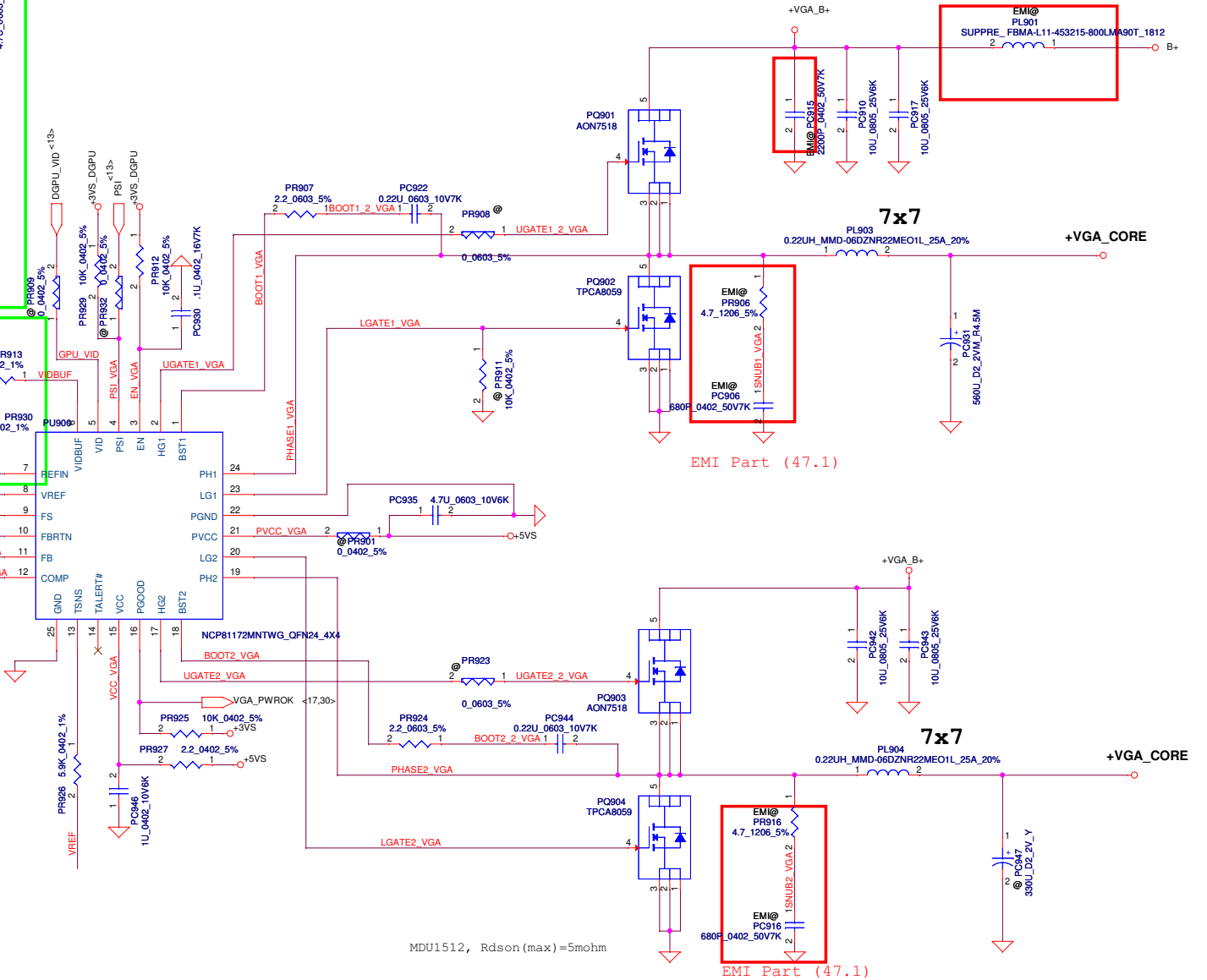


	N14P-GV2	N14M-GL
R1 PR913	20 Kohm	39 Kohm
R2 PR915	20 Kohm	30 Kohm
R3 PR930	2 Kohm	3 Kohm
R4 PR914	18 Kohm	27 Kohm
C PC940	2.7 nF	1.8 nF

- GL@ PR913 39K_0402_1%
- GL@ PR915 30K_0402_1%
- GL@ PR930 3K_0402_1%
- GL@ PR914 27K_0402_1%
- GL@ PC940 1800P_0402_50V7K

VGA_CORE controller (43.1), Support component (43.2)

EMI Part (47.1)



MDU1512, Rdson(max)=5mohm

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Issued Date	2012/09/24	Deciphered Date	2013/09/24	Title
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				Document Number
				VFKAA
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				0.1
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				Sheet 54 of 56

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				Document Number	Rev	
				QFKAA	0.1	
				Date: Monday, March 11, 2013	Sheet 55 of 56	

HW PIR (Product Improve Record)

VFKAA LA-9863P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 to 0.2
GERBER-OUT DATE: 2012/12/06

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	11/20	06	Mount CC37	To solve S3 shutdown issue
2.	11/20	29	Change USB port 10 to NC	No support NFC
3.	11/20	42	Delete JNFC	No support NFC
4.	11/20	37	Add QW1, RW3, RW4; change JCARD.10 to SDWP# and JCARD.11 to SDCD	To solve card reader no function issue
5.	11/27	40	Change JSPK to ACES_50228-0067N-001_6P	For SPK recognize design
6.	11/28	08	Mount CC17, CC18, CC19	For ESD request
7.	11/28	29	Mount CB13	For ESD request
8.	11/28	05	Mount CC63	For ESD request
9.	12/03	38	Add S&C 14640/14641 co-layout circuit	Reserved for S&C SPEC update

VFKAA LA-9863P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2 to 0.3
GERBER-OUT DATE: 2013/01/23

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	12/19	41	Change CB13 to SE071101J80 (100pF)	ESD request
2.	12/26	17	Change RV43 to 270K, RV53 to 10K, RV54 to 33K	For VGA power sequence
3.	01/16	41	Add RB12, RB37, connect EC_MUTE_INT from codec to EC	To solve audio "bo" sound issue
4.	01/16	42	Modify JTP pin define	For ME drawing update
5.	01/16	13	Connect GPIO12 as GPS_DOWN# to EC	For GPS function
6.	01/16	26	Mount RH38	For EMI request
7.	01/16	22	Reserve R266, R267	For EMI request

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