

Compal Confidential

UMA M/B Schematics Document

Haswell with DDRIII + Lynx Point PCH

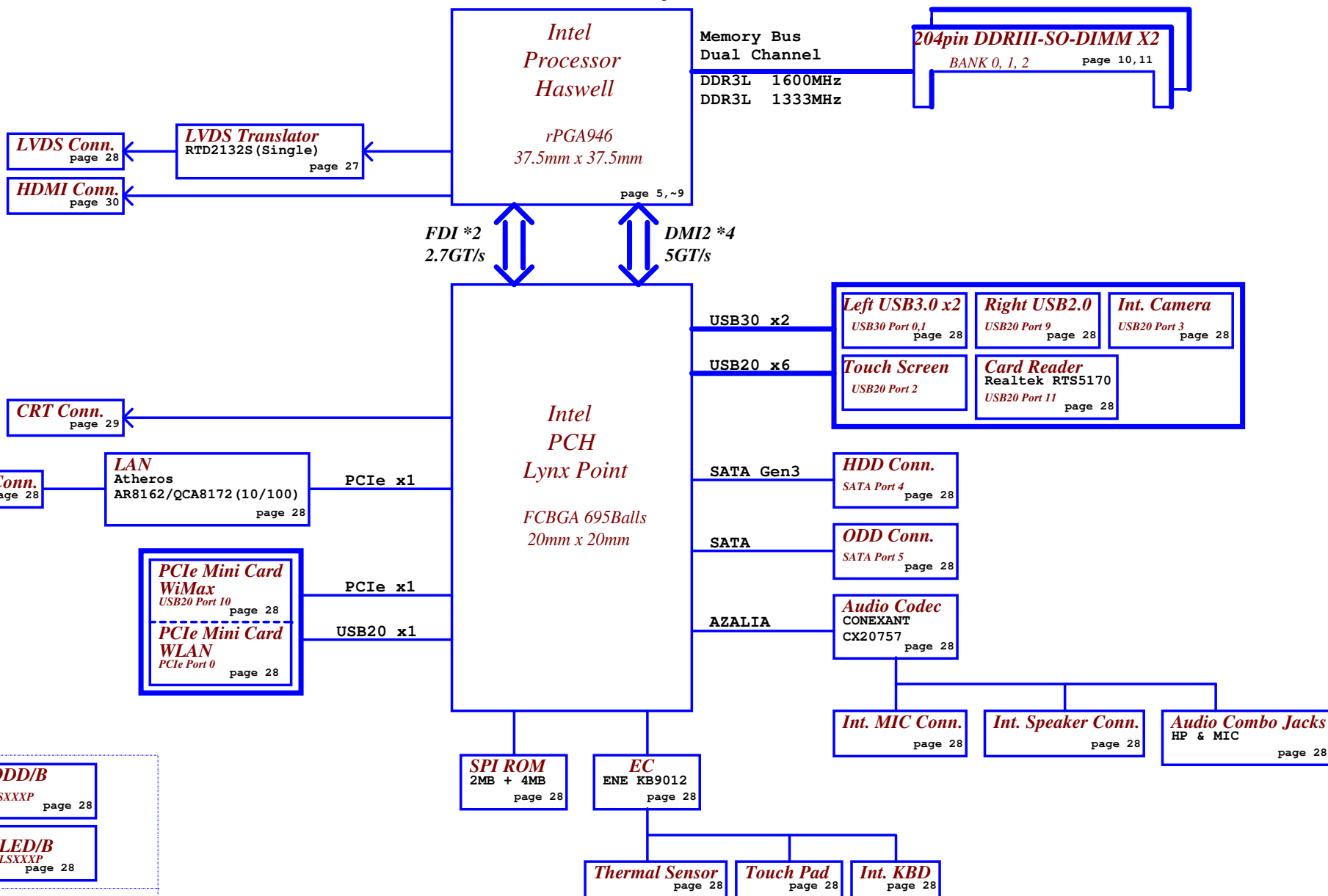
2012-10-03

LA-9642P

REV: 0.1

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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Cover Page
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Shark Bay



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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Block Diagram
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Voltage Rails				
power plane	+B	+5VALW +3VALW	+1.35V	+5VS +3VS
				+VCC_CORE +VGA_CORE +1.5VS +0.675VS +1.05VS
State				
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%	Board ID / SKU ID Table for AD channel				
Ra/Rc/Re	100K +/- 5%					
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	Porject	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Y-series	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Y-series	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Y-series	PVT
7	NC	2.500 V	3.300 V	3.300 V	Y-series	MP

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	Left USB3.0
		1	Left USB3.0
	UHCI1	2	Touch screen
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
7			
EHCI2	UHCI4	8	
		9	Right USB2.0
	UHCI5	10	WLAN
		11	Card reader
	UHCI6	12	
		13	

BOM Structure Table

BTO Item	BOM Structure
HDMI	HDMI@
Connector	ME@
45 LEVEL	45@
10/100 LAN	
LAN LDO Mode	LDO@
LAN Switch mode	SWR@
Camera	CMOS@
For QIWG5 (14")	14@
For QIWG6 (15")	15@
Unpop	@

EC SM Bus1 address EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011Xb	Thermal Sensor F75303M	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

NV-GPU SM Bus address

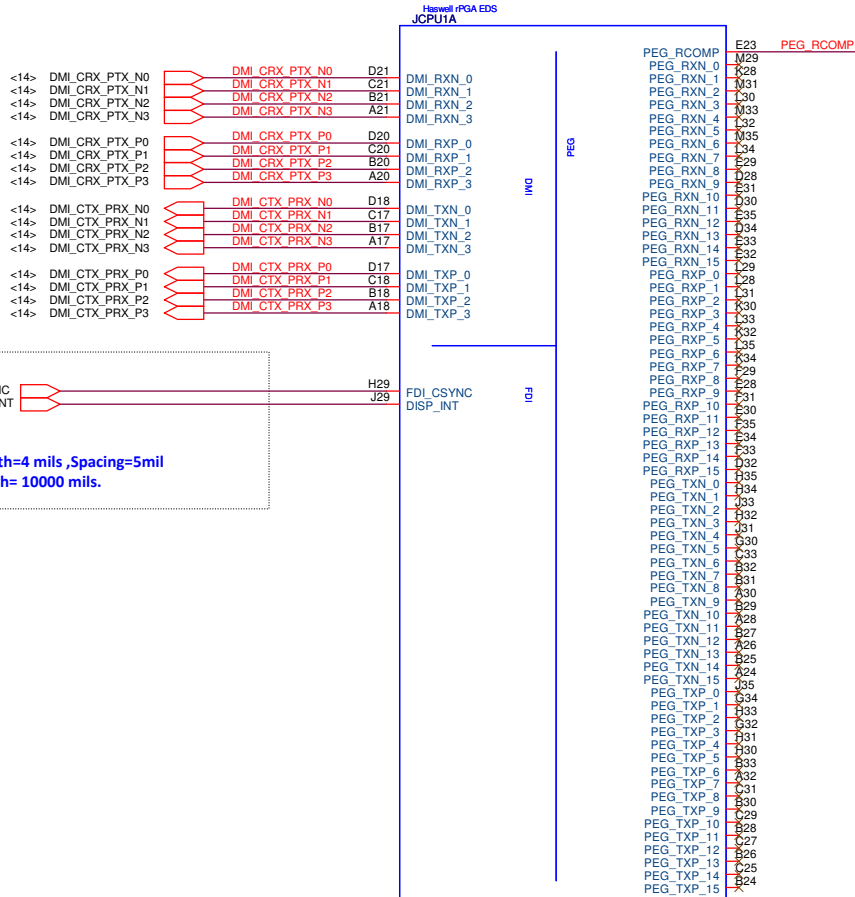
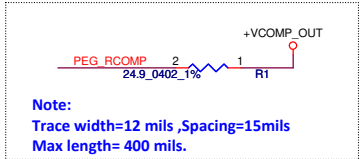
Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH	RTD2132
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW						
SMB_EC_CK2	KB9012	X	X	X	X	X	X	X	X
SMB_EC_DA2	+3VALW							+3VS	+3VS
SMBCLK	PCH	X	X	X	V	V	X	X	X
SMBDATA	+3VALW				+3VS	+3VS			
SML0CLK	PCH	X	X	X	X	X	X	X	X
SML0DATA	+3VALW								
SML1CLK	PCH	V	X	V	X	X	V	X	V
SML1DATA	+3VALW	+3VS		+3VS			+3VS		+3VS

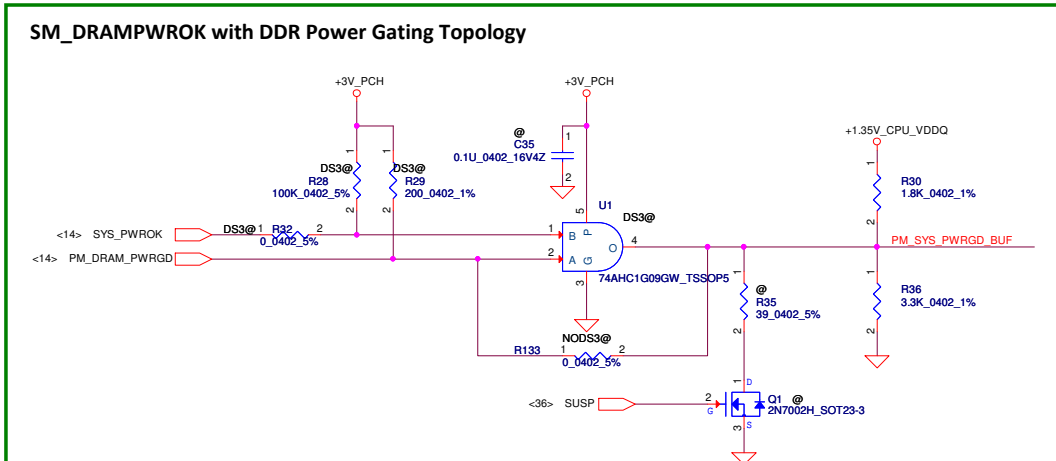
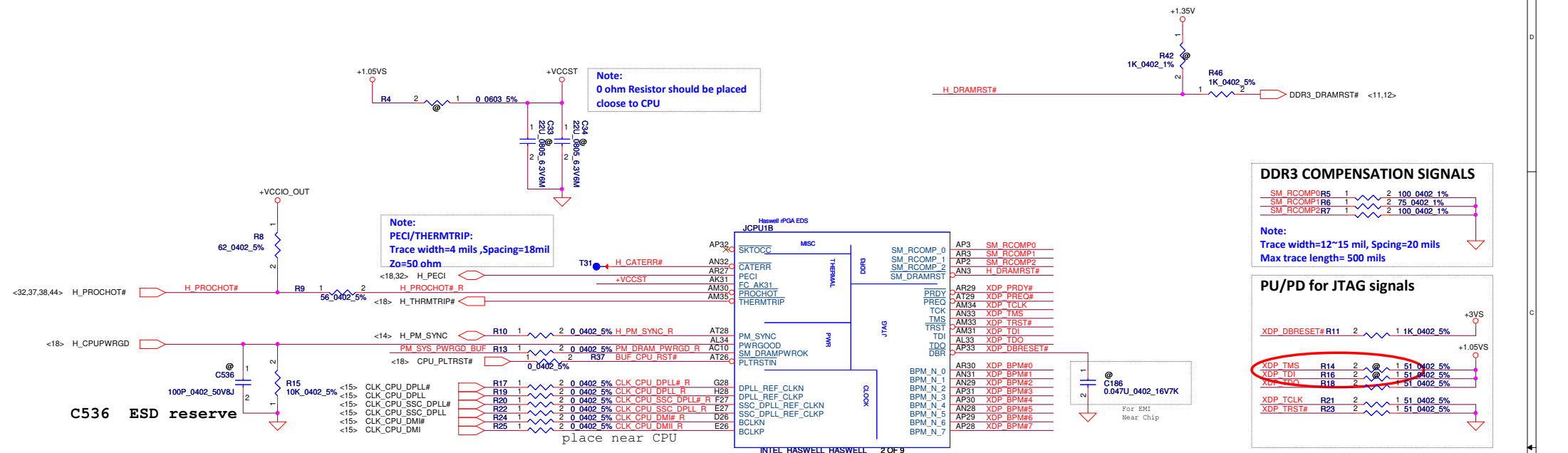
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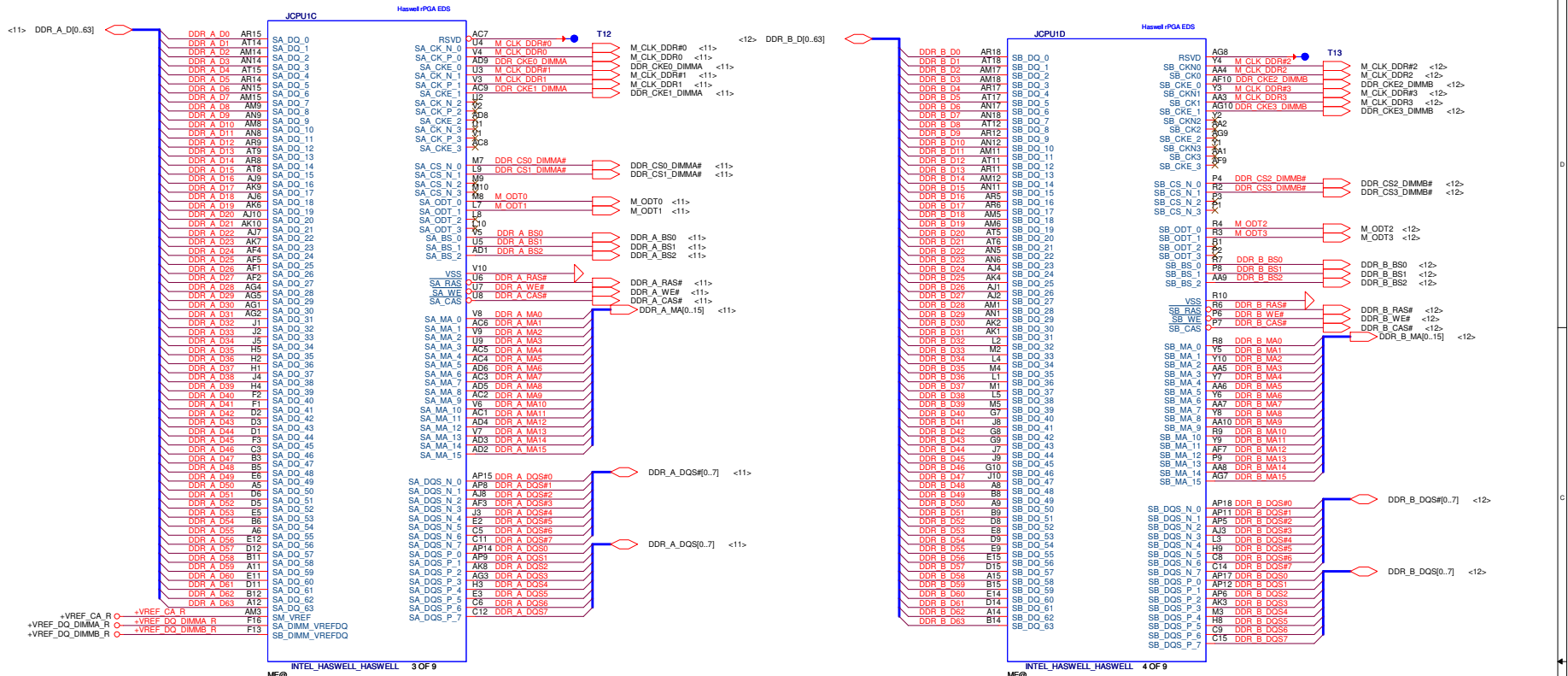
ZZZ1
PCB LA9641



INTEL_HASWELL_HASWELL 1 OF 9
ME@

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								Size		Document Number		Rev	
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CPI DRIVER VREF PATH IS DEFAULT

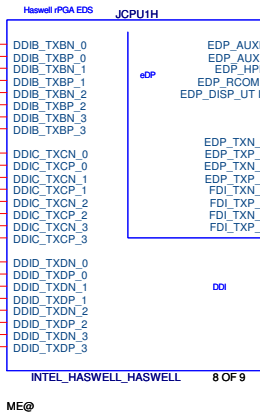
*M3+M1:Default Recommendation
M1:VREF_DQ driven by a voltage Divider Network during
Processor power-off state.
M3:VREF_DQ driven by Processor.

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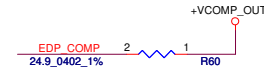
HDMI D2
HDMI D1
HDMI D0
HDMI CLK

HDMI

Place on connector side

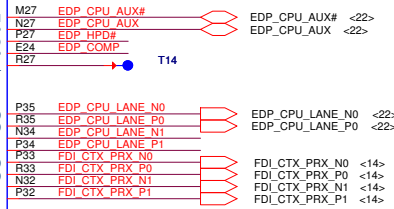


COMPENSATION PU FOR eDP

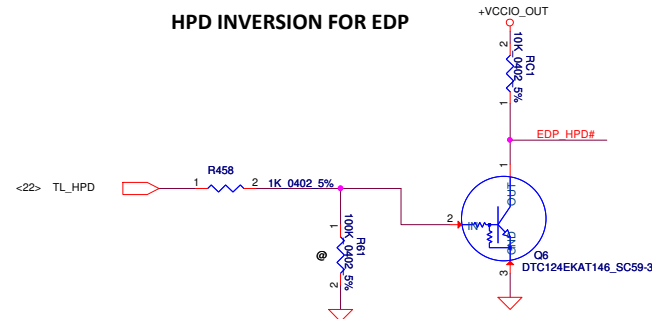


Note:

Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.



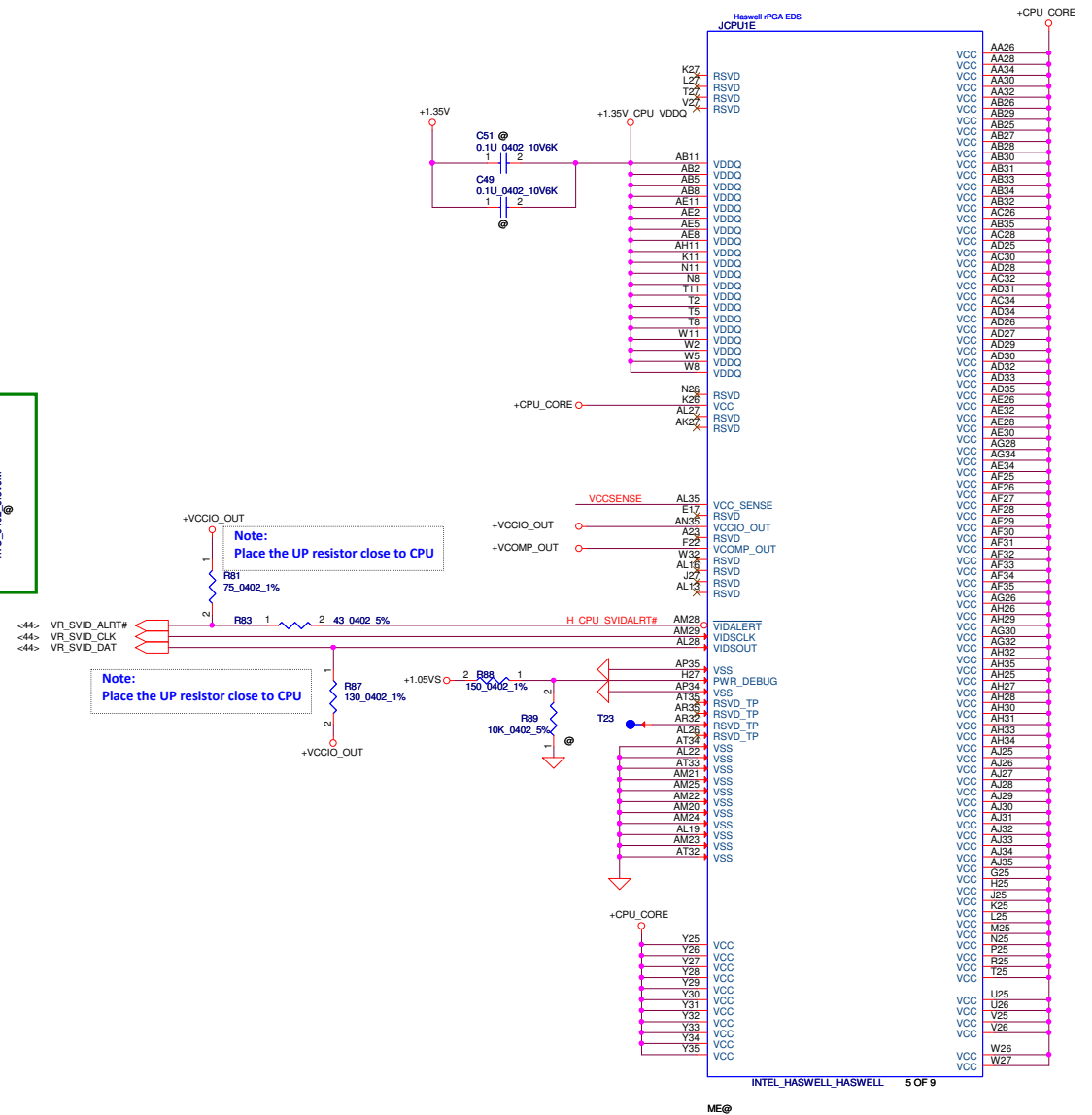
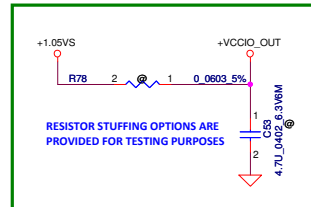
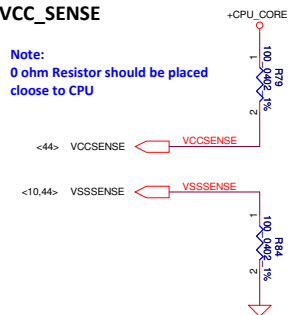
HPD INVERSION FOR EDP



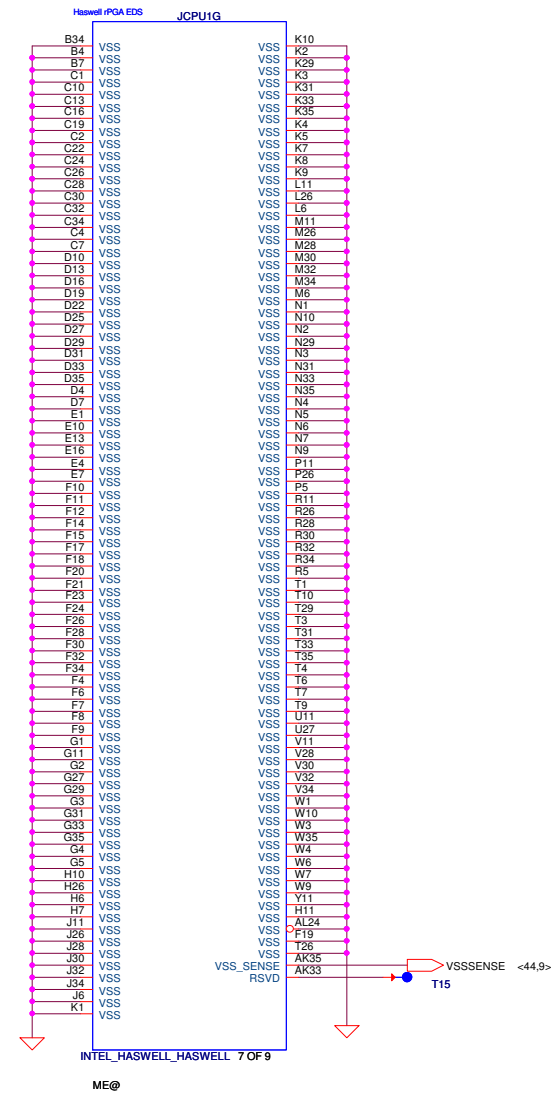
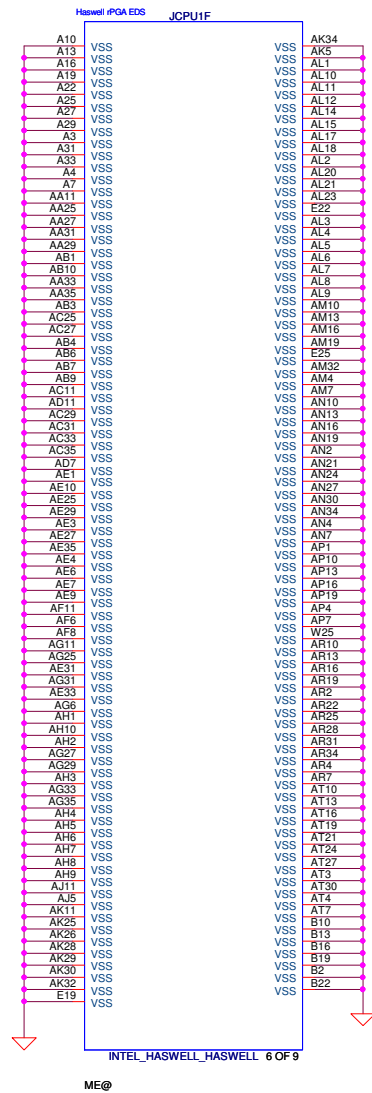
HPD is a active high signal from device. The HPD processor input is a low voltage active signal.

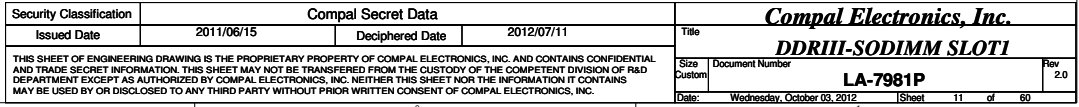
The diagram shows a circuit connection between two pins. Pin 14, labeled 'CFG4', is connected to pin 32, labeled 'WROK <14,32>'. A resistor, labeled 'R63 1K_0402_1%', is connected between these two pins. The resistor is represented by a zigzag line. The pin 32 is also labeled with a red triangle symbol.

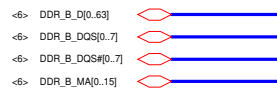
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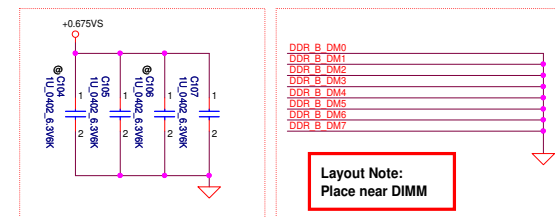
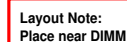
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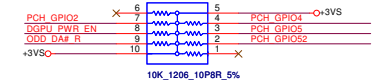
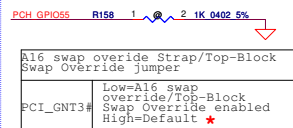
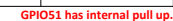
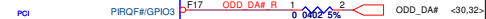
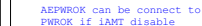




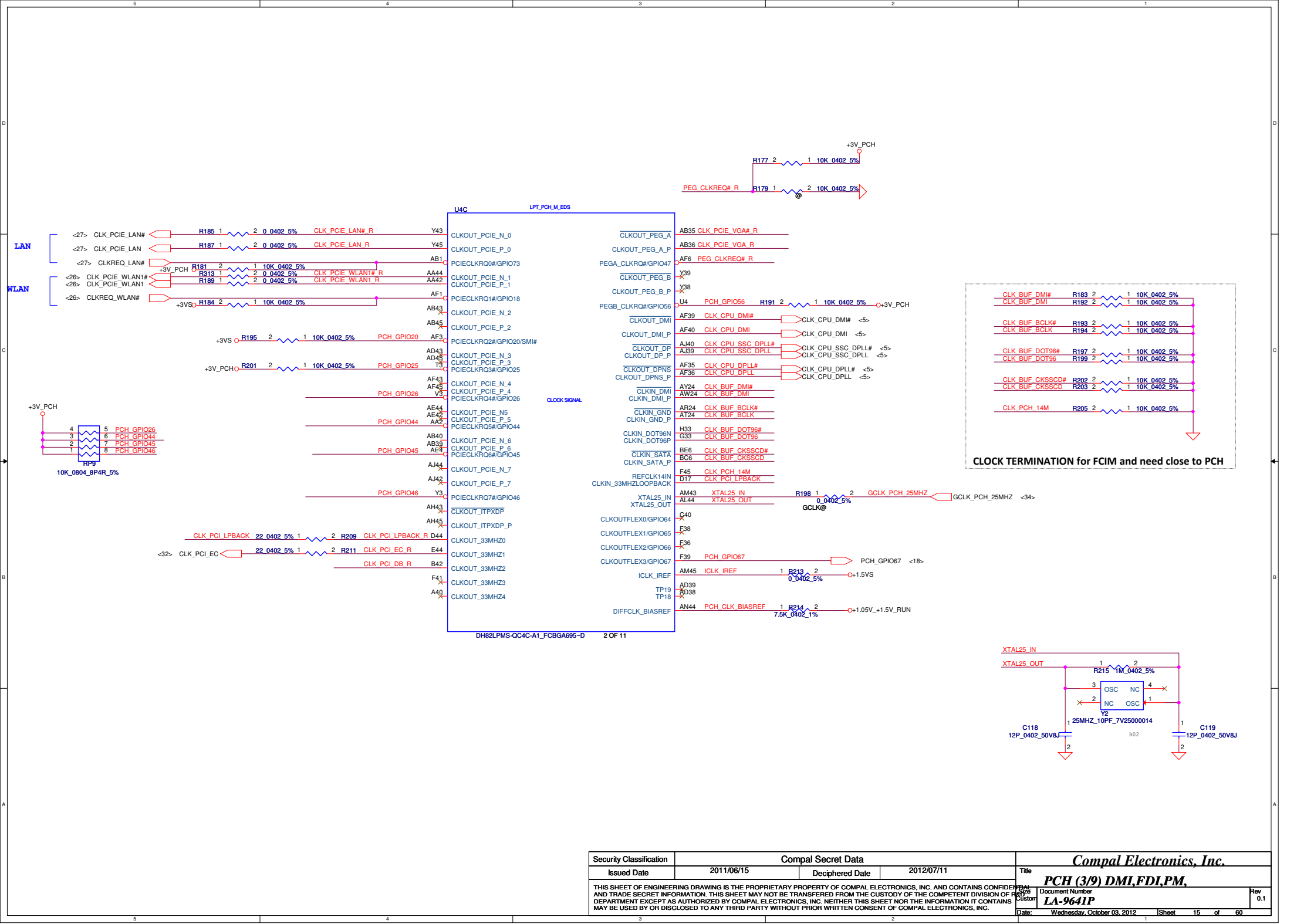
(10uF_0603_6.3V) *8
(0.1uF_402_10V) *4

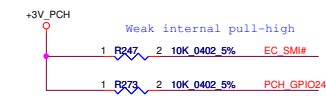


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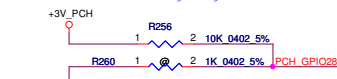


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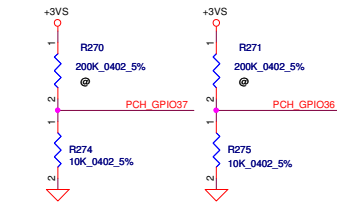
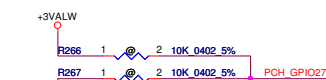




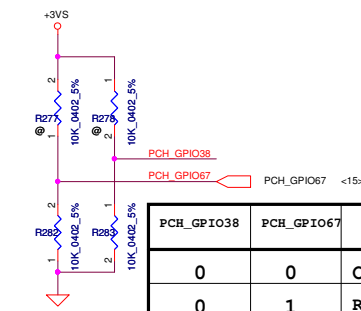
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable (Default)
L : On-Die PLL Voltage Regulator disable



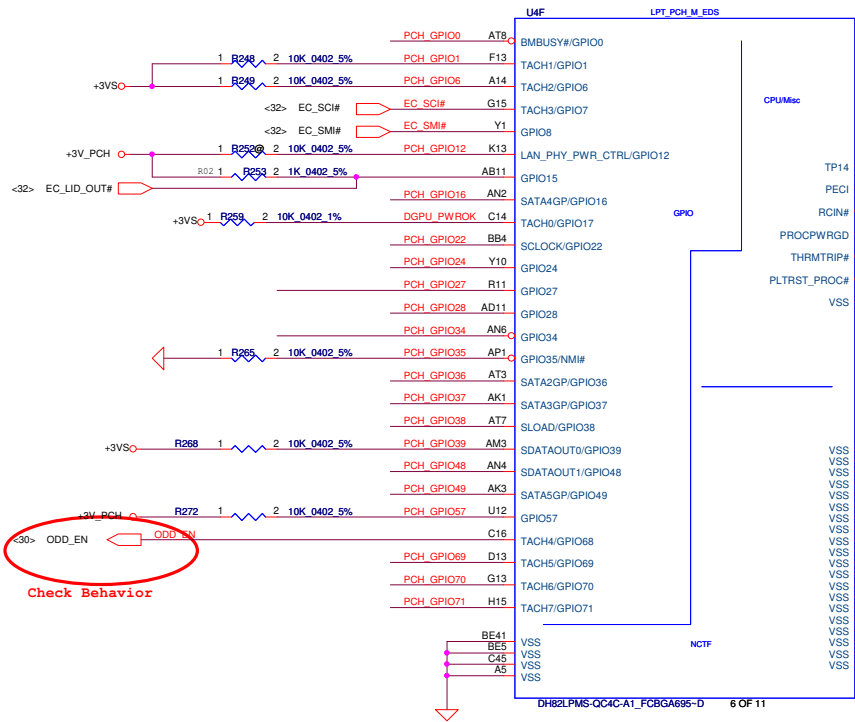
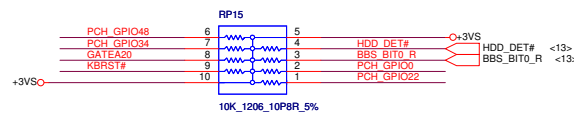
★ PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable



BIOS Request SKU ID



PCH_GPIO38	PCH_GPIO67	Function
0	0	Optimus
0	1	Reserved
1	0	DIS
1	1	UMA



Check Behavior

Config	GPIO16 & 49
USB3.0 x4, PCIe x8, SATA x6	11
★ USB3.0 x6, PCIe x8, SATA x4	01

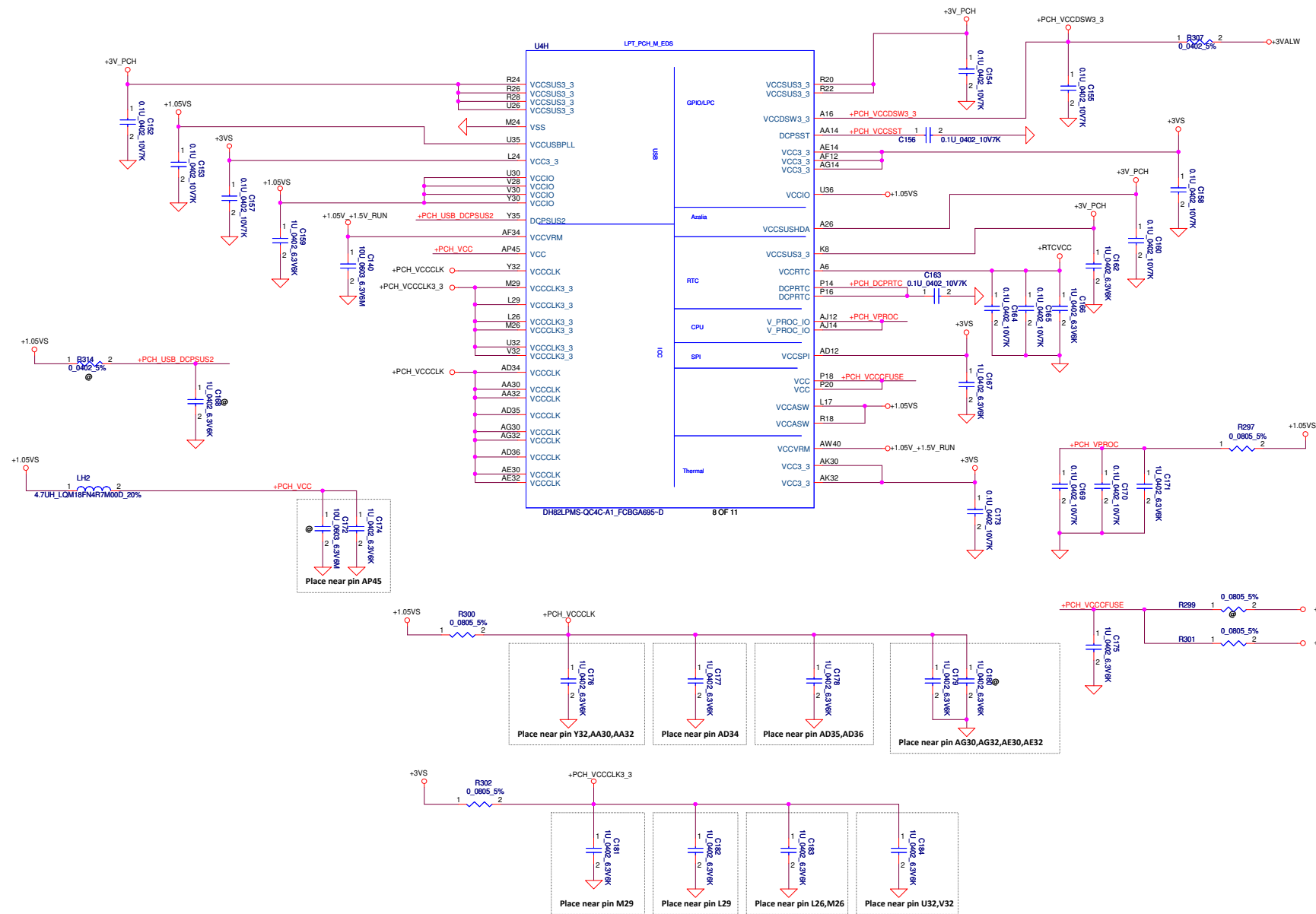
Fixed Signals	Muxed Signals	Fixed Signals	Muxed Signals	Fixed Signals
USB3 1	PCIe 1	PCIe 3	SATA 4	SATA 1
USB3 2	PCIe 2	PCIe 4	SATA 5	SATA 2
USB3 5	PCIe 3	PCIe 5	SATA 6	SATA 3
USB3 6	PCIe 4	PCIe 6	SATA 7	
	PCIe 5	PCIe 7	SATA 8	
	PCIe 6	PCIe 8	SATA 9	
	PCIe 7	PCIe 9	SATA 10	
	PCIe 8	PCIe 10	SATA 11	
	PCIe 9	PCIe 11	SATA 12	
	PCIe 10	PCIe 12	SATA 13	

Check list requir 1K pull high, CRB 100 ohm@

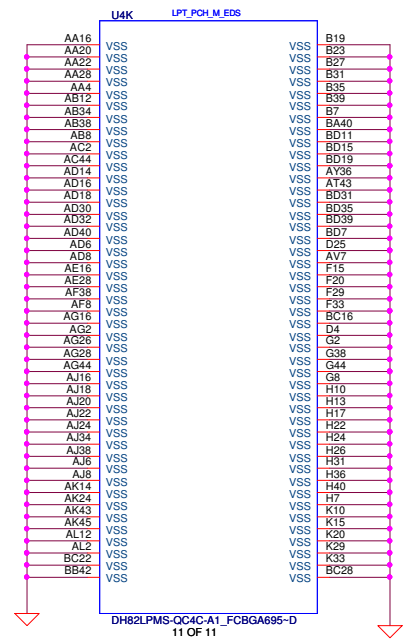
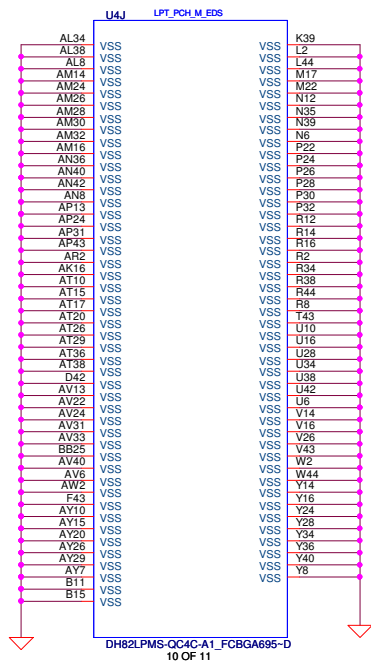
Need Update

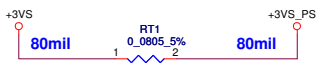
PCH_GPIO69	Function
0	
1	

PCH_GPIO70	Function
0	
1	
PCH_GPIO71	
0	
1	

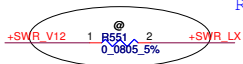


PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

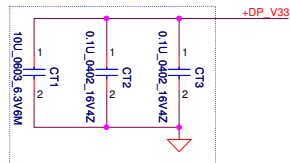




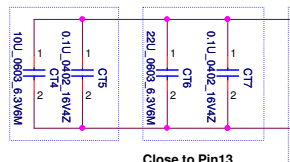
RTD2132R LDO MODE



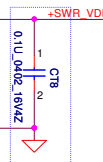
Close to Pin3



Close to L87

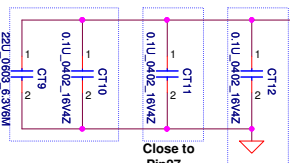


Close to Pin18



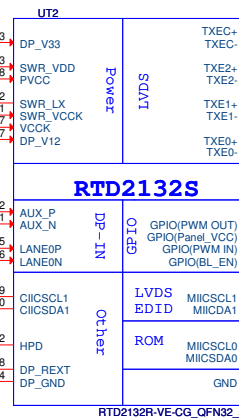
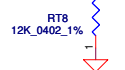
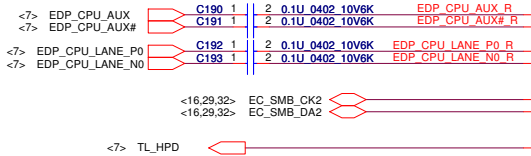
Close to Pin13

Close to L29



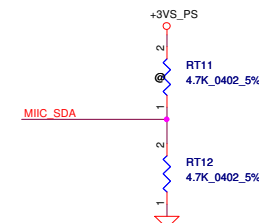
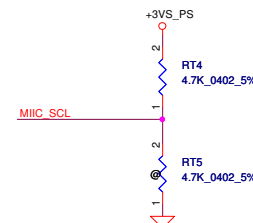
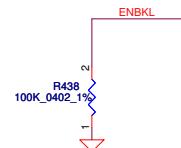
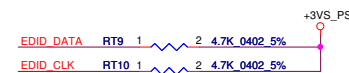
Close to Pin27

Close to Pin7



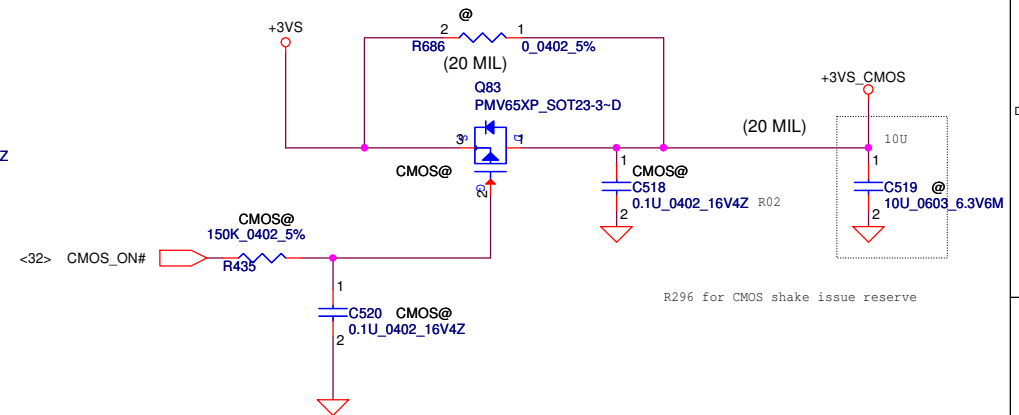
TL_ENVDD need 40 mil if use for LVDS power on R version

ADD TP on trace or via

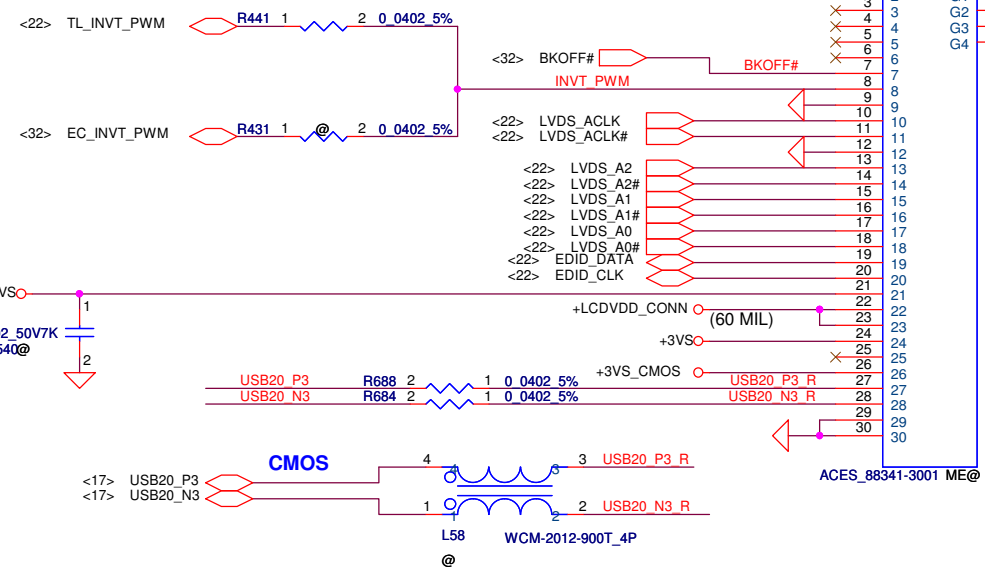


MIIC_SCL \ MIIC_SDA	MIIC_SDA	
	0	1
0	X	EC CODE
1	Internal ROM	EEPROM

CMOS Camera

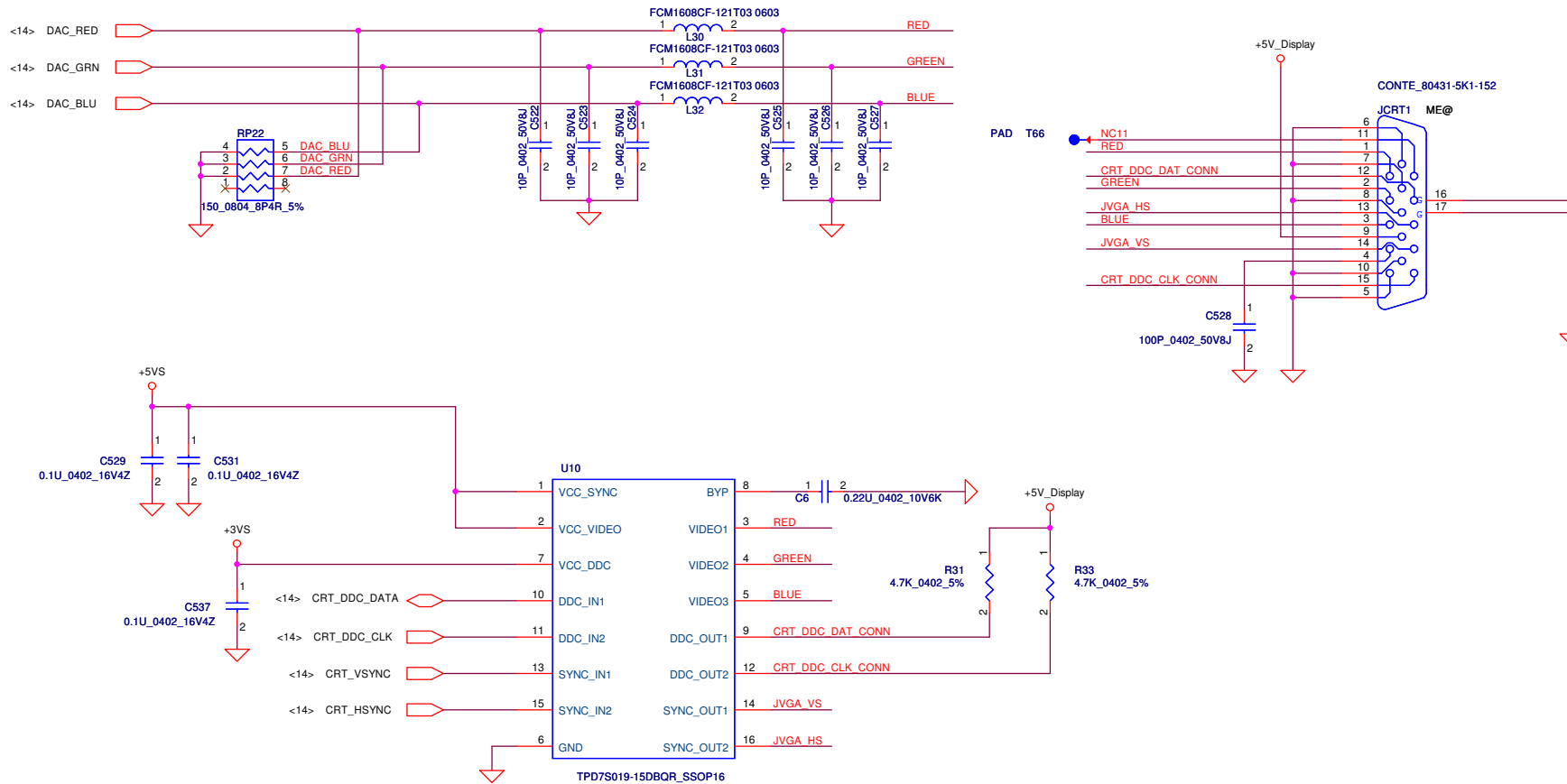


RTD2132R Internal load switch for +LCD_VCC

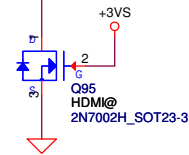
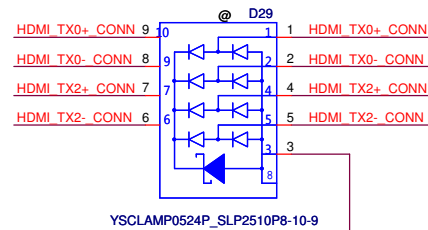
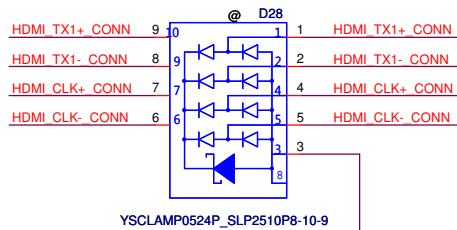
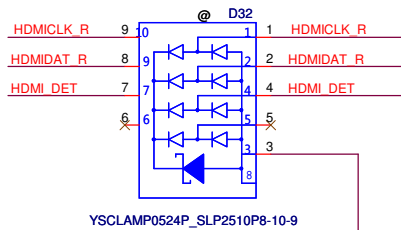
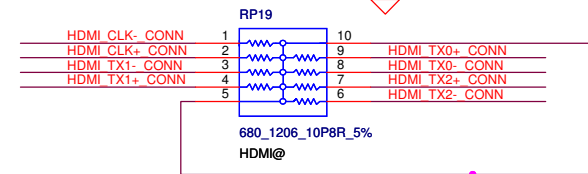
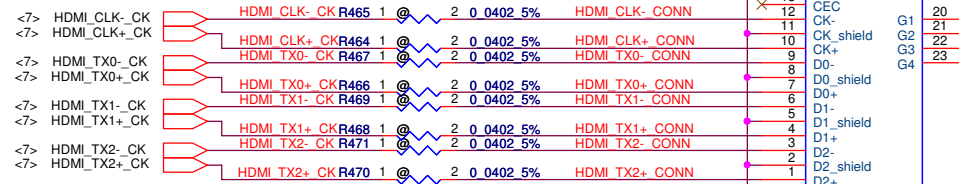
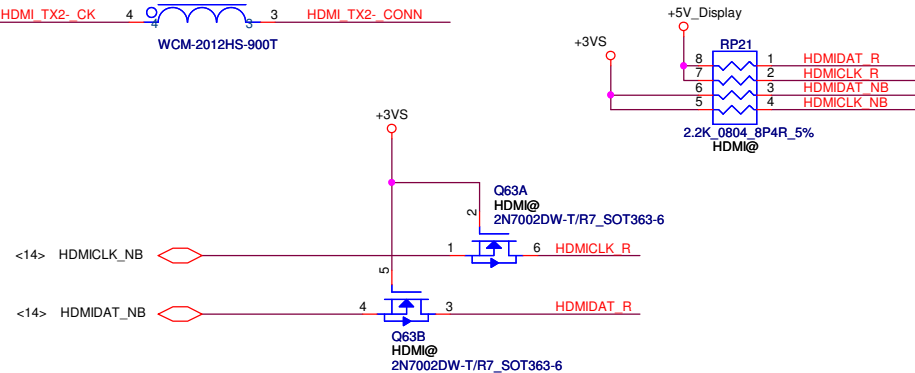
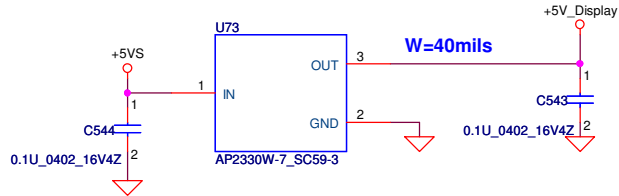
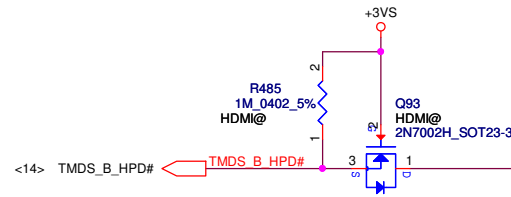
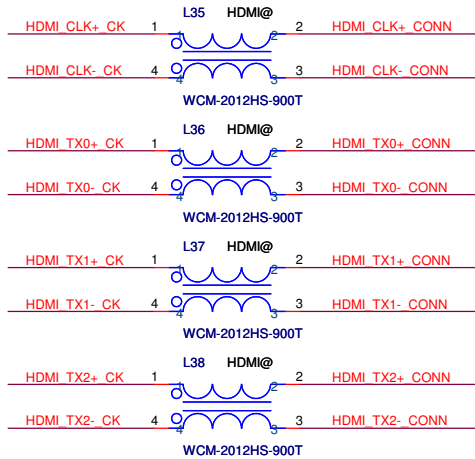


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				Size	Document Number			Rev		
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CRT Connector

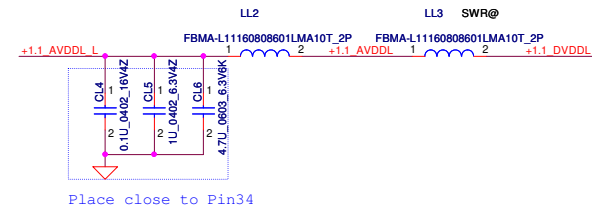
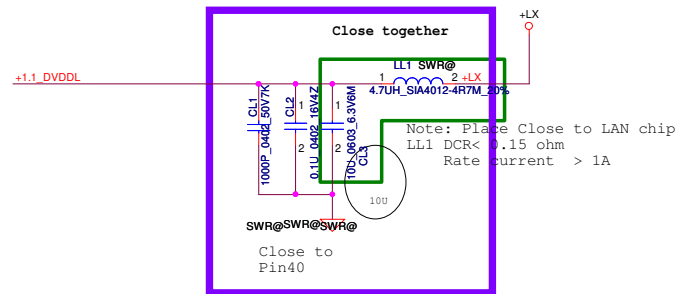


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				Custom	LA-9641P	2.0	
				Date:	Wednesday, October 03, 2012	Sheet	24 of 60



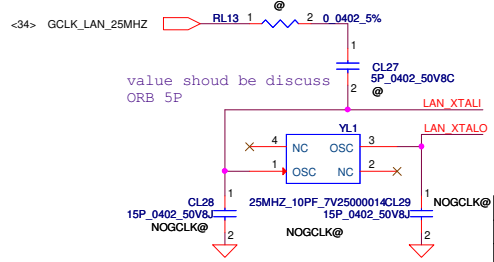
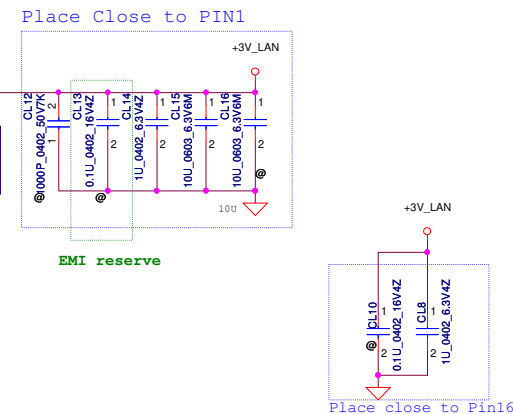
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Issued Date				2011/06/15		Deciphered Date		2012/07/11		Title	
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										LA-9641P	
										Rev	
										2.0	
										Date: Wednesday, October 03, 2012	
										Sheet 25 of 60	

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					LA-9641P	2.0
				Date: Wednesday, October 03, 2012	Sheet 26 of 60	



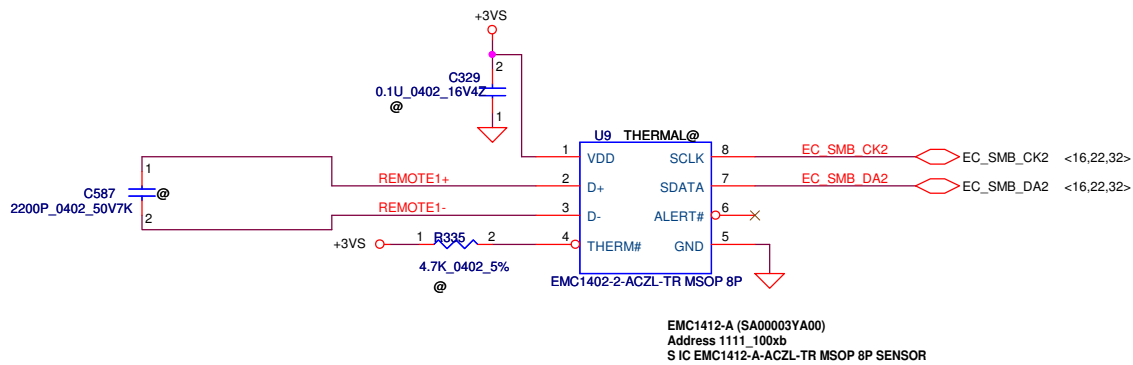
UL1 8162@
AR8162-AL3A-R

SA000065400 S IC QCA8172-AL3A-R QFN 40P E-LAN CTRL
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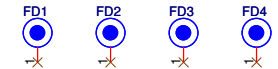
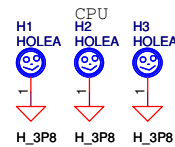


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						Custom		LA-7982P		1.0	
						Date:		Wednesday, October 03, 2012		Sheet 27 of 60	

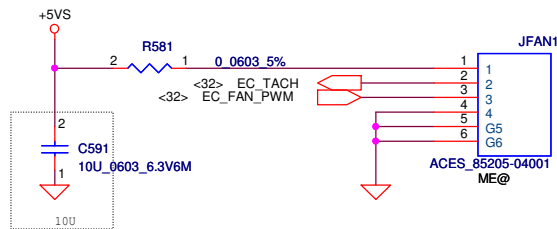
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REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



FAN1 Conn

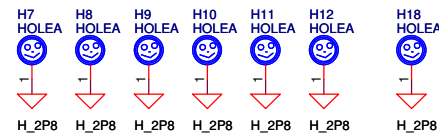


A

B

M/B 橢圓孔

M/B 圓孔



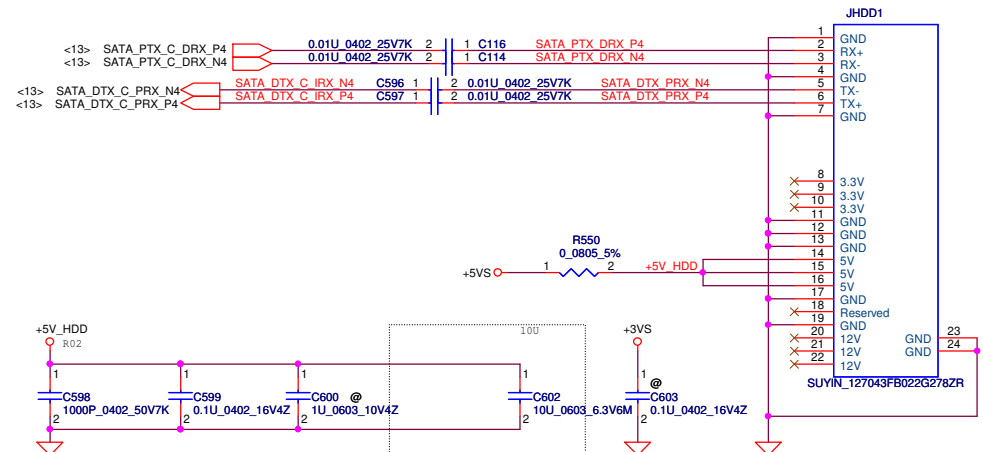
2P8 * 7 pcd

D

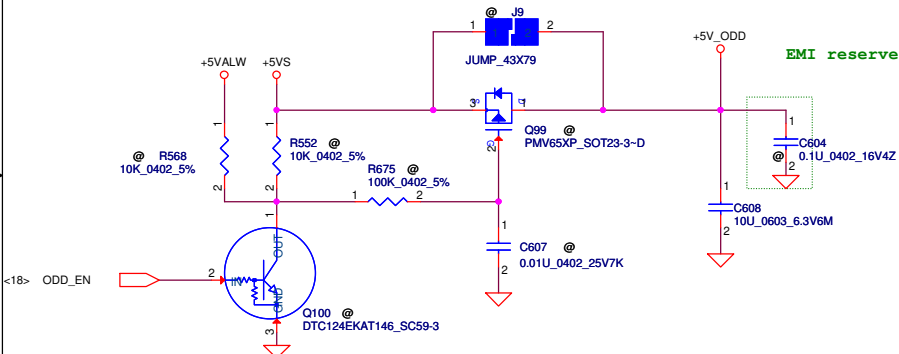
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				LA-9641P	
Date: Wednesday, October 03, 2012				Sheet	29 of 60

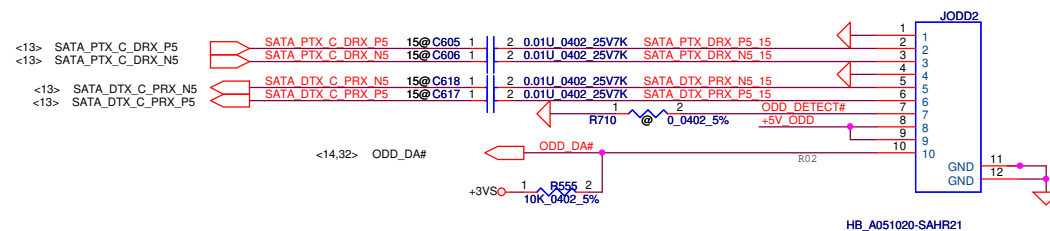
SATA HDD Conn.



ODD Power Control

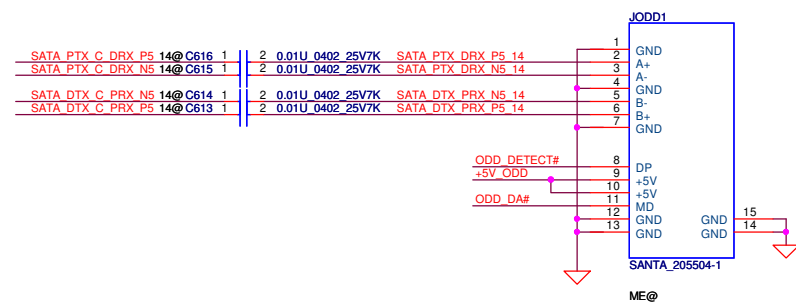


FOR 15" SATA ODD FFC Conn.



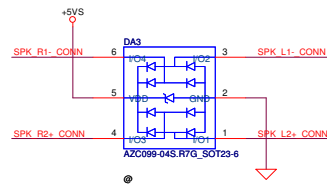
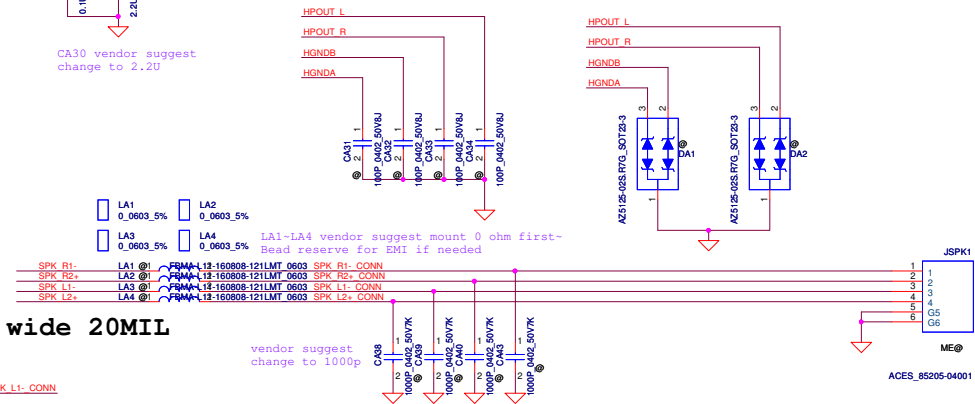
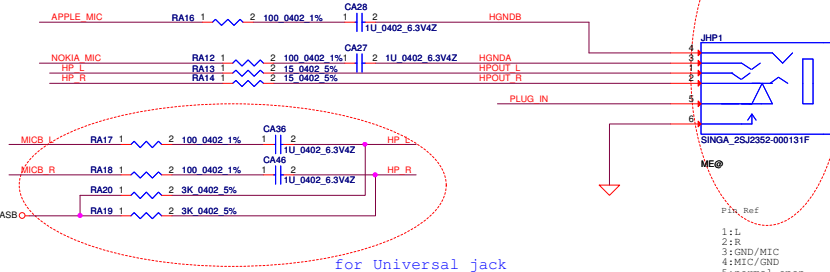
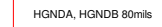
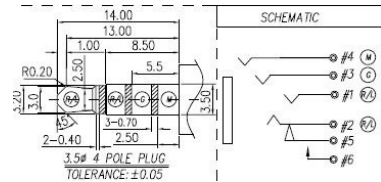
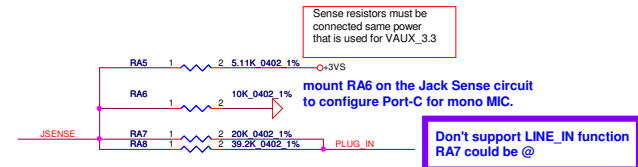
Co-lay

FOR 14" SATA ODD Conn.

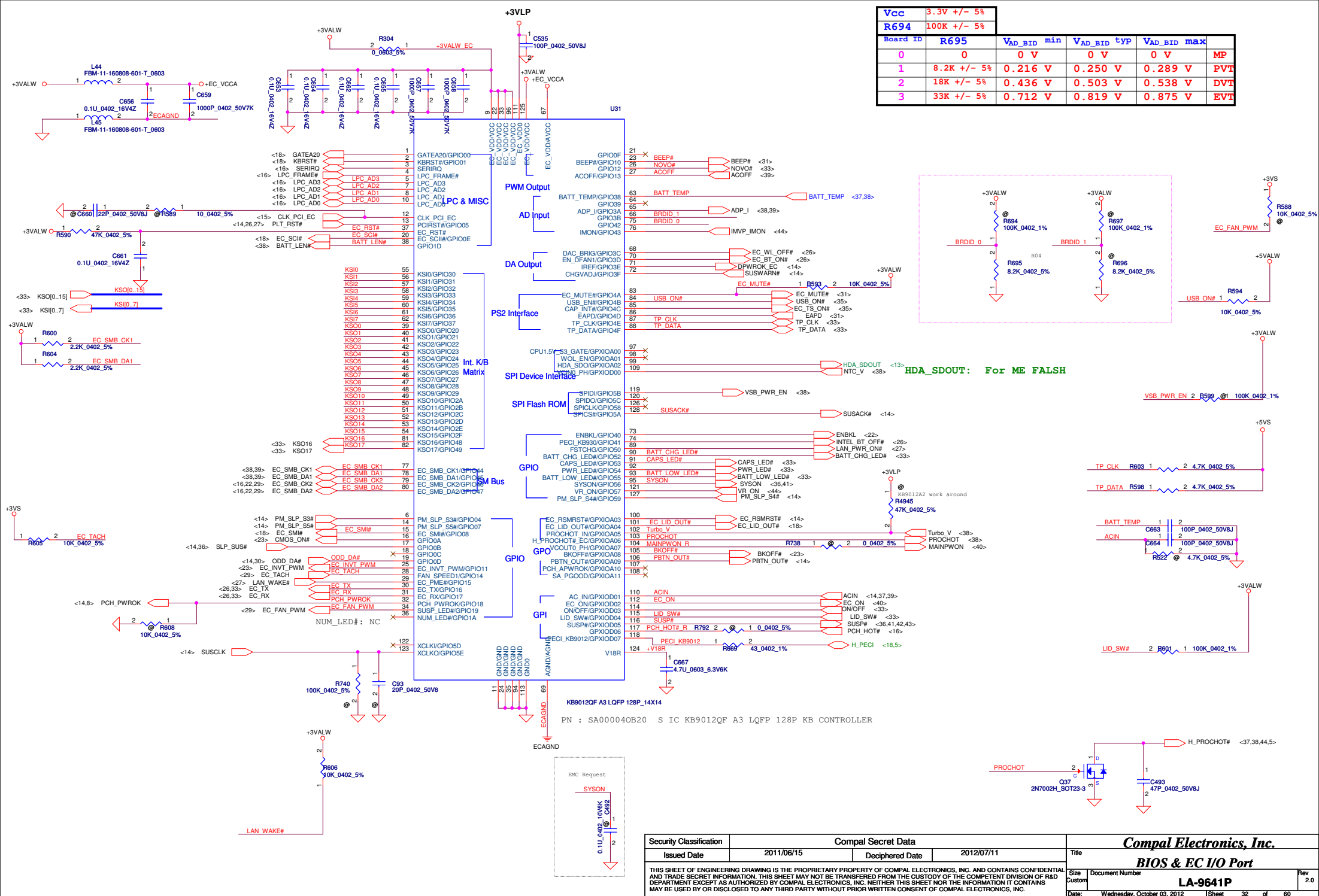


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				Size	Document Number	Rev
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CX20751
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

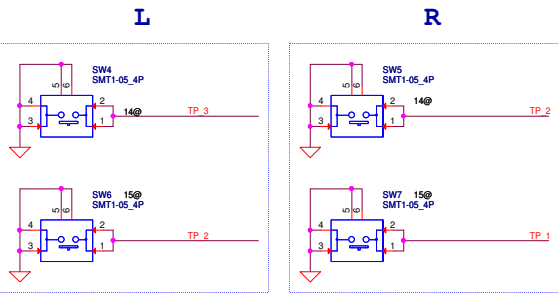
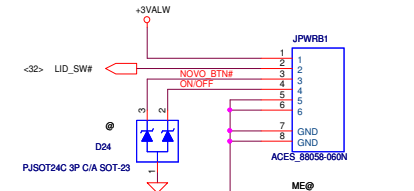
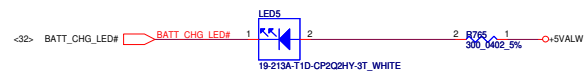
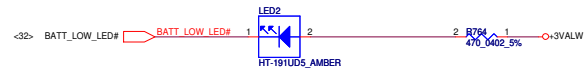
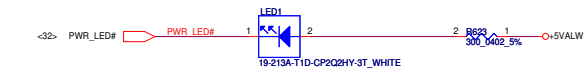
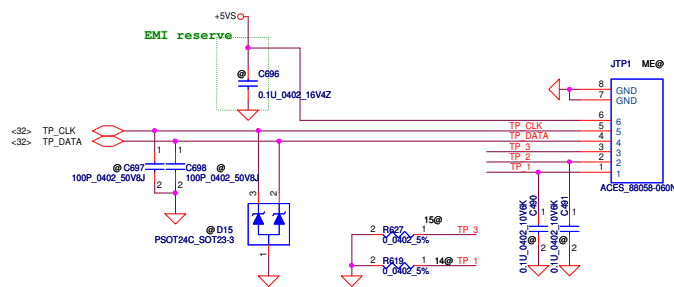
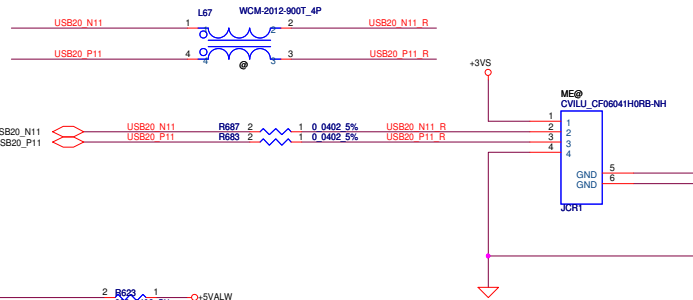
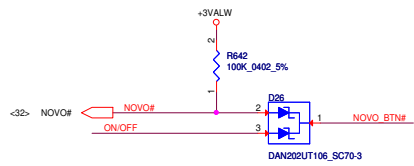
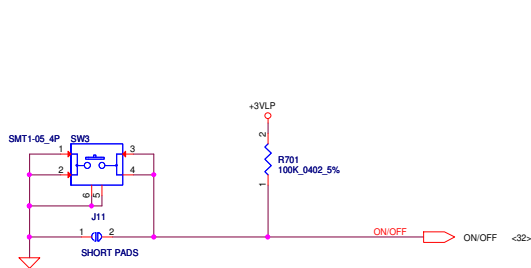
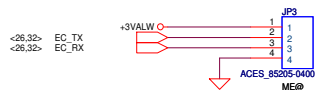
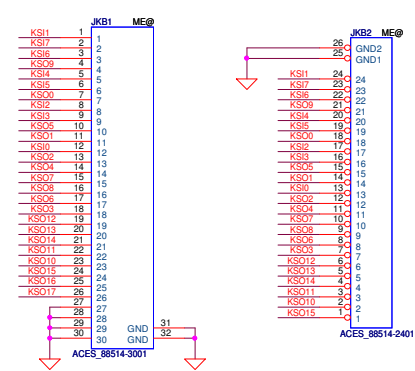


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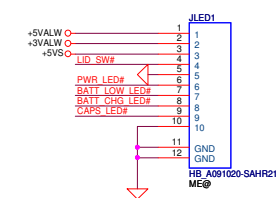
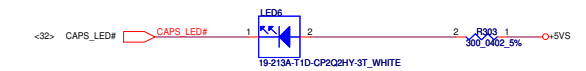


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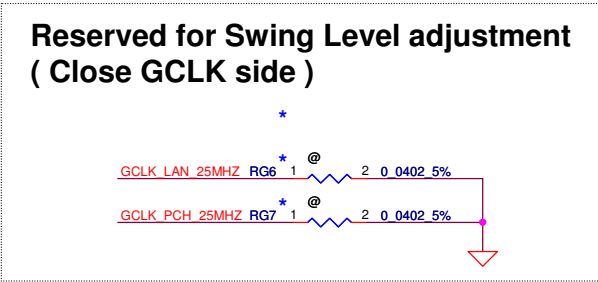
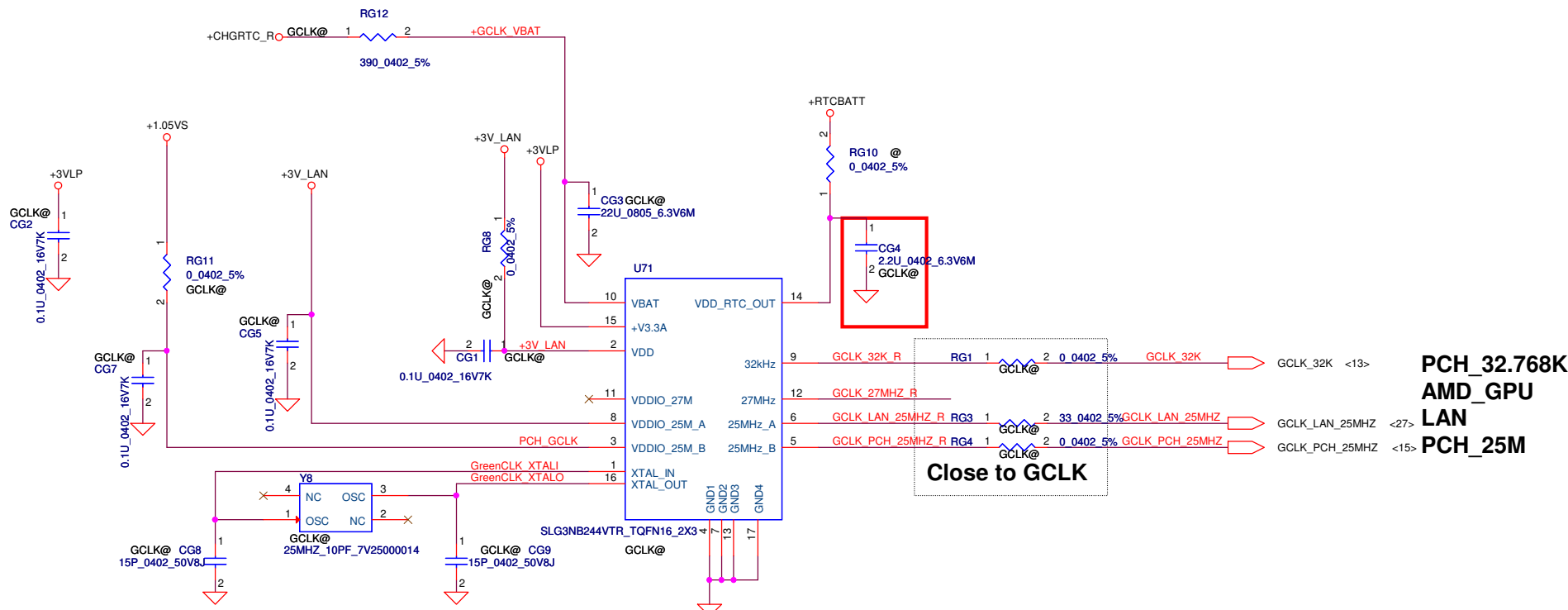
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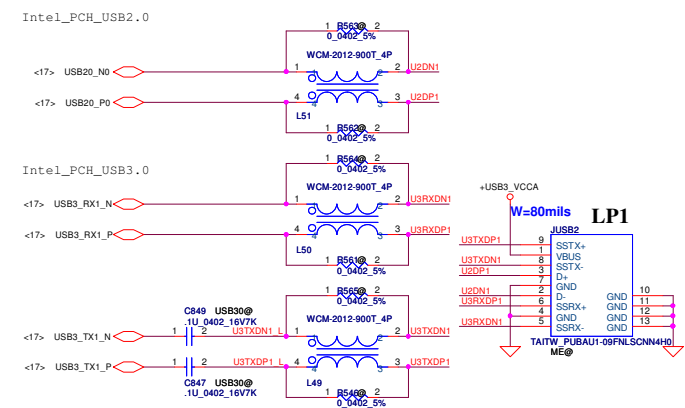
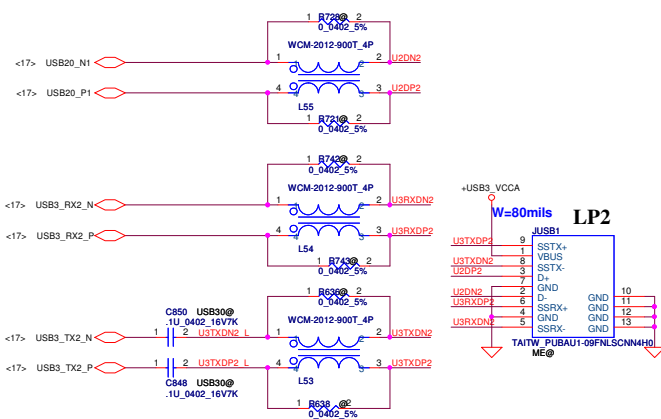
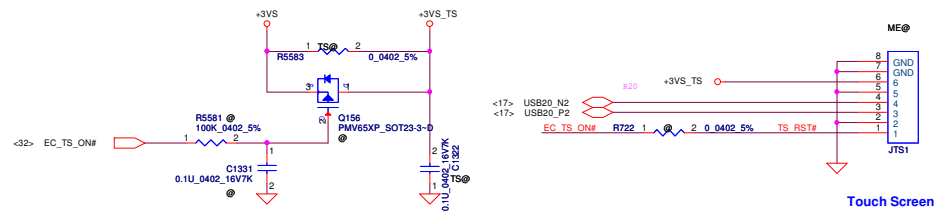
15"	14"
1 VCC	1 VCC
2 CLK	2 CLK
3 DAT	3 DAT
4 GND	4 L
5 L	5 R
6 R	6 GND



Green Clock

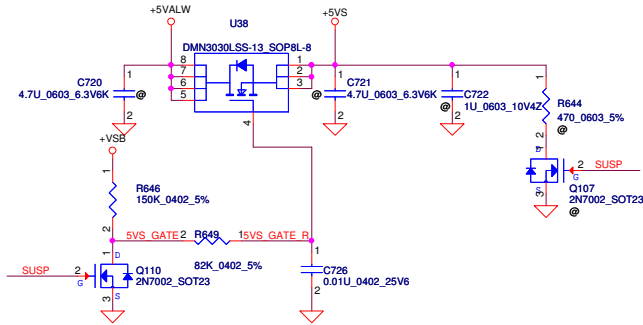


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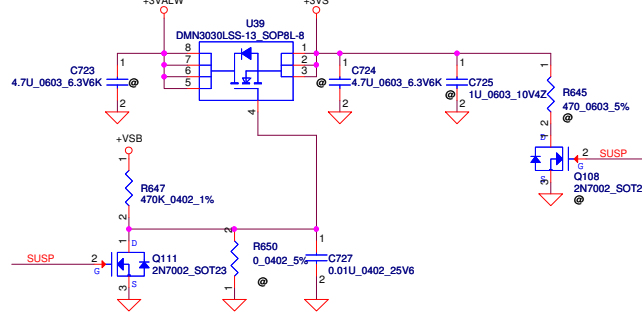
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				2.0	
Date:		Wednesday, October 03, 2012		Sheet 35 of 60	

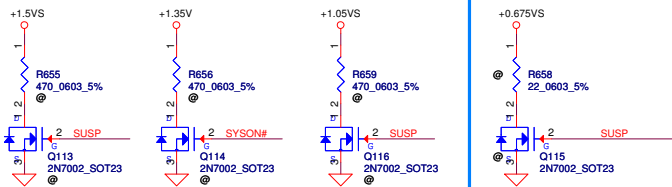
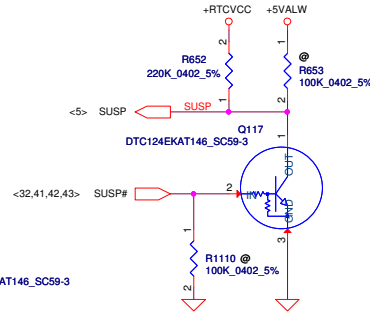
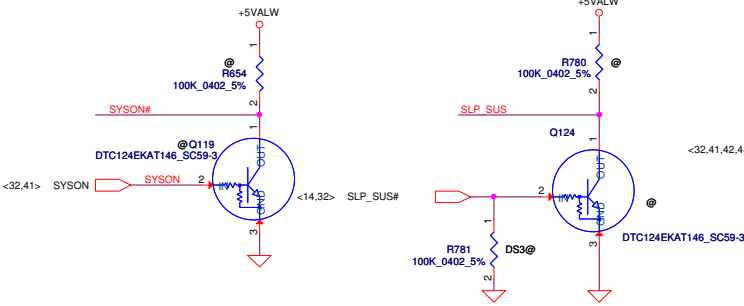
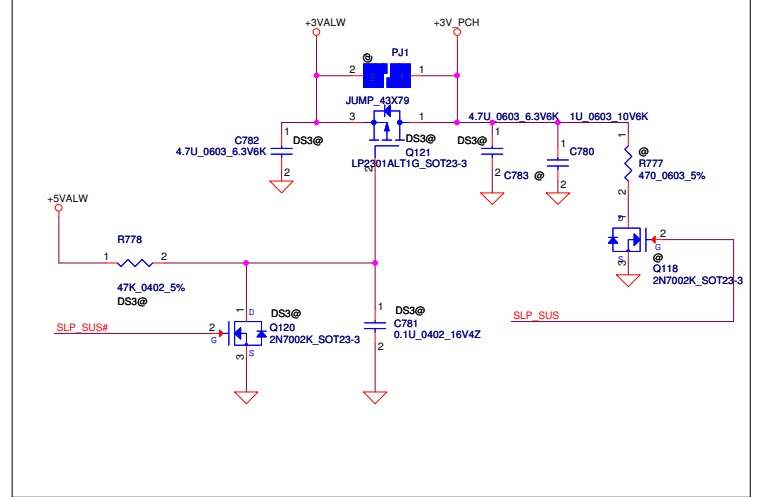
+5VALW TO +5VS



+3VALW TO +3VS



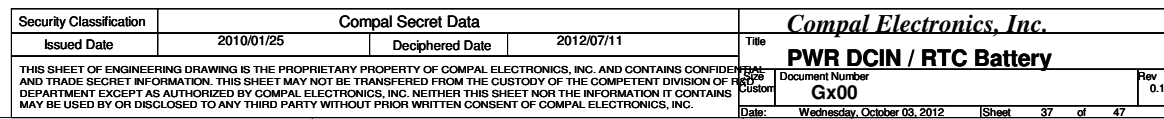
+3VALW TO +3VALW(PCH AUX Power)

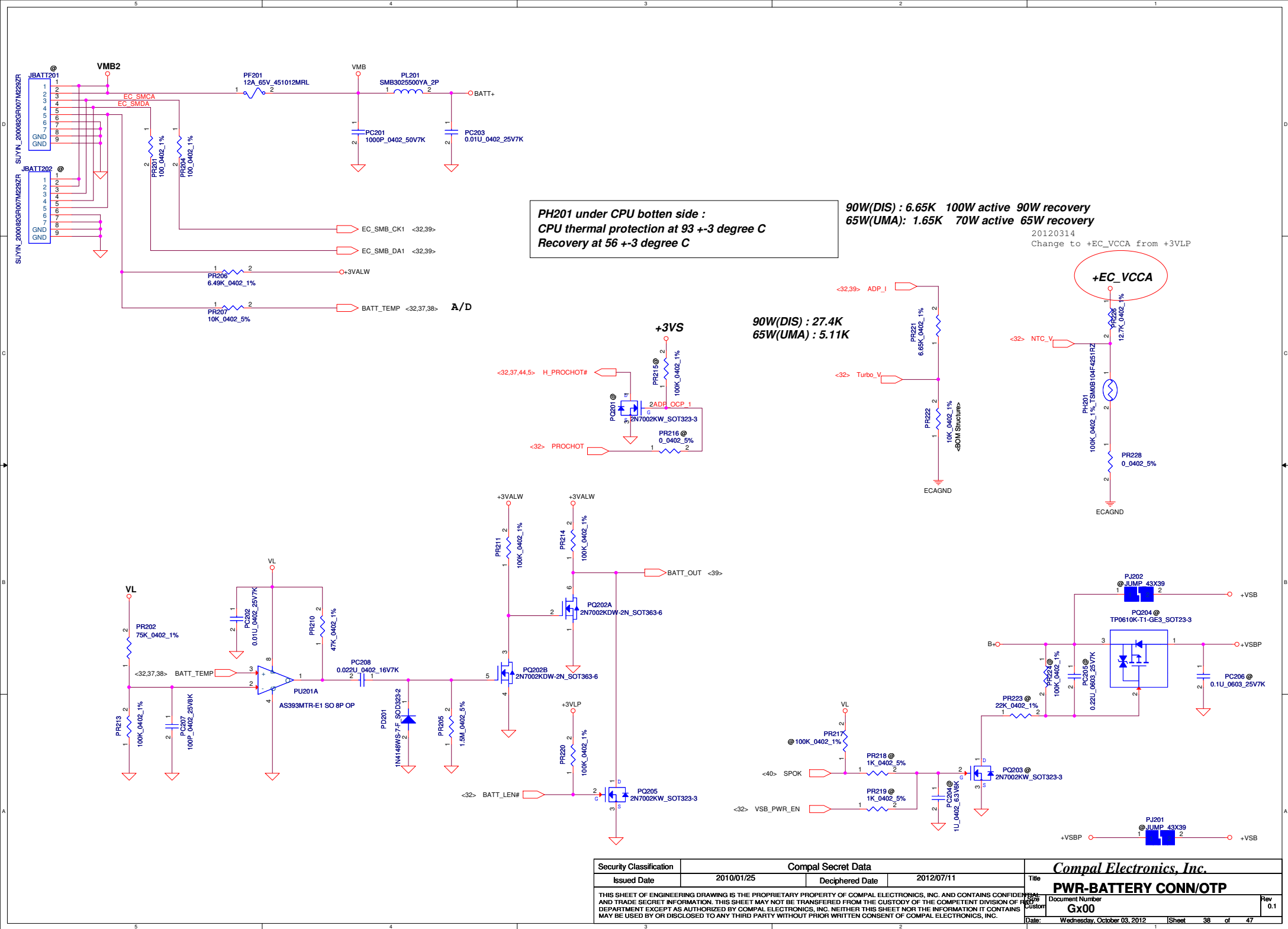


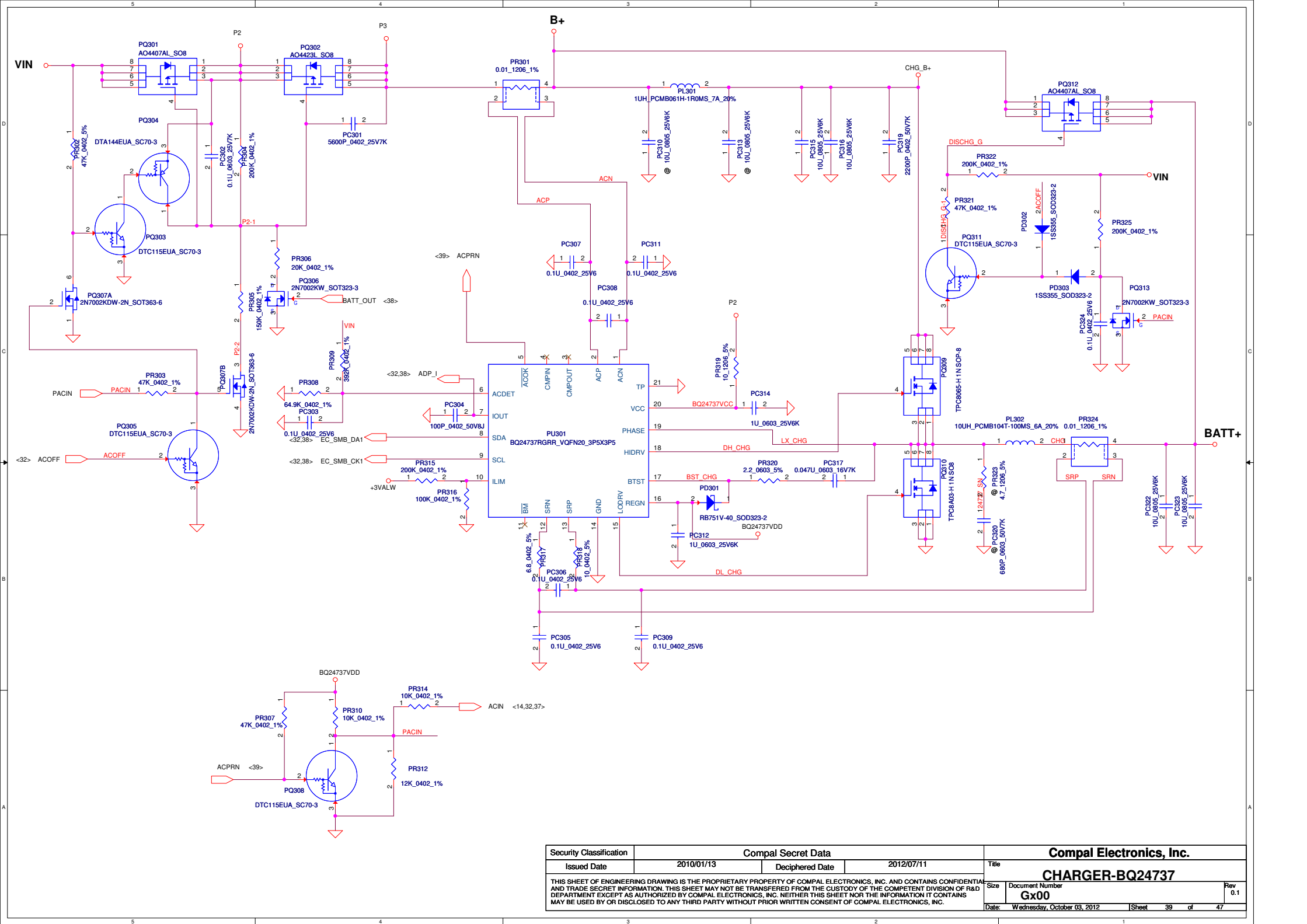
For Intel S3 Power Reduction.

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				Date: Wednesday, October 03, 2012	Sheet 36 of 60

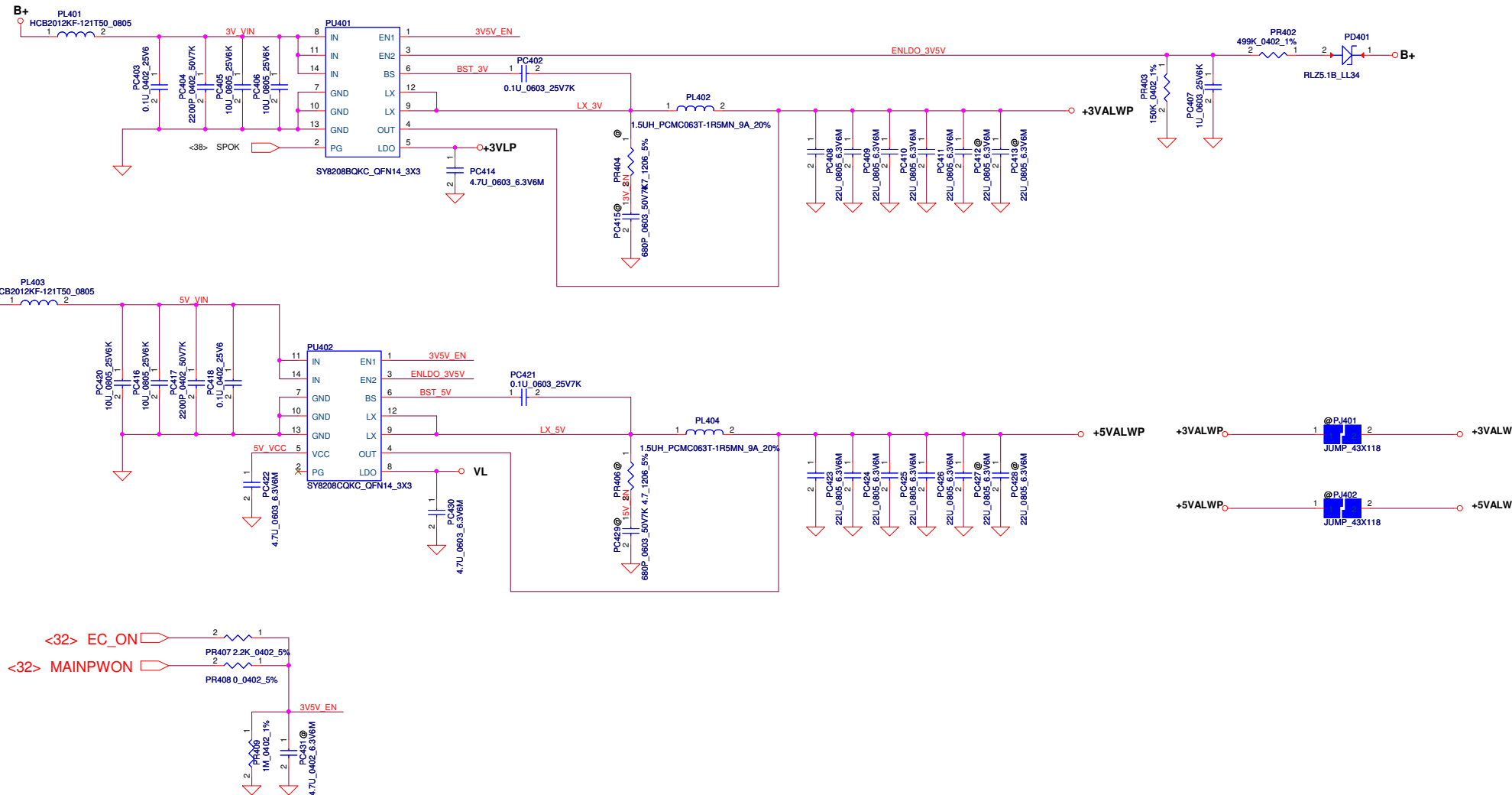
4602-Q04C-09R 4P P2.5 JDCIN101







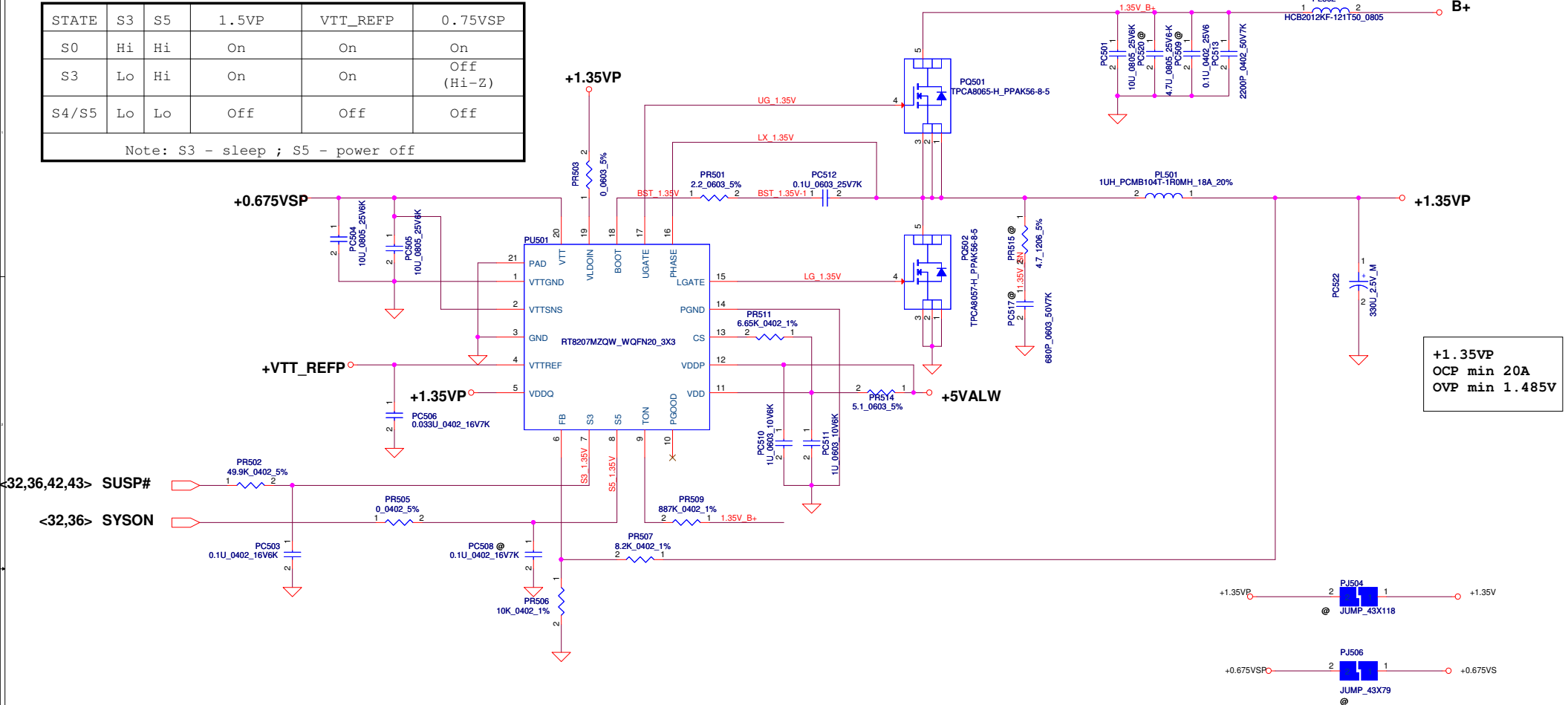
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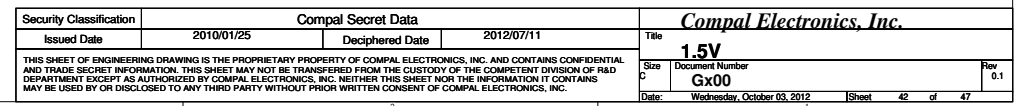
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2011/10/03				2014/12/31				PWR- 3VALWP/5VALWP			
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				Gx00				0.1			
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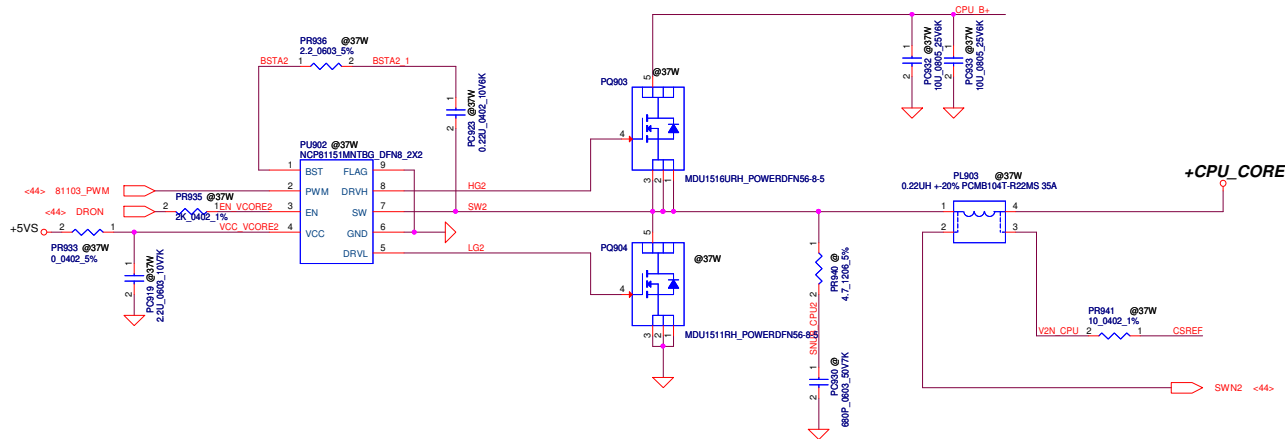
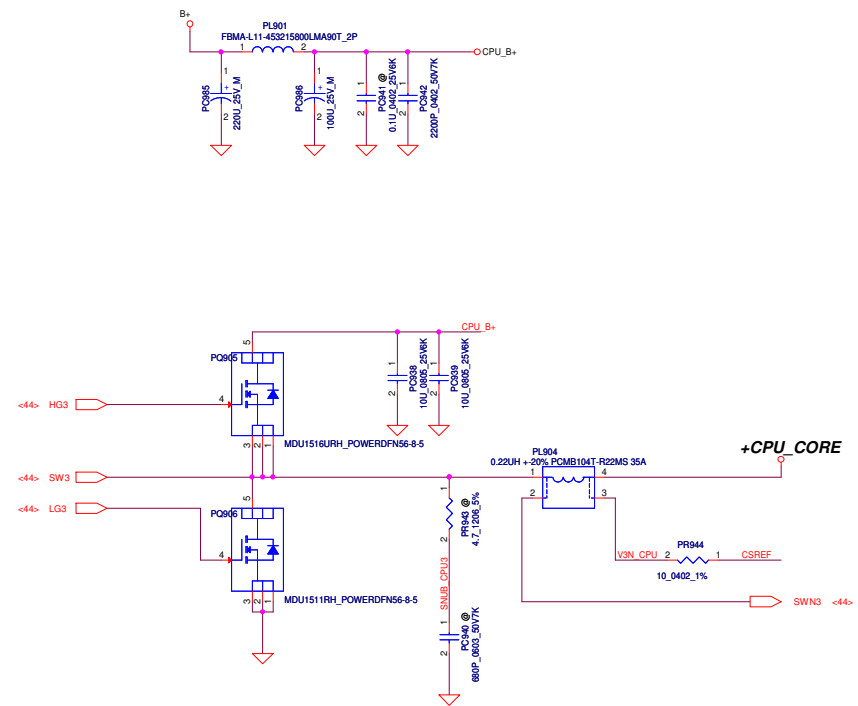
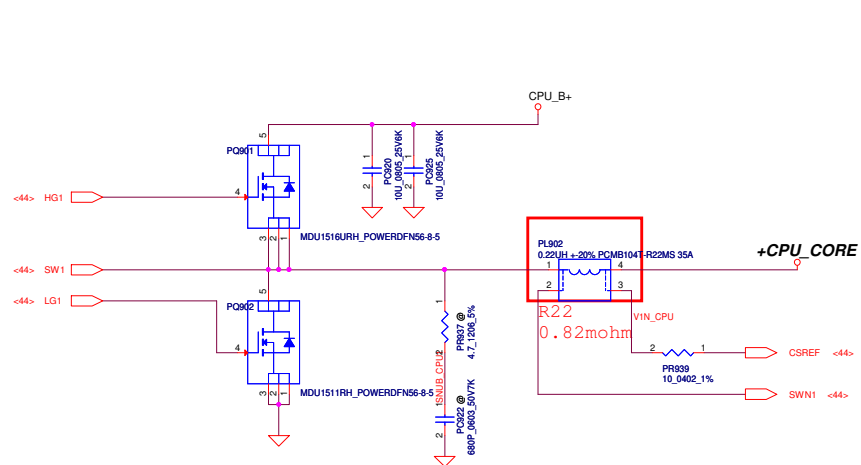
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off



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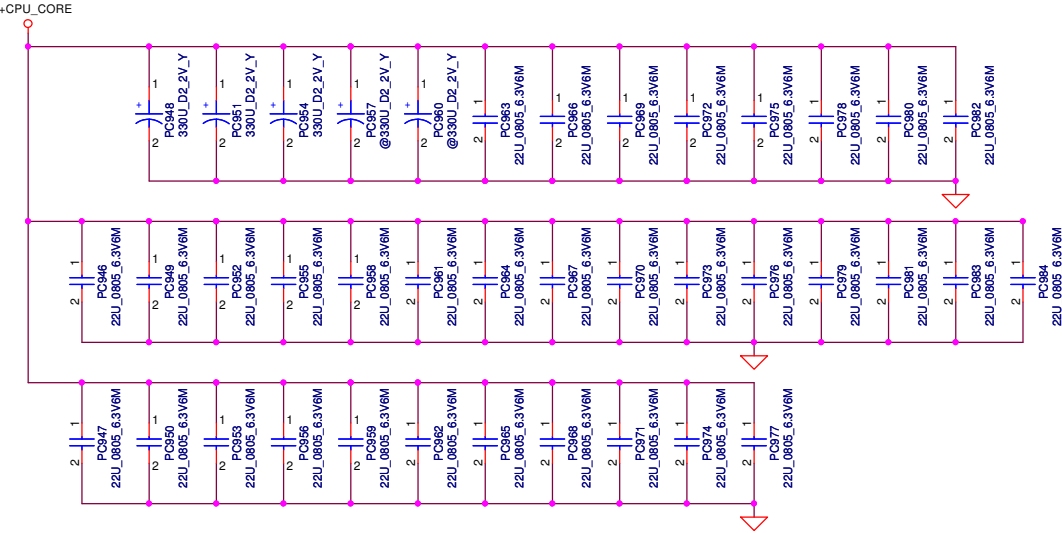
+CPU_CORE

3 X 330u/9m (47W)

2X330u/9m (37W)

34 X 22u/0805

34 X 22u/0805



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		Size	Document Number		Rev
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Item	Reason for change	PG#	Modify List	Date	Phase
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2					
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