

Compal Confidential

KALG1 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2009-03-02

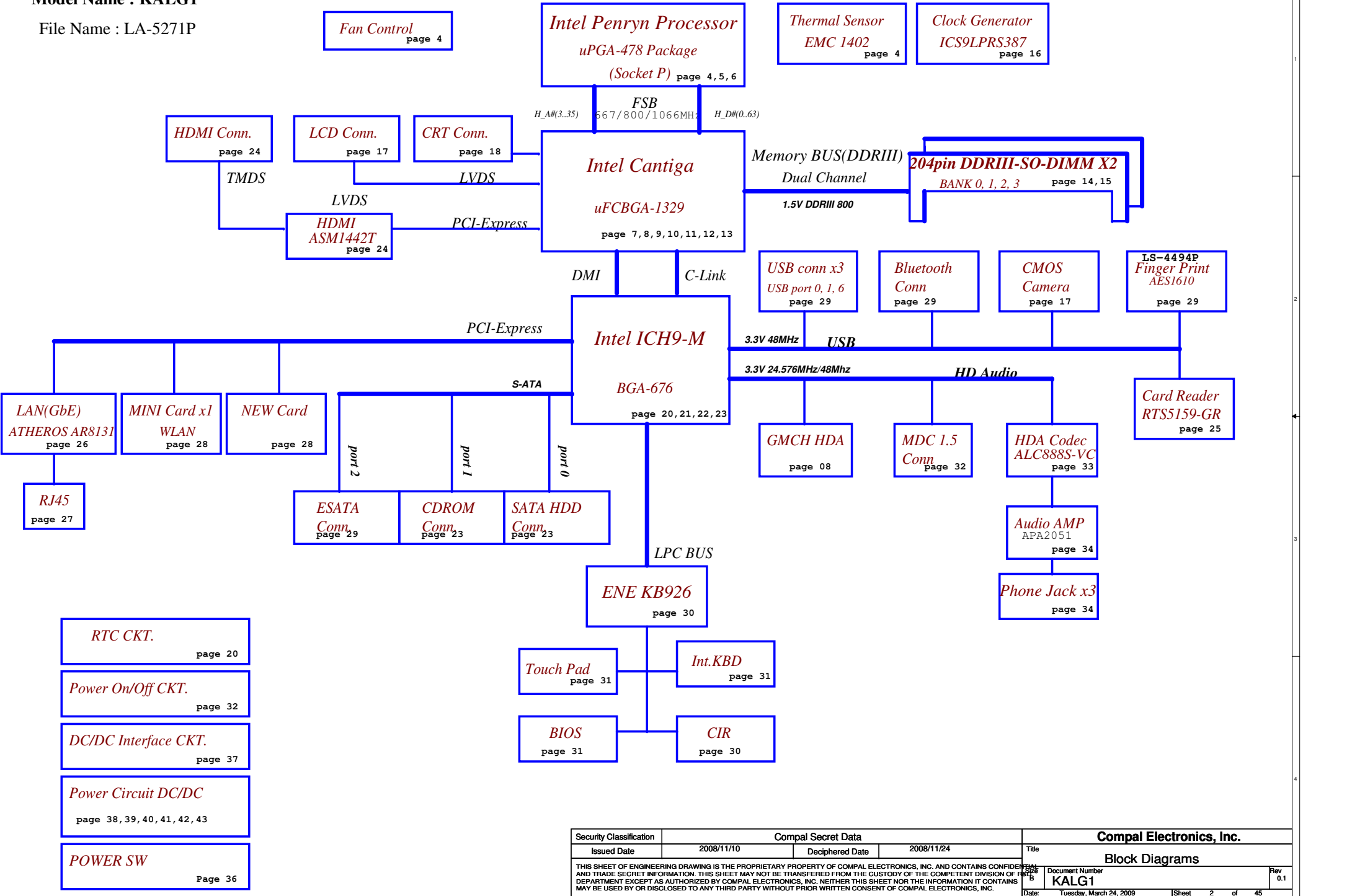
REV 02

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Issued Date	2008/11/10	Deciphered Date	2008/11/24	Title	Cover Page
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Model Name : KALG1

File Name : LA-5271P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75VS power rail for DDR3 terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for NB(LVDS)	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3V	3.3V power rail for SB	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail for SB	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 100X b

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS367, SLG8SP556V)	1101 001Xb
DDR3 DIMMA	1001 000Xb
DDR3 DIMMB	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1				
2				
3				
4				
5				
6				
7				

BOARD ID Table

Board ID	PCB Revision
0	PCB 08Y LA-5271P REV0 M/B
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

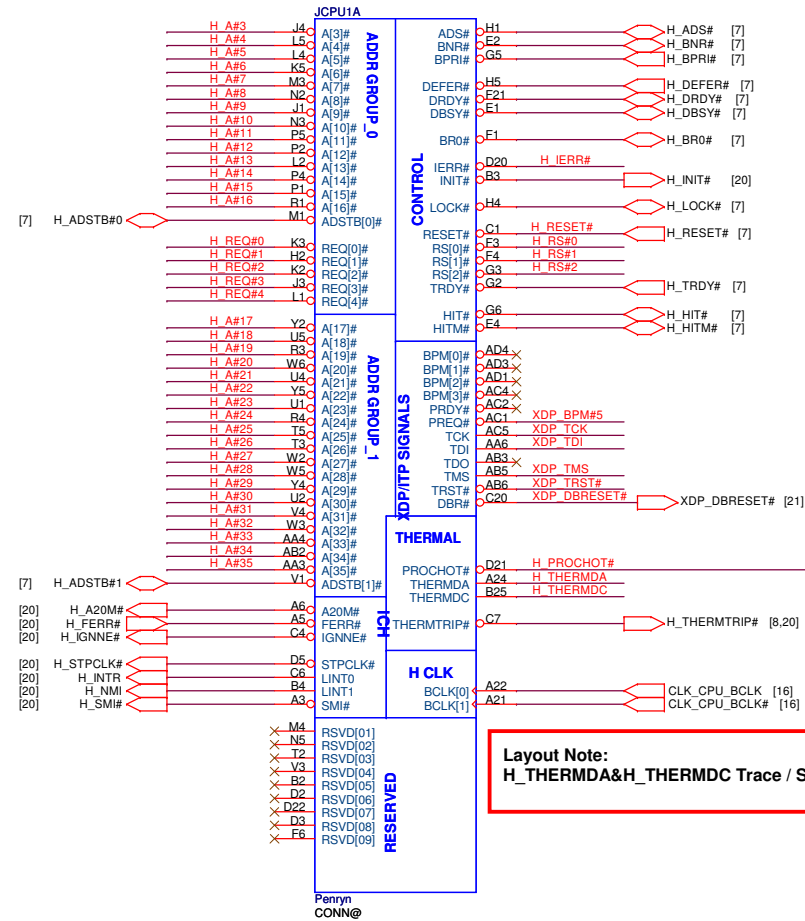
BTO Item	BOM Structure
GL40	GL40@
GM45	GM45@

BOM Configuration Table

Project	BOM Configuration
KALG1-GM45	GM45@/KALG1@/KAL90_G0_90+@
KALG1-GL40	GL40@/KALG1@/KAL90_G0_90+@

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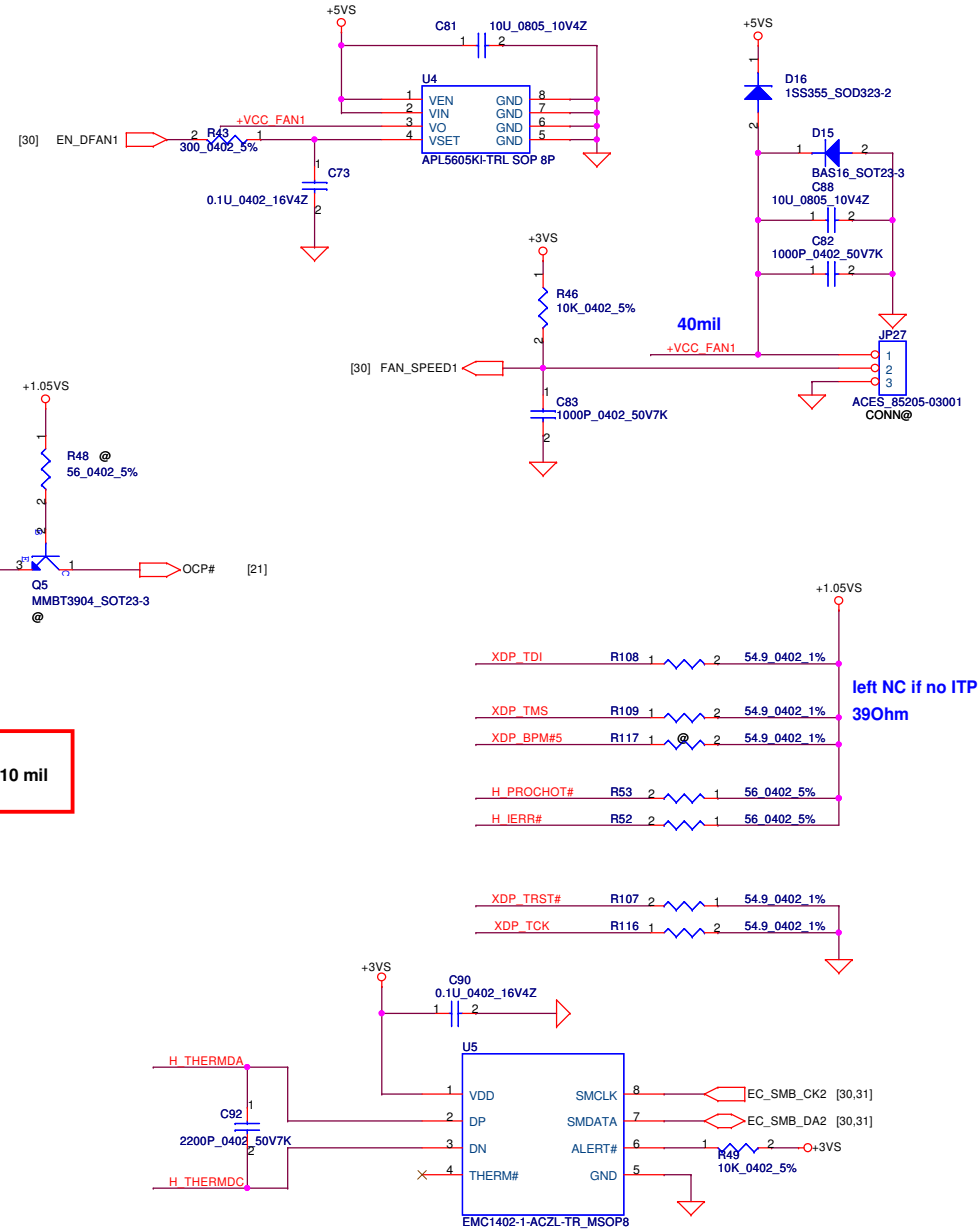
[7] H_A# [3..35]  H_A# [3..35]
 [7] H_REQ# [0..4]  H_REQ# [0..4]
 [7] H_RS# [0..2]  H_RS# [0..2]



Layout Note:
 H_THERMDA&H_THERMDC Trace / Space = 10 / 10 mil

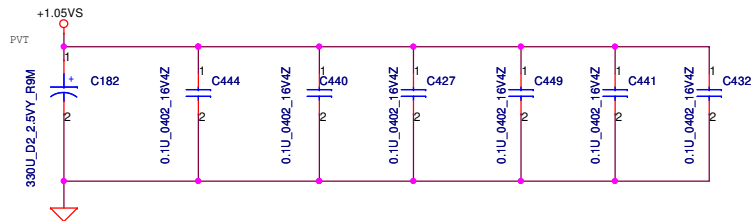
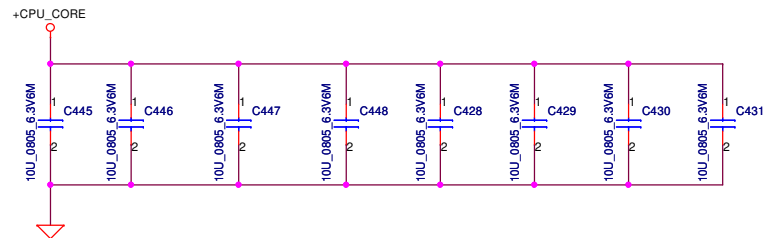
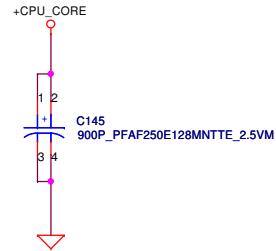
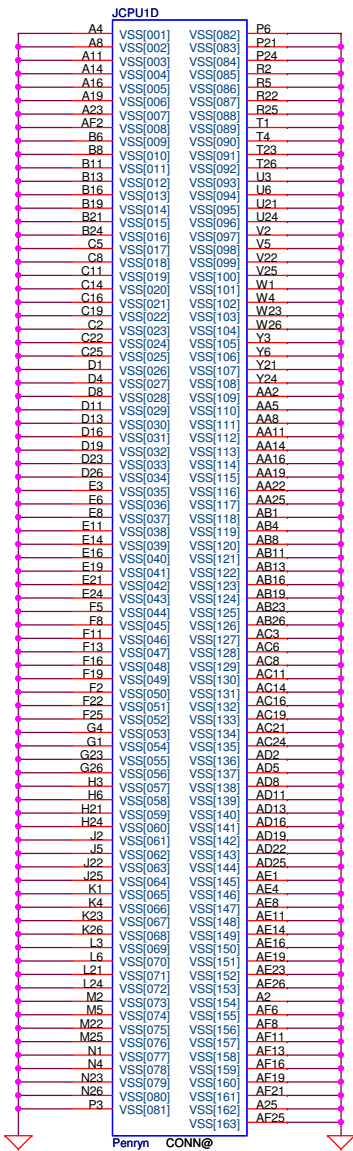
BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166

FAN1 Conn

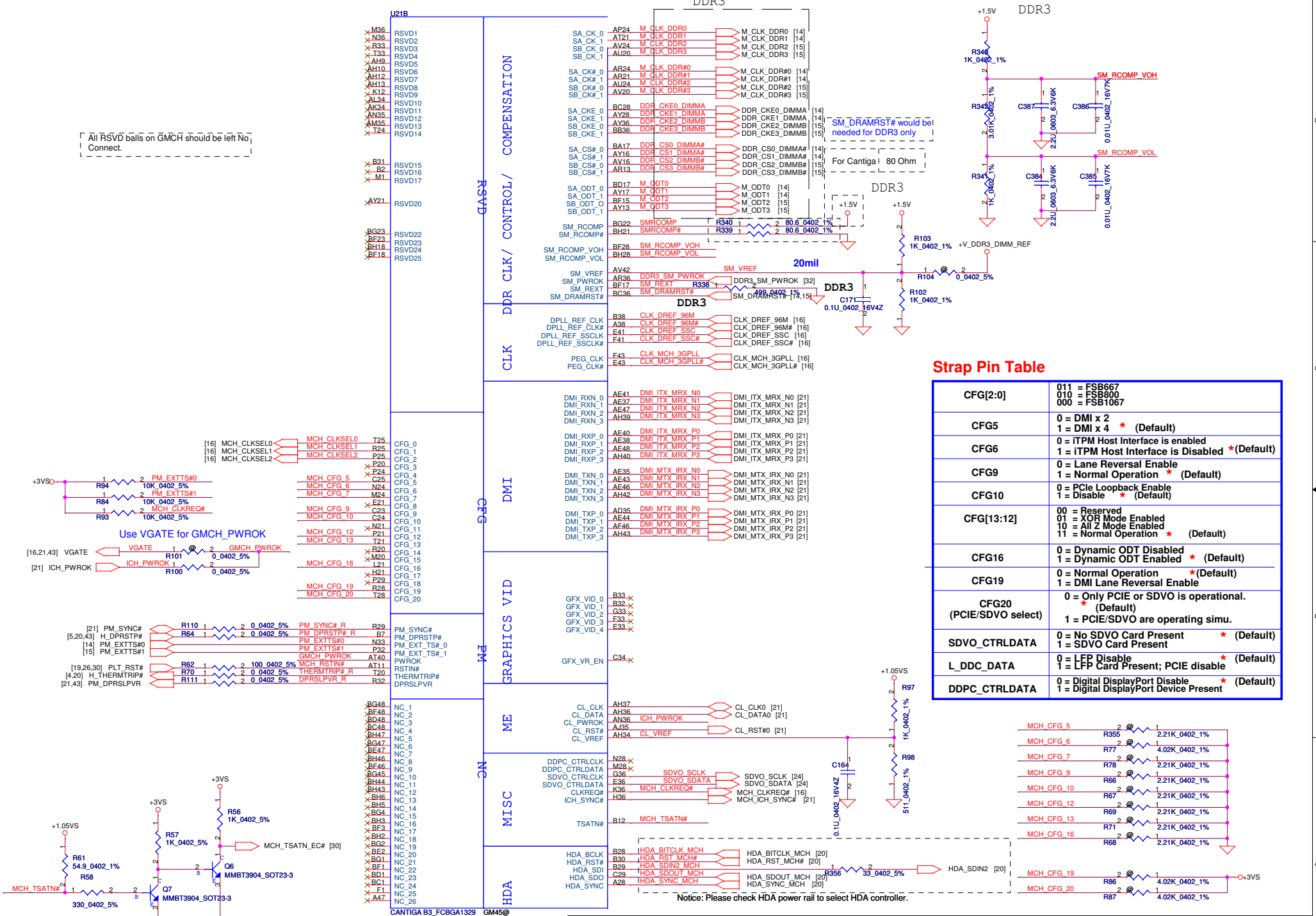


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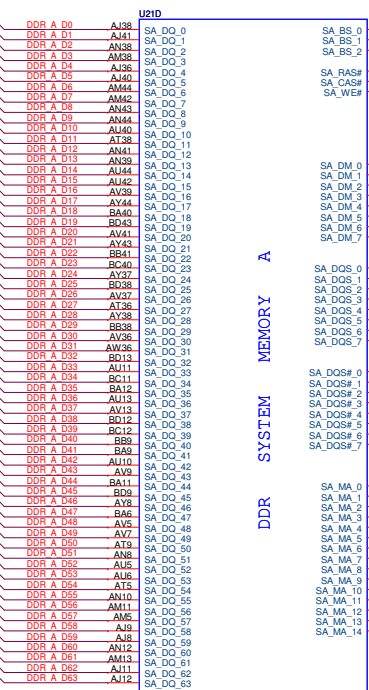
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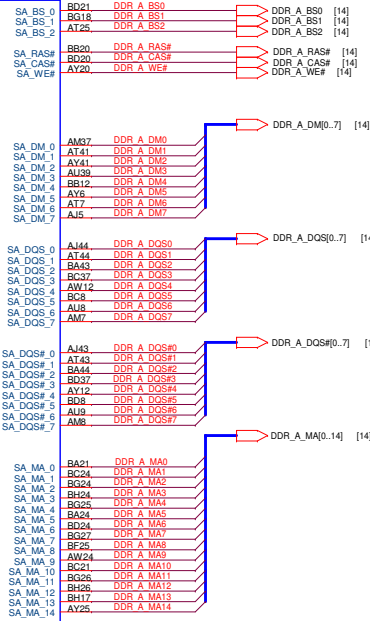
Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. (Default) 1 = PCIe/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present 1 = SDVO Card Present * (Default)
L_DDC_DATA	0 = LFP Disable 1 = All Card Present; PCIe disable * (Default)
DDPC_CTRLDATA	0 = Digital DisplayPort Disable 1 = Digital DisplayPort Device Present * (Default)

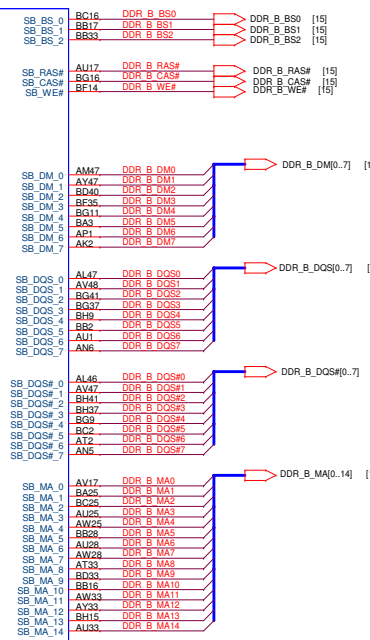
[14] DDR_A_D[0..63]



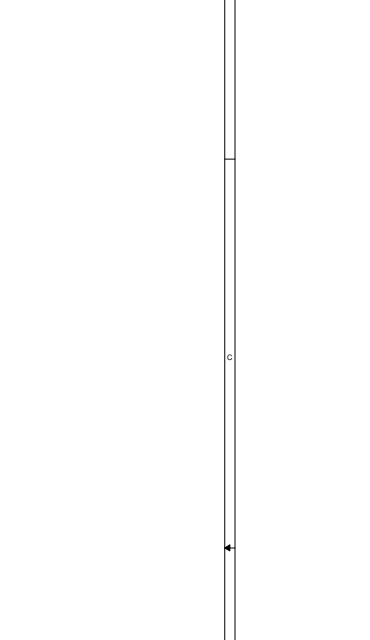
DDR SYSTEM MEMORY A



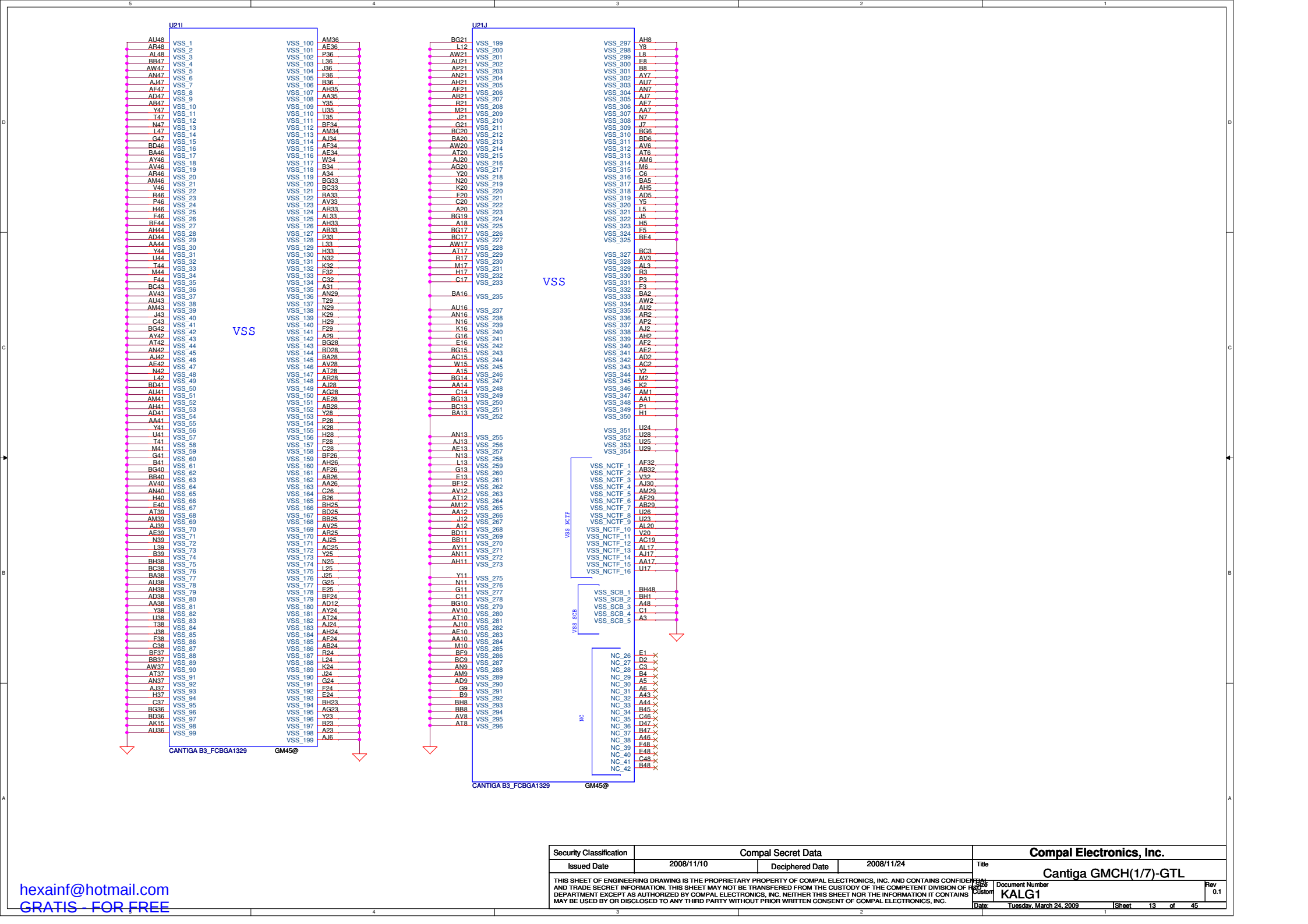
DDR SYSTEM MEMORY B

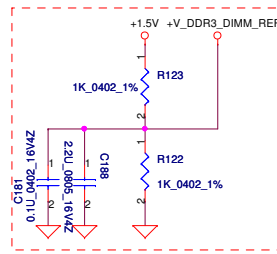
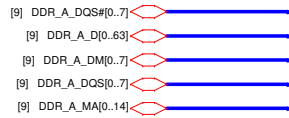


DDR SYSTEM MEMORY B



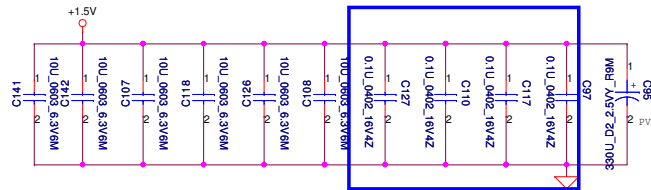
DDR SYSTEM MEMORY B



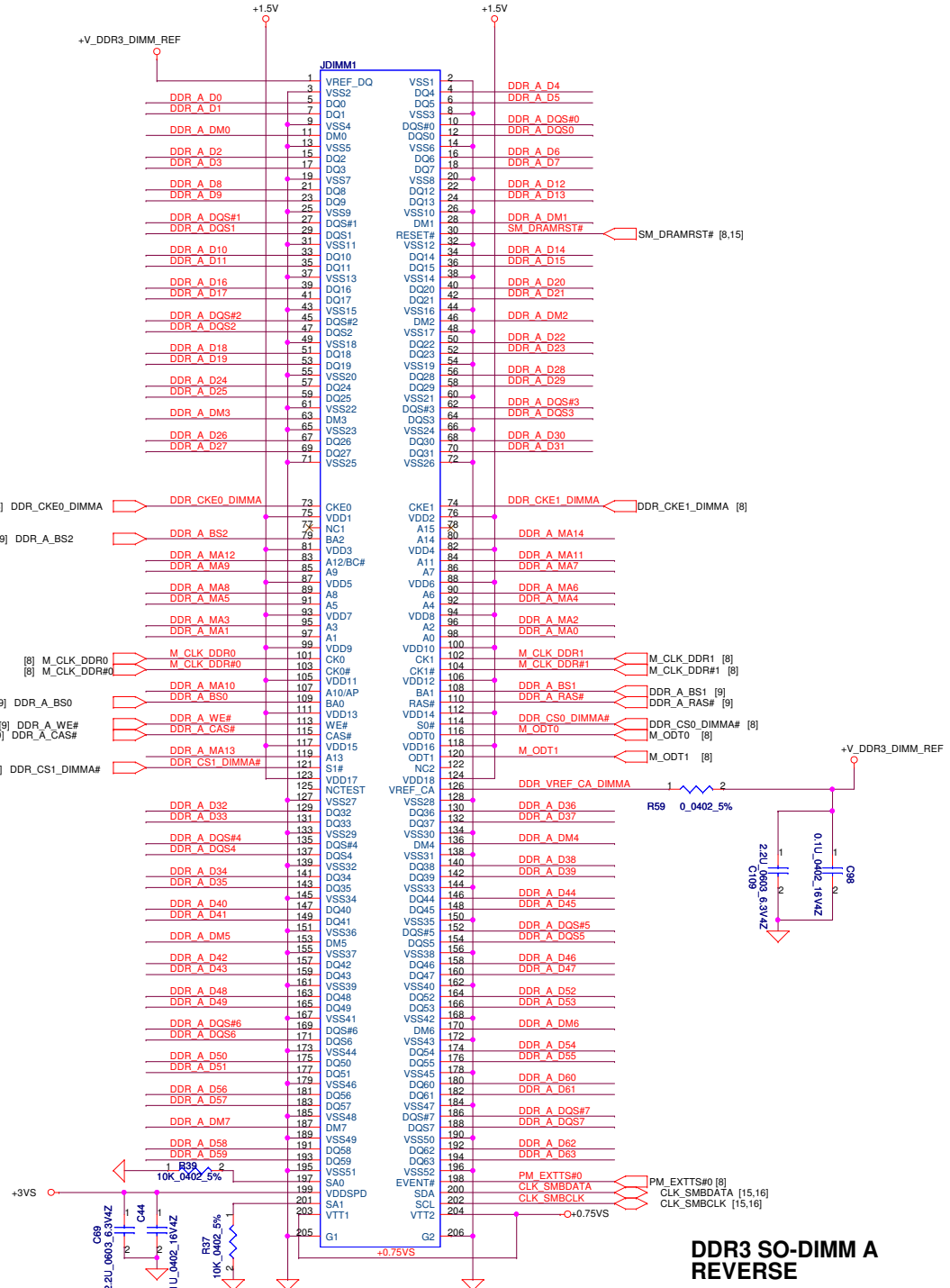
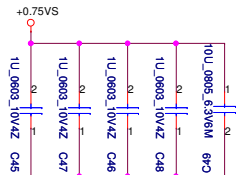


Layout Note:
Place near JP4

Layout Note: Place these 4 Caps near Command
and Control signals of DIMM

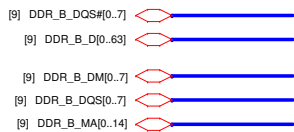


Layout Note:
Place near JP4.203 & JP4.204



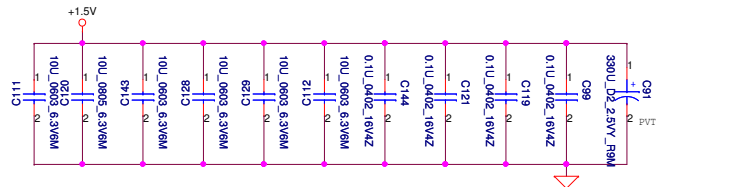
DDR3 SO-DIMM A REVERSE

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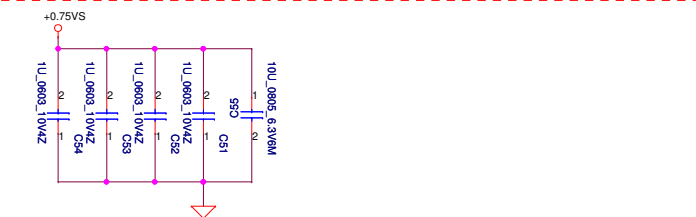


Layout Note:
Place near JP5

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMB



Layout Note:
Place near JP5.203 & JP5.204

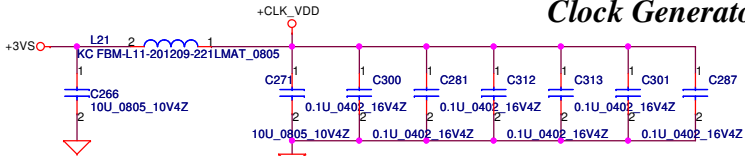
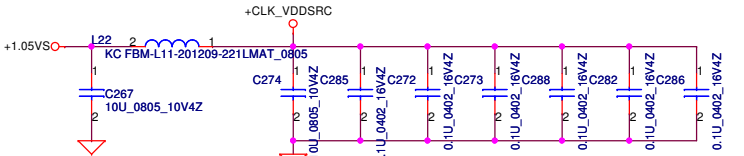
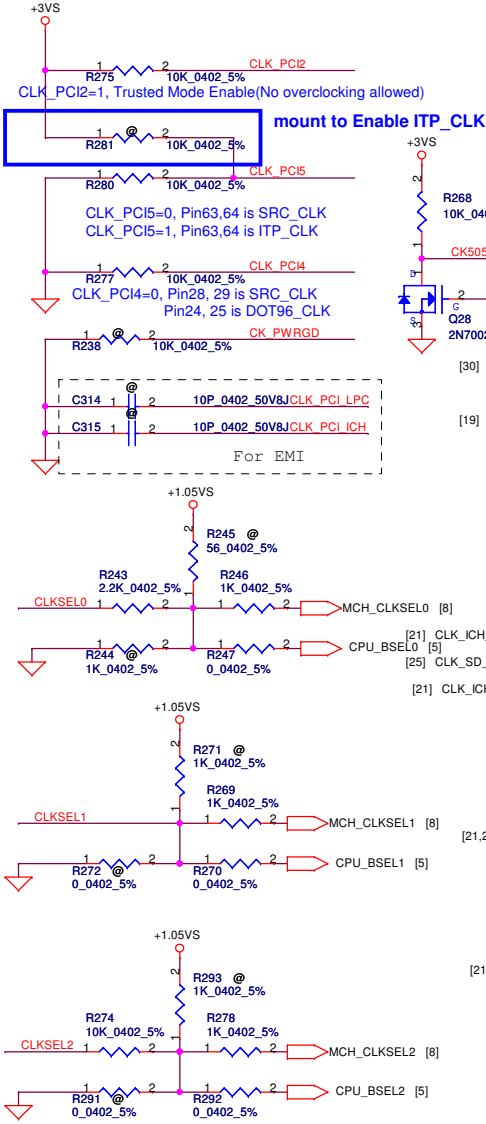


FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

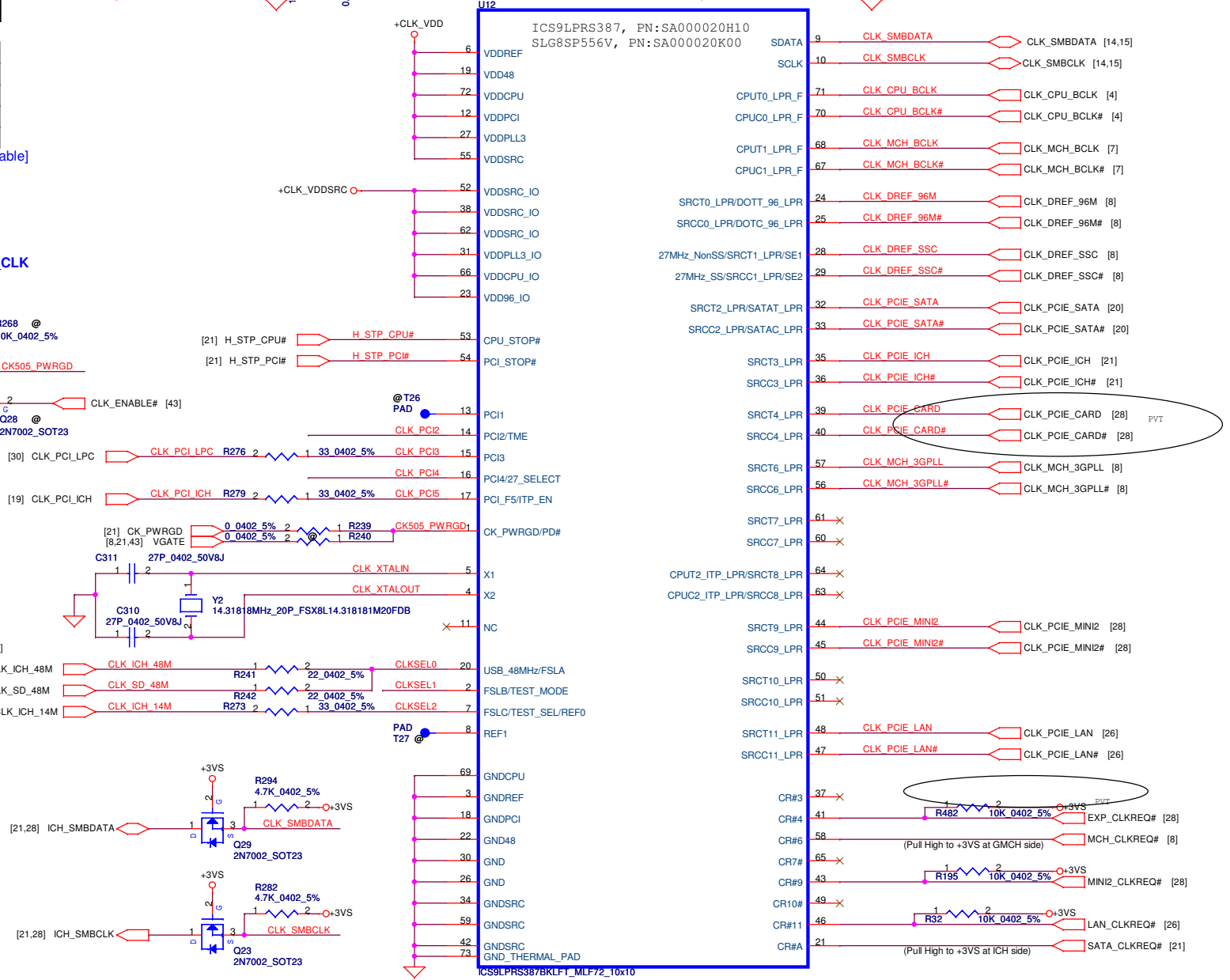
Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

SRC7(VGA_CLK): Discrete VGA[Enable] UMA[Disable]

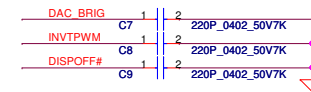
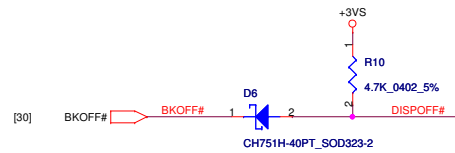
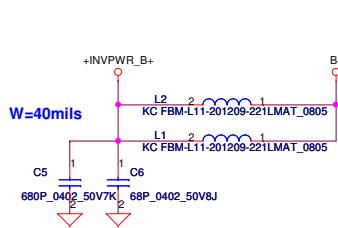
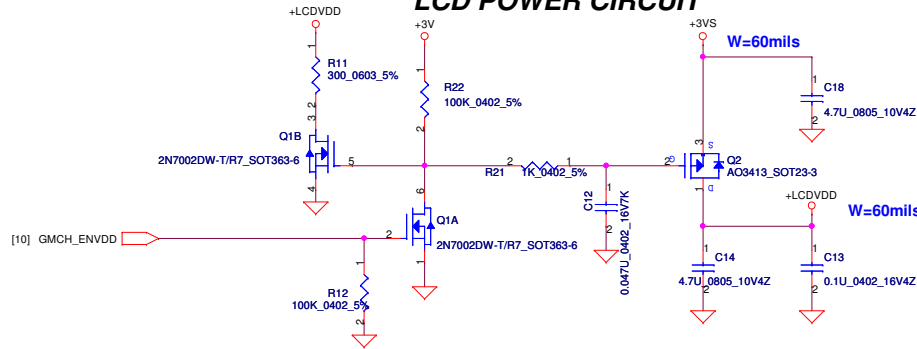


Clock Generator

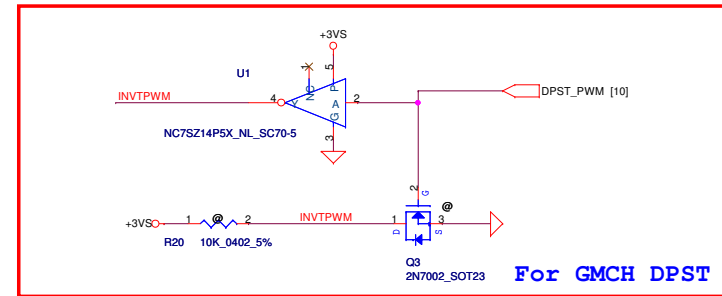
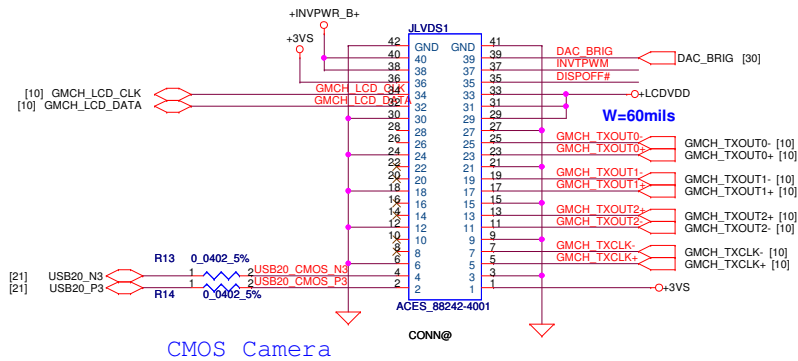


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LCD POWER CIRCUIT

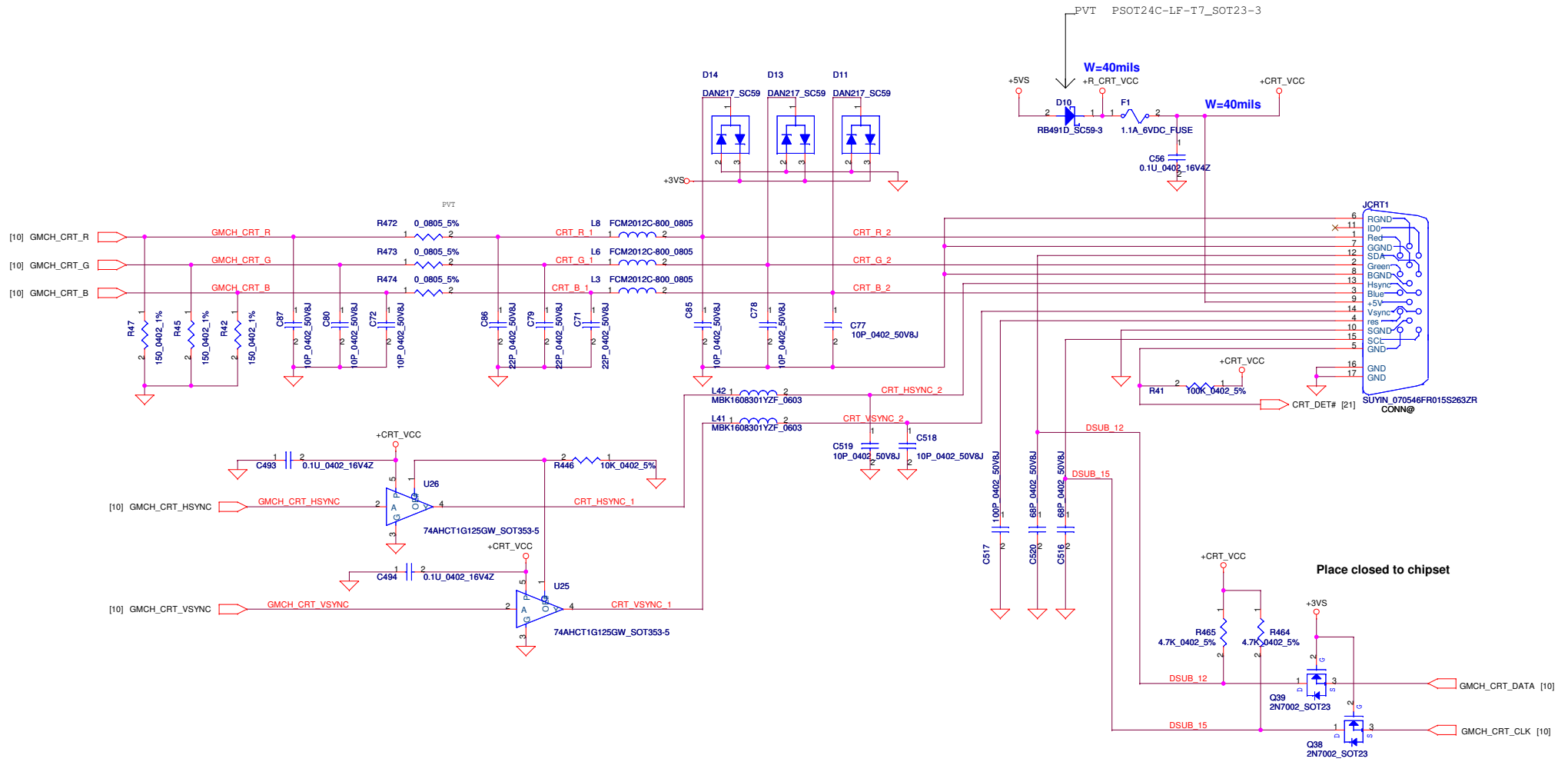


LCD/PANEL BD. Conn.

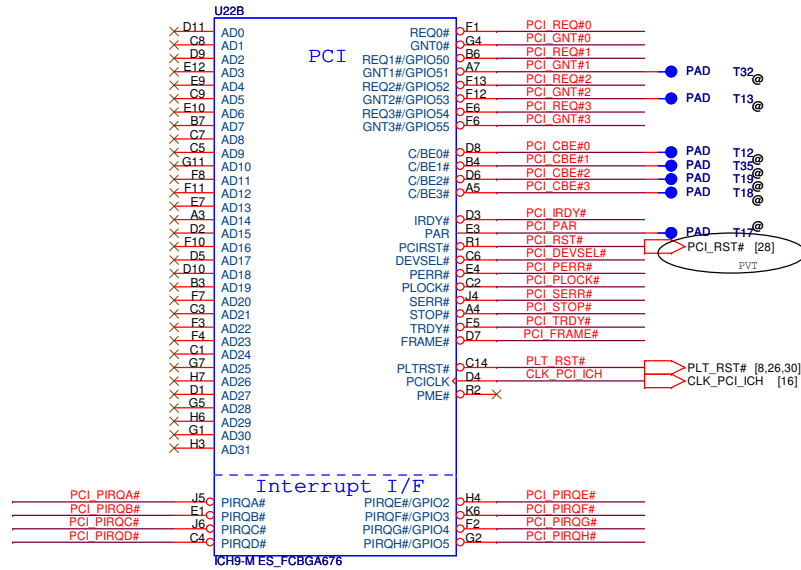
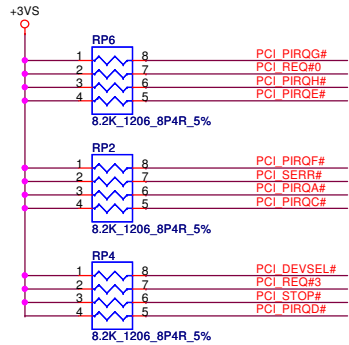
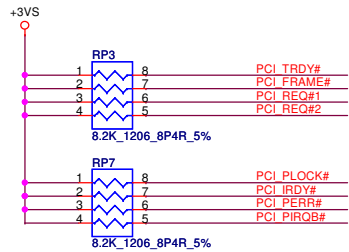


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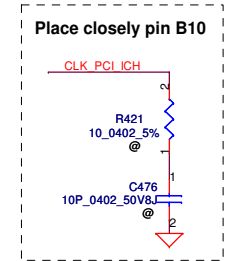
CRT Connector



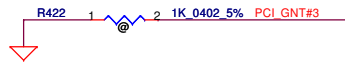
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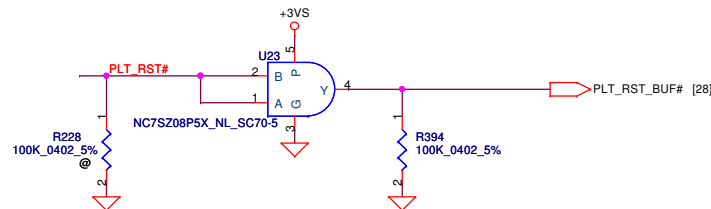
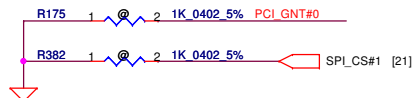
DMI for ESI-compatible operation
PCI_GNT#1 Low= DMI for ESI-compatible operation
 High= Default* (Internal pull-up)



A16 Swap Override Strap
PCI_GNT#3 Low= A16 swap override Enable
 High= Default*



Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

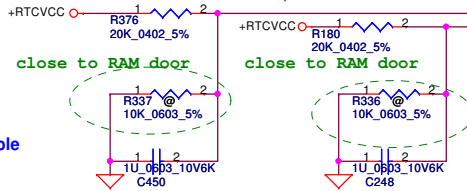
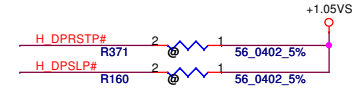


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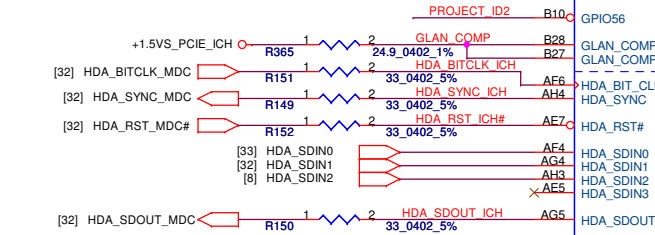
CMOS Settings		R337
Clear CMOS		SHORT
Keep CMOS		OPEN

TPM Settings		R336
Clear ME RTC Registers		SHORT
Keep ME RTC Registers		OPEN

Reset r1290 for power on then shut down issue

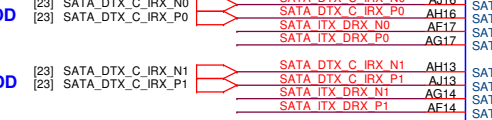


High = Internal VR Enable



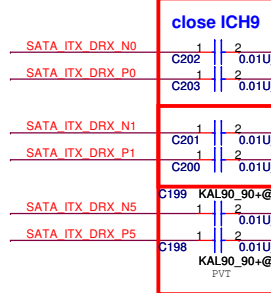
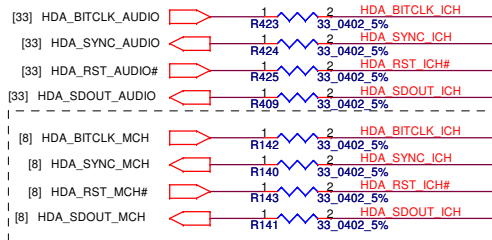
SATA for HDD

SATA for ODD



HDA for AUDIO

HDA for GMCH



close ICH9

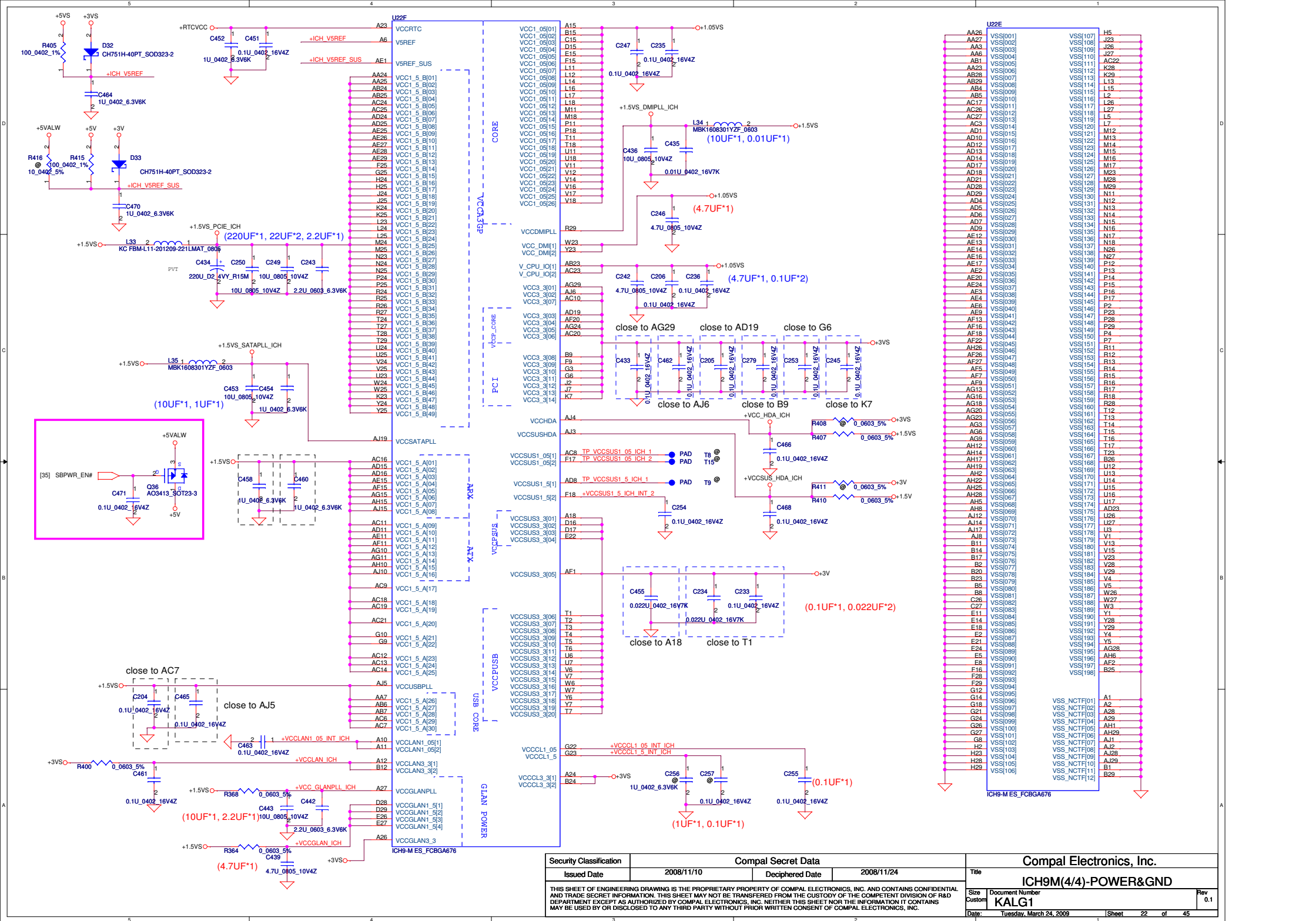
Flash Descriptor Security Override Strap
GPIO33 Low= Descriptor Security override
High= Default* (Internal pull-up)

XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

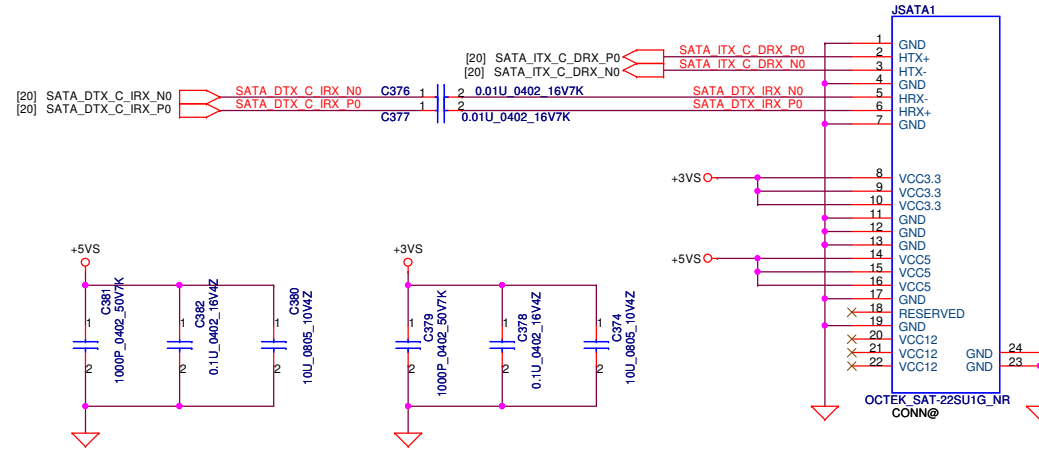
Security Classification		Compal Secret Data	
Issued Date	2008/11/10	Deciphered Date	2008/11/24

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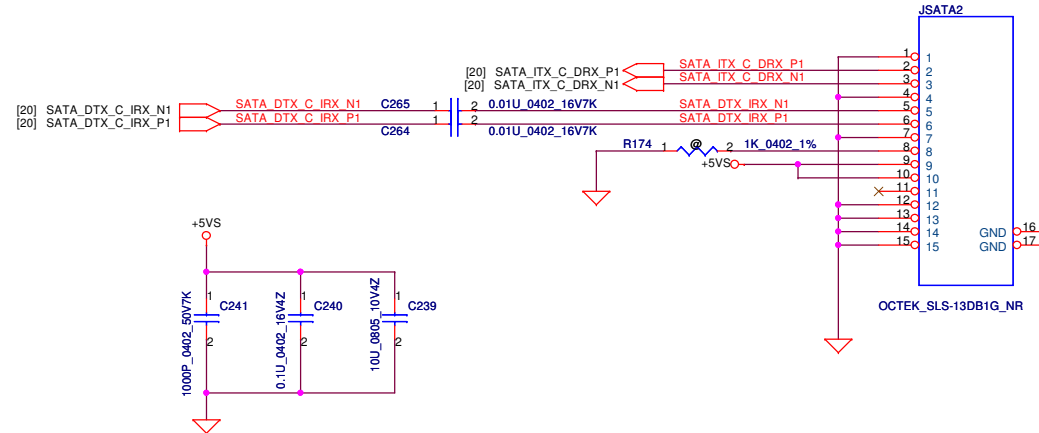
Compal Electronics, Inc.			
Title			
ICH9M(2/4)-LAN, IDELPC, RTC			
Size	Document Number	Rev	
Custom	KALG1	0.1	
Date:	Tuesday, March 24, 2009	Sheet	20 of 45



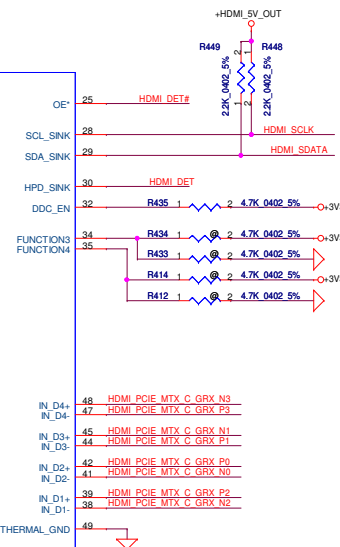
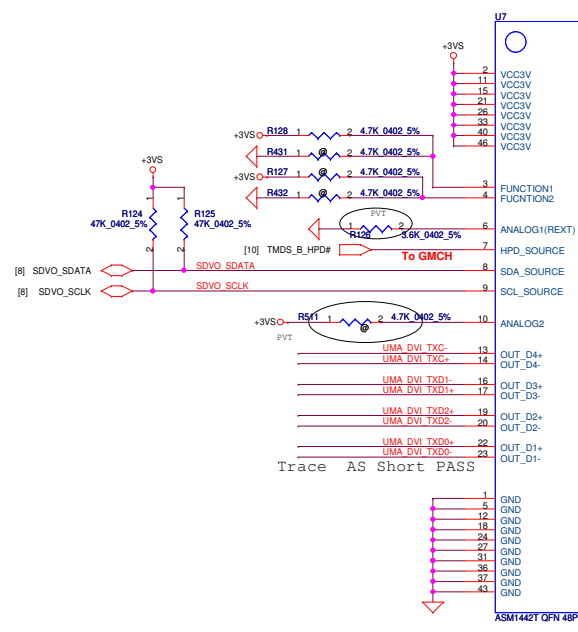
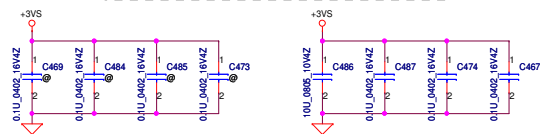
SATA HDD Conn.



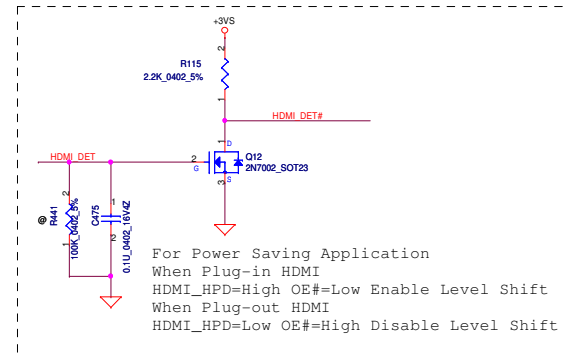
SATA ODD Conn.



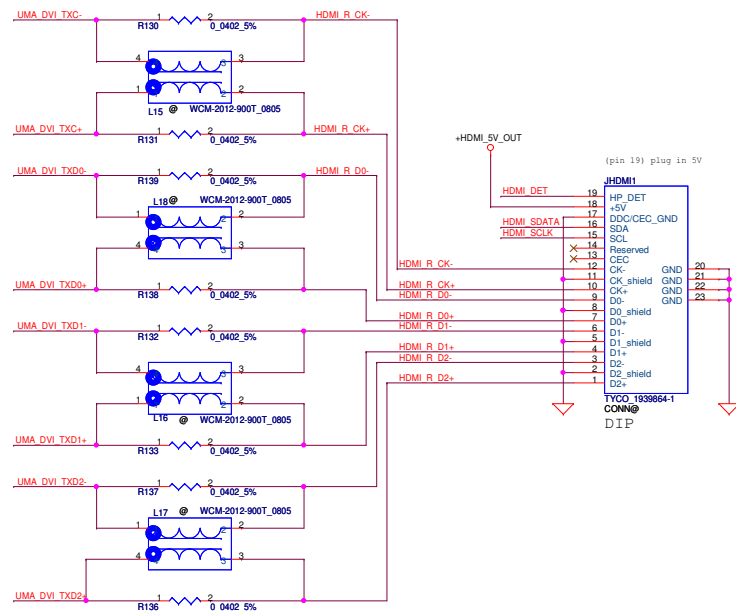
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Issued Date	2008/11/10	Deciphered Date	2008/11/24	Title	
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				Date:	Tuesday, March 24, 2009
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				Rev	0.1



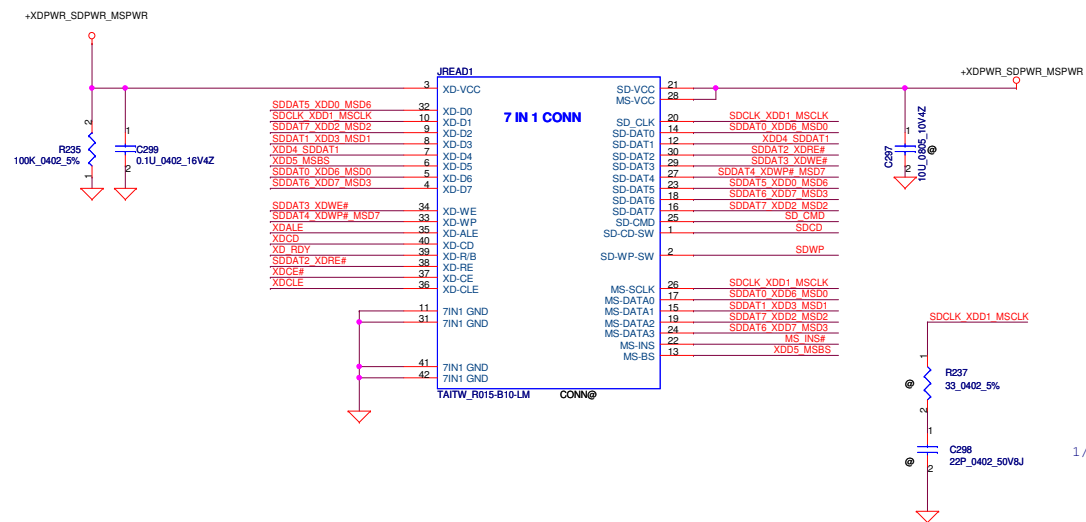
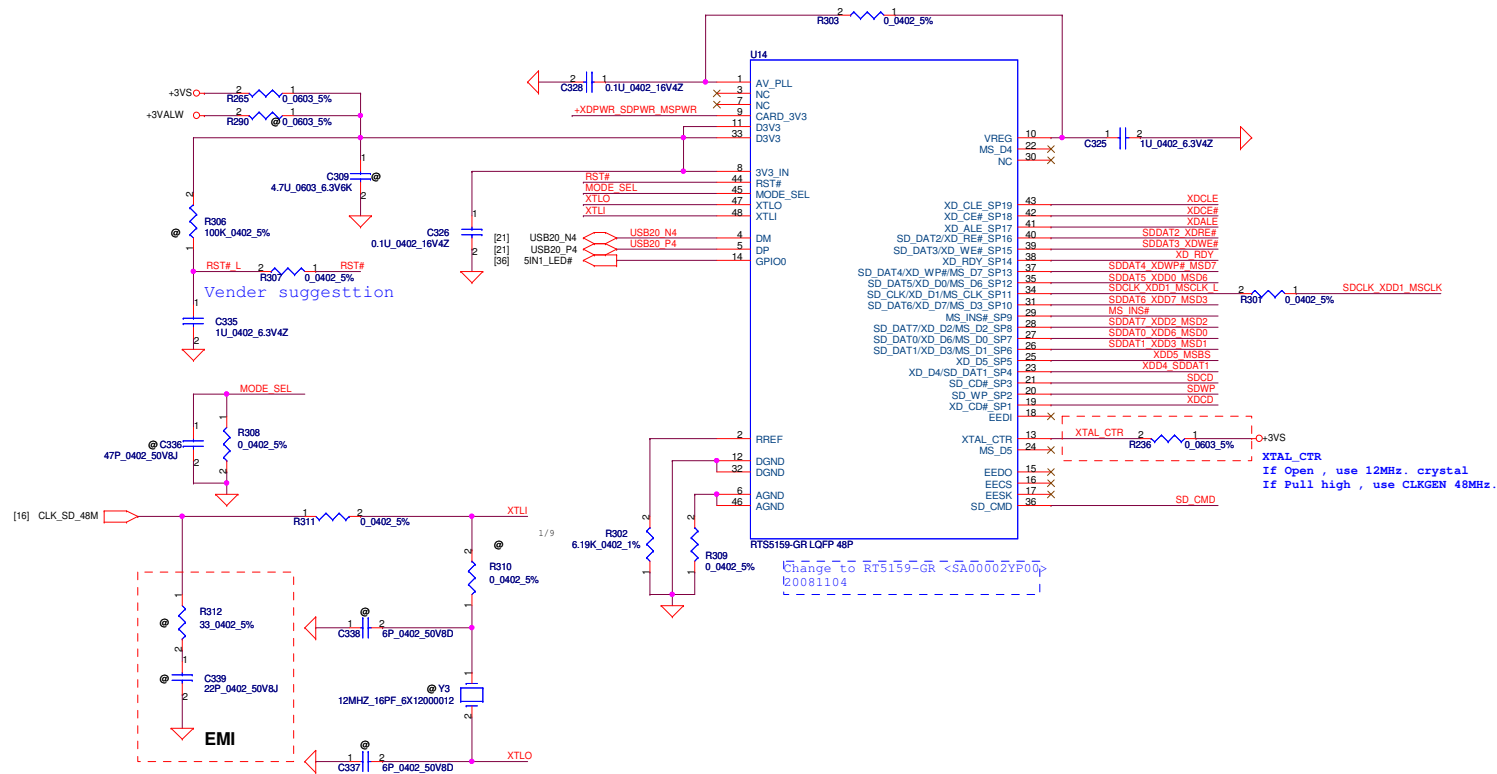
The schematic diagram shows the internal components of the PSOT24C-LF-T7_SOT23-3 module. It includes a PVT, PSOT24C-LF-T7_SOT23-3, RB4910_SC59-3, D20, F2, C172, and 01U_0402_16V4Z. The circuit is powered by +5VS and +HDMI 5V. The output is +HDMI_SV_OUT. The circuit is labeled with W=40mils and 1.1A_6VDC_FUSE.



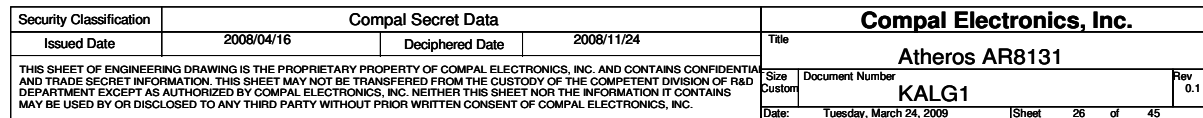
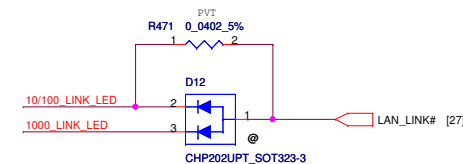
<u>HDMI_PCIE_MTX_C_GRX_N[0..3]</u>		HDMI_PCIE_MTX_C_GRX_N[0..3]	[10]
<u>HDMI_PCIE_MTX_C_GRX_P[0..3]</u>		HDMI_PCIE_MTX_C_GRX_P[0..3]	[10]

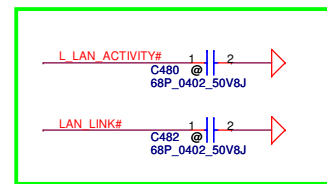
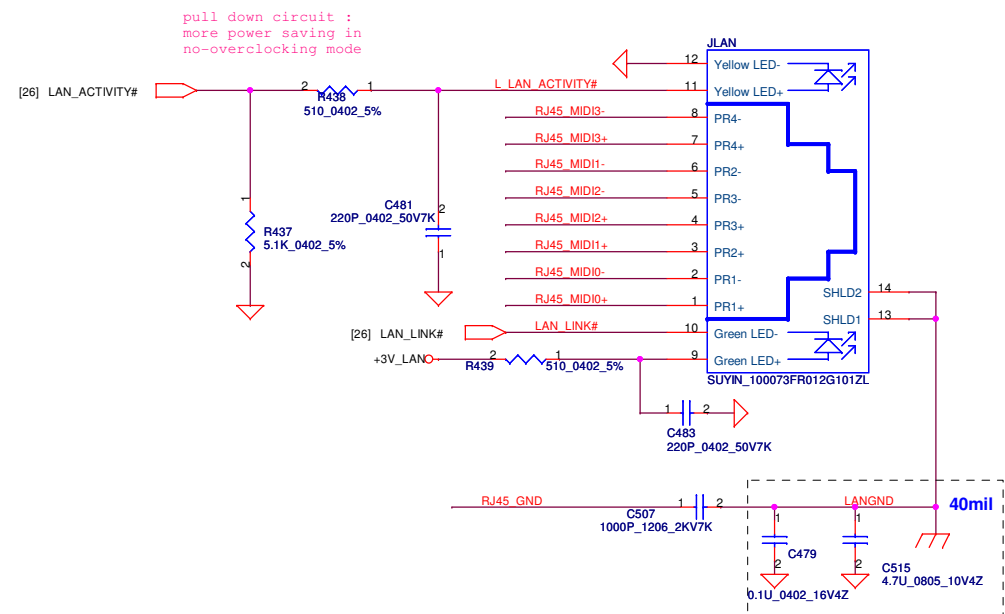
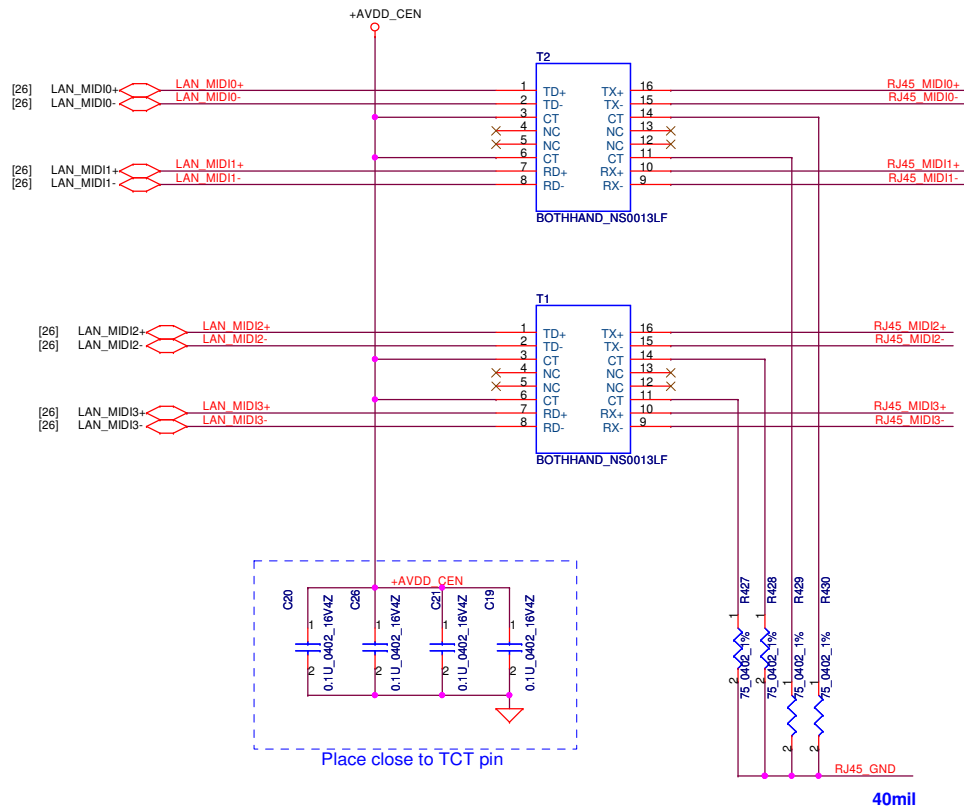


Intel Cantiga TMDs Pin Definition	
TMDs_B_CLK	PEG_TXP_3
TMDs_B_CLK#	PEG_TXN_3
TMDs_B_DATA0	PEG_TXP_2
TMDs_B_DATA0#	PEG_TXN_2
TMDs_B_DATA1	PEG_TXP_1
TMDs_B_DATA1#	PEG_TXN_1
TMDs_B_DATA2	PEG_TXP_0
TMDs_B_DATA2#	PEG_TXN_0
TMDs_B_HPD#	PEG_RXP_3



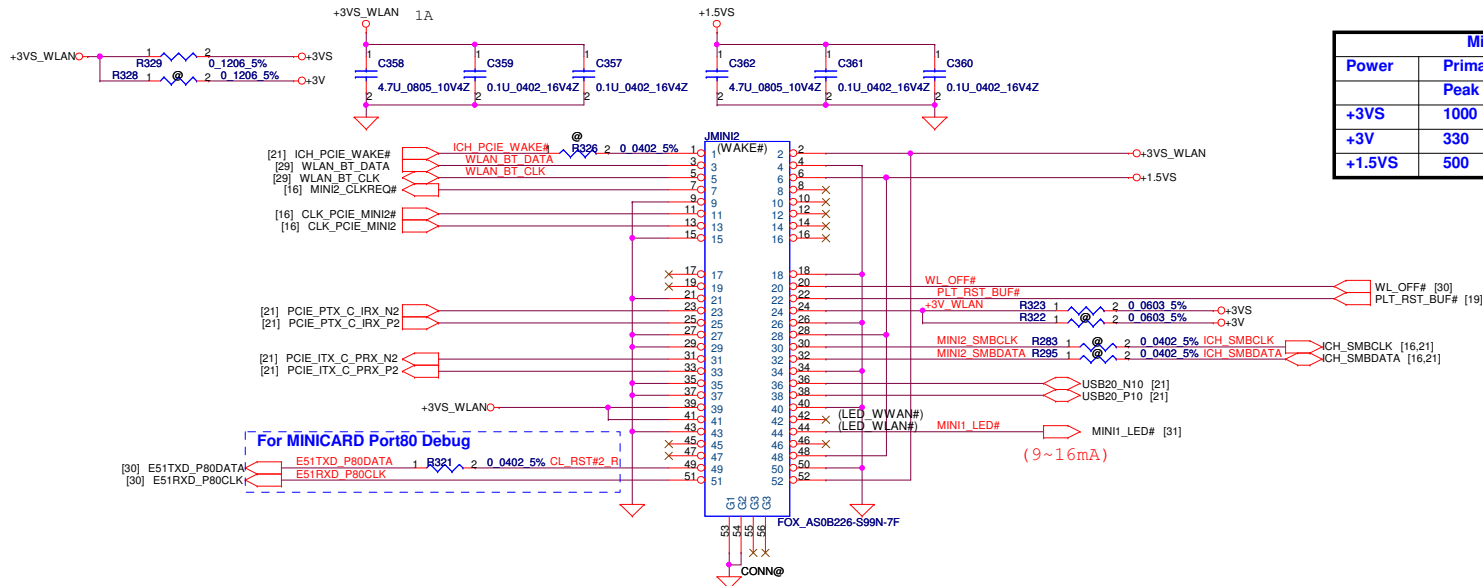
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
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				Size	Document Number	Rev
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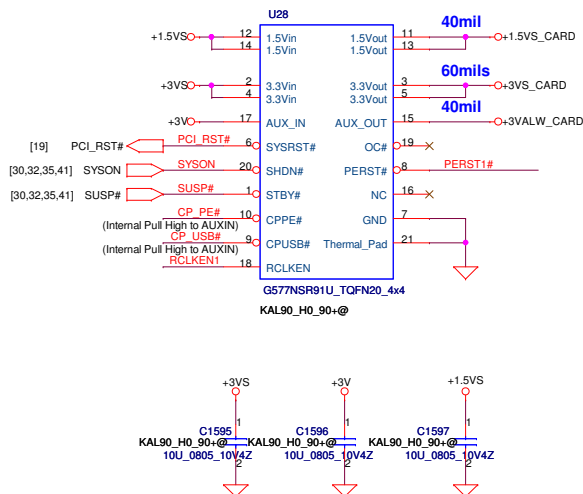
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Size	B	Document Number	KALG1	Date	Tuesday, March 24, 2009
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For Wireless LAN

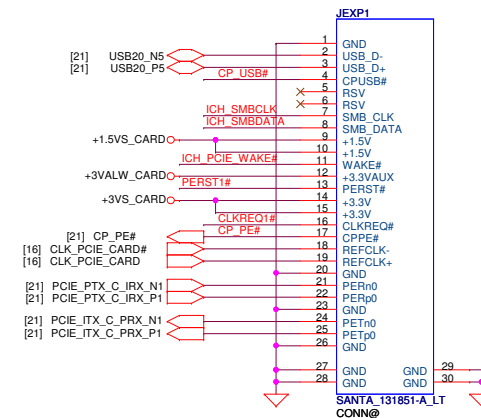


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

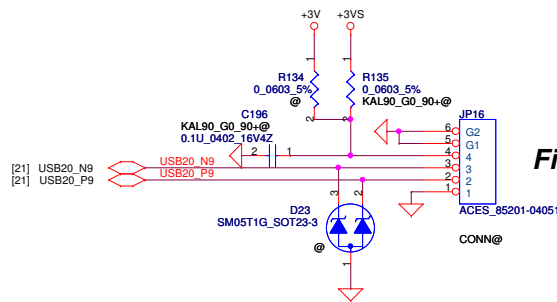
New Card Power Switch



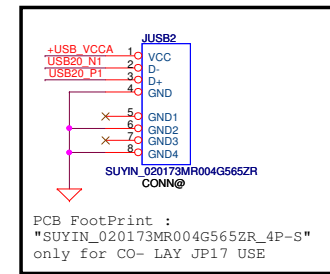
New Card Socket (Left/TOP)



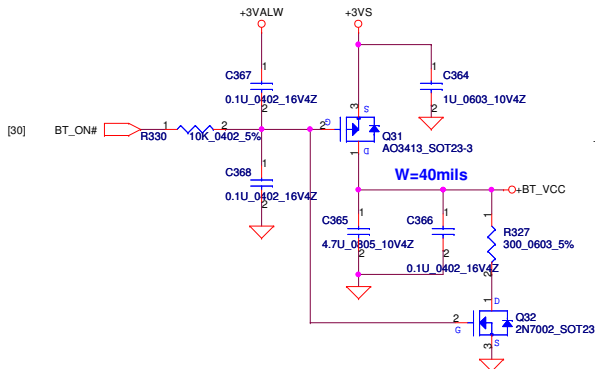
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Issued Date				2008/11/10				Title			
Deciphered Date				2008/11/24				NEW CARD & MINI CARD-WLAN			
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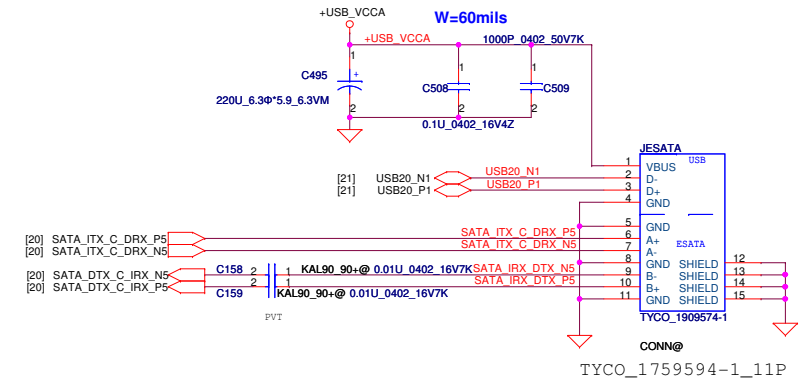
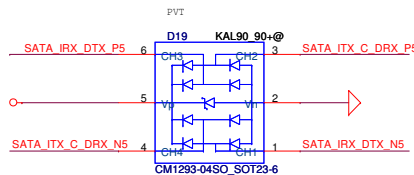
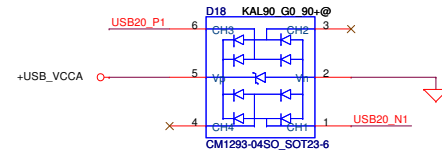
Finger Print Conn.



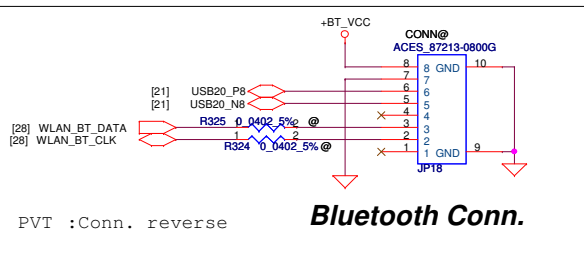
ESATA Conn.



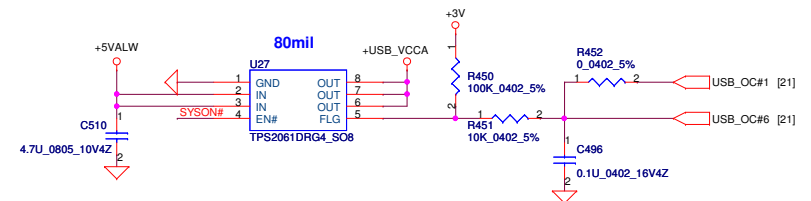
Bluetooth Conn.



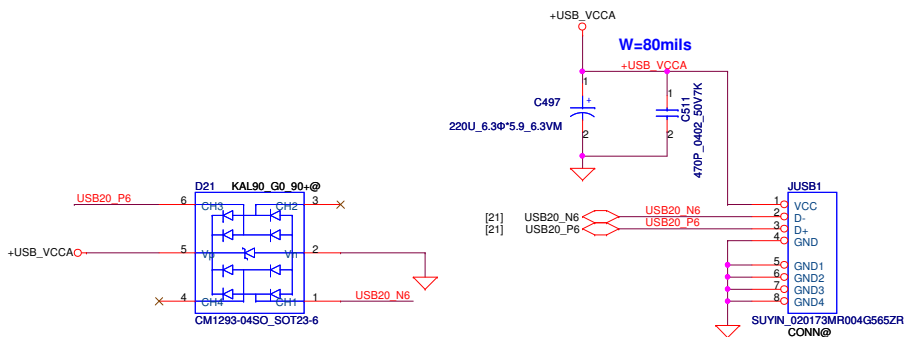
CONN@



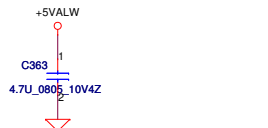
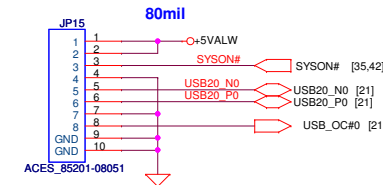
PVT :Conn. reverse



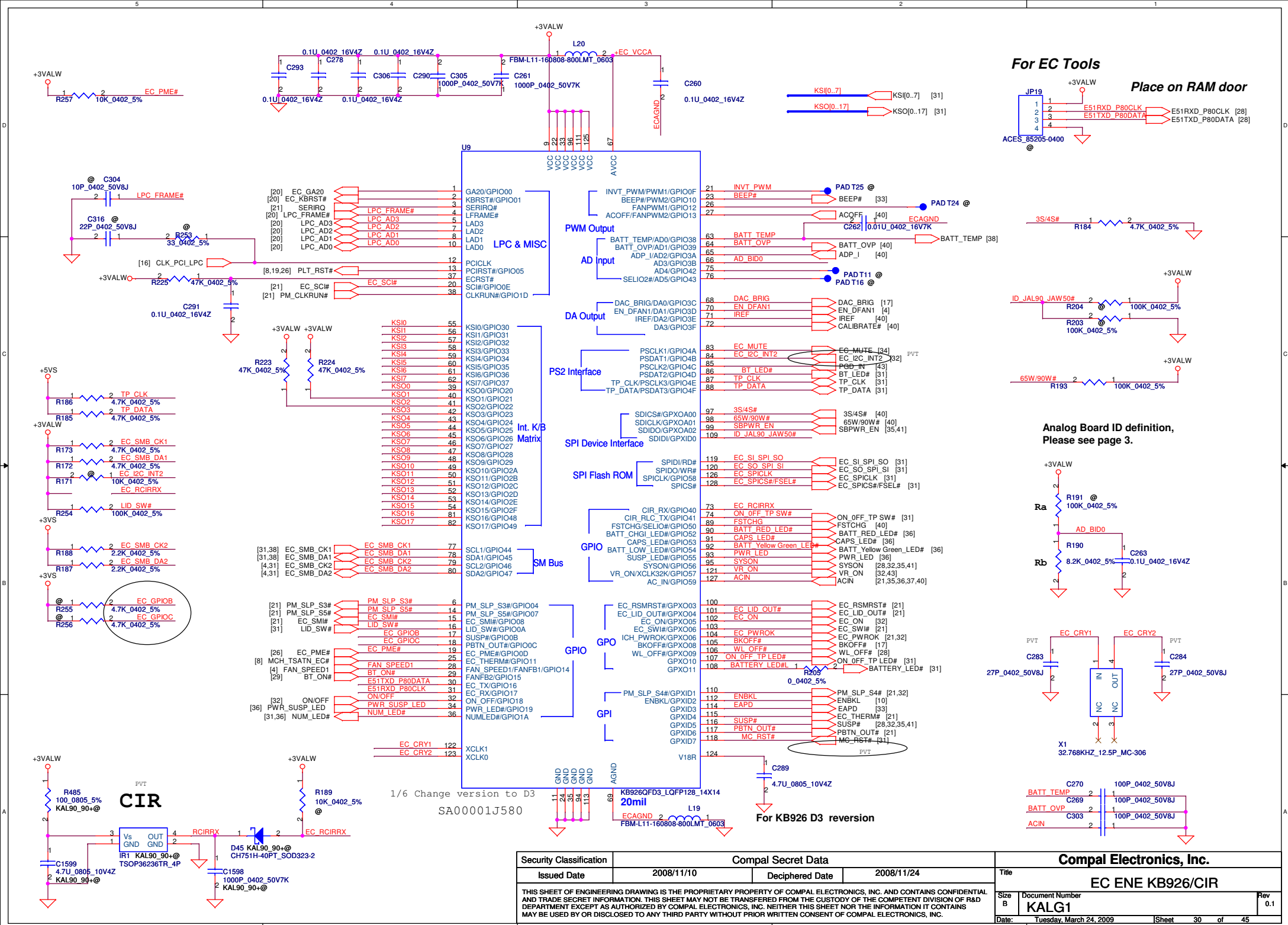
To USB/B Connector

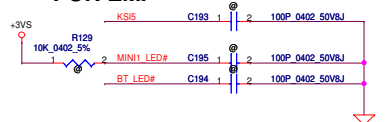
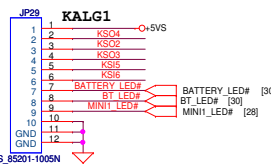
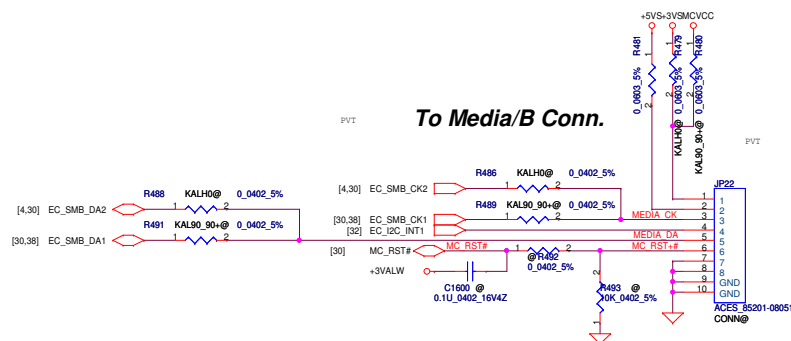
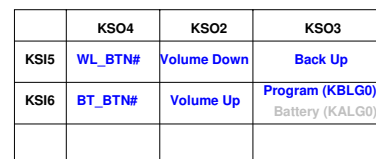
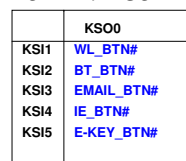
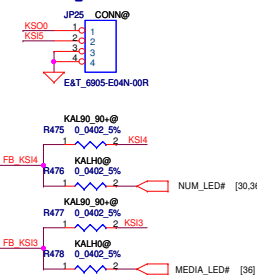
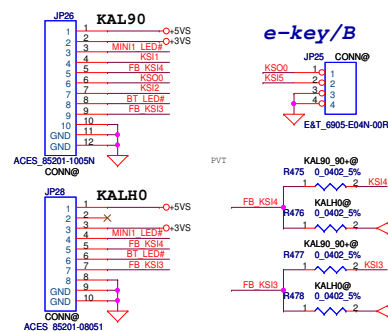
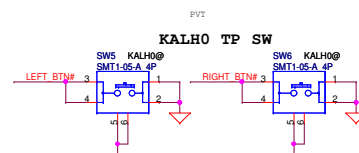
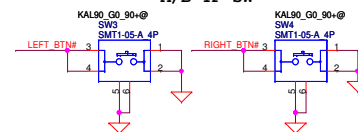
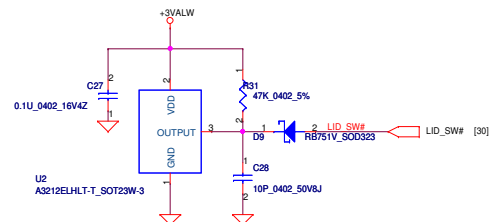
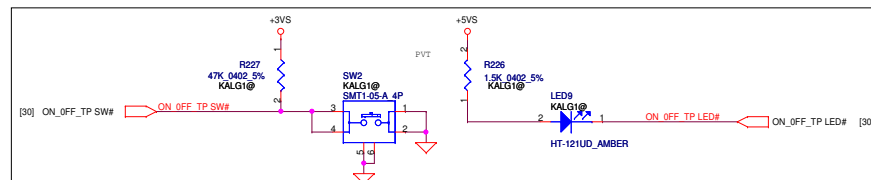
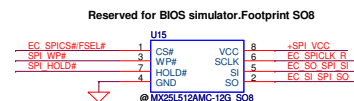


USB Conn.



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								KALG1		0.1	
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hexainf@hotmail.com
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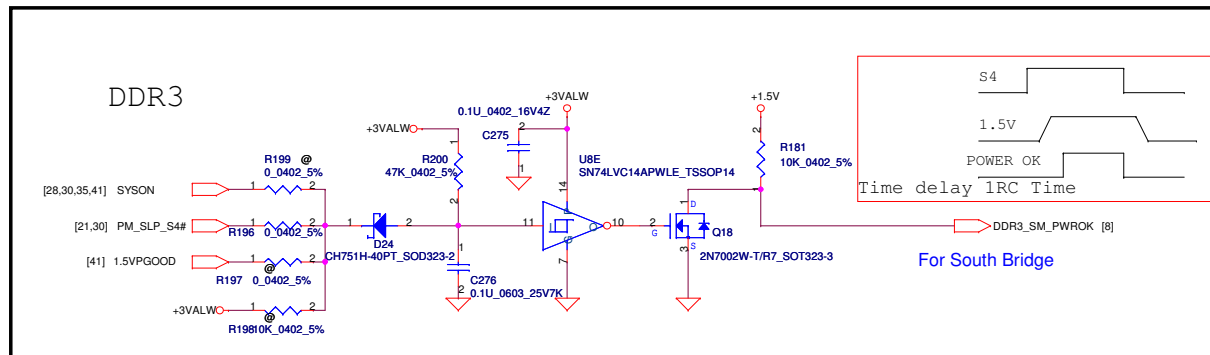
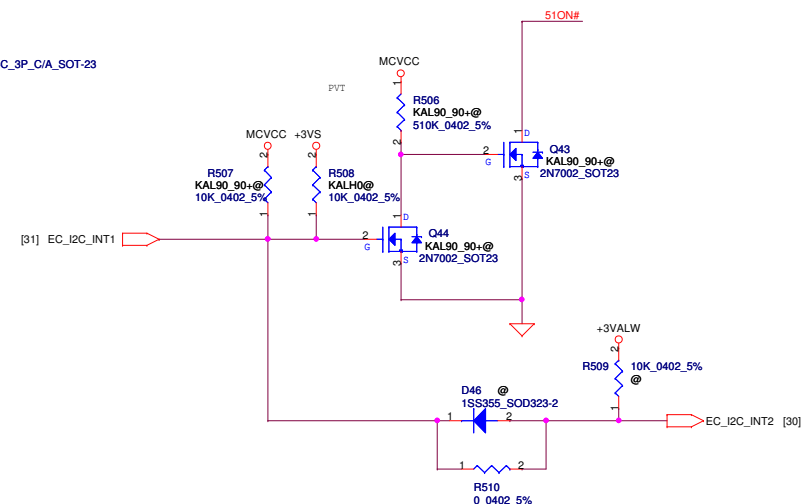
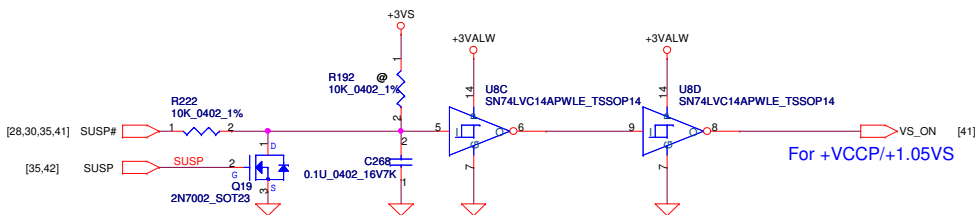
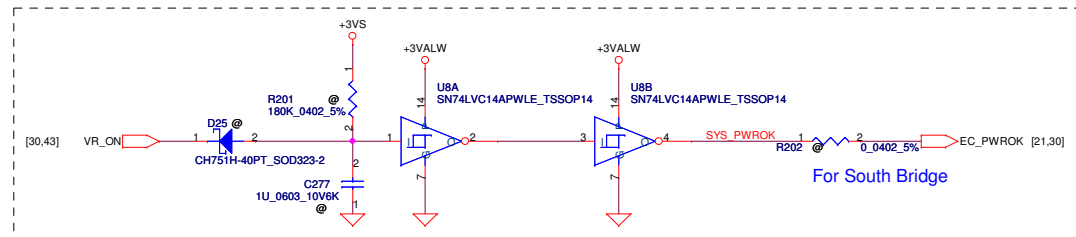
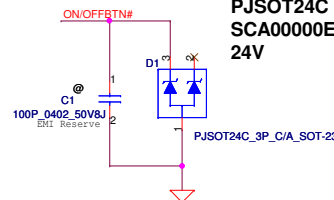
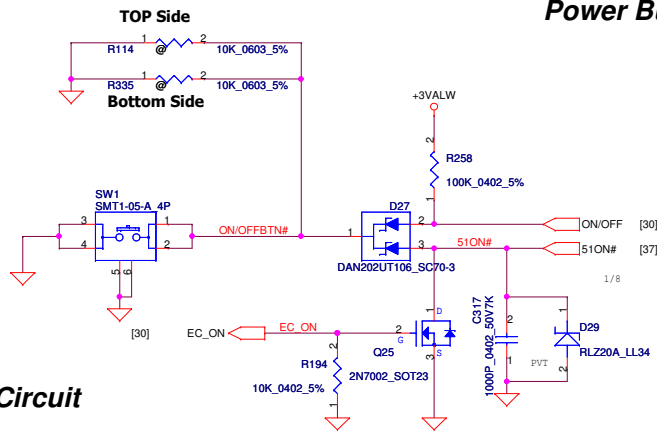
Power Button

D58 USE
PJSOT24C 3P C/A SOT-23
SCA00000E00
24V

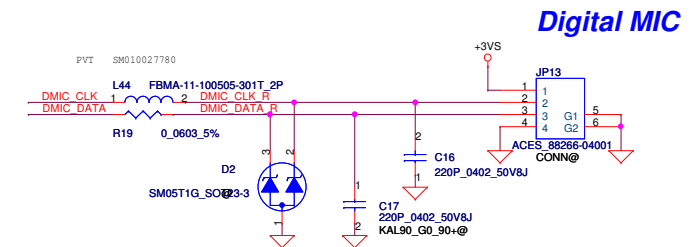
Power ON Circuit

HDA MDC Conn.

DDR3



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				32	



Gain= 10dB

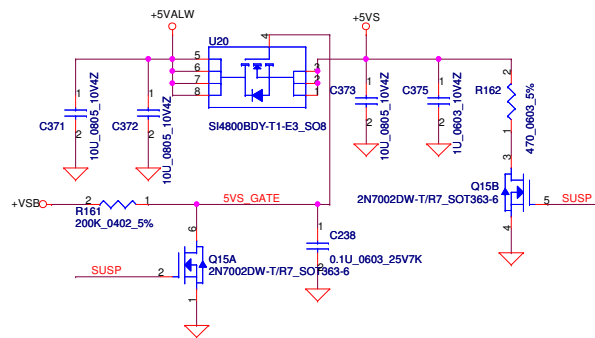
Int. Speaker Conn.

(HDA Jack)
MIC JACK

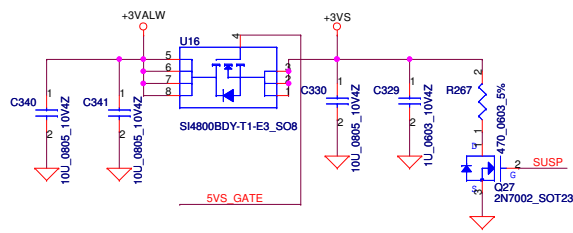
(HDA Jack)
LINE-IN JACK

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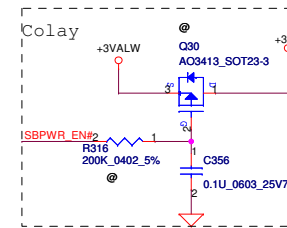
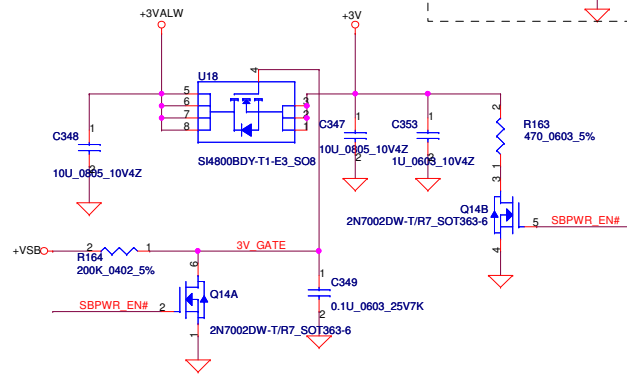
+5VALW TO +5VS

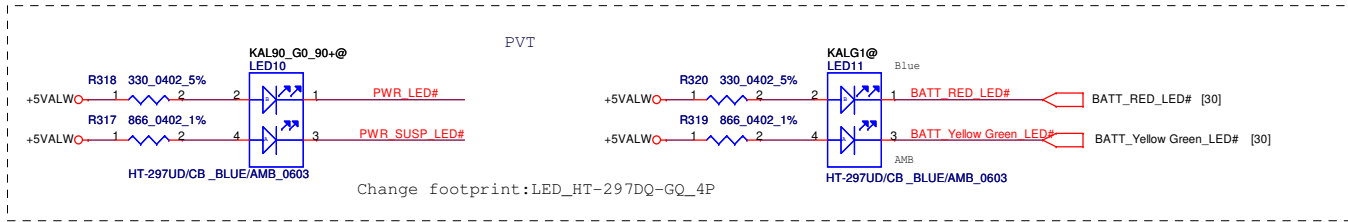
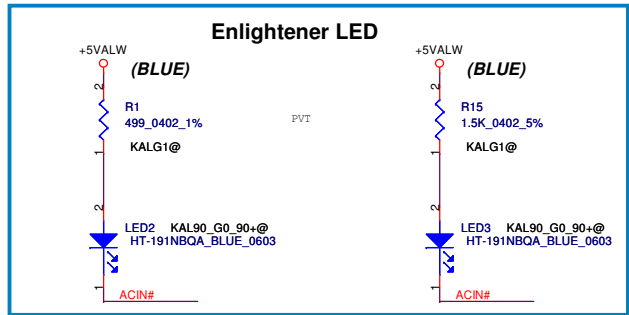


+3VALW TO +3VS

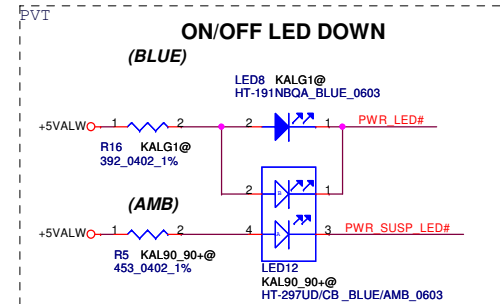
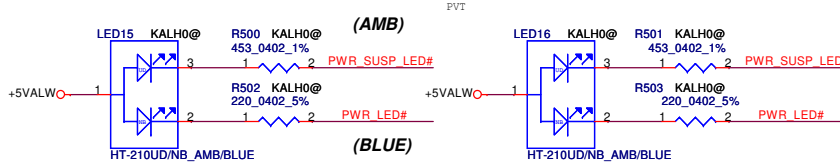
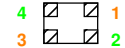


+3VALW TO +3V_SB(ICH8M AUX Power)

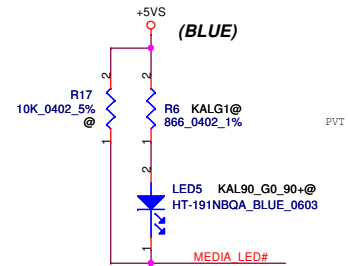




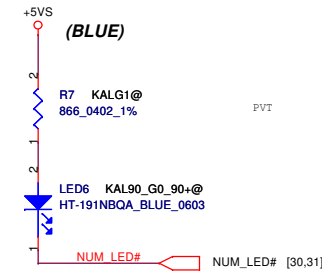
Compal Footprint



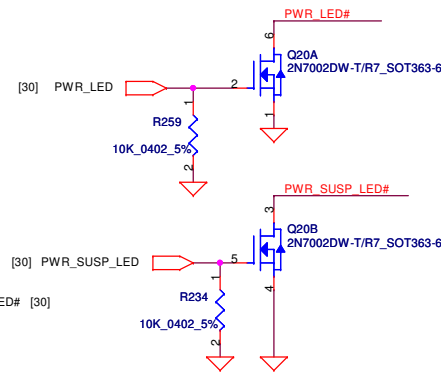
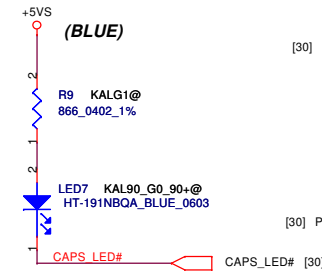
MEDIA_LED



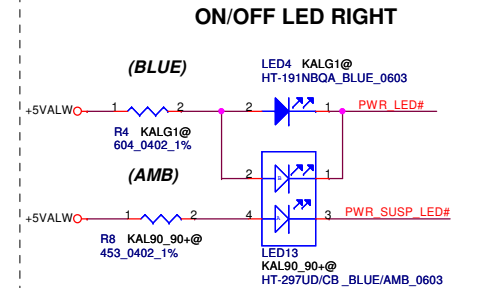
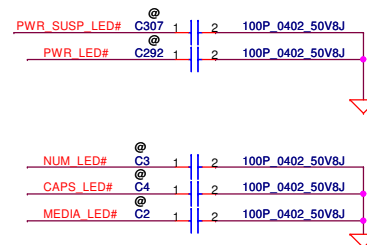
NUM_LED



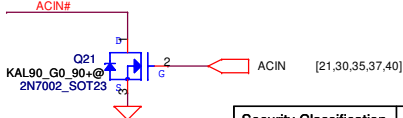
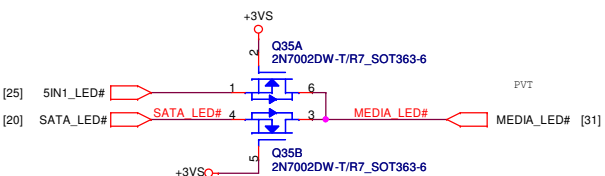
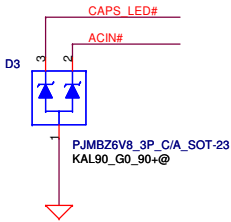
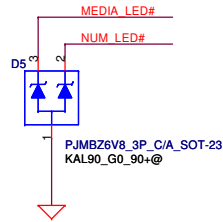
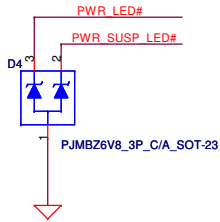
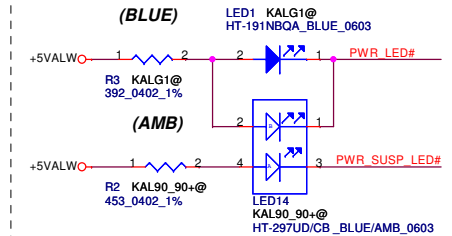
CAPS_LED



FOR EMI

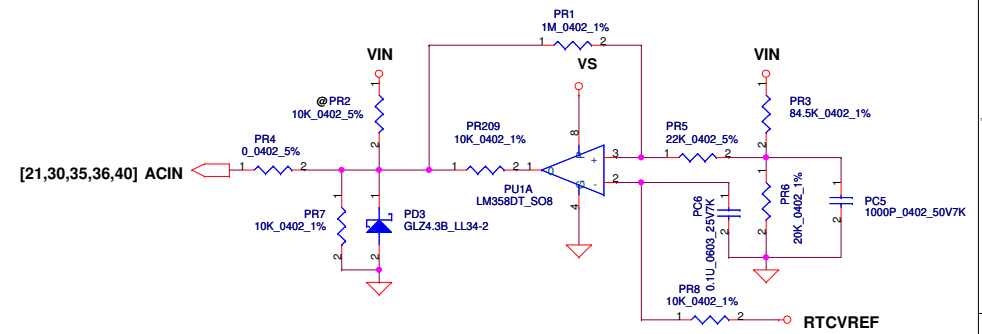
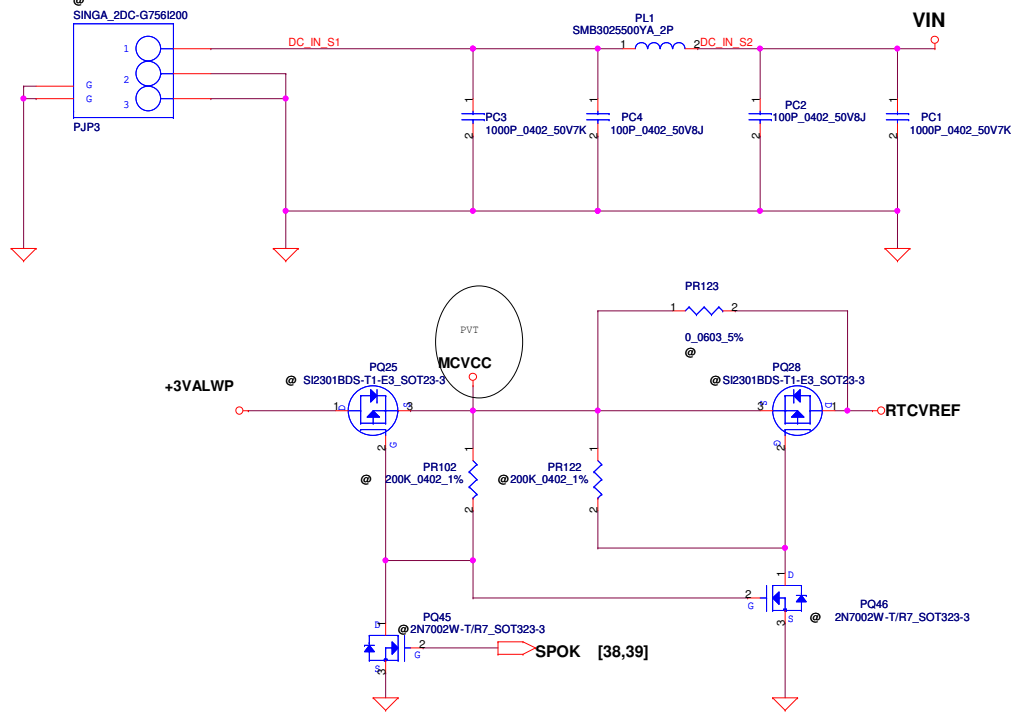


ON/OFF LED LEFT



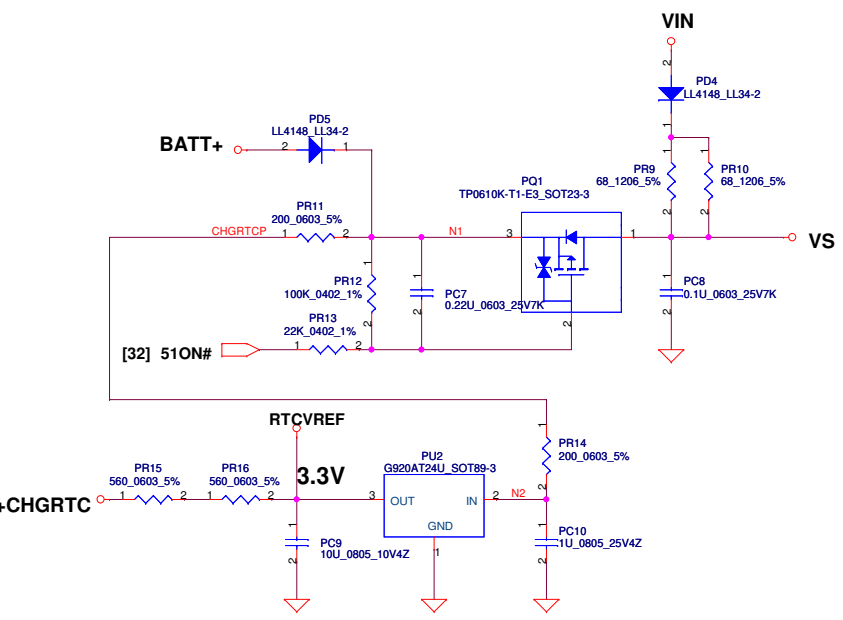
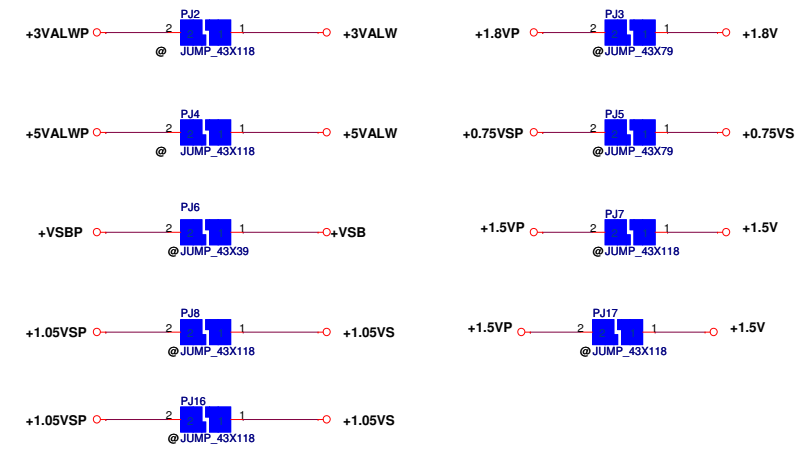
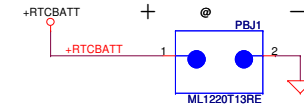
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								PWR/B							
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						Custom		KALG1		0.1					
						Date:		Tuesday, March 24, 2009				Sheet		36 of 45	

DC231000500



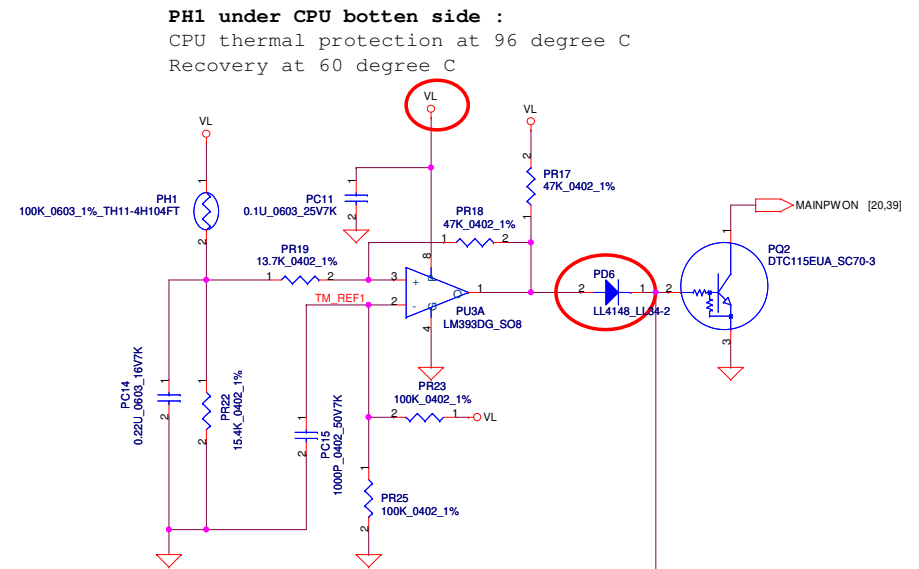
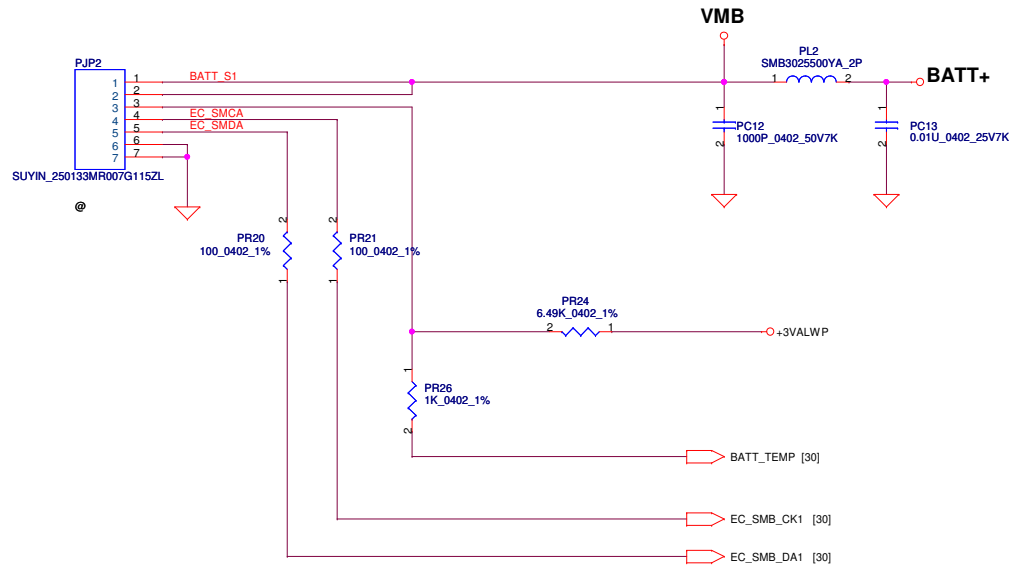
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H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

RTC Conn

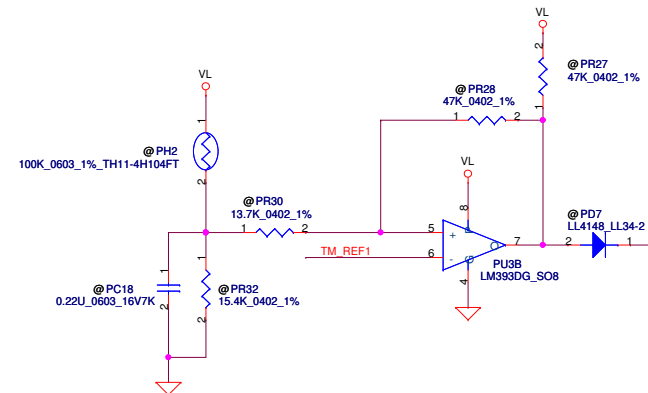
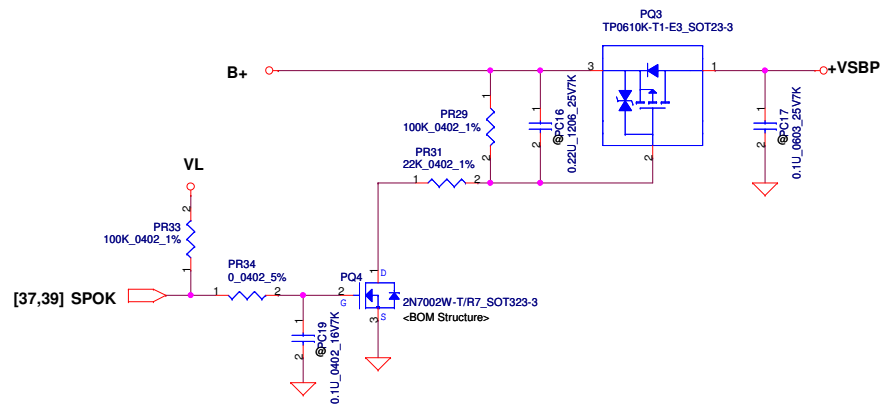


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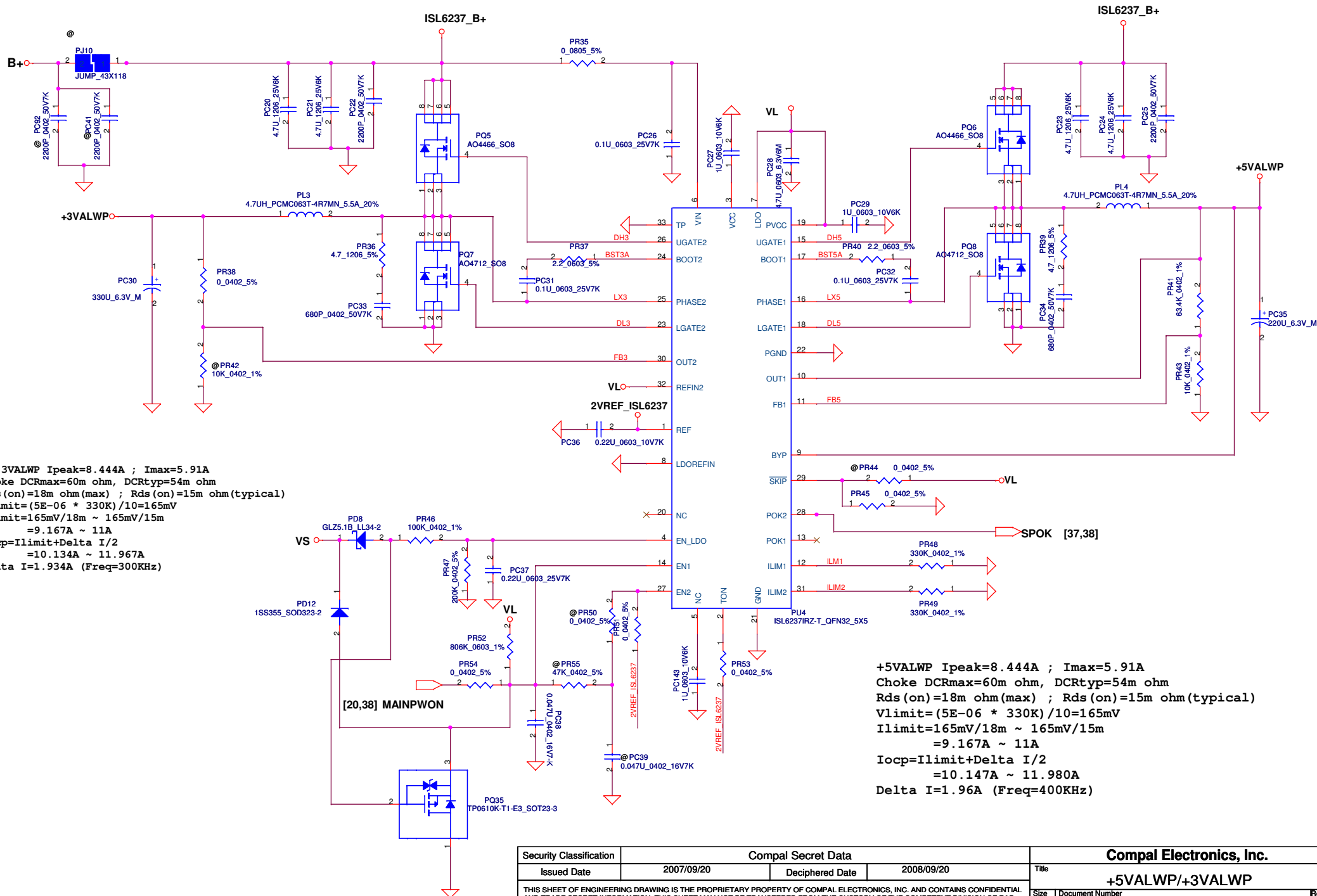
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Issued Date				2007/09/20				Deciphered Date			
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PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 47 degree C



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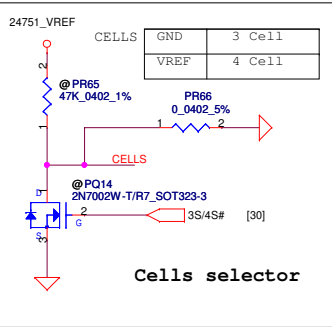
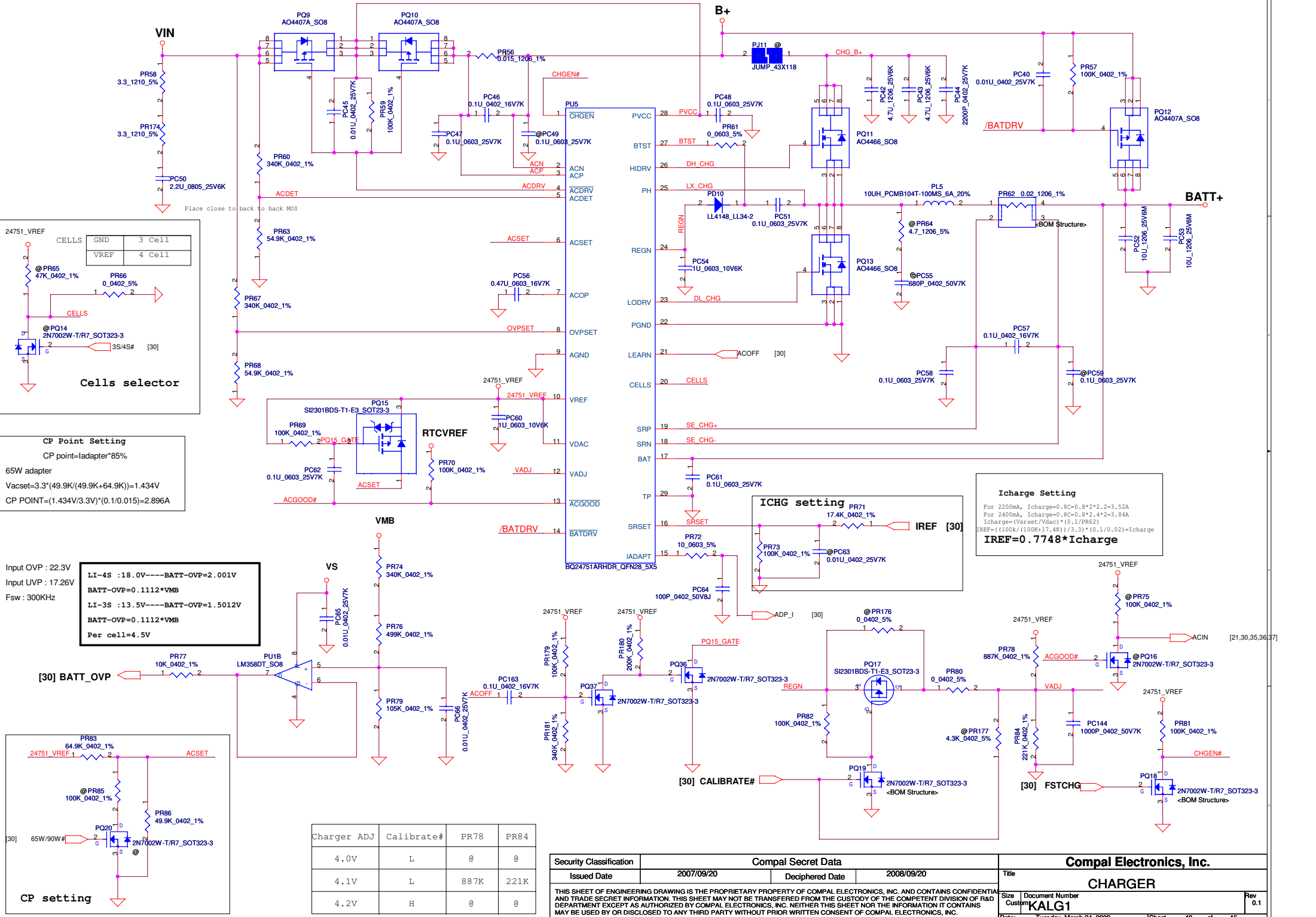


+3.3VALWP Ipeak=8.444A ; Imax=5.91A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.134A ~ 11.967A
Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.147A ~ 11.980A
Delta I=1.96A (Freq=400KHz)

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CP Point Setting

CP point=ladapter*85%

65W adapter

Vacset=3.3*(49.9K/(49.9K+64.9K))=1.434V

CP POINT=(1.434V/3.3V)*(0.1/0.015)=2.896A

Input OVP : 22.3V

Input UVP : 17.26V

Fsw : 300KHz

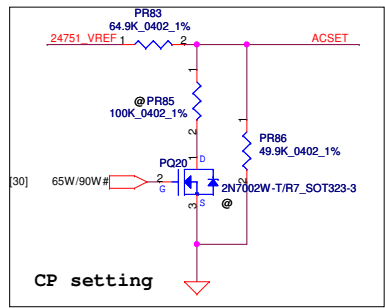
LI-4S : 18.0V----BATT-OVP=2.001V

BATT-OVP=0.1112*VMB

LI-3S : 13.5V----BATT-OVP=1.5012V

BATT-OVP=0.1112*VMB

Per cell=4.5V



Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V	H	@	@

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Icharge Setting

For 2200mA, Icharge=0.8*(0.8*2*2.2+3.52A)

For 2400mA, Icharge=0.8*(0.8*2.4+3.84A)

Icharge=(Varset/Vdac)*(0.1/PR62)

IREF=(100K/(100K+17.4K))/3.3*(0.1/0.02)=Icharge

IREF=0.7748*Icharge

Compal Electronics, Inc.			
CHARGER			
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[30,35] SBPWR_EN

[32] VS_ON

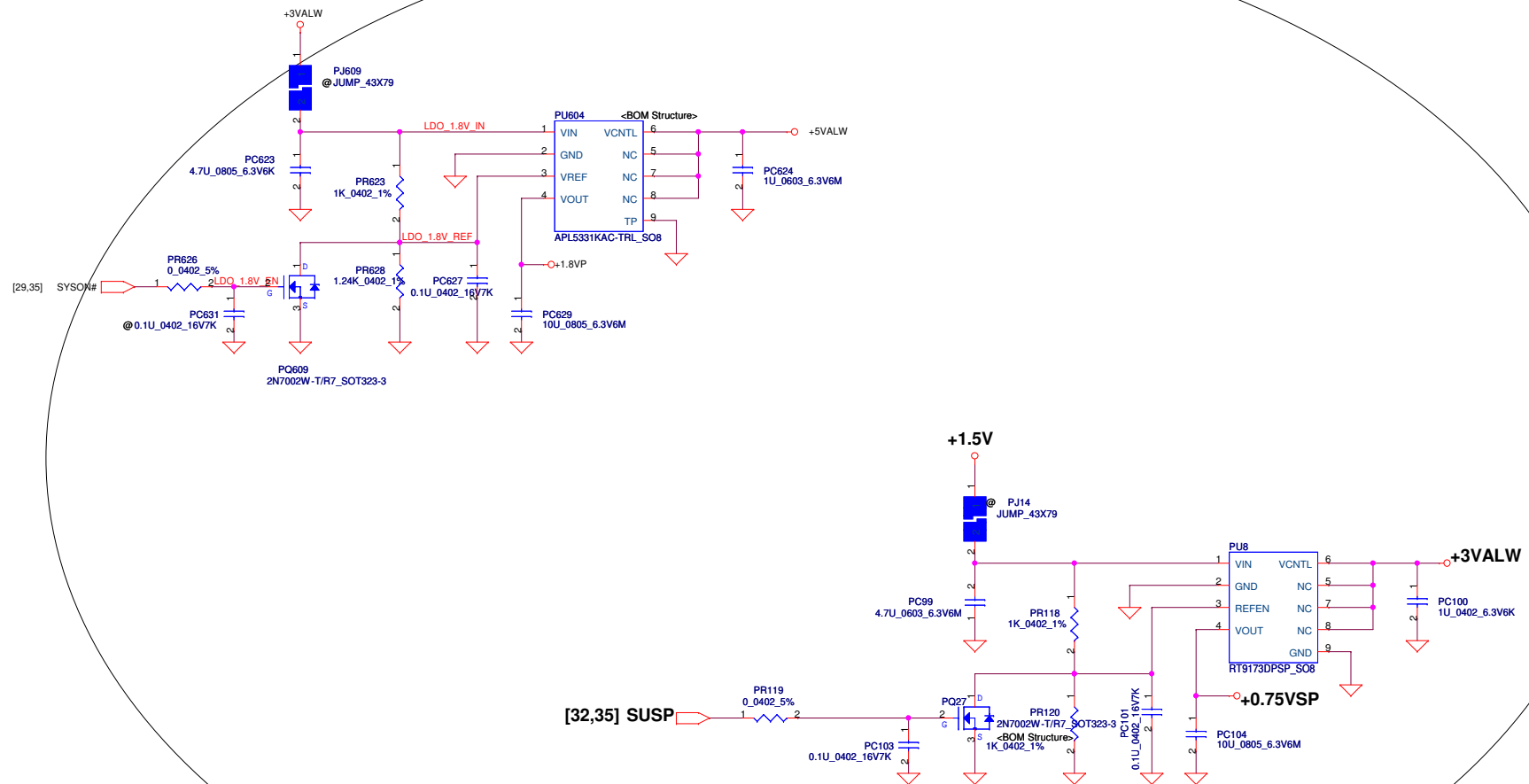
12/25

[30,32,35] SVSON

12/25

12/25

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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Add 3/5V boost resister for EMI request			Change PR37 and PR40 to 2.2 OHM		
2		Modify 1.5V and 1.05V choke to cyntec for eff.			PL501 & PL502		
3		Modify 1.5V and 1.05V frequnce from 336K to 264K for eff.			Change PR525 & PR501 from 240K to 300K		
4		Modify 1.5V and 1.05V low side mos for eff.			Change PQ506 & PQ508 from FDS6670 to A04456		
5		Add CPU_core boost resister for EMI request			Change PR138 and PR158 to 2.2 OHM		
6		Modify 1.5V & 1.05V OCP to 14A			Change PR530 & PR522 to 5.9K		
7		Modify 3V & 5V choke to 4.7UH for eff.			Change PL3 & PL4 from 8.2UH to 4.7UH		
8		Modify 5V output cap to OS-CON for costdown			Change PC35		
9		Modify 3V output cap to OS-CON for costdown			Change PC30		
10		Modify dischager mos to A04407A for rating risk			Change PQ12		
11		Add 30K OHM to TPS51117 EN pin , Disable SMPS mode			ADD PR910 & PR911		
12							
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PCB



LA-5271P MB Rev0: DA60000C500

PCB 08Y LA-5271P REV0 M/B

North Bridge

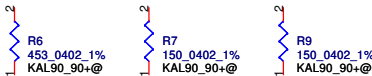


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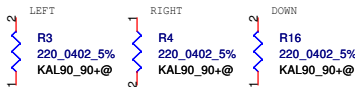
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GL40@

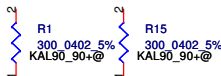
MEDIA_LED NUM_LED CAPS_LED



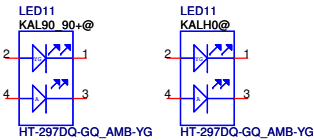
ON/OFF LED Risiter



Enlightener LED



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