

Compal Confidential

KAL90/KALH0 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRII + ICH9M

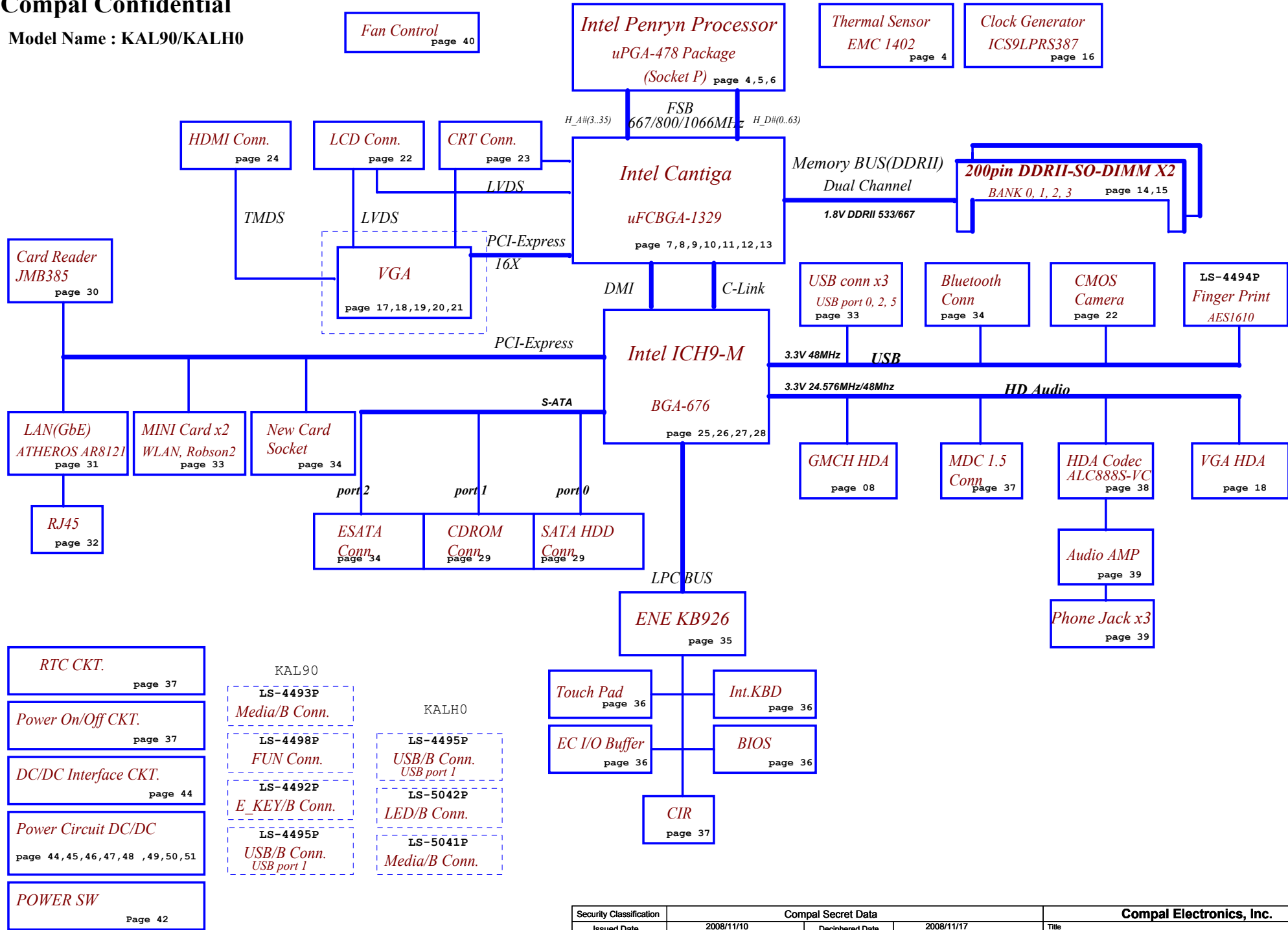
2008-12-17

REV:1.0

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Model Name : KAL90/KALH0



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Device	IDSEL#	REQ#/GNT#	Interrupts
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b
MEDIA CONSOLE	1010 000X b	NB9M THERMAL SENSOR	

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b
MEDIA CONSOLE	1010 000X b	NB9M THERMAL SENSOR	

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS367, SLG8SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

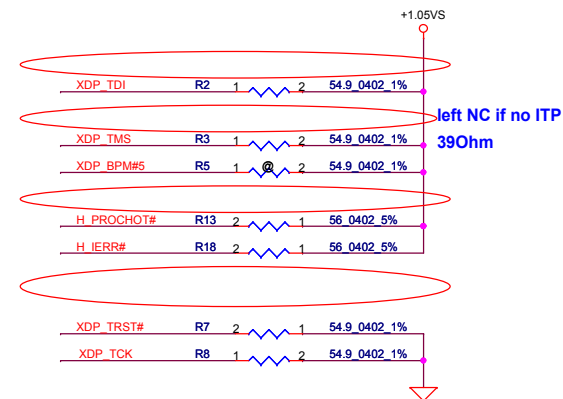
BTO Option Table

BTO Item	BOM Structure
KAL90	JAL90@
UMA	GM@
PM@	PM@
ALC888VC	888VC@
ALC888VB	888VB@
AR8121	8121@
AR8112	8112@
ALC268	268@
GL40	GL40@
GM45	GM45@

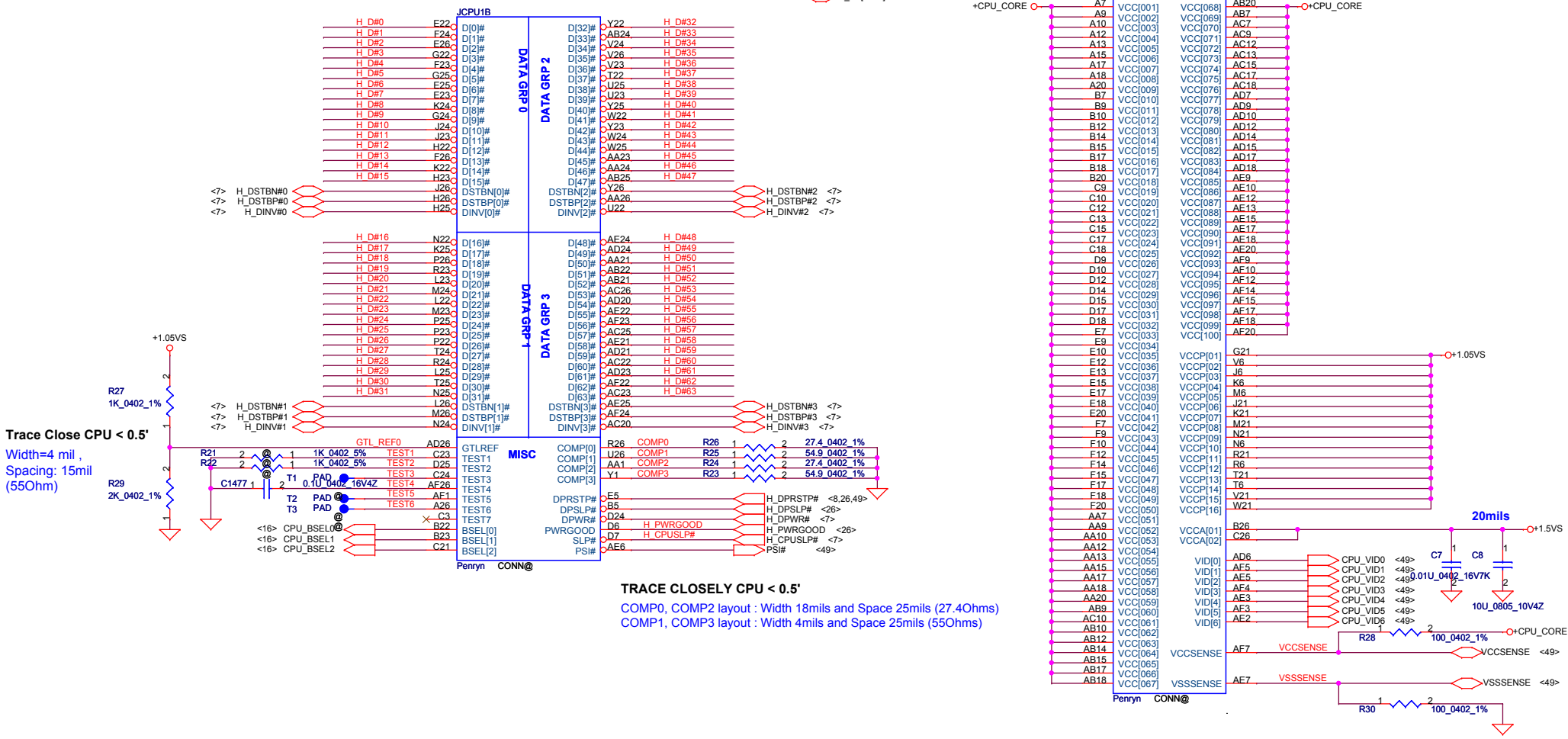
BOM Configuration Table

Project	BOM Configuration
KAL90-UMA	XXXXXXXXXX:KAL90@/GM@/888VC@/8121@/GM45@
KAL90-Dis	XXXXXXXXXX:KAL90@/PM@/888VC@/8121@
KAL90-GM45	XXXXXXXXXX:KALH0@/GM@/888VC@/8121@/GM45@
KAL90-GL40	XXXXXXXXXX:KALH0@/GM@/888VC@/8121@/GL40@
KAL90-PM45	XXXXXXXXXX:KALH0@/PM@/888VC@/8121@

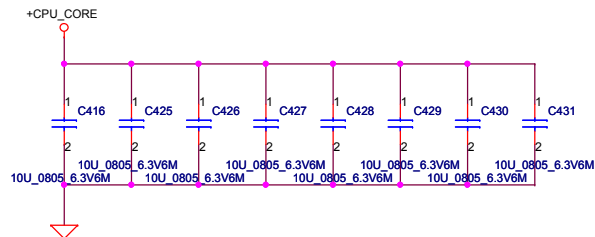
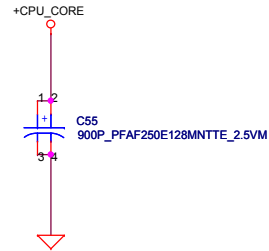
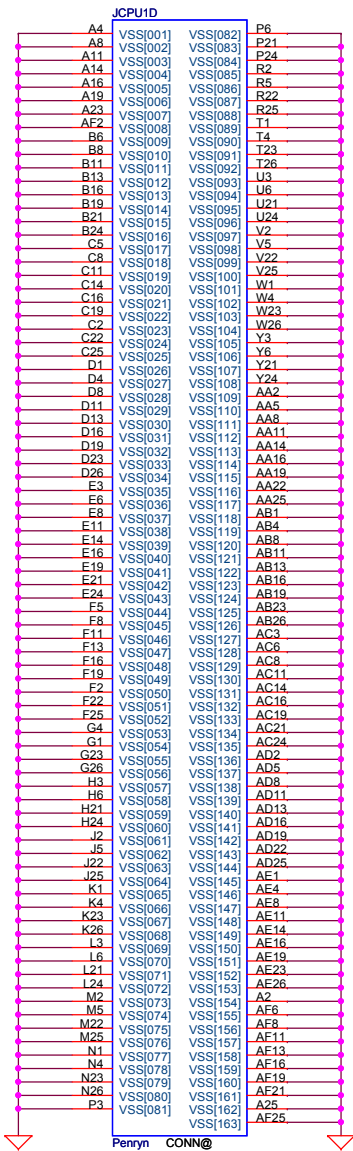
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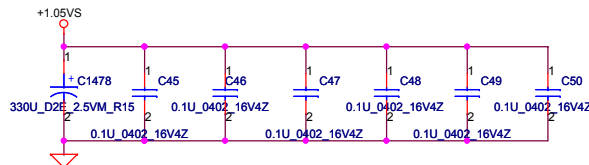
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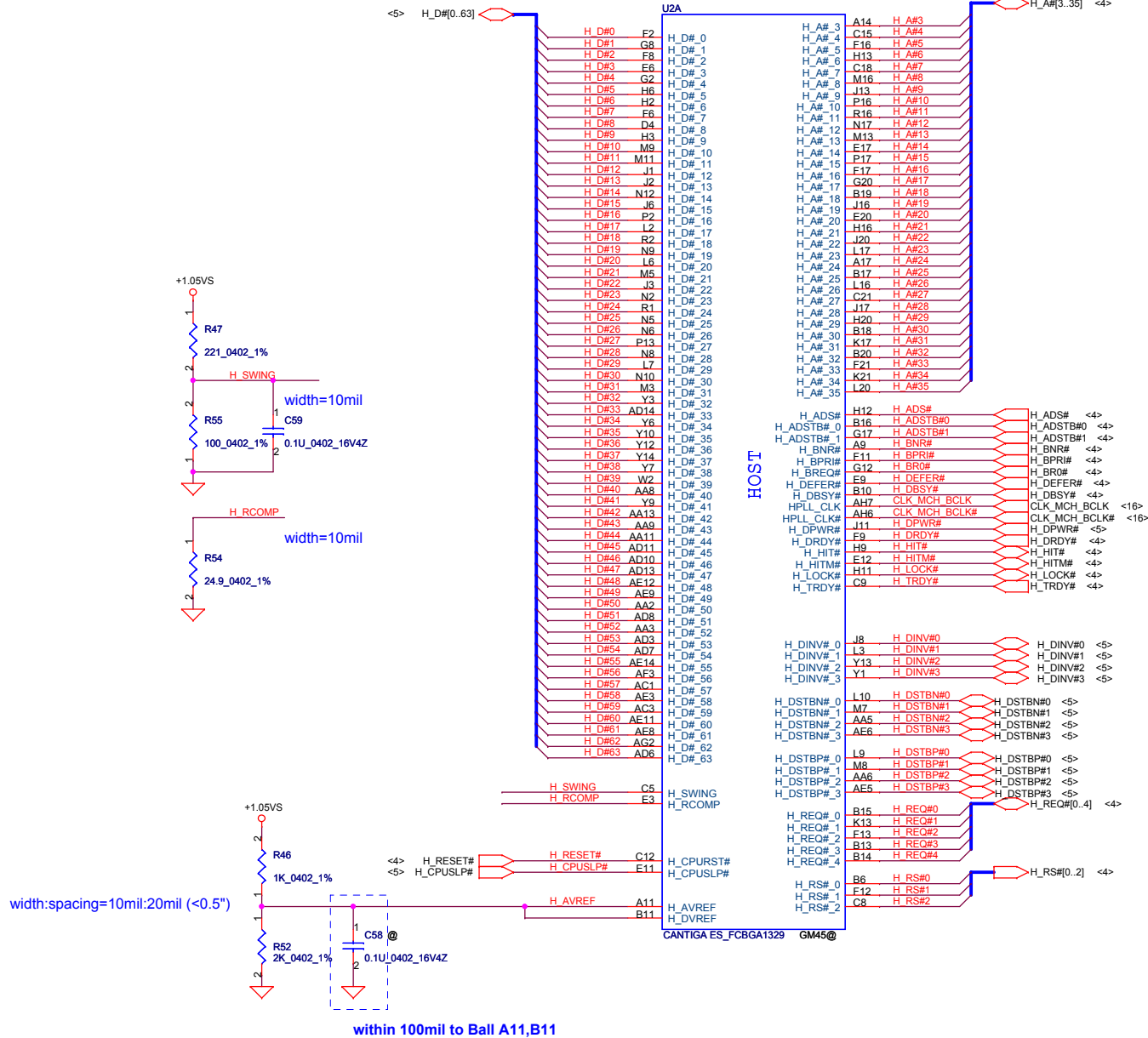


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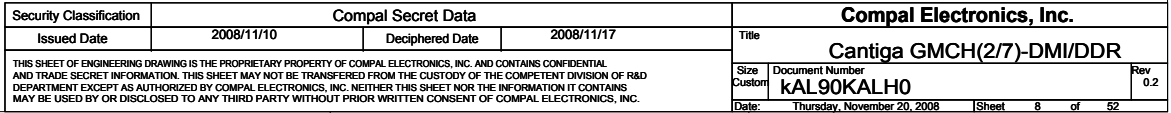


+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



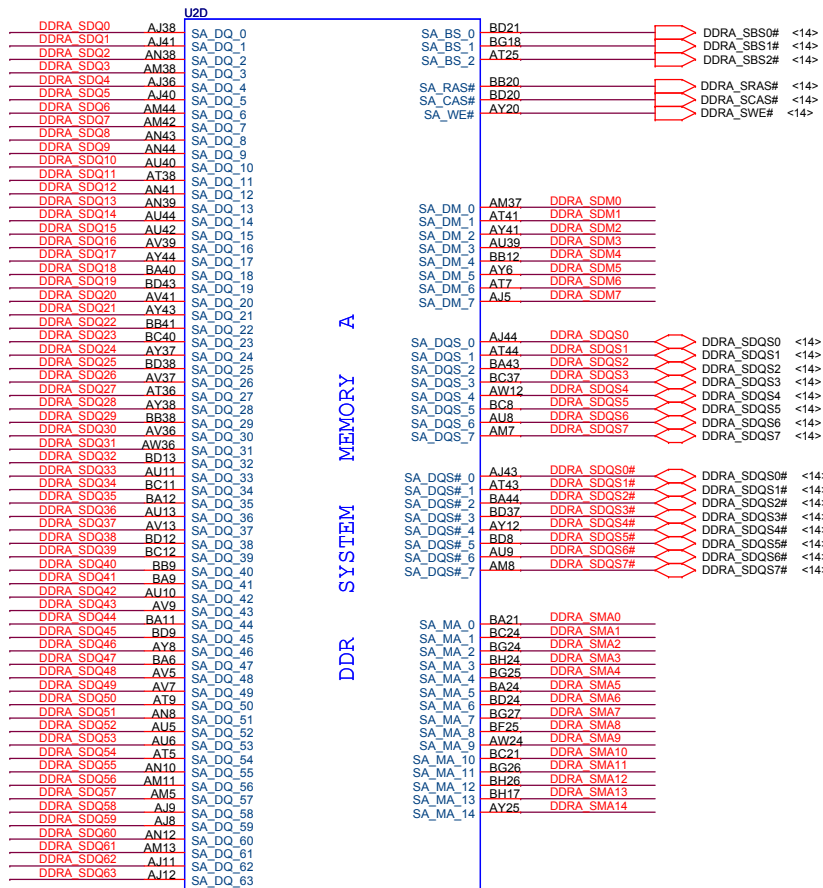


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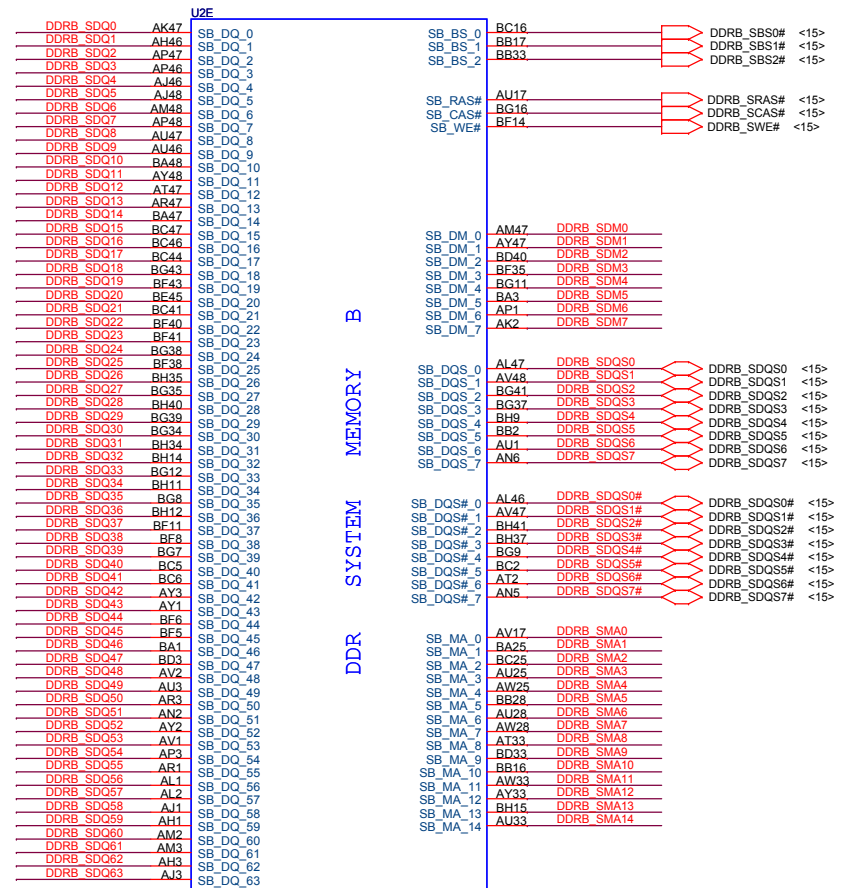


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<14> DDRA_SDM[0..7] DDRA_SDM[0..7]
<14> DDRA_SMA[0..14] DDRA_SMA[0..14]

<15> DDRB_SDQ[0..63] DDRB_SDQ[0..63]
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<15> DDRB_SMA[0..14] DDRB_SMA[0..14]

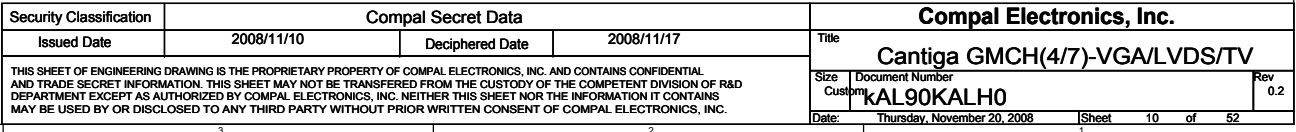


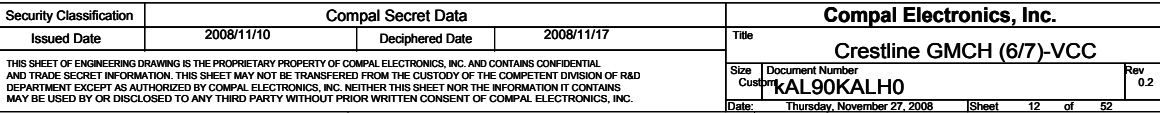
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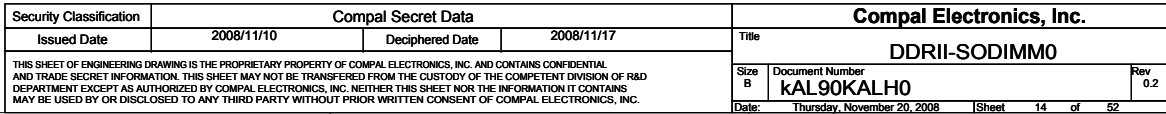


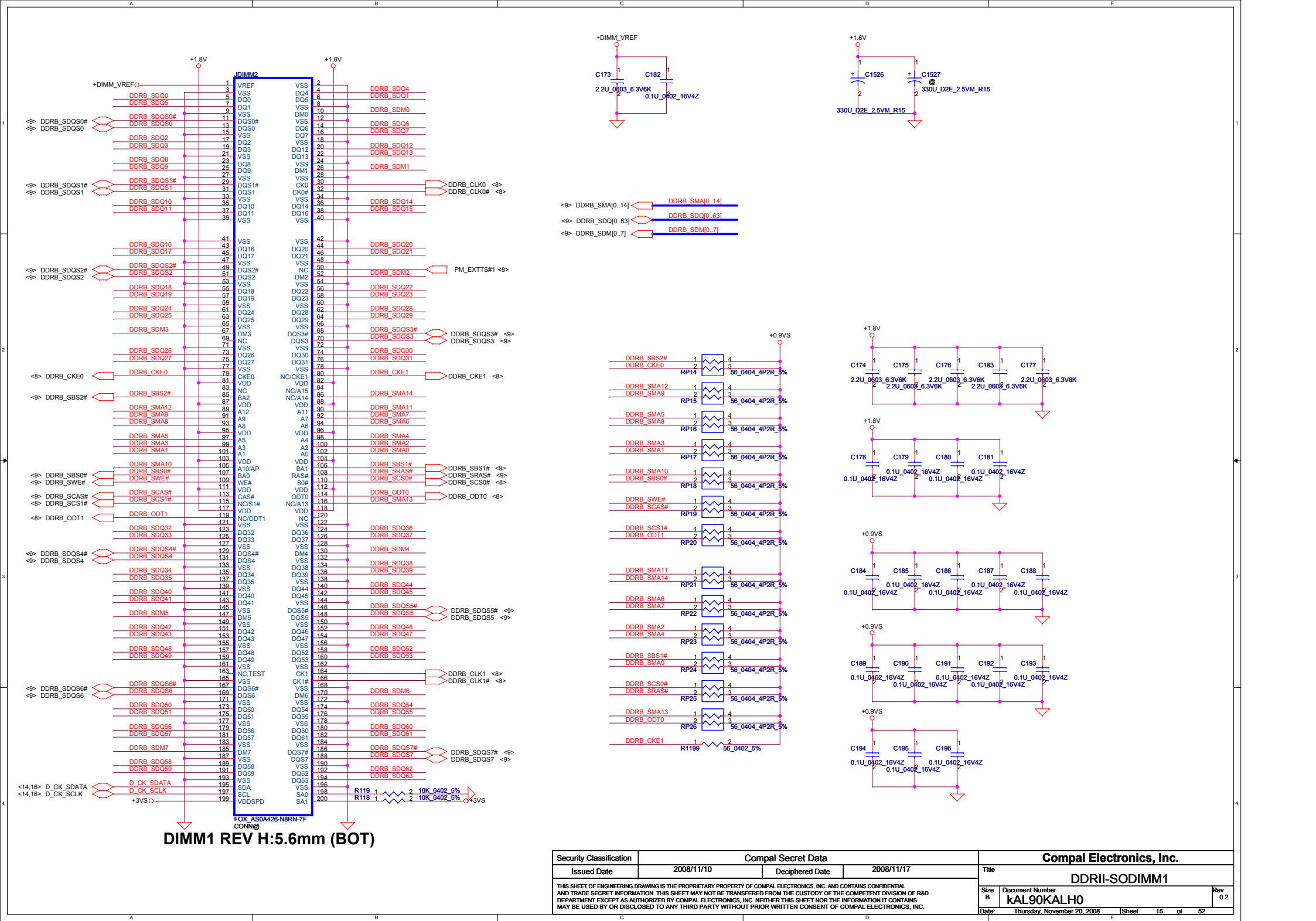
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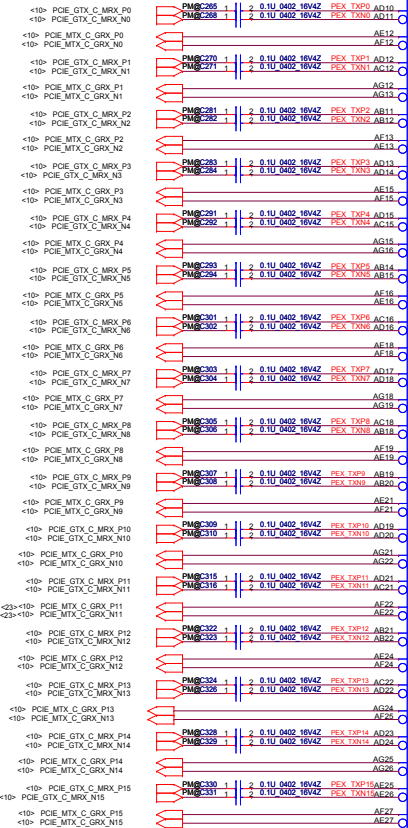
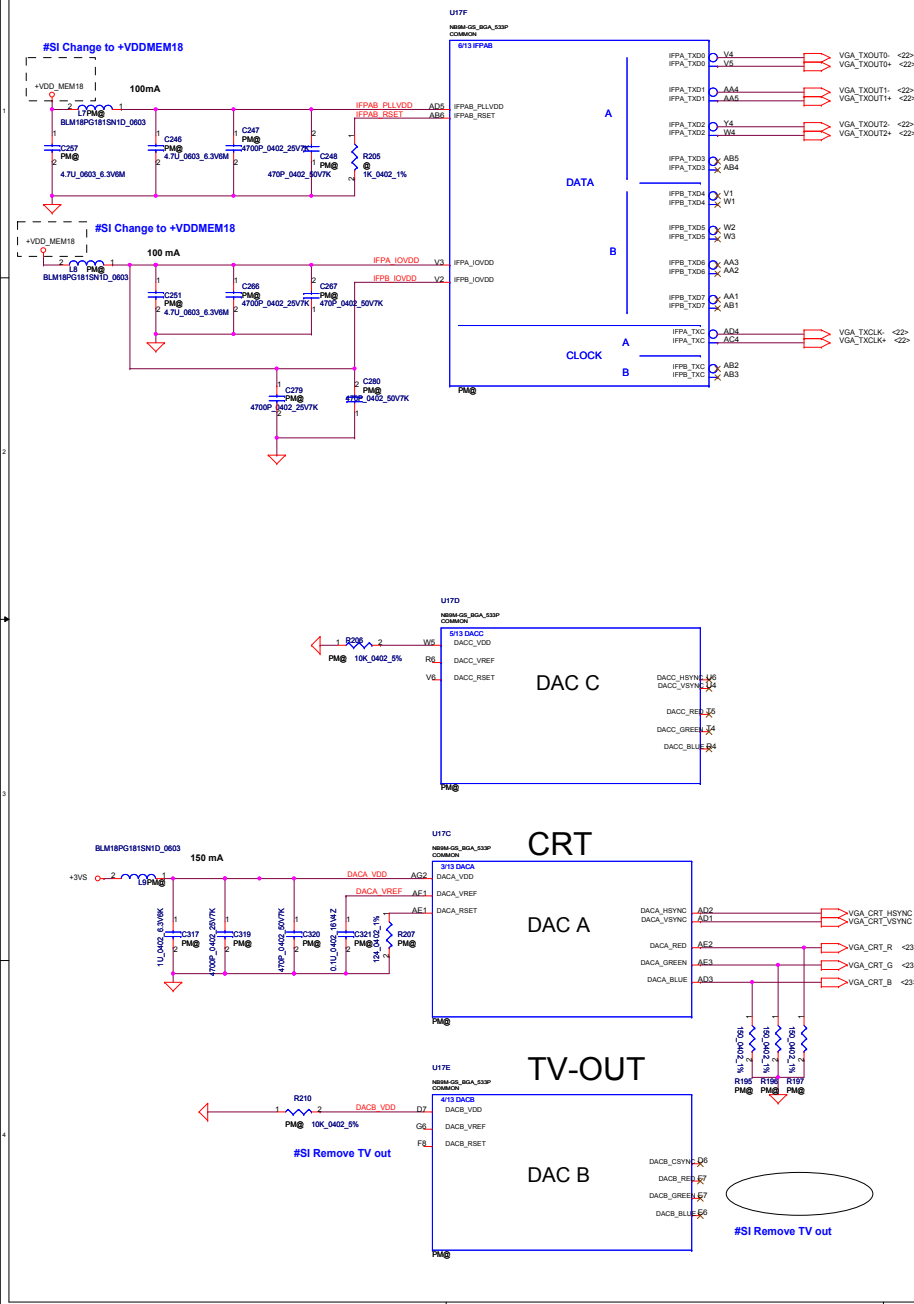


DIMM1 REV H:5.6mm (BOT)

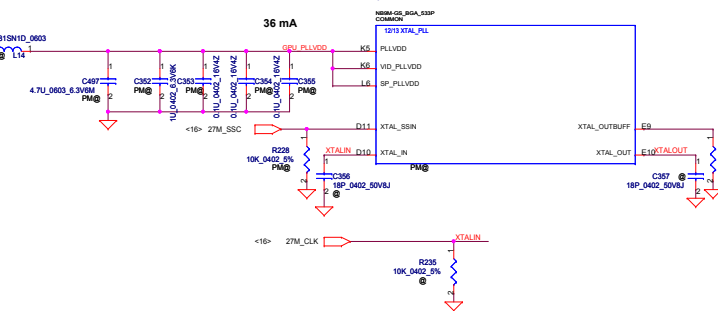
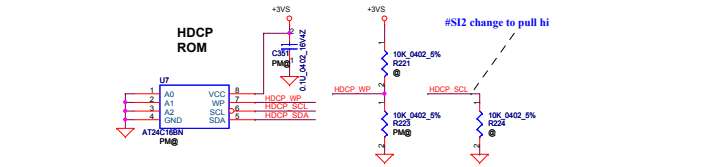
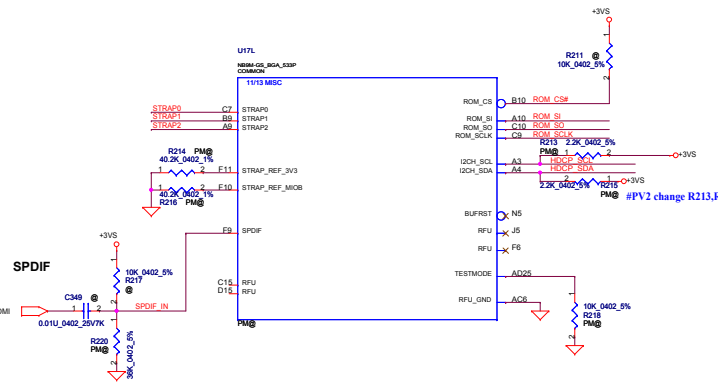
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LVDS & DAC Interface

PEG Interface

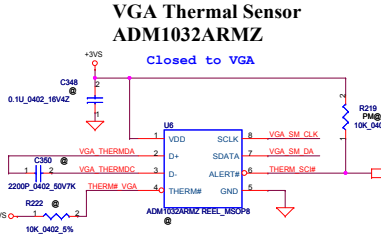
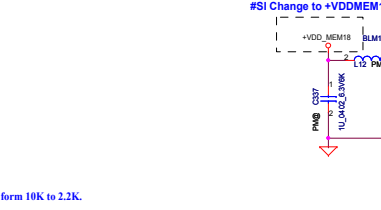
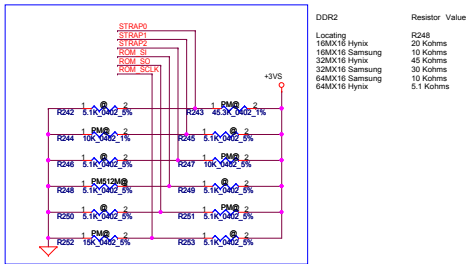


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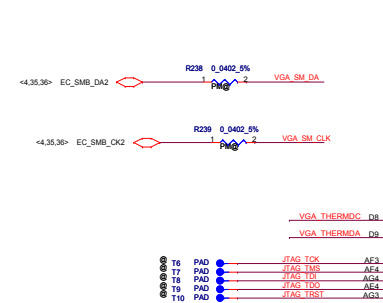
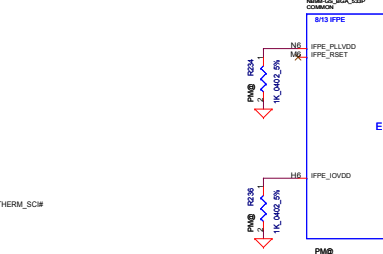
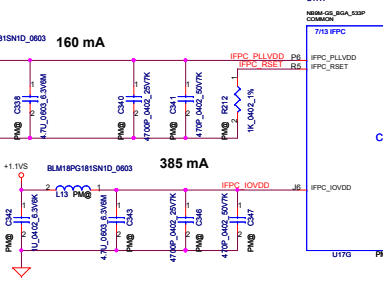
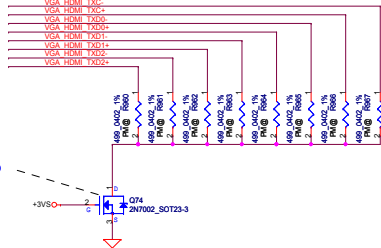


Straps

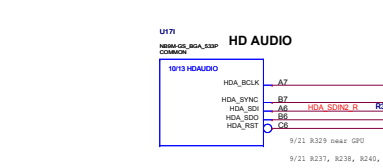
MULTI LEVEL STRAPS



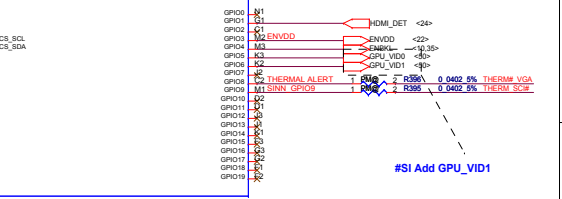
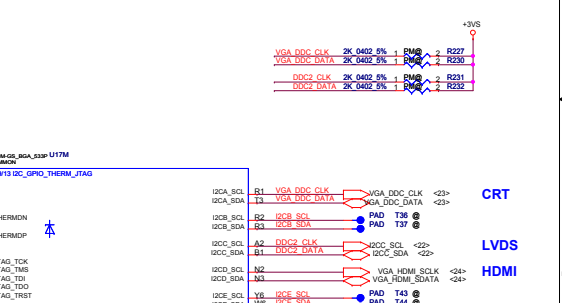
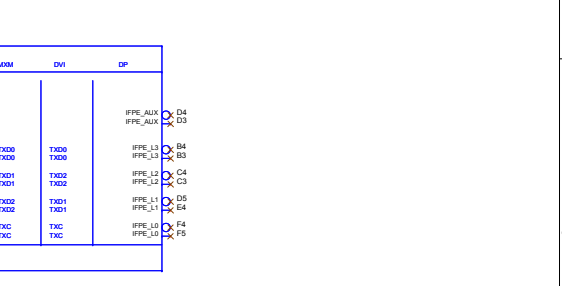
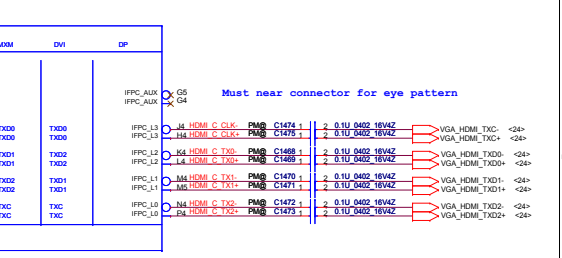
GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	Primary DVI Hot-plug
GPIO1	IN	N/A	2nd DVI Hot-plug
GPIO2	OUT	H	Panel Back-Light PWM
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light Enable
GPIO5	OUT	N/A	NVDD VID0
GPIO6	OUT	N/A	NVDD VID1
GPIO7	OUT	N/A	FBVDD VID0
GPIO8	IN	L	Thermal Alert
GPIO9	OUT	L	FAN PWM
GPIO10	OUT	N/A	FBVref Select
GPIO11	OUT	N/A	SLI SYNC
GPIO12	IN	N/A	AC Detect
GPIO13	OUT	L	PS Control or HDMI_CEC
GPIO14	OUT	H	PS Control



GPU_VID1	GPU_VID0	+VGA_CORE
0	0	0.9V
0	1	1.17V
1	0	unused



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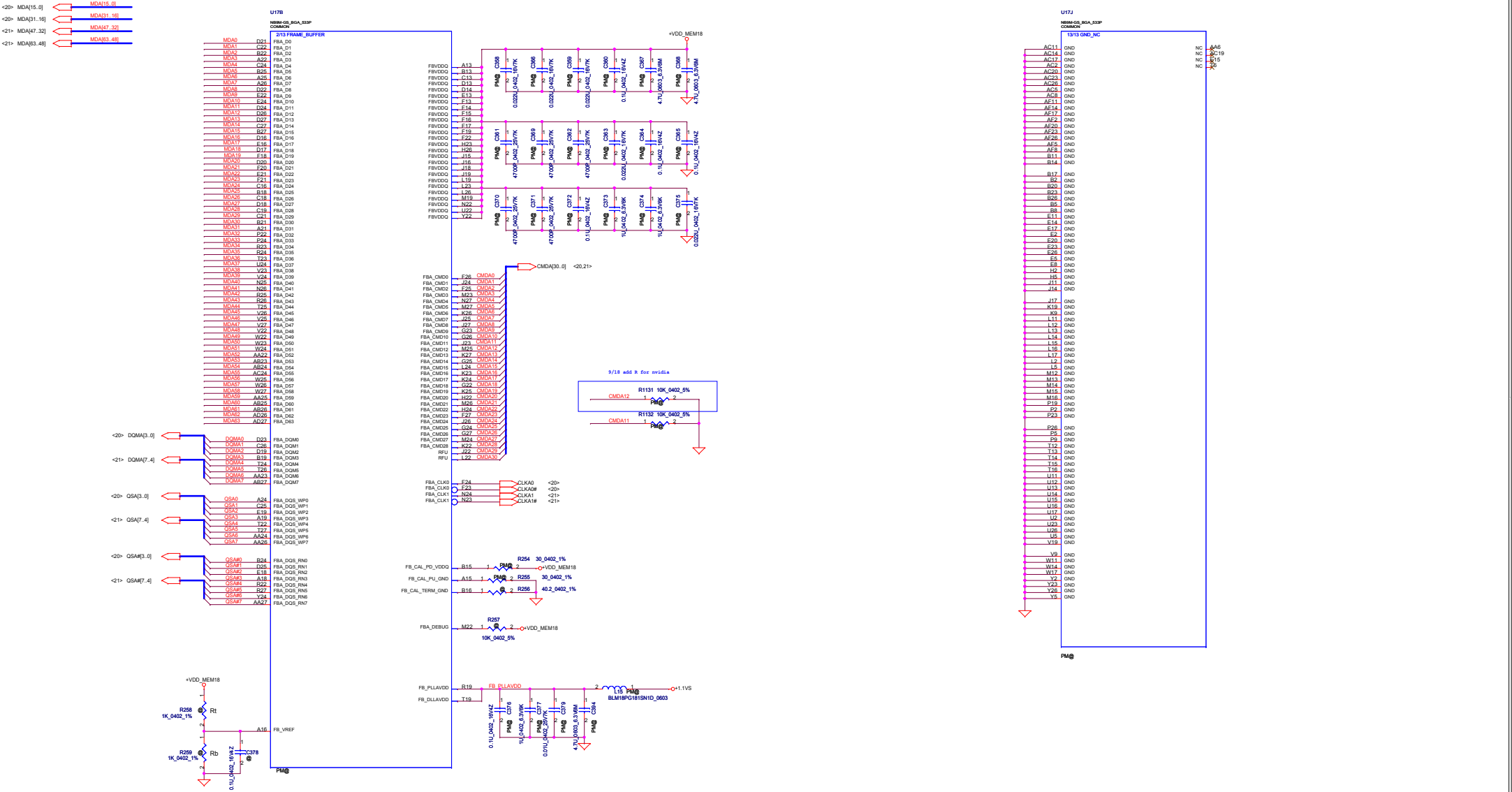


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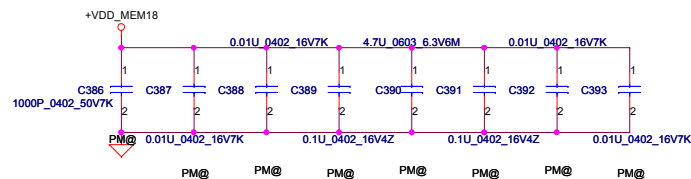
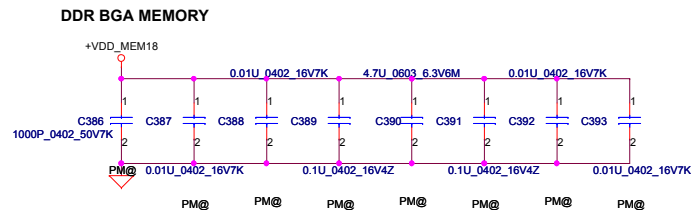
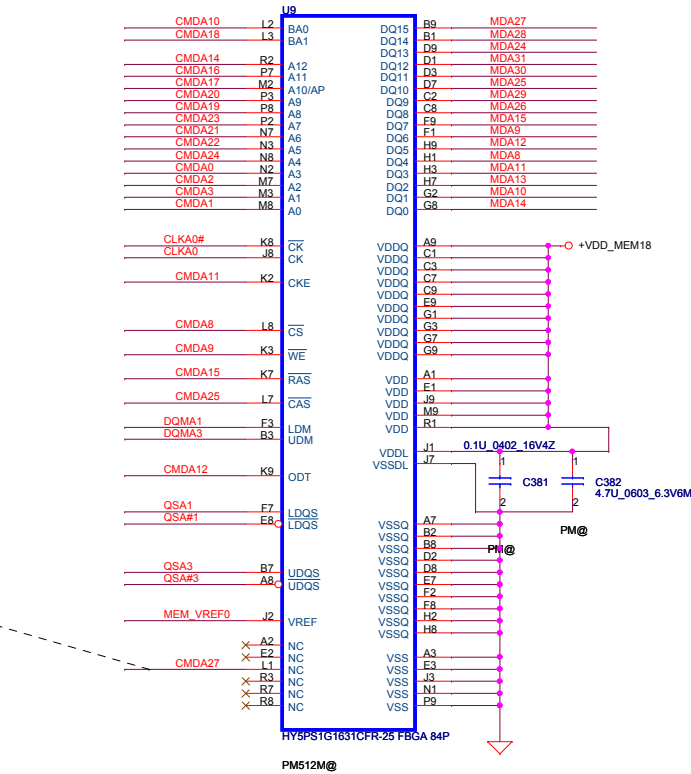
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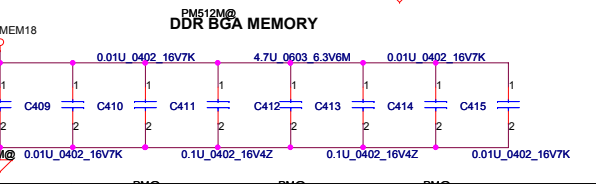
VRAM Interface

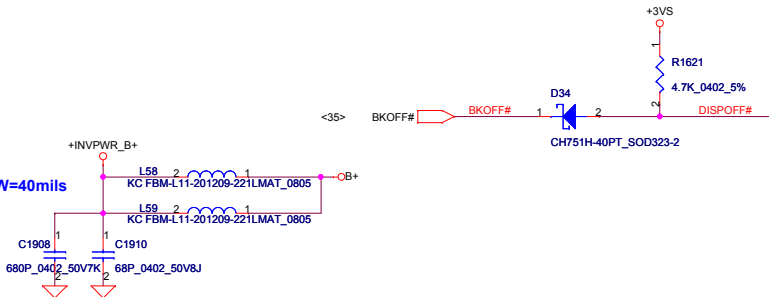
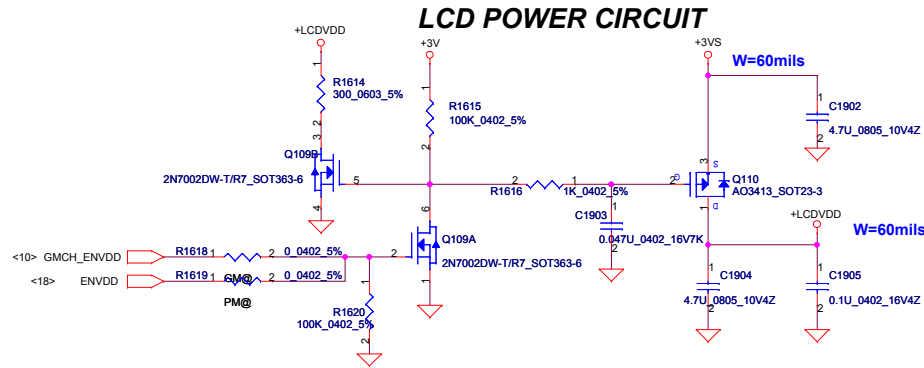


64Mx16 DDR2 400MHz*4==>512MB

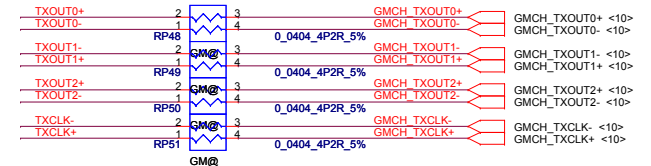
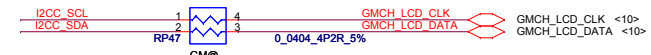
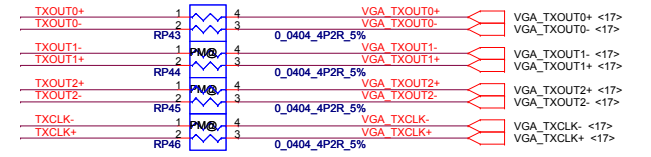
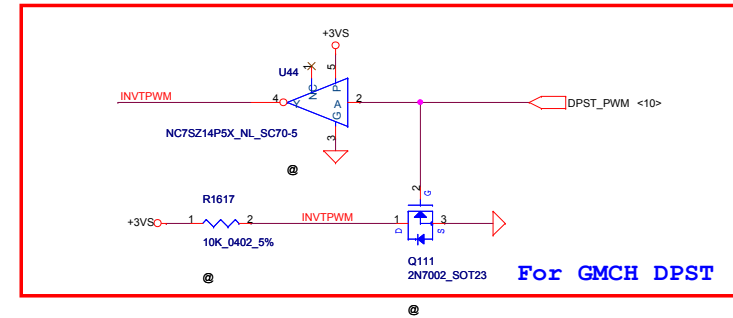
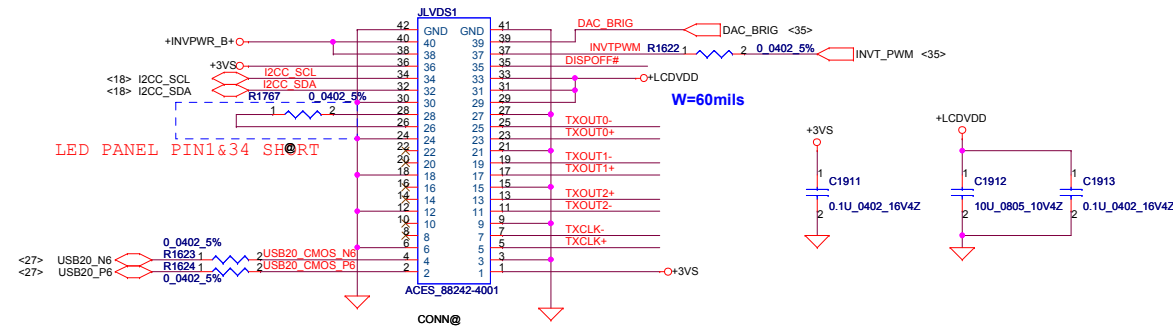


64Mx16 DDR2 400MHz*4==>512MB



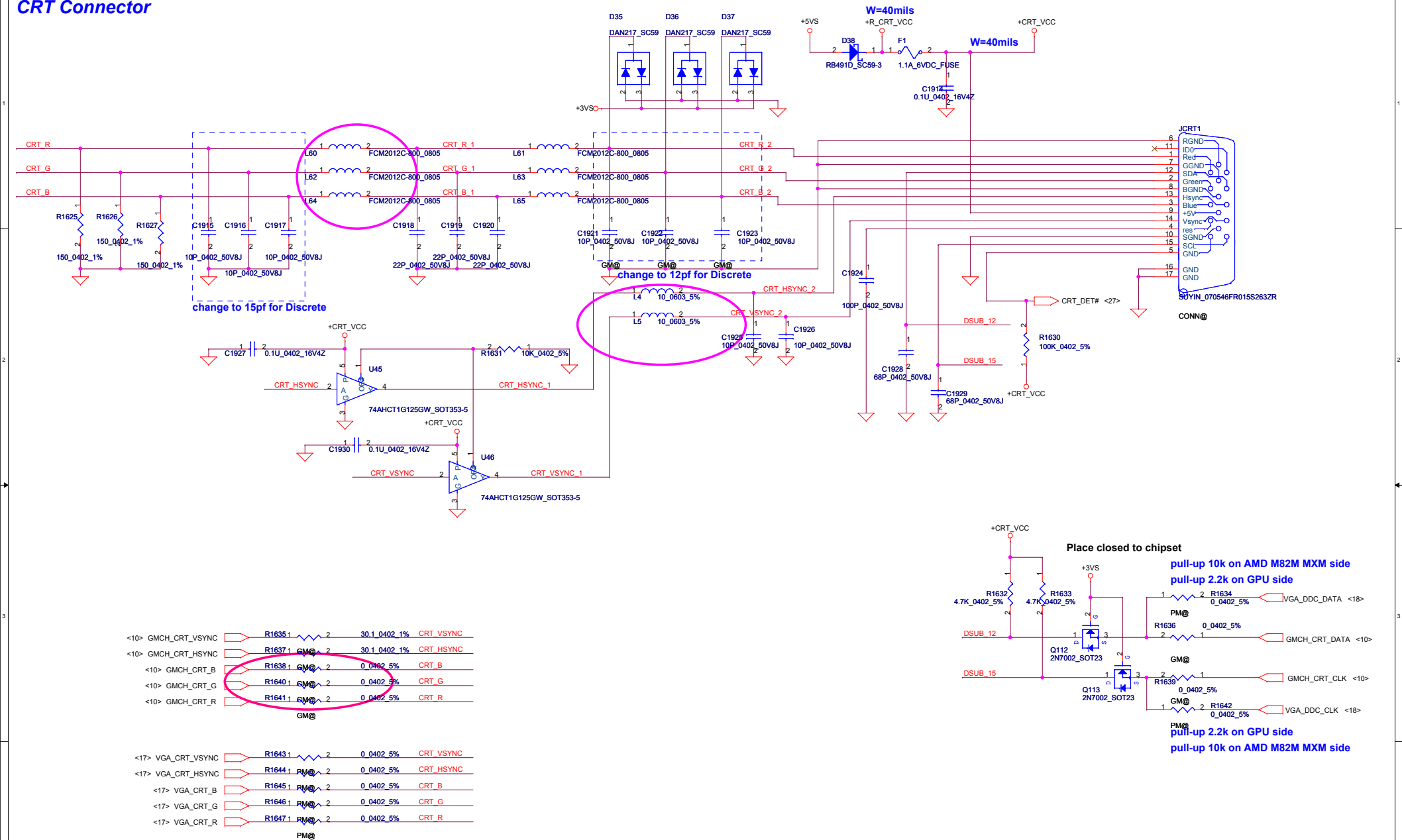


LCD/PANEL BD. Conn.

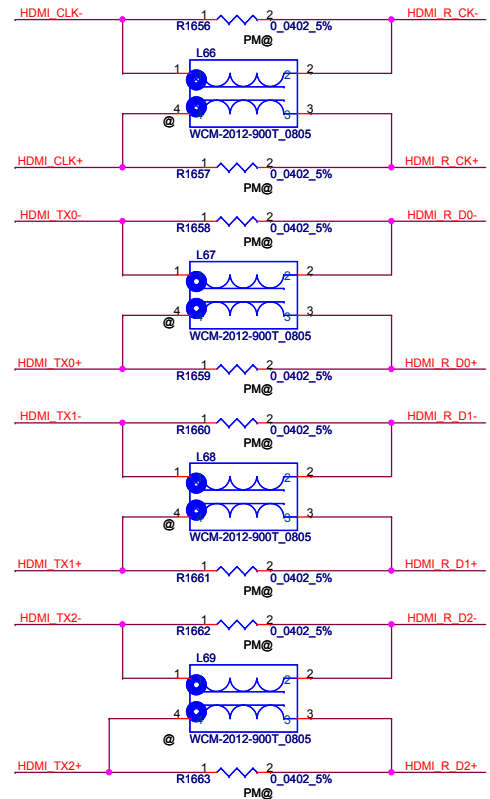
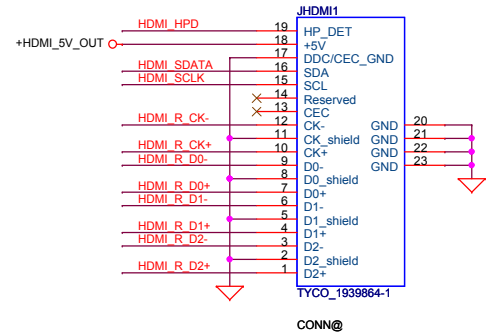
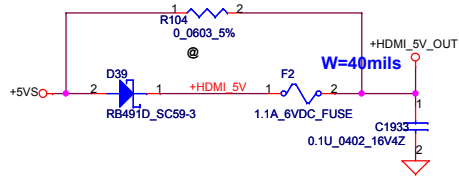
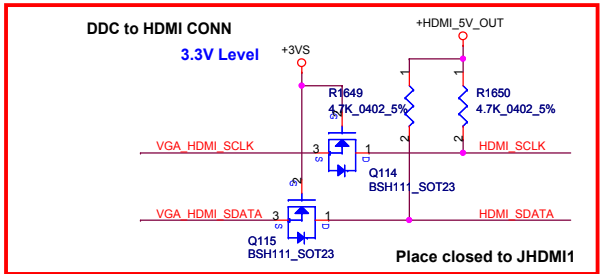
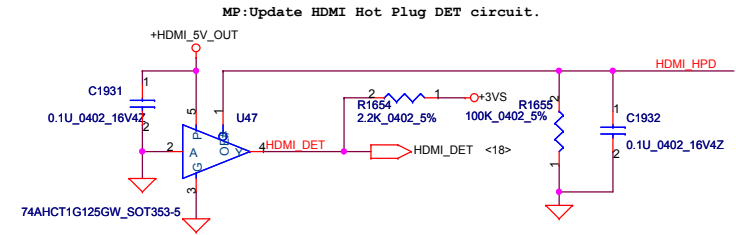
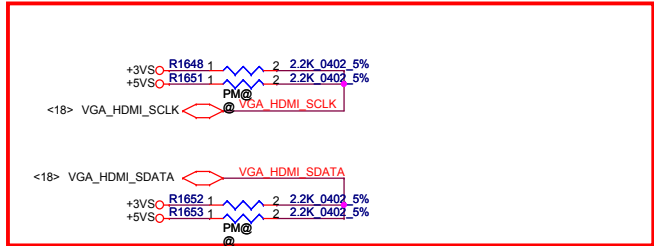


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Size		Document Number		Rev	
Custom		KAL90KALH0		0.2	
Date		Thursday, November 20, 2008		Sheet 22 of 52	

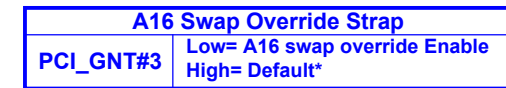
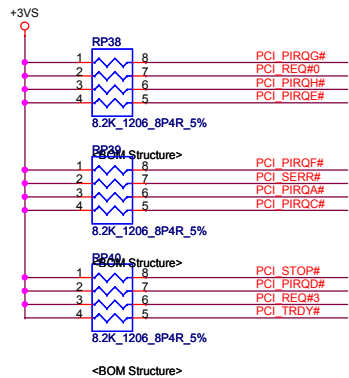
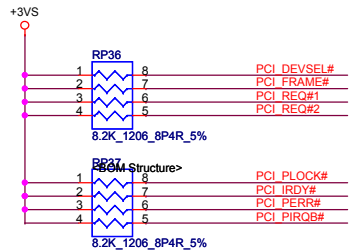
CRT Connector



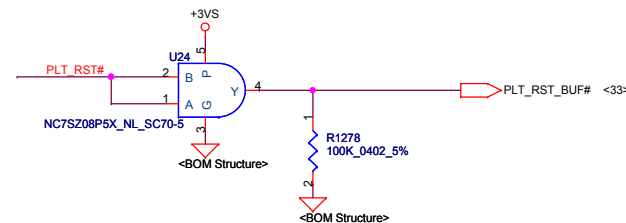
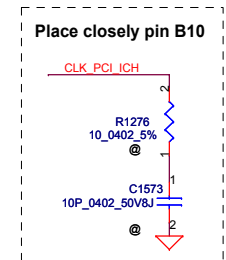
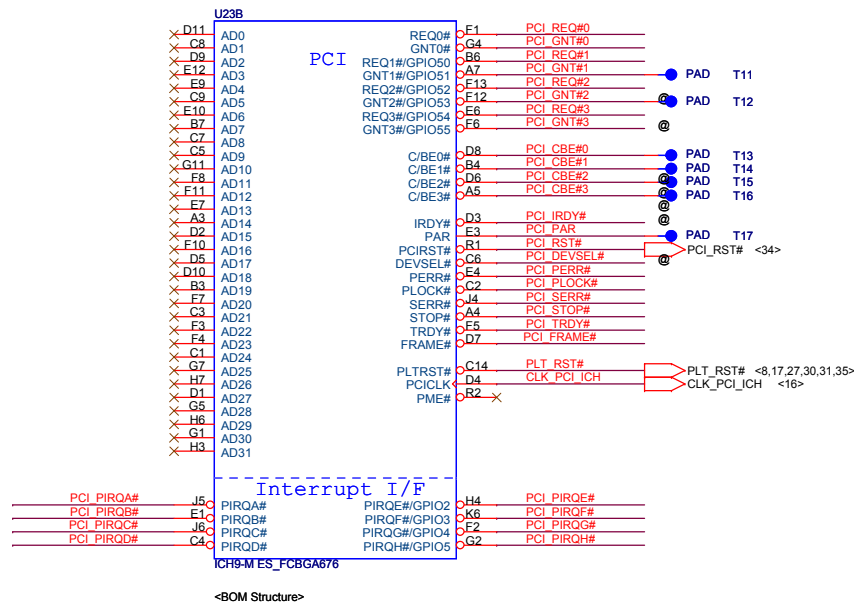
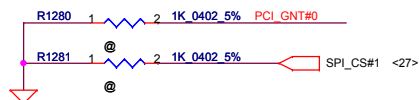
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title CRT Connector		
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				KAL90KALH0		0.2
				Date: Thursday, November 20, 2008		Sheet 23 of 52



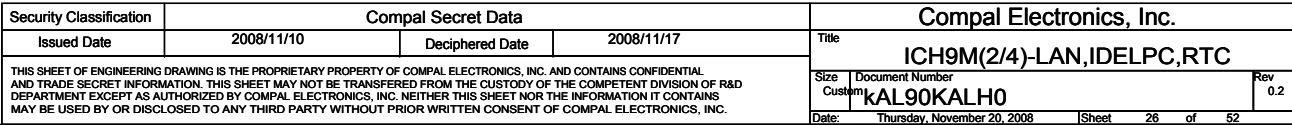
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2008/11/10				Deciphered Date			
2008/11/10				2008/11/17				Title			
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								Document Number			
								KAL90KALH0			
								Date			
								Thursday, November 20, 2008			
								Sheet			
								24 of 52			
								Rev			
								0.2			

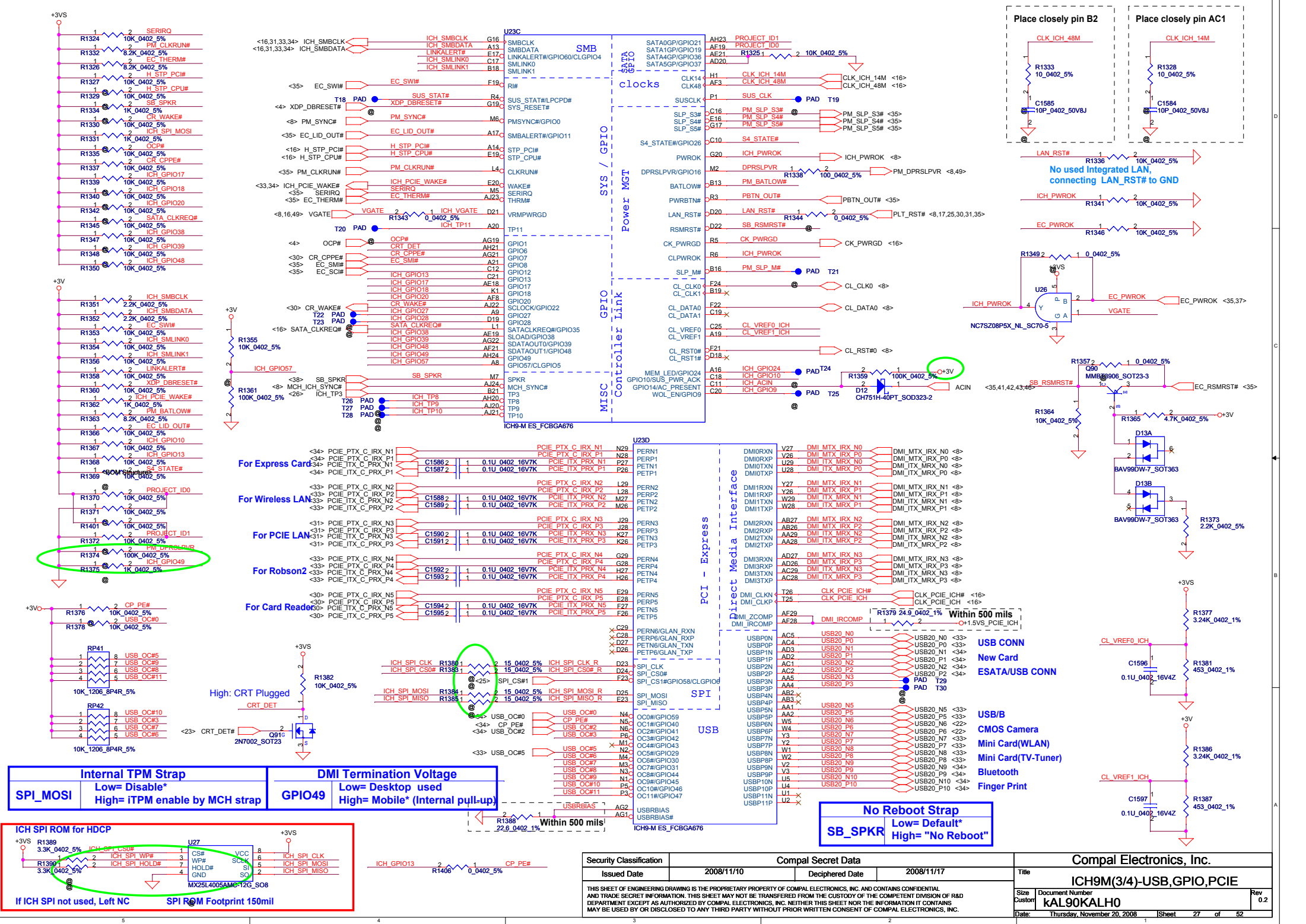


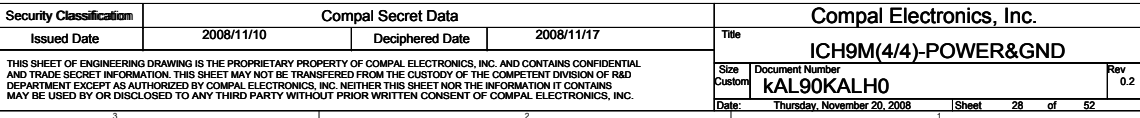
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

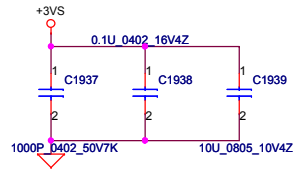


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Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title					
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				Size	Document Number			Rev	
				KAL90KALH0				0.2	
				Date:				Thursday, November 20, 2008	Sheet 25 of 52

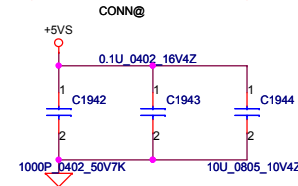
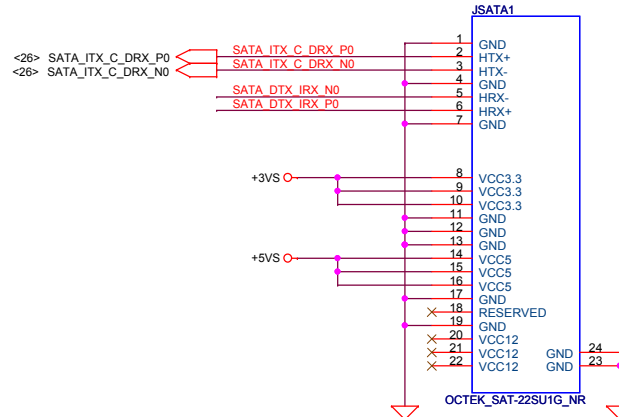
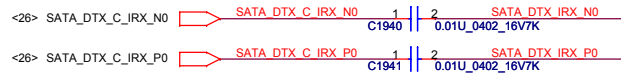




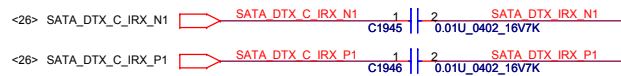
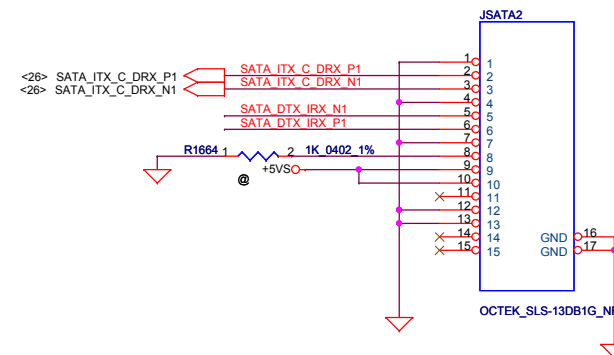




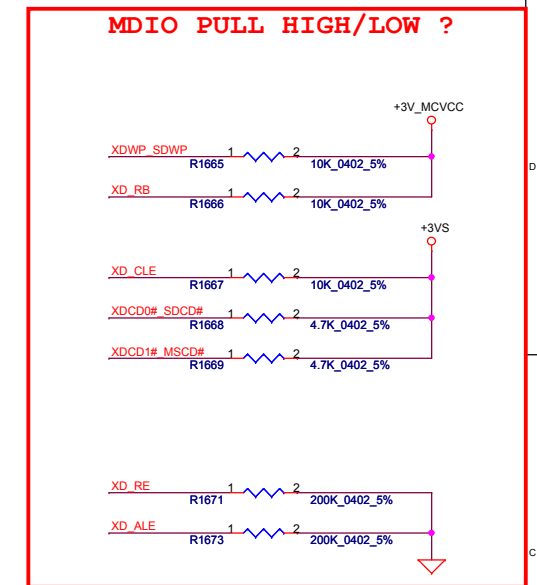
SATA HDD Conn.



SATA ODD Conn.

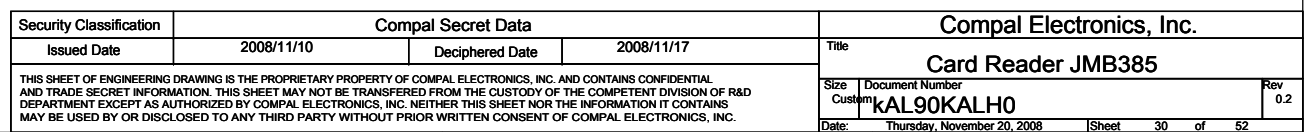


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				Custom	KAL90KALH0
				Date	Thursday, November 20, 2008
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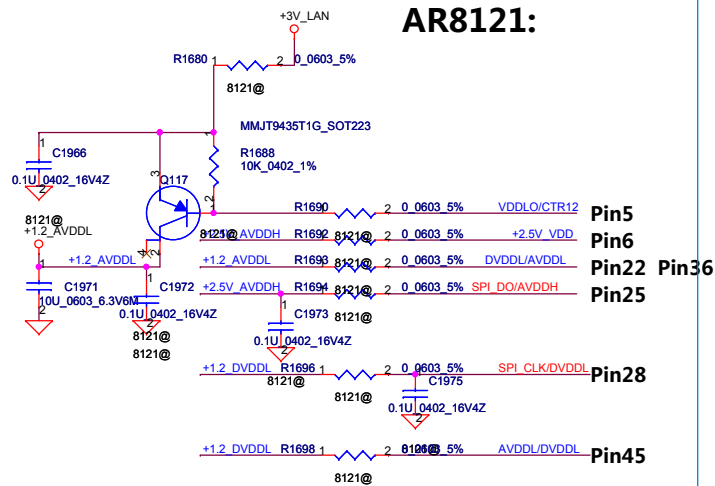


Pin connection diagram for the J7110 module. The diagram shows the J7110 module (left) connected to a J7110 module (right). The J7110 module has pins 1-32 and 33-42. The J7110 module has pins 1-32 and 33-42. The connections are as follows:

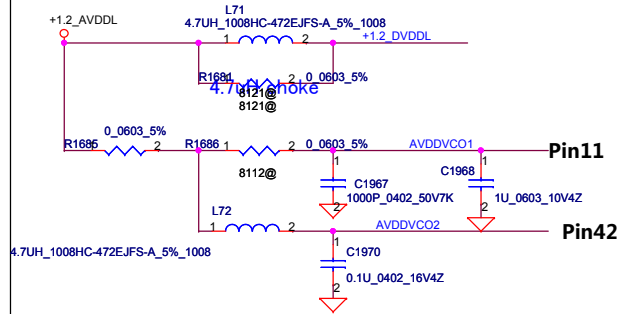
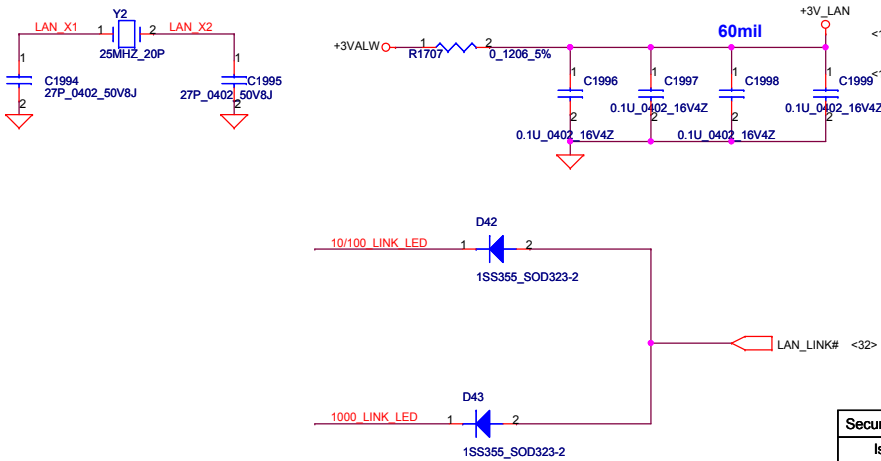
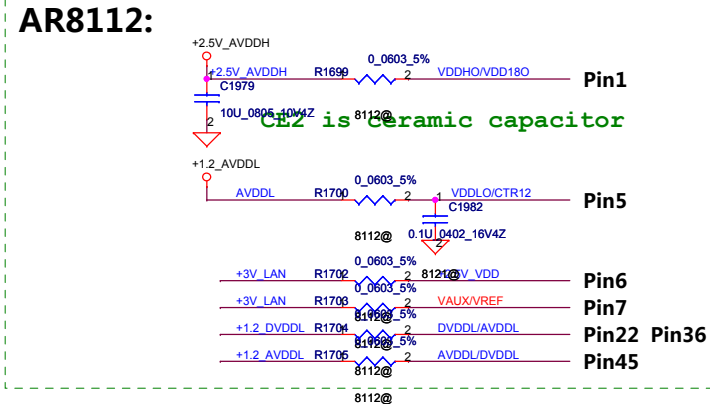
- J7110 Pin 1 to J7110 Pin 1 (3V_MCVCC)
- J7110 Pin 2 to J7110 Pin 2 (3V_MCVCC)
- J7110 Pin 3 to J7110 Pin 3 (XD-VCC)
- J7110 Pin 4 to J7110 Pin 4 (XD-VCC)
- J7110 Pin 5 to J7110 Pin 5 (XD-D0)
- J7110 Pin 6 to J7110 Pin 6 (XD-D1)
- J7110 Pin 7 to J7110 Pin 7 (XD-D2)
- J7110 Pin 8 to J7110 Pin 8 (XD-D3)
- J7110 Pin 9 to J7110 Pin 9 (XD-D4)
- J7110 Pin 10 to J7110 Pin 10 (XD-D5)
- J7110 Pin 11 to J7110 Pin 11 (XD-D6)
- J7110 Pin 12 to J7110 Pin 12 (XD-D7)
- J7110 Pin 13 to J7110 Pin 13 (SDCMD_MSBS_XDWE#)
- J7110 Pin 14 to J7110 Pin 14 (XDWP_SDWP)
- J7110 Pin 15 to J7110 Pin 15 (XD_ALE)
- J7110 Pin 16 to J7110 Pin 16 (XD_CD#)
- J7110 Pin 17 to J7110 Pin 17 (XD_RB)
- J7110 Pin 18 to J7110 Pin 18 (XD_RE)
- J7110 Pin 19 to J7110 Pin 19 (XDCE_SDCLK_MSCLK)
- J7110 Pin 20 to J7110 Pin 20 (XD_CLE)
- J7110 Pin 21 to J7110 Pin 21 (7IN1 GND)
- J7110 Pin 22 to J7110 Pin 22 (7IN1 GND)
- J7110 Pin 23 to J7110 Pin 23 (7IN1 GND)
- J7110 Pin 24 to J7110 Pin 24 (7IN1 GND)
- J7110 Pin 25 to J7110 Pin 25 (7IN1 GND)
- J7110 Pin 26 to J7110 Pin 26 (7IN1 GND)
- J7110 Pin 27 to J7110 Pin 27 (7IN1 GND)
- J7110 Pin 28 to J7110 Pin 28 (7IN1 GND)
- J7110 Pin 29 to J7110 Pin 29 (7IN1 GND)
- J7110 Pin 30 to J7110 Pin 30 (7IN1 GND)
- J7110 Pin 31 to J7110 Pin 31 (7IN1 GND)
- J7110 Pin 32 to J7110 Pin 32 (7IN1 GND)
- J7110 Pin 33 to J7110 Pin 33 (7IN1 GND)
- J7110 Pin 34 to J7110 Pin 34 (7IN1 GND)
- J7110 Pin 35 to J7110 Pin 35 (7IN1 GND)
- J7110 Pin 36 to J7110 Pin 36 (7IN1 GND)
- J7110 Pin 37 to J7110 Pin 37 (7IN1 GND)
- J7110 Pin 38 to J7110 Pin 38 (7IN1 GND)
- J7110 Pin 39 to J7110 Pin 39 (7IN1 GND)
- J7110 Pin 40 to J7110 Pin 40 (7IN1 GND)
- J7110 Pin 41 to J7110 Pin 41 (7IN1 GND)
- J7110 Pin 42 to J7110 Pin 42 (7IN1 GND)



AR8121:

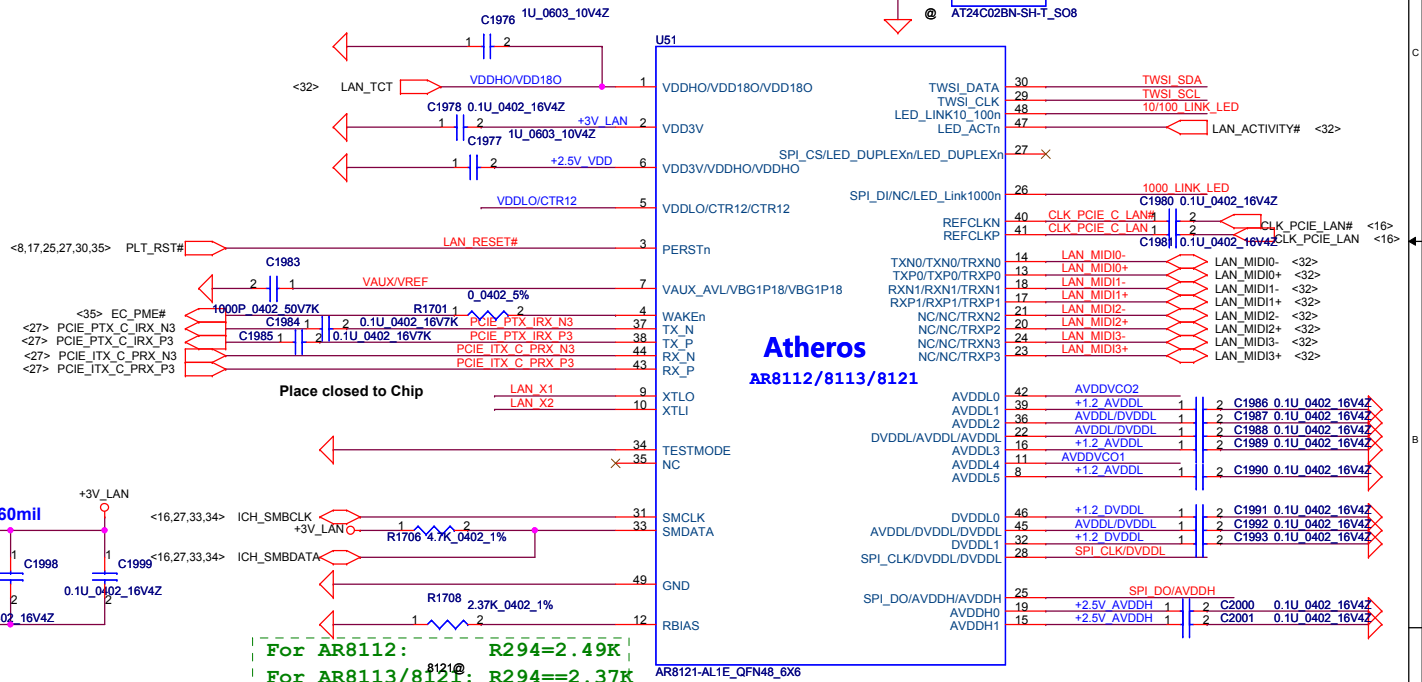
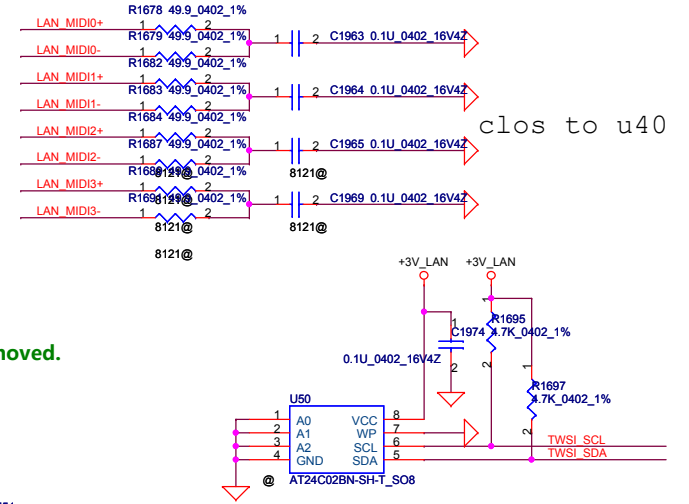


AR8112:



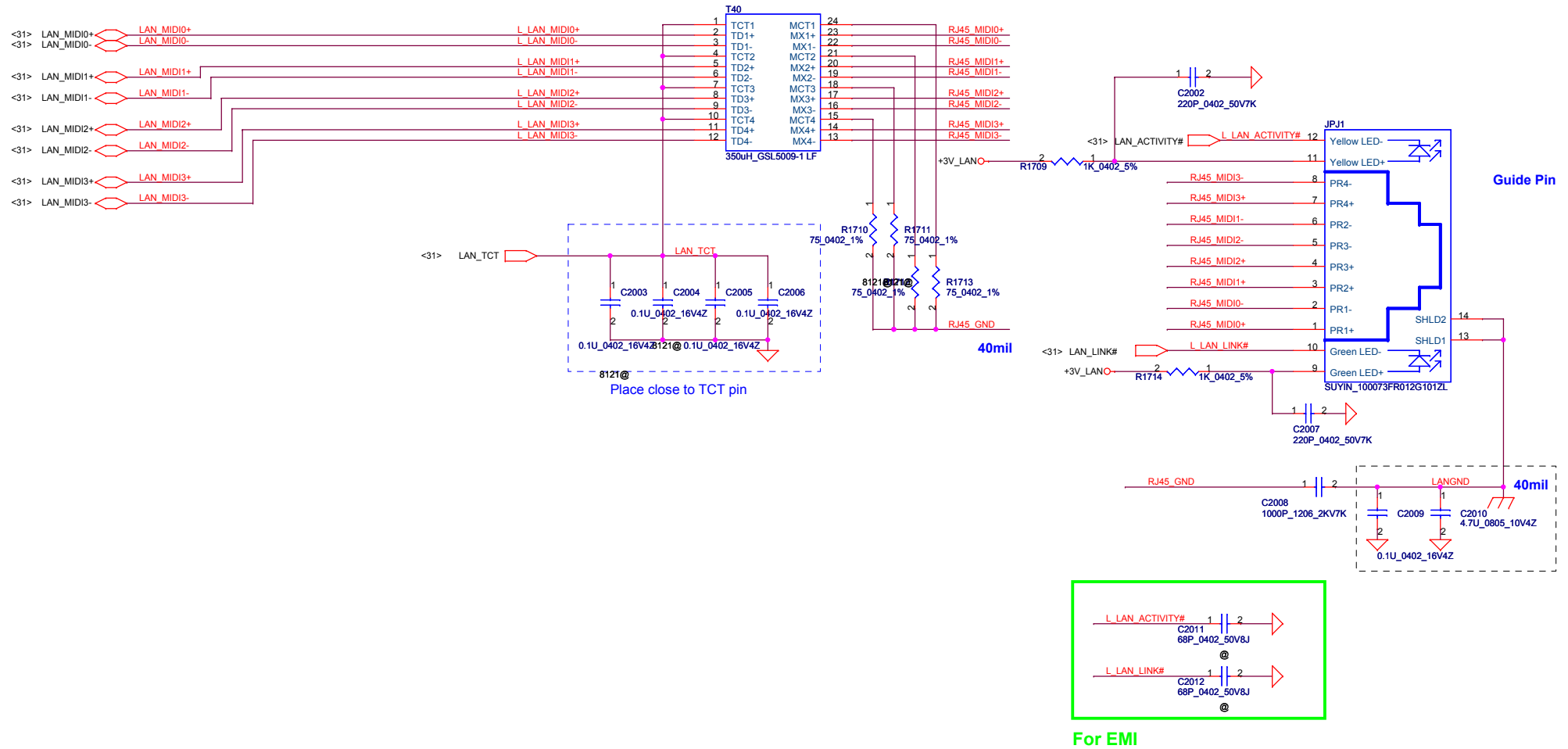
AR8113/AR8121: If overclocking, R592, L49 stuffed and removed. If not overclocking, R591, L49 stuffed and R592 removed.

AR8112: Stuff R591, R48 and L49 for all mode.



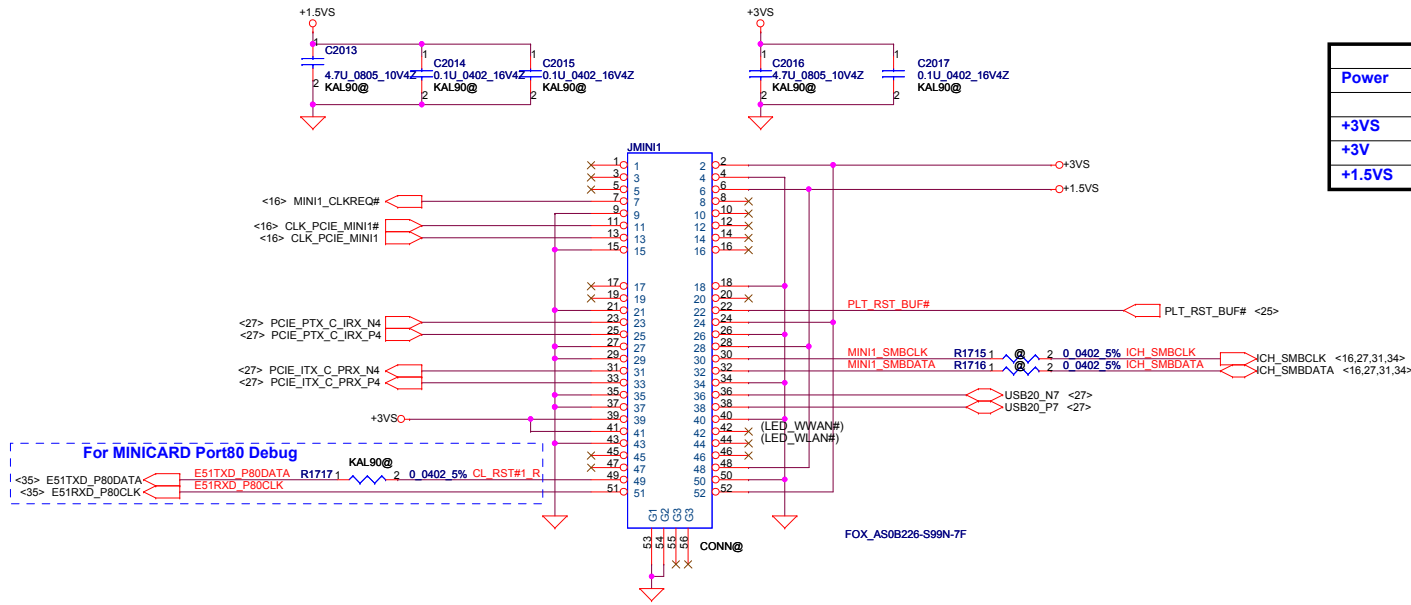
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Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title Atheros Ar121/8112			
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				Customer	KAL90KALH0	0.2	
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LAN AR8121/8112



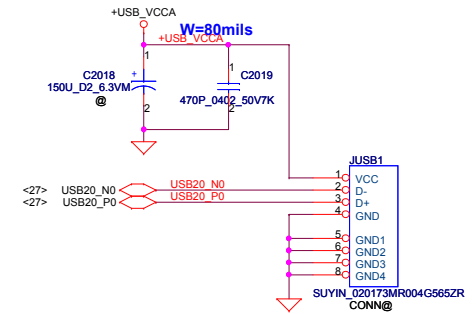
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title	
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				Date	Thursday, November 20, 2008
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				Rev	0.2

For Robson2

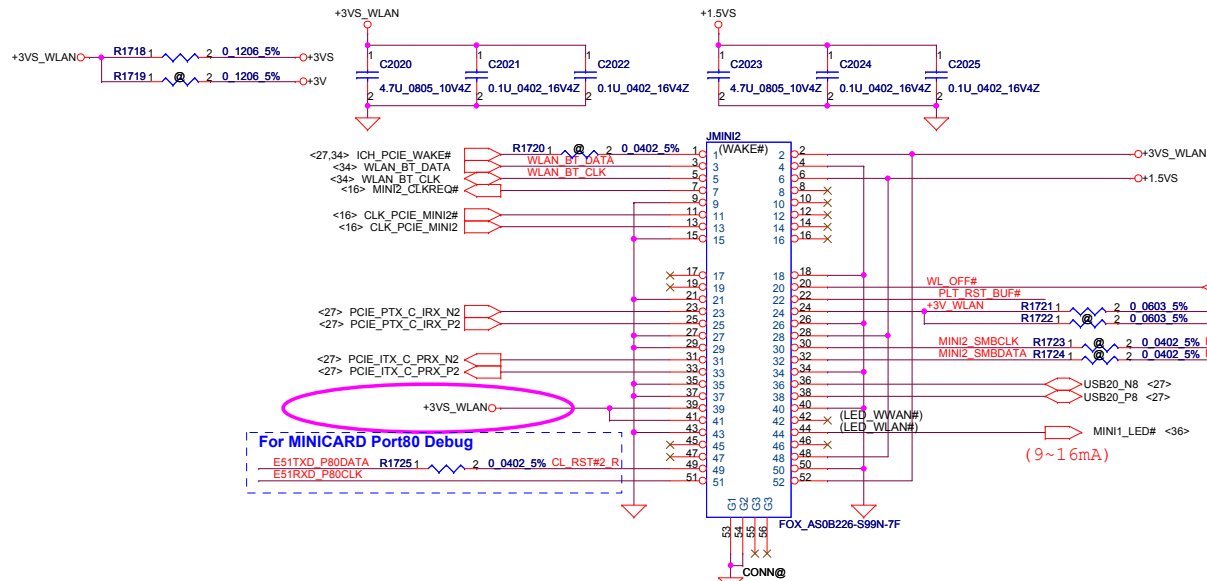


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

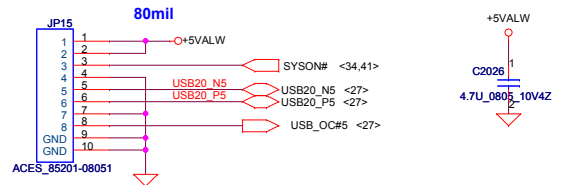
USB CONN.



For Wireless LAN

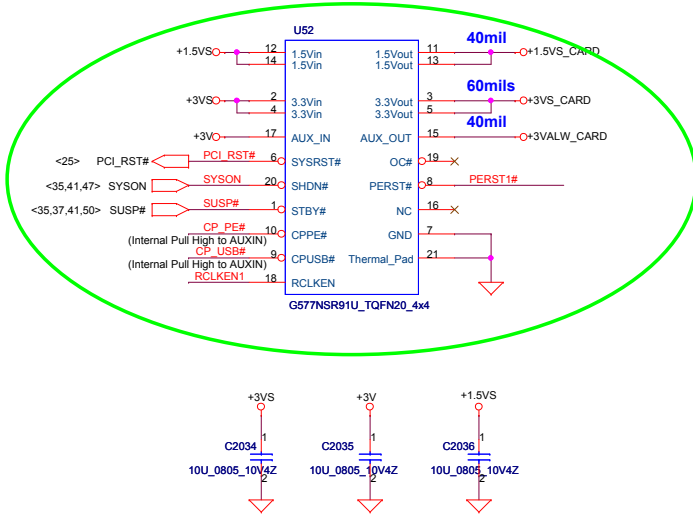


To USB/B Connector

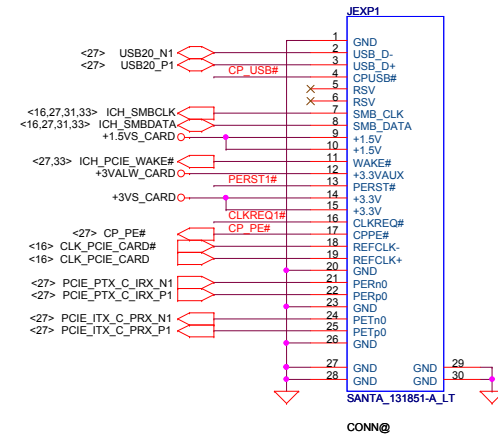


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				Size B	Document Number kAL90KALH0	Rev 0.2
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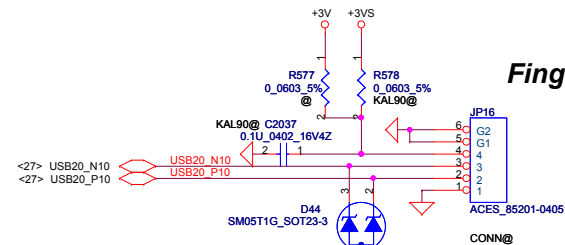
New Card Power Switch



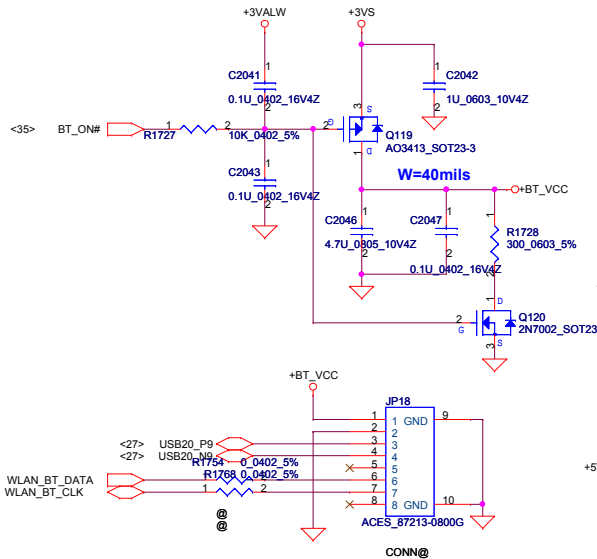
New Card Socket (Left/TOP)



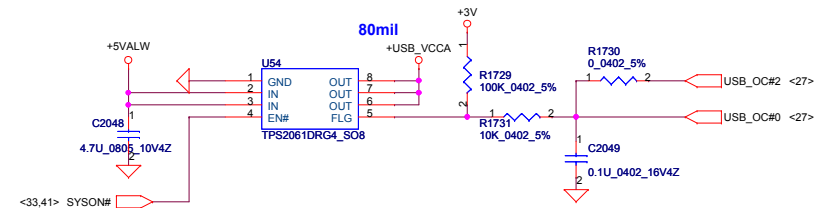
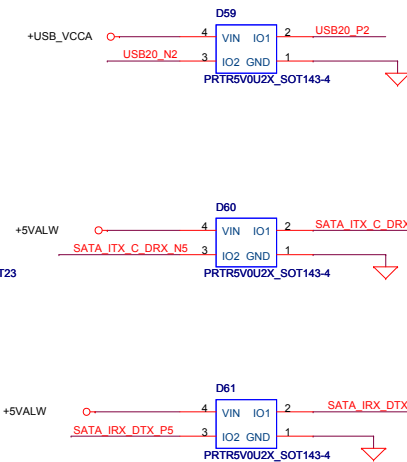
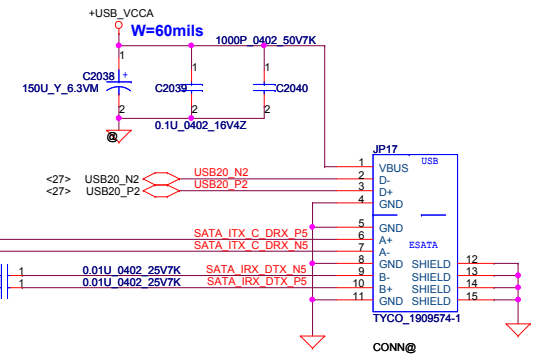
Finger Print Conn.



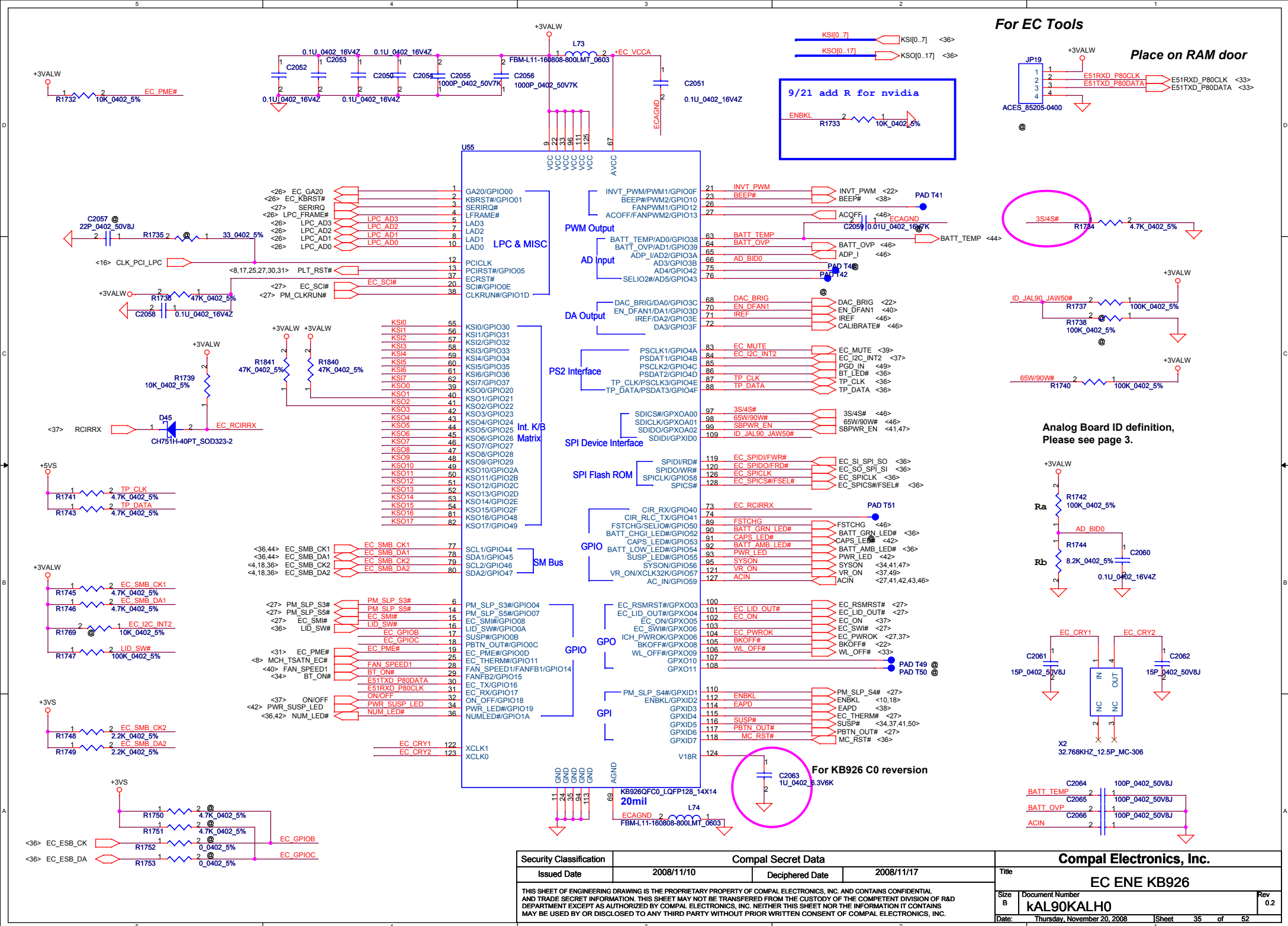
Bluetooth Conn.



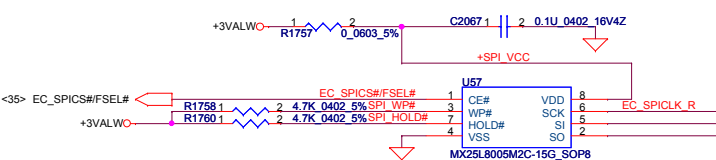
ESATA CONN



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Issued Date	2008/11/10	Deciphered Date	2008/11/17	NEW CARD & eSATA Connector	
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				Date:	Thursday, November 20, 2008
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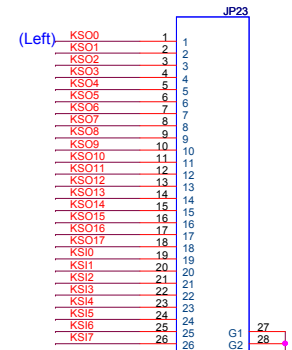


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Issued Date	2008/11/10	Deciphered Date	2008/11/17	EC ENE KB926			
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				Size B	Document Number KAL90KALH0	Rev 0.2	
Date:				Thursday, November 20, 2008	Sheet	35	of 52

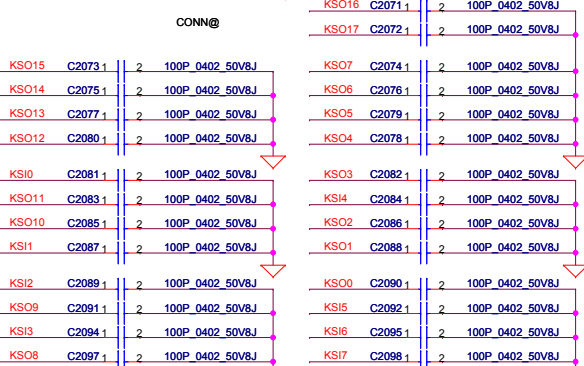


ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz

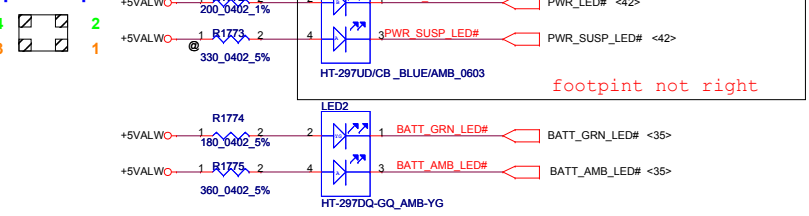
INT_KBD Conn.



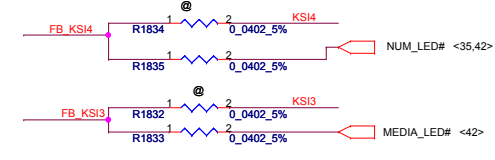
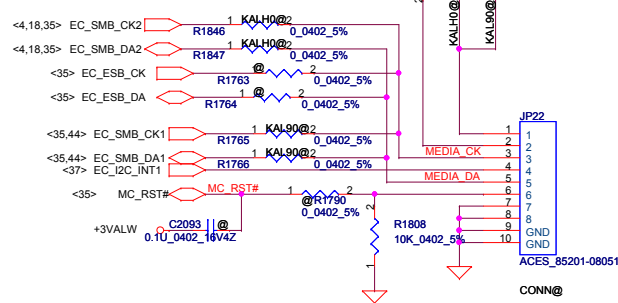
(Right)



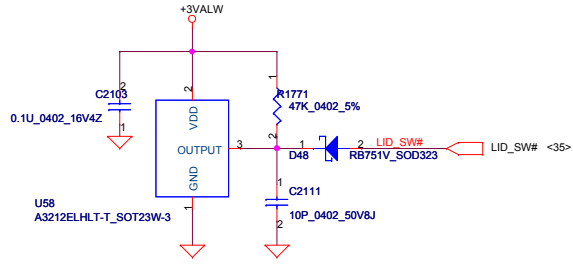
Compal Footprint



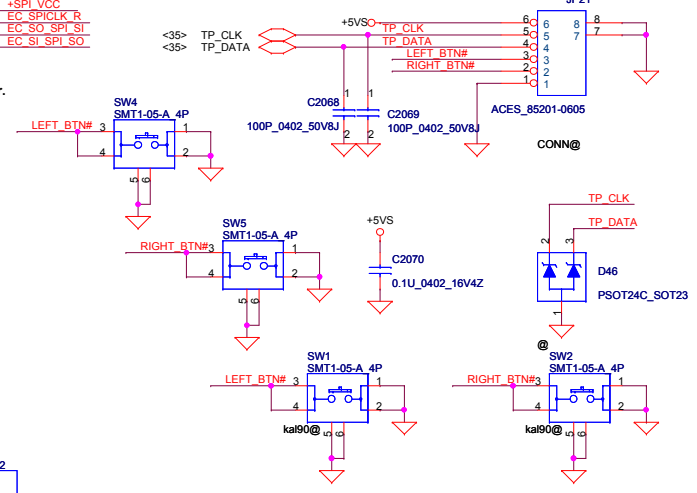
To Media/B Conn.



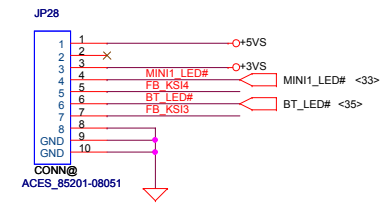
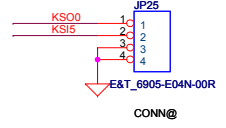
Lid Switch (Hall Effect Switch)



To TP/B Conn.

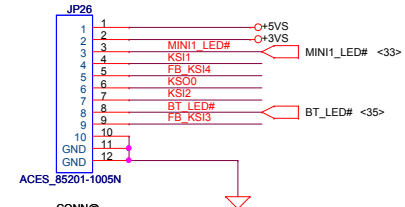


e-key/B

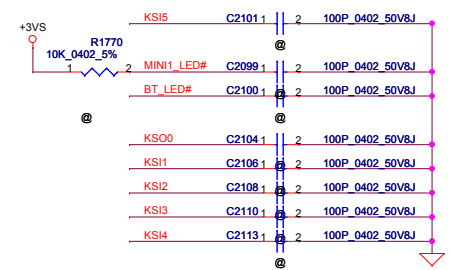


To BTN/B Conn.

	KSO0
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#



FOR EMI



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Size B	Document Number	KAL90KALH0		Rev	0.2	
Date:	Tuesday, January 06, 2009	Sheet	36	of	52	

ON/OFF switch

[illegible]

The schematic diagram illustrates the power management section for the South Bridge and VCCP/+1.05VS. It is divided into two main horizontal sections.

Top Section (South Bridge):

- Inputs:** +3VS, +3VALW, VR_ON (<35,49>).
- Components:**
 - VR_ON is connected to pin 1 of D51 (CH751H-40PT_SOD323-2).
 - D51 is connected to pin 2 of R1784 (180K_0402_5%).
 - R1784 is connected to pin 1 of U59A (SN74LVC14APWLE_TSSOP14).
 - U59A is connected to pin 14 of U59B (SN74LVC14APWLE_TSSOP14).
 - U59B is connected to pin 1 of R1785 (10K_0402_5%).
 - R1785 is connected to pin 1 of SYS_PWROK (<27,35>).
- Outputs:** +3VALW, SYS_PWROK, EC_PWROK (<27,35>).
- Other Components:** C2117 (1U_0603_10V6K) is connected to the ground of the South Bridge section.

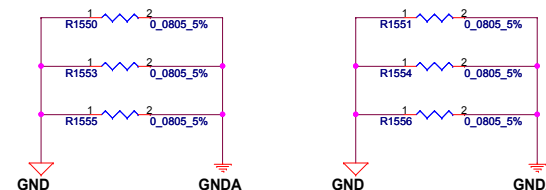
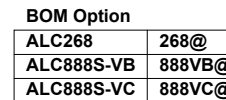
Bottom Section (VCCP/+1.05VS):

- Inputs:** +3VS, +3VALW, SUSP (<50>), SUSP (<48>).
- Components:**
 - SUSP (<50>) is connected to pin 1 of R1787 (10K_0402_1%).
 - R1787 is connected to pin 2 of Q123 (2N7002_SOT23).
 - Q123 is connected to pin 2 of C2118 (0.1U_0402_16V7K).
 - C2118 is connected to pin 2 of U59C (SN74LVC14APWLE_TSSOP14).
 - U59C is connected to pin 14 of U59D (SN74LVC14APWLE_TSSOP14).
 - U59D is connected to pin 1 of VS_ON (<47,48>).
- Outputs:** +3VALW, VS_ON (<47,48>).

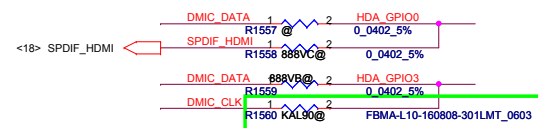
Labels:

- For South Bridge:** Located above the top section.
- For +VCCP/+1.05VS:** Located below the bottom section.

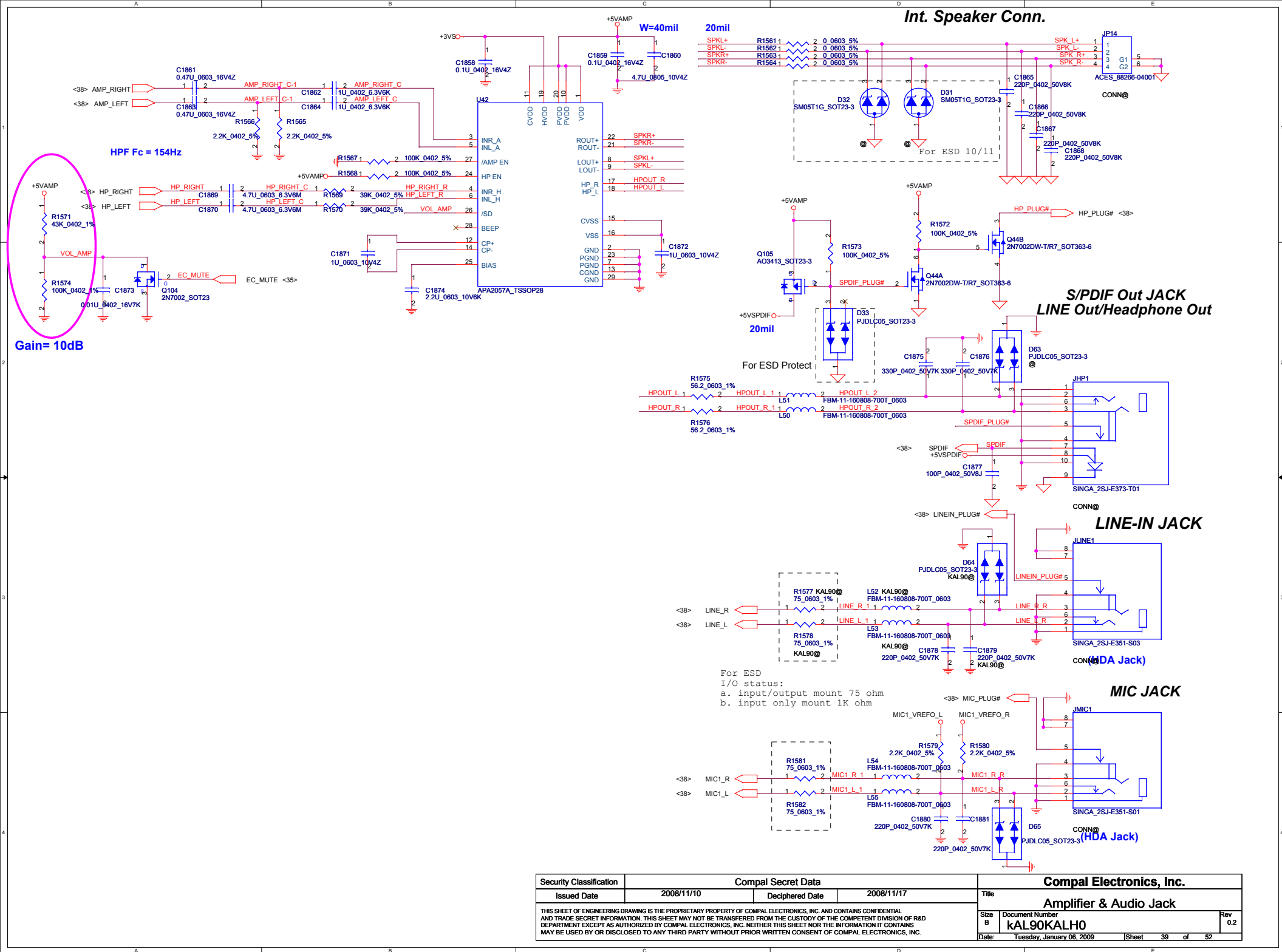
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title Power OK, Reset,RTC, CIR, MDC		
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				KAL90KALH0		
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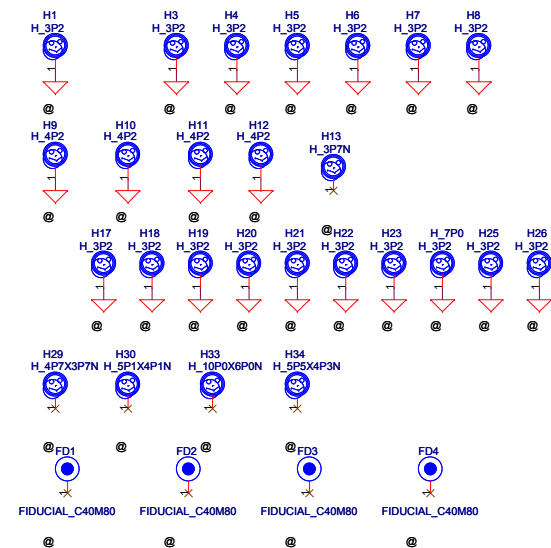
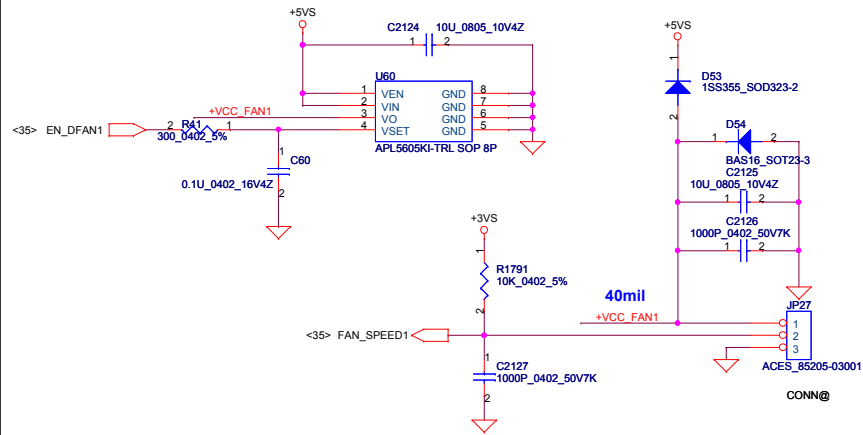
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



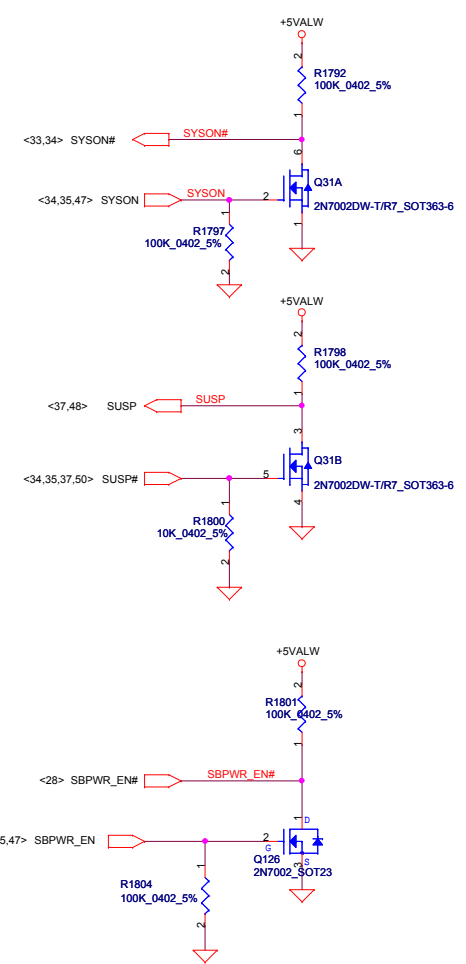
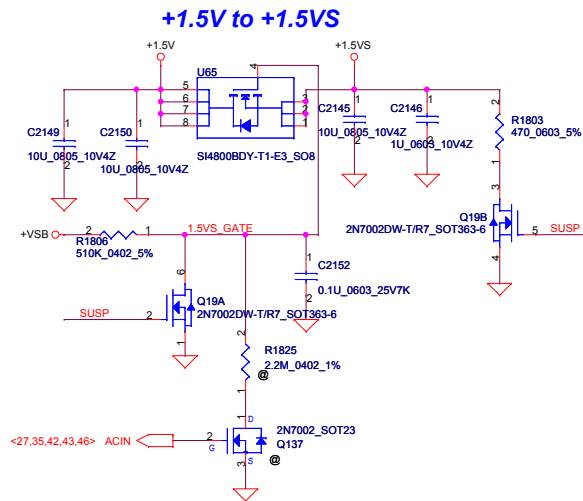
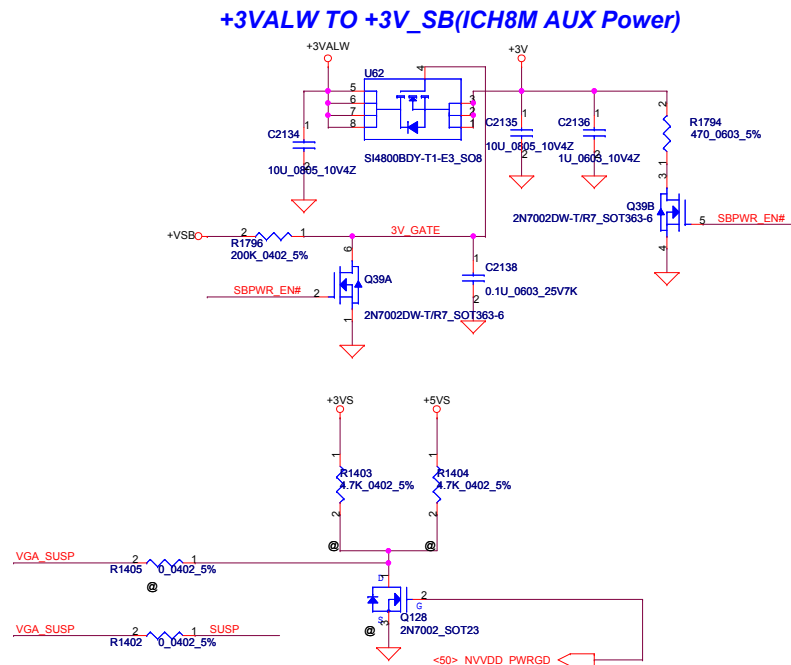
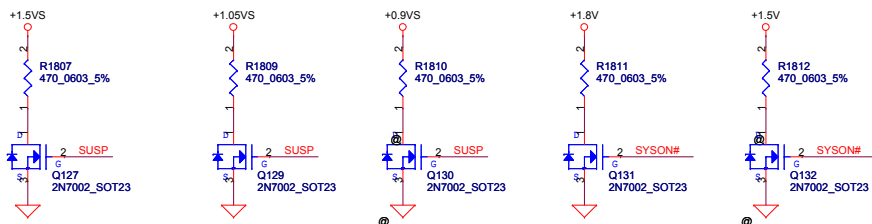
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title	HD Audio Codec ALC888S-VC	
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				kAL90KALH0		
				Date:	Wednesday, December 10, 2008	Sheet 38 of 52



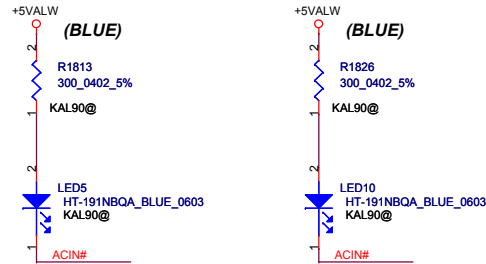
FAN1 Conn



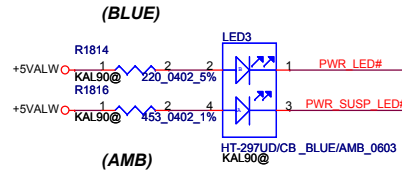
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2008/11/10		Deciphered Date	
2008/11/10		2008/11/17		Title	
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				Document Number	
				KAL90KALH0	
				Rev	
				0.2	
				Date:	
				Thursday, November 20, 2008	
				Sheet	
				40	
				of	
				52	



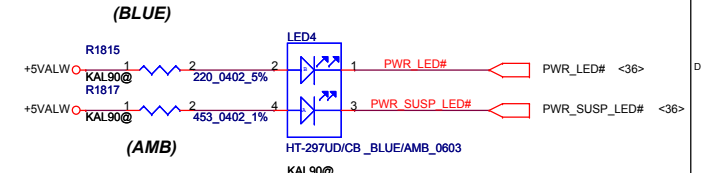
Enlightener LED



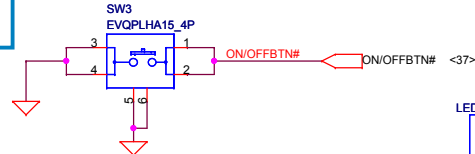
ON/OFF LED LEFT



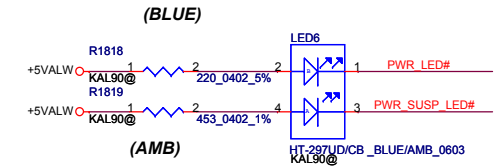
ON/OFF LED RIGHT



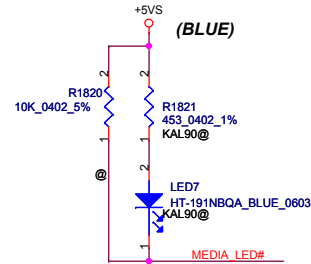
ON/OFF Button



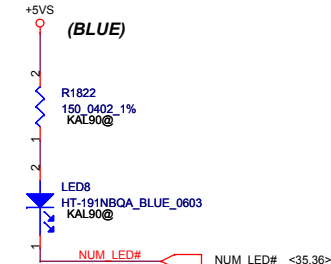
ON/OFF LED DOWN



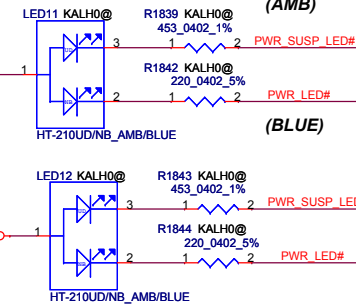
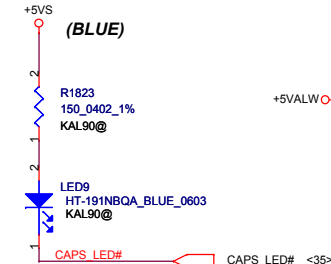
MEDIA_LED



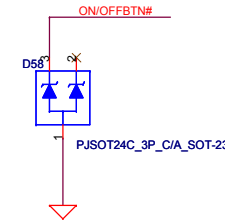
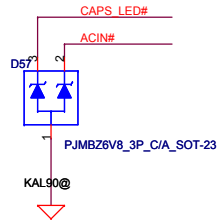
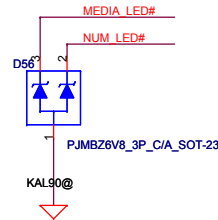
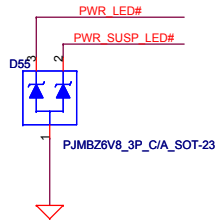
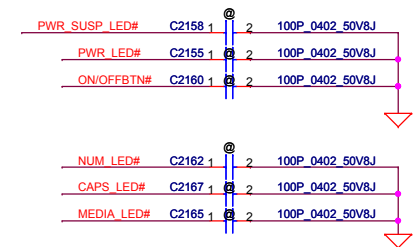
NUM_LED



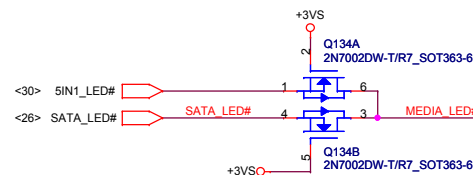
CAPS_LED



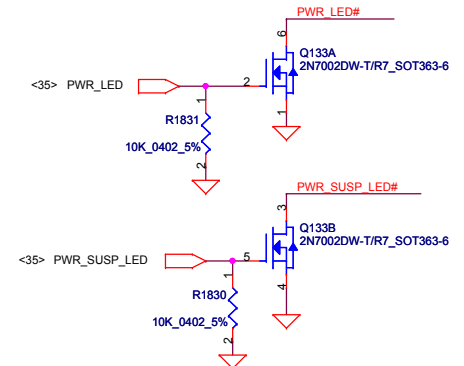
FOR EMI



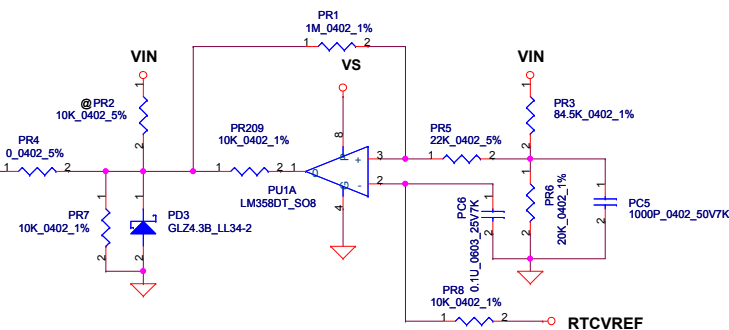
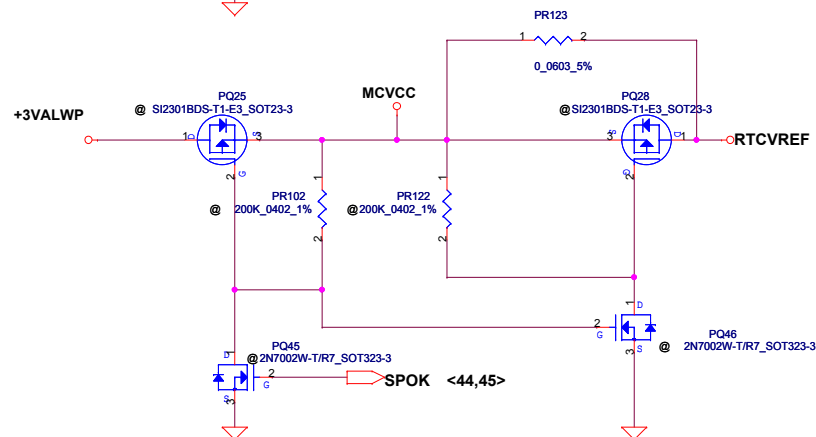
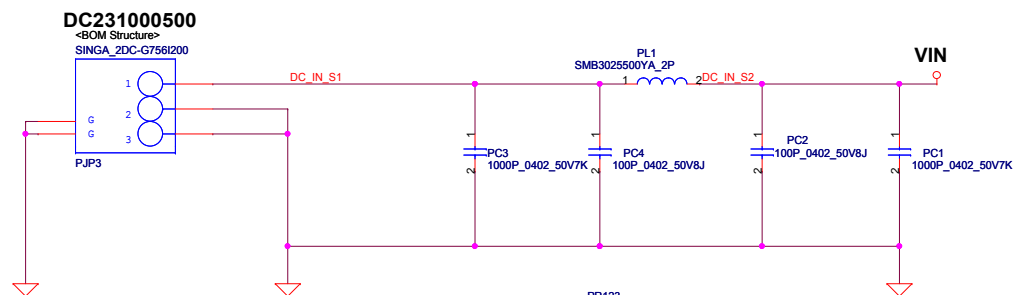
D1 D2 D3 USE PANJIT PJM826V8
SCA00000I00
6.8V



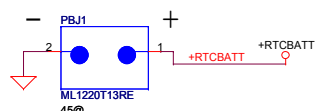
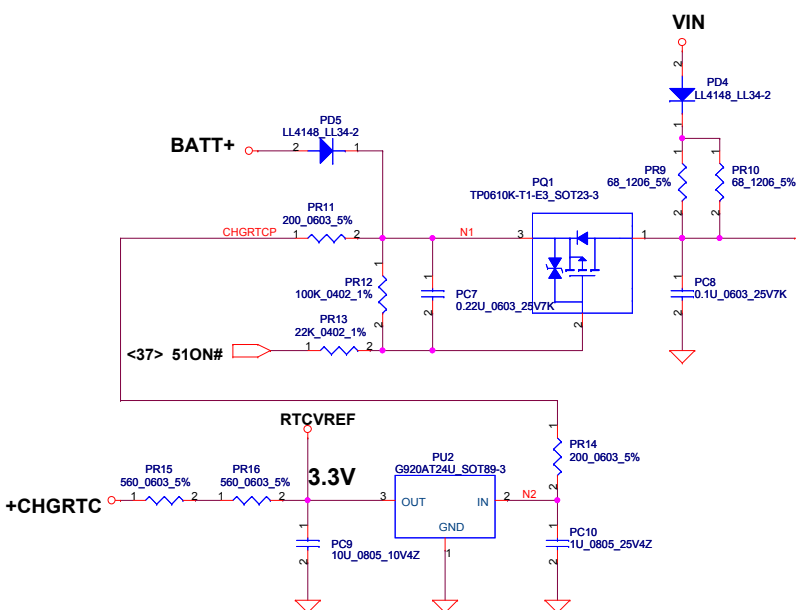
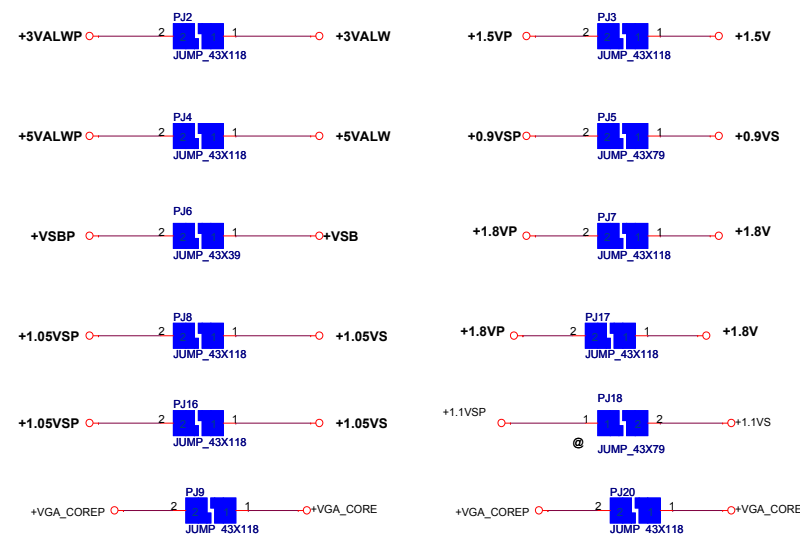
D4 USE
PJSOT24C 3P C/A SOT-23
SCA00000E00
24V



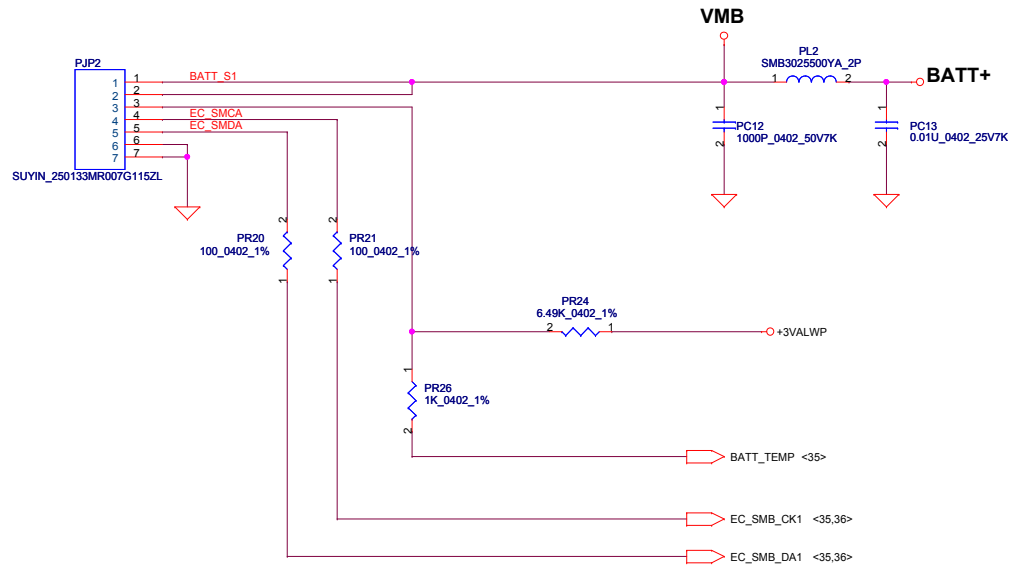
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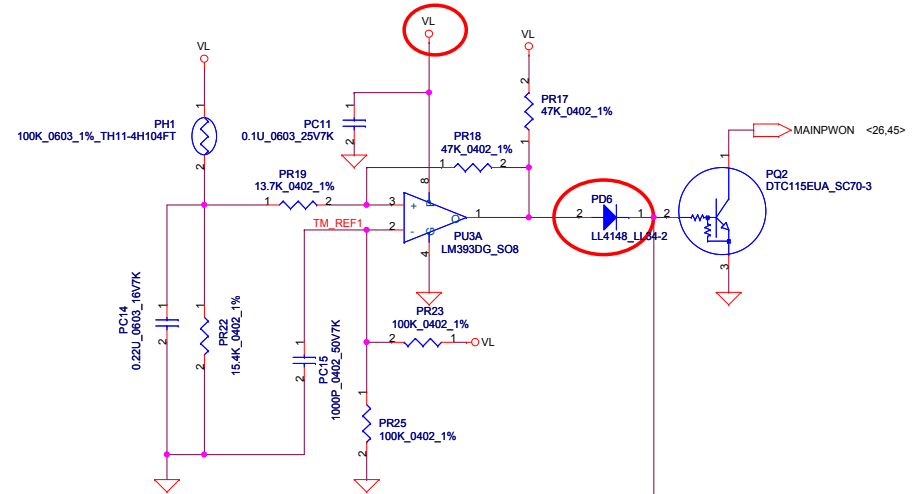
Vin Detector				
	Min.	Typ	Max.	
H-->L	16.976V	17.525V	17.728V	
L-->H	17.430V	17.901V	18.384V	



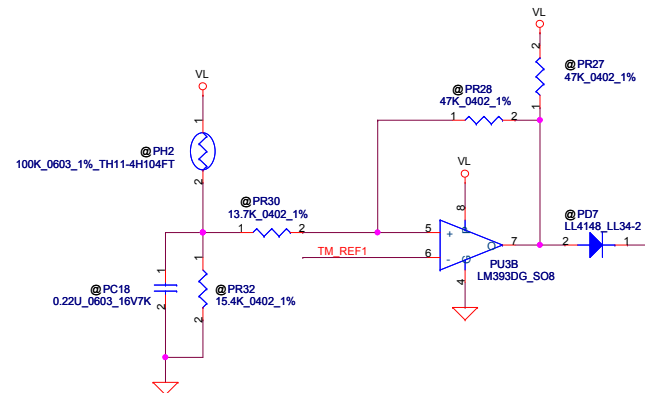
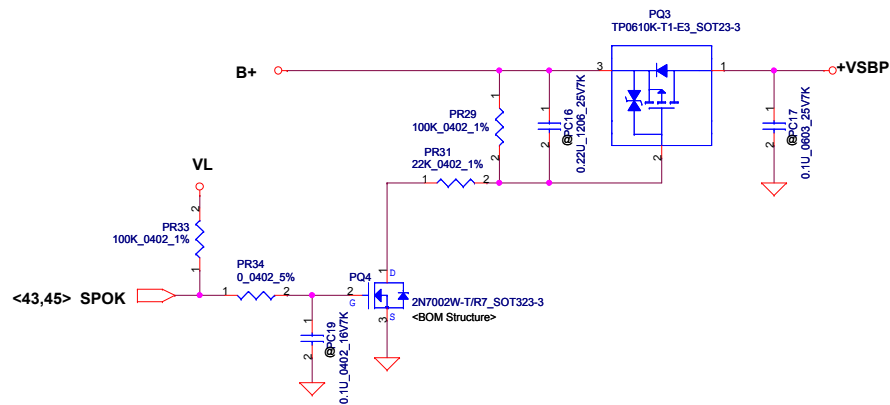
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title	
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Size	Document Number	Customer	KAL90KALH0	Rev	0.2
Date:	Tuesday, December 09, 2008	Sheet	43	of	52



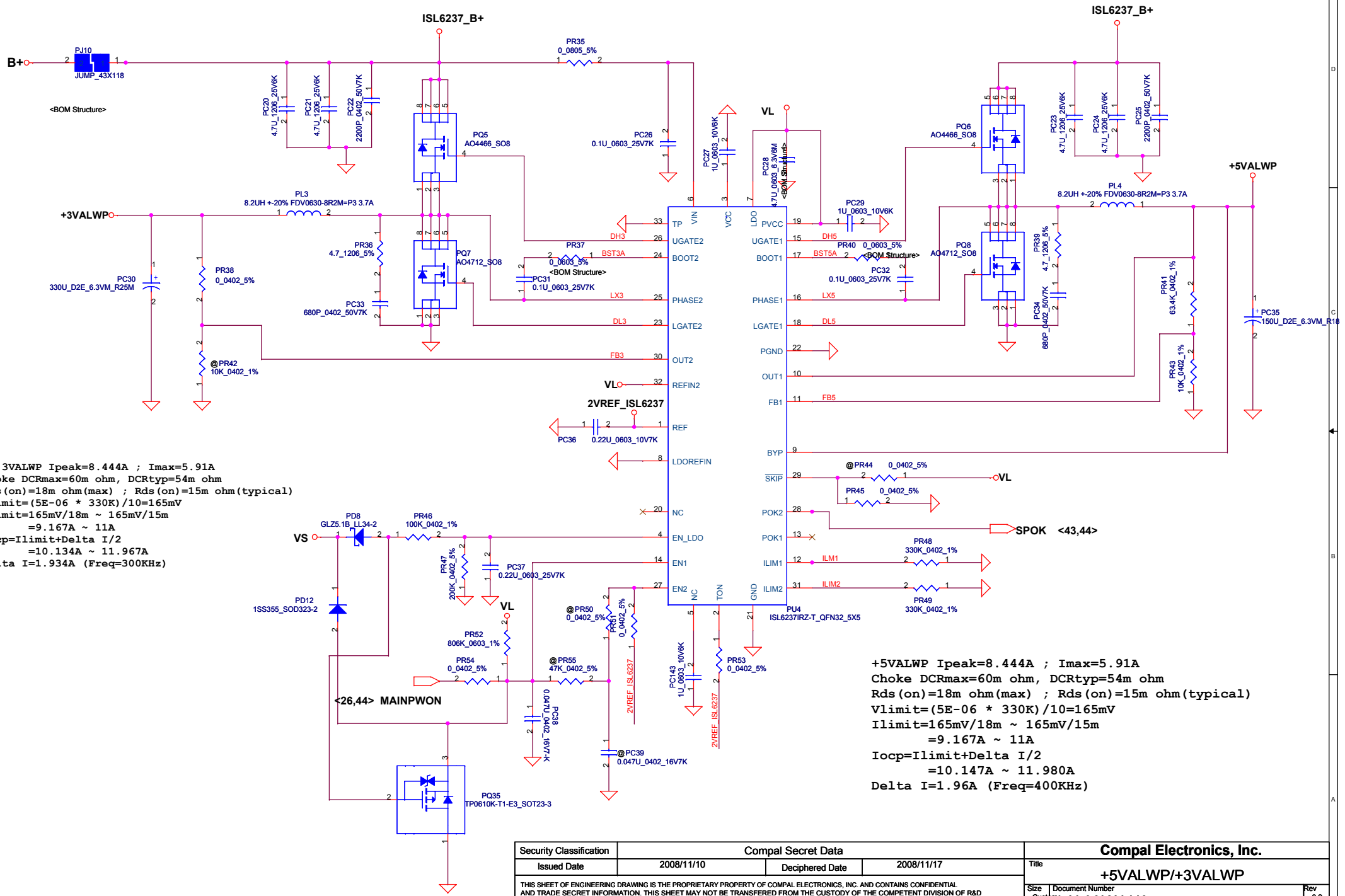
PH1 under CPU botten side :
CPU thermal protection at 96 degree C
Recovery at 60 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 47 degree C



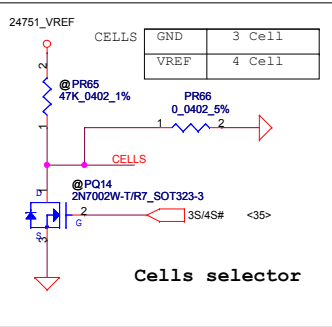
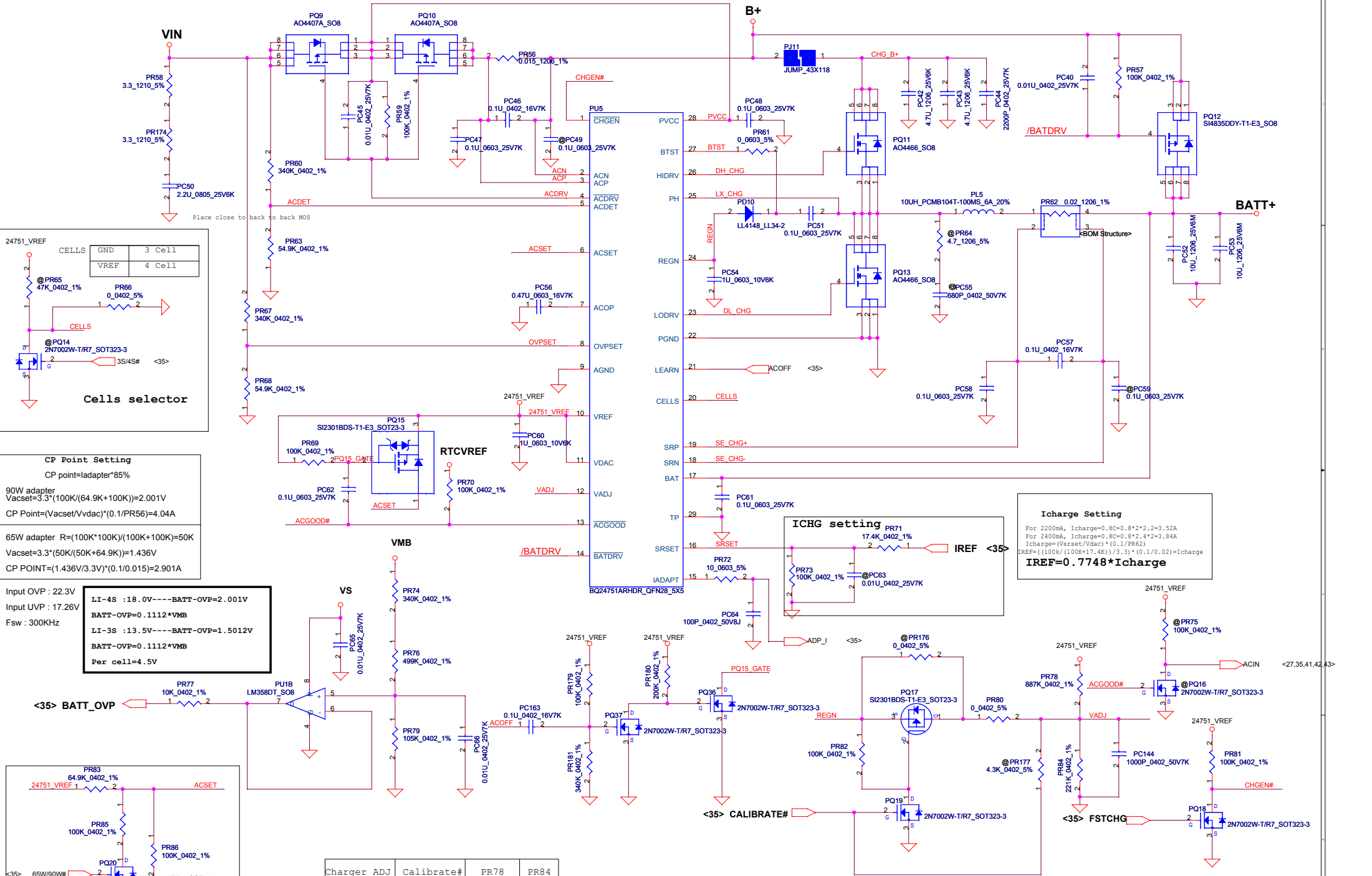
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title	
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Size	Document Number	Rev		Date	
Custom	KAL90KALH0	0.2		Thursday, November 20, 2008	
Sheet		44		of 52	



+3.3VALWP Ipeak=8.444A ; Imax=5.91A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.134A ~ 11.967A
Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.147A ~ 11.980A
Delta I=1.96A (Freq=400KHz)

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				Custom	KAL90KALH0
				Date	Thursday, November 20, 2008
				Sheet	45 of 52
				Rev	0.2



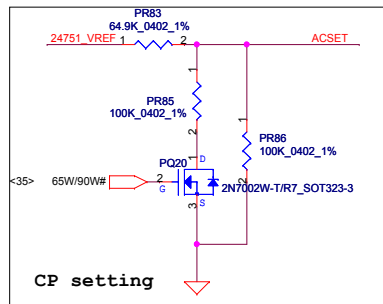
CP Point Setting
CP point=lapter*85%

90W adapter
Vacset=3.3*(100K/(64.9K+100K))=2.001V
CP Point=(Vacset/Vvdac)*(0.1/PR56)=4.04A

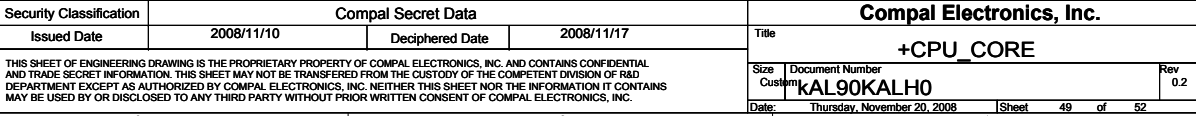
65W adapter R=(100K*100K)/(100K+100K)=50K
Vacset=3.3*(50K/(50K+64.9K))=1.436V
CP POINT=(1.436V/3.3V)*(0.1/0.015)=2.901A

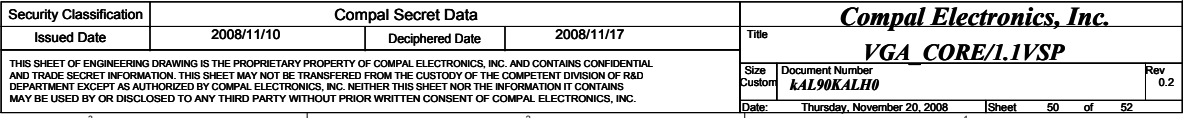
Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz

LI-4S : 18.0V----BATT-OVP=2.001V
BATT-OVP=0.1112*VMB
LI-3S : 13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=4.5V



Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V	H	@	@





Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	cpu load line fail	Measure cpu load line can't fit spec	0.2	49	change the resistance value of pr173.from 4.42k to 3.83k	2008/08/08	DVT
2	Change resistance size	EMI request	0.2	49	Change pc116 and pc117 size from 0402 to 0603	2008/08/08	DVT
3	Change p-mos part number	Vender change EOL	0.2	46	PQ12 part number from 4835bdy to 483500y	2008/08/08	DVT
4	Change device size	device too large can't fit layout space	0.2	44-50	PQ4, PQ14, PQ16, PQ18, PQ19, PQ20, PQ27, PQ36, PQ37, PQ41, PQ42 change to sot323-3	2008/08/12	DVT
5	Change resistance value	1.05V tranient fail	0.2	47	PR94 from 60.4k to 59k	2008/08/12	DVT
6	change resistance	for hdmi	0.2	45	pr41 change from 61.3k to 63.4k	2008/08/14	DVT

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		2008/11/17		Title	
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A --> C Change List

1120-----
Page 35,Chang
R1745,R1746 to 4.7K SD028470180

1120-----
Page 36,Add
R106,R109,R1846,R1847 to 0R

1120-----
Page 37,Add
R1845 to 10K

1120-----
Page 37,Add
R49 to 1K, JP24 to ACES_88266_02001

1217-----
Page 42,Delete
R1814,R1815,R1816,R1817,R1818,R1819

0106-----
Page 39, Delete D63 for Microsoft certification;
Page 36, Delelte R1773, modify value or R1774, R1775 for LED color.

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