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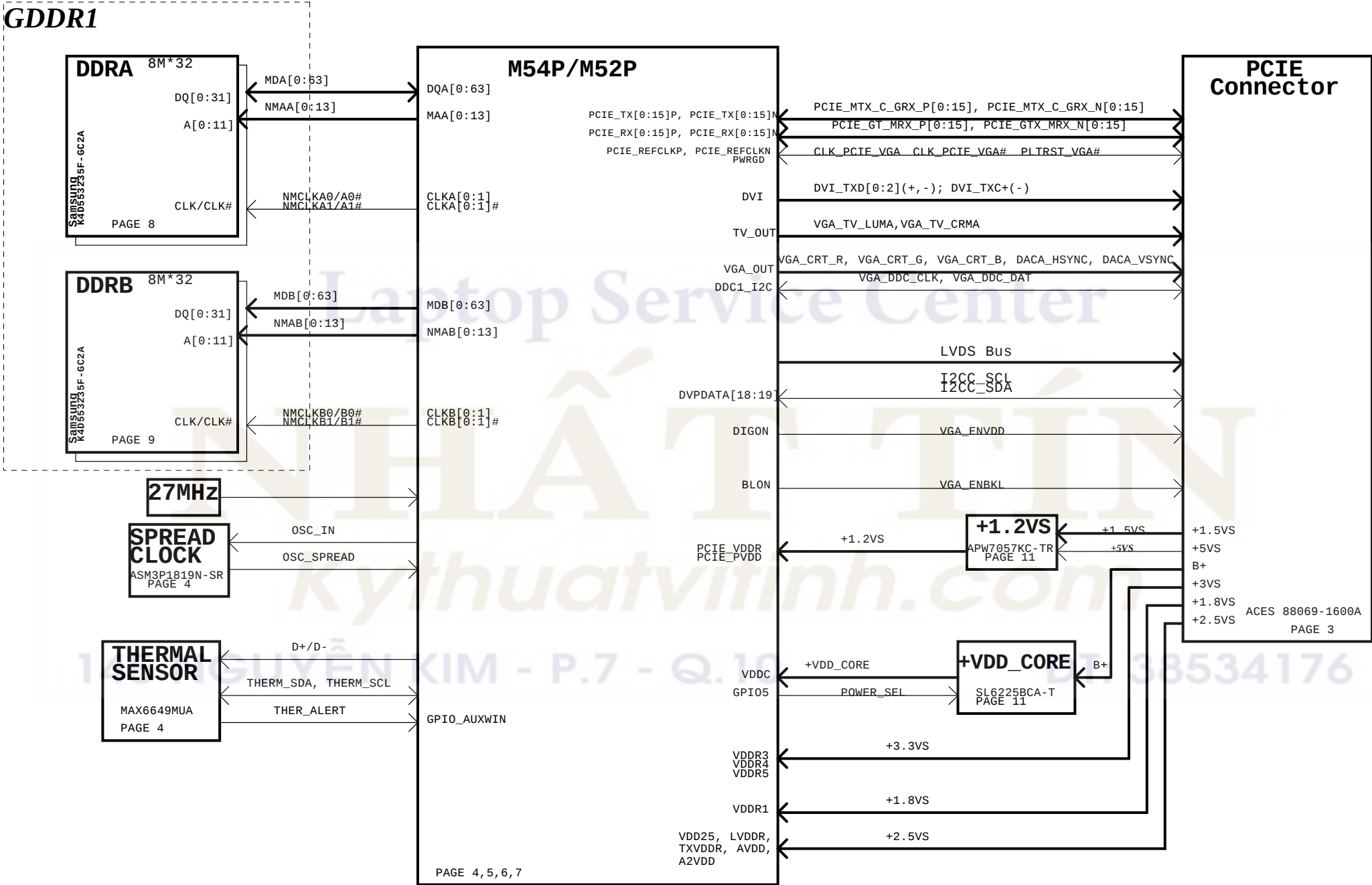
Mini (EFL50) ATI VGA/B M52-P

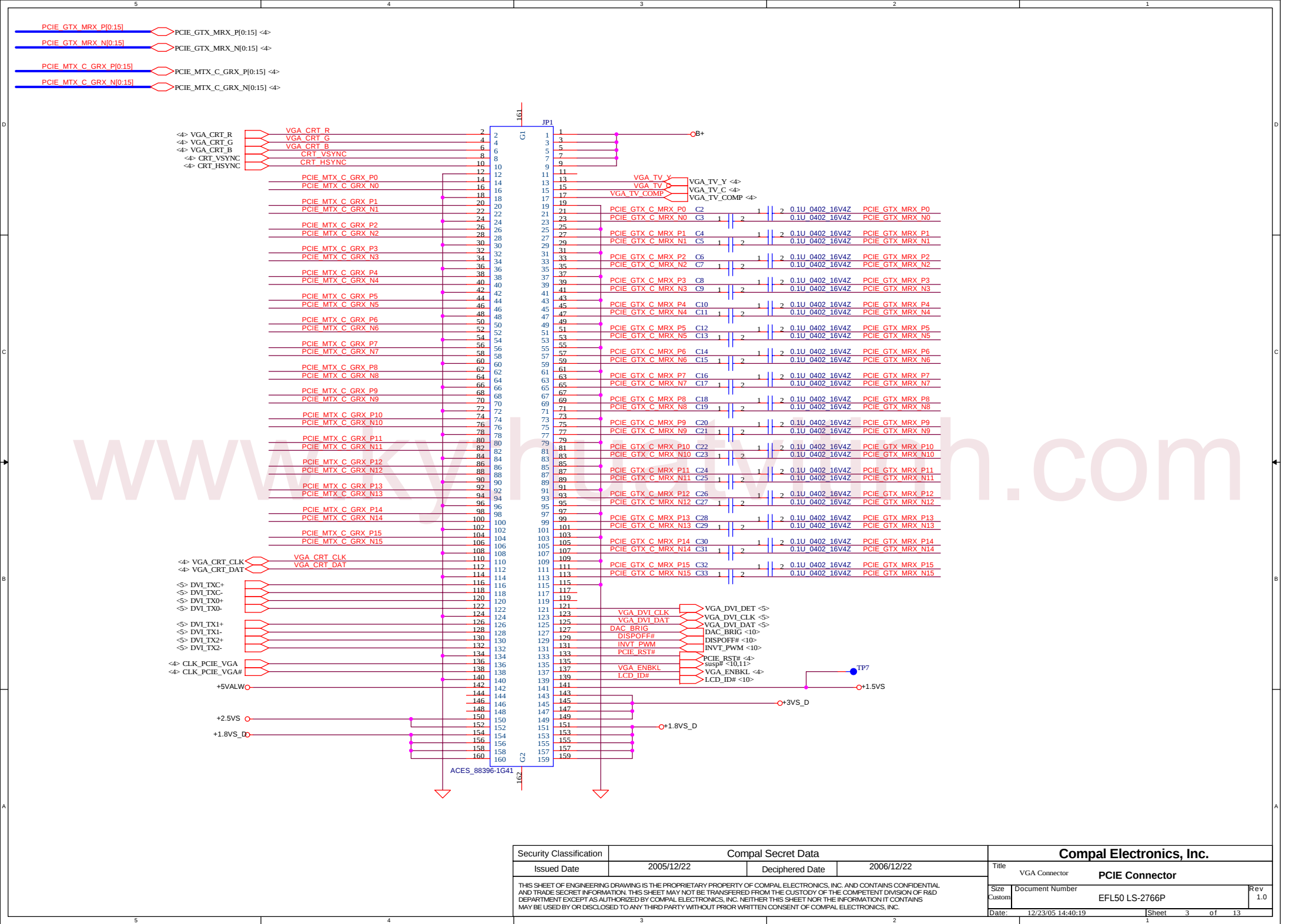
Revision 1.0

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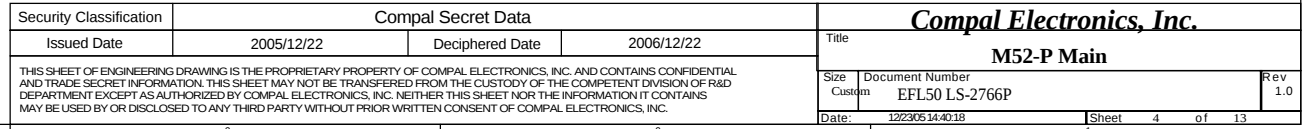
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Issued Date	2005/12/22	Deciphered Date	2006/12/22	Title Cover Sheet	
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M54P/M52P BLOCK DIAGRAM

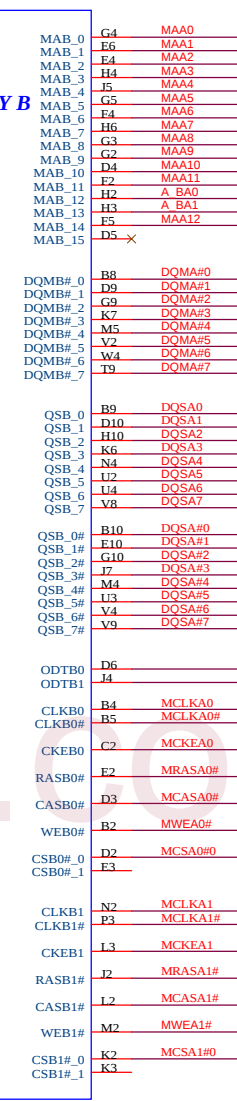
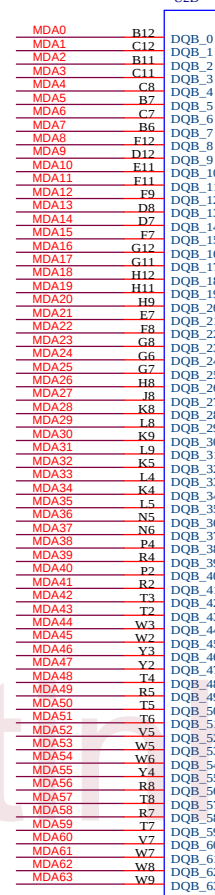
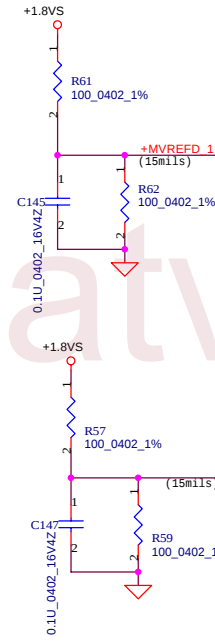
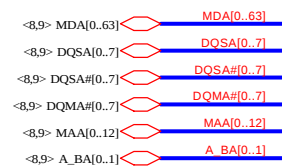
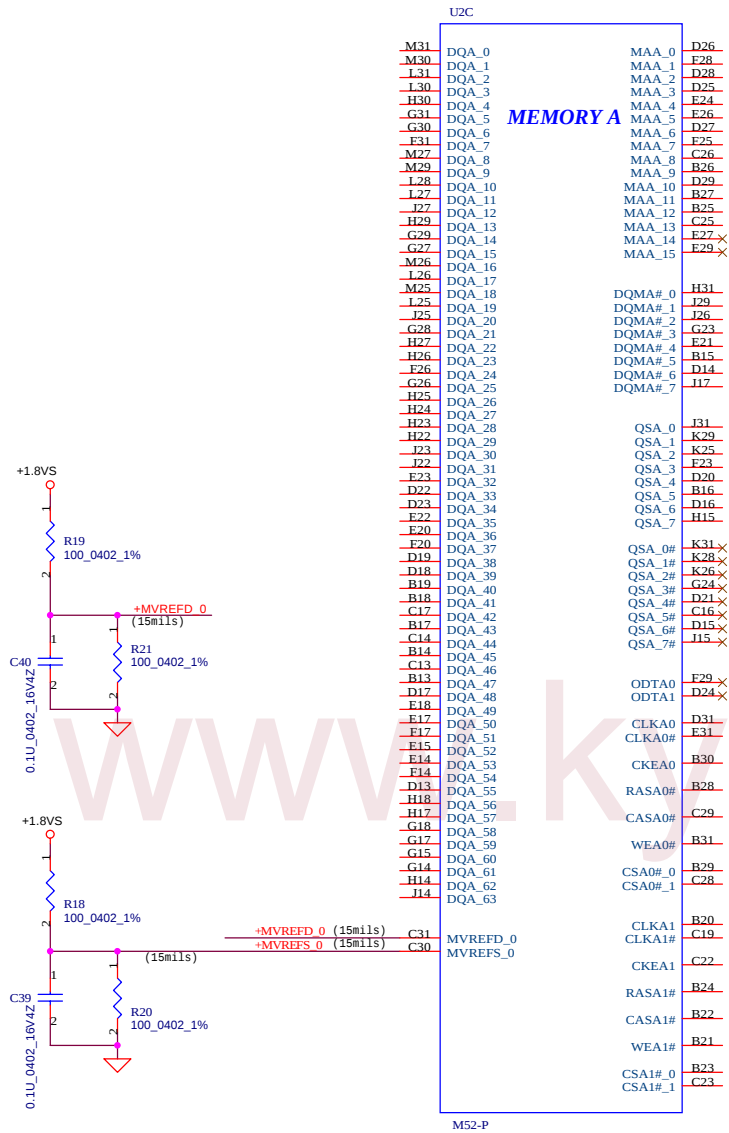




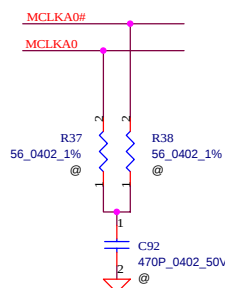
PCI-Express Data Bus Lane Reversal and Polarity Inversion



GDDR2

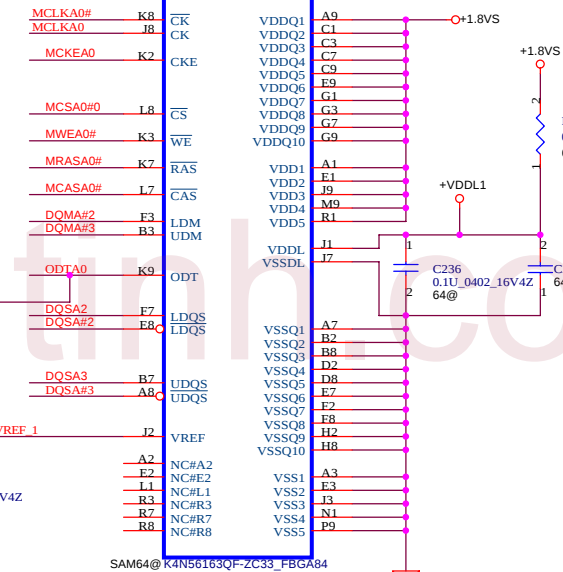
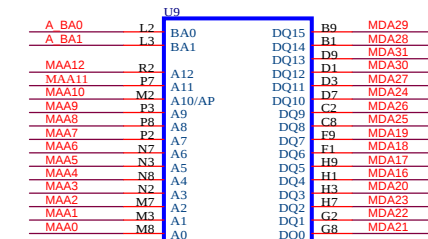
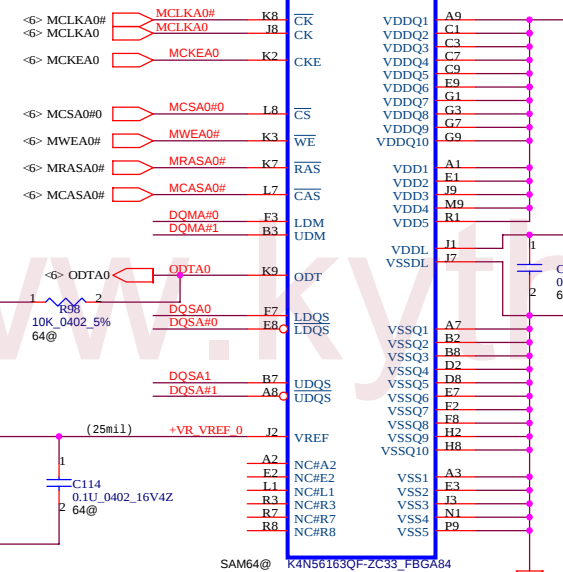
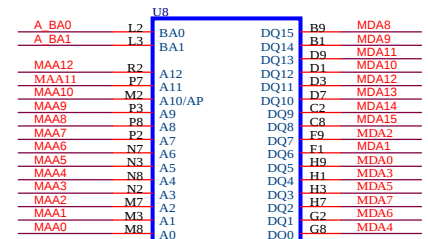


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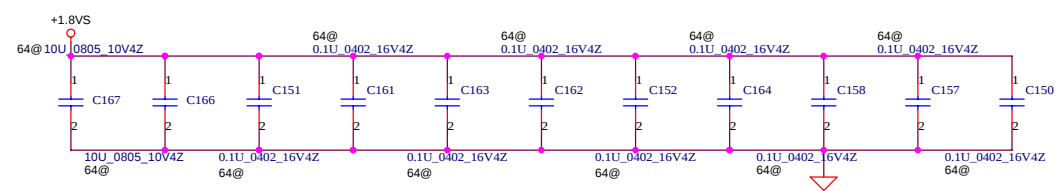
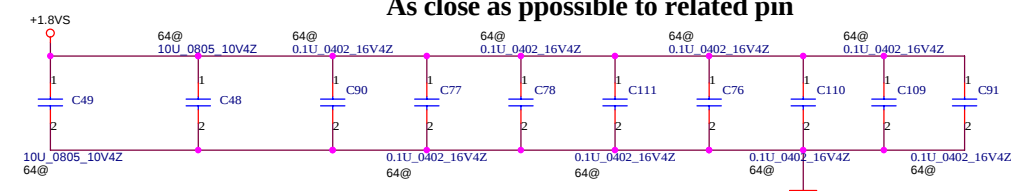


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<6,9> DQSA[0..7] DQSA[0..7]
<6,9> DQSA# [0..7] DQSA# [0..7]
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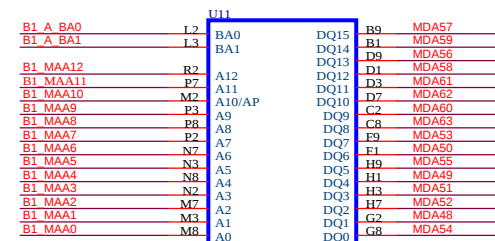
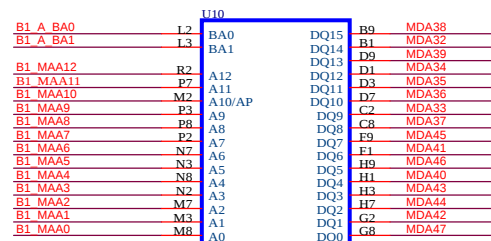
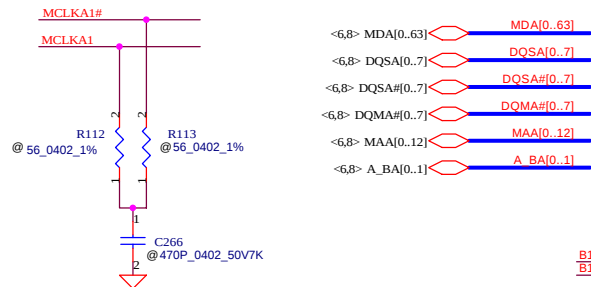
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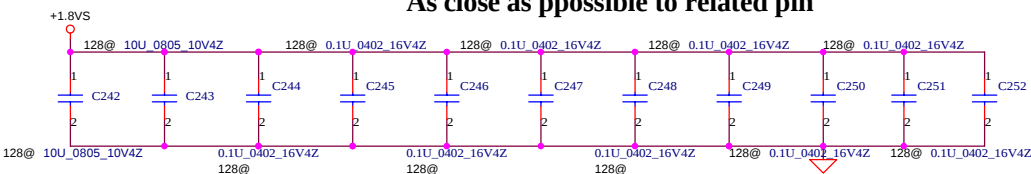
As close as ppossible to related pin



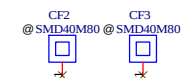
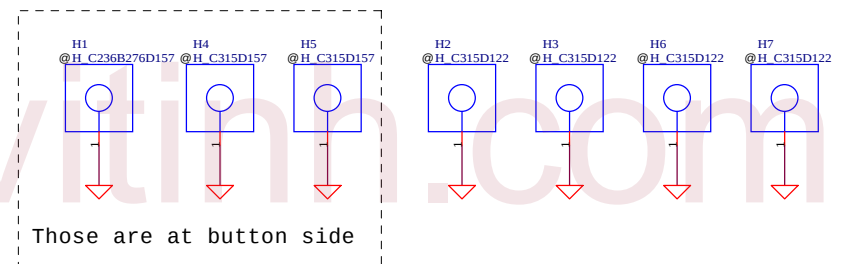
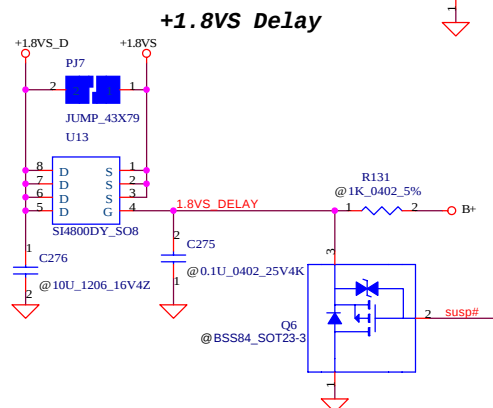
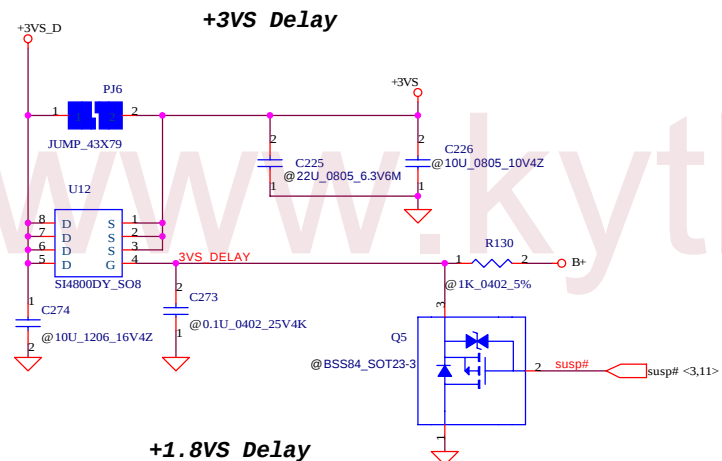
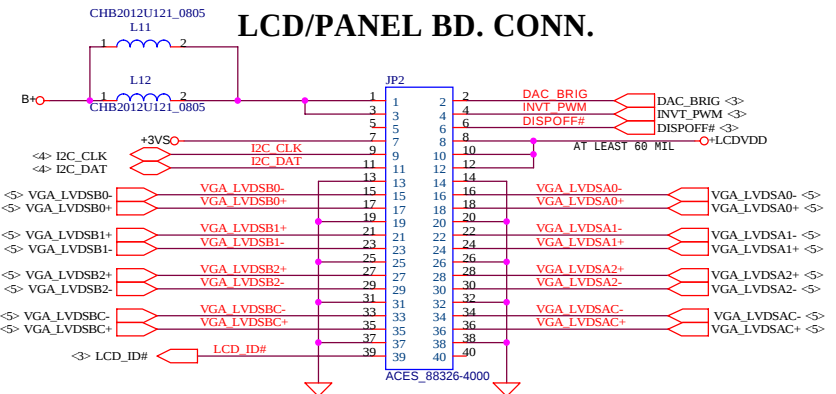
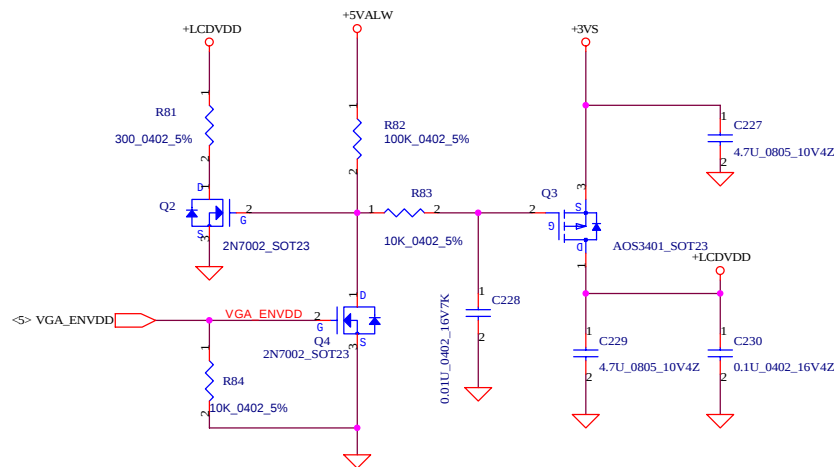
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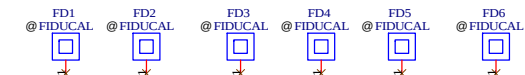
Default VRAM chip is SAM: SA00000YC00.



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				Size	Document Number
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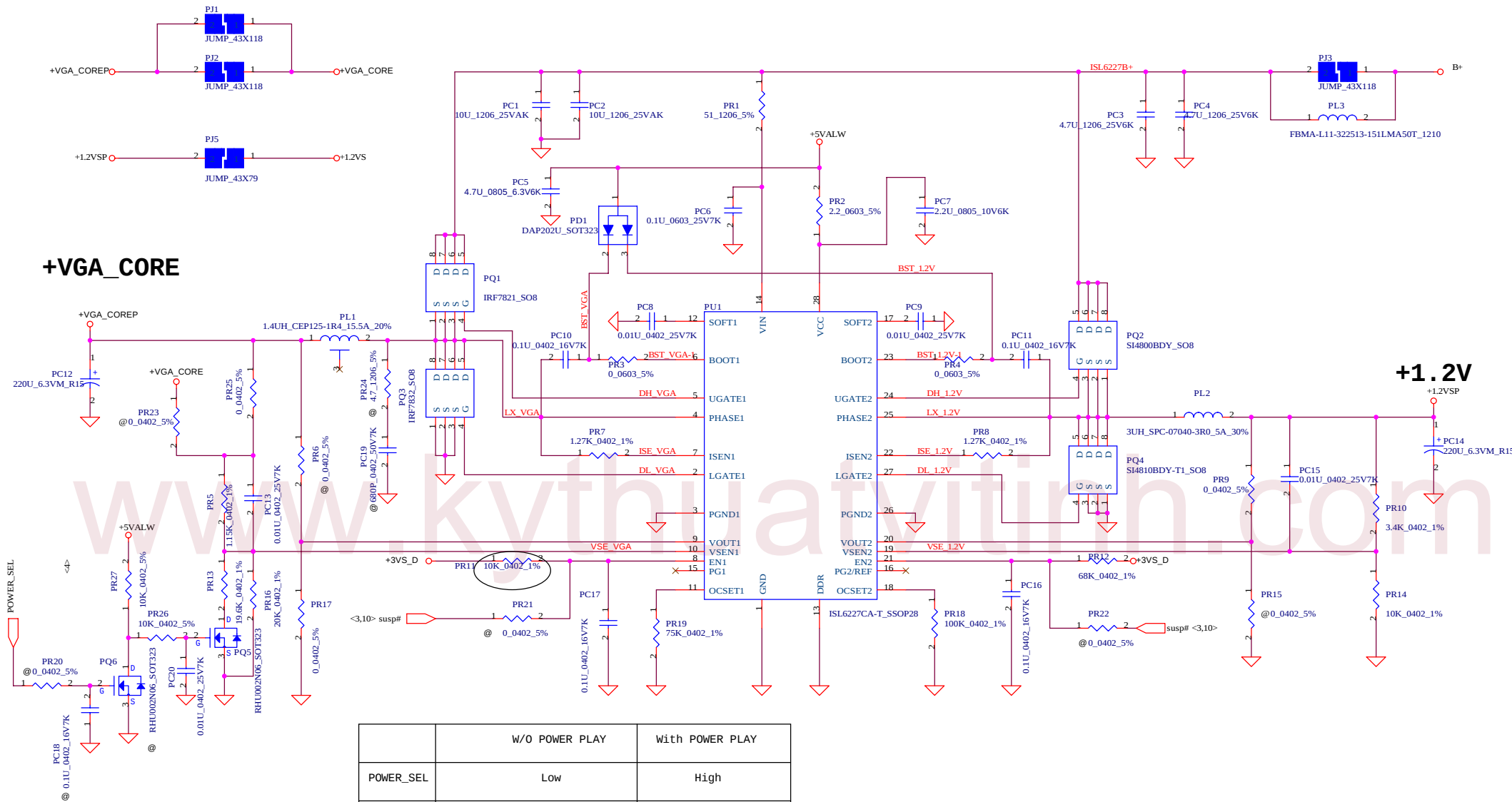


For IC FIXED



For Board FIXED

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Version change list (P.I.R. List)

===== 2005/12 R0.2 =====

- 01. Reserve +3VS and +1.8VS delay circuit and reserve Jump. == To meet ATI PWR sequence.
Reserve PJ6, PJ7, U12, U13, C273, C274, C275, C276,
Q5, Q6, R130 and R131.
- 02. Change C42, C45, C46, C47 and C51, from 0.1U to 1U. == For 3D hang issue.
- 03. Change C101, from 0.1U to 1U. == For 3D hang issue.
- 04. Add C44 as 330U == For 3D hang issue.
- 05. Delete R63, 10K_0402_5% == PCIE TX power saving.

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ZZZ
DA800005F10
--PCB ZKD LS-2766P
REV1 VGA/B

DA800005F10

U9
SA00000JW00
--S IC D2 16M16/600
HY5PS561621AFP-33
FBGA

HYN64@ SA00000JW00

U9
SA00000JW00
--S IC D2 16M16/600
HY5PS561621AFP-33
FBGA

HYN64@ SA00000JW00

U10
SA00000JW00
--S IC D2 16M16/600
HY5PS561621AFP-33
FBGA

HYN128@ SA00000JW00

U11
SA00000JW00
--S IC D2 16M16/600
HY5PS561621AFP-33
FBGA

HYN128@ SA00000JW00

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				Date: 12230514:40:19	Rev 1.0
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