

Compal Confidential

NEW71/91 M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M NV N11P-GV2H

2009-12-23

REV : 0 . 1

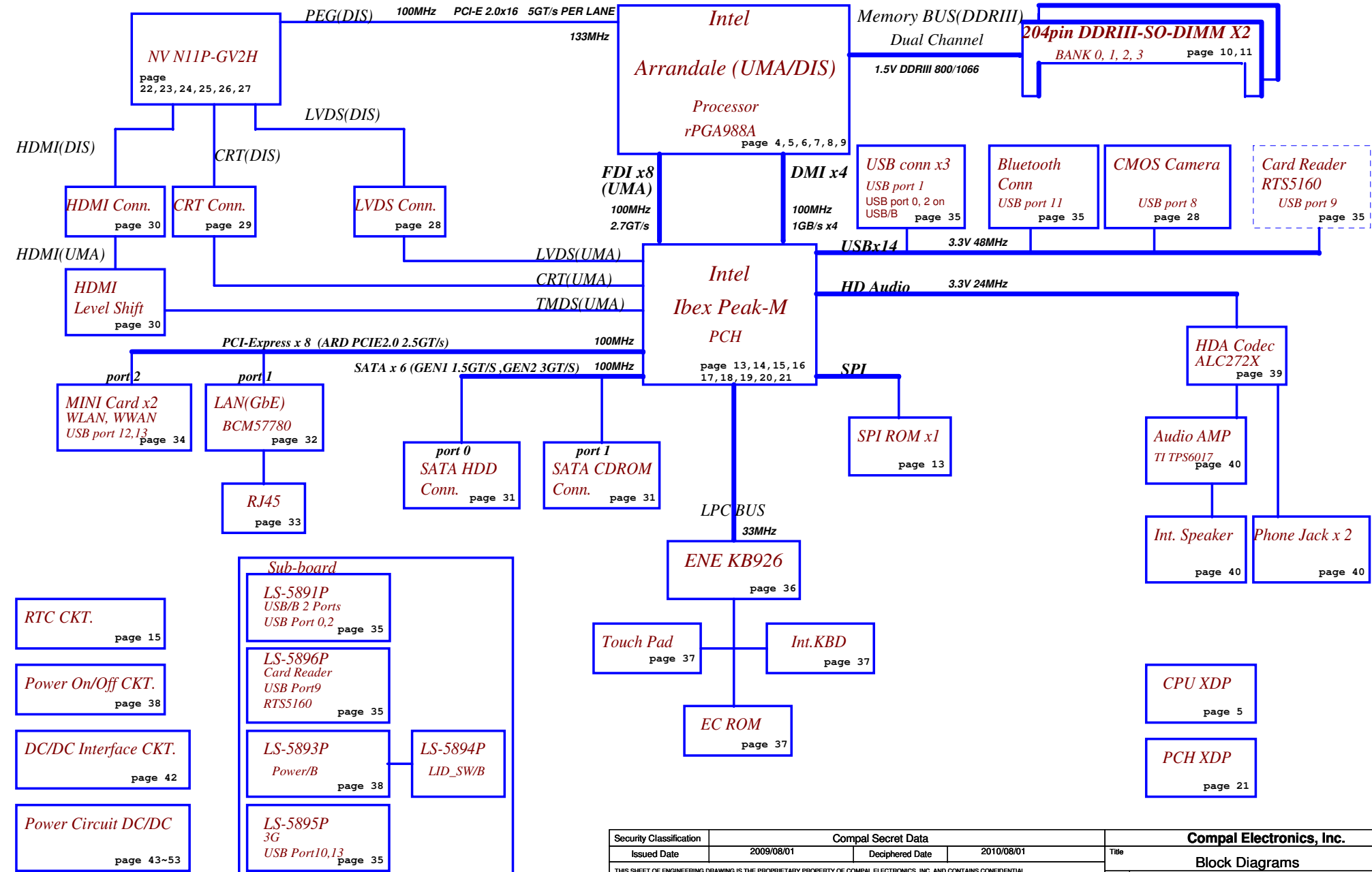
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				Size	Document Number
				Custom	NEW71/91 M/B LA-5893P Schematic
				Date	Wednesday, December 23, 2009
				Sheet	1 of 56

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Model Name : NEW71/91
File Name : LA5893P

Fan Control
page 41

Clock Generator
IDT: 9LVS3199AKLFT
Realtek: RTM890N-631-VB-GRT
133/120/100/96/14.318MHZ to PCH
page 12



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Arrandale GPU (only for arrandaleCPU)	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for ARD CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3V	+3VALW to +3V power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V	+5VALW to +5V switched power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BOM Config	
NEW71 SKU DISCTETE ONLY	BT@,3G@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,XDP@
NEW91 SKU DISCTETE ONLY	BT@,3G@,DIS@,DIS ONLY@,NonSG@,91@,X7621@,XDP@

VRAM BOM Config
X7621@: X76198BOL21 ALT. GROUP PARTS 1G SAM
X7622@ X76198BOL22 ALT. GROUP PARTS 1G HYN

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

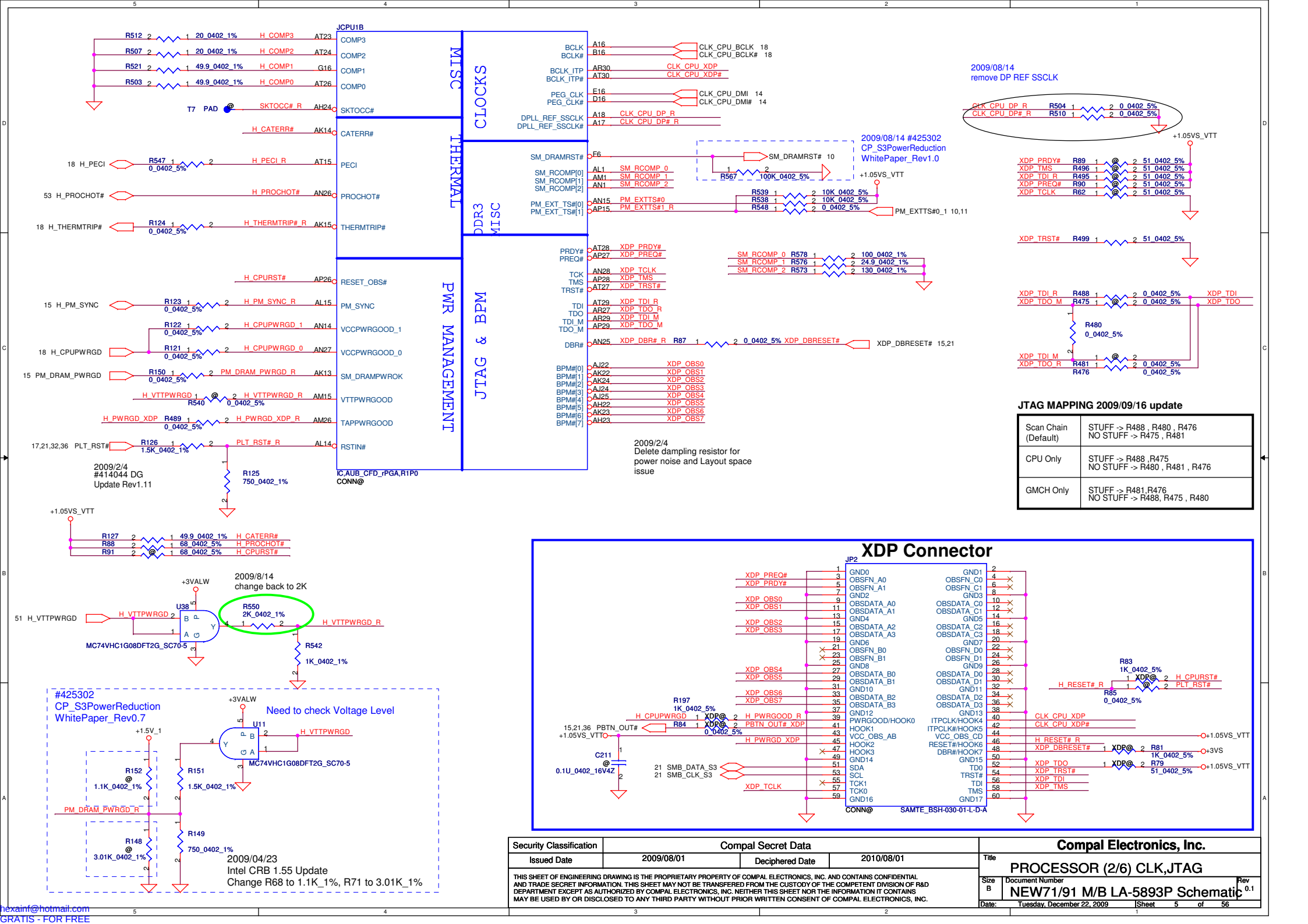
BTO Item	BOM Structure
UMA	UMA@
UMA Only	UMA ONLY@
Discrete	DIS@
Discrete Only	DIS ONLY@
VRAM	X76@
Switchable	SG@
Connector	CONN@
3G	3G@
Blue Tooth	BT@
Unpop	@
XDP	XDP@
NonSG	NonSG@
NEW71	71@
NEW91	91@

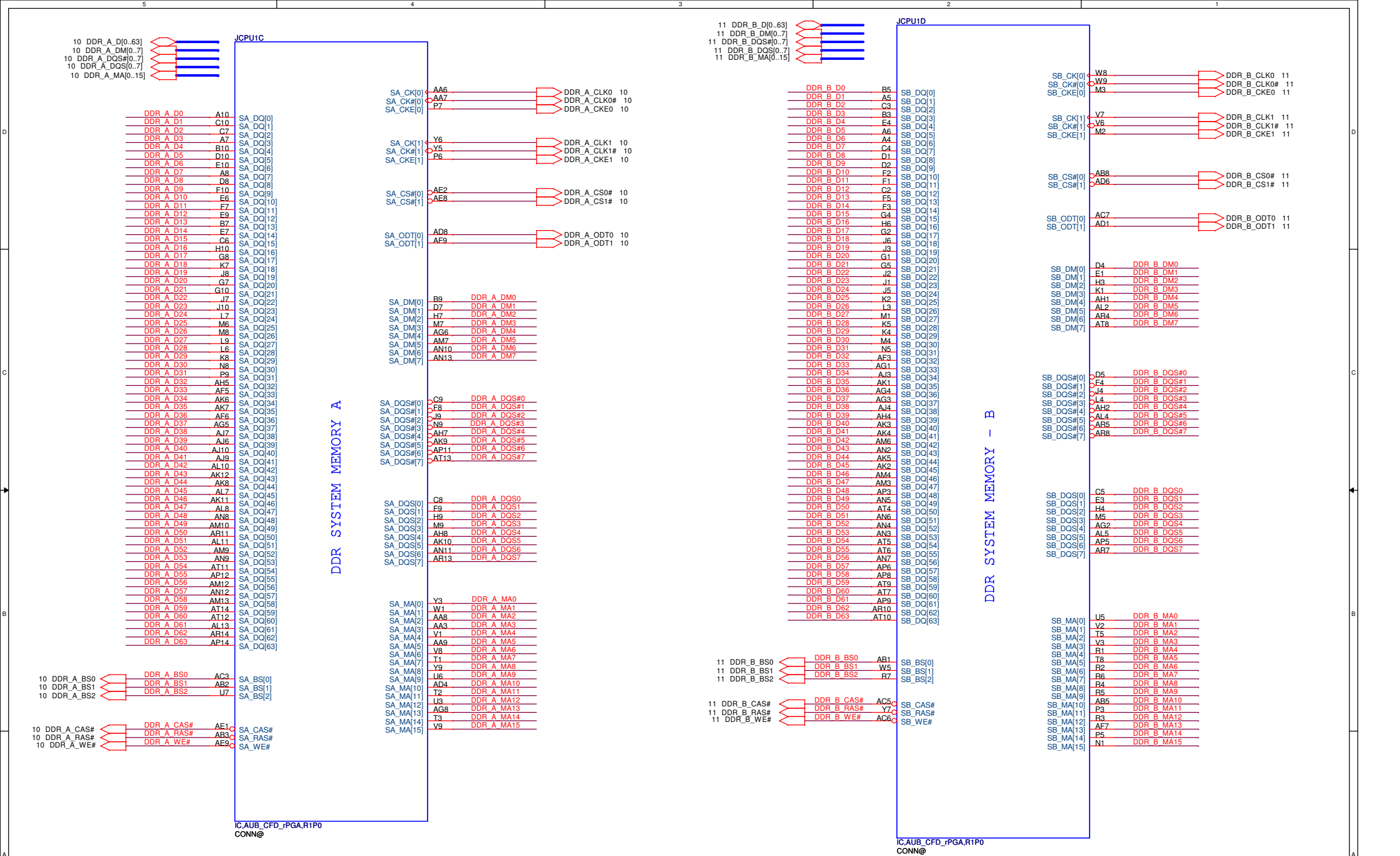
VRAM P/N :
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)

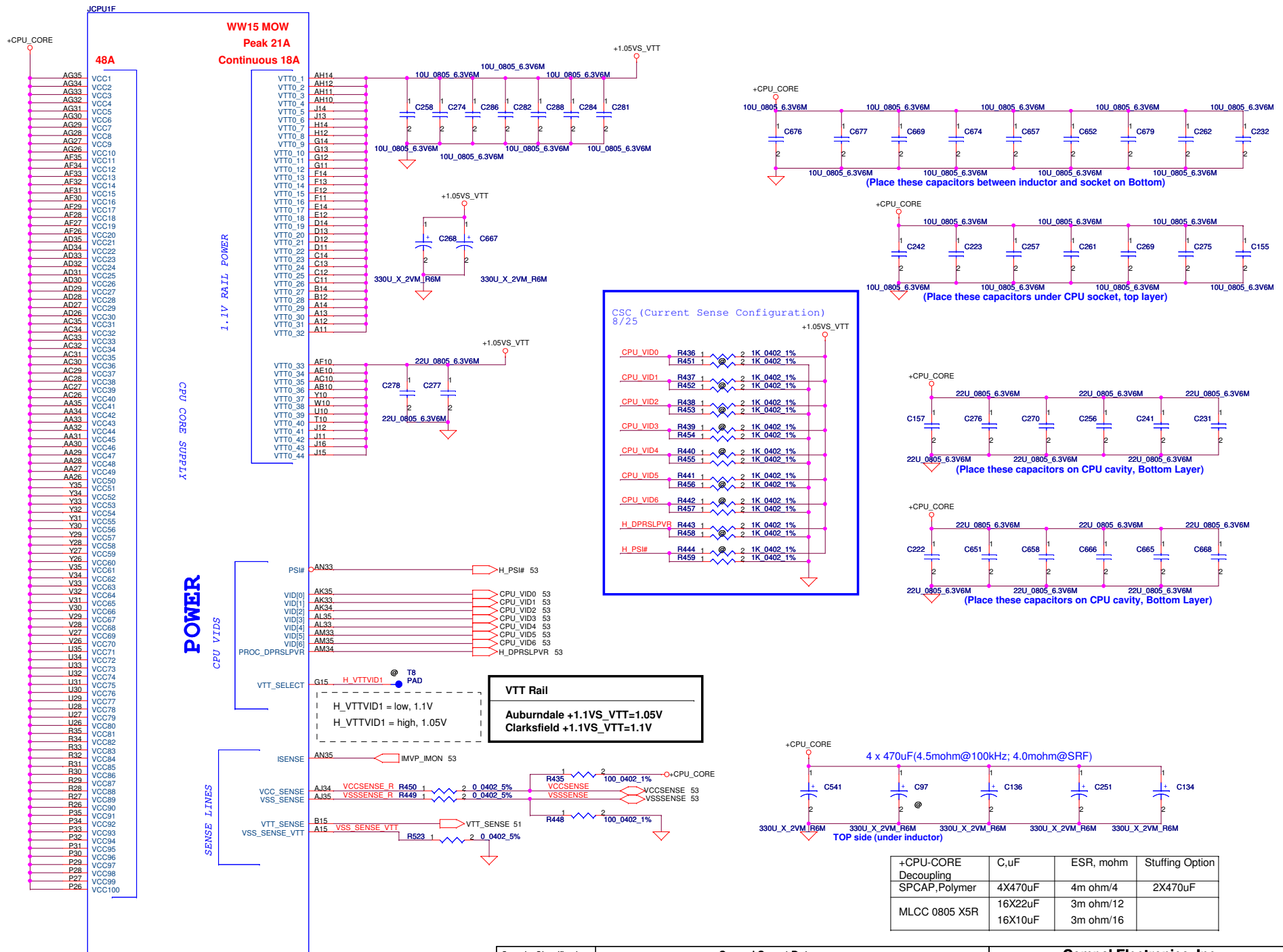
USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB/B (Right Side)
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Camera
		9	Card Reader
	UHCI5	10	SIM Card
		11	Blue Tooth
	UHCI6	12	Mini Card(WLAN)
		13	Mini Card(GPS)

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Size B	Document Number			Rev	
	NEW71/91 M/B LA-5893P Schematic			0.1	
Date:	Tuesday, December 22, 2009	Sheet	3	of 56	

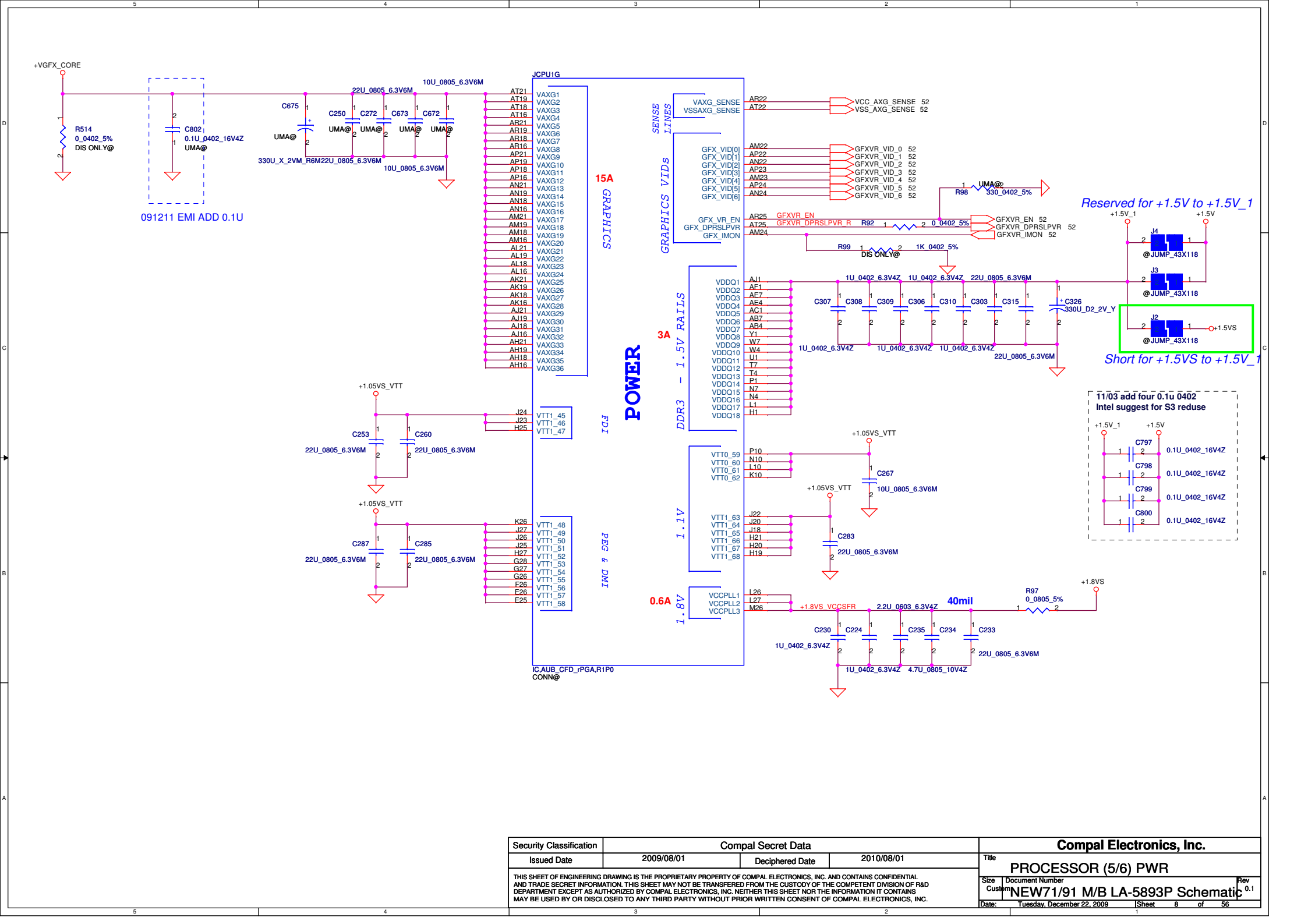


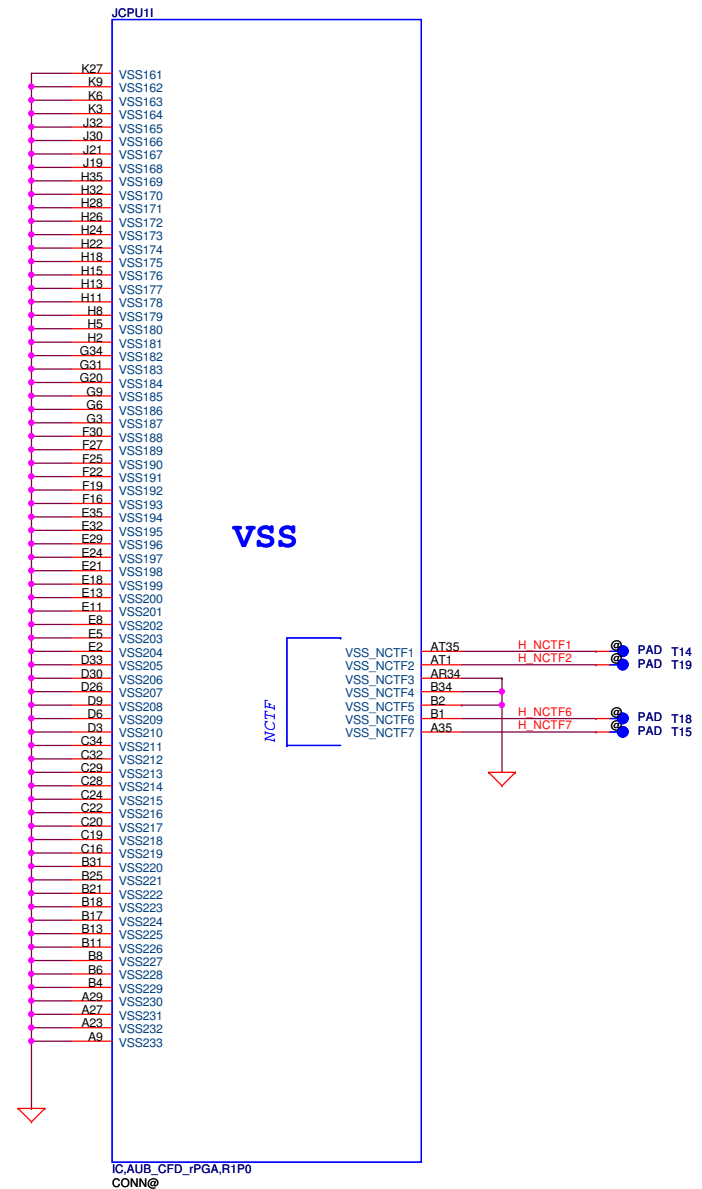
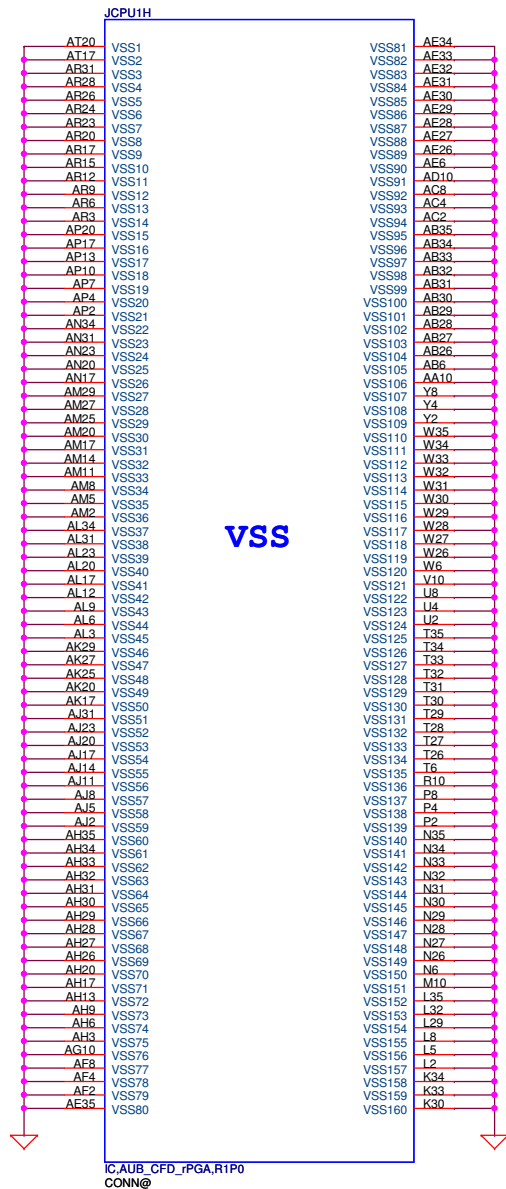




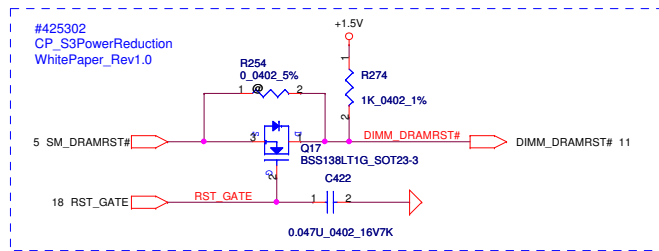
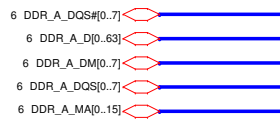
IC_AUB_CFD_PGA_R1P0
CONN@

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Size		Document Number		Rev	
Customer		NEW71/91 M/B LA-5893P Schematic		0.1	
Date		Tuesday, December 22, 2009		1 Sheet 7 of 56	



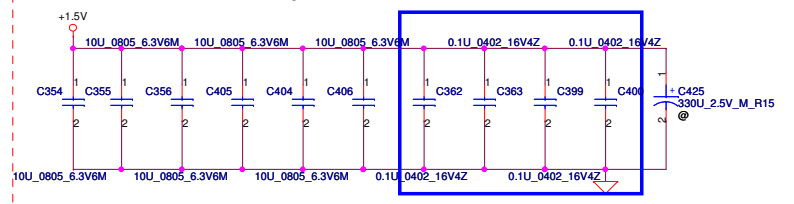


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						Customer		NEW71/91 M/B LA-5893P Schematic		0.1	
						Date:		Friday, December 18, 2009		Sheet 9 of 56	

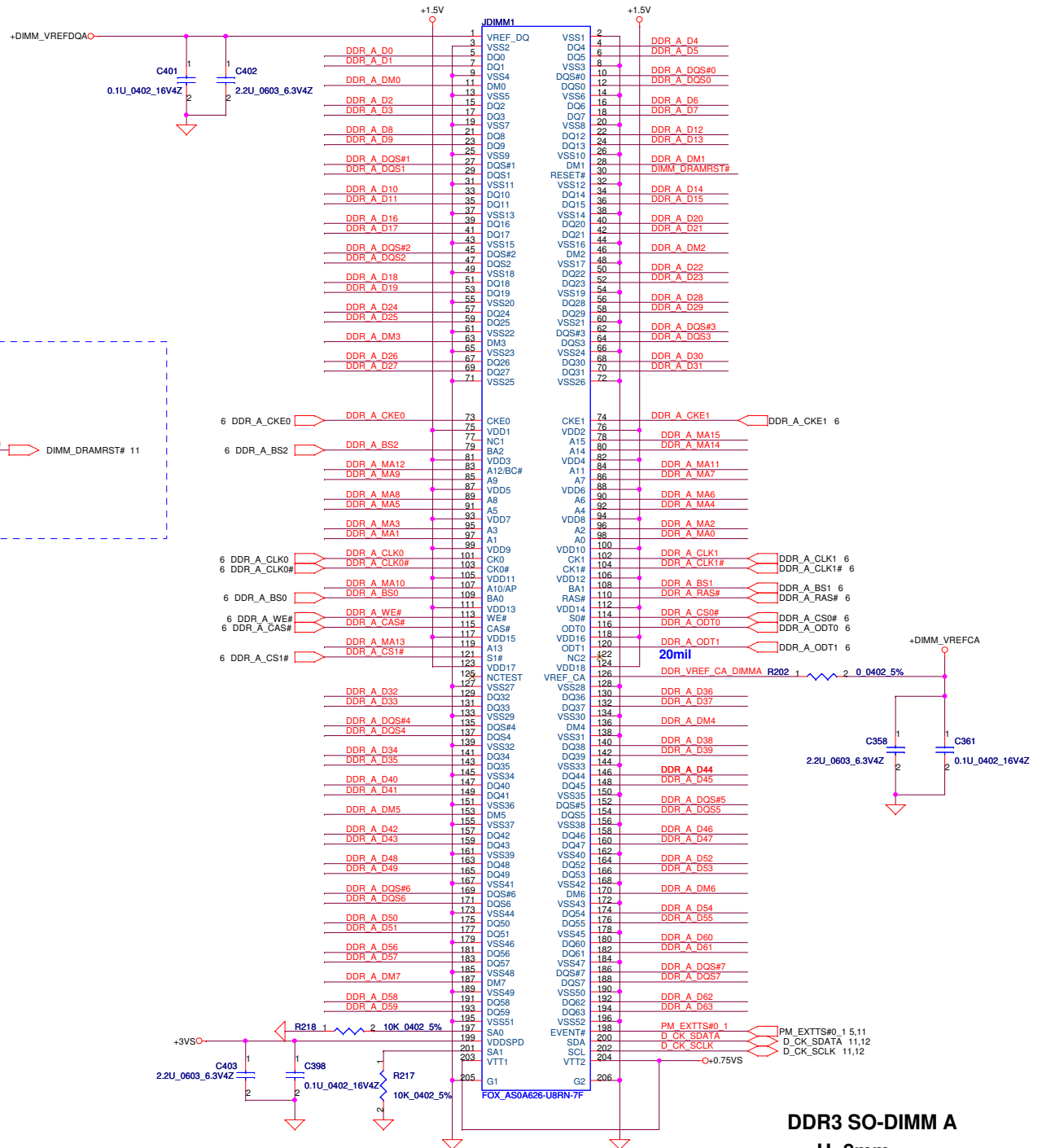
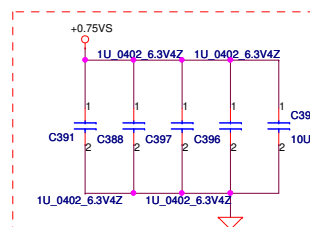


Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



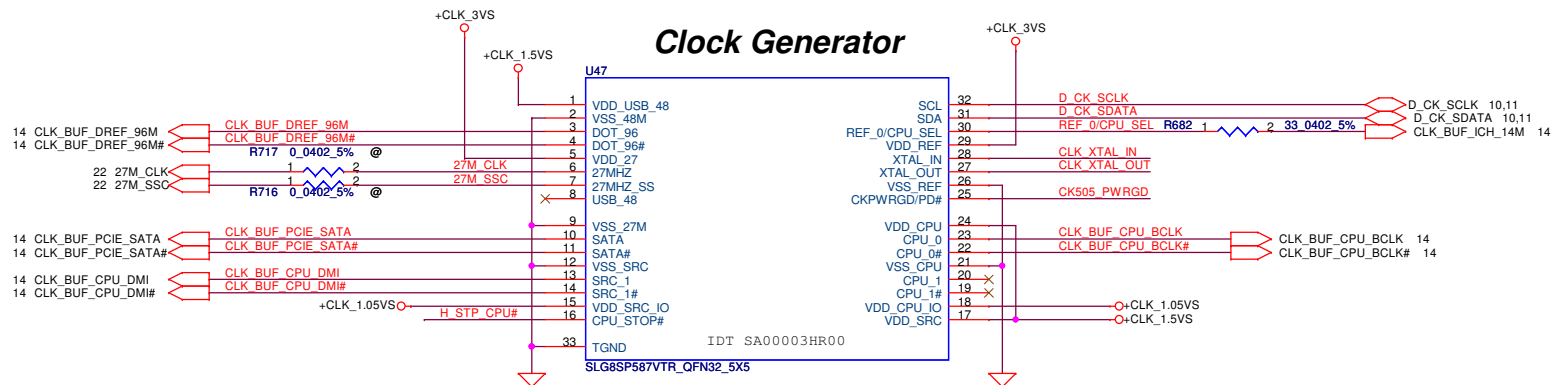
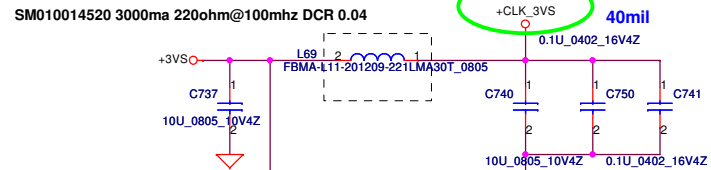
Layout Note:
Place near JDIMM1.203 & JDIMM1.204



DDR3 SO-DIMM A
H=8mm

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				Customer	NEW71/91 M/B LA-5893P Schematic
				Date:	Tuesday, December 22, 2009
				Sheet	10 of 56



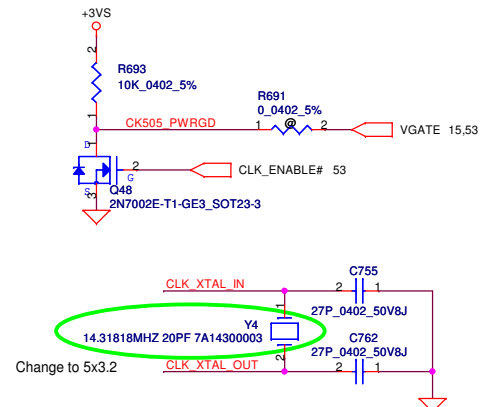
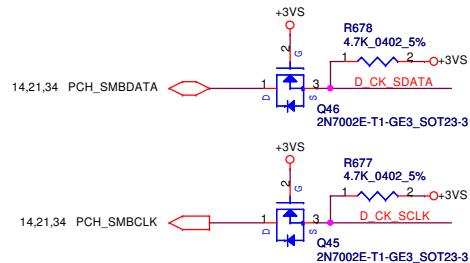


Silego Have Internal Pull-Up

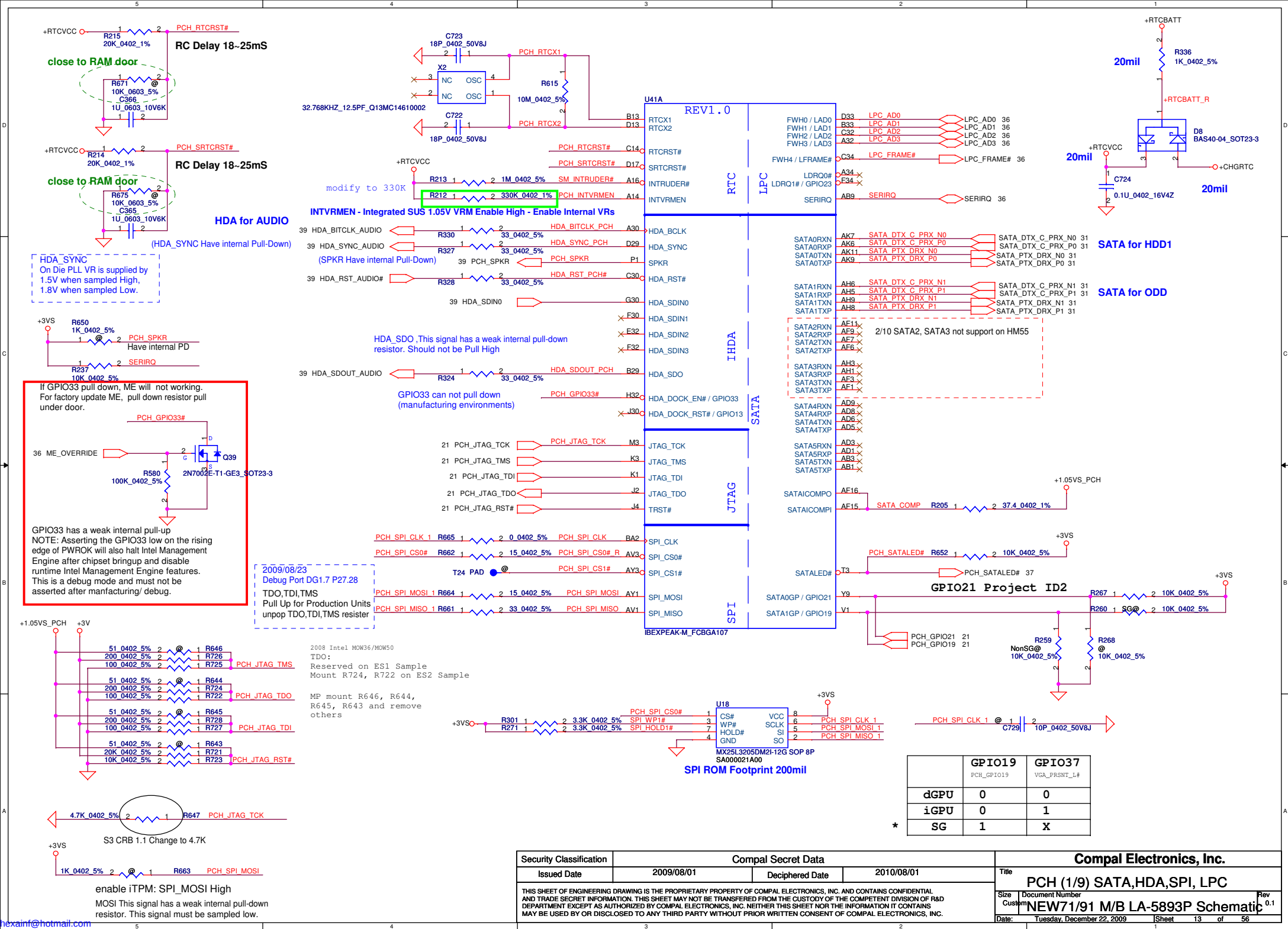
The diagram shows a +3VS supply connected to a resistor network. The network consists of a 10K resistor in series with a parallel combination of a 0402 resistor and a 5% resistor. The output is labeled H STP CPU#.

R683 1 2 10K 0402 5% REF 0/CPU SEL

PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz



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				Cust	NEW71/91 M/B LA-5893P Schematic	0.1
				Date:	Tuesday, December 22, 2009	Sheet 12 of 56



For PCIE LAN

For Wireless LAN

For Mini2

For PCIE LAN

For Wireless LAN

Schematic Checklist_Rev1.6

GPIO18 Main (core) power well (+V3.3S) Mixed with PCIECLKRQ1#. If not used, requires 8.2-k to 10-k pull-up to +Vcc_3.3 (+V3.3S)

GPIO25 Resume (Sus) well (+V3.3A) Mixed with PCIECLKRQ3#. If not used, requires 8.2-k to 10-k pull-up to +V3.3A rail.

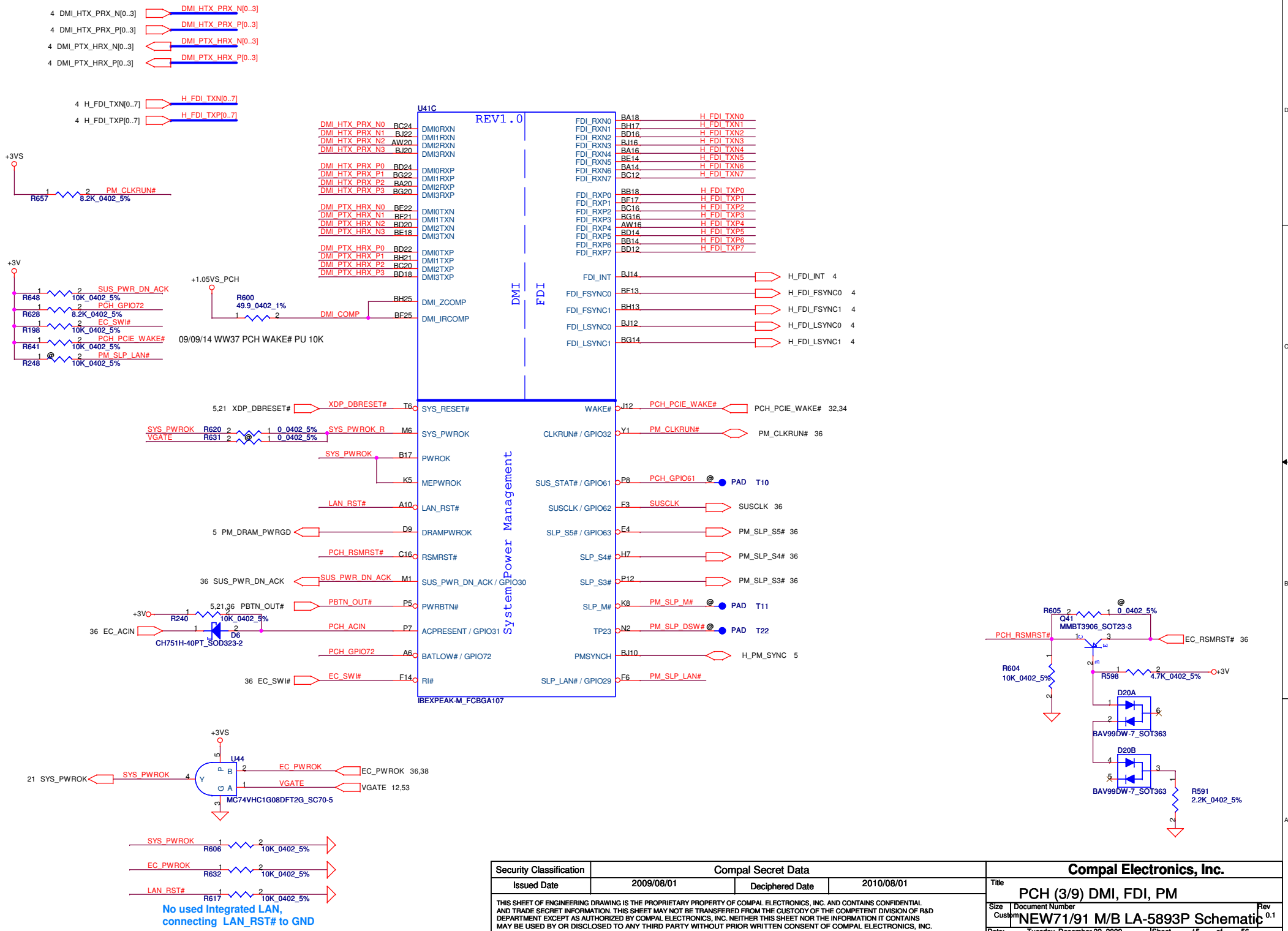
Project Structure			
GPIO21 ID2	GPIO65 ID1	GPIO66 ID0	Structure
0	0	0	NEW70
0	0	1	NEW80
0	1	0	NEW90
1	0	0	NEW71/91

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								PCH (2/9) PCIE, SMBUS, CLK		
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								NEW71/91 M/B LA-5893P Schematic		
								Customer		
Date:		Tuesday, December 22, 2009				Sheet		14	of	56

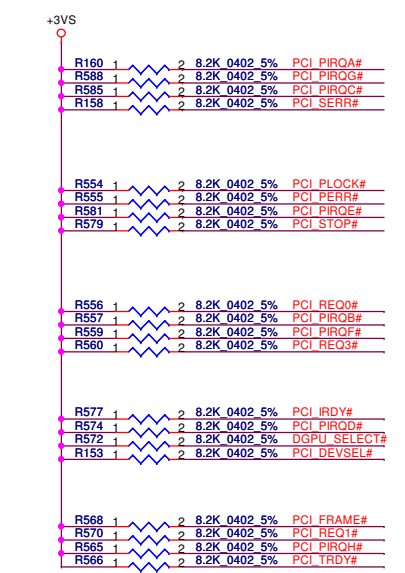
1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS
3. Level Shift2, Pull-Up to +3VS
4. Level Shift3, Pull-Up to +3VS

6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics

Change to 5x3.2



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				Size	Document Number	Rev
				Customer	NEW71/91 M/B LA-5893P Schematic	
				Date:	Tuesday, December 22, 2009	Sheet 15 of 56



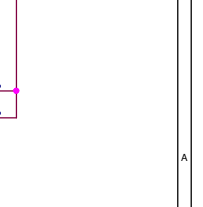
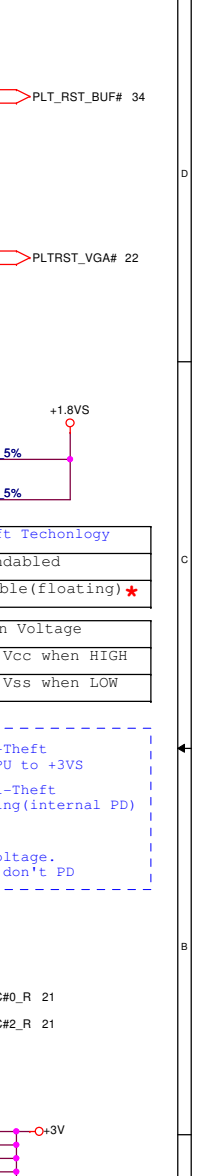
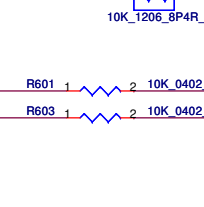
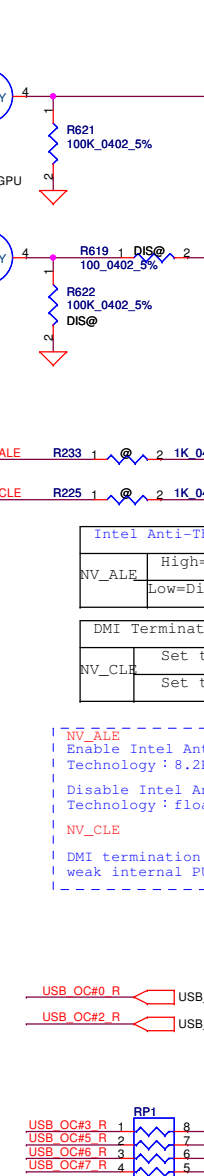
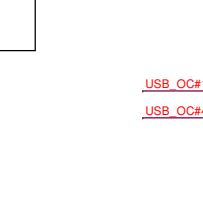
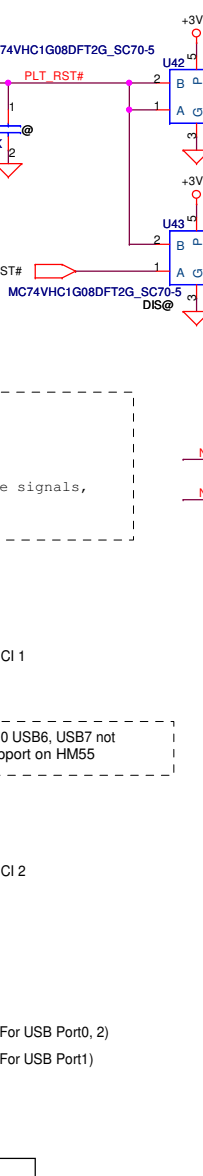
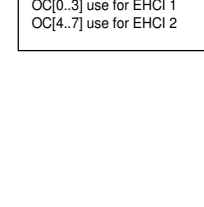
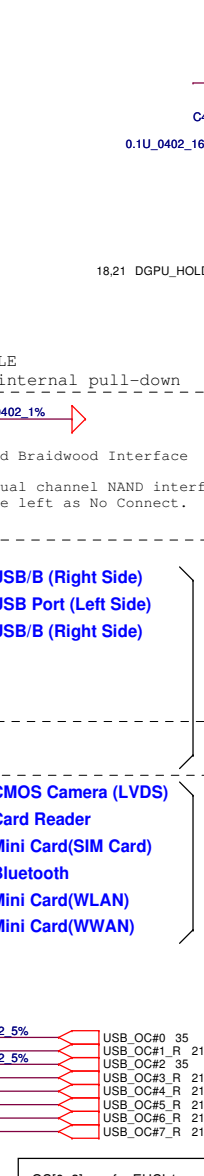
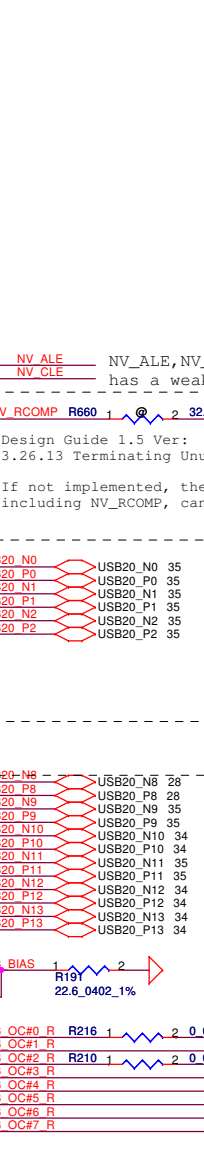
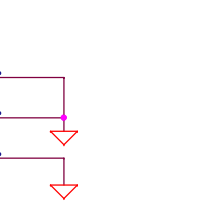
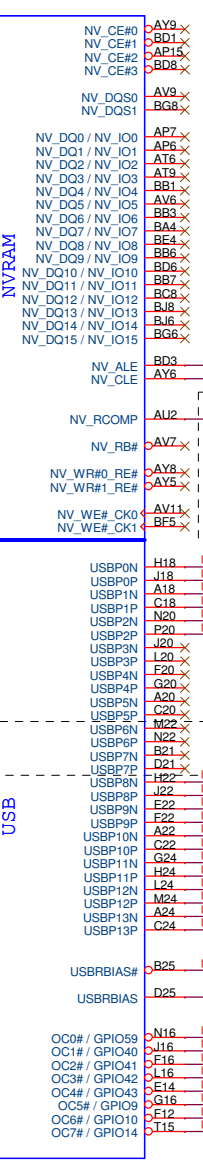
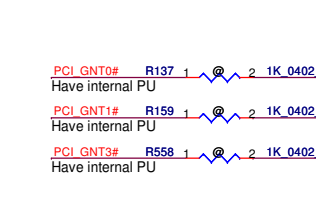
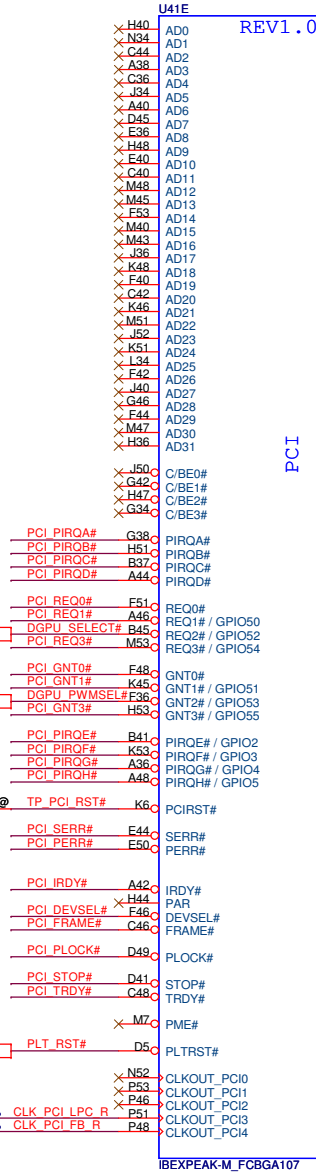
PCI_GNT0#, PCI_GNT1#, PCI_GNT2#, PCI_GNT3# has a weak internal pull-up

PCI_GNT2# ESI Strap (Server Only) this signal should not be pulled low

2008/1/6 2009MOW01 change to 22 ohm

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled High=Default ★

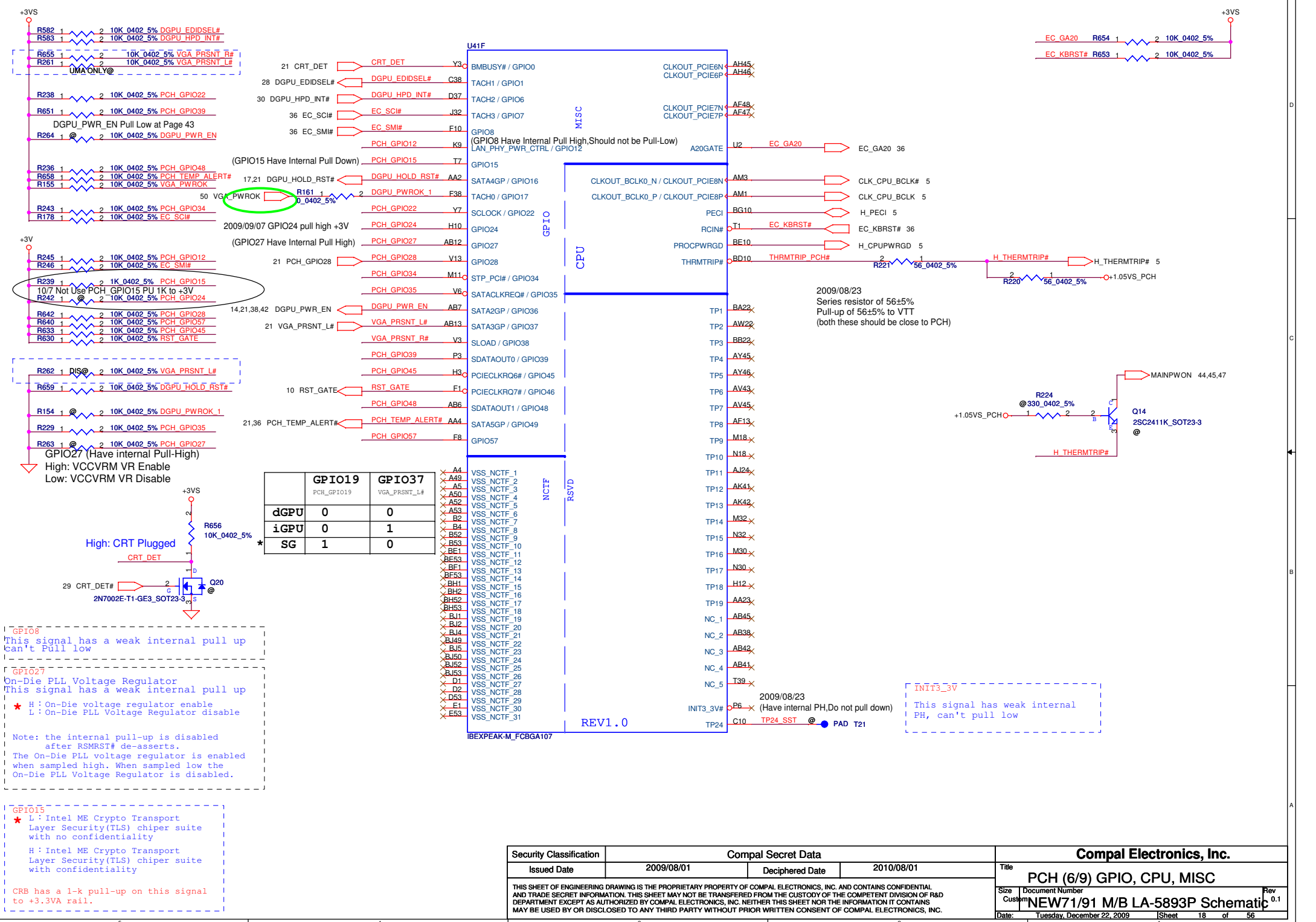


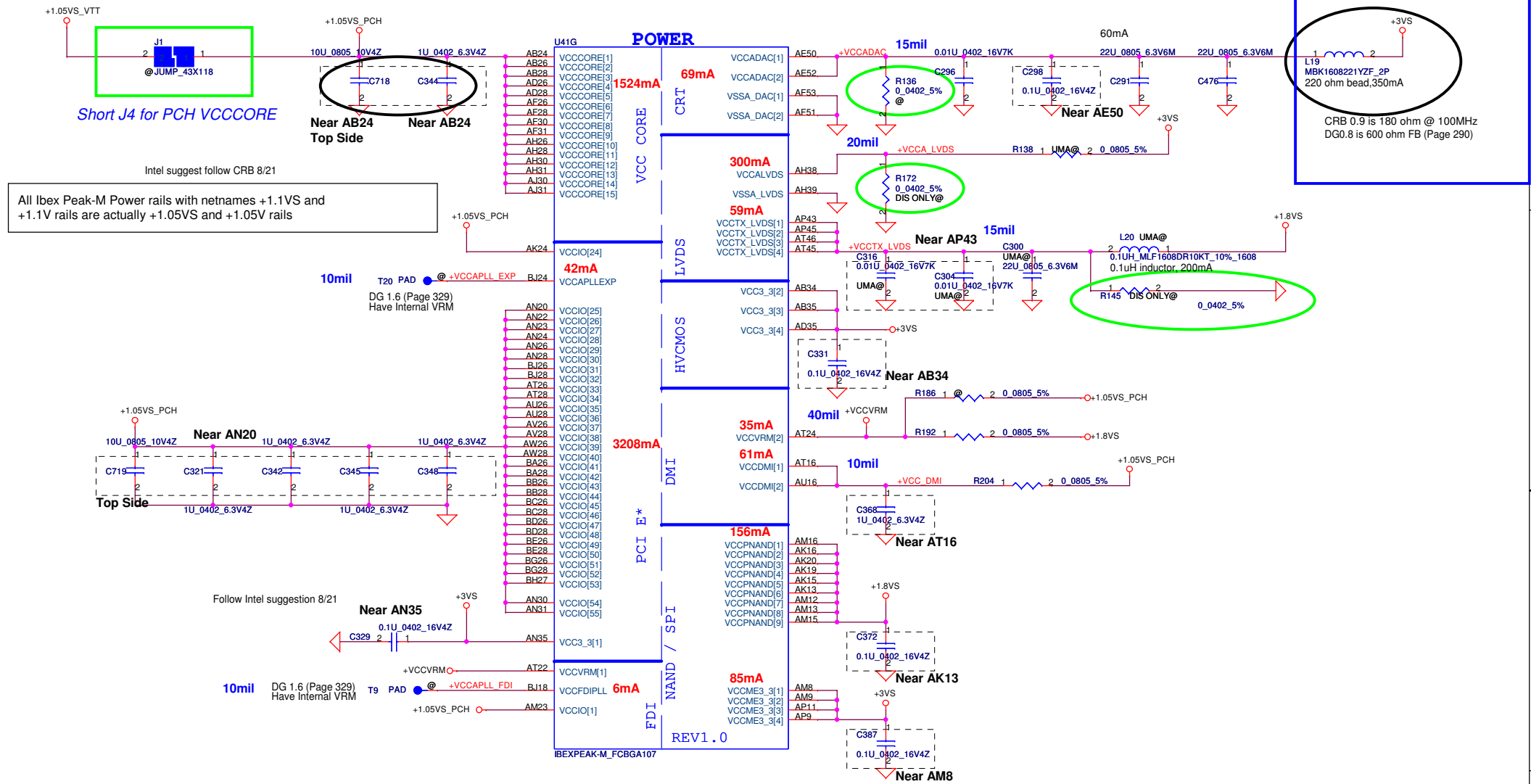
Intel Anti-Theft Technology	
NV_ALE	High=Enabled
NV_CLE	Low=Disable(floating)★

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
NV_CLE	Set to Vss when LOW

NV_ALE Enable Intel Anti-Theft Technology : 8.2K PU to +3VS
Disable Intel Anti-Theft Technology : floating(internal PD)
NV_CLE DMI termination voltage. weak internal PU, don't PD

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								Size		Document Number		Rev	
								Customer		NEW71/91 M/B LA-5893P Schematic		0.1	
								Date:		Tuesday, December 22, 2009		Sheet 17 of 56	



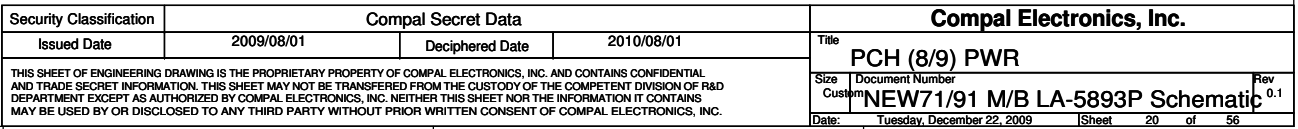


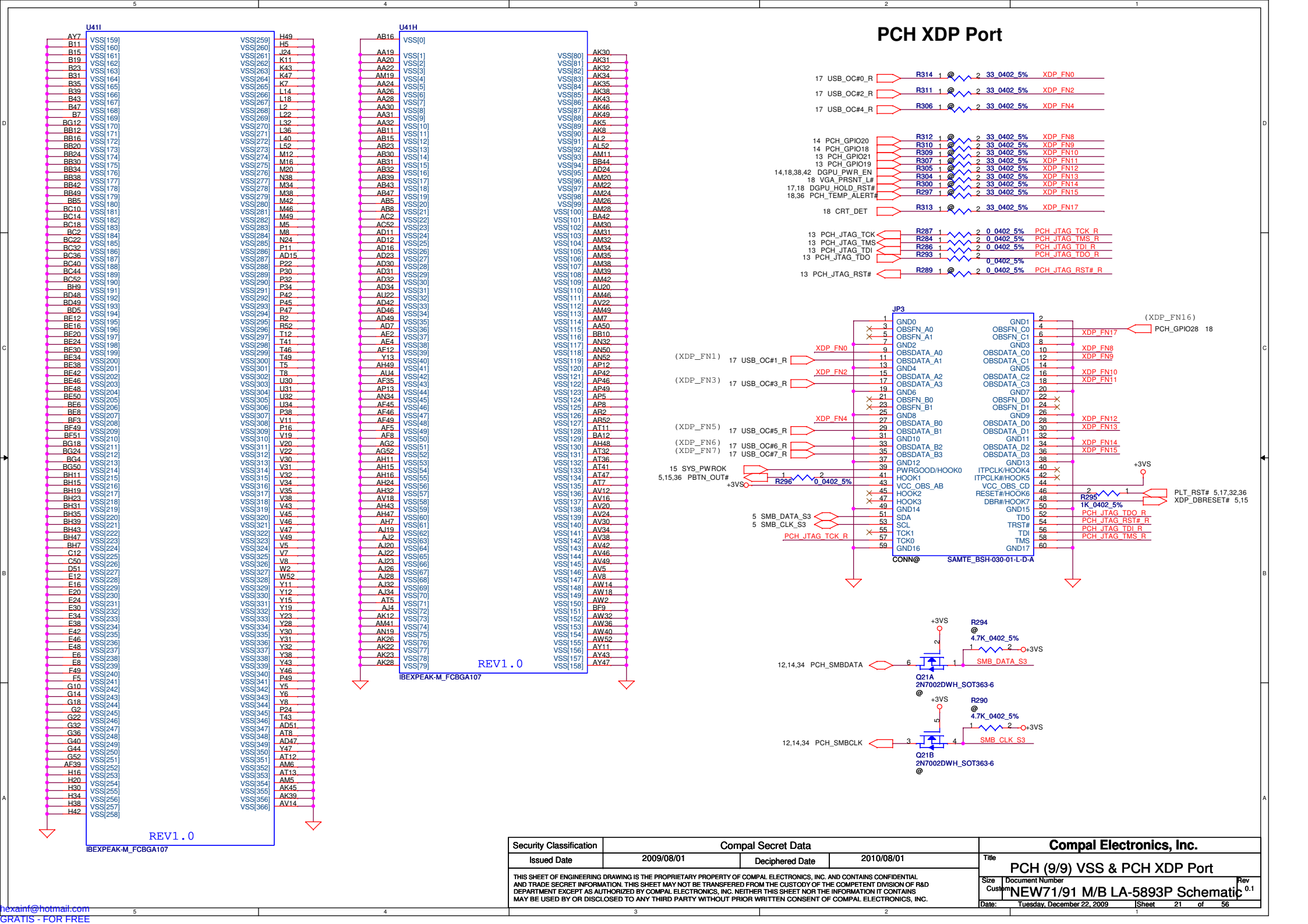
All Ibex Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails

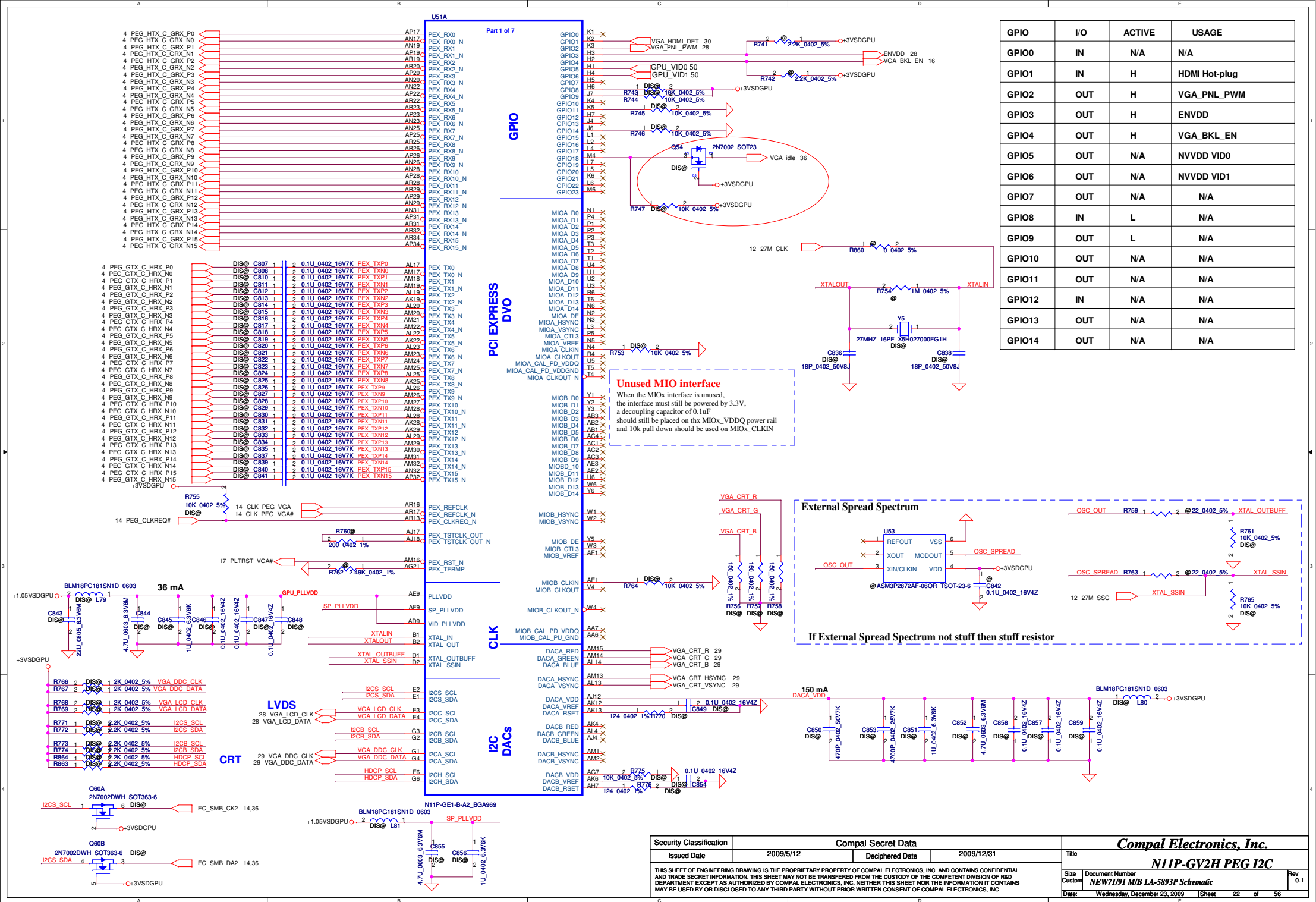
Need Modify
180 ohm @
100MHz Bead

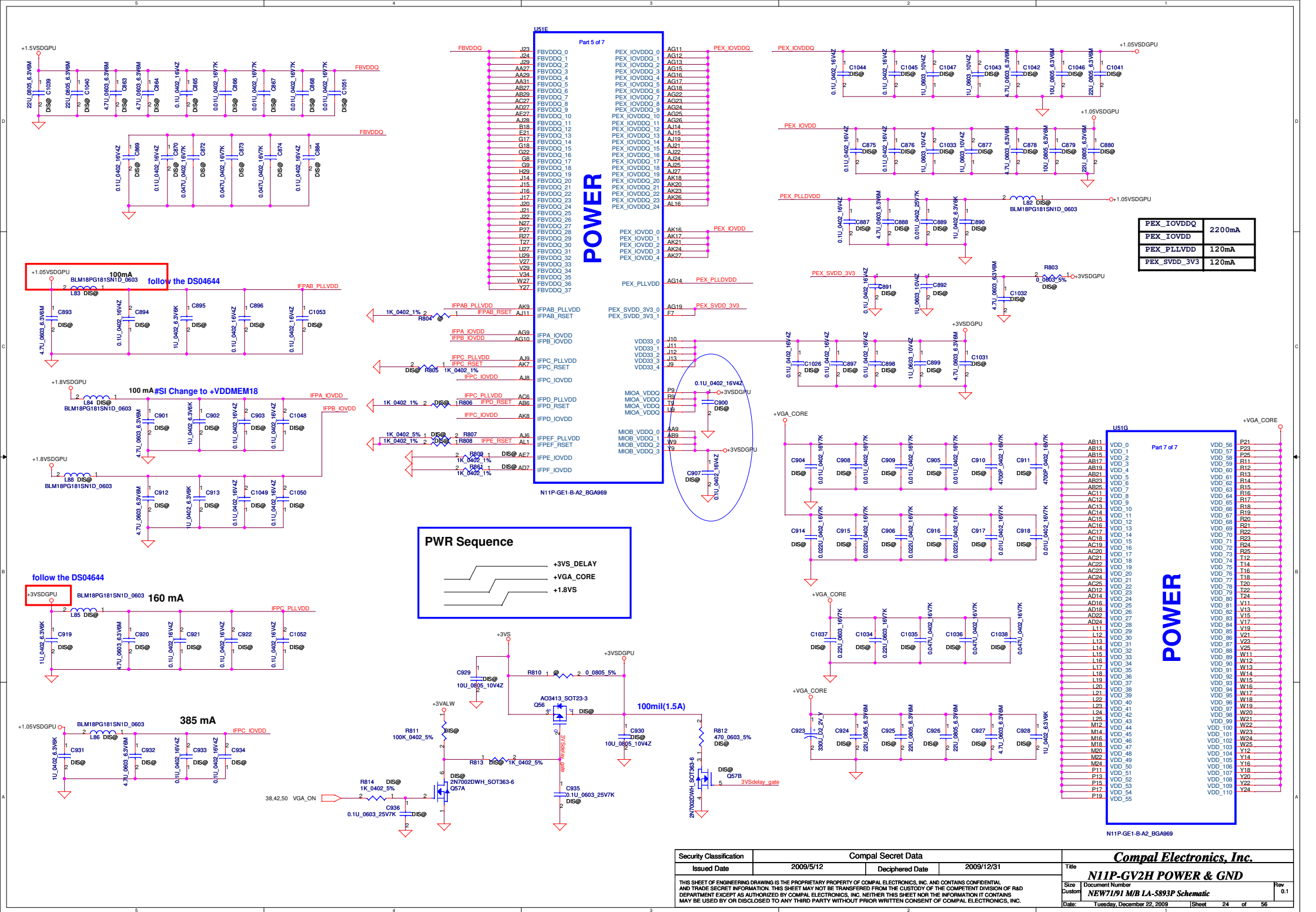
CRB 0.9 is 180 ohm @ 100MHz
DG0.8 is 600 ohm FB (Page 290)

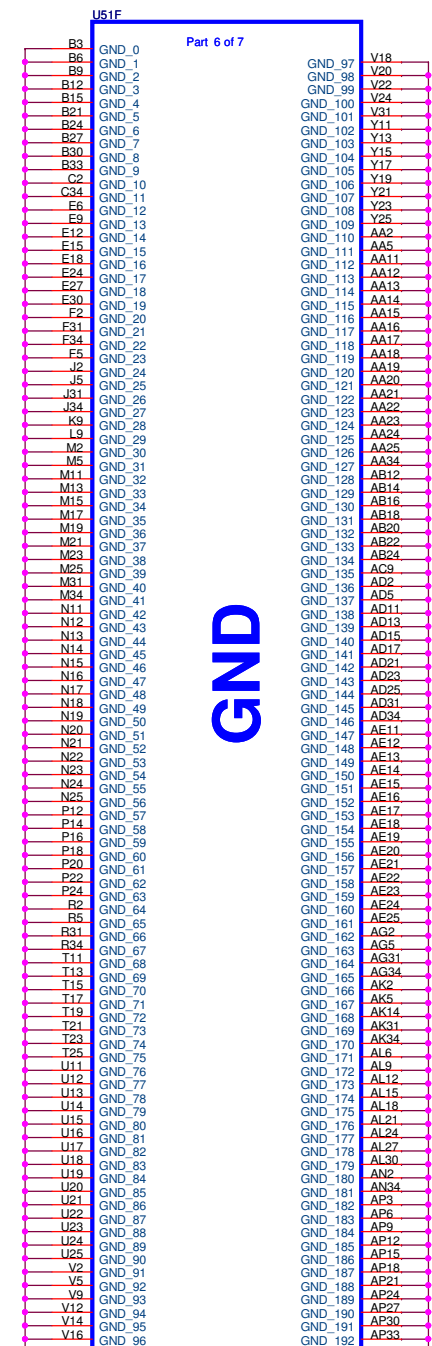
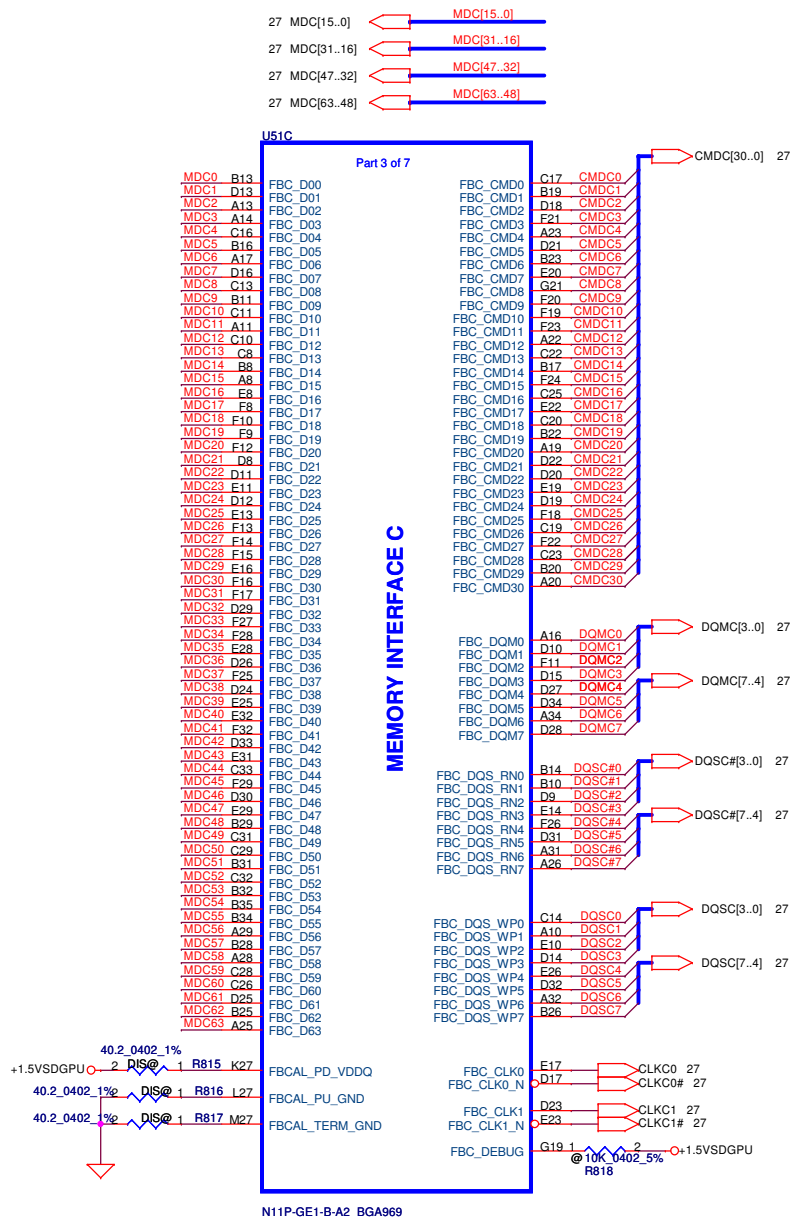
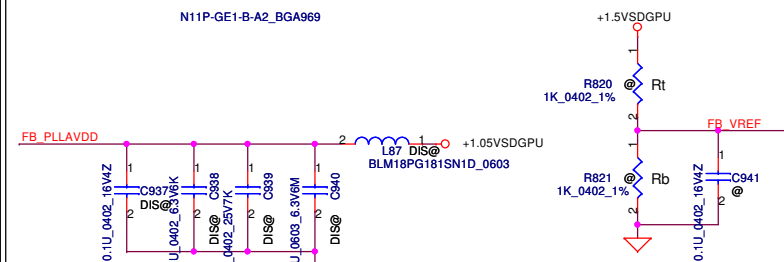
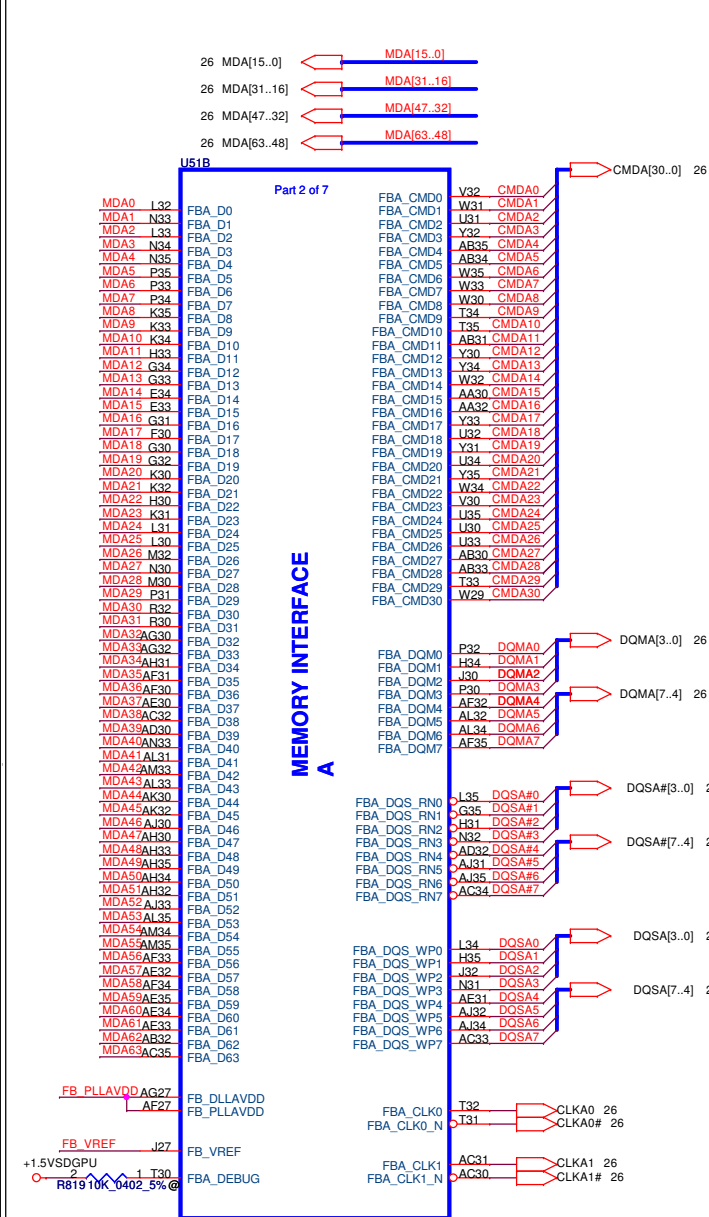
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title	PCH (7/9) PWR
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				Customer	NEW71/91 M/B LA-5893P Schematic
				Date	Friday, December 18, 2009
				Sheet	19 of 56











Security Classification		Compal Secret Data		Compal Electronics, Inc. Title <i>N11P-GV2H VRAM</i>	
Issued Date	2009/5/12	Deciphered Date	2009/12/31	Size Document Number Custom <i>NEW7191 M/B LA-5893P Schematic</i>	Rev 0.1
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SM10014520 3000ma 220ohm@100mhz DCR 0.04

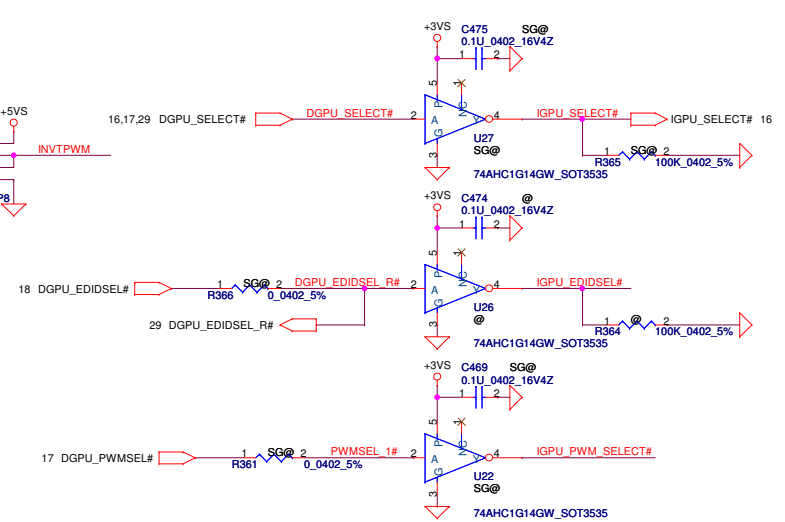
PCB layout for the USB20 module, showing the connection of the USB20 module to the main board. The layout includes the USB20 module footprint, the USB20 module pinout, and the main board pinout.

USB20 Module Pinout (Left):

- 1: INVPWR_B+
- 2: +LVD5_R
- 3: R679 0.0603 5%
- 4: LCDVDD
- 5: LCDVDD
- 6: +3VS
- 7: INVTPWM
- 8: DISPOFF#
- 9: I2CC_SGL
- 10: I2CC_SDA
- 11: DAC_BRIG 36
- 12: TXOUT0-
- 13: TXOUT0+
- 14: TXOUT1-
- 15: TXOUT1+
- 16: TXOUT2-
- 17: TXOUT2+
- 18: TXCLK-
- 19: TXCLK+
- 20: 0.0402 5% 2 @ 1 R368
- 21: 0.0402 5% 2 @ 1 R369
- 22: LOCAL_DIM 36
- 23: COLOR_ENG_EN 36
- 24: USB20_CMOS_N8
- 25: USB20_CMOS_P8
- 26: USB20_N8 17
- 27: USB20_P8 17
- 28: 1109 RF request
- 29: 1109 RF request
- 30: 1109 RF request
- 31: 1109 RF request
- 32: 1109 RF request
- 33: 1109 RF request
- 34: 1109 RF request
- 35: 1109 RF request
- 36: 1109 RF request
- 37: 1109 RF request
- 38: 1109 RF request
- 39: 1109 RF request
- 40: 1109 RF request

Main Board Pinout (Right):

- 1: +3VS
- 2: +LVD5
- 3: Place closed to JLVDS1
- 4: C464 0.1U_0402_16V4Z
- 5: C461 10U_0805_10V4Z
- 6: C458 0.1U_0402_16V4Z
- 7: DAC_BRIG
- 8: INVTPWM
- 9: DISPOFF#
- 10: C467 220P_0402_50V7K
- 11: C468 220P_0402_50V7K
- 12: C473 220P_0402_50V7K
- 13: DISPOFF# 0.0402 5% 2
- 14: R363
- 15: BKOFF
- 16: 10K 0402 5% 2
- 17: R362
- 18: LOCAL_DIM 36
- 19: COLOR_ENG_EN 36
- 20: USB20_CMOS_N8
- 21: USB20_CMOS_P8
- 22: USB20_N8 17
- 23: USB20_P8 17
- 24: 1109 RF request
- 25: 1109 RF request
- 26: 1109 RF request
- 27: 1109 RF request
- 28: 1109 RF request
- 29: 1109 RF request
- 30: 1109 RF request
- 31: 1109 RF request
- 32: 1109 RF request
- 33: 1109 RF request
- 34: 1109 RF request
- 35: 1109 RF request
- 36: 1109 RF request
- 37: 1109 RF request
- 38: 1109 RF request
- 39: 1109 RF request
- 40: 1109 RF request



SWITCHABLE 2009/8/27 ADD SWITCHABLE

Pin-to-pin comparison diagram for P31VD400ZFE and P31VD400ZF.

Top Pin List (P31VD400ZFE):

Signal	Pin	Signal	Pin
VGA TXCLK+	48	0B1	48
VGA TXCLK-	47	1B1	47
VGA TXOUT2+	43	1B1	43
VGA TXOUT2-	42	2B1	42
VGA TXOUT1+	37	3B1	37
VGA TXOUT1-	36	4B1	36
VGA TXOUT0+	32	5B1	32
VGA TXOUT0-	31	6B1	31
VGA LCD CLK	22	7B1	22
VGA LCD DATA	23	9B1	23

Bottom Pin List (P31VD400ZF):

Signal	Pin	Signal	Pin
PCH TXCLK+	46	0B2	46
PCH TXCLK-	45	1B2	45
PCH TXOUT2+	41	2B2	41
PCH TXOUT2-	40	3B2	40
PCH TXOUT1+	35	4B2	35
PCH TXOUT1-	34	5B2	34
PCH TXOUT0+	30	6B2	30
PCH TXOUT0-	29	7B2	29
PCH LCD CLK	25	8B2	25
PCH LCD DATA	26	9B2	26
DGPU EIDSEL R#	54	SEL2	54
	52	NC	52
	5	NC	5
	51	NC	51
	57	Thermal_GND	57
		GND	

Internal Connections (Schematic):

- 3V3S SWITCH
- SG0, SG1, SG2, SG3
- C63, C64, C66
- 0.1uF 0402, 18V4Z
- 0.1uF 0402, 18V4Z
- DGPU_SELECT#
- SEL1
- GND

Bottom Labels:

- P31VD400ZFE_TXFN56_1TXS
- SG0#
- P31VD400ZF with 2 SEL pin

Timing diagram for UIMA ONLY. The diagram shows the relationship between various signals and their timing parameters. The signals are listed in the left column, and their timing parameters are listed in the middle column. The signal sources are listed in the right column. The signals are: TXOUT0+, TXOUT1+, TXOUT2+, TXCLK+, I2CC_SCL, I2CC_SDA, and PCH_LCD_CLK. The timing parameters are: 0, 0.402, 5%, 2. The signal sources are: UIMA ONLY, R416, R412, R405, R410, R401, R389, R393, R396, R418, R420. The diagram also shows a 3V5 supply and a 5/4 PCH_LCD_CLK & PCH_LCD_DATA pull-up note.

Signal	Timing Parameters	Signal Source
TXOUT0+	0 0.402 5% 2	UIMA ONLY @ R416
TXOUT0-	0.402 5% 2	UIMA ONLY @ R412
TXOUT1+	0 0.402 5% 2	UIMA ONLY @ R405
TXOUT1-	0 0.402 5% 2	UIMA ONLY @ R410
TXOUT2+	0 0.402 5% 2	UIMA ONLY @ R401
TXOUT2-	0 0.402 5% 2	UIMA ONLY @ R389
TXCLK+	0 0.402 5% 2	UIMA ONLY @ R393
TXCLK-	0 0.402 5% 2	UIMA ONLY @ R396
I2CC_SCL	0 0.402 5% 2	UIMA ONLY @ R418
I2CC_SDA	0 0.402 5% 2	UIMA ONLY @ R420

3V5

5/4 PCH_LCD_CLK & PCH_LCD_DATA
Pull high 2.2K change to 4.7K

R29 1 UIMA @ 2.7K 0.402 5% PCH_LCD_CLK

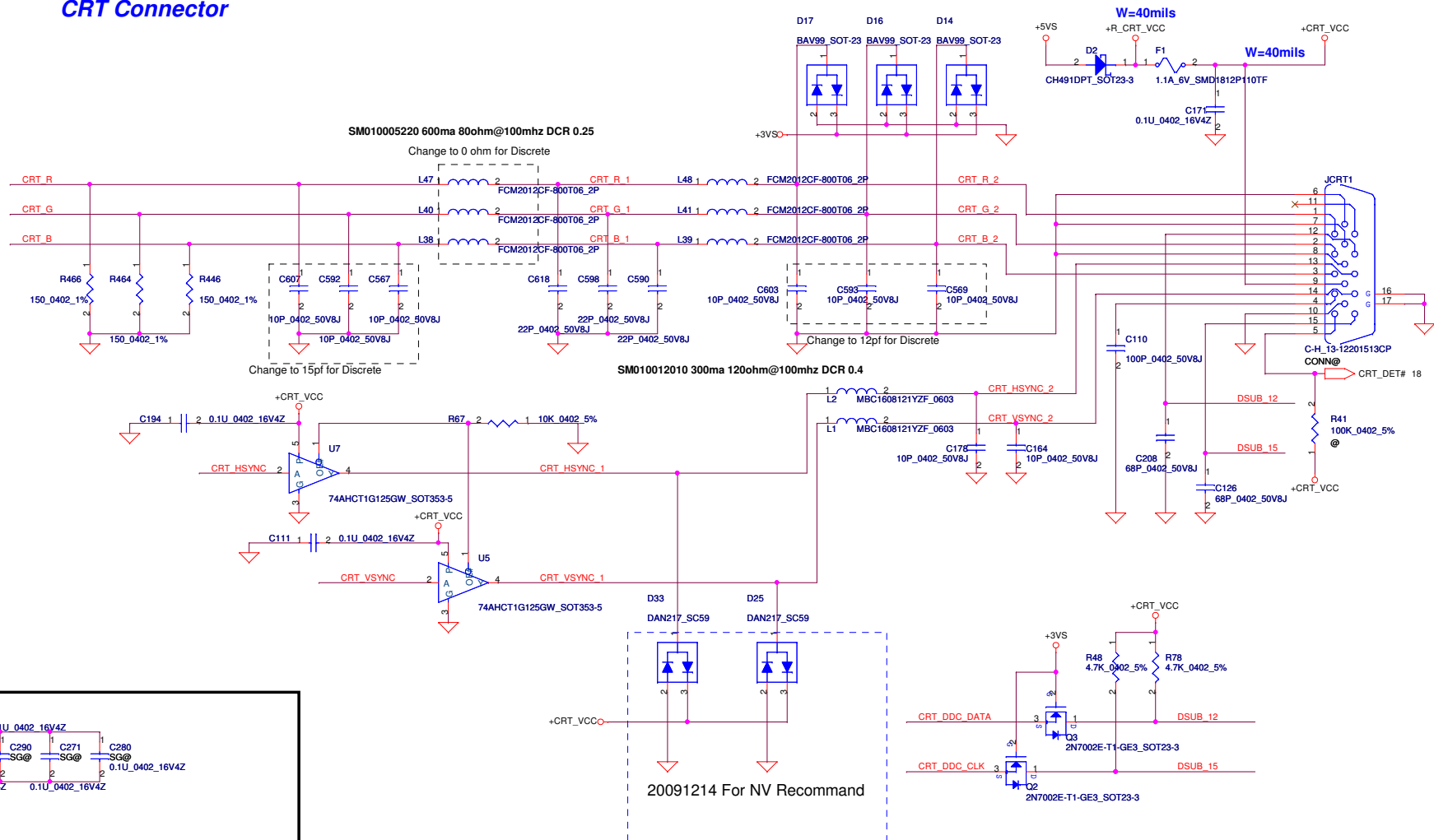
R32 1 UIMA @ 2.7K 0.402 5% PCH_LCD_DATA

Discrete ONLY

TXOUT0+	0	0402	5%	2	DIS_ONLY	R26	VGA_TXOUT0+	VGA_TXOUT0+ 23
TXOUT0-	0	0402	5%	2	DIS_ONLY	R24	VGA_TXOUT0-	
TXOUT1+	0	0402	5%	2	DIS_ONLY	R22	VGA_TXOUT1+	VGA_TXOUT1+ 23
TXOUT1-	0	0402	5%	2	DIS_ONLY	R23	VGA_TXOUT1-	
TXOUT2+	0	0402	5%	2	DIS_ONLY	R20	VGA_TXOUT2+	VGA_TXOUT2+ 23
TXOUT2-	0	0402	5%	2	DIS_ONLY	R21	VGA_TXOUT2-	
TXCLK+	0	0402	5%	2	DIS_ONLY	R18	VGA_TXCLK+	VGA_TXCLK+ 23
TXCLK-	0	0402	5%	2	DIS_ONLY	R19	VGA_TXCLK-	
I2CC_SCL	0	0402	5%	2	DIS_ONLY	R419	VGA_LCD_CLK	VGA_LCD_CLK 22
I2CC_SDA	0	0402	5%	2	DIS_ONLY	R421	VGA_LCD_DATA	

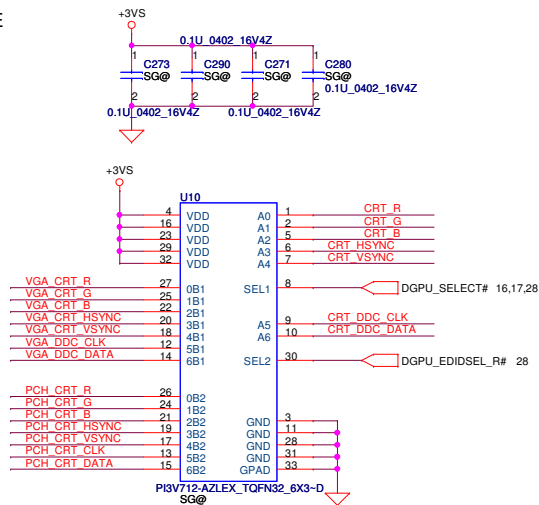
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				Size	Document Number	Rev	
				Custom	NEW7/191 M/B LA-5893P Schematic	0.1	
Date:	Tuesday, December 22, 2009	Sheet	28	of	56		

CRT Connector



SWITCHABLE

2009/08/27



L	B1	DIS
H	B2	UMA

Discrete only

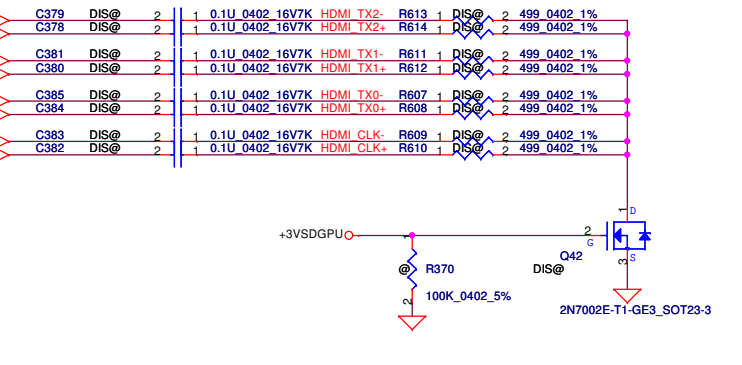
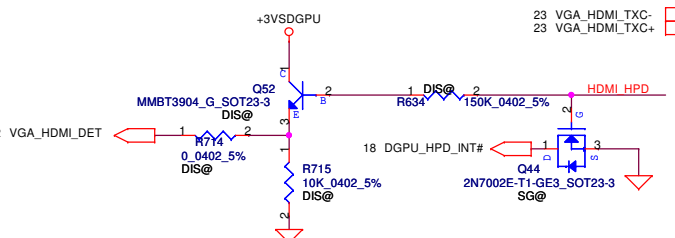
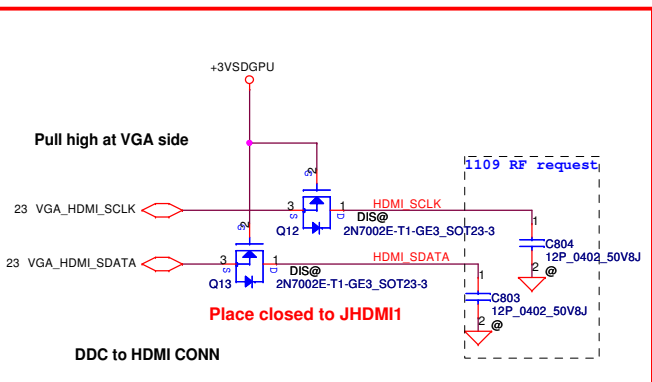
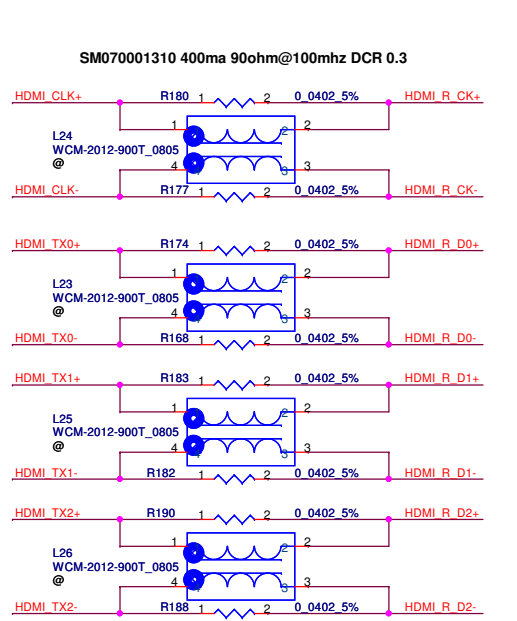
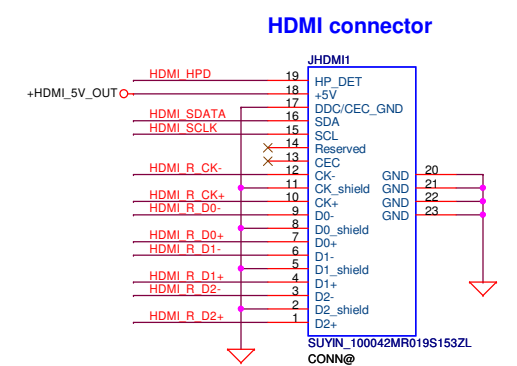
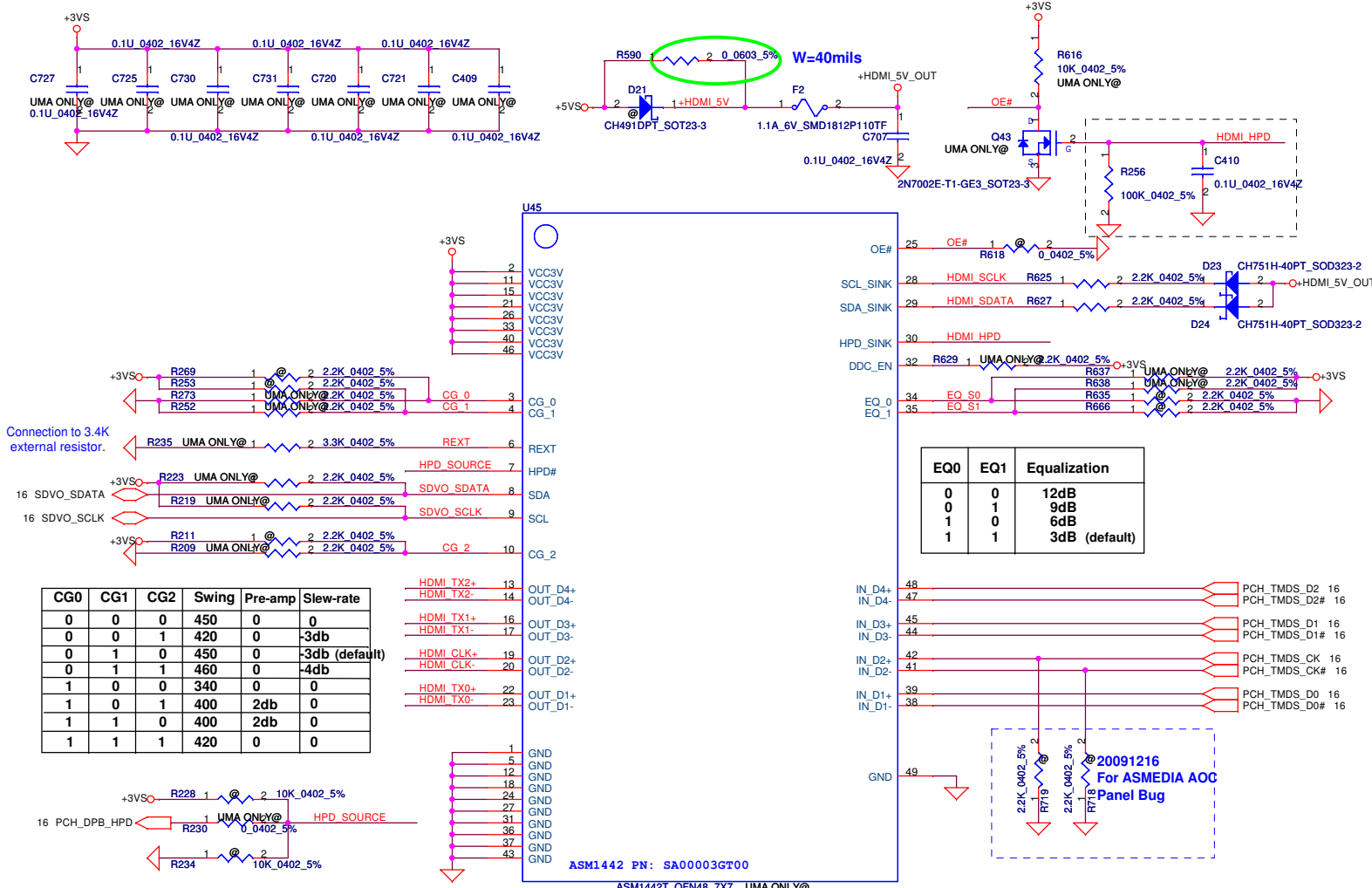
22	VGA_CRT_R		VGA CRT_R	R537	2	DIS_ONLY	0	0402	5%	CRT_R
22	VGA_CRT_G		VGA CRT_G	R535	2	DIS_ONLY	0	0402	5%	CRT_G
22	VGA_CRT_B		VGA CRT_B	R533	2	DIS_ONLY	0	0402	5%	CRT_B
22	VGA_CRT_HSYNC		VGA CRT HSYNC	R531	2	DIS_ONLY	0	0402	5%	CRT_HSYNC
22	VGA_CRT_VSYNC		VGA CRT VSYNC	R529	2	DIS_ONLY	0	0402	5%	CRT_VSYNC
22	VGA_DDC_CLK		VGA DDC_CLK	R527	2	DIS_ONLY	0	0402	5%	CRT_DDC_CLK
22	VGA_DDC_DATA		VGA DDC_DATA	R526	2	DIS_ONLY	0	0402	5%	CRT_DDC_DATA

VGA_DDC_DATA and VGA_DDC_CLK Pull high at Page22

UMA only

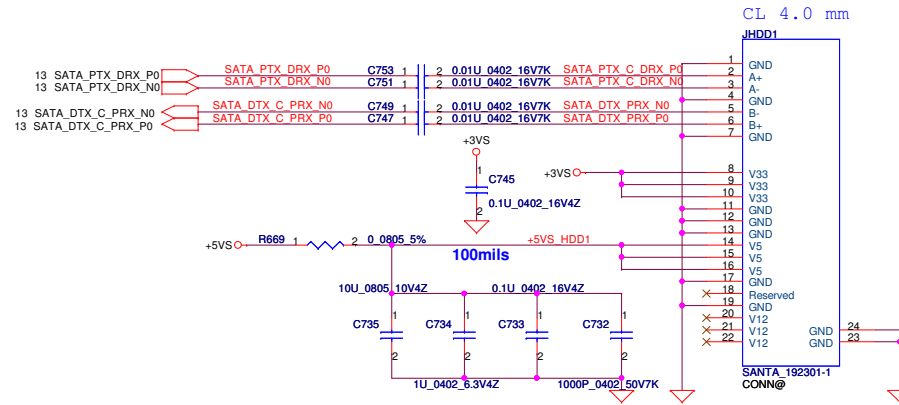
16	PCH_CRT_R	PCH CRT R	R536	2	UMA ONLY@	0	0.002	5%	CRT R
16	PCH_CRT_G	PCH CRT G	R534	2	UMA ONLY@	0	0.002	5%	CRT G
16	PCH_CRT_B	PCH CRT B	R532	2	UMA ONLY@	0	0.002	5%	CRT B
16	PCH_CRT_HSYNC	PCH CRT HSYNC	R530	2	UMA ONLY@	0	0.002	5%	CRT HSYNC
16	PCH_CRT_VSYNC	PCH CRT VSYNC	R528	2	UMA ONLY@	0	0.002	5%	CRT VSYNC
16	PCH_CRT_CLK	PCH CRT CLK	R544	2	UMA ONLY@	0	0.002	5%	CRT DDC CLK
16	PCH_CRT_DATA	PCH CRT DATA	R543	2	UMA ONLY@	0	0.002	5%	CRT DDC DATA

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				CRT Connector	
				Size B	Document Number NEW71/91 M/B LA-5893P Schematic
Date		Tuesday, December 22, 2009		Sheet	29 of 56

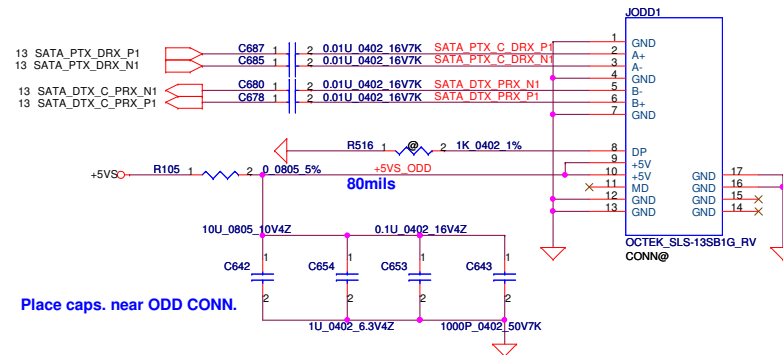


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Size	Document Number	Rev		NEW71/91 M/B LA-5893P Schematic	
Custom					
Date:	Tuesday, December 22, 2009	Sheet	30	of 56	

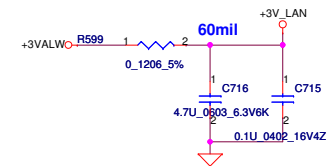
SATA HDD1 Conn.



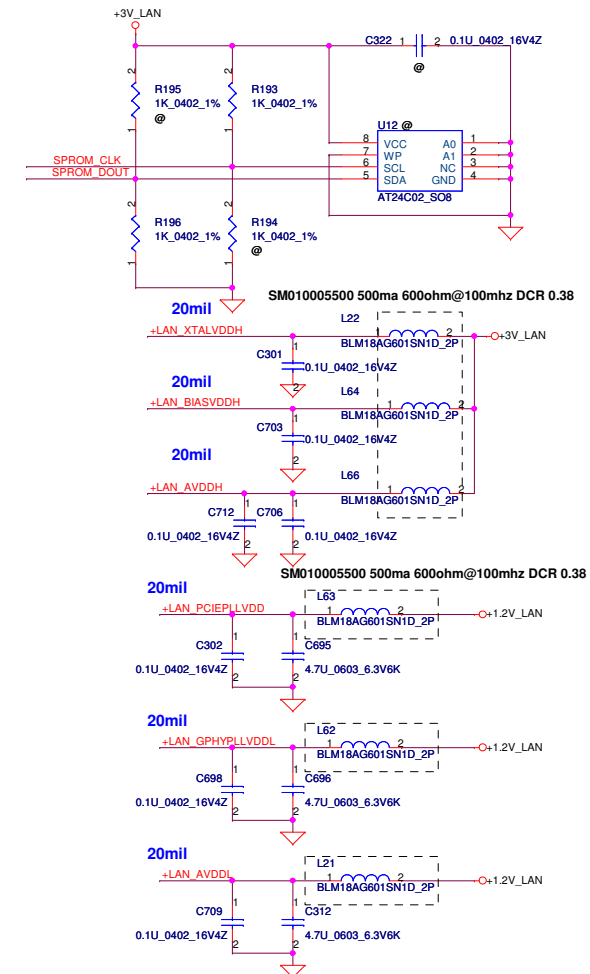
SATA ODD Conn.



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				Customer	NEW71/91 M/B LA-5893P Schematic
				Date	Tuesday, December 22, 2009
				Sheet	31 of 56

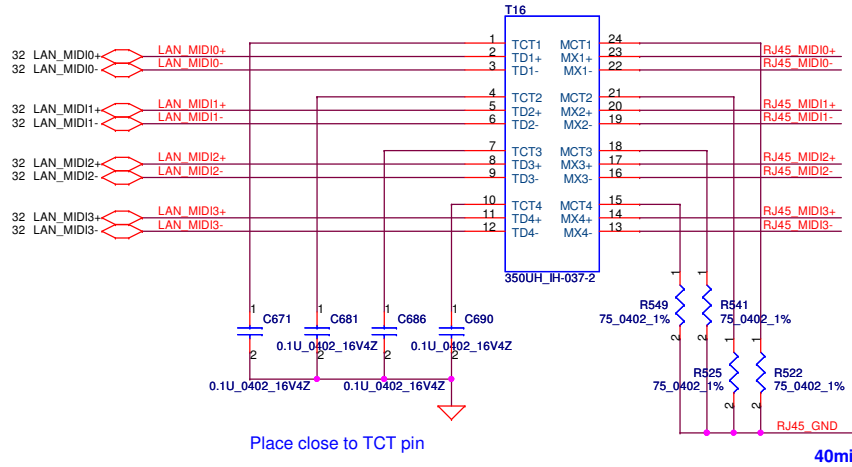


	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

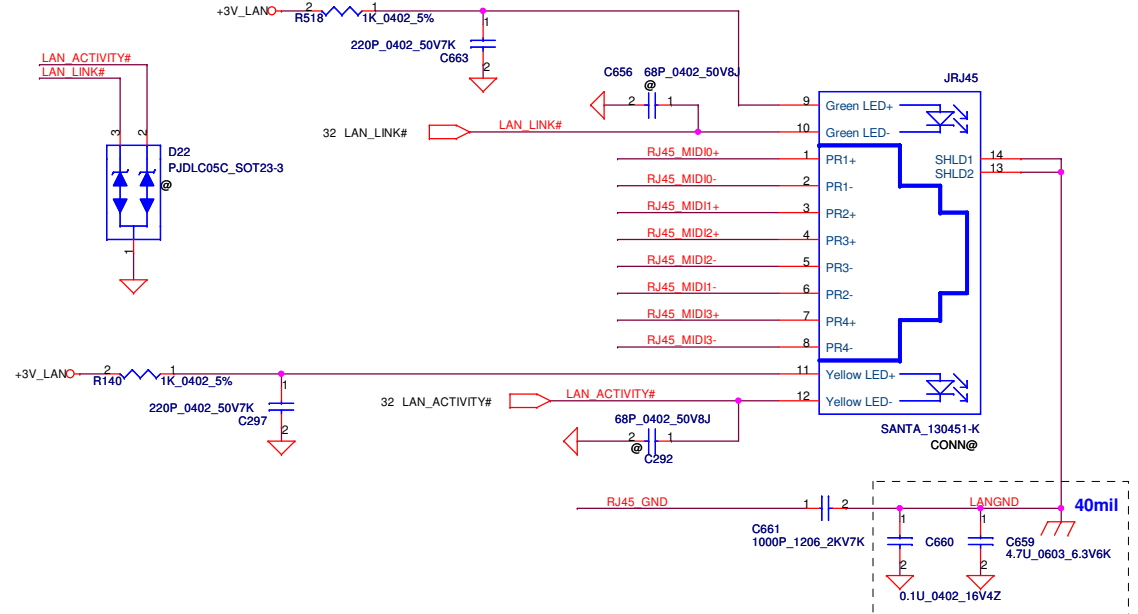


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Date:				Tuesday, December 22, 2009		Sheet		32 of 56					

LAN Connector

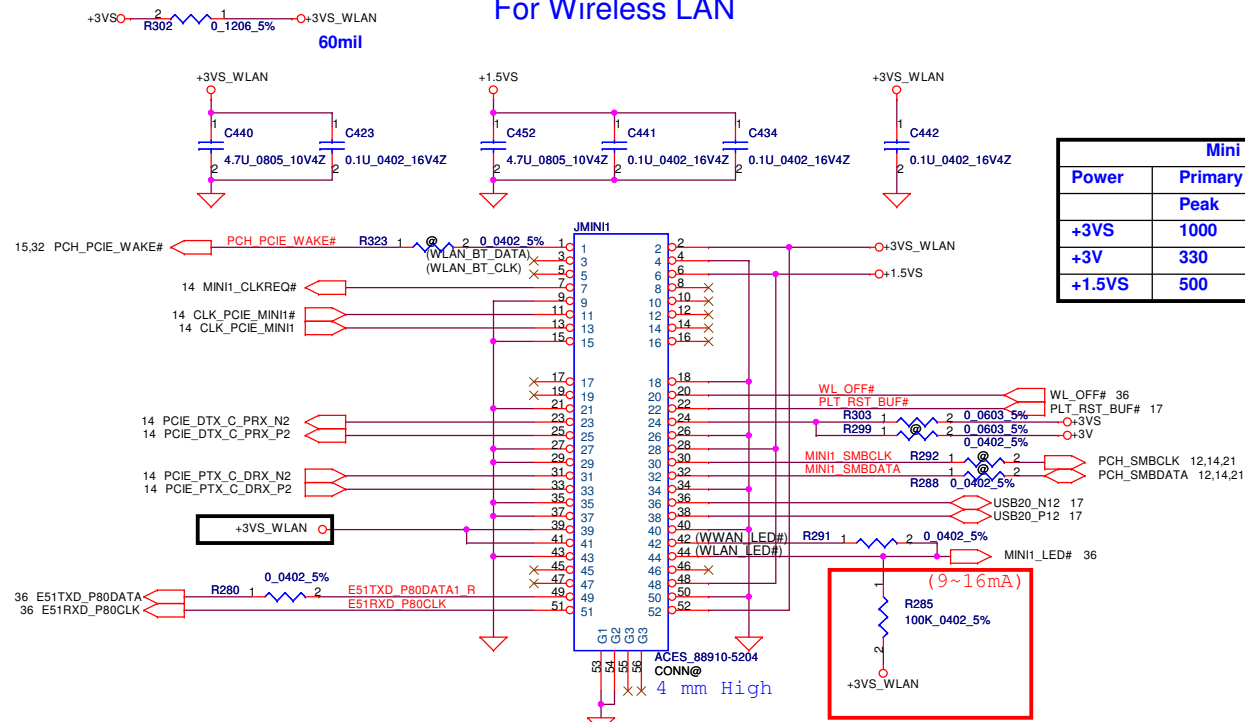


BOTH HAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG: S X'FORM_ IH-160 LAN, SP050006F00



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Size	Document Number	Customer		Rev	
NEW71/91	M/B LA-5893P Schematic	Date		Tuesday, December 22, 2009	
Sheet	33	of		56	

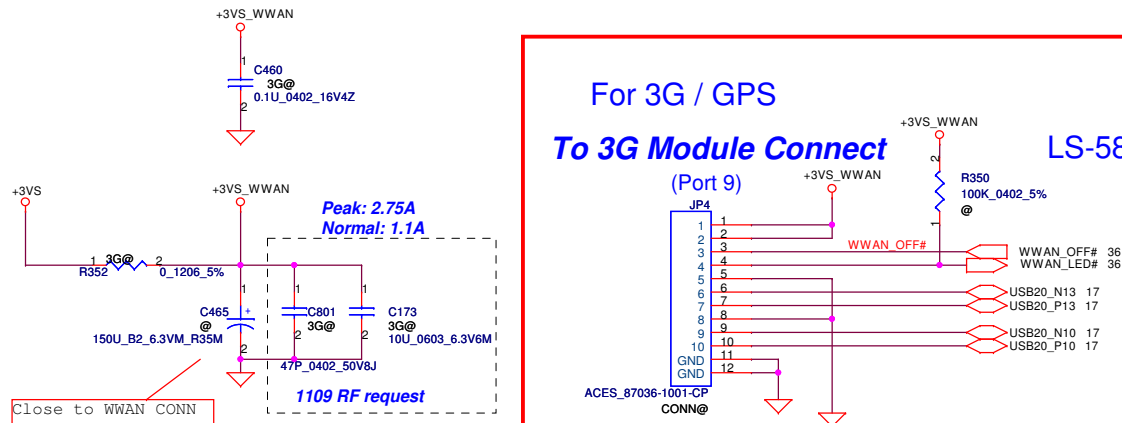
For Wireless LAN

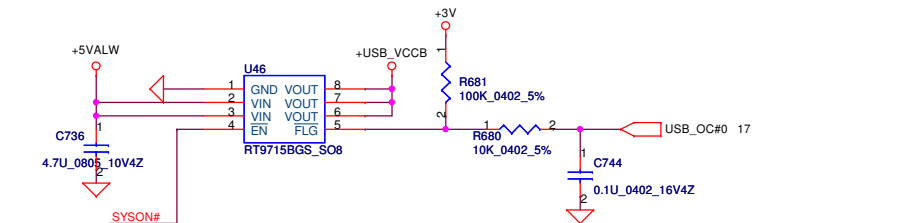
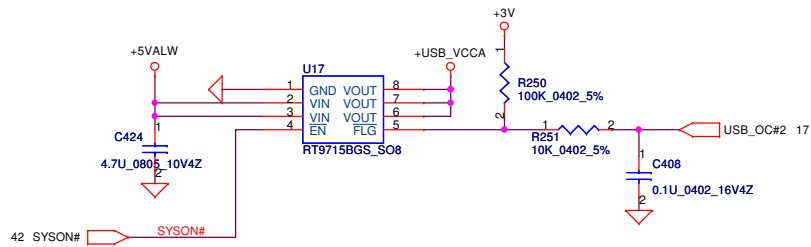


For 3G / GPS

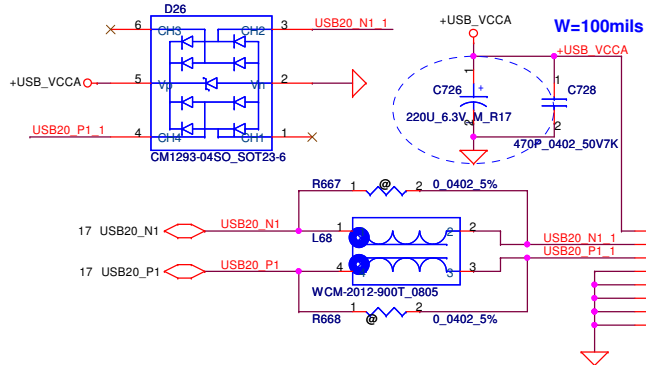
To 3G Module Connect

LS-5895



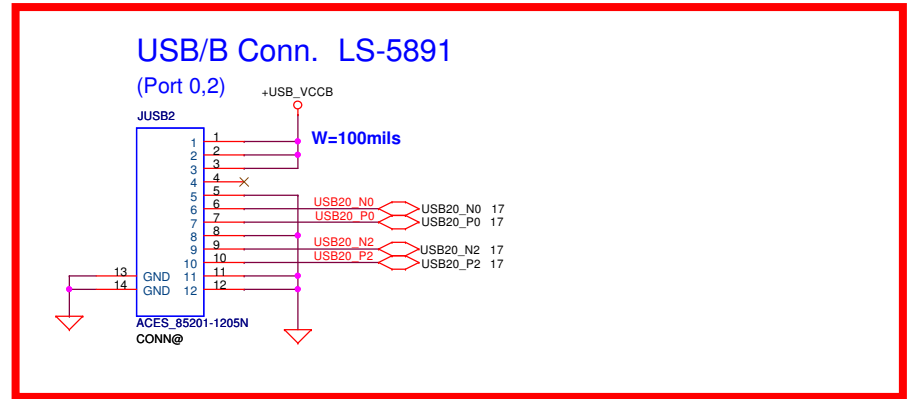


2009/08/14 CHANGE cap



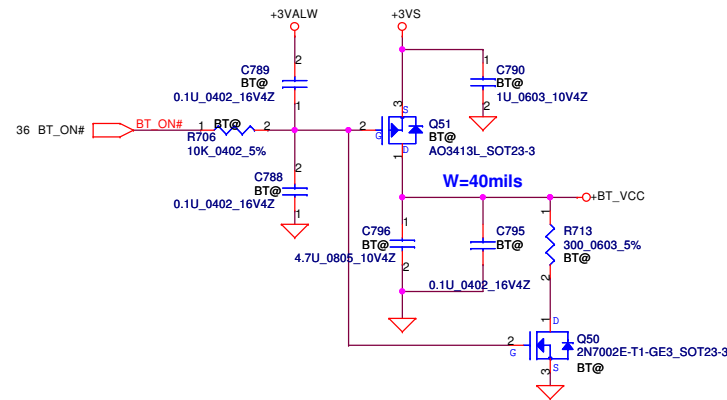
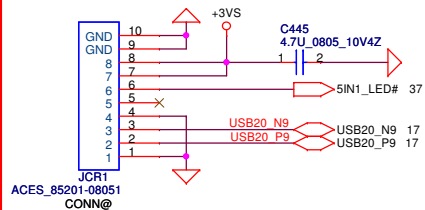
2009/08/25 Update Footprint(follow NAL00)

USB Conn.
(Port 1)



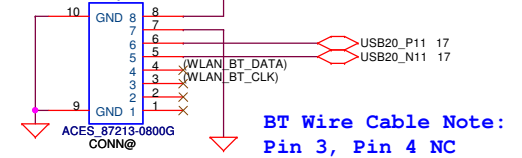
2009/08/24 CHANGE Conn to FFC Type

Card Reader Conn. LS-5896



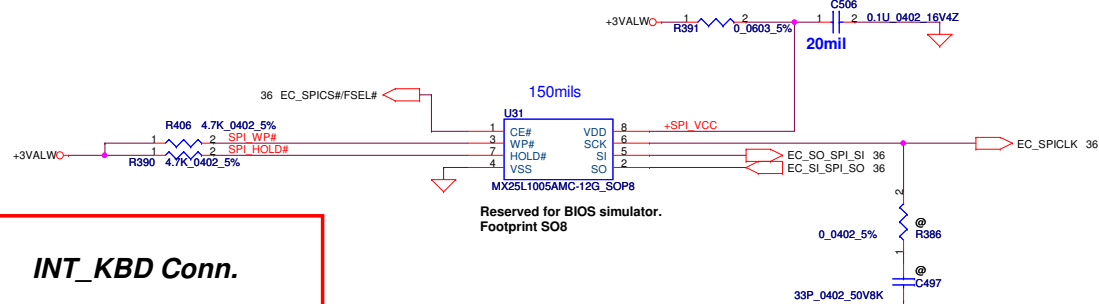
BT Conn.

(Port 11)

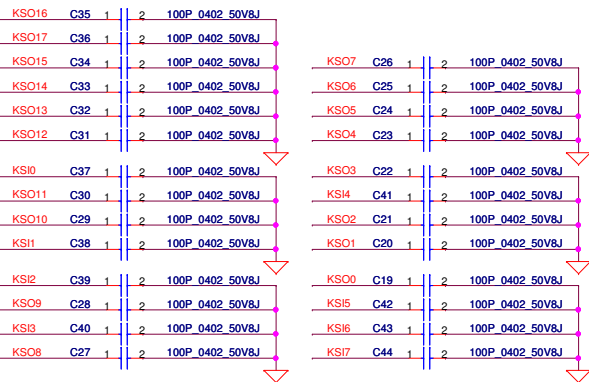
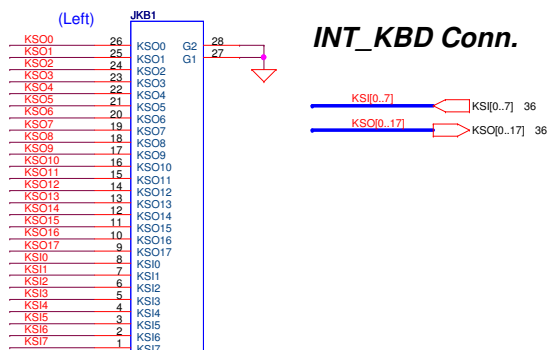


BT Wire Cable Note:
Pin 3, Pin 4 NC

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2010/08/01				Title				USB / BT / USBB			
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				Customer				NEW71/91 M/B LA-5893P Schematic			
				Date				Thursday, December 24, 2009			
				Sheet				35 of 56			

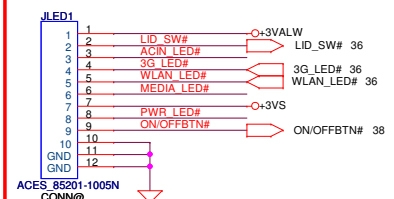


INT_KBD Conn.

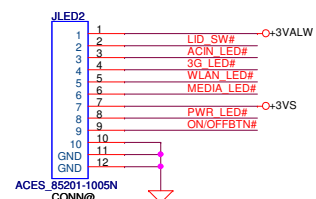


LS-5893+LS-5894(Lid Board)

LED/B RIGHT (90)

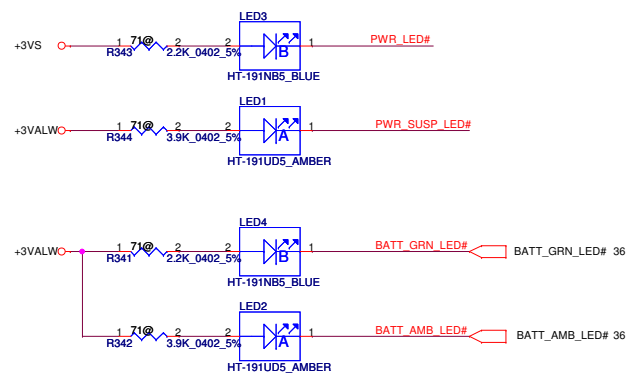
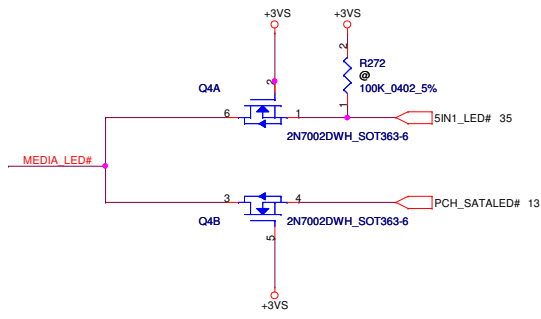
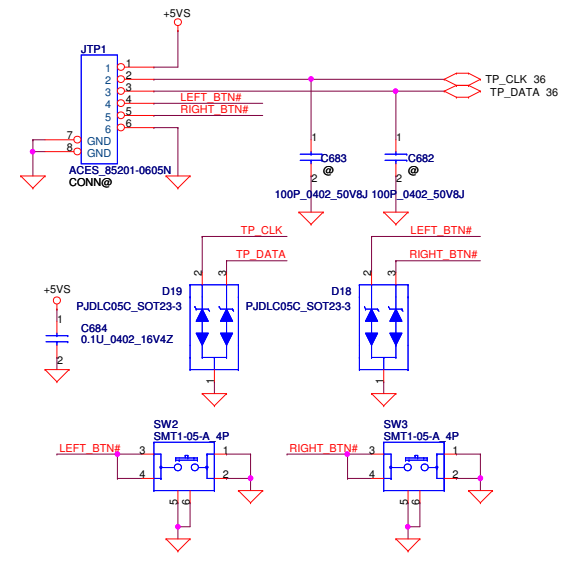


LED/B LEFT (70)

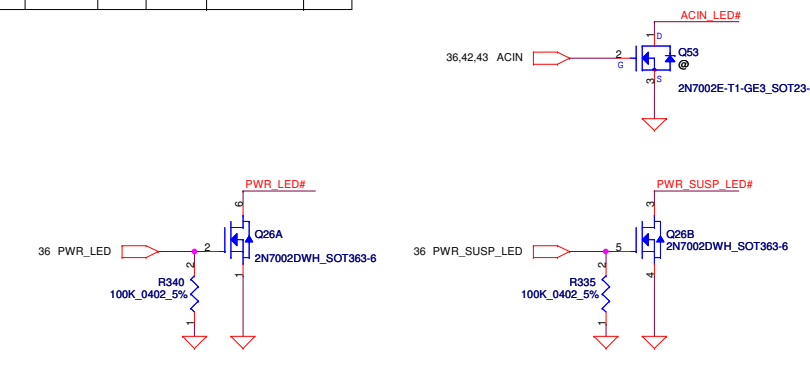


LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber	Blue	Amber		

To TP/B Conn.



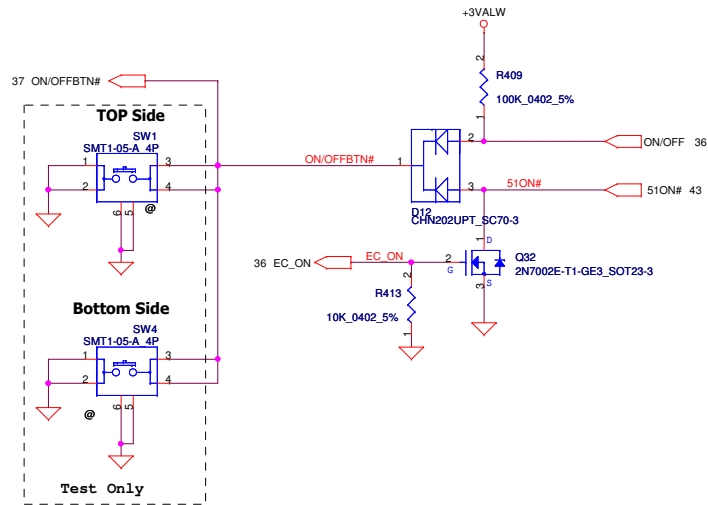
Bom option
For 71 and 91



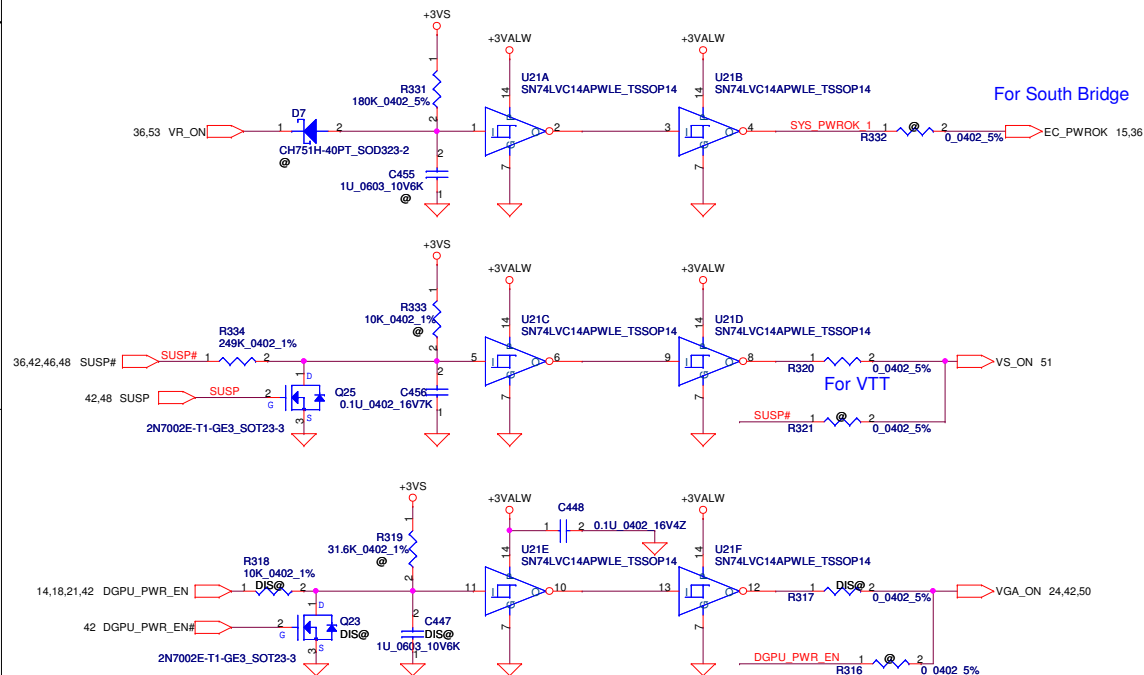
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Issued Date		2008/08/10		Deciphered Date		2010/08/01		Title							
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								Size B	Document Number						Rev
									NEW71/91 M/B LA-5893P Schematic						0.1
Date:				Tuesday, December 22, 2009		Sheet		37 of 56							

Power Button

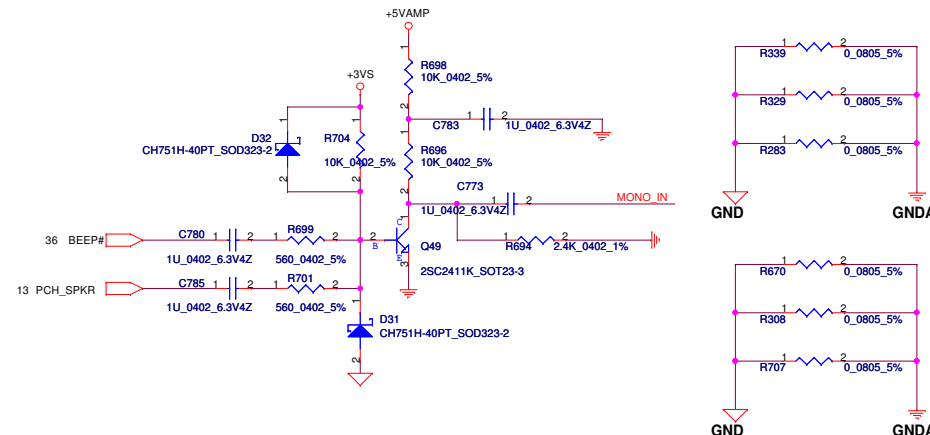
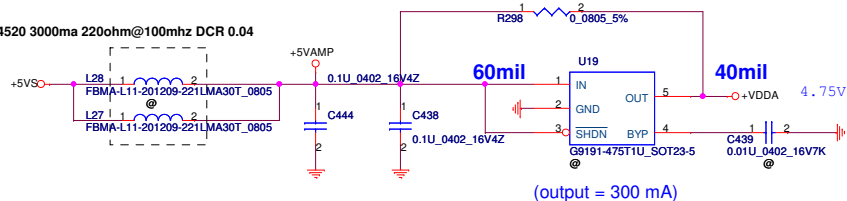
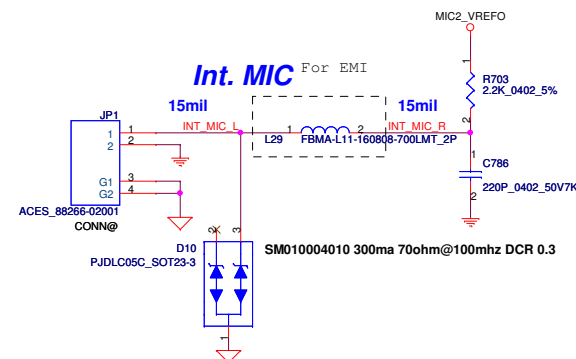
ON/OFF switch



Power ON Circuit

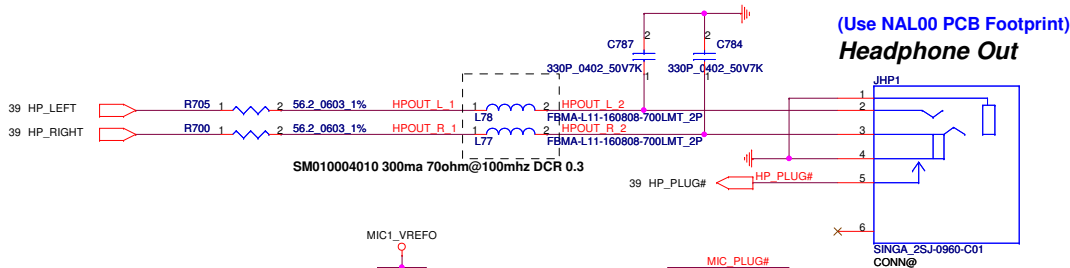
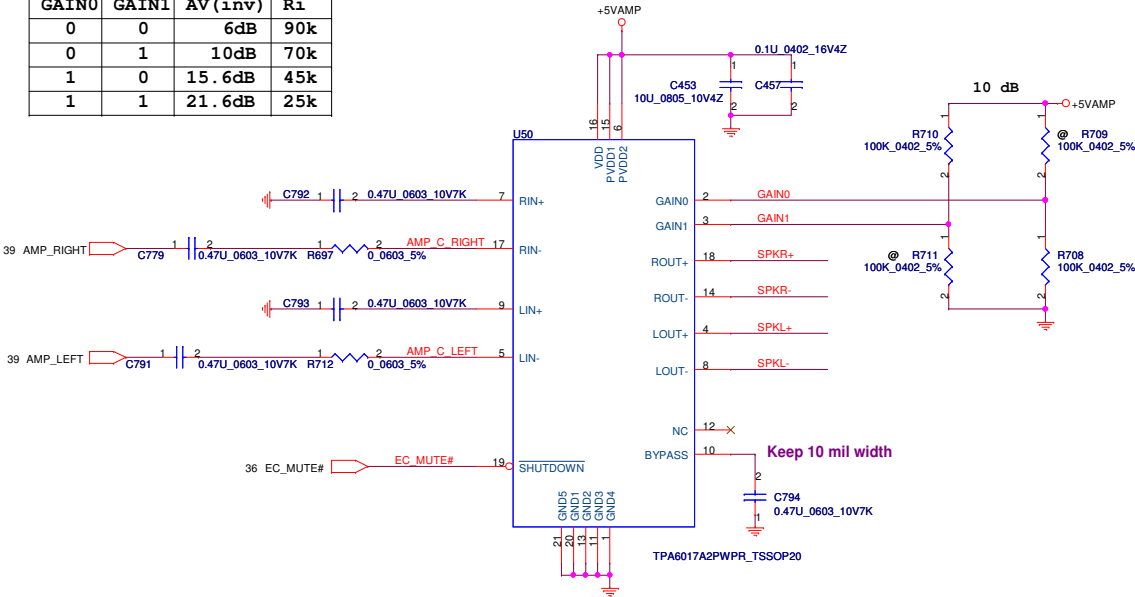


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Issued Date		2008/08/10	Deciphered Date	2010/08/01	Title		
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					Size B	Document Number	Rev
					NEW71/91 M/B LA-5893P Schematic	0.1	
					Date:	Tuesday, December 22, 2009	Sheet 36 of 56

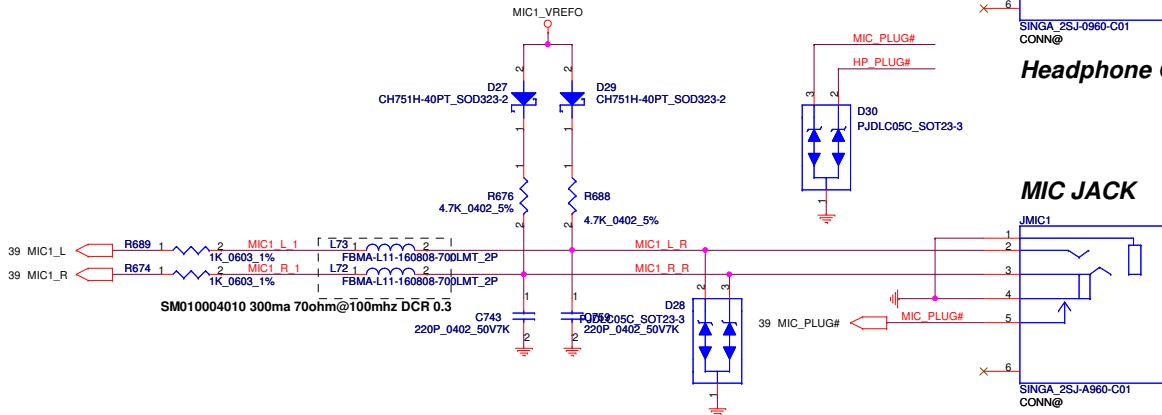
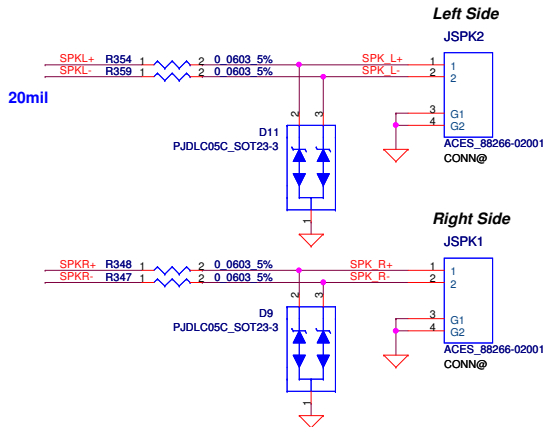
[illegible]

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/08/10	Deciphered Date	2010/08/01	Title	HD Audio Codec ALC272X
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				Custom	NEW7/91 M/B LA-5893P Schematic
				Date:	Tuesday, December 22, 2009
				Sheet	39 of 56

GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k

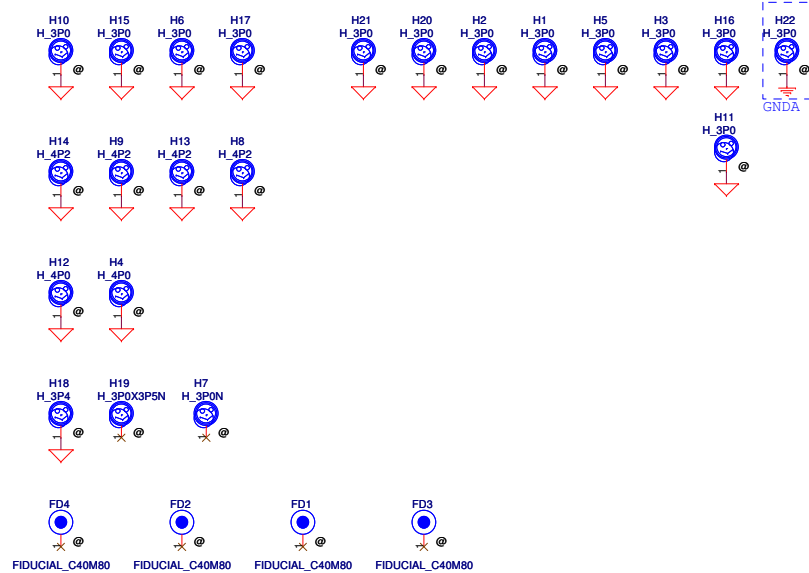
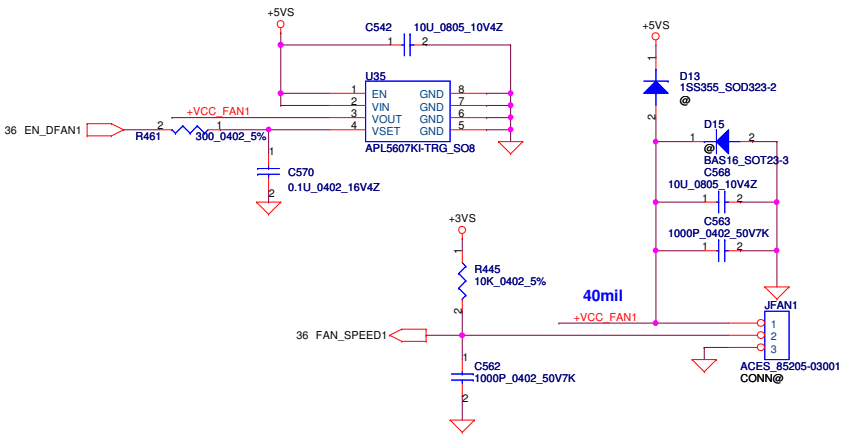


Int. Speaker Conn.



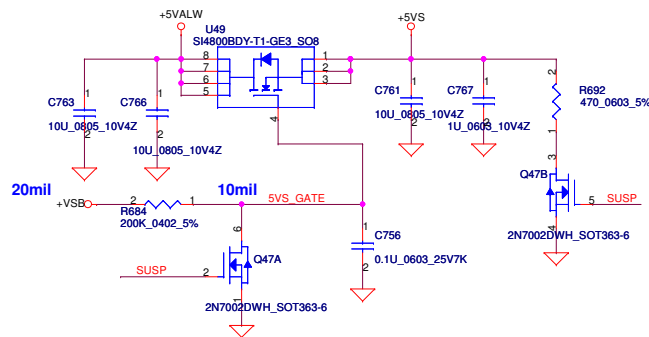
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2008/08/10				Deciphered Date			
								2010/08/01			
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								Amplifier & Audio Jack			
								Size Document Number			
								Customer NEW71/91 M/B LA-5893P Schematic			
								Date: Tuesday, December 22, 2009			
								Sheet 40 of 56			

FAN1 Conn



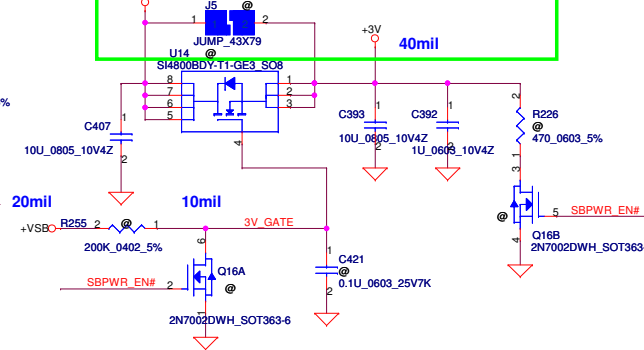
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Issued Date	2008/08/10	Deciphered Date	2010/08/01	Title	
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Size	B	Document Number	NEW71/91 M/B LA-5893P Schematic	Rev	0.1
Date:	Tuesday, December 22, 2009	Sheet	41	of	56

+5VALW TO +5VS

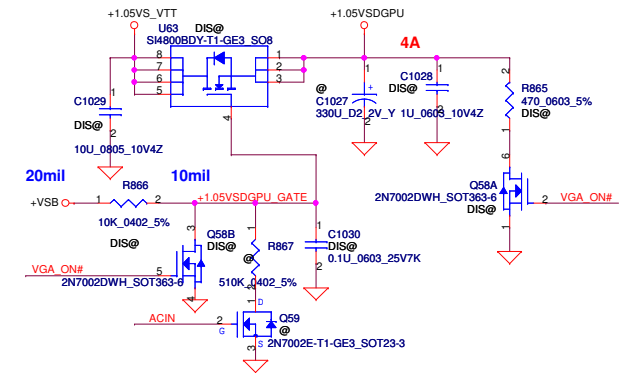


+3VALW TO +3V (PCH AUX Power)

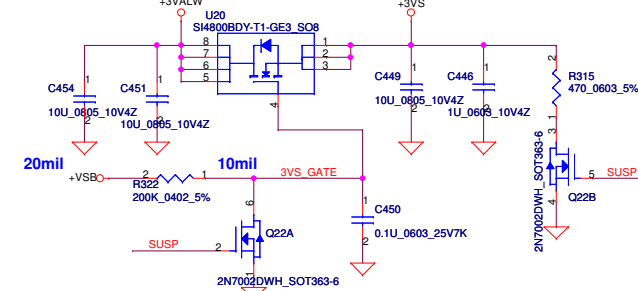
Short J5 for PCH VCCSUS3.3



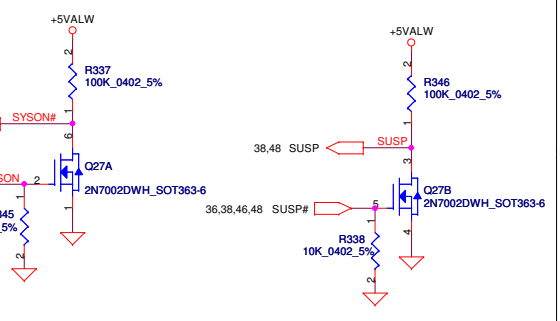
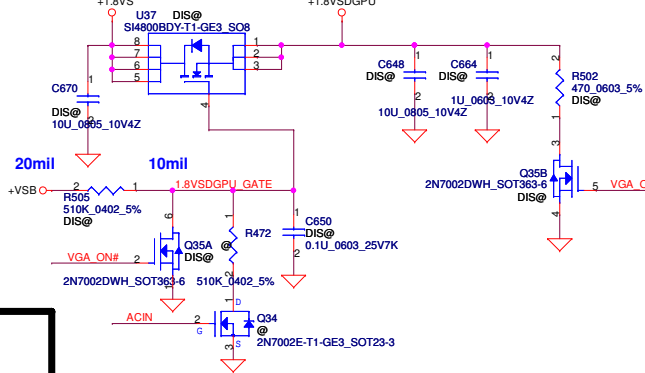
+1.05VS_VTT to +1.05VSDGPU for GPU



+3VALW TO +3VS

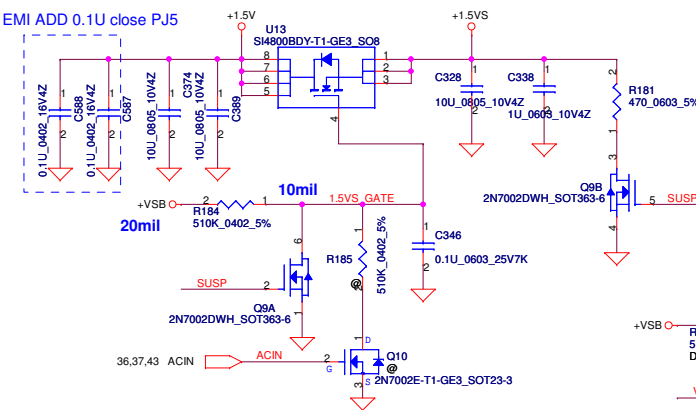


+1.8VS to +1.8VSDGPU for GPU

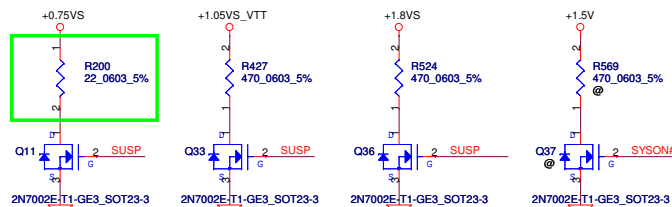
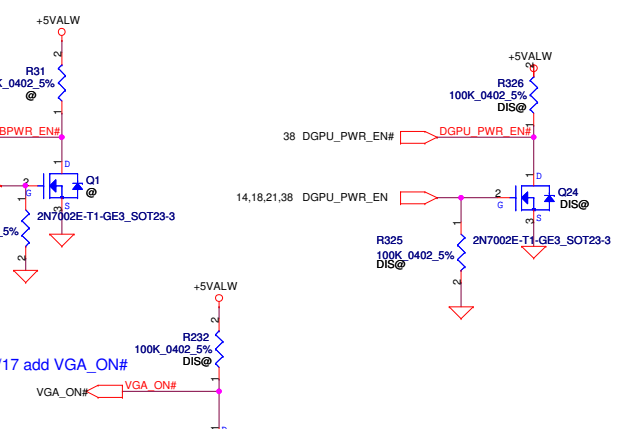
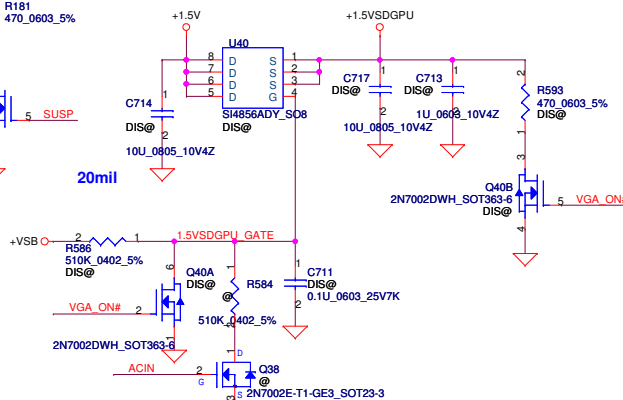


+1.5V to +1.5VS

1211 EMI ADD 0.1U close PJ5

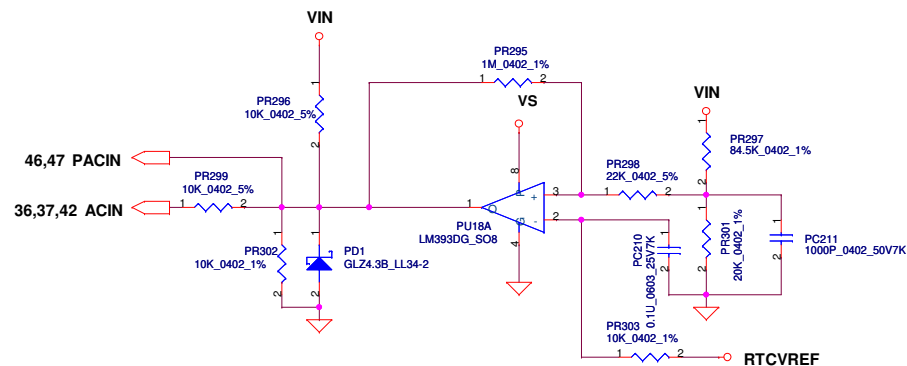


+1.5V to +1.5VSDGPU for GPU

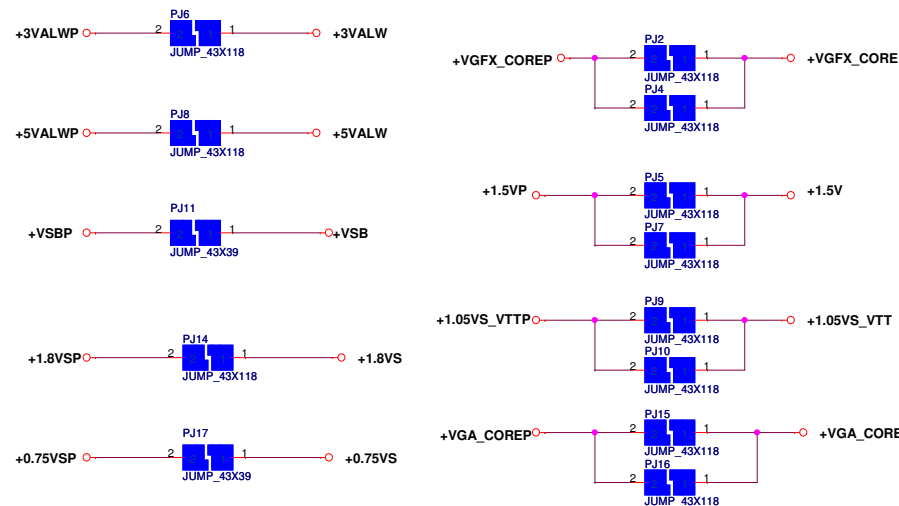


2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge

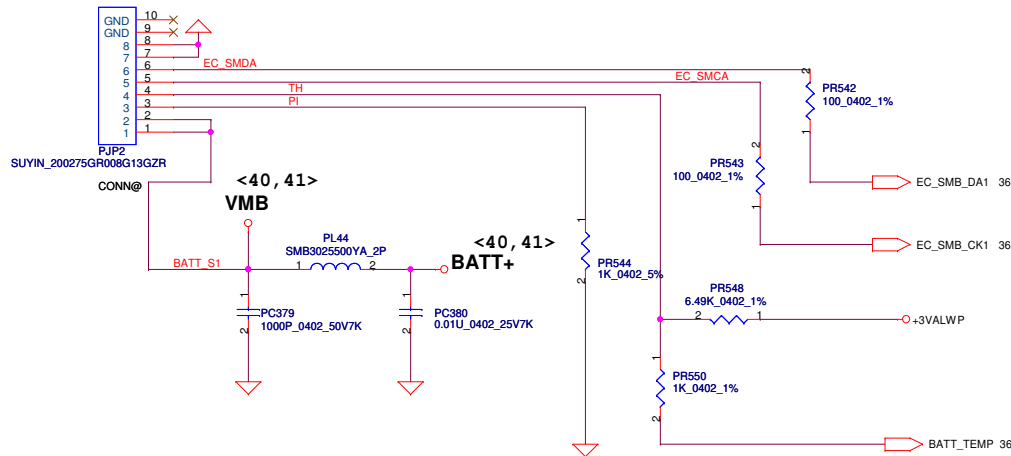
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2008/08/10				Title			
Deciphered Date				2010/08/01				DC Interface			
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				2009/08/17 add VGA_ON#				NEW71/91 M/B LA-5893P Schematic			
				Date: Tuesday, December 22, 2009				Sheet 42 of 56			



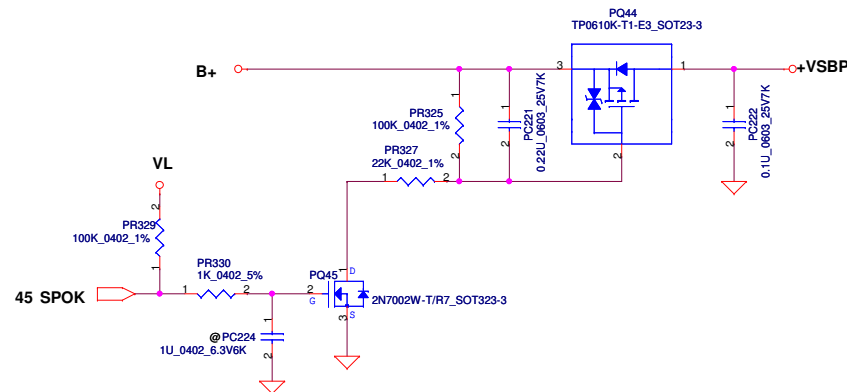
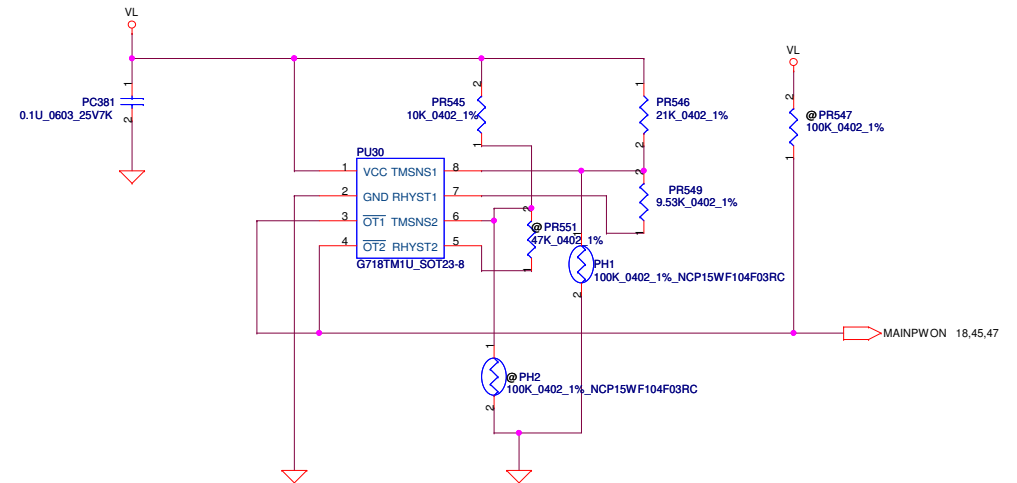
Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



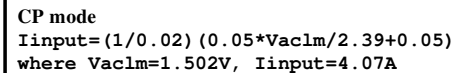
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2007/09/20	Deciphered Date	2010/08/01	Title		
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				Size	Document Number	Rev
				Custom	NEW71	0.1
Date:	Tuesday, December 22, 2009	Sheet	43	of	56	



PH1 under CPU botten side :
CPU thermal protection at 92 degree C



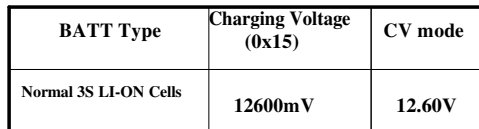
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2007/09/20	Deciphered Date	2010/08/01	
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				BATTERY CONN / OTP	
				Size	Document Number
Custom		NEW71		0.1	
Date:		Tuesday, December 22, 2009	Sheet	44	of 56

$$\begin{aligned} \text{CP} &= 85\% \cdot I_{\text{ada}} ; \text{CP} = 4.07\text{A} \\ \text{CP} &= 85\% \cdot I_{\text{ada}} ; \text{CP} = 2.91\text{A} \end{aligned}$$


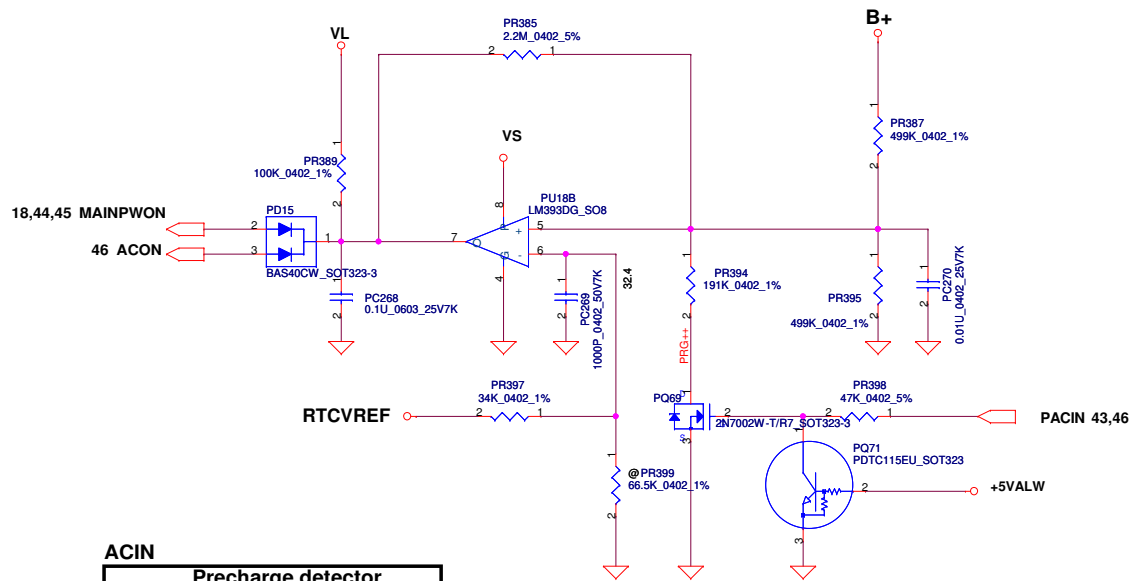
```
Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrg=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrg =>Ki=0.7224
```

```
Kv
Rinternal ic=514K Rec=3K Rl=PR379=15.4K R2=PR381=31.6K
r=514K/31.6K/(15.4K+28K)=11.372K
r=514K/514K/31.6K=28.14K
Vcell=0.175*Vadj3+3.99V
4.2V=0.175*Vadj3+3.99V ==>Vadj=1.2V
Vadj=Vref*(R/(R+S14K))
1.1463=CALIBRATE*0.6046 ==>CALIBRATE=1.899
1.899=(4.2-(Vcell1*A*0.175))*Kv=(4.2-(4.2*A*0.175))*Kv
A=Vref*(R/(R+S14K))=0.052
Kv=9.451
```

```
LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=4.5V
```



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Issued Date	2007/09/20	Deciphered Date	2010/08/01	Title CHARGER	
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				Custom Document Number NEW71	0.1
Date:		Tuesday, December 22, 2009		Sheet	46 of 56

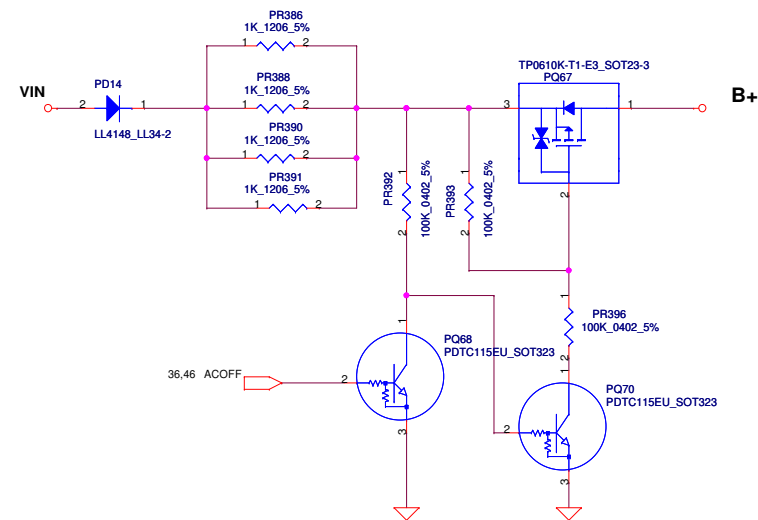


ACIN

Precharge detector			
Min.	typ.	Max.	
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector			
Min.	typ.	Max.	
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



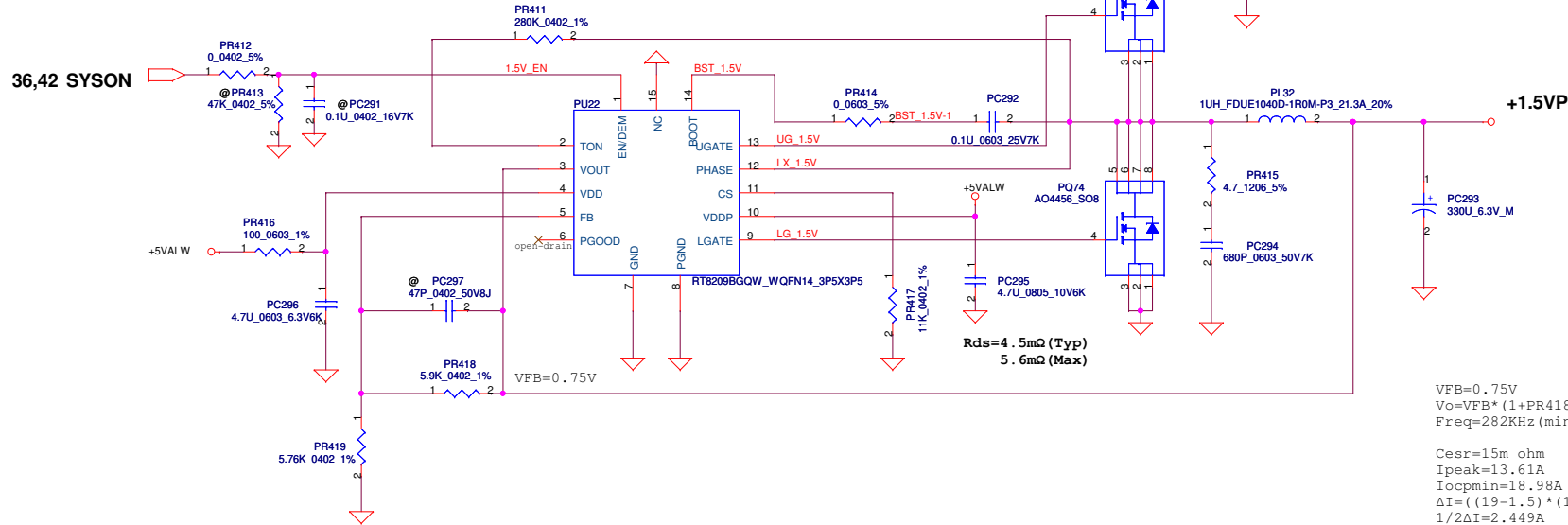
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Issued Date	2007/09/20	Deciphered Date	2010/08/01	Title	PRECHARGE
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				Custom	NEW71
				Date	Tuesday, December 22, 2009
				Sheet	47 of 56
				Rev	0.1



Date:	Tuesday, December 22, 2009	Sheet	48	of	56
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EN_PSV
 1. GND=>Disable SMPS
 2. FLOAT=>PWM_only mode
 3. HIGH=>Auto_skip mode

Because +1.5VSP has 17.74A power budget, it includes
 DDR3, VGA chip, VRAM, so must use molding choke.

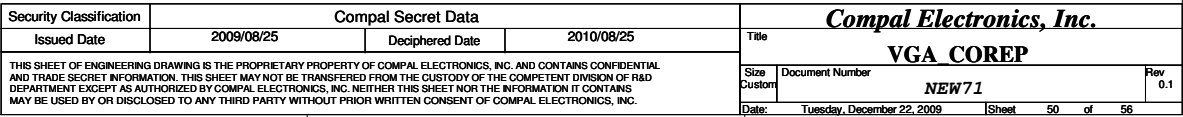


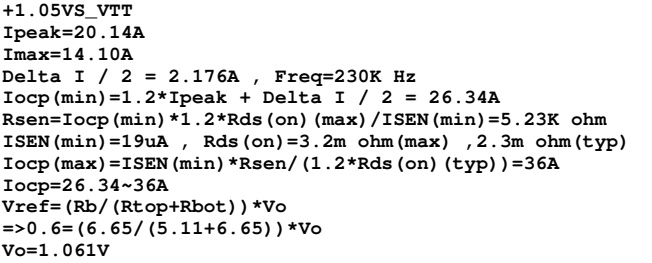
VFB=0.75V
 $V_o = VFB * (1 + PR418 / PR419) = 1.52V$
 Freq=282KHz(min) , 300KHz (typ)

Cesr=15m ohm
 Ipeak=13.61A
 Iocpmin=18.98A
 $\Delta I = ((19 - 1.5) * (1.5 / 19)) / (L * Freq) = 4.899A$
 $1 / 2 \Delta I = 2.449A$

Iocp=18.09A~29.13A

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Issued Date	2008/08/10	Deciphered Date	2010/08/01	Title	
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Size	Document Number	Rev			0.1
Custom	NEW71				
Date:	Tuesday, December 22, 2009	Sheet	49	of	56





hexainf@hotmail.com
GRATIS - FOR FREE

D

A

PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD

ADP3212MNR2G_QFN48_7X17

Place PH1 close to PHASE 1 inductor on the same layer

Avoid high dV/dt

Connect to input caps

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Issued Date	2009/02/04	Deciphered Date	2010/08/01	CPU CORE	
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Size C	Document Number	NEW71/91 M/B LA-5893P Schematic			Date: Tuesday, December 22, 2009
		Sheet	53	of	56

Version change list (P.I.R. List)

Page 1 of 3
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	For BOM unique.	For BOM unique.	0.1	46	Change PD8 from SC1SS355003(S DIO 1SS355) to SC100001K00(DIO 1SS355 SOD323 T/R-5K)	2009-1021	to DVT
2	For BOM unique.	For BOM unique.	0.1	54	Delete PQ86/PQ91 SB00000HL00(S TR TPCA8030-H 1N SOP). Add PQ87/PQ90 SB00000HL00(S TR TPCA8030-H 1N SOP).	2009-1021	to DVT
3	For UMA Arrandale CPU commond design.	For UMA Arrandale CPU, we just only pop 1 HS MOS and 1 LS MOS.	0.1	54	Delete PQ89/PQ93 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
4	For VTT Power rail commond design.	For VTT Power rail commond design, we pop 1 HS MOS and 1LS MOS.	0.1	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
5	CIS link error.	CIS link error.	0.1	54	Change PR500 from SD028100A00(S RES 1/16W 10 +-5% 0402) to SD028100A80(S RES 1/16W 10 +-5% 0402)	2009-1021	to DVT
6	BOM unique.	BOM unique.	0.1	47	Chnage PC265 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
7	BOM unique.	BOM unique.	0.1	49	Chnage PC284 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
8	BOM unique.	BOM unique.	0.1	54	Chnage PC350 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
9	BOM unique.(For Madison/Park SKU)	BOM unique.(For Madison/Park SKU)	0.1	52	Chnage PC367 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
10	BOM unique.	BOM unique.	0.1	46	Change PC225/PC227 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
11	BOM unique.	BOM unique.	0.1	54	Change PC339/PC341 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206) Change PC354/PC355 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
12	+1.05VS_VTTP Cost down 1 LS MOS. HW request.	+1.05VS_VTTP Cost down 1 LS MOS. Because +1.05VS_VTT has voltage drop issue, HW request, remote sense to close to PCH.	0.2	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP) Delete PR471 SD028000080(S RES 0 0402 5%) Delete PR473 from SD034100A80(S RES 10 0402 5%) Add PR564 SD028000080(S RES 1/16W 0 0402 5%)	2009-1029	to DVT
14	Adjust +1.05VS_VTTP OCP.	Because we remove a LS MOS, so OCP must adjust.	0.2	52	Change PR467 from SD000004080(S RES 1/16W 2.2K +-1% 0402) to SD034499180(S RES 1/16W 4.99K 0402 1%)	2009-1029	to DVT
15	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PU19 SA00001NC00 (S IC APL5913-KAC-TRL SO 8P)	2009-1029	to DVT
16	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PR402 SD034150280, PR404 SD034120280.	2009-1029	to DVT
17	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PC273 SE075103K80 PC275 SE000000I10 Delete PC272 SE107475K80, PC271 SE107105M80	2009-1029	to DVT
18	+VGA_COREP, efficiency issue.	Increase Freq, decrease choke, to improve efficiency.	0.2	51	Delete PR401 and PR403 SD028220280, PC274 SE026474K80 Change PR196 from SD034442280 to SD034365280.	2009-1029	to DVT
19	+VGA_COREP, OVP issue.	Becasue if PR199/PR202 pop 0ohm, it will cause OVP when VID change from 00 to 11)	0.2	51	Change PL14 from SL200000V00 to SH000005680 Change PR199/PR202 from SD028000080 to SD028100280 (S RES 1/16W 10K 0402 5%)	2009-1029	to DVT
20	+VGA_COREP, cost issue.	Cost down.	0.2	51	Change PQ75/PQ78 from SB00000GL00(S TR TPCA8028-H 1N SOP) to SB000009F80(S TR AO4456 1N S08)	2009-1029	to DVT
21	+VGA_COREP, satndard design.	+VGA_COREP, satndard design, pop 1HS MOS and 2LS MOS, so remove one HS MOS PQ79.	0.2	51	Delete PQ79 SB000008L80 (S TR SI7686DP-T1-E3 1N POWERPAK S08)	2009-1029	to DVT
22	+GFX_COREP, spike issue.	Because +GFX_COREP has spike voltage issue, add schottky diode across GFXVR_EN and VS_ON to solve it.	0.2	51	Add PD17 SCS00000Z00 (S SCH DIO RB751V-40 SOD-323)	2009-1029	to DVT
23	+VGA_COREP, OCP caaculation erroe issue.	Because VGA_CORE has 2 LS MOS, APW7138 detect LS Rdson, so when caculate OCP, Rdson must reduce 1/2.	0.2	51	Change PR190 from SD034649180 to SD034511180 (S RES 1/16W 5.11K 0402 1%)	2009-1029	to DVT

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				Date:	Tuesday, December 22, 2009
				Sheet	54 of 56
				Rev	0.1

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				Size	Document Number
				Custom	NEW71/91 M/B LA-5891P Schematic
Date:		Friday, December 18, 2009		Sheet	55 of 56

PCB
ZZZ
LA-5893P REV0 M/B

ZZZ1
X7621@
X76198BOL21
ALT. GROUP PARTS 1G SAM

ZZZ2
X7622@
X76198BOL22
ALT. GROUP PARTS 1G HYN

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				Size Custom	Document Number NEW70 M/B LA-5891P Schematic
				Date: Monday, December 21, 2009	Rev 0.1
				Sheet 56 of 56	