

ZZZ8
DAZ@
DAZ04300100
PCB

ZZZ1
DA2@
MAIN BOARD
DA600007E10
PCB

ZZZ2
DA2@
E board
DA40000A910
PCB

ZZZ3
DA2@
FP board
DA600007D10
PCB

ZZZ4
DA2@
Function board
DA40000AA10
PCB

ZZZ5
DA2@
USB board
DA40000AB10
PCB

ZZZ6
DA2@
IO board
DA40000AC10
PCB

ZZZ7
DA2@
Power board
DA40000AD10
PCB

Compal Confidential

KAQB0 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2009-03-27

REV:1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2007/09/29	Deciphered Date	2007/09/29	Title	SCHEMATIC, MB A5011
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Model Name : KAQB0

File Name : LA5011P

P/N:DA60000B110

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LVDS

multiplex
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LVDS

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C-Link

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LS-501A
HDMI board
7318 Level shift
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PCI-Express

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New Card
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power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +1.8VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

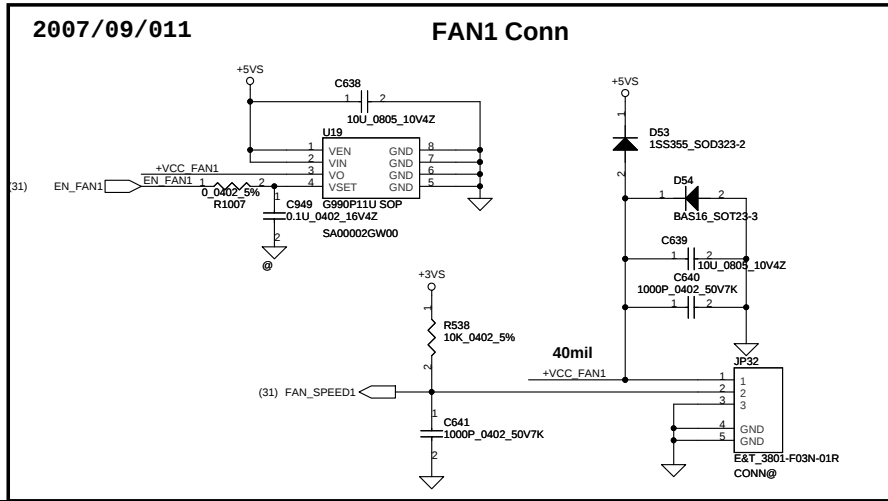
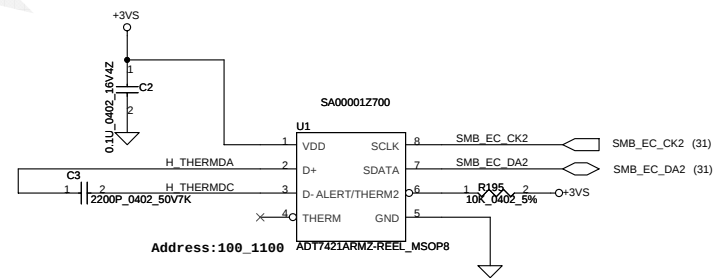
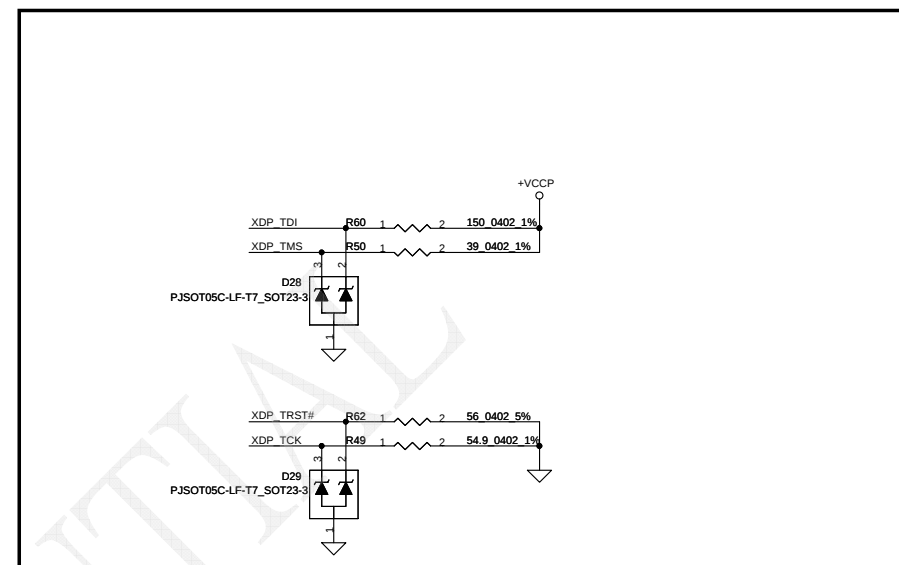
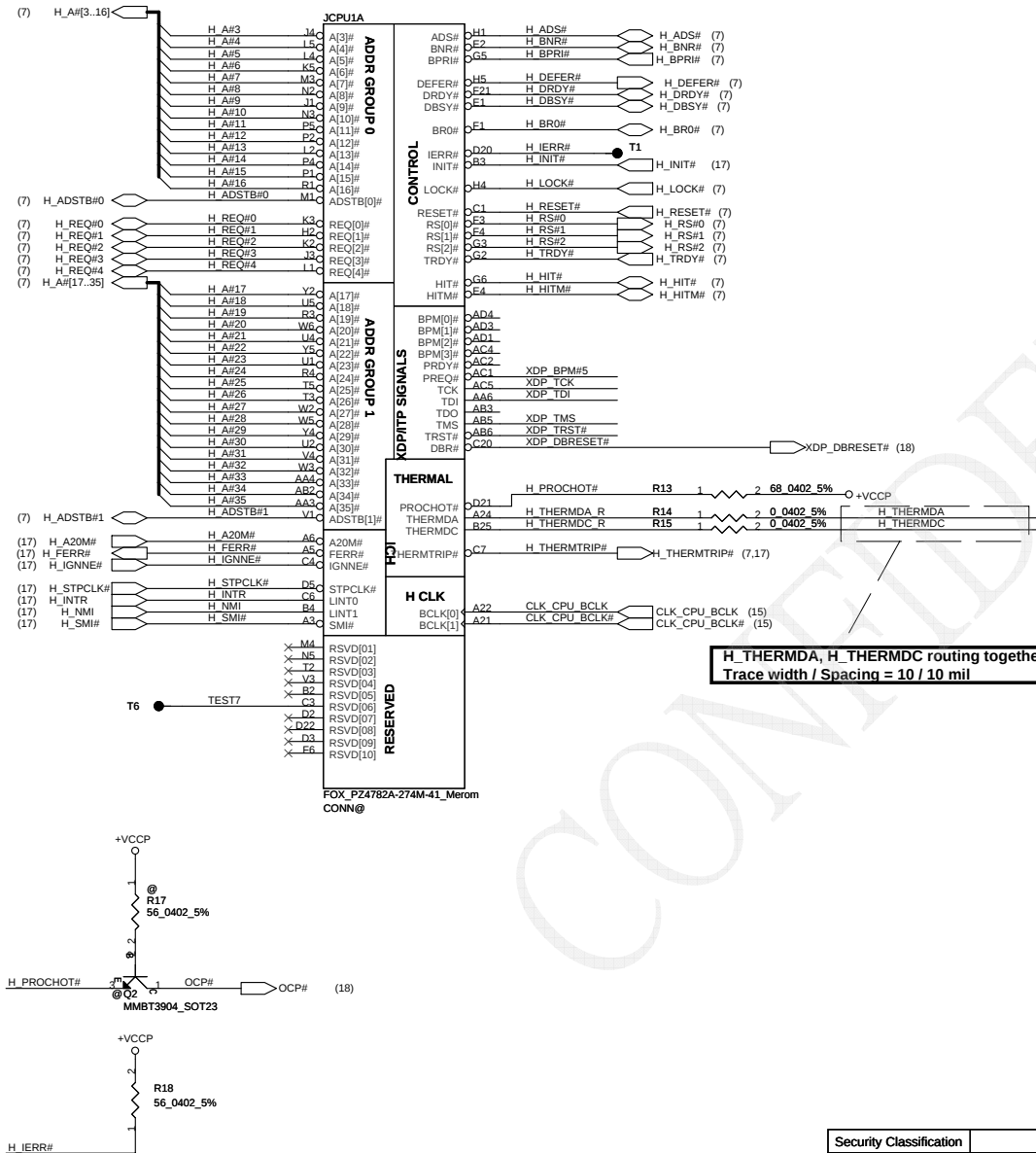
@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

SMBUS Control Table

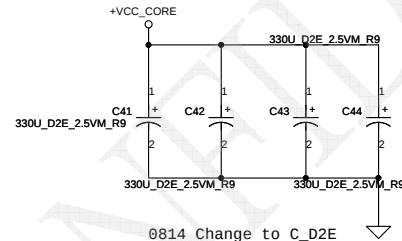
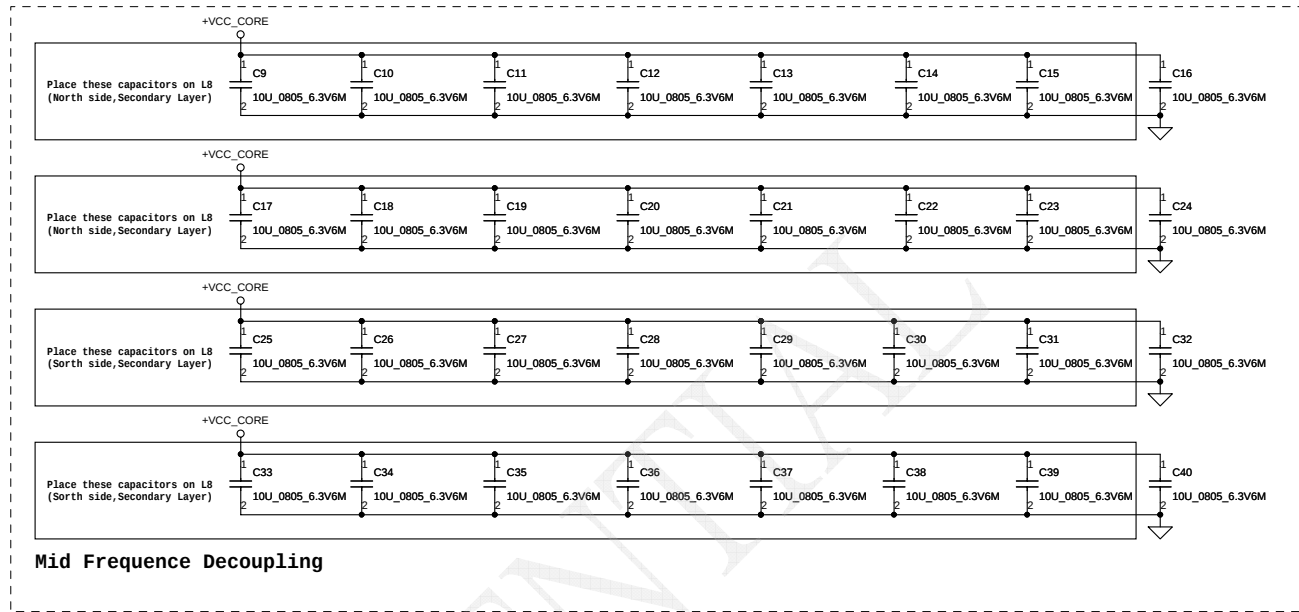
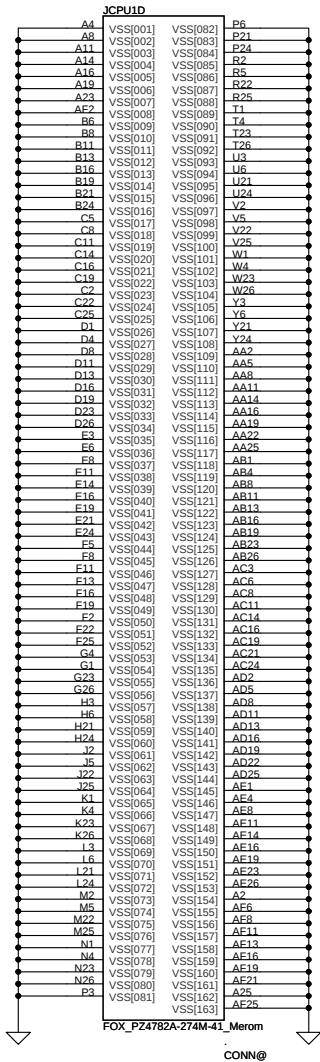
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

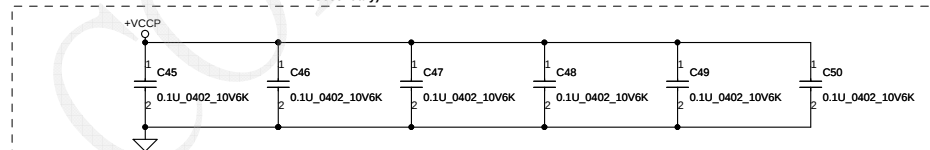
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010



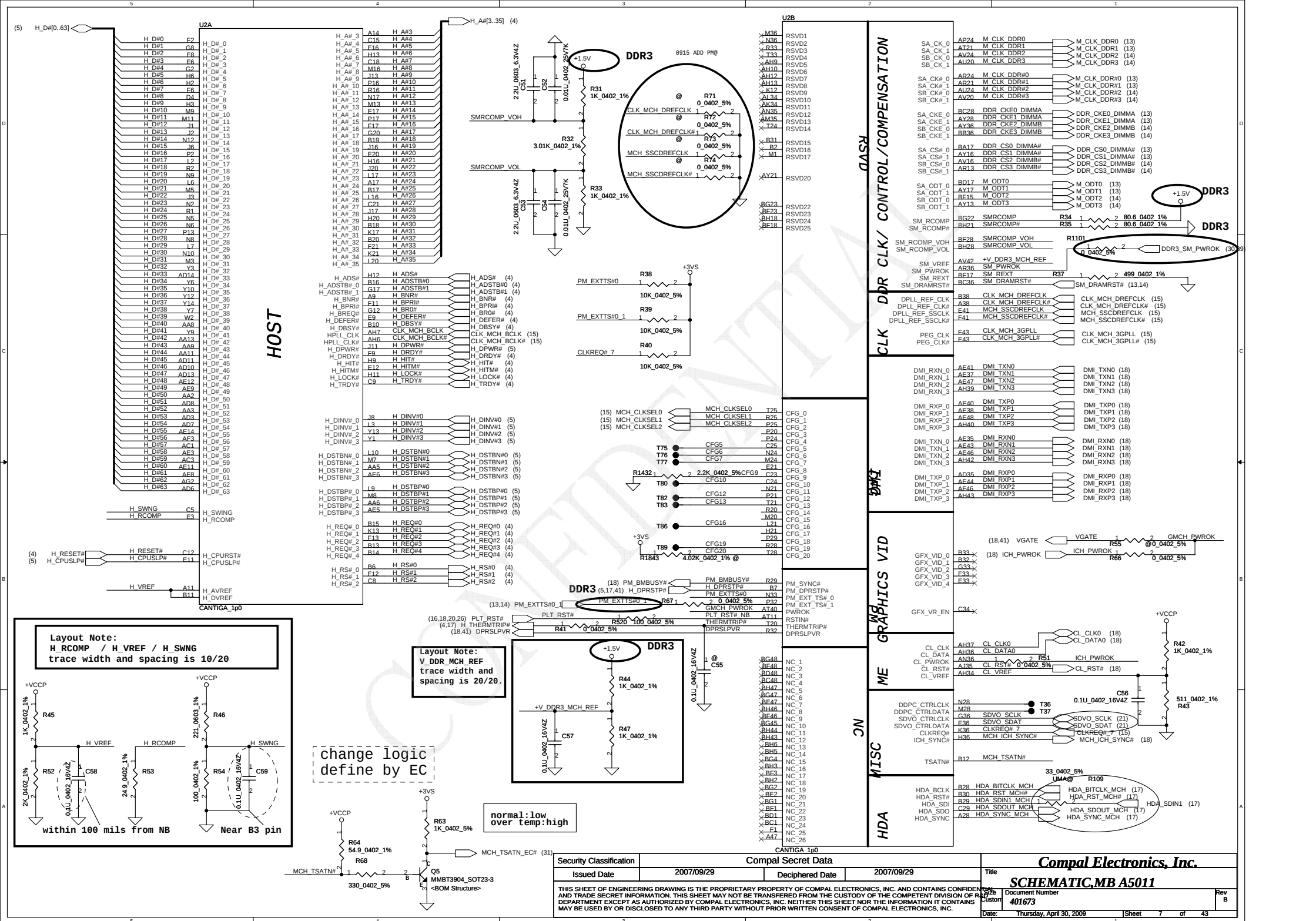
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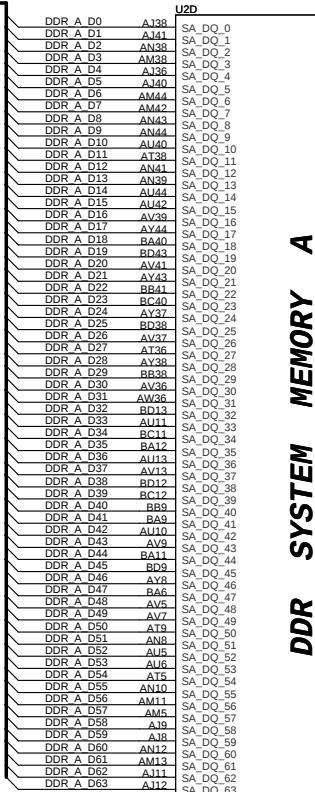
Place these inside socket cavity on L8 (North side Secondary)



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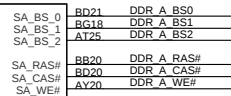


(13) DDR_A_D[0..63]

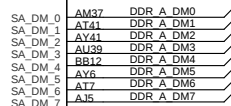


DDR SYSTEM MEMORY A

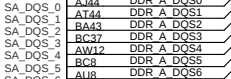
CANTIGA_1p0



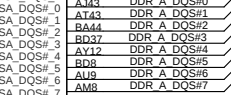
DDR_A_DM[0..7] (13)



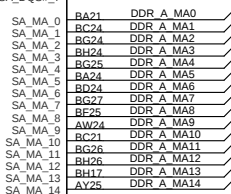
DDR_A_DQS[0..7] (13)



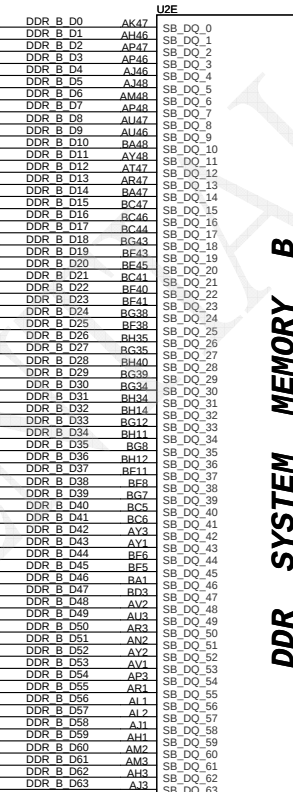
DDR_A_DQS#[0..7] (13)



DDR_A_MA[0..14] (13)

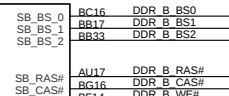


(14) DDR_B_D[0..63]

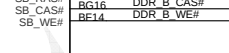


DDR SYSTEM MEMORY B

CANTIGA_1p0



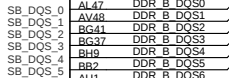
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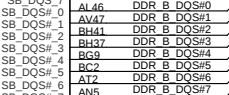
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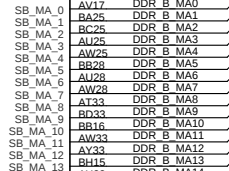
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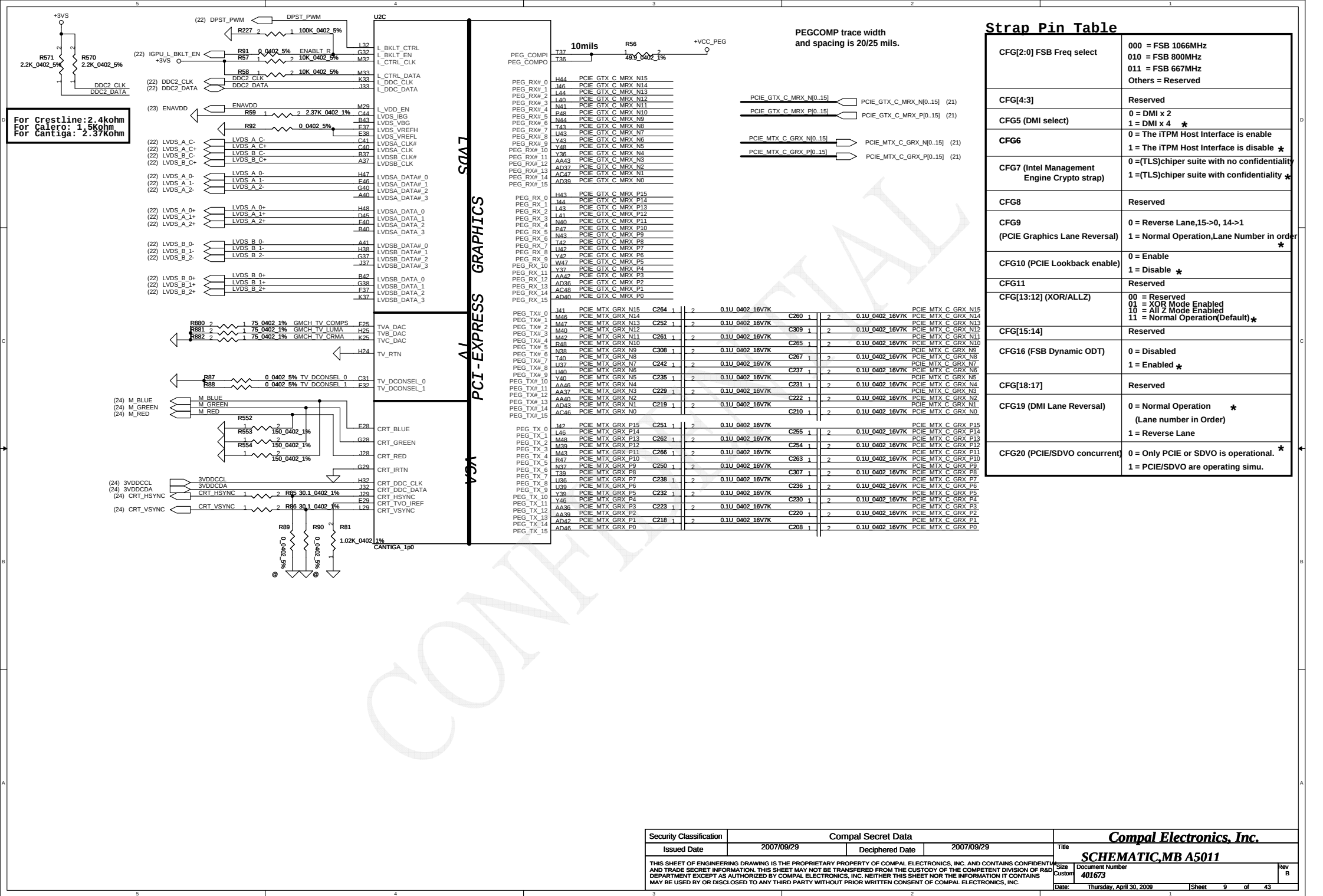


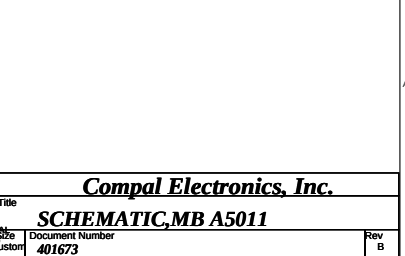
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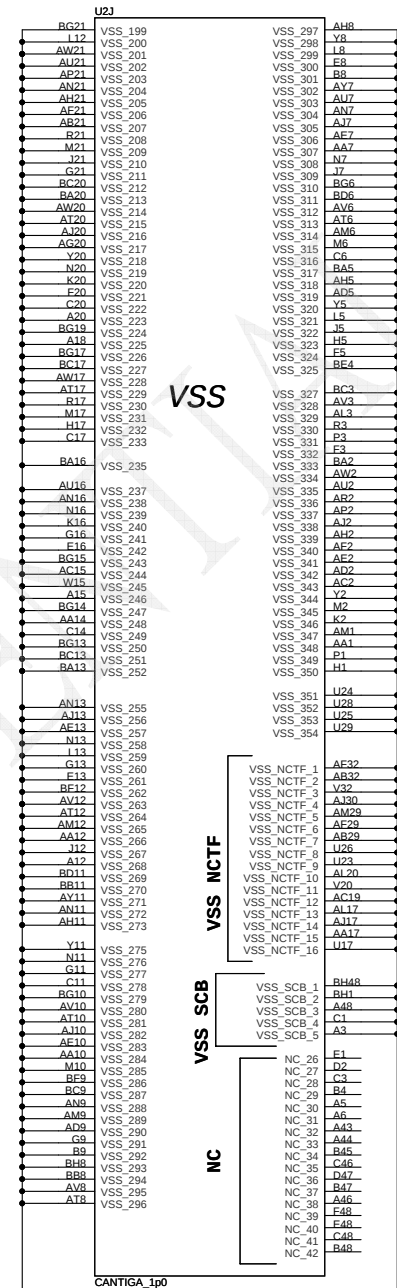
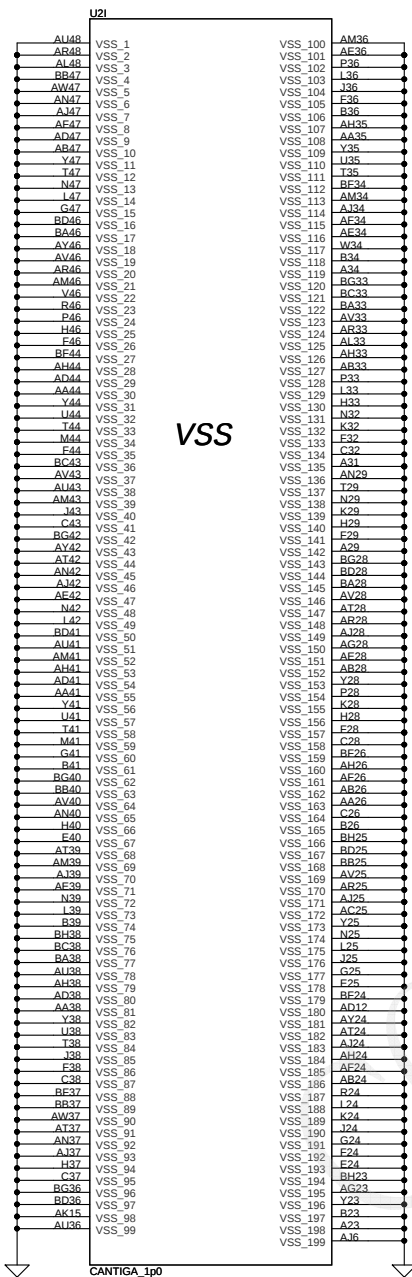


DDR_B_MA[0..14] (14)

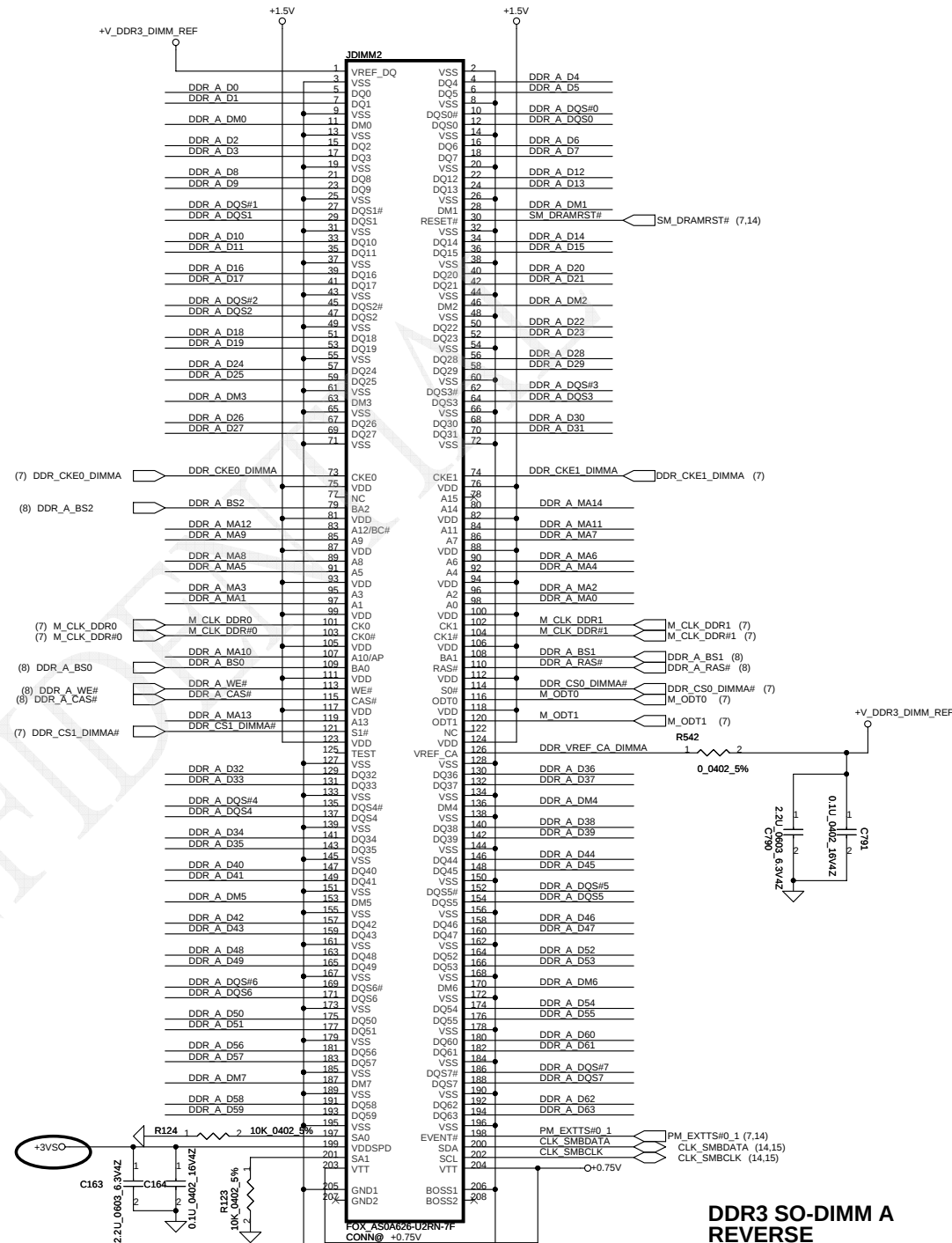
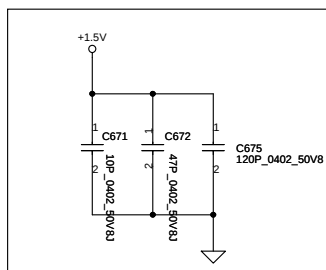
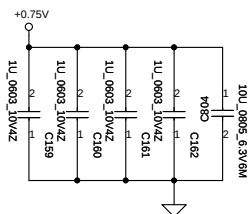
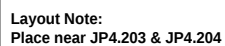
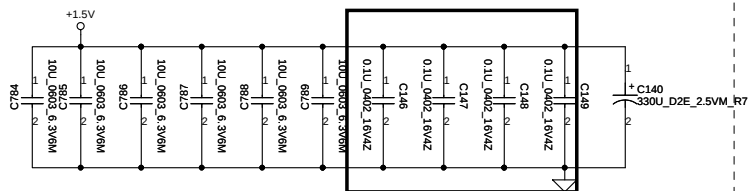
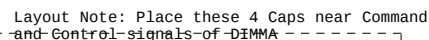
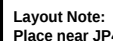
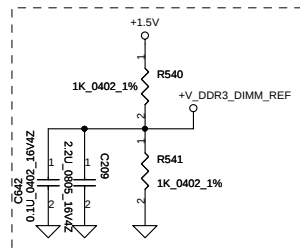




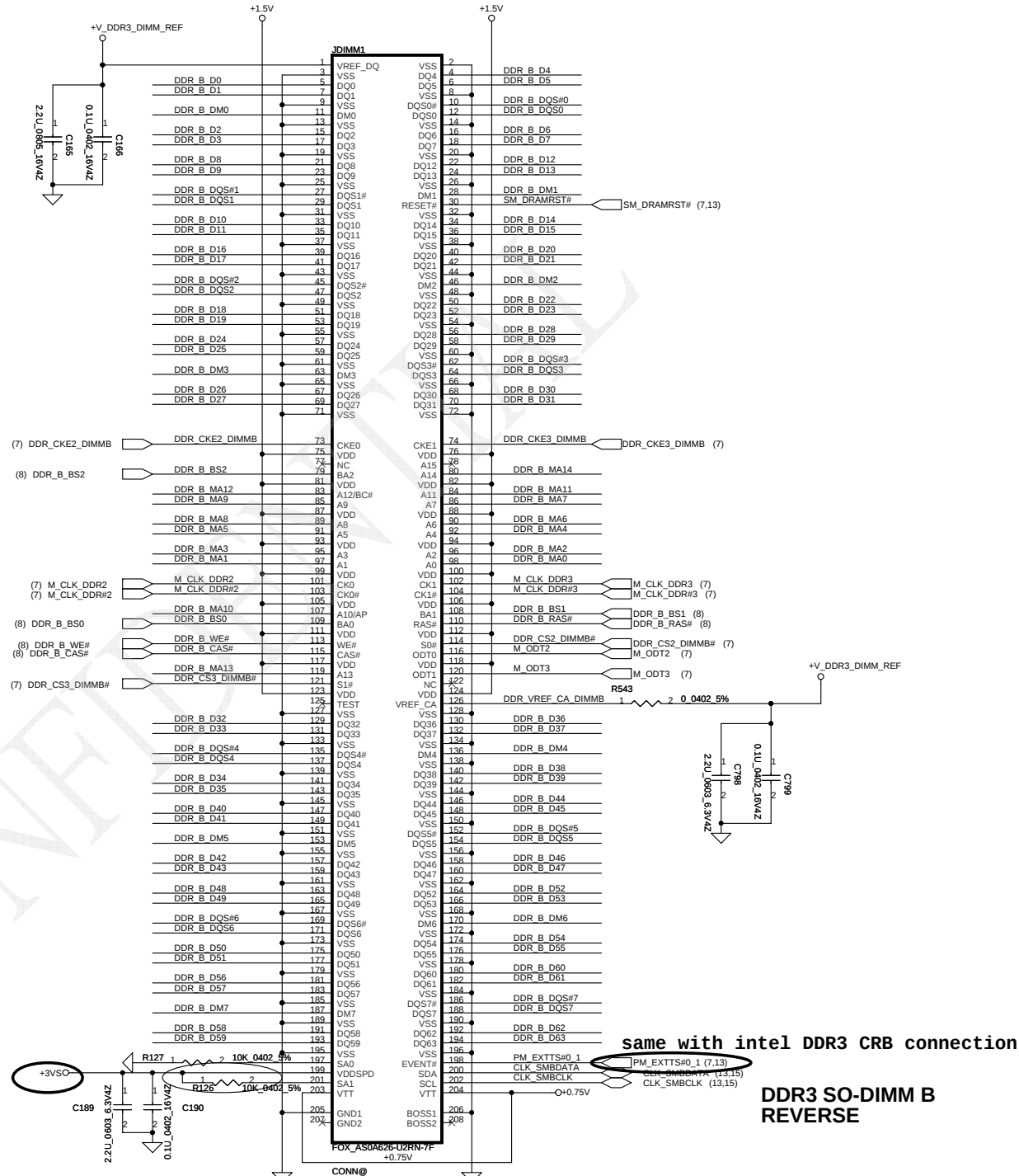
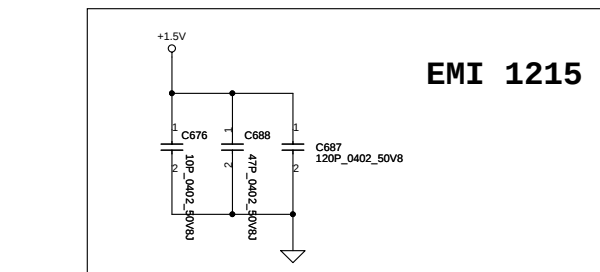
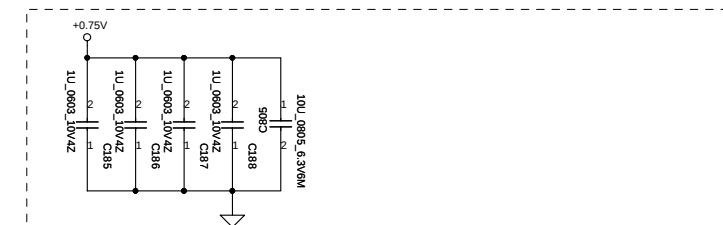
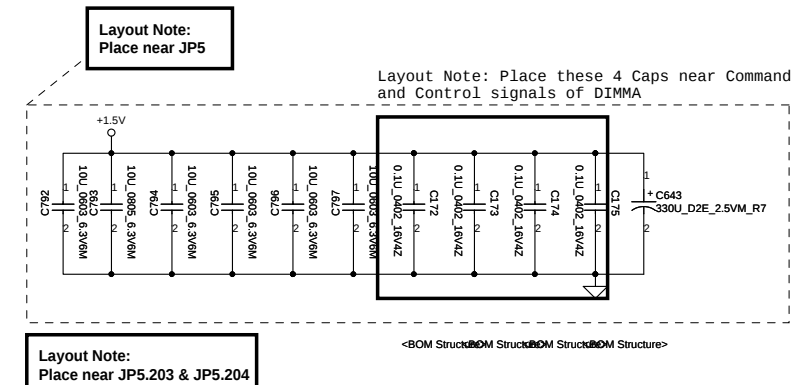
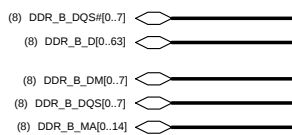




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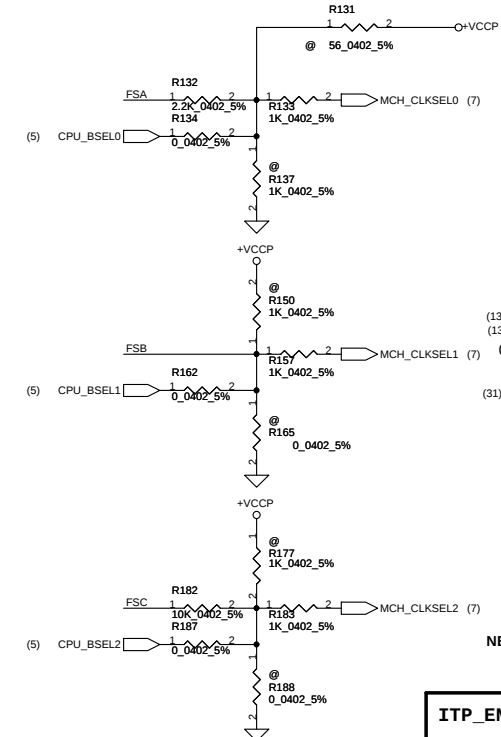
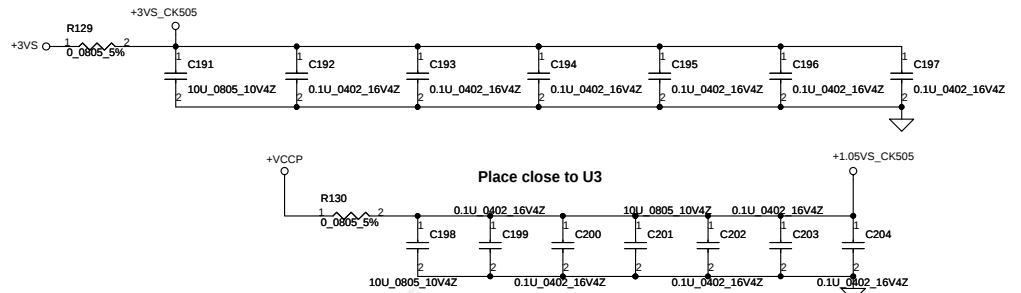
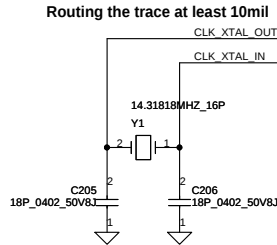


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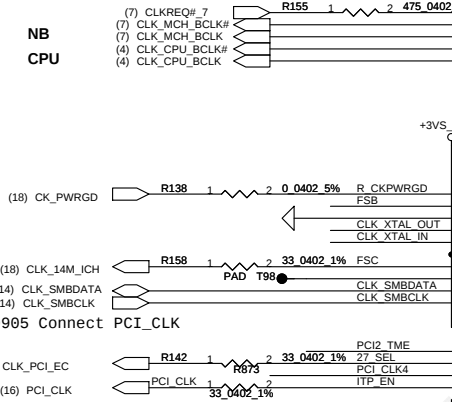


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FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHZ	MHZ	MHZ	MHZ	MHZ	MHZ
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



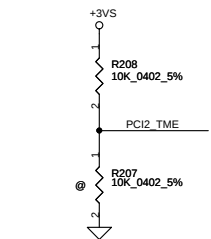
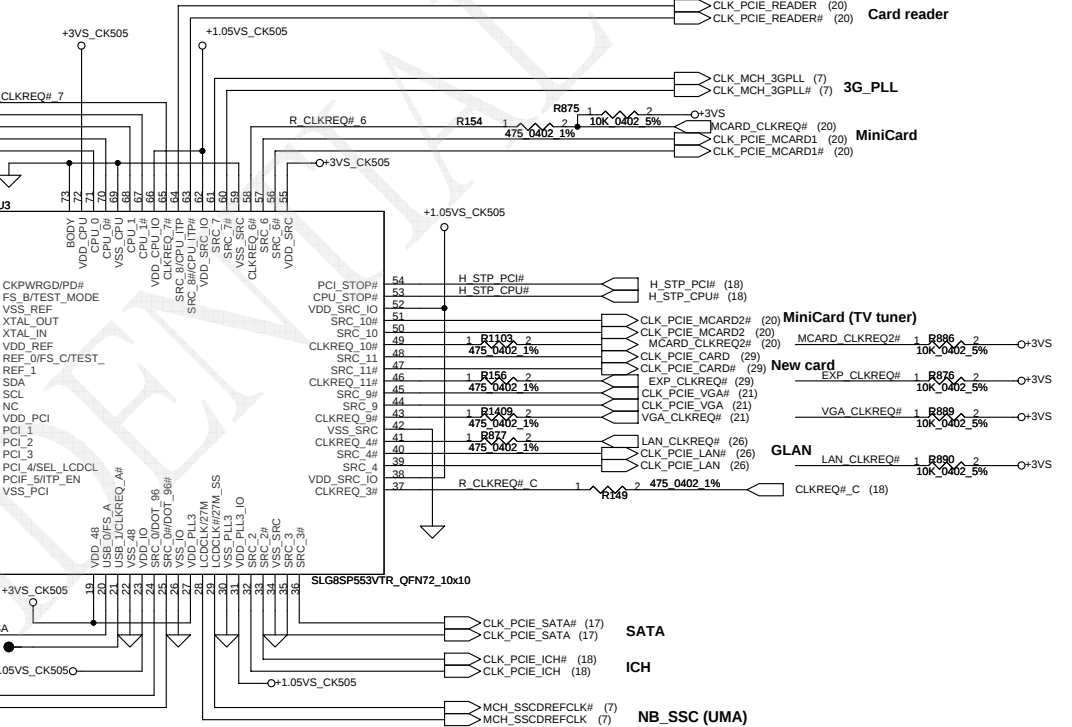
NB
CPU



NB (UMA)

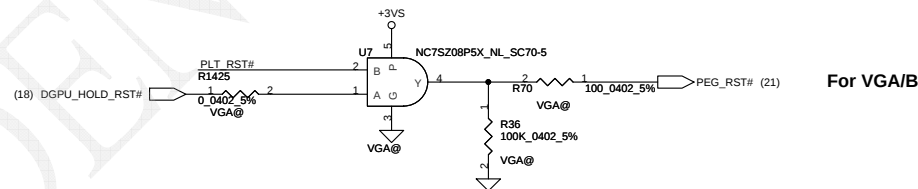
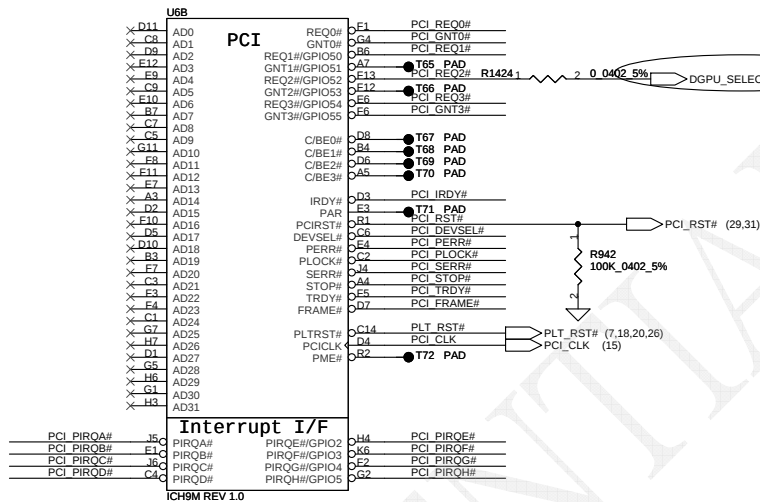
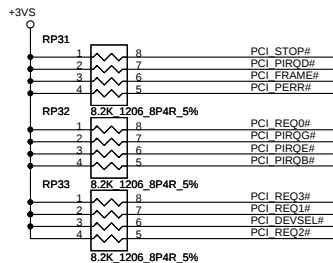
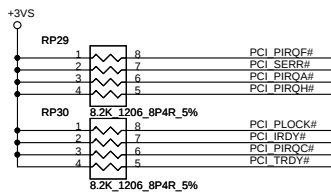
(7) CLK_MCH_DREFCLK#
(7) CLK_MCH_DREFCLK#

ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
PCI_CLK3	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)

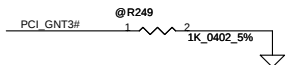


for ICS Overclocking setting
0=Overclocking of CPU and SRC allowed
1=Overclocking of CPU and SRC NOT allowed

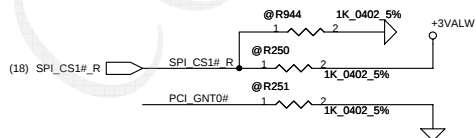
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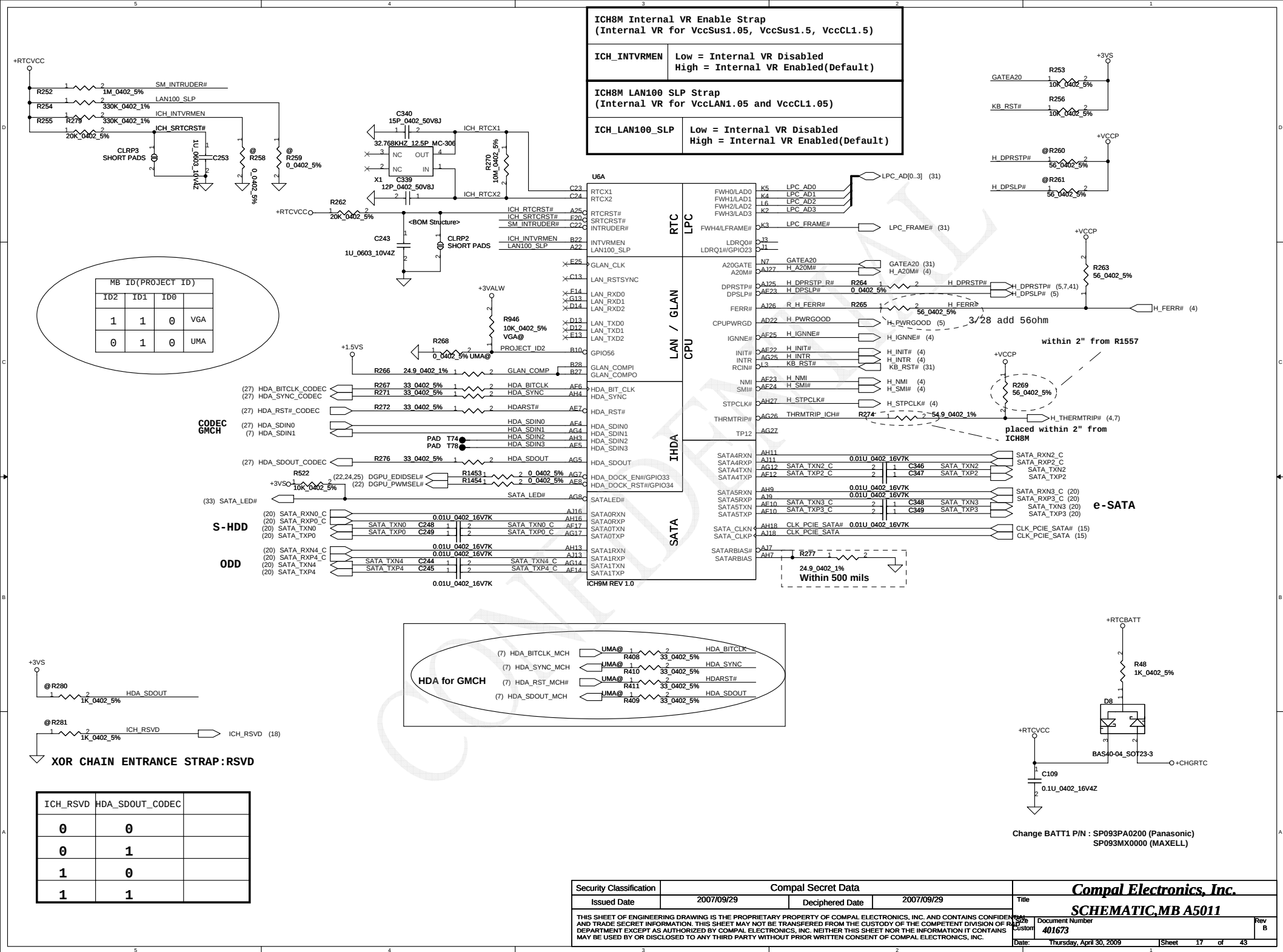


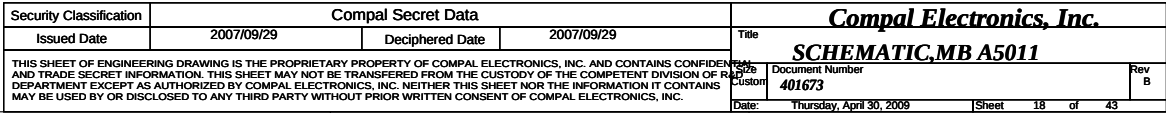
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *

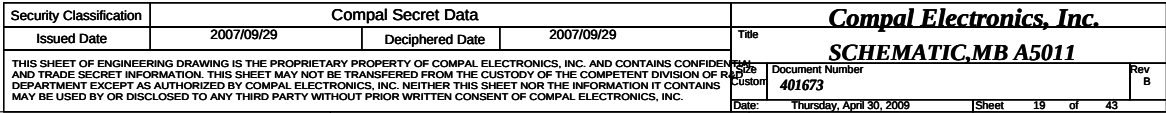


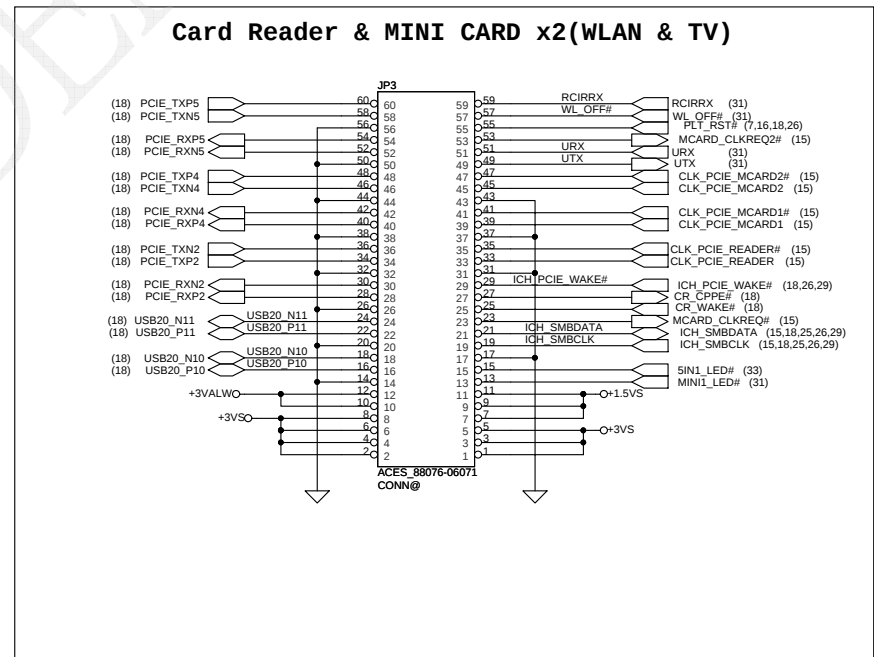
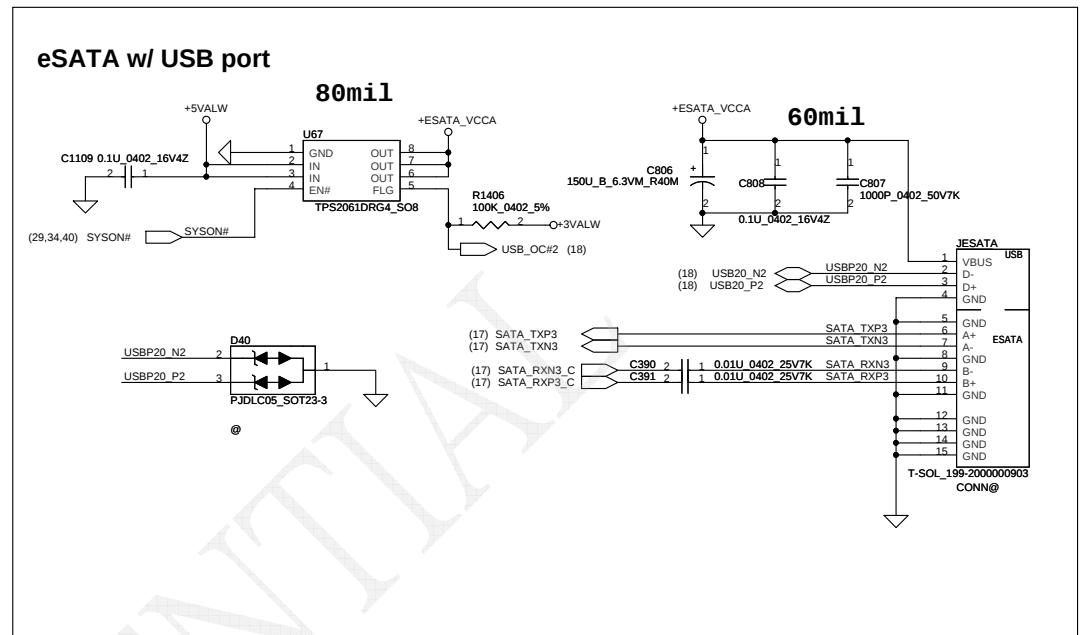
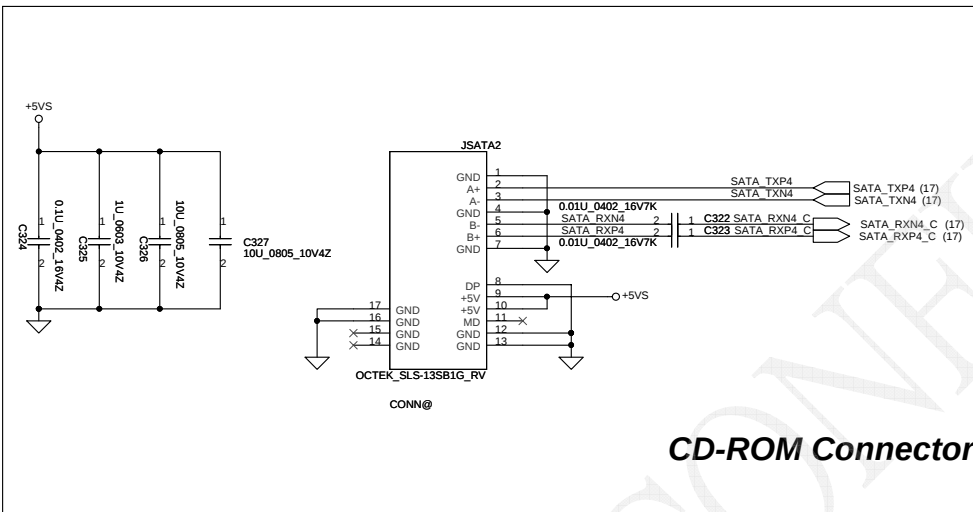
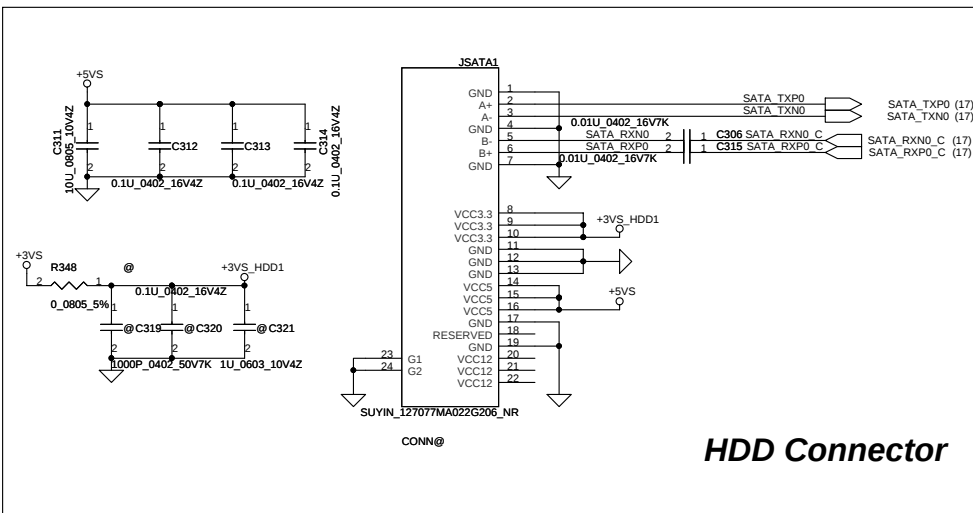
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



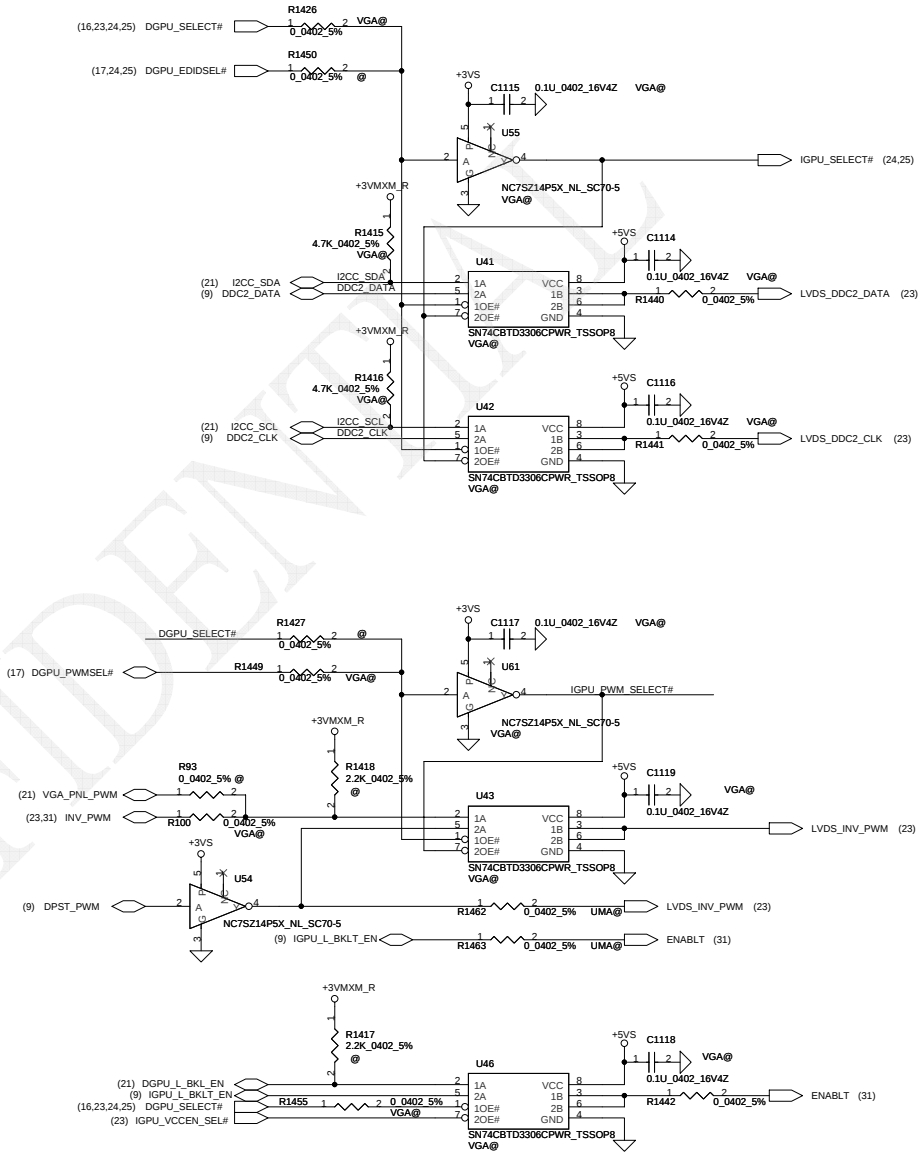
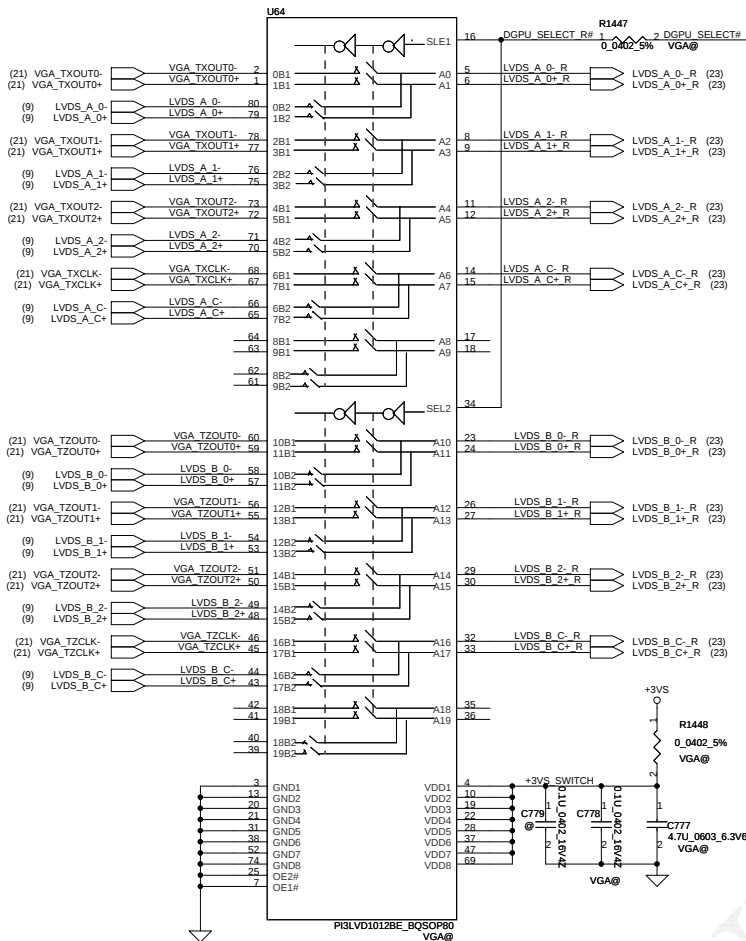






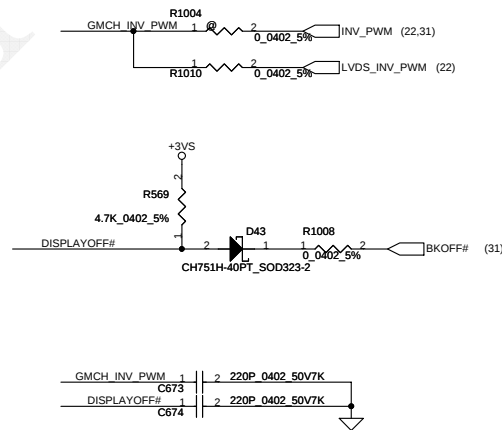
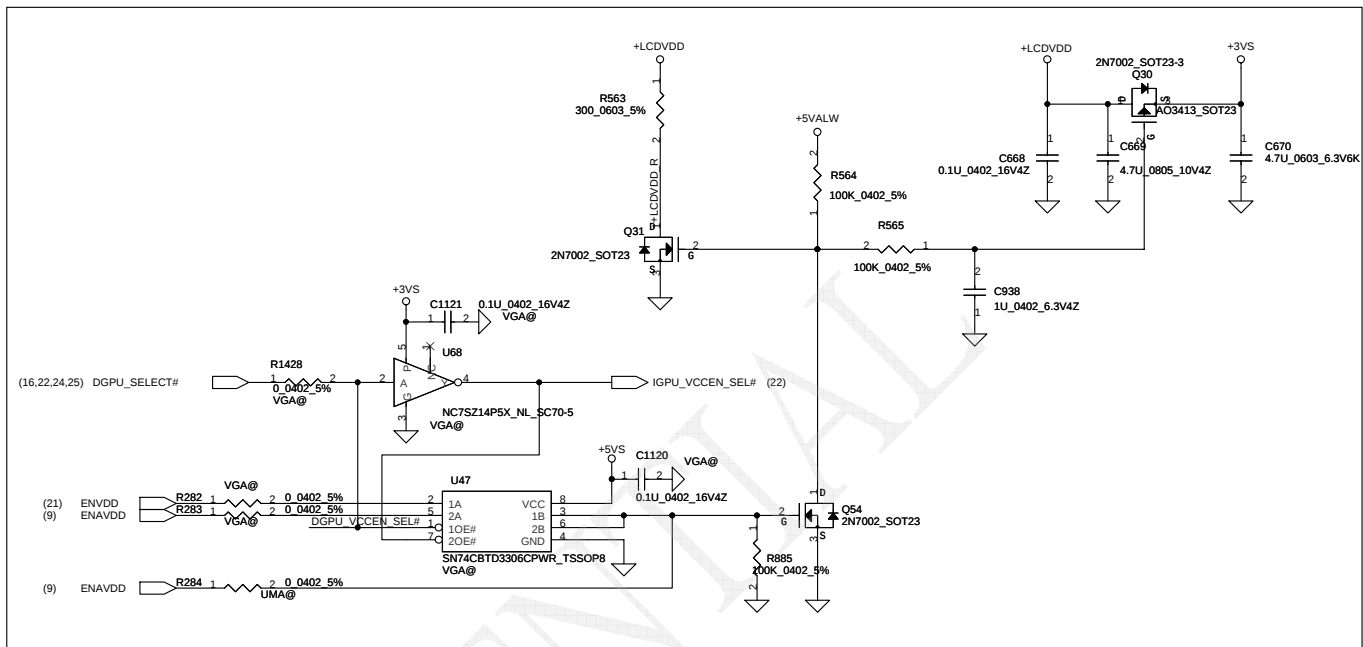
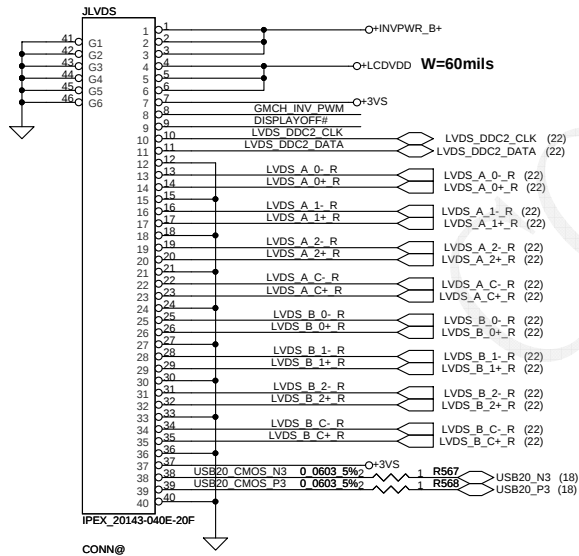
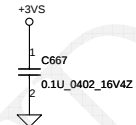
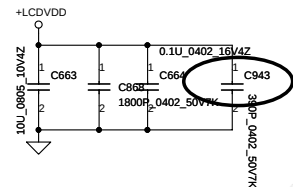
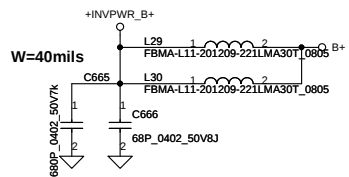


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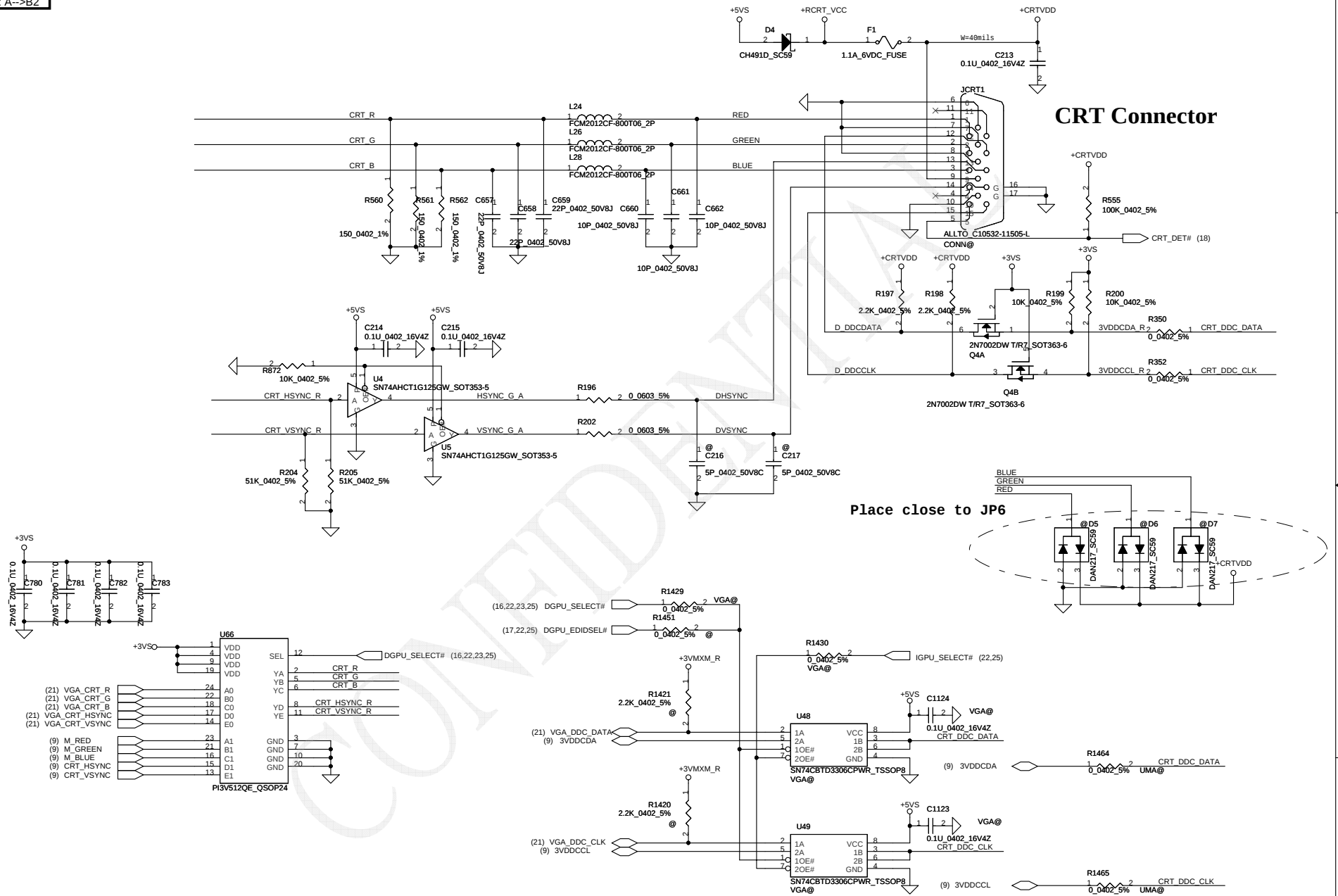
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				SCHEMATIC, MB A5011	
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LVDS and USB CAM connector

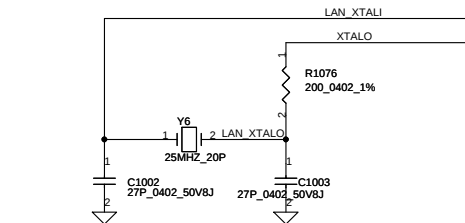
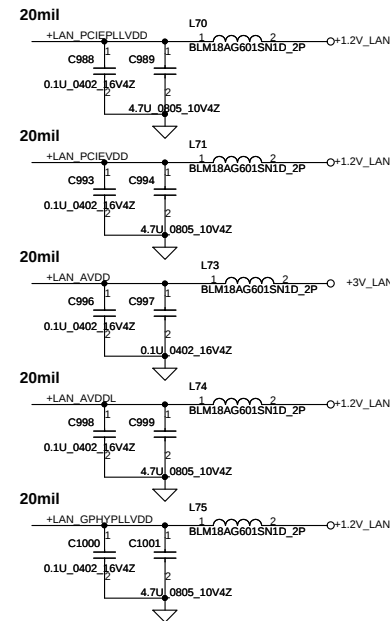
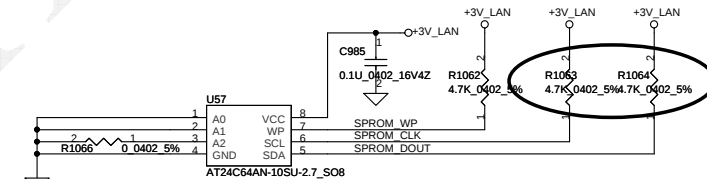
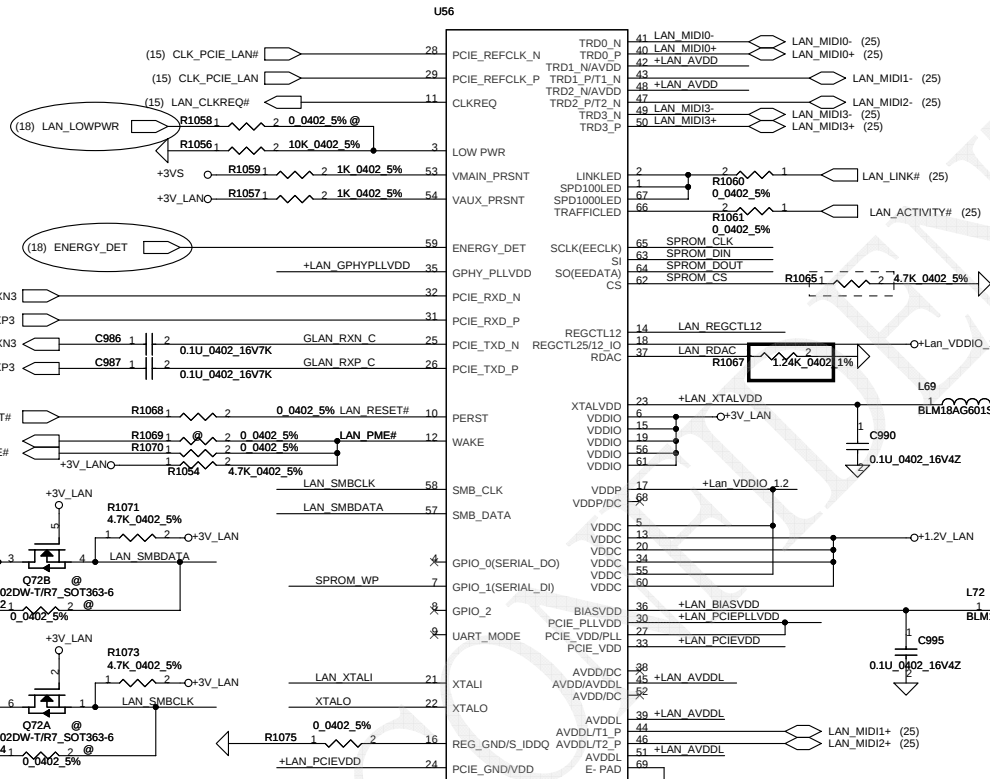
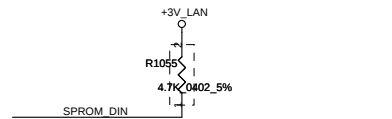
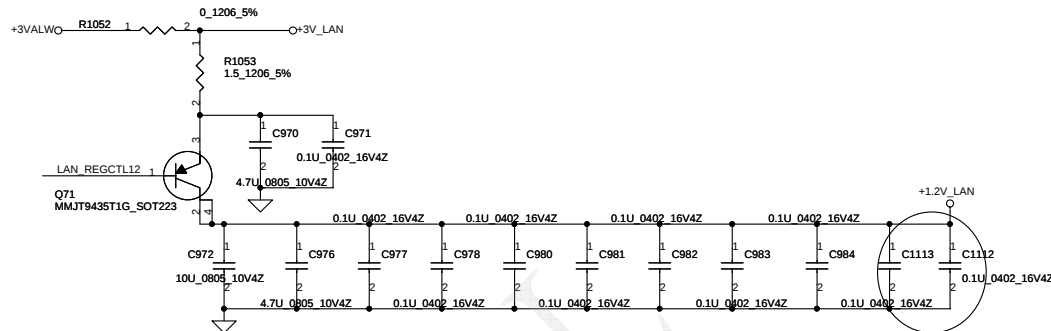
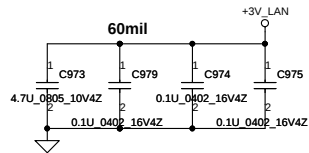


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NOTE: L : $A \rightarrow B_1$
H: $A \rightarrow B_2$

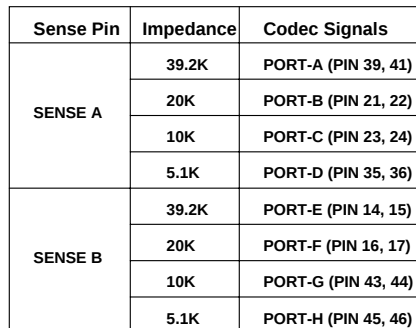


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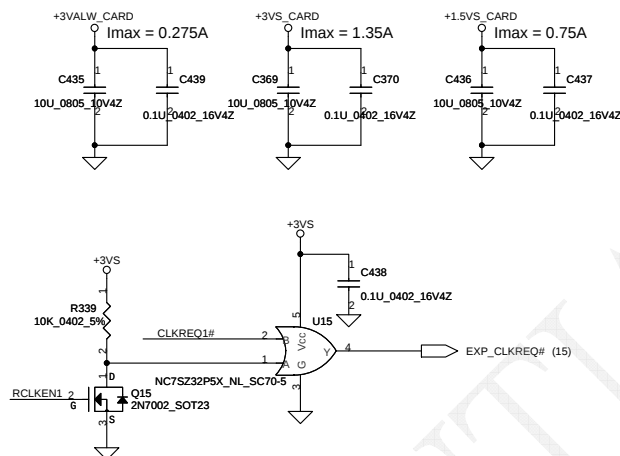
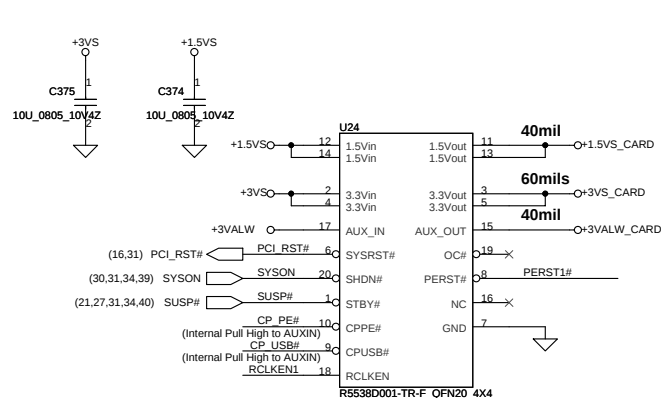
Place closed to Pin2 & Pin59

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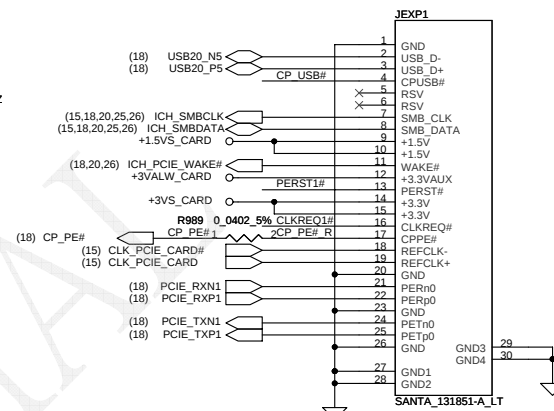


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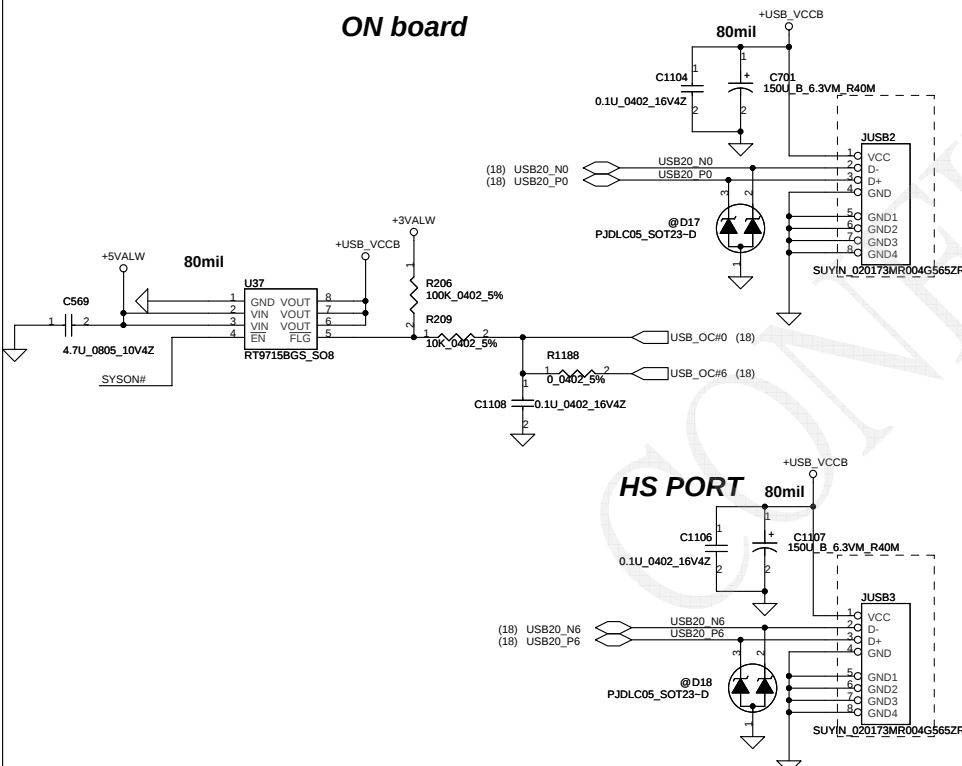
New Card Power Switch



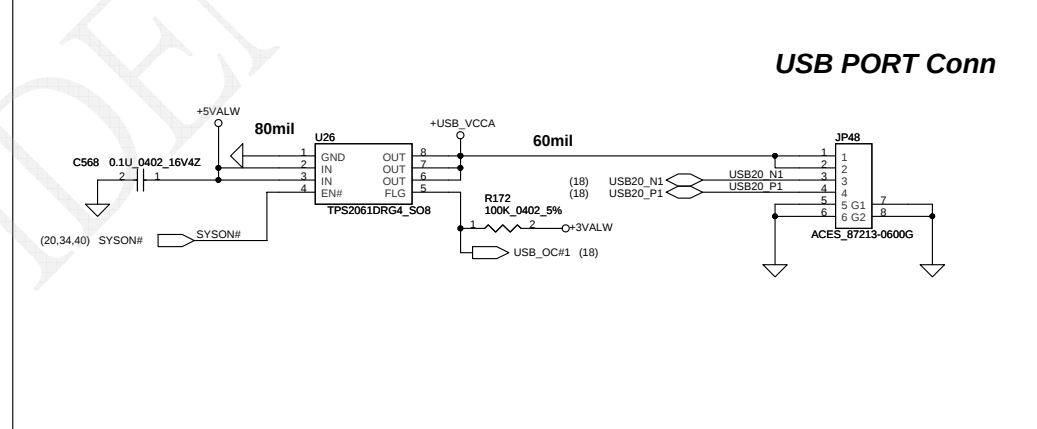
New Card Socket (Left/TOP)



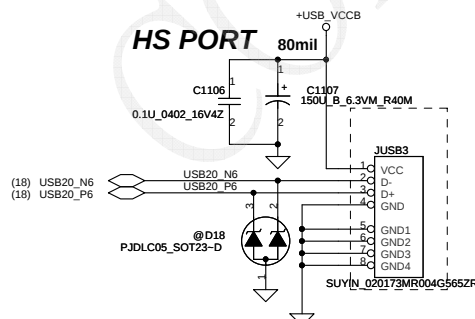
ON board



USB PORT Conn

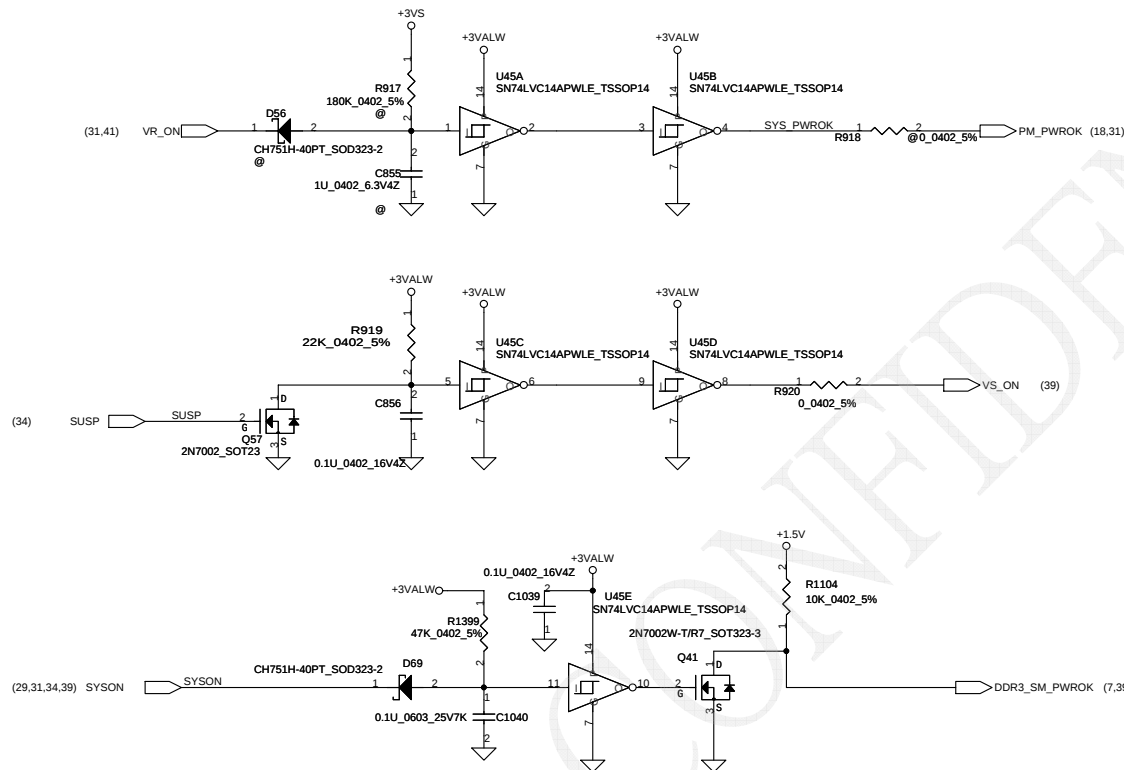
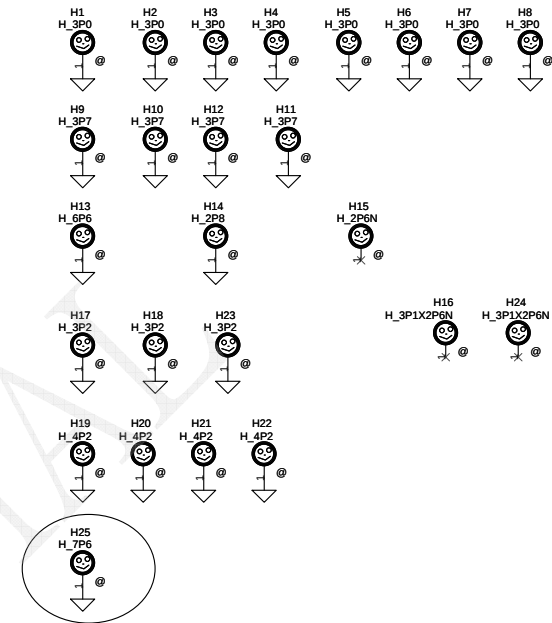
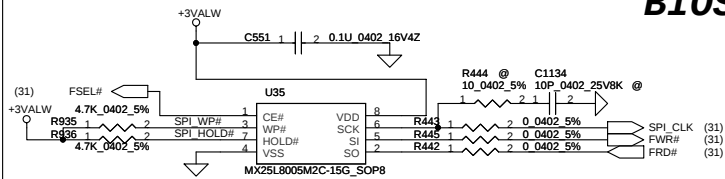


HS PORT

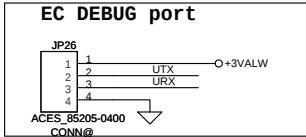


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BIOS



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VCC	3.3V+/-5%				
Ra	100K+/-5%				
Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	
0		0V	0V	0.155V	
1	8.2K+/-5%	0.168V	0.250V	0.362V	
* 2	18K+/-5%	0.375V	0.503V	0.621V	
3	33K+/-5%	0.634V	0.819V	0.945V	
4	56K+/-5%	0.958V	1.185V	1.359V	
5	100K+/-5%	1.372V	1.650V	1.838V	
6	200K+/-5%	1.851V	2.200V	2.420V	
7	NC	2.433V	3.300V	3.300V	

TP CLK R462 1 2 4.7K 0402 5% +5VS

TP DATA R463 1 2 4.7K 0402 5%

F LPC ROM

The diagram shows a horizontal line representing the chip's pins. Pin 1 is on the left, connected to +5VALWO. Pin 2 is in the middle, connected to EC RCIRRX. Pin 13 is on the right, connected to RCIRRX (20). A resistor R213 (10K_0402_5%) is connected between pins 1 and 2. A diode D13 is connected between pins 2 and 13, with the cathode towards pin 2.

CH751H-40PT_S0P323-2

For EMI

CP1

KSO0 1 8
KSO1 2 7
KSO2 3 6
KSO3 4 5

100P, 1206, 8P4C, 50V8

CP2

KSIO 1 8
KSII 2 7
KSIZ 3 6

100P, 1206, 8P4C, 50V8

Figure 1: Pin connections of the 100P_1206_8P4C_50V8. The diagram shows two 8-pin packages. The left package is labeled '100P_1206_8P4C_50V8' and has pins KSO0 to KSO7. The right package is labeled '100P_1206_8P4C_50V8' and has pins KS04 to KS07. The left package has pins G1 and G2, and the right package has pins CP3 and CP4. The diagram shows the following connections: KSO0 to KS04, KSO1 to KS05, KSO2 to KS06, KSO3 to KS07, KSO4 to KS04, KSO5 to KS05, KSO6 to KS06, KSO7 to KS07. The left package has pins G1 and G2, and the right package has pins CP3 and CP4. The diagram shows the following connections: G1 to CP3, G2 to CP4. The diagram shows the following connections: KSO0 to KS04, KSO1 to KS05, KSO2 to KS06, KSO3 to KS07, KSO4 to KS04, KSO5 to KS05, KSO6 to KS06, KSO7 to KS07. The left package has pins G1 and G2, and the right package has pins CP3 and CP4. The diagram shows the following connections: G1 to CP3, G2 to CP4.

P VIEW

100P_1206_8P4C_50V8

CP5

KS08	1	8
KS09	2	7
KS10	3	6
KS11	4	5

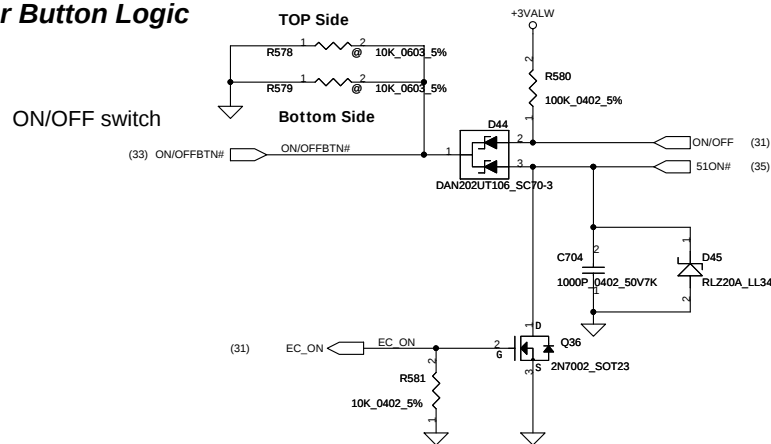
100P_1206_8P4C_50V8

CP6

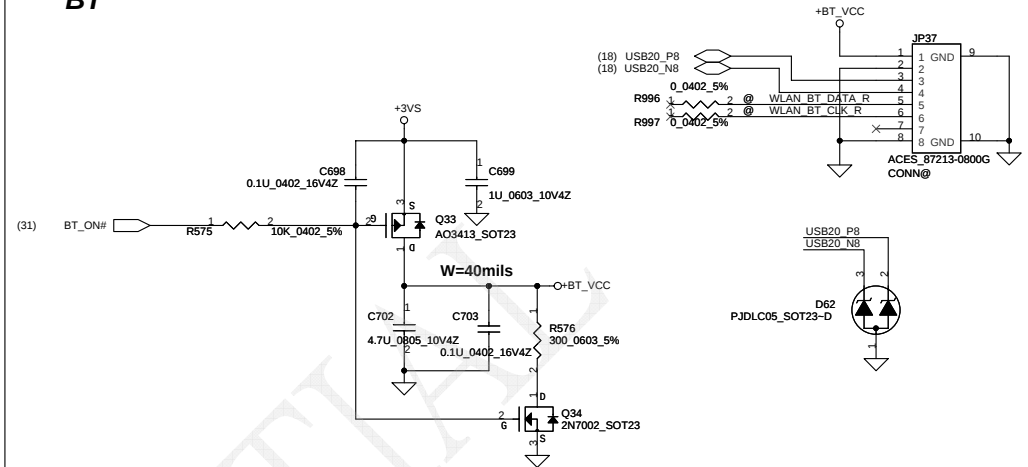
KS012	1	8
KS013	2	7
KS014	3	6
KS015	4	5

(Right)	ACES_88747-2601	100F-1200-8F-AC-SUVS	
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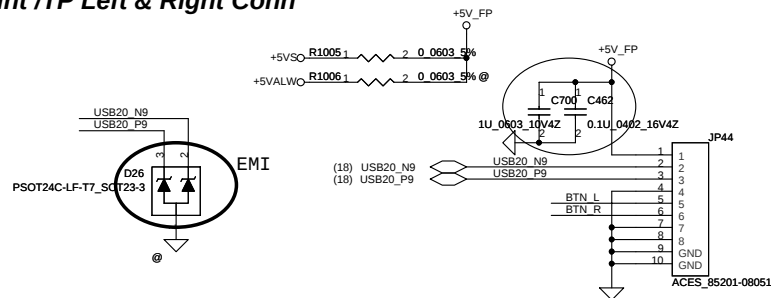
Power Button Logic



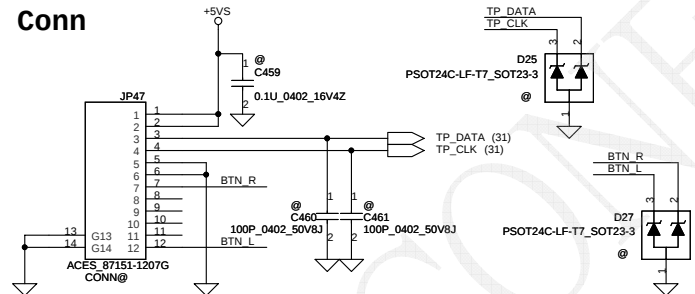
BT



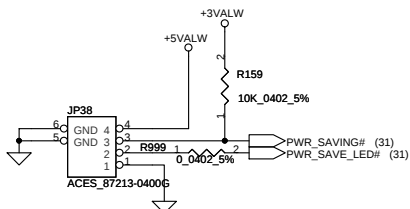
Finger Print /TP Left & Right Conn



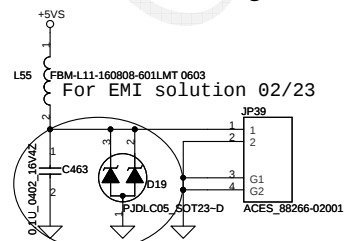
T/P Board Conn



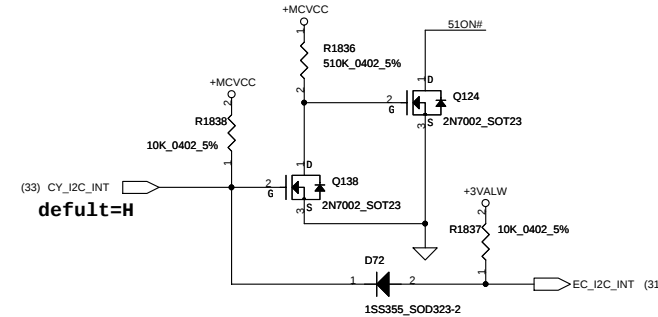
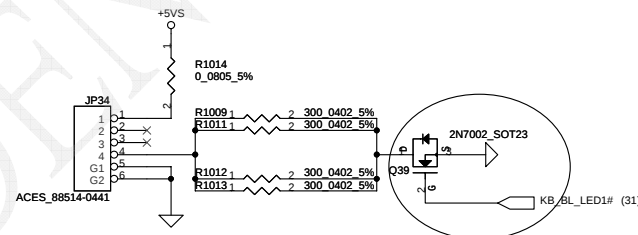
POWER SAVING Conn



ACER LOGO BackLight Conn



KB back light Conn

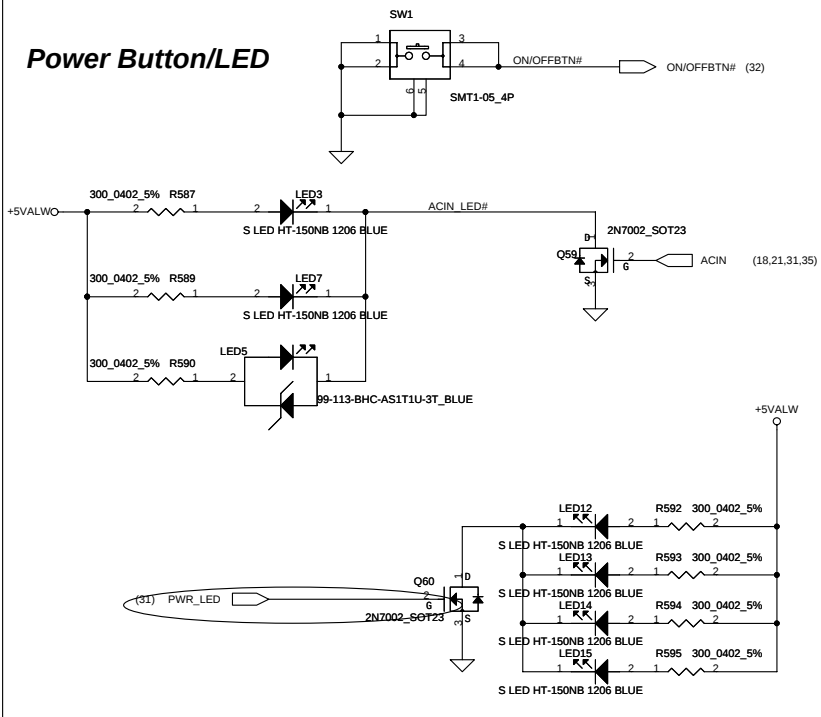


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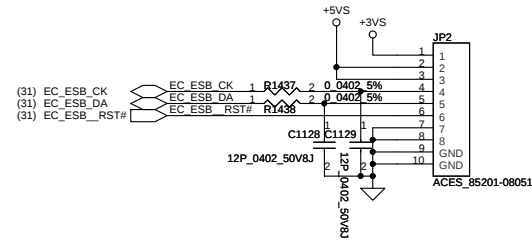
Compal Electronics, Inc.

SCHEMATIC, MB A5011

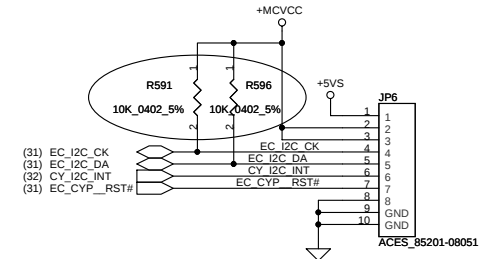
Power Button/LED



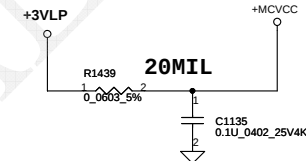
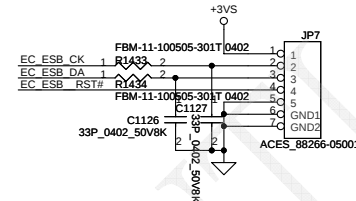
CAP Sensor left(ENE)



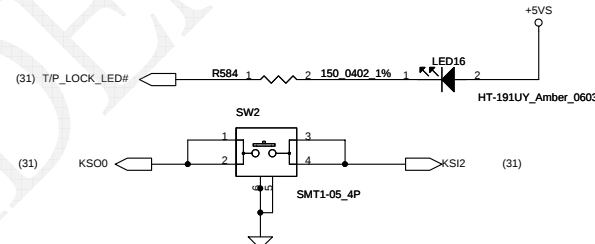
CAP Sensor right(Cypress)



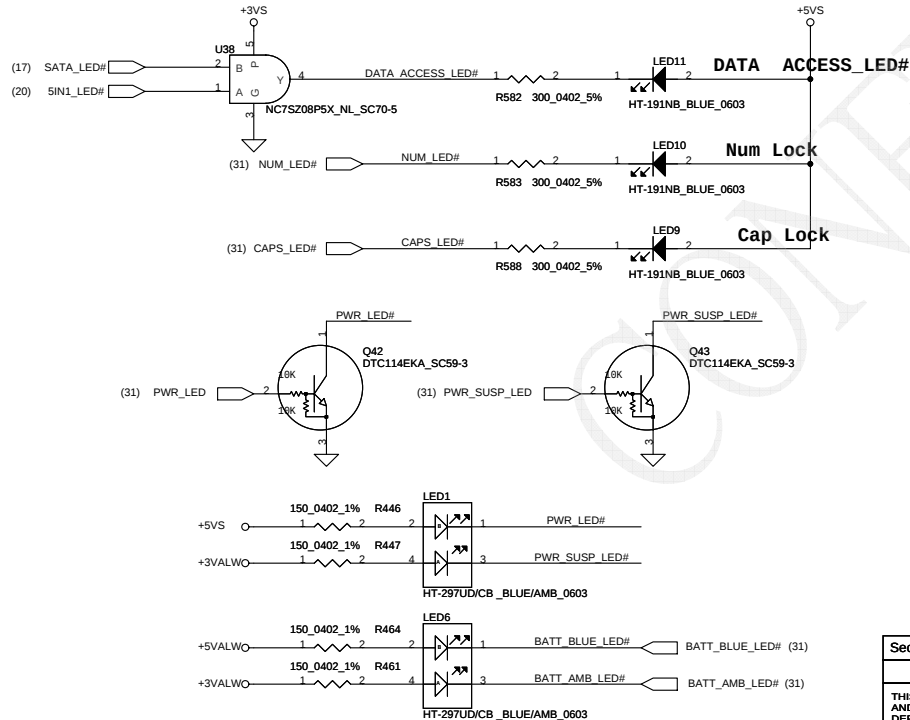
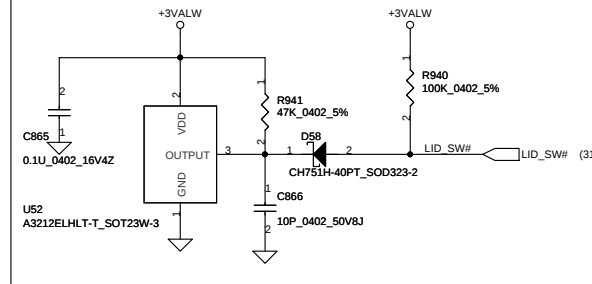
CAP Sensor B COVER(ENE)



T/P Lock Button/LED



(Hall Effect Switch)



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[illegible][illegible]

U31 UMA6 SB54800310

SI4800DY_S08

+3VALW to +3VMXM Transfer

+3VALW

R556 330K_0402_5%

+VSB

C705 10U_0805_10V4Z

U32 2N7002_SOT23 VQA@

+3VMXM_GATE

U33 AO4430_S08 VQA@

+3VMXM

C706 0.1U_0402_16V4Z

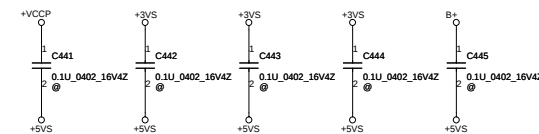
C707 10U_0805_10V4Z

DGPI_PWR_EN

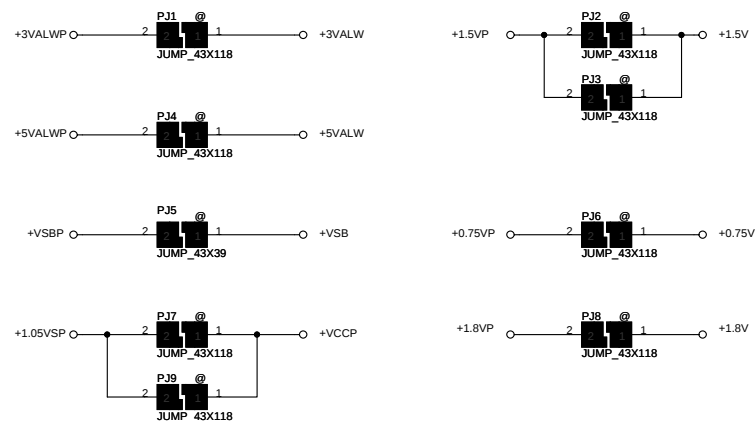
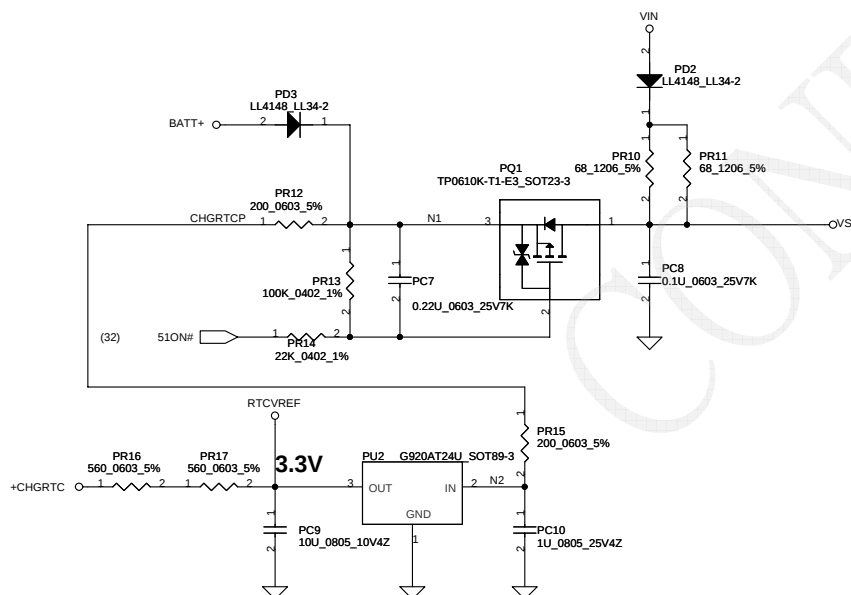
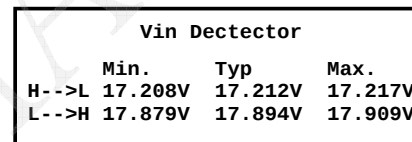
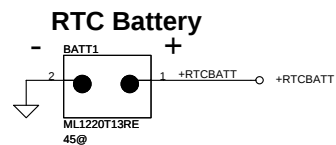
MXM Discharge circuit

Discharge circuit

The diagrams illustrate various discharge paths for the 470_0402_5% resistor. Each circuit includes a resistor connected to a specific voltage source and a transistor (Q9A, Q9B, Q10A, Q10B, Q11A, Q11B) that controls the discharge current to the SUSP pin. The transistors are 2N7002DW T1R7_SOT363-6.

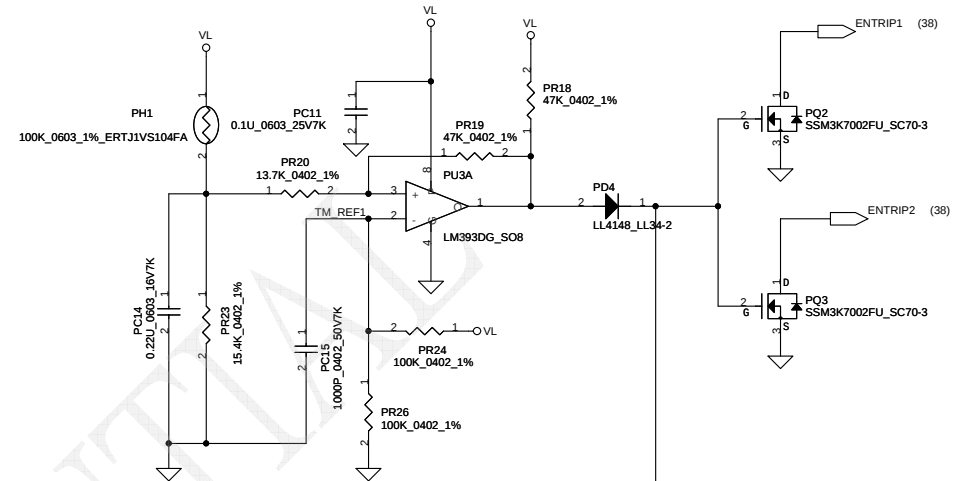


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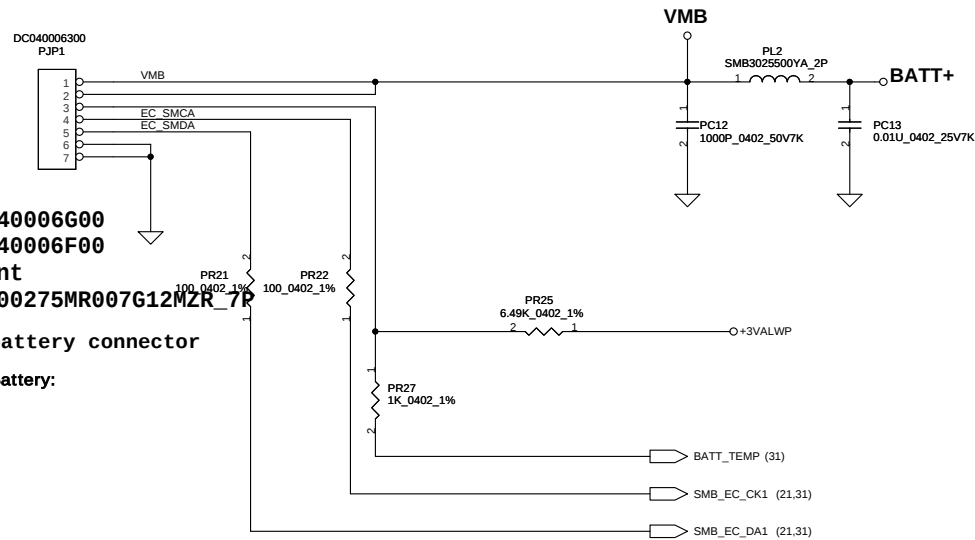
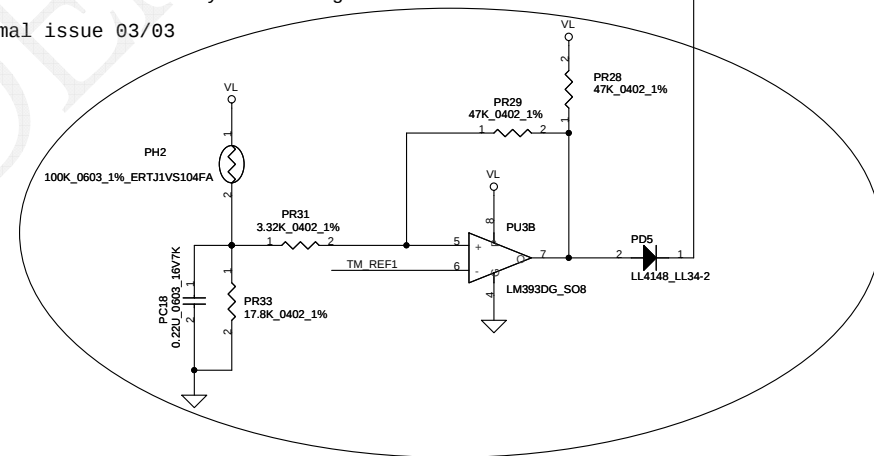
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PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 76 degree C
Recovery at 72 degree C

solve battery thermal issue 03/03



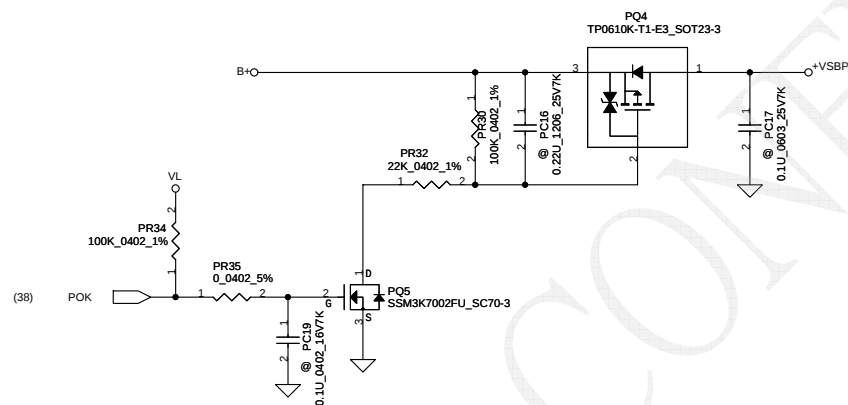
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nd DC040006F00

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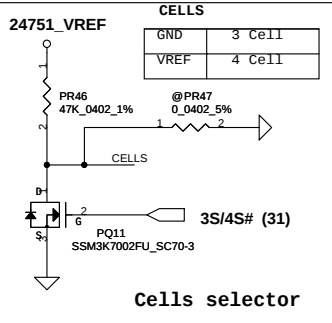
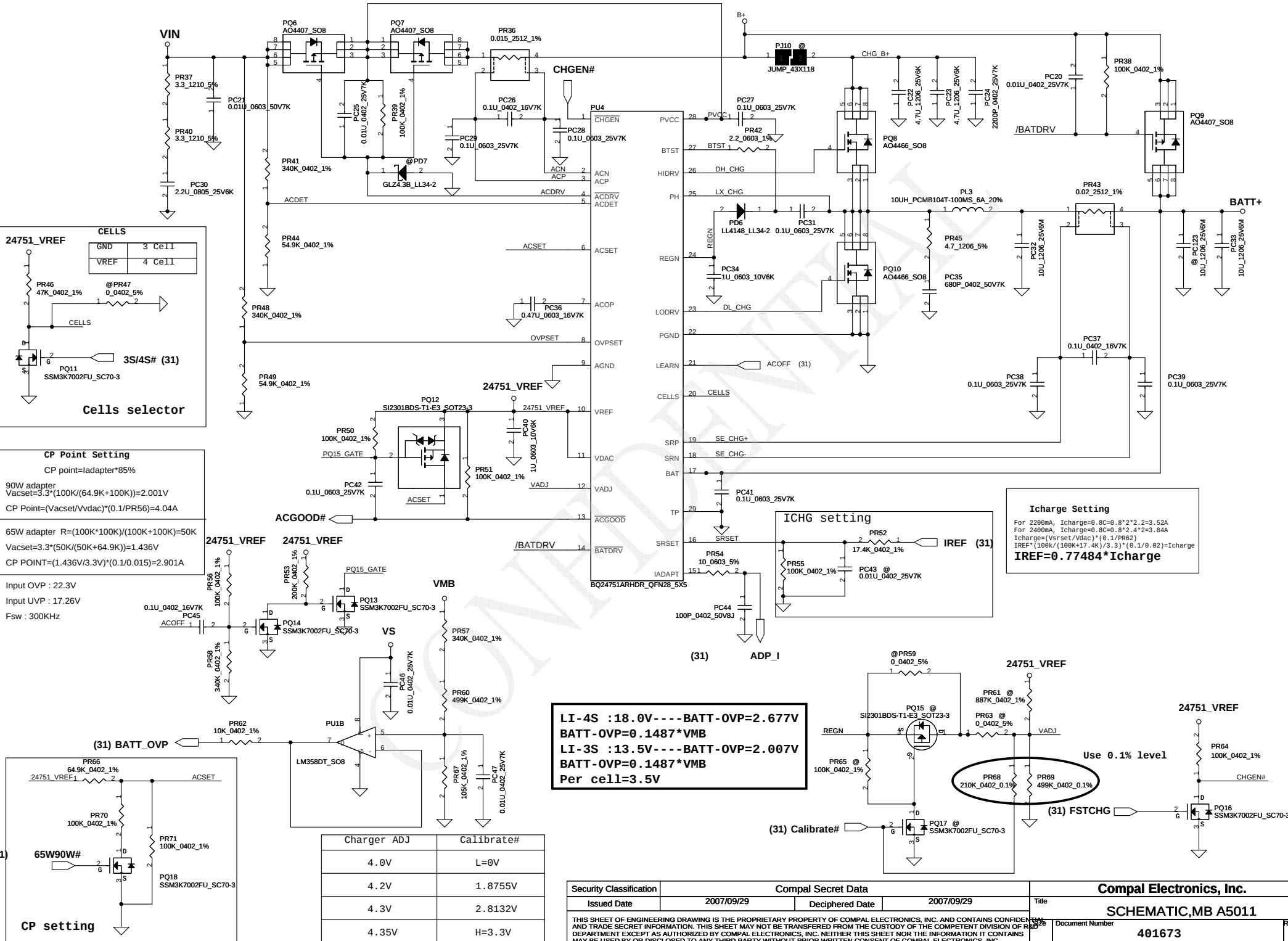
PJP1 battery connector

SMART Battery:

- 1.VMB
2.VMB
3.TSA
4.SMC
5.SMD
6.GND
7.GND



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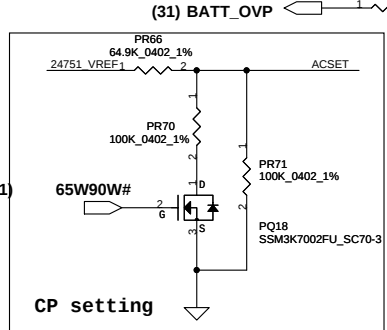


CP Point Setting
CP point=ladapter*85%

90W adapter
 $V_{acset}=3.3 \cdot (100K / (64.9K + 100K)) = 2.001V$
CP Point=(V_{acset} / V_{vdac}) * (0.1 / PR56) = 4.04A

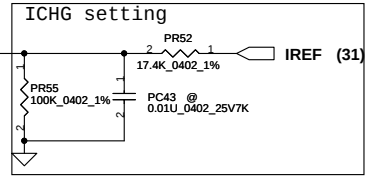
65W adapter $R = (100K \cdot 100K) / (100K + 100K) = 50K$
 $V_{acset} = 3.3 \cdot (50K / (50K + 64.9K)) = 1.436V$
CP POINT=($1.436V / 3.3V$) * (0.1 / 0.015) = 2.901A

Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz

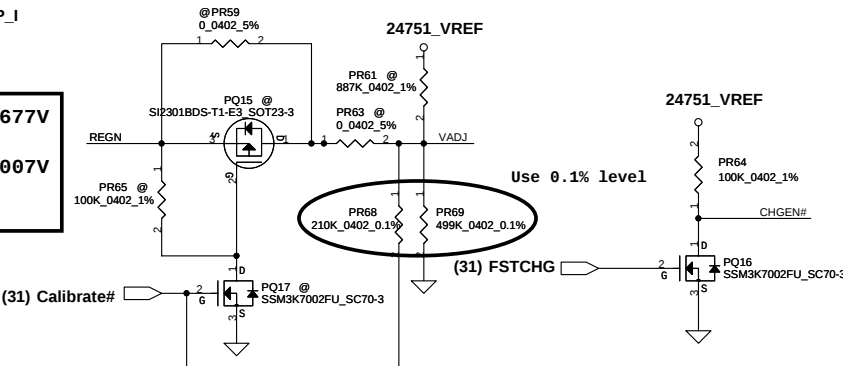


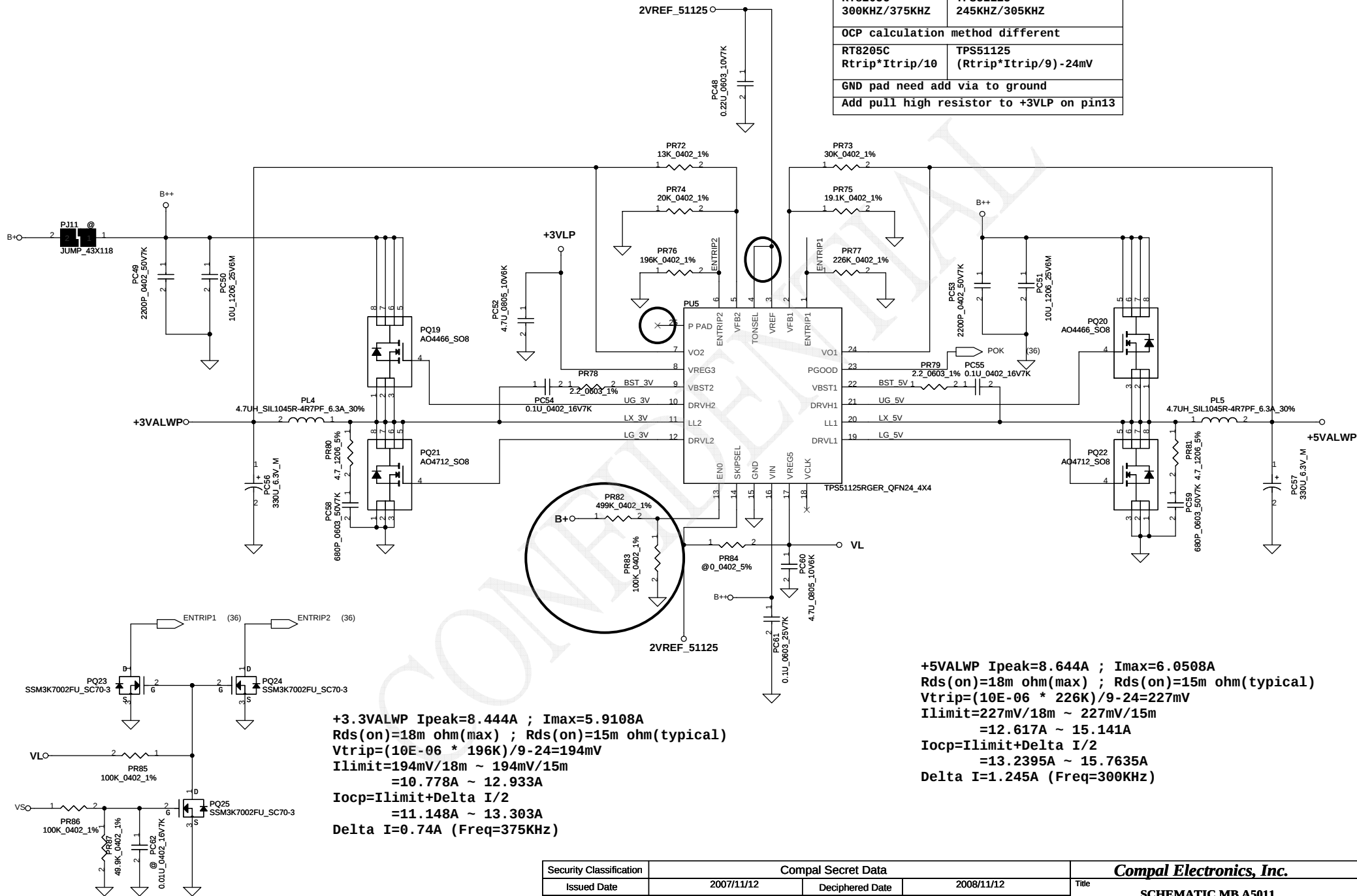
Charger ADJ	Calibrate#
4.0V	L=0V
4.2V	1.8755V
4.3V	2.8132V
4.35V	H=3.3V

LI-4S : 18.0V --- BATT-OVP=2.677V
BATT-OVP=0.1487*VMB
LI-3S : 13.5V --- BATT-OVP=2.007V
BATT-OVP=0.1487*VMB
Per cell=3.5V

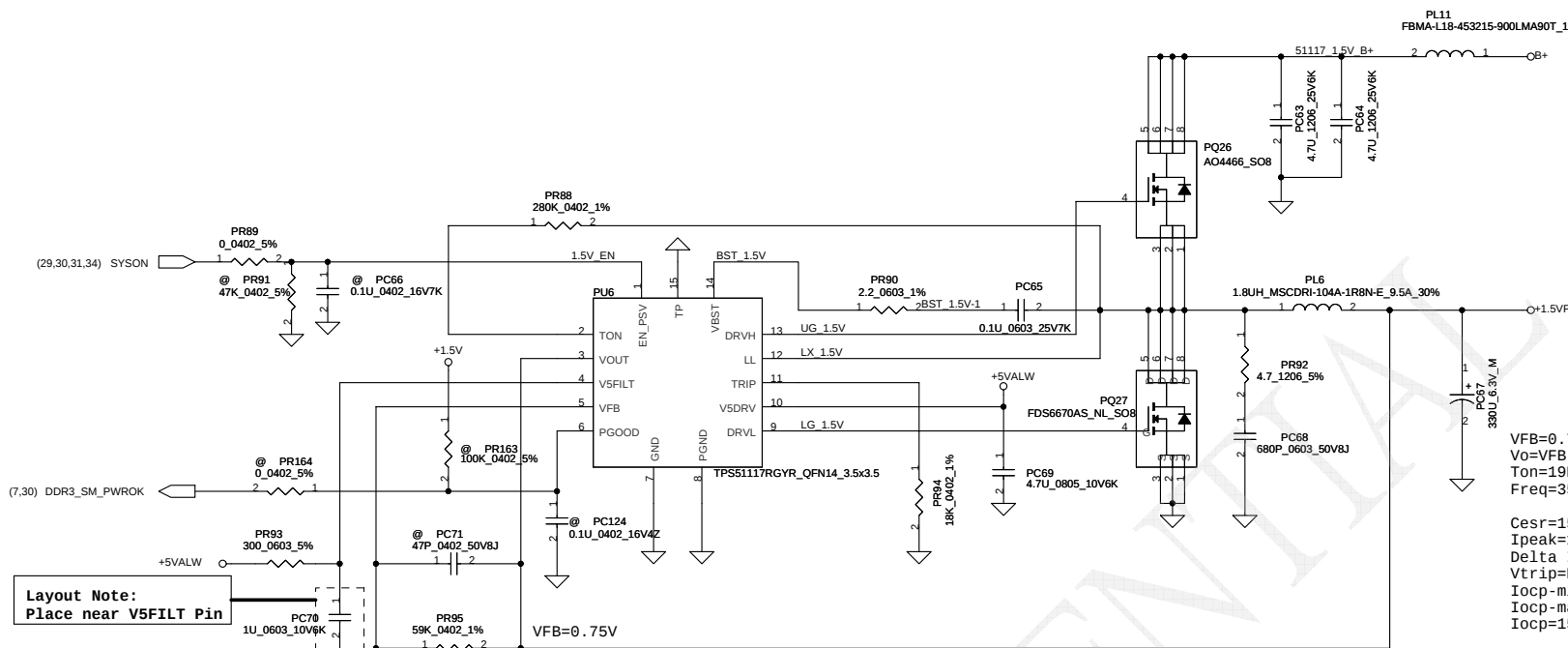


Icharge Setting
For 2200mA, Icharge=0.8C=0.8*2*2.2=3.52A
For 2400mA, Icharge=0.8C=0.8*2.4*2=3.84A
Icharge=(V_{srset} / V_{dac}) * (0.1 / PR62)
IREF=($180K / (180K + 17.4K) / 3.3$) * (0.1 / 0.02) = Icharge
IREF=0.77484*Icharge





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$$VFB=0.75V$$

$$Vo=VFB*(1+PR95/PR96)=1.5V$$

$$Ton=19E-12*Ron*((2/3)*Vo+150mV)/Vin+50ns=4.68E-7$$

$$Freq=356KHz$$

$$Cesr=15m\ ohm$$

$$Ipeak=13.67A\ I_{max}=9.569A$$

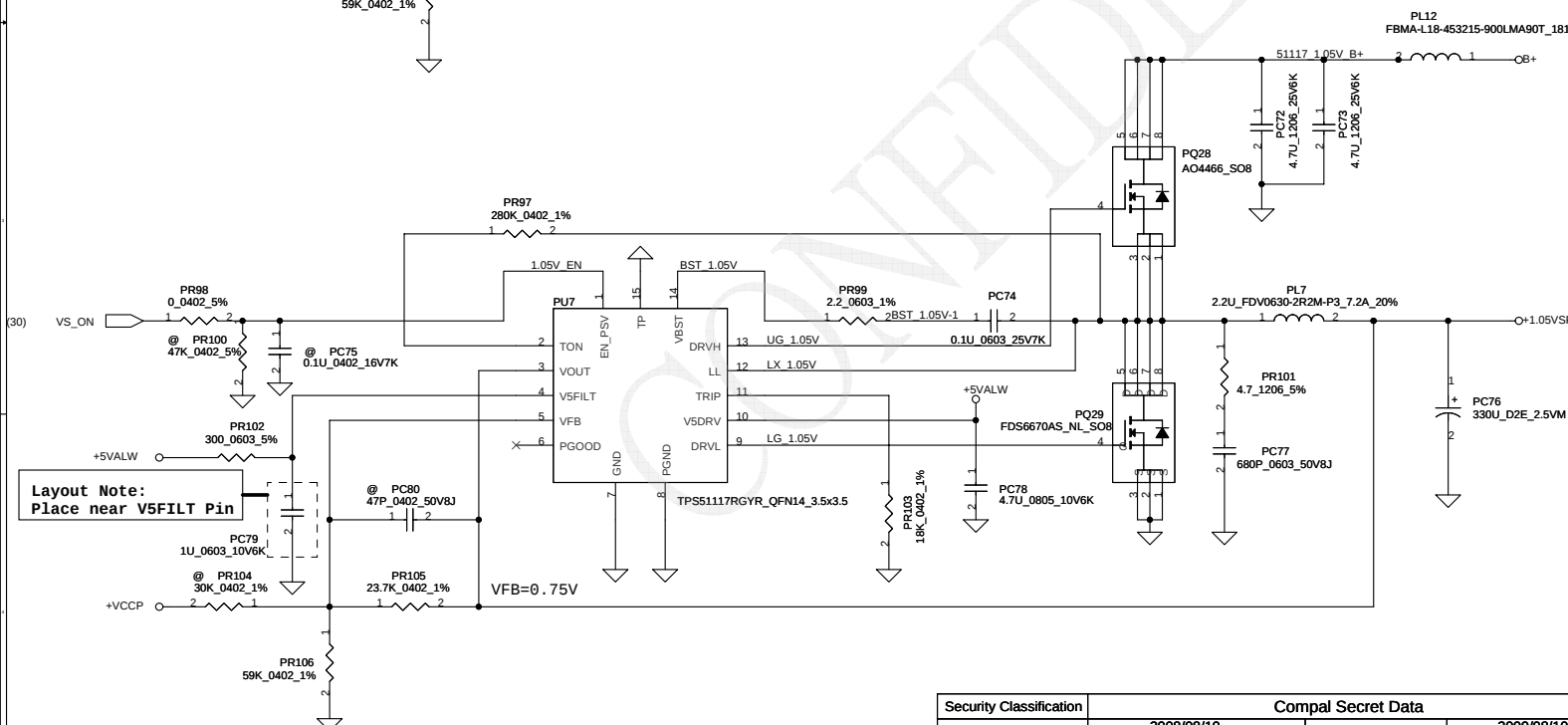
$$\Delta I=((19.5-1.5)*(1.5/19.5))/(L*Freq)=2.429A$$

$$V_{trip}=R_{trip}*10\mu A=0.180V$$

$$I_{ocp_min}=V_{trip}/R_{dsonmax}*1.1+2.429=15.161A$$

$$I_{ocp_max}=V_{trip}/R_{dsonmax}*1.1+2.429=23.436A$$

$$I_{ocp}=15.161-23.436A$$



$$VFB=0.75V$$

$$Vo=VFB*(1+PR105/PR106)=1.05V$$

$$Ton=19E-12*Ron*((2/3)*Vo+150mV)/Vin+50ns=3.54E-07$$

$$Freq=330KHz$$

$$Cesr=15m\ ohm$$

$$Ipeak=17.47A\ I_{max}=12.229A$$

$$\Delta I=((19.5-1.05)*(1.05/19.5))/(L*Freq)=1.597A$$

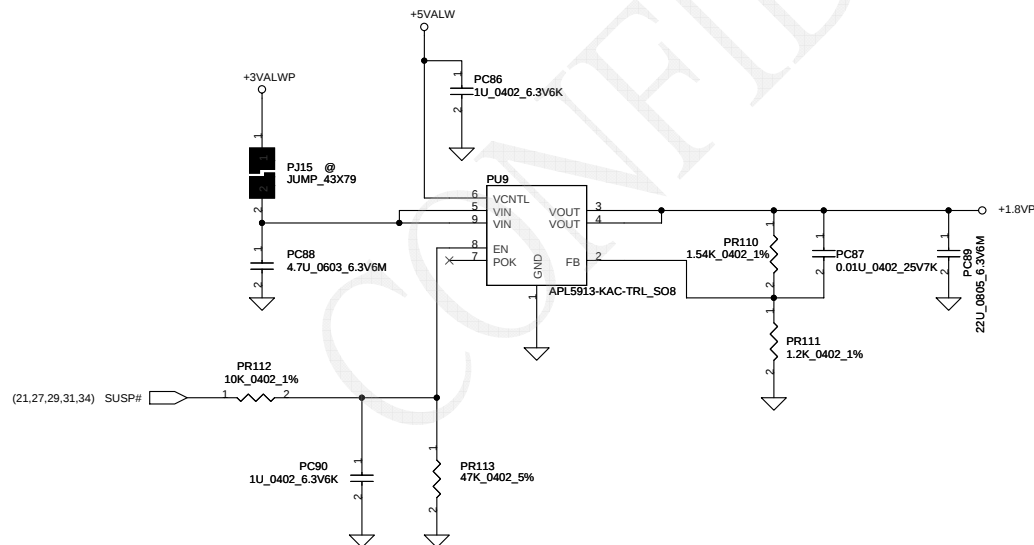
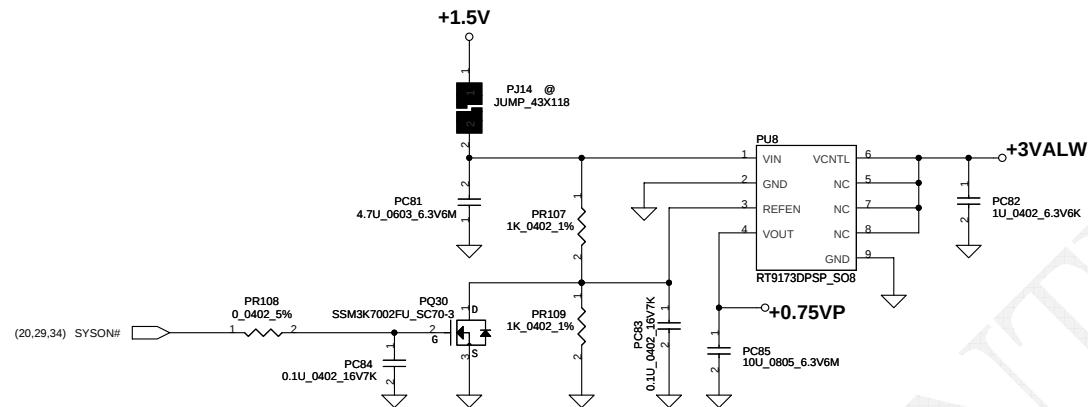
$$V_{trip}=R_{trip}*10\mu A=0.180V$$

$$I_{ocp_min}=V_{trip}/R_{dsonmax}*1.1+1.597=14.745A$$

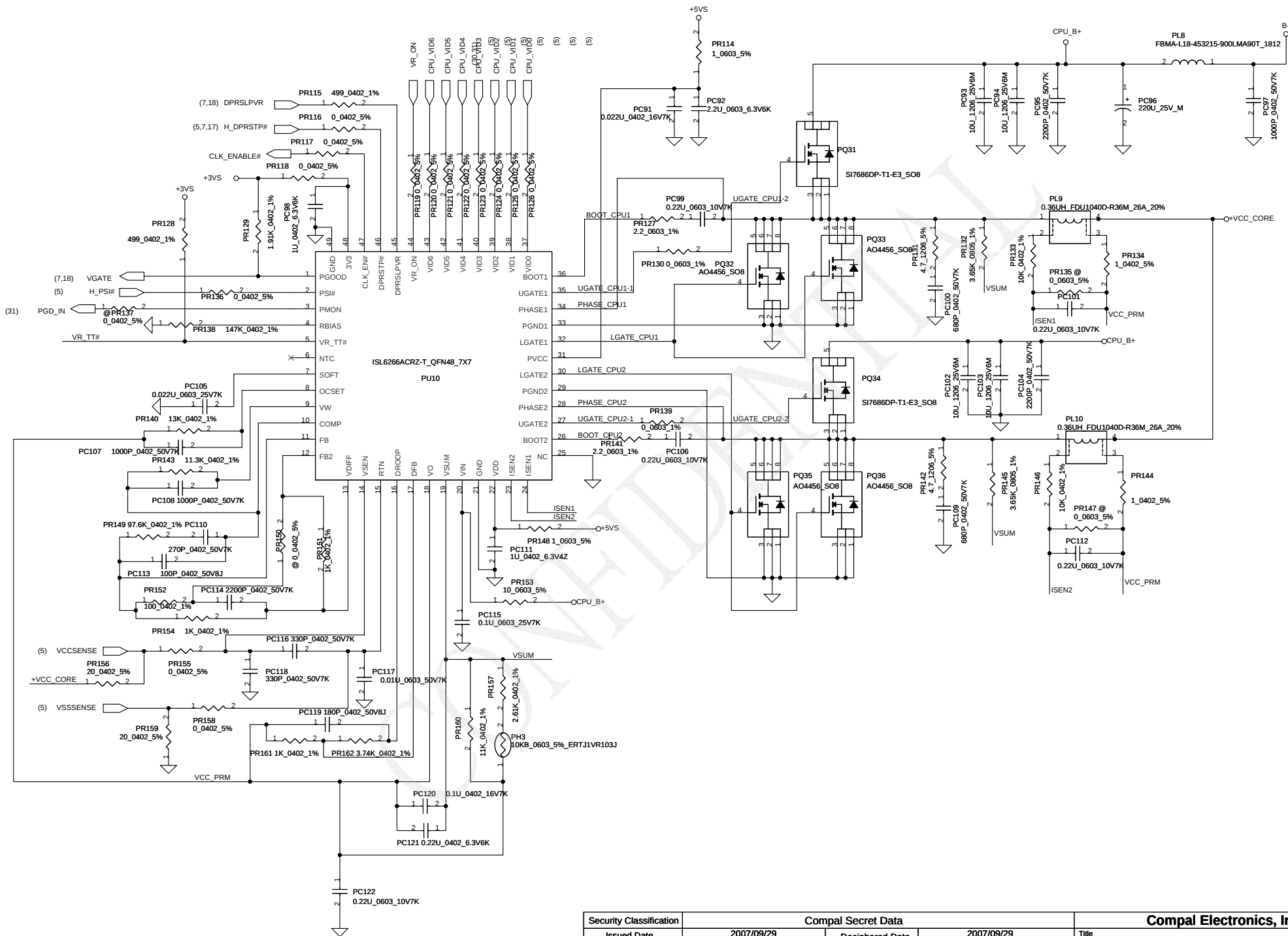
$$I_{ocp_max}=V_{trip}/R_{dsonmax}*1.1+1.597=23.019A$$

$$I_{ocp}=14.745-23.019A$$

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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1		Unite parts			PQ5,PQ11,PQ13,PQ14,PQ16,PQ17,PQ18,PQ30 Change from SB000006800、SB000009080 to SB000009610	2008 12/19	EVT
2		EMI request			Add PR80,PR81,PR131,PR142 SD001470B80 (S RES 1/4W 4.7 +-5% 1206)	2008 12/19	EVT
3		EMI request			Change PR78,PR79,PR127,PR141 from 0 to 2.2 (SD014220B80)	2008 12/19	EVT
4		Reduse 1.5V, 1.05V frequency to about 300KHz			Change PR88,PR97 from 180K to 280K(SD034280380)	2008 12/19	EVT
5	Output voltage error	Set 1.8V voltage			Change PR111 from 1.71K to 1.2K(SD034120180)	2008 12/19	EVT
6		Down size			Change PC88 from 0805 to 0603(SE093475K80)	2008 12/19	EVT
7	Heavy load efficiency fail	Raise heavy load efficiency		38	Change PL4,PL5 from 10uF to 4.7uF(SH000006J80)	2008 12/19	EVT
8		EMI request			Add PC58,PC59 S CER CAP 680P 50V K X7R 0603 (SE025681K80)	2008 12/19	EVT
9		EMI request			Add PC100,PC109 S CER CAP 680P 50V K X7R 0402 (SE074681K80)	2008 12/19	EVT
10				41	Change PR143 from 8.25K to 11.3K(SD034113280)	2008 12/19	EVT
11		Improve load line		41	Change PR162 from 4.42K to 3.74K(SD034374180)	2008 12/22	EVT
12		New charge voltage setting		37	Delete PQ15,PQ17,PR61,PR63,PR65	2008 12/23	EVT
13		New charge voltage setting		37	Add PR68 210K_0402_1%(SD034210380)	2008 12/23	EVT
14		New charge voltage setting		37	Change PR69 from 221K to 49.9K(SD034499280)	2008 12/23	EVT
15	Battery can't charge to 100%			37	Change PR69 from 49.9K to 499K(SD034499380)	2009 01/12	DVT
16	HDMI 5V voltage test fail(should 4.8~5.3V)	Raise 5V voltage		38	Change PR75 from 20K to 19.1K(SD034191280)	2009 01/17	DVT
17		Prevent spike		37	Add PD7	2009 01/21	DVT
18		Improve charge voltage		37	Change PR68, PR69 from 1% to 0.1%	2009 01/22	DVT
19		EMI request		39	Change PR90, PR99 from 0 to 2.2(SD014220B80) Enable PR92, PR101, PC68, PC77	2009 02/04	DVT
20		EMI request		39	Change PJ12 to PL11(SM010020720) Change PJ13 to PL12(SM010020720)	2009 02/04	DVT
21		EMI request		37	Change PR42 from 0 to 2.2(SD014220B80) Enable PR45, PC35	2009 02/04	DVT
22	Protect logic low	Set trigger point at 76		36	Enable PD5, PH2, PR28, PR29, PR31, PR33, PC18	2009 02/25	PVT
23							

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