

Compal Confidential

HQD70/HDQ71 Schematics Document

Intel Dothan Processor with 915PM/915GM + DDRII + ICH6M
(With ATi M26-P)

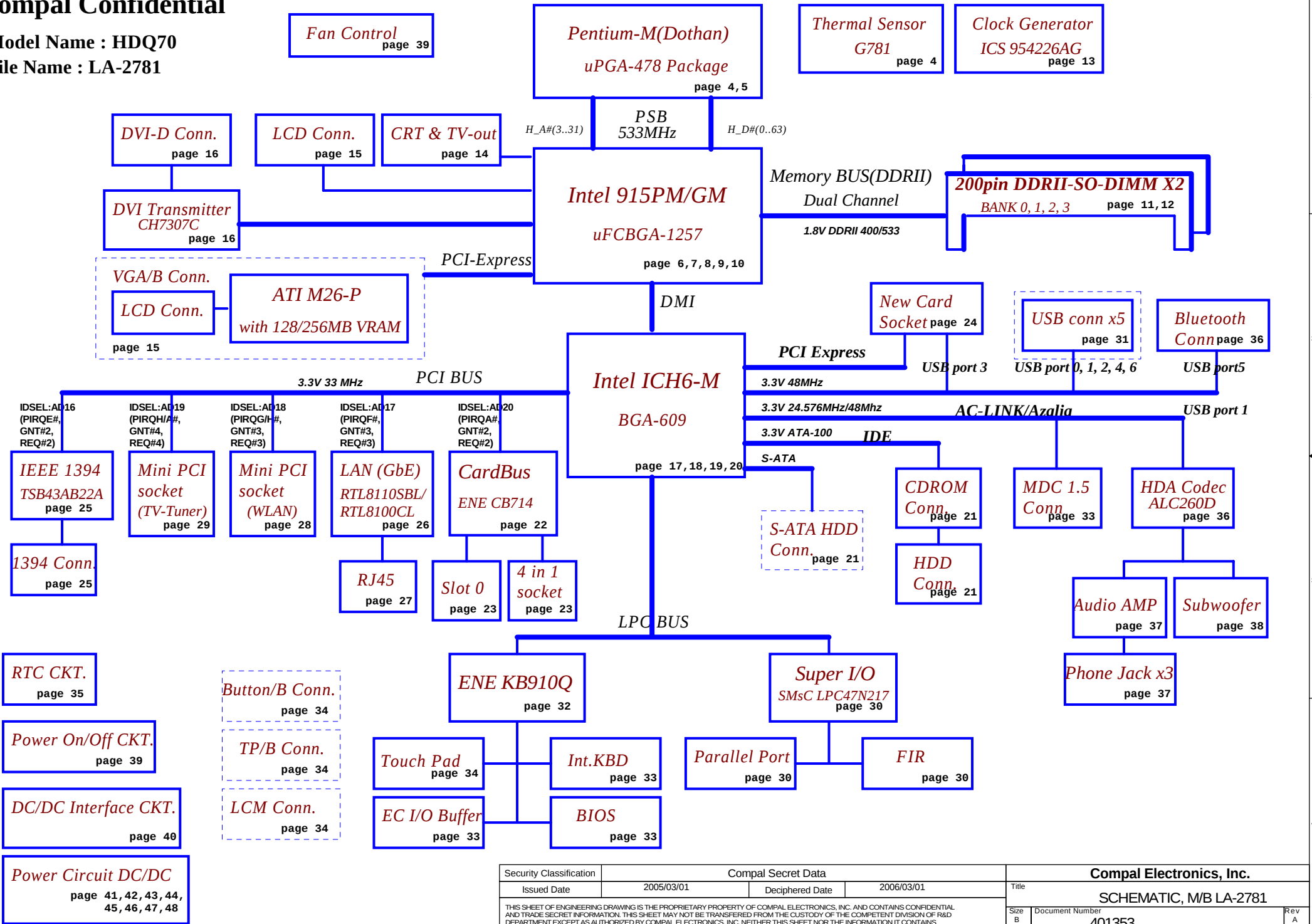
2005-05-12

REV: 0.2 (For DVT)

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				SCHEMATIC / B LA-2781	
Size	B	Document Number			Rev
		401353			A
Date:		星期五, 六月 03, 2005		Sheet	1 of 50

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Model Name : HDQ70
File Name : LA-2781



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN	AD17	3	PIRQF
Mini-PCI(WLAN)	AD18	1	PIRQG/PORQH
Mini-PCI(TV-Tuer)	AD19	4	PIRQH/PORQA

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	GMT G781	1001 110X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 110X b		

EC SM Bus2 address

ICH6M SM Bus address

Device	Address
Clock Generator (ICS 954226)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
VGA	@PM @GM
LAN	@8110S
LCM	@LCM @NO_LCM

SKU ID Table

SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

6 H_A#[3..31] H_A#[3..31]

6 H_REQ#[0..4] H_REQ#[0..4]

6 H_RS#[0..2] H_RS#[0..2]

6 H_TRDY#

6 H_DBSY#
18 H_DPSLP#
18 H_DPRSTP#
6 H_DPWR#

18 H_PWRGOOD
6,18 H_CPUSLP#

6,18 H_THERMTRIP#

H_A#3 P4#
H_A#4 U4#
H_A#5 V3#
H_A#6 R3#
H_A#7 V2#
H_A#8 W1#
H_A#9 T4#
H_A#10 W2#
H_A#11 Y4#
H_A#12 Y1#
H_A#13 U1#
H_A#14 AA3#
H_A#15 Y3#
H_A#16 AA2#
H_A#17 AF4#
H_A#18 AC4#
H_A#19 AC7#
H_A#20 AC3#
H_A#21 AD3#
H_A#22 AE4#
H_A#23 AD2#
H_A#24 AB4#
H_A#25 AC6#
H_A#26 AD5#
H_A#27 AE2#
H_A#28 AD6#
H_A#29 AF3#
H_A#30 AE1#
H_A#31 AF1#

H_REQ#0 R2#
H_REQ#1 P3#
H_REQ#2 T2#
H_REQ#3 P1#
H_REQ#4 T1#

6 H_ADSTB#0 U3#
6 H_ADSTB#1 AE5#

13 CLK_CPU_BCLK
13 CLK_CPU_BCLK#

6 H_ADS# N2#
6 H_BNR# L1#
6 H_BPR# J3#
6 H_BR0# N4#
6 H_DEFER# L4#
6 H_DRDY# H2#
6 H_HIT# K3#
6 H_HITM# K4#
6 H_IERR# A4#
6 H_LOCK# J2#
6 H_CPURST# B11#

H_RS#0 H1#
H_RS#1 K1#
H_RS#2 L2#
H_TRDY# M3#

X C8 BPM0#
X B8 BPM1#
X A9 BPM2#
X C9 BPM3#

ITP_DBRRESET# A7#
M2#
DBSY# B7#
DPSLP# G1#
DPRSTP# C19#
DPWR# X A10#
PRDY# X B10#
PREQ# B17#
PROCHOT#

H_PWRGOOD E4#
H_CPUSLP# A6#
ITP_TCK A13#
ITP_TDI C12#
ITP_TDO A12#
TEST1 C5#
TEST2 F23#
ITP_TMS C11#
ITP_TRST# B13#

THERMDA B18#
THERMDC A18#
THERMTRIP# C17#

JP33A
A3#
A4#
A5#
A6#
A7#
A8#
A9#
A10#
A11#
A12#
A13#
A14#
A15#
A16#
A17#
A18#
A19#
A20#
A21#
A22#
A23#
A24#
A25#
A26#
A27#
A28#
A29#
A30#
A31#

REQ0#
REQ1#
REQ2#
REQ3#
REQ4#

ADSTB0#
ADSTB1#

ITP_CLK0
ITP_CLK1
BCLK0
BCLK1

ADS#
BNR#
BPR#
BR0#
DEFER#
DRDY#
HIT#
HITM#
IERR#
LOCK#
RESET#

RS0#
RS1#
RS2#
TRDY#

BPM0#
BPM1#
BPM2#
BPM3#

DBR#
DPSY#
DPSLP#
DPRSTP#
DPWR#
PRDY#
PREQ#
PROCHOT#

PWRGOOD
SLP#
TCK
TDO
TEST1
TEST2
TMS
TRST#

THERMDA
THERMDC
THERMTRIP#

Dothan
ADDR GROUP
DATA GROUP

HOST CLK

CONTROL GROUP

MISC

LEGACY CPU

THERMAL DIODE

D0# A19#
D1# A25#
D2# A22#
D3# B21#
D4# A24#
D5# B26#
D6# A21#
D7# B20#
D8# C20#
D9# B24#
D10# D24#
D11# E24#
D12# C26#
D13# B23#
D14# E23#
D15# C25#
D16# H23#
D17# G25#
D18# L23#
D19# M26#
D20# H24#
D21# E25#
D22# G24#
D23# J23#
D24# M23#
D25# J25#
D26# L26#
D27# N24#
D28# M25#
D29# H26#
D30# N25#
D31# K25#
D32# Y26#
D33# AA24#
D34# T25#
D35# U23#
D36# V23#
D37# R24#
D38# R26#
D39# R23#
D40# AA23#
D41# U26#
D42# V24#
D43# U25#
D44# V26#
D45# Y23#
D46# AA26#
D47# Y25#
D48# AB25#
D49# AC23#
D50# AB24#
D51# AC20#
D52# AC22#
D53# AC25#
D54# AD23#
D55# AE22#
D56# AF23#
D57# AD24#
D58# AF20#
D59# AE21#
D60# AD21#
D61# AF25#
D62# AE22#
D63# AF26#

H_DIN#0 6
H_DIN#1 6
H_DIN#2 6
H_DIN#3 6

DSTBN#0 C23#
DSTBN#1 K24#
DSTBN#2 W25#
DSTBN#3 AE24#
DSTBP#0 C22#
DSTBP#1 L24#
DSTBP#2 W24#
DSTBP#3 AE25#

H_A20M# 18
H_FERR# 18
H_IGNNE# 18
H_INIT# 18
H_INTR# 18
H_NMI# 18

H_STPCLK# 18
H_SM# 18

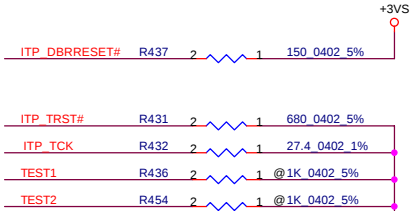
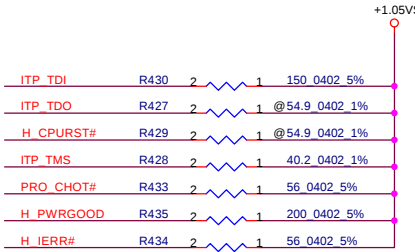
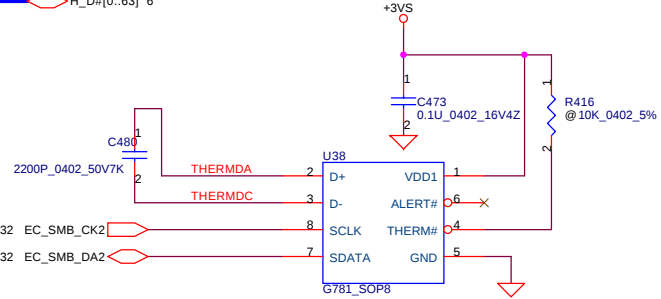
H_DIN#0 6
H_DIN#1 6
H_DIN#2 6
H_DIN#3 6

H_DSTBN#0 6
H_DSTBN#1 6
H_DSTBN#2 6
H_DSTBN#3 6
H_DSTBP#0 6
H_DSTBP#1 6
H_DSTBP#2 6
H_DSTBP#3 6

H_A20M# 18
H_FERR# 18
H_IGNNE# 18
H_INIT# 18
H_INTR# 18
H_NMI# 18

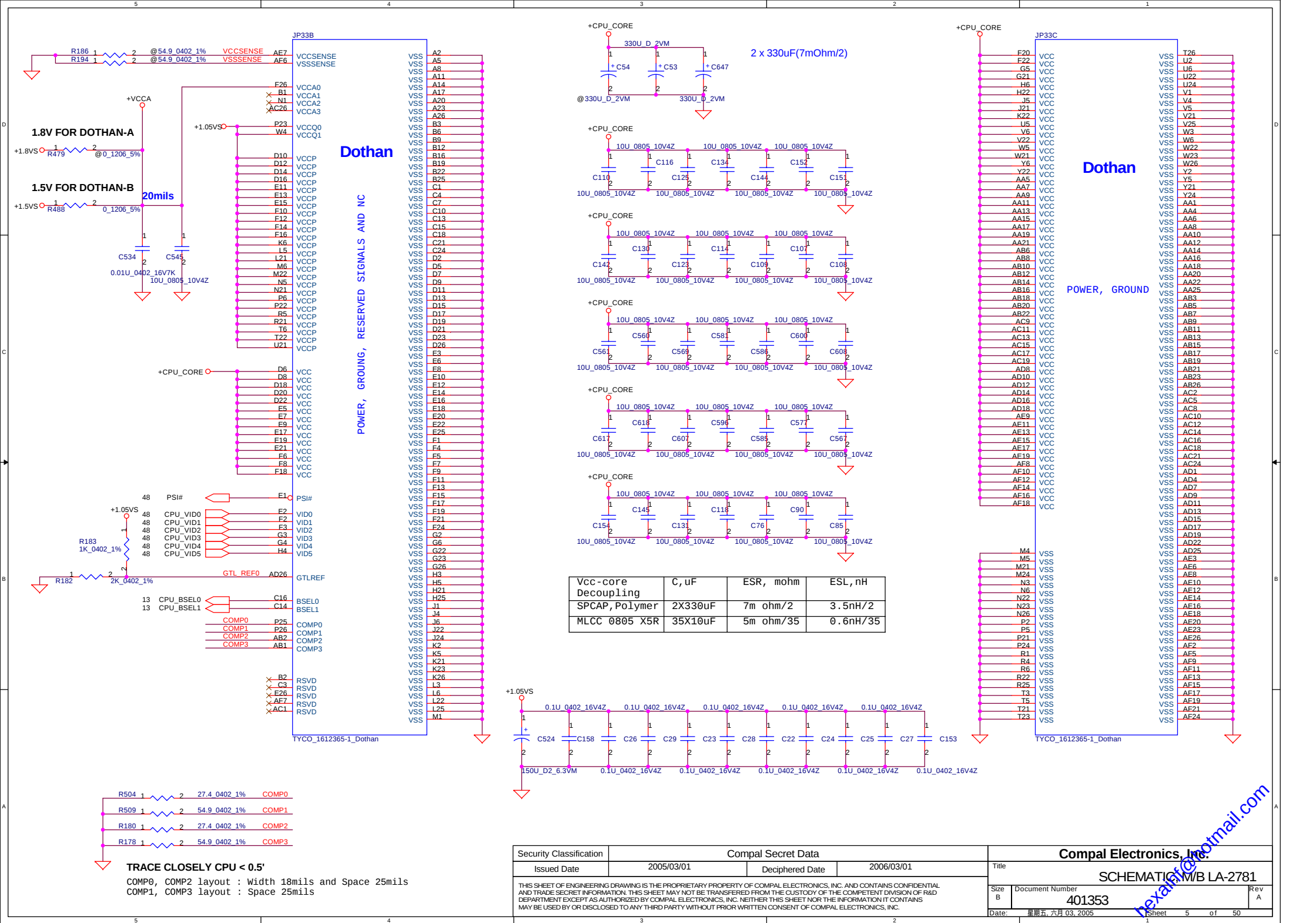
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H_SM# 18

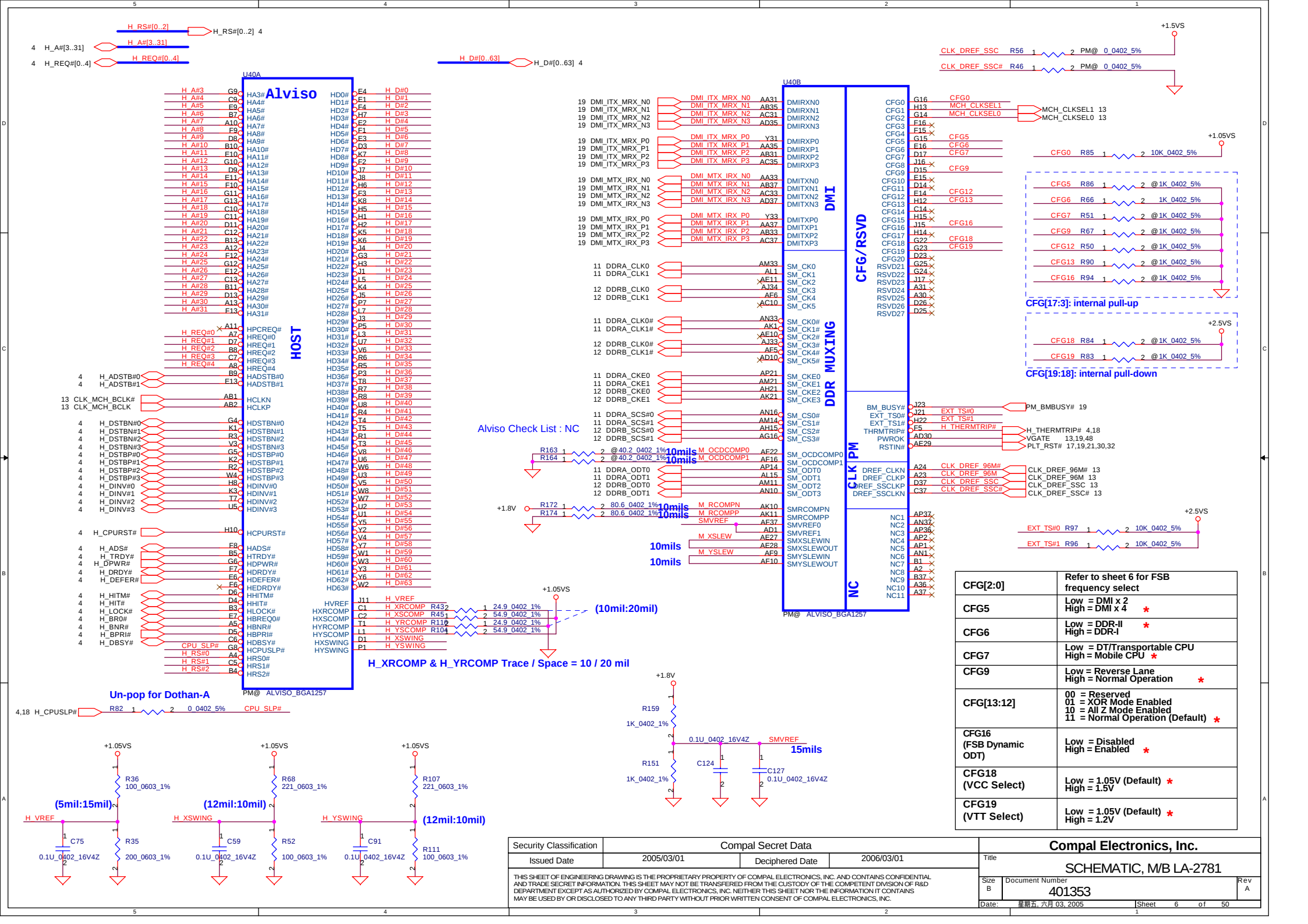
H_D#[0..63] H_D#[0..63] 6



THERMDA & THERMDC Trace / Space = 10 / 10 mil

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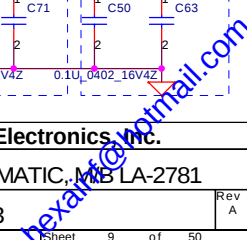


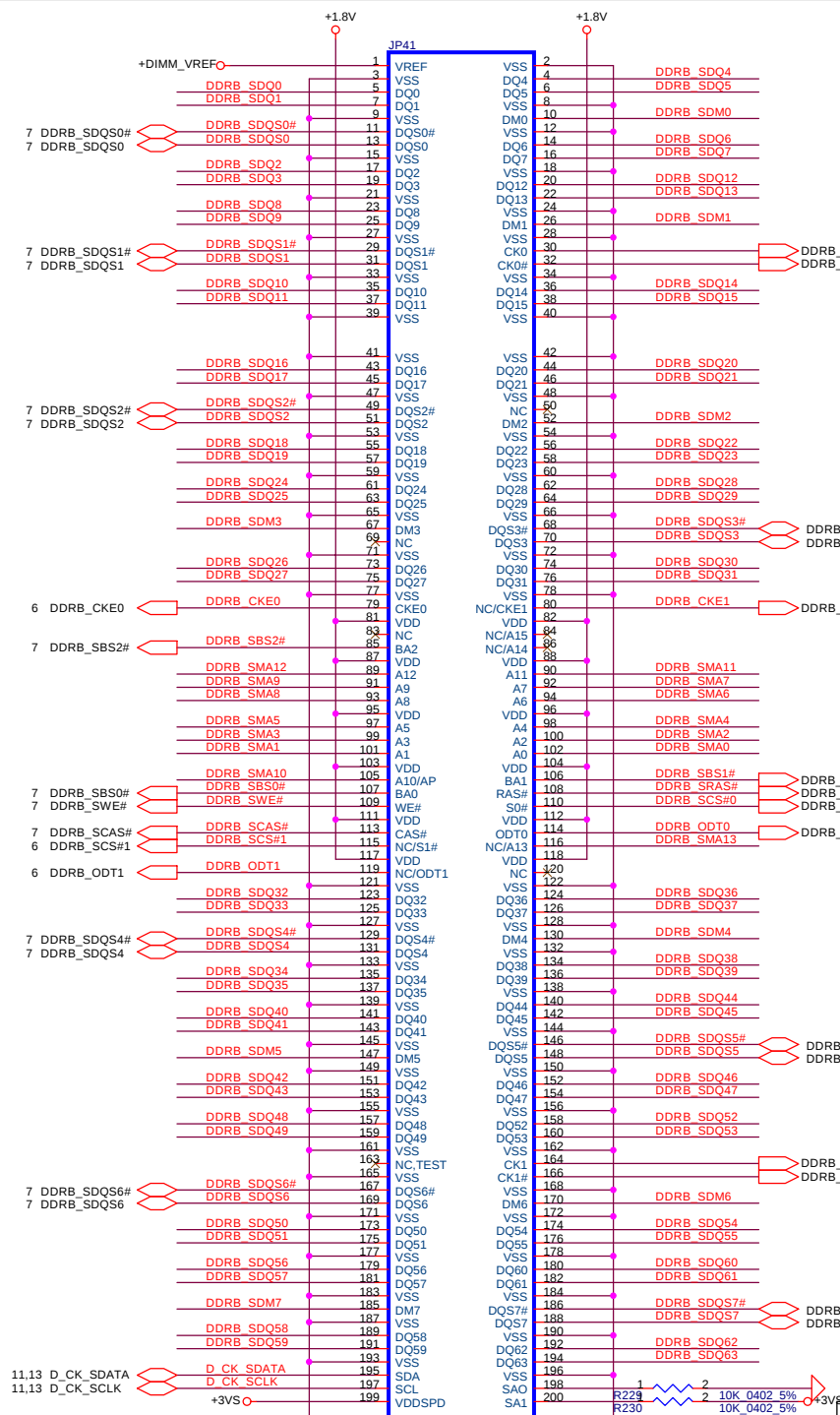
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11 DDRA_SDM[0..7] < DDRA_SDM[0..7]
11 DDRA_SMA[0..13] < DDRA_SMA[0..13]

12 DDRB_SDQ[0..63] < DDRB_SDQ[0..63]
12 DDRB_SDM[0..7] < DDRB_SDM[0..7]
12 DDRB_SMA[0..13] < DDRB_SMA[0..13]

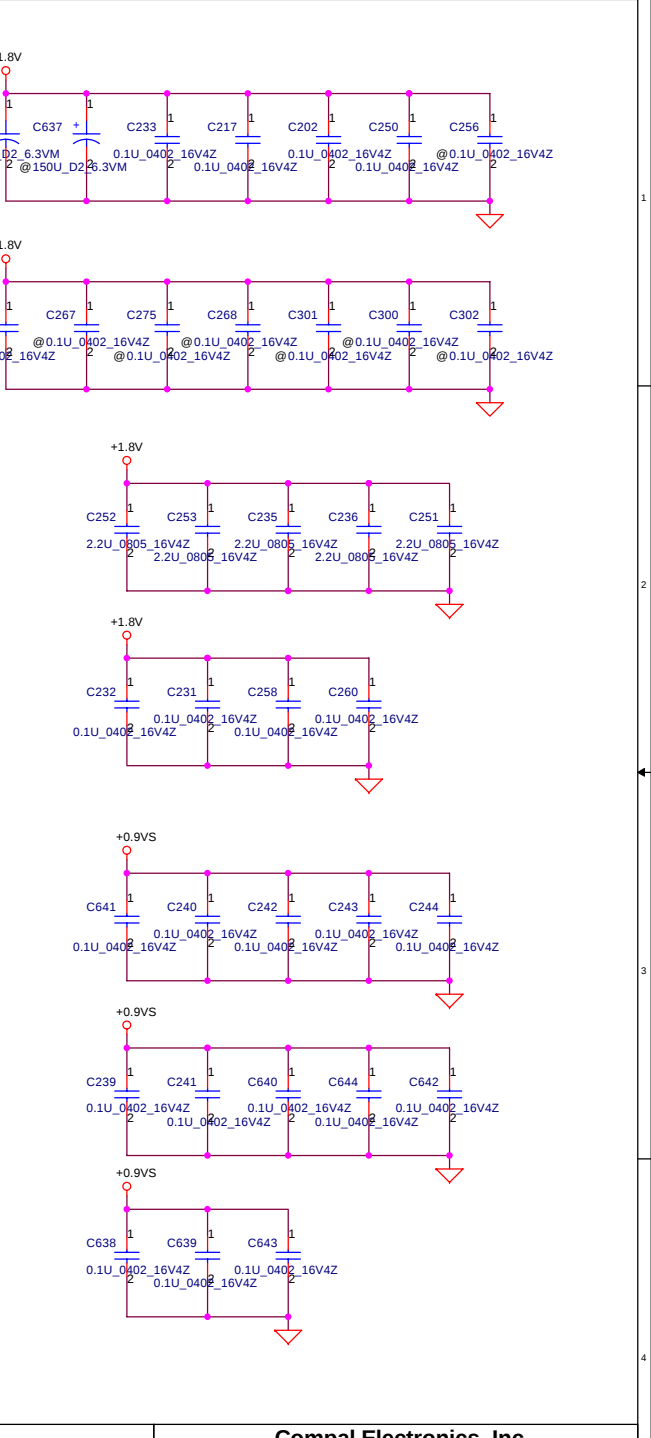
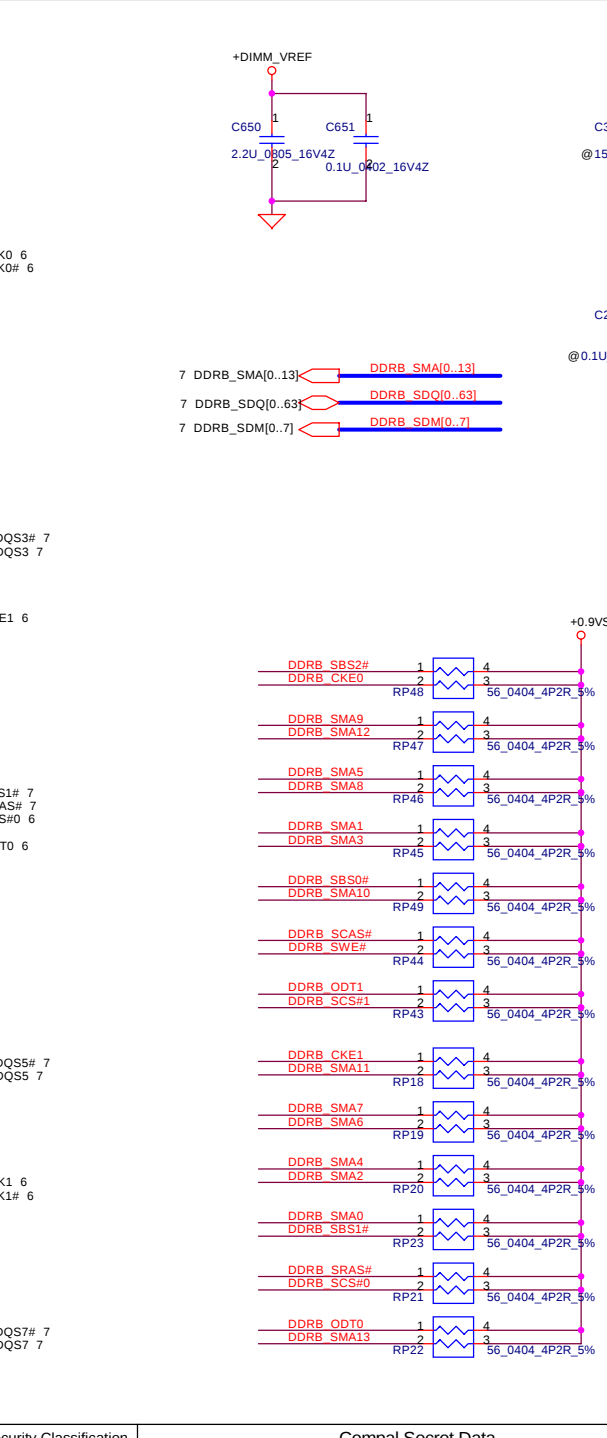


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DIMM1 STD H:9.2mm (BOT)

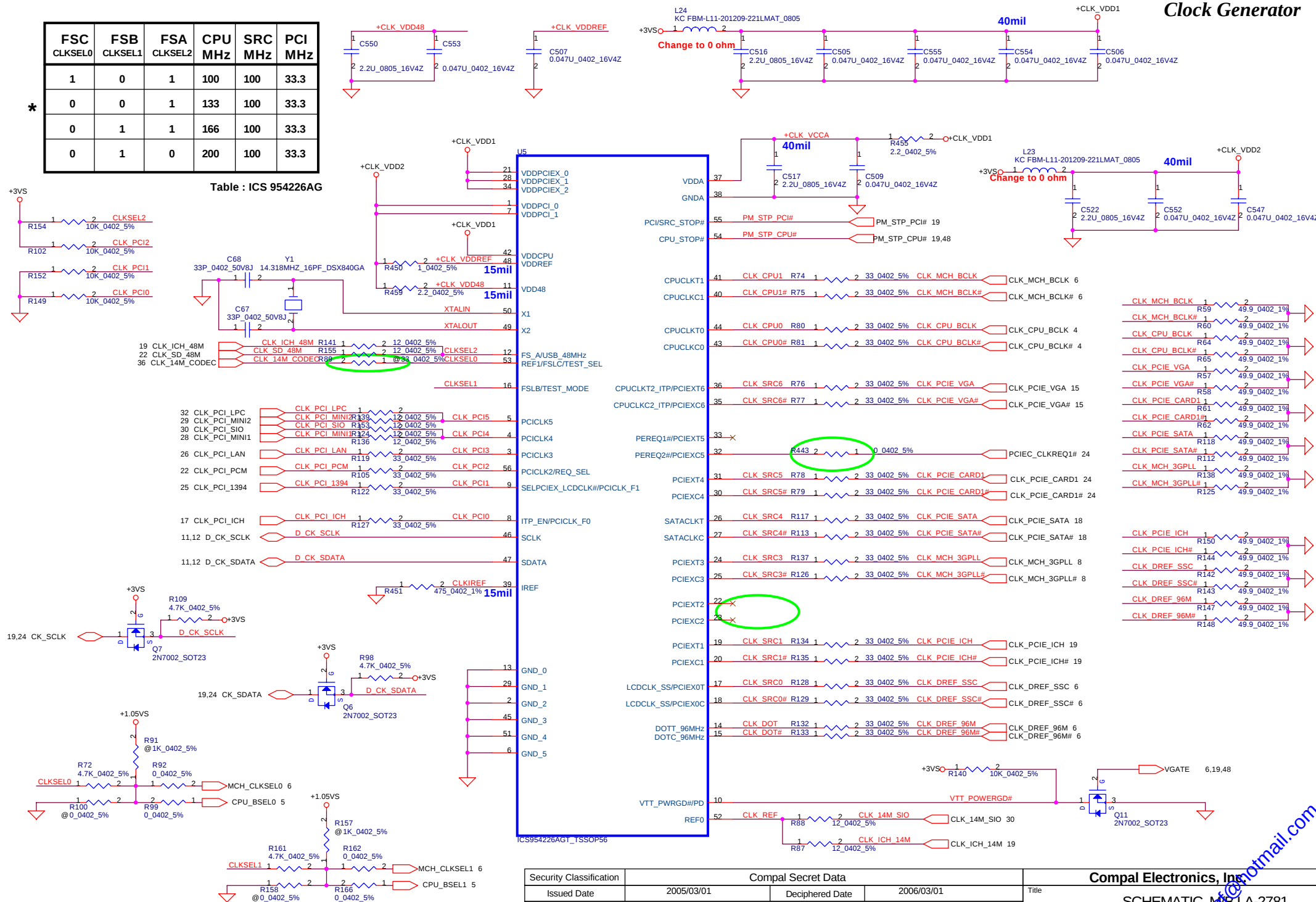


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FSC CLKSEL0	FSB CLKSEL1	FSA CLKSEL2	CPU MHz	SRC MHz	PCI MHz
1	0	1	100	100	33.3
0	0	1	133	100	33.3
0	1	1	166	100	33.3
0	1	0	200	100	33.3

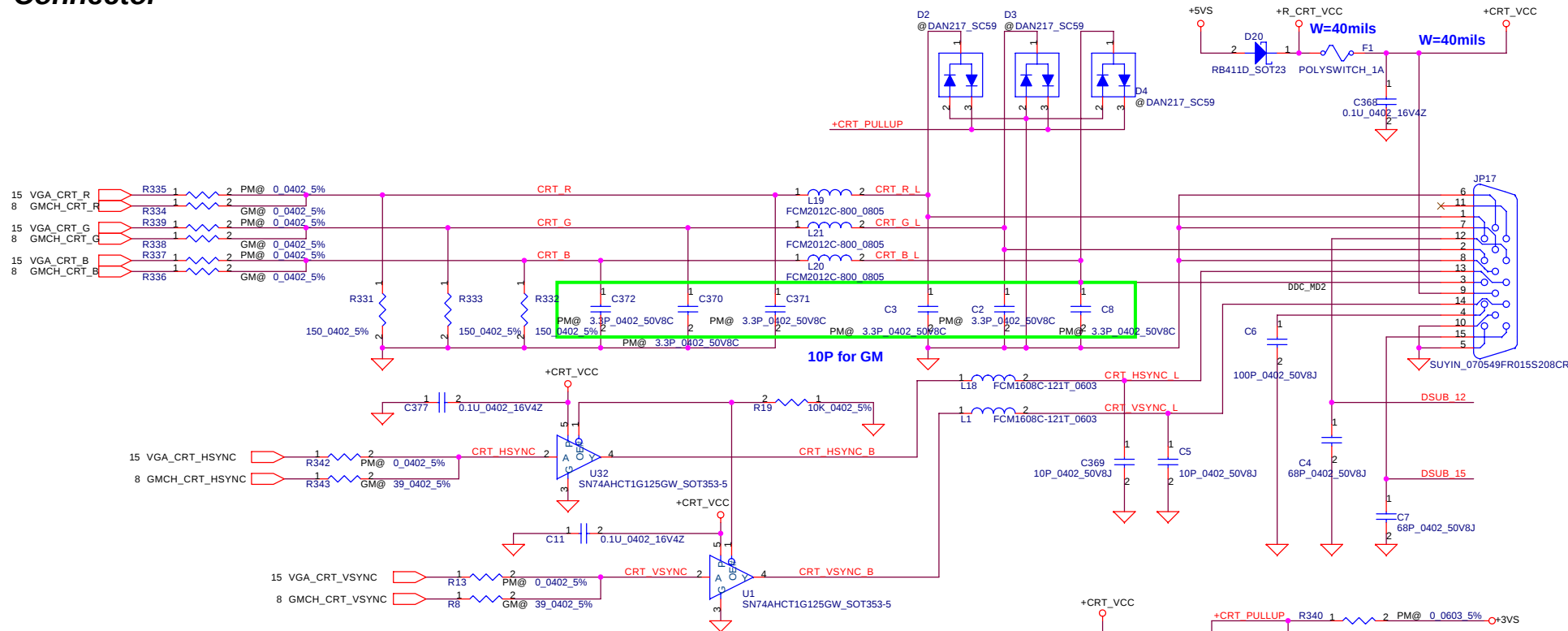
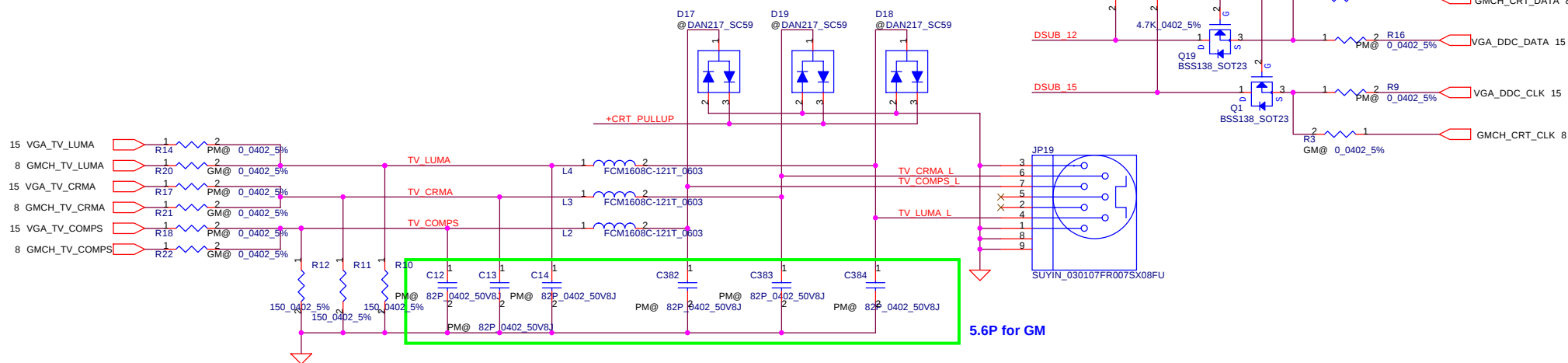
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Clock Generator



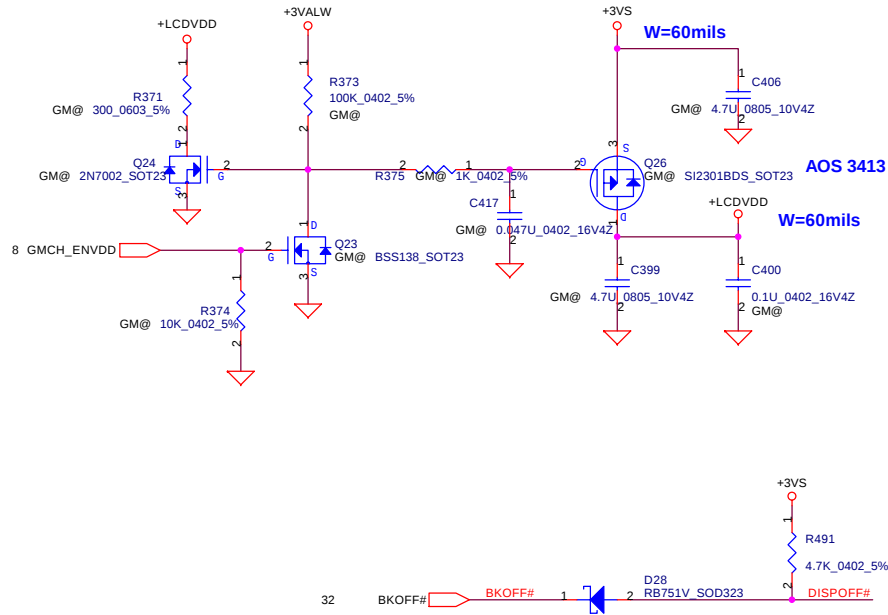
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CRT Connector

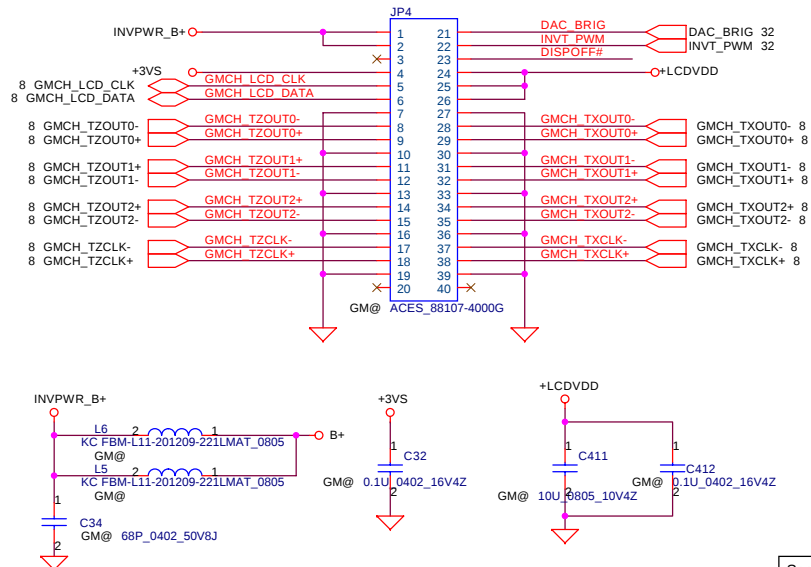
**TV-OUT Conn.**

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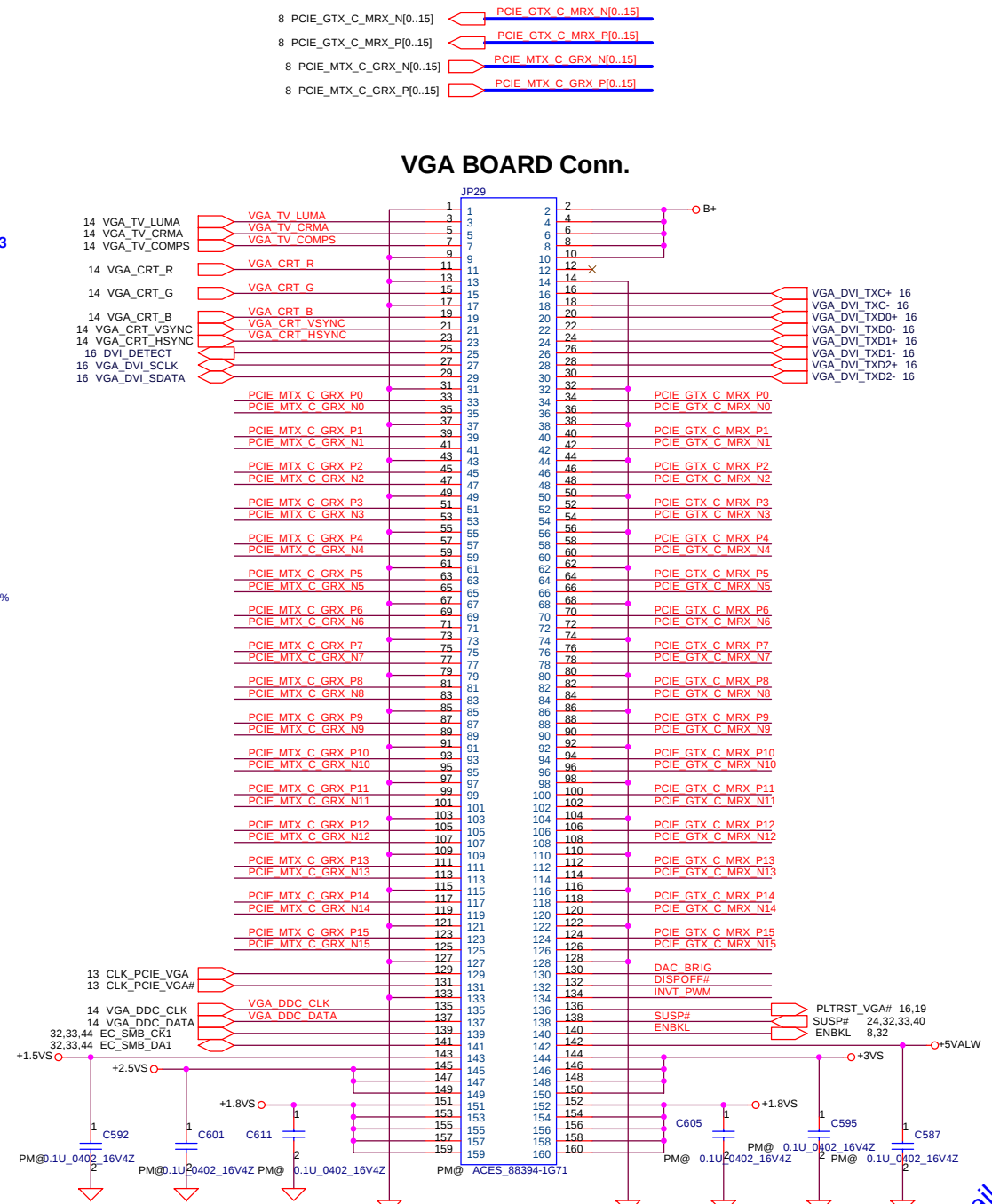
LCD POWER CIRCUIT



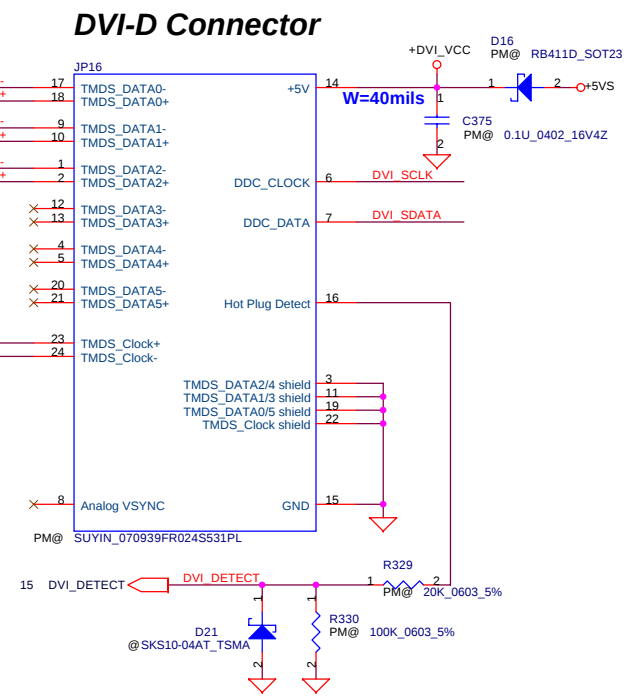
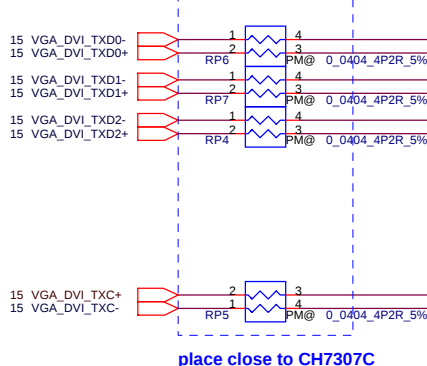
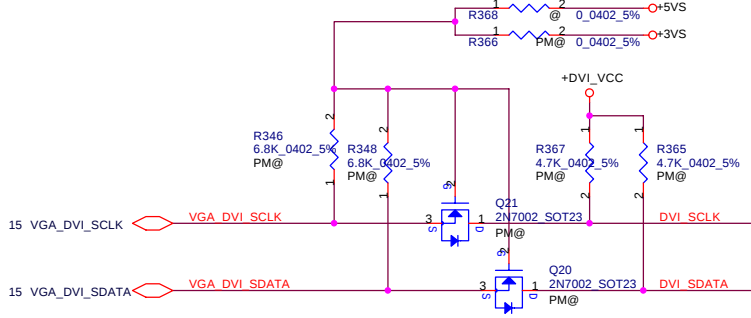
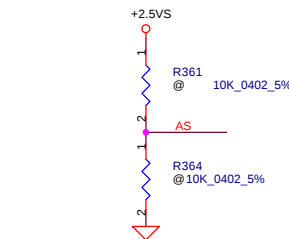
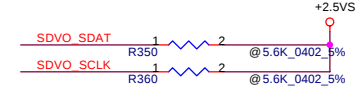
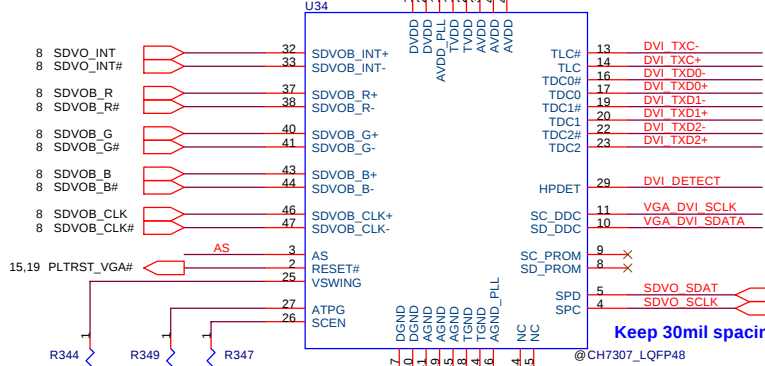
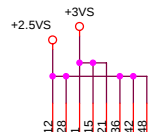
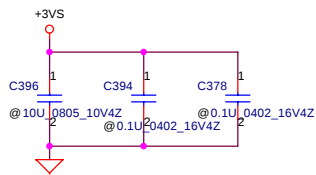
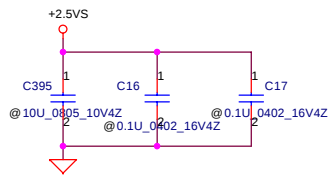
LCD Conn.



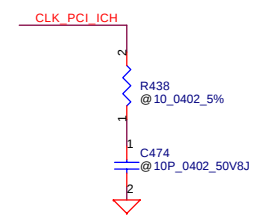
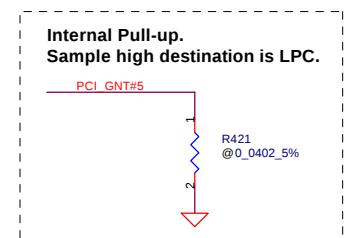
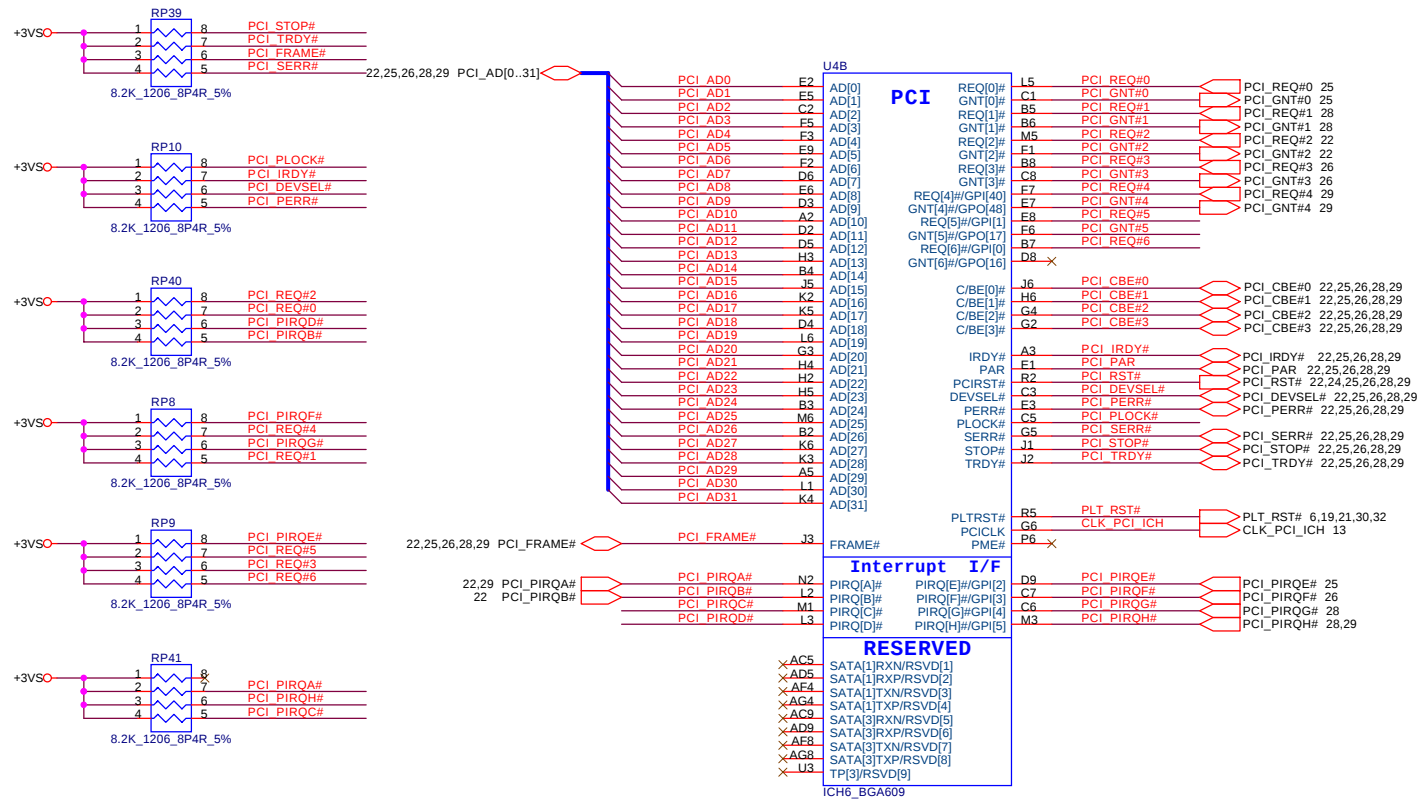
VGA BOARD Conn.



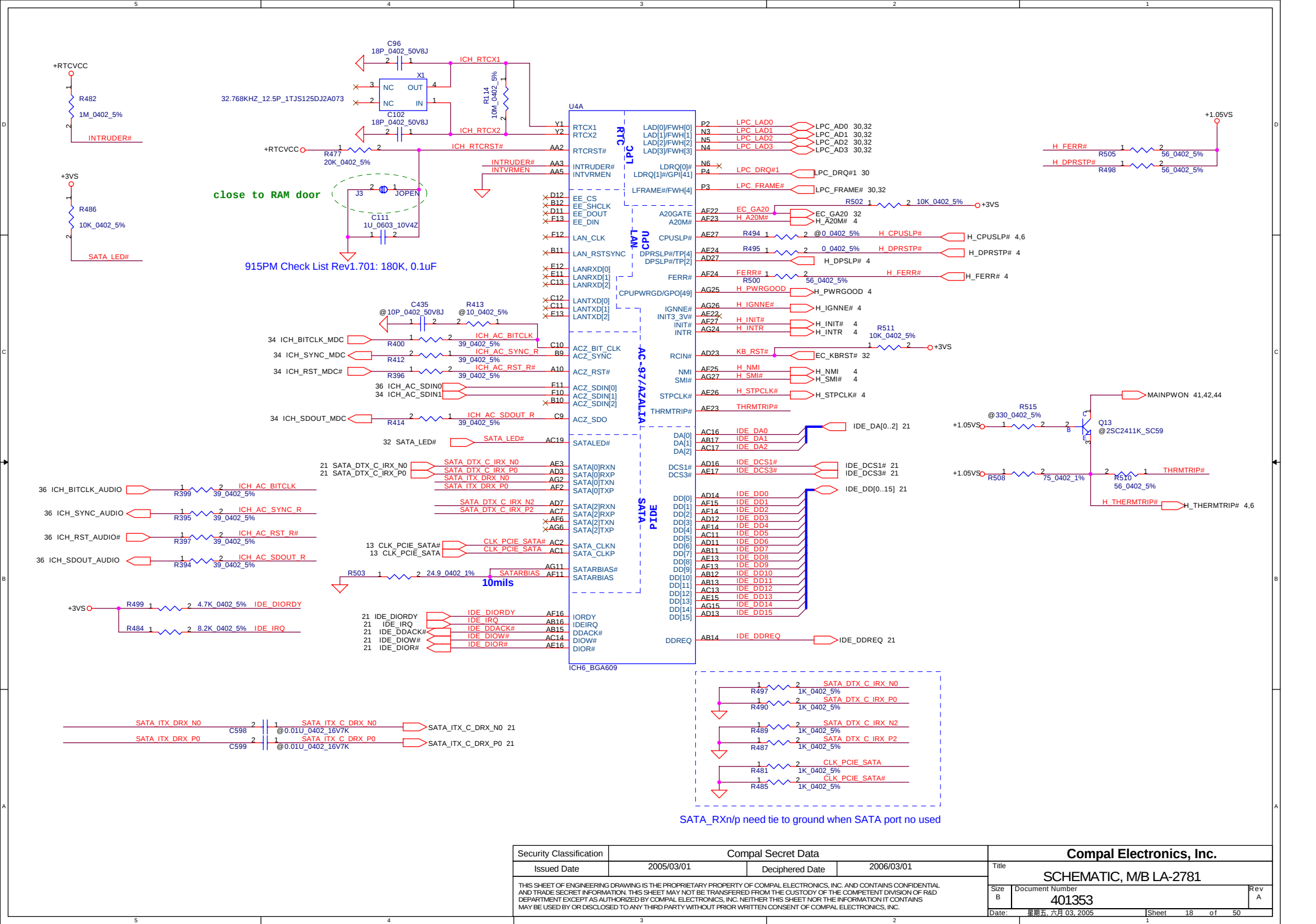
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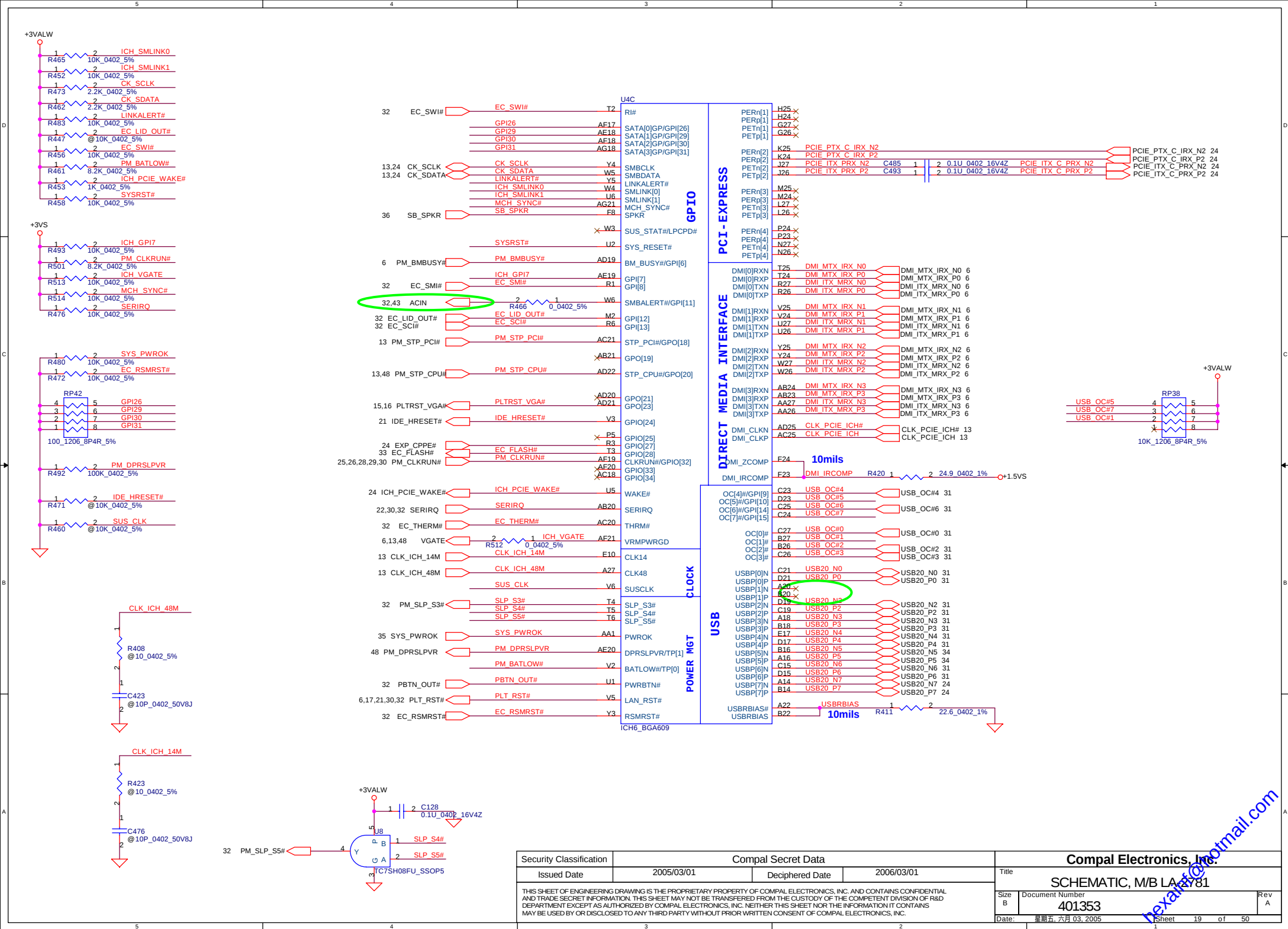
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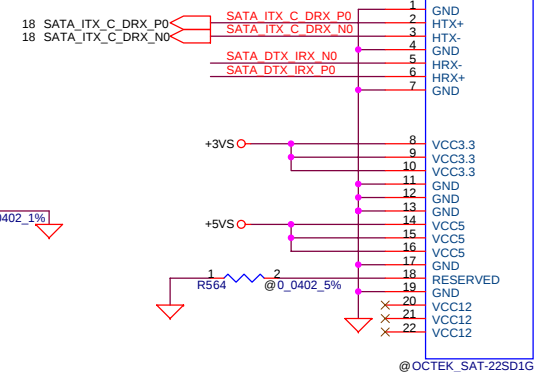
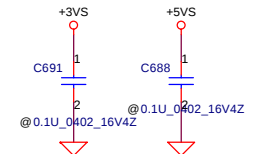
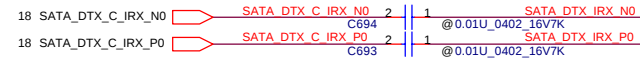
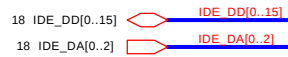


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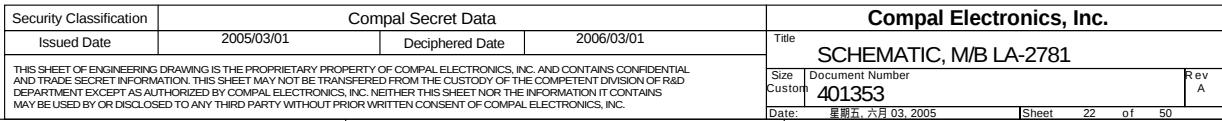
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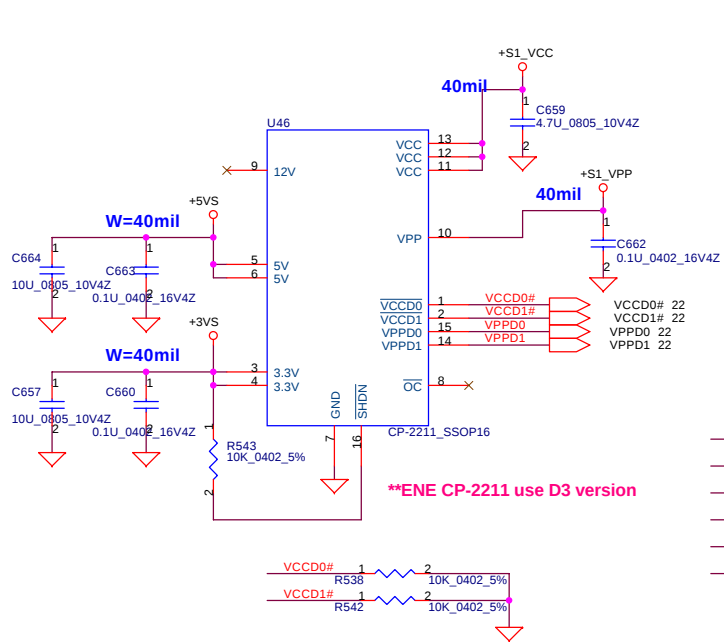


Remove the JP47 and C362,C366,C675,C678,C681

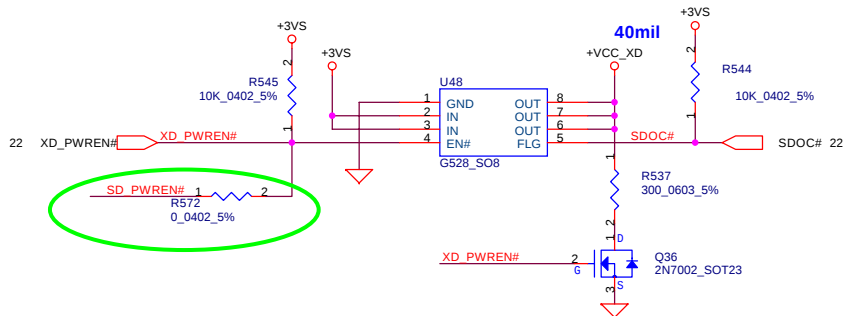
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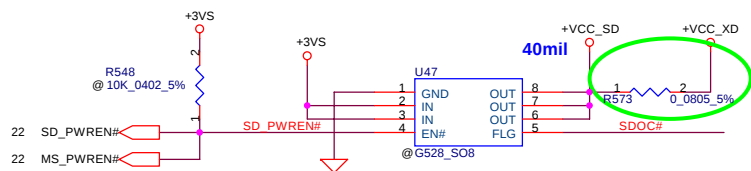
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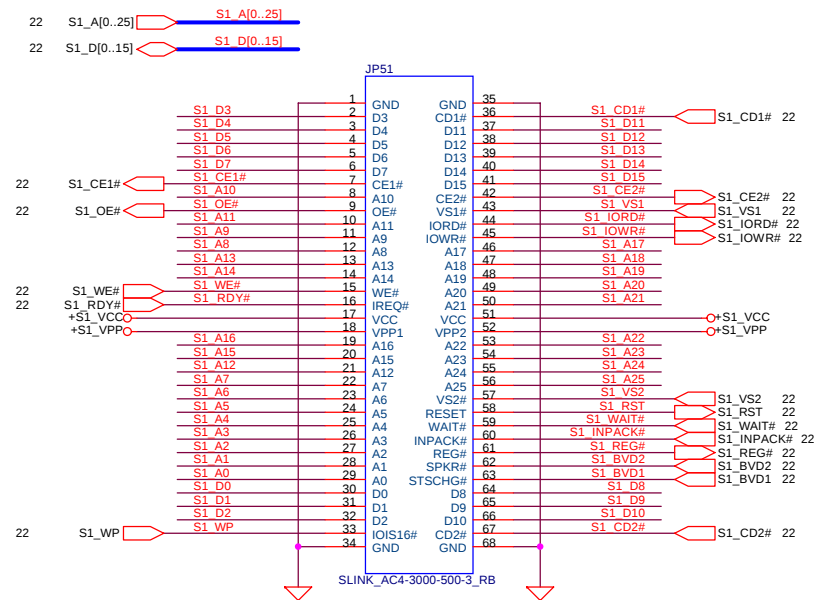
XD Power Control



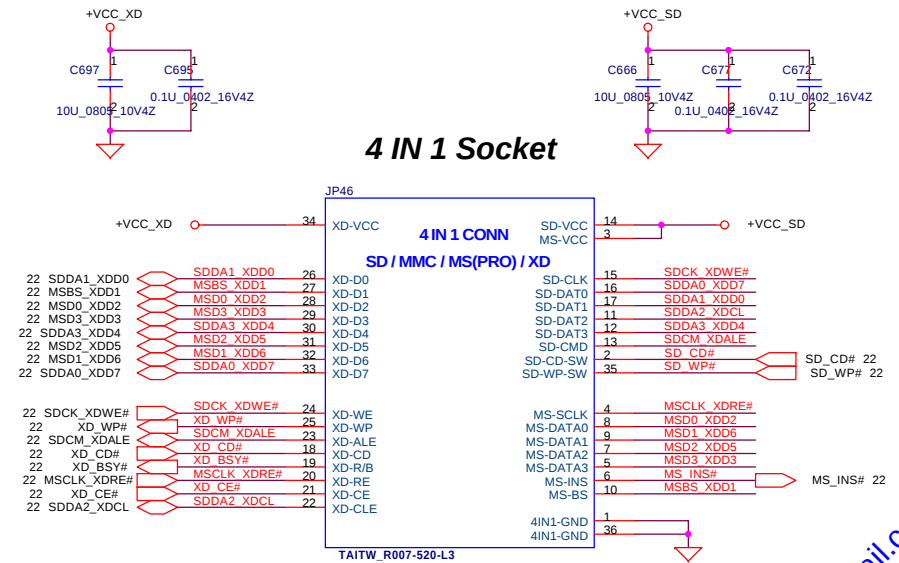
SD/MS Power Control



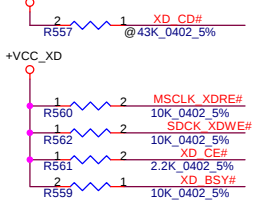
PCMCIA Socket



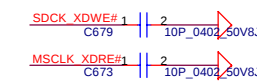
4 IN 1 Socket



xD PU and PD. Close to Socket

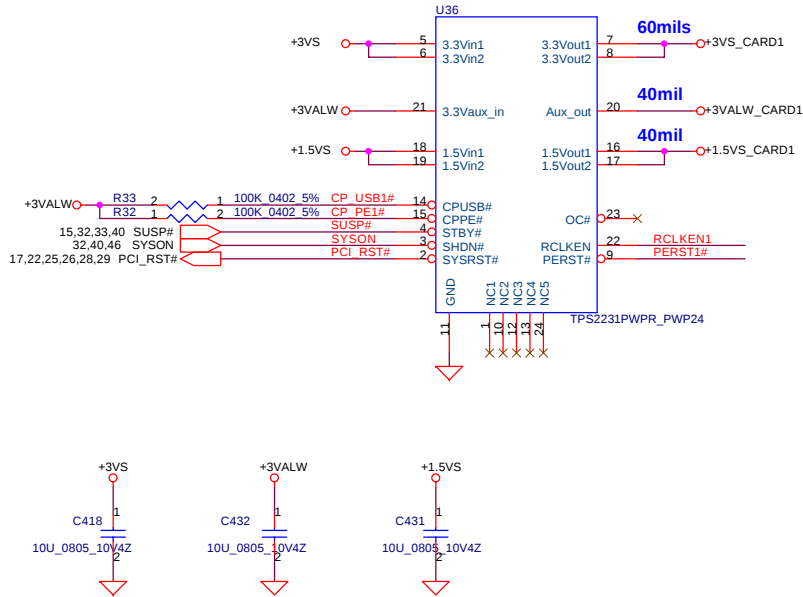


Reserve for SD,MS CLK.
Close to Socket

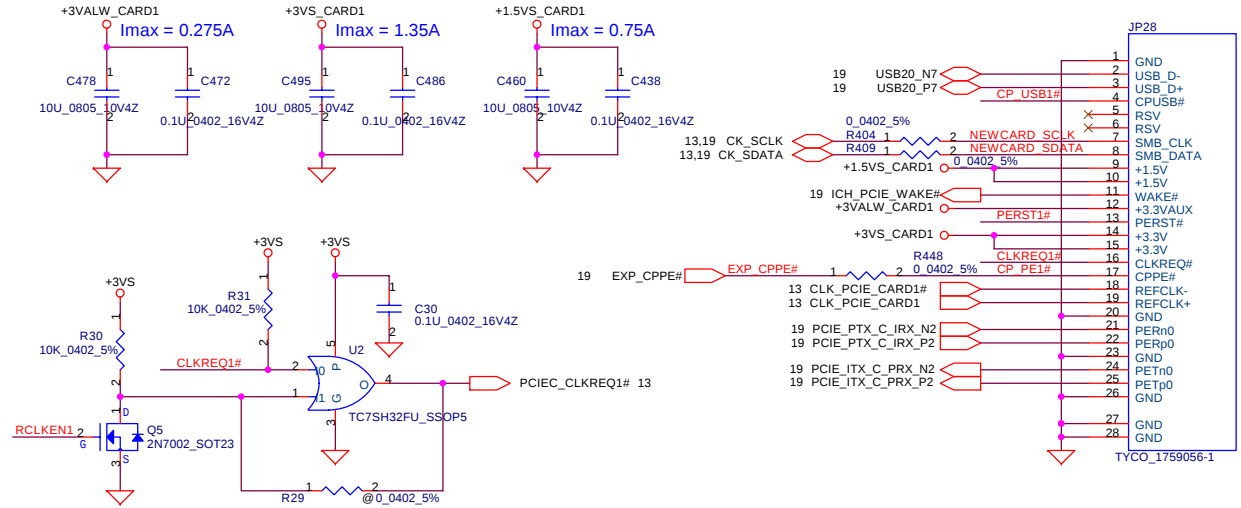


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New Card Power Switch

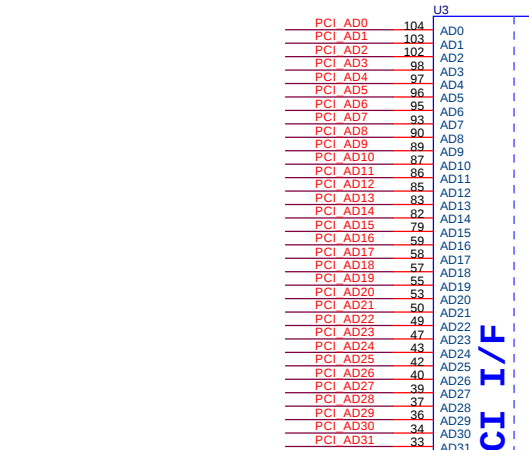


New Card Socket (Left)

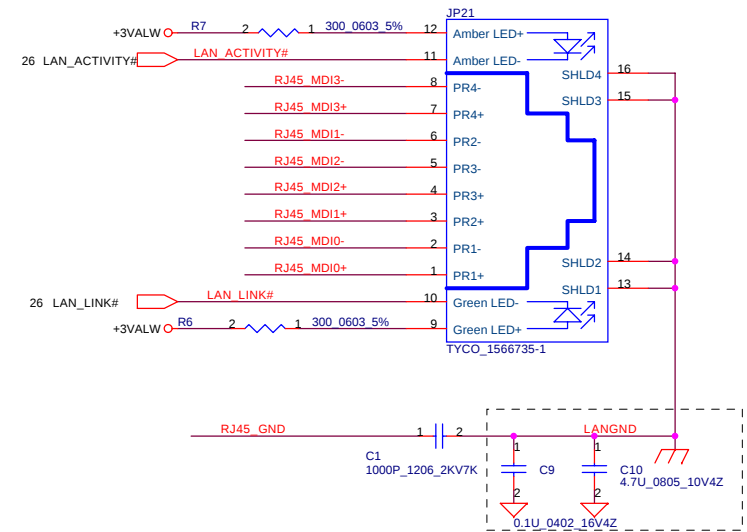
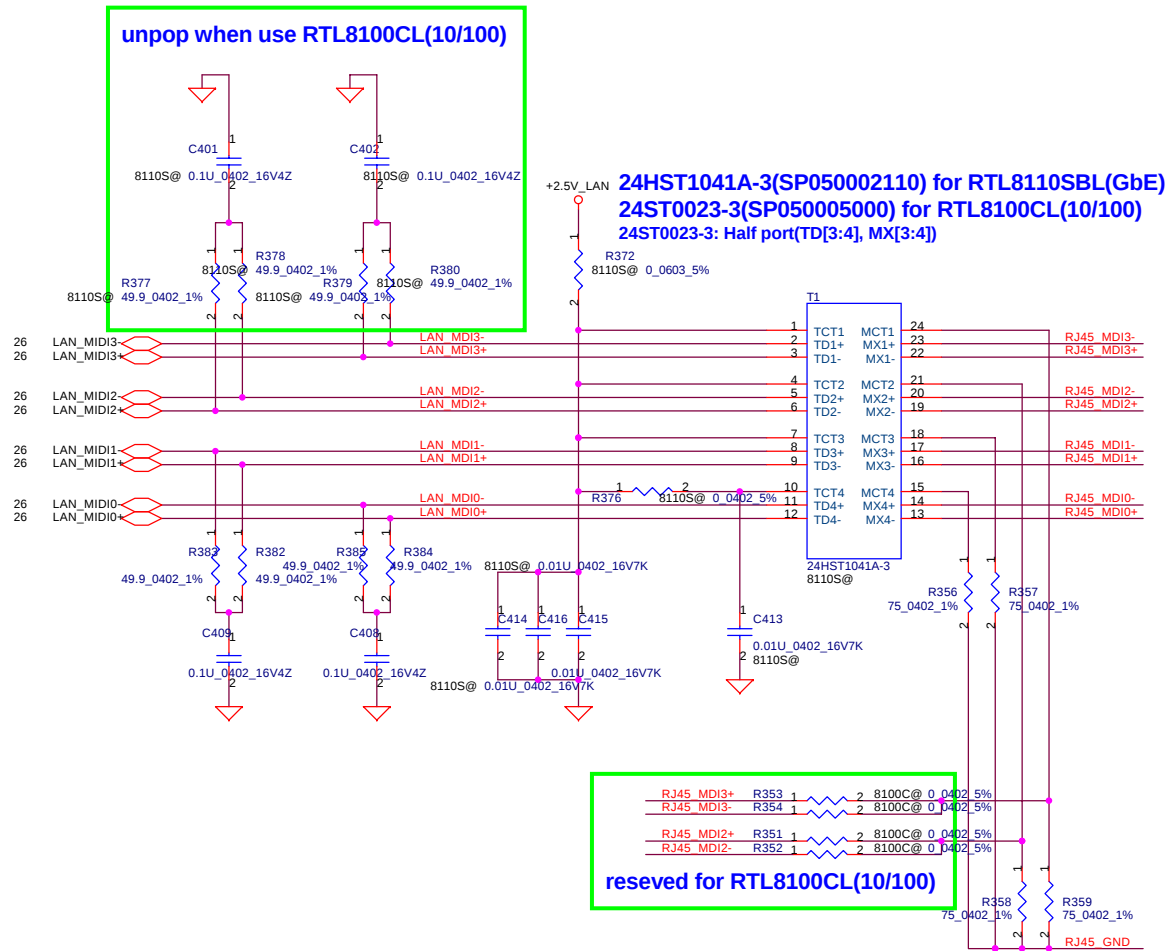


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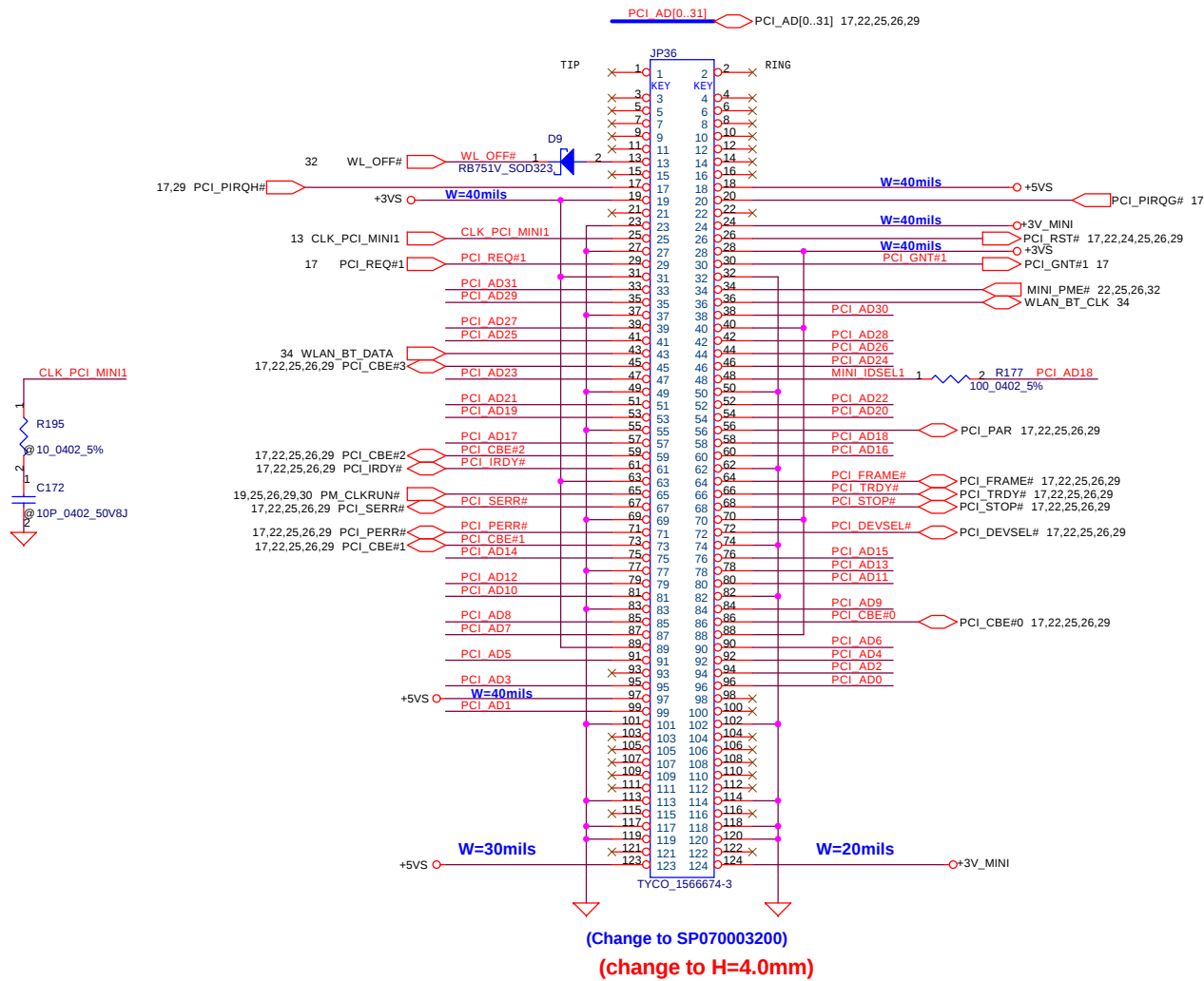
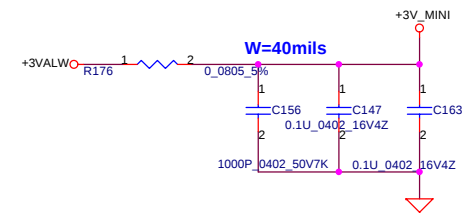
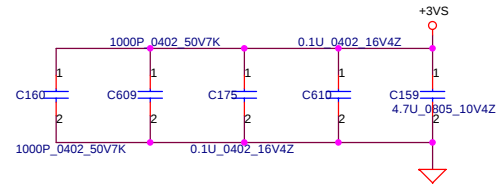
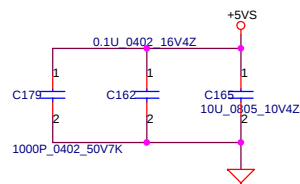
17,22,25,28,29 PCI_AD[0..31] PCI_AD[0..31]



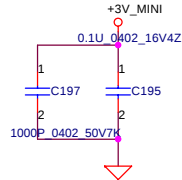
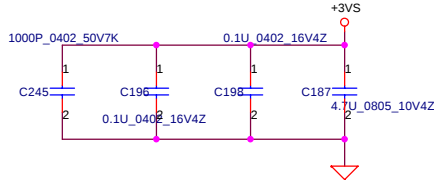
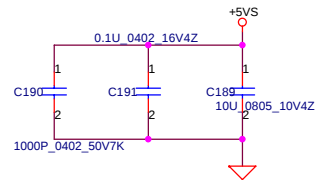
LAN RTL8110SBL/RTL8100CL



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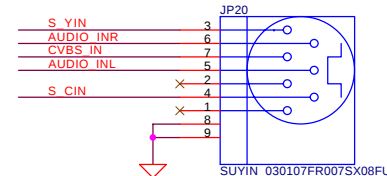


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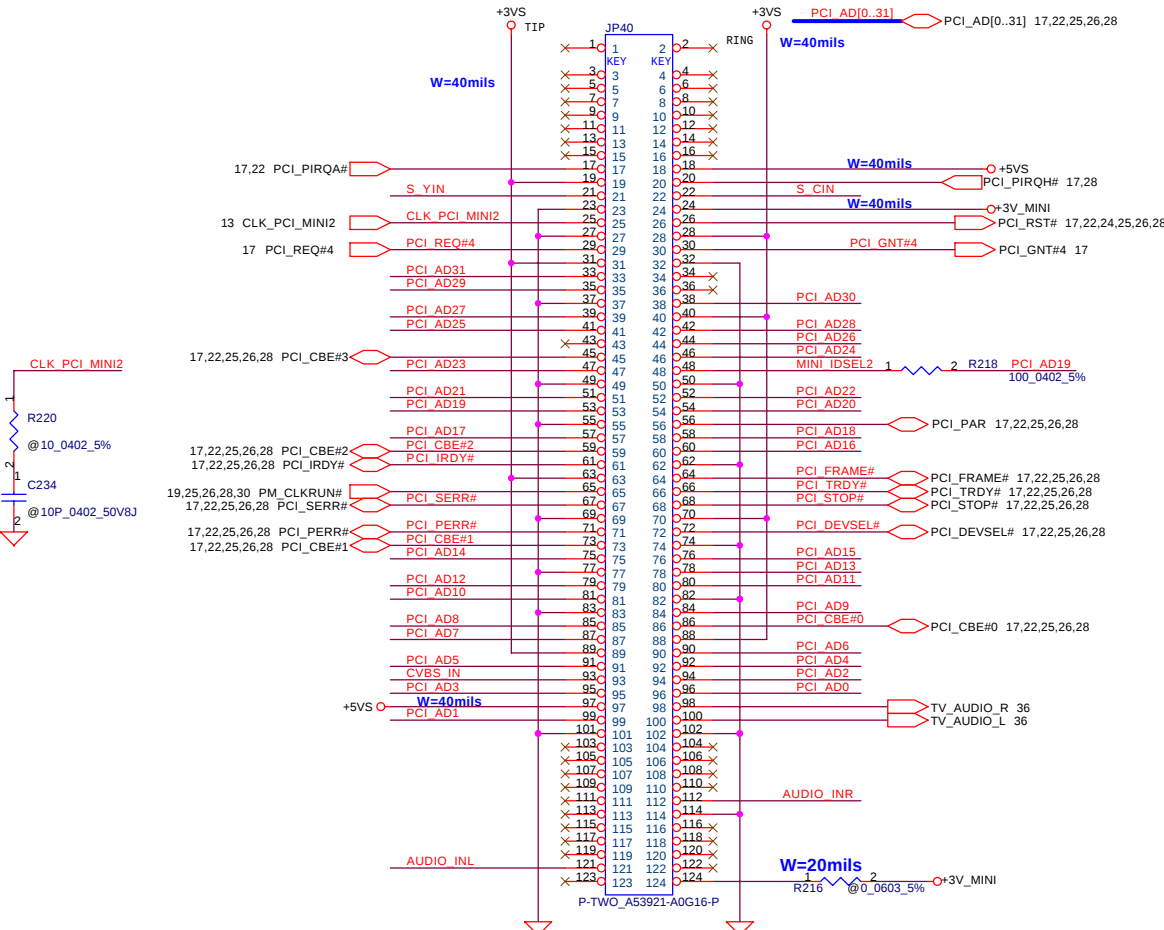


TV-Tuner

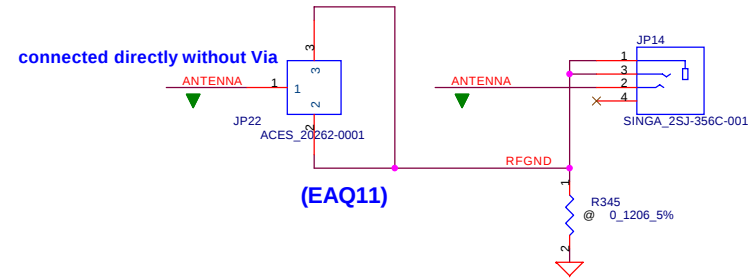
AV In



Acer TV-Tuner Design Guide Rev1.1
 1. N/A
 2. N/A
 3. S-Video - Y
 4. S-Video - C
 5. Audio - Left
 6. Audio - Right
 7. CVBS



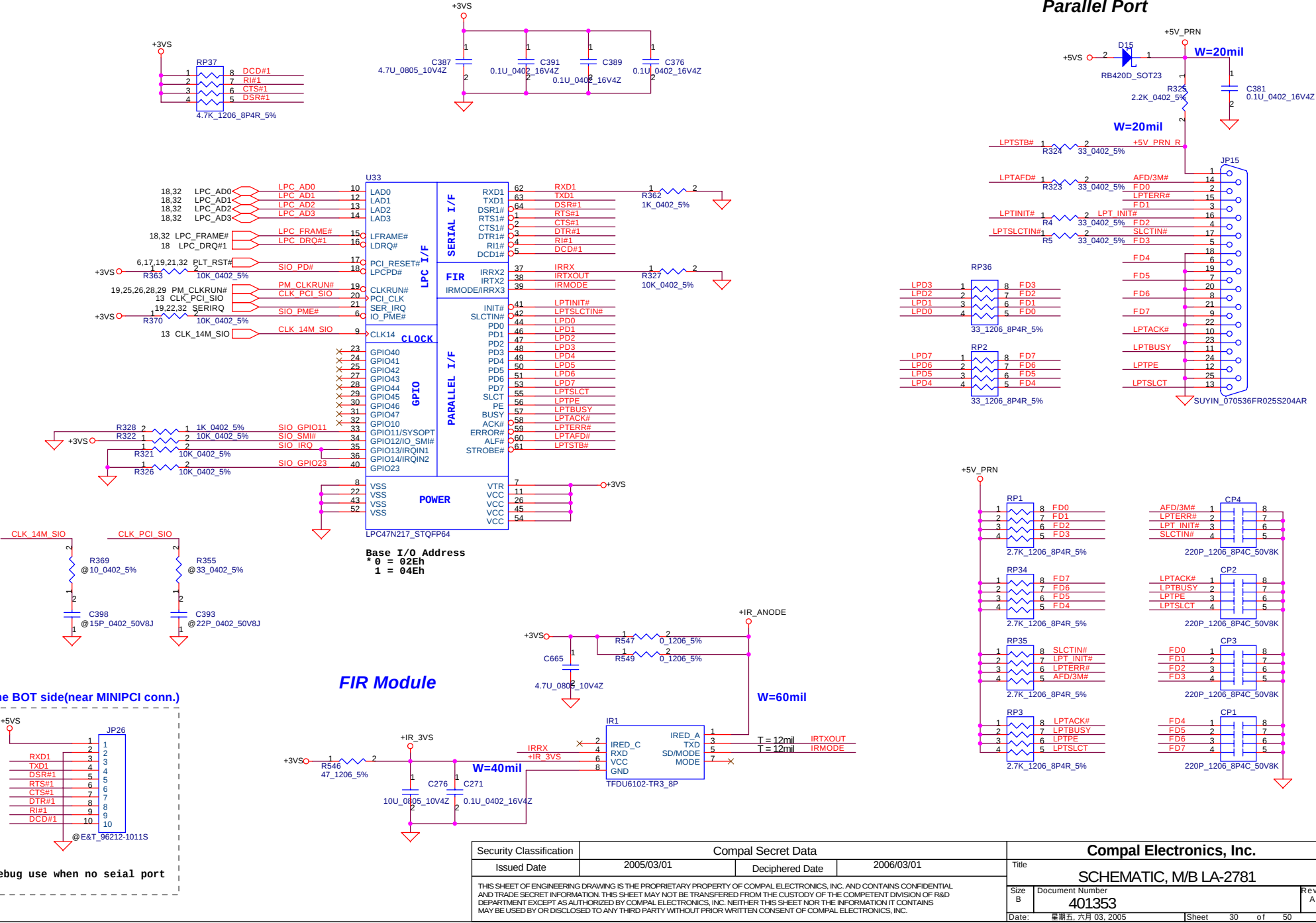
RF In



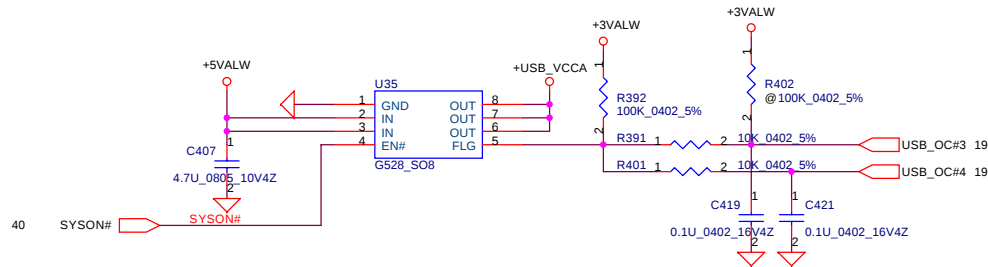
(EDL71 pin define)
 (For TV-Tuner change to H=9.2mm)

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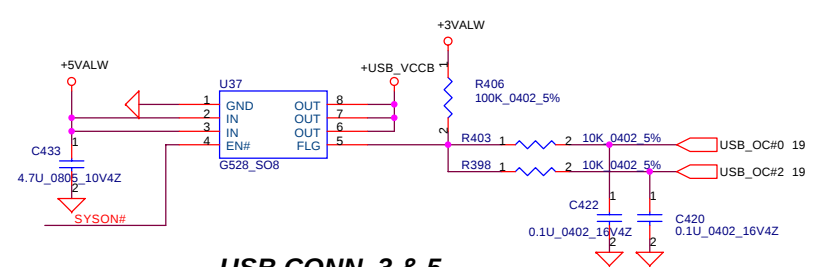
SUPER I/O SMC LPC47N217



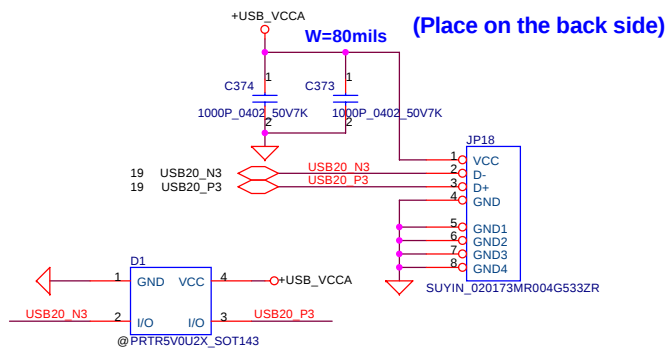
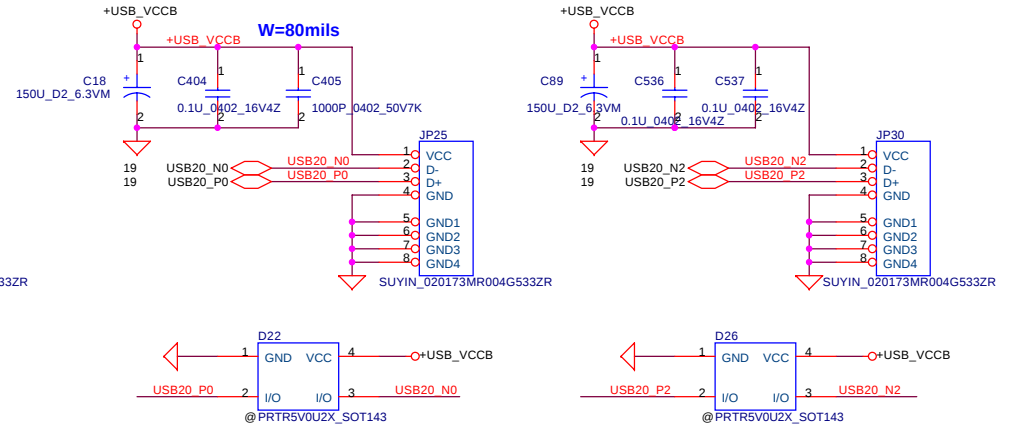
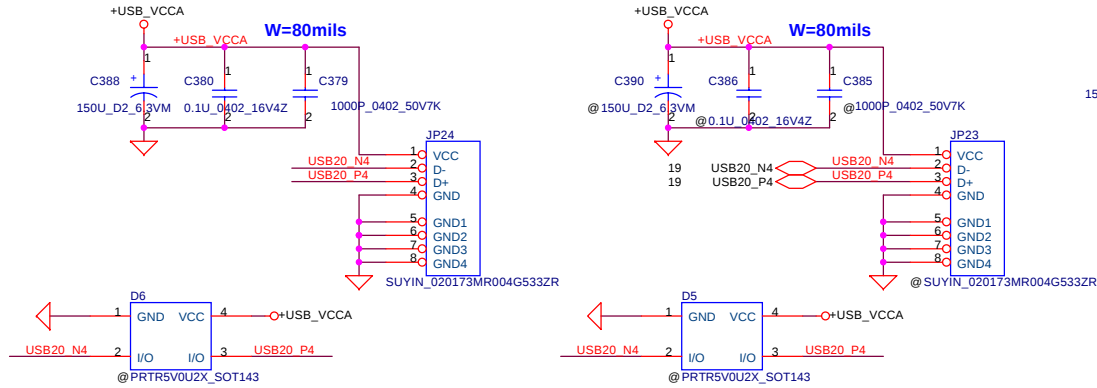
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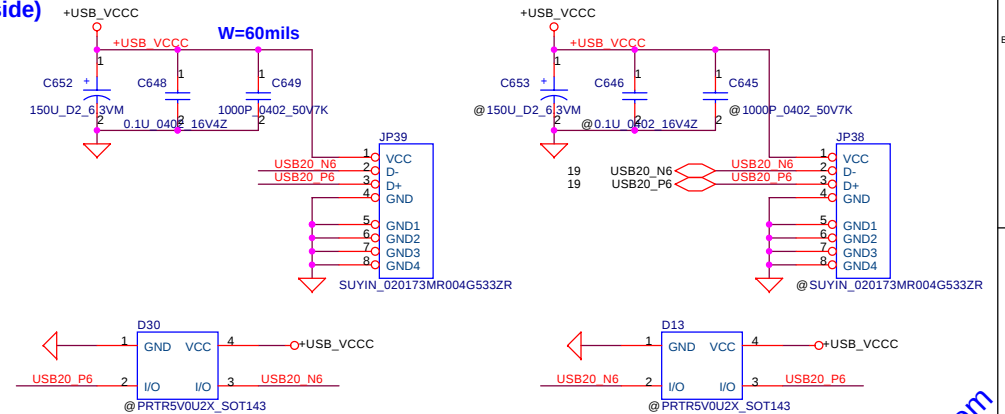
USB CONN. 1 & 2
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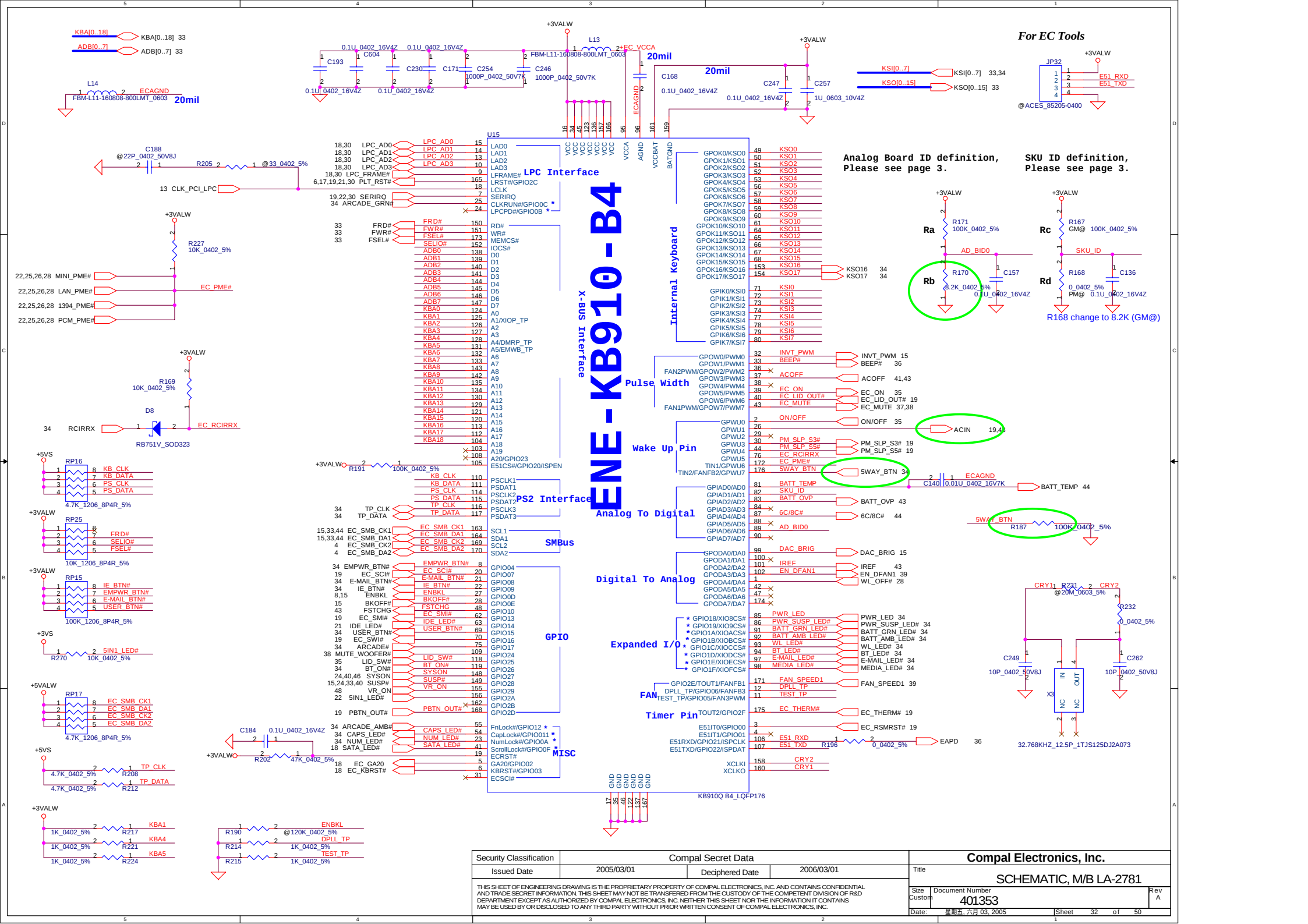
USB CONN. 3 & 5
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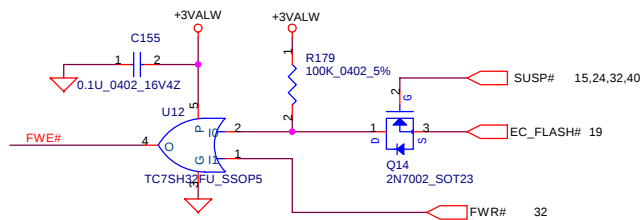


USB CONN. 5
(Place on the left-front side)



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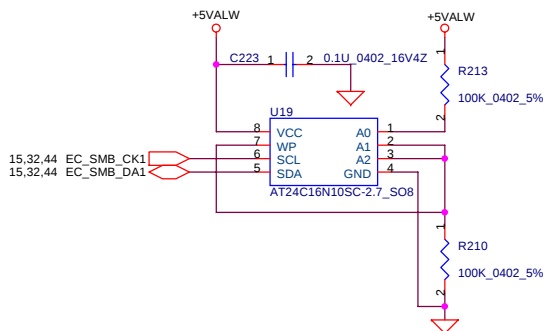
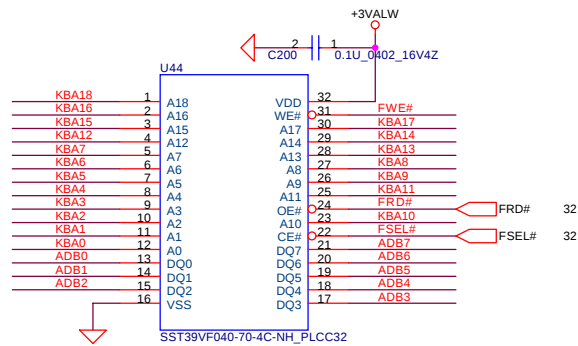




512KB Flash ROM

32 KBA[0..18] KBA[0..18]

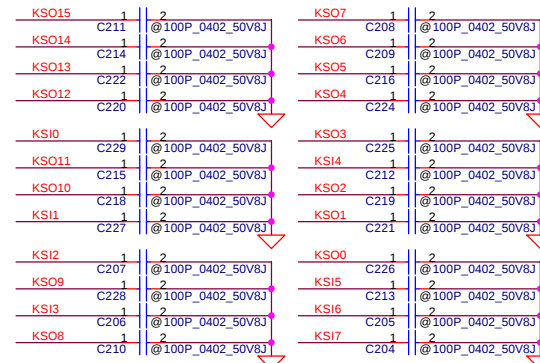
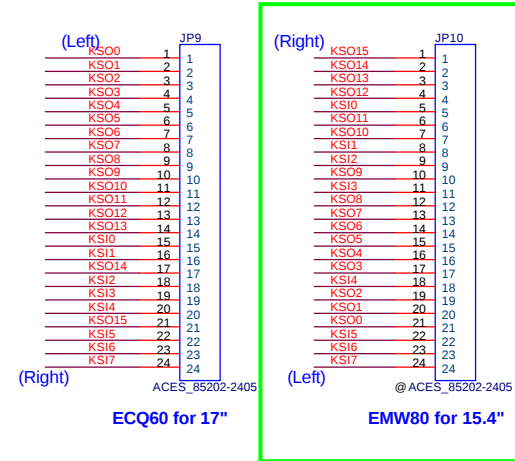
32 ADB[0..7] ADB[0..7]



INT_KBD Conn.

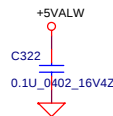
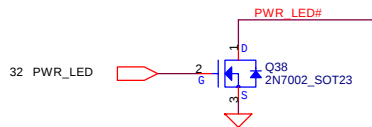
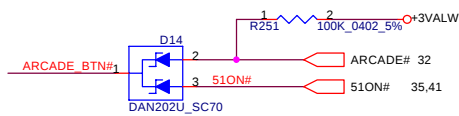
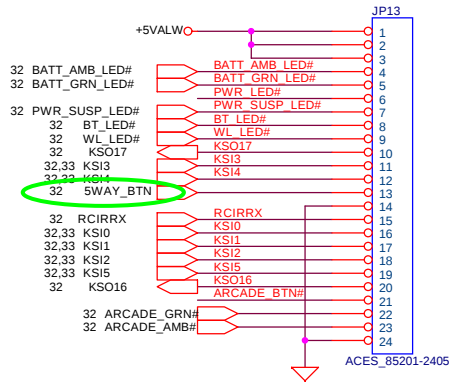
KSI[0..7] KSI[0..7] 32,34

KSO[0..15] KSO[0..15] 32



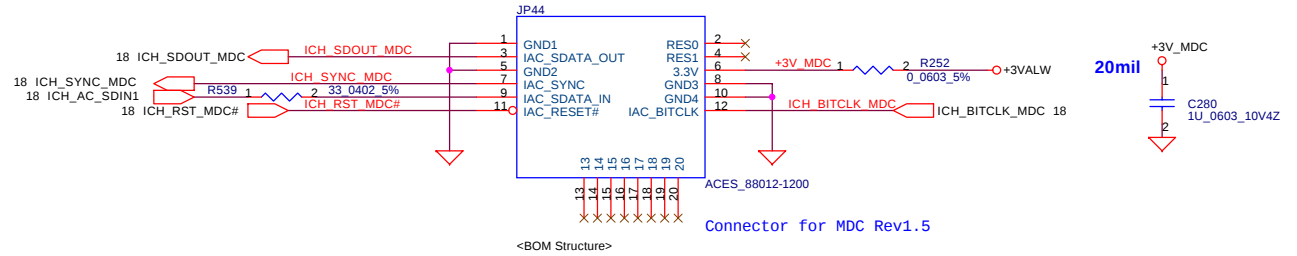
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To Media/B Conn.

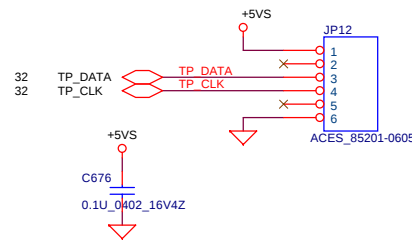


	KSO16	KSO17
KSI0	VOL_UP	LEFT
KSI1	RIGHT	VOL_DOWN
KSI2	PLAY	ENTER
KSI3	STOP	BT_EN#
KSI4	REV	WL_EN#
KSI5	NEXT	

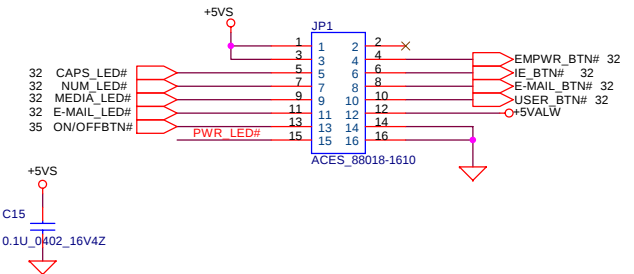
MDC Conn.



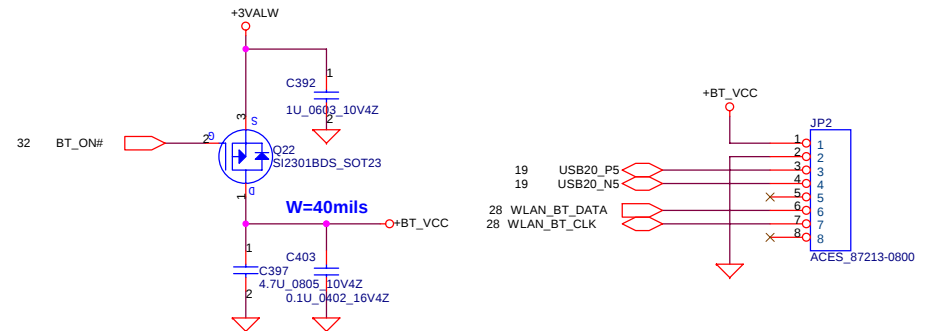
To TP/B Conn.



To LED/B Conn.

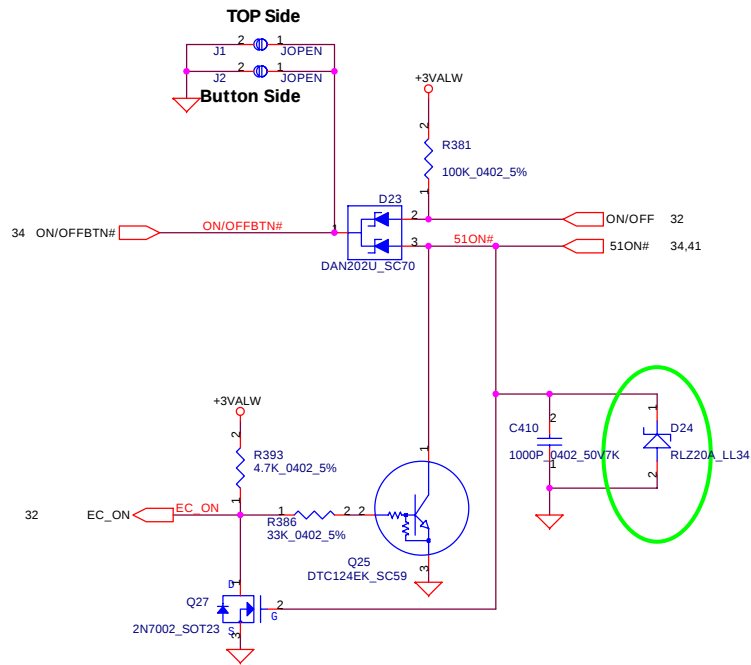


Bluetooth Conn.

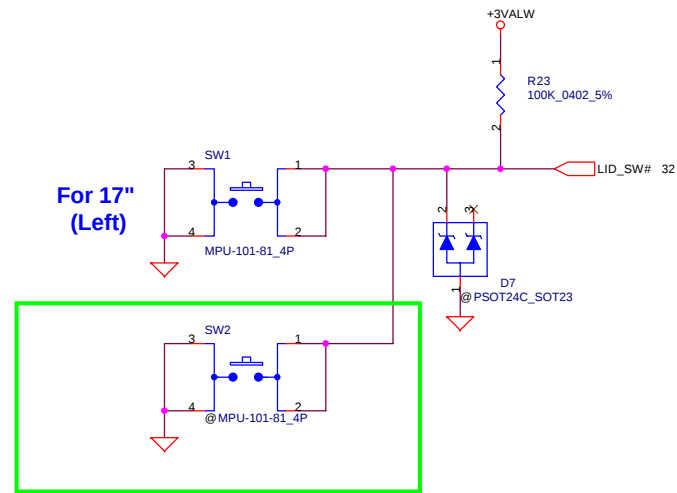


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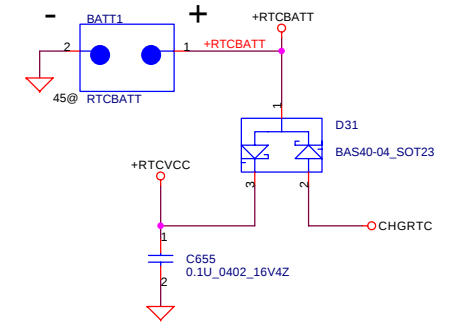
ON/OFF switch



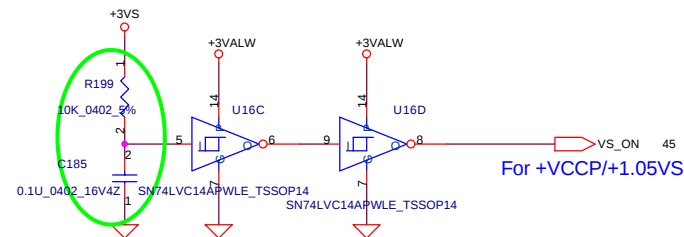
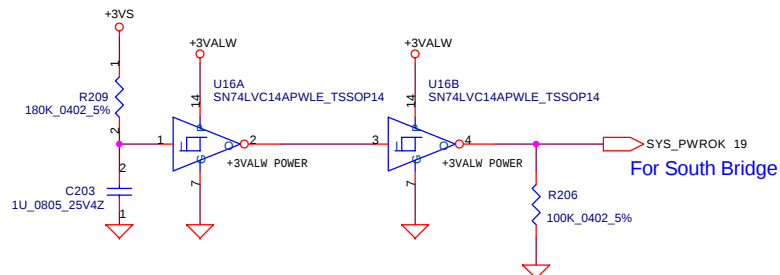
Lid Switch



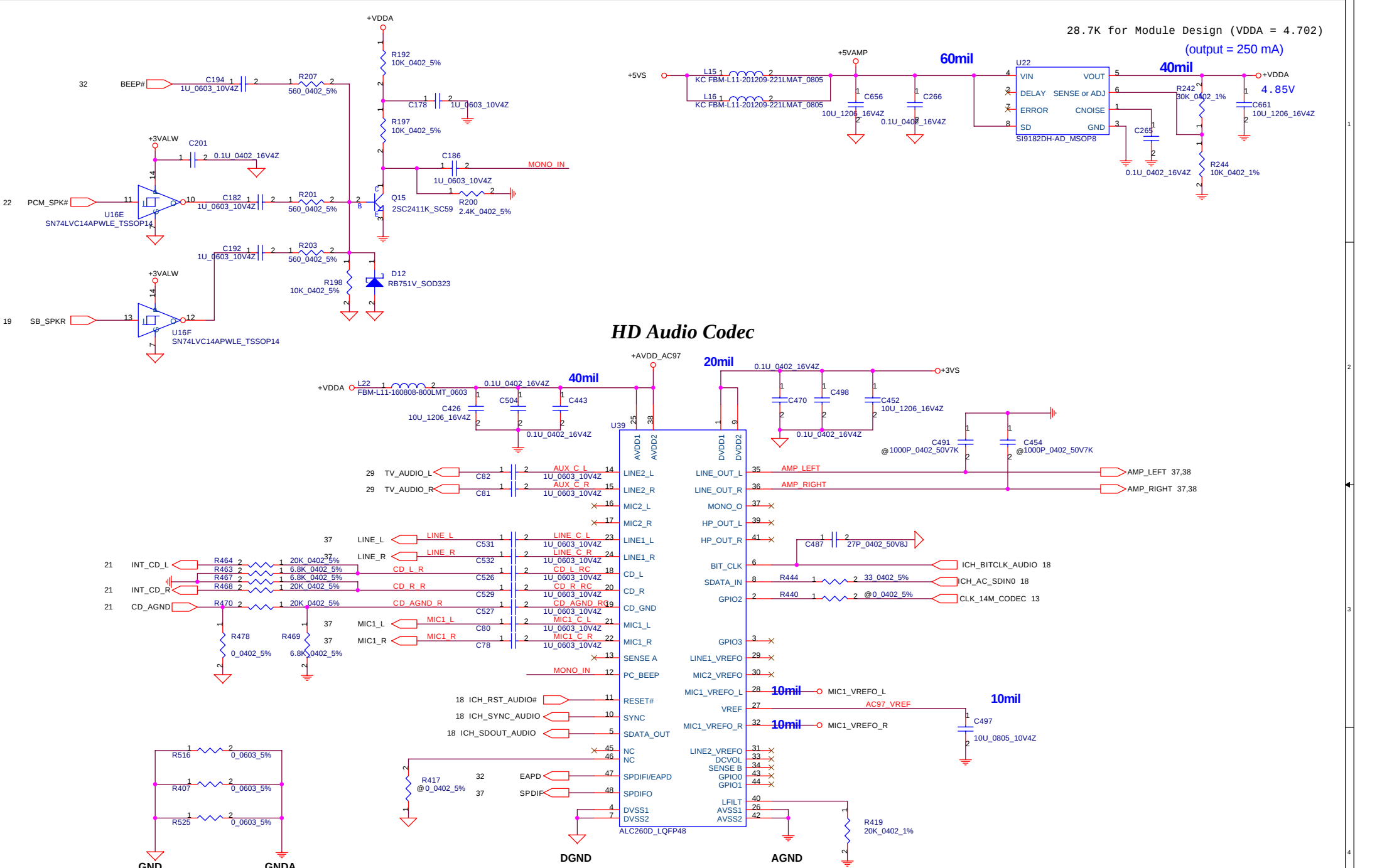
RTC Battery



Power ON Circuit

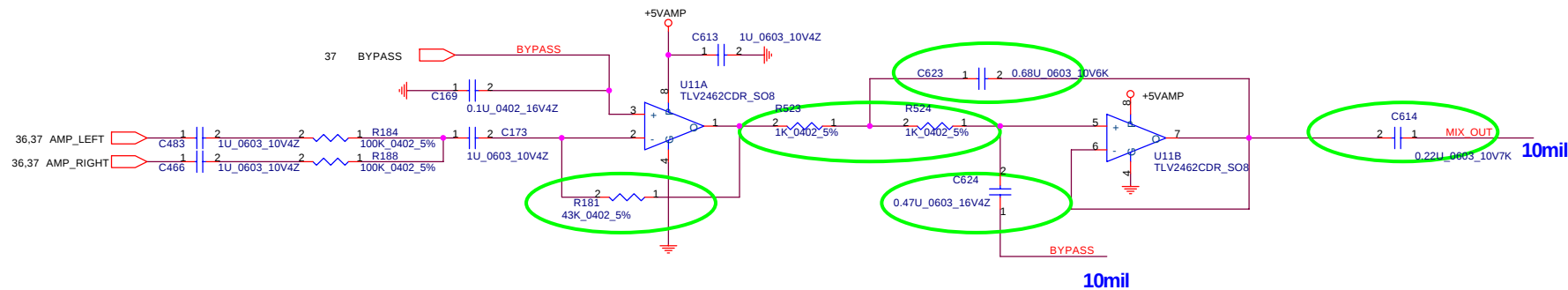


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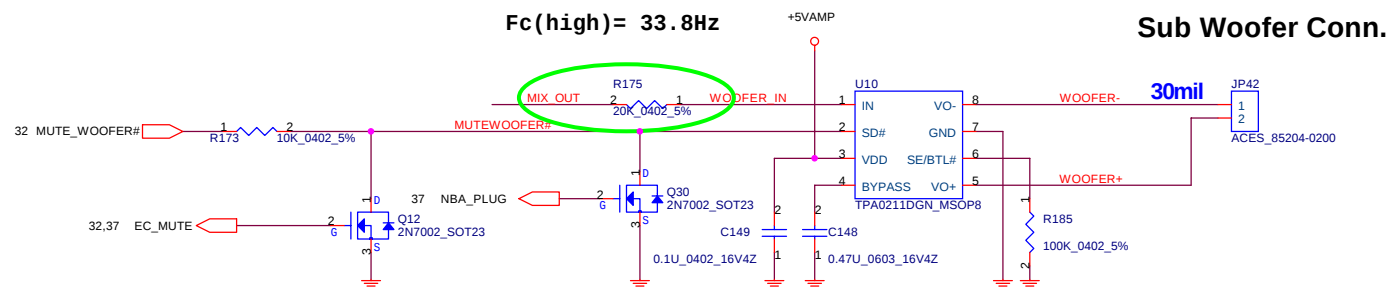


HD Audio Codec

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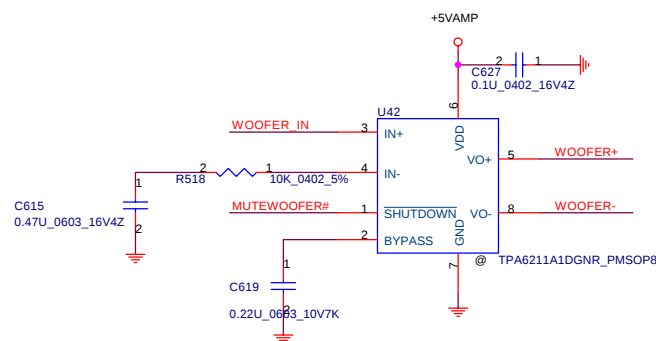


$f_0 = 725 \text{ Hz}$



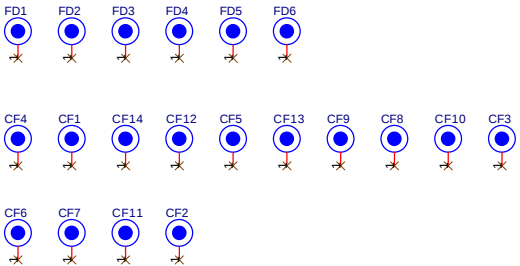
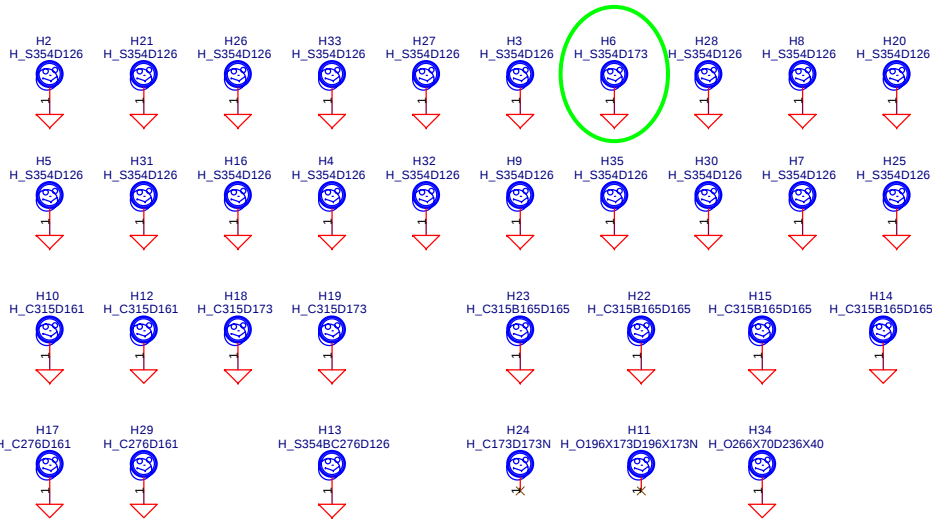
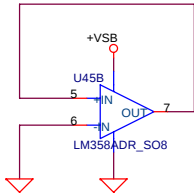
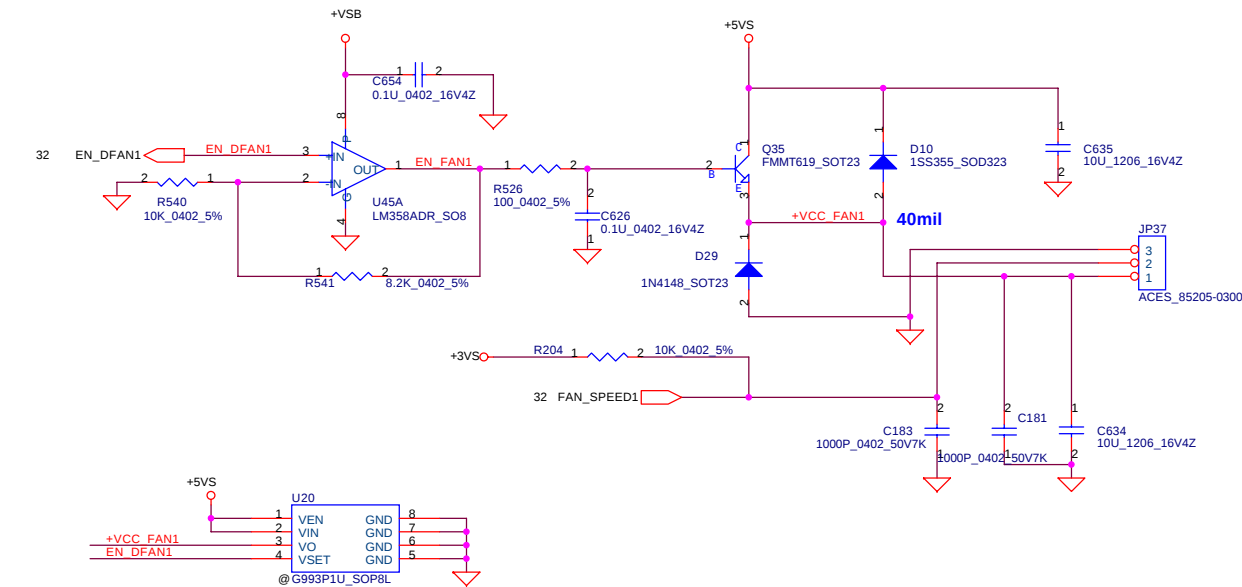
$F_c(\text{high}) = 33.8 \text{ Hz}$

Sub Woofer Conn.

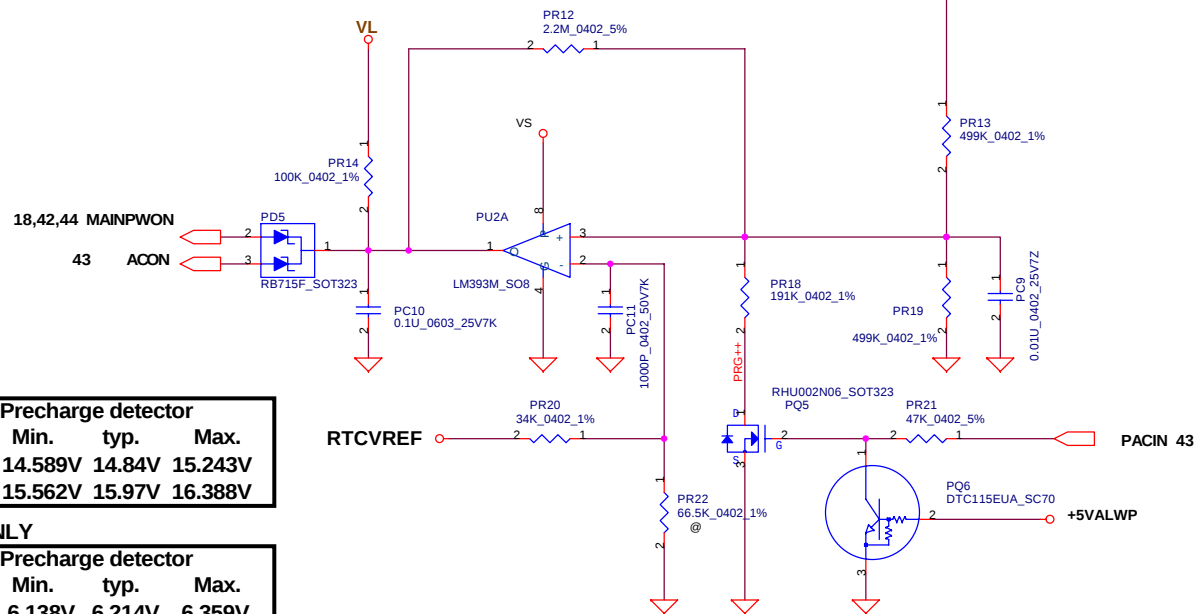
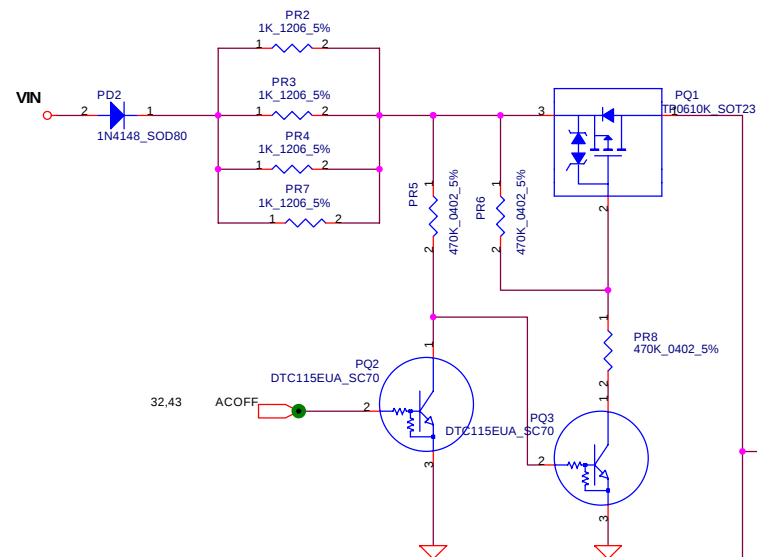
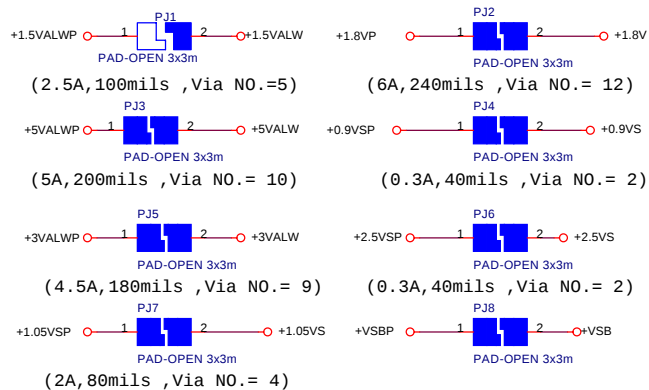
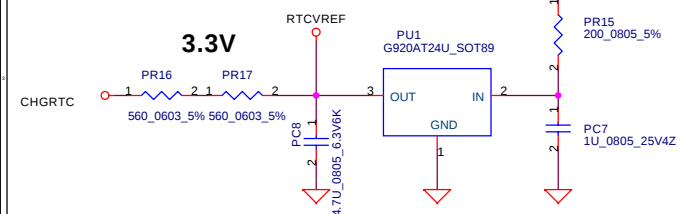
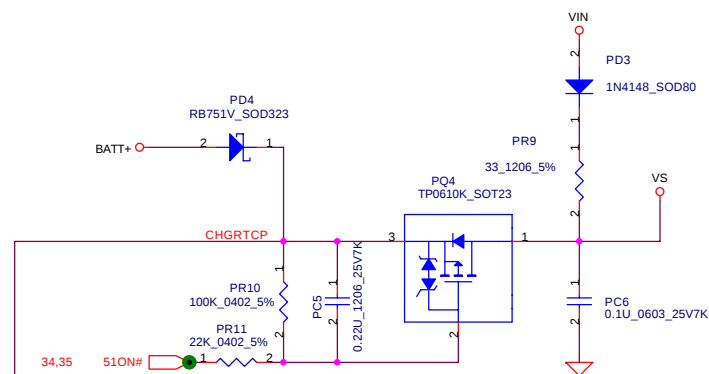
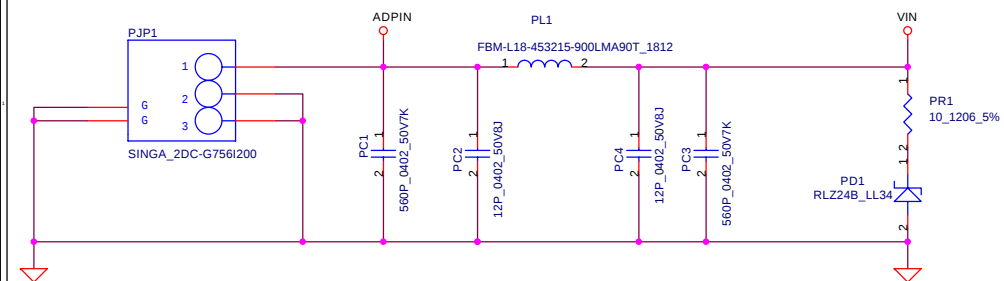


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FAN Conn



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ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

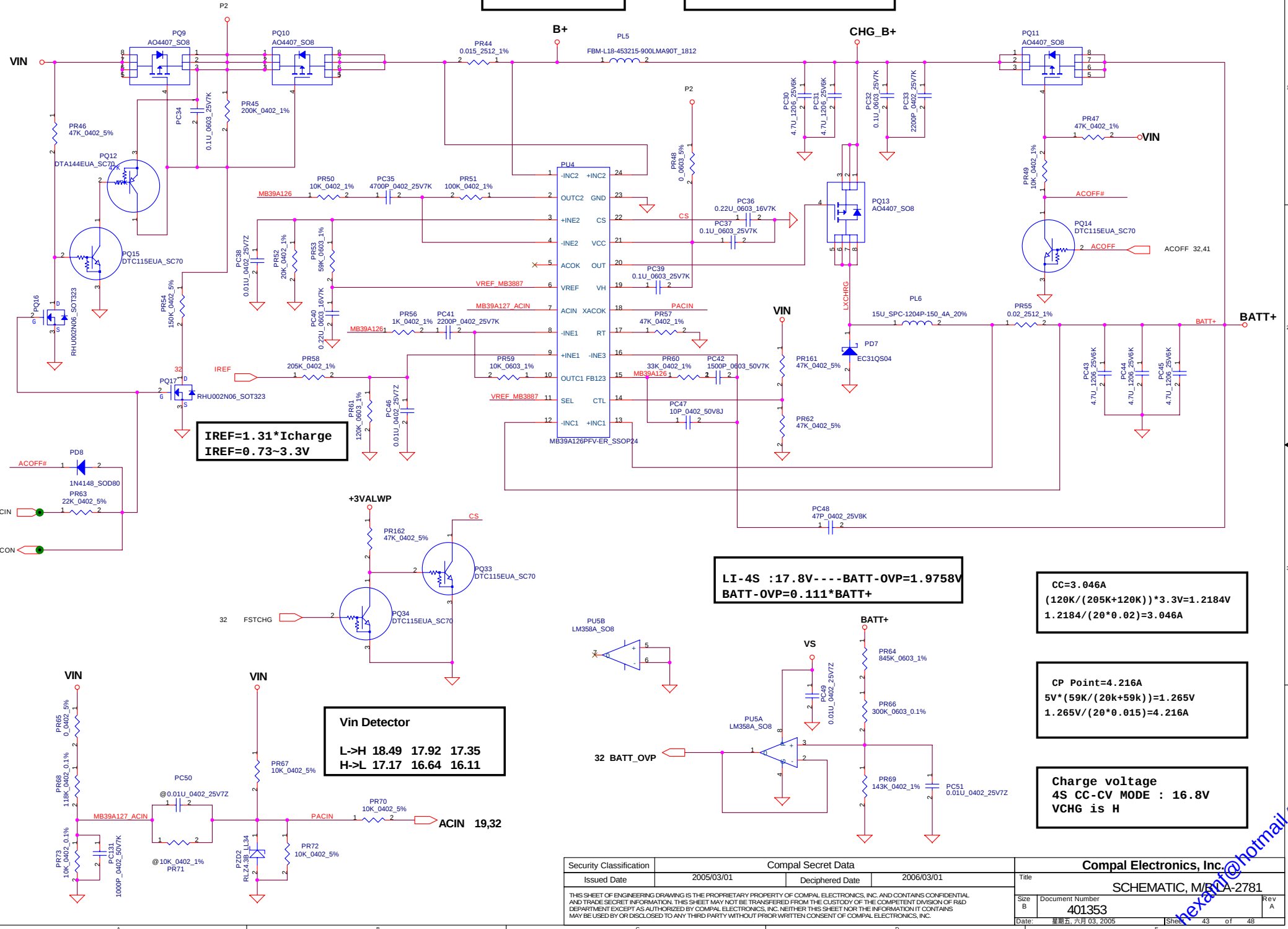
Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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Iadp=0~4.74A(90W)

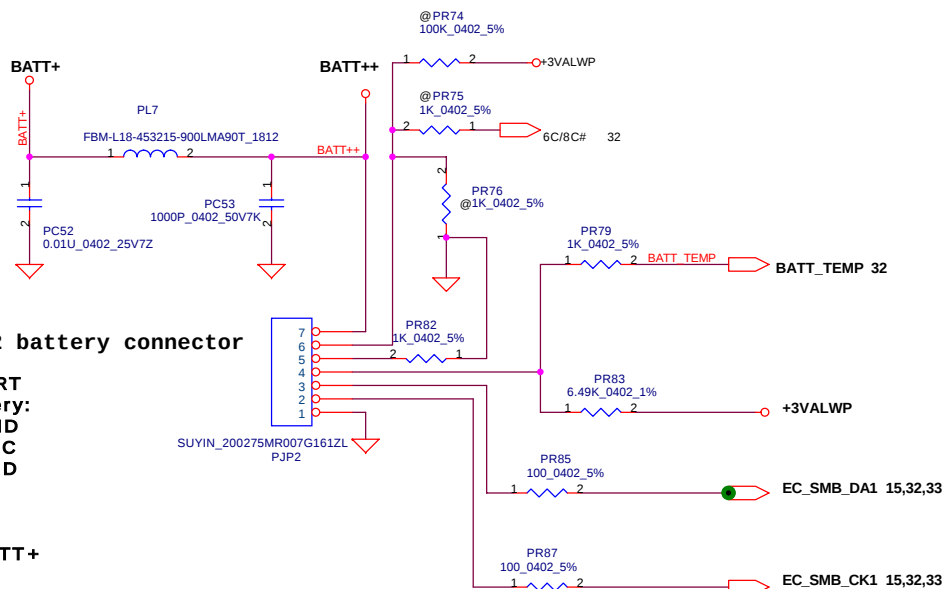
Fosc=14100/Rt=14100/47=300KHz

Charger

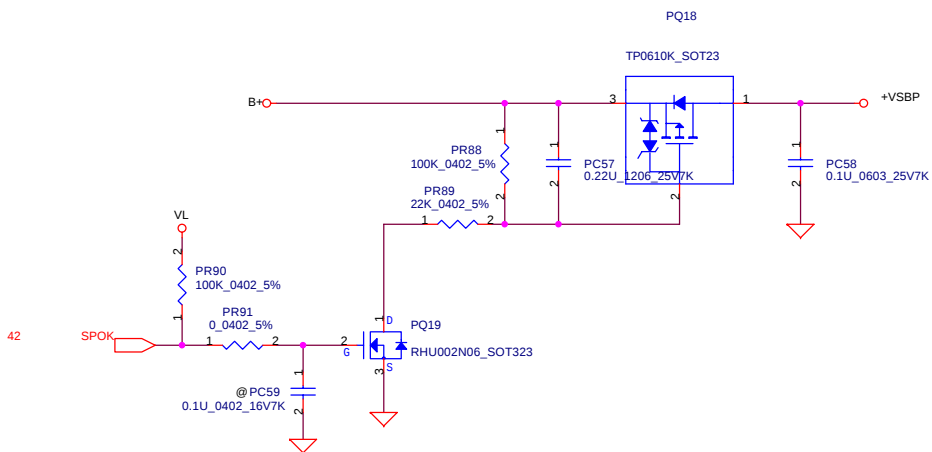
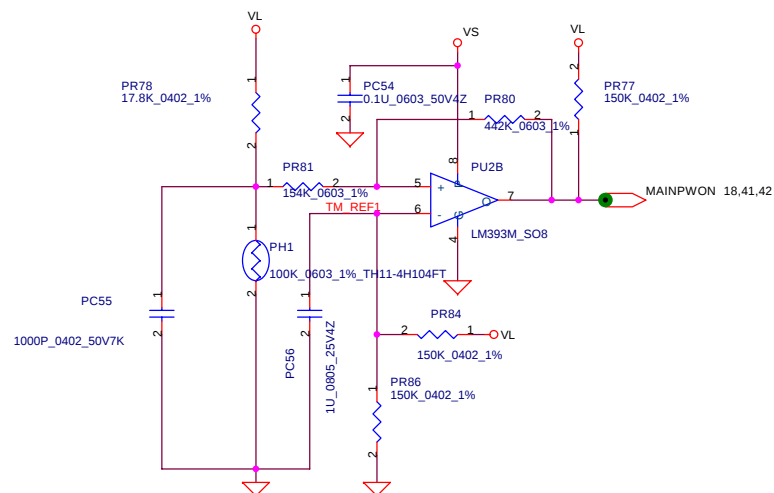


PJP2 battery connector

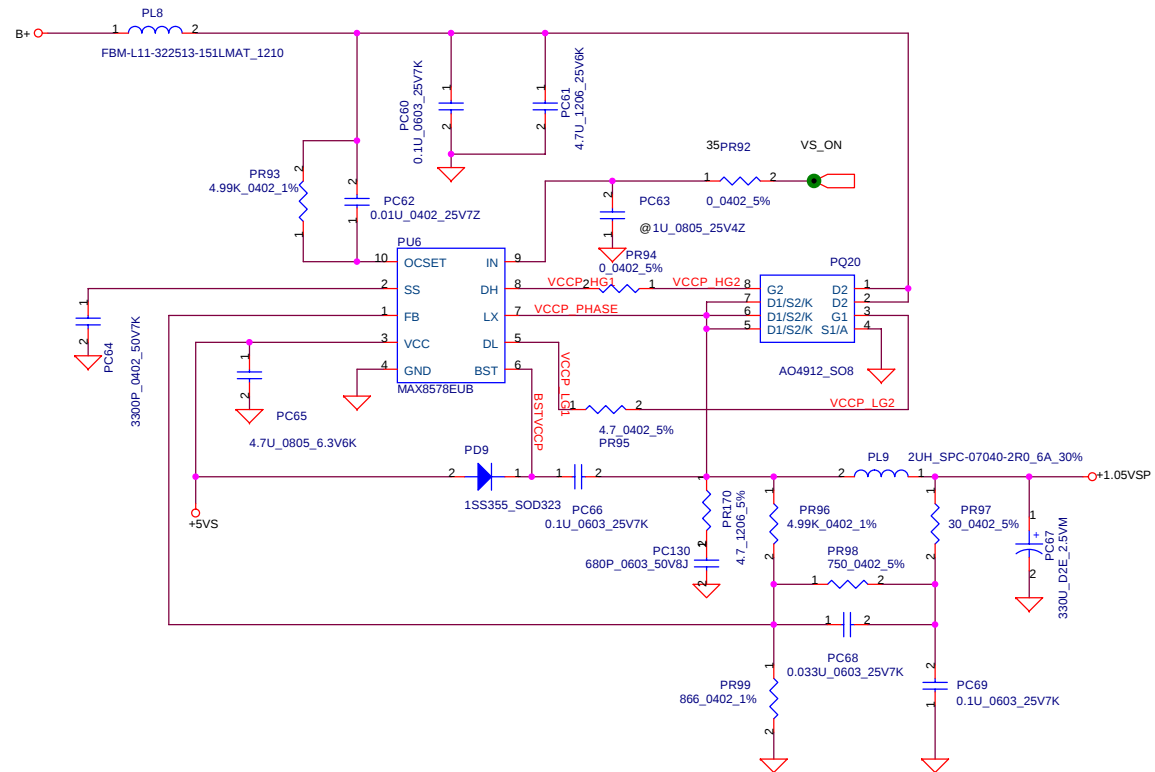
SMART Battery:
1.GND
2.SMC
3.SMD
4.TS
5.B/I
6.ID
7.BATT+



PH1 under CPU bottom side :
 CPU thermal protection at 80 degree C
 Recovery at 44(45) degree C

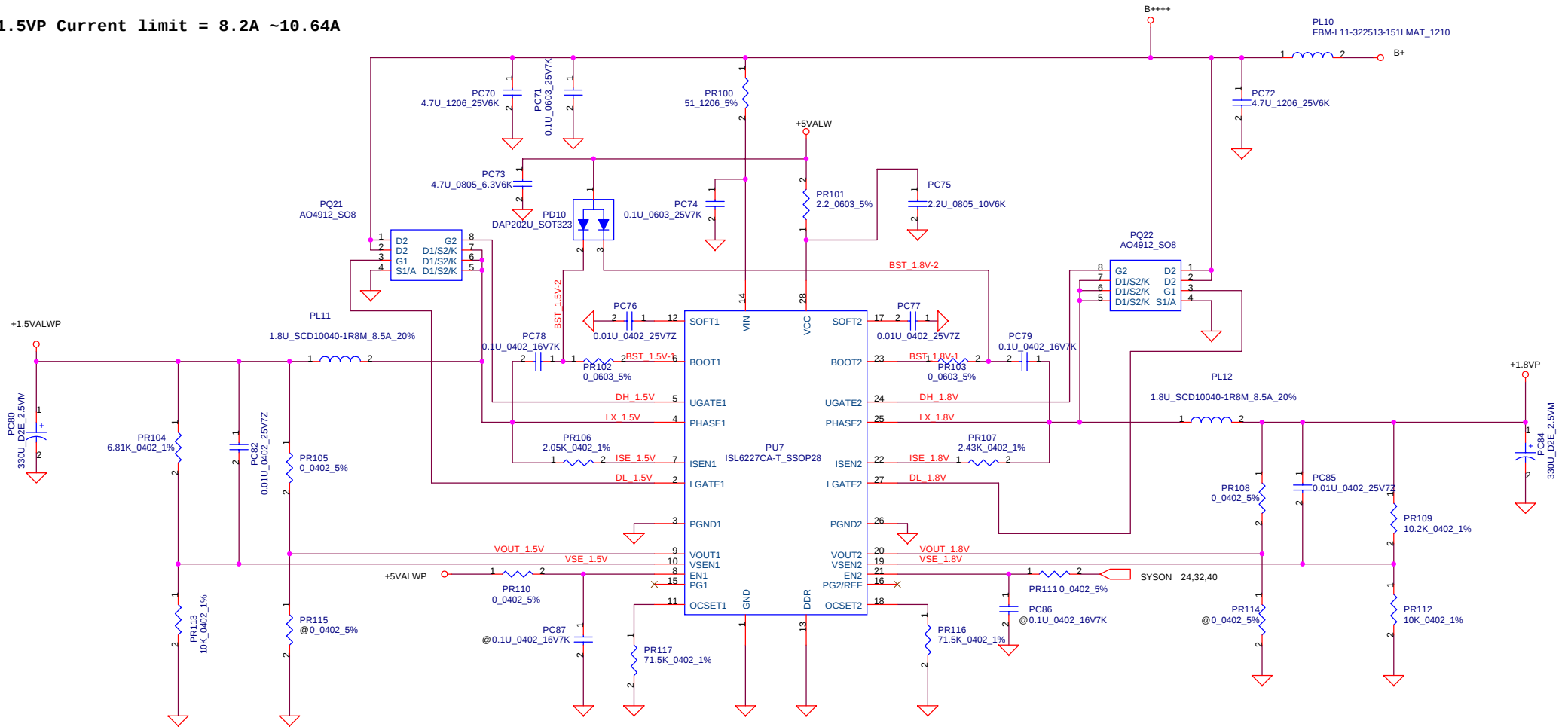


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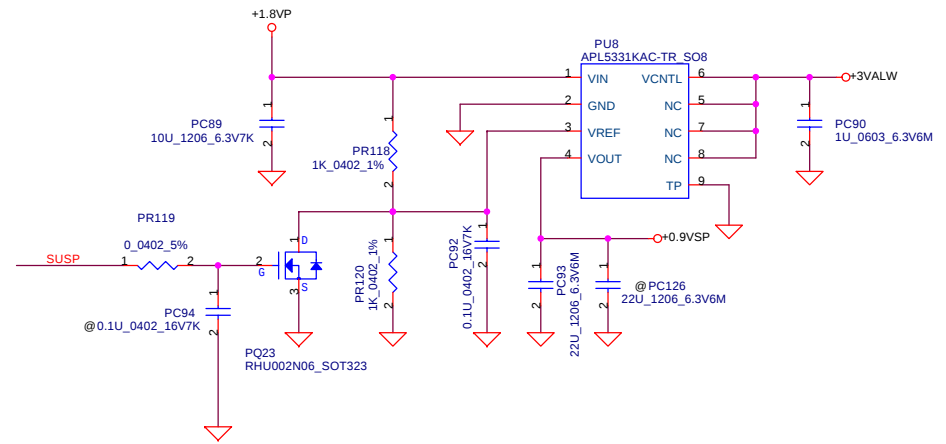
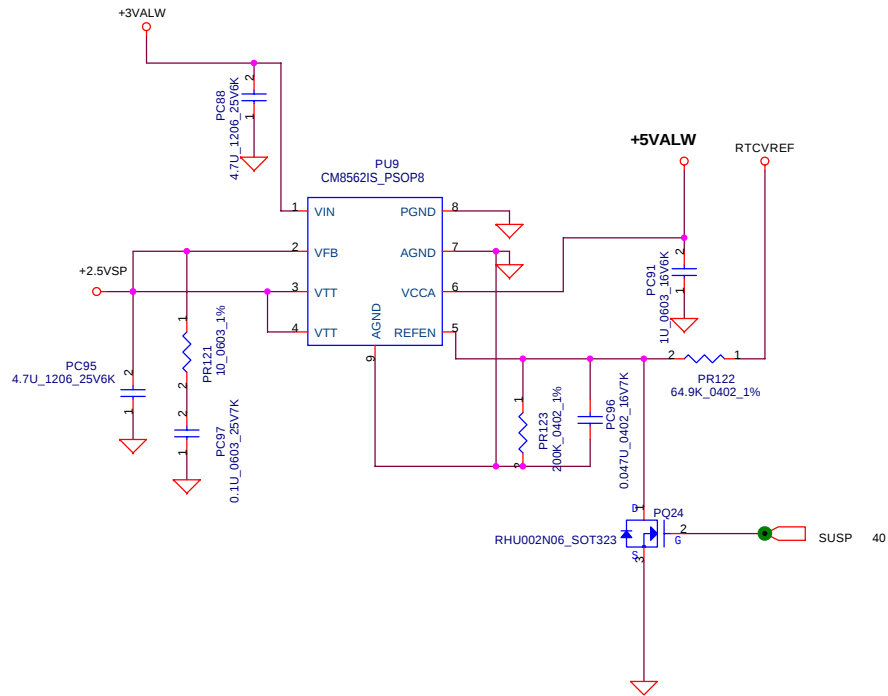


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+1.5VP Current limit = 8.2A ~10.64A



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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	B.Ver #	Phase
1	For HDQ70, change RTC change current.	Because the charge current needs to meet battery spec.	0.1	41	Change PR16 and PR17 from SD028300000 to SD028560000.	0.1	DVT
2	For HDQ70, change MAX1999 to MAX8734A	Because MAX1999 has triggered UVP when AC Adapter plug in or plug out.	0.1	42	Change PU3 from SA019990000(S IC MAX1999EEI QSOP28 PWM) to SA00000G100(MAX8734AEEI+ QSOP 28P)	0.1	DVT
3	For HDQ70, fix Vin detector accuracy.	For HDQ70, fix Vin detector accuracy.	0.1	43	Change PR65 from SD034150200(S RES 1/16W 15K 0402 1%) to SD034000000(S RES 1/16W 0 0402 1%).	0.1	DVT
4	For HDQ70, fix Vin detector accuracy.	For HDQ70, fix Vin detector accuracy.	0.1	43	Change PR68 from SD034100300(S RES 1/16W 100K 0402 1%) to SD000008A00(S RES 1/16W 118K 0402 0.1%).	0.1	DVT
5	For HDQ70, fix Vin detector accuracy.	For HDQ70, fix Vin detector accuracy.	0.1	43	Change PR73 from SD034100200(S RES 1/16W 10K 0402 1%) to SD0000008B00(S RES 1/16W 10K 0402 0.1%).	0.1	DVT
6	For HDQ70, fix the battery temp curve	Because we need to improve the curve of temp detector of battery more smoothly.	0.1	44	Change PR83 from SD034255200(S RES 1/16W 25.5K 0402 1%) to SD034649100(S RES 1/16W 6.49K 0402 1%).	0.1	DVT
7	For HDQ70, change 1.05VSP OCP point.	For HDQ70, change 1.05VSP OCP point.	0.1	45	Change PR93 from SD034412100(S RES 1/16W 4.12K 0402 1%) to SD034499100(S RES 1/16W 4.99K 0402 1%).	0.1	DVT
8	For HDQ70, fix the output voltage.	For HDQ70, fix the output voltage within spec.	0.1	45	Change PR96 from SD034715100(S RES 1/16W 7.15K 0402 1%) to SD034499100(S RES 1/16W 4.99K 0402 1%).	0.1	DVT
9	For HDQ70, fix the FB voltage.	For HDQ70, fix the FB voltage within spec.	0.1	45	Change PC68 from SE075682K00(S CER CAP 6800P 25V +-10% X7R 0402) to SE042333K00(S CER CAP .033U 25V K X7R 0603).	0.1	DVT
10	For HDQ70, add snuber on LX.	Add snuber on LX to improve high side noise.	0.1	45	Add PR170 SD011470BT9(S RES 1/10W 4.7 +-5% 1206).	0.1	DVT
11	For HDQ70, add snuber on LX.	Add snuber on LX to improve high side noise.	0.1	45	Add PC130 SE024681J00(S CER CAP 680P 50V J NPO 0603).	0.1	DVT
12	For HDQ70, 1.5VALWP ripple voltage is too large.	Because we need to improve the ripple of 1.5VALWP.	0.1	46	Change PC80 from SGA20151330 to SGASGA19331D00.	0.1	DVT
13	For HDQ70, 1.8VP ripple voltage is too large.	Because we need to improve the ripple of 1.8VP.	0.1	46	Change PC84 from SGA20151330 to SGASGA19331D00.	0.1	DVT
14	For HDQ70, change 1.8VP OCP point.	For HDQ70, change 1.8VP OCP point.	0.1	46	Change PR107 from SD034174100(S RES 1/16W 1.74K 0402 1%) to SD034243100(S RES 1/16W 2.43K 0402 1%)	0.1	DVT
15	For HDQ70, change 1.8VP OCP point.	For HDQ70, change 1.8VP OCP point.	0.1	46	Change PR116 from SD034806200(S RES 1/16W 80.6K 0402 1%) to SD034715200(S RES 1/16W 71.5K 0402 1%).	0.1	DVT
16	For HDQ70, fix the 2.5VSP's power sequence.	Because we need to fix the power sequence of 2.5VSP.	0.1	47	Change PC96 from SE075222K00(S CER CAP 2200P 25V +-10% X7R 0402) to SE076473K00(S CER CAP 0.047U 16V K X7R 0402).	0.1	DVT

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Item	Reason for change	PG #	Modify List	Date	
1	AC_IN Signal	P.32	Remove R189, D11		DVT(Rev01)
2	LAN LED on 8110SBL	P.26	Unpop R449 on both 8100CL and 8110SBL		DVT(Rev01)
3	Modify +1.8VS and +1.5VS power sequence	P.40	Change R531,R551 value from 100K to 180K		DVT(Rev01)
4	5 Way BTN problem	P.33,34	Add 5WAY_BTN signal and R184		DVT(Rev01)
5	Remove New Card circuit	P.24	Remove New Card Circiut		DVT(Rev01)
6	New Card Clock Request	P.13	Connect PCIE_CLKREQ1# to Clock Gen pin.32		DVT(Rev01)
7	Change IEEE1394 Connector	P.25	Change IEEE1394 Connector Type		DVT(Rev01)
8	Codec VREF capacitor	P.36	Change C497 value from 0.1uf to 10uf		DVT(Rev01)
9	+SD_VCC and +XD_VCC Power Switch	P.23	Add R572, R573 for SD, XD Power Switch		DVT(Rev01)
10	Un-used Codec Clock	P.13	unpoped R89		DVT(Rev01)
11	Un-used ODD Connector	P.21	Remove the JP47 and C362,C366,C675,C678,C681		DVT(Rev01)
12	Add 10uF capacitor on GMCH	P.9	Add C703 on +3VS_DAC		DVT(Rev01)
13	Changed for Speaker and Subwoofer	P.37,38	Change Main Amplifier Gain form 10dB to 8dB, and Modify Woofer BPF value		DVT(Rev01)
14	Change CRT and TV-out Pi Filter Value	P.14	Change CRT and TV-out Pi Filter Value to Following Chipset Recommand		DVT(Rev01)
15	Change DVI SMBUS Pull-up Value	P.16	Change R346,R348 from 30K to 6.8K		DVT(Rev01)