

Dunlin LA-2601 Schematics Document

Intel Dothan / Alviso GM(PM) / DDR-2 / ICH6-M

(NV43/44M)

2005 / 03 / 14

Rev:1.0

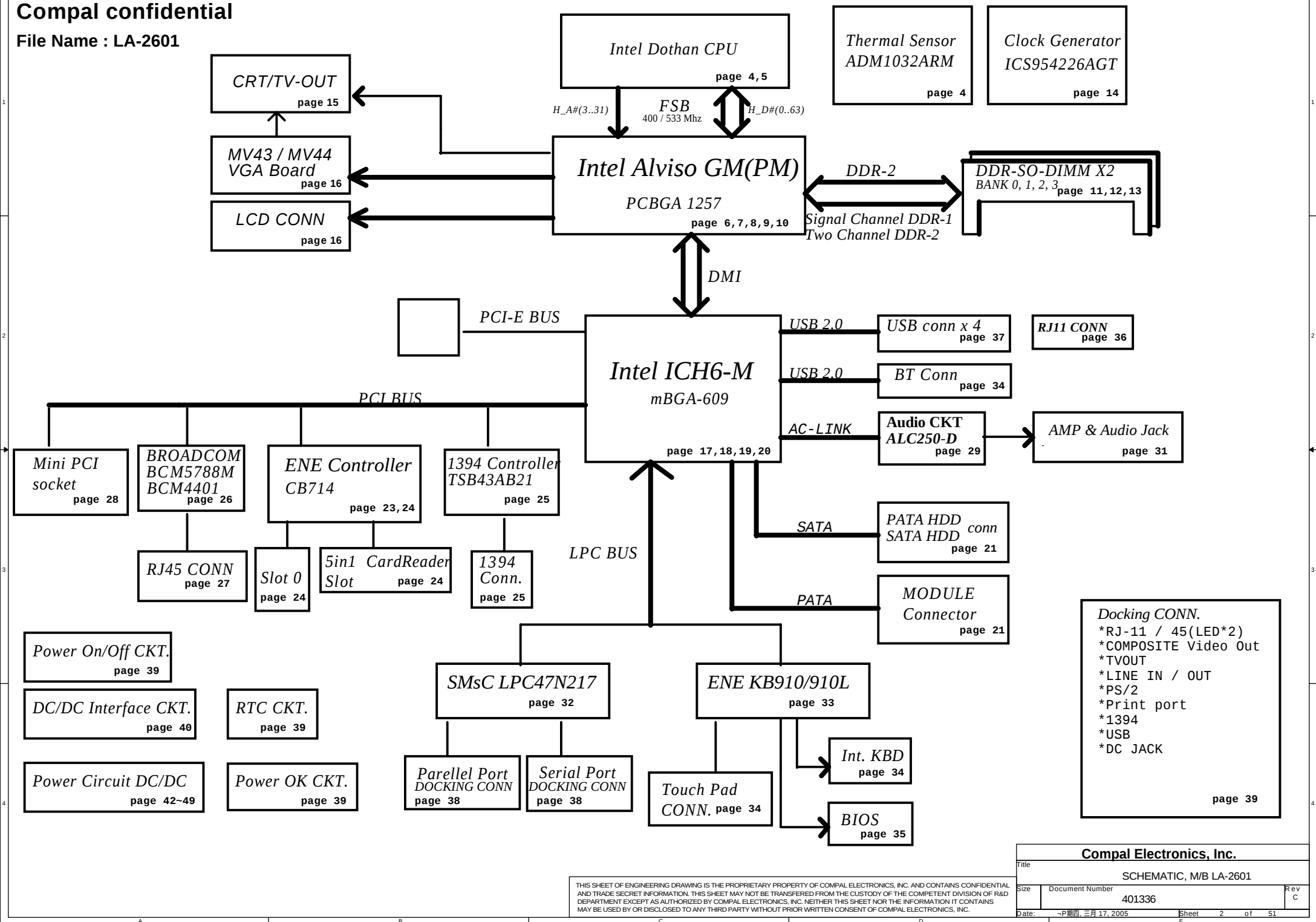
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File Name : LA-2601



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+DDRVTT	1.25V switched power rail for DDR terminator	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+DDRVCC	2.5V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5VMOD	5V switched power rail for Module Bay	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
SD	AD20	2	PIRQA/PIRQB
Mini-PCI	AD18	1	PIRQG/PIRQH
LAN	AD17	3	PIRQF

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b	2'nd Battery	1001 011X b
(24C04)	1011 000Xb		

ICH6M SM Bus address

Device	Address
Clock Generator (ICS 952623)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

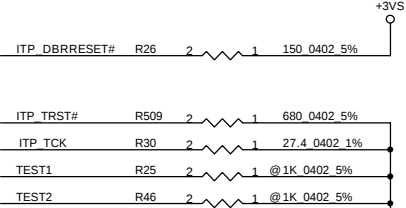
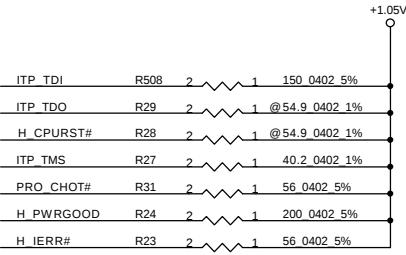
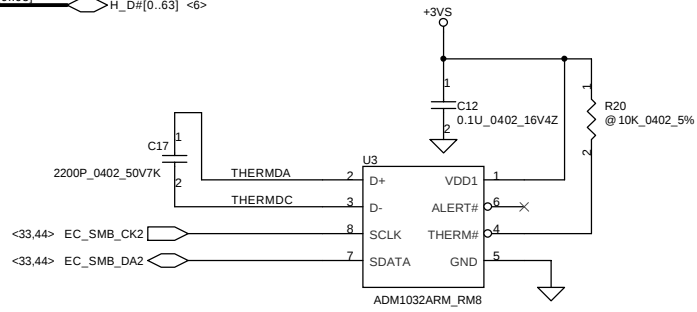
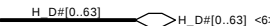
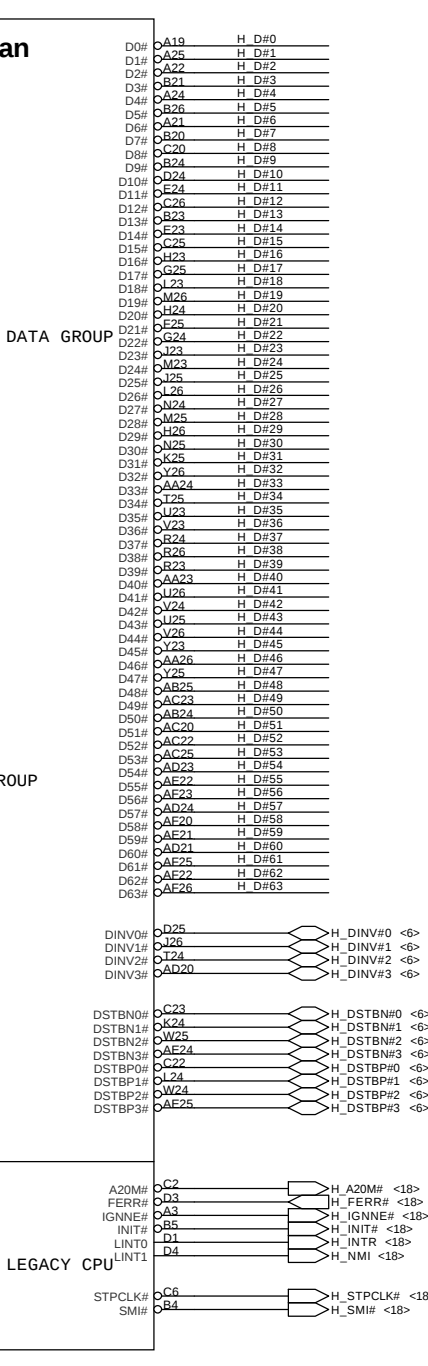
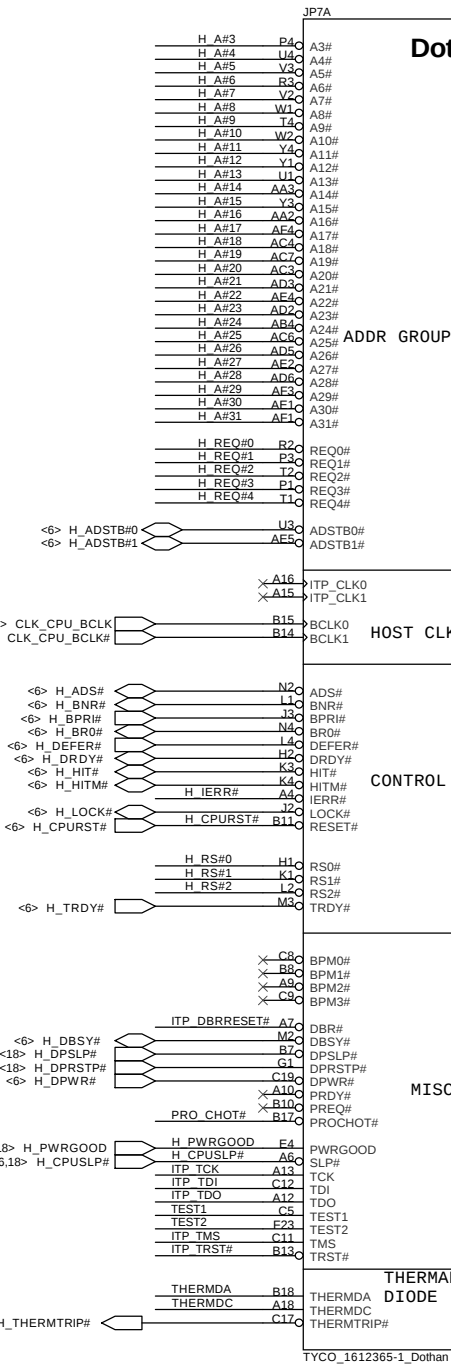
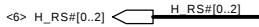
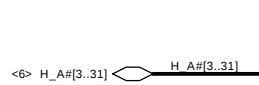
Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

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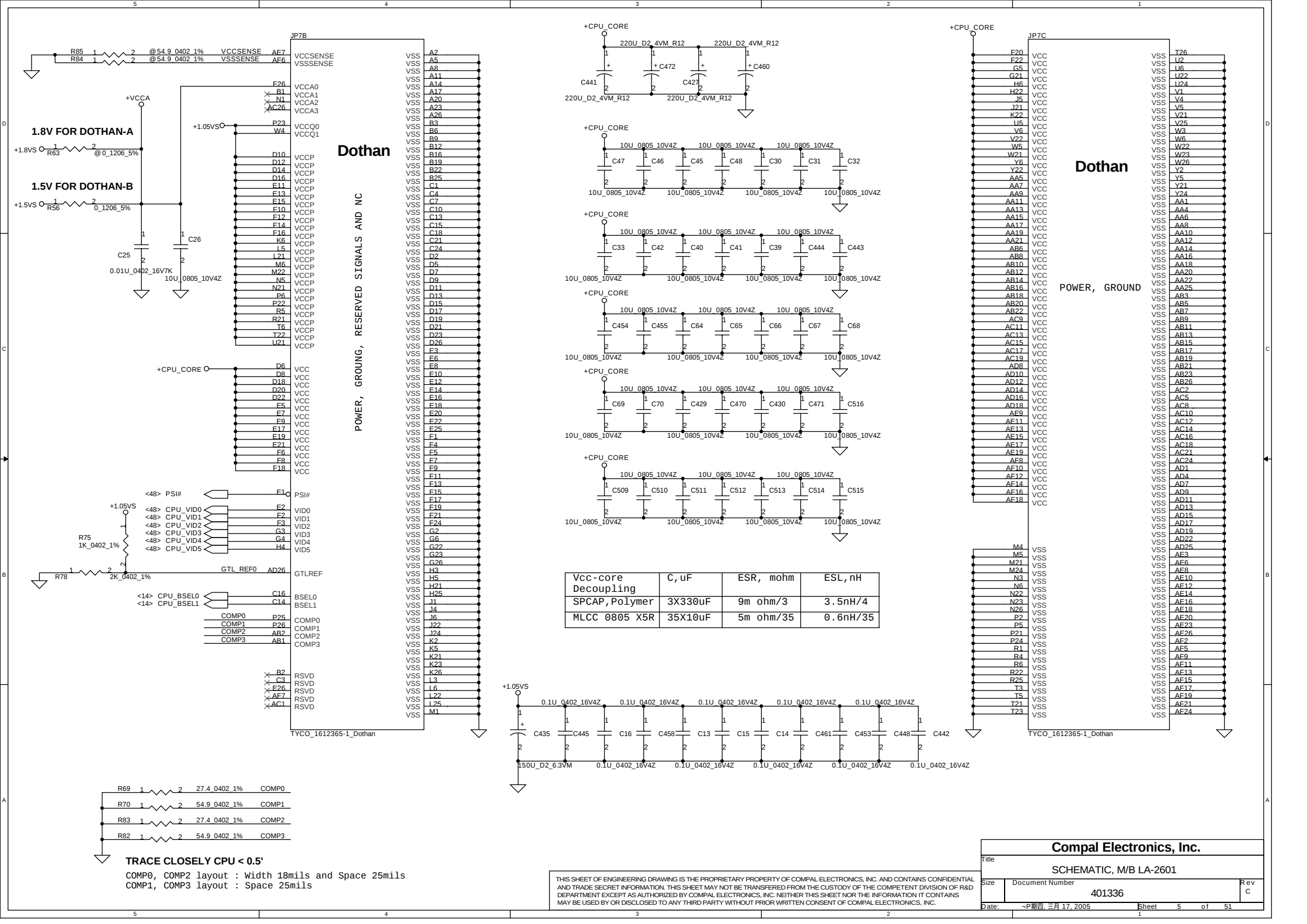
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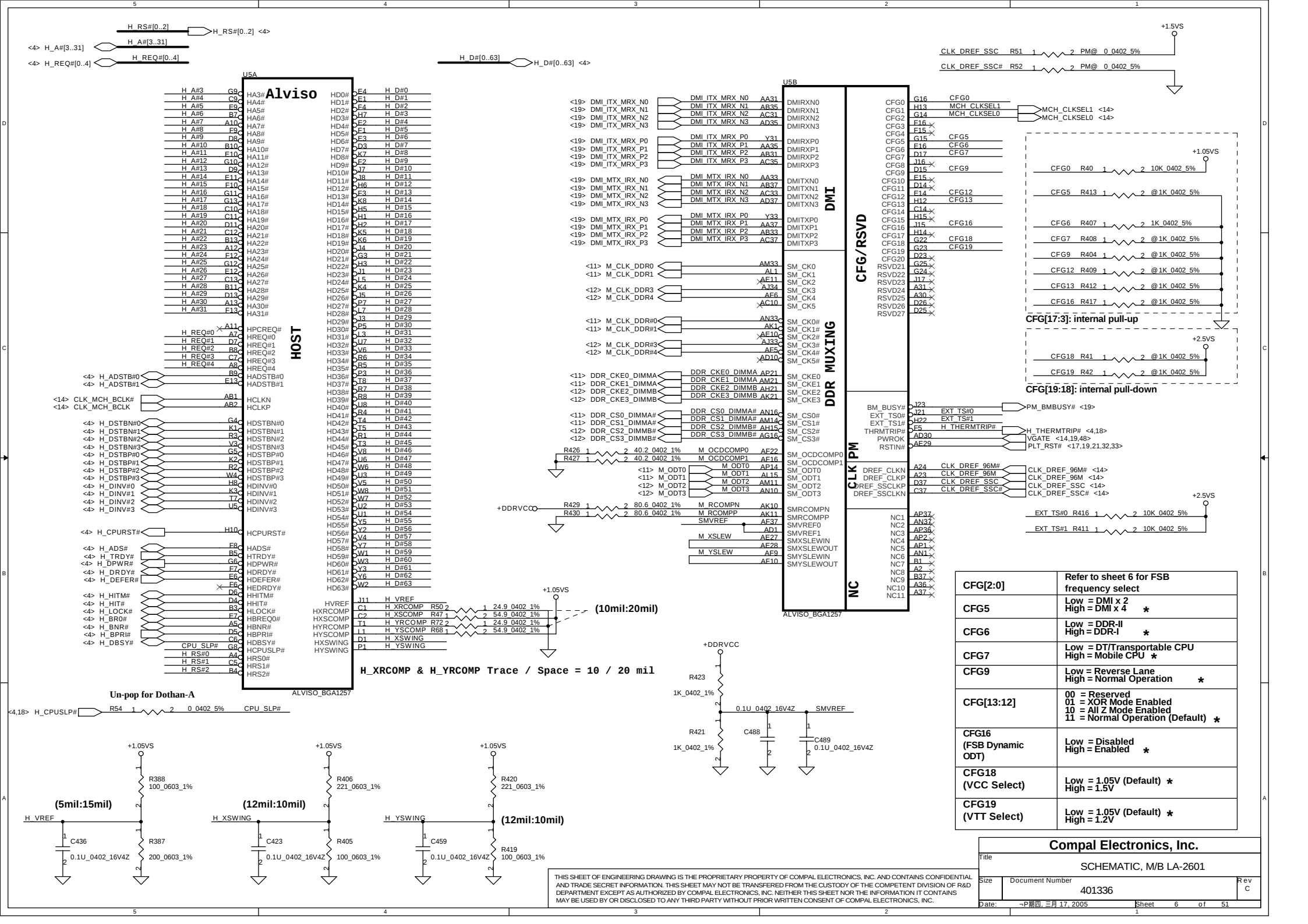


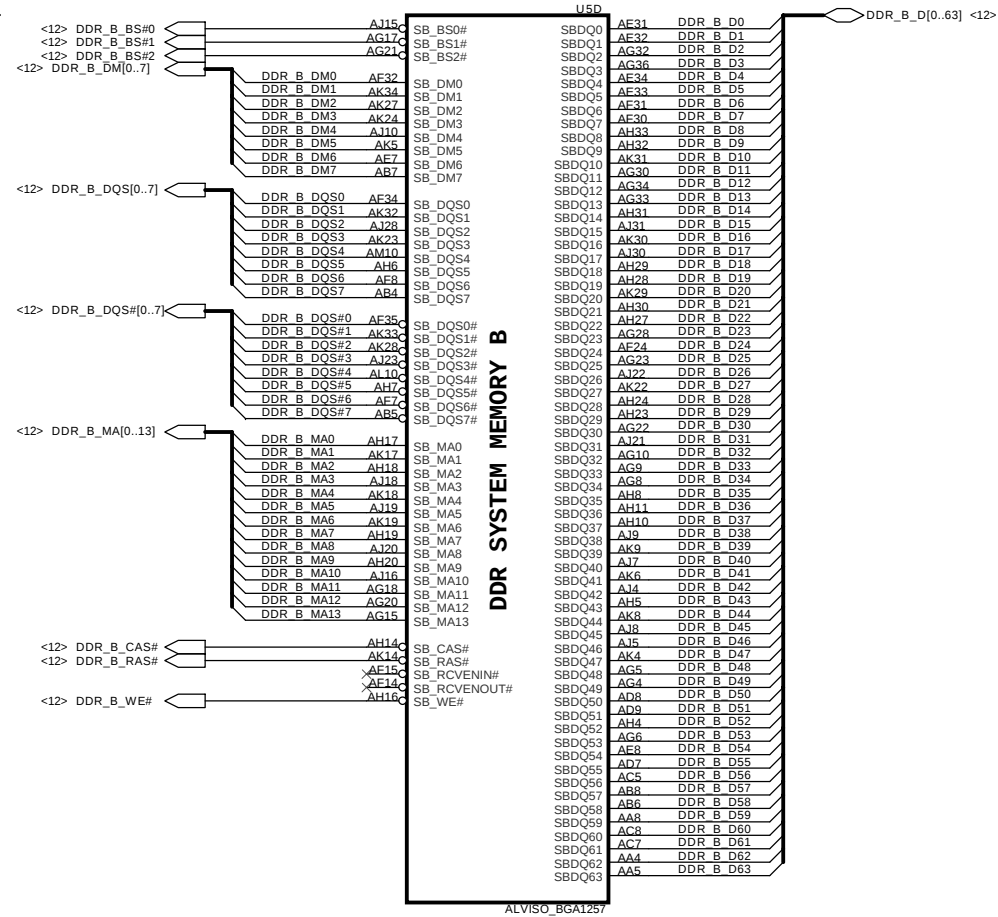
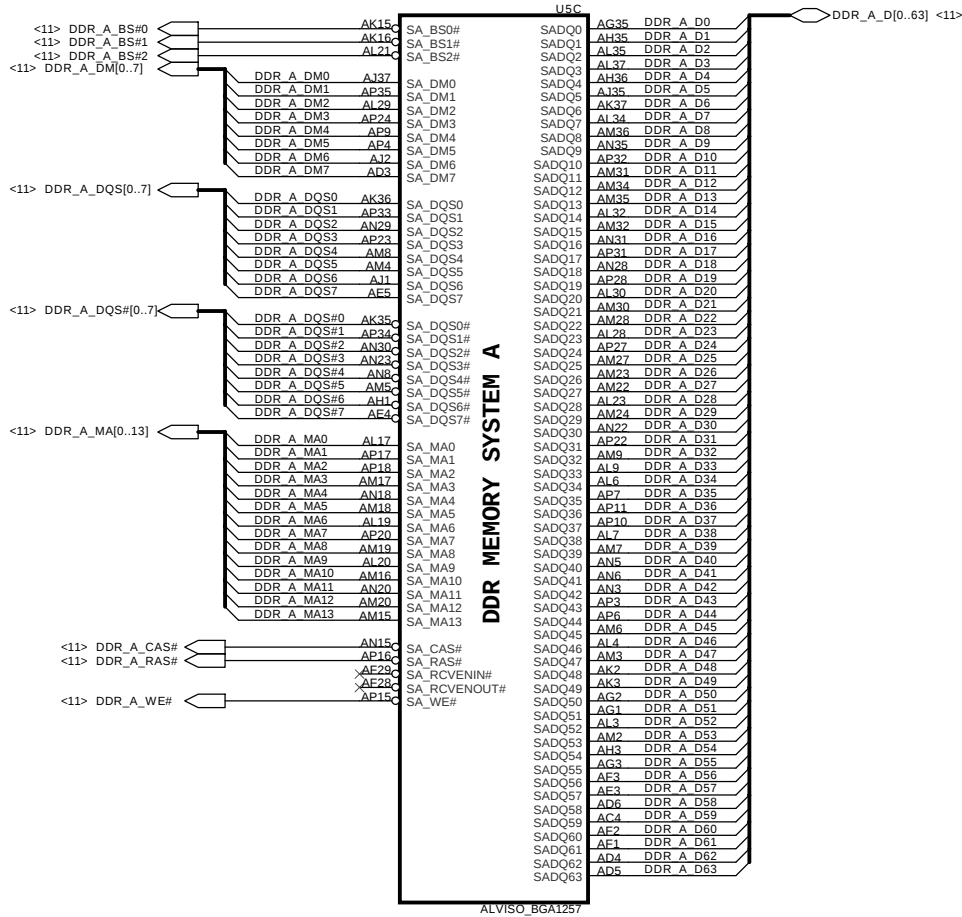
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THERMDA & THERMDC Trace / Space = 10 / 10 mil

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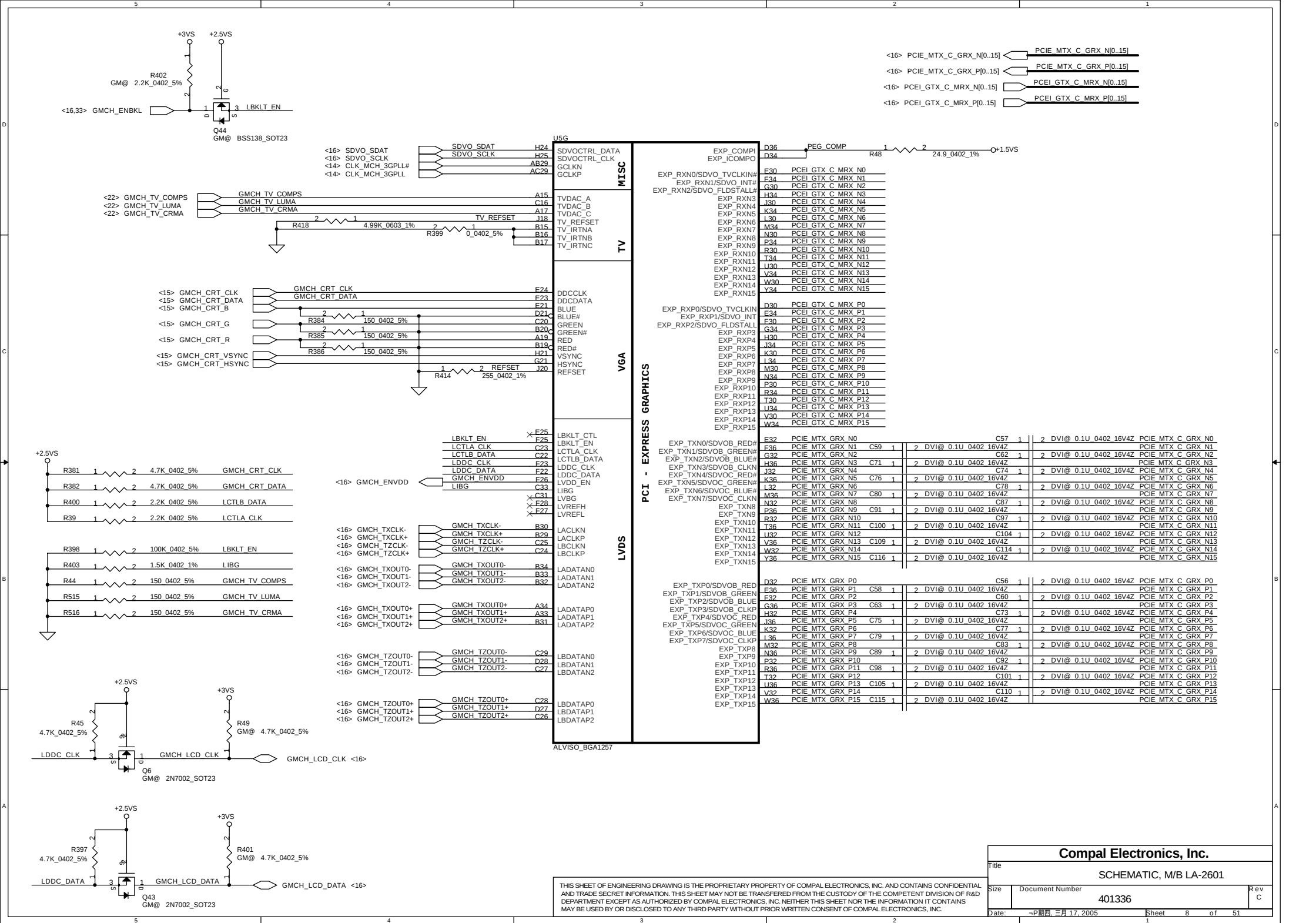


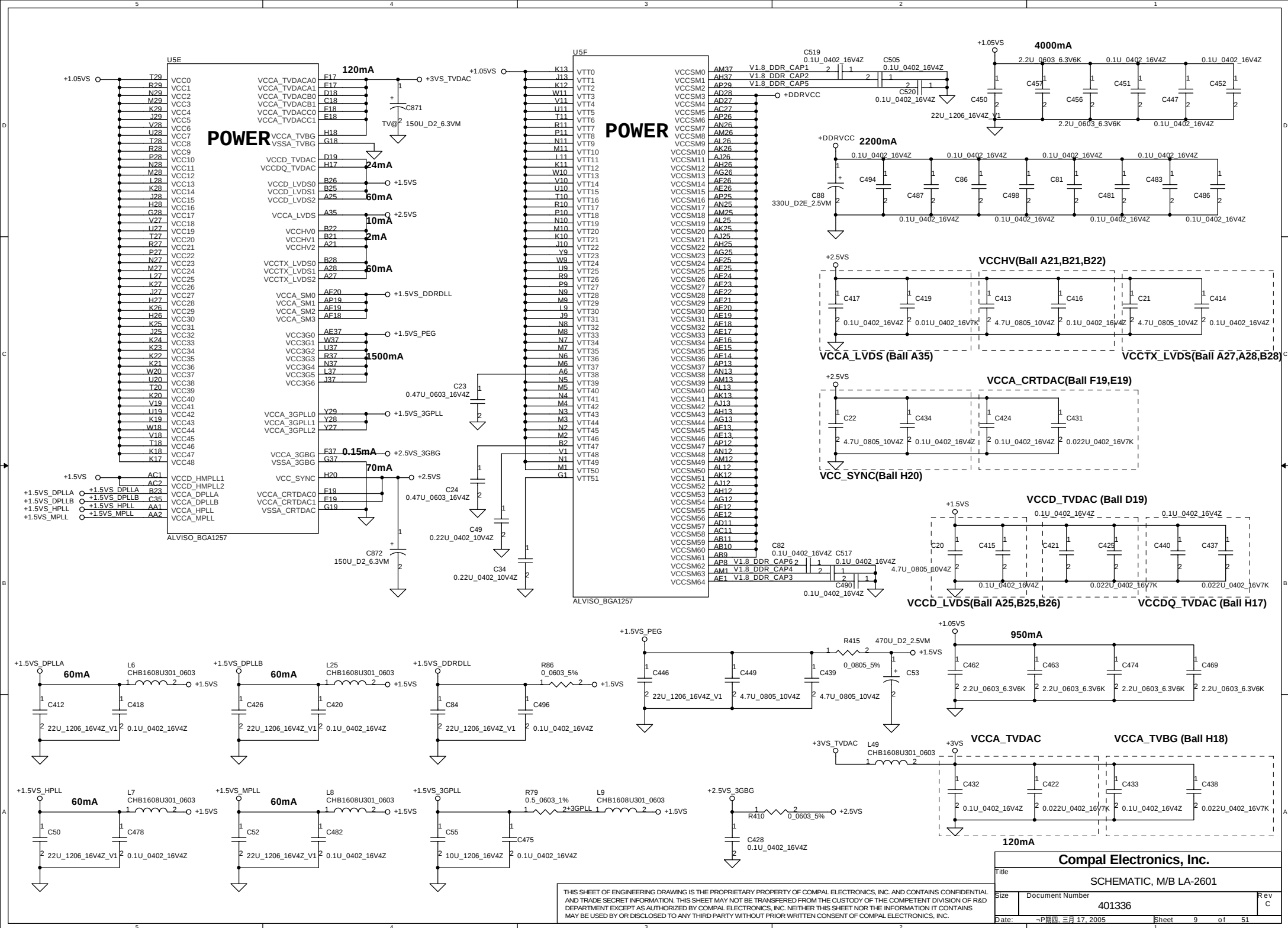


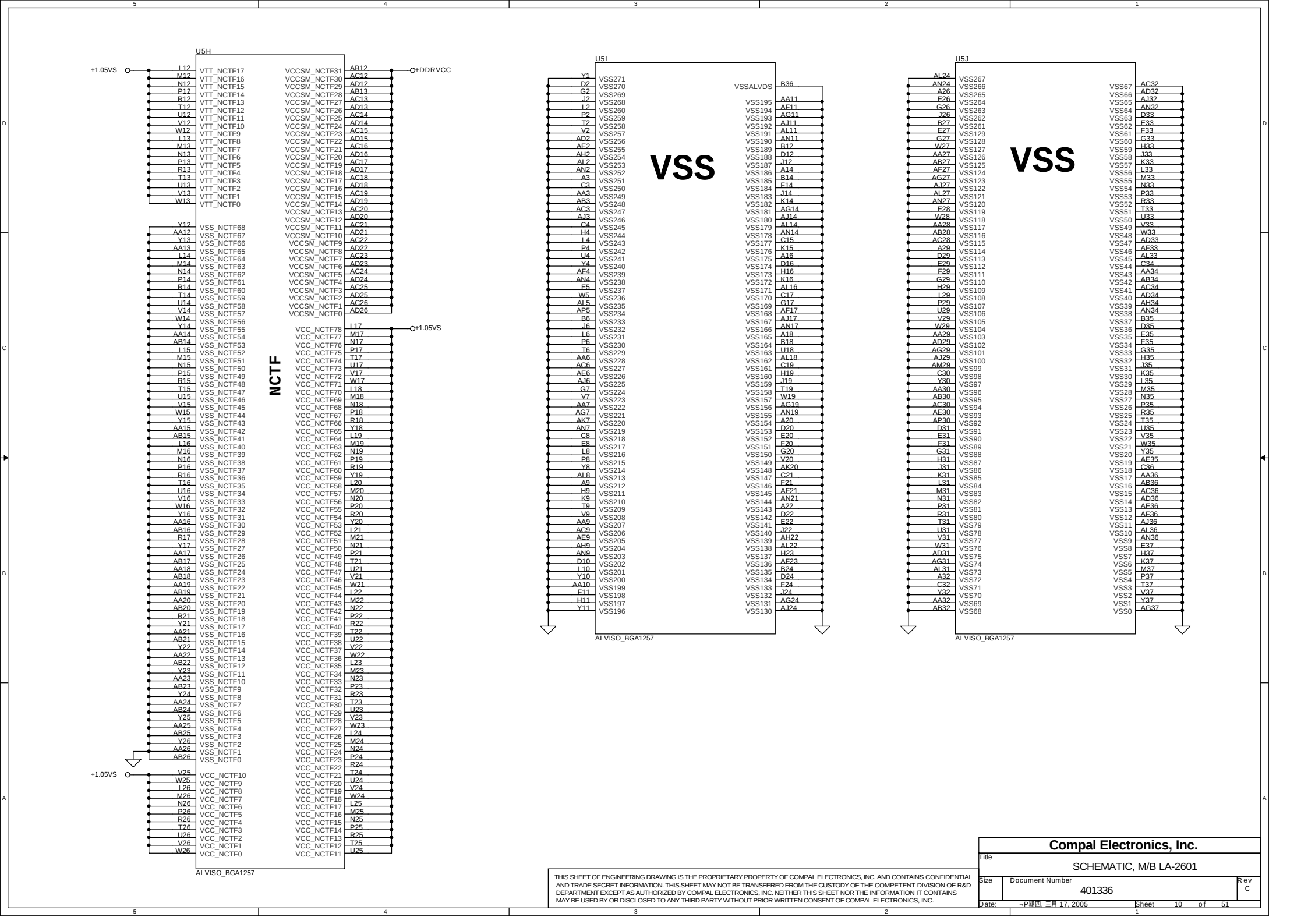


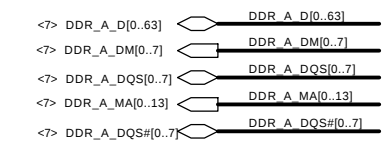
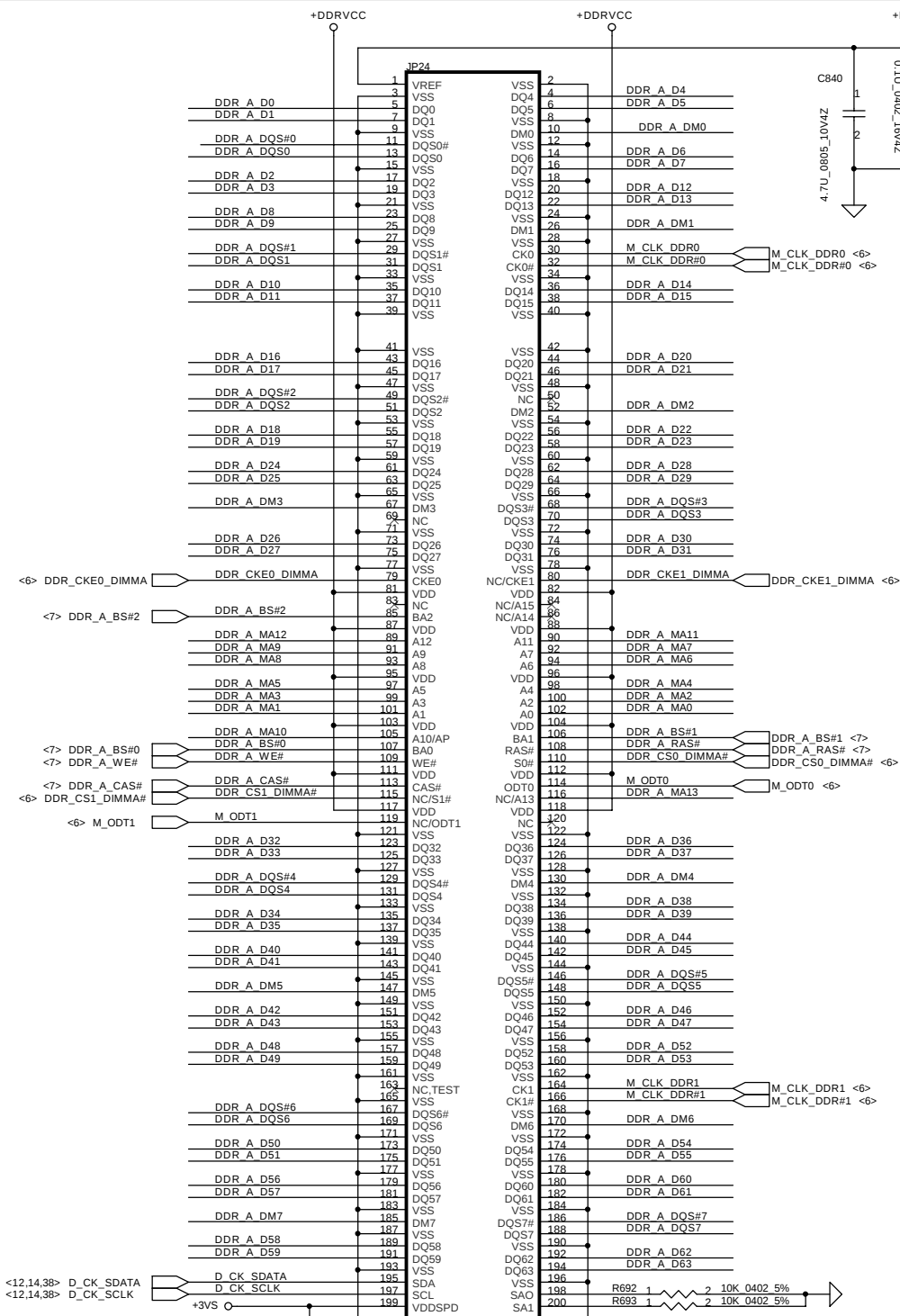
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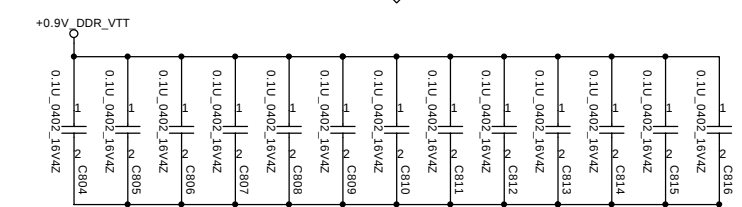
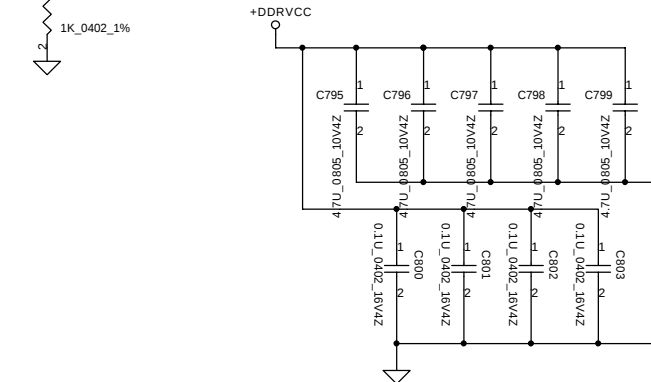




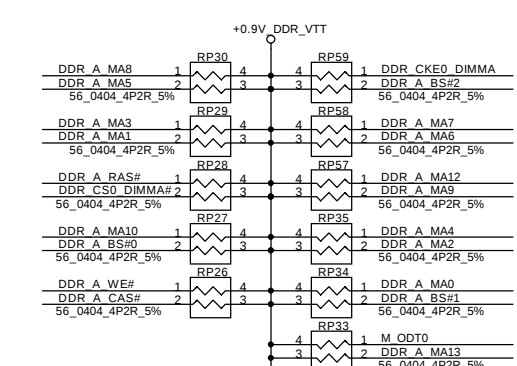




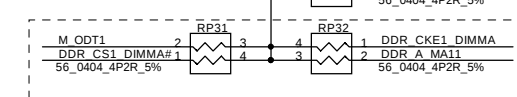
Layout Note:
Place near DIMM



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT



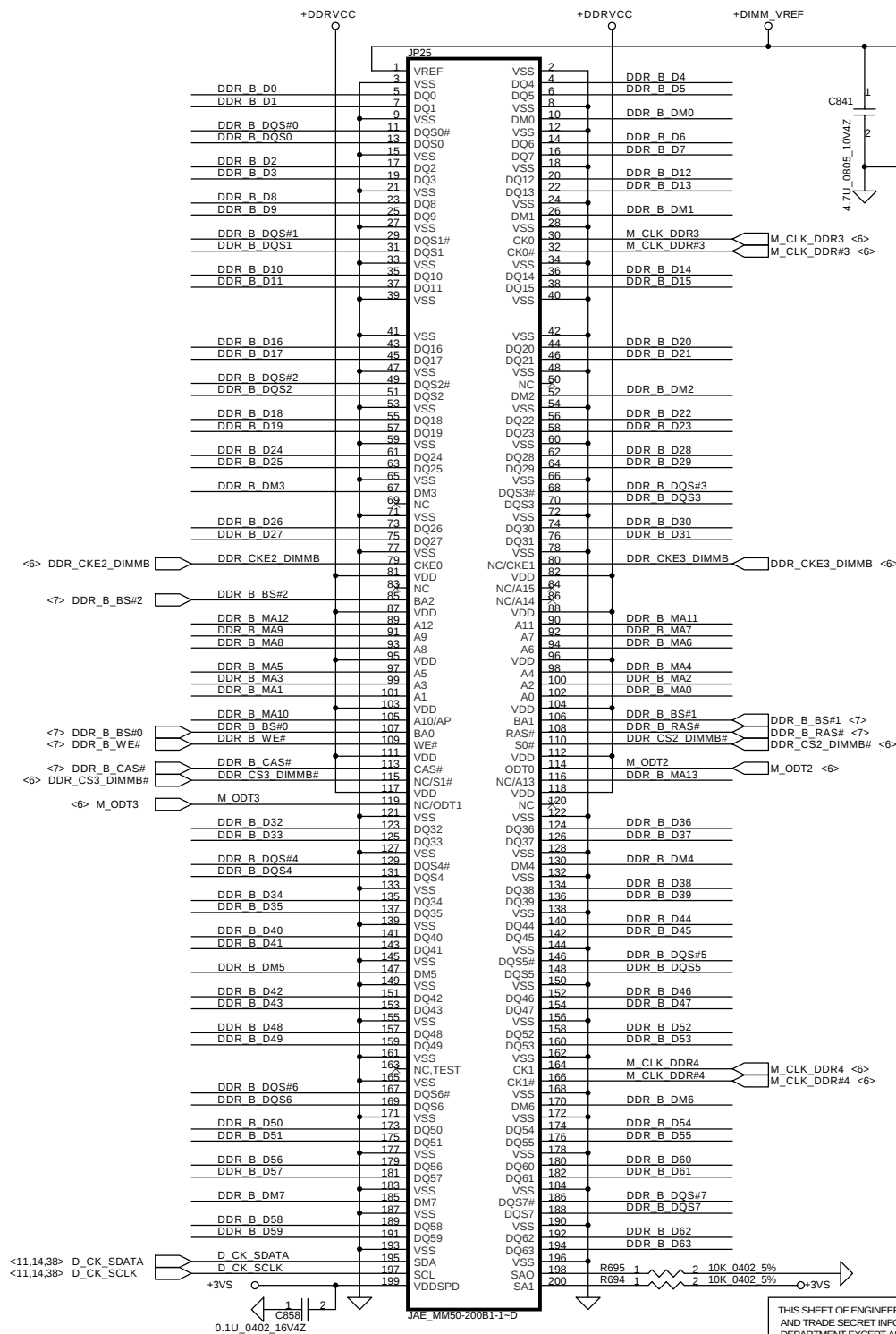
Layout Note:
Place these resistor
closely DIMM0, all
trace length<750 mil



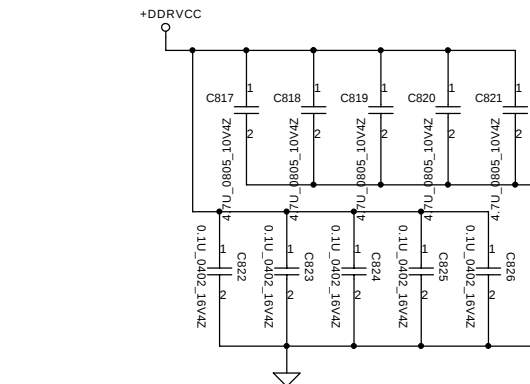
Layout Note:
Place these resistor
closely DIMM0, all
trace length
Max=1.3"

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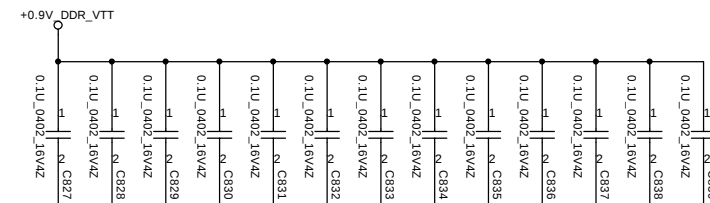
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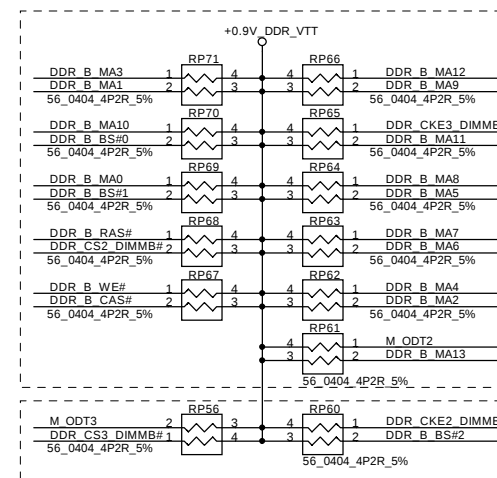
<7> DDR_B_D[0..63]
 <7> DDR_B_DM[0..7]
 <7> DDR_B_DQS[0..7]
 <7> DDR_B_MA[0..13]
 <7> DDR_B_DQS#[0..7]



Layout Note:
Place near DIMM



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



Layout Note:
Place these resistor closely DIMM0, all trace length < 750 mil

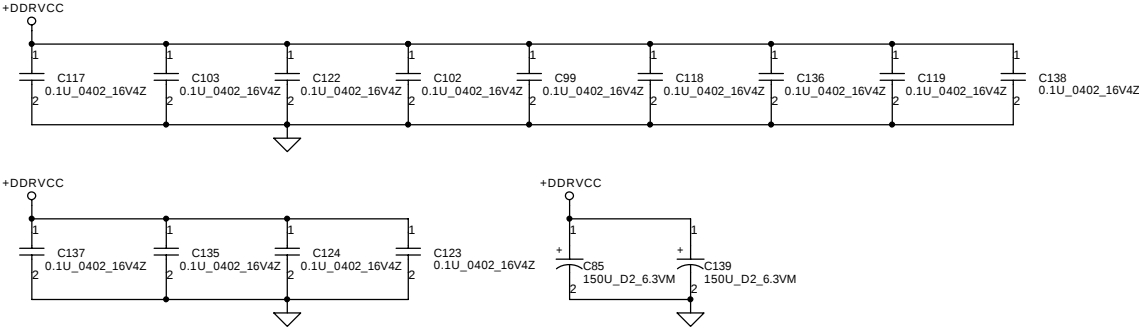
Layout Note:
Place these resistor closely DIMM0, all trace length Max=1.3"

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Layout note :
Distribute as close as possible
to DDR-SODIMM.



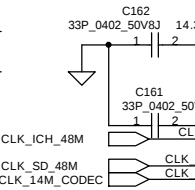
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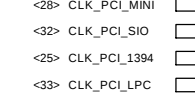
FSC	FSB	FSA	CPU	SRC	PCI
CLKSEL0	CLKSEL1	CLKSEL2	MHz	MHz	MHz
1	0	1	100	100	33.3
0	0	1	133	100	33.3
0	1	1	166	100	33.3
0	1	0	200	100	33.3

Table : ICS 954206B

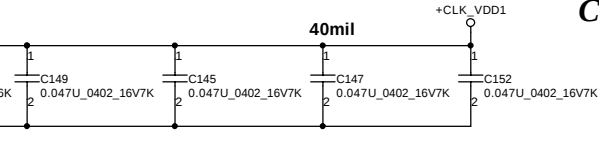
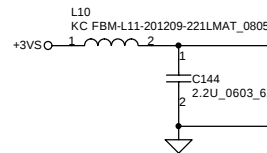
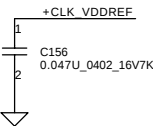
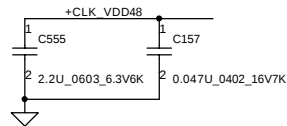
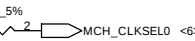
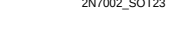
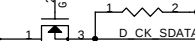
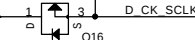
CLK_PC12 = 1, Pin 32,33
are PEREQ# pin



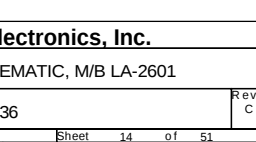
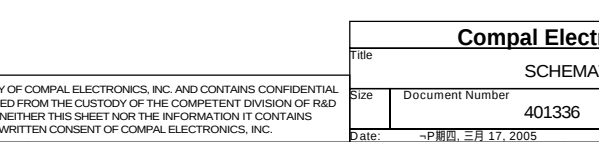
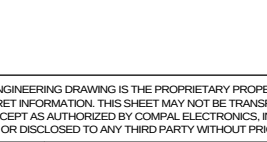
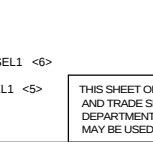
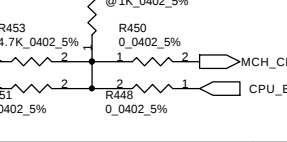
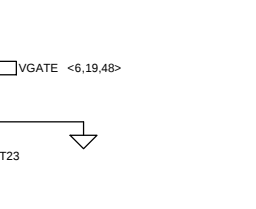
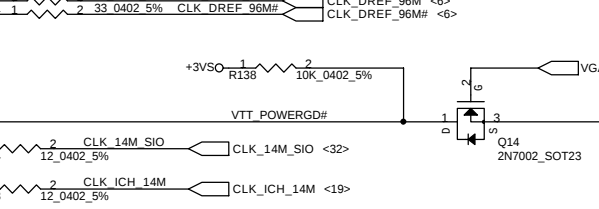
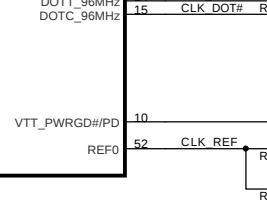
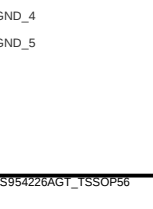
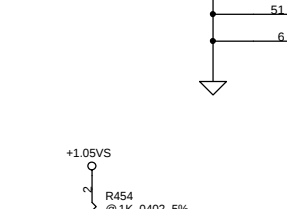
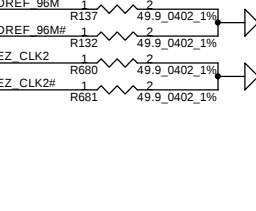
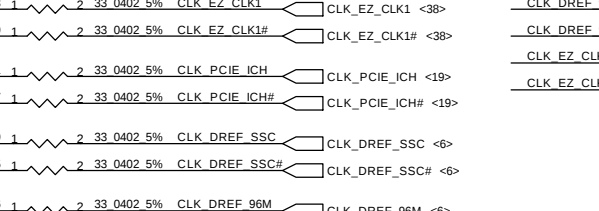
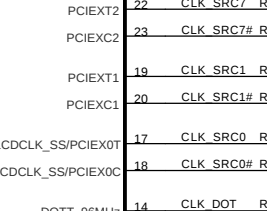
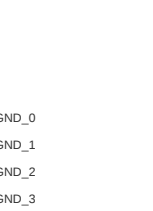
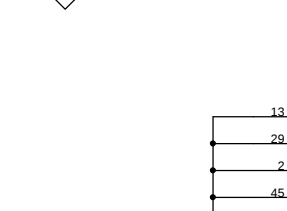
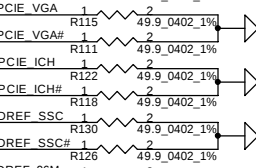
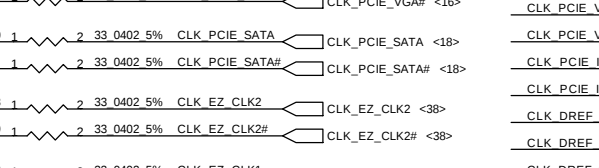
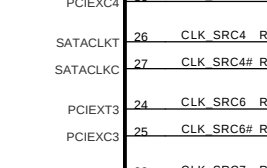
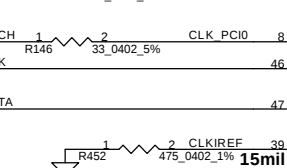
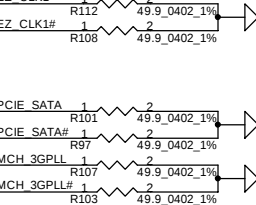
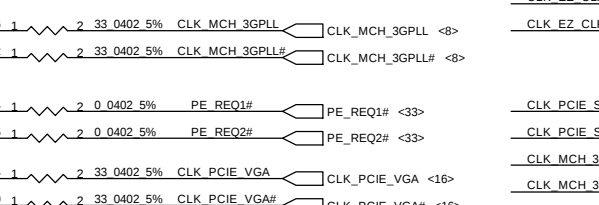
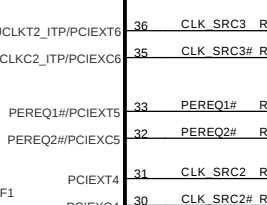
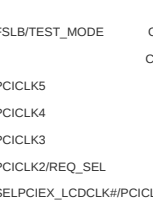
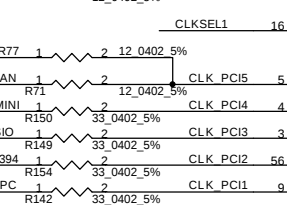
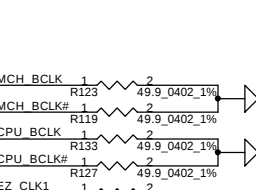
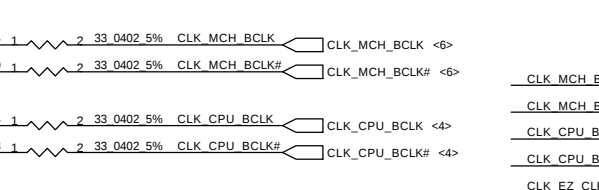
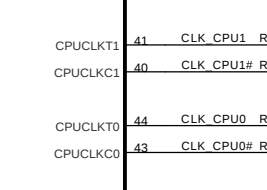
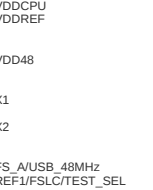
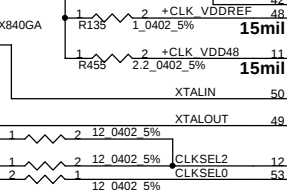
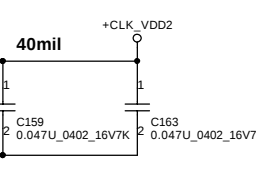
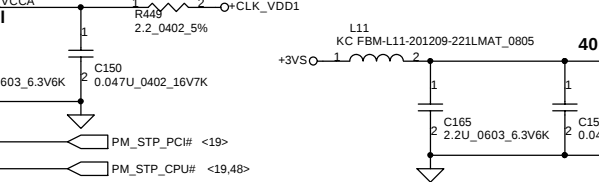
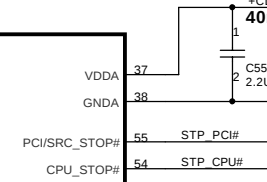
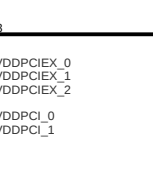
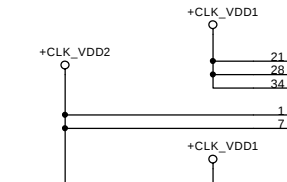
CLK_PC10 = 0, Pin 35,36
are PCIe CLK pair



CLK_PC11 = 0, Pin 17,18
are 96Mhz



Clock Generator

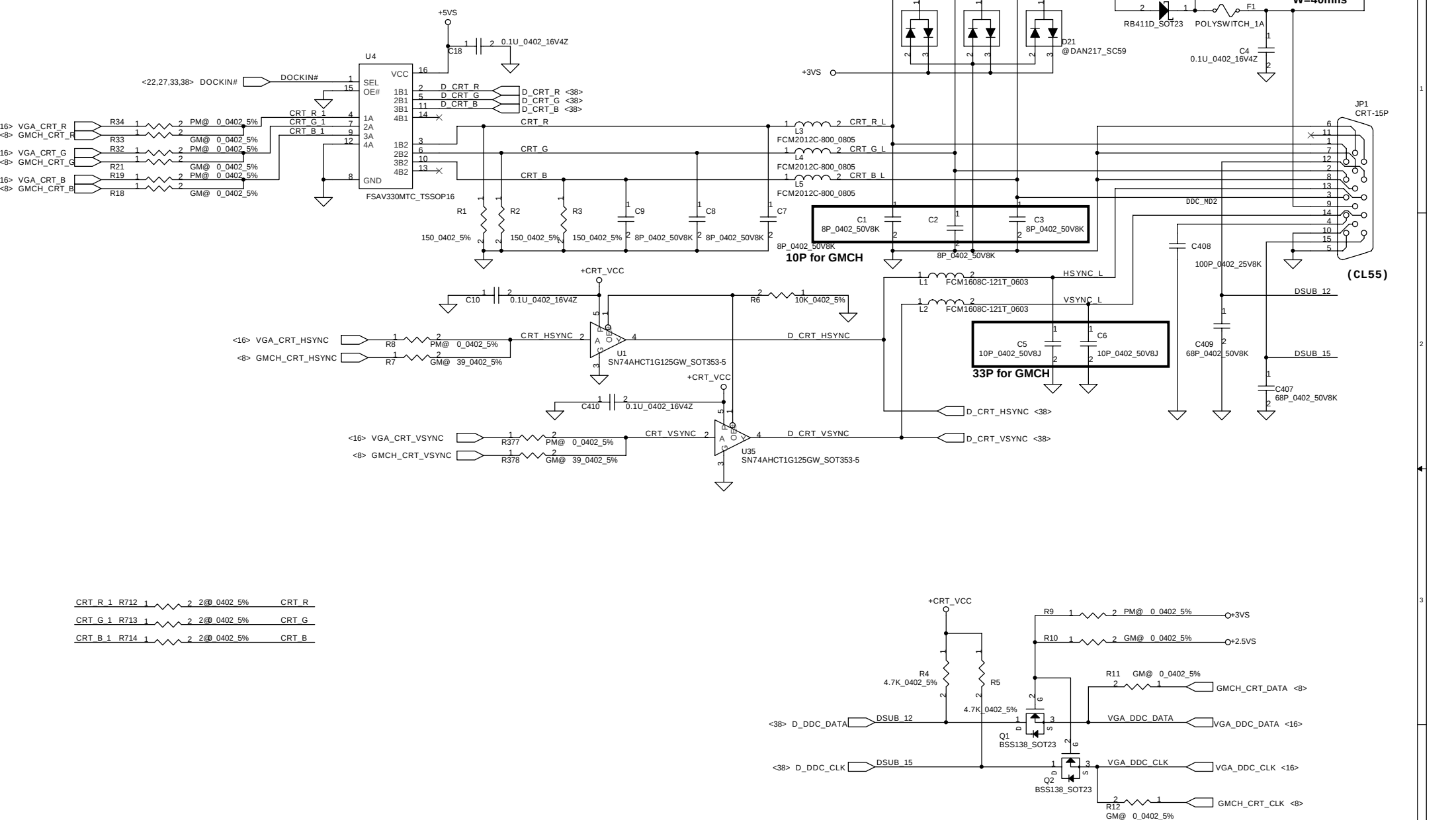


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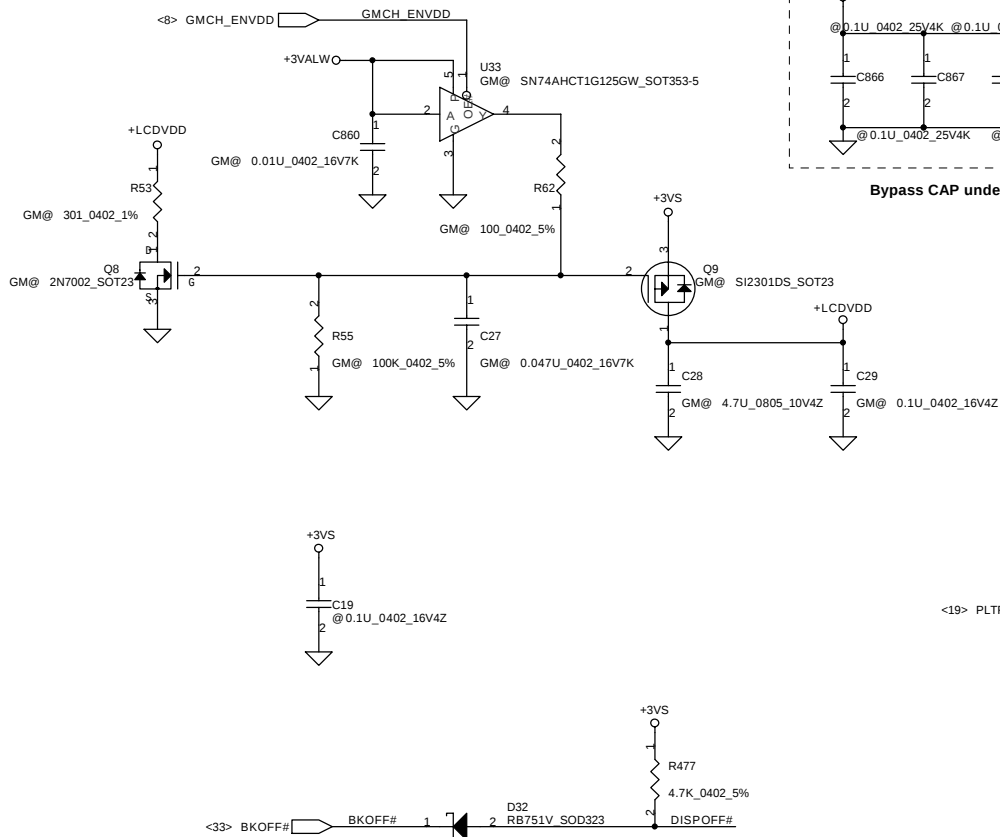
CRT Connector



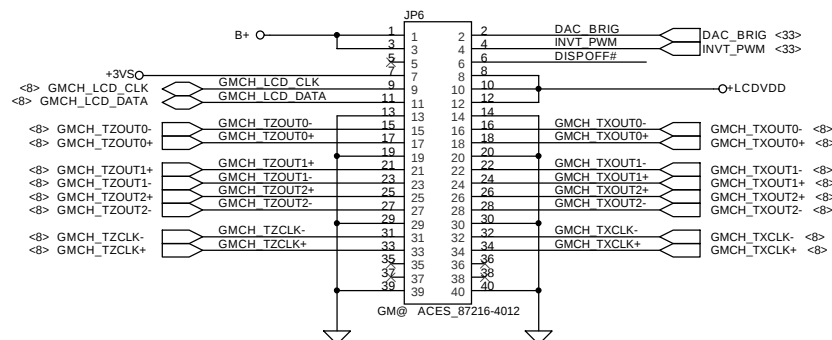
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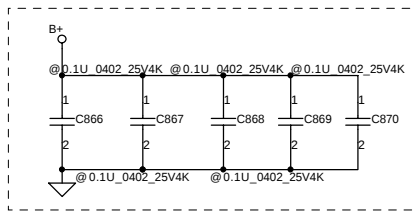
LCD POWER CIRCUIT



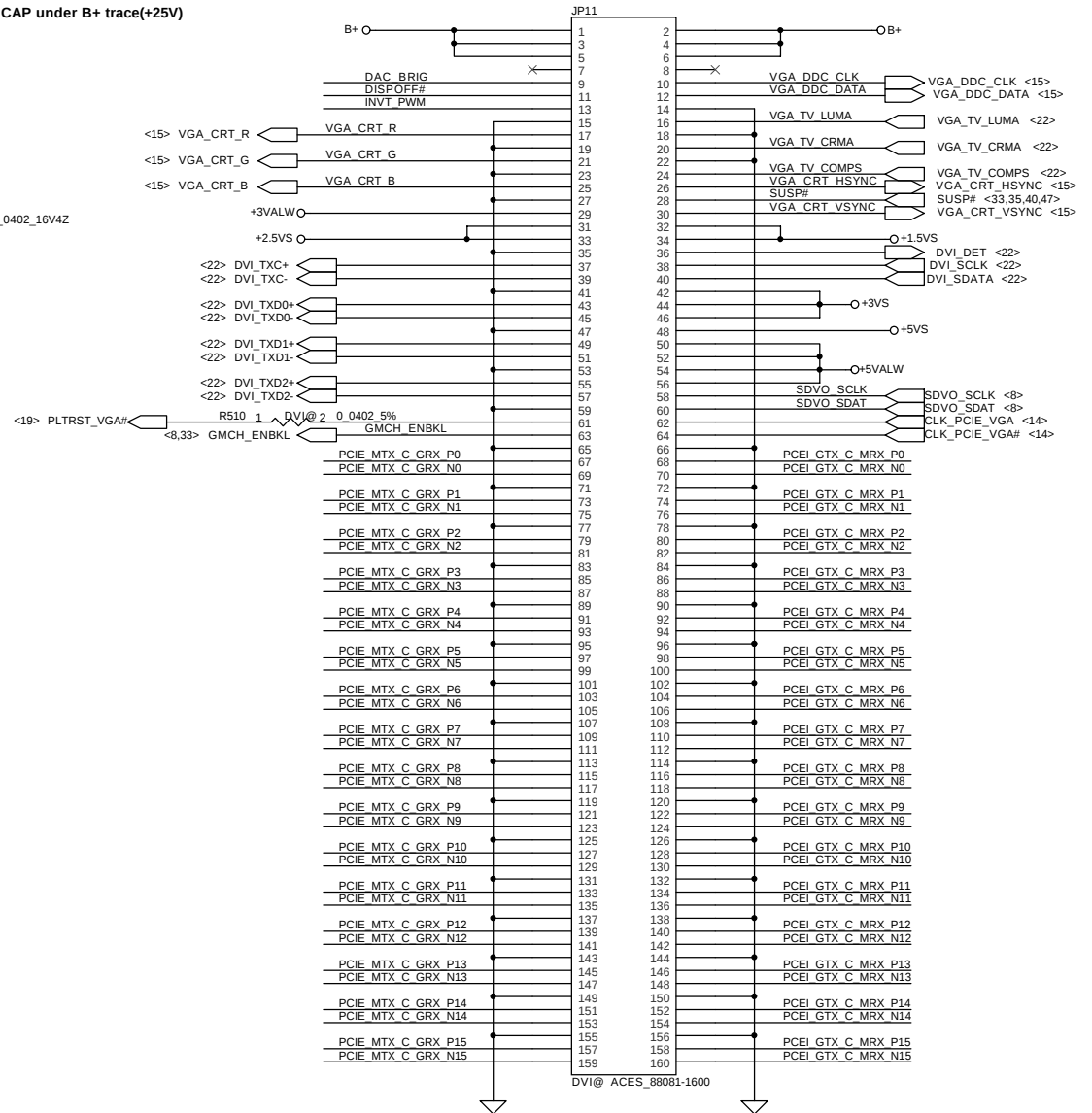
LCD/PANEL BD. Conn.



Bypass CAP under B+ trace(+25V)



VGA BOARD Conn.



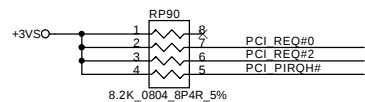
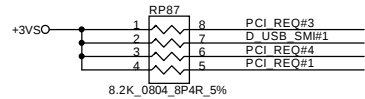
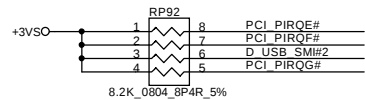
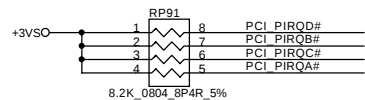
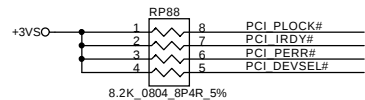
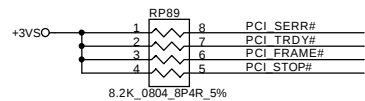
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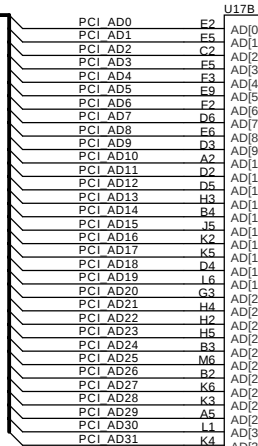


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<23,25,26,28> PCI_FRAME#

<23> PCI_PIRQA#

<23> PCI_PIRQB#



PCI_FRAME# J3

PCI_PIRQA# N2

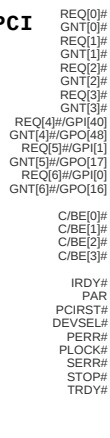
PCI_PIRQB# I2

PCI_PIRQC# M1

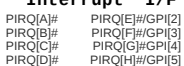
PCI_PIRQD# I3

U17B

PCI



Interrupt I/F

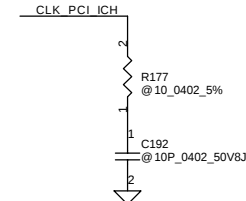
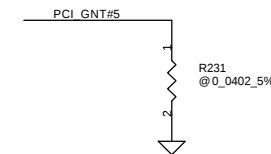


RESERVED



ICH6_BGA609

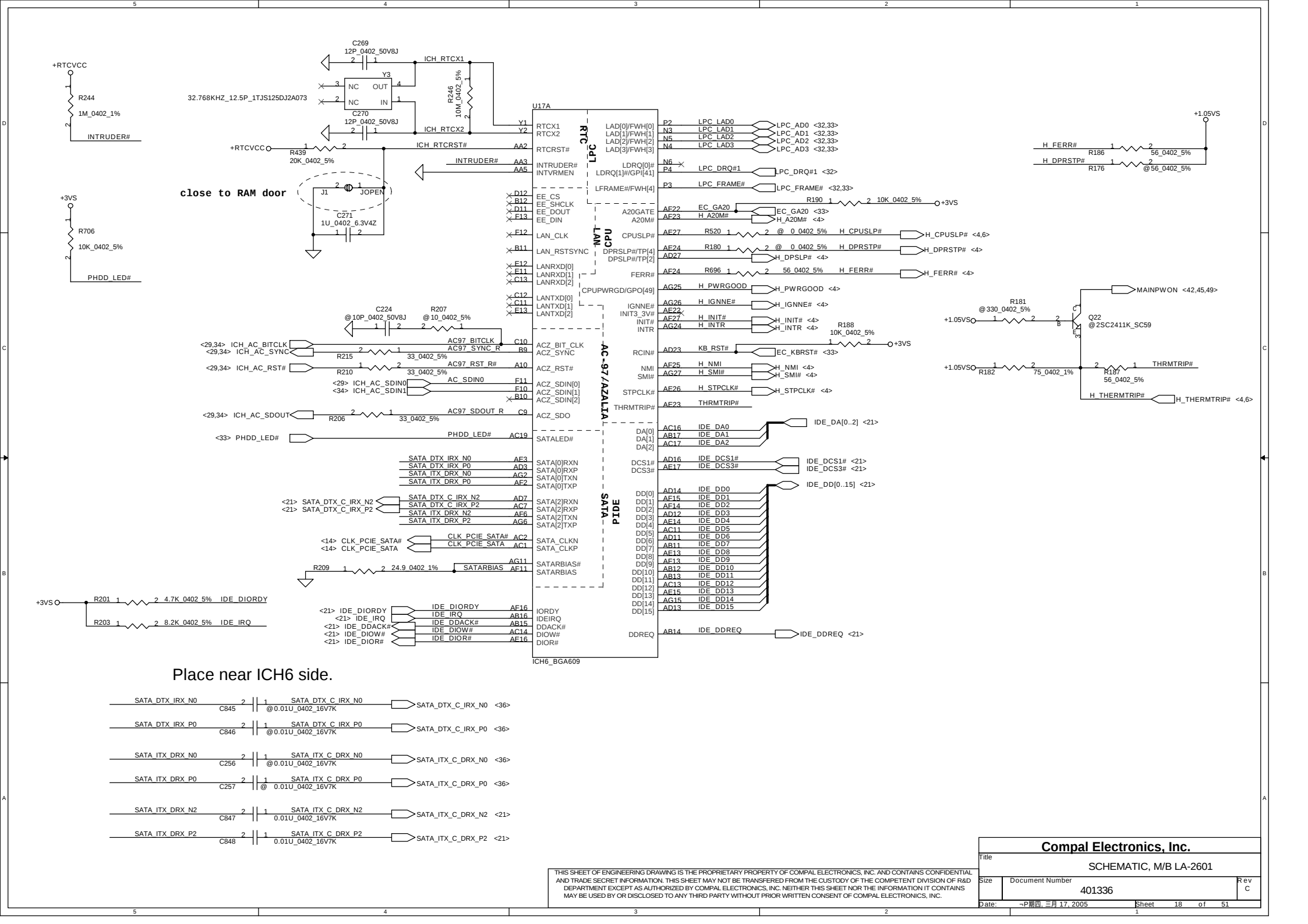
Internal Pull-up.
Sample high destination is LPC.

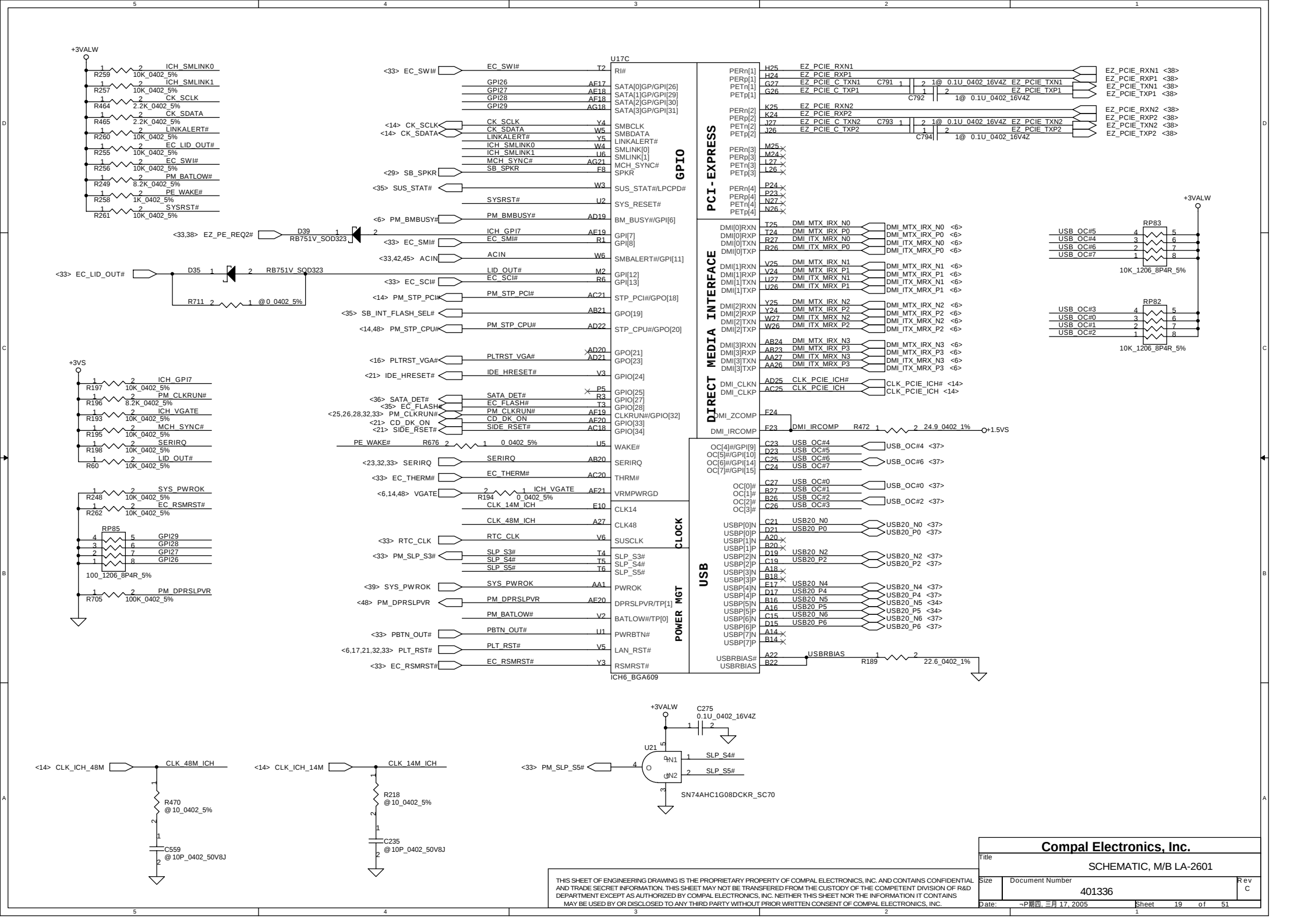


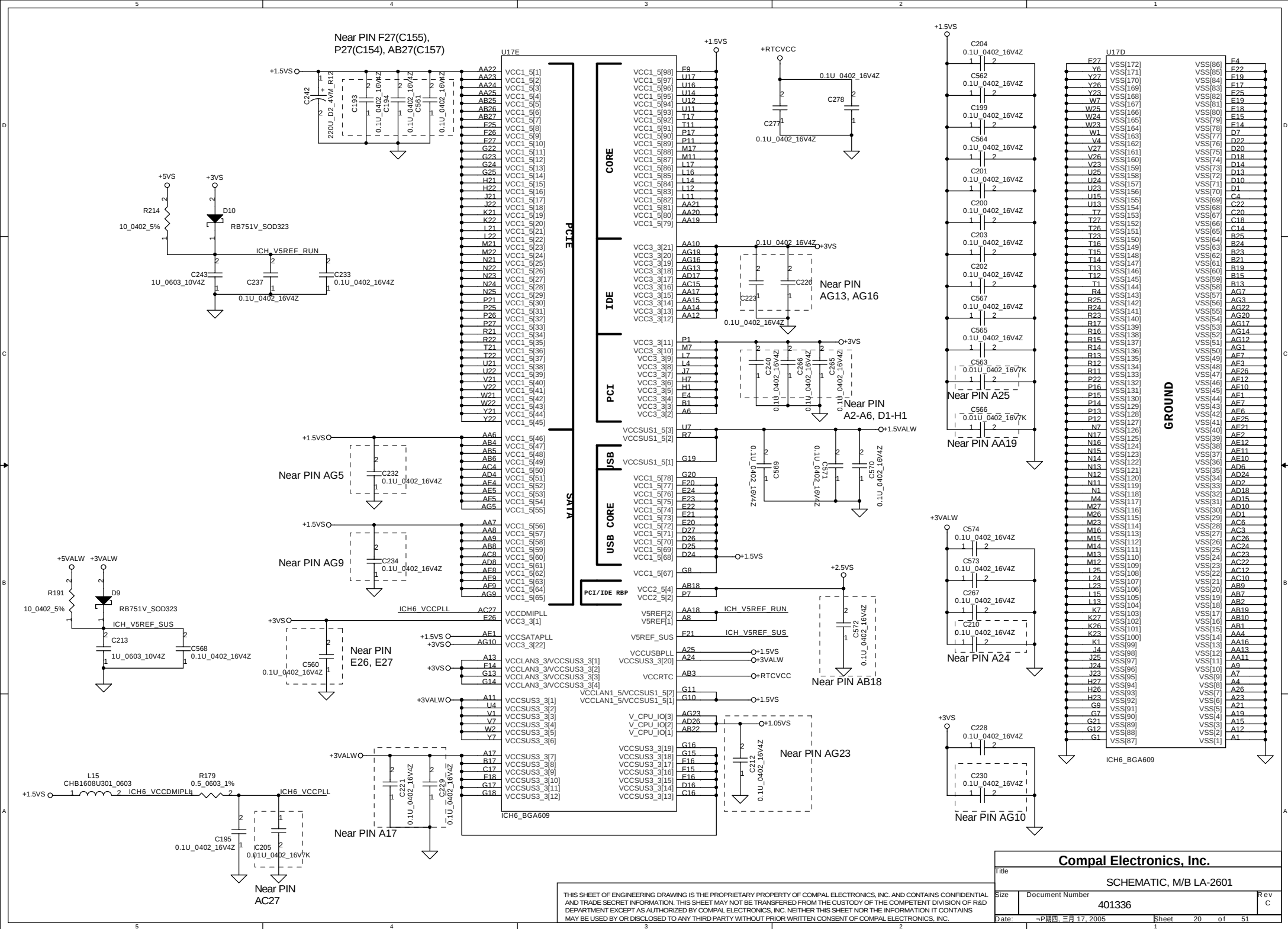
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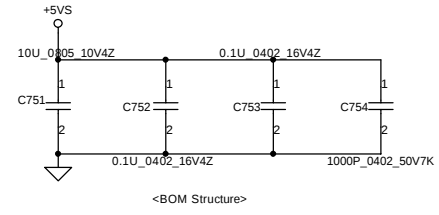
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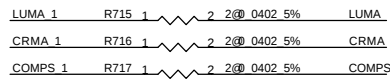
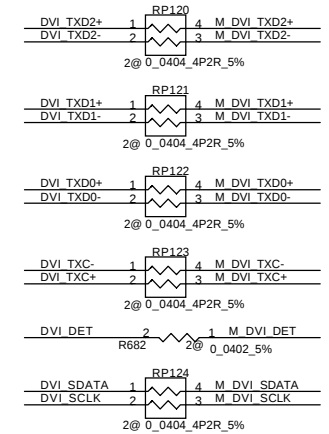
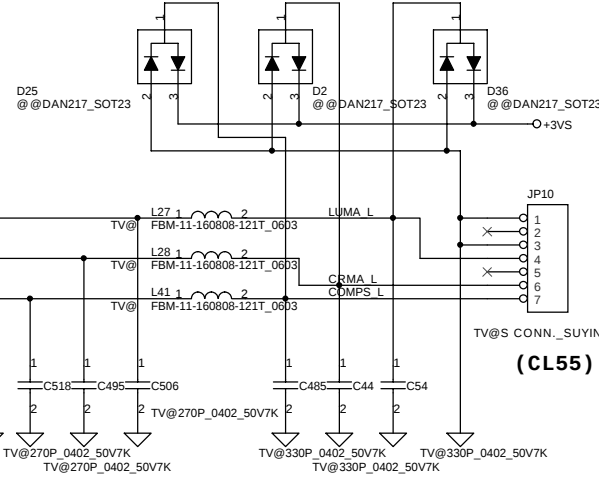
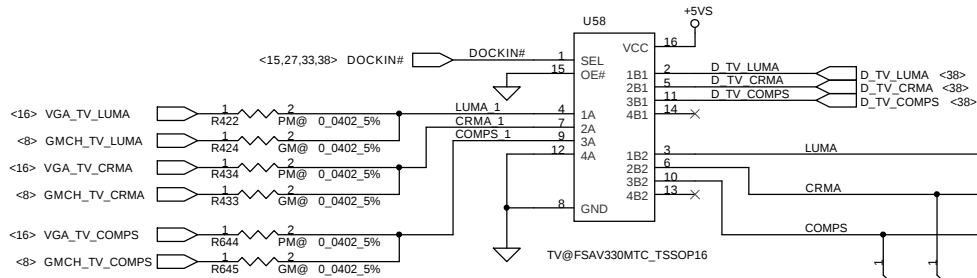
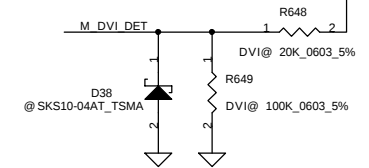
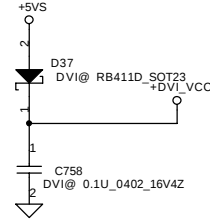
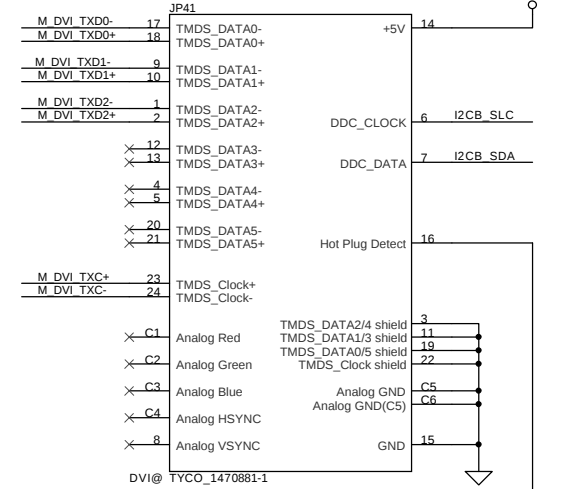
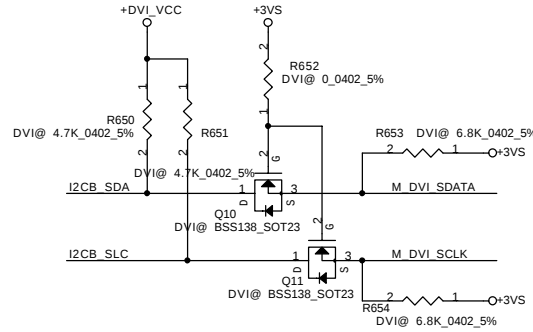
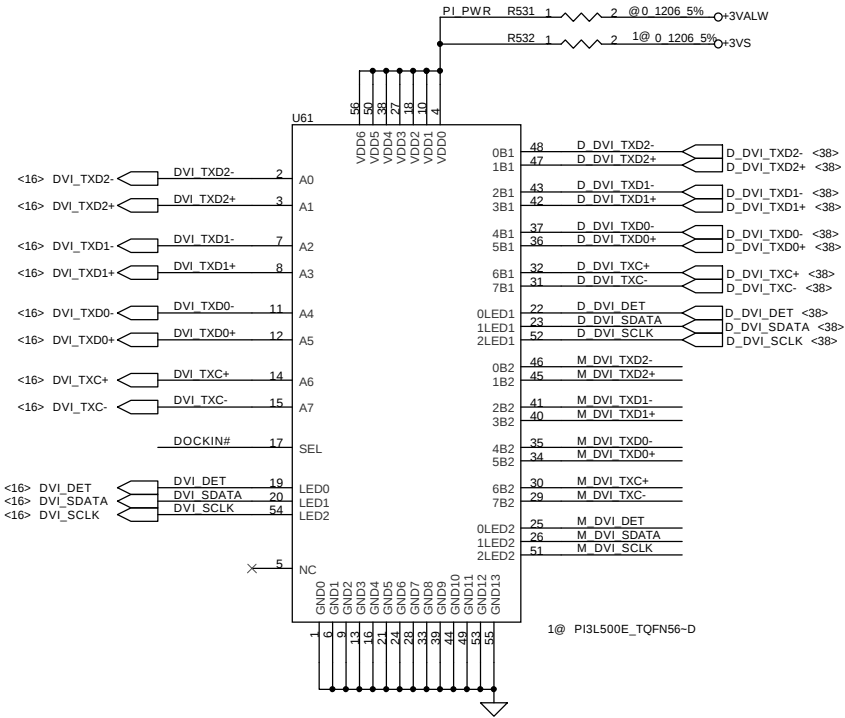




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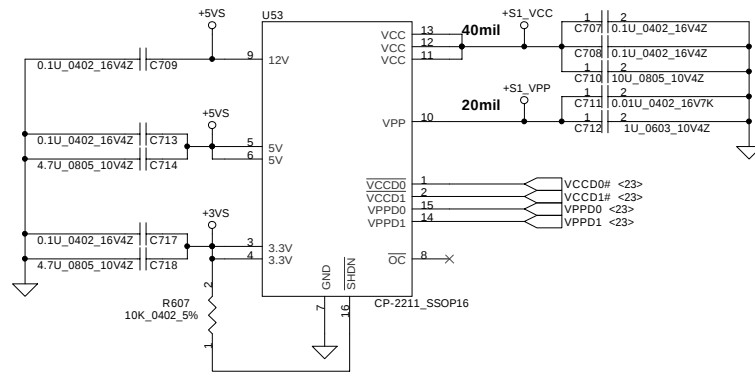
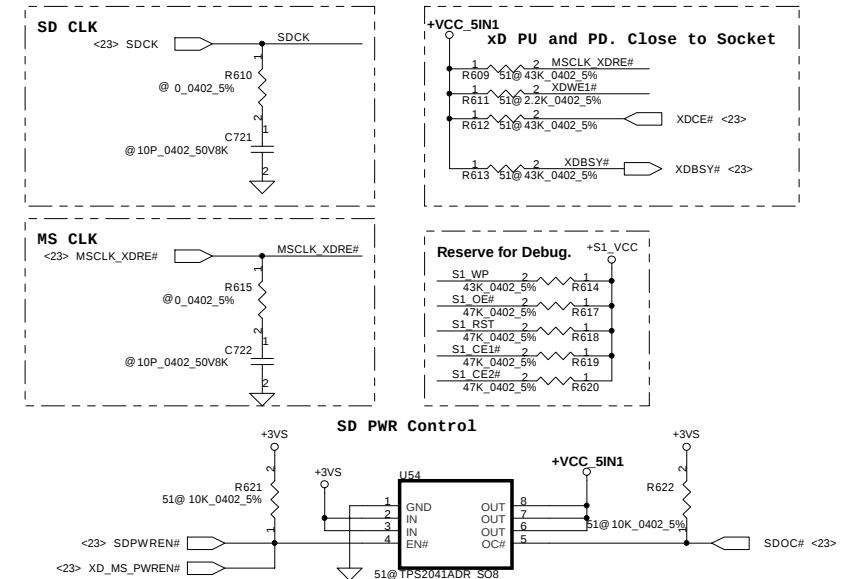
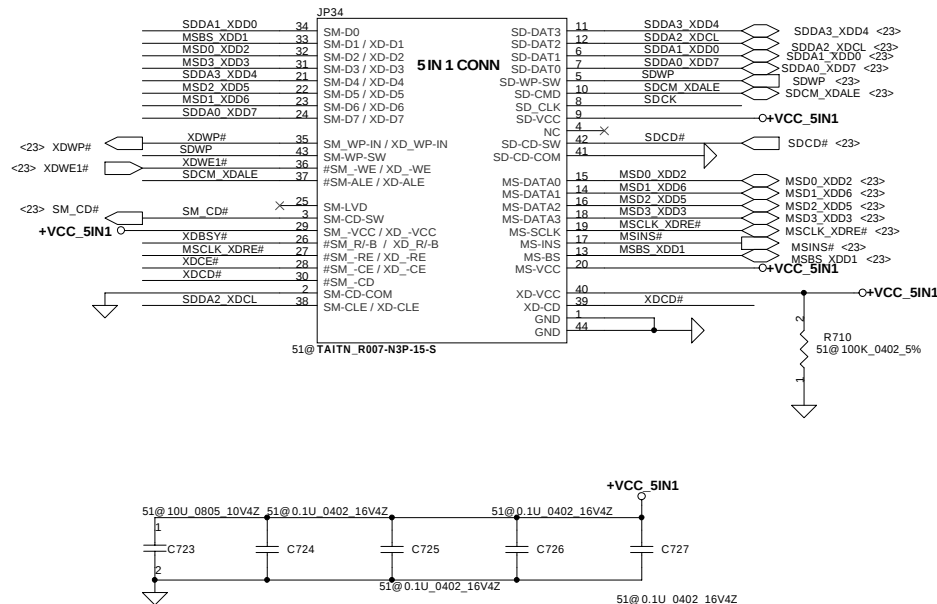
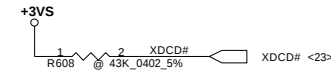
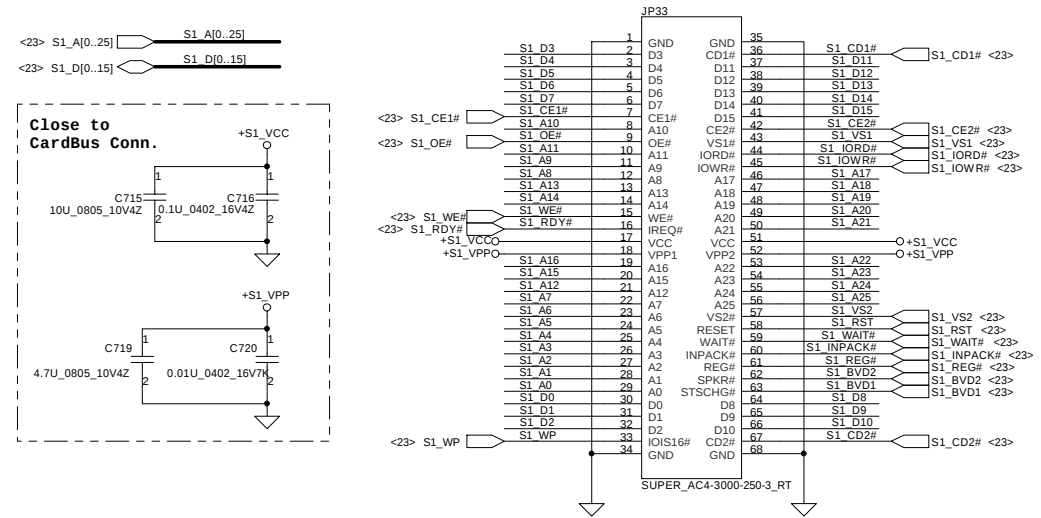
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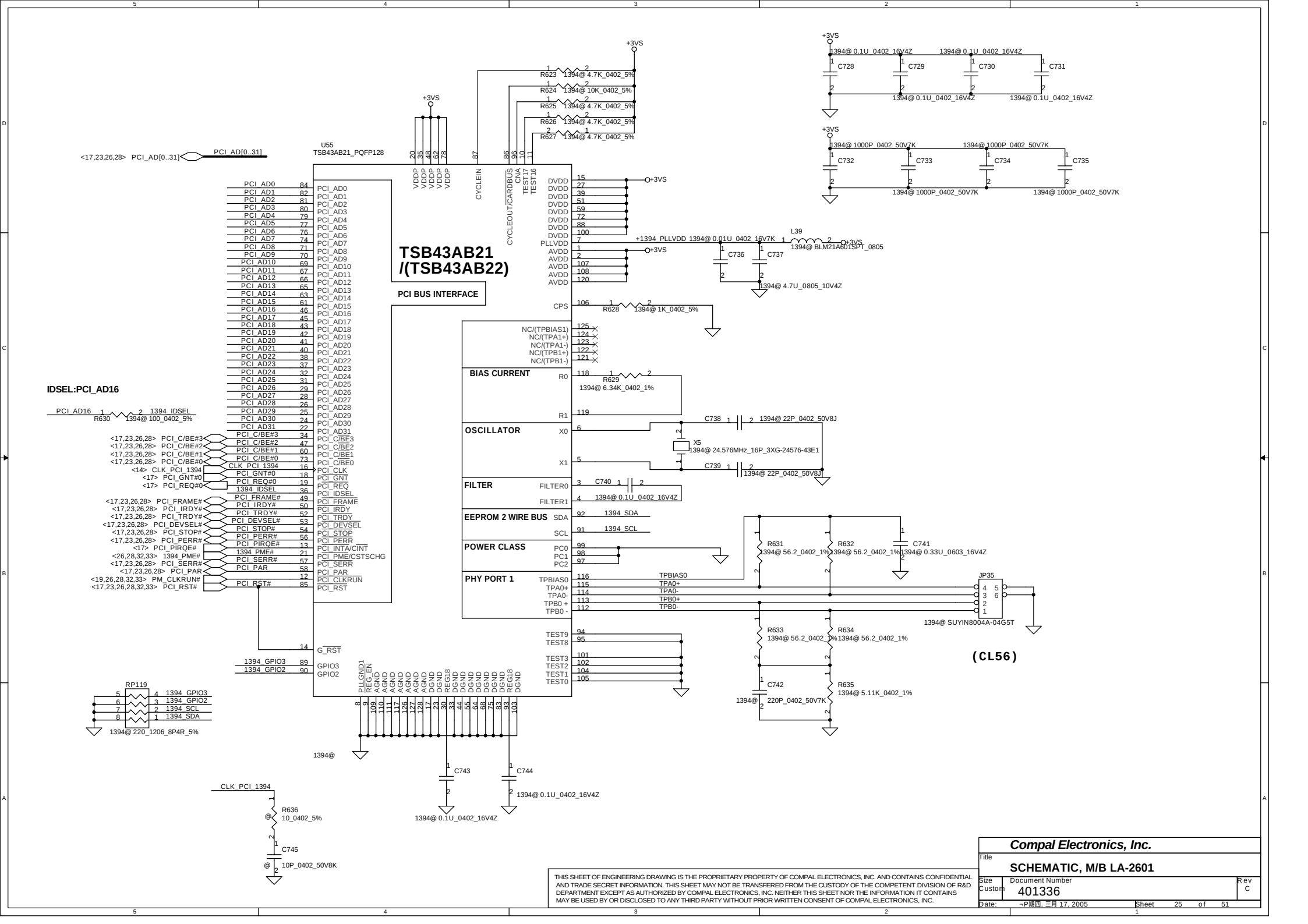


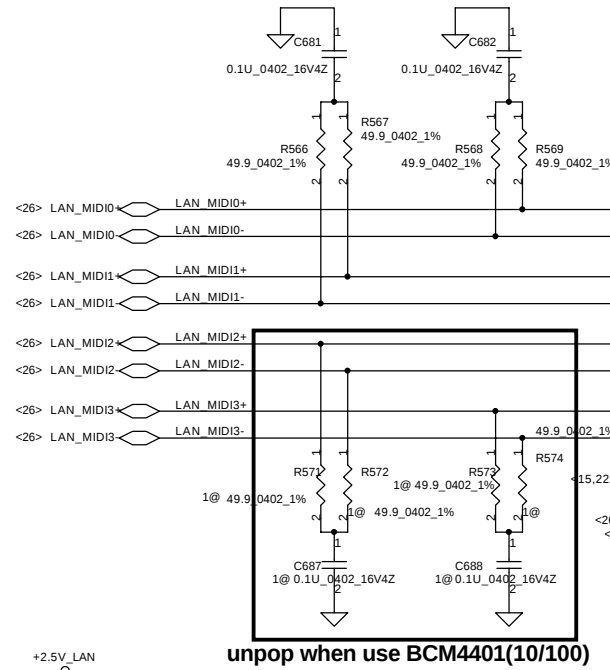
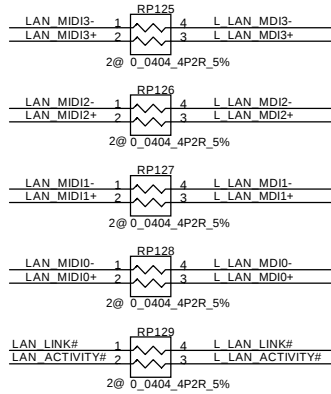
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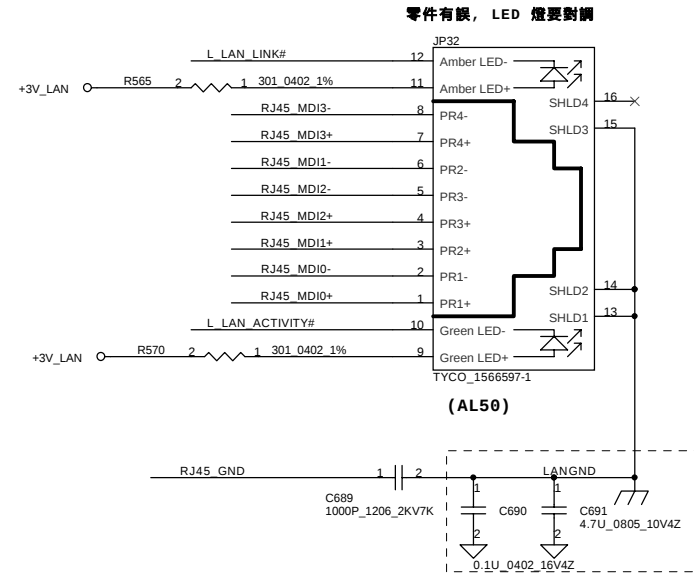
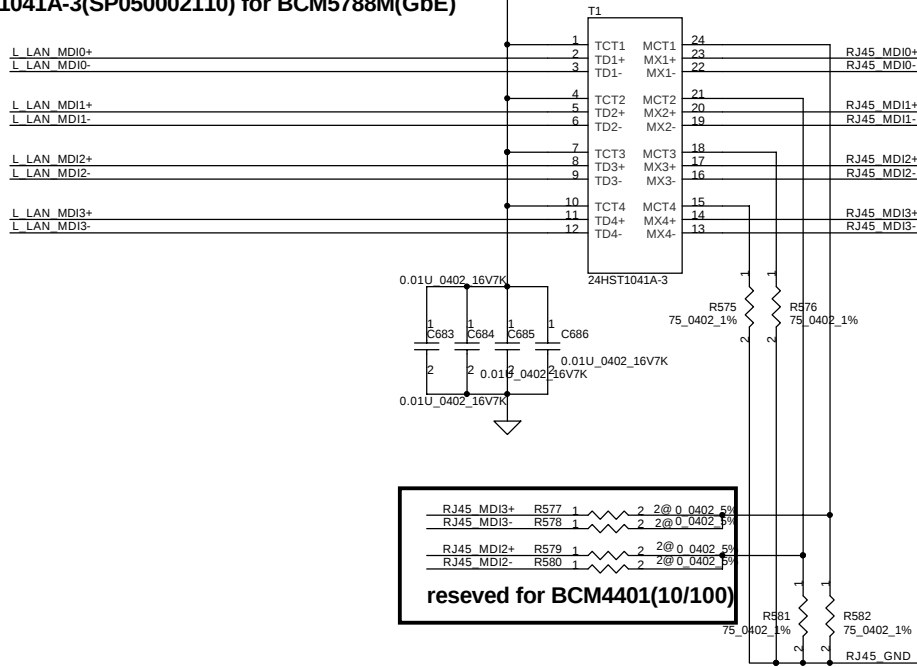
PCMCIA Power Controller

**CardBus Socket**





24ST0023-3(SP050004200) for BCM4401(10/100)
24HST1041A-3(SP050002110) for BCM5788M(GbE)

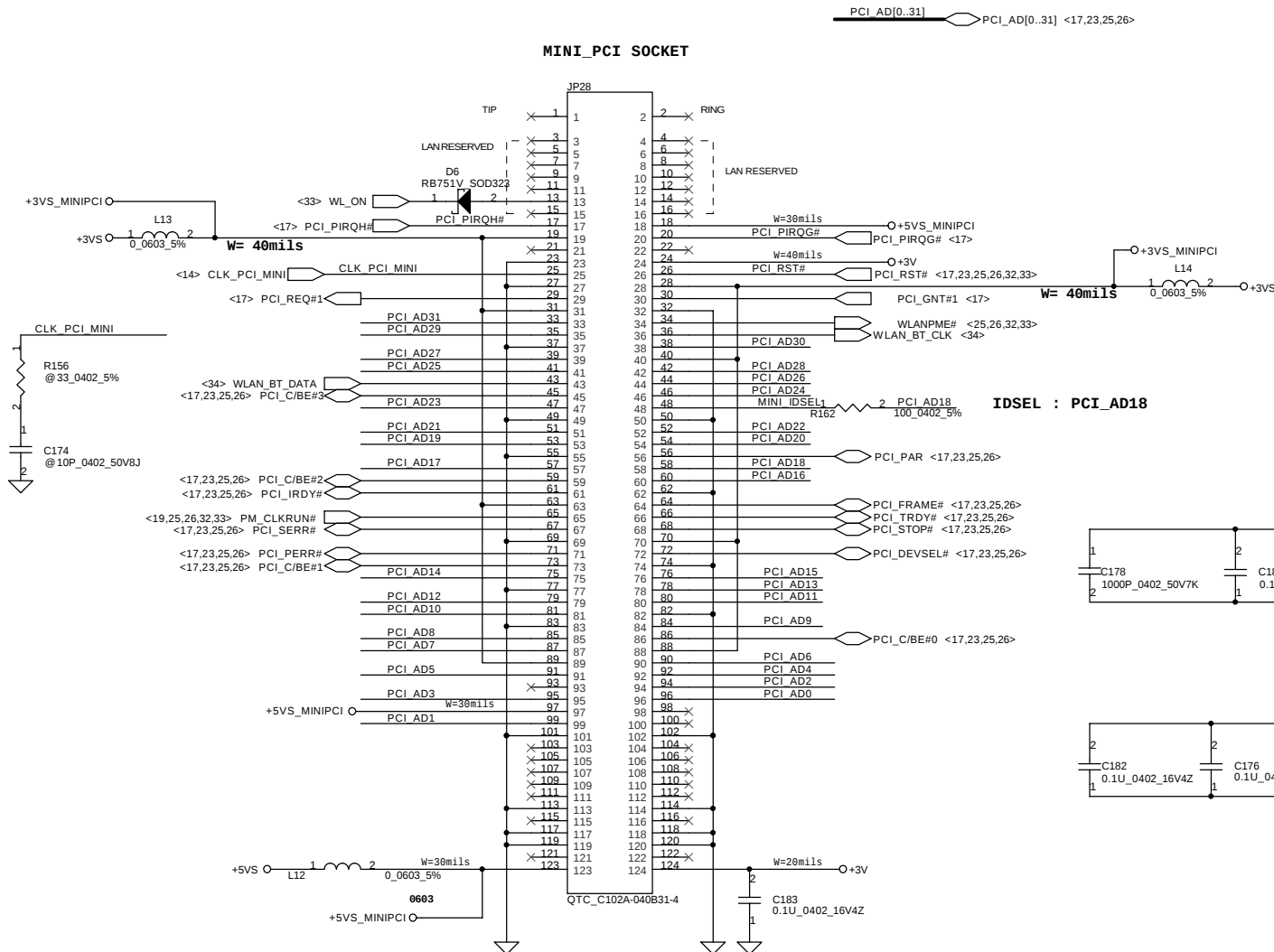


LAN BCM5788M/BCM4401KFB

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MINI_PCI SOCKET

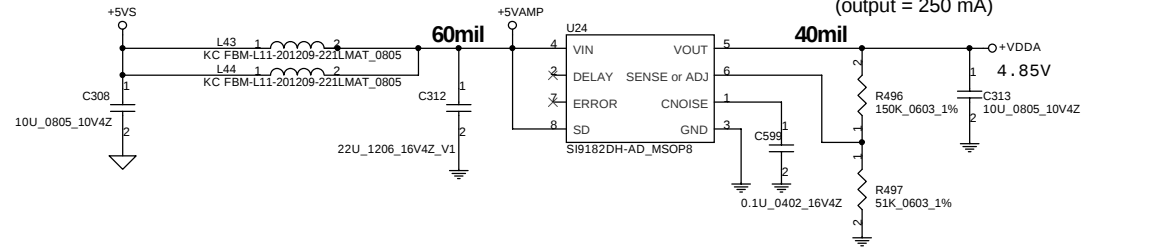
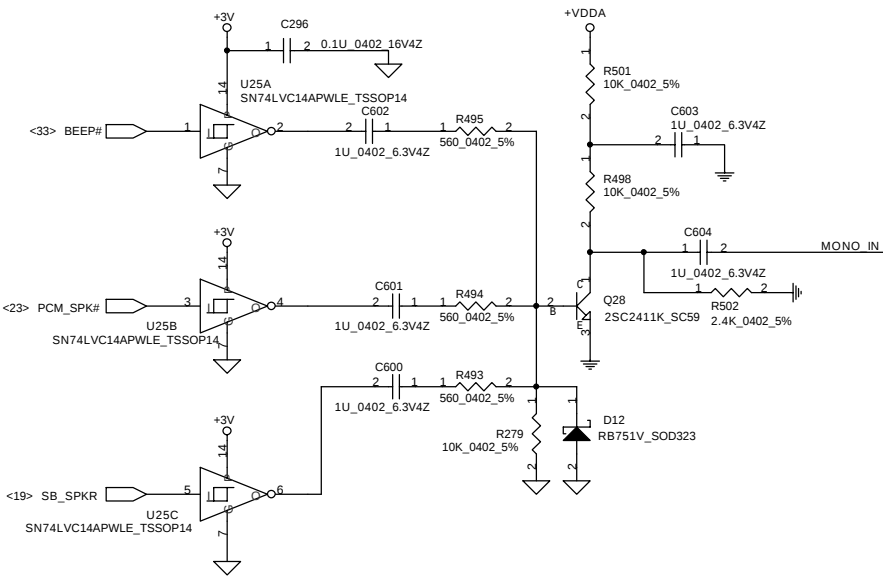


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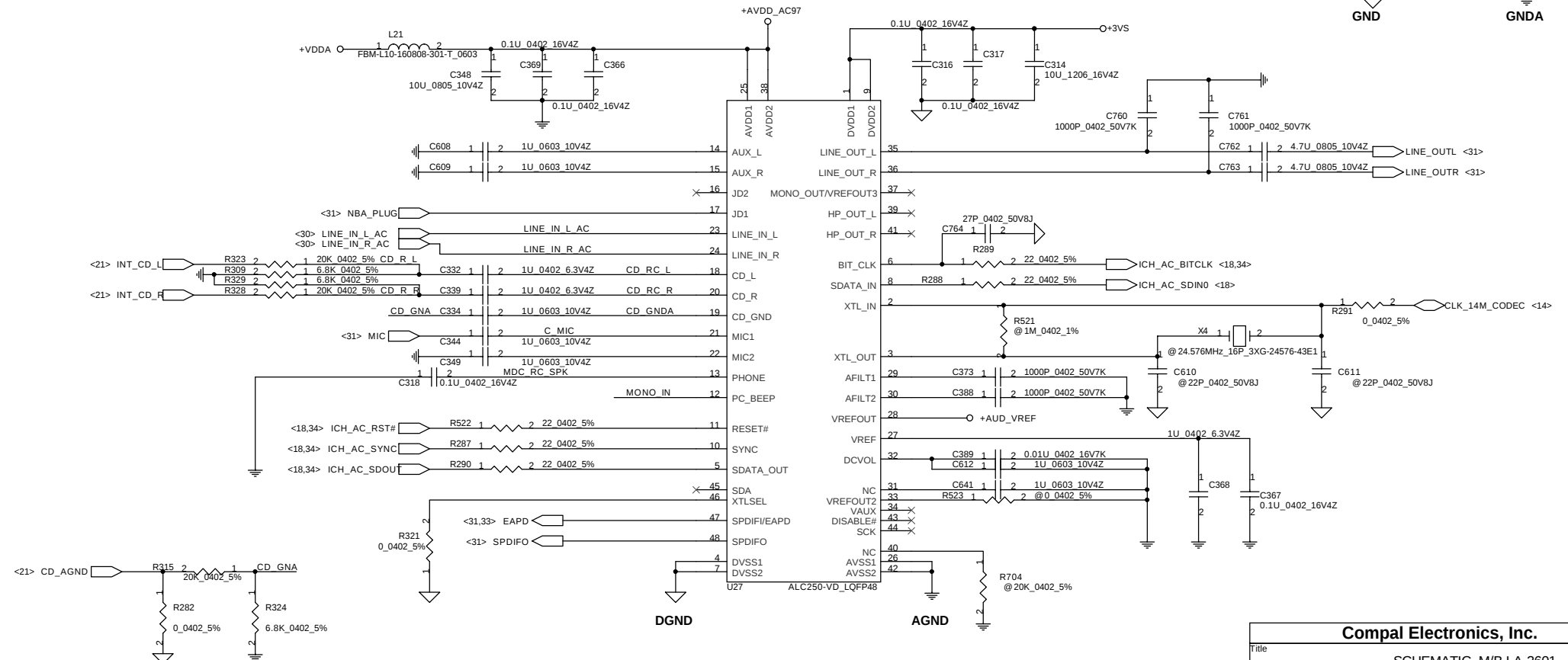
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AC97 Codec

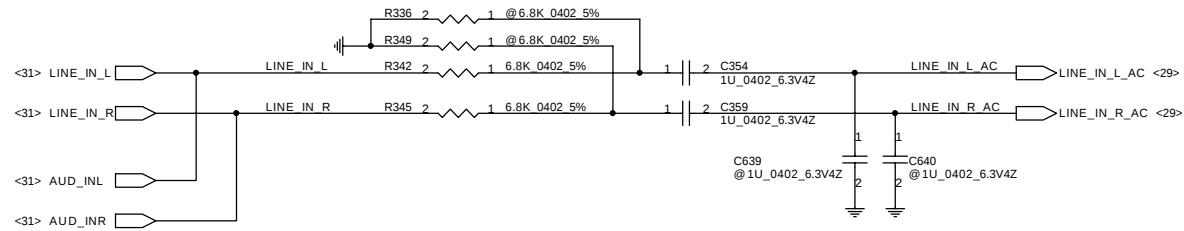


With 14.318Mhz : R321 POP
With 24.576Mhz : R321 DEPOP

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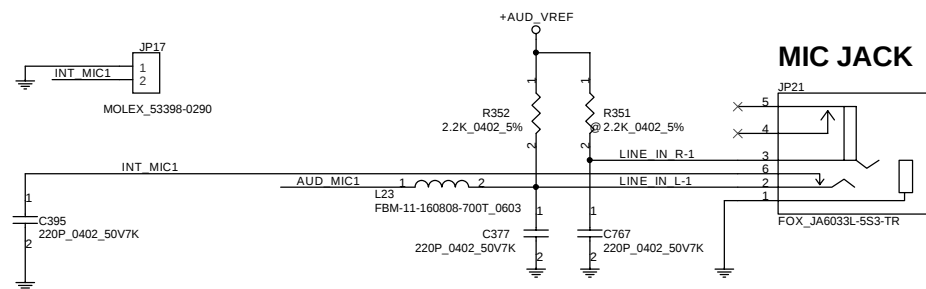
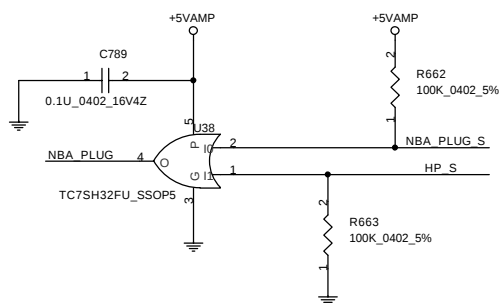
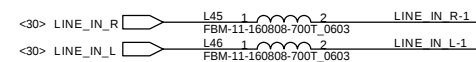
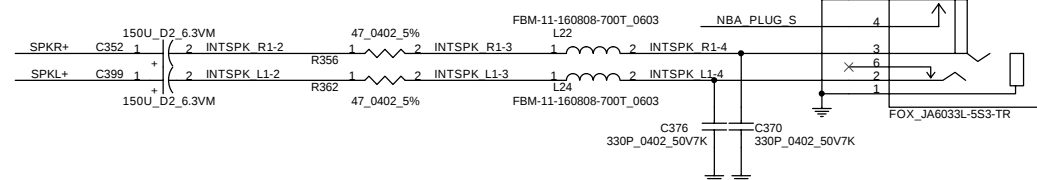
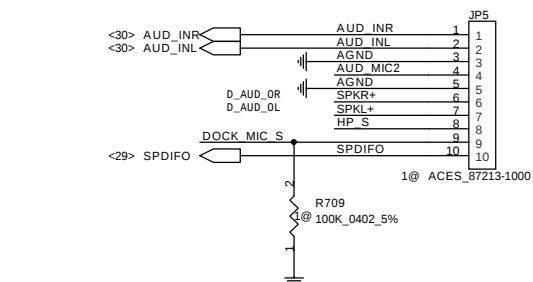
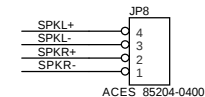
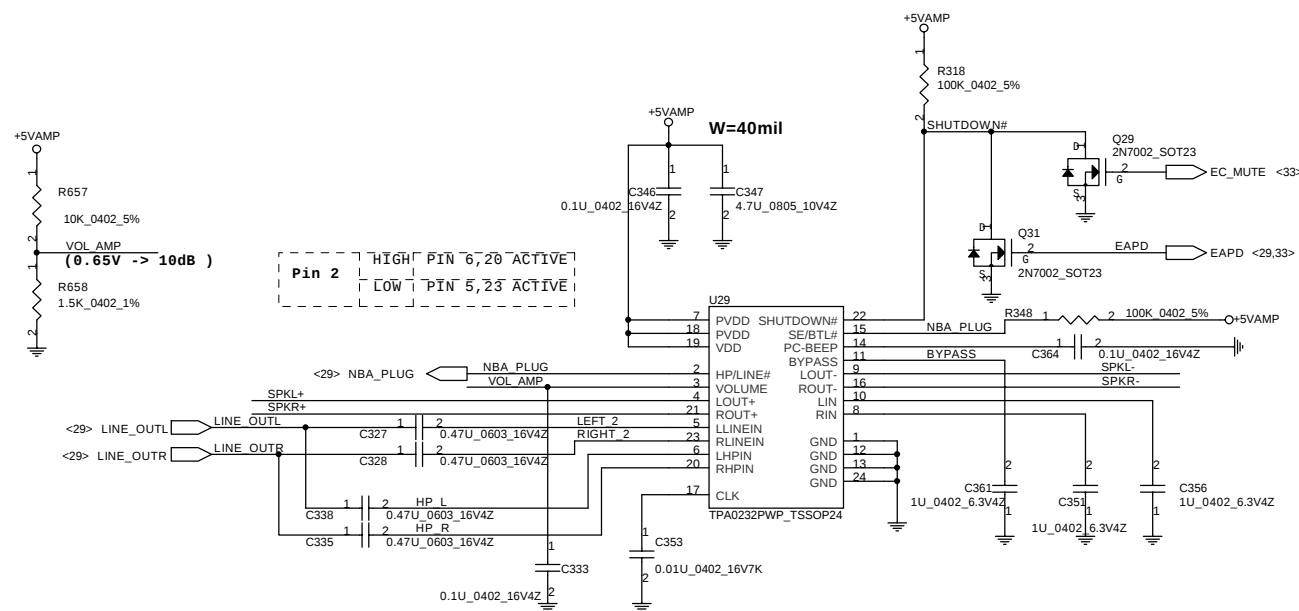
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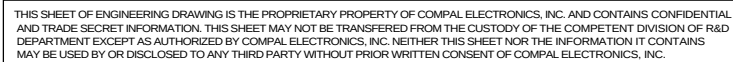
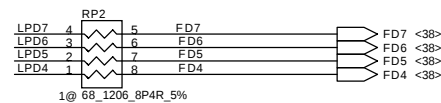
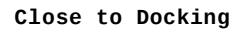
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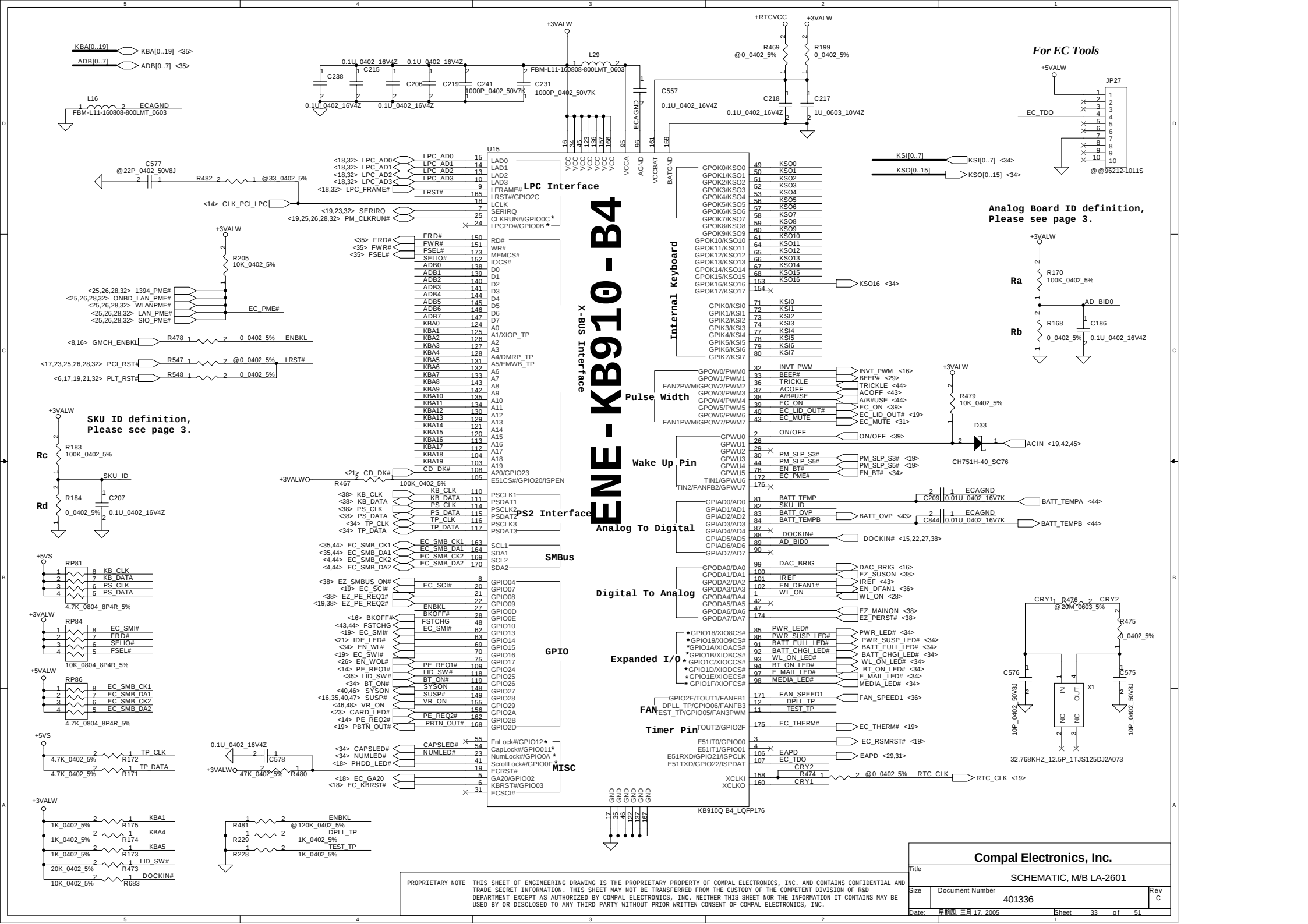
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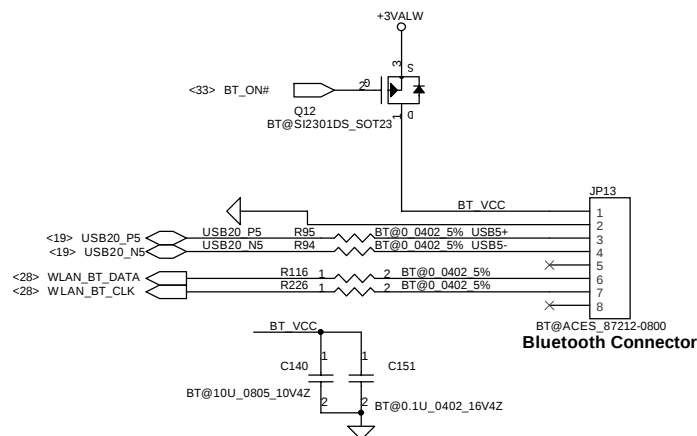
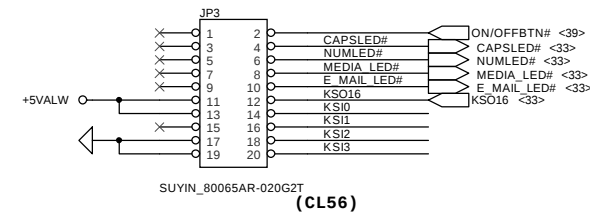


HeadPhone JACK

MIC JACK



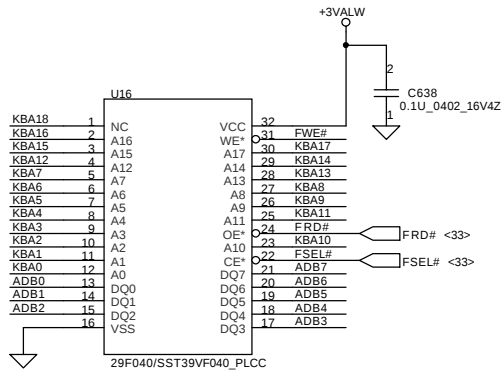




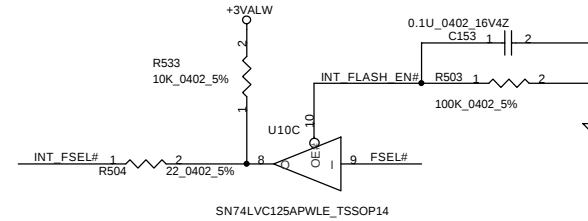
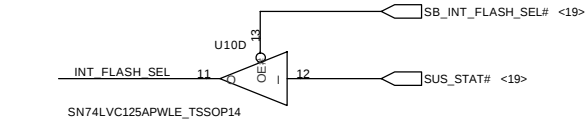
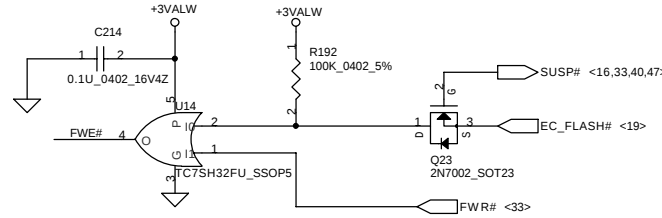
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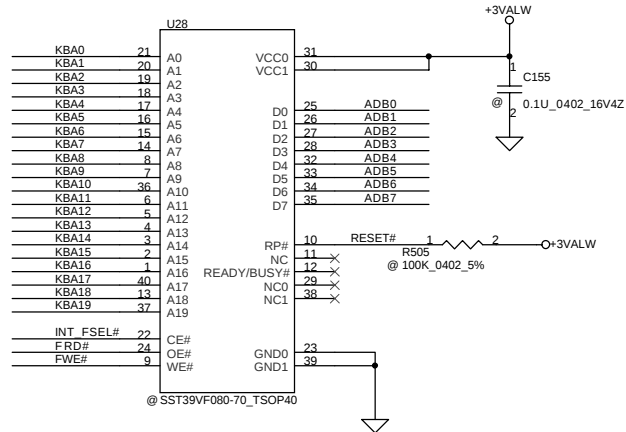
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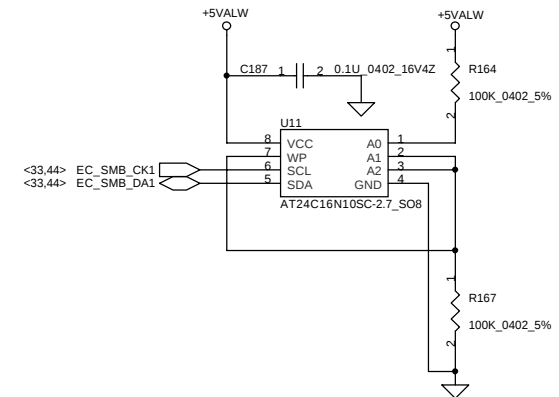
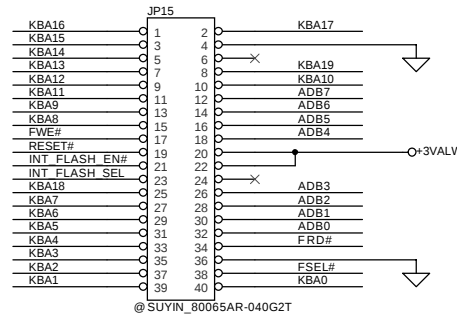
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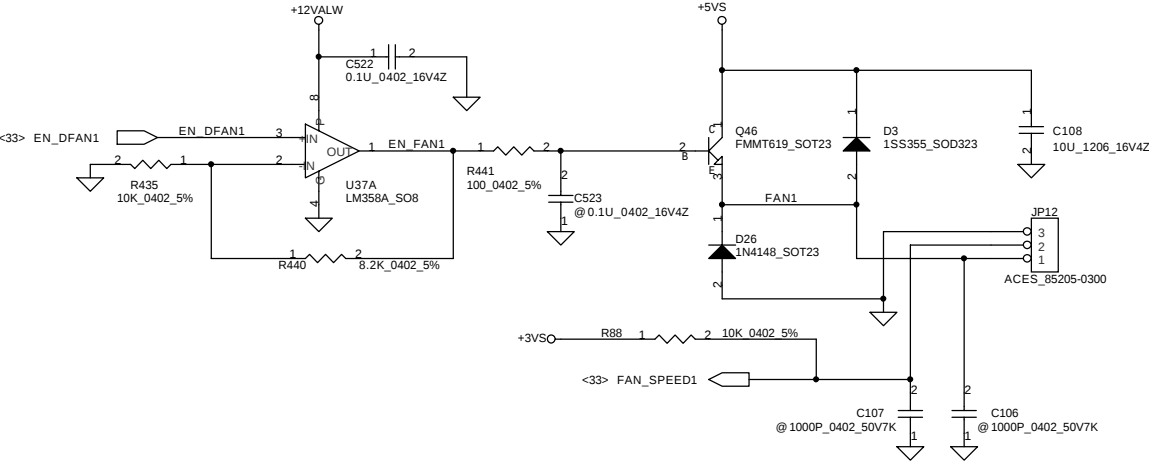
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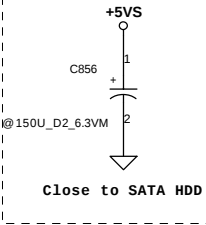
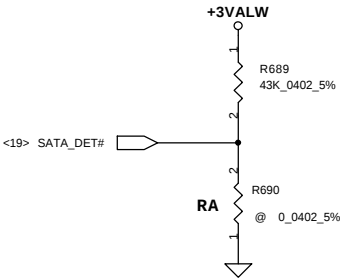
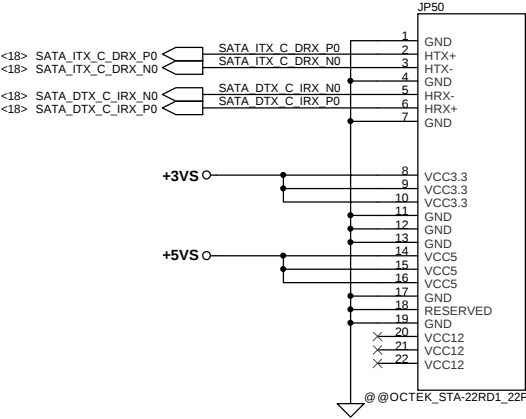
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FAN Conn

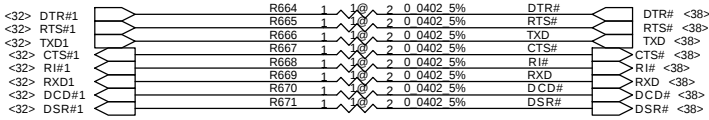


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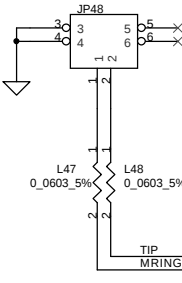


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Presence	POP
Removed	NO POP

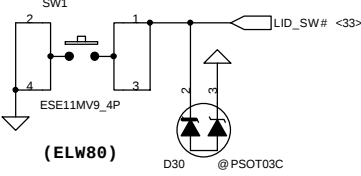
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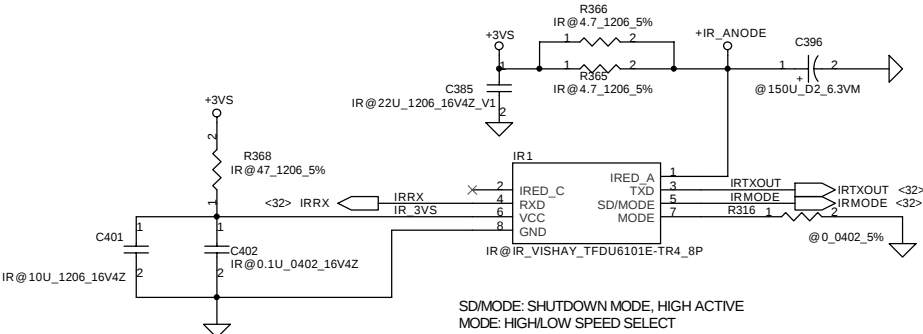
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MOLEX_53398-0290
(ELW80)

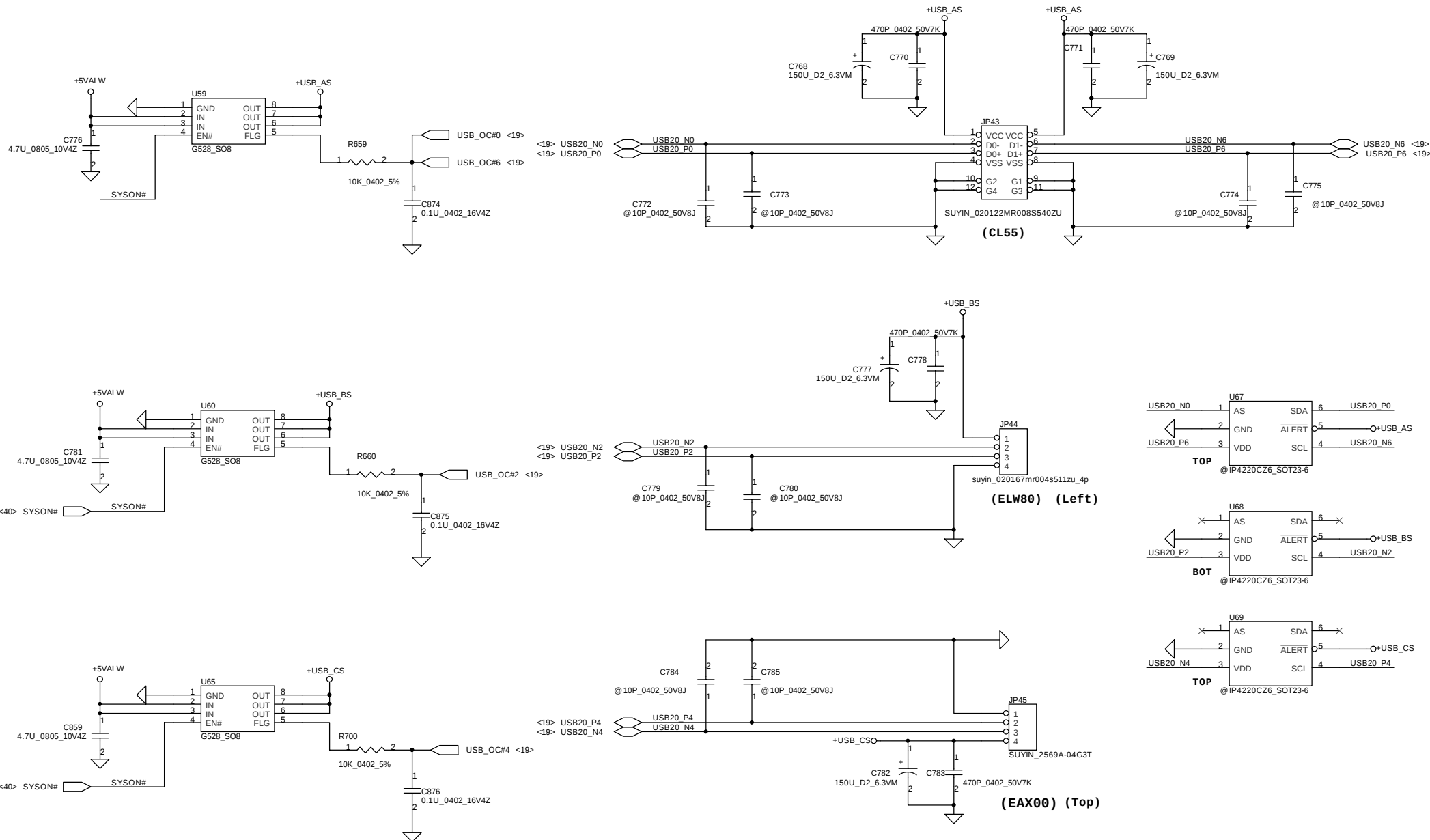


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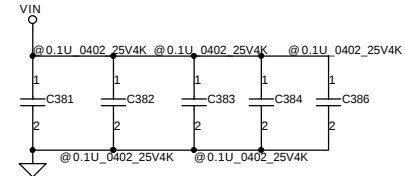
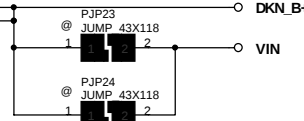
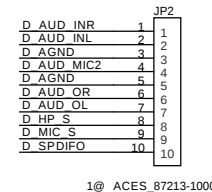
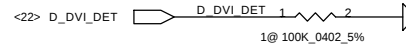
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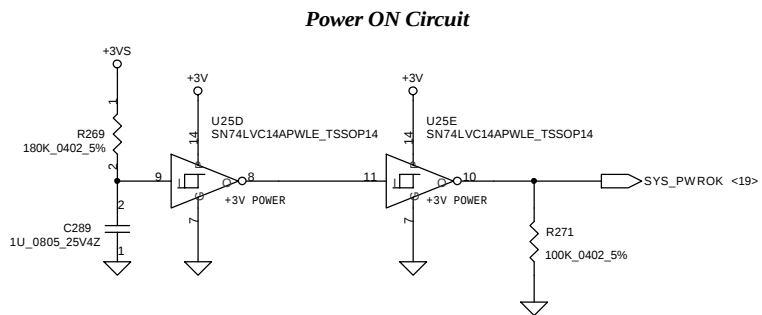
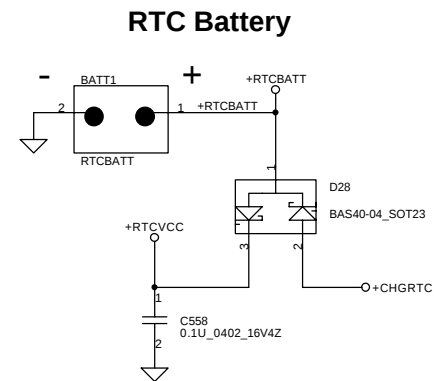
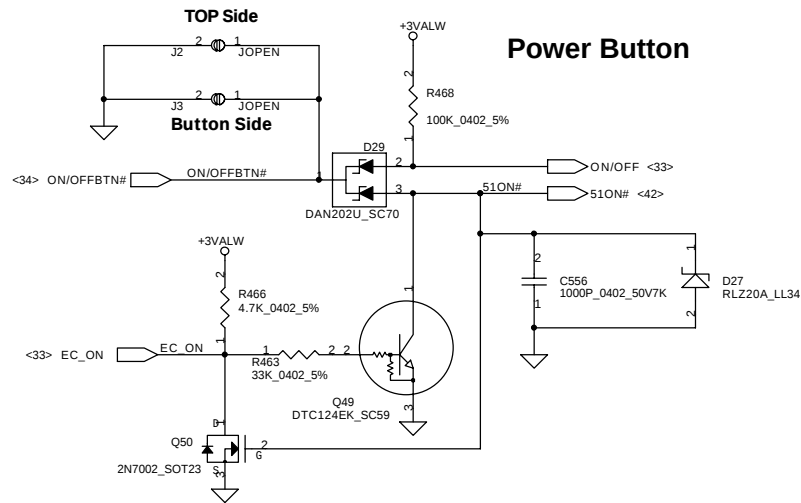
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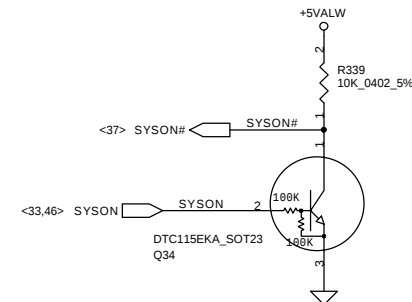
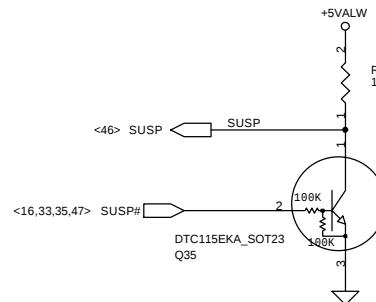
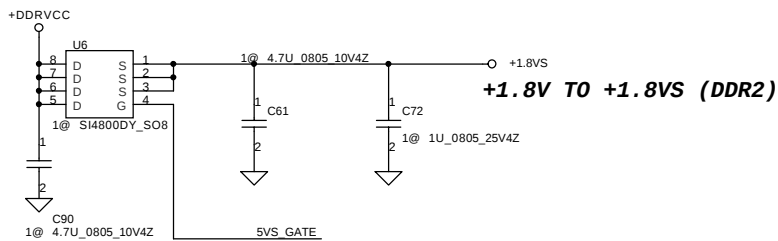
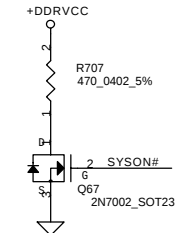
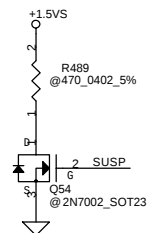
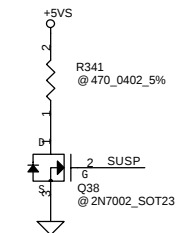
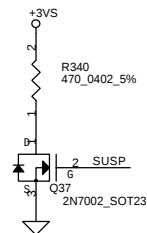
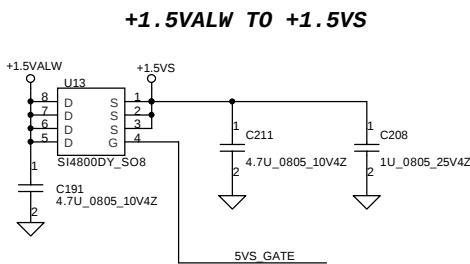
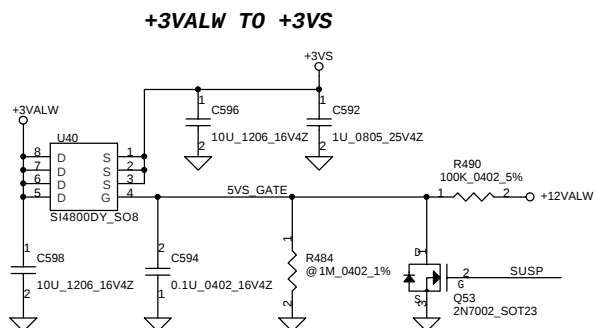
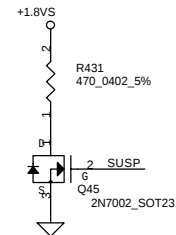
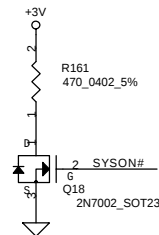
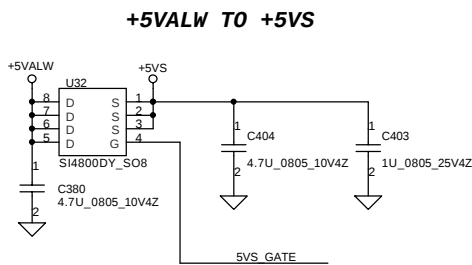
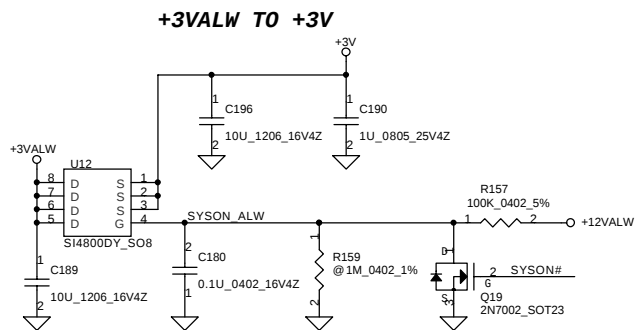
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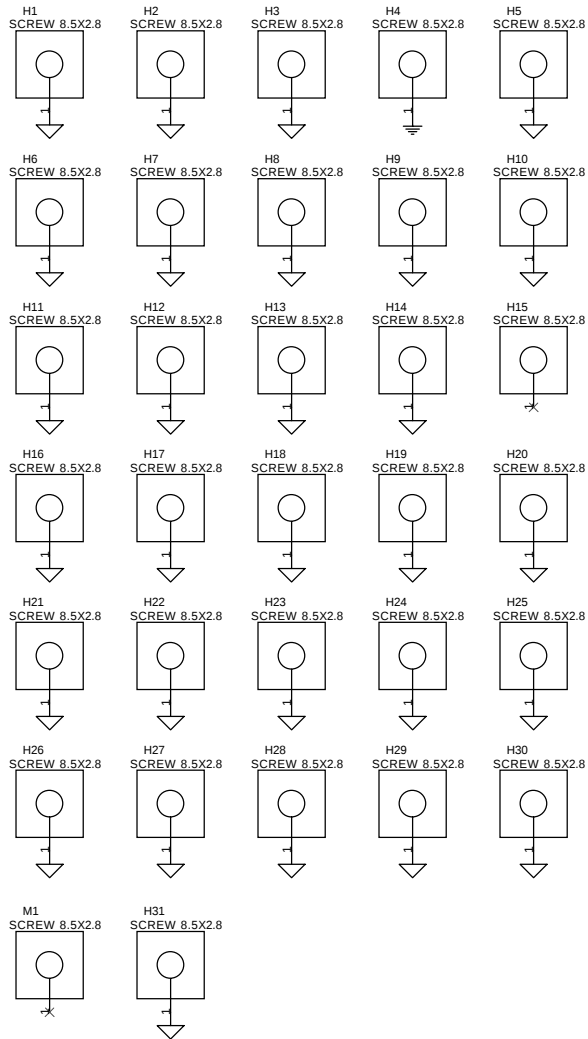
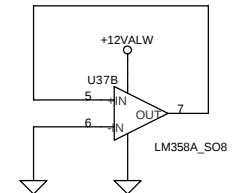
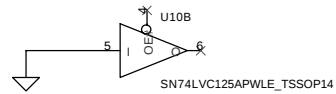
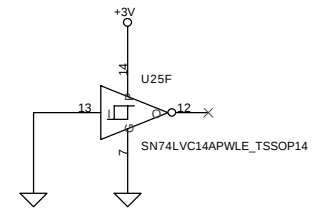
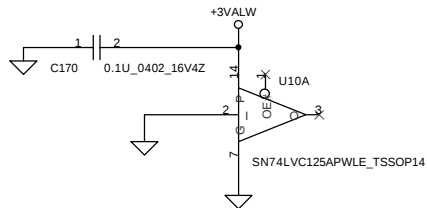
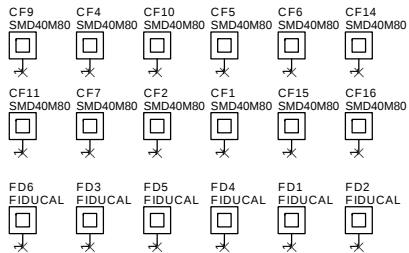
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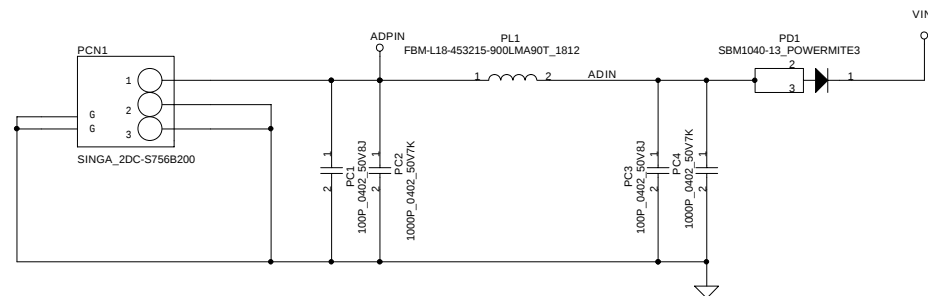
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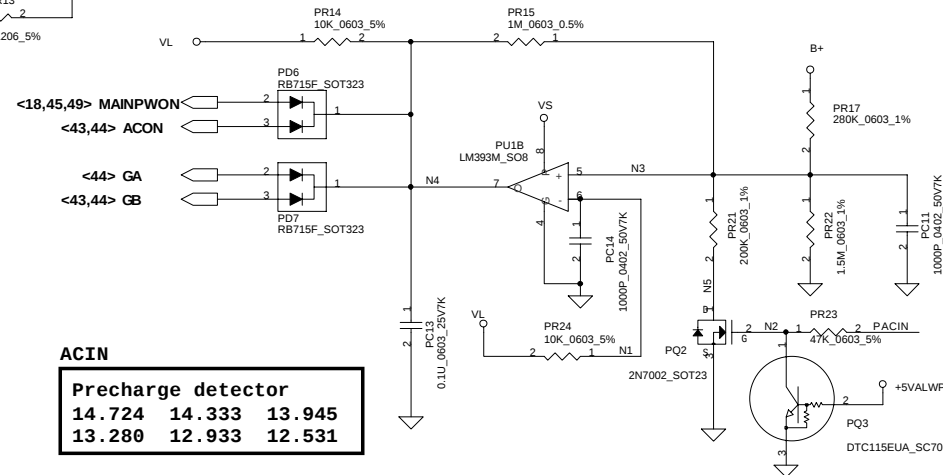
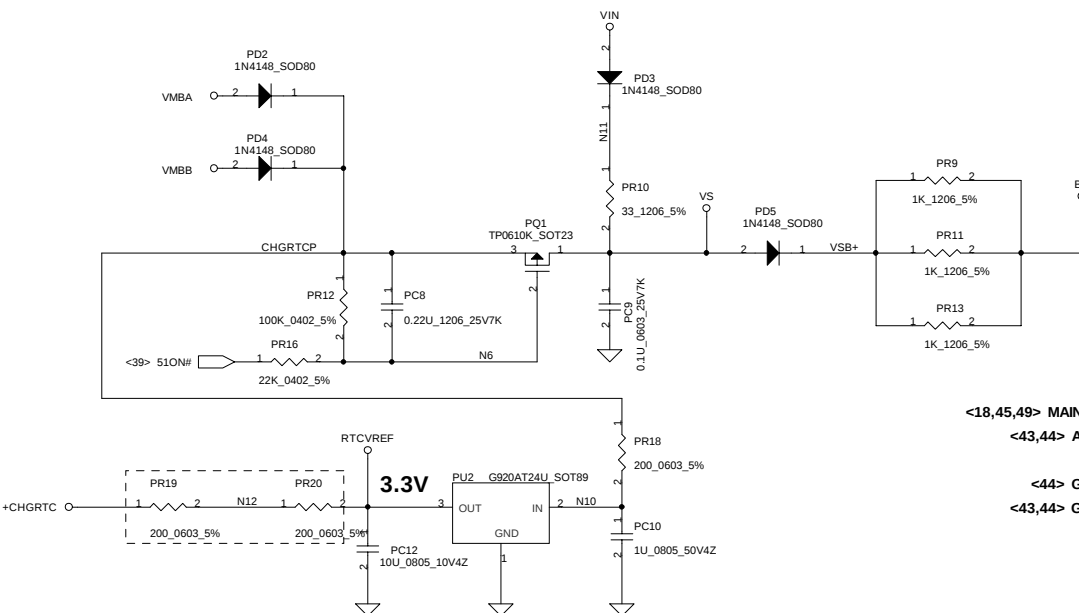
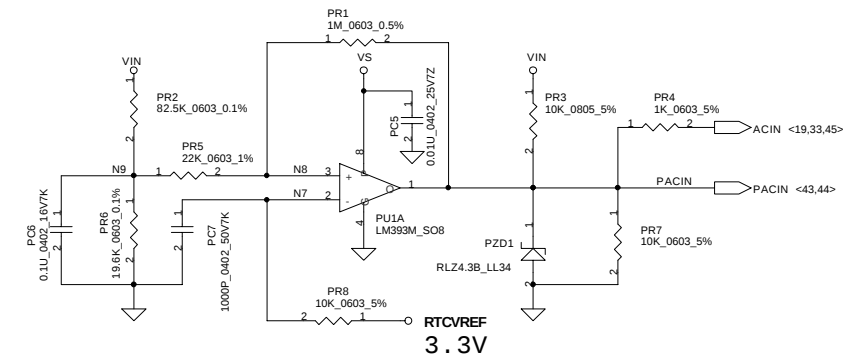
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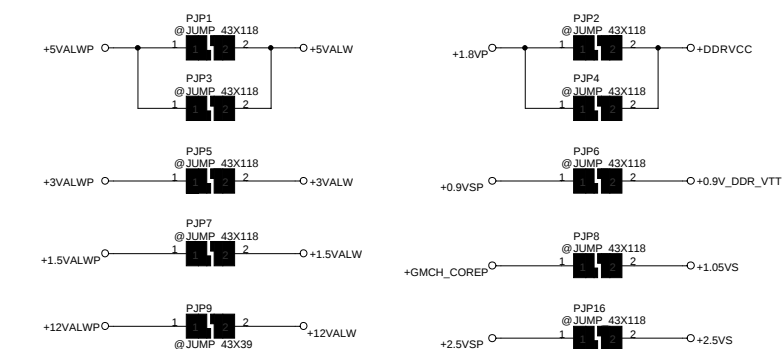


Vin Detector		
18.234	17.841	17.449
17.597	17.210	16.813



ACIN		
Precharge detector		
14.724	14.333	13.945
13.280	12.933	12.531

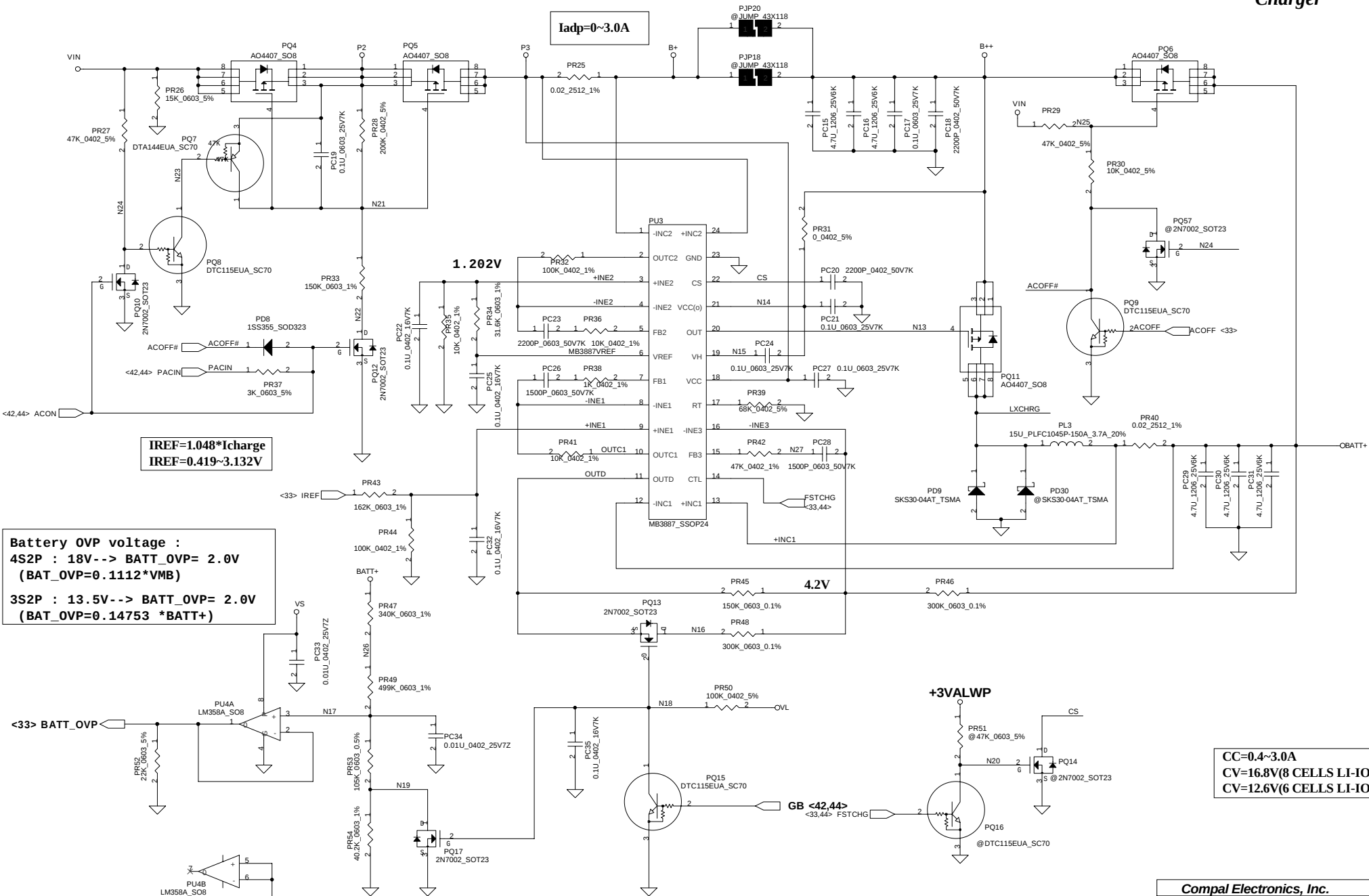
BATT		
Precharge detector		
7.558	7.333	7.112
6.108	5.933	5.704



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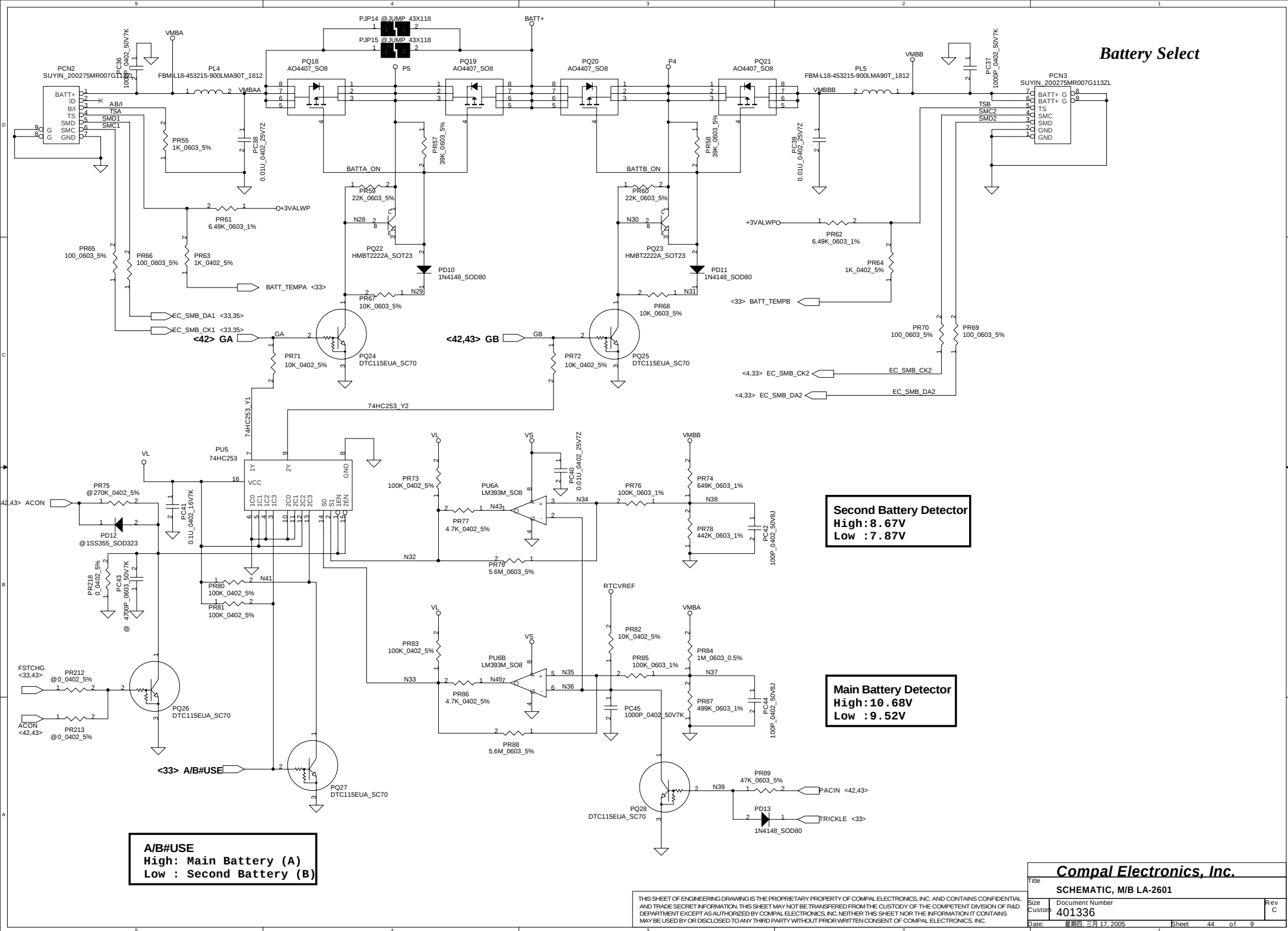
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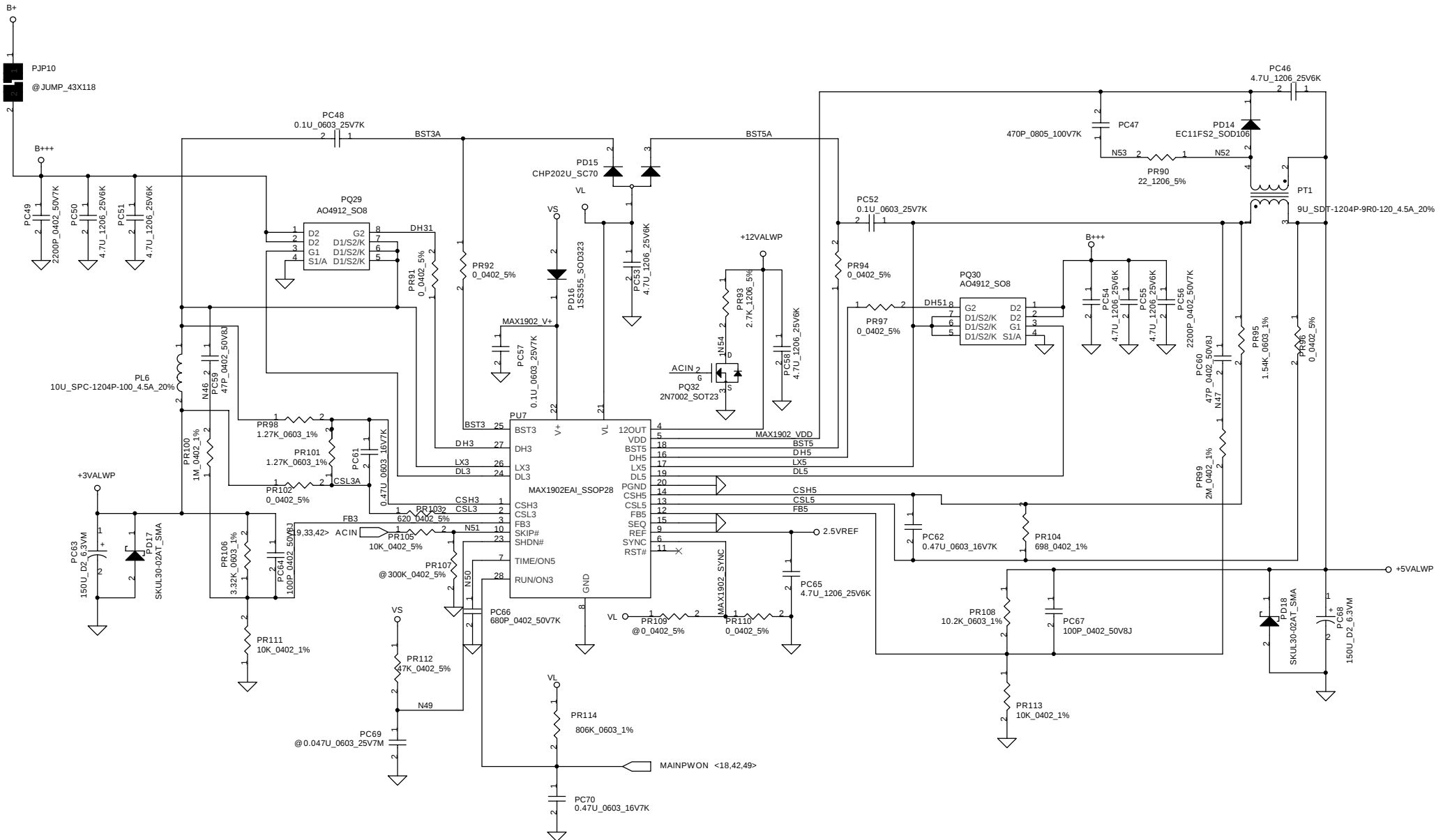
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Battery Select



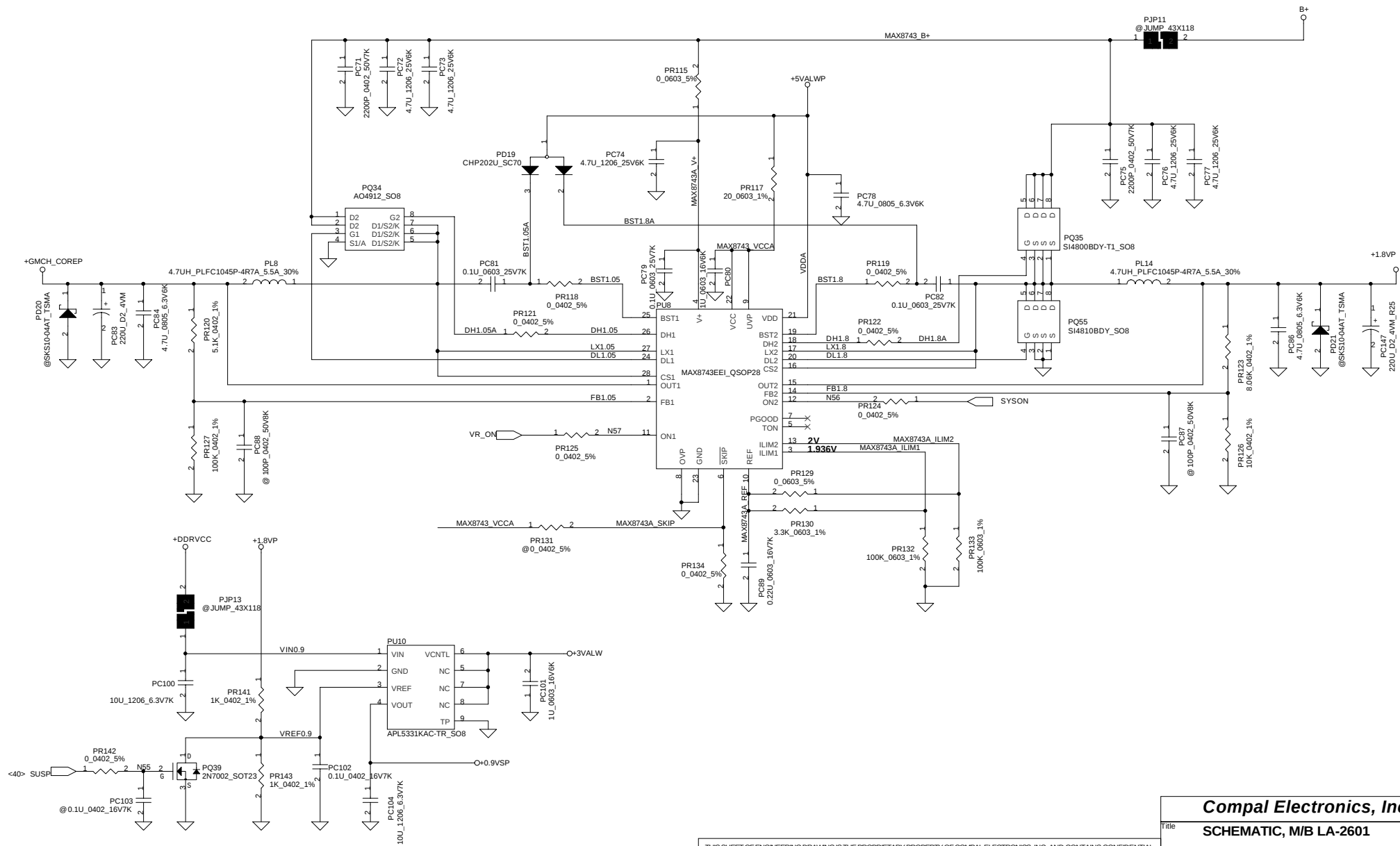
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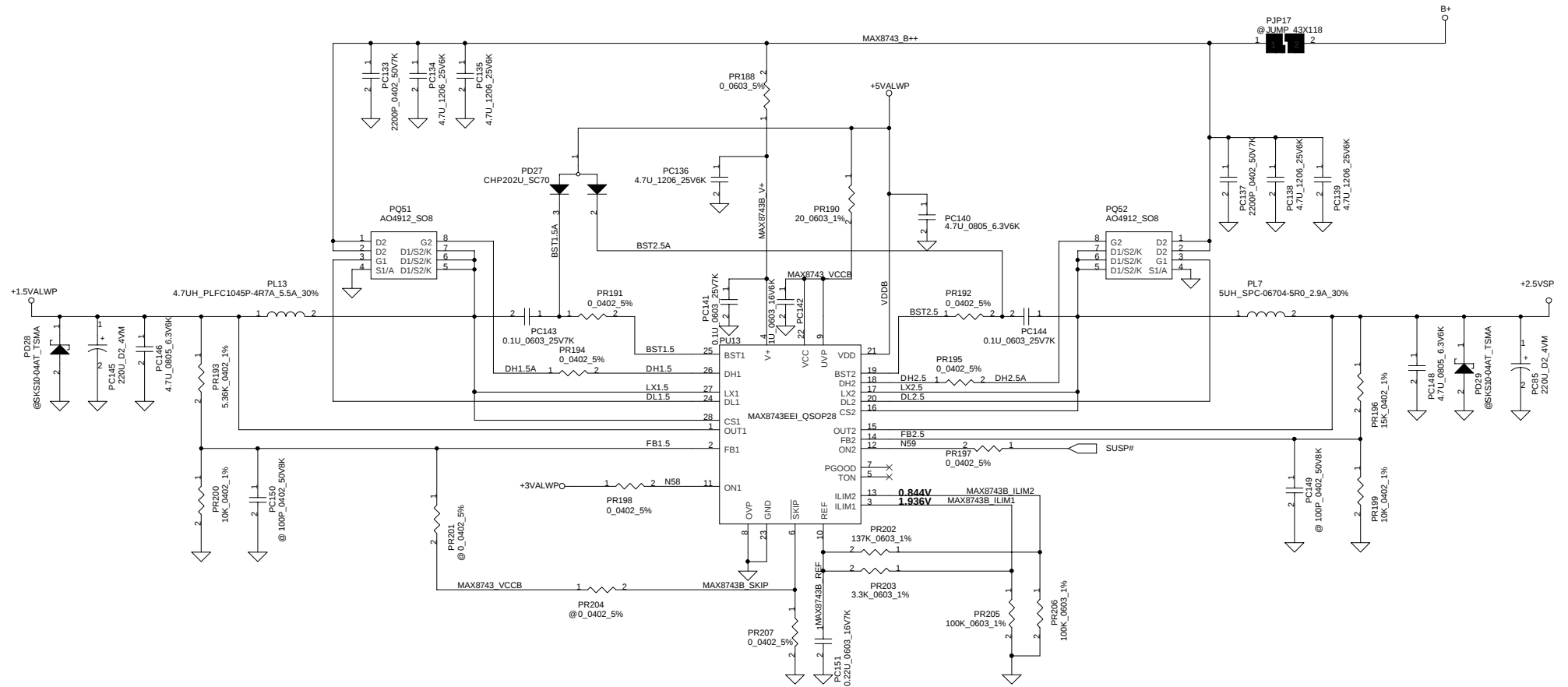
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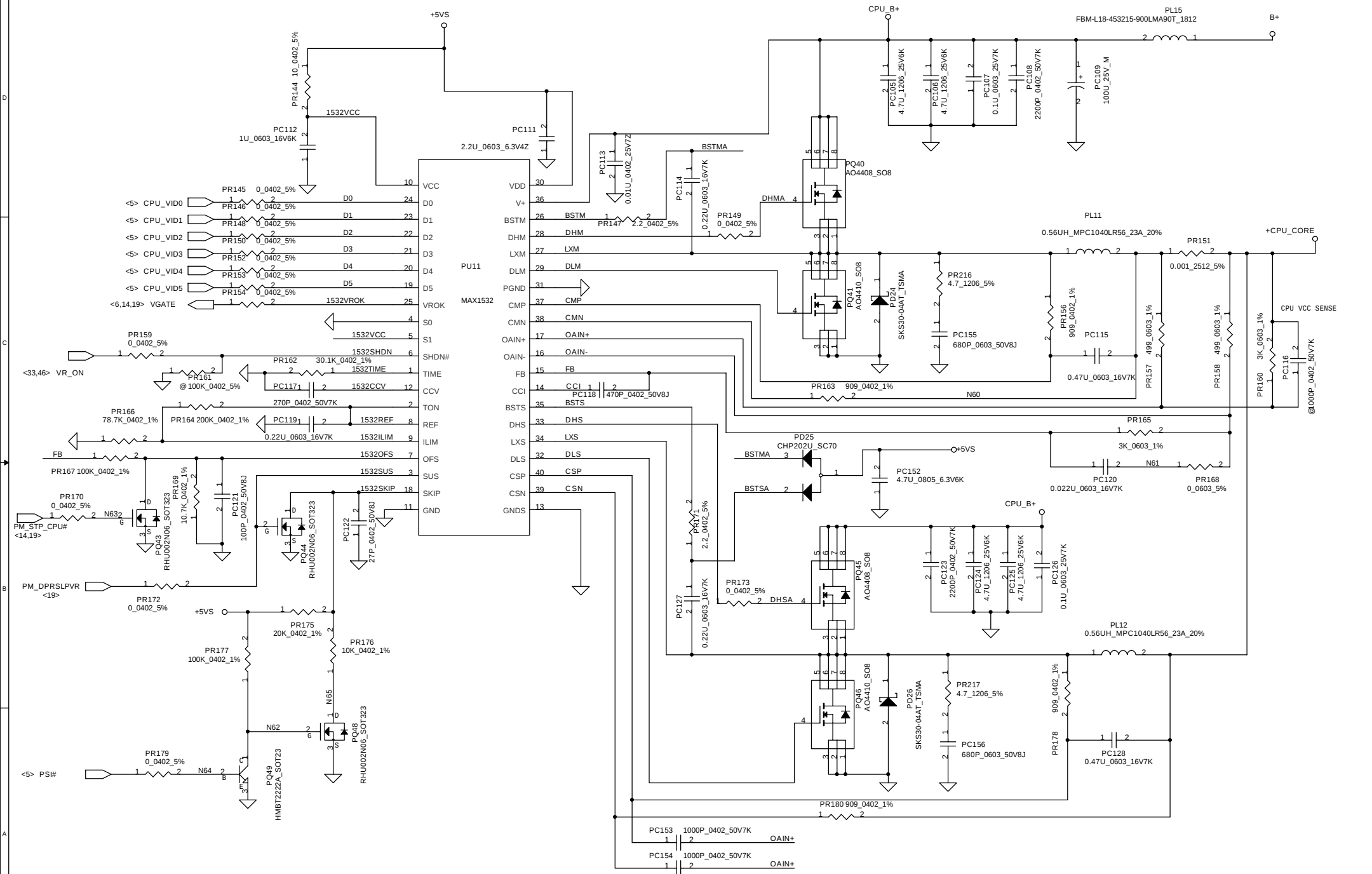
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+2.5VSP/+1.5VALWP



CPU CORE



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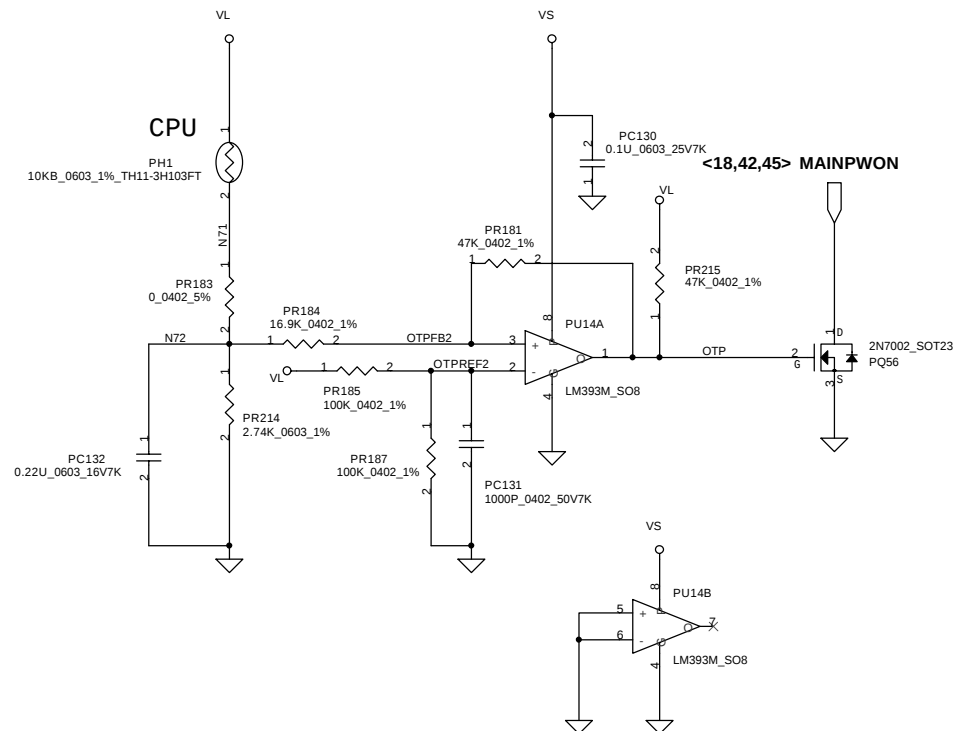
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PH1 under CPU botten side :
 CPU thermal protection at 90 $\pm$ 3 degree C
 Recovery at 50 $\pm$ 3 degree C



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Item	Reason for change	PG#	Modify List	Date	B.Ver#
1	Change DC JAcK and second battery connect.	42,44	Change DC JAcK from DC231105200 to DC231000500. Change second battery connect from	2004.10.28	
2	Modify OTP schematic.	45,49	Change PR114 from 47K_0402_5% to 806K_0603_1%; Change PR183 from 0_0402_5% to 1.37K_0402_1%; Change PR184 from 16.9K_0402_1% to 10K_0402_1%; Change PC132 from 0.22u_0603_16V to 1U_0603_16V; Change PC70 from 0.047uF to 0.47uF; Delete PR186, PR182, PU12 and PQ50.	2004.11.30	
3	To increase the pre-charge current.	42	Change PR21 from 169K_0603_1% to 200K_0603_1%; Change PR10 from 47_1206_5% to 33_1206_5%; Change PR9,PR11 and PR13 from 1.5K_1206_5% to 1K_1206_5%.	2004.12.28	
4	Change OTP schematic to EVT design.	49	Change PR183 from 1.37K_0402_1% to 0_0402_5%; Change PR184 from 10K_0402_1% to 16.9K_0402_1%; Change PC132 from 1U_0603_16V to 0.22u_0603_16V; Add PR215 47K_0402_1%; Add PR214 2.74K_0603_1%; Add PU14 LM393 and PQ56 2N7002.	2005.01.05	
5	For EMI request.	48	Add PR216 and PR217, 4.7_1206_5%; Add P155 and PC156, 680P_0603_50V; Add PL15, FBM-L18-453215-900LMA90T.	2005.01.10	
6	To increase 1.5V power plan to 1.57V by H/W request.	47	Delete PR201; Add PR200 10K_0402_1%; Add PR193 5.36K_0402_1%.	2005.01.10	

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EAT10 PIR List

***** Rev:0.2 PIR List 2004/08/10 Writer by Jason *****

P05 : Add @ in R63
Del @ in R56

P06 : Del @ in R54
Del JP9

P18: New add R512

P21 : New add R513
New add X3
New add C607

P21 : New add R534, R535

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