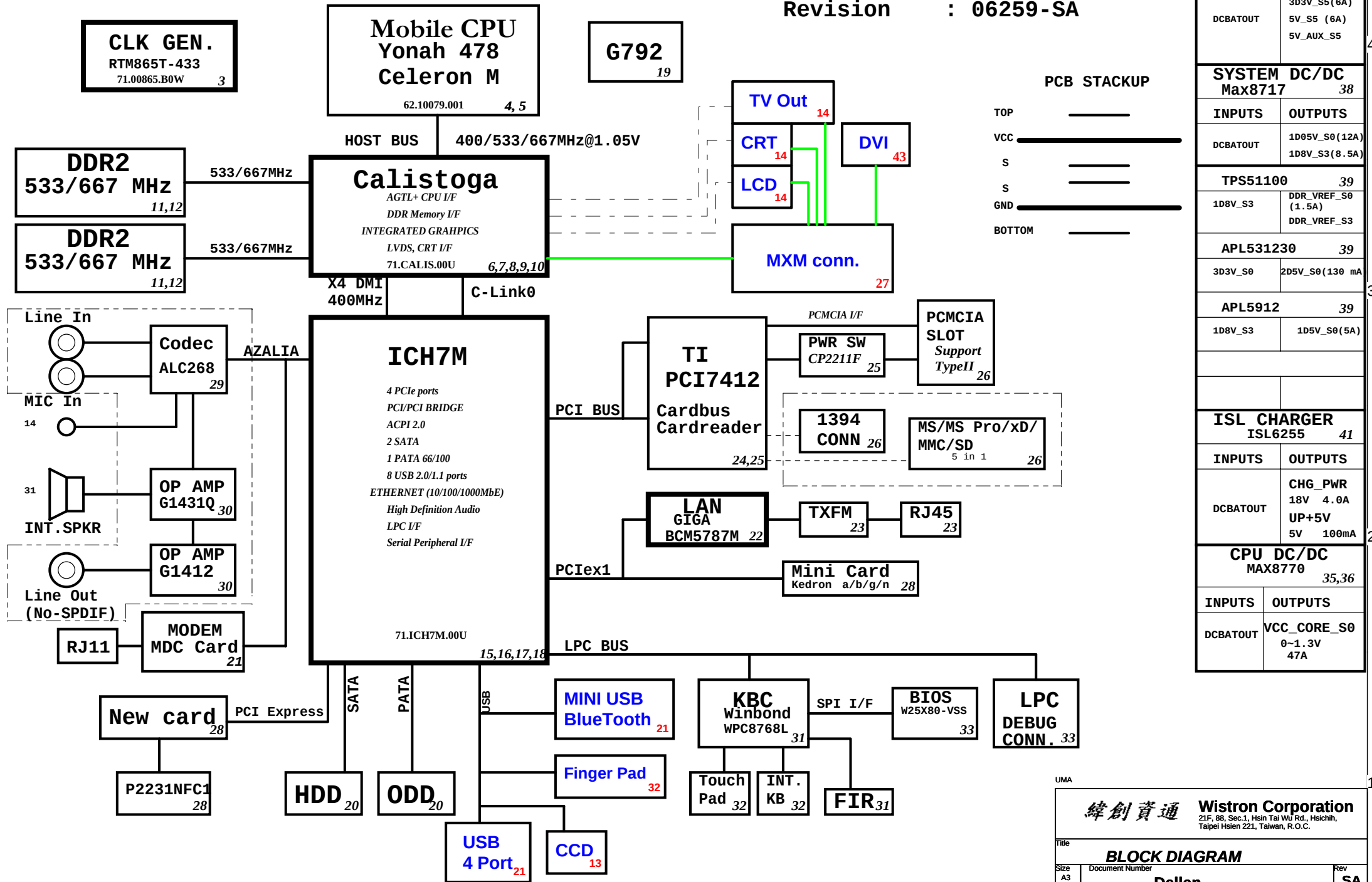


# Dellen Block Diagram

**Project code: 91.4V401.001**  
**PCB P/N : 48.4T307.0SA**  
**Revision : 06259-SA**



ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

|                                                                                                                                                                      |                                |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|
| EE_DIN,EE_DOUT, GNT[3:0], GPIO[25],<br>GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#,<br>LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0]<br><br>LDRQ[0], LDRQ[1]/GPIO[41],<br>PWRBTN#, TP[3] | ICH7 internal 20K pull-ups     |
| DD[7], DDREQ                                                                                                                                                         | ICH7 internal 11.5K pull-downs |
| ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0],<br>ACZ_SDOUT,ACZ_SYNC, DPRSLPVR/GPIO16,<br>EE_CS,SPI_ARB, SPI_CLK, SPKR,                                                       | ICH7 internal 20K pull-downs   |
| USB[7:0][P,N]                                                                                                                                                        | ICH7 internal 15K pull-downs   |
| SATALED#                                                                                                                                                             | ICH7 internal 15K pull-up      |
| LAN_CLK                                                                                                                                                              | ICH7 internal 100K pull-down   |

ICH7M IDE Integrated Series Termination Resistors

|                                                                                  |                      |
|----------------------------------------------------------------------------------|----------------------|
| DD[15:0], D10W#, DIOR#, DREQ,<br>DDACK#, IORDY, DA[2:0], DCS1#,<br>DCS3#, IDEIRQ | approximately 33 ohm |
|----------------------------------------------------------------------------------|----------------------|

ICH7M Functional Strap Definitions

page 16

| Signal                                 | Usage/When Sampled                                                    | Comment                                                                                                                                                                                                          |
|----------------------------------------|-----------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ACZ_SDOUT                              | XOR Chain Entrance/<br>PCIE Port Config bit1,<br>Rising Edge of PWROK | Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)                                                       |
| ACZ_SYNC                               | PCIE bit0,<br>Rising Edge of PWROK.                                   | Sets bit0 of RPC.PC(Config Registers:Offset 224h)                                                                                                                                                                |
| EE_CS                                  | Reserved                                                              | This signal should not be pull high.                                                                                                                                                                             |
| EE_DOUT                                | Reserved                                                              | This signal should not be pull low.                                                                                                                                                                              |
| GNT2#                                  | Reserved                                                              | This signal should not be pull low.                                                                                                                                                                              |
| GNT3#                                  | Top-Block<br>Swap Override.<br>Rising Edge of PWROK.                  | Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space).<br>Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down. |
| GNT5#/<br>GPIO17#,<br>GNT4#/<br>GPIO48 | Boot BIOS Destination<br>Selection.<br>Rising Edge of PWROK.          | Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10).<br>GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.                                                                                   |
| DPRSLPVR                               | Reserved                                                              | This signal should not be pull high.                                                                                                                                                                             |
| GPIO25                                 | Reserved.<br>Rising Edge of RSMRST#.                                  | This signal should not be pull low.                                                                                                                                                                              |
| INTVRMEN                               | Integrated VccSusi_05<br>VRM Enable/Disable.<br>Always sampled.       | Enables integrated VccSusi_05 VRM when sampled high                                                                                                                                                              |
| LINKALERT#                             | Reserved                                                              | Requires an external pull-up resistor.                                                                                                                                                                           |
| REQ[4:1]#                              | XOR Chain Selection.<br>Rising Edge of PWROK.                         | TBD, Chapter 8.                                                                                                                                                                                                  |
| SATALED#                               | Reserved                                                              | This signal should not be pull low.                                                                                                                                                                              |
| SPKR                                   | No Reboot.<br>Rising Edge of PWROK.                                   | If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.                                            |
| TP3                                    | XOR Chain Entrance.<br>Rising Edge of PWROK.                          | This signal should not be pull low unless using XOR Chain testing.                                                                                                                                               |

ICH8M Integrated Pull-up and Pull-down Resistors

ICH8-M EDS 21762 2.0V1

| SIGNAL              | Resistor Type/Value |
|---------------------|---------------------|
| HDA_BIT_CLK         | PULL-DOWN 20K       |
| HDA_RST#            | NONE                |
| HDA_SDIN[3:0]       | PULL-DOWN 20K       |
| HDA_SDOUT           | PULL-DOWN 20K       |
| HDA_SYNC            | PULL-DOWN 20K       |
| GNT[3:0]            | PULL-UP 20K         |
| GPIO[20]            | PULL-DOWN 20K       |
| LDA[3:0]#/FHW[3:0]# | PULL-UP 20K         |
| LAN_RXD[2:0]        | PULL-UP 10K         |
| LDRQ[0]             | PULL-UP 20K         |
| LDRQ[1]/GPIO23      | PULL-UP 20K         |
| PME#                | PULL-UP 20K         |
| PWRBTN#             | PULL-UP 20K         |
| SATALED#            | PULL-UP 15K         |
| SPI_CS1#            | PULL-UP 20K         |
| SPI_CLK             | PULL-UP 20K         |
| SPI_MOSI            | PULL-UP 20K         |
| SPI_MISO            | PULL-UP 20K         |
| TACH_[3:0]          | PULL-UP 20K         |
| SPKR                | PULL-DOWN 20K       |
| TP[3]               | PULL-UP 20K         |
| USB[9:0][P,N]       | PULL-DOWN 15K       |
| CL_RST#             | PULL-UP 13K         |

History

PCI Routing

page 17

|        | IDSEL | INT                                               | REQ | GNT |
|--------|-------|---------------------------------------------------|-----|-----|
| TI7412 | AD22  | G:CARDBUS<br>B:1394<br>F:Flash Media<br>G:SD Host | 0   | 0   |

PCIE Routing

|       |               |
|-------|---------------|
| LANE1 | LAN BCM5787M  |
| LANE2 | MiniCard WLAN |
| LANE3 | NewCard WLAN  |

USB Table

| USB ports definition |           |
|----------------------|-----------|
| Pair                 | Device    |
| 0                    | USB1      |
| 1                    | USB3      |
| 2                    | USB2      |
| 3                    | USB4      |
| 4                    | FingerPad |
| 5                    | BlueTooth |
| 6                    | CCD       |
| 7                    | NewCard   |

Calistoga Strapping Signals and Configuration

EDS 17050 0.71 page 7

| Pin Name      | Strap Description                      | Configuration                                                                                                                |
|---------------|----------------------------------------|------------------------------------------------------------------------------------------------------------------------------|
| CFG[2:0]      | FSB Frequency Select                   | 001 = FSB533<br>011 = FSB667<br>others = Reserved                                                                            |
| CFG[4:3]      | Reserved                               |                                                                                                                              |
| CFG5          | DMI x2 Select                          | 0 = DMI x2<br>1 = DMI x4 (Default)                                                                                           |
| CFG6          | Reserved                               |                                                                                                                              |
| CFG7          | CPU Strap                              | 0 = Reserved<br>1 =Mobile CPU(Default)                                                                                       |
| CFG8          | Reserved                               |                                                                                                                              |
| CFG9          | PCI Express Graphics<br>Lane Reversal  | 0 = Reverse Lanes,15->0,14->1 ect..<br>1= Normal operation(Default):Lane<br>Numbered in order                                |
| CFG[11:10]    | Reserved                               |                                                                                                                              |
| CFG[13:12]    | XOR/ALL Z test<br>straps               | 00 = Reserved<br>01 = XOR mode enabled<br>10 = All Z mode enabled<br>11 = Normal Operation<br>(Default)                      |
| CFG[15:14]    | Reserved                               | Reserved                                                                                                                     |
| CFG16         | FSB Dynamic ODT                        | 0 = Dynamic ODT Disabled<br>1 = Dynamic ODT Enabled (Default)                                                                |
| CFG17         | Global R-comp Disable<br>(All R-comps) | 0 = All R-comp Disable<br>1 = Normal Operation (Default)                                                                     |
| CFG18         | VCC Select                             | 0 = 1.05V (Default)<br>1 = 1.5V                                                                                              |
| CFG19         | DMI Lane Reversal                      | 0 = Normal operation (Default):lane<br>Numbered in order<br>1 =Reverse Lane,4->0,3->1 ect...                                 |
| CFG20         | SDVO/PCIE<br>Concurrent                | 0 = only SDVO or PCIE x1 is<br>operational (Default)<br>1 =SDVO and PCIE x1 are operating<br>simultaneously via the PEG port |
| SDVOCTRL_DATA | SDVO Present                           | 0 = No SDVO Card present<br>(Default)<br>1= SDVO Card present                                                                |

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

TitleReference

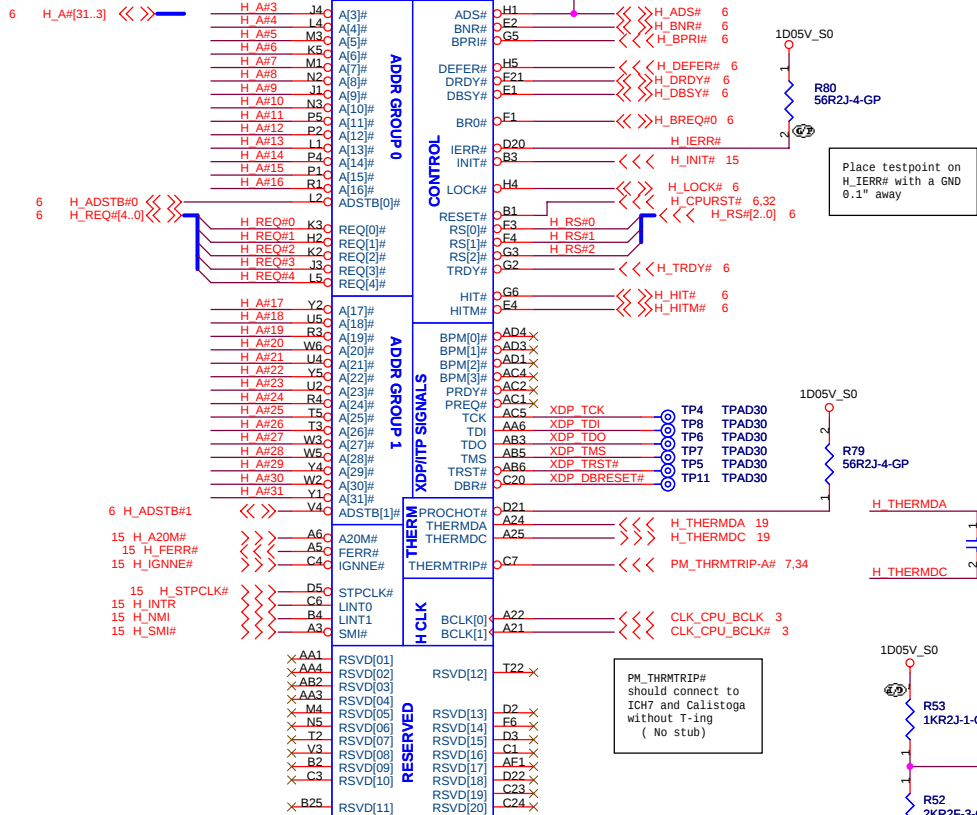
SizeA3Document NumberDellenRevSA

Date: Tuesday, January 16, 2007Sheet 2 of 43



2nd source: 62.10053.401

U41A  
BGA479-SKT6-GPU3  
62.10079.001

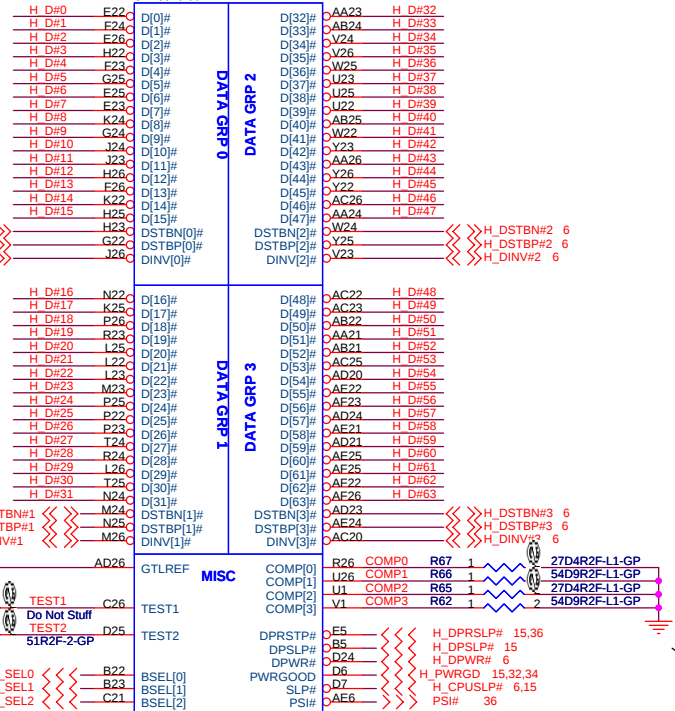


Place testpoint on  
H\_IERR# with a GND  
0.1" away

PM\_THRMTRIP#  
should connect to  
ICH7 and Calistoga  
without T-ing  
( No stub )

Layout Note:  
0.5" max length.

U41B  
BGA479-SKT6-GPU3  
62.10079.001

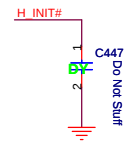
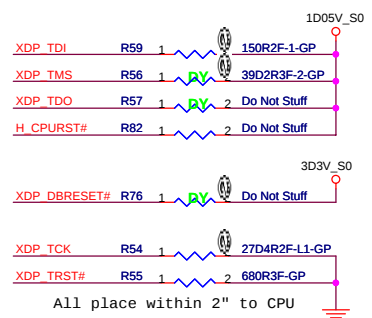


H\_DINV#[3..0] 6  
H\_DSTBN#[3..0] 6  
H\_DSTBP#[3..0] 6  
H\_D#[63..0] 6

H\_DSTBN#0  
H\_DSTBP#0  
H\_DINV#0

H\_DSTBN#1  
H\_DSTBP#1  
H\_DINV#1

Layout Note:  
Comp0, 2 connect with Zo=27.4 ohm, make  
trace length shorter than 0.5" .  
Comp1, 3 connect with Zo=55 ohm, make  
trace length shorter than 0.5" .



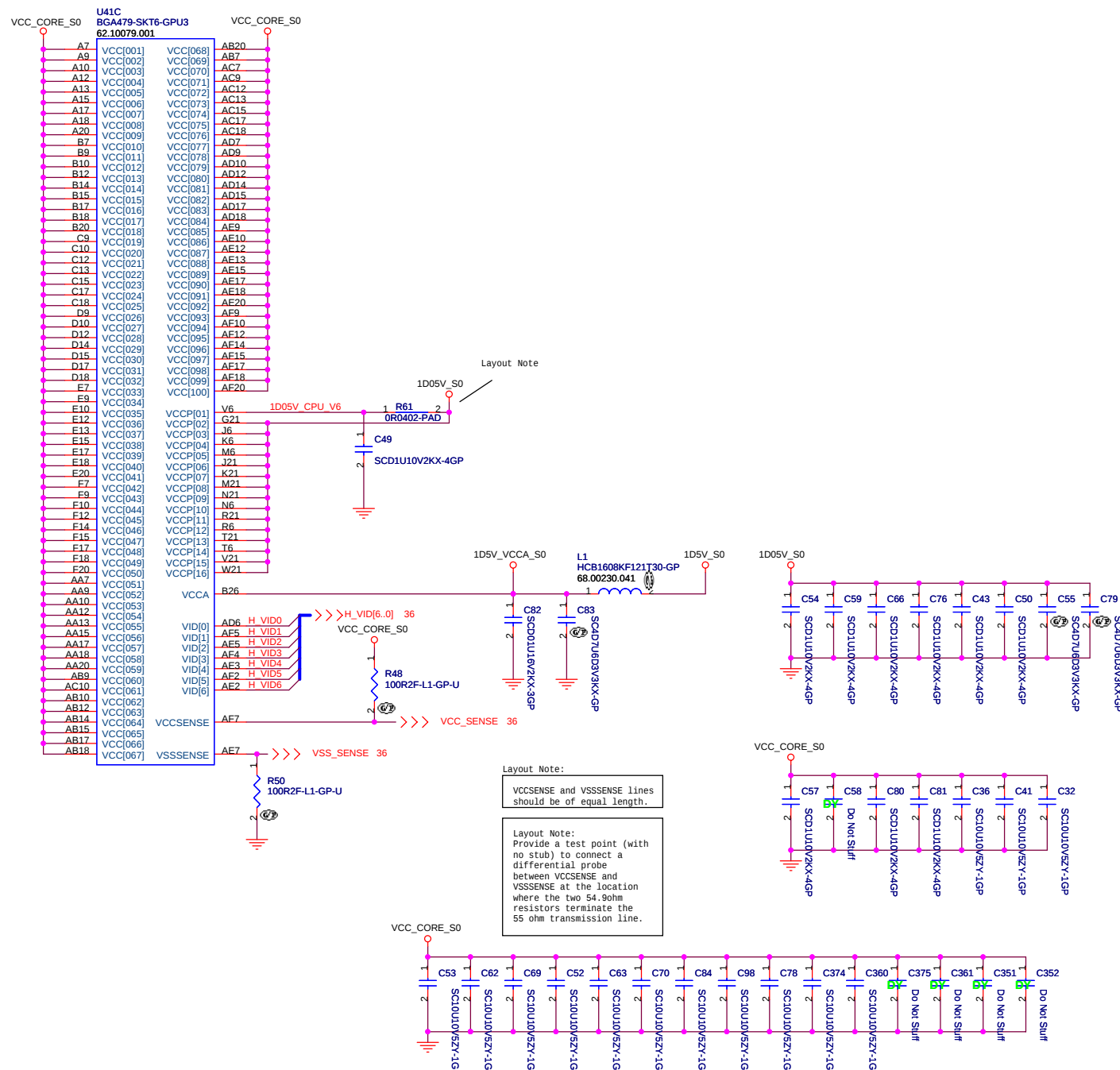
UMA

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

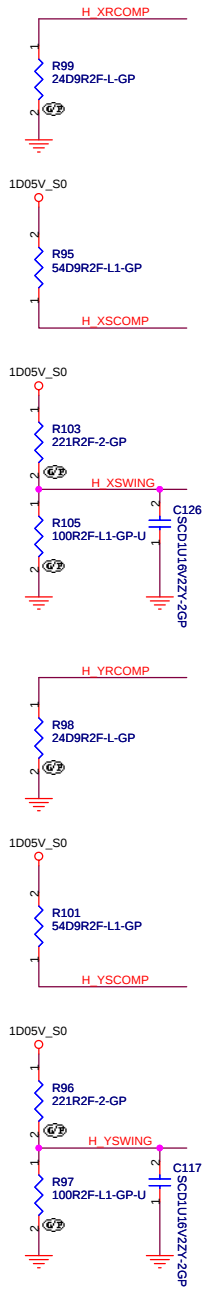
Title: **CPU (1 of 2)**

Size: A3 Document Number: Dellen Rev: SA

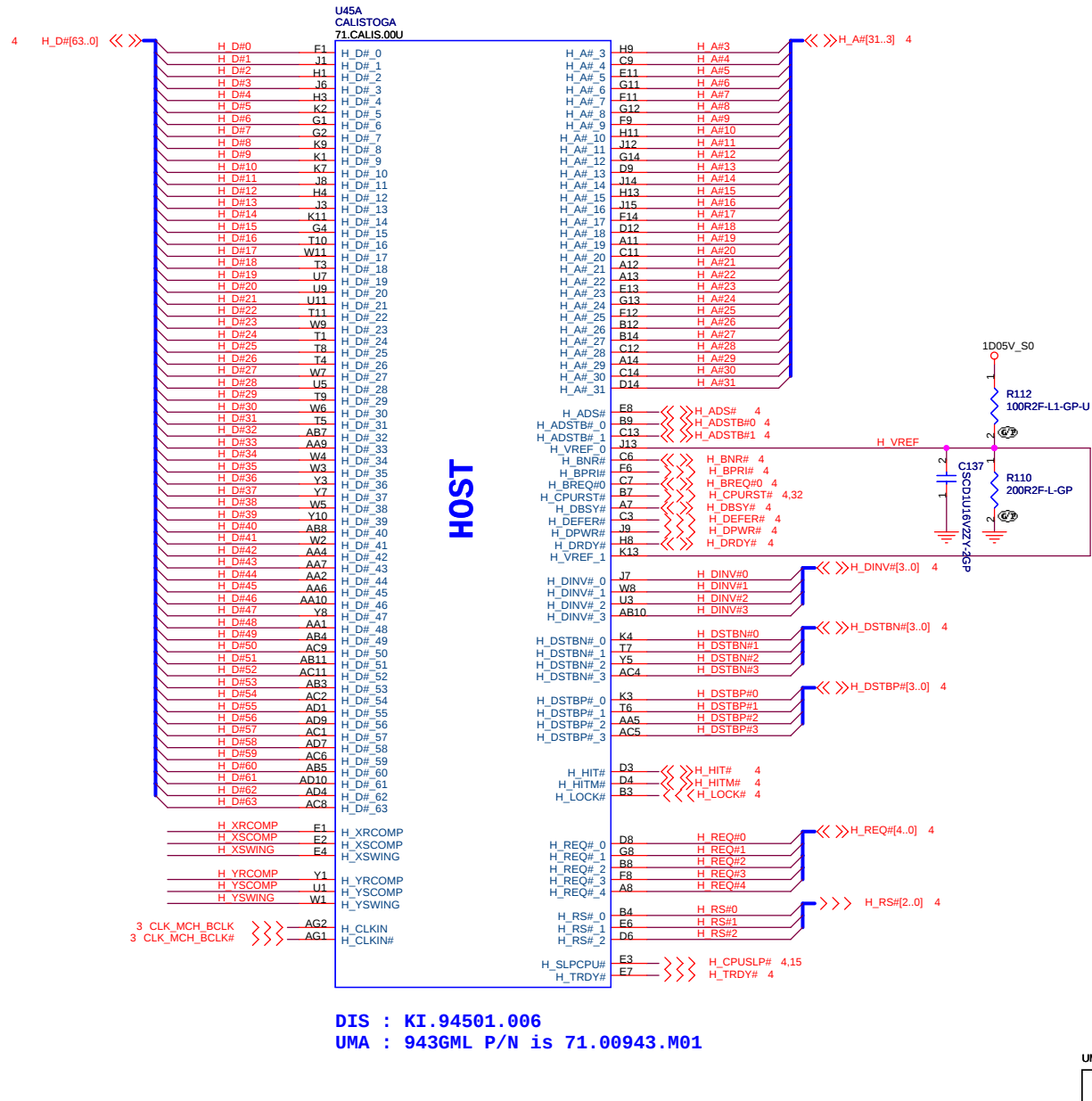
Date: Tuesday, January 16, 2007 Sheet: 4 of 43



| U1D1<br>BG4A7-SKT6-GP-U3<br>62.10079.001 |          |          |
|------------------------------------------|----------|----------|
| A4                                       | VSS[001] | VSS[082] |
| A8                                       | VSS[002] | VSS[083] |
| A11                                      | VSS[003] | VSS[084] |
| A14                                      | VSS[004] | VSS[085] |
| A16                                      | VSS[005] | VSS[086] |
| A23                                      | VSS[006] | VSS[087] |
| A26                                      | VSS[007] | VSS[088] |
| A26                                      | VSS[008] | VSS[089] |
| B6                                       | VSS[009] | VSS[090] |
| B8                                       | VSS[010] | VSS[091] |
| B11                                      | VSS[011] | VSS[092] |
| B13                                      | VSS[012] | VSS[093] |
| B16                                      | VSS[013] | VSS[094] |
| B19                                      | VSS[014] | VSS[095] |
| B21                                      | VSS[015] | VSS[096] |
| B24                                      | VSS[016] | VSS[097] |
| C5                                       | VSS[017] | VSS[098] |
| C8                                       | VSS[018] | VSS[099] |
| C11                                      | VSS[020] | VSS[101] |
| C16                                      | VSS[021] | VSS[102] |
| C19                                      | VSS[022] | VSS[103] |
| C22                                      | VSS[023] | VSS[104] |
| C25                                      | VSS[024] | VSS[105] |
| D1                                       | VSS[025] | VSS[106] |
| D4                                       | VSS[026] | VSS[107] |
| D8                                       | VSS[027] | VSS[108] |
| D8                                       | VSS[028] | VSS[109] |
| D13                                      | VSS[029] | VSS[110] |
| D16                                      | VSS[030] | VSS[111] |
| D19                                      | VSS[031] | VSS[112] |
| D19                                      | VSS[032] | VSS[113] |
| D23                                      | VSS[033] | VSS[114] |
| D26                                      | VSS[034] | VSS[115] |
| E3                                       | VSS[035] | VSS[116] |
| E8                                       | VSS[036] | VSS[117] |
| E8                                       | VSS[037] | VSS[118] |
| E11                                      | VSS[038] | VSS[119] |
| E11                                      | VSS[039] | VSS[120] |
| F16                                      | VSS[040] | VSS[121] |
| F19                                      | VSS[041] | VSS[122] |
| F21                                      | VSS[042] | VSS[123] |
| F24                                      | VSS[043] | VSS[124] |
| F8                                       | VSS[044] | VSS[125] |
| F11                                      | VSS[045] | VSS[126] |
| F13                                      | VSS[046] | VSS[127] |
| F16                                      | VSS[047] | VSS[128] |
| F19                                      | VSS[048] | VSS[129] |
| F22                                      | VSS[049] | VSS[130] |
| F22                                      | VSS[050] | VSS[131] |
| F25                                      | VSS[051] | VSS[132] |
| G4                                       | VSS[052] | VSS[133] |
| G5                                       | VSS[053] | VSS[134] |
| G1                                       | VSS[054] | VSS[135] |
| G23                                      | VSS[055] | VSS[136] |
| H3                                       | VSS[056] | VSS[137] |
| H6                                       | VSS[057] | VSS[138] |
| H21                                      | VSS[058] | VSS[139] |
| H24                                      | VSS[059] | VSS[140] |
| H24                                      | VSS[060] | VSS[141] |
| J2                                       | VSS[061] | VSS[142] |
| J25                                      | VSS[062] | VSS[143] |
| J25                                      | VSS[063] | VSS[144] |
| K1                                       | VSS[064] | VSS[145] |
| K4                                       | VSS[065] | VSS[146] |
| K4                                       | VSS[066] | VSS[147] |
| K23                                      | VSS[067] | VSS[148] |
| K26                                      | VSS[068] | VSS[149] |
| L1                                       | VSS[069] | VSS[150] |
| L21                                      | VSS[070] | VSS[151] |
| L24                                      | VSS[071] | VSS[152] |
| M2                                       | VSS[072] | VSS[153] |
| M2                                       | VSS[073] | VSS[154] |
| M5                                       | VSS[074] | VSS[155] |
| M22                                      | VSS[075] | VSS[156] |
| M25                                      | VSS[076] | VSS[157] |
| N1                                       | VSS[077] | VSS[158] |
| N4                                       | VSS[078] | VSS[159] |
| N23                                      | VSS[079] | VSS[160] |
| N26                                      | VSS[080] | VSS[161] |
| P3                                       | VSS[081] | VSS[162] |

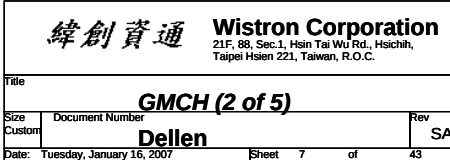


Place them near to the chip (< 0.5")



DIS : KI.94501.006  
UMA : 943GML P/N is 71.00943.M01

UMA



11 M\_A\_DQ[63.0] << >>

|          |      |         |
|----------|------|---------|
| M A DQ0  | AJ35 | SA DQ0  |
| M A DQ1  | AJ34 | SA DQ1  |
| M A DQ2  | AM31 | SA DQ2  |
| M A DQ3  | AM33 | SA DQ3  |
| M A DQ4  | AJ36 | SA DQ4  |
| M A DQ5  | AK35 | SA DQ5  |
| M A DQ6  | AJ32 | SA DQ6  |
| M A DQ7  | AH31 | SA DQ7  |
| M A DQ8  | AN35 | SA DQ8  |
| M A DQ9  | AP33 | SA DQ9  |
| M A DQ10 | AR31 | SA DQ10 |
| M A DQ11 | AP31 | SA DQ11 |
| M A DQ12 | AN38 | SA DQ12 |
| M A DQ13 | AM36 | SA DQ13 |
| M A DQ14 | AM34 | SA DQ14 |
| M A DQ15 | AN33 | SA DQ15 |
| M A DQ16 | AK26 | SA DQ16 |
| M A DQ17 | AL27 | SA DQ17 |
| M A DQ18 | AM26 | SA DQ18 |
| M A DQ19 | AN24 | SA DQ19 |
| M A DQ20 | AK23 | SA DQ20 |
| M A DQ21 | AL28 | SA DQ21 |
| M A DQ22 | AM24 | SA DQ22 |
| M A DQ23 | AP26 | SA DQ23 |
| M A DQ24 | AP23 | SA DQ24 |
| M A DQ25 | AL22 | SA DQ25 |
| M A DQ26 | AP21 | SA DQ26 |
| M A DQ27 | AN20 | SA DQ27 |
| M A DQ28 | AL23 | SA DQ28 |
| M A DQ29 | AP24 | SA DQ29 |
| M A DQ30 | AP20 | SA DQ30 |
| M A DQ31 | AT21 | SA DQ31 |
| M A DQ32 | AR12 | SA DQ32 |
| M A DQ33 | AR14 | SA DQ33 |
| M A DQ34 | AP13 | SA DQ34 |
| M A DQ35 | AP12 | SA DQ35 |
| M A DQ36 | AT13 | SA DQ36 |
| M A DQ37 | AT12 | SA DQ37 |
| M A DQ38 | AL14 | SA DQ38 |
| M A DQ39 | AL12 | SA DQ39 |
| M A DQ40 | AK9  | SA DQ40 |
| M A DQ41 | AN7  | SA DQ41 |
| M A DQ42 | AK8  | SA DQ42 |
| M A DQ43 | AK7  | SA DQ43 |
| M A DQ44 | AP9  | SA DQ44 |
| M A DQ45 | AT5  | SA DQ45 |
| M A DQ46 | AL5  | SA DQ46 |
| M A DQ47 | AY2  | SA DQ47 |
| M A DQ48 | AY2  | SA DQ48 |
| M A DQ49 | AW2  | SA DQ49 |
| M A DQ50 | AP1  | SA DQ50 |
| M A DQ51 | AN2  | SA DQ51 |
| M A DQ52 | AV2  | SA DQ52 |
| M A DQ53 | AT3  | SA DQ53 |
| M A DQ54 | AN1  | SA DQ54 |
| M A DQ55 | AL2  | SA DQ55 |
| M A DQ56 | AG7  | SA DQ56 |
| M A DQ57 | AF9  | SA DQ57 |
| M A DQ58 | AG4  | SA DQ58 |
| M A DQ59 | AF6  | SA DQ59 |
| M A DQ60 | AG9  | SA DQ60 |
| M A DQ61 | AH6  | SA DQ61 |
| M A DQ62 | AF4  | SA DQ62 |
| M A DQ63 | AF8  | SA DQ63 |

U45D  
CALISTOGA  
71.CALIS.00U

DDR SYSTEM MEMORY A

|              |      |                |
|--------------|------|----------------|
| SA_BS_0      | AU12 | M A BS#0 11.12 |
| SA_BS_1      | AV14 | M A BS#1 11.12 |
| SA_BS_2      | BA20 | M A BS#2 11.12 |
| SA_BS_2      |      | M A CAS# 11.12 |
| SA_BS_2      |      | M A_DM[7.0] 11 |
| SA_CAS#      | AY13 |                |
| SA_DM_0      | AJ33 | M A DM0        |
| SA_DM_1      | AM35 | M A DM1        |
| SA_DM_2      | AL26 | M A DM2        |
| SA_DM_3      | AN22 | M A DM3        |
| SA_DM_4      | AM14 | M A DM4        |
| SA_DM_5      | AL9  | M A DM5        |
| SA_DM_6      | AR3  | M A DM6        |
| SA_DM_7      | AH4  | M A DM7        |
| SA_DQS_0     | AK33 | M A DQS0       |
| SA_DQS_1     | AT33 | M A DQS1       |
| SA_DQS_2     | AN28 | M A DQS2       |
| SA_DQS_3     | AM22 | M A DQS3       |
| SA_DQS_4     | AN12 | M A DQS4       |
| SA_DQS_5     | AN8  | M A DQS5       |
| SA_DQS_6     | AP3  | M A DQS6       |
| SA_DQS_7     | AG5  | M A DQS7       |
| SA_DQS#_0    | AK32 | M A DQS#0      |
| SA_DQS#_1    | AU33 | M A DQS#1      |
| SA_DQS#_2    | AN27 | M A DQS#2      |
| SA_DQS#_3    | AM21 | M A DQS#3      |
| SA_DQS#_4    | AM12 | M A DQS#4      |
| SA_DQS#_5    | AL8  | M A DQS#5      |
| SA_DQS#_6    | AN3  | M A DQS#6      |
| SA_DQS#_7    | AH5  | M A DQS#7      |
| SA_MA_0      | AY16 | M A A0         |
| SA_MA_1      | AU14 | M A A1         |
| SA_MA_2      | AW16 | M A A2         |
| SA_MA_3      | BA16 | M A A3         |
| SA_MA_4      | BA17 | M A A4         |
| SA_MA_5      | AU16 | M A A5         |
| SA_MA_6      | AV17 | M A A6         |
| SA_MA_7      | AU17 | M A A7         |
| SA_MA_8      | AT16 | M A A8         |
| SA_MA_9      | AU13 | M A A9         |
| SA_MA_10     | AT17 | M A A10        |
| SA_MA_11     | AV20 | M A A11        |
| SA_MA_12     | AV12 | M A A12        |
| SA_MA_13     | AV12 | M A A13        |
| SA_RAS#      | AW14 | M A_RAS# 11.12 |
| SA_RCVENIN#  | AK23 | SA RCVENIN#    |
| SA_RCVENOUT# | AK24 | SA RCVENOUT#   |
| SA_WE#       | AY14 | M A_WE# 11.12  |

Place Test PAD Near to Chip  
as could as possible

11 M\_B\_DQ[63.0] << >>

|          |      |         |
|----------|------|---------|
| M B DQ0  | AK39 | SB DQ0  |
| M B DQ1  | AJ37 | SB DQ1  |
| M B DQ2  | AP39 | SB DQ2  |
| M B DQ3  | AR41 | SB DQ3  |
| M B DQ4  | AJ38 | SB DQ4  |
| M B DQ5  | AK38 | SB DQ5  |
| M B DQ6  | AN41 | SB DQ6  |
| M B DQ7  | AP41 | SB DQ7  |
| M B DQ8  | AT40 | SB DQ8  |
| M B DQ9  | AV41 | SB DQ9  |
| M B DQ10 | AU38 | SB DQ10 |
| M B DQ11 | AV38 | SB DQ11 |
| M B DQ12 | AP38 | SB DQ12 |
| M B DQ13 | AR40 | SB DQ13 |
| M B DQ14 | AW38 | SB DQ14 |
| M B DQ15 | AV38 | SB DQ15 |
| M B DQ16 | BA38 | SB DQ16 |
| M B DQ17 | AV36 | SB DQ17 |
| M B DQ18 | AR36 | SB DQ18 |
| M B DQ19 | AP36 | SB DQ19 |
| M B DQ20 | BA36 | SB DQ20 |
| M B DQ21 | AU36 | SB DQ21 |
| M B DQ22 | AP34 | SB DQ22 |
| M B DQ23 | AP34 | SB DQ23 |
| M B DQ24 | AY33 | SB DQ24 |
| M B DQ25 | BA33 | SB DQ25 |
| M B DQ26 | AT31 | SB DQ26 |
| M B DQ27 | AU29 | SB DQ27 |
| M B DQ28 | AU31 | SB DQ28 |
| M B DQ29 | AW31 | SB DQ29 |
| M B DQ30 | AV29 | SB DQ30 |
| M B DQ31 | AW29 | SB DQ31 |
| M B DQ32 | AM19 | SB DQ32 |
| M B DQ33 | AL19 | SB DQ33 |
| M B DQ34 | AP14 | SB DQ34 |
| M B DQ35 | AN14 | SB DQ35 |
| M B DQ36 | AN17 | SB DQ36 |
| M B DQ37 | AM16 | SB DQ37 |
| M B DQ38 | AP15 | SB DQ38 |
| M B DQ39 | AL15 | SB DQ39 |
| M B DQ40 | AJ11 | SB DQ40 |
| M B DQ41 | AH10 | SB DQ41 |
| M B DQ42 | AJ9  | SB DQ42 |
| M B DQ43 | AN10 | SB DQ43 |
| M B DQ44 | AK13 | SB DQ44 |
| M B DQ45 | AH11 | SB DQ45 |
| M B DQ46 | AK10 | SB DQ46 |
| M B DQ47 | AJ8  | SB DQ47 |
| M B DQ48 | BA10 | SB DQ48 |
| M B DQ49 | AW10 | SB DQ49 |
| M B DQ50 | BA4  | SB DQ50 |
| M B DQ51 | AW4  | SB DQ51 |
| M B DQ52 | AY10 | SB DQ52 |
| M B DQ53 | AY9  | SB DQ53 |
| M B DQ54 | AY5  | SB DQ54 |
| M B DQ55 | AV4  | SB DQ55 |
| M B DQ56 | AR5  | SB DQ56 |
| M B DQ57 | AK4  | SB DQ57 |
| M B DQ58 | AK3  | SB DQ58 |
| M B DQ59 | AT4  | SB DQ59 |
| M B DQ60 | AK5  | SB DQ60 |
| M B DQ61 | AJ5  | SB DQ61 |
| M B DQ62 | AJ3  | SB DQ62 |
| M B DQ63 | AJ3  | SB DQ63 |

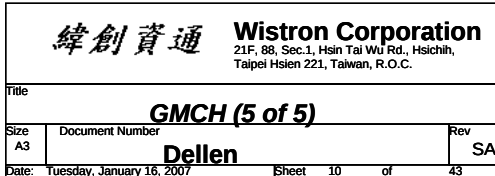
U45E  
CALISTOGA  
71.CALIS.00U

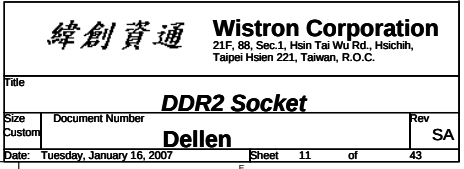
DDR SYSTEM MEMORY B

|              |      |                |
|--------------|------|----------------|
| SB_BS_0      | AT24 | M B BS#0 11.12 |
| SB_BS_1      | AV23 | M B BS#1 11.12 |
| SB_BS_2      | AY28 | M B BS#2 11.12 |
| SB_BS_2      |      | M B CAS# 11.12 |
| SB_BS_2      |      | M B_DM[7.0] 11 |
| SB_CAS#      | AR24 |                |
| SB_DM_0      | AK36 | M B DM0        |
| SB_DM_1      | AR38 | M B DM1        |
| SB_DM_2      | AT36 | M B DM2        |
| SB_DM_3      | BA31 | M B DM3        |
| SB_DM_4      | AL17 | M B DM4        |
| SB_DM_5      | AH8  | M B DM5        |
| SB_DM_6      | BA5  | M B DM6        |
| SB_DM_7      | AN4  | M B DM7        |
| SB_DQS_0     | AM39 | M B DQS0       |
| SB_DQS_1     | AT39 | M B DQS1       |
| SB_DQS_2     | AU35 | M B DQS2       |
| SB_DQS_3     | AR29 | M B DQS3       |
| SB_DQS_4     | AR16 | M B DQS4       |
| SB_DQS_5     | AR10 | M B DQS5       |
| SB_DQS_6     | AR7  | M B DQS6       |
| SB_DQS_7     | AN5  | M B DQS7       |
| SB_DQS#_0    | AM40 | M B DQS#0      |
| SB_DQS#_1    | AU39 | M B DQS#1      |
| SB_DQS#_2    | AT35 | M B DQS#2      |
| SB_DQS#_3    | AP29 | M B DQS#3      |
| SB_DQS#_4    | AP16 | M B DQS#4      |
| SB_DQS#_5    | AT10 | M B DQS#5      |
| SB_DQS#_6    | AT7  | M B DQS#6      |
| SB_DQS#_7    | AP5  | M B DQS#7      |
| SB_MA_0      | AY23 | M B A0         |
| SB_MA_1      | AW24 | M B A1         |
| SB_MA_2      | AY24 | M B A2         |
| SB_MA_3      | AR28 | M B A3         |
| SB_MA_4      | AT27 | M B A4         |
| SB_MA_5      | AT28 | M B A5         |
| SB_MA_6      | AU27 | M B A6         |
| SB_MA_7      | AV28 | M B A7         |
| SB_MA_8      | AV27 | M B A8         |
| SB_MA_9      | AW27 | M B A9         |
| SB_MA_10     | AV24 | M B A10        |
| SB_MA_11     | BA27 | M B A11        |
| SB_MA_12     | AY27 | M B A12        |
| SB_MA_13     | AR23 | M B A13        |
| SB_RAS#      | AU23 | M_B_RAS# 11.12 |
| SB_RCVENIN#  | AK18 | SB RCVENIN#    |
| SB_RCVENOUT# | AK18 | SB RCVENOUT#   |
| SB_WE#       | AR27 | M_B_WE# 11.12  |

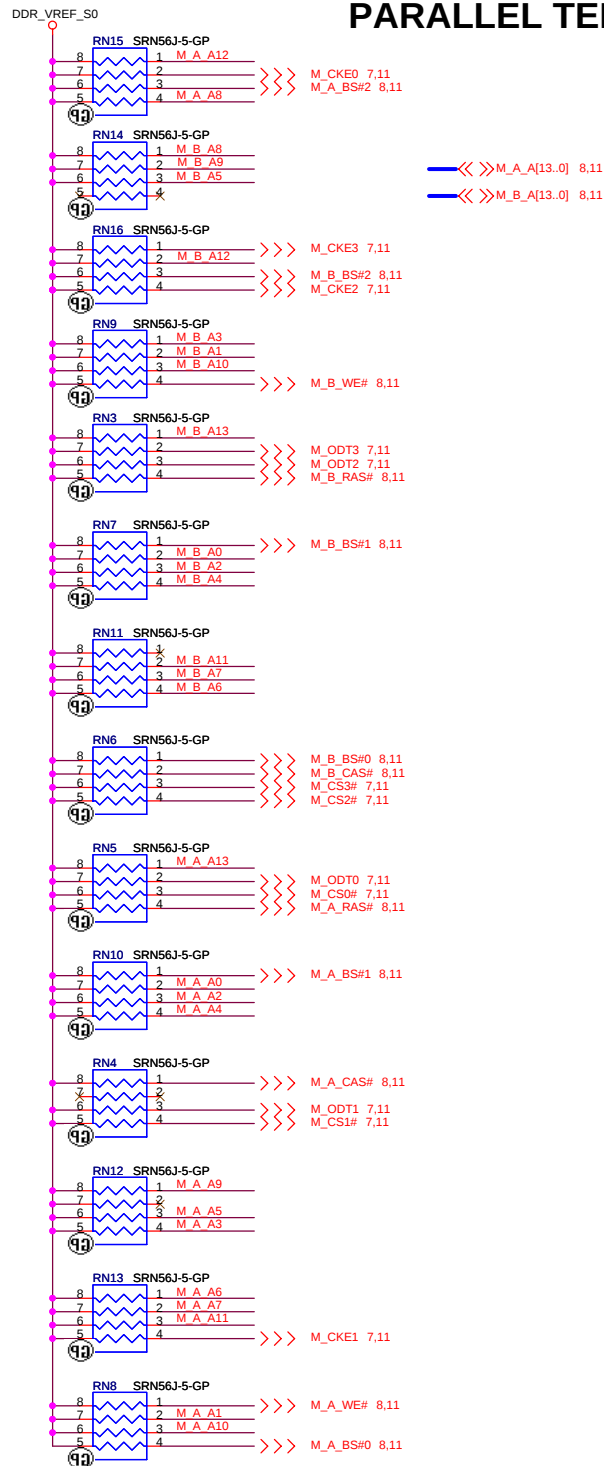
Place Test PAD Near to Chip  
as could as possible



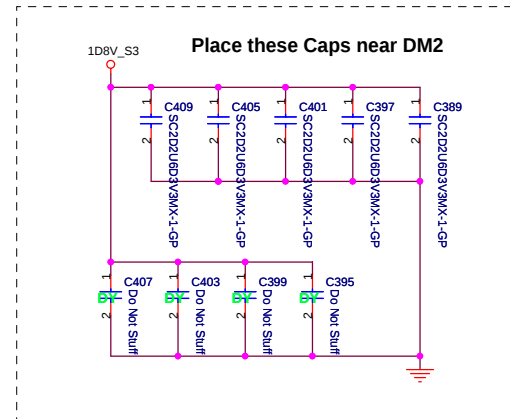
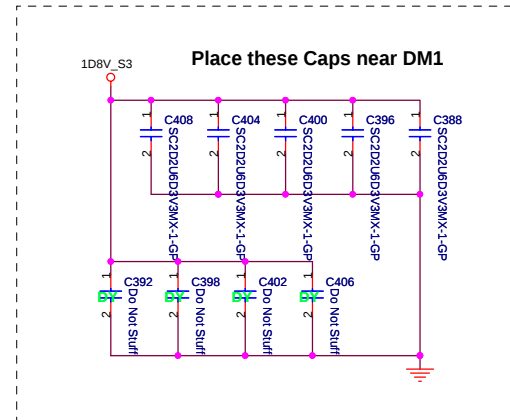
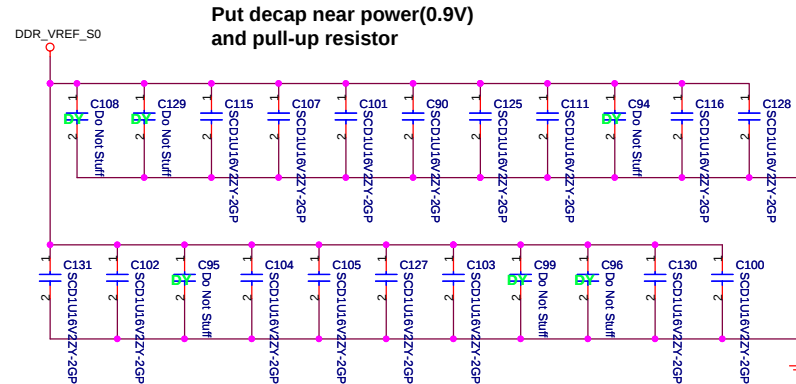


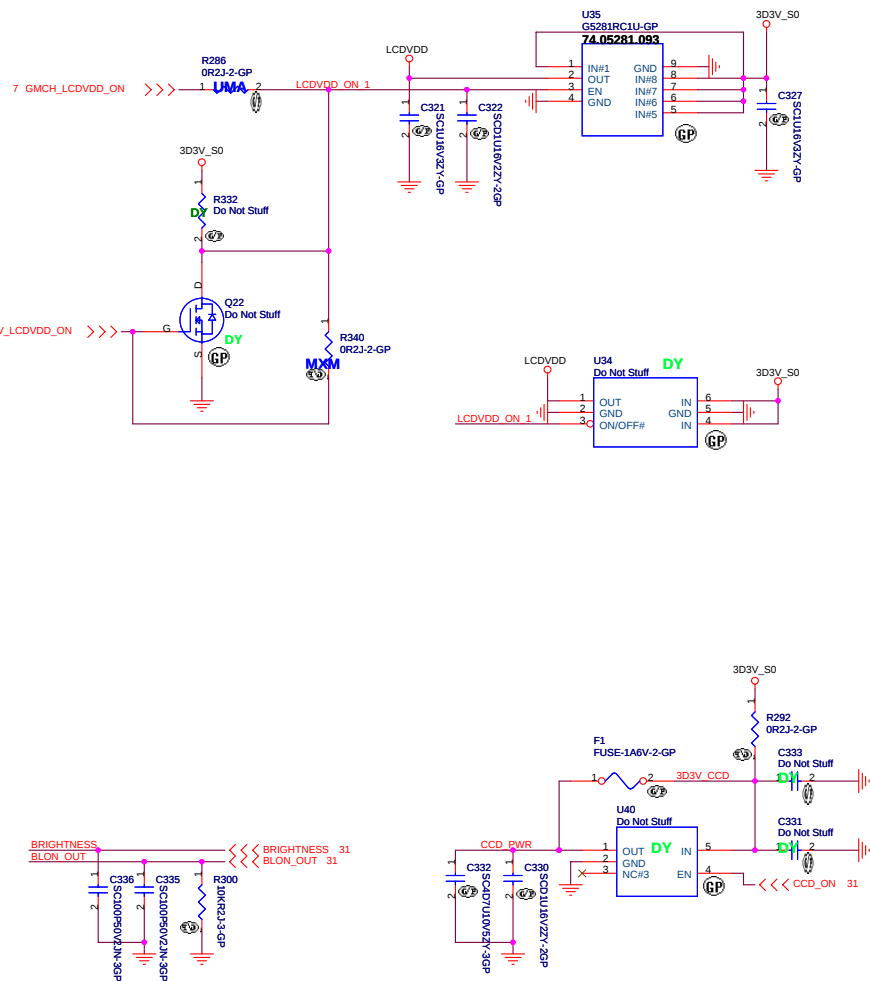


# PARALLEL TERMINATION

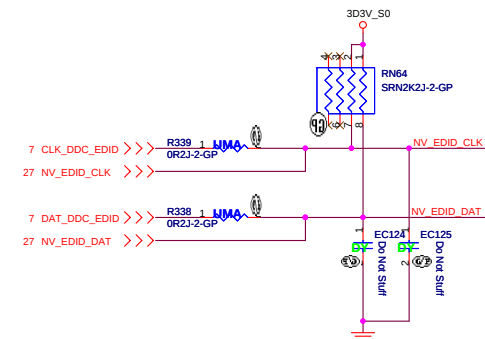
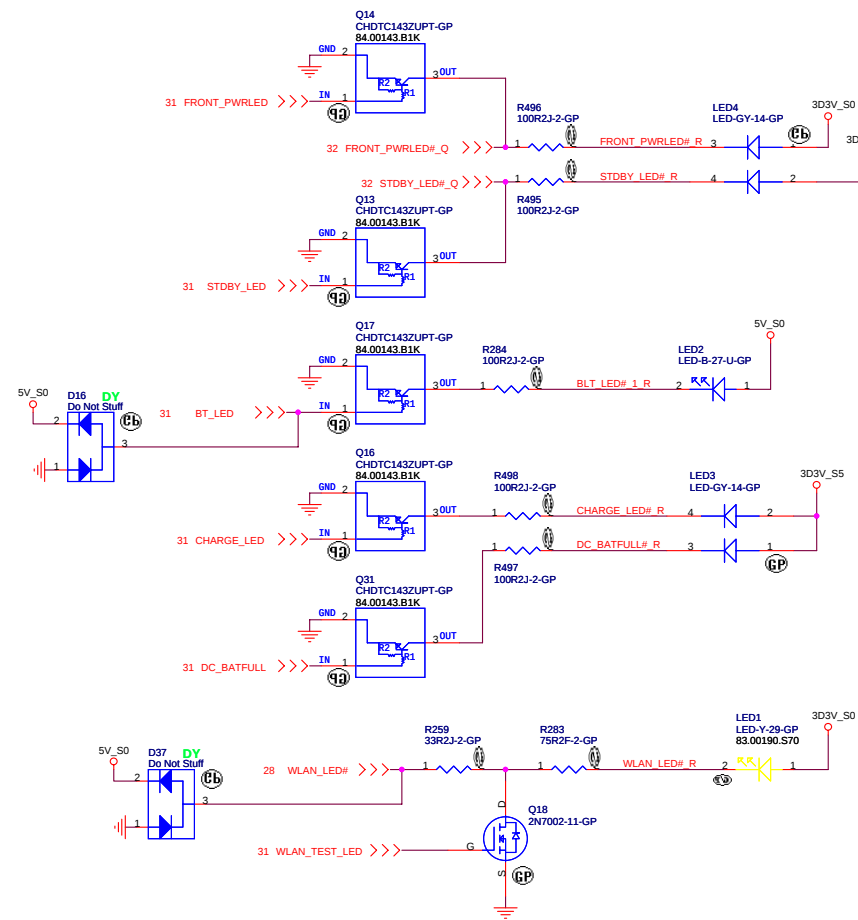
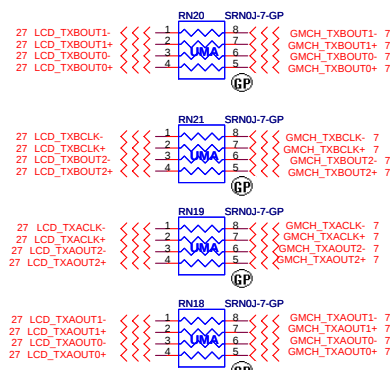
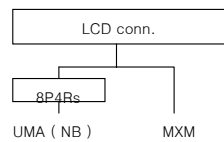
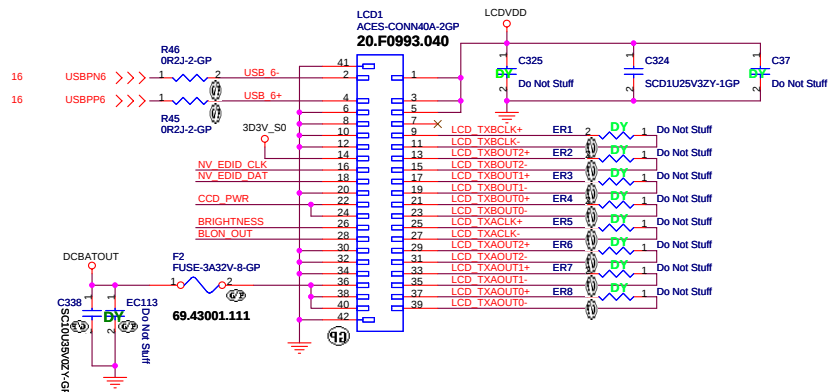


# Decoupling Capacitor





## LCD / Inverter conn.

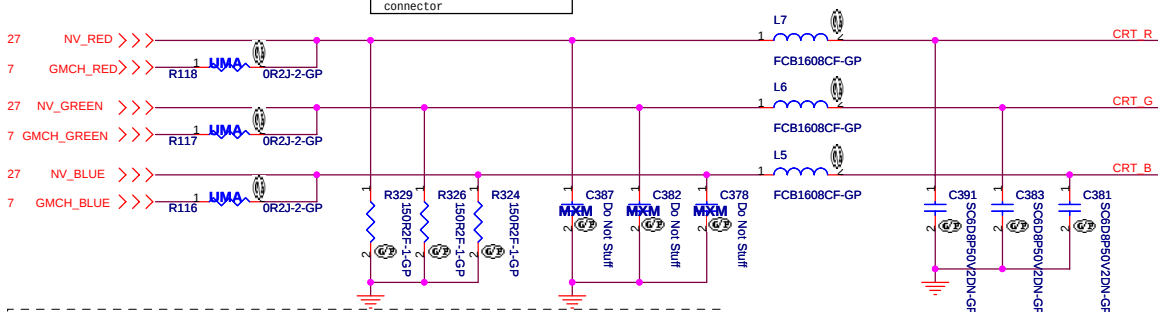


|                                                                                                               |                                  |                  |  |
|---------------------------------------------------------------------------------------------------------------|----------------------------------|------------------|--|
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| <b>Title</b><br>LCD CONN & LED                                                                                |                                  |                  |  |
| <b>Size</b><br>Custom                                                                                         | <b>Document Number</b><br>Dellen | <b>Rev</b><br>SA |  |
| <b>Date</b><br>Tuesday, January 16, 2007                                                                      | <b>Sheet</b><br>13               | <b>of</b><br>43  |  |

Layout Note:  
Place these resistors  
close to the CRT-out  
connector

Ferrite bead impedance: 10 ohm@100MHz

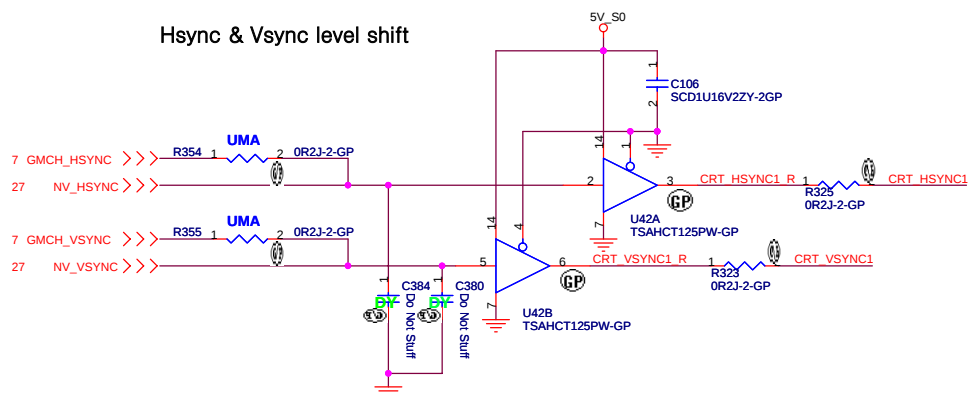
## CRT I/F & connector



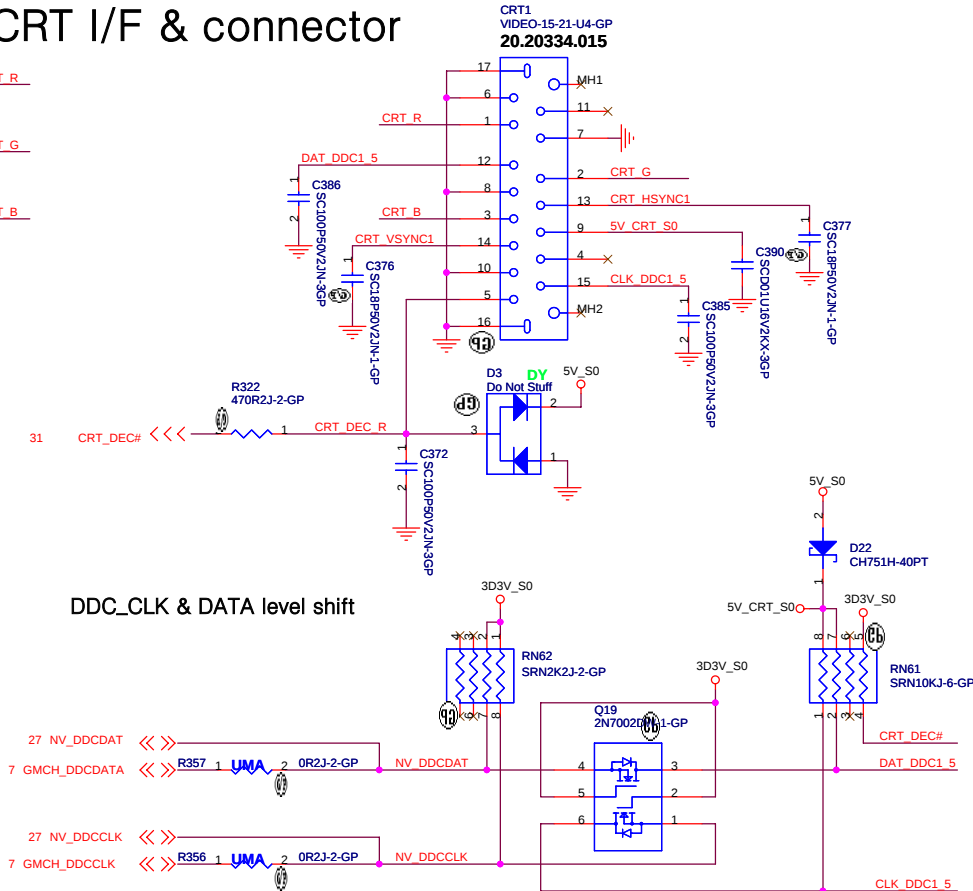
### Layout Note:

\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

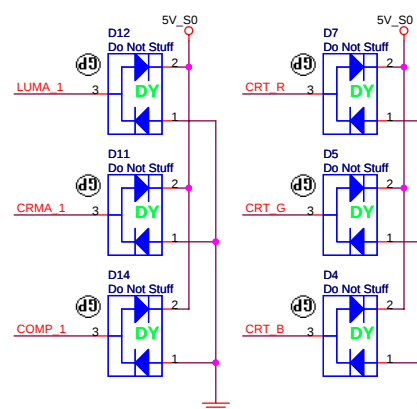
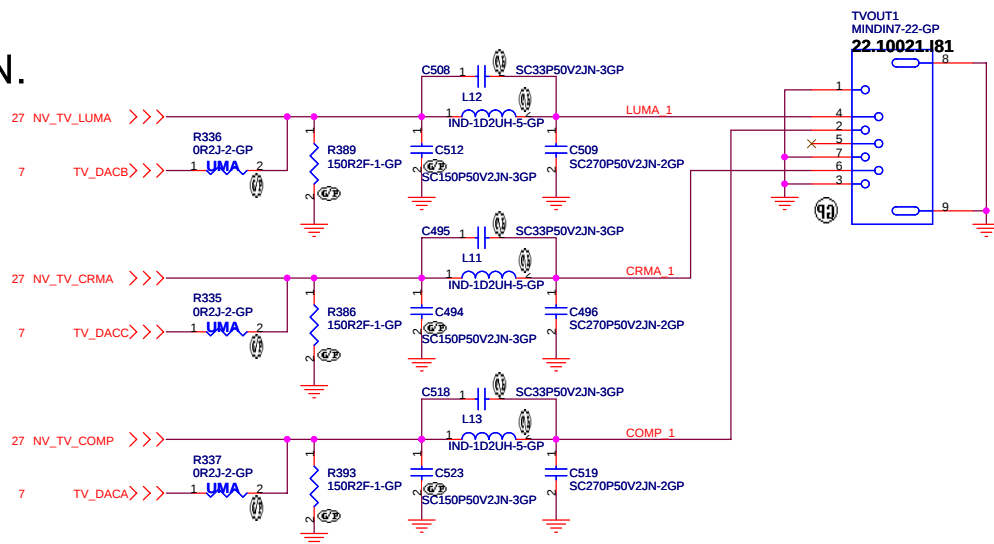
### Hsync & Vsync level shift



### DDC\_CLK & DATA level shift



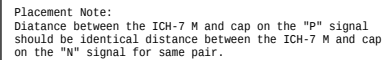
## TV CONN.



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|       |                           |        |                  |       |
|-------|---------------------------|--------|------------------|-------|
| Title |                           |        | CRT/TV Connector |       |
| Size  | Document Number           | Rev    |                  | SA    |
| A3    |                           | Dellen |                  |       |
| Date: | Tuesday, January 16, 2007 | Sheet  | 14               | of 43 |

RTC1  
BAT-CON2-1-GP  
**62.70001.011**



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Taipei Hsien 221, Taiwan, R.O.C.

**ICH7-M (1 of 4)**

## Dellen

Sheet 15 of 43

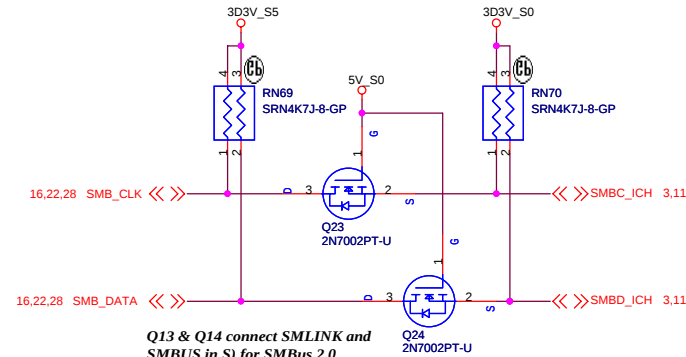
SA





|                                   |         |          |
|-----------------------------------|---------|----------|
| U15E<br>ICH7-M-GP<br>71.ICH7M.00U |         |          |
| A4                                | VSS[1]  | VSS[98]  |
| A23                               | VSS[2]  | VSS[99]  |
| B1                                | VSS[3]  | VSS[100] |
| B8                                | VSS[4]  | VSS[101] |
| B11                               | VSS[5]  | VSS[102] |
| B14                               | VSS[6]  | VSS[103] |
| B17                               | VSS[7]  | VSS[104] |
| B20                               | VSS[8]  | VSS[105] |
| B26                               | VSS[9]  | VSS[106] |
| B28                               | VSS[10] | VSS[107] |
| C2                                | VSS[11] | VSS[108] |
| C6                                | VSS[12] | VSS[109] |
| C27                               | VSS[13] | VSS[110] |
| D10                               | VSS[14] | VSS[111] |
| D13                               | VSS[15] | VSS[112] |
| D18                               | VSS[16] | VSS[113] |
| D21                               | VSS[17] | VSS[114] |
| D24                               | VSS[18] | VSS[115] |
| E1                                | VSS[19] | VSS[116] |
| E2                                | VSS[20] | VSS[117] |
| E4                                | VSS[21] | VSS[118] |
| E8                                | VSS[22] | VSS[119] |
| E15                               | VSS[23] | VSS[120] |
| F3                                | VSS[24] | VSS[121] |
| F4                                | VSS[25] | VSS[122] |
| F5                                | VSS[26] | VSS[123] |
| F12                               | VSS[27] | VSS[124] |
| F27                               | VSS[28] | VSS[125] |
| F28                               | VSS[29] | VSS[126] |
| G1                                | VSS[30] | VSS[127] |
| G2                                | VSS[31] | VSS[128] |
| G5                                | VSS[32] | VSS[129] |
| G6                                | VSS[33] | VSS[130] |
| G9                                | VSS[34] | VSS[131] |
| G14                               | VSS[35] | VSS[132] |
| G18                               | VSS[36] | VSS[133] |
| G21                               | VSS[37] | VSS[134] |
| G24                               | VSS[38] | VSS[135] |
| G25                               | VSS[39] | VSS[136] |
| G26                               | VSS[40] | VSS[137] |
| H3                                | VSS[41] | VSS[138] |
| H4                                | VSS[42] | VSS[139] |
| H5                                | VSS[43] | VSS[140] |
| H24                               | VSS[44] | VSS[141] |
| H27                               | VSS[45] | VSS[142] |
| H28                               | VSS[46] | VSS[143] |
| J1                                | VSS[47] | VSS[144] |
| J2                                | VSS[48] | VSS[145] |
| J5                                | VSS[49] | VSS[146] |
| J24                               | VSS[50] | VSS[147] |
| J25                               | VSS[51] | VSS[148] |
| J26                               | VSS[52] | VSS[149] |
| K24                               | VSS[53] | VSS[150] |
| K27                               | VSS[54] | VSS[151] |
| K28                               | VSS[55] | VSS[152] |
| L13                               | VSS[56] | VSS[153] |
| L15                               | VSS[57] | VSS[154] |
| L24                               | VSS[58] | VSS[155] |
| L25                               | VSS[59] | VSS[156] |
| L26                               | VSS[60] | VSS[157] |
| M3                                | VSS[61] | VSS[158] |
| M4                                | VSS[62] | VSS[159] |
| M5                                | VSS[63] | VSS[160] |
| M12                               | VSS[64] | VSS[161] |
| M13                               | VSS[65] | VSS[162] |
| M14                               | VSS[66] | VSS[163] |
| M15                               | VSS[67] | VSS[164] |
| M16                               | VSS[68] | VSS[165] |
| M17                               | VSS[69] | VSS[166] |
| M24                               | VSS[70] | VSS[167] |
| M27                               | VSS[71] | VSS[168] |
| M28                               | VSS[72] | VSS[169] |
| N1                                | VSS[73] | VSS[170] |
| N2                                | VSS[74] | VSS[171] |
| N5                                | VSS[75] | VSS[172] |
| N6                                | VSS[76] | VSS[173] |
| N11                               | VSS[77] | VSS[174] |
| N12                               | VSS[78] | VSS[175] |
| N13                               | VSS[79] | VSS[176] |
| N14                               | VSS[80] | VSS[177] |
| N15                               | VSS[81] | VSS[178] |
| N16                               | VSS[82] | VSS[179] |
| N17                               | VSS[83] | VSS[180] |
| N18                               | VSS[84] | VSS[181] |
| N24                               | VSS[85] | VSS[182] |
| N25                               | VSS[86] | VSS[183] |
| N26                               | VSS[87] | VSS[184] |
| P3                                | VSS[88] | VSS[185] |
| P4                                | VSS[89] | VSS[186] |
| P12                               | VSS[90] | VSS[187] |
| P13                               | VSS[91] | VSS[188] |
| P14                               | VSS[92] | VSS[189] |
| P15                               | VSS[93] | VSS[190] |
| P16                               | VSS[94] | VSS[191] |
| P17                               | VSS[95] | VSS[192] |
| P24                               | VSS[96] | VSS[193] |
| P27                               | VSS[97] | VSS[194] |

## SMBUS

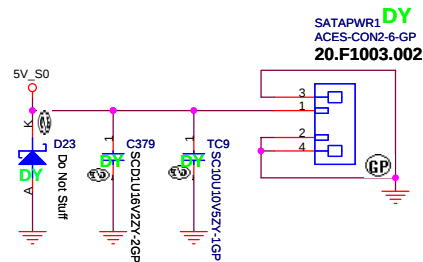
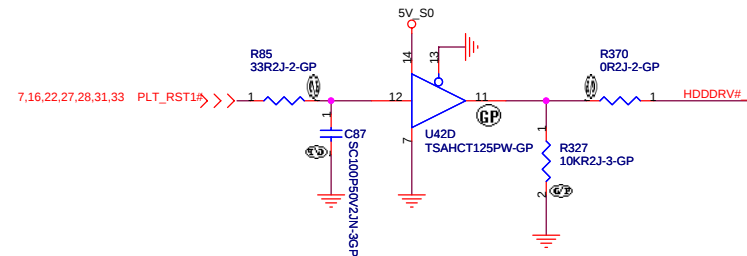
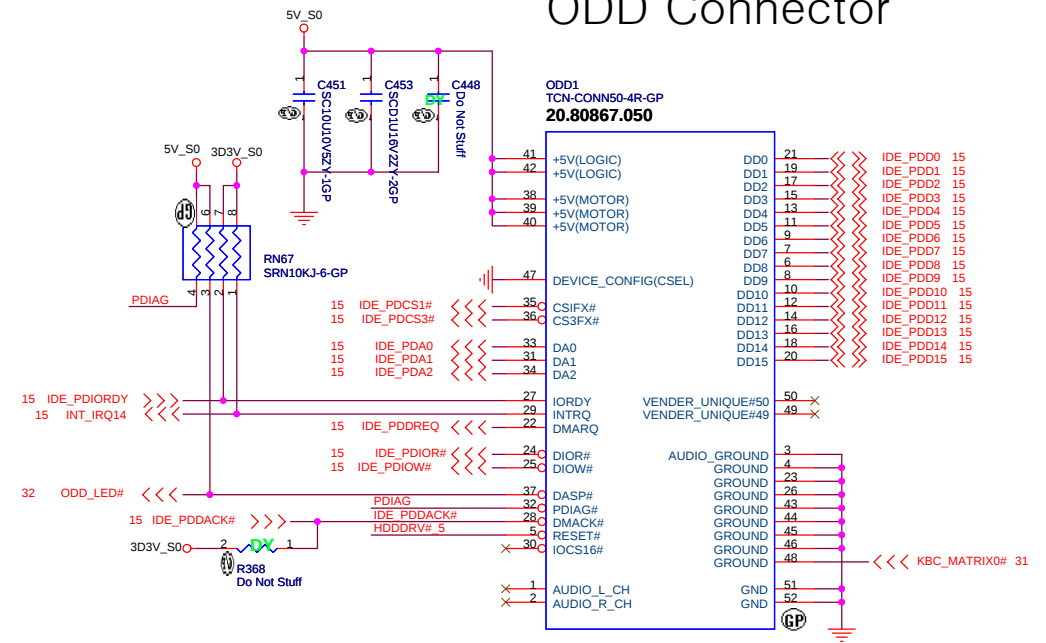


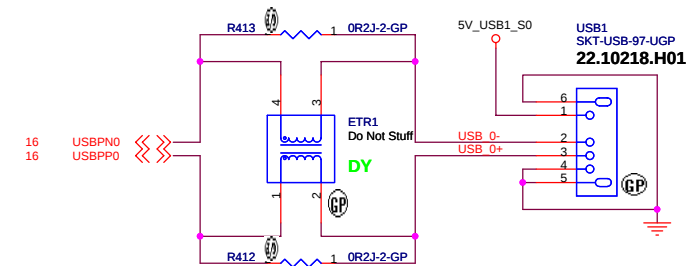
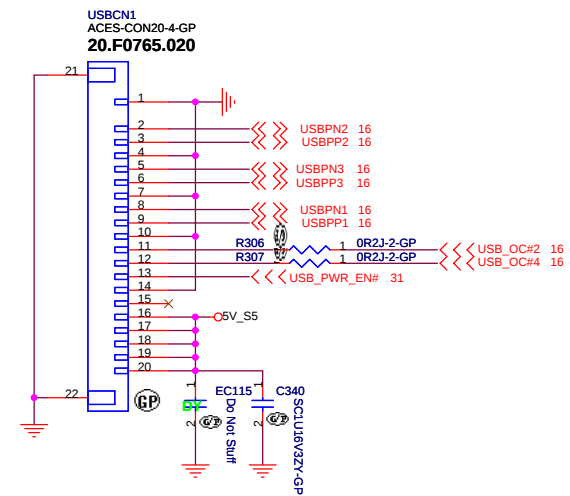
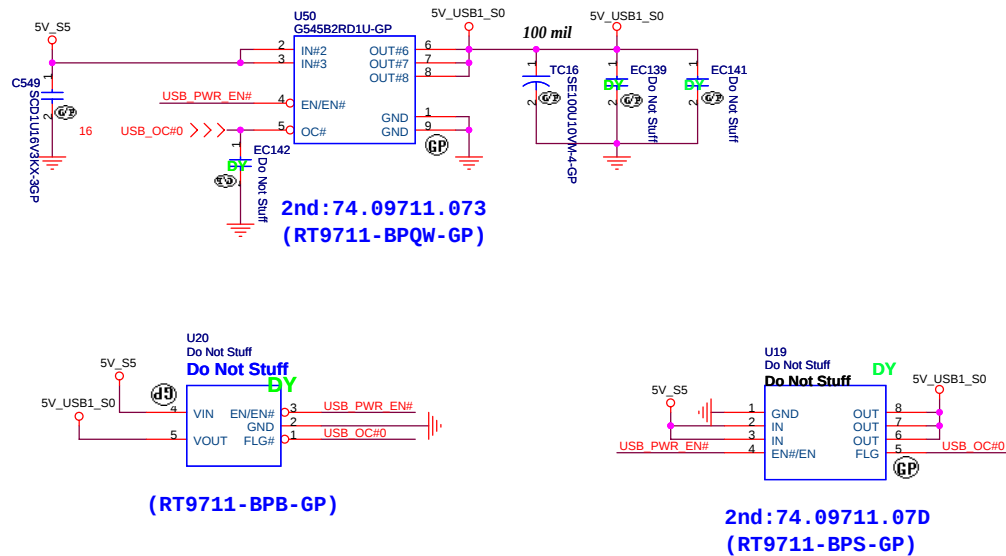
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|                 |                           |                |
|-----------------|---------------------------|----------------|
| Title           |                           |                |
| ICH7-M (4 of 4) |                           |                |
| Size            | Document Number           | Rev            |
| A3              | Dellen                    | SA             |
| Date:           | Tuesday, January 16, 2007 | Sheet 18 of 43 |

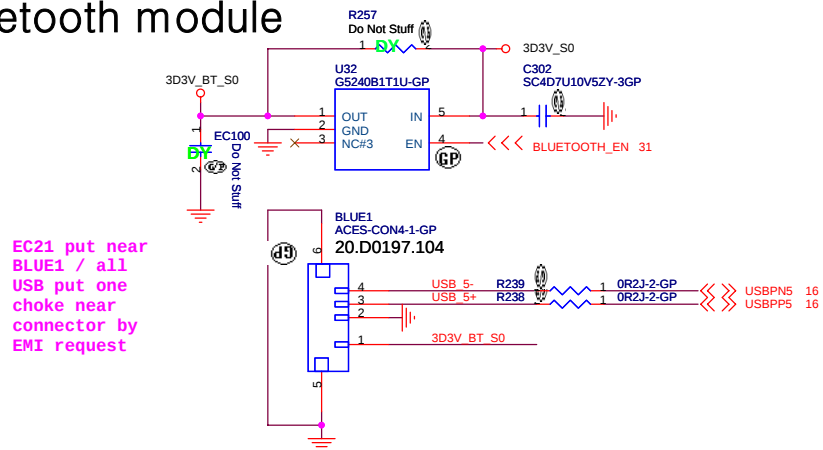


## ODD Connector

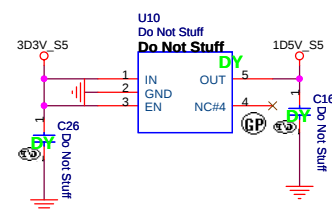
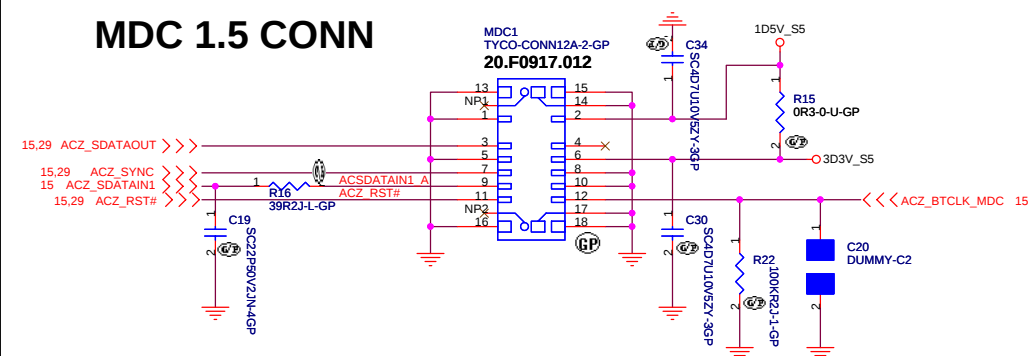




## Bluetooth module



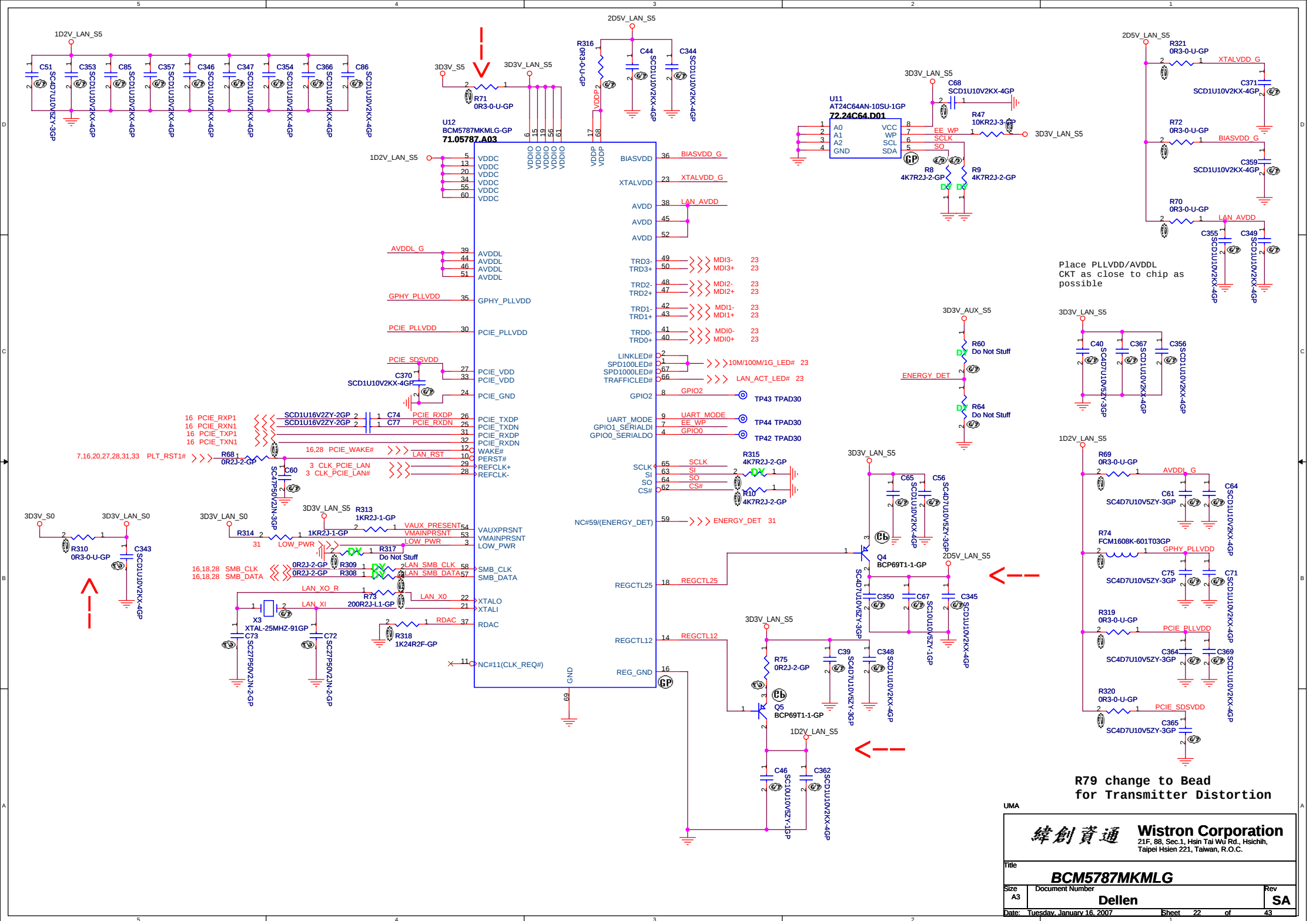
## MDC 1.5 CONN



UMA

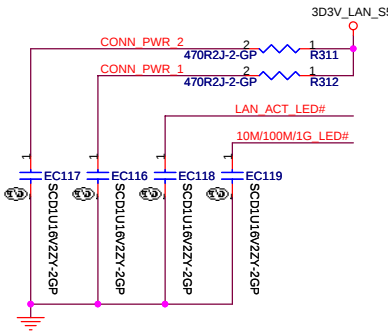
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| Title                           |                 |    |    |
|---------------------------------|-----------------|----|----|
| USB / MDC / BLUETOOTH           |                 |    |    |
| Size A3                         | Document Number | SA |    |
| Date: Tuesday, January 16, 2007 | Sheet 21        | of | 43 |

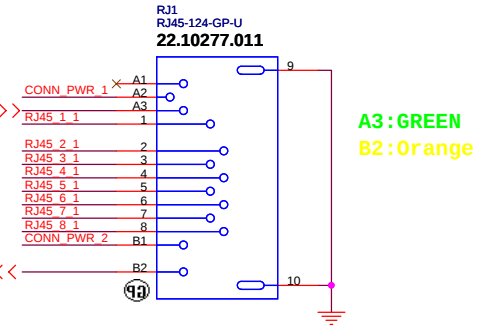


# LAN Connector

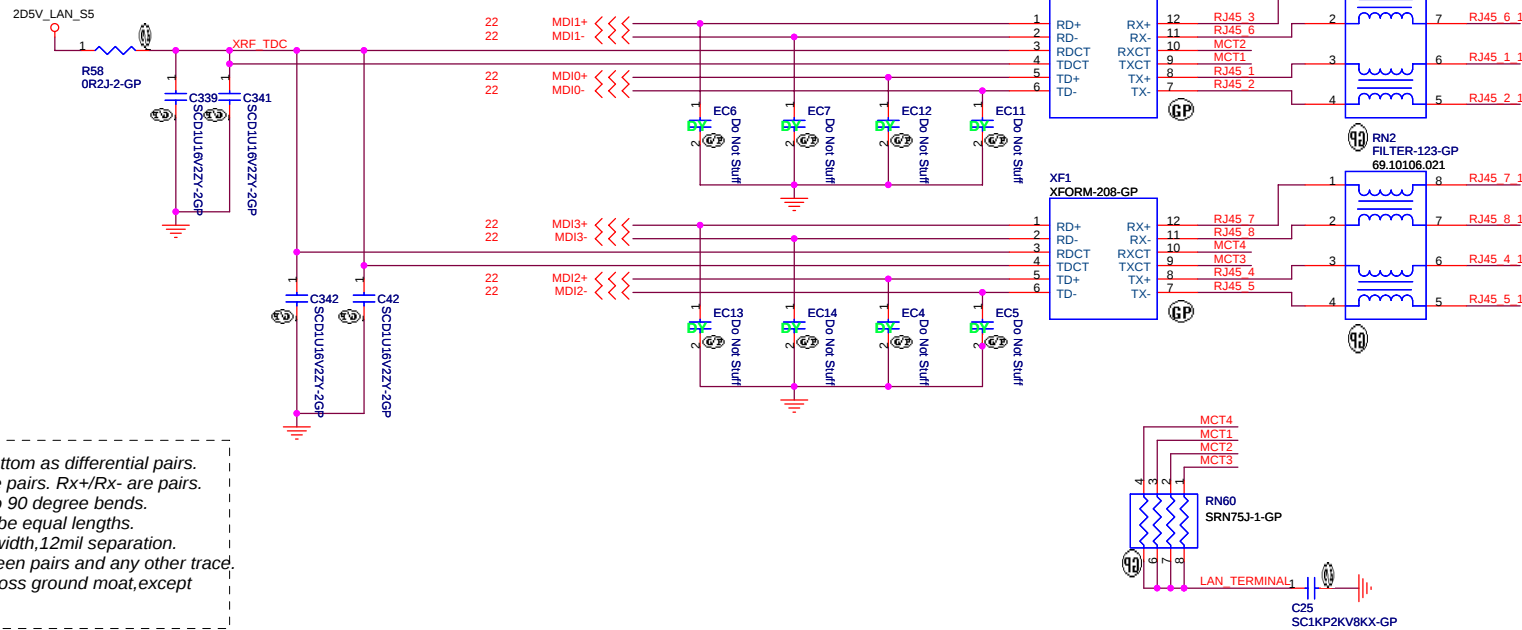
| Voltage Rail | 4401E       | 5789        | 5787       |
|--------------|-------------|-------------|------------|
| VDDIO_PCI    | 3D3V_LAN_S5 | 3D3V_S0     | Don't Care |
| VDDC         | 1D8V_LAN_S5 | 1D2V_LAN_S5 |            |
| VDDIO        | 3D3V_LAN_S5 | 3D3V_LAN_S5 |            |
| VESD         | 3D3V_LAN_S5 | 3D3V_S0     | Don't Care |
| VDDP         | Don't Care  | 2D5V_S5     |            |
| 3D3V_2D5V_S5 | 3D3V_S5     | 2D5V_S5     |            |
| 1D8V_1D2V_S5 | 1D8V_LAN_S5 | 1D2V_S5     |            |



22 10M/100M/1G\_LED# >>>  
22 LAN\_ACT\_LED# <<<



## GIGA Lan Transformer



- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC\_TIP,DOC\_RING,TIP,RING:  
W/S : 10/100 @ Surface layers  
10/20 @ Inner layers

| 10/100 LAN Transformer | RJ45 PIN |
|------------------------|----------|
| TD+ --> TX+            | RJ45-1   |
| TD- --> TX-            | RJ45-2   |
| RD+ --> RX+            | RJ45-3   |
| RD- --> RX-            | RJ45-6   |

UMA

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Title: **LAN Connector**

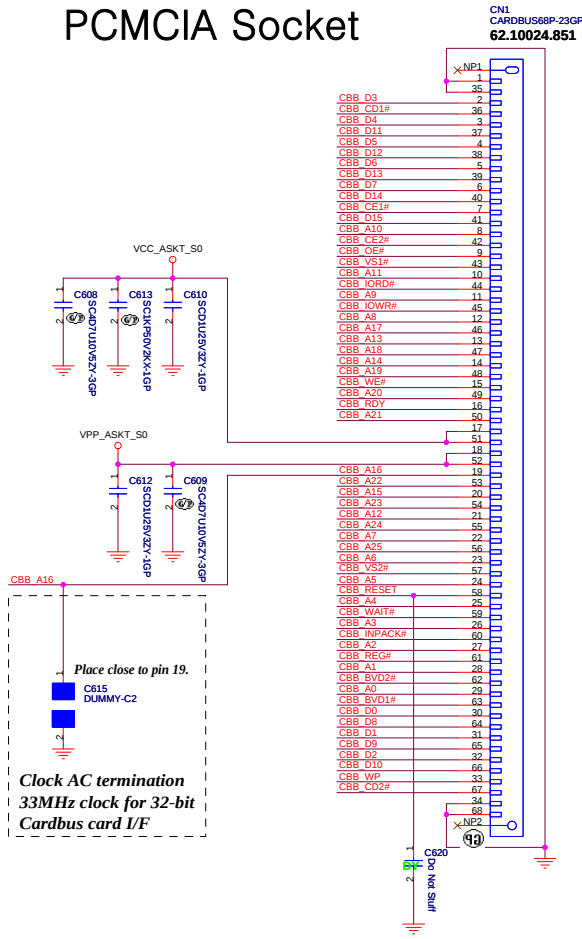
Size A3 Document Number: **Dellen** Rev: **SA**

Date: Tuesday, January 16, 2007 Sheet 23 of 43

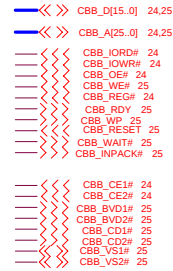




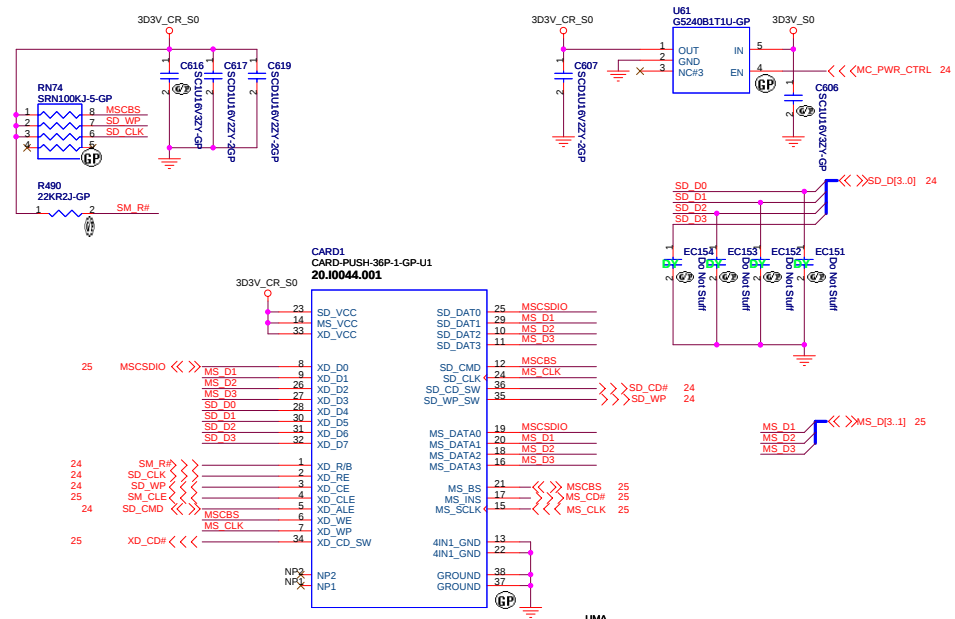
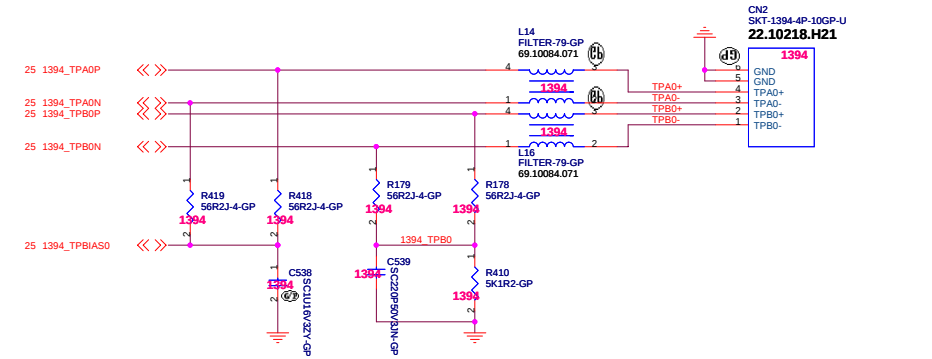
# PCMCIA Socket



## Cardbus I/F



## 1394 Connector



XD  
 MS / MS PRO  
 SD / SD IO / MMC

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**Title**  
PCMCIA / 1394 / CARD READER

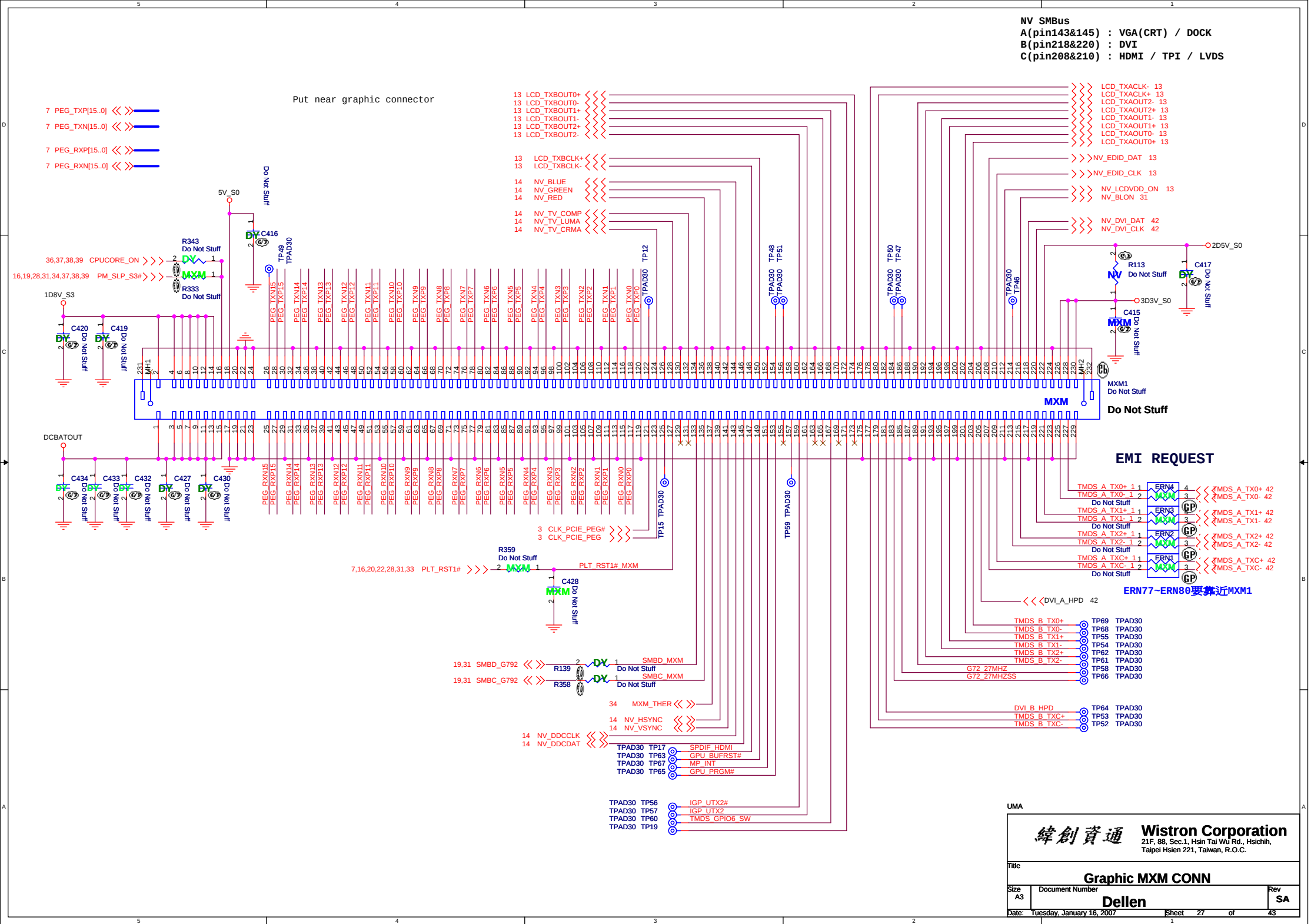
**Size**  
Custom

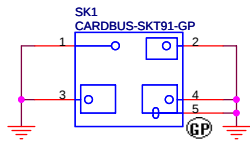
**Document Number**  
Dellen

**Rev**  
SA

**Date:** Tuesday, January 16, 2007

**Sheet** 26 **of** 43

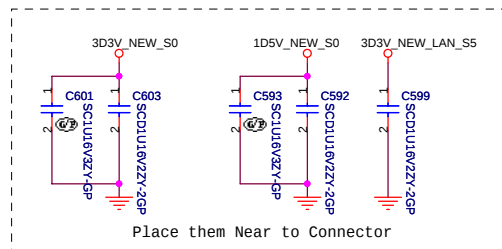
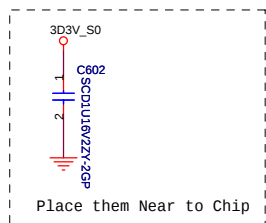
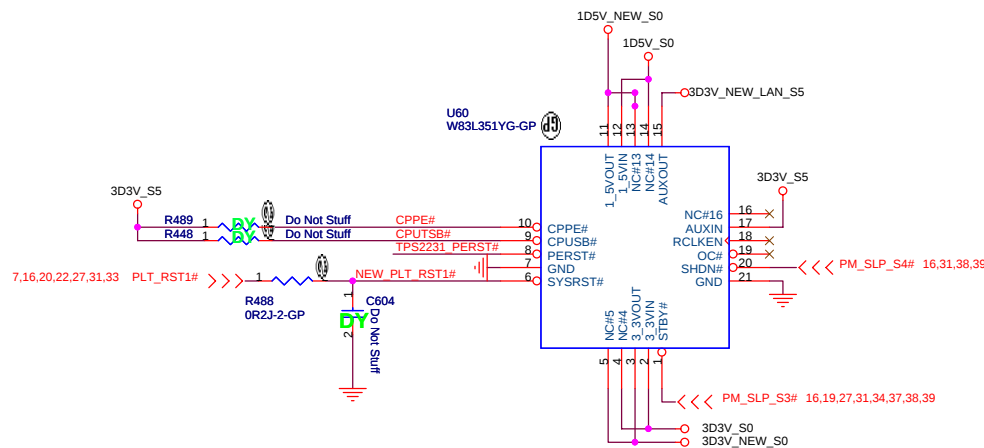
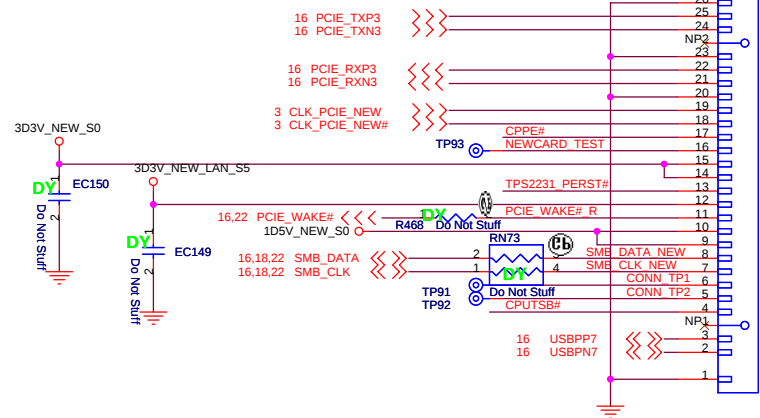




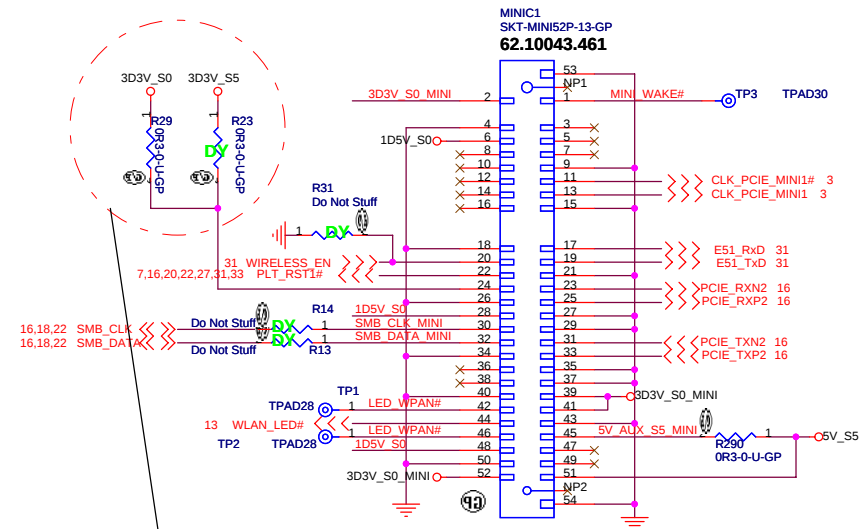
## NEWCARD Connector

Reserve the symbol  
for bottom side  
connector

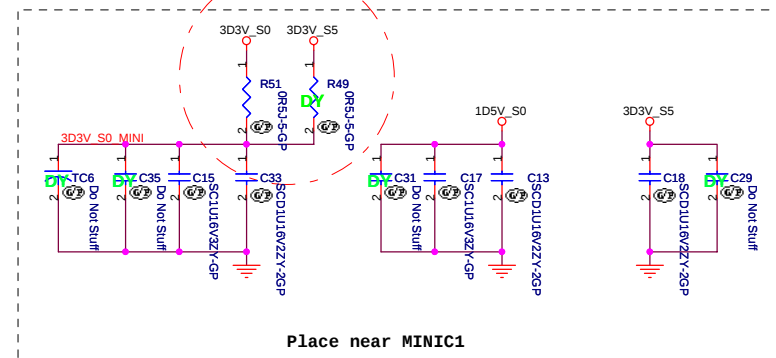
NEW1  
CARDBUS26P-8GP  
62.10024.881



## Mini Card Connector



## PCIE Mini Card For WLA W/O iAMT, TV or 3G



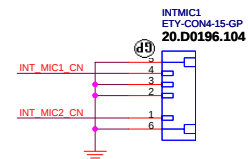
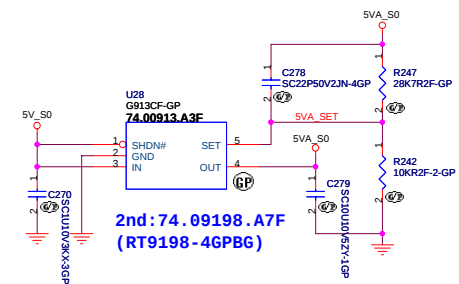
Place near MINIC1

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|                      |                           |                |     |
|----------------------|---------------------------|----------------|-----|
| Title                |                           |                |     |
| MINI CARD / NEW CARD |                           |                |     |
| Size                 | Document Number           |                | Rev |
| A3                   | Dellen                    |                | SA  |
| Date:                | Tuesday, January 16, 2007 | Sheet 28 of 43 |     |



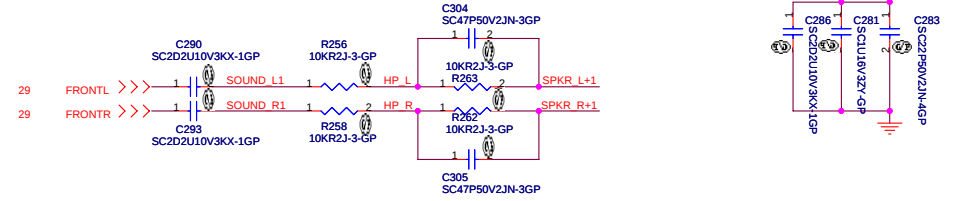
# AUDIO OP AMPLIFIER

R, L 1.5W Speaker  
 mount R274, R281  
 R269->63.36334.1DL  
 R268->63.33334.1DL

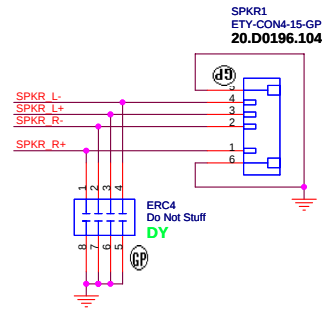
R, L 1W Speaker  
 mount R280, R281  
 R269->63.15334.1DL  
 R268->63.12334.1DL

R, L 1.2W Speaker  
 mount R280, R281  
 R269->63.10334.1DL  
 R268->63.68234.1DL

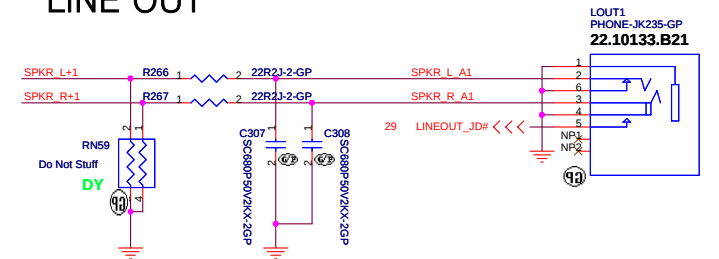
## KBC\_MUTE\_GPI08



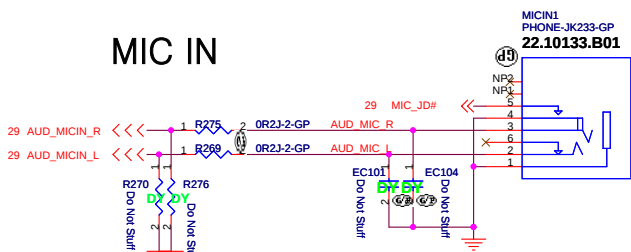
## Internal Speaker



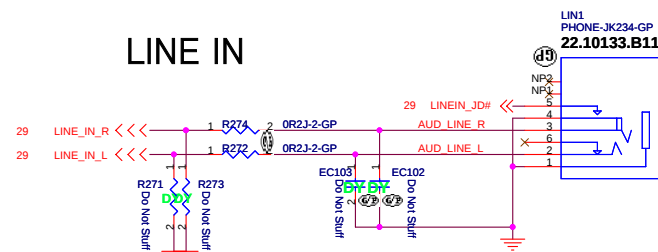
## LINE OUT



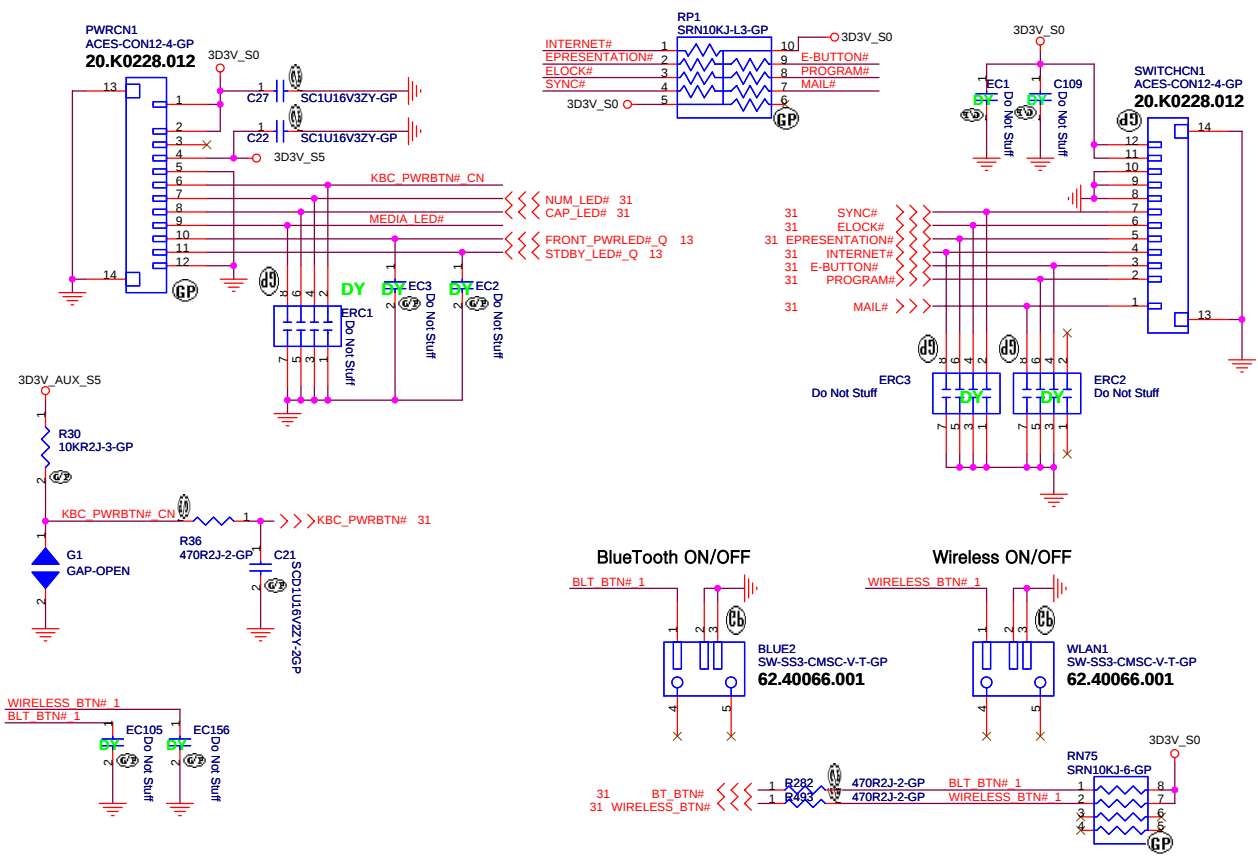
## MIC IN



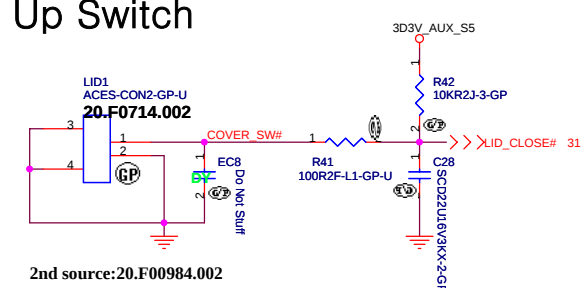
## LINE IN



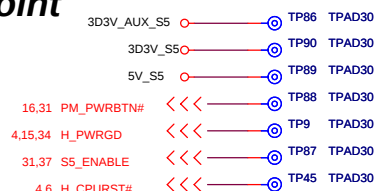




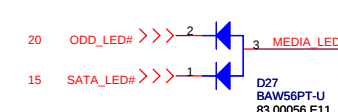
## Cover Up Switch



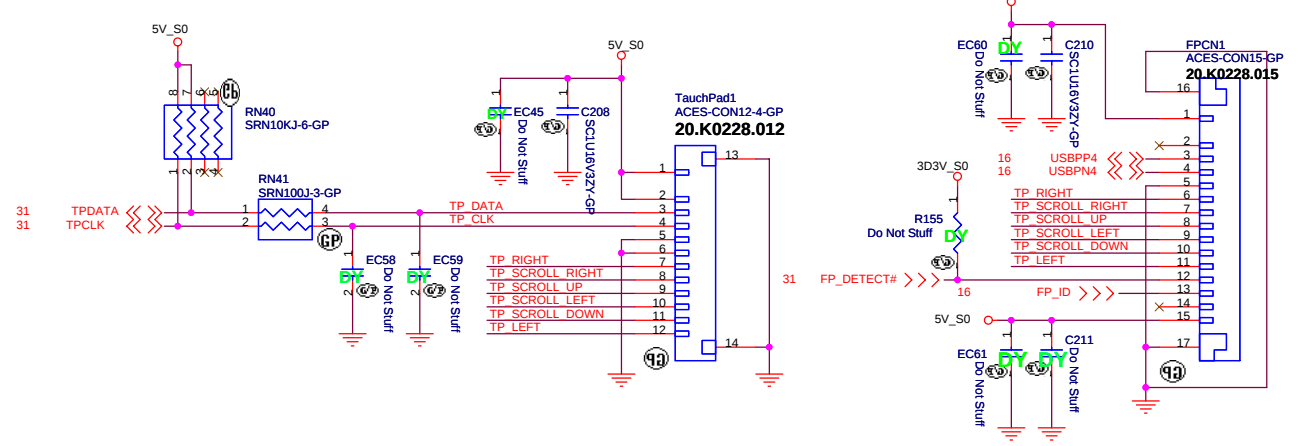
## Check test point



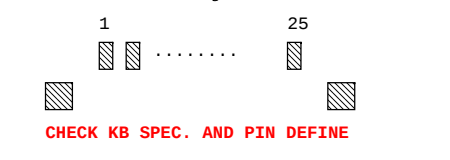
Test Point 放在 Dimm Door 打開可量測處



## TouchPad & FingerPad

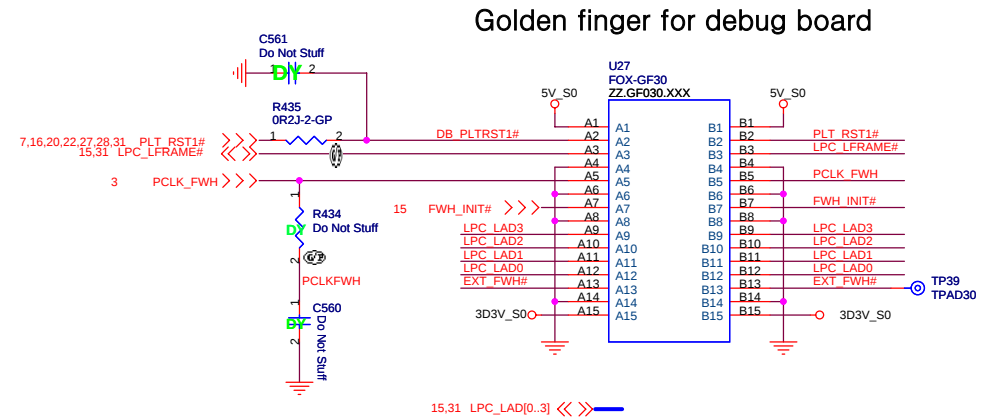
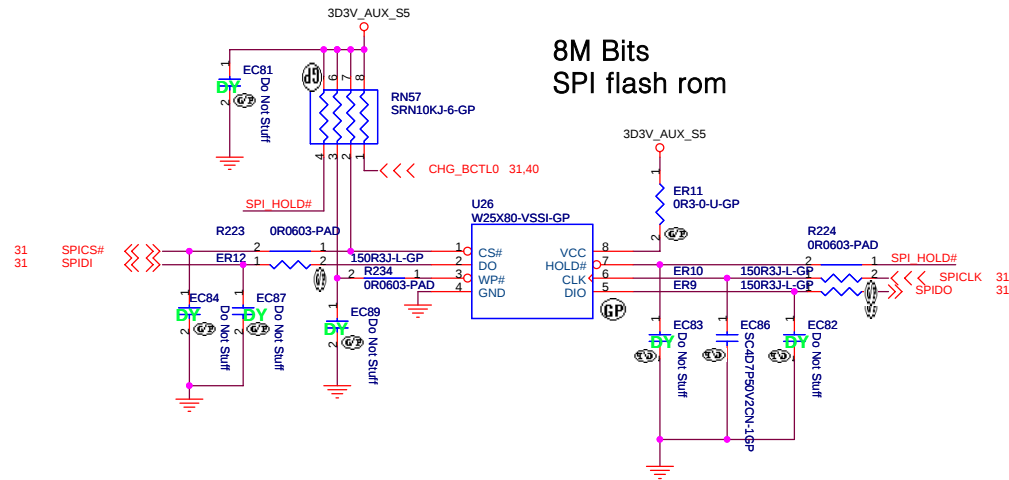


## Internal KeyBoard conn.



## EMI Bypass cap.

|        |      |   |                  |
|--------|------|---|------------------|
| KCOL13 | EC32 | 1 | SC220P50V2JN-3GP |
| KCOL14 | EC33 | 1 | SC220P50V2JN-3GP |
| KCOL15 | EC34 | 1 | SC220P50V2JN-3GP |
| KCOL16 | EC35 | 1 | SC220P50V2JN-3GP |
| KCOL5  | EC28 | 1 | SC220P50V2JN-3GP |
| KCOL6  | EC29 | 1 | SC220P50V2JN-3GP |
| KCOL7  | EC30 | 1 | SC220P50V2JN-3GP |
| KCOL8  | EC31 | 1 | SC220P50V2JN-3GP |
| KCOL1  | EC46 | 1 | SC220P50V2JN-3GP |
| KCOL2  | EC47 | 1 | SC220P50V2JN-3GP |
| KCOL3  | EC48 | 1 | SC220P50V2JN-3GP |
| KCOL4  | EC49 | 1 | SC220P50V2JN-3GP |
| KCOL17 | EC36 | 1 | SC220P50V2JN-3GP |
| KCOL18 | EC37 | 1 | SC220P50V2JN-3GP |
| KROW8  | EC41 | 1 | SC220P50V2JN-3GP |
| KROW7  | EC40 | 1 | SC220P50V2JN-3GP |
| KROW6  | EC39 | 1 | SC220P50V2JN-3GP |
| KROW5  | EC38 | 1 | SC220P50V2JN-3GP |
| KROW4  | EC57 | 1 | SC220P50V2JN-3GP |
| KROW3  | EC56 | 1 | SC220P50V2JN-3GP |
| KROW2  | EC55 | 1 | SC220P50V2JN-3GP |
| KROW1  | EC54 | 1 | SC220P50V2JN-3GP |
| KCOL9  | EC50 | 1 | SC220P50V2JN-3GP |
| KCOL10 | EC51 | 1 | SC220P50V2JN-3GP |
| KCOL11 | EC52 | 1 | SC220P50V2JN-3GP |
| KCOL12 | EC53 | 1 | SC220P50V2JN-3GP |

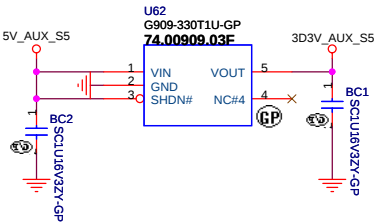


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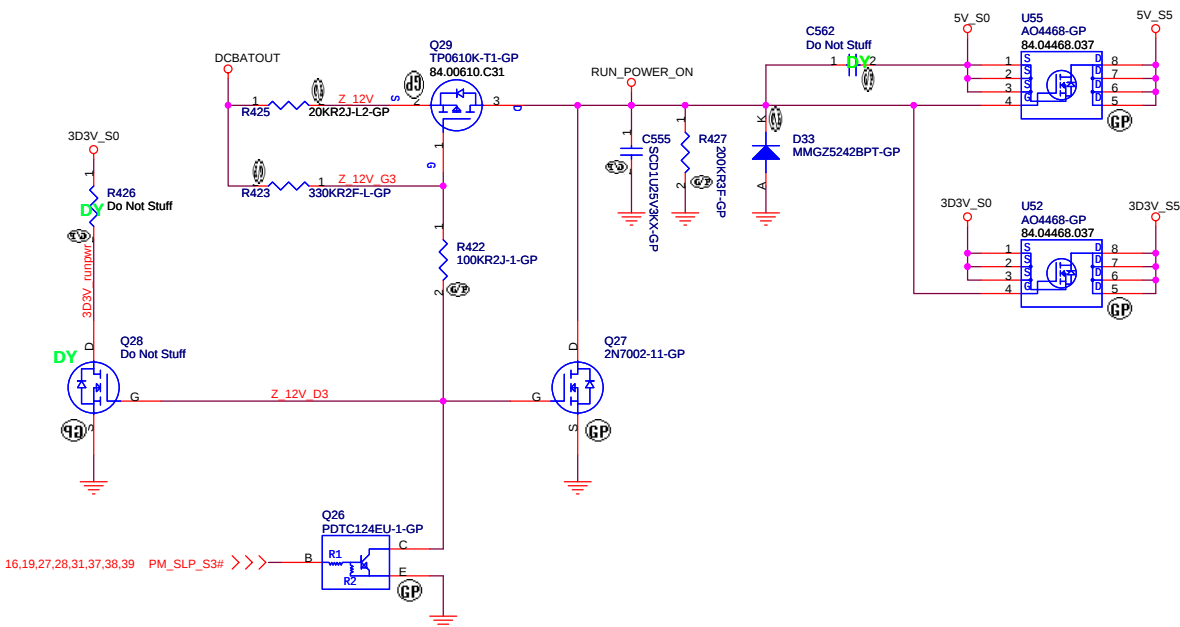
Aux Power

3D3V\_AUX\_S5

I max = 150 mA

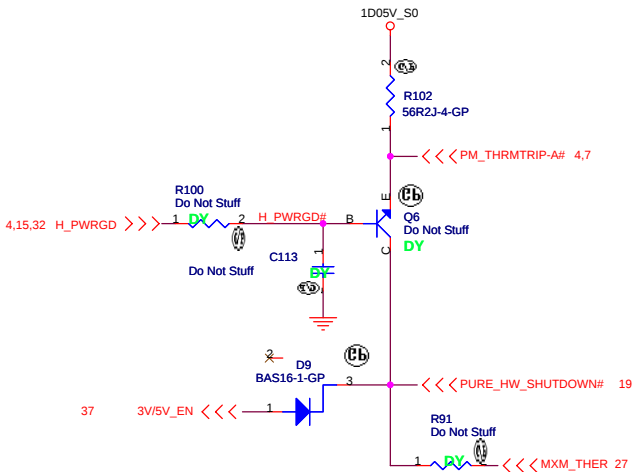


Run Power

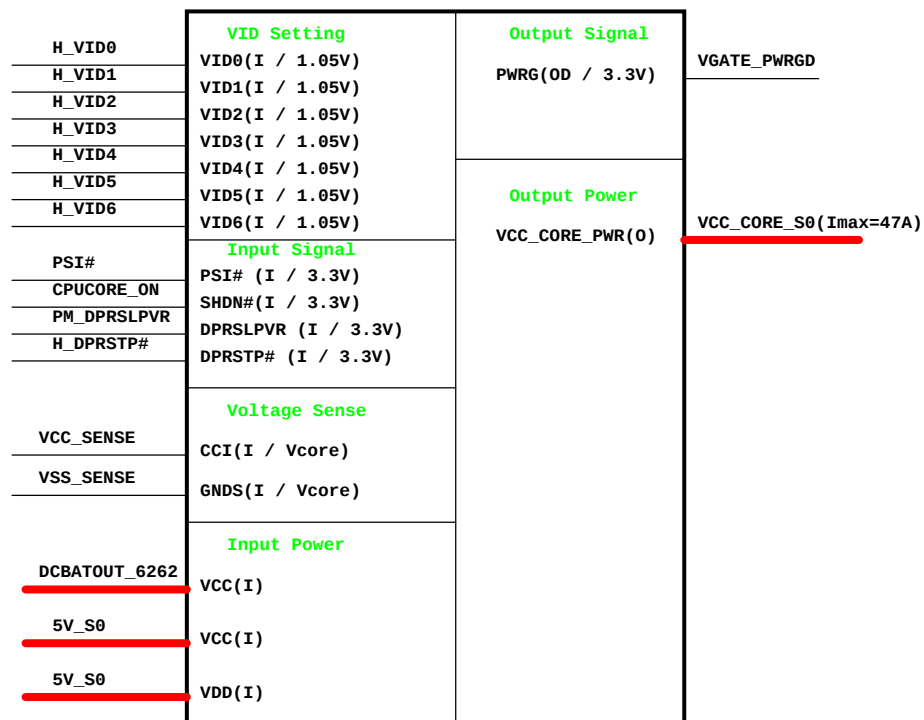


5V\_S0

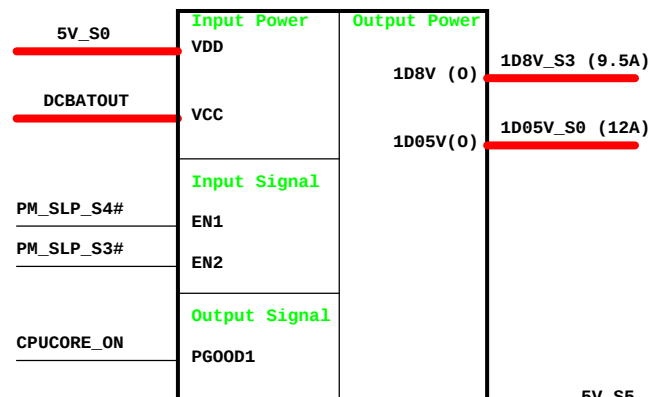
3D3V\_S0



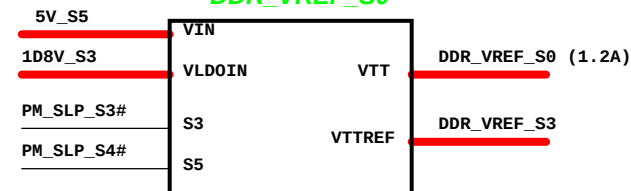
CPU\_CORE  
MAX8770



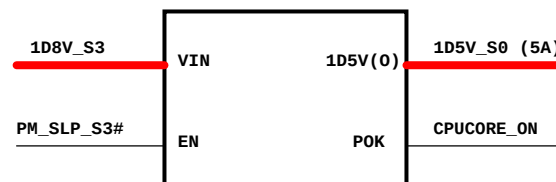
MAX8717  
1D8V\_S3 / 1D05V\_S0



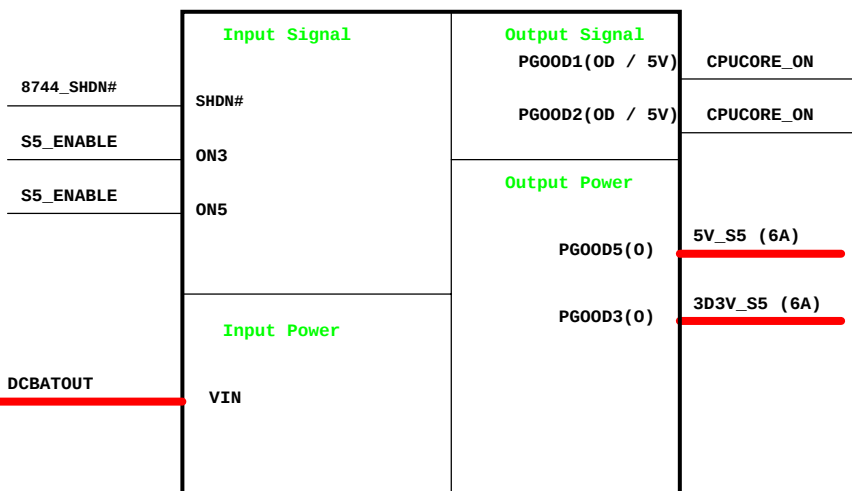
TPS51100  
DDR\_VREF\_S0



APL5912  
1D5V\_S0



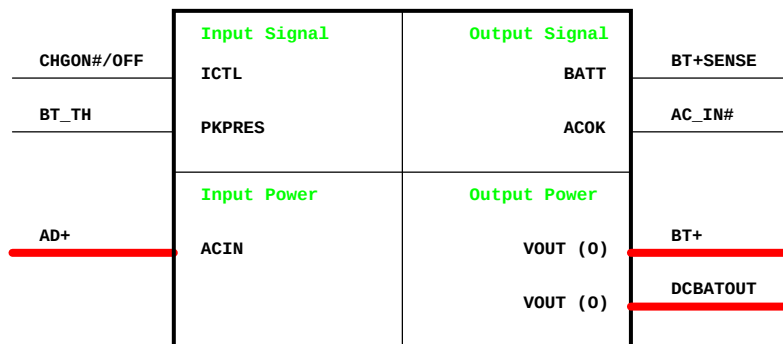
MAX8744  
5V\_S5 / 3D3V\_S5

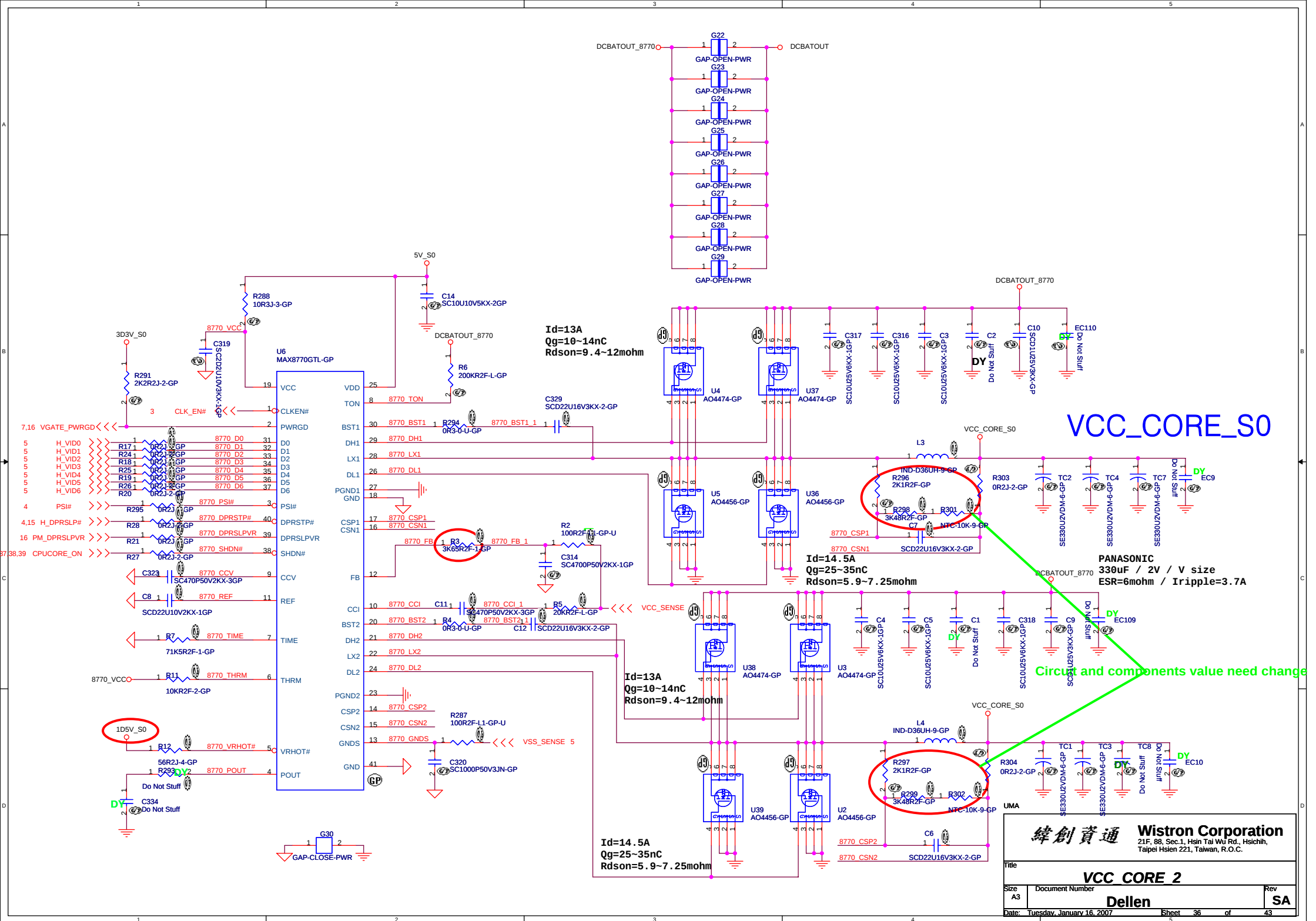


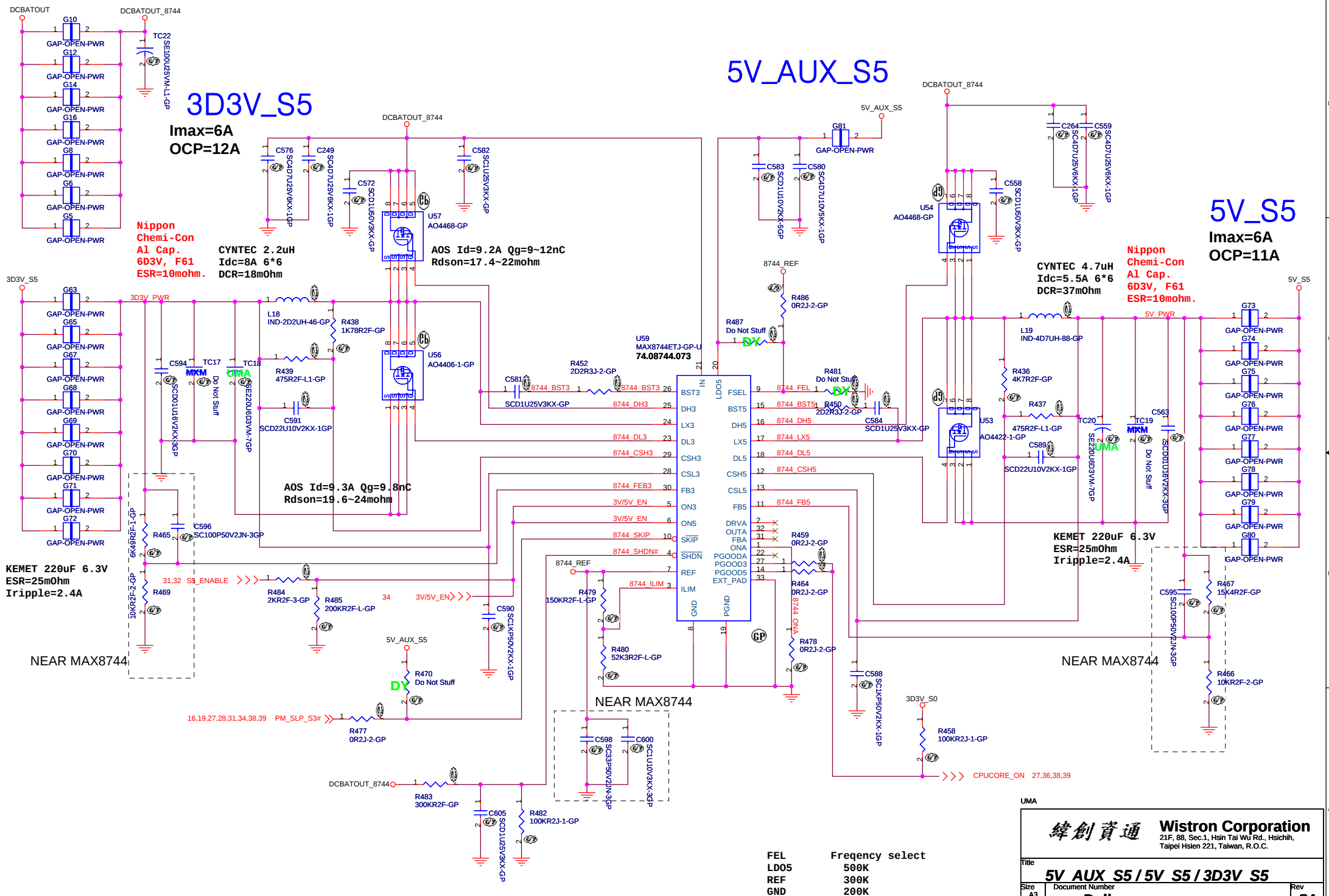
APL5312  
2D5V\_S0



Charger ISL6255



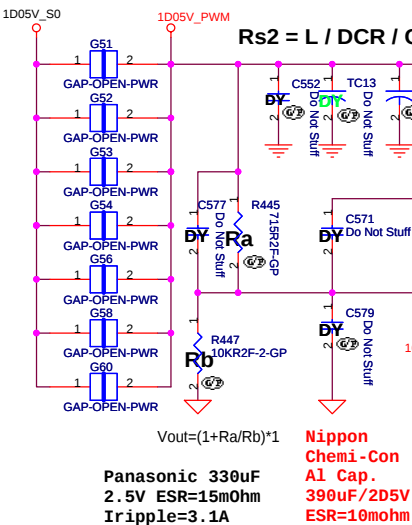




# 1D05V\_S0

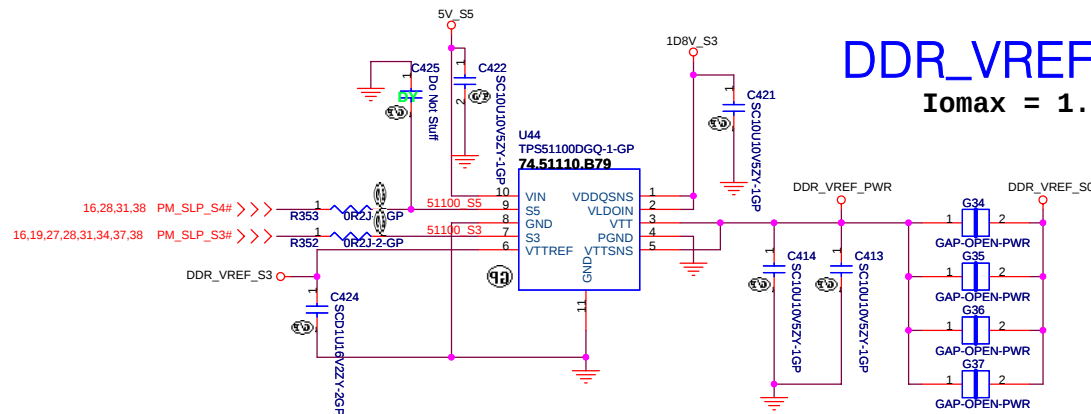
1D05V I<sub>max</sub>=12A  
OCP>19A

V<sub>cal</sub>=1.0511V



# DDR\_VREF\_S0

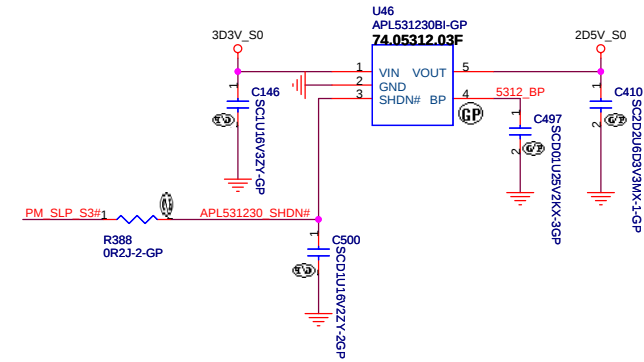
Iomax = 1.2A



# DDR\_VREF\_S3

# 2D5V\_S0

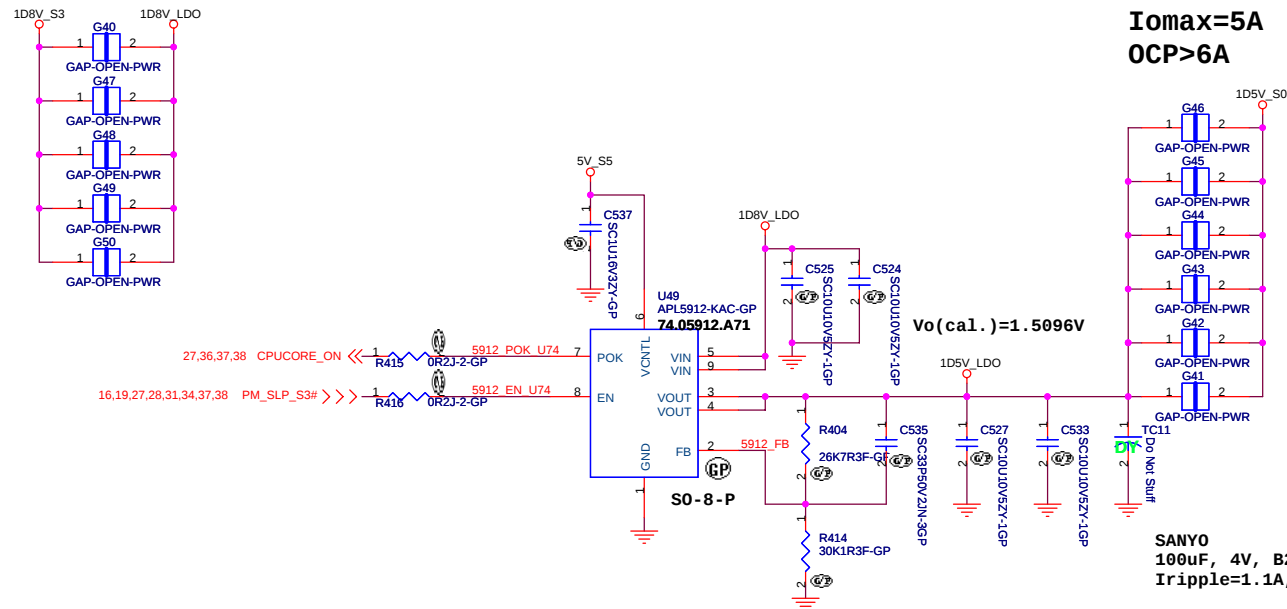
Iomax = 130mA



# 1D5V\_S0

Iomax=5A

OCP>6A

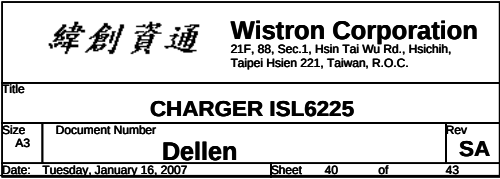


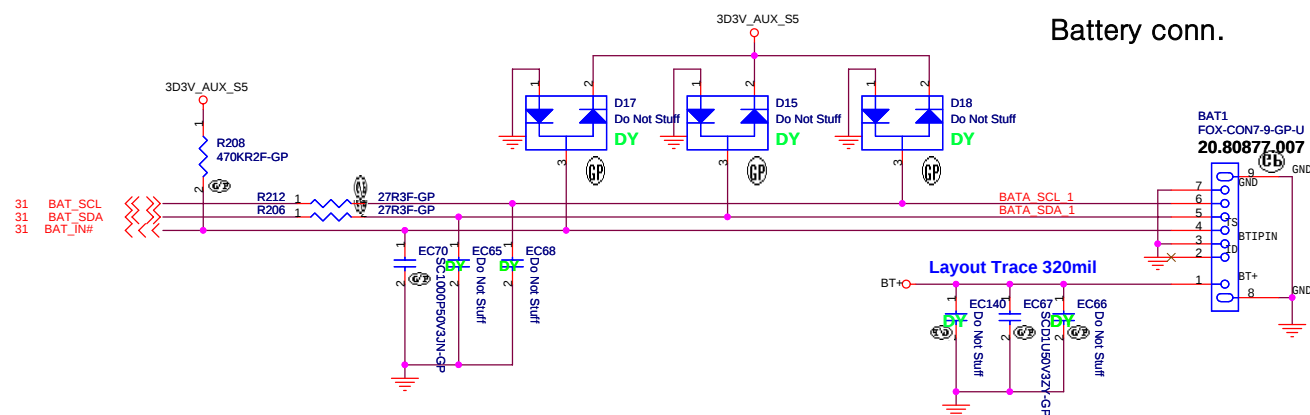
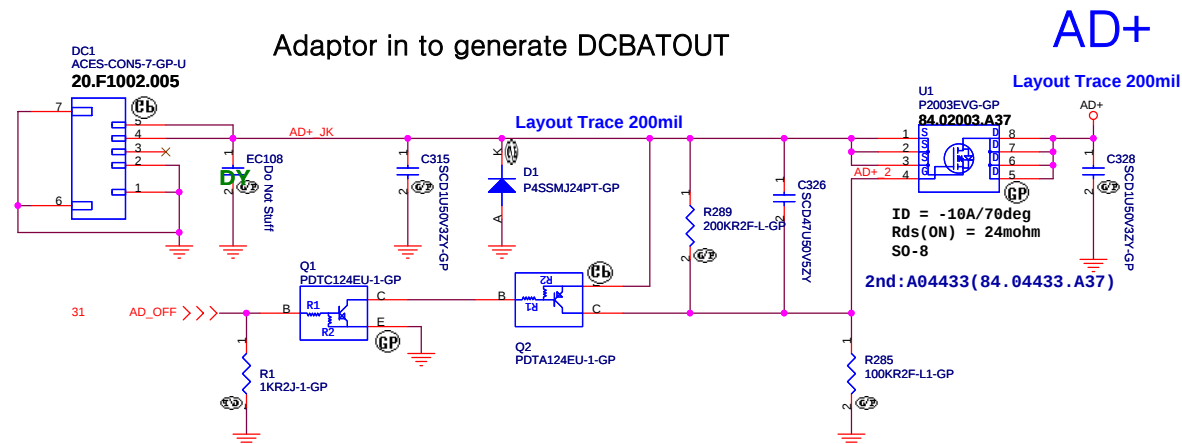
$$Vo=0.8*(1+(R1/R2))$$

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|                                 |                 |     |
|---------------------------------|-----------------|-----|
| Title                           |                 |     |
| 1D5V_S0 / 2D5V_S0 / DDR_VREF_S0 |                 |     |
| Size                            | Document Number | Rev |
| A3                              | Dellen          | SA  |
| Date: Tuesday, January 16, 2007 |                 |     |
| Sheet 39 of 43                  |                 |     |

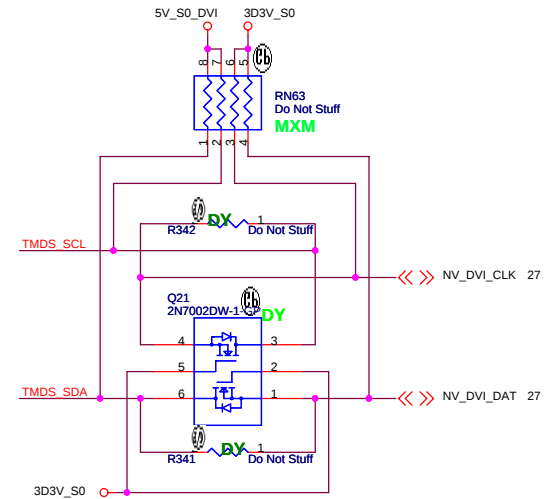
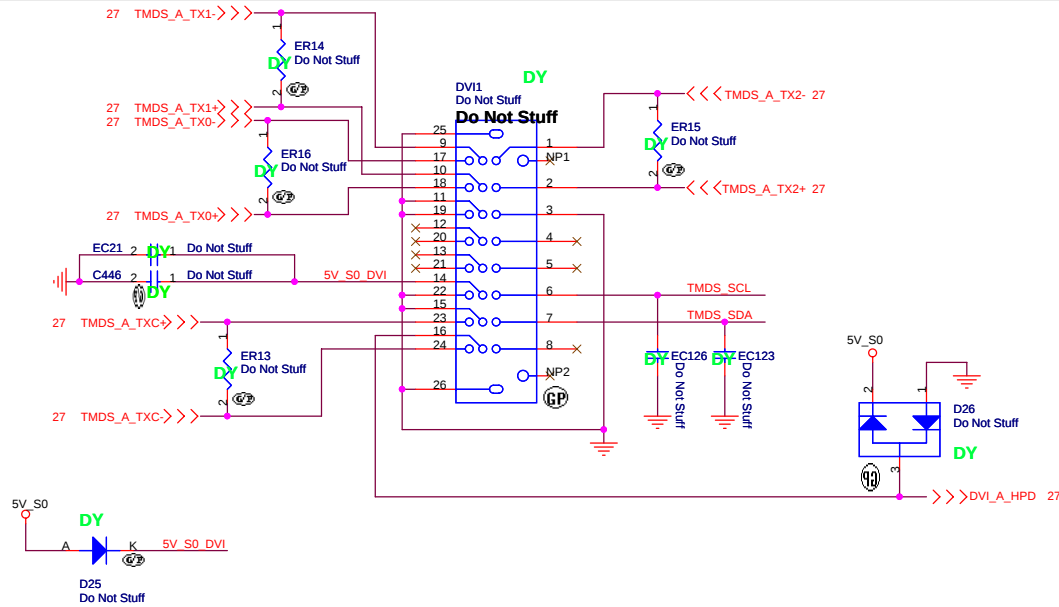




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|                                 |                 |     |
|---------------------------------|-----------------|-----|
| Title                           |                 |     |
| AD / BATT conn.                 |                 |     |
| Size                            | Document Number | Rev |
| A3                              | Dellen          | SA  |
| Date: Tuesday, January 16, 2007 |                 |     |
| Sheet 41 of 43                  |                 |     |



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|                                                                            |                 |                     |          |
|----------------------------------------------------------------------------|-----------------|---------------------|----------|
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| Title                                                                      |                 |                     |          |
| DVI CONNECTOR                                                              |                 |                     |          |
| Size                                                                       | Document Number | Rev                 |          |
| A3                                                                         |                 | SA                  |          |
| Date: Tuesday, January 16, 2007                                            |                 | Sheet               | 42 of 43 |

