QMLE4/5

Eureka UMA

LA-8864P REV 0.3 Schematic

AMD Trinity FS1r2 APU / Hudson M3 FCH

2012-03-14 Rev 0.3

Security Classification	Compal Secret Data		
Issued Date	2011/11/21	Deciphered Date	2011/12/11

Compal Electronics, Inc.		
Title: SCHEMATIC,MB LA-8864		
Size: B	Document Number: 4019IS	Rev: A
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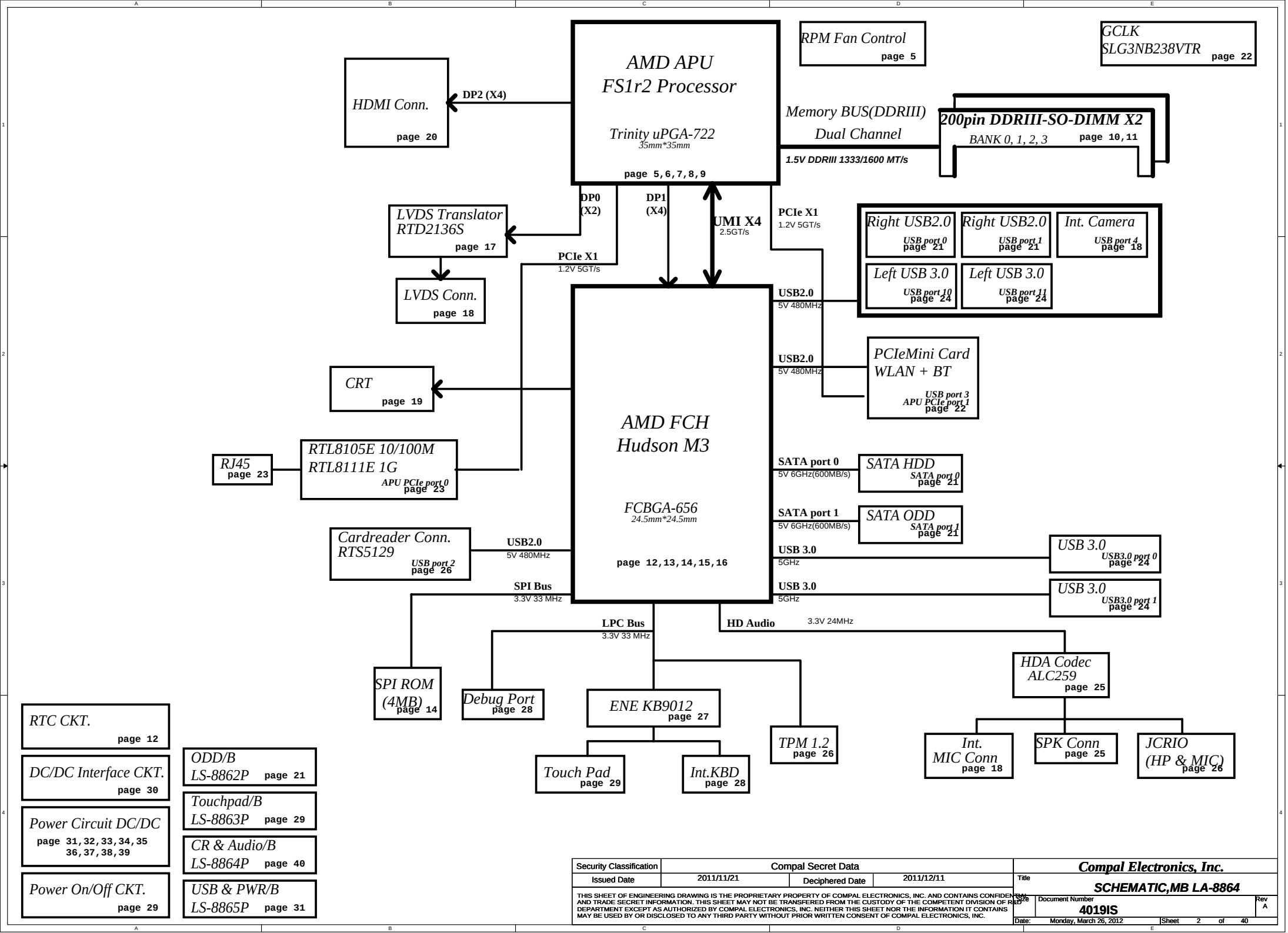

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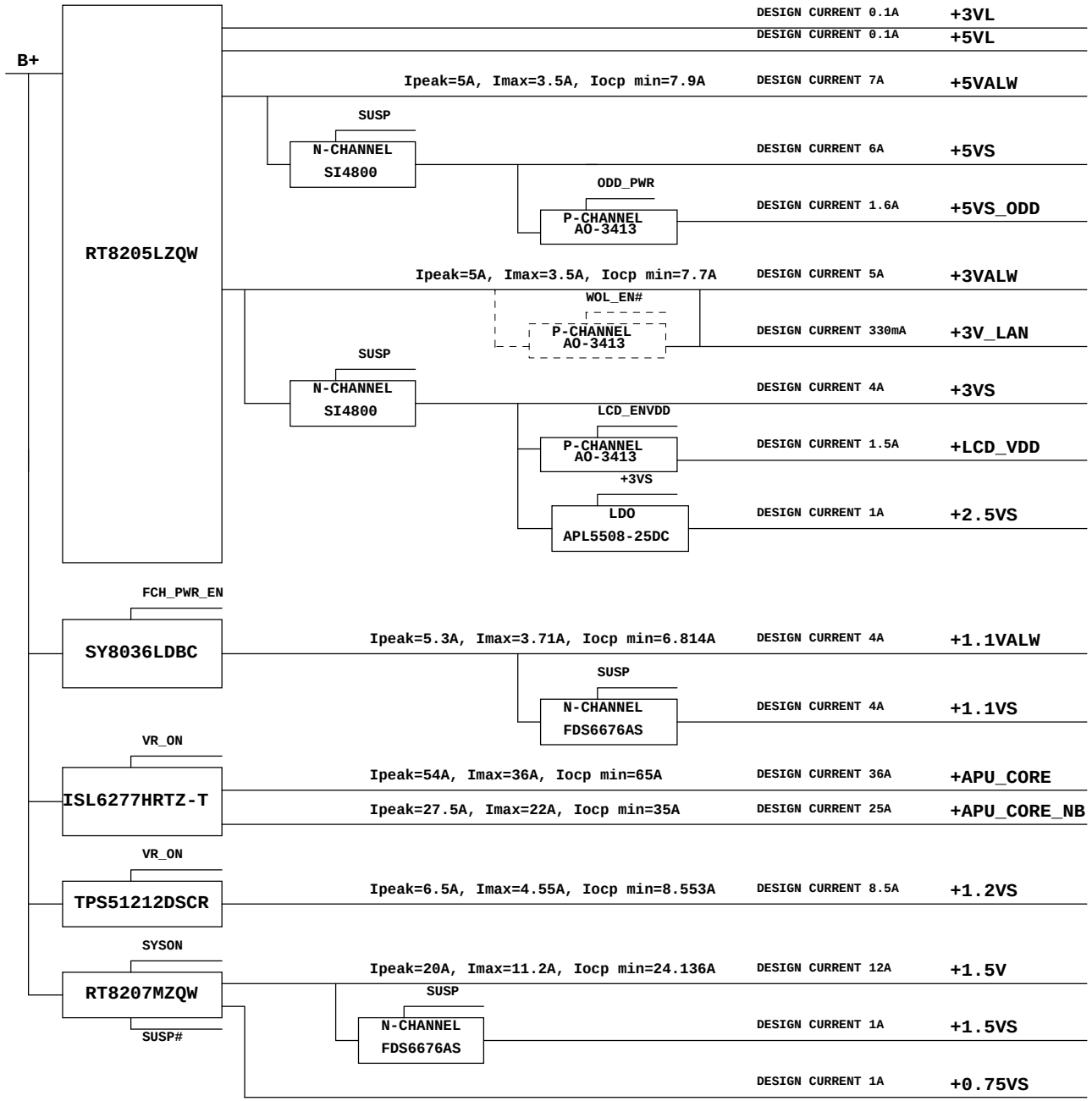

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	VL +3VL	+5VALW +3VALW +1.1VALW +VSB	+1.5V	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +APU_CORE +APU_CORE_NB
S0	0	0	0	0	0	0
S1	0	0	0	0	0	0
S3	0	0	0	0	0	X
S5 S4/AC	0	0	0	0	X	X
S5 S4/ Battery only	0	0	0	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X	X

BTO Option Table

Function	FCH			Clock	
description	Hudson-M3			Clock	
explain	R1	R3	UNBW	Green Clock	No Green Clock
BTO	HUDM3R1@	HUDM3R3@	HUDM3UNBW@	GCLK@	NOGCLK@

Function	LAN		Camera	Internal Analog MIC	TPM	
description	LAN		Camera	Internal Analog MIC	TPM	
explain	10/100M	GIGA	Camera	Internal Analog MIC	9635	9655
BTO	8105ELDO@	8111FVB@	CAM@	AMIC@	TPM9635@	TPM9655@

FCH SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 000X b
+3VS	DDR SO-DIMM 1	A2 H	1010 001X b
+3VS	WLAN		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Charger	12 H	0001 0010 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VL	SB-TSI	98 H	1001 1001 b

EC SM Bus3 Address

Power	Device	HEX	Address
+3VS	LVDS Translator	94 H	1001 0100 b

STATE / SIGNAL	SLP_S3#	SLP_S5#
Full ON	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH
S4 (Suspend to Disk)	LOW	HIGH
S5 (Soft OFF)	LOW	LOW
G3	LOW	LOW

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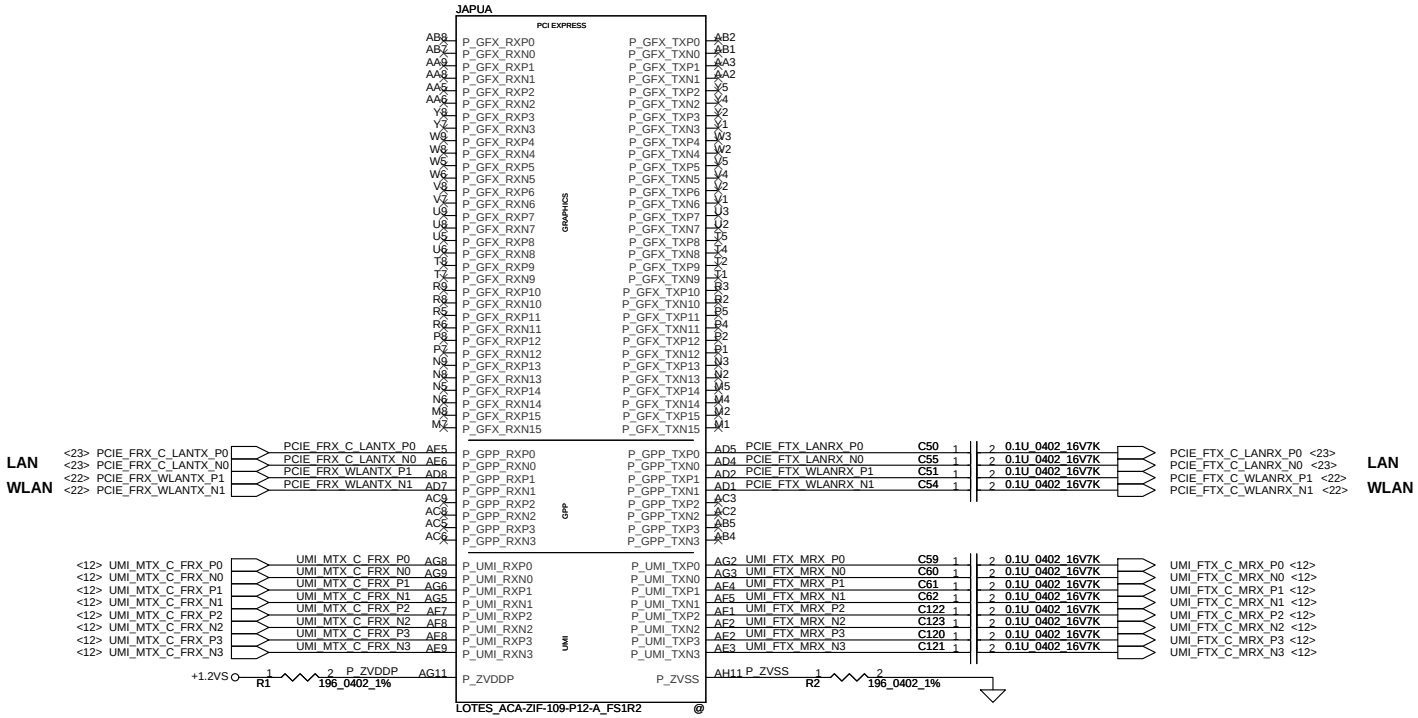
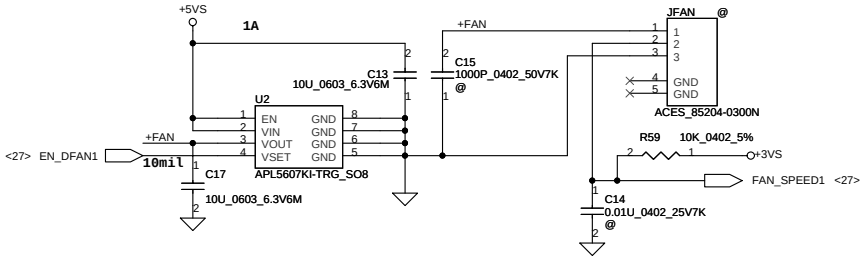


FAN Control Circuit



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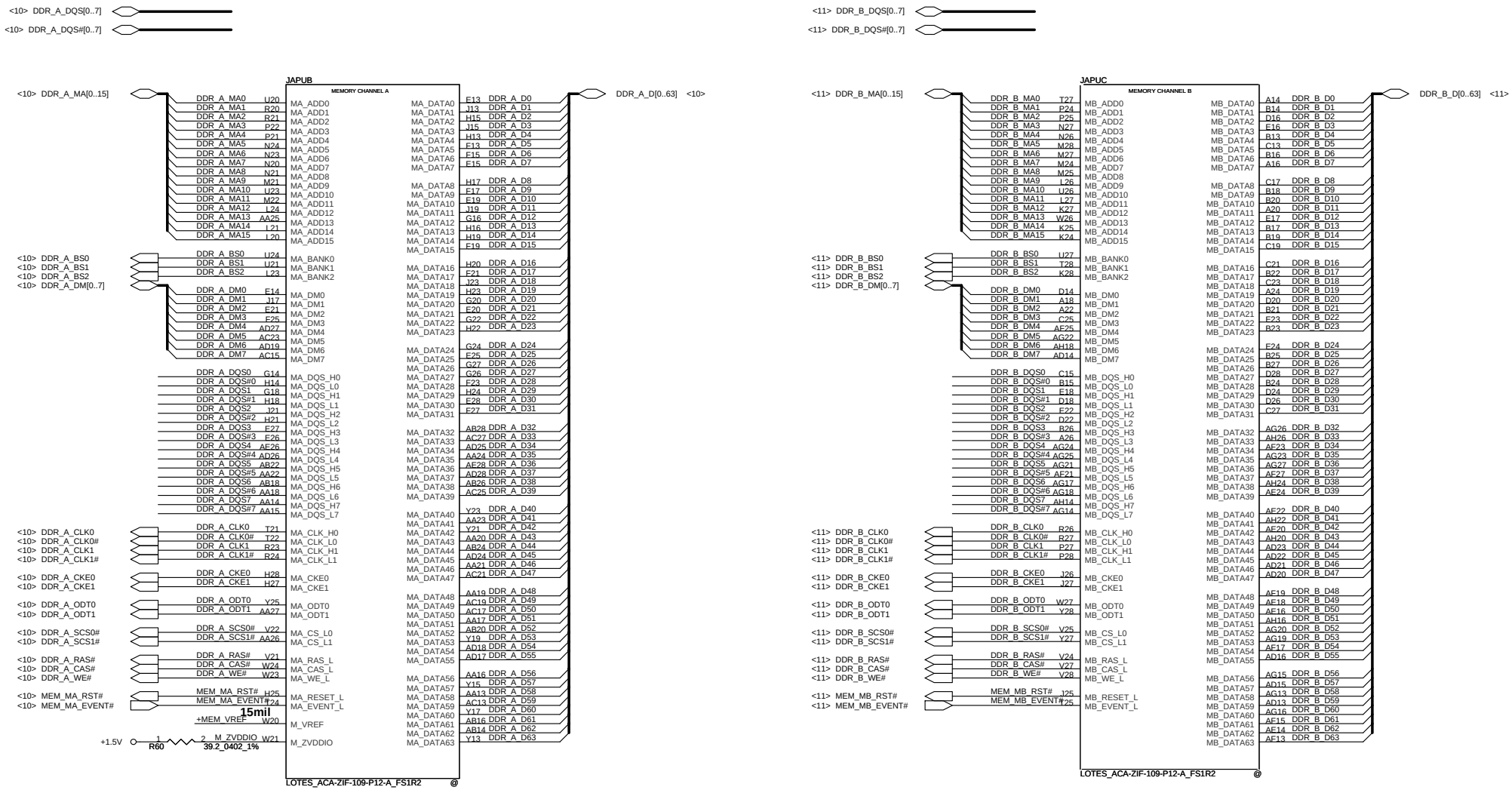
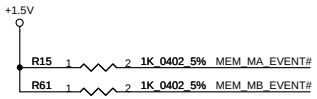
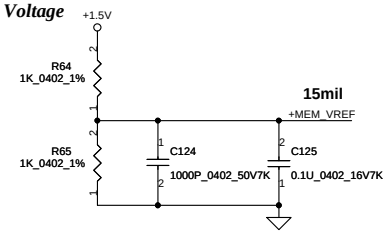


EVENT# pull high



0.75V Reference Voltage



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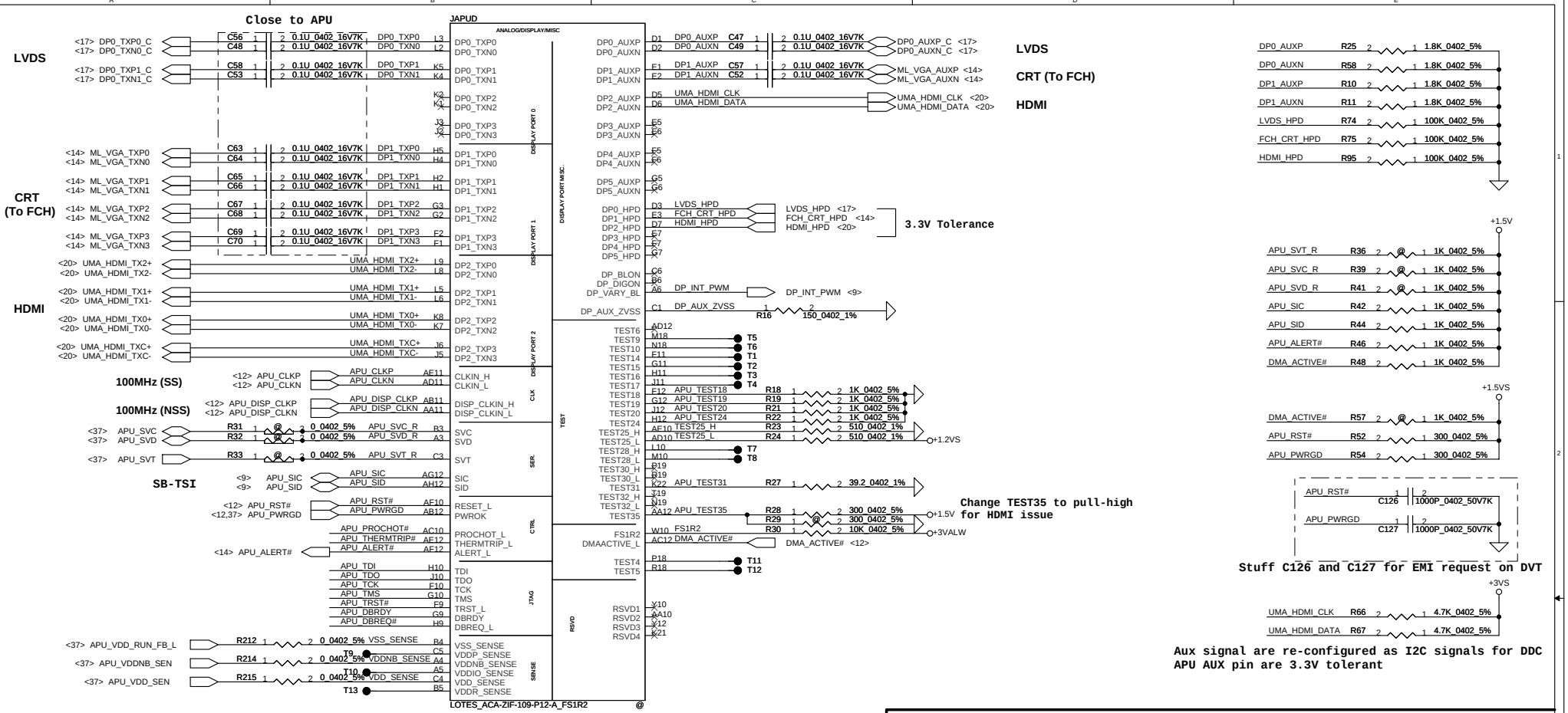

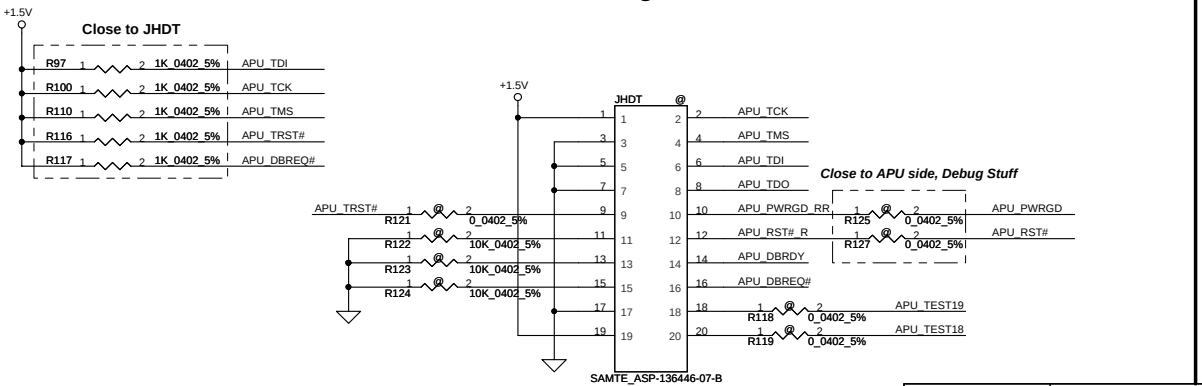

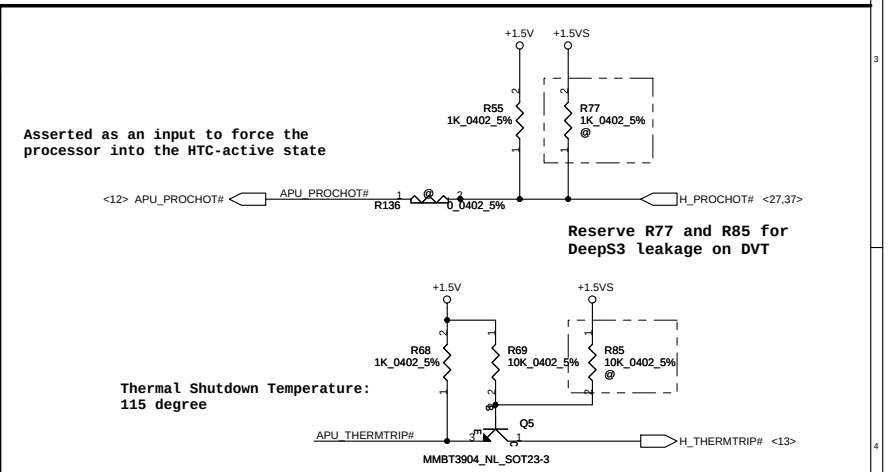

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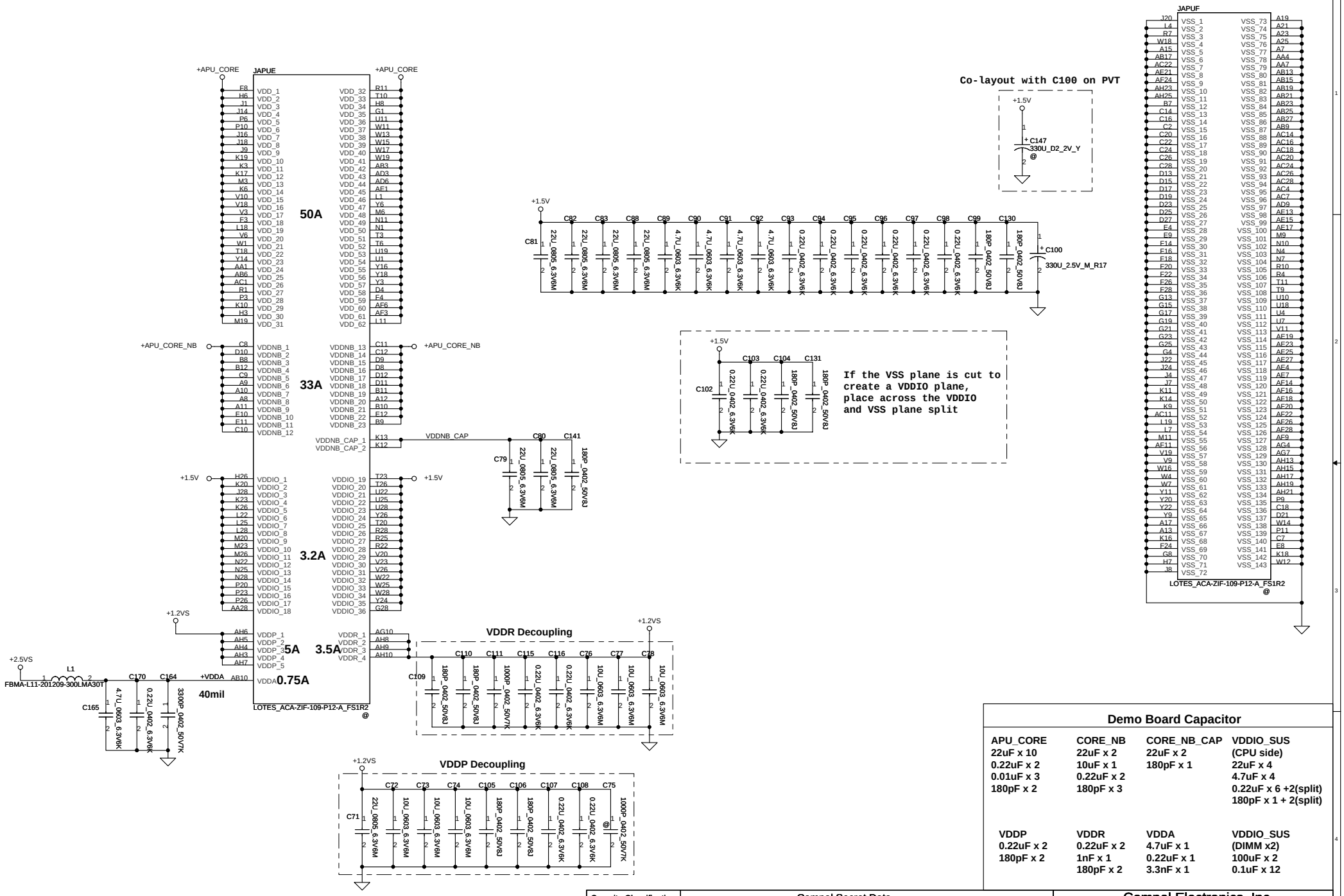

Demo Board Capacitor

APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	180pF x 1	22uF x 4
0.01uF x 3	0.22uF x 2		4.7uF x 4
180pF x 2	180pF x 3		0.22uF x 6 +2(split)
			180pF x 1 + 2(split)

VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 1	0.22uF x 1	100uF x 2
	180pF x 2	3.3nF x 1	0.1uF x 12

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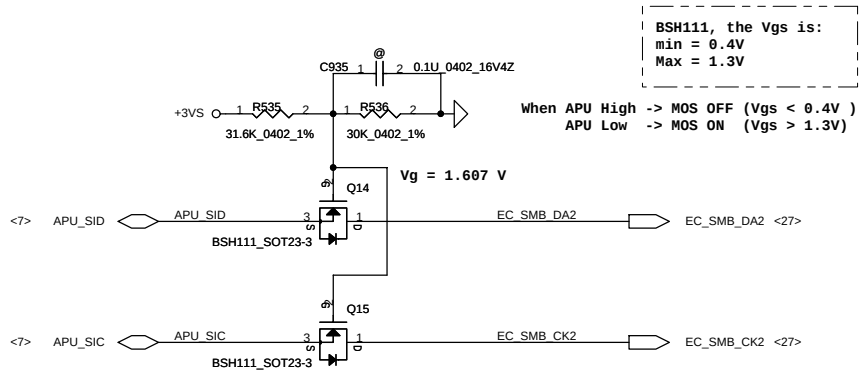
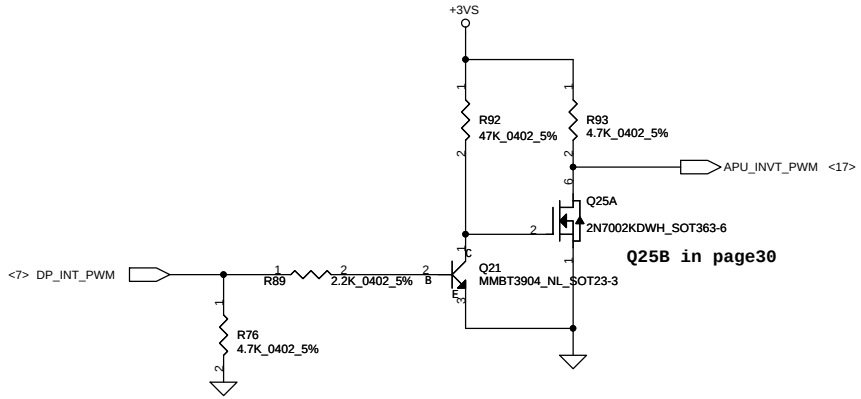
SB-TSI



Panel PWM



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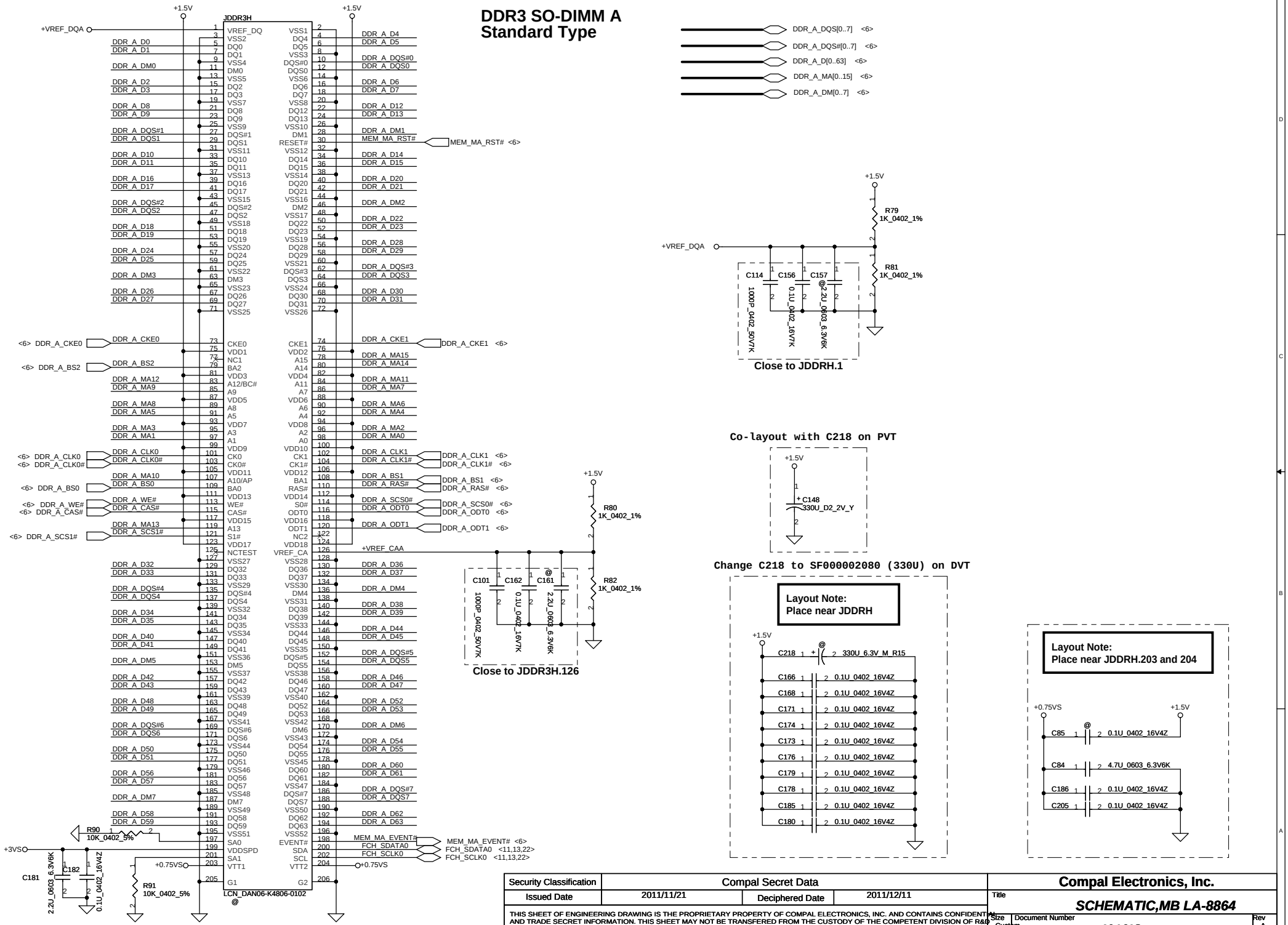
DDR3 SO-DIMM A
Standard Type



DDR_A_DQS[0..7] <6>
DDR_A_DQS#[0..7] <6>
DDR_A_D[0..63] <6>
DDR_A_MA[0..15] <6>
DDR_A_DM[0..7] <6>

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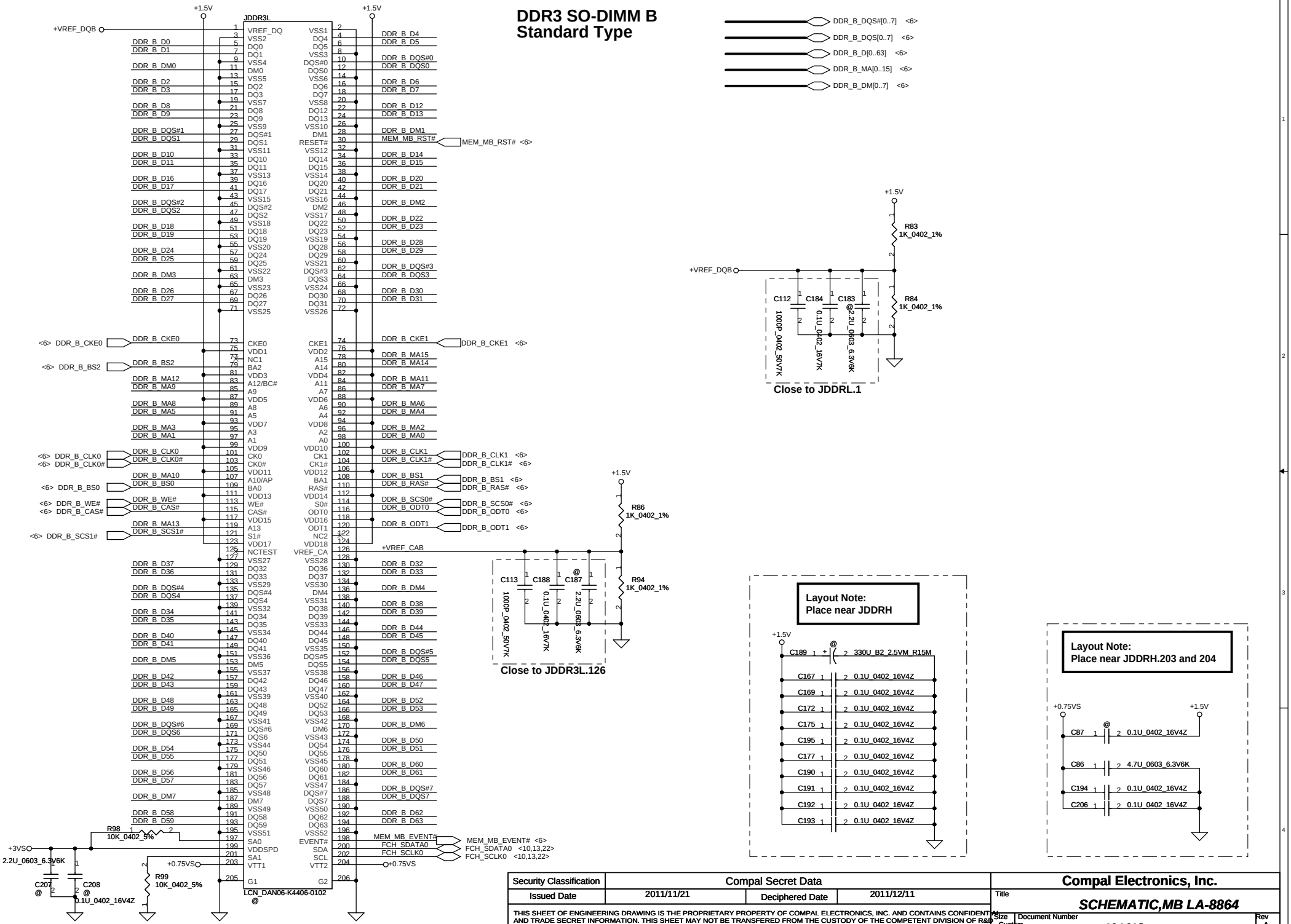
DDR3 SO-DIMM B
Standard Type



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U1A

HUDM3R3@

HUDSON-2

HUDSON-M3_FCBGA656

PCI EXPRESS INTERFACES

PCI INTERFACE

CLOCK GENERATOR

PCI CLKS

LPC

APU

S5 PLUIS

PCIE_RST# is for PCIE devices on APU

A_RST# is for LPC devices

Input from external clock generator
NC for internal clock generator

SS

APU Display

NSS

APU

SS

WLAN

LAN

SS

Place close to Y2

Place close to Y1

Strap

Strap

Strap

Strap

Function	GPIO30	GPIO31
PowerXpress	0	0
Reserved	0	1
Discrete	1	0
UMA	1	1

If use GCLK, please delete D14

DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.

S5_CORE_EN is for S5+ mode used to turn off +1.1VALW and +3VALW of FCH on S5+ mode

Update RTC schematic on PVT

CMOS Setting
Place under DDR Door

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PCIE_RST2# is for PCIE devices on FCH

U1D

HUDSON-2

HUDM3R3@

SM Bus 0-->S0 PWR domain
SM Bus 1-->S5 PWR domain
(for ASF device only)

USB_OC1# is for left USB3.0 ports
USB_OC0# is for right USB2.0 ports

Internal Pull-up ?

SM Bus 2-->S5 PWR domain
SM Bus 3-->APU_VDDIO domain for SB-TSI

Strap

Place R425 and C363 close to FCH for ESD

For FCH internal debug use (Internal 10K pull-down)

HUDSON-M3_FCBGA656

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HDD

14" ODD

15"/17" ODD

<21> SATA_FTX_DRX_P0
<21> SATA_FTX_DRX_N0
<21> SATA_FTX_DRX_N0
<21> SATA_FRX_C_DTX_P0
<21> SATA_FTX_DRX_P1
<21> SATA_FTX_DRX_N1
<21> SATA_FRX_C_DTX_N1
<21> SATA_FRX_C_DTX_P1
<21> SATA_FTX_DRX_P2
<21> SATA_FTX_DRX_N2
<21> SATA_FRX_C_DTX_N2
<21> SATA_FRX_C_DTX_P2

SATA_FTX_DRX_P0 AK19 SATA_TX0P
SATA_FTX_DRX_N0 AM19 SATA_TX0N
SATA_FRX_C_DTX_N0 AL20 SATA_RX0N
SATA_FRX_C_DTX_P0 AN20 SATA_RX0P
SATA_FTX_DRX_P1 AN22 SATA_TX1P
SATA_FTX_DRX_N1 AL22 SATA_TX1N
SATA_FRX_C_DTX_N1 AH20 SATA_RX1N
SATA_FRX_C_DTX_P1 AJ20 SATA_RX1P
SATA_FTX_DRX_P2 AJ22 SATA_TX2P
SATA_FTX_DRX_N2 AH22 SATA_TX2N
SATA_FRX_C_DTX_N2 AM23 SATA_RX2N
SATA_FRX_C_DTX_P2 AK23 SATA_RX2P
AH24 SATA_TX3P
AJ24 SATA_TX3N
AN24 SATA_RX3N
AL24 SATA_RX3P
AL26 SATA_TX4P
AN26 SATA_TX4N
AJ26 SATA_RX4N
AH26 SATA_RX4P
AN29 SATA_TX5P
AL28 SATA_TX5N
AK27 SATA_RX5N
AM27 SATA_RX5P
AL29 NC6
AN31 NC7
AL31 NC8
AL33 NC9
AH33 NC10
AH31 NC11
AJ33 NC12
AJ31 NC13

SERIAL ATA

U1B HUDM3R3@

HUDSON-2

SD_CLK/SCLK_2/GPIO73 AL14
SD_CMD/SLOAD_2/GPIO74 AN14
SD_CD/GPIO75 AJ12
SD_WP/GPIO76 AH12
SD_DATA0/SDATI_2/GPIO77 AK13
SD_DATA1/SDATO_2/GPIO78 AM13
SD_DATA2/GPIO79 AH15
SD_DATA3/GPIO80 AJ14

SD CARD

HDMI_EN# 2 R443 1K_0402_1% 1

Need HDMI_EN# Strap ?

HDMI_EN# (Internal 8.2K PU)

HDMI_EN#	H	L
SKU	Non-HDMI SKU	HDMI SKU

GBE_COL AC4
GBE_CRS AD3
GBE_MDCK AD9
GBE_MDIO W10
GBE_RXCLK AB8
GBE_RXD3 AH7
GBE_RXD2 AE7
GBE_RXD1 AE7
GBE_RXD0 AD7
GBE_RXCTL/RXDV AG8
GBE_RXERR AD1
GBE_TXCLK AB7
GBE_TXD3 AF9
GBE_TXD2 AG6
GBE_TXD1 AE8
GBE_TXD0 AD8
GBE_TXCTL/TXEN AB9
GBE_PHY_PD AC2
GBE_PHY_RST# AA7
GBE_PHY_INTR W9 GBE_PHY_INTR 1 R352 10K_0402_5% 2 +3VALW_FCH

GBE LAN

SPI_DI/GPIO164 V6 FCH_SPI_MISO
SPI_DO/GPIO163 V5 FCH_SPI_MOSI
SPI_CLK/GPIO162 V3 FCH_SPI_CLK
SPI_CS1#/GPIO165 T6 FCH_SPI_CS1#
ROM_RST#/SPI_WP#/GPIO161 V1

SPI ROM

If an SPI ROM is shared between FCH and the Embedded Controller, a 10-k pull-up resistor to +3.3V_S5 is installed

+3VALW_FCH
FCH_SPI_CS1# 1 @ R113 10K_0402_5% 2

+3VS
UMA_CRT_DATA 1 R454 2.2K_0402_5% 2
UMA_CRT_CLK 1 R455 2.2K_0402_5% 2

VGA_RED L30 UMA_CRT_R UMA_CRT_R <19>
VGA_GREEN L32 UMA_CRT_G UMA_CRT_G <19>
VGA_BLUE M29 UMA_CRT_B UMA_CRT_B <19>
VGA_HSYNC/GPO68 M28 UMA_CRT_HSYNC UMA_CRT_HSYNC <19>
VGA_VSYNC/GPO69 N30 UMA_CRT_VSYNC UMA_CRT_VSYNC <19>
VGA_DDC_SDA/GPO70 M33 UMA_CRT_DATA UMA_CRT_DATA <19>
VGA_DDC_SCL/GPO71 N32 UMA_CRT_CLK UMA_CRT_CLK <19>

VGA DAC

UMA_CRT_R 1 R367 150_0402_1% 2
UMA_CRT_G 1 R368 150_0402_1% 2
UMA_CRT_B 1 R369 150_0402_1% 2

VGA_DAC_RSET K31 VGA_DAC_RSET 1 R366 715_0402_1% 2

AUX_VGA_CH_P V28 ML_VGA_AUXP ML_VGA_AUXP <7>
AUX_VGA_CH_N V29 ML_VGA_AUXN ML_VGA_AUXN <7>
AUXCAL U28 AUXCAL 1 R364 100_0402_1% 2 +VDDAN_11_ML

ML_VGA_L0P T31 ML_VGA_TXP0 ML_VGA_TXP0 <7>
ML_VGA_L0N T33 ML_VGA_TXN0 ML_VGA_TXN0 <7>
ML_VGA_L1P T29 ML_VGA_TXP1 ML_VGA_TXP1 <7>
ML_VGA_L1N T28 ML_VGA_TXN1 ML_VGA_TXN1 <7>
ML_VGA_L2P R32 ML_VGA_TXP2 ML_VGA_TXP2 <7>
ML_VGA_L2N R30 ML_VGA_TXN2 ML_VGA_TXN2 <7>
ML_VGA_L3P P29 ML_VGA_TXP3 ML_VGA_TXP3 <7>
ML_VGA_L3N P28 ML_VGA_TXN3 ML_VGA_TXN3 <7>

VGA MAINLINK

+FCH_VDDAN_33_DAC_R
FCH_CRT_HPD 1 R365 10K_0402_5% 2

ML_VGA_HPD/GPIO229 C29 FCH_CRT_HPD FCH_CRT_HPD <7>

+5VS
R444 10K_0402_5% SATA_LED#
R446 20K_0402_5%

To avoid LED flashing

+AVDD_SATA
R336 1K_0402_1% SATA_CALRP AE28 SATA_CALRP
R130 931_0402_1% SATA_CALRN AE27 SATA_CALRN

<29> SATA_LED# AD22 SATA_ACT#/GPIO67

AE21 SATA_X1

AG21 SATA_X2

+3VS
R147 10K_0402_5%
<21> ODD_SEL ODD_SEL AH16 FANOUT0/GPIO52
AM15 FANOUT1/GPIO53
AJ16 FANOUT2/GPIO54

ODD_SEL	SATA port	SKU
High	Port 1	14"
Low	Port 2	15"/17"

T16 AK15 FANIN0/GPIO56
AN16 FANIN1/GPIO57
AL16 FANIN2/GPIO58

<30> ODD_PWR ODD_PWR K6 TEMPIN0/GPIO171
R111 10K_0402_5% K5 TEMPIN1/GPIO172
R103 10K_0402_5% K3 TEMPIN2/GPIO173
FCH_ALERT# M6 TEMPIN3/TALERT#/GPIO174

HW MONITOR

VIN0/GPIO175 N2 R101 10K_0402_5%
VIN1/GPIO176 M3 R102 10K_0402_5%
VIN2/SDATI_1/GPIO177 L2 R105 10K_0402_5%
VIN3/SDATO_1/GPIO178 N4 R106 10K_0402_5%
VIN4/SLOAD_1/GPIO179 P1 R128 10K_0402_5%
VIN5/SCLK_1/GPIO180 P3 SLP_CHG#1 R126 10K_0402_5%
VIN6/GBE_STAT3/GPIO181 M1 R115 10K_0402_5%
VIN7/GBE_LED3/GPIO182 M5 R114 10K_0402_5%

Enable integrated pull-down/up and leave unconnected

<24> SLP_CHG# SLP_CHG# 1 @ R134 10K_0402_5% 2 +3VALW_FCH

NC1 AG16
NC2 AH10
NC3 A28
NC4 G27
NC5 L4

HUDSON-M3_FCBGA656

4M Byte

U13
FCH_SPI_CS1# 1 CS# VCC 8
FCH_SPI_MISO 2 SO/SIO1 HOLD# 7
+3VALW_FCH 3 WP# SCLK 6 FCH_SPI_CLK
4 GND SI/SIO0 5 FCH_SPI_MOSI
W25Q32BVSSIG_SO8

+3VALW_FCH
C498 1 2 0.1U_0402_16V4Z

For EMI

FCH_SPI_CLK
@ R402 10_0402_5%
@ C257 10P_0402_50V8J

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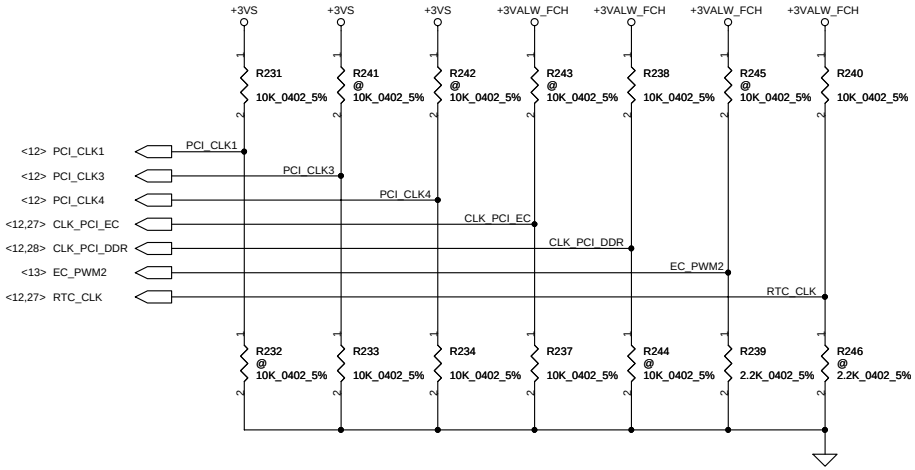
STRAP PINS

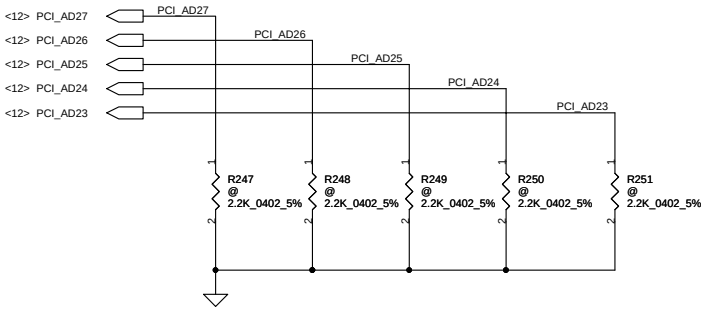
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	ENABLE DEBUG STRAP	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM (INTERNAL 10K PULL-UP)	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	DISABLE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



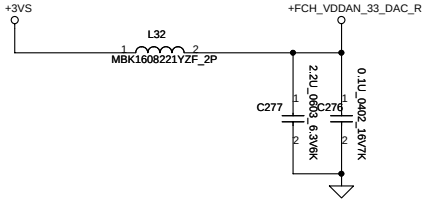
DEBUG STRAPS

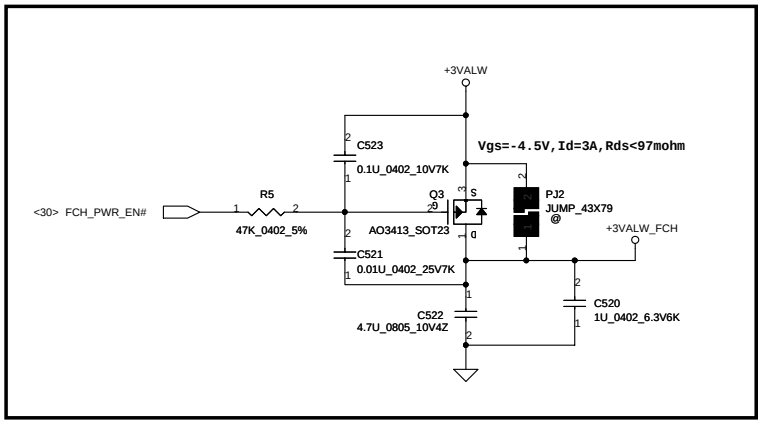
FCH HAS 15K INTERNAL PU-UP FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



CRT Power Down Circuit





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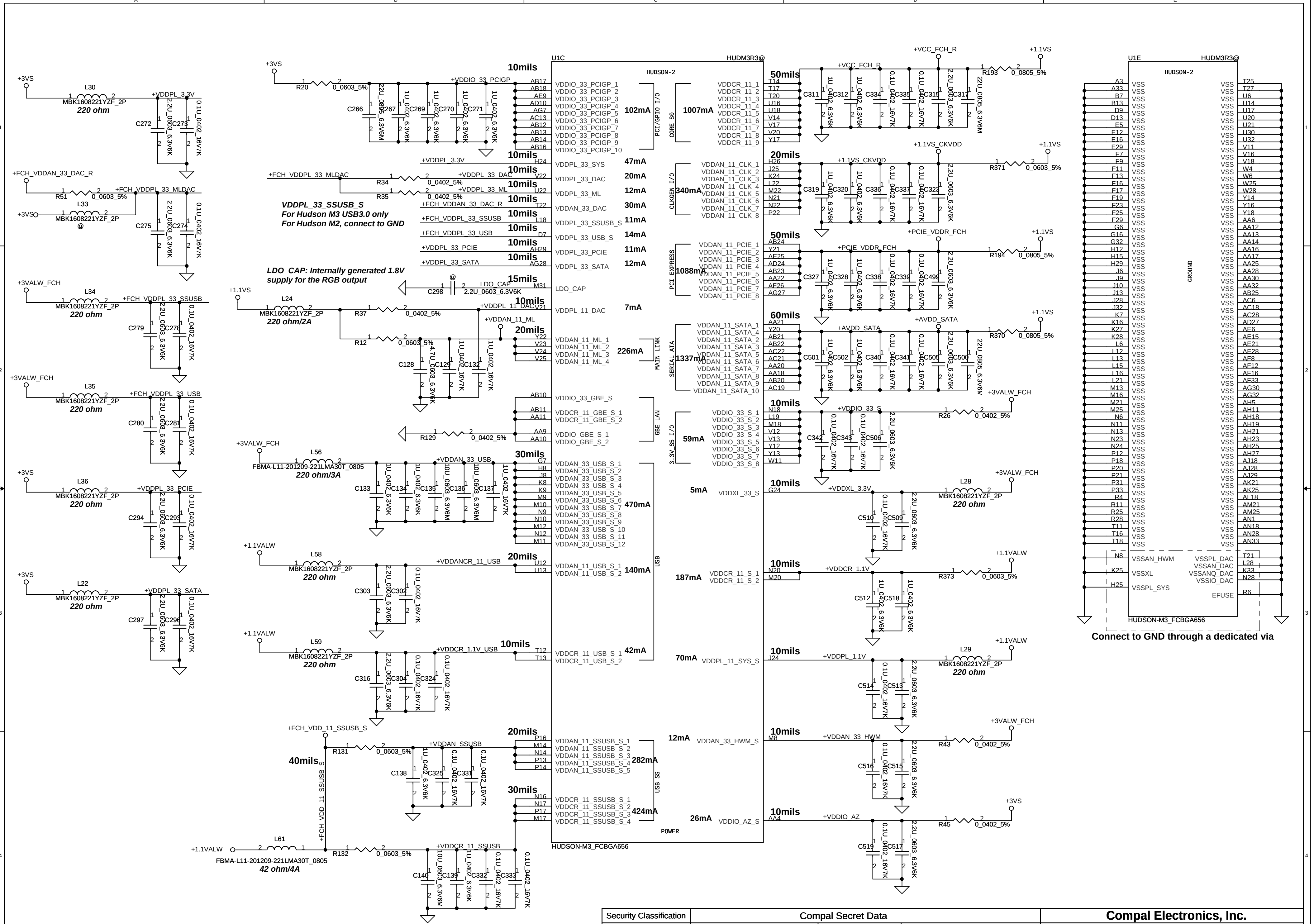

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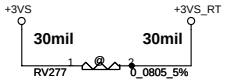
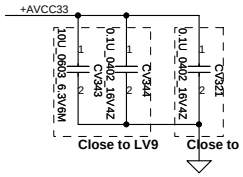
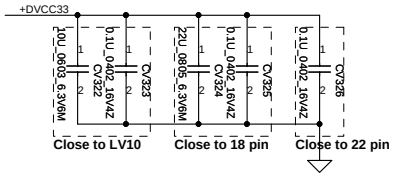
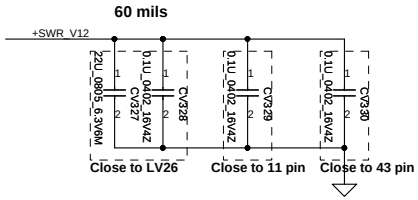
Power Consumption:

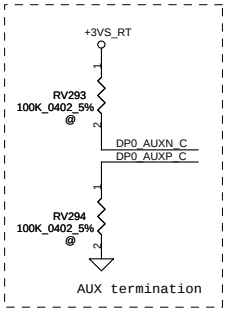
Pin5 (DPV33) < 20mA
Pin 11 (DPV12) < 100mA
Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
Pin 22 (PVCC) < 50 mA
Pin 43 (VCCK) < 50mA

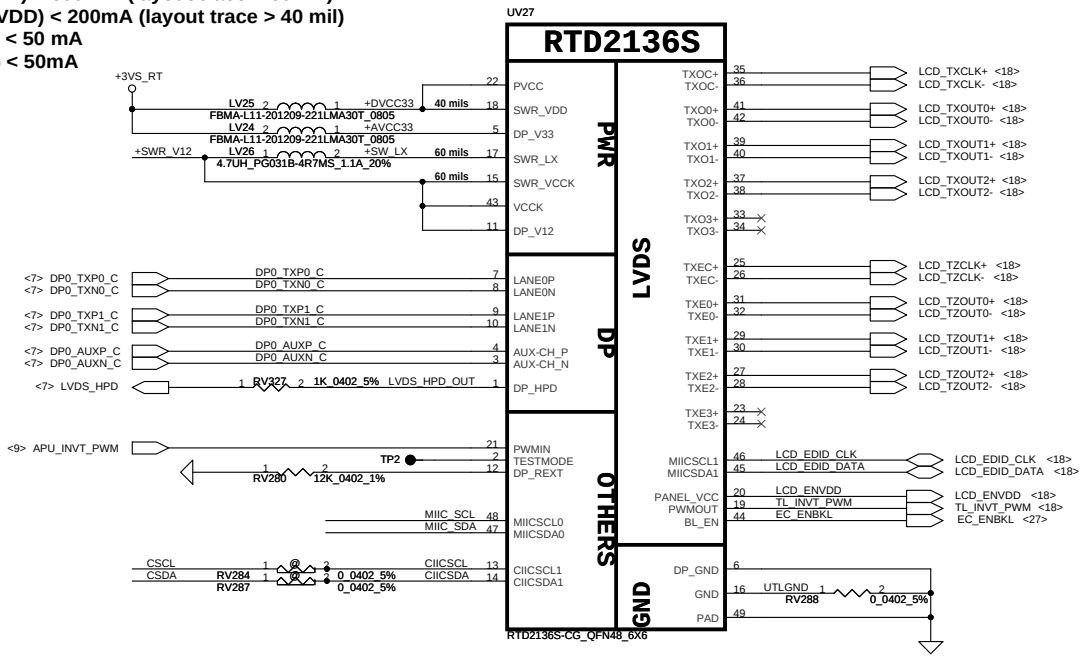


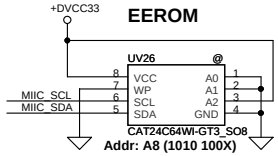


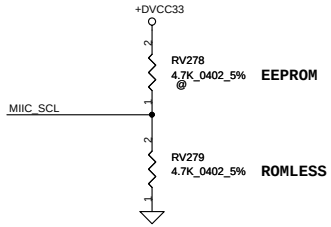


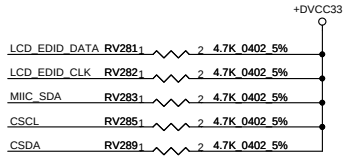


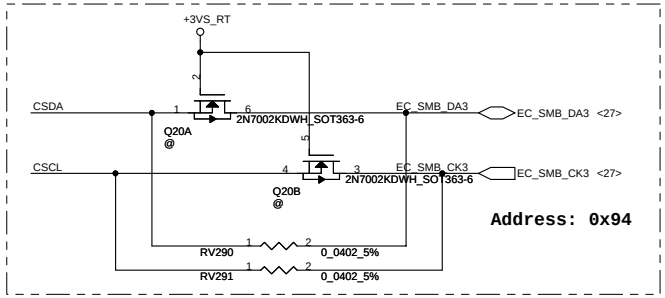


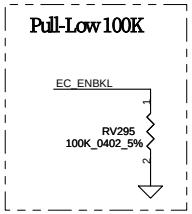












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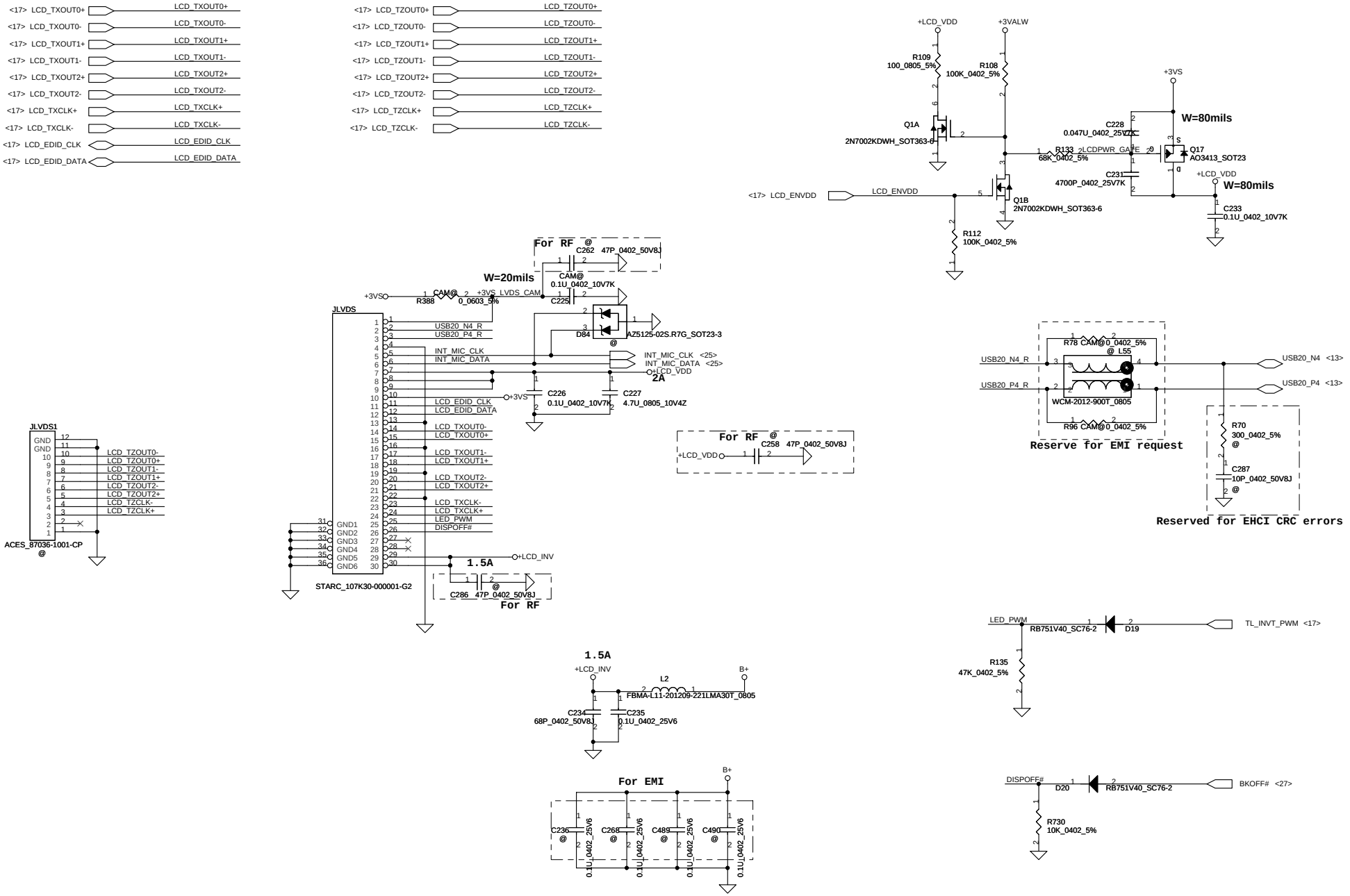

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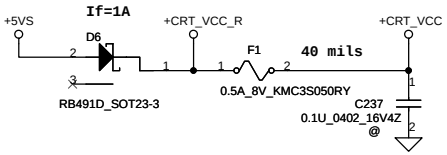
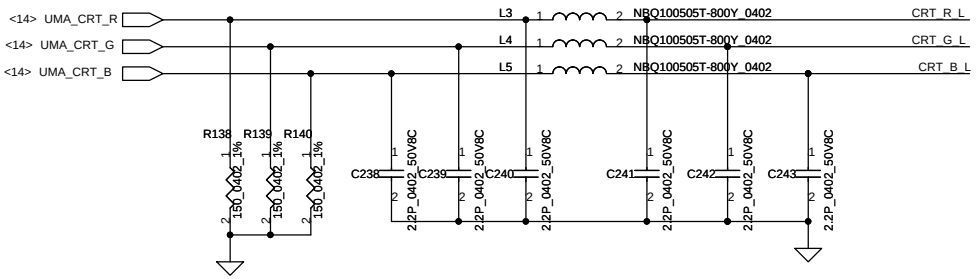
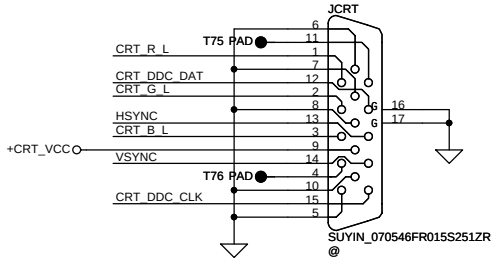
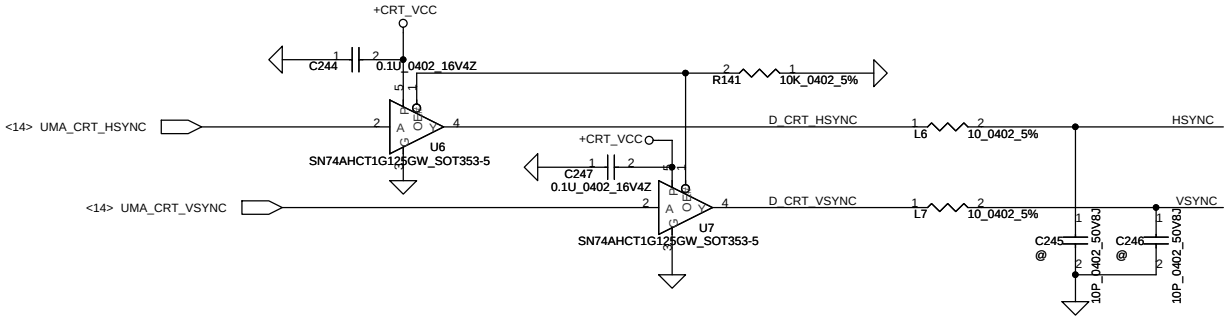
CRT CONNECTOR

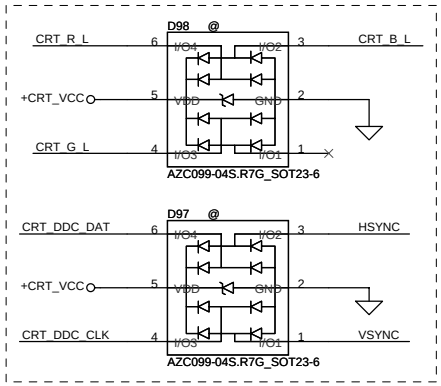


Remove D3~D5 on DVT

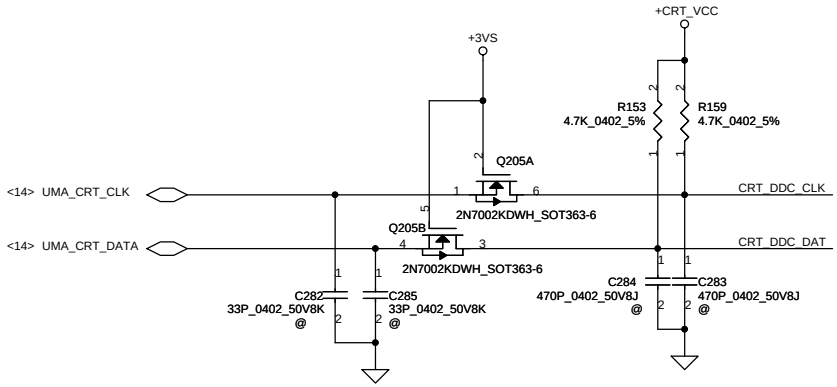








Reserve ESD for CRT connector on DVT



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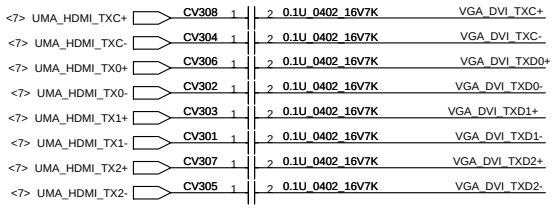
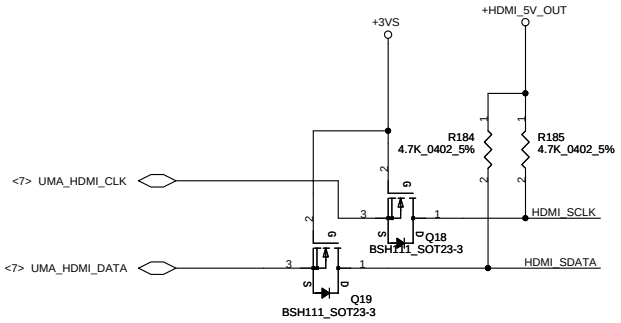
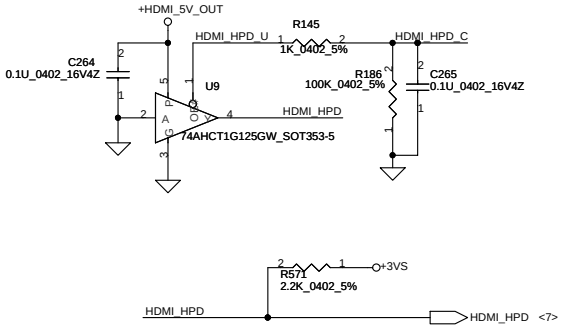
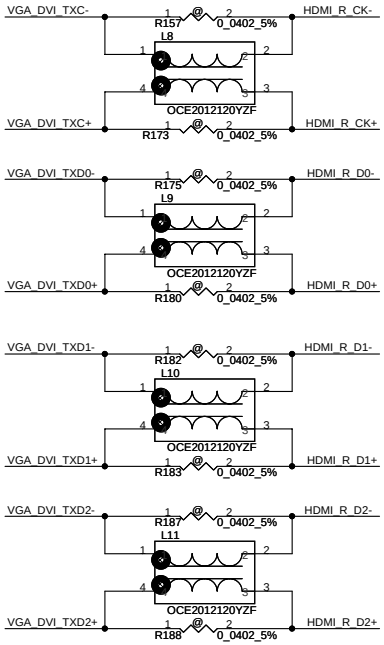
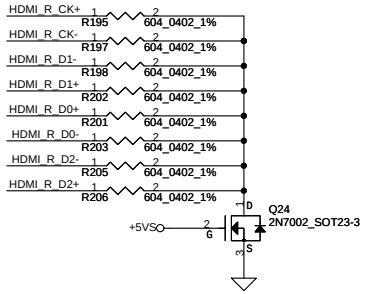
Change R184 and R185 from 2K to 4.7K for HDMI detect issue on preMP



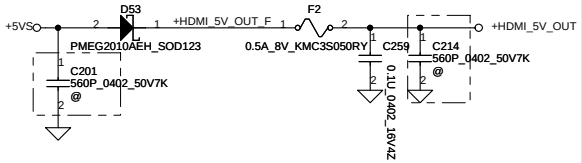


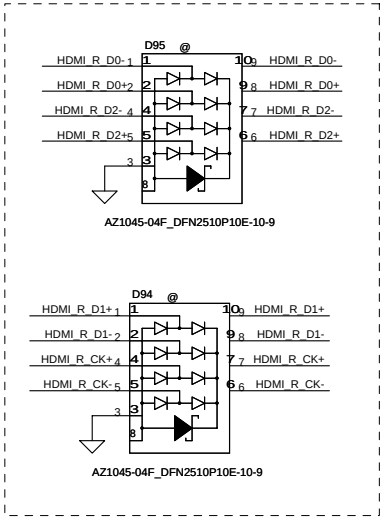


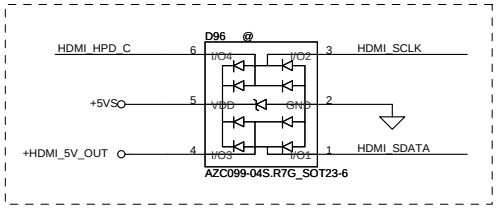




Add C201 and C214 for EMI request on PVT

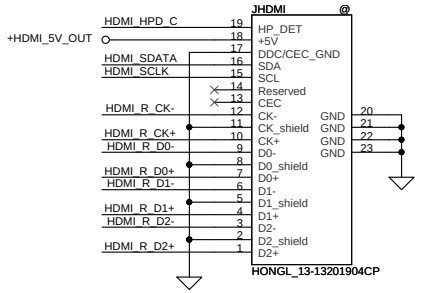






Reserve ESD for HDMI conn. on DVT

HDMI Connector



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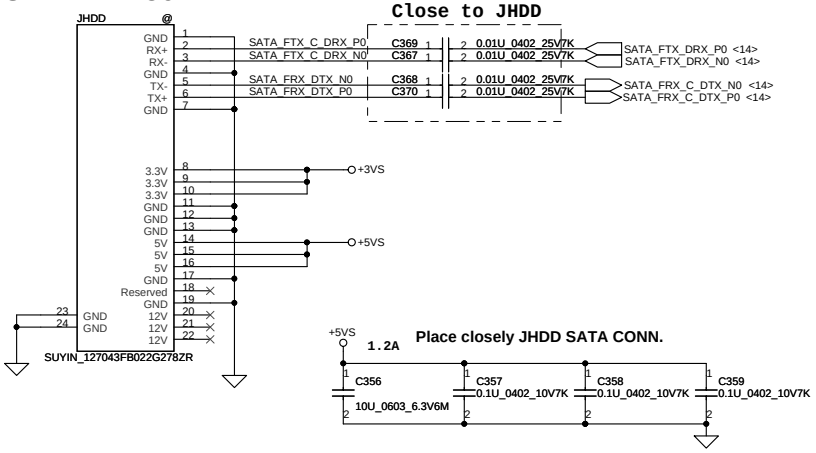
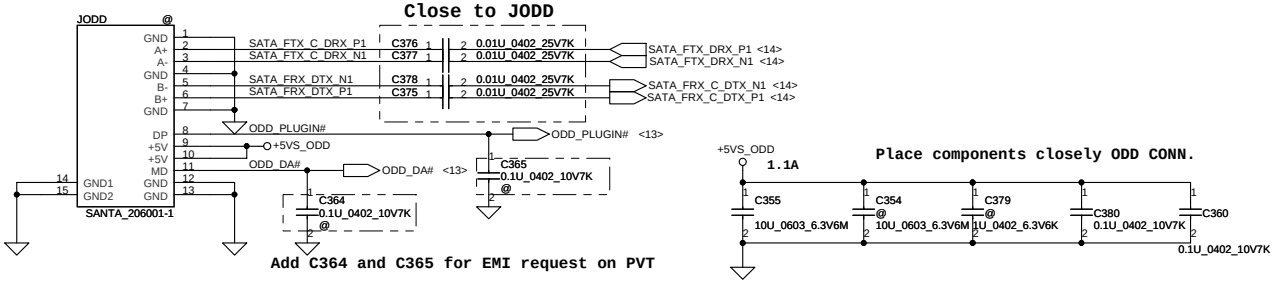
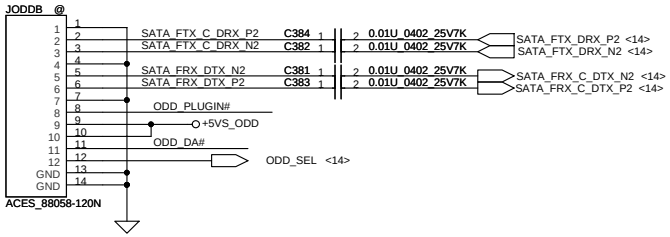
SATA HDD Conn.



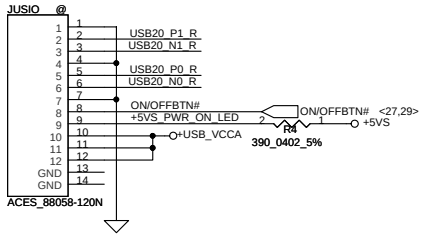
SATA ODD Conn (for 14")

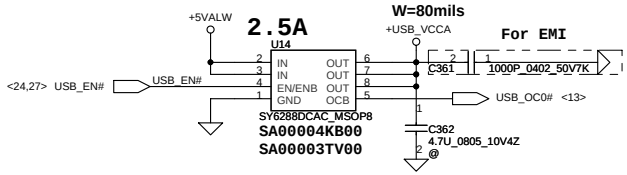


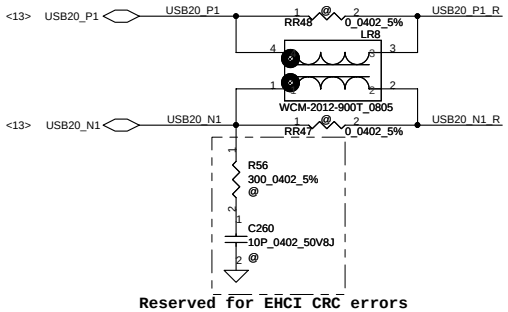
SATA ODD Conn (for 15"/17")

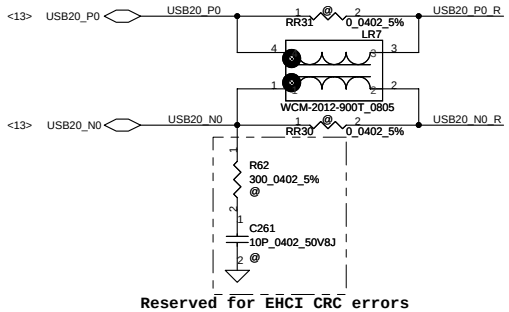


Power Button & RUSB connector









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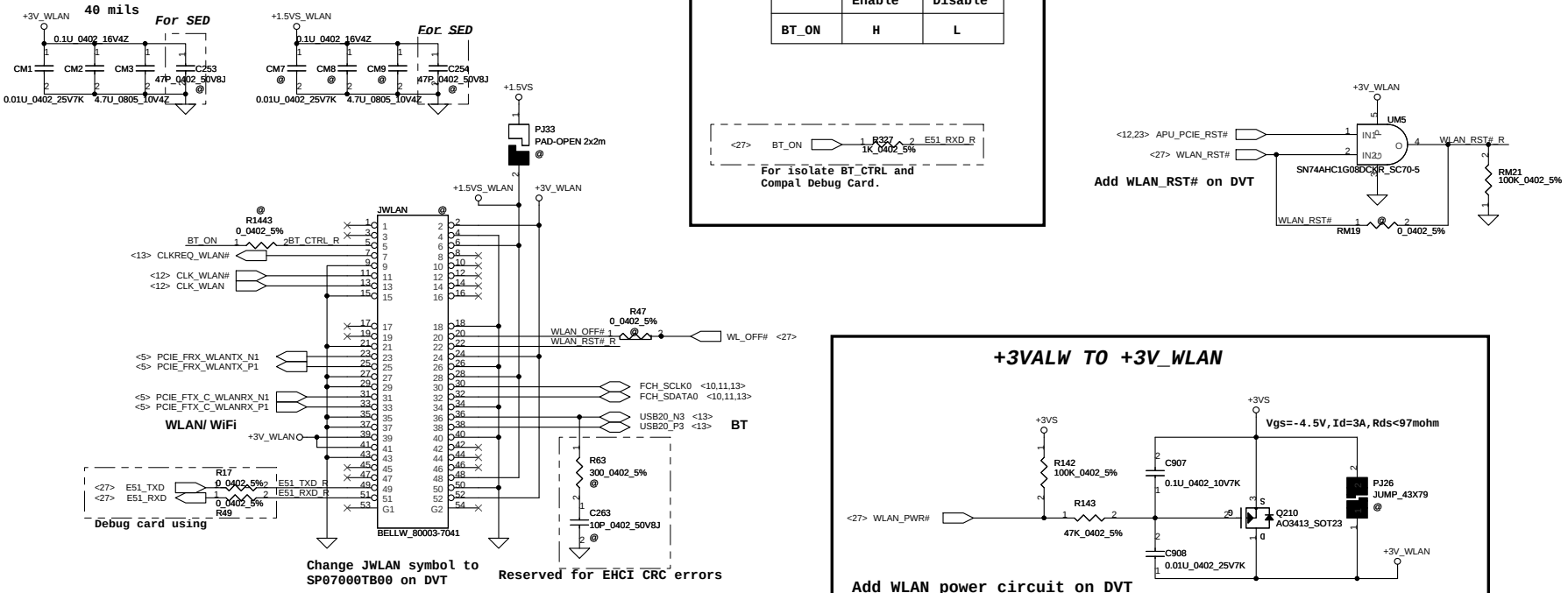
Slot 1 Half PCIe Mini Card-WLAN



WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON	H	L

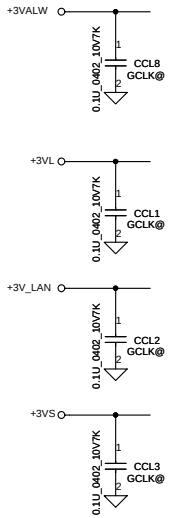
For isolate BT_CTRL and Compal Debug Card.

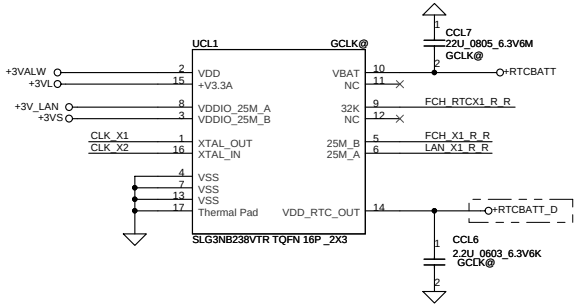
Add WLAN_RST# on DVT

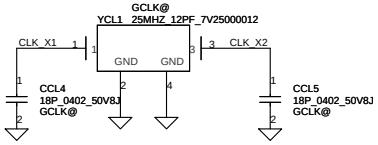
+3VALW TO +3V_WLAN

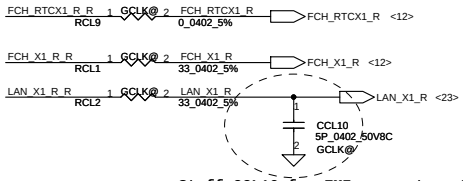
Add WLAN power circuit on DVT

Green Clock Generator

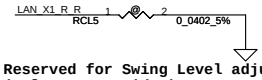








Stuff CCL10 for EMI request on DVT



Reserved for Swing Level adjustment
(Close GCLK side)

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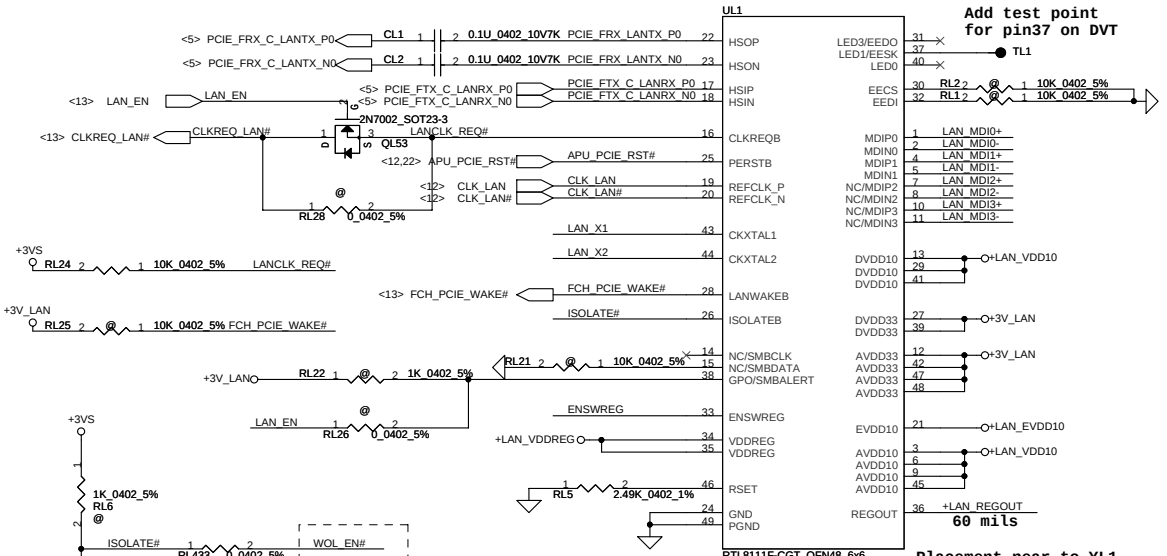


	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN#	LOW	HIGH	HIGH

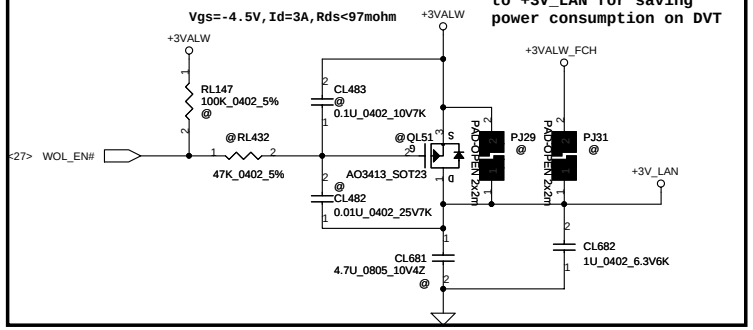
	RTL8105E	RTL8111E/F
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	NC	1K ohm PH

	8105E-VL/VD 8111F/F-VB PWM Mode	8105E-VL/VD LDO Mode
RL4	0 ohm (Pull High)	NC
RL23	NC	0 ohm (Pull Down)

+3VALW TO +3V_LAN

Vgs=-4.5V,Id=3A,Rds<97mohm

Reserve +3VALW_FCH to +3V_LAN for saving power consumption on DVT



NOGCLK@ YL1 25MHZ_20PF_7V25000016

CL26 27P_0402_50V8J NOGCLK@

CL27 27P_0402_50V8J NOGCLK@

+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

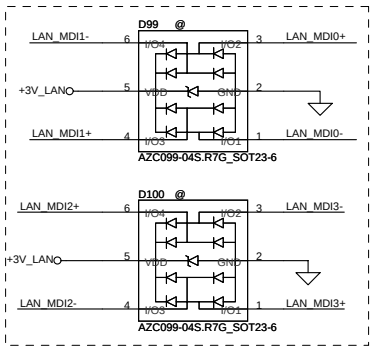
LAN	WOL	LAN_EN S0	LAN_EN Sx	ISOLATEB S0	ISOLATEB Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

*

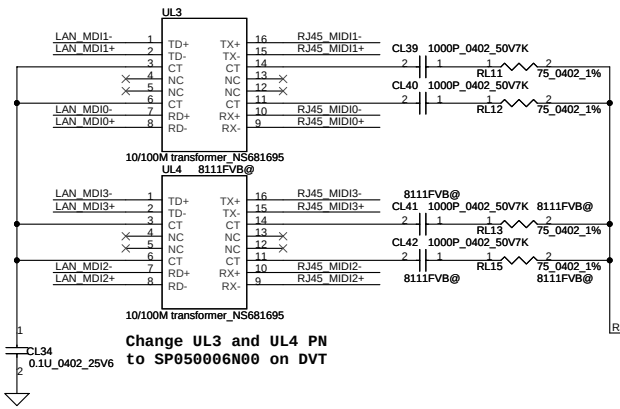
S3: after SUSP# assert low over 100ms

S4/S5: after SYSON assert low over 100ms

Reserve ESD for LAN on DVT

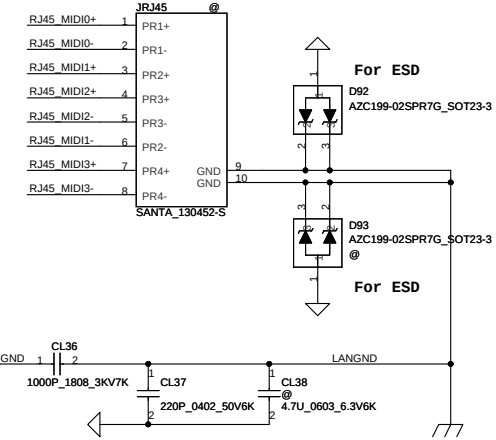


Swap MDI0 and MDI1 on DVT



Change UL3 and UL4 PN to SP050006N00 on DVT

LAN Conn.



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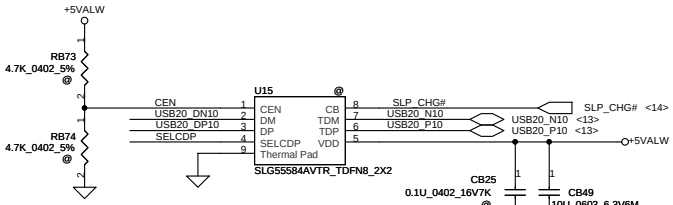
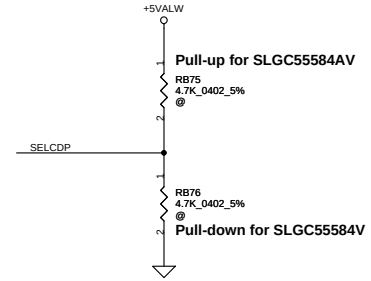
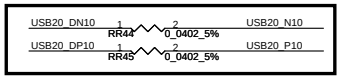
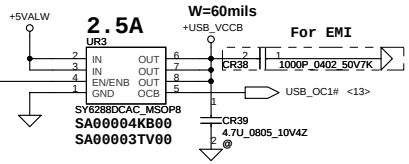
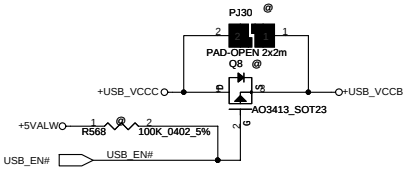


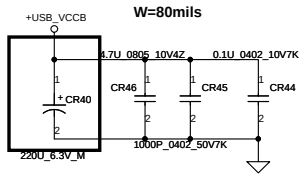




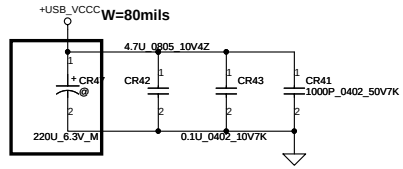
SLP_CHG#	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only

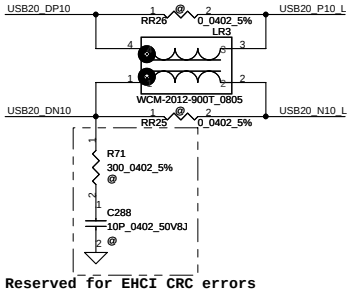




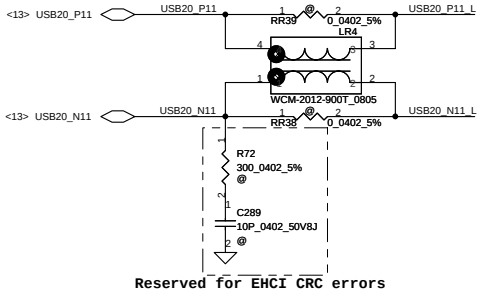


150uFx2 or 220uFx1





Reserved for EHCI CRC errors



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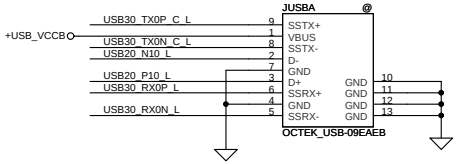

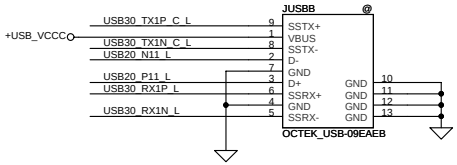

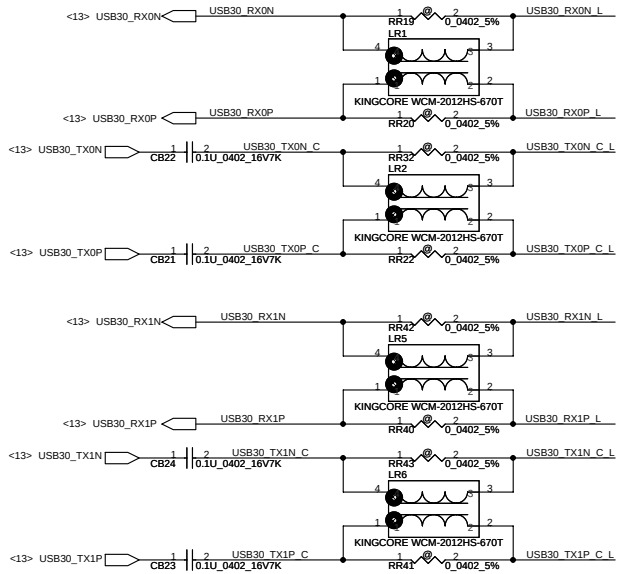

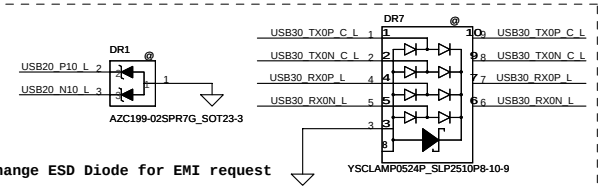

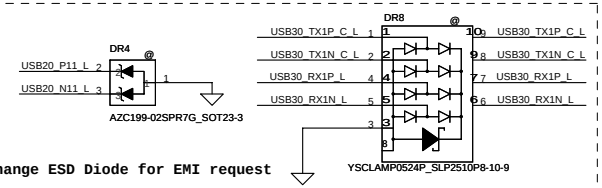

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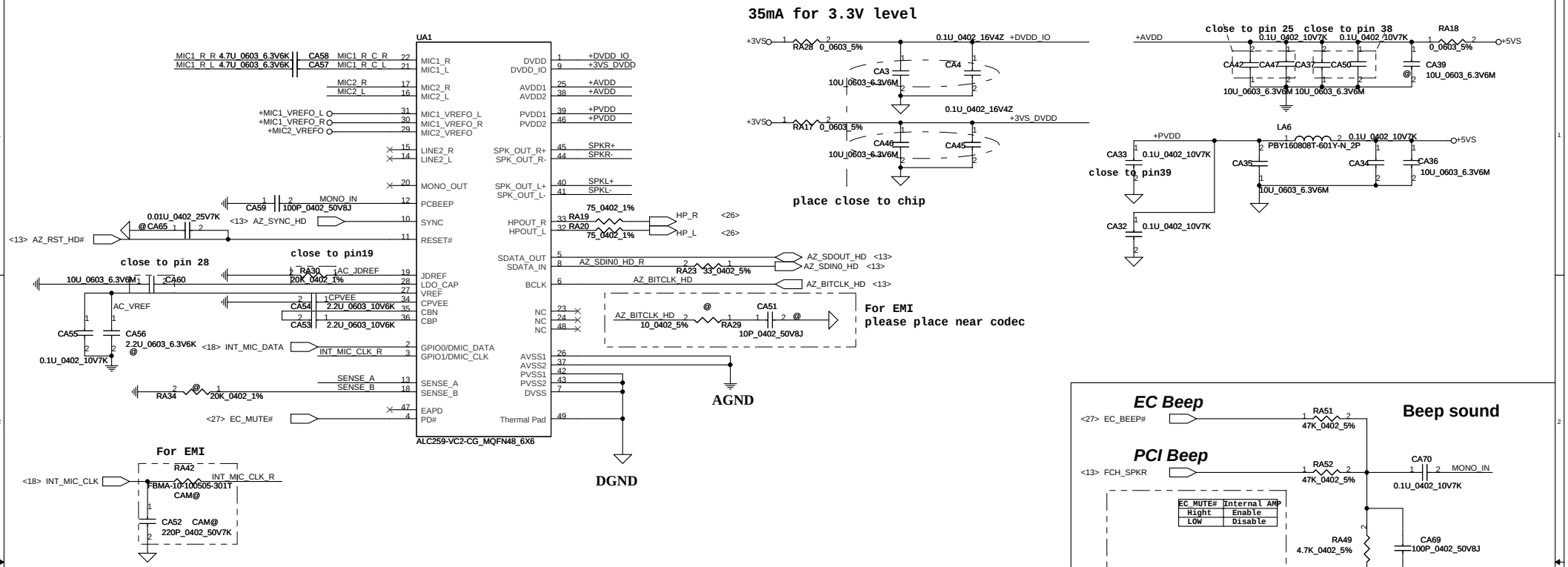
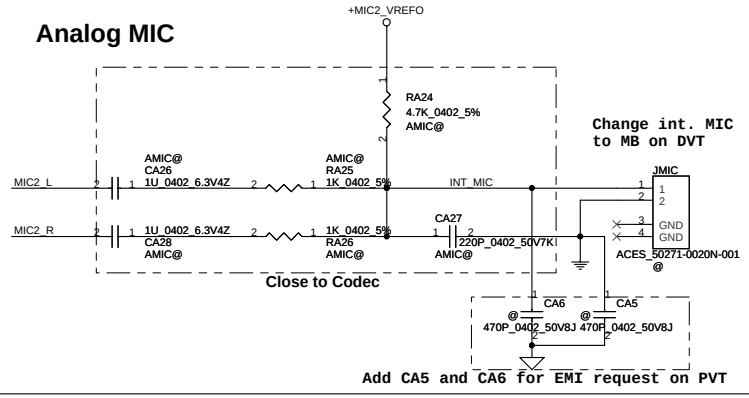
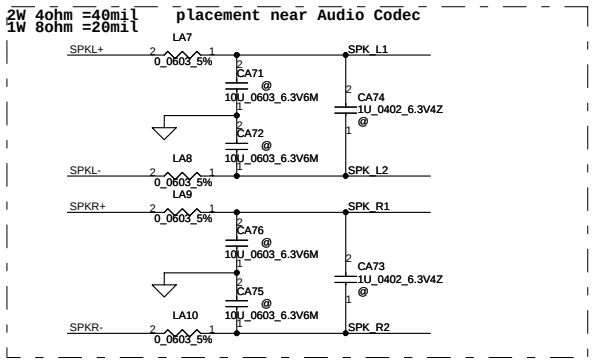
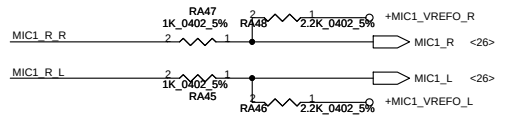
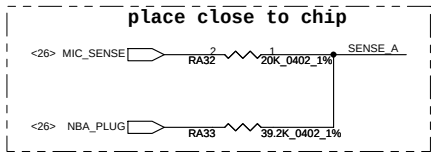


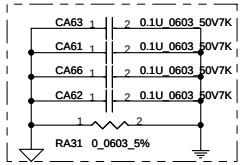


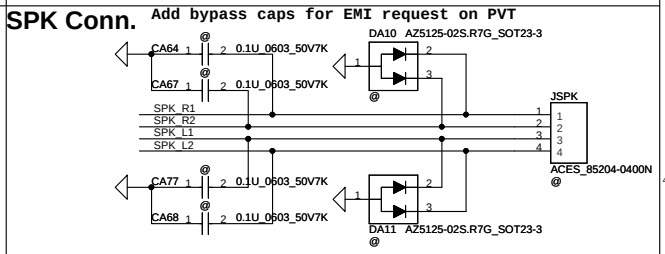




Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	







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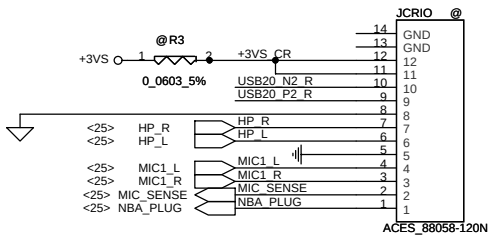
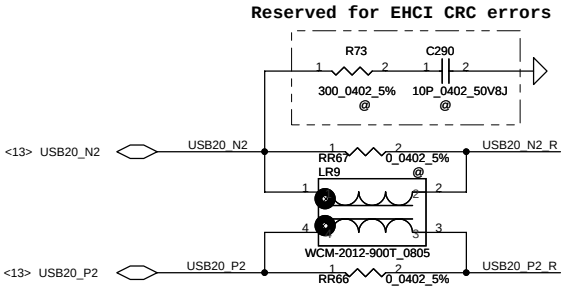
CardReader & Audio Conn.

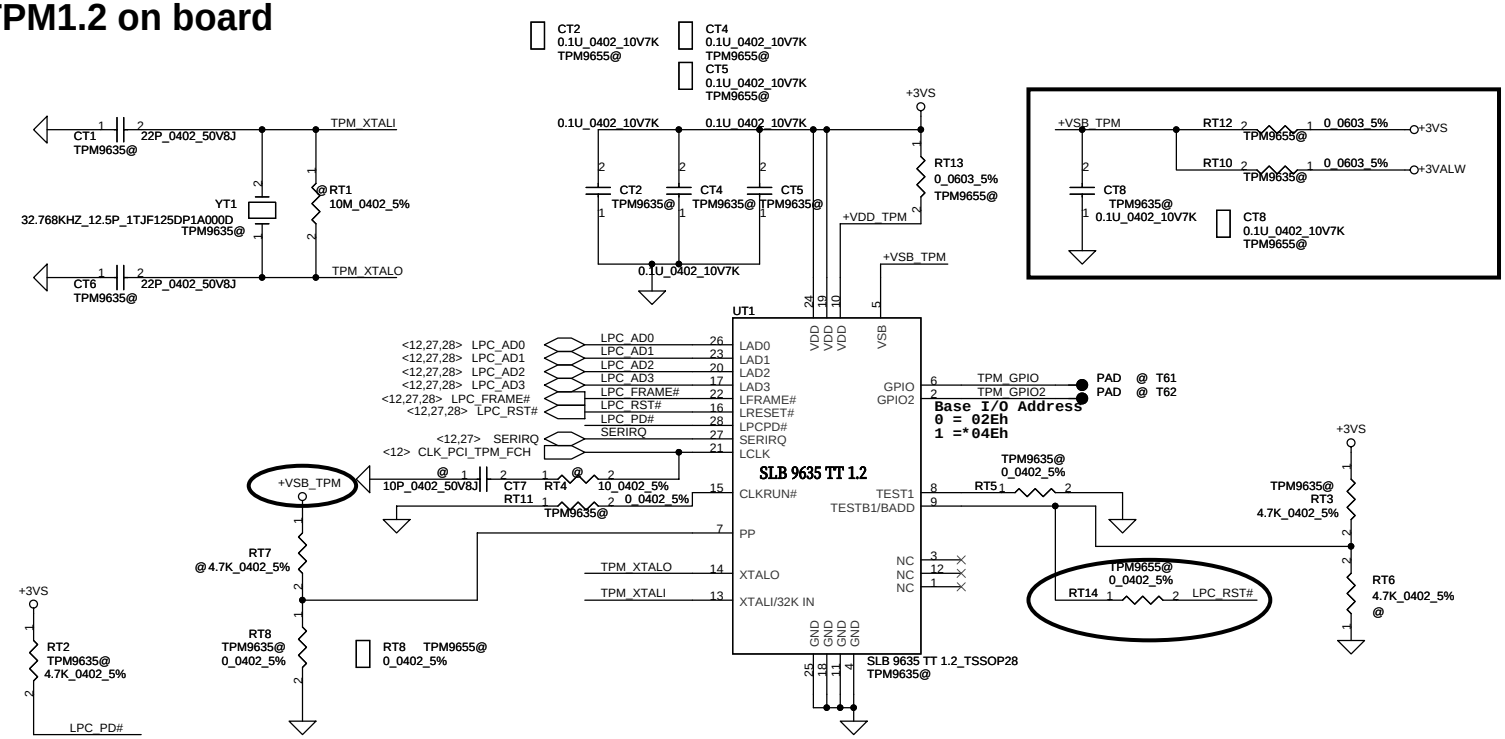


Update JCRIO pin definition on DVT

Reserved for EHCI CRC errors



TPM1.2 on board



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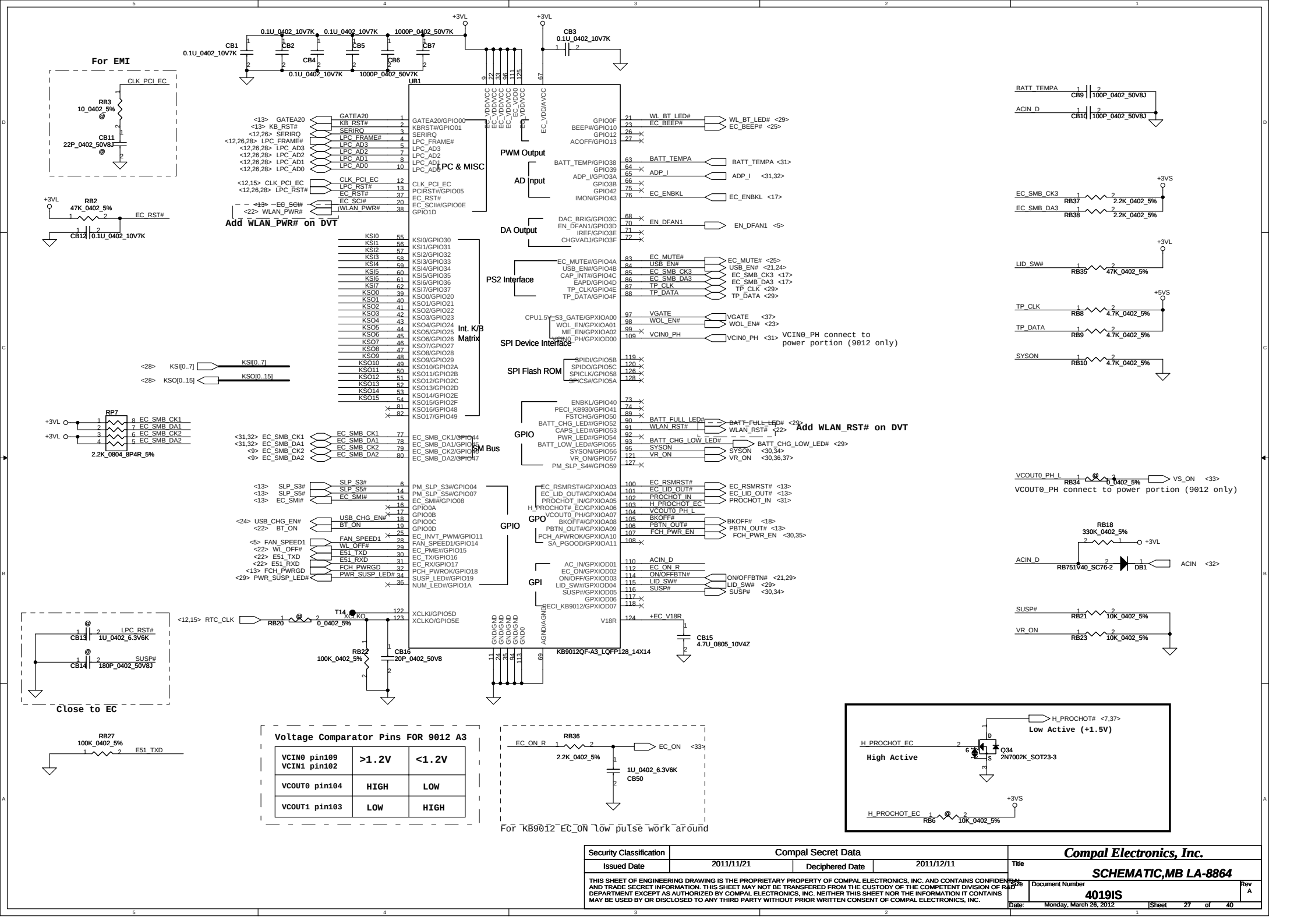

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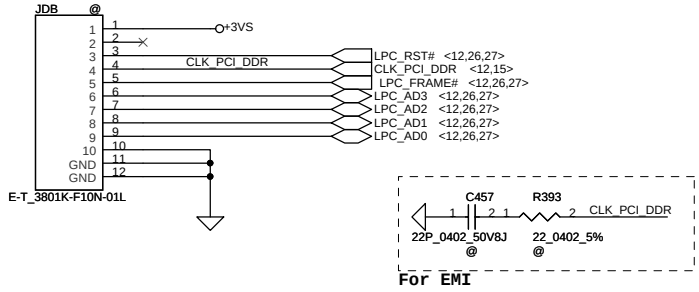
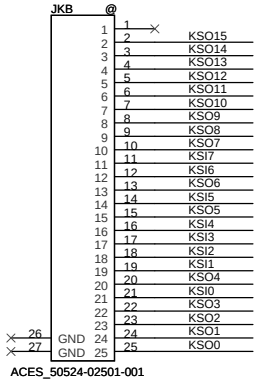
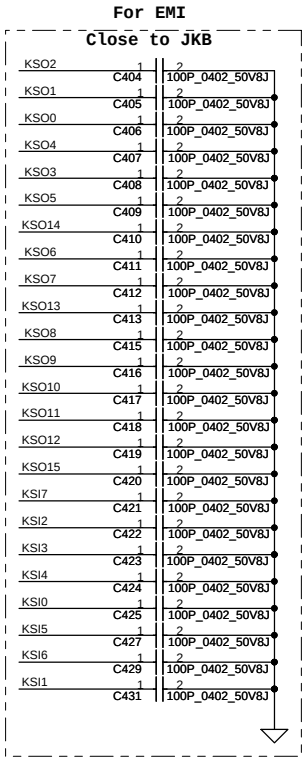
LPC Debug Port



KEYBOARD CONN.





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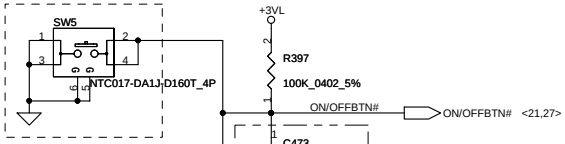
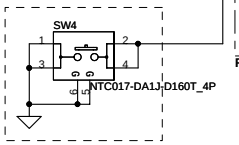
For debug

Place on TOP



For debug

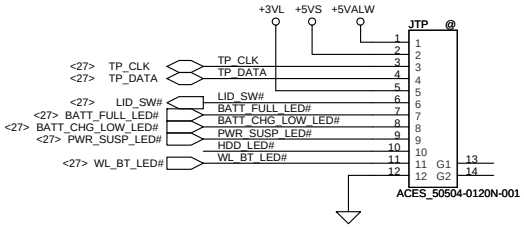
Place on BOT

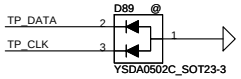


For EMI request

Touchpad Connector

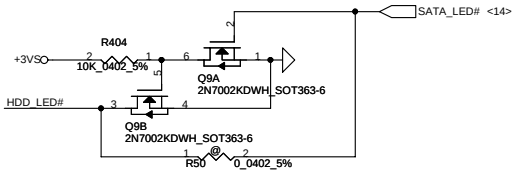
Change JTP symbol to SP01001BF10 on DVT





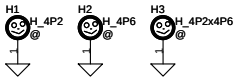
Place close to JTP

HDD LED

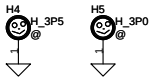


Screw Hole

CPU

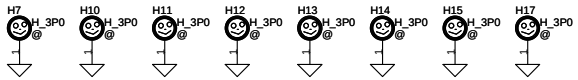


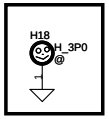
VGA



FCH

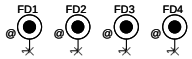
PTH





NPTH

PCB Fedical Mark PAD



ISPD

U1 HUDM3R1@

SA000043IN0

218-0755097 A14 HUDSON-M3

ZZZ

DA60000T800

PCB LA-8864P

U1 HUDM3UNBW@

SA000043I00

218-0755097 A14 HUDSON-M3

PJP1 45@

CONN SET 0CL DCJACK-MB 322215-3

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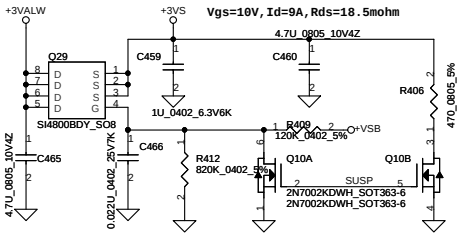
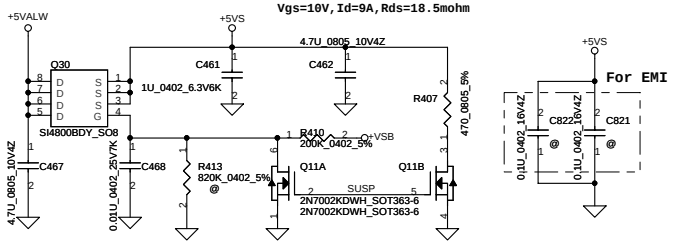
+3VALW TO +3VS

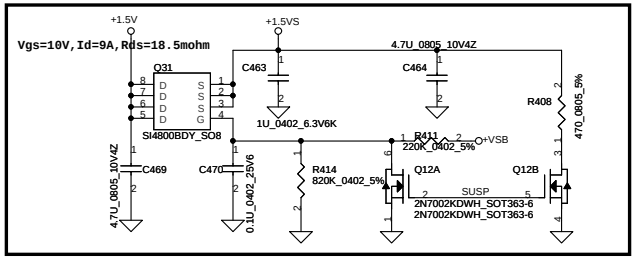


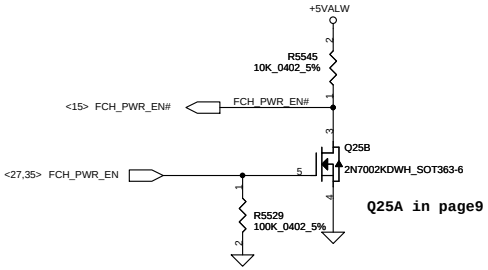
+5VALW TO +5VS

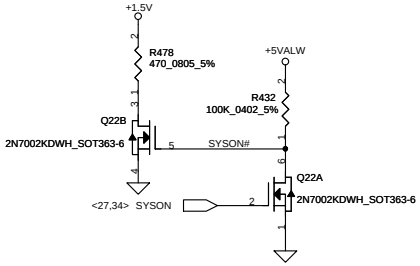


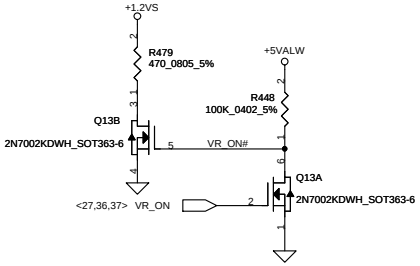
+1.5V to +1.5VS

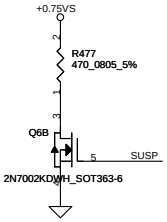
Change +1.5VS MOS to Smaller Current ?

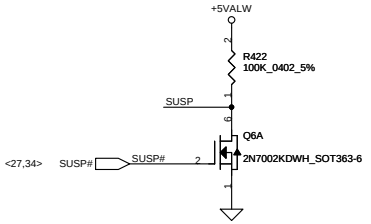




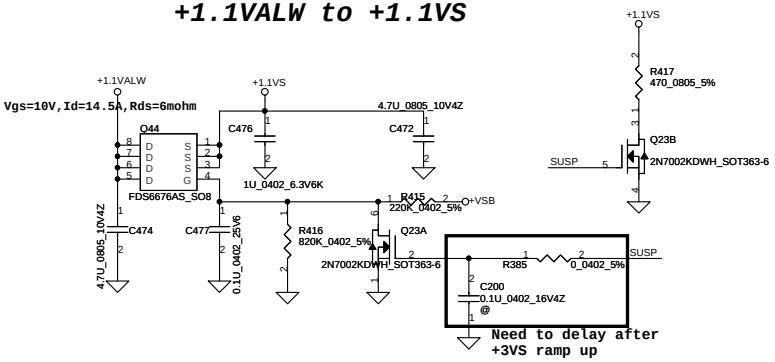




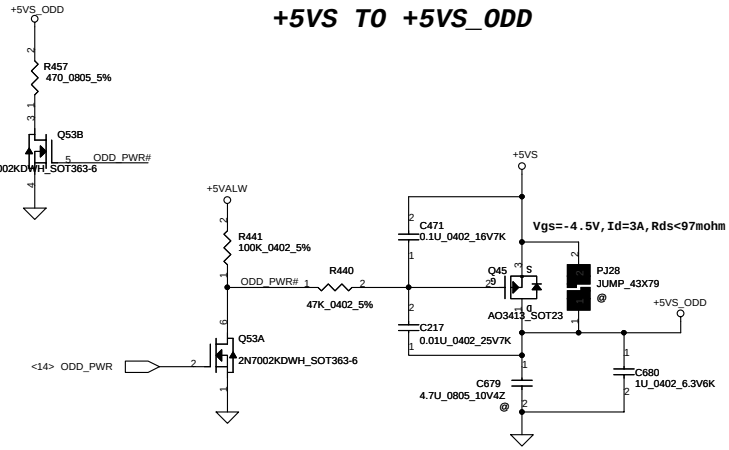




+1.1VALW to +1.1VS



+5VS TO +5VS_ODD



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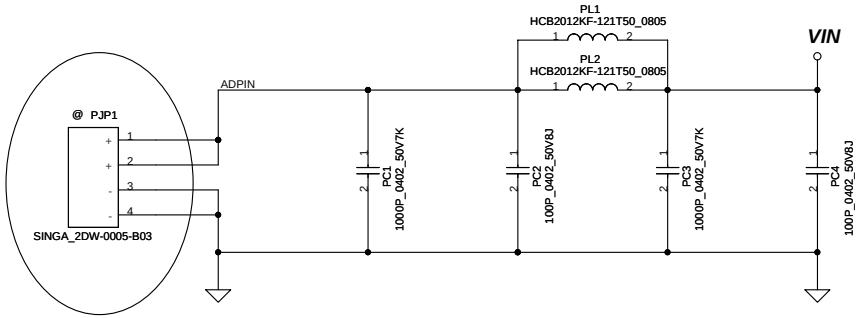
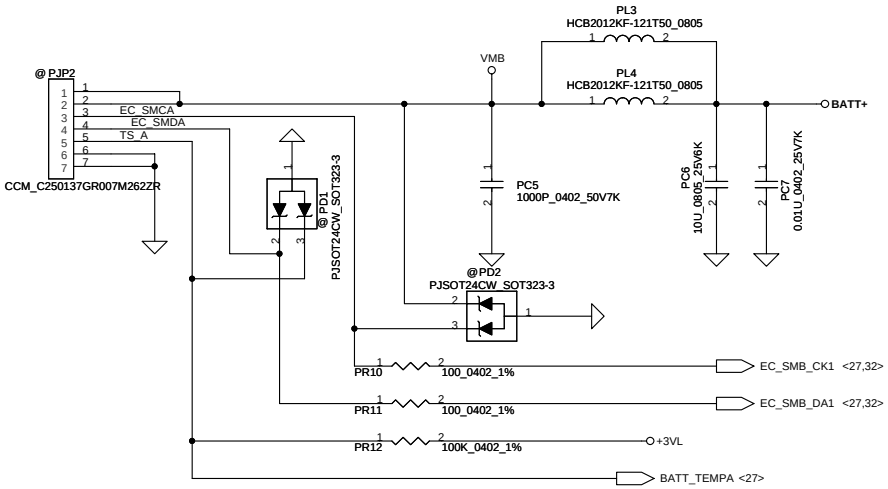
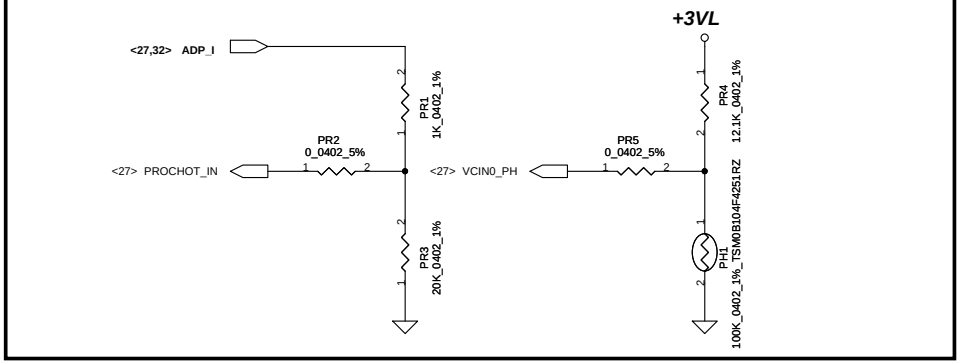
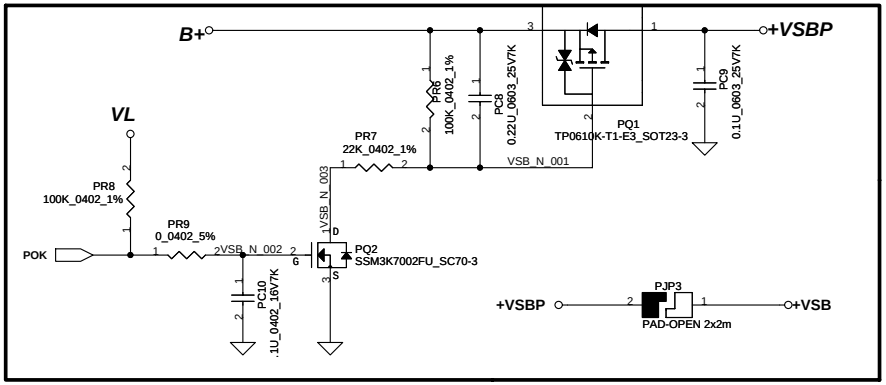


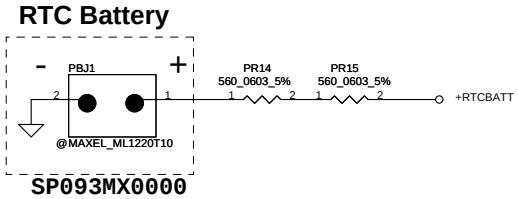


PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

Please locate these parts
Near EC chip







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for reverse input protection

PQ209 SI1304BDL-T1-E3_SC70-3
PR225 1M_0402_5%
PR226 3M_0402_5%

VIN
PQ203 TPCA8057-H_PPAK56-8-5
PC230 2200P_0402_50V7K
PR231 @ 0_0402_5%
PC231 0.1U_0402_25V6
P1
PQ205 DMG4406LSS_SO8
P2
BQ24725_ACDRV_1

PR211 0.01_1206_1%
B+
PL201 1UH_NRS4018T1R0NDGJ_3.2A_30%
CHG_B+
PC218 0.1U_0402_25V6
PC217 0.1U_0402_25V6
PC207 1U_0603_25V6K
PC208 1U_0603_25V6K
PC211 @ 10U_0805_25V6K
PC212 @ 10U_0805_25V6K
PC213 10U_0805_25V6K
PC214 10U_0805_25V6K
PC215 @ 0.1U_0402_25V6
PC216 0.1U_0402_25V6

PQ207 DMG4406LSS_SO8
PC234 0.01U_0402_50V7K
PR232 @ 0_0402_5%
BQ24725_BATDRV
BQ24725_BATDRV_1
PR233 4.12K_0603_1%

VIN
PD230 BAS40CW_SOT323-3
PC235 0.1U_0402_25V6
PC236 0.1U_0402_25V6
0.047U_0402_25V7K
PC237
PR228 10_1206_1%
PR229 2.2_0603_5%
PD231 RB751V-40_SOD323-2
PC238 0.1U_0603_25V7K
PC239 1U_0603_25V6K
PC205 1U_0603_25V6K
PR234 4.12K_0603_1%
PR235 4.12K_0603_1%

PQ201 AON7408L
DH_CHG
PL202 4.7UH_ETQP3W4R7WFN_5.5A_20%
BQ24725_LX
CHG
PR222 0.02_1206_1%
BATT+
PQ202 FDMC7692S_MLP8-5
PR206 4.7_1206_5%
PC206 680P_0402_50V7K
PC242 0.1U_0603_16V7K
CSOP1
CSON1
PC240 0.1U_0402_25V6
PC241 0.1U_0402_25V6
PC221 @ 10U_0805_25V6K
PC222 10U_0805_25V6K
PC223 10U_0805_25V6K
PC224 2200P_0402_50V7K
PC225 0.01U_0402_50V7K

PU200 BQ24725RGRR_VQFN20_3P5X3P5
PAD VCC PHASE HIDRV BTST REGN
ACN LODRV DL_CHG
ACP GND
CMSRC SRP SRP CSOP1
ACDRV SRN SRN CSON1
ACOK BATDRV BQ24725_BATDRV
ACDET IOUT SDA SCL ILIM
BQ24725_VCC BQ24725_LX BQ24725_BST BQ24725_REGN BQ24725_ACN BQ24725_ACP
BQ24725_CMSRC
BQ24725_ACDRV

PR236 10_0603_1%
PR237 6.8_0603_5%

+3VALW
@PR238 10K_0402_1%
BQ24725_ACOK
+3VL
PR239 10K_0402_1%
<27> ACIN
PR240 10K_0402_1%

+3VALW
PR241 150K_0402_1%
BQ24725_ILIM
PR242 100K_0402_1%
PC243 0.01U_0402_25V7K

VIN
PR243 270K_0402_1%
PR244 154K_0402_1%
BQ24725_ACDET
PC244 0.1U_0402_25V6
PR245 66.5K_0402_1%
PC245 100P_0402_50V8J
PR246 100_0402_5%

EC_SMB_CK1 <27,31>
EC_SMB_DA1 <27,31>
ADP_I <27,31>

Please locate the RC
Near EC chip
2011-02-22

Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	

ILIM and external DPM 3.97A

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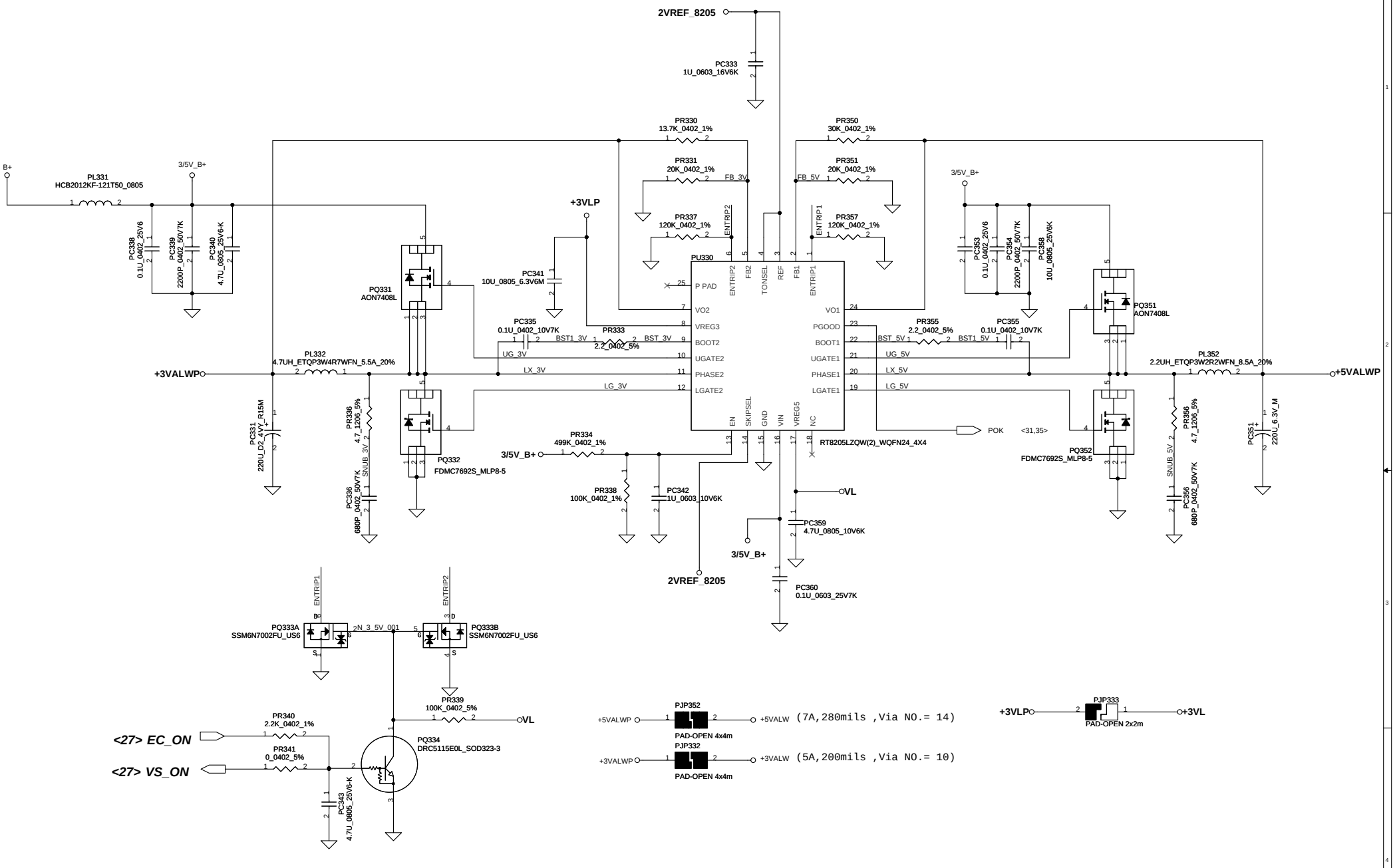

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

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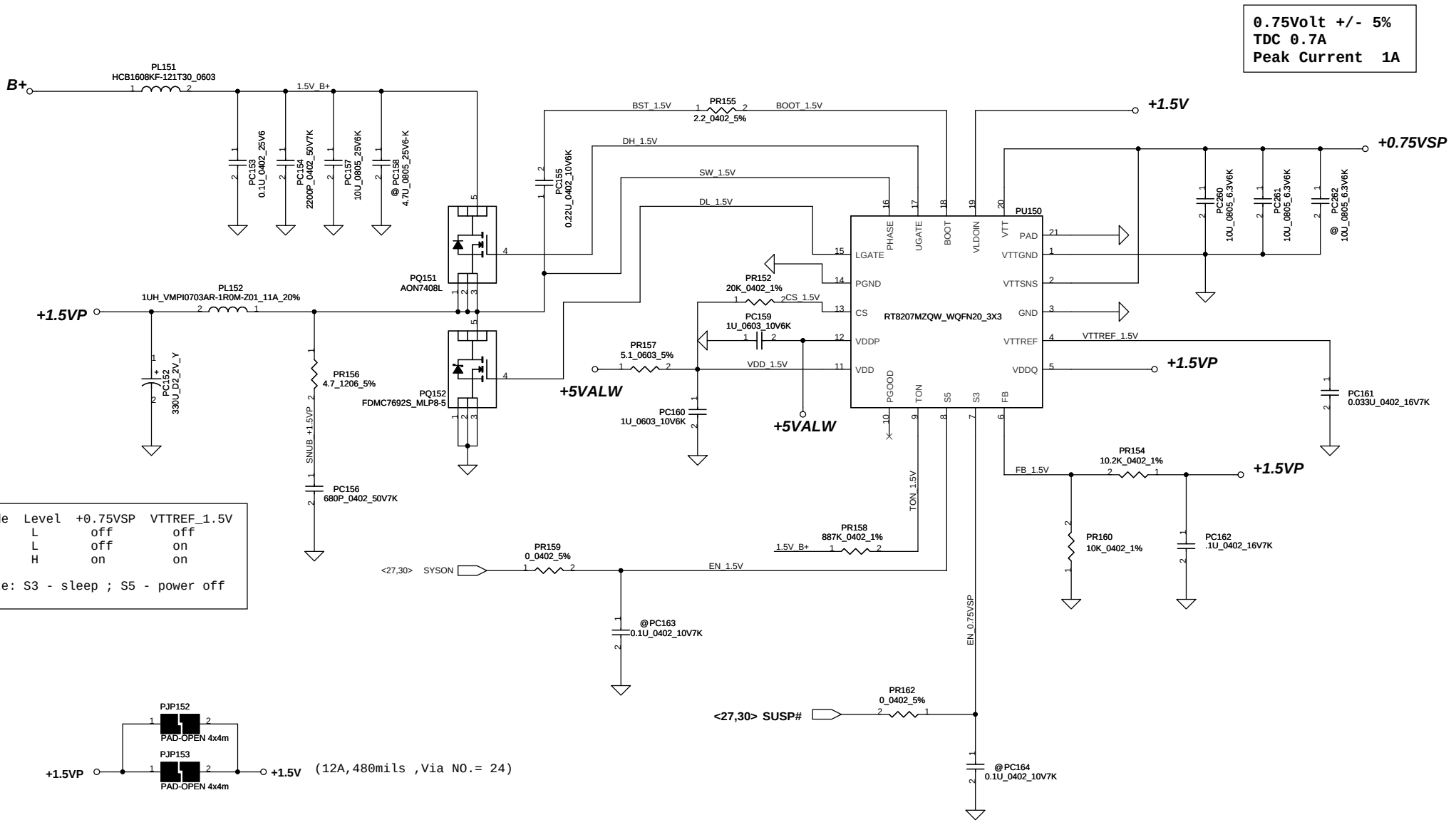

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

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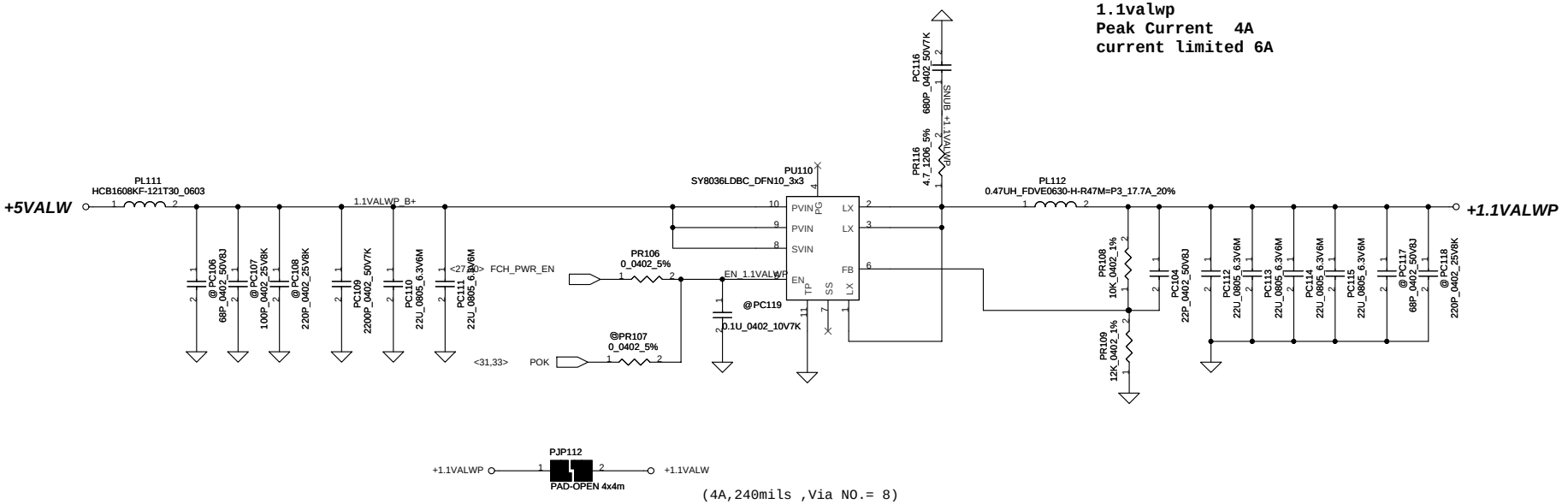
1.1valwp
Peak Current 4A
current limited 6A



(4A,240mils ,Via NO.= 8)

Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	

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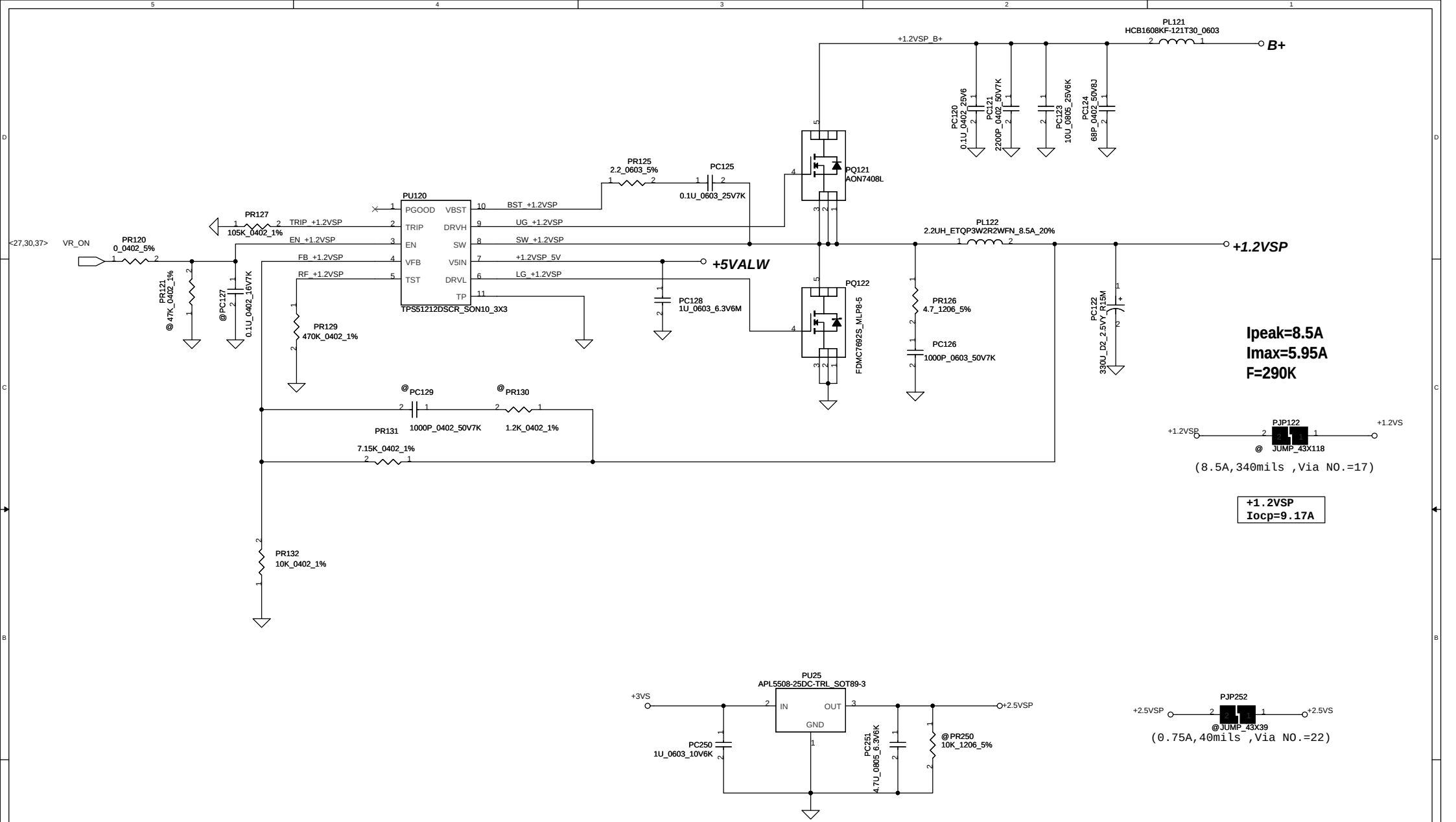

Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	

Compal Electronics, Inc.

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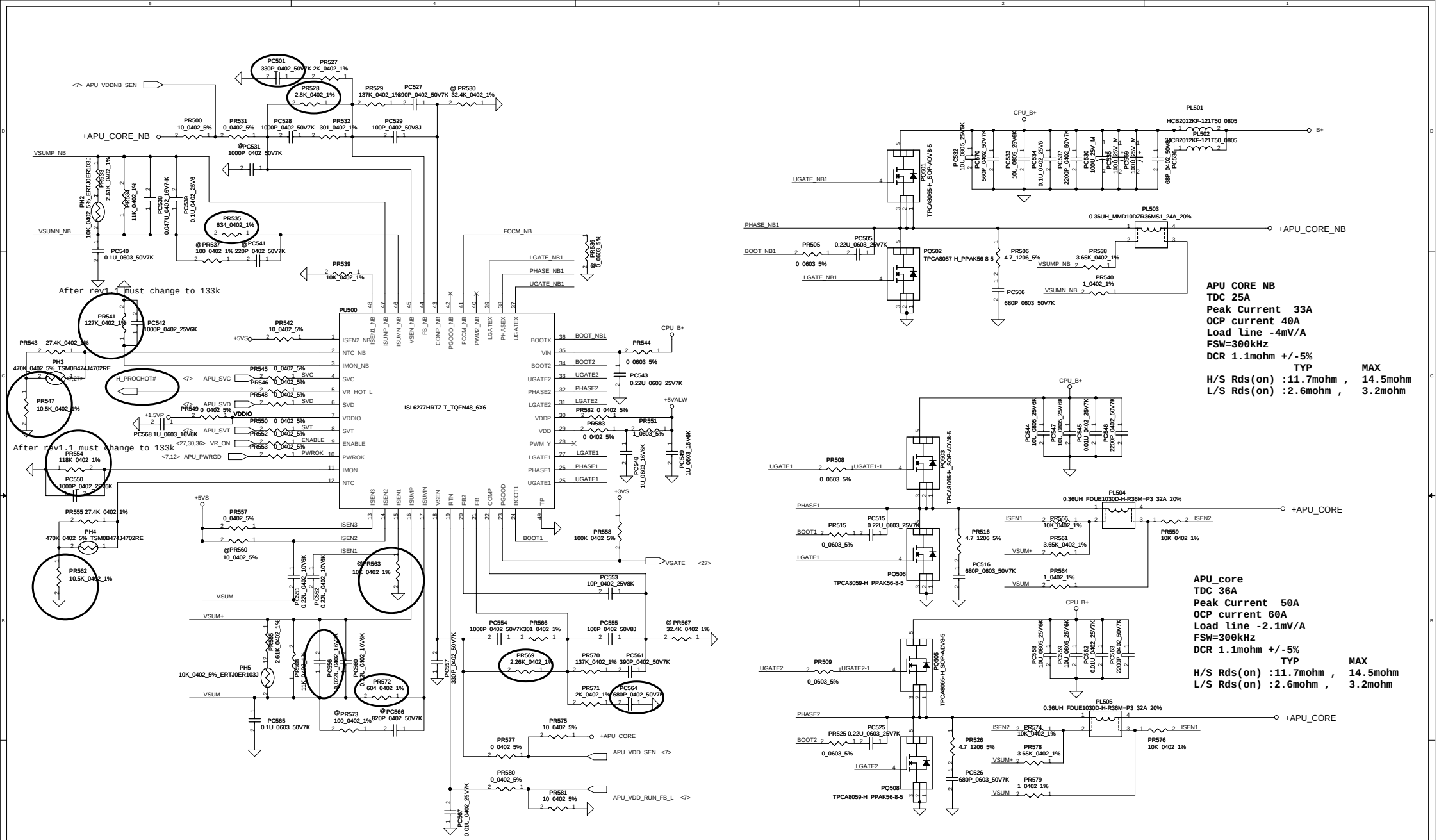

Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

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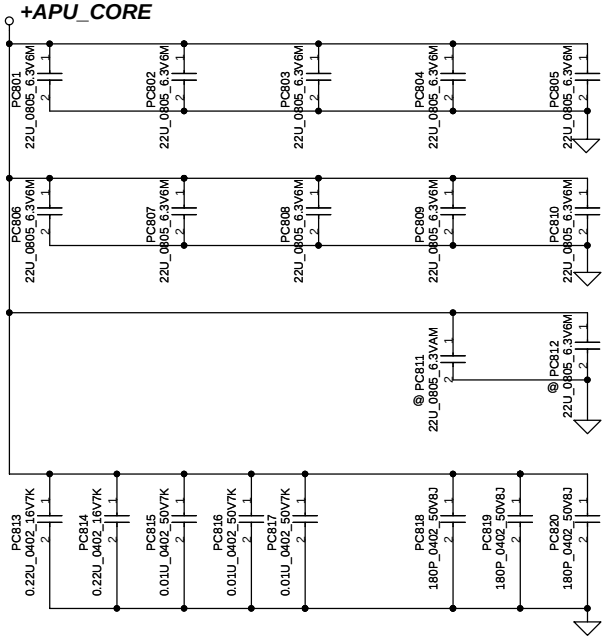
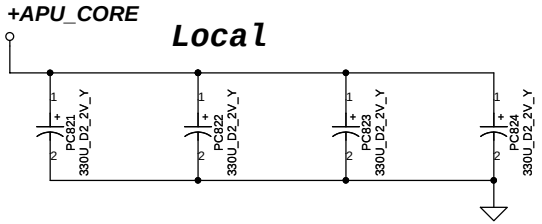
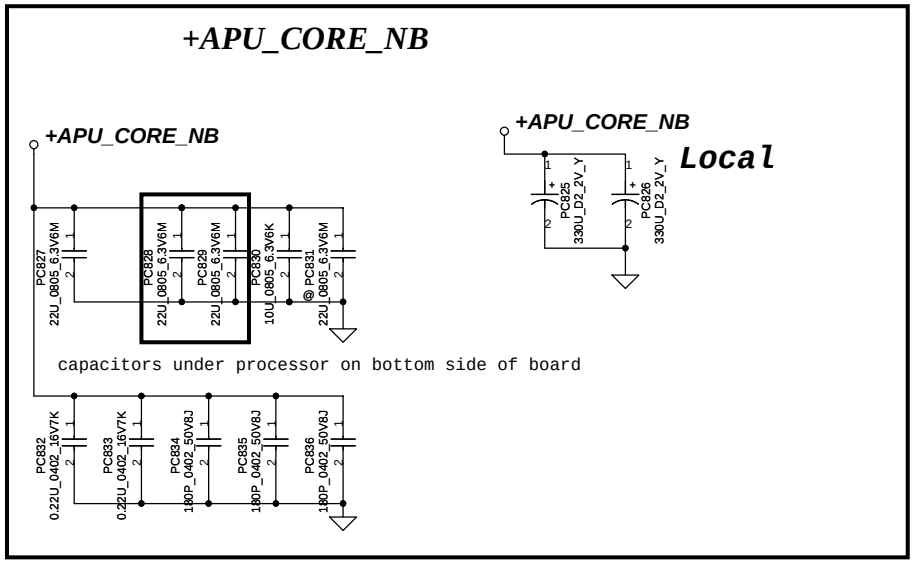
+APU_CORE







Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	2012/01/04	P31-PWR-DCIN/BATT CONN/OTP	Change PQ1 to SB906100280	Change source
2.	2012/01/04	P32-PWR-CHARGER	Change PQ209 to SB00000GC10,PQ203 to PCA8057 PQ202 to FDMC7692,PR241 to150K,PR243 to 270K Change PC211,PC212 to unmount ,add PC206,PR206	Change source Circuit modify
3.	2012/01/04	P33-PWR-3.3VALWP/5VALWP	Change PR350 to 30K,PR351 to 20K,PR337,PR357 to120K add PC336,PR336,PC356,PR356	Circuit modify
4.	2012/01/04	P34-PWR-1.5VP/+0.75VSP	Add PR156,PC156	
5.	2012/01/04	P37-PWR +CPU_CORE	Change PL503 to SH00000HD00,PQ502 to TPCA8057	Change source

Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2012/12/31

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HW PIR (Product Improve Record)

QMLE4 LA-8864P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2
GERBER-OUT DATE: 2012/02/13

Item	Date	Page	Solution	Request
1.	1/10	P23	Add PJ31	For saving power consumption
2.	1/12	P29	Change JTP symbol to SP01001BF10	For ME request
3.	1/30	P25	Add internal MIC to MB	For customer request
4.	1/31	P23	Swap UL3 MDI0 and MDI1	For LAN trace routing
5.	2/1	P22	Add PJ33, WLAN power circuit and reset pin	For customer request
6.	2/2	P26	Update JCRIO pin definition	Change int. MIC to MB
7.	2/2	P25	Remove CA64, add RA32 and RA33	Move sense resistors to MB
8.	2/3	P22	Change JWLAN symbol to SP07000TB00	For ME request
9.	2/3	P27	Add WLAN_PWR# and WLAN_RST#	For customer request
10.	2/8	P23	Add test point TL1 for pin37	For vendor request
11.	2/8	P29	Add screw H17, H20 and H21	For ME request
12.	2/9	P10	Change C218 from 390U to 330U (SF000002080)	For cost down
13.	2/9	P20	Reserve ESD D94~D96 for HDMI	For ESD request
14.	2/9	P19	Remove D3~D5 and add D97 and D98	For ESD request
15.	2/9	P23	Reserve ESD D99 and D100 for LAN	For ESD request
16.	2/9	P21	Add resistors to improve SATA signal quality	For SATA ODD co-layout
17.	2/10	P7	Stuff C126 and C127	For EMI request
18.	2/10	P22	Stuff CCL10	For EMI request
19.	2/10	P7	Reserve R77 and R85	For DeepS3 leakage
20.	2/21	P23	Change UL3 and UL4 PN to SP050006N00	For EMI request

REVISION CHANGE: 0.2 TO 0.3
GERBER-OUT DATE: 2012/03/12

Item	Date	Page	Solution	Request
1.	3/1	P12	Update RTC scematic	For avoiding +3VL short to GND
2.	2/29	P22	Change R108 pull-high from +3VS to +3VALW	For LVDS sequence issue
3.	3/7	P26	Add R292 and reserve R293	To avoid PXS_PWREN floating
4.	3/7	P7	Unstuff R121~R124,R118,R119	For debug use
5.	3/7	P27	Update U13 footprint	
6.	3/7	P27/30	Connect SATA port2 to 15"ODD connector, and add GPIO54	To solve SATA EA fail issue
7.	3/8		Change RB20,RB34,R3,RV102,R425,R136,R31,R32,R33,RV284,RV287 R62,RV277 to short pad	
8.	3/12	P20	Add C201 and C214	For EMI request
9.	3/12	P21	Add C364 and C365	For EMI request
10.	3/12	P25	Add CA5, CA6, CA64, CA67, CA68 and CA77	For EMI request
11.	3/14	P8	Add C147 co-layout with C100	To avoid damage by SMT process
12.	3/14	P10	Add C148 co-layout with C218	To avoid damage by SMT process

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