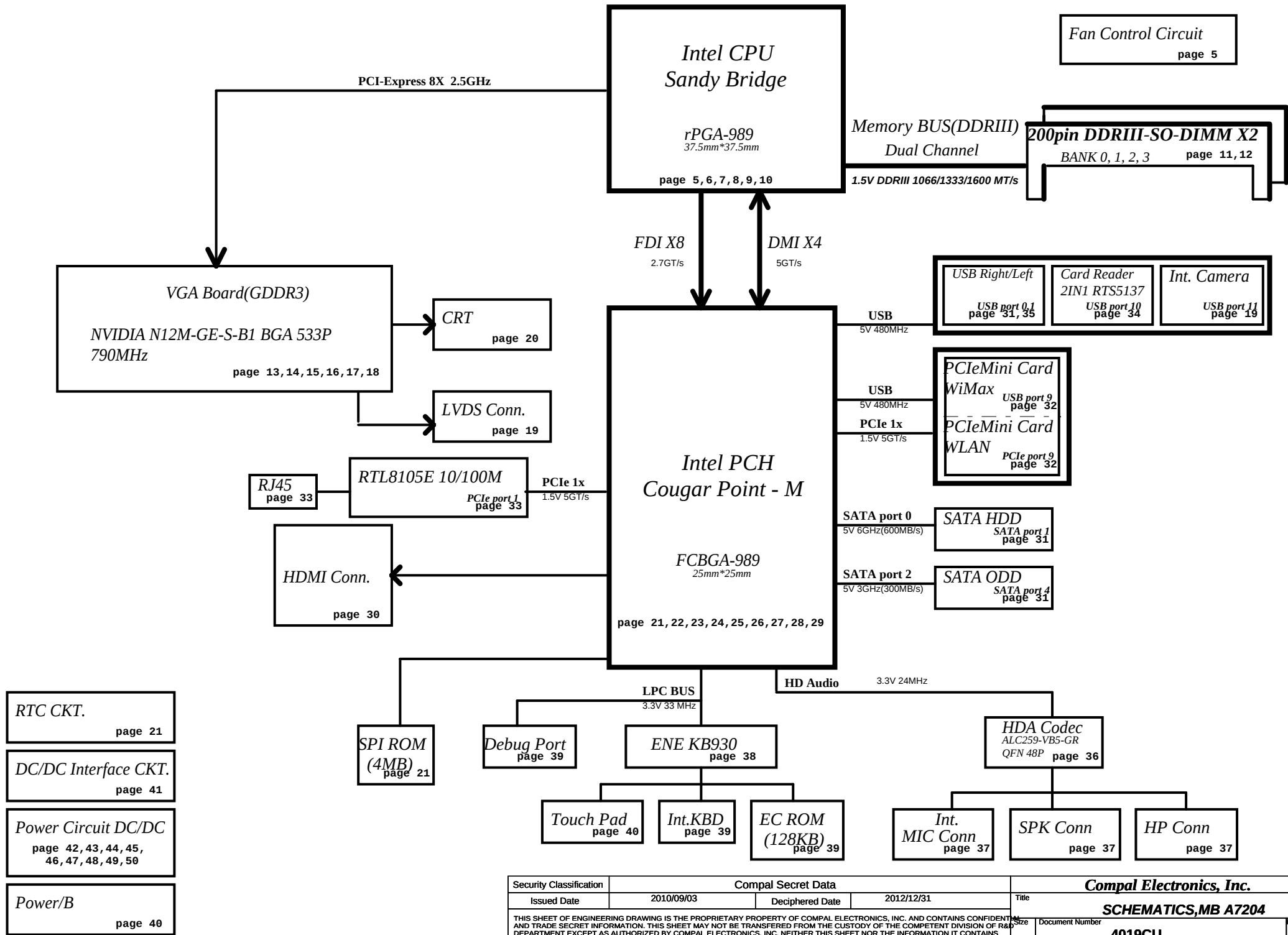


PWWHA
Delhi 10RG

LA-7204P REV 0.1 Schematic

Intel Processor(Sandy Bridge) / PCH(Cougar Point)
2010-12-19 Rev 0.1

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				B	A
				Date	Thursday, January 13, 2011
				Sheet	1 of 53



B+

TPS51125ARGER

DESIGN CURRENT 0.1A +3VL

Ipeak=5A, Imax=3.5A, Iocp min=7.9A DESIGN CURRENT 10A +5VALW

SUSP#

SY8033BDBC

DESIGN CURRENT 1.8A +1.8VS

SUSP

N-CHANNEL

SI4800

DESIGN CURRENT 5.5A +5VS

Ipeak=5A, Imax=3.5A, Iocp min=7.7A DESIGN CURRENT 6A +3VALW

WOL_EN#

SUSP

P-CHANNEL
A0-3413

DESIGN CURRENT 330mA +3V_LAN

N-CHANNEL

SI4800

DESIGN CURRENT 4.5A +3VS

VGA_ENVDD

SUSP or 0.75VR_EN#

P-CHANNEL
A0-3413

DESIGN CURRENT 2A +LCD_VDD

G2992F1U

DESIGN CURRENT 0.5A +0.75VS

VR_ON

Ipeak=53A, Imax=36A, Iocp min=70A DESIGN CURRENT 53A +CPU_CORE

ISL95831CRZ-T

SUSP#

TPS51218DSCR

Ipeak=20A, Imax=14A, Iocp min=26A DESIGN CURRENT 21A +VGA_CORE

SUSP#

TPS5117

Ipeak=12.5A, Imax=8.75A, Iocp min=21.4A DESIGN CURRENT 17A +1.05VS_VCCP

VCCPPWRGD

TPS51117

Ipeak=6A, Imax=4.2A, Iocp min=7.76A DESIGN CURRENT 6A +VCCSA

SYSON

TPS51117RGYR

Ipeak=16.5A, Imax=11.55A, Iocp min=21.03A DESIGN CURRENT 20A +1.5V

SUSP

N-CHANNEL

FDS6676AS

DESIGN CURRENT 2A +1.5V_CPU

SUSP

N-CHANNEL

FDS6676AS

DESIGN CURRENT 0.7A +1.5VS

VGA_PWR0K#

N-CHANNEL

FDS6676AS

DESIGN CURRENT 3A +1.5V_MEM_GFX

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				Date	Thursday, January 13, 2011
				Sheet	3 of 53
				Rev	A

Voltage Rails

(0 MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +GFX_CORE
S0	0	0	0	0	0	0
S1	0	0	0	0	0	0
S3	0	0	0	0	0	X
S5 S4/AC	0	0	0	0	X	X
S5 S4/ Battery only	0	0	0	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	WLAN/WIMAX		

EC SM Bus1 Address

EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b

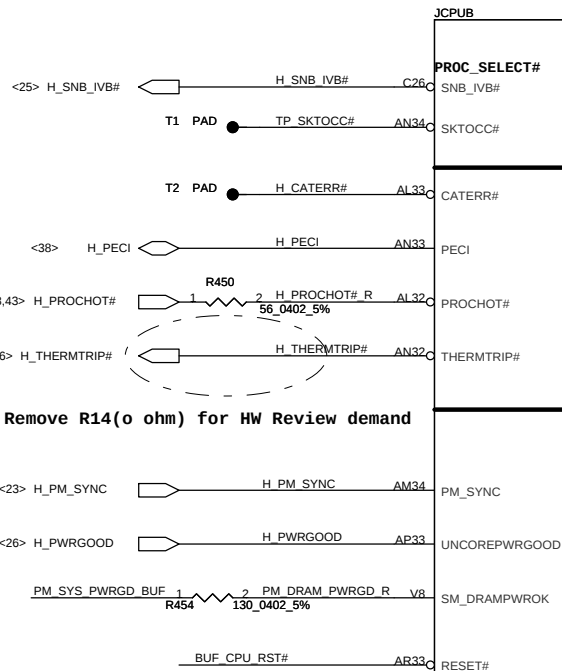
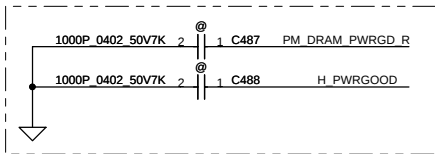
BTO Option Table

Function	DIS only	MINI PCI-E SLOT	LAN			Camera & Mic
description		SLOT1	LAN			Camera & Mic
explain		WIMAX	10/100M	Giga		Camera & Mic
BTO	DIS@	WIMAX@	8105ELD0@	8105ESWR@	8111E@	CAM@

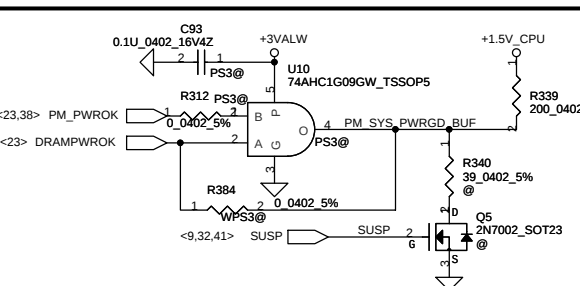
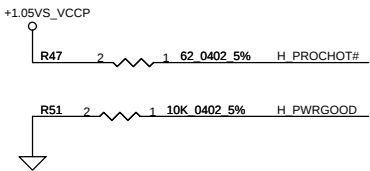
Function	PCH	HDMI			
description					
explain					
BTO	Q65R3@	HDMI@			

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1(Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

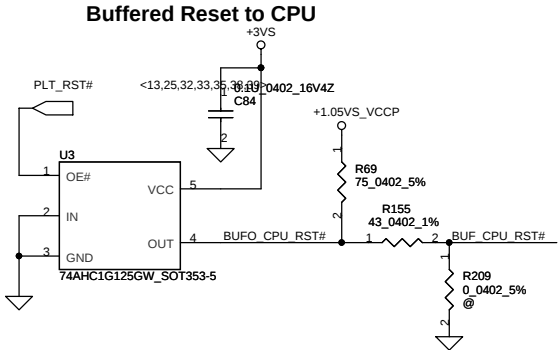
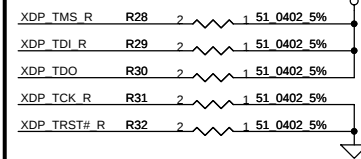
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				Custom	4019CU	A
				Date	Thursday, January 13, 2011	Sheet 4 of 53



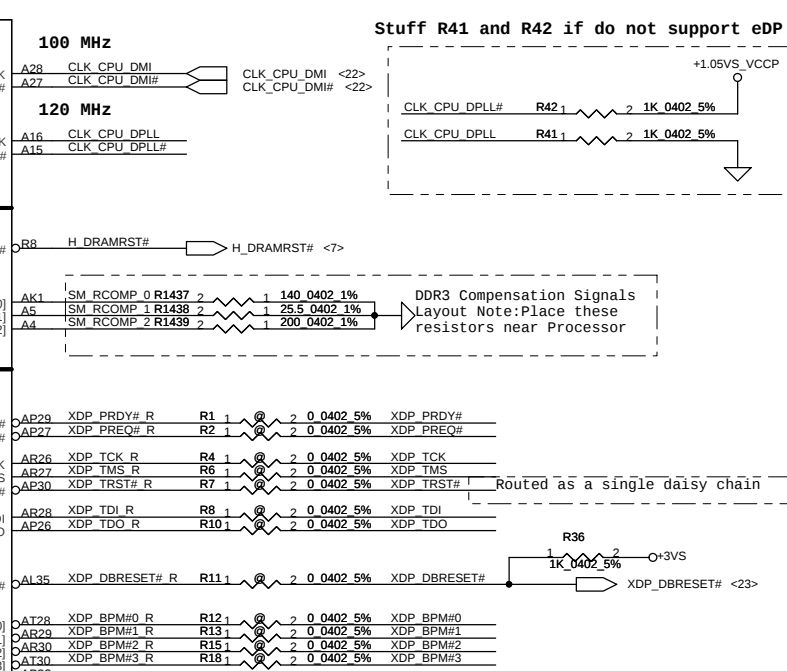
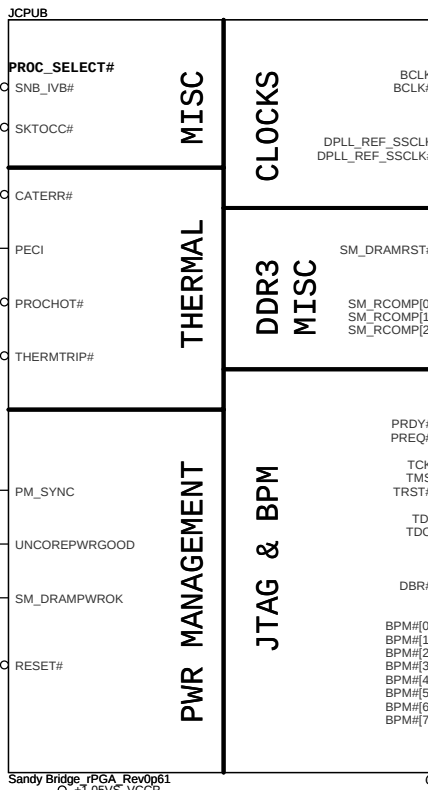
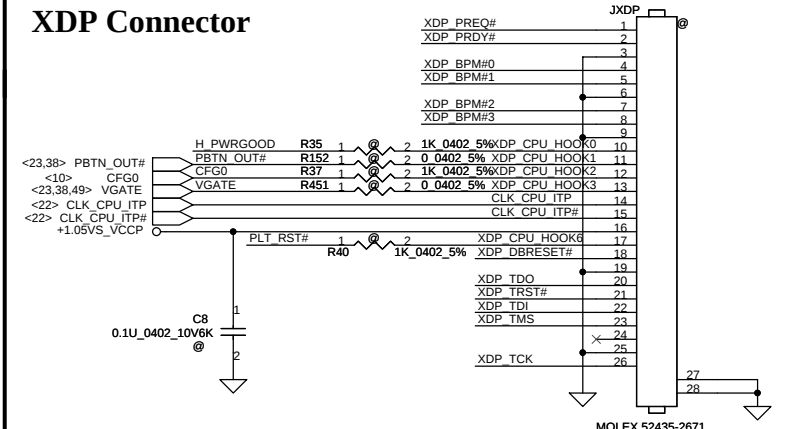
Remove R14(0 ohm) for HW Review demand



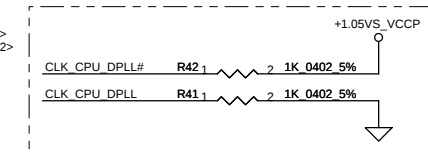
PU/PD for JTAG signals



XDP Connector



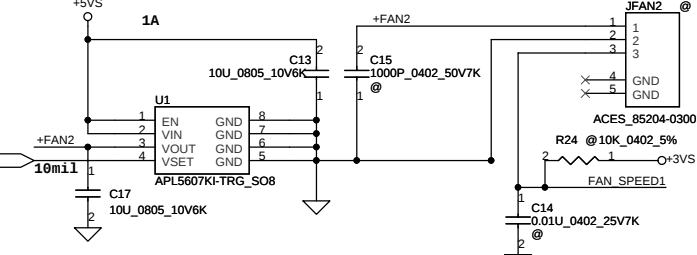
Stuff R41 and R42 if do not support eDP



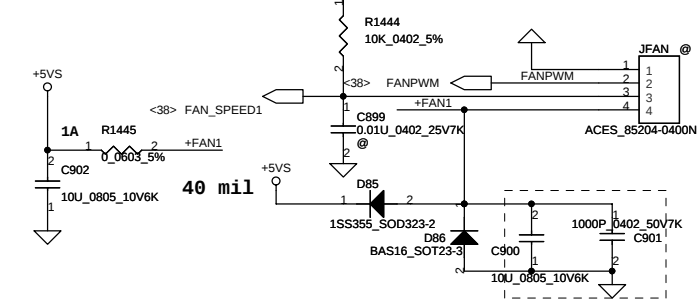
DDR3 Compensation Signals
Layout Note: Place these resistors near Processor

Routed as a single daisy chain

FAN Control Circuit (RPM and PWM)

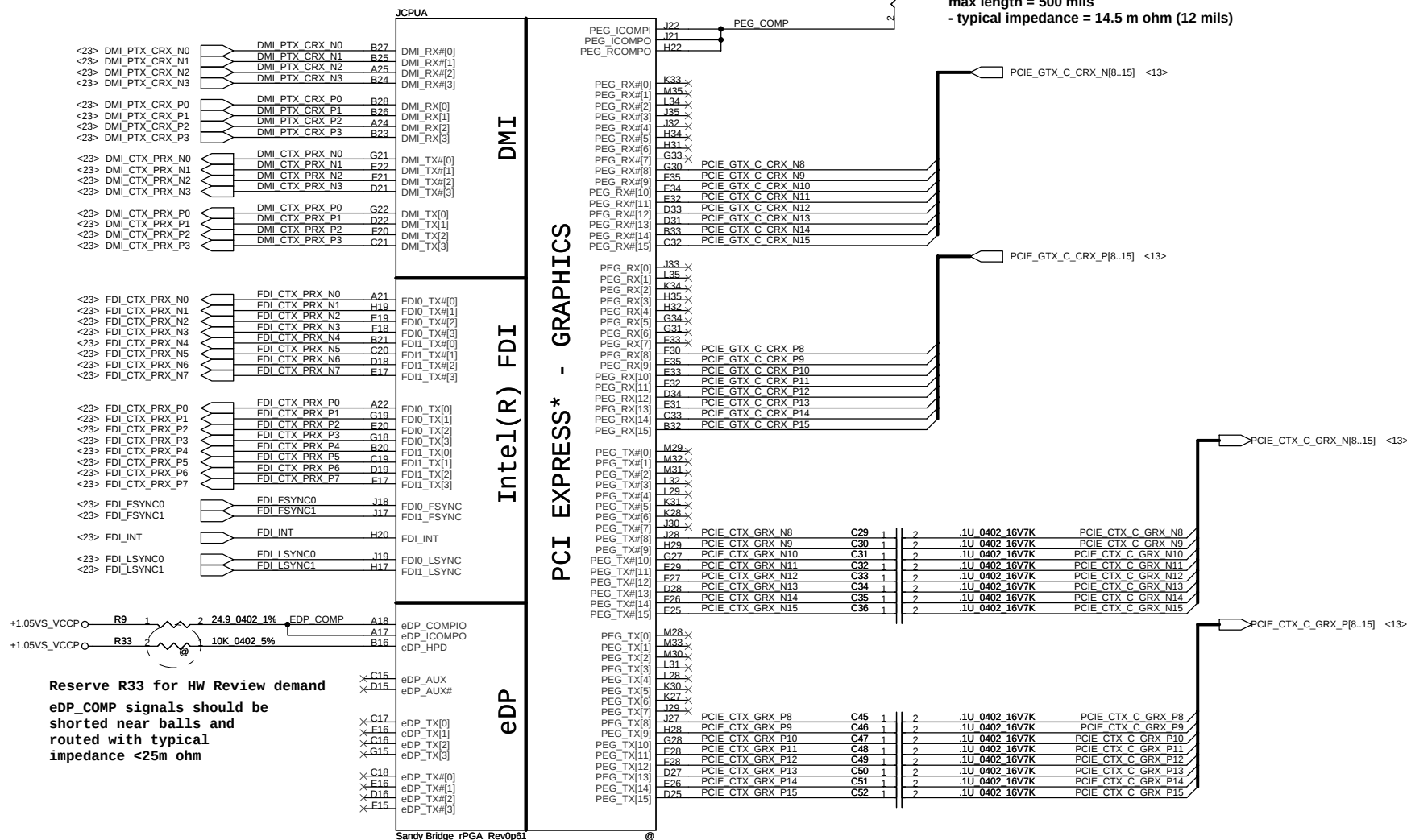


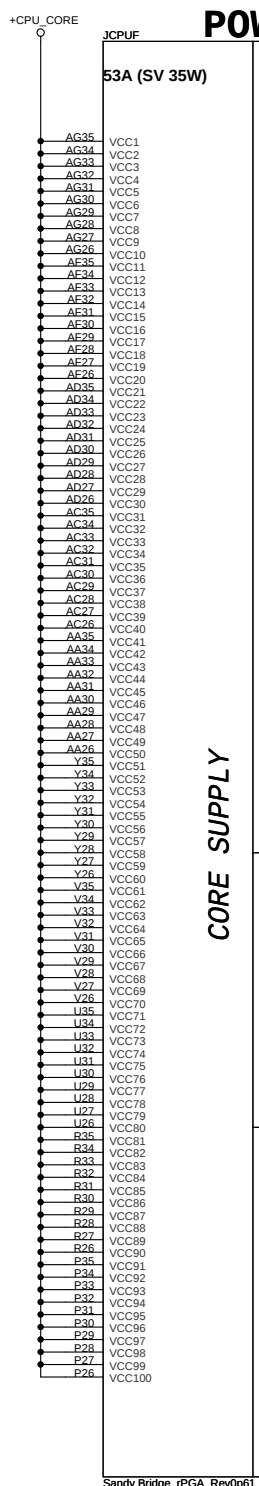
FAN Control Circuit



Close to Connector

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				Date	Thursday, January 13, 2011
				Sheet	5 of 53





POWER

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

8.5A

TOP Socket Cavity x 7

Bottom Socket Cavity x 5

+1.05VS_VCCP Decoupling:
2X 330U (6m ohm), 12X 22U

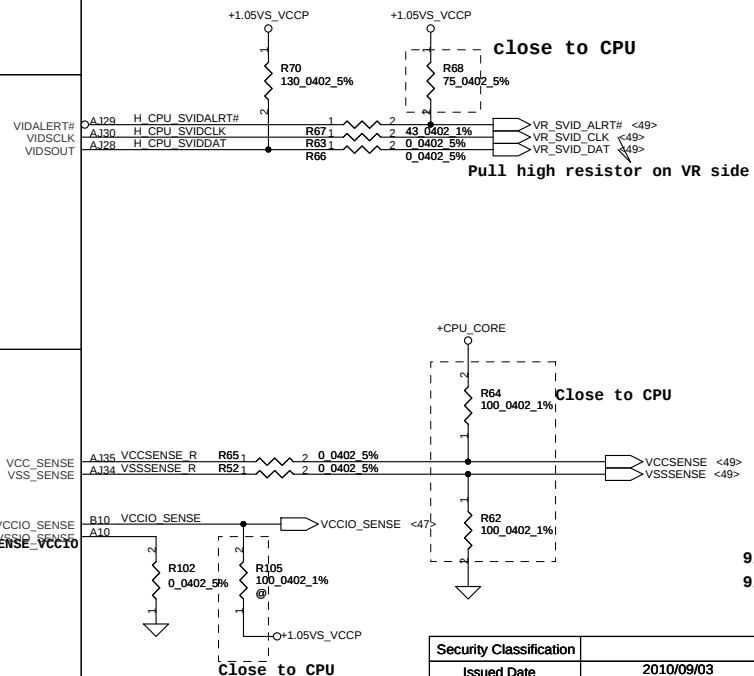
+CPU_CORE Decoupling:
4X 470U (4m ohm), 16X 22U, 10X 10U

Bottom Socket Cavity

Top Socket Edge

Top Socket Cavity

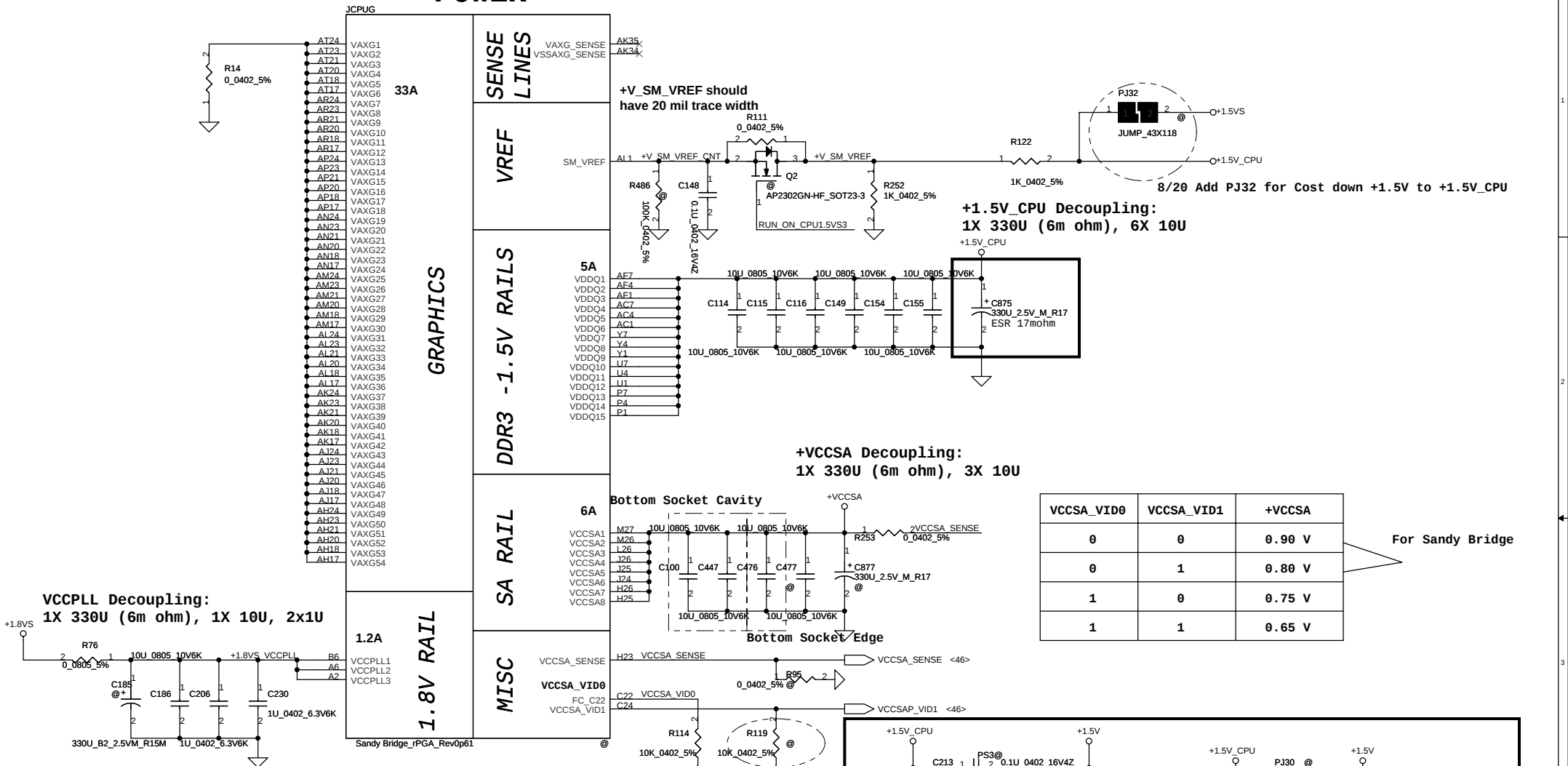
Bottom Socket Edge

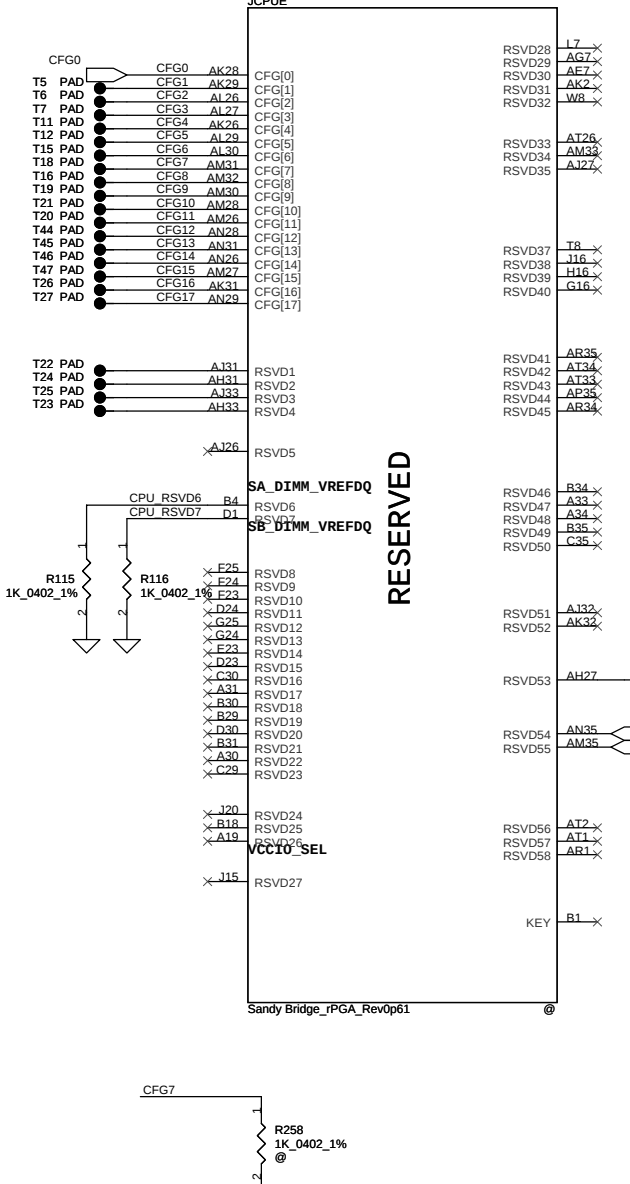
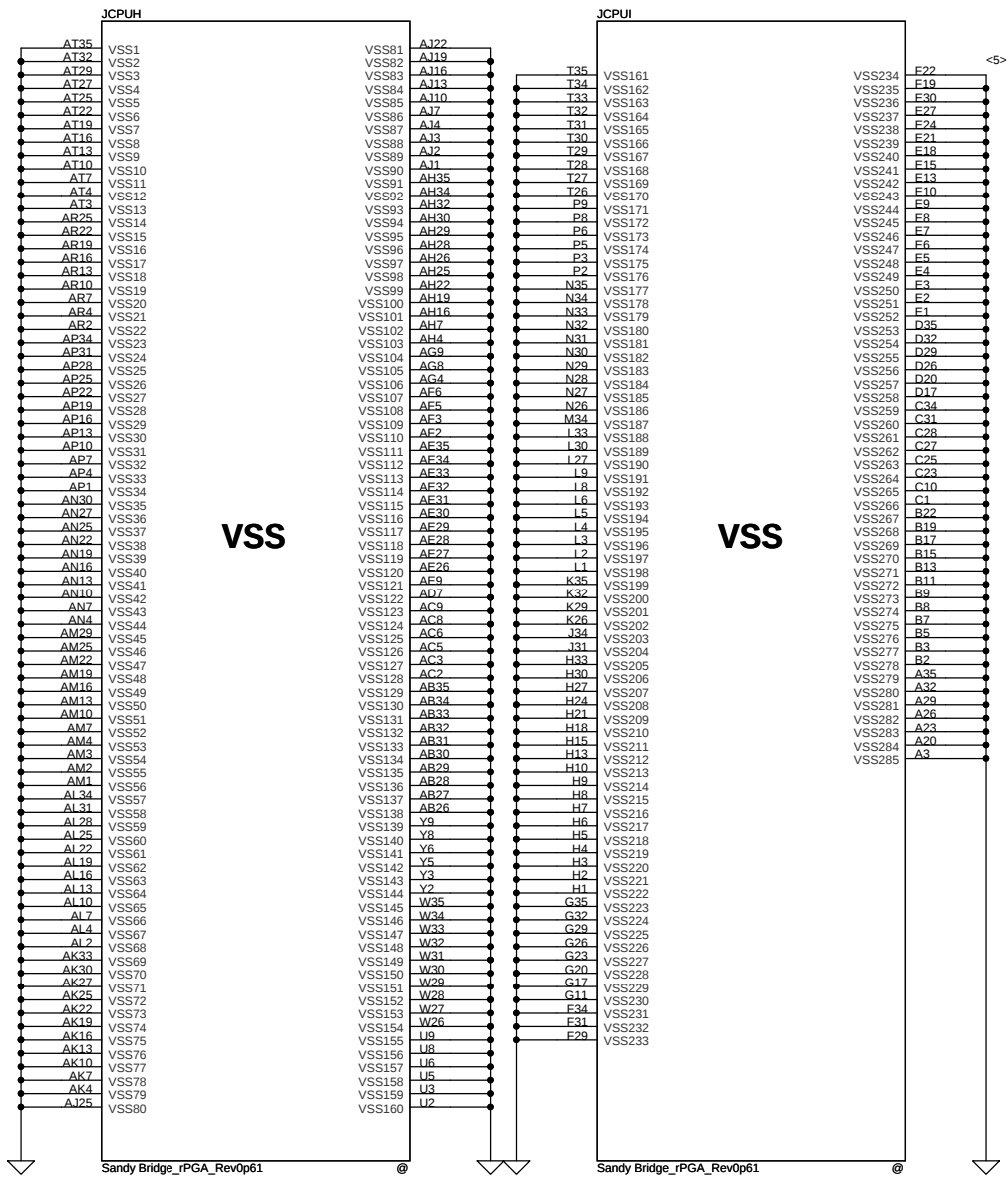


9/02 Add C898 3Pin Bulk Cap by Power Demand
9/02 Change C890, C891, C894 from SGA00005R00 to SGA00004X80 for Power demand

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		4019CU		A	
Date:		Thursday, January 13, 2011		Sheet	
		8		of	
				53	

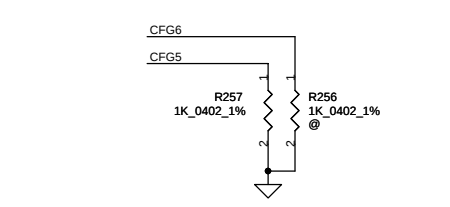
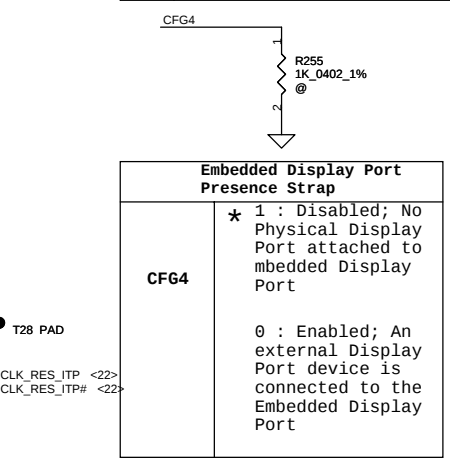
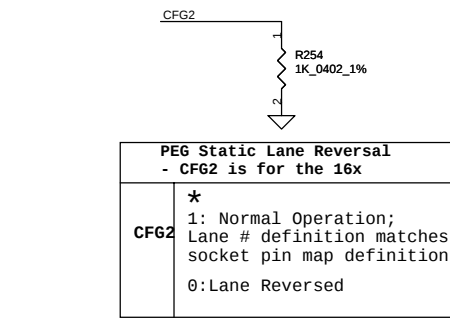
POWER





CFG Straps for Processor

(CFG[17:0] internal pull high to VCCIO)

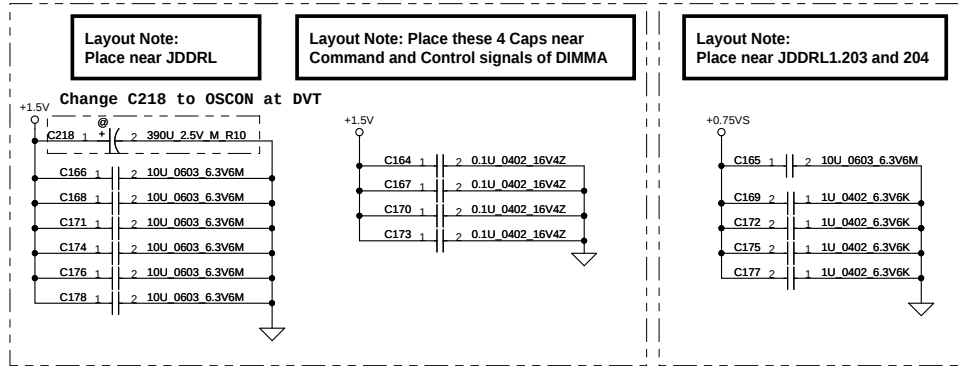
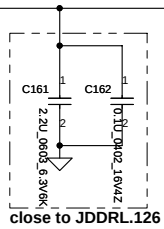
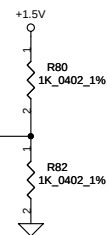
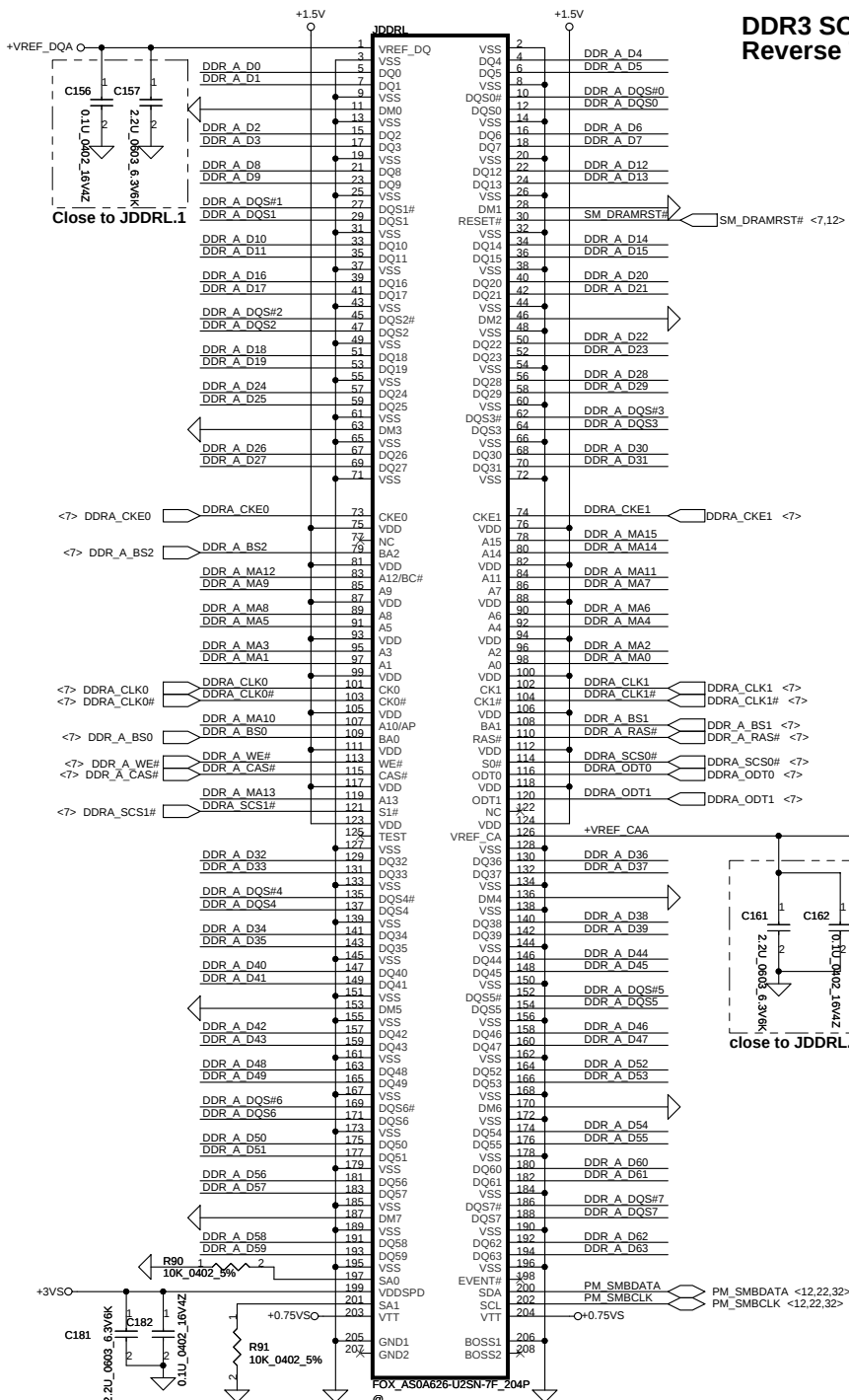


PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled
	★ 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

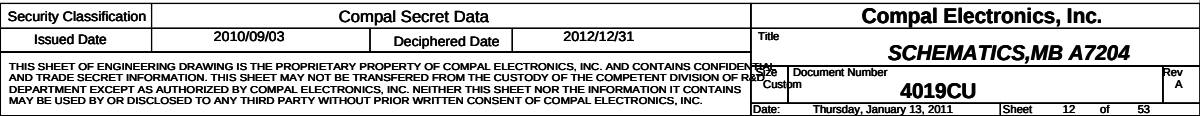
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

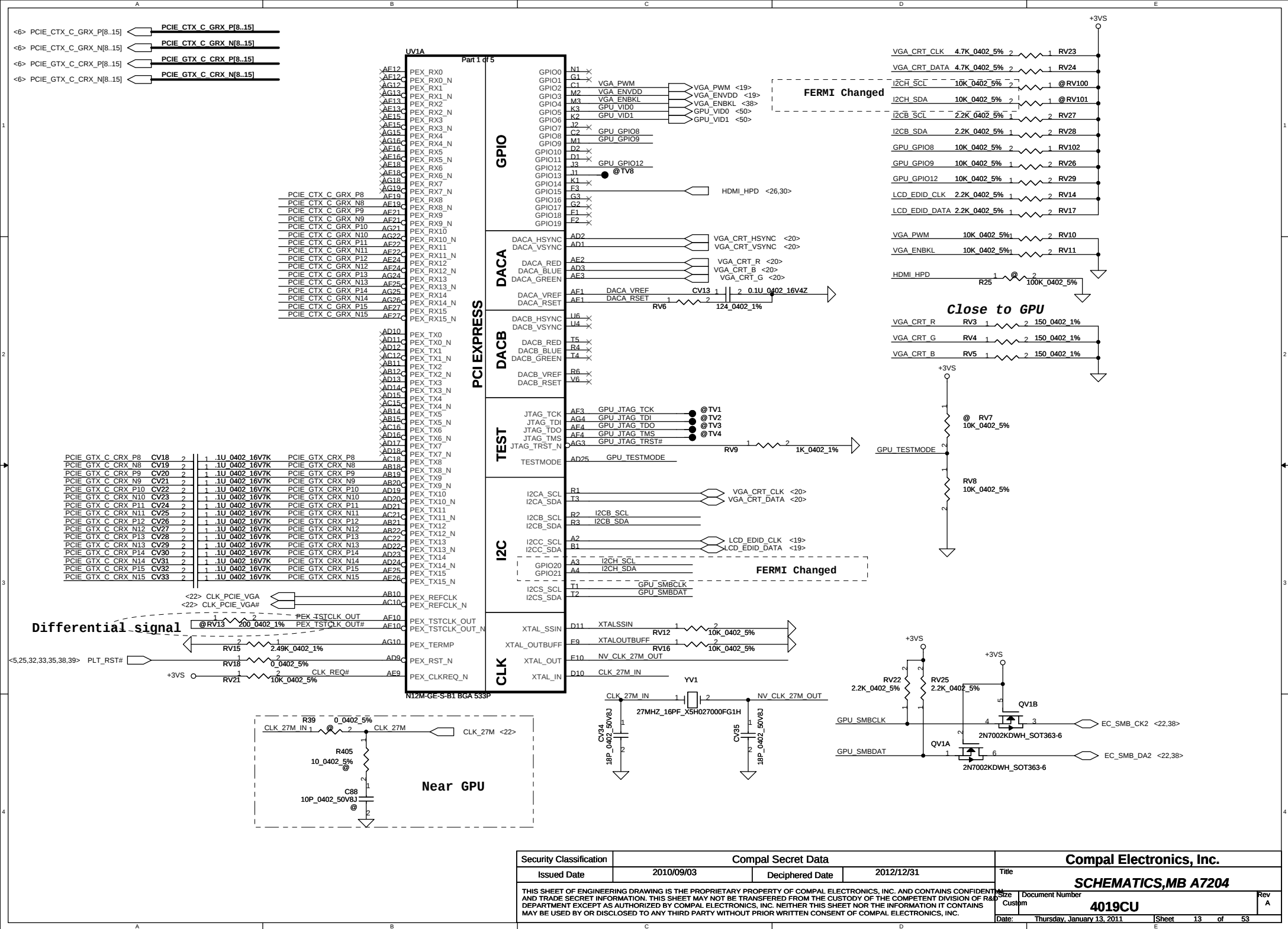
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				Date: Thursday, January 13, 2011	Sheet 10 of 53

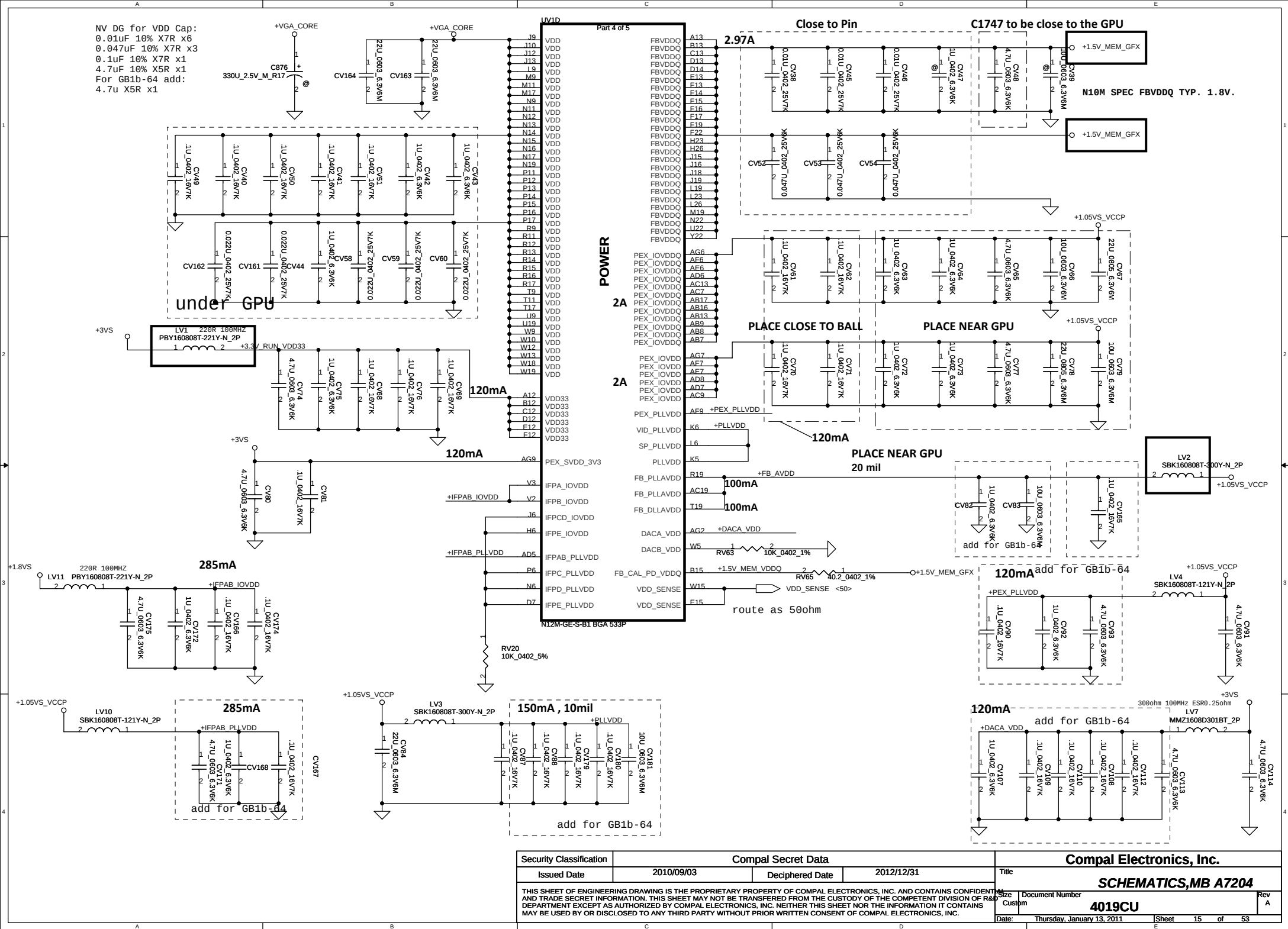
DDR3 SO-DIMM A Reverse Type

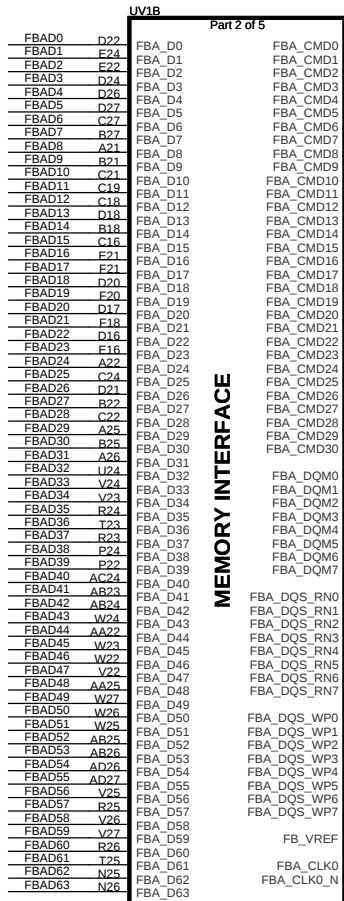
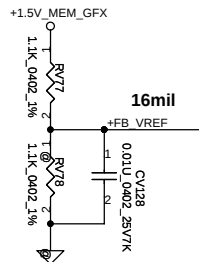
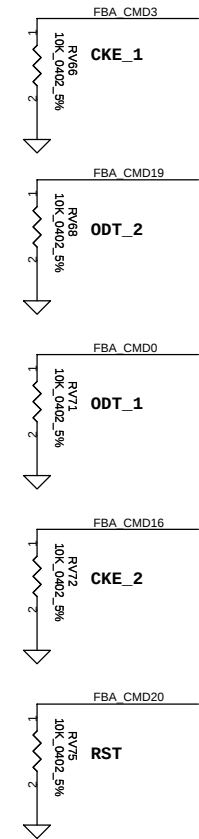
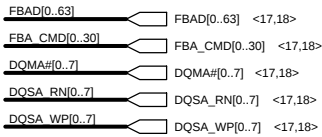


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				4019CU
				Rev A
				Date: Thursday, January 13, 2011
				Sheet 11 of 53









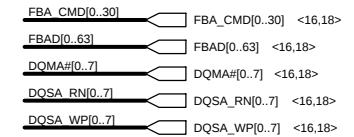
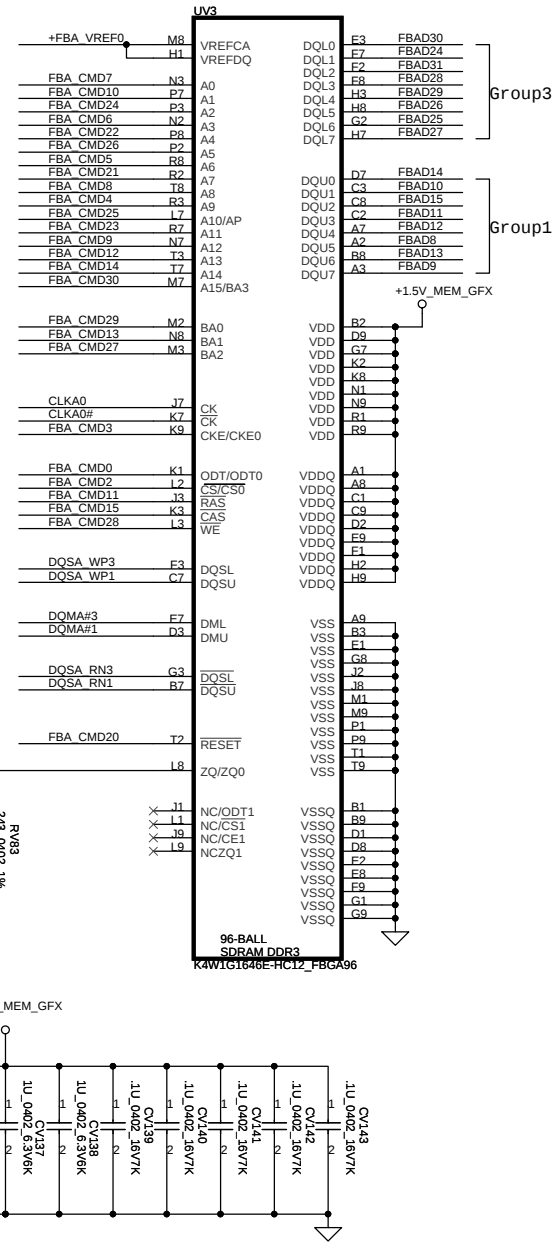
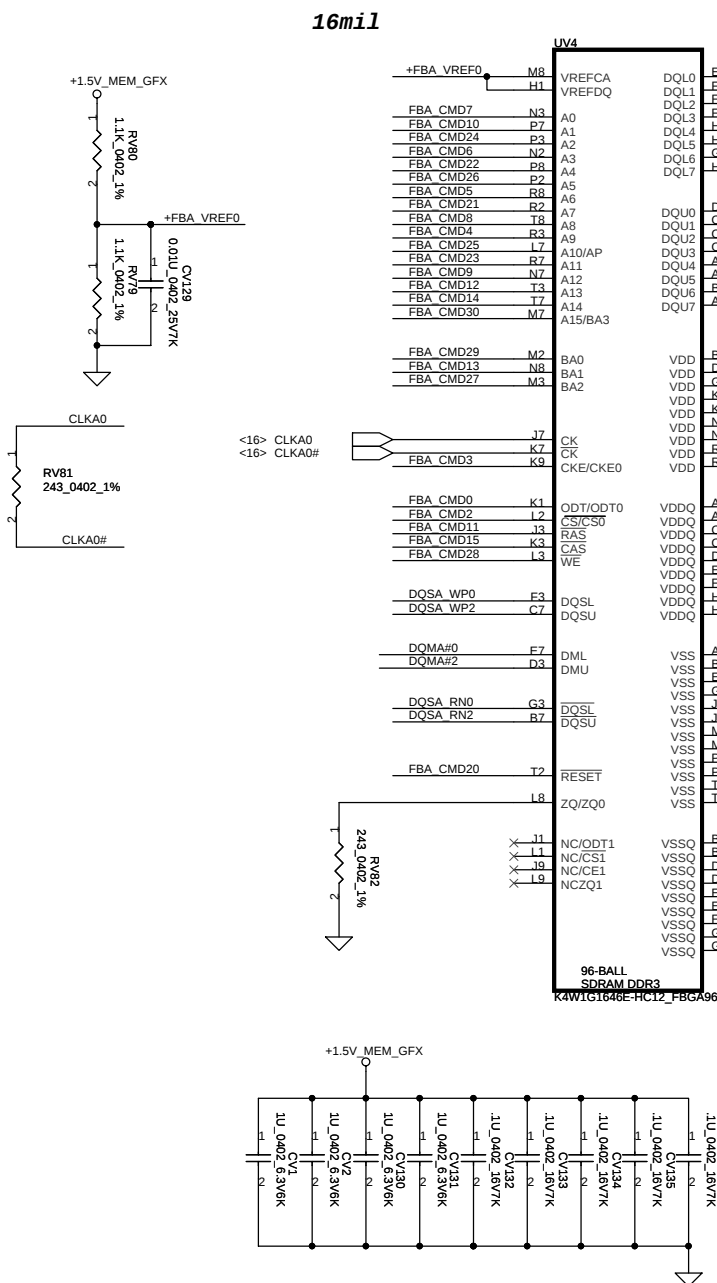
N12M-GE-S-B1 BGA 533P

Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

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				Date	Thursday, January 13, 2011
				Sheet	16 of 53

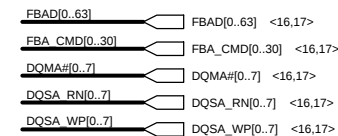
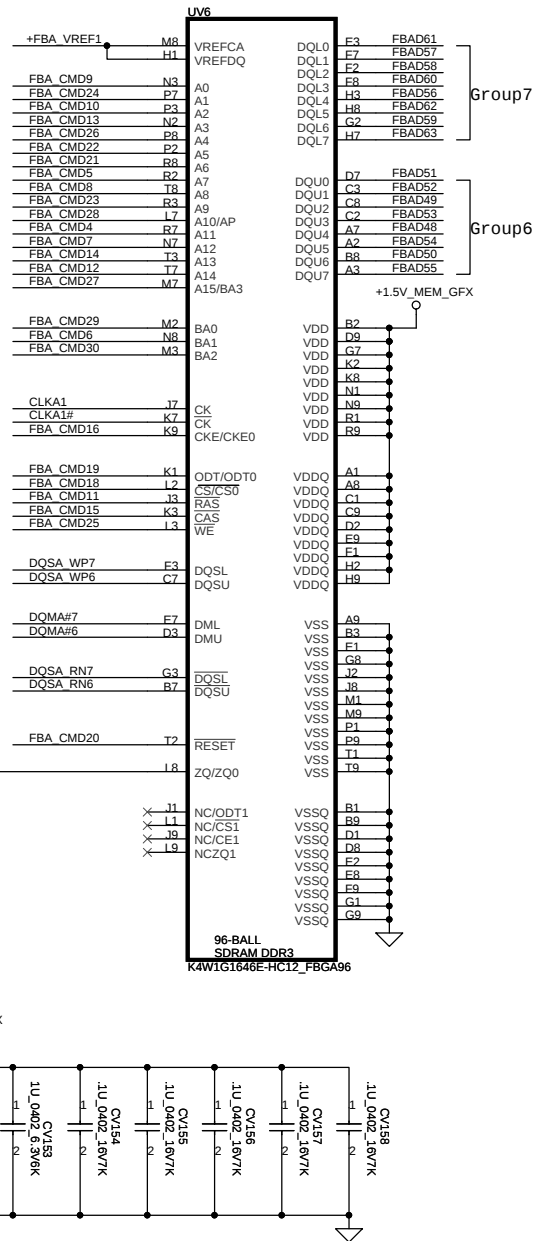
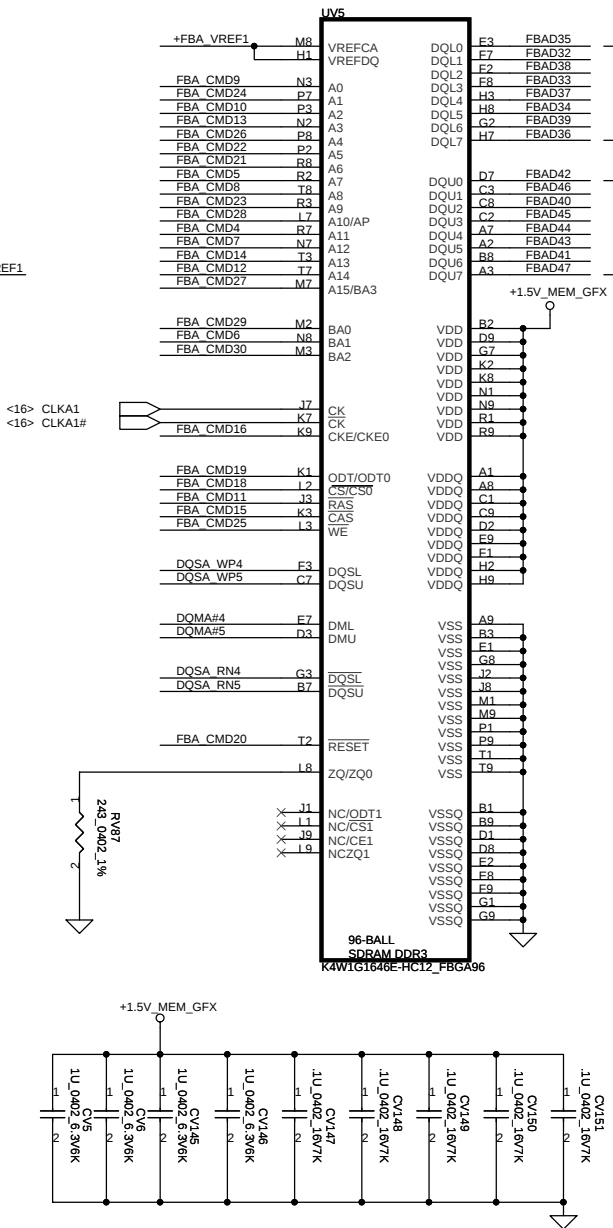
Memory Partition A - Lower 32 bits



Mode E - Mirror Mode Mapping

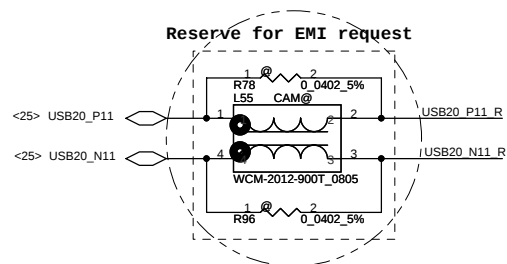
	DATA Bus	
Address	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

Memory Partition A - Upper 32 bits

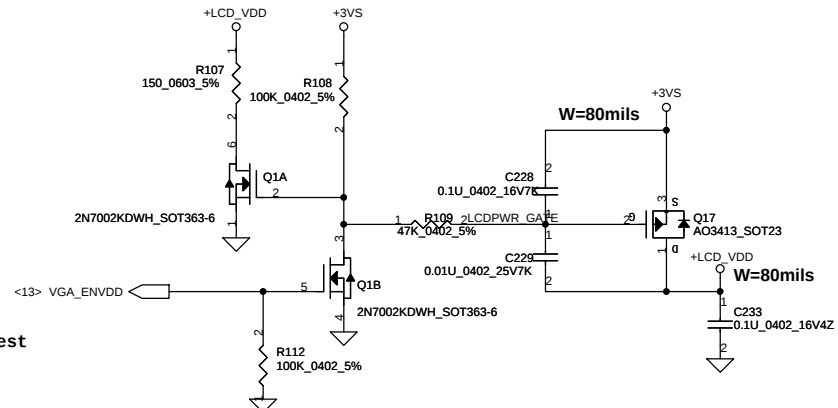


Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0...31	32...63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

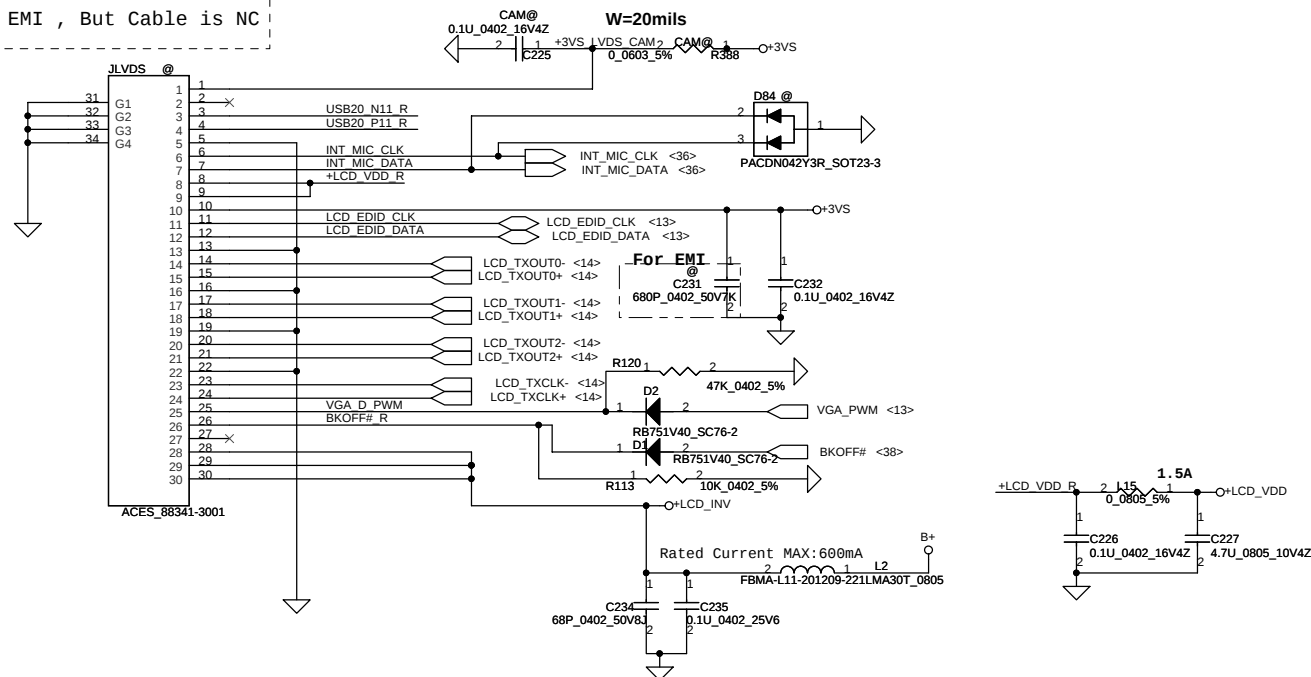


8/20 Swap USB20_P11 and USB20_N11 for layout request

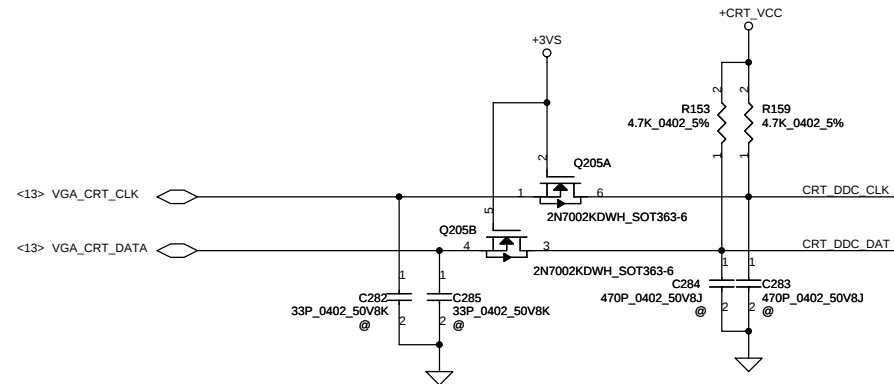
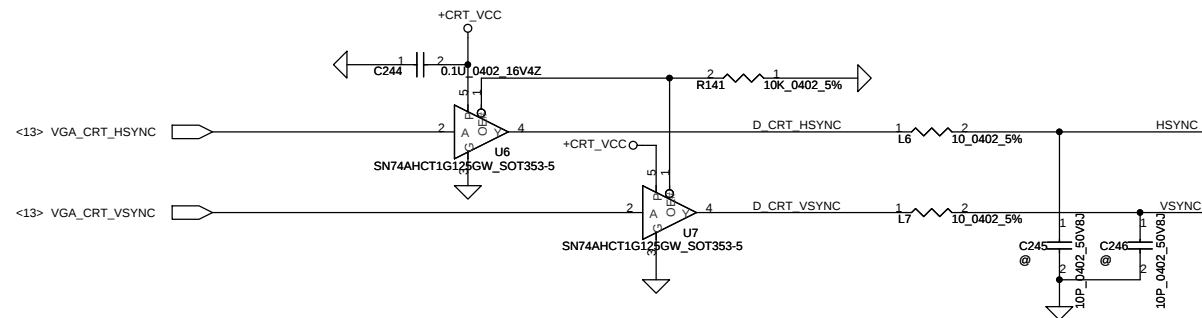
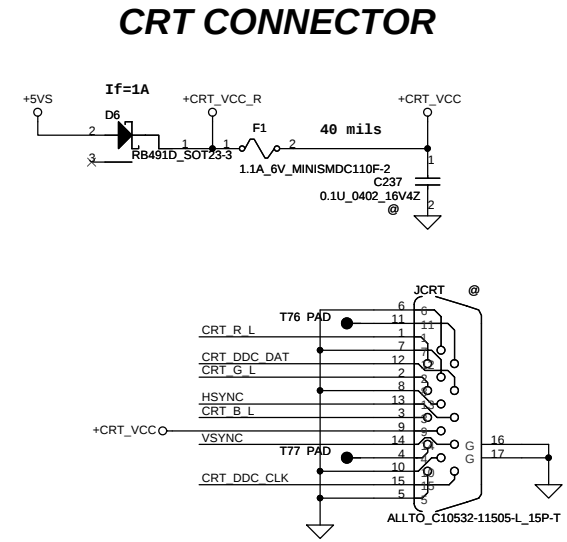
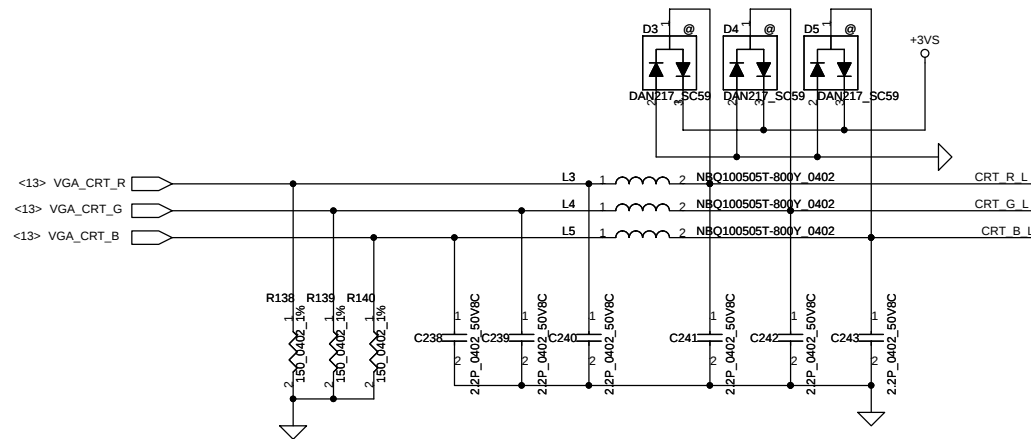


LCD/PANEL BD. Conn.

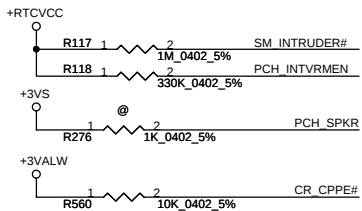
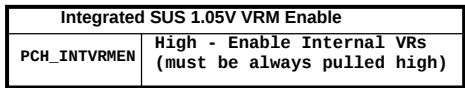
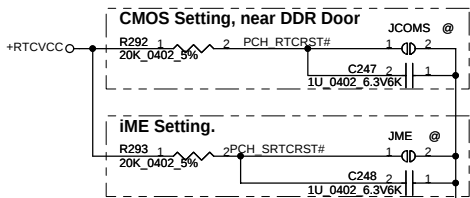
Pin13 GND for EMI , But Cable is NC



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Size		Document Number		Rev	
Custom		4019CU		A	
Date:		Thursday, January 13, 2011		Sheet 19 of 53	



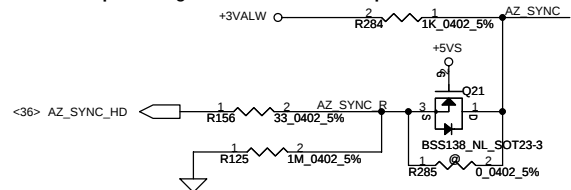
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				Date	Thursday, January 13, 2011
				Sheet	20 of 53



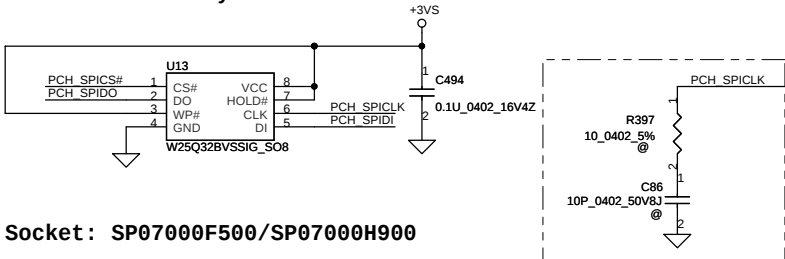
PCH_SPK
High = Enabled (No Reboot)
Low = Disabled (Default)

HDA_SDO
ME debug mode,
this signal has a weak internal pull down
*Low = Disable (default)
High = Enable (flash descriptor security override)

HDA_SYNC
*This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
Need to pull high for Huron River platform



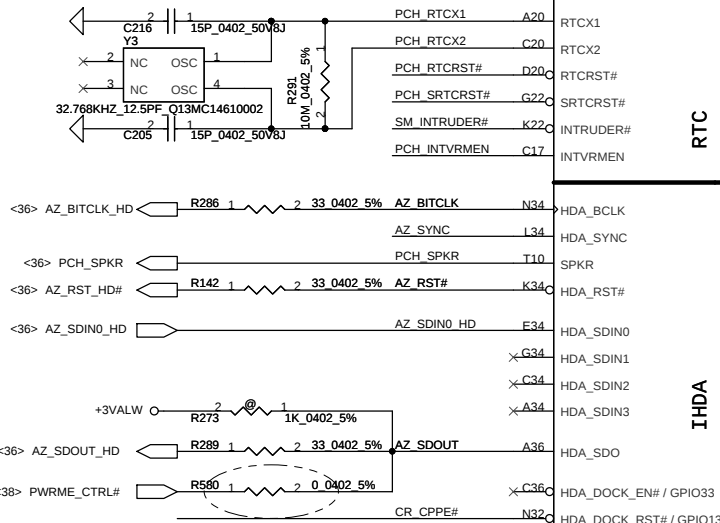
4M Byte



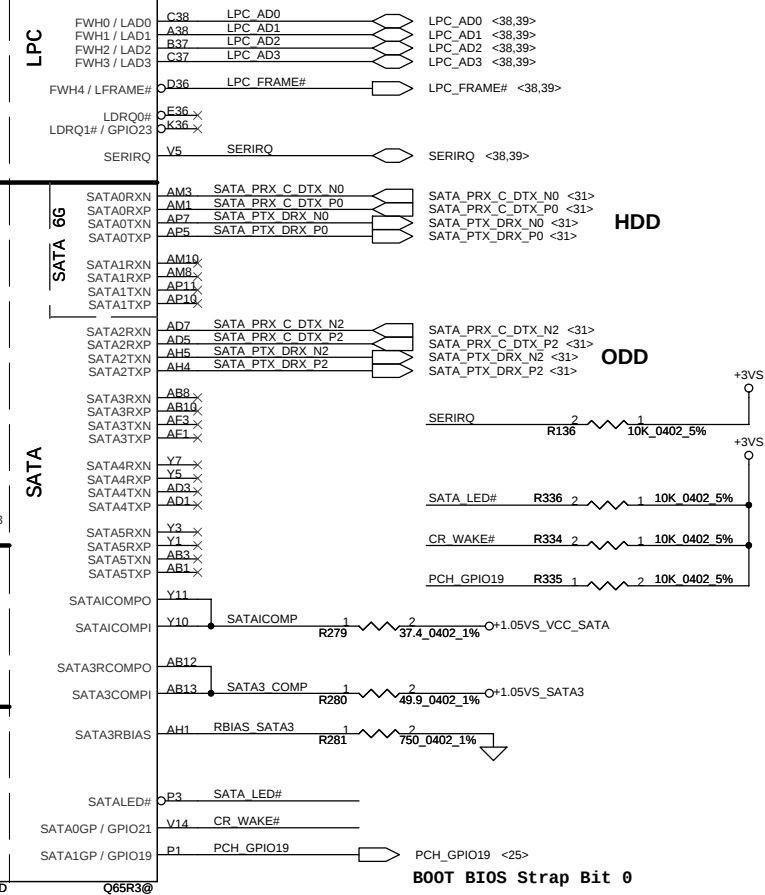
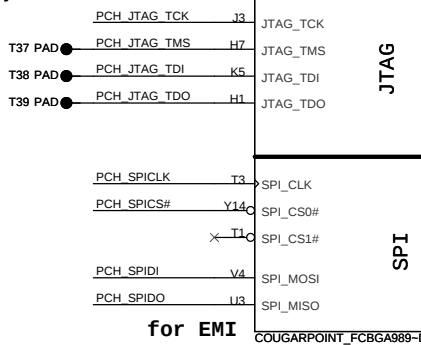
Socket: SP07000F500/SP07000H900

Please close to U2 PCH

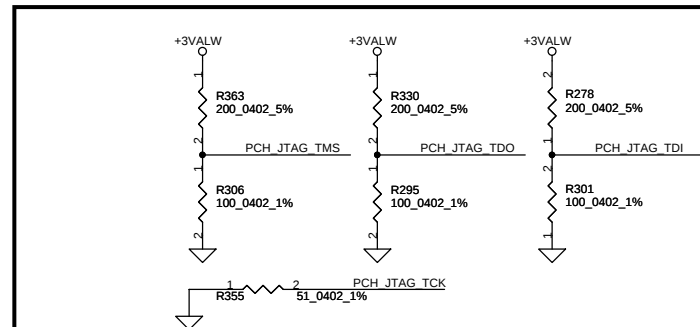
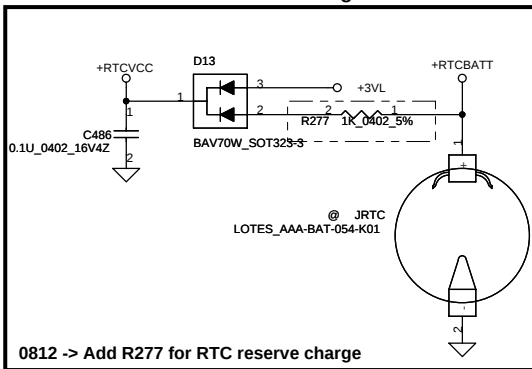
8/30 Change U13 from SA000021A00 to SA000031N00 due to EOL of SA000021A00



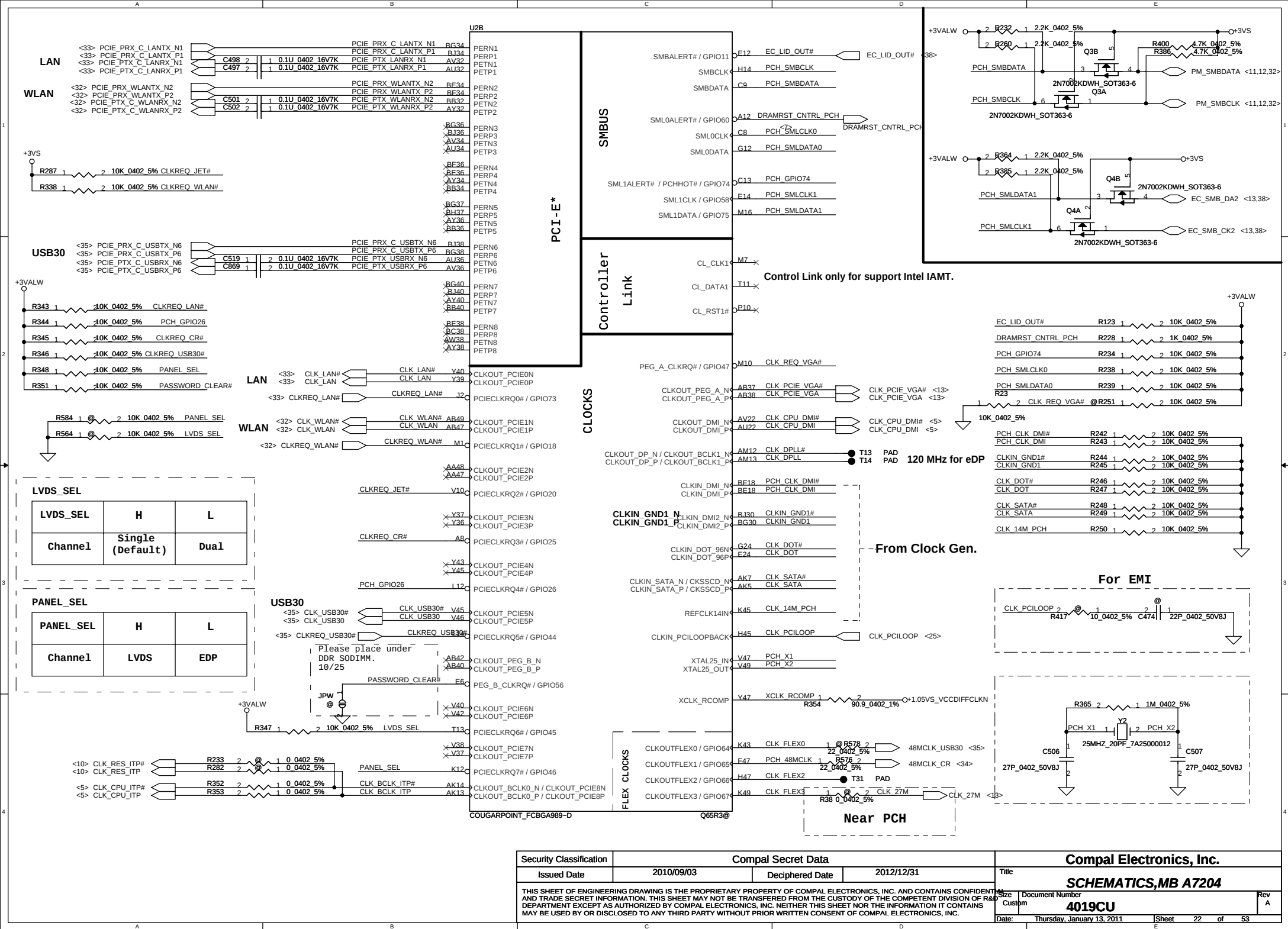
8/30 Change PWRME_CTRL# to HDA_SDO by PCH EDS



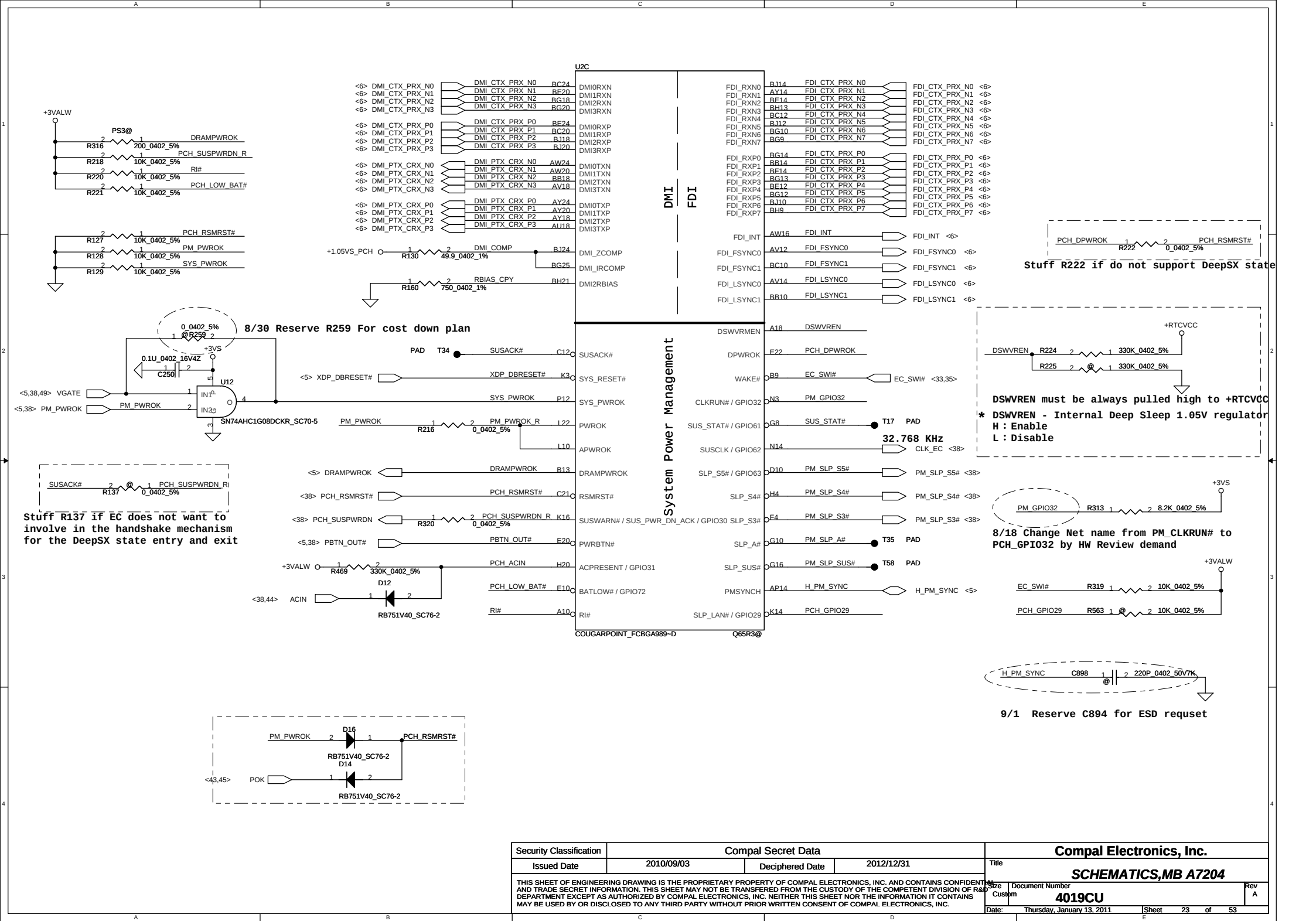
RTC schematic for non-chargeable

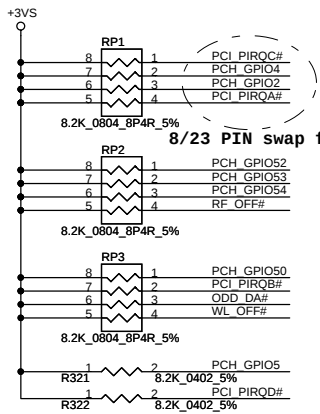


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				Custom	4019CU
				Date	Thursday, January 13, 2011
				Sheet	21 of 53
				Rev	A

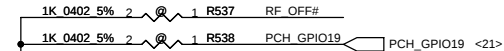


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						Size		Document Number		Rev	
						Custom		4019CU		A	
						Date:		Thursday, January 13, 2011		Sheet 22 of 53	





Boot BIOS Strap		
RF_OFF#	PCH_GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *



A16 Swap Override Strap	
WL_OFF#	
*	Low= A16 swap override Enable High= A16 swap override Disable



<32> WL_OFF#

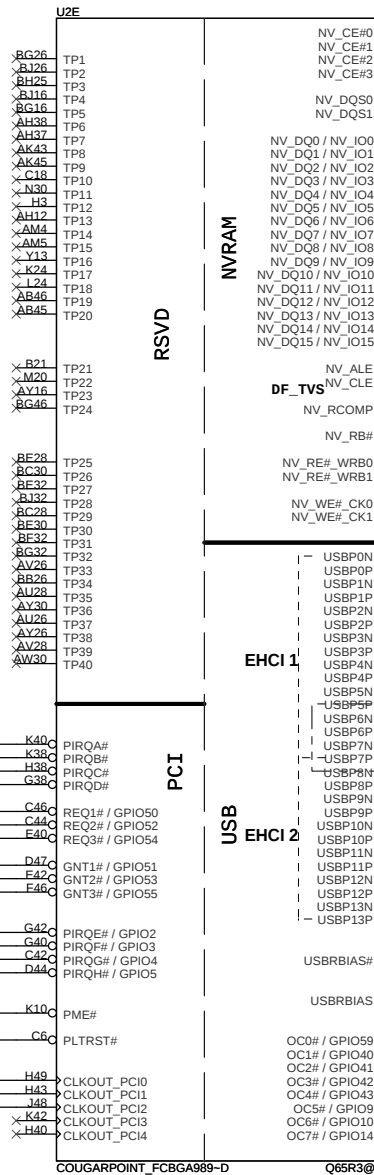
<31> ODD_DA#

T32 PAD

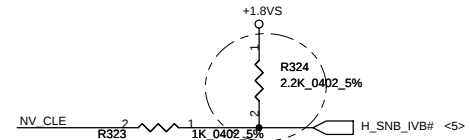
PLT_RST#

<38> CLK_PCI_EC
 <22> CLK_PCILoop
 <39> CLK_PCI_DDR

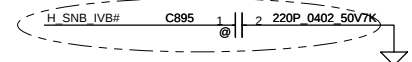
22 0402 5% 1 R525 CLK_EC_R
 22 0402 5% 1 R526 CLK_PCH
 22 0402 5% 1 R527 CLK_SIO



DMI & FDI Termination Voltage	
NV_CLE	
	Set to VCC when HIGH Set to VSS when LOW

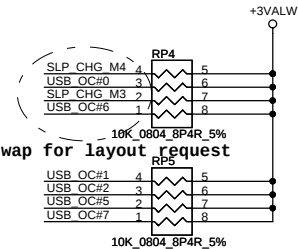


8/18 Change R324 From 1K to 2.2K by Intel check list demand



9/1 Reserve C895 for ESD request

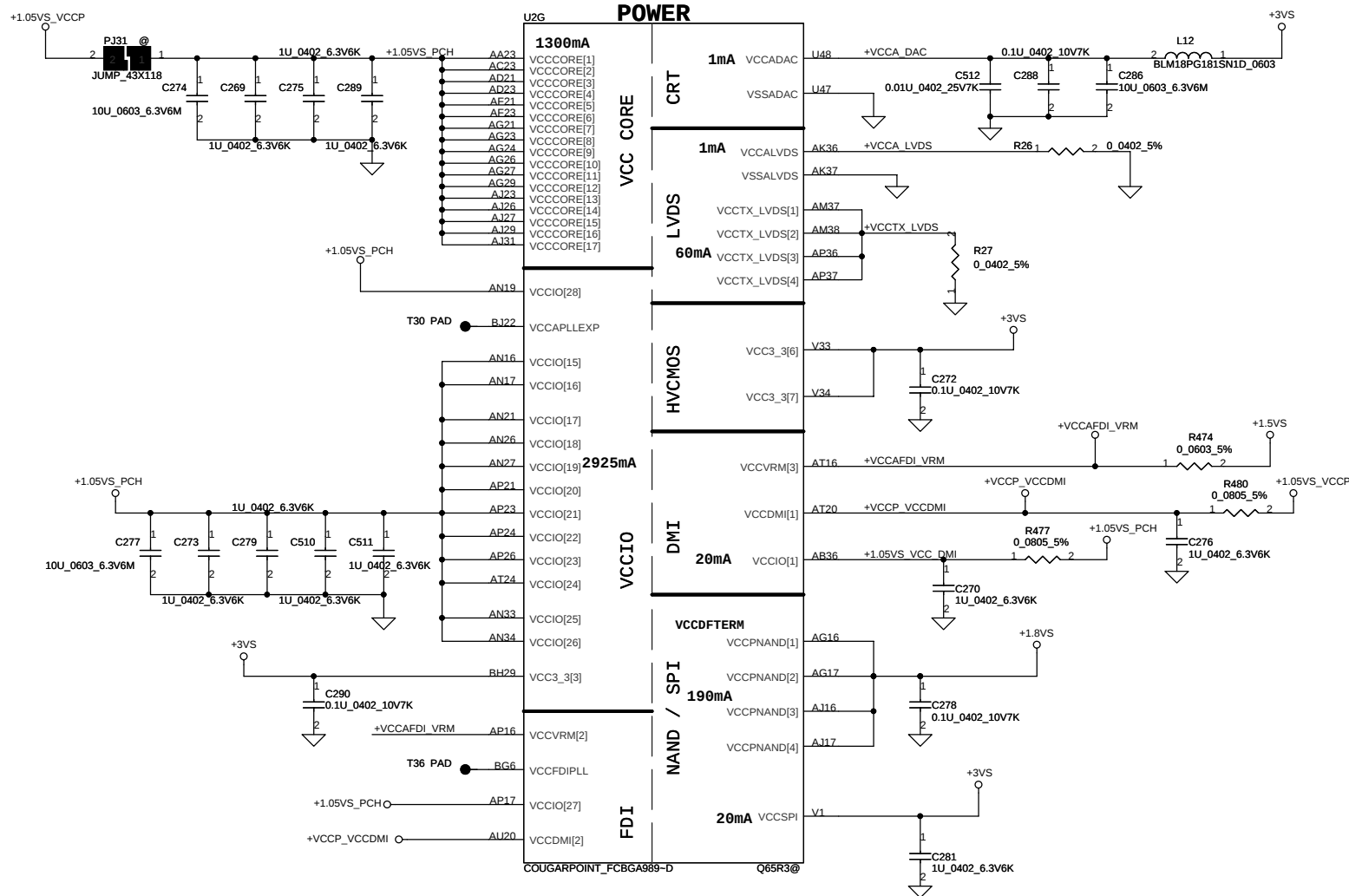
USB port6 and port7 are disabled on HM65



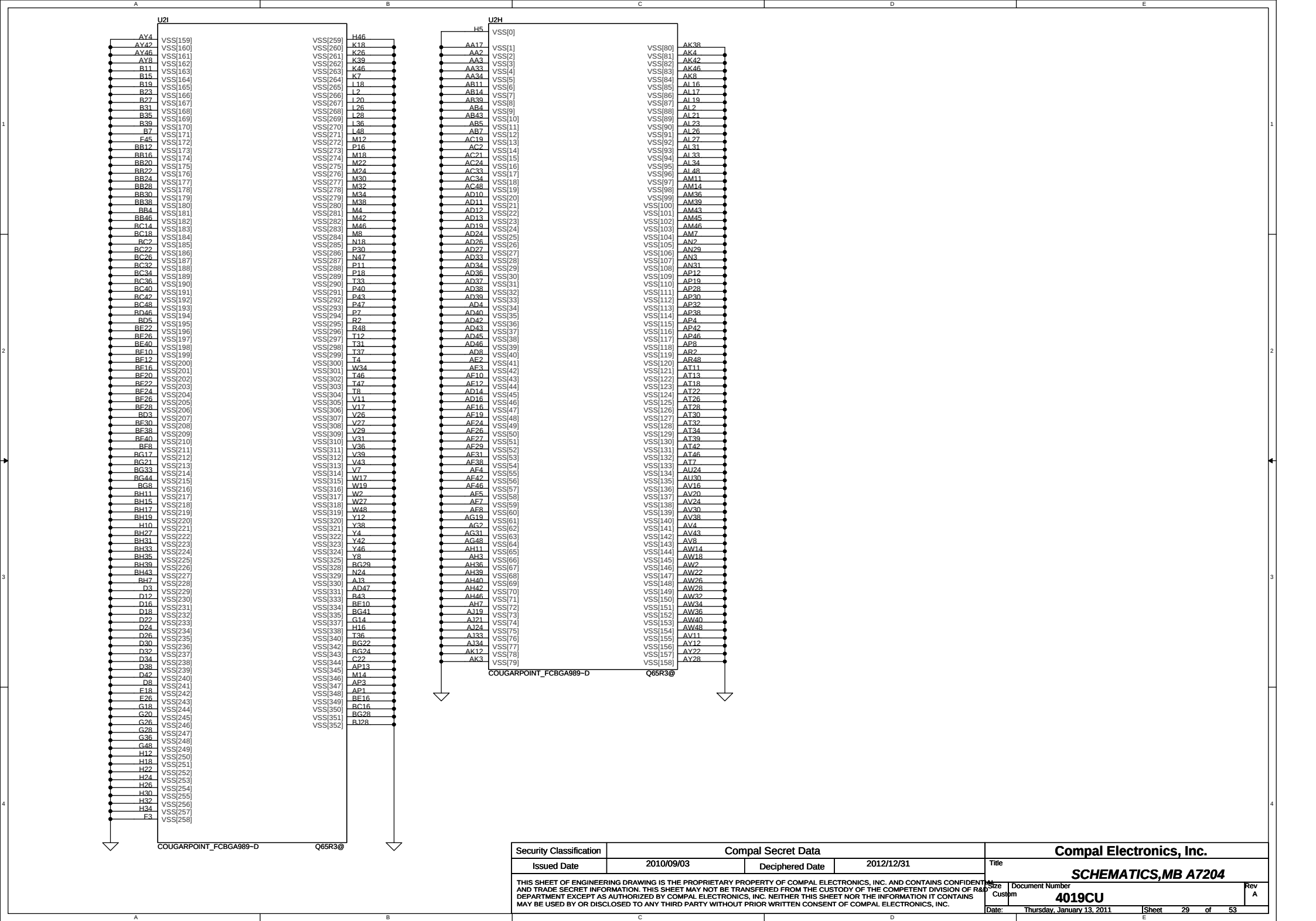
8/23 PIN swap for layout request

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				Date	Thursday, January 13, 2011
				Sheet	25 of 53

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				Custom	4019CU	A
				Date:	Thursday, January 13, 2011	Sheet 26 of 53



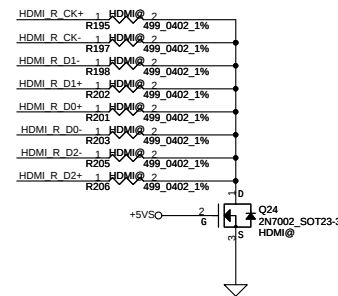
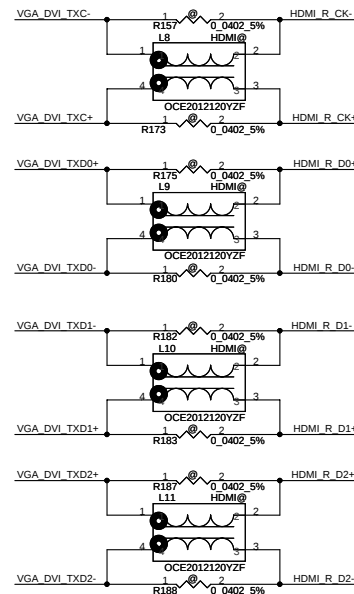
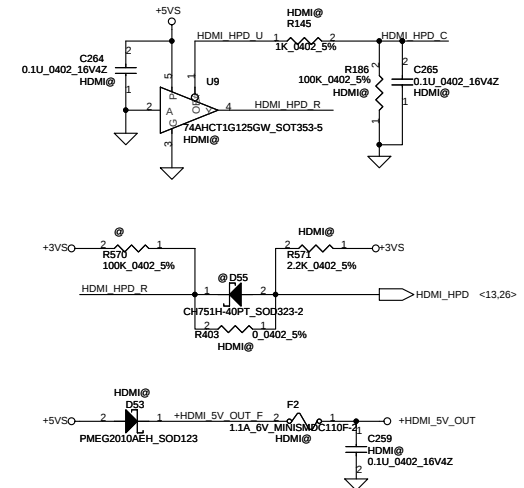
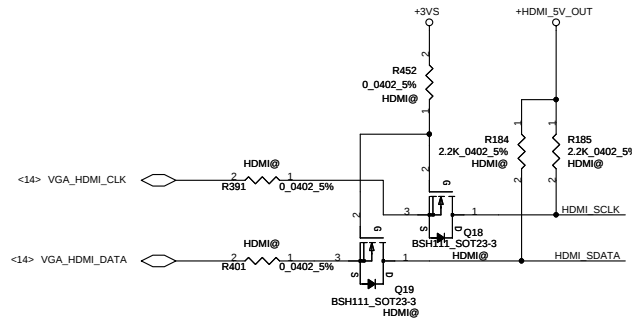
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_I0	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCADAC	3.3	0.001
VCCADPLLA	1.05	0.08
VCCADPLLB	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTERM	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3	0.97
VCCSushDA	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCTX_LVDS	1.8	0.06



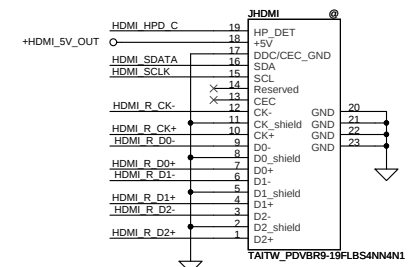
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				4019CU	A
Date:		Thursday, January 13, 2011		Sheet	29 of 53

For DISCRETE

<14> VGA_HDMI_CLK+	CV296	1	2	0.1U 0402 16V7K HDMI@	VGA DVI_TXC+
<14> VGA_HDMI_CLK-	CV293	1	2	0.1U 0402 16V7K HDMI@	VGA DVI_TXC-
<14> VGA_HDMI_TX0+	CV294	1	2	0.1U 0402 16V7K HDMI@	VGA DVI_TXD0+
<14> VGA_HDMI_TX0-	CV297	1	2	0.1U 0402 16V7K HDMI@	VGA DVI_TXD0-
<14> VGA_HDMI_TX1+	CV299	1	2	0.1U 0402 16V7K HDMI@	VGA DVI_TXD1+
<14> VGA_HDMI_TX1-	CV298	1	2	0.1U 0402 16V7K HDMI@	VGA DVI_TXD1-
<14> VGA_HDMI_TX2+	CV295	1	2	0.1U 0402 16V7K HDMI@	VGA DVI_TXD2+
<14> VGA_HDMI_TX2-	CV300	1	2	0.1U 0402 16V7K HDMI@	VGA DVI_TXD2-

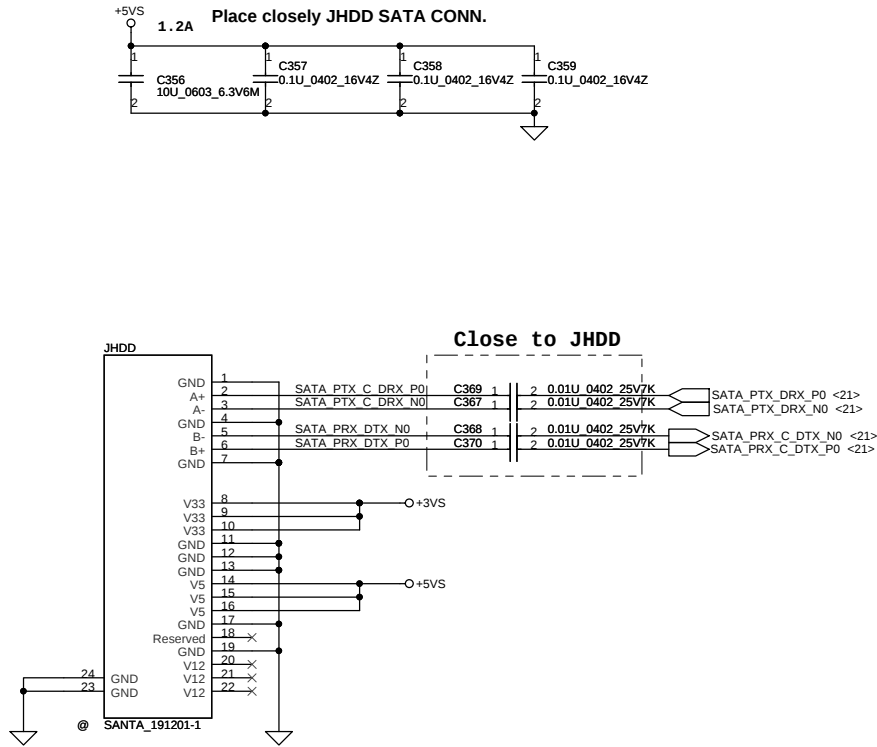


HDMI Connector

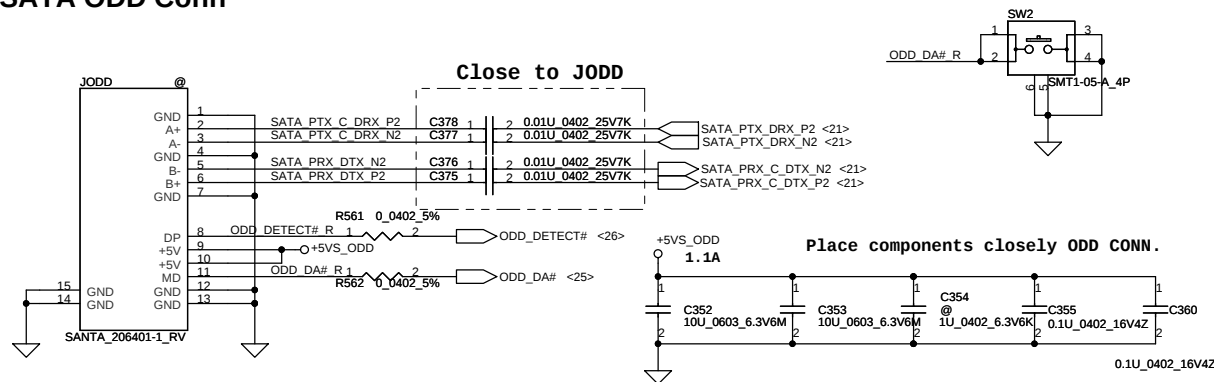


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				4019CU	Rev A
				Date	Thursday, January 13, 2011
				Sheet	30 of 53

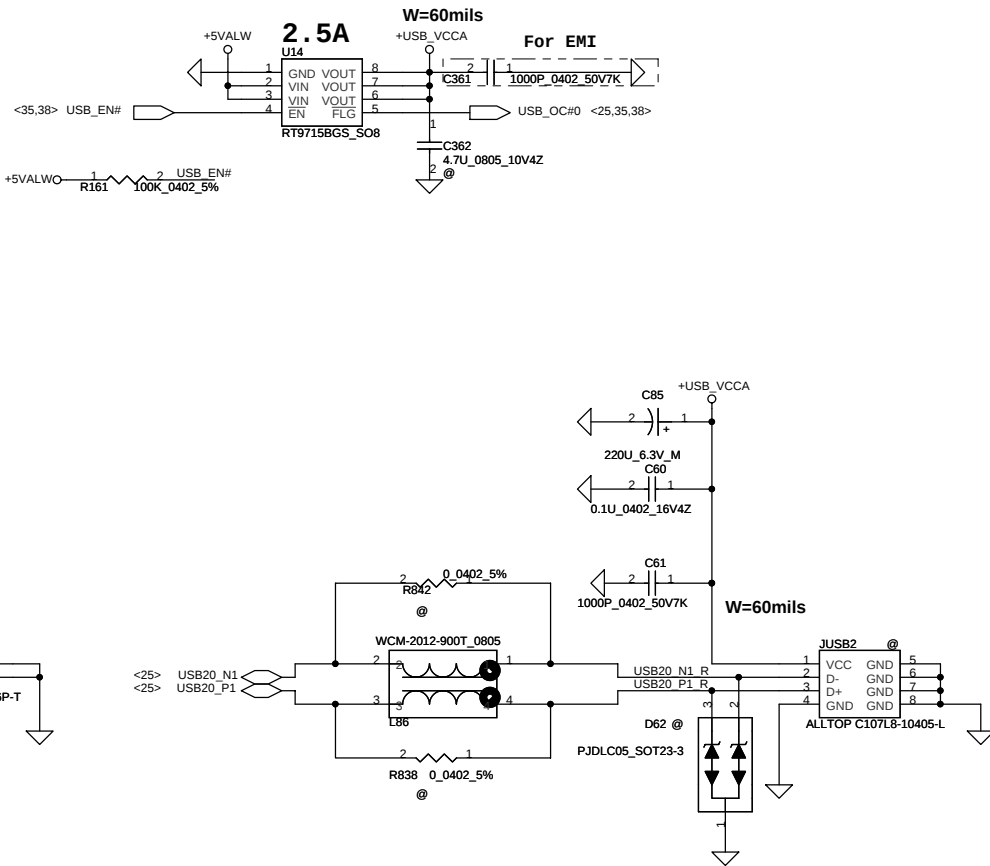
SATA HDD Conn



SATA ODD Conn

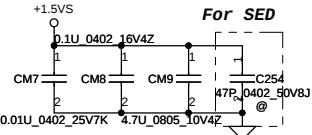
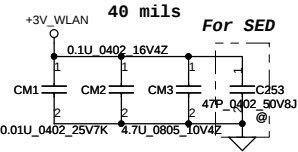
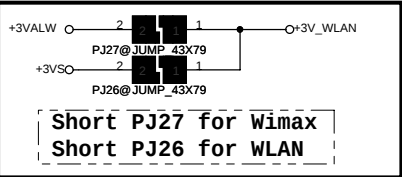


USB Conn



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						Size		Document Number		Rev A	
								4019CU			
Date:						Thursday, January 13, 2011		Sheet 31 of 53			

Half PCIe Mini Card-WLAN/ WiMax

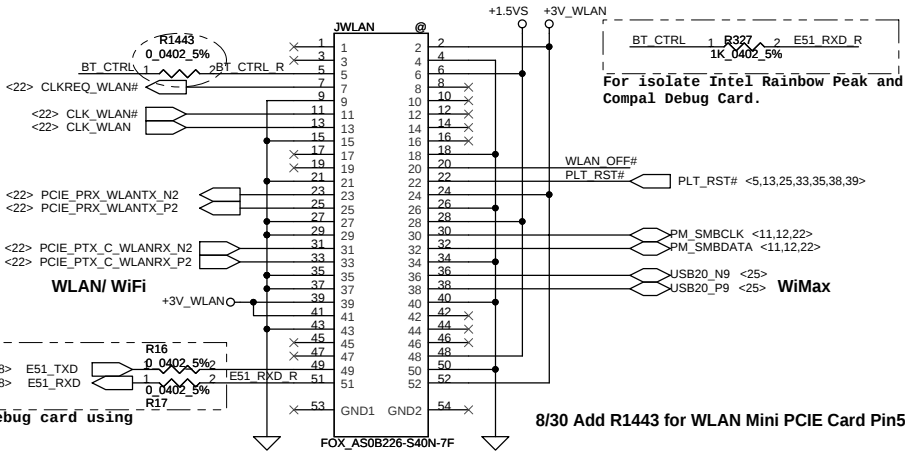
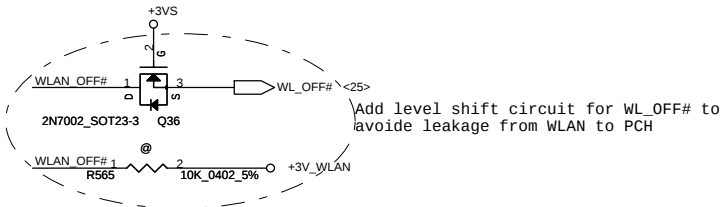
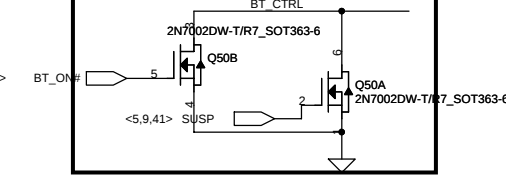


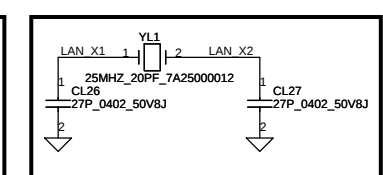
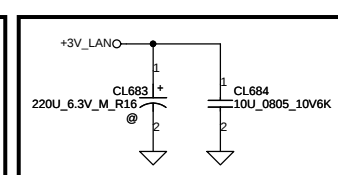
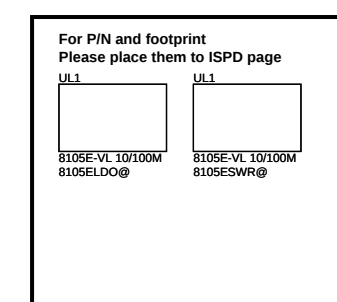
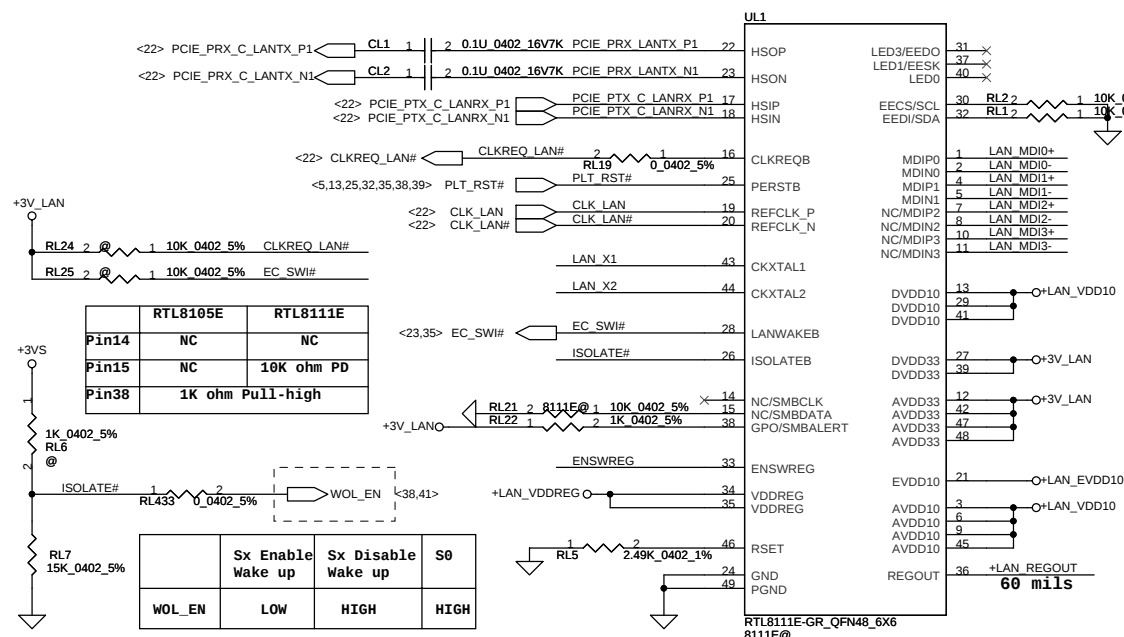
<26> BT_ON#

WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H

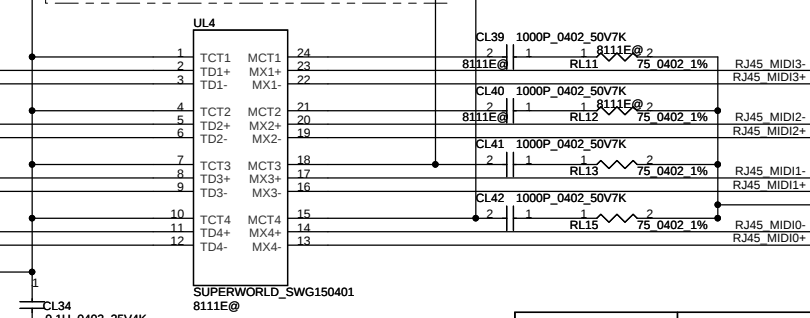
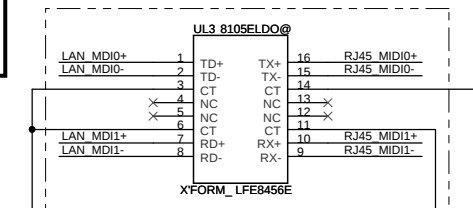
**If +3V_WLAN is +3VS, please remove D24



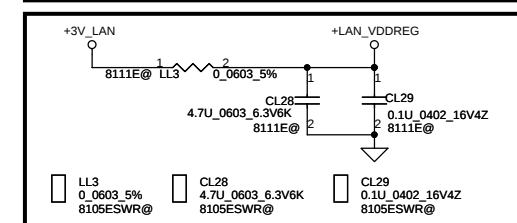
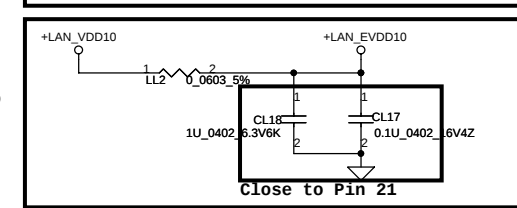
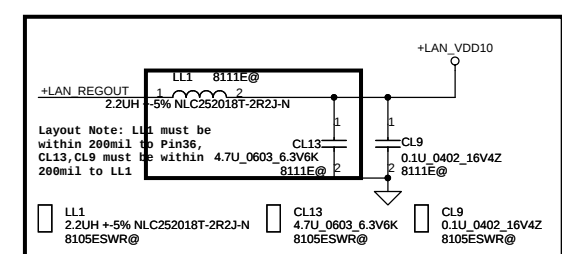


FOR EMI ISN TEST DEMAND.

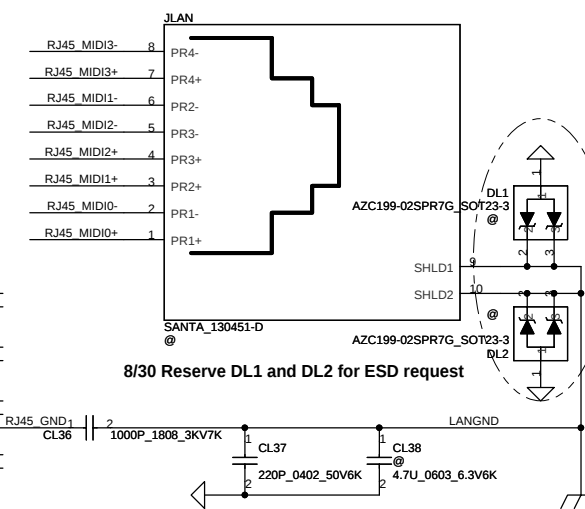
8/30 Add UL3 at DVT



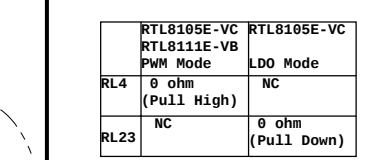
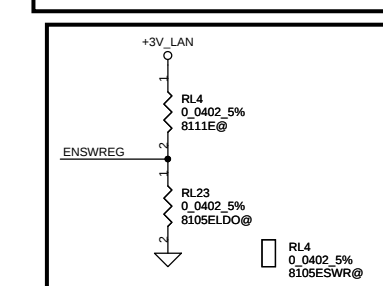
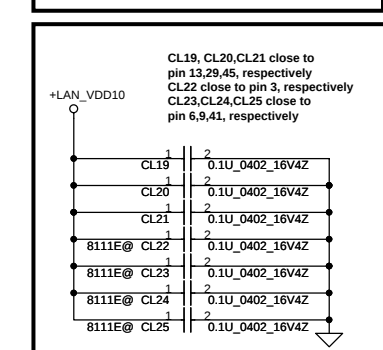
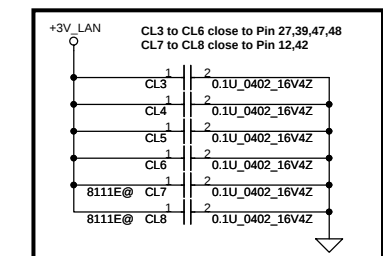
Place CL34, CL35 close to LAN chip

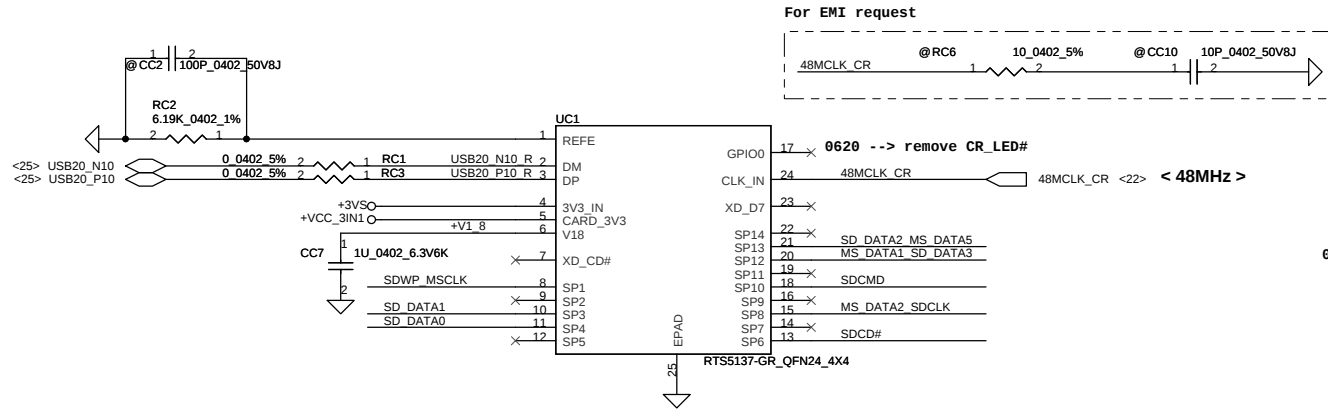


LAN Conn.



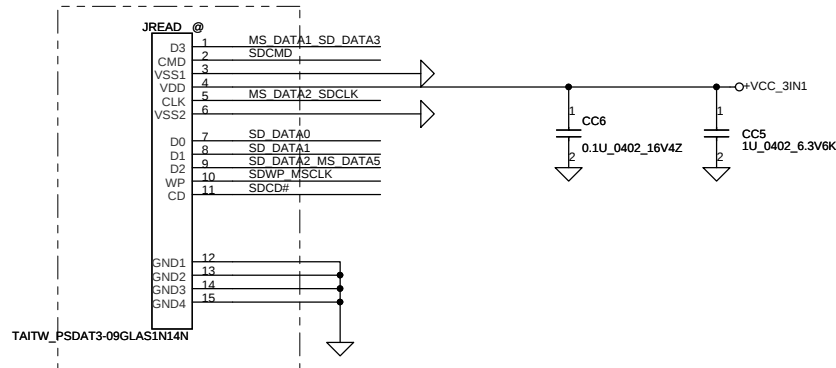
8/30 Reserve DL1 and DL2 for ESD request



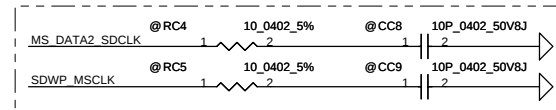


< 2 in 1 Card Reader >

0624 --> change CARDREADER conn.

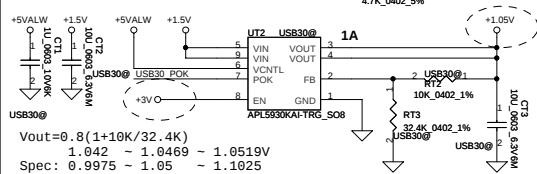


For EMI request

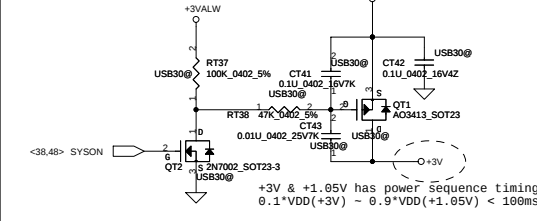


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				Document Number	Rev A
				Date	Thursday, January 13, 2011
				Sheet	34 of 53

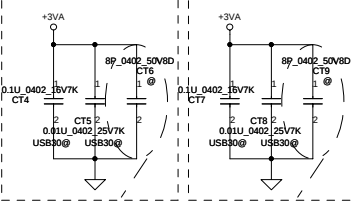
+1.5V to +1.05V Transfer



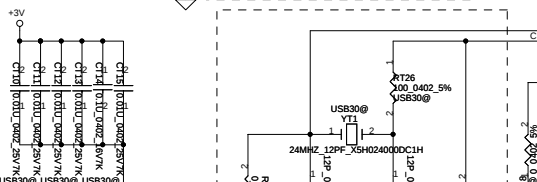
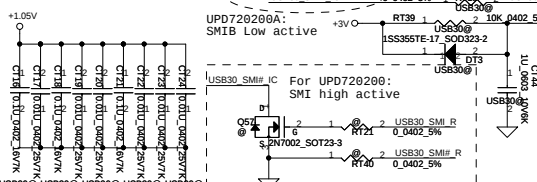
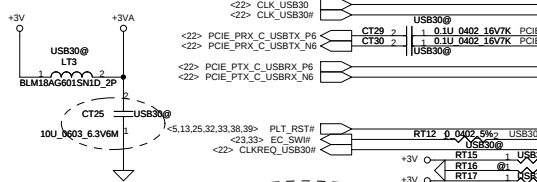
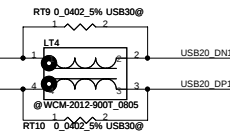
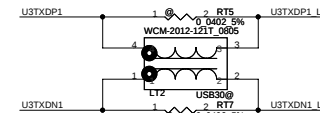
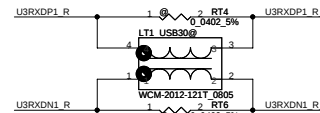
+3VALW to +3V Transfer



Close to U102.D7 Close to U102.P13

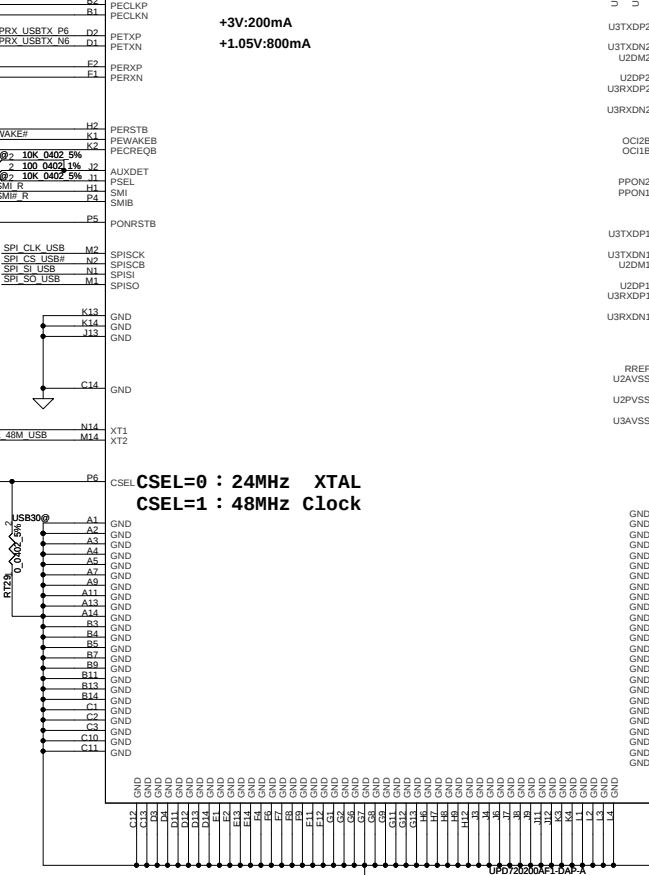
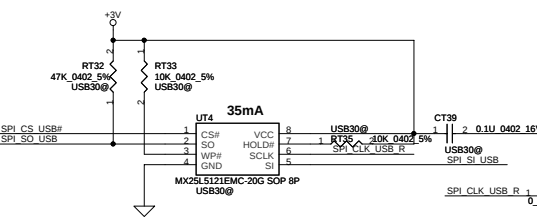


Follow Vendor recommend.



Place as close as possible to U102.N14 and U102.M14

9/2 Change CT25 from SE093106K80 (10uF_0805) to SE00005T80 (10uF_0603) by sourcer demand

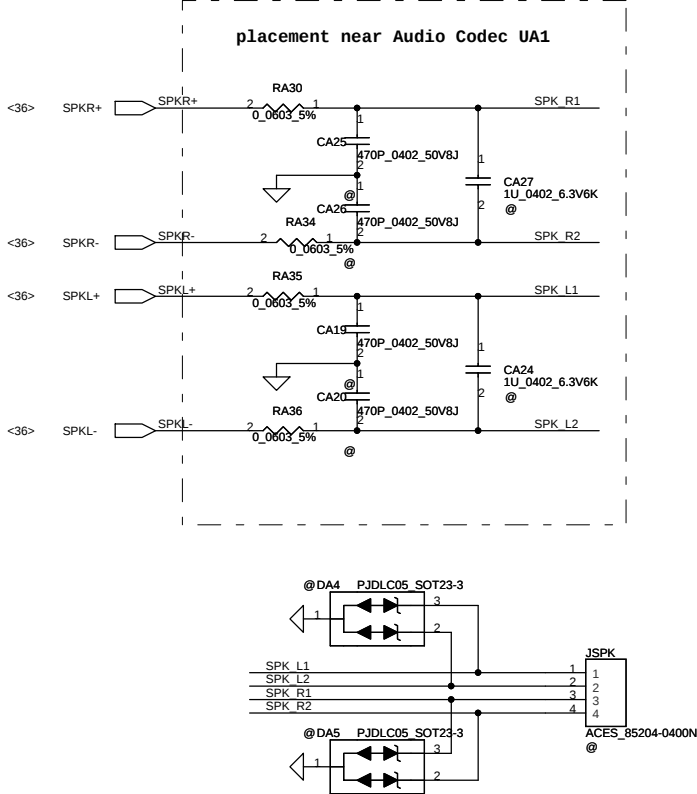


CSEL=0 : 24MHz XTAL
CSEL=1 : 48MHz Clock

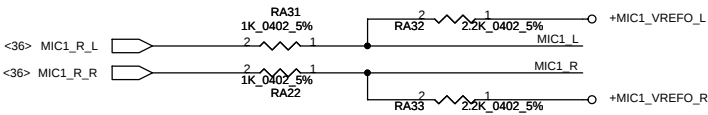
Close to U37.6

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Issued Date	2010/09/03	Deciphered Date	2012/12/31	SCHEMATICS, MB A7204	
Size		Document Number		4019CU	
Date		Thursday, January 13, 2011		Sheet 35 of 53	

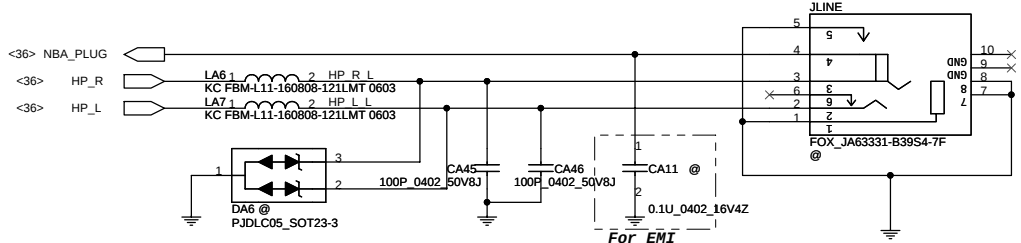
Speaker Connector



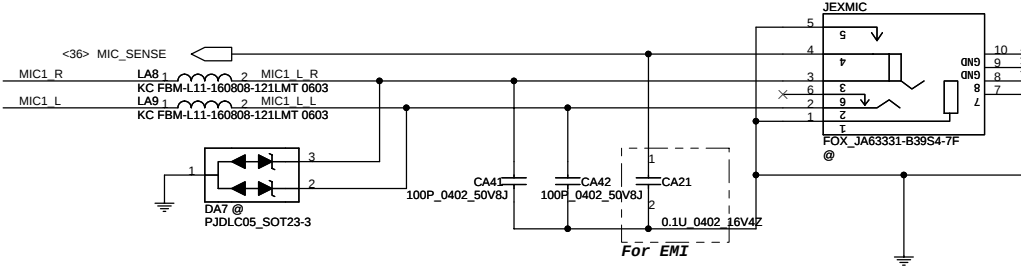
Ext. Mic



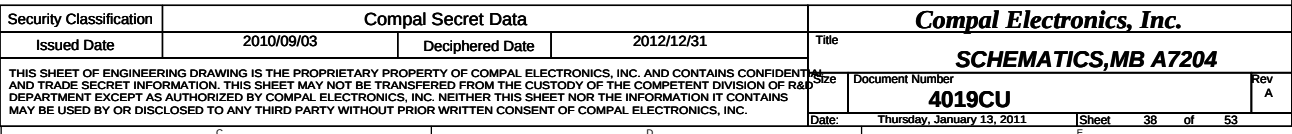
HeadPhone/LINE Out JACK



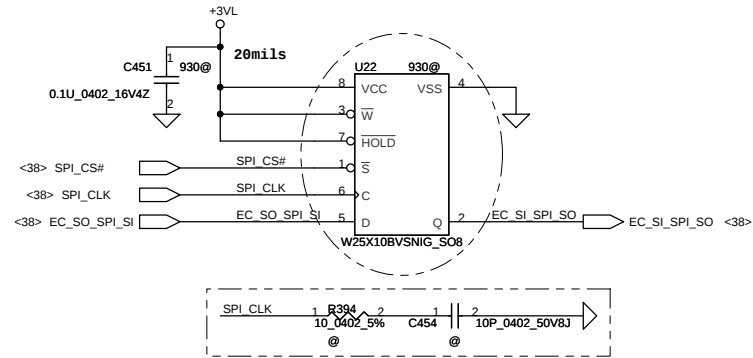
Ext.MIC/LINE IN JACK



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				Date	Thursday, January 13, 2011
				Sheet	37 of 53



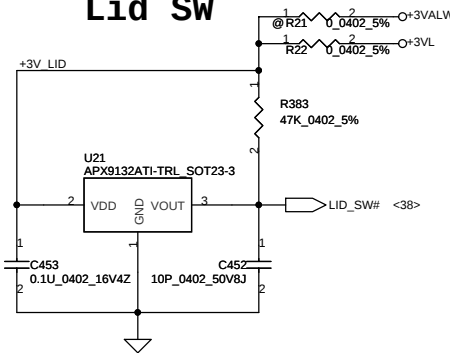
SPI Flash (256KB)



8/30 Change U22 From SA00003GK00 to SA00003GM10 due to EOL of SA00003GK00

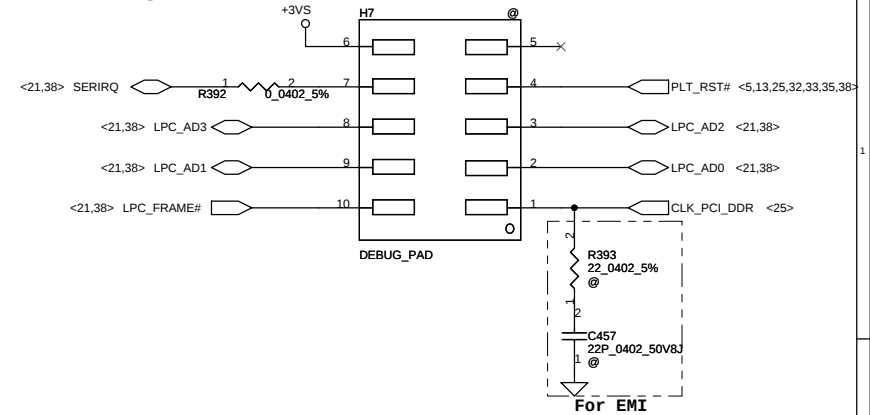
9/03 Change U22 change to SA00003FL10

Lid SW



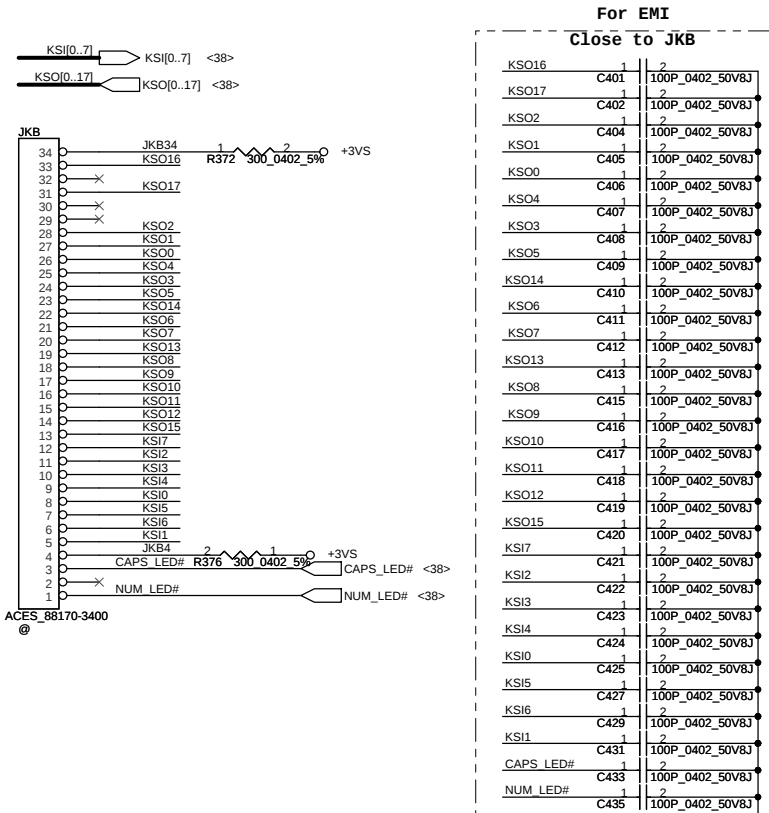
LPC Debug Port

Place the PAD under DDR DIMM.



KEYBOARD CONN.

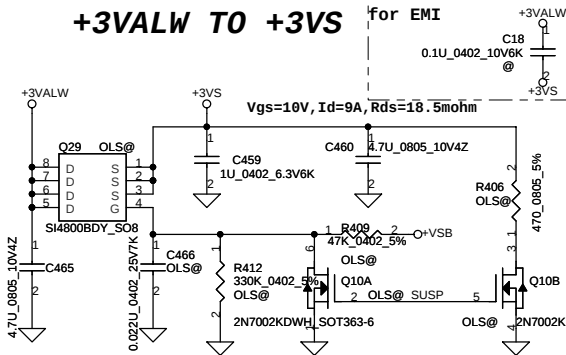
Noticed: KB Connector Pin Definition
Reversed with KB Membrane Pin Definition



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				4019CU	
				Date:	Thursday, January 13, 2011
				Sheet	39 of 53

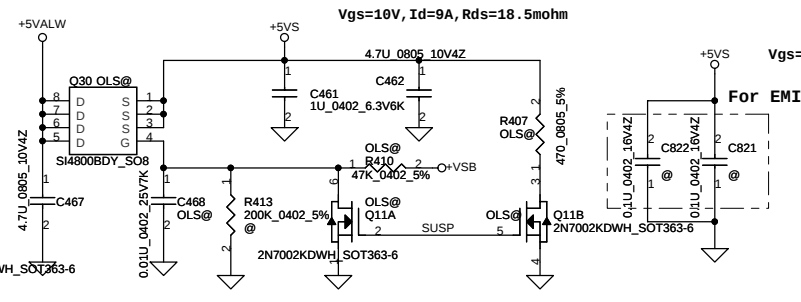
+3VALW TO +3VS

for EMI



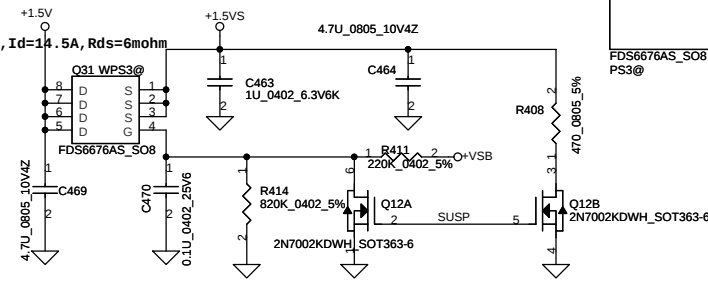
+5VALW TO +5VS

Vgs=10V, Id=9A, Rds=18.5mohm

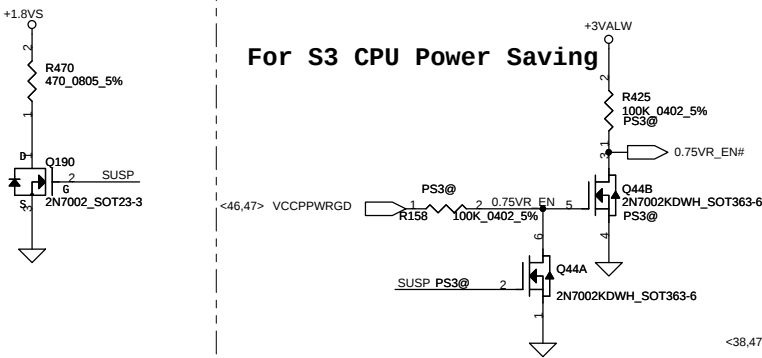


+1.5V to +1.5VS

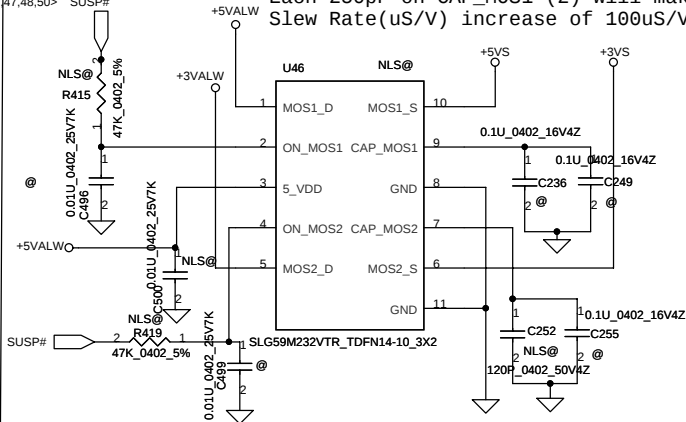
Vgs=10V, Id=14.5A, Rds=6mohm



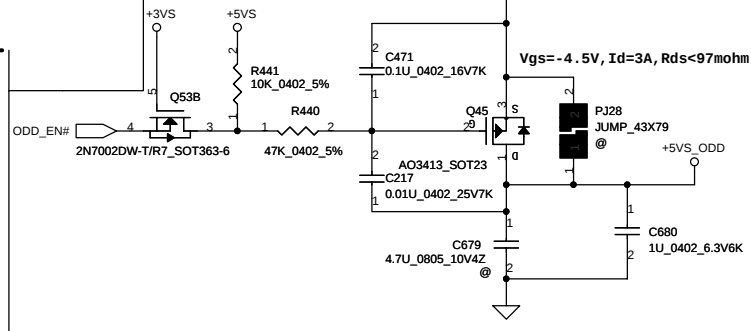
For S3 CPU Power Saving



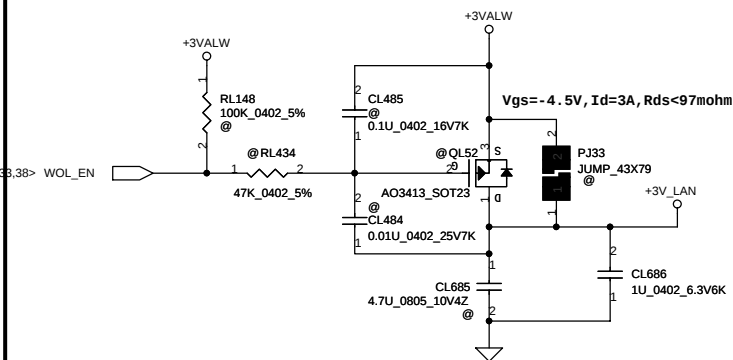
Each 250pF on CAP_MOS1 (2) will make Slew Rate(uS/V) increase of 100uS/V



+5VS TO +5VS_ODD



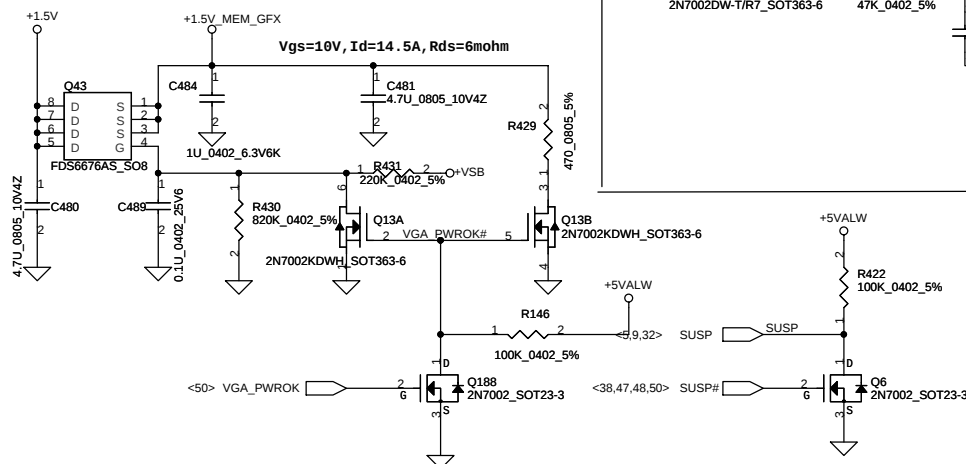
+3VALW TO +3V_LAN



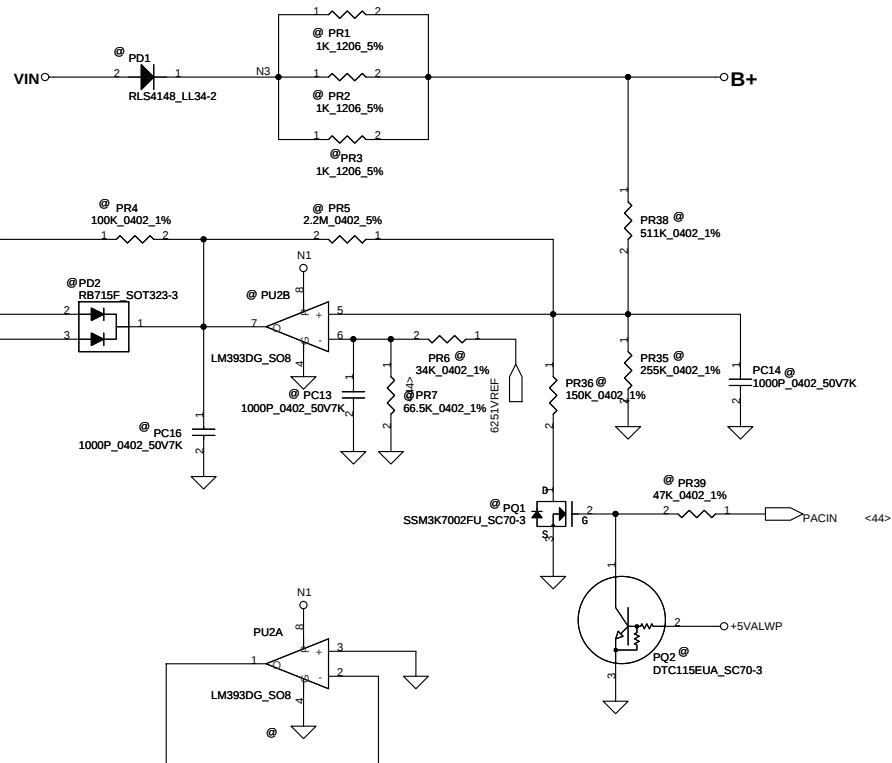
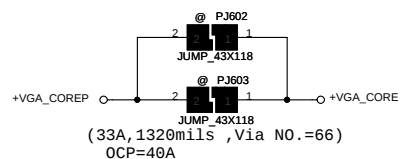
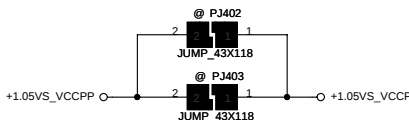
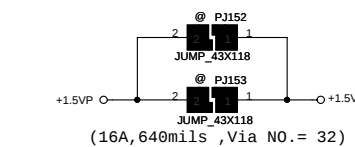
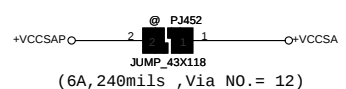
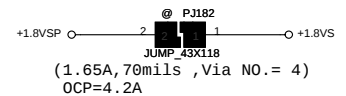
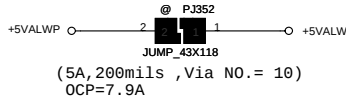
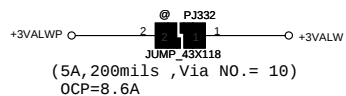
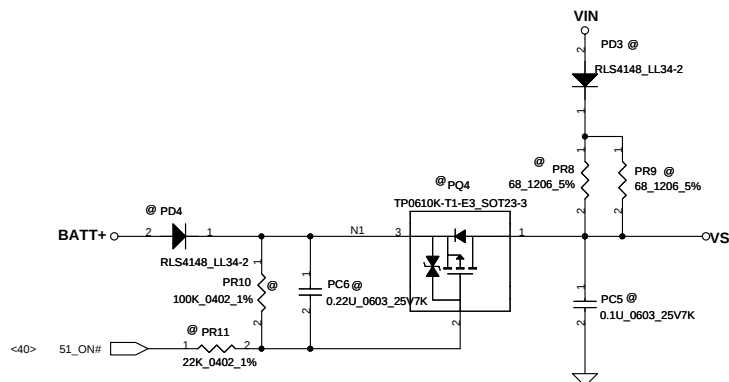
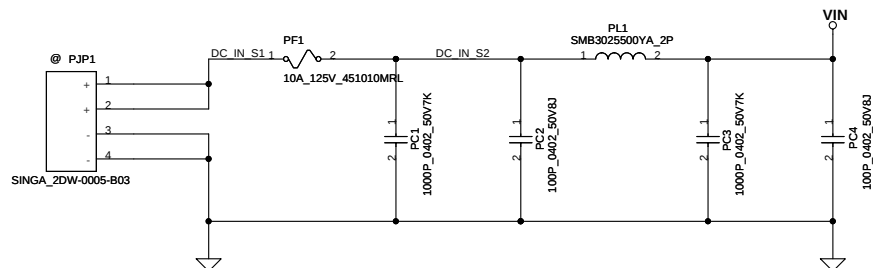
+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

+1.5V to +1.5V_MEM_GFX

Vgs=10V, Id=14.5A, Rds=6mohm

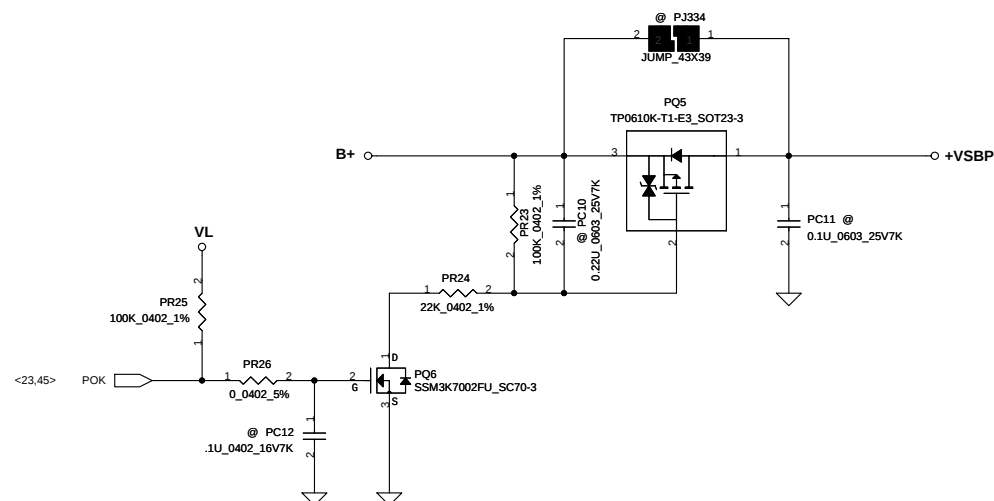
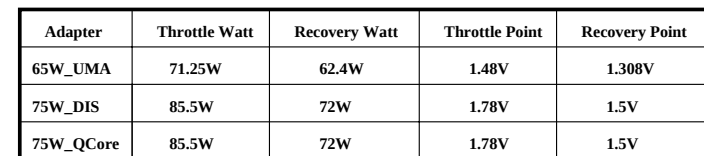
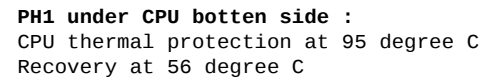


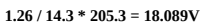
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4019CU				Document Number	Rev A
Date: Thursday, January 13, 2011				Sheet	41 of 53



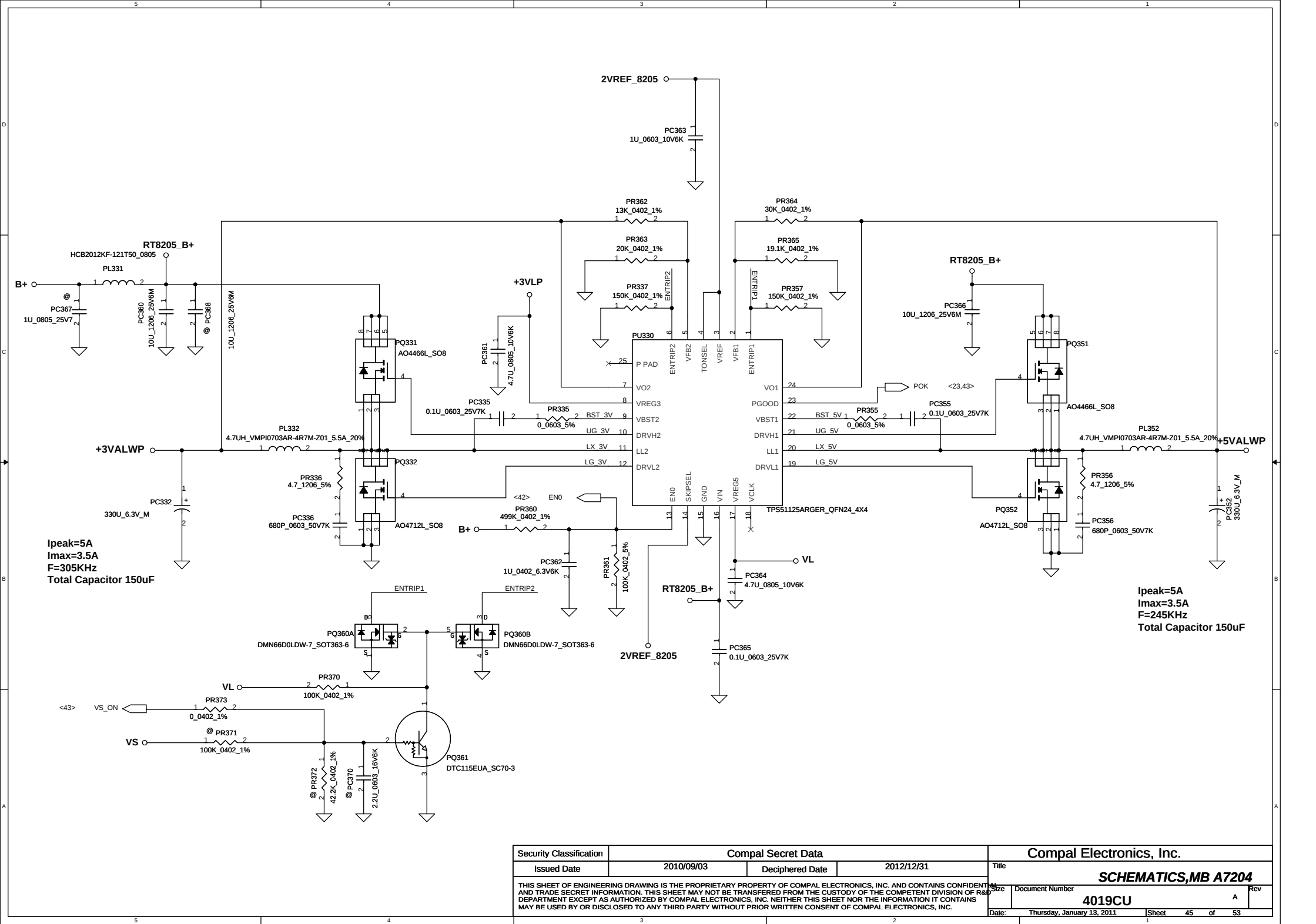
ACIN			
Precharge detector			
	Min.	typ.	Max
H->L	14.42V	14.74V	15.23V
L->H	15.39V	15.88V	16.39V

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4019CU				Date: Thursday, January 13, 2011				Sheet 42 of 53			

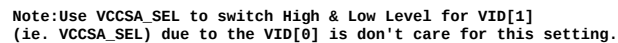




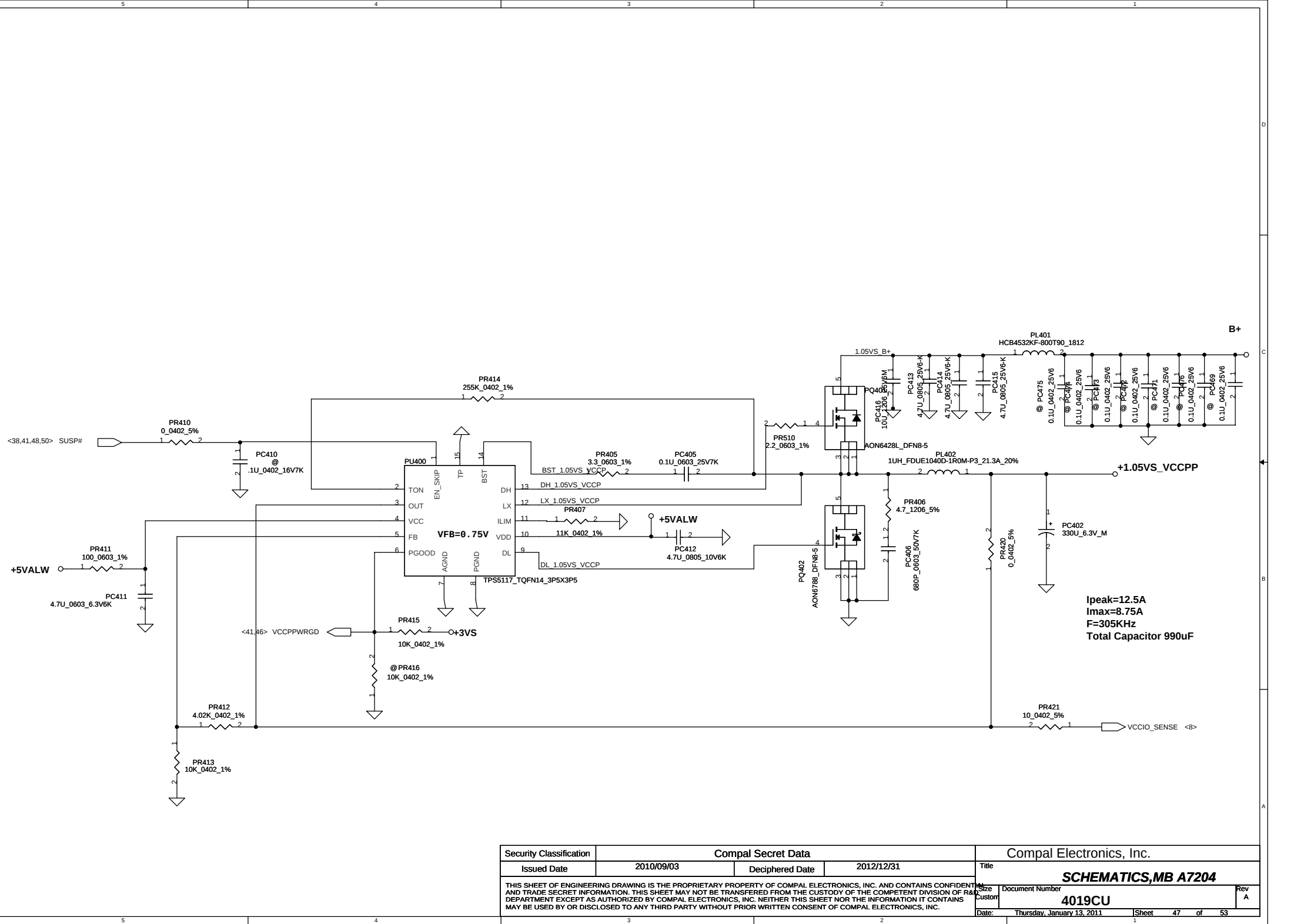
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				Date	4019CU		A
				Thursday, January 13, 2011		Sheet	44 of 53



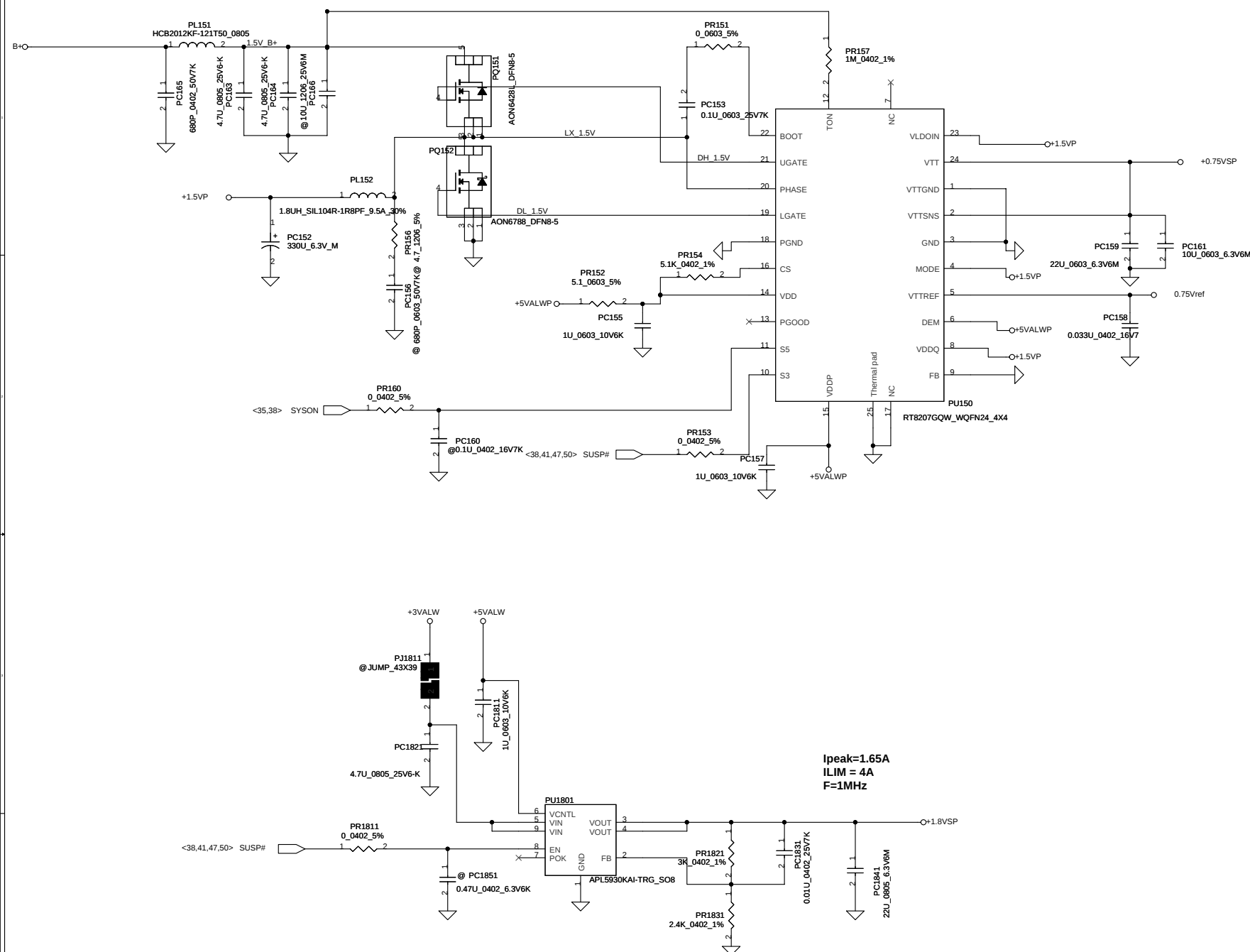
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				4019CU	A
				Date	Thursday, January 13, 2011
				Sheet	45 of 53

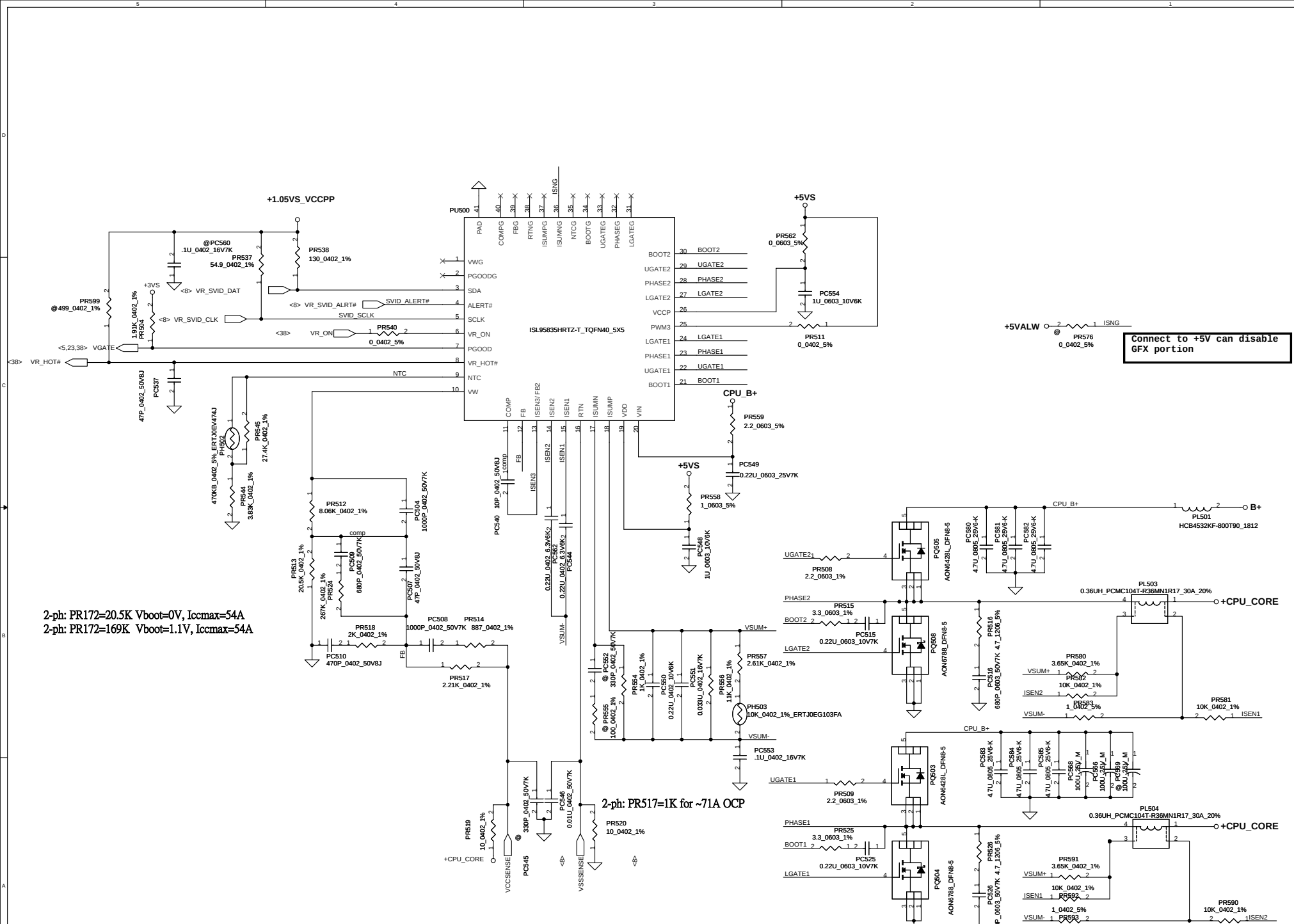


Date: Thursday, January 13, 2011 Sheet 46 of 53



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				Date	Thursday, January 13, 2011
				Sheet	47 of 53





2-ph: PR172=20.5K Vboot=0V, Iccmax=54A
2-ph: PR172=169K Vboot=1.1V, Iccmax=54A

2-ph: PR517=1K for ~71A OCP

Connect to +5V can disable
GFX portion

+CPU_CORE	+GFX_CORE
Iocp=72A, IccMAX=53A	Iocp=40A, IccMAX=24A
Load line=1.9mohm	Load line=3.9mohm
DCR=1.1mohm	DCR=1.1mohm

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				4019CU
				Rev A
				Date: Thursday, January 13, 2011 Sheet 49 of 53

	A		B		C		D		E
NO	DATE	PAGE	MODIFICATION LIST			PURPOSE			

1	2010/04/20	P36-P45	Release						

HW PIR (Product Improve Record)

PWWHA LA-7201P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2010/10/29

NO	DATE	PAGE	MODIFICATION LIST
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PURPOSE

1	10/29	17	SWAP FBA_CMD2 and FBA_CMD11	Schematic error
2	10/29	18	SWAP FBA_CMD18 and FBA_CMD11	Schematic error
3	10/29	21	Chane +3V_SPI to +3VS	Schematic error
4	10/29	22	Add R23 for CLK_REQ_VGA#	Reserve pull down for clock request

REVISION CHANGE: 0.2 TO 0.3

GERBER-OUT DATE: 2010/11/11

NO	DATE	PAGE	MODIFICATION LIST
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PURPOSE

1	11/03	25,31	Add USB20_N9 & USB20_P9	Support Wimax
2	11/03	32	Co-Lay Giga LAN	Giga LAN support
3	11/22	22	Add R584 & R564 for Panel select	For HW common design
4	11/22	5	change D86 (SC100001M00)	For HW common design
5	11/22	5	cancel D85 @	For HW common design
6	11/24	32	LAN 8105E-VC update to 8105E-VL	For HW common design

REVISION CHANGE: 0.3 TO 0.4

GERBER-OUT DATE: 2010/12/29

NO	DATE	PAGE	MODIFICATION LIST
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PURPOSE

1	11/22	22	Add R584 & R564 for Panel select	For HW common design
2	11/22	5	change D86 (SC100001M00)	For HW common design
3	11/22	5	cancel D85 @	For HW common design
4	11/24	32	LAN 8105E-VC update to 8105E-VL	For HW common design
5	11/29	32	Add W0L_EN output pin	For HW common design
6	12/03	28,23	D7,D8,D12,D14,D16,D21 Change material	For HW common design
7	12/03	21	SC1N202U010 (CHENMKO) change use SC600000B00	For HW common design
8	12/03	21	change U13 and follow UMA schematics (45@)	For HW common design
9	12/03	19	R103 change use D1(SCS00002G00)	For HW common design
10	12/03	13	net VGA_BL_PWM change to VGA_PWM and Add D2	For HW common design
11	12/03	39	Add +5VS TO +5VS_ODD schematics for ODD	For PRD request
12	12/03	36	Add R349(100K)pull down for E51_TXD	For HW common design
13	12/07	30	JODD Pin8 add ODD_DETECT#	For PRD request
14	12/07	30	JODD Pin11 add ODD_DA#	For PRD request
15	12/07	30	Change +5VS to +5VS_ODD	For PRD request
16	12/14	15	+VGA_CORE add 330u (C876)	For HW common design
17	12/18	30	Add SW2	For test Zero power ODD
18	12/18	8	Add C3	To increase number of +CPU_CORE CAP
19	12/18	36	Add R739 to connect PM_SLP_S4# with SLP_S5#	For HW common design
20	12/18	5	Add FAN RPM circuit	For FAN BTO
21	12/19	30	Add USB3.0 function	For USB3.0 BTO
22	12/19	30	Cancel USB2.0(JUSB2)	For PRD request
23	12/19	27	Add HDMI function	For PRD request
24	12/23	19	change LVDS connectorFor PUR request	
25	12/24	41	Add U46	For Low Switch
26	12/24	28	Cancel R541,C514,C513,C256,L1	For HW common design
27	12/24	13	Add circuit for PCH to GPU 27Mhz	For HW test
28	12/29	38	Change EC Schematic	
29	12/29	33	Change UL3 material	For HW common design
30	12/29	17,18	Change UV3,UV4,UV5,UV6 material	For NVidia require
31	12/29	21	Change U2 material For PJE require	
32	12/29	2	Modify Block Diagram	

Update

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				Custom	4019CU
				Date:	Thursday, January 13, 2011
				Sheet	52 of 53
				Rev	A

HW PIR (Product Improve Record)

REVISION CHANGE: 0.3 TO 0.4

GERBER-OUT DATE: 2011/01/04

MODIFICATION LIST				PURPOSE
NO	DATE	PAGE		
1	01/04	41	Change C252 0.1u to 120p	Update HW design
2	01/04	19	Change C120 10K to 47K	Update HW design
3	01/04	5	Change U10,R312,C93 to PS3@	Update HW design
4	01/04	7	Change Q14,R463,C140,R465 to PS3@	Update HW design
5	01/04	9	Change C213,C212,C211,C210 to PS3@	Update HW design
6	01/04	23	Change R316 to PS3@	Update HW design