MODEL NAME : ZAVA1/ZAVC1
PCB NO : DA80011D000 LA-B015P-R1.0

Compal Confidential

Schematic Document

Intel BoardWell ULT
ZAVA1/ZAVC1
DIS AMD 25W/M2+DDR3x8

2014-10-17 Rev: 1.0

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Security Classification	Compal Secret Data		
Issued Date	2014/10/17	Deciphered Date	2018/04/30

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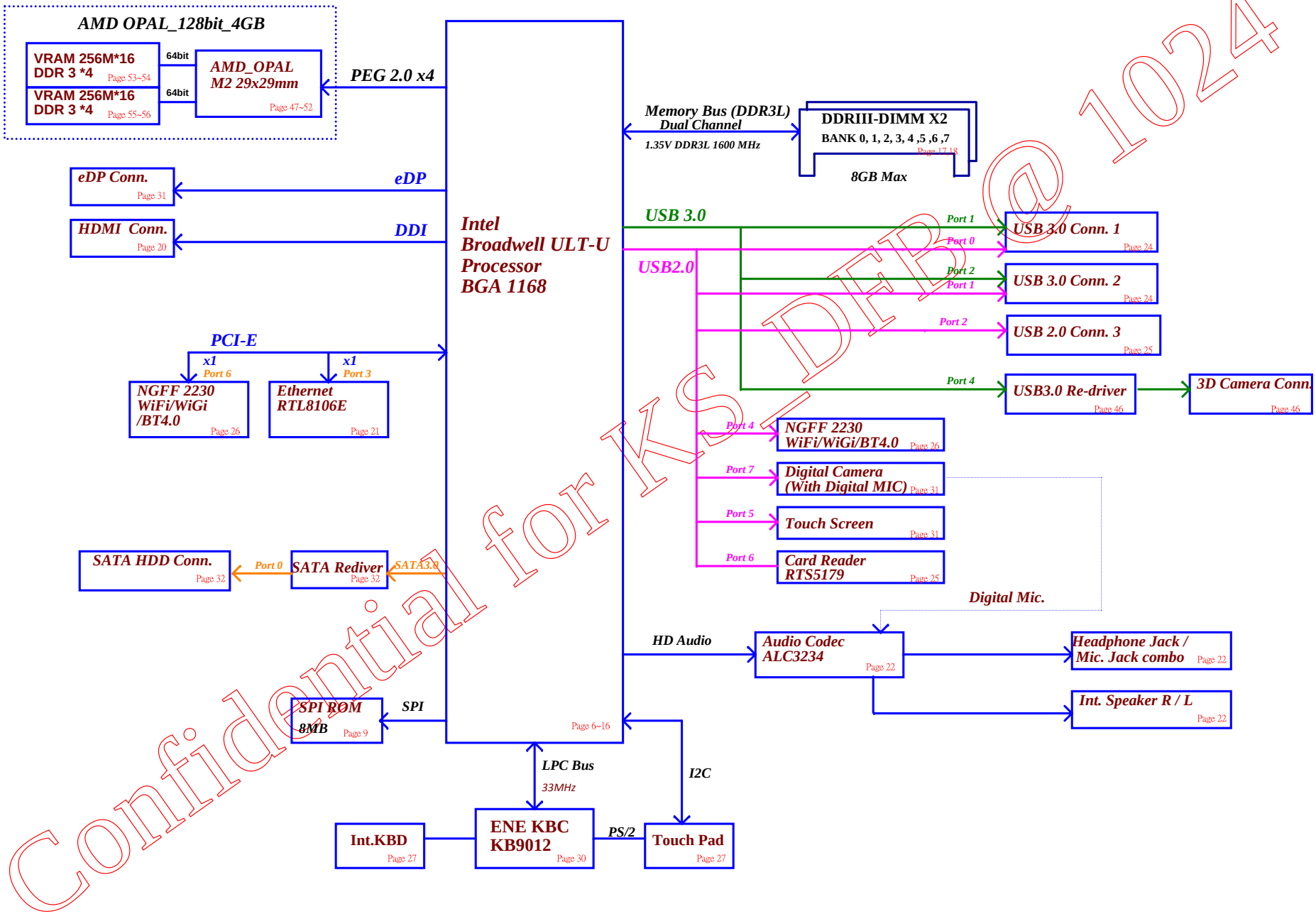
Compal Electronics, Inc.

Title: **Cover Page**

Document Number: **LA-B015P** Rev: 1.0

Date: Friday, October 17, 2014 Sheet 1 of 56



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Issued Date	2014/10/17	Deciphered Date	2018/04/30	Title: Block Diagram
				Size / Document Number: LA-B015P	Rev: 1.0
				Date: Friday, October 17, 2014	Sheet 2 of 56

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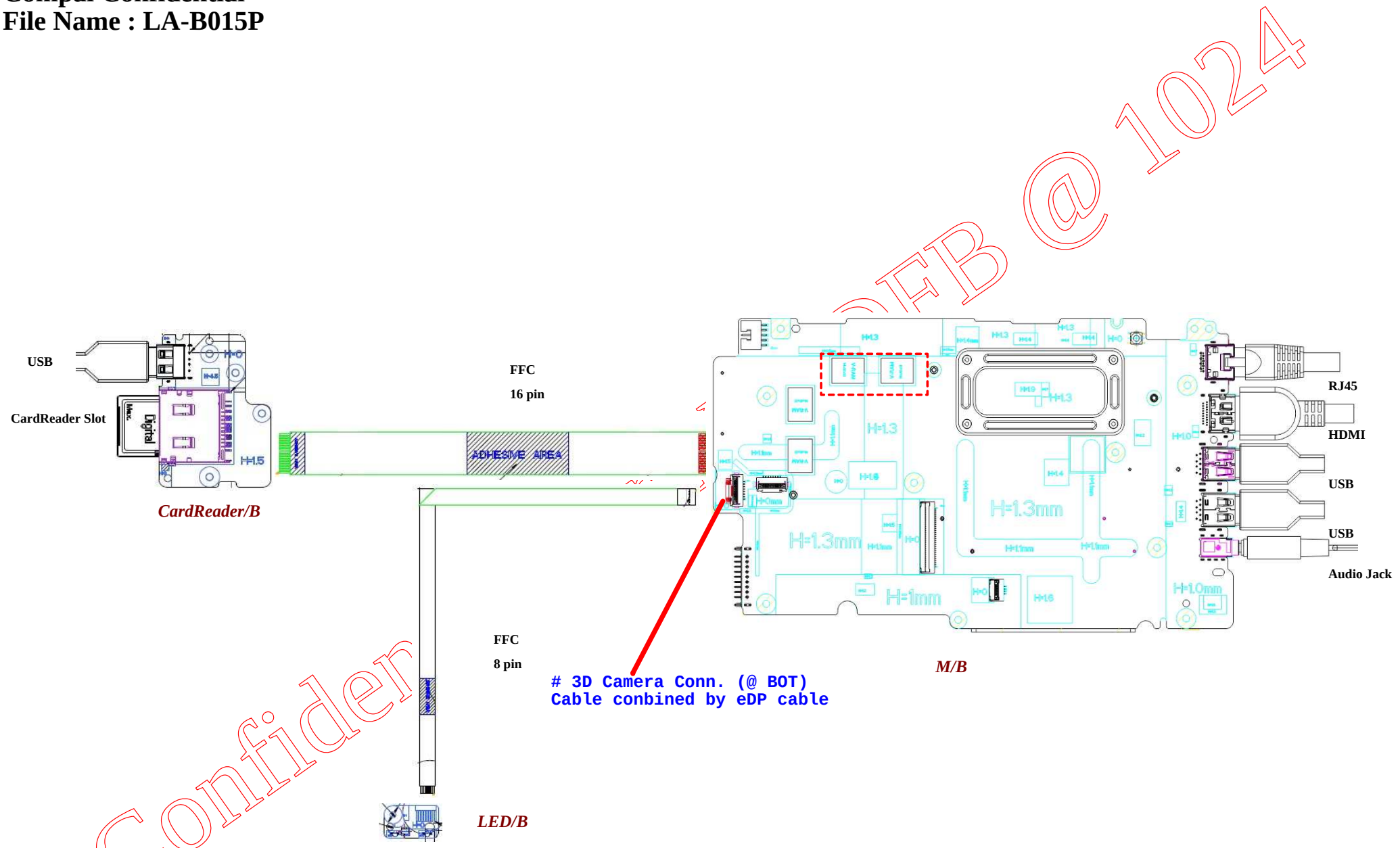

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Security Classification	Compal Secret Data		
Issued Date	2014/10/17	Deciphered Date	2018/04/30

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Compal Electronics, Inc.

Title: **MB/DB Drawing**

Size | Document Number: **LA-B015P** | Rev 1.0

Date: Friday, October 17, 2014 | Sheet 3 of 56

Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

	SOURCE	BATT	Charger	VGA	DIMM	XDP	Thermal Sensor	FFS
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9012			V			V	
SMBCLK SMBDATA	ULT				V			V
SML0CLK SML0DATA	ULT							
SML1CLK SML1DATA	ULT							

Link

Symbol Note :

: means Digital Ground

: means Analog Ground

HSW BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)	DIS(OPAL)
0	[redacted]			
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				

BDW BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)	DIS(OPAL)
0	1.0_3D CAM			
1		1.0_3D CAM		
2			1.0_3D CAM	
3	SSI(BDW)			
4		SSI(BDW)		
5			SSI(BDW)	
6	PT(BDW) SSI_3D CAM			
7		PT(BDW) SSI_3D CAM		
8			PT(BDW) SSI_3D CAM	
9	ST(BDW) PT_3D CAM			
10		ST(BDW) PT_3D CAM		
11			ST(BDW) PT_3D CAM	
12	1.0(BDW) ST_3D CAM			
13		1.0(BDW) ST_3D CAM		
14			1.0(BDW) ST_3D CAM	
15				SSI
16				PT
17				ST
18				1.0

CLOCK SIGNAL (Diff. 100MHz)	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

ULT		
	USB3.0	
	Port1	USB connector 1
	Port2	USB connector 2
	Port3	
	Port4	3D Camera
	USB2.0	
	Port0	USB connector 1
	Port1	USB connector 2
	Port2	USB connector 3 (D/B)
	Port3	
	Port4	MINI Card (WLAN)
	Port5	Touch Screen Panel
	Port6	Card Reader
	Port7	Camera
	PCI EXPRESS	
	Lane 1	
	Lane 2	
	Lane 3	10/100 LAN
	Lane 4	MINI Card (WLAN)
	Lane 5	PEG (AMD JET/TOBAZ)
	Lane 6	
	SATA	
	SATA0	HDD
	SATA1	
	SATA2	
	SATA3	

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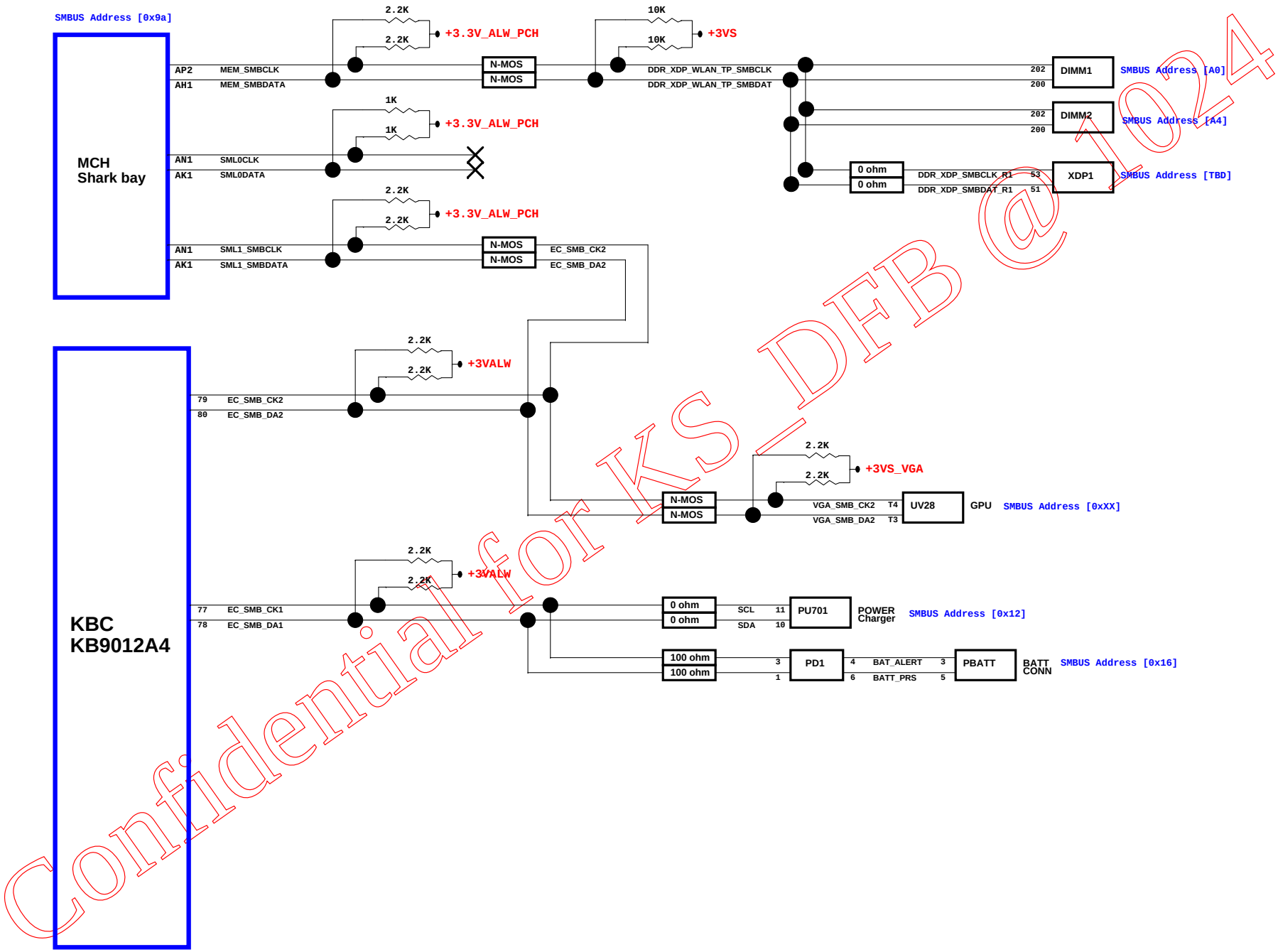

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Compal Electronics, Inc.

Title: **SMBus/I2C Connection Map**

Document Number: **LA-B015P** Rev 1.0

Date: Friday, October 17, 2014 Sheet 5 of 56

BDW_Pre-QS for DVT2 BDW_QS for DVT2

i3 CPU

i5 CPU

UC1 I5_1.2G@

CL8065801674128 QG21 C0 1.2G

SA00007OS0L

i7 CPU

UC1 I7_1.2G@

CL8065801675027 QG22 C0 1.2G

SA00007OT0L

i3 CPU

i5 CPU

UC1 I5_2.2G@

FH8065801620204 QH3G F0 2.2G

SA00008990L

i7 CPU

UC1 I7_2.4G@

FH8065801620004 QH3E F0 2.4G

SA000089A0L

BDW (ES2) CPU for 3D / 4G

UC1 1.8G1600@

CL8065801703601 QGH9 D0 1.8G

SA00007U90L

UC1 1.6G1600@

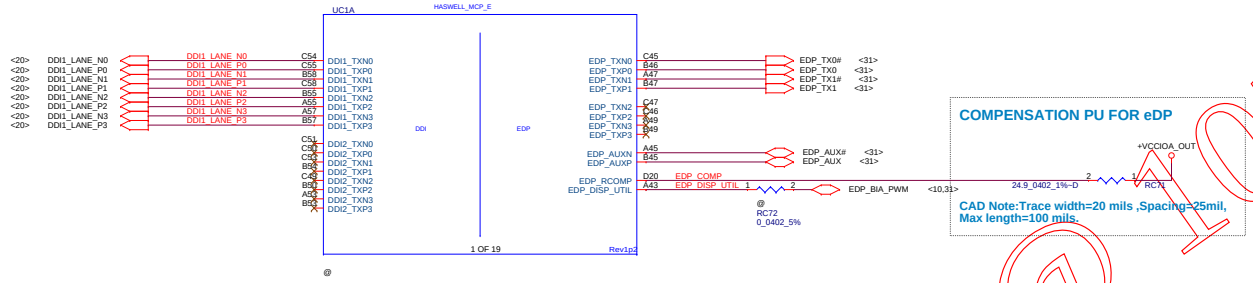
CL8065801703603 QGHB D0 1.6G

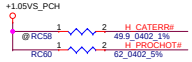
SA00007UH0L

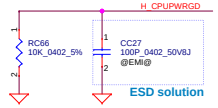
UC1 1.6G1333@

CL8065801703602 QGHA D0 1.6G

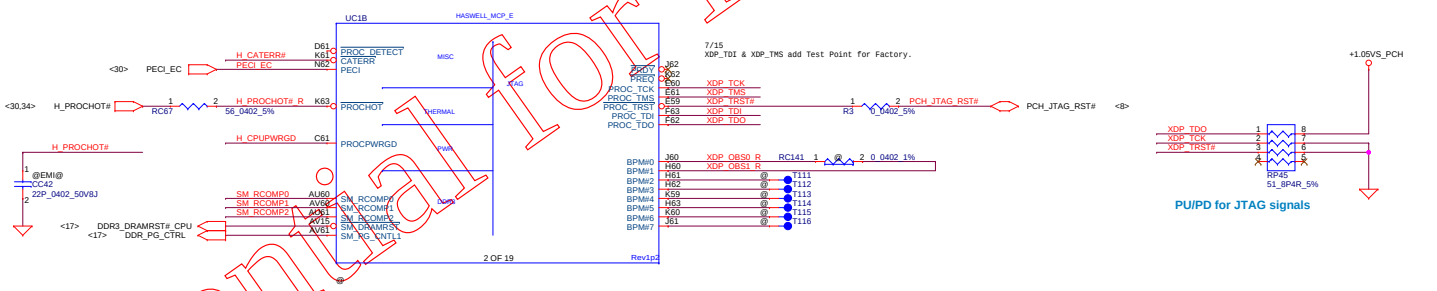
SA00007UG0L



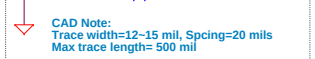




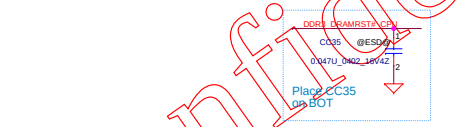
CAD Note:
Avoid stub in the PWRGD path while placing resistors RC115



DDR3 COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil



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Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title: MCP(1,2/19) eDP,XDP,MISC
				Size: Document Number: LA-B015P Rev: 0.1
				Date: Friday, October 17, 2014 Sheet 6 of 56

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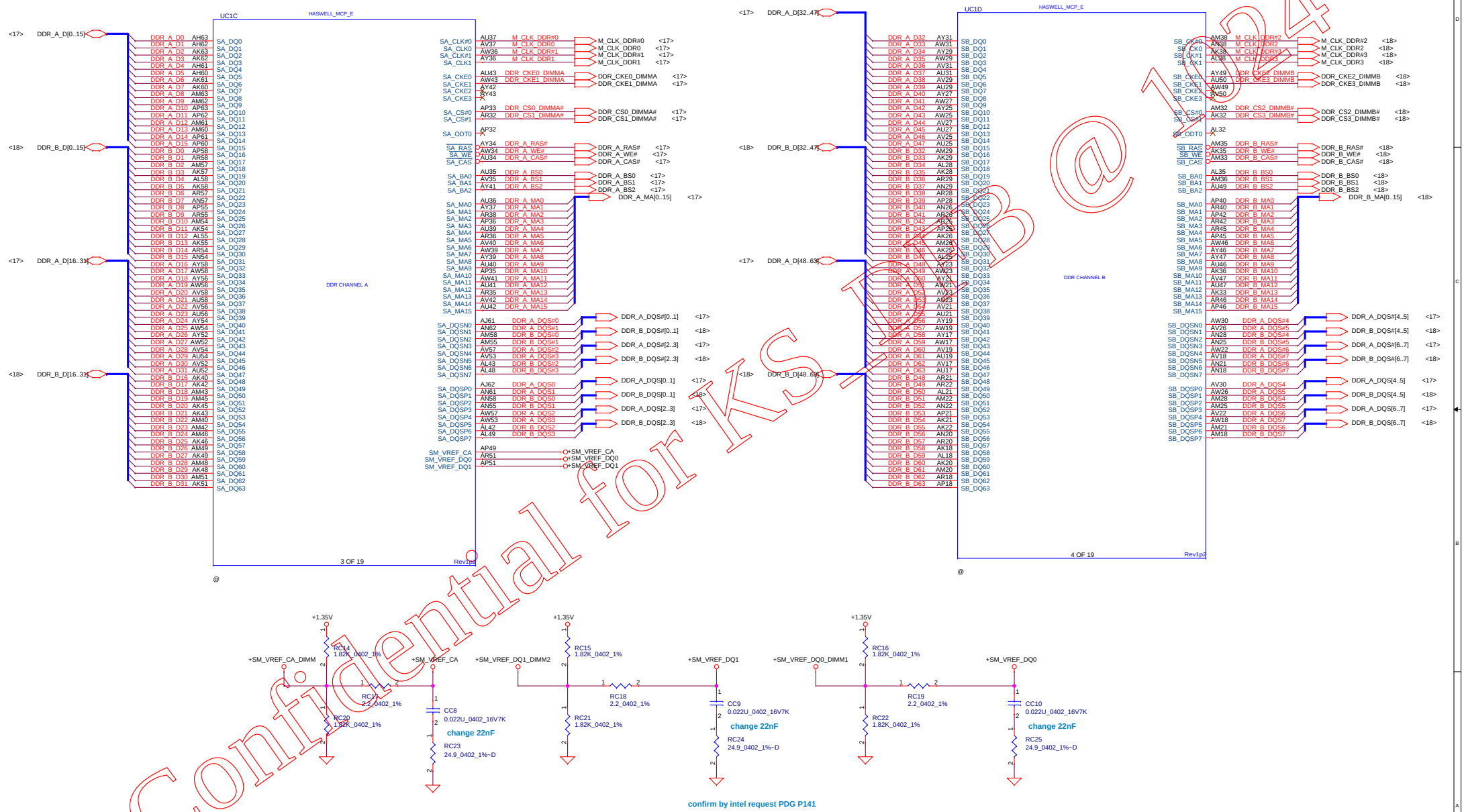
Interleaved Memory



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Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title: MCP(3,4/19) DDR3

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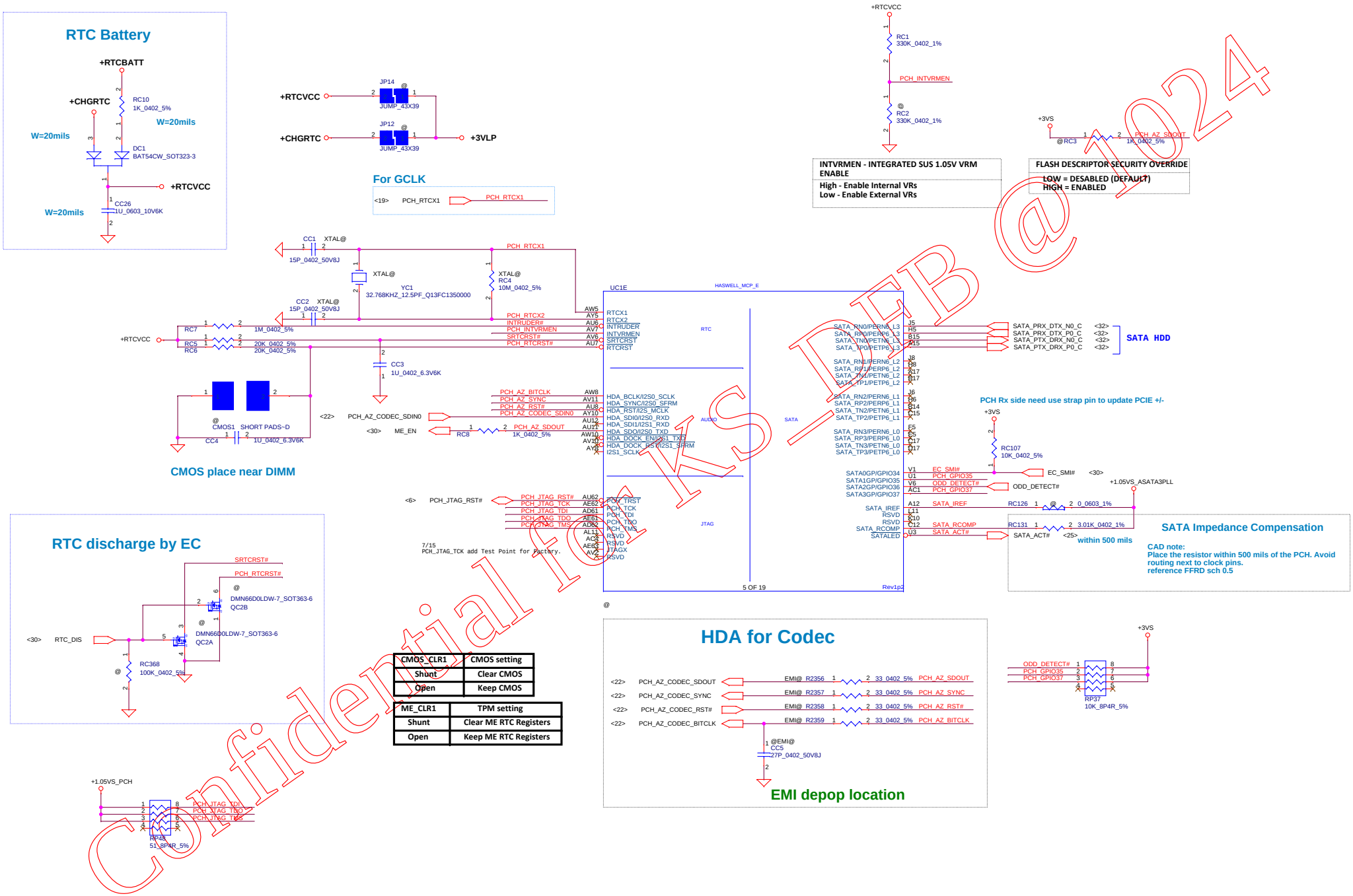
Size	Document Number	Rev
	LA-B015P	0.1

Date: Wednesday, September 10, 2014 Sheet 7 of 56



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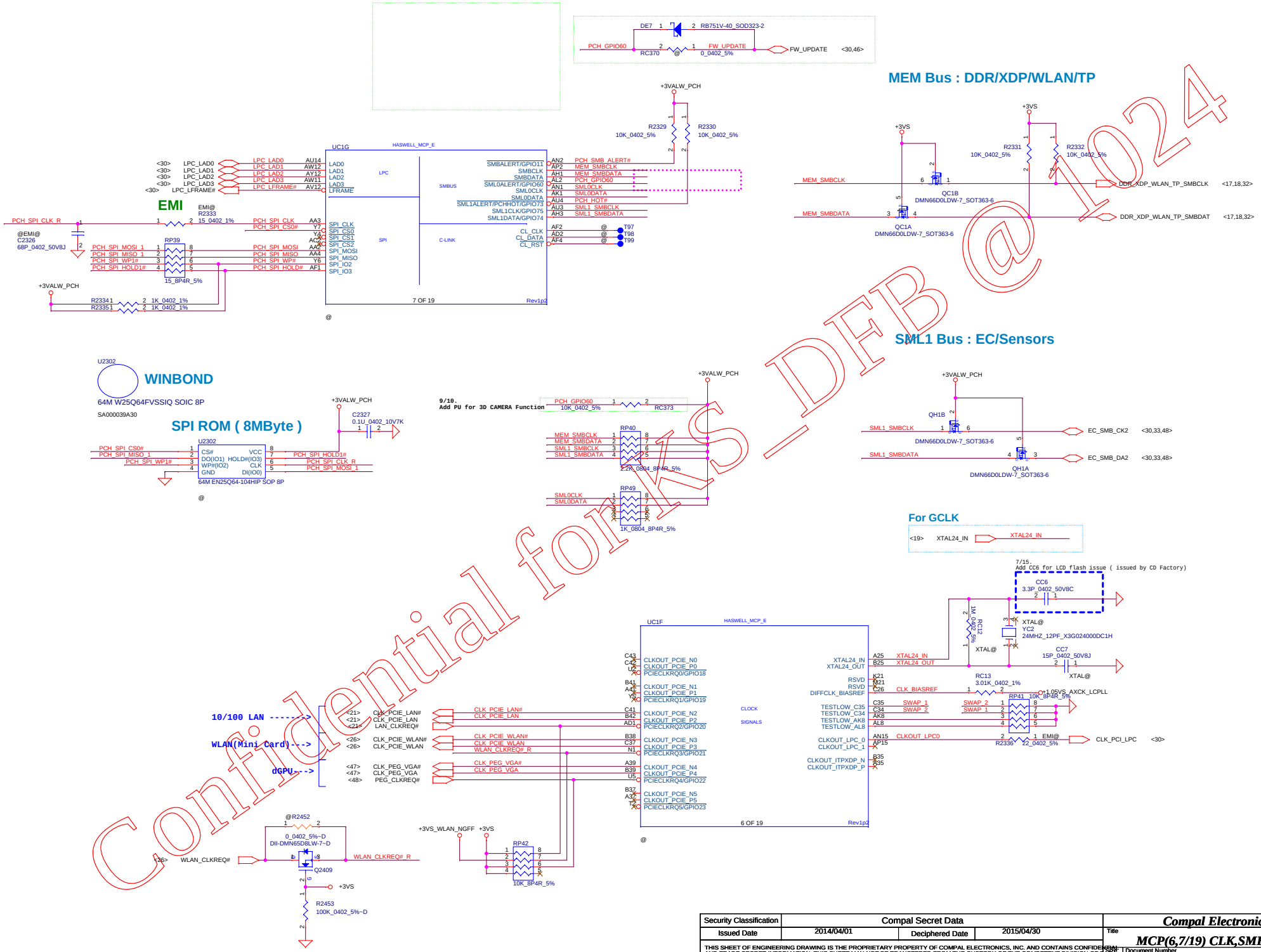
Compal Electronics, Inc.

Title: MCP(5/19) RTC,SATA,HDA,JTAG

Document Number: LA-B015P

Rev: 0.1

Date: Wednesday, September 10, 2014 | Sheet 8 of 56



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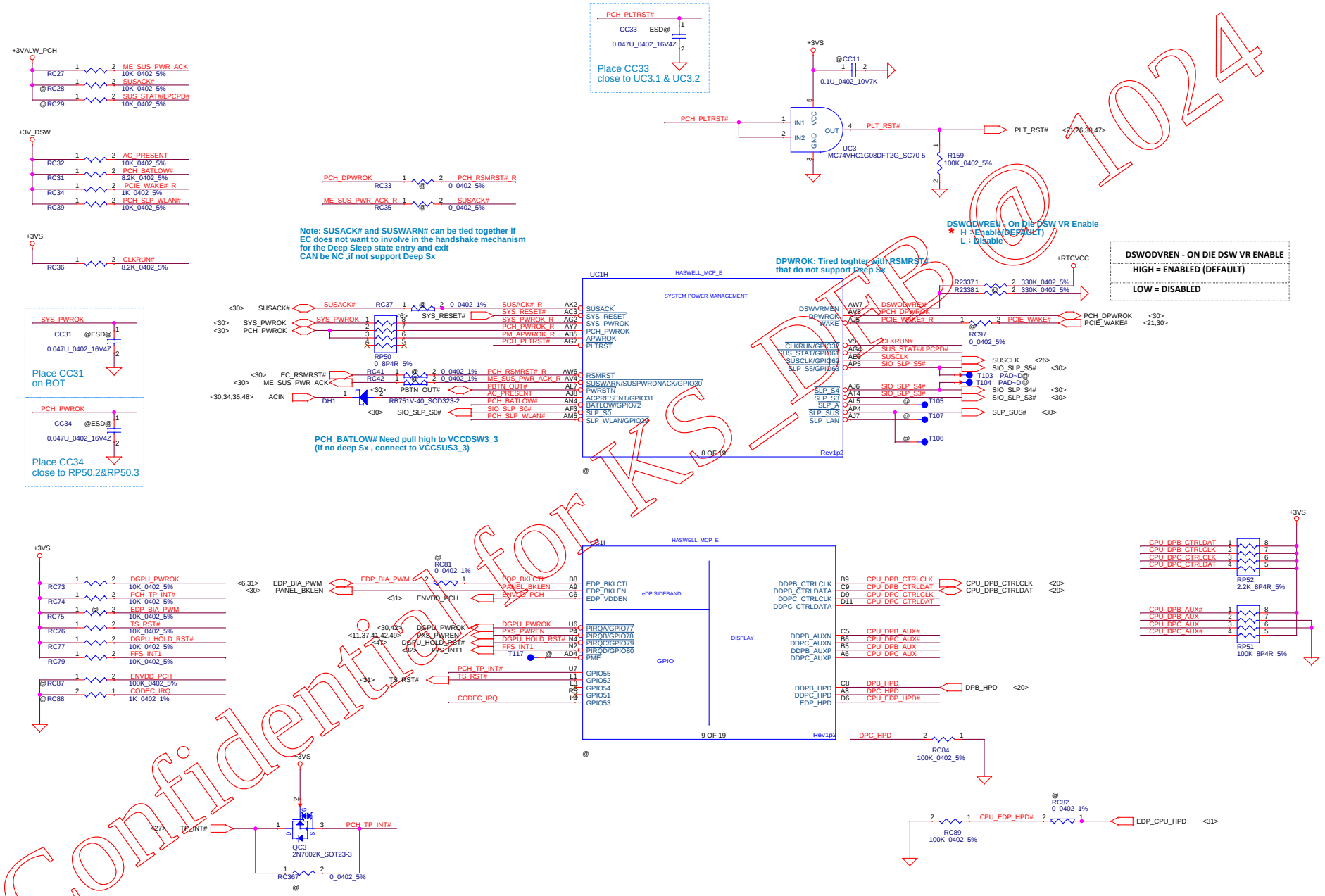
Compal Electronics, Inc.

Title: **MCP(6,7/19) CLK,SMB,SPI,LPC**

Document Number: **LA-B015P** Rev: 0.1

Date: Tuesday, September 16, 2014 Sheet 9 of 56



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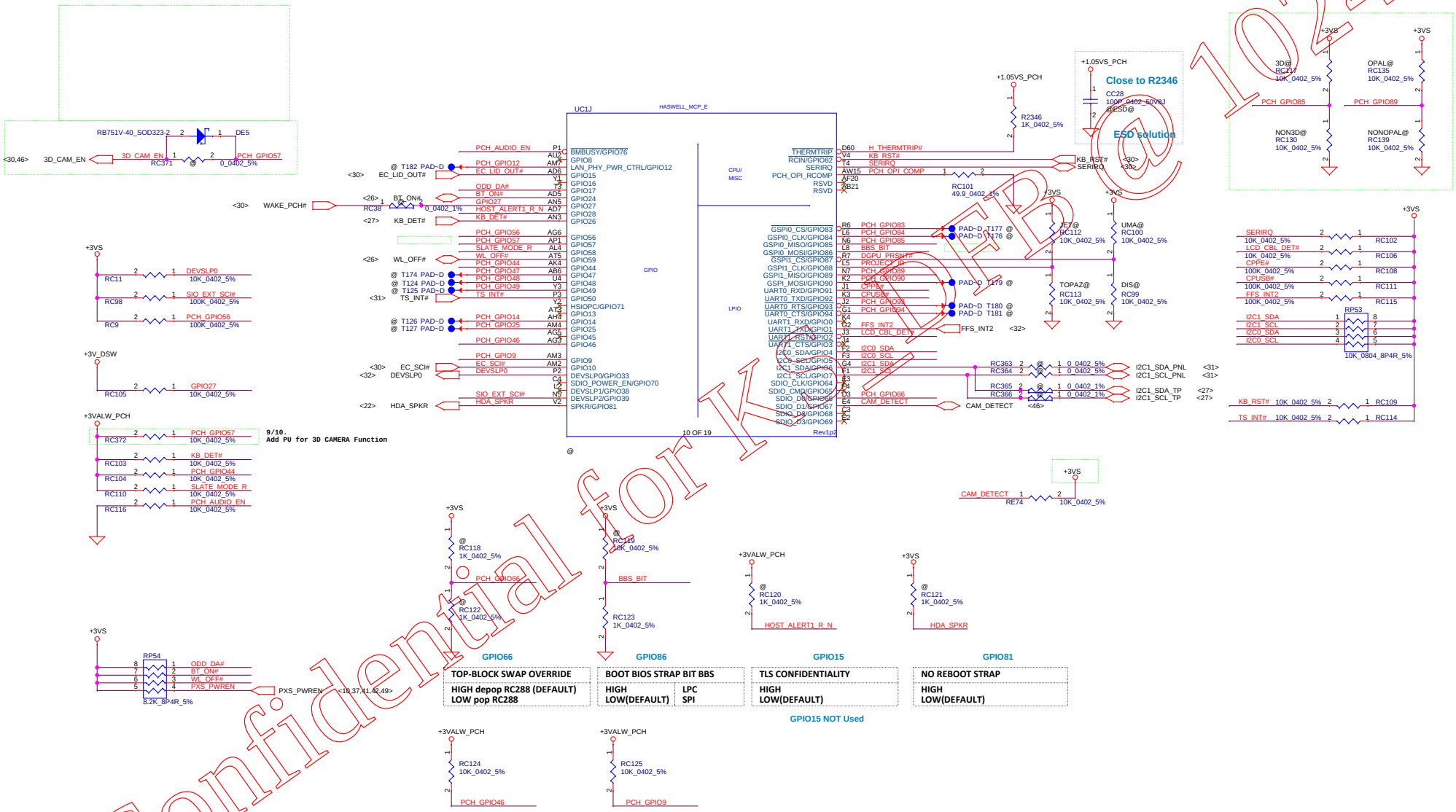
Compal Electronics, Inc.

Title: **MCP(8,9/19) DDI,EDP,GPIO**

Document Number: **LA-B015P** Rev: 0.1

Date: Wednesday, September 10, 2014 Sheet 10 of 56



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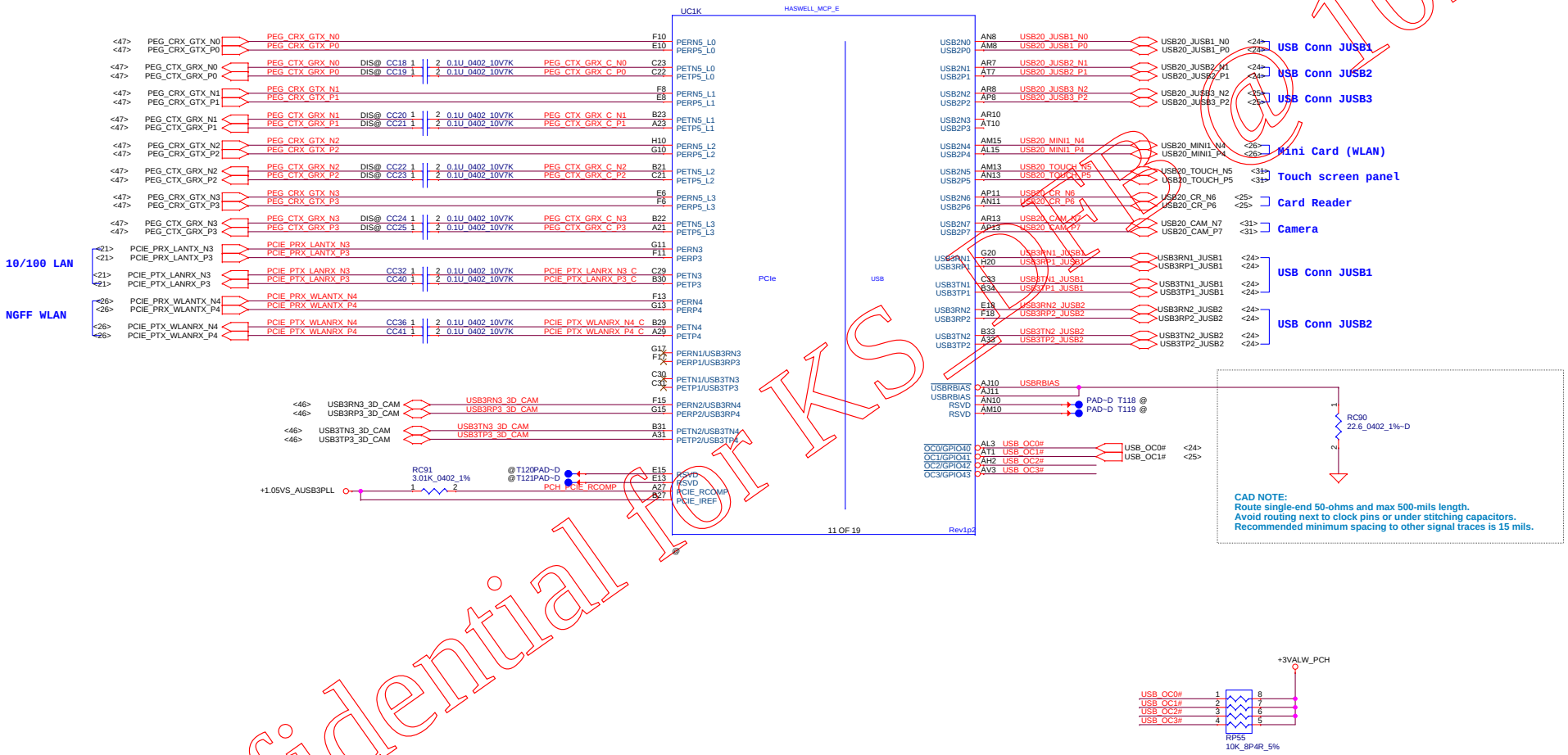
Compal Electronics, Inc.

Title: **MCP(10/19) GPIO,LPIO,MISC**

Document Number: **LA-B015P** Rev: 0.1

Date: Tuesday, September 16, 2014 Sheet 11 of 56



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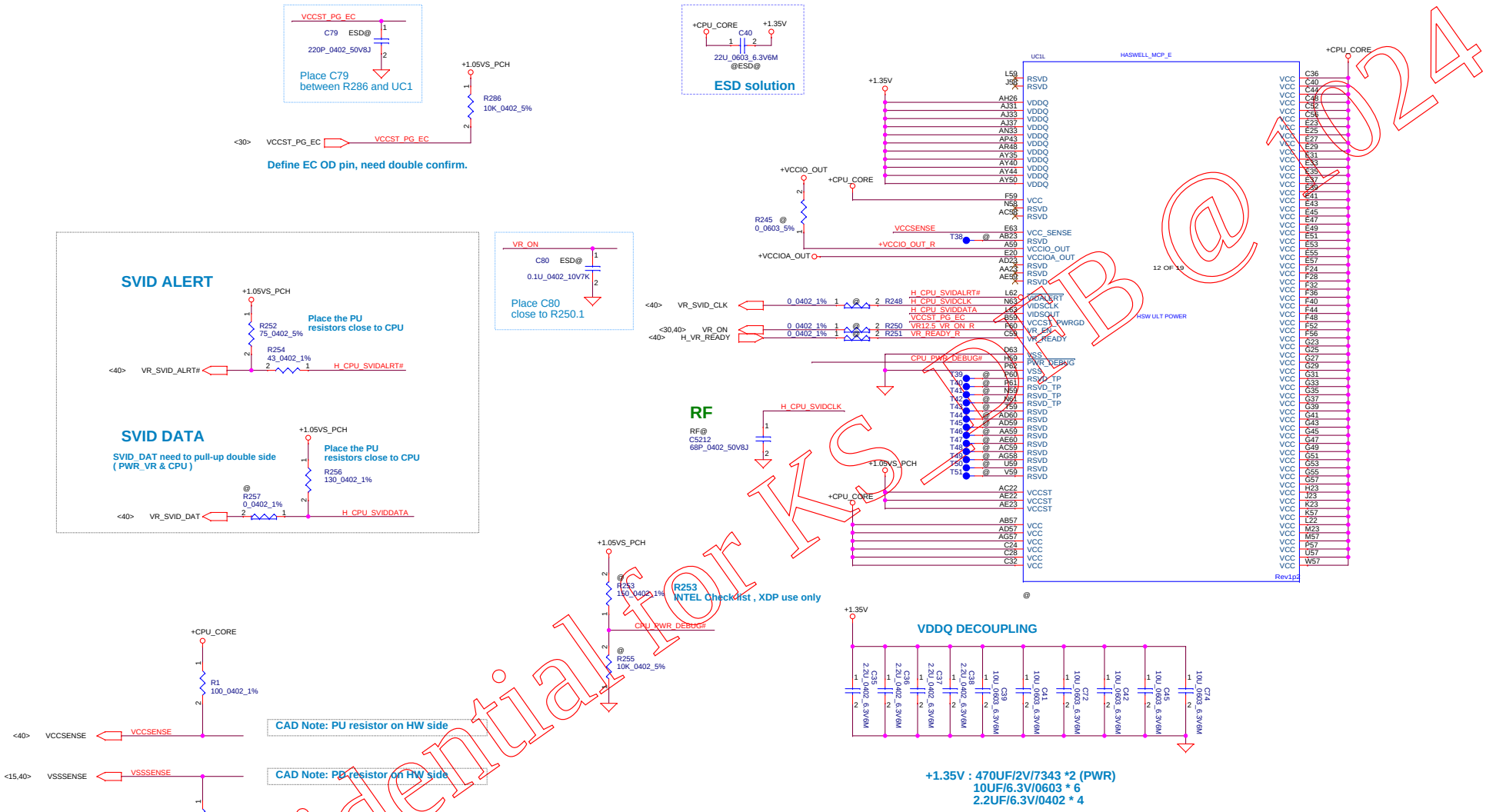
Compal Electronics, Inc.

Title: **MCP(11/19) PCIE,USB**

Document Number: **LA-B015P** | Rev: 0.1

Date: Wednesday, September 10, 2014 | Sheet 12 of 56



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Compal Electronics, Inc.

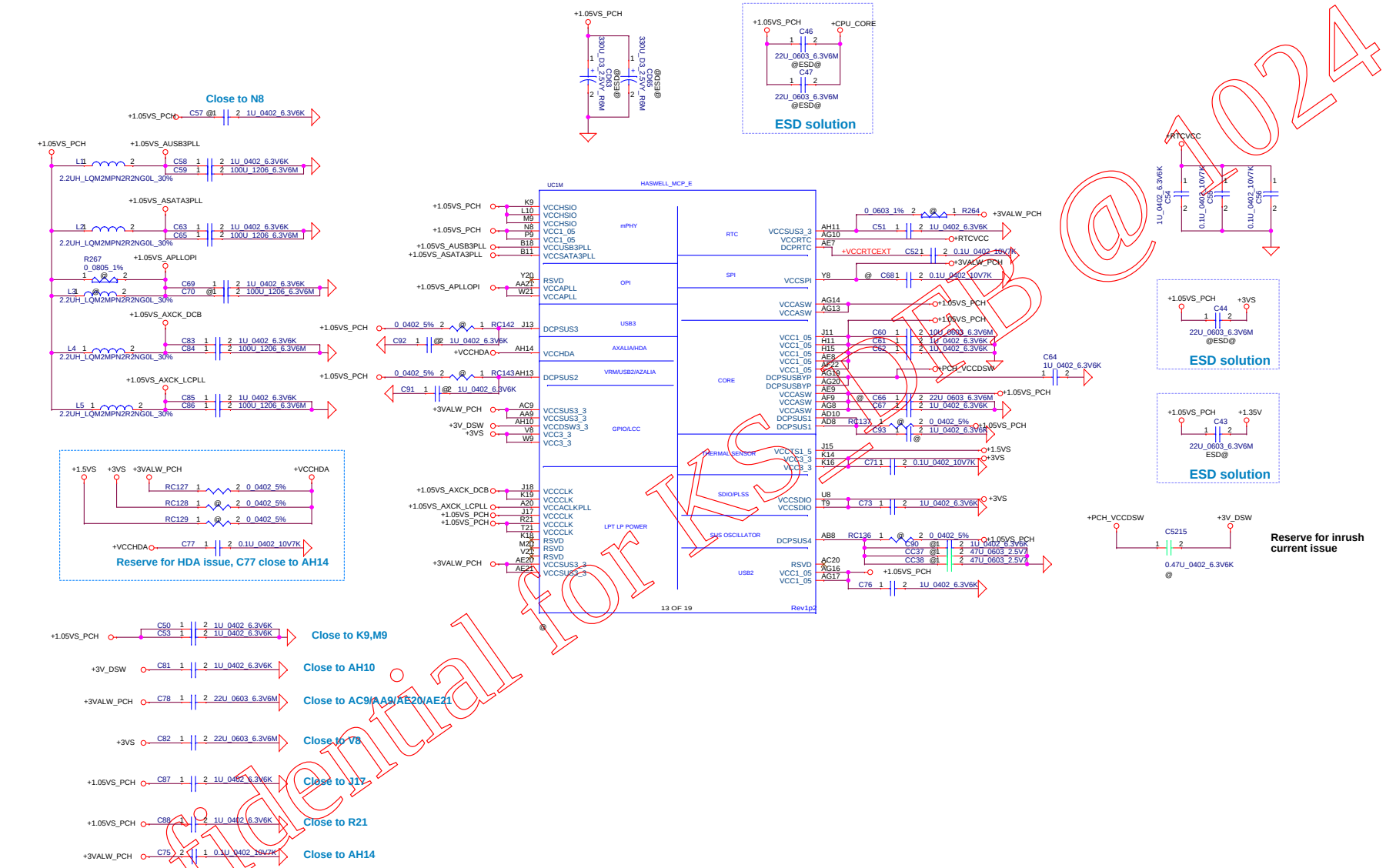
Title: **MCP(12/19) Power**

Document Number: **LA-B015P**

Rev: 0.1

Date: Friday, October 17, 2014

Sheet 13 of 56



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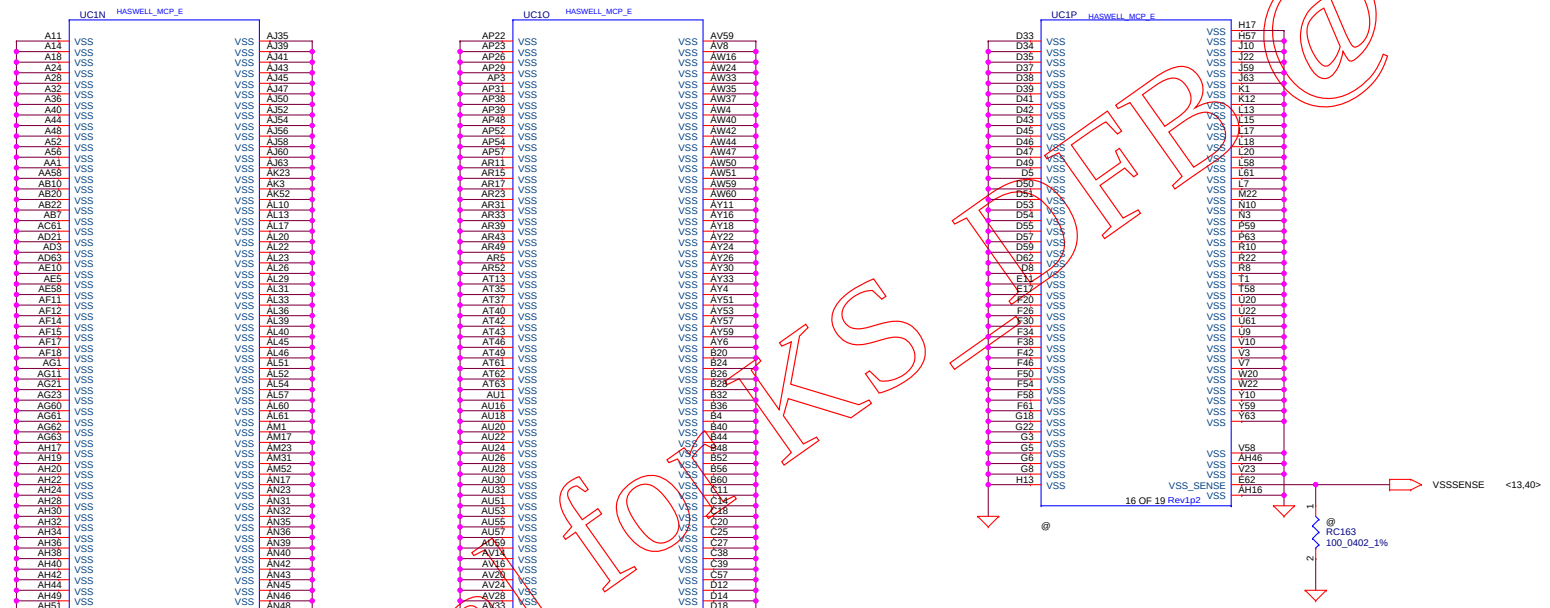
Compal Electronics, Inc.

Title: **MCP(13/19) Power**

Document Number: **LA-B015P** Rev: 0.1

Date: Friday, October 17, 2014 Sheet 14 of 56



CAD Note: RC163 SHOULD BE PLACED CLOSE TO CPU

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Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

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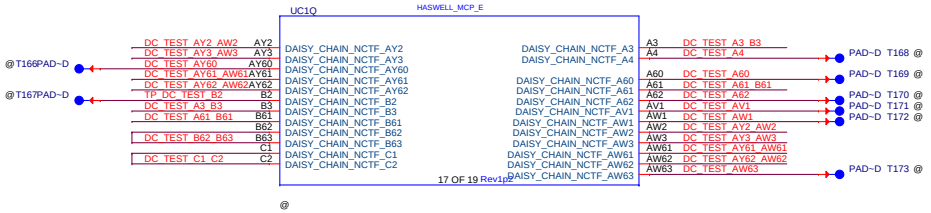
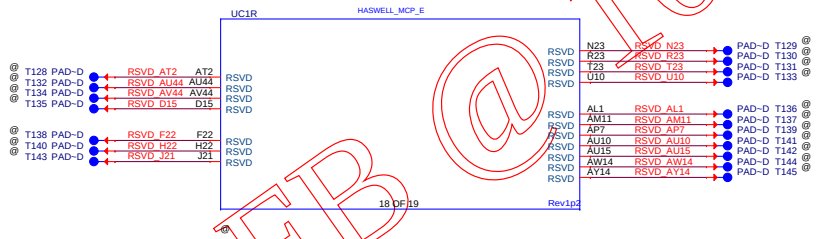
Compal Electronics, Inc.

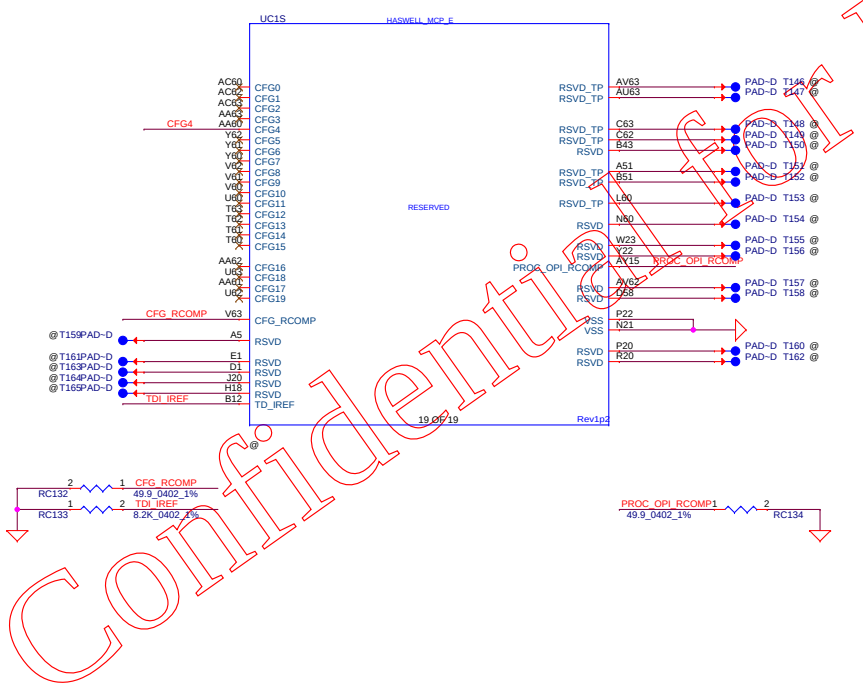
Title: **MCP(14,15,16/19) VSS**

Document Number: **LA-B015P** Rev: 0.1

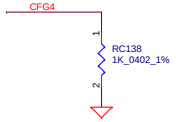
Date: Wednesday, September 10, 2014 Sheet 15 of 56







CFG STRAPS for CPU



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

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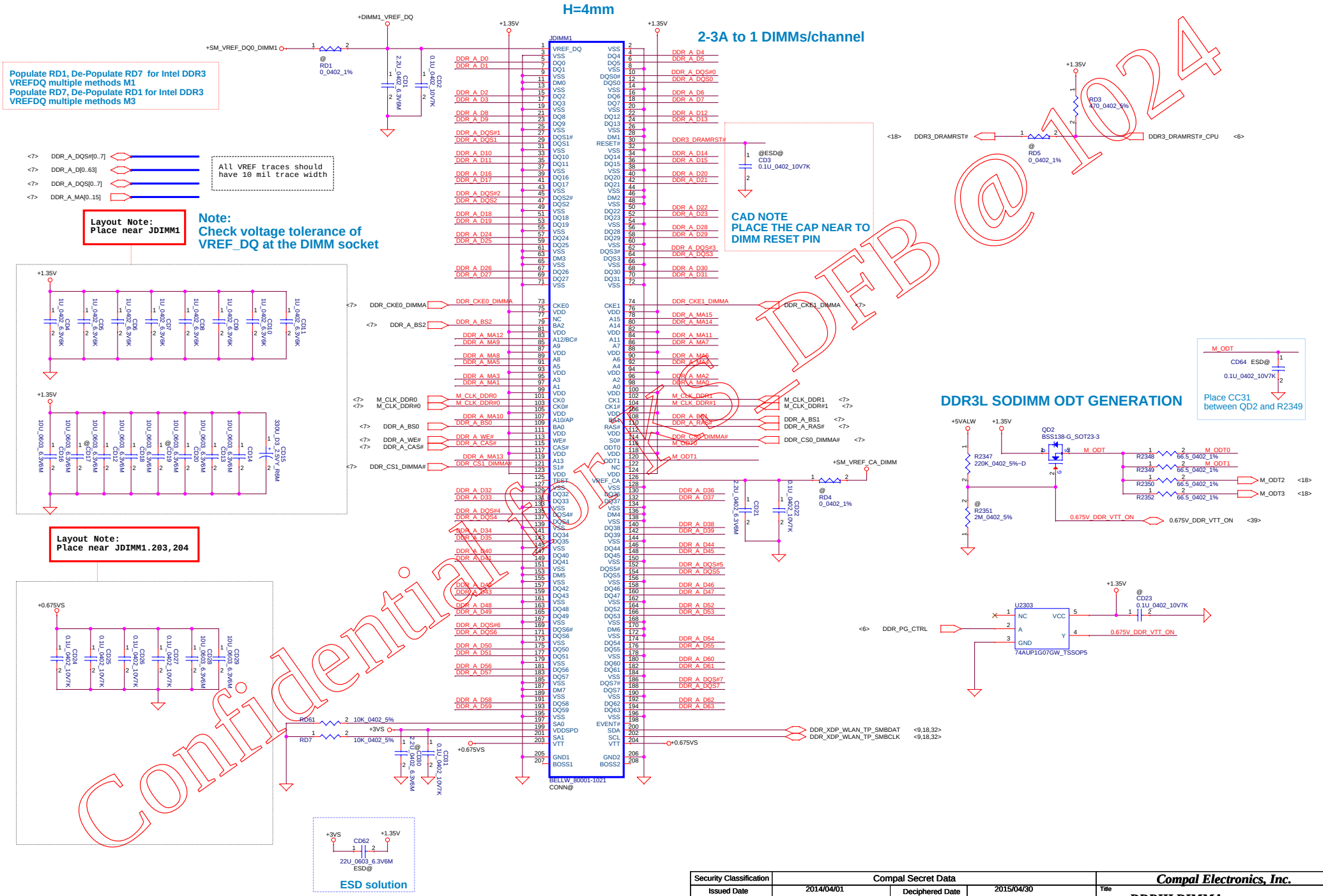
Compal Electronics, Inc.

Title: MCP(17,18,19/19) CFG,RSVD

Document Number: LA-B015P

Rev: 0.1

Date: Wednesday, September 10, 2014 | Sheet 16 of 56



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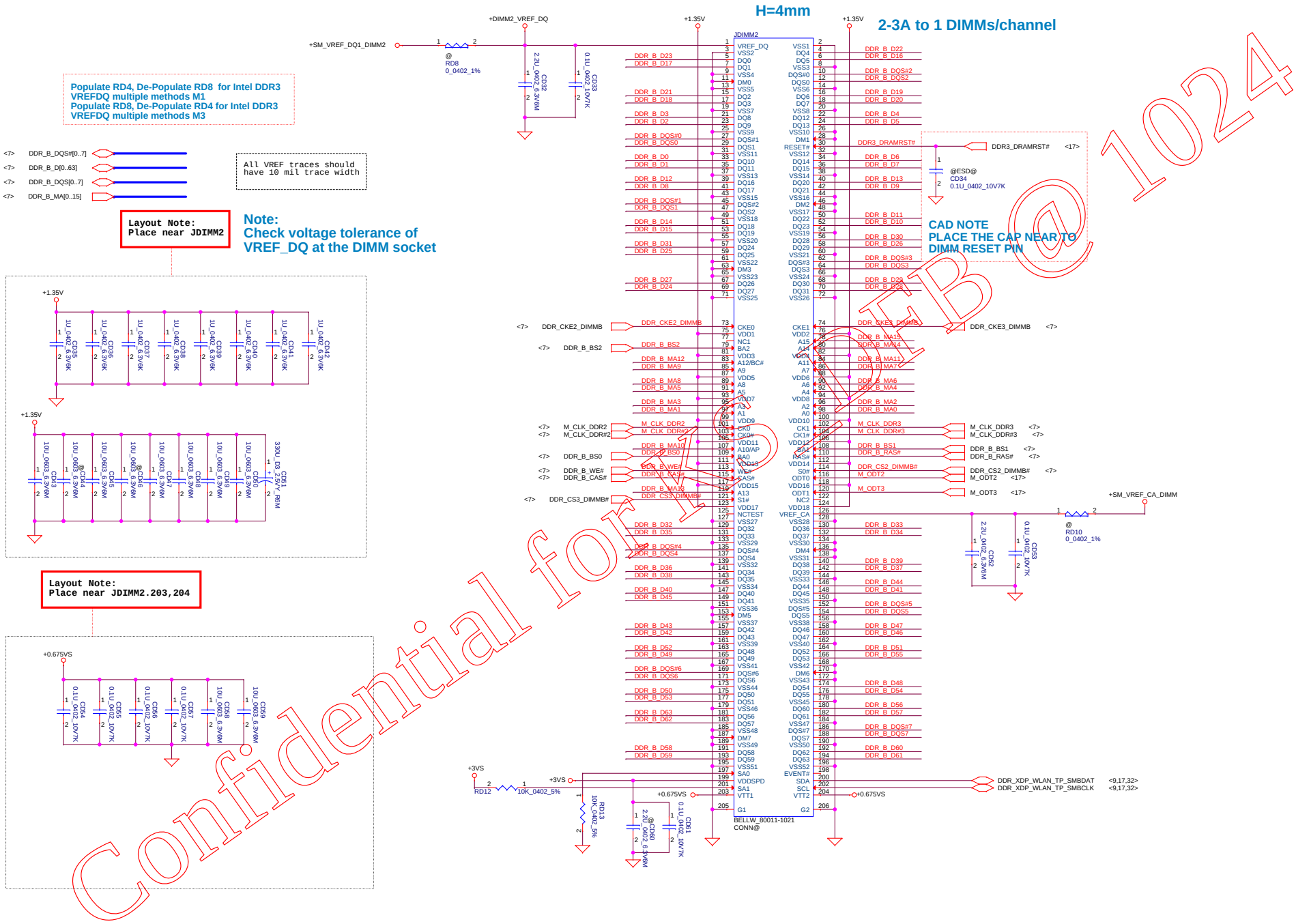
Compal Electronics, Inc.

Title: **DDRIII DIMMA**

Document Number: **LA-B015P** Rev: 0.1

Date: Wednesday, September 10, 2014 Sheet 17 of 56



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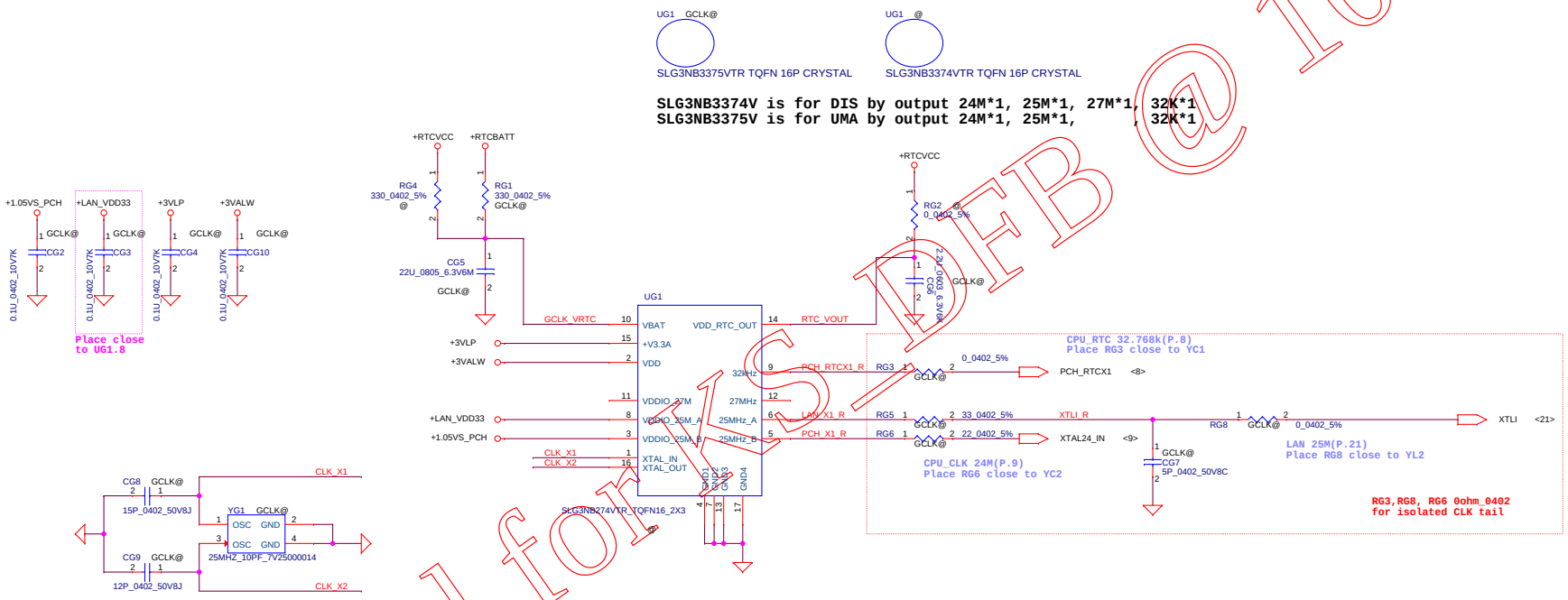
Compal Electronics, Inc.

Title: **DDRIII DIMMB**

Document Number: **LA-B015P** Rev: 0.1

Date: Wednesday, September 10, 2014 Sheet 18 of 56



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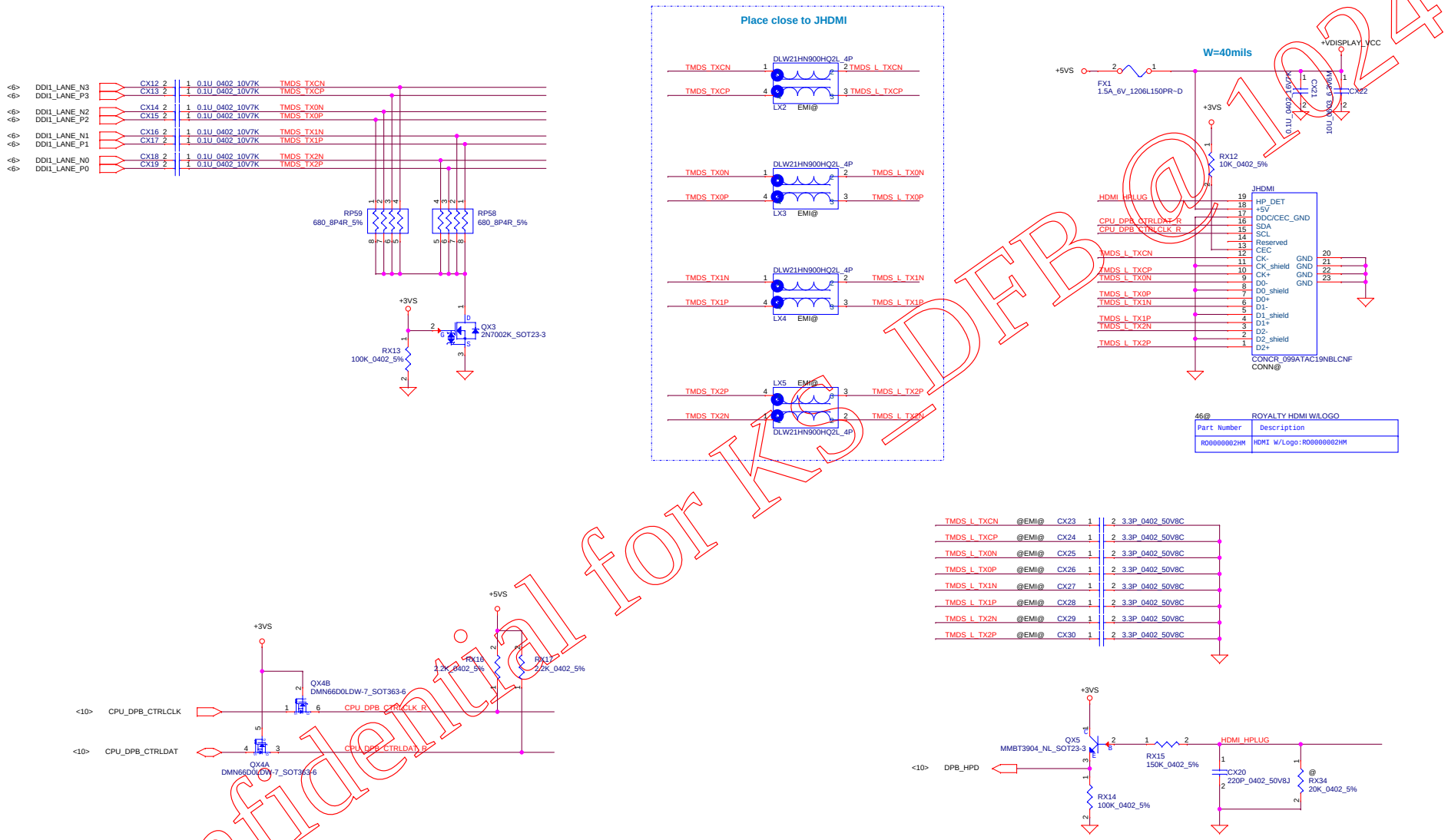
Compal Electronics, Inc.

Title: **Green CLK**

Document Number: **LA-B015P** Rev: 0.1

Date: Wednesday, September 10, 2014 Sheet 19 of 56



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Issued Date	2014/04/01	Deciphered Date	2015/04/30

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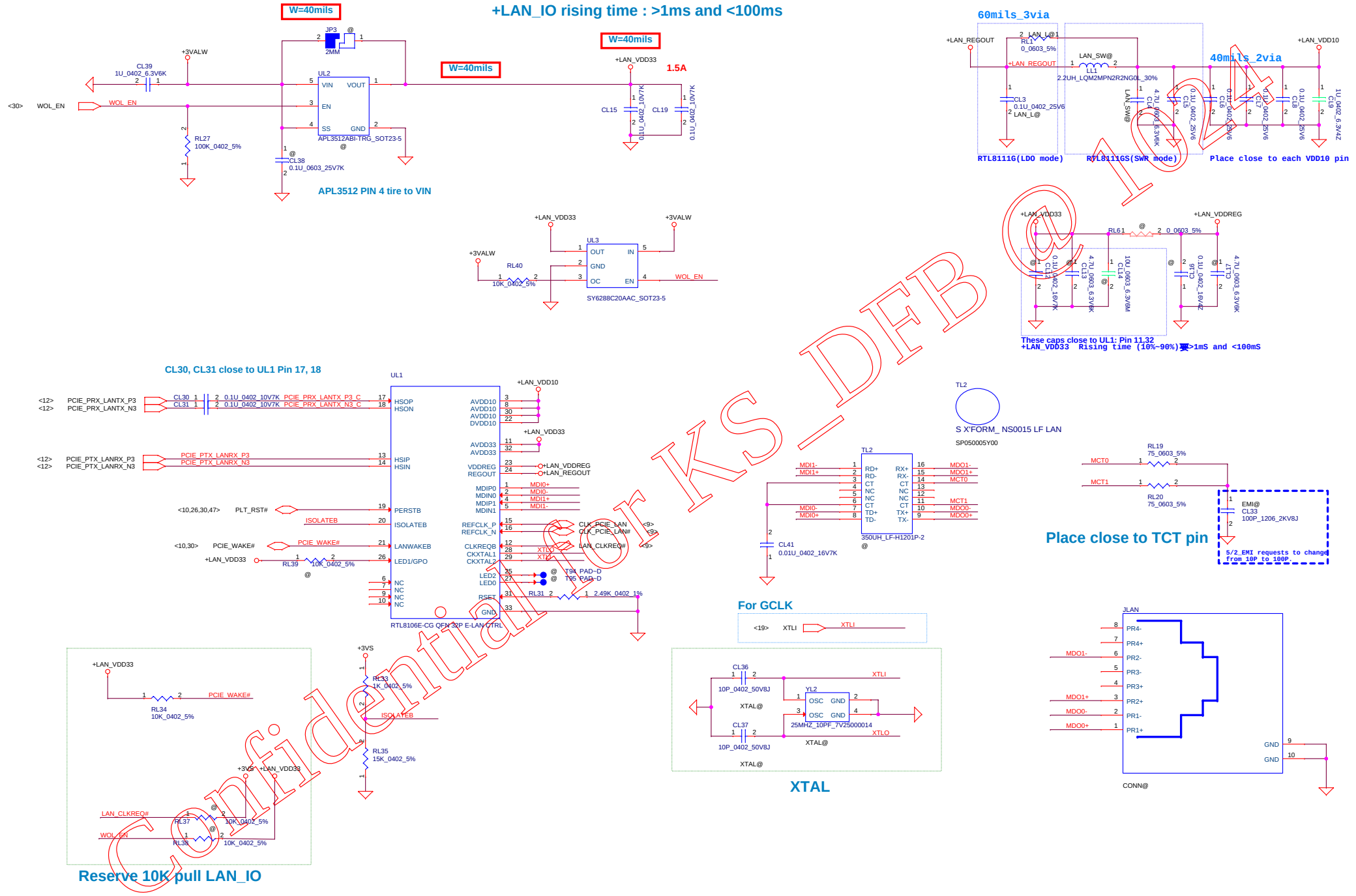
Compal Electronics, Inc.

Title: **HDMI**

Document Number: **LA-B015P** Rev: 0.1

Date: Tuesday, September 16, 2014 Sheet 20 of 56



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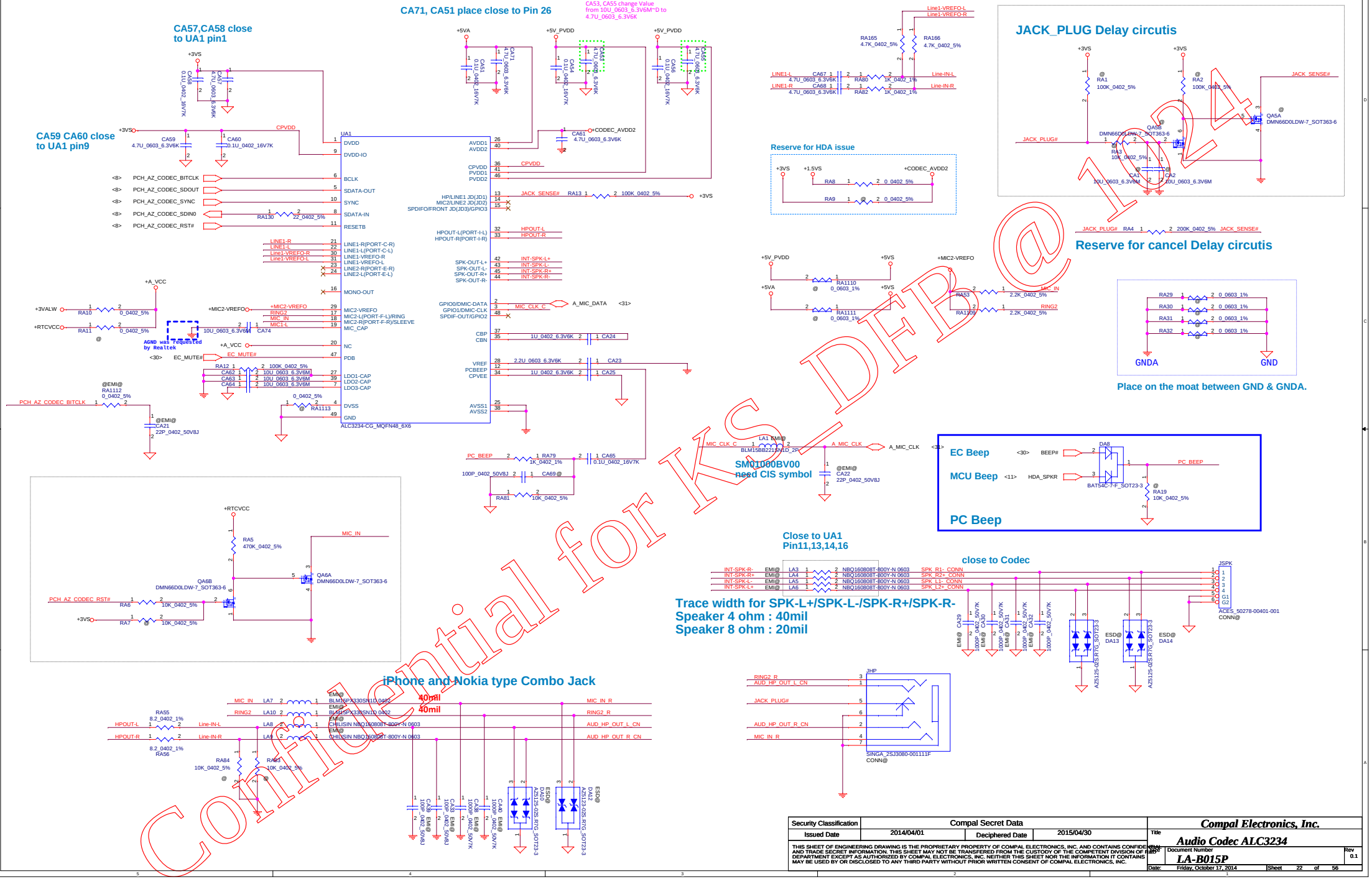
Compal Electronics, Inc.

Title: 10/100 LAN

Size: Custom | Document Number: LA-B015P | Rev: 0.1

Date: Wednesday, September 10, 2014 | Sheet 21 of 56



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Issued Date	2014/04/01	Deciphered Date	2015/04/30

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Compal Electronics, Inc.

Title: Audio Codec ALC3234

Document Number: LA-B015P

Rev: 0.1

Date: Friday, October 17, 2014 | Sheet 22 of 56

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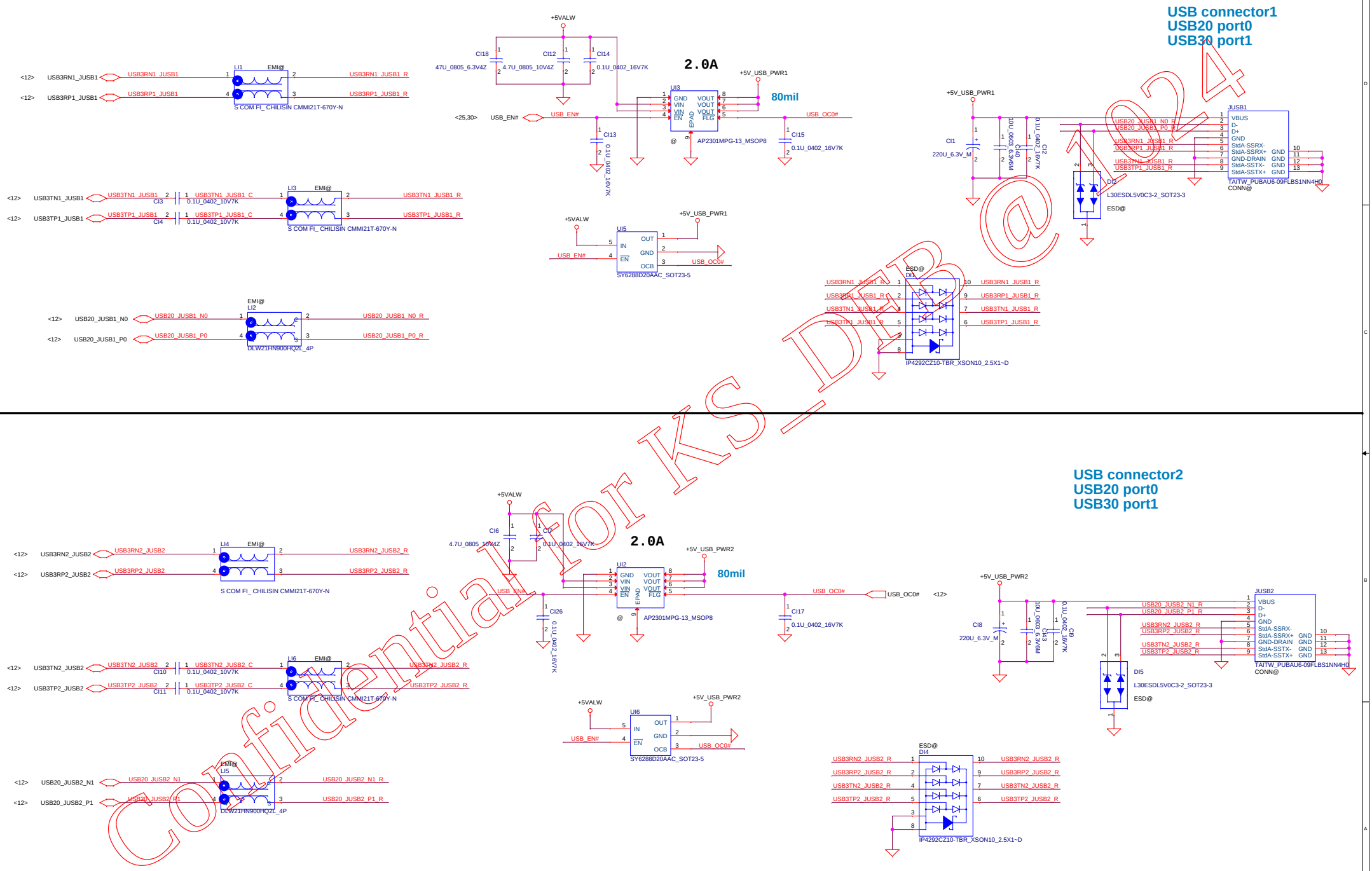
Compal Electronics, Inc.

Title: **Reserved Page**

Document Number: **LA-B015P**

Rev: 0.1

Date: Wednesday, September 10, 2014 | Sheet 23 of 56



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Compal Electronics, Inc.

Title: USB3.0

Document Number: LA-B015P

Rev: 0.1

Date: Tuesday, September 16, 2014

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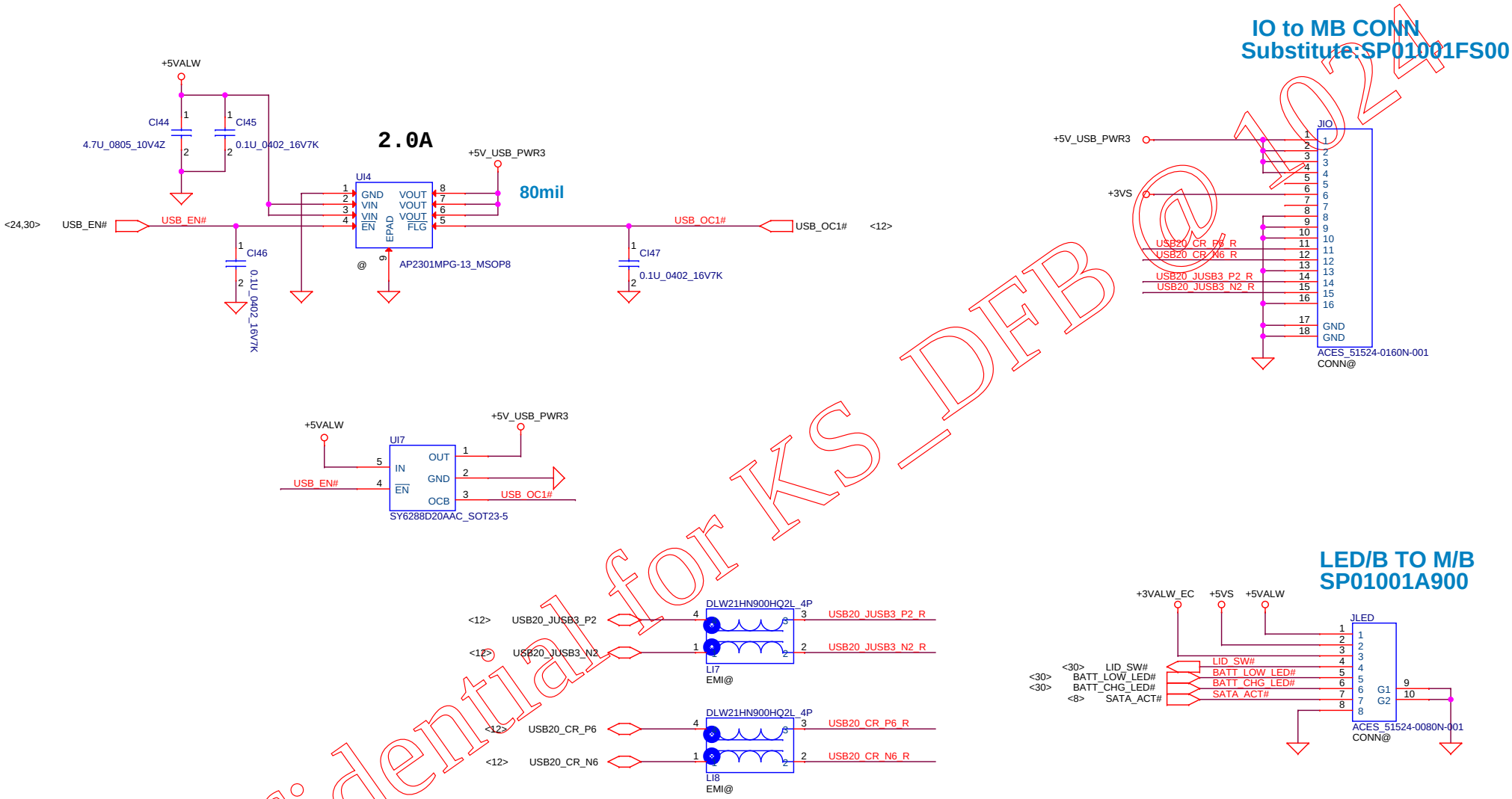

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Issued Date	2014/04/01	Deciphered Date	2015/04/30

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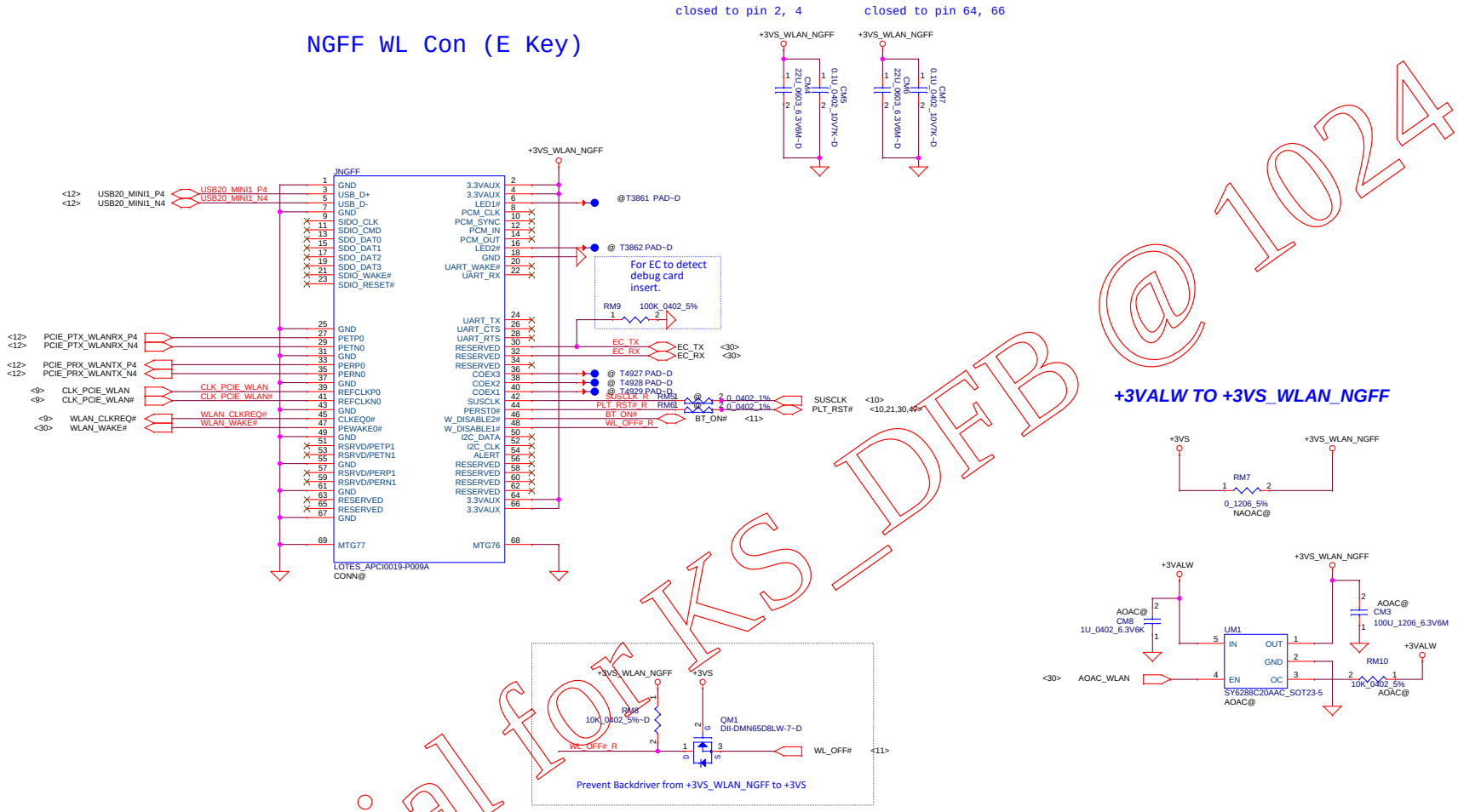
Title: **IO/B, LED/B**

Size: B | Document Number: **LA-B015P** | Rev: 0.1

Date: Tuesday, September 16, 2014 | Sheet 25 of 56

NGFF WL Con (E Key)



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Compal Electronics, Inc.

Title: **NGFF WLAN**

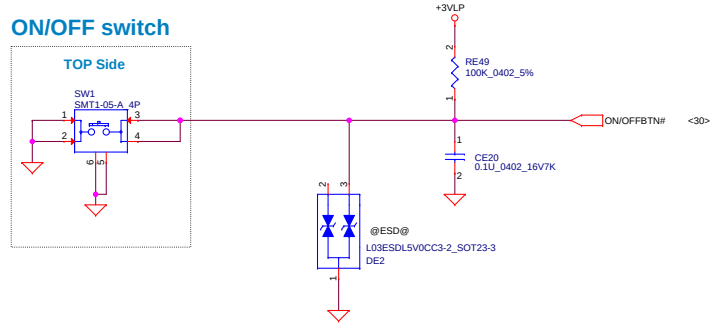
Document Number: **LA-B015P**

Rev: 0.1

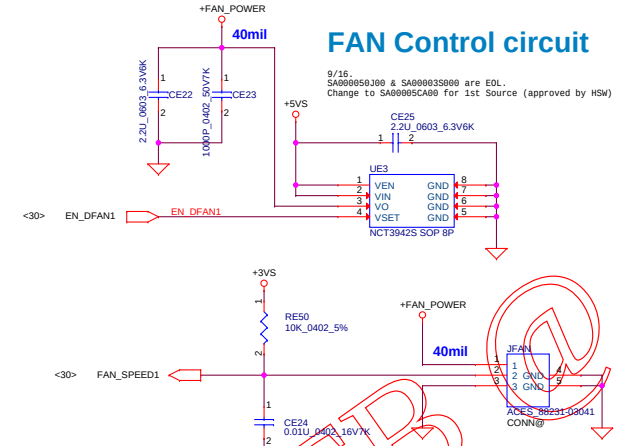
Date: Wednesday, September 10, 2014 | Sheet 26 of 56

Power ON Circuit

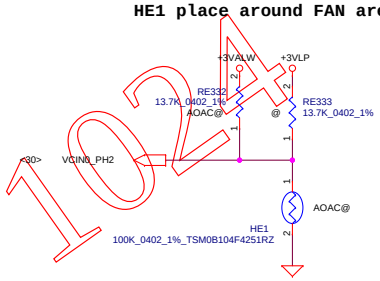
ON/OFF switch

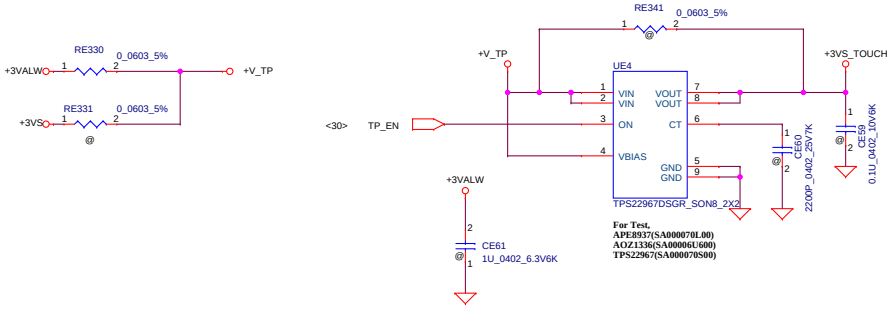


FAN Control circuit

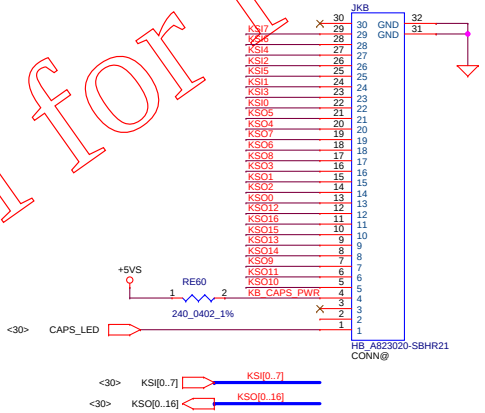


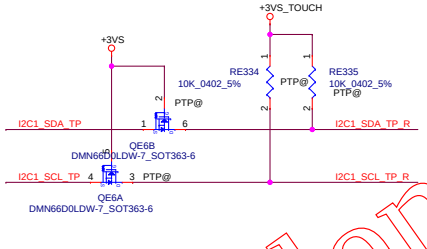
HE1 place around FAN area.



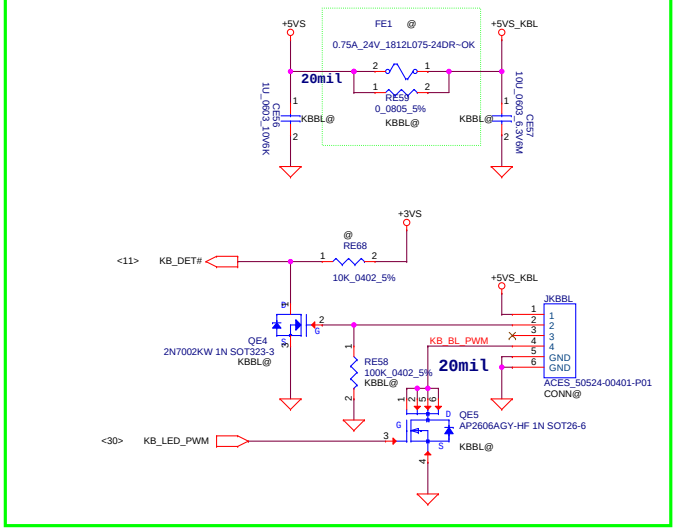


INT_KBD Connector

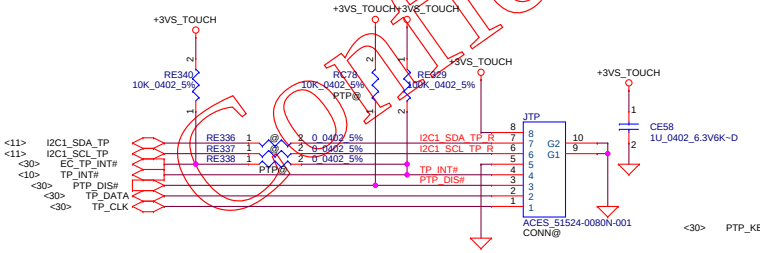




* Key Board Back Light



Touch pad



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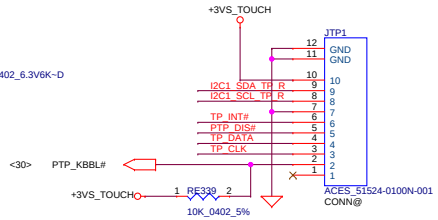

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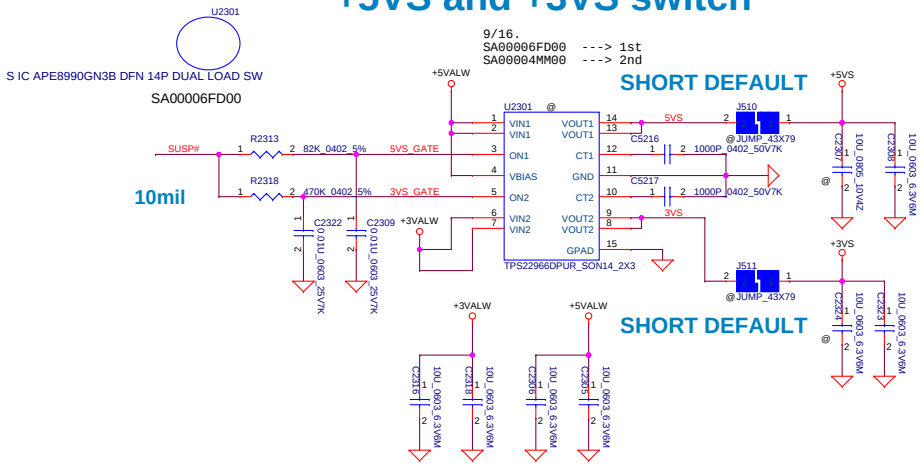
Compal Electronics, Inc.

Title: **FAN / TP / PWR SW / KBBL**

Document Number: **LA-B015P** Rev: 0.1

Date: Friday, October 17, 2014 Sheet 27 of 56

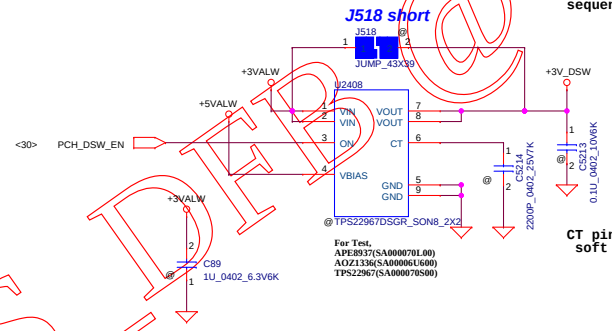
+5VS and +3VS switch



+3VALW TO +3V_DSW

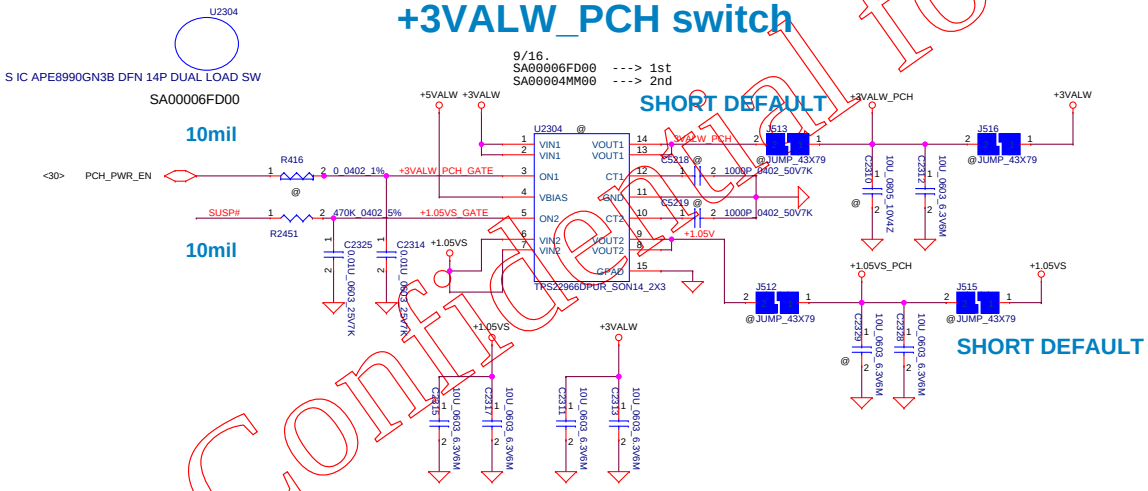
J518 short

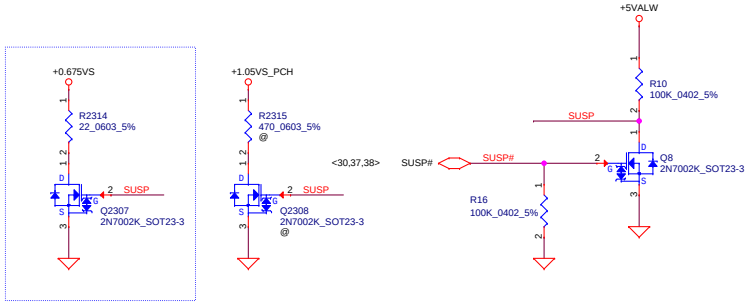
+3V_DSW have soft start sequence: +3V_DSW stable > +3VALW_PCH > 0ms



CT pin use 2200pf for soft start tuning

+3VALW_PCH switch





For Intel S3 Power Reduction

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Compal Electronics, Inc.

Title: **DC/DC Interface**

Document Number: **LA-B015P** Rev: 0.1

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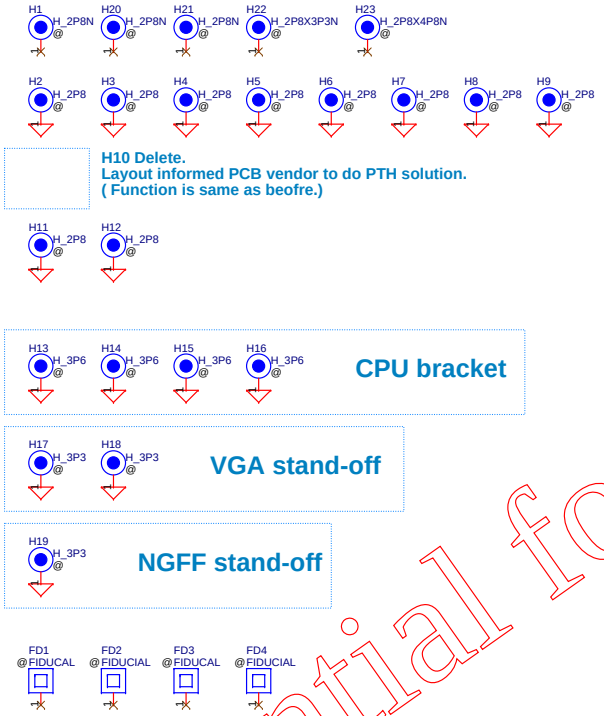
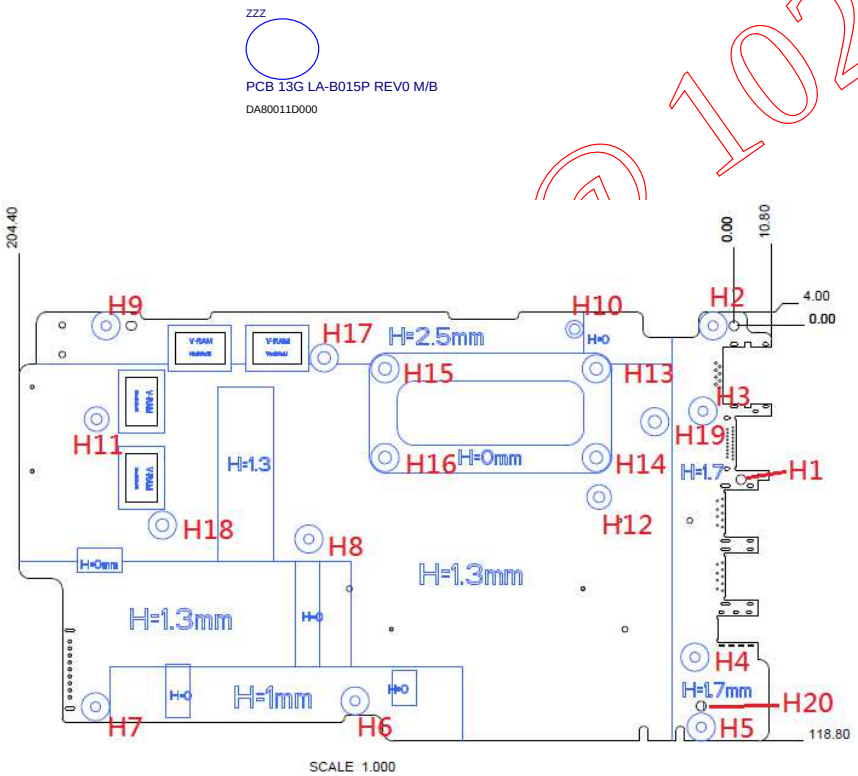
Screw Hole





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Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title: Screw Hole
				Size / Document Number: LA-B015P / Rev: 0.1
				Date: Wednesday, September 10, 2014 / Sheet 29 of 56

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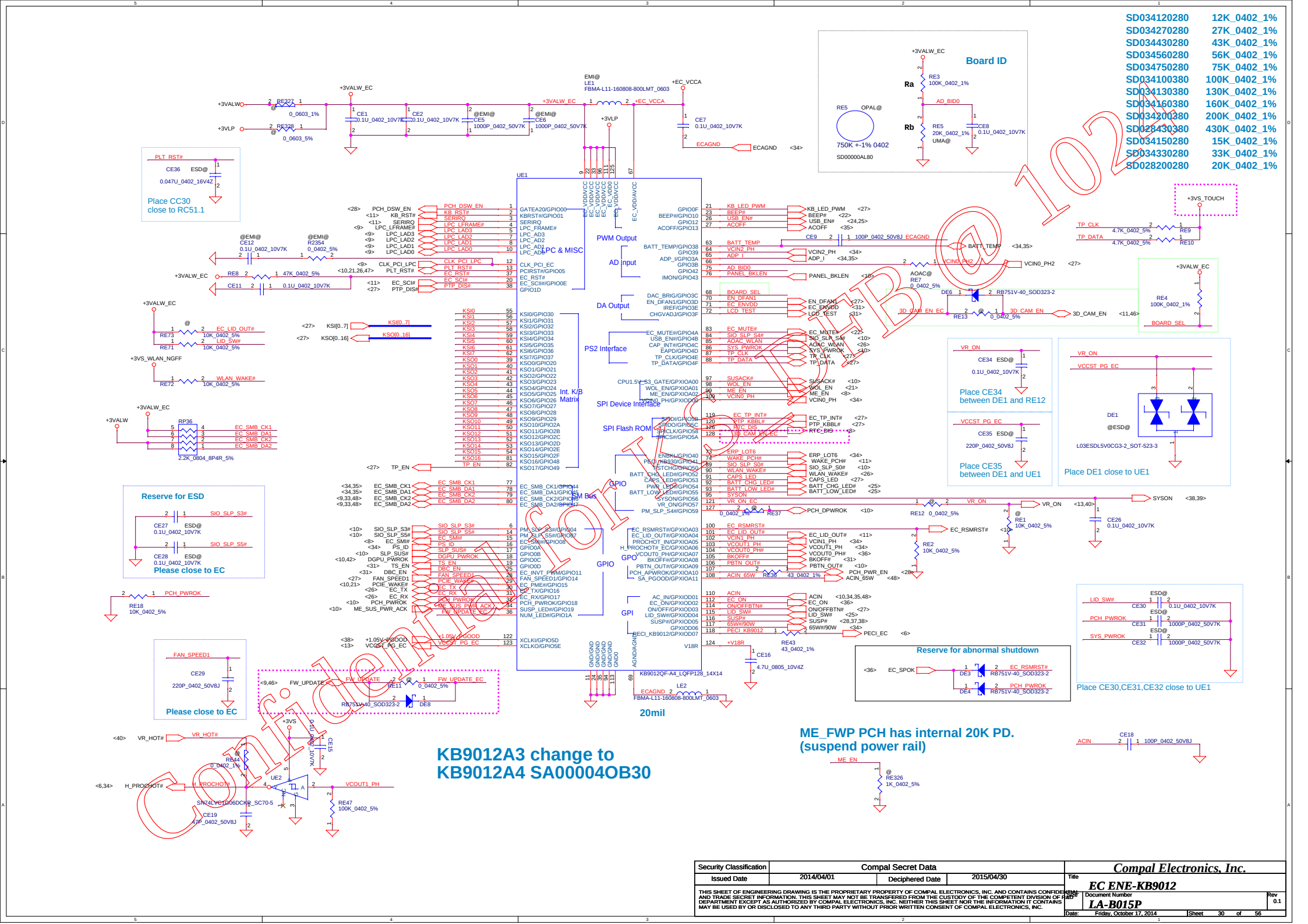

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title: EC ENE-KB9012
				Size: Document Number: LA-B015P — Rev: 0.1
				Date: Friday, October 17, 2014 — Sheet 30 of 56

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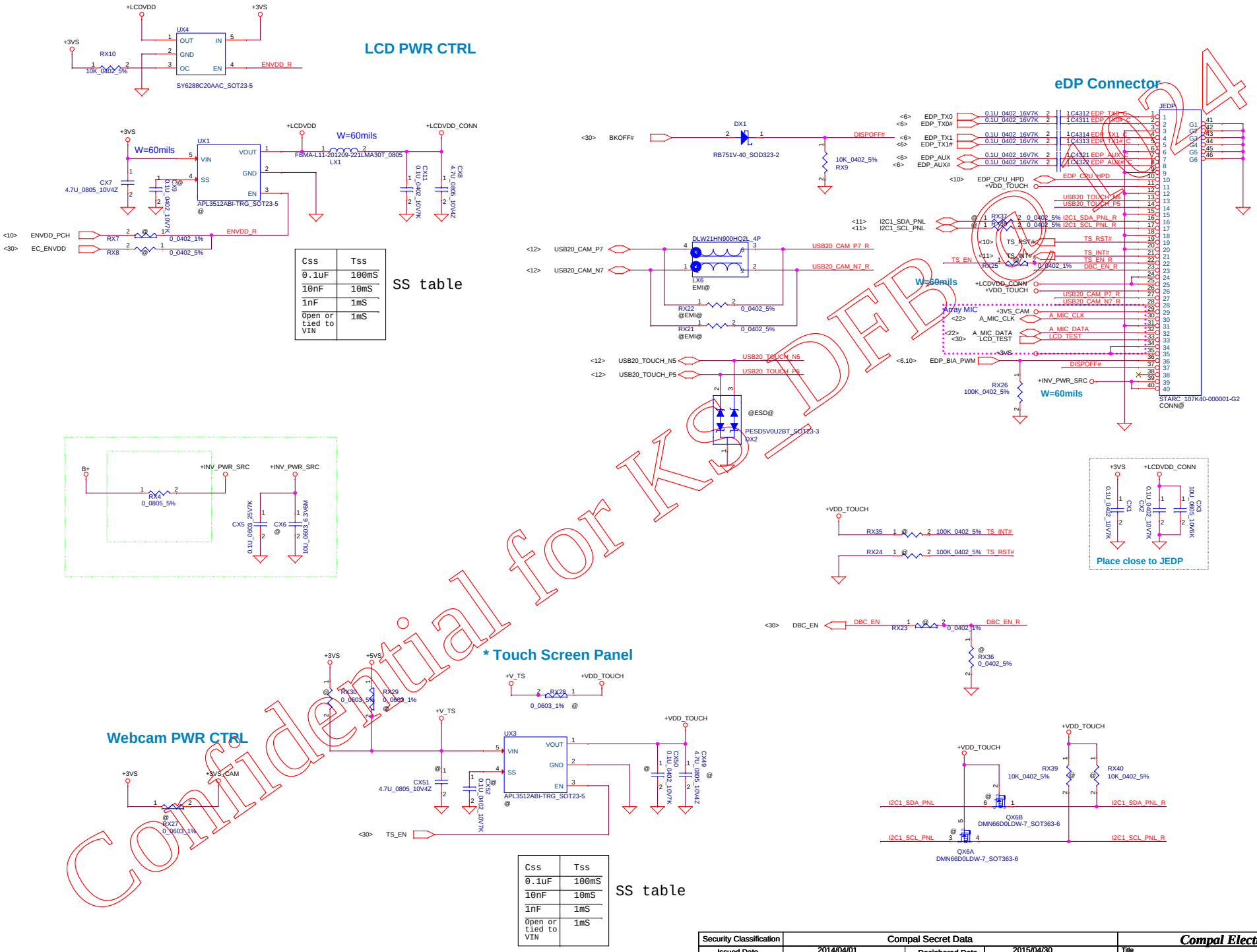

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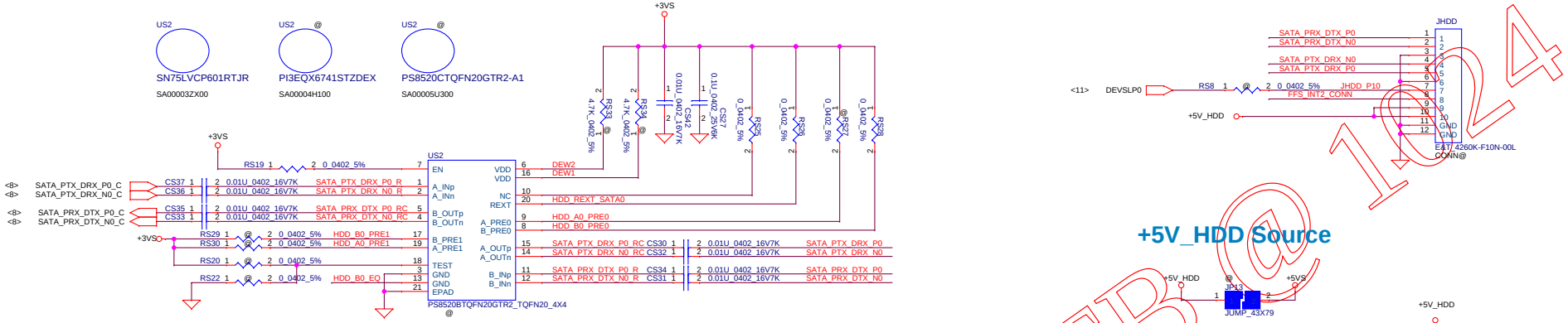
Compal Electronics, Inc.

Title: **eDP / webcam / TouchScreen**

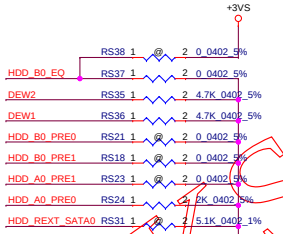
Document Number: **LA-B015P** Rev: 0.1

Date: Tuesday, September 16, 2014 Sheet 31 of 56

SATA HDD Connector

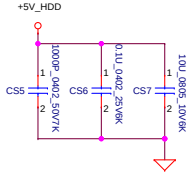


	US2	RS35	RS36	RS18	RS22	RS23	RS24	RS28
TI	SA00003ZX00	4.7K	4.7K	NC	NC	NC	2K	V
PARADE	SA00007JU00	7.5K	NC	V	V	V	NC	NC

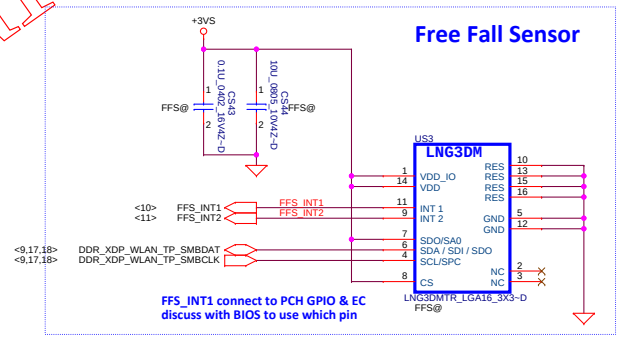


+5V_HDD Source

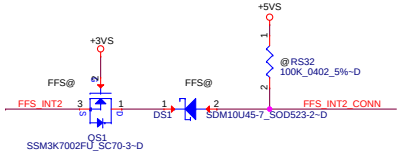
SHORT DEFAULT



Free Fall Sensor



FFS_INT1 connect to PCH GPIO & EC discuss with BIOS to use which pin



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Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

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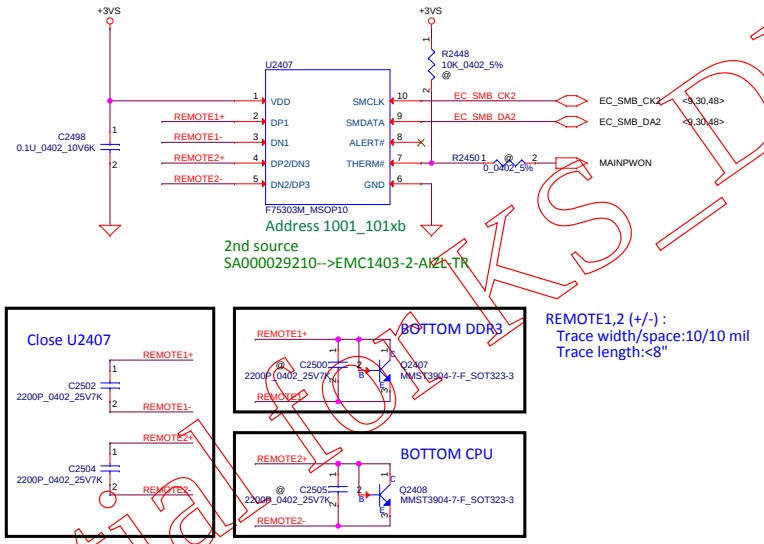
Compal Electronics, Inc.

Title: **HDD / Free Fall Sensor**

Document Number: **LA-B015P** Rev 0.1

Date: Wednesday, September 10, 2014 Sheet 32 of 56

Fintek thermal sensor placed near by TOP DDR3



Confidential_OKS_DFB @ 1024

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title: Thermal Sensor
				Size: A3 / Document Number: LA-B015P / Rev: 0.1
				Date: Wednesday, September 10, 2014 / Sheet 33 of 56

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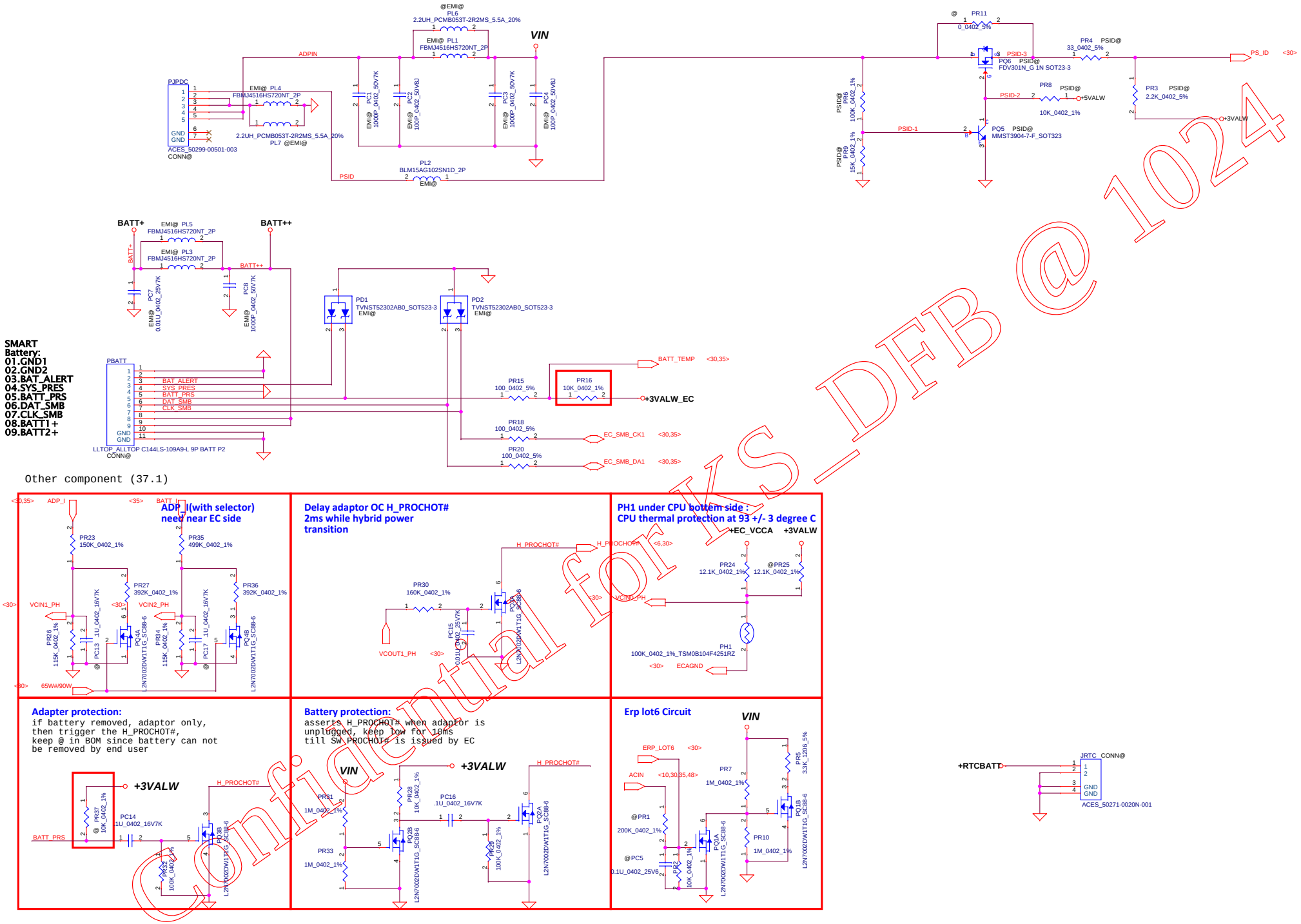

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Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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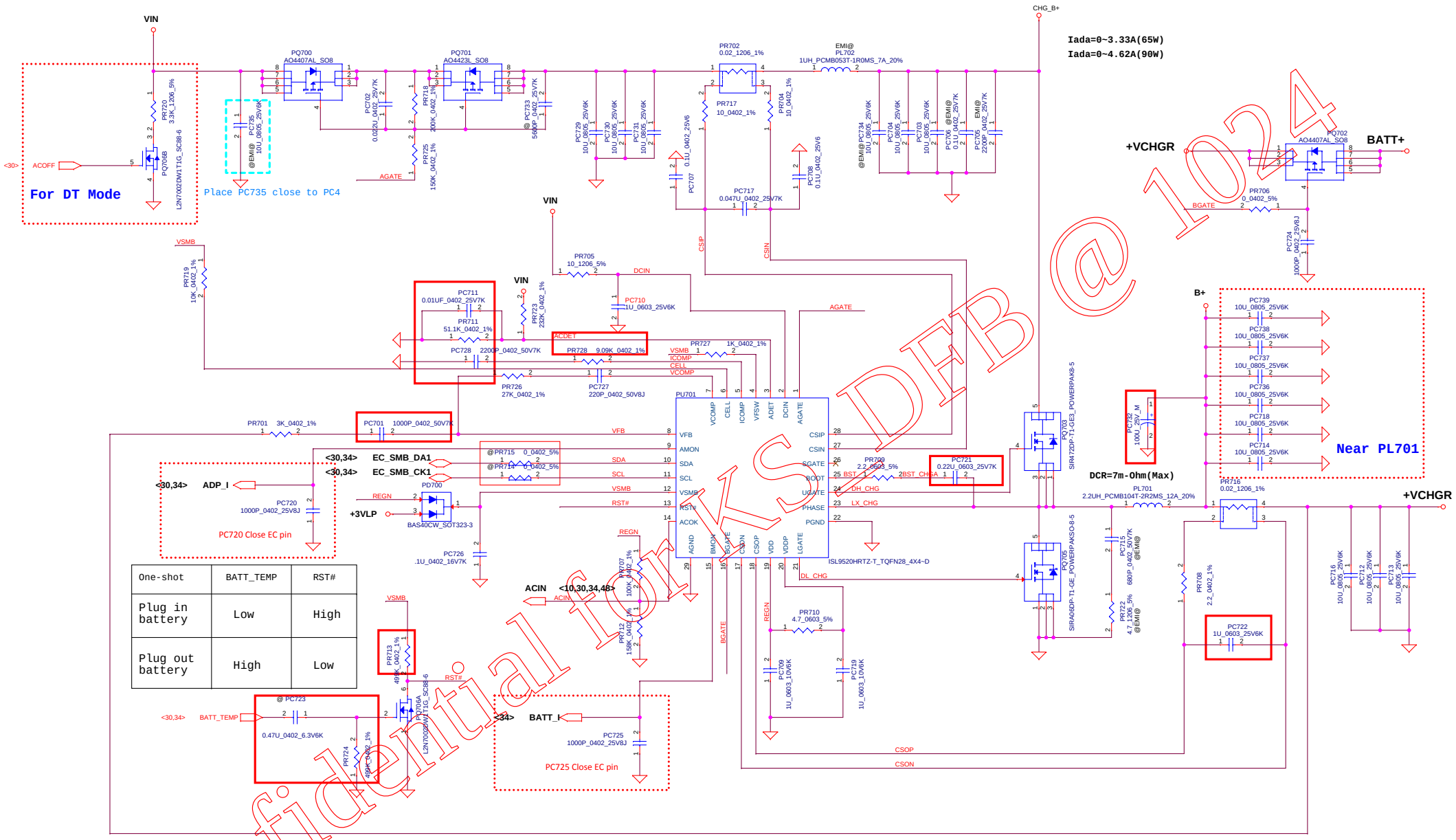
Compal Electronics, Inc.

Title: **PWR_DCIN/BATT CONN/OTP**

Size: | Document Number: **LA-B012P** | Rev: 1.0

Date: Wednesday, September 10, 2014 | Sheet 34 of 56



One-shot	BATT_TEMP	RST#
Plug in battery	Low	High
Plug out battery	High	Low

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Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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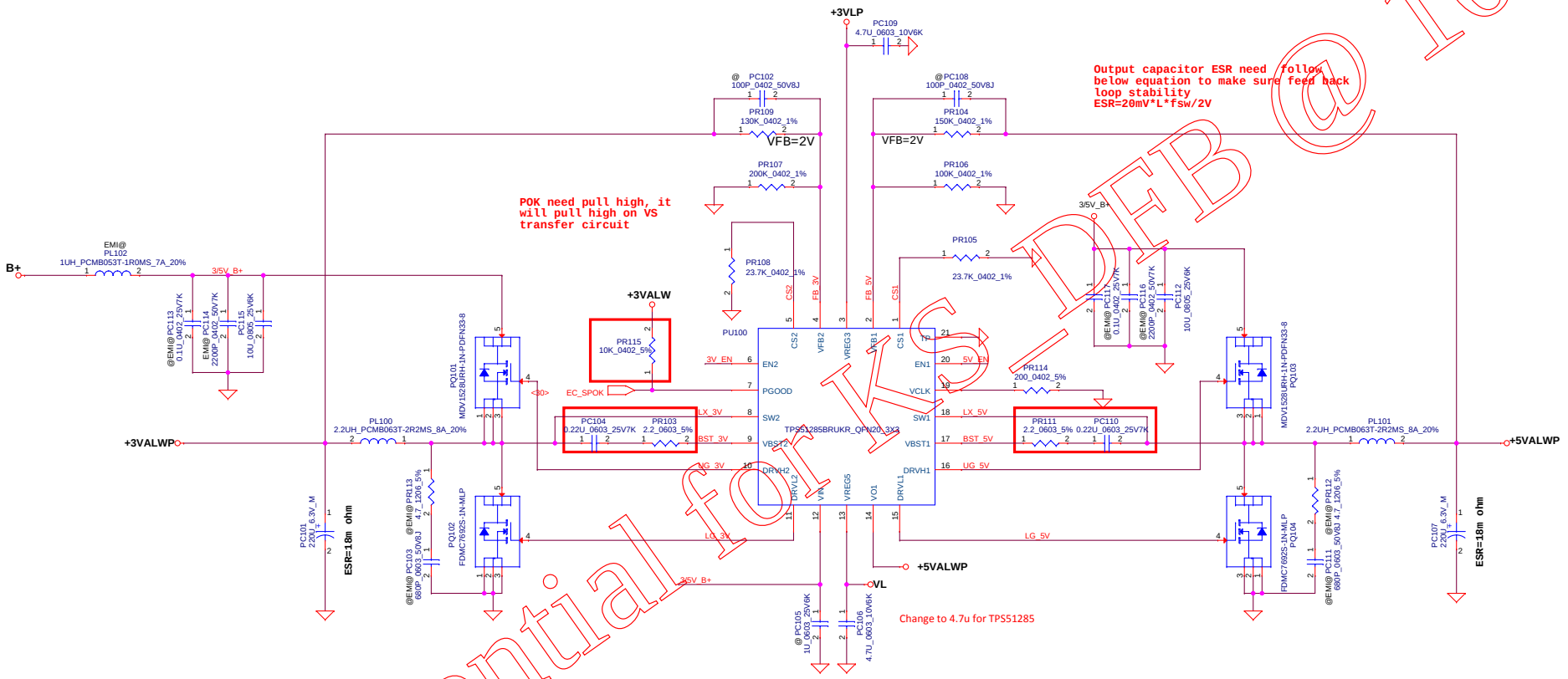
Compal Electronics, Inc.

Title: **PWR_CHARGER**

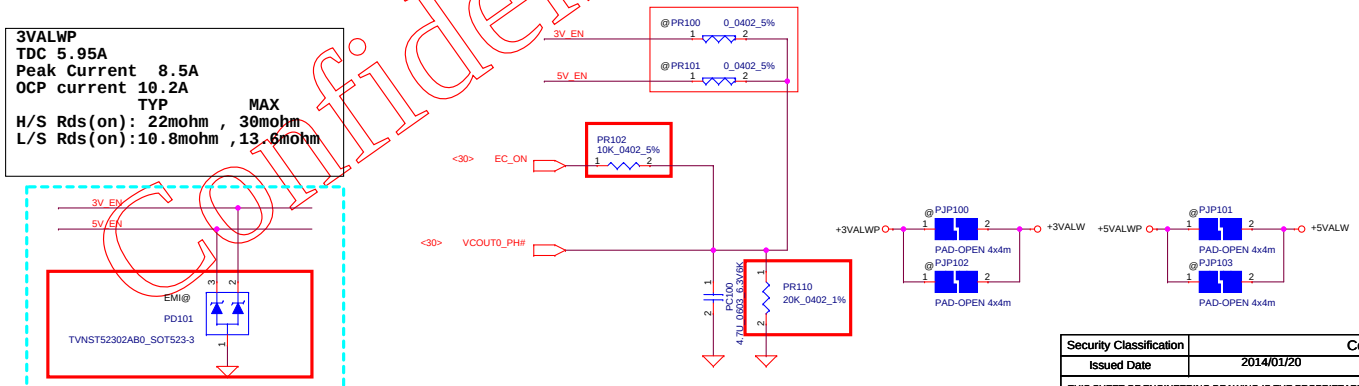
Size: A3 | Document Number: **LA-B012P** | Rev: 1.0

Date: Wednesday, September 10, 2014 | Sheet 35 of 56



3VALWP
TDC 5.95A
Peak Current 8.5A
OCP current 10.2A

	TYP	MAX
H/S Rds(on):	22mohm ,	30mohm
L/S Rds(on):	10.8mohm ,	13.6mohm



5VALWP
TDC 5.96A
Peak Current 8.51A
OCP current 10.2A

	TYP	MAX
H/S Rds(on):	22mohm ,	30mohm
L/S Rds(on):	10.8mohm ,	13.6mohm

Confidential for KS-DFB@1024

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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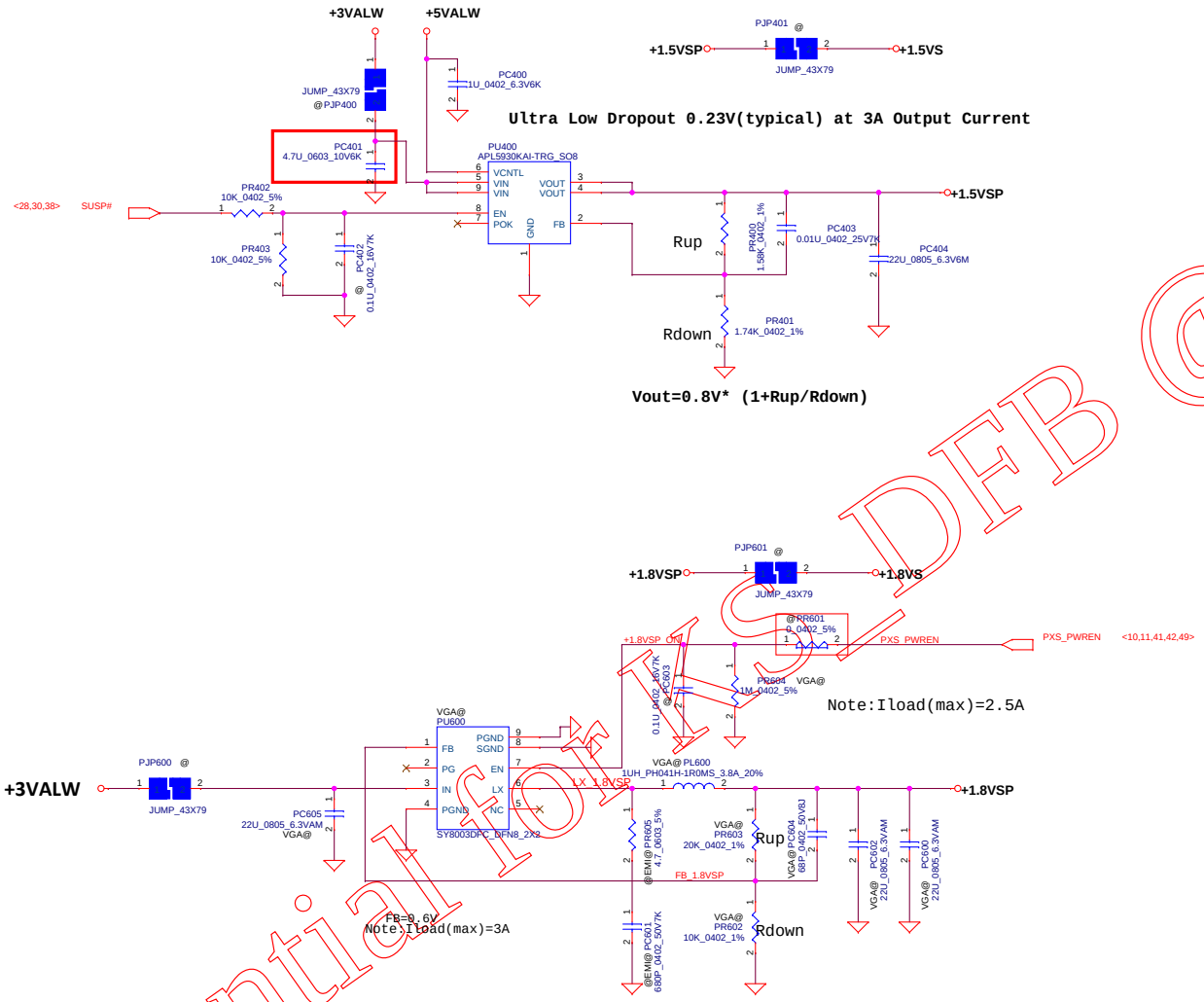
Compal Electronics, Inc.

Title: **PWR_3.3VALWP/5VALWP**

Size: A | Document Number: **LA-B012P** | Rev: 1.0

Date: Wednesday, September 10, 2014 | Sheet 36 of 56



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Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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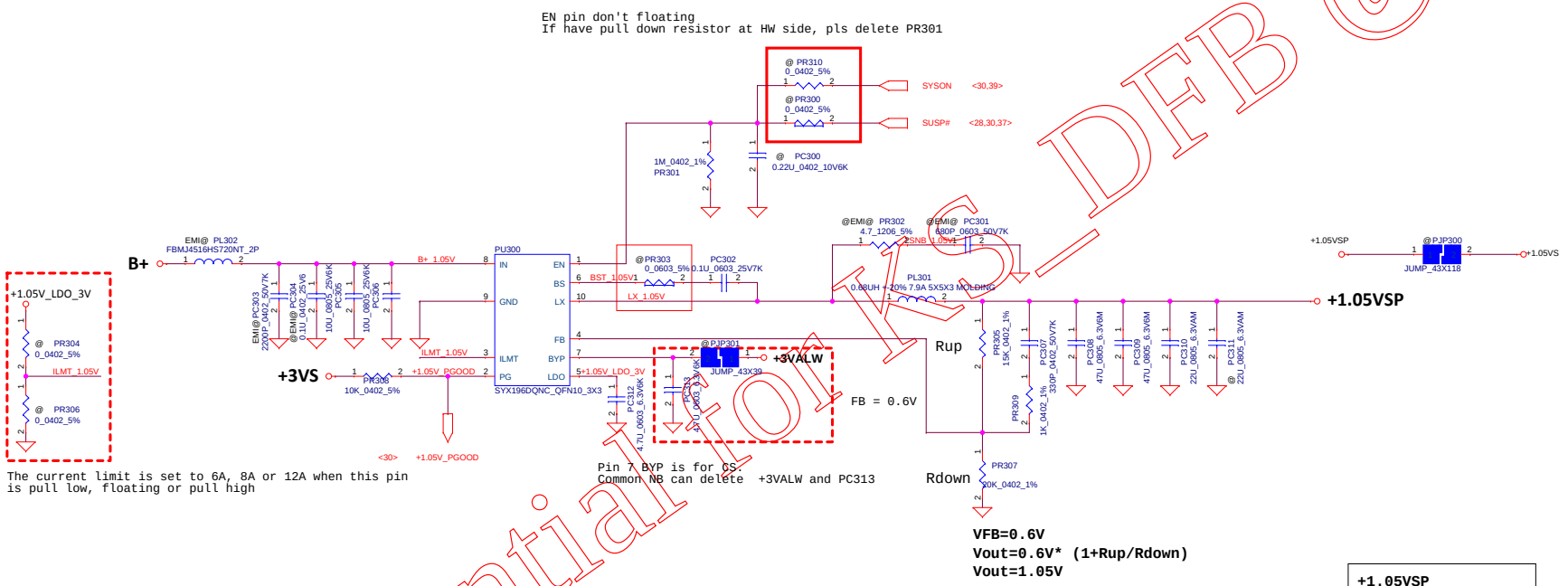
Compal Electronics, Inc.

Title: **PWR_1.5VSP / 1.8VSP**

Size: | Document Number: **LA-B012P** | Rev: 1.0

Date: Wednesday, September 10, 2014 | Sheet 37 of 56



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Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/01/20	Deciphered Date	2015/01/19	Title: PWR_+VCCIO
				Size: C; Document Number: LA-B012P; Rev: 1.0
				Date: Wednesday, September 10, 2014; Sheet 38 of 56

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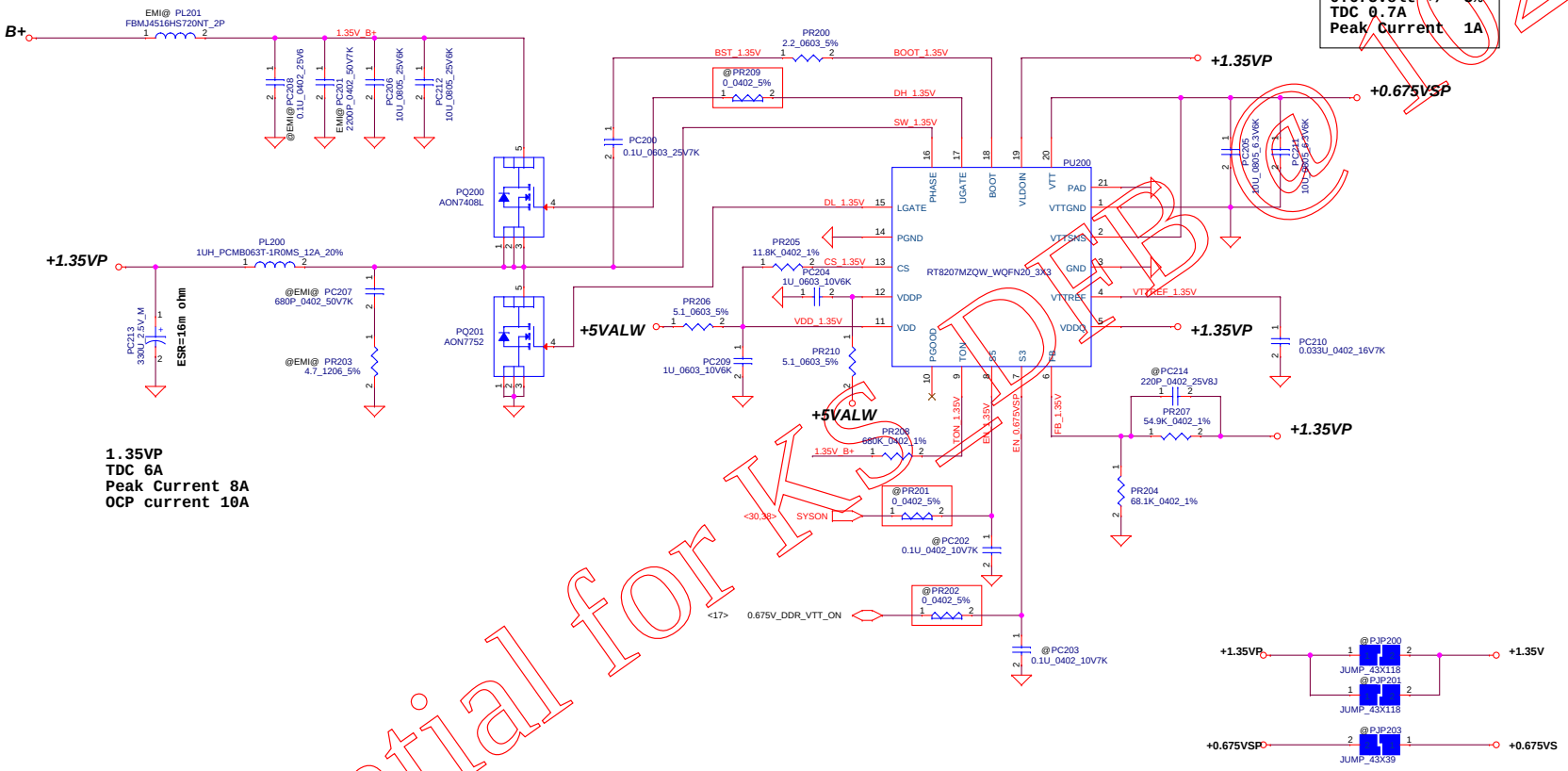

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Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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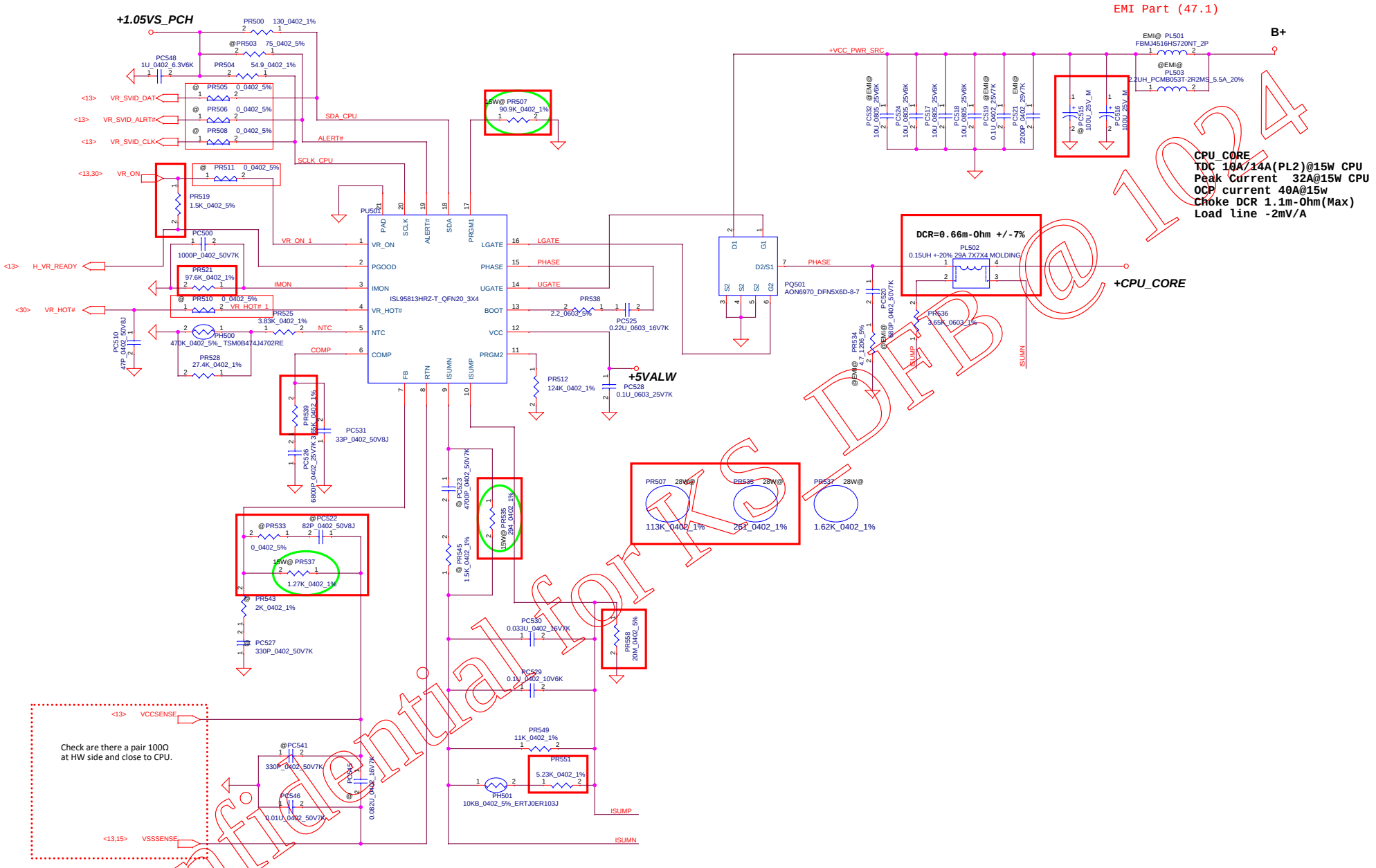
Compal Electronics, Inc.

Title: **PWR_+1.35VP/0.675VSP**

Document Number: **LA-B012P** | Rev 1.0

Date: Wednesday, September 10, 2014 | Sheet 39 of 56



Confidential for KS DPB@1024

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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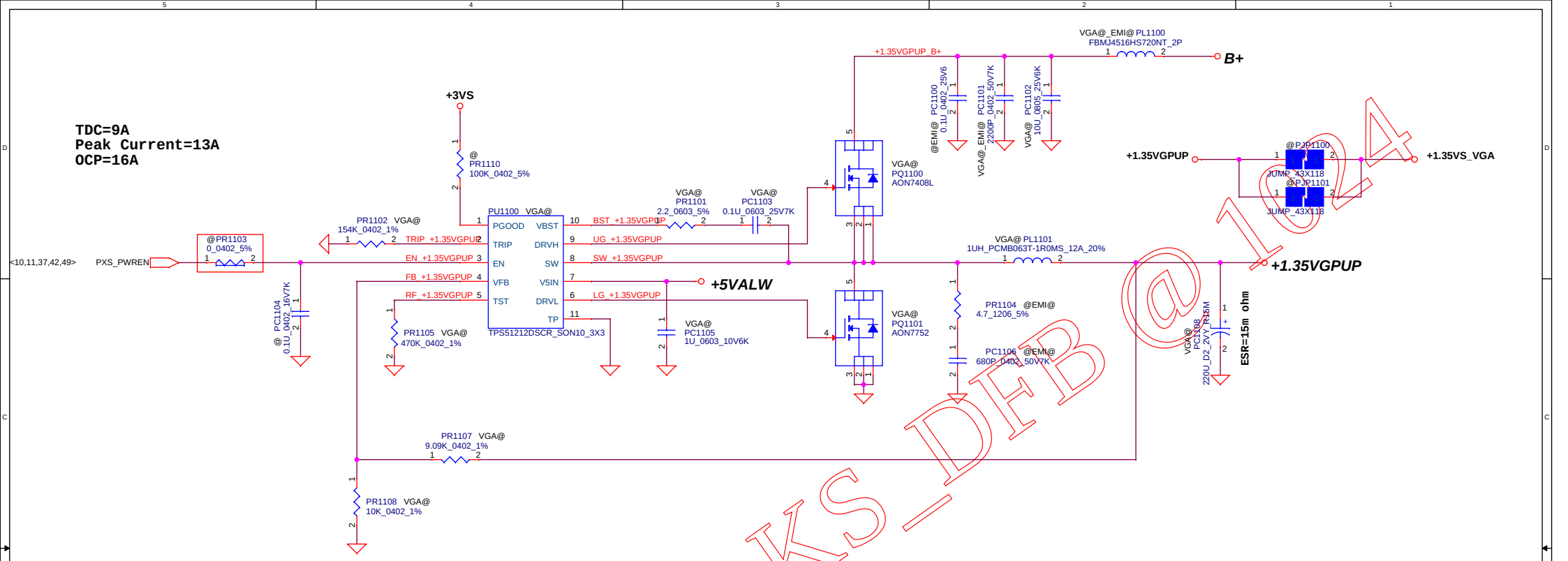
Compal Electronics, Inc.

Title: **PWR_VCORE**

Document Number: **LA-B012P** Rev 1.0

Date: Wednesday, September 10, 2014 Sheet 40 of 56



Confidential for KS_DFB @ 1024

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/01/20	Deciphered Date	2015/01/19	Title: PWR_+1.35VGPU
				Size: Document Number: LA-B012P — Rev: 1.0
				Date: Wednesday, September 10, 2014 — Sheet 41 of 56

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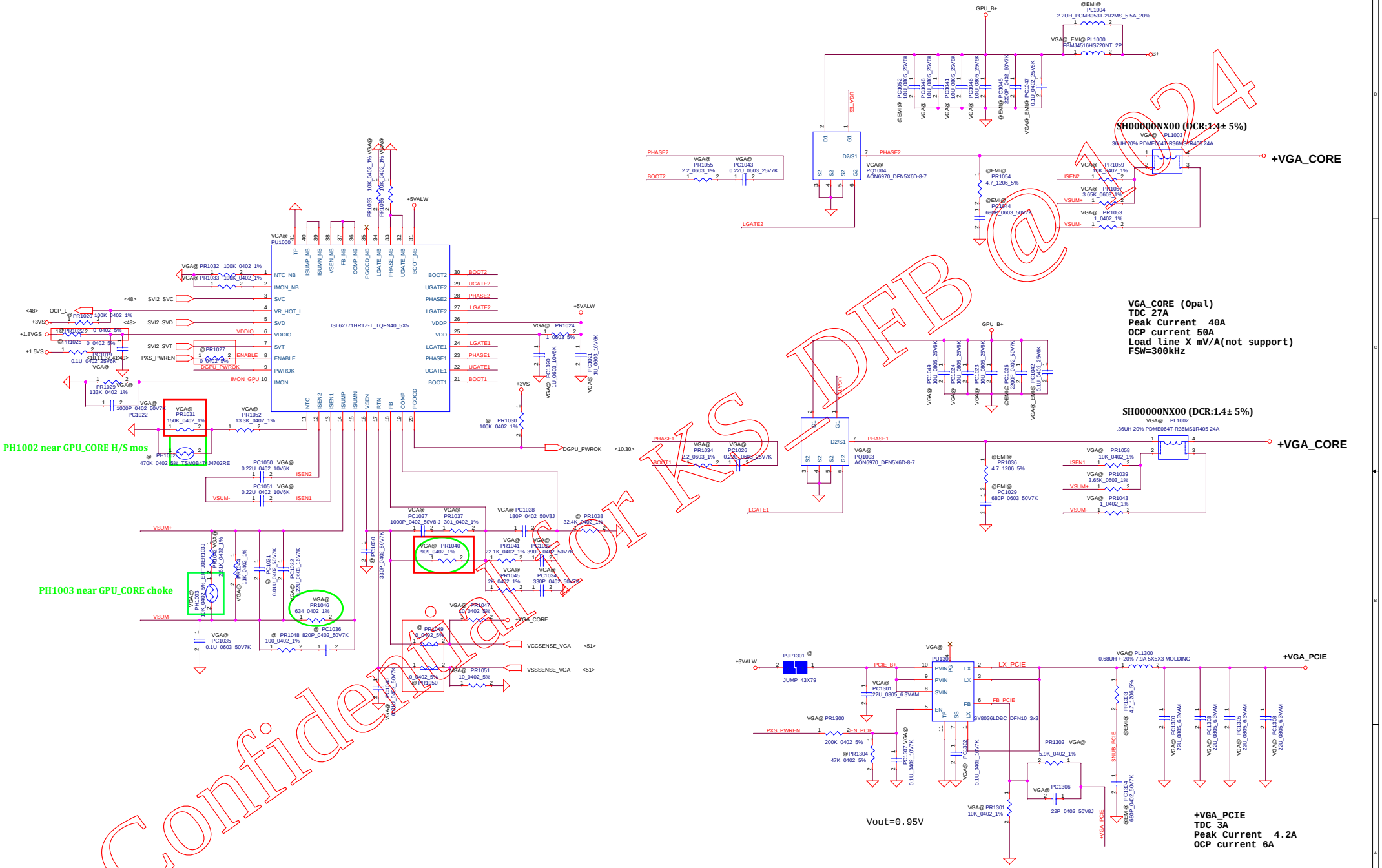

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Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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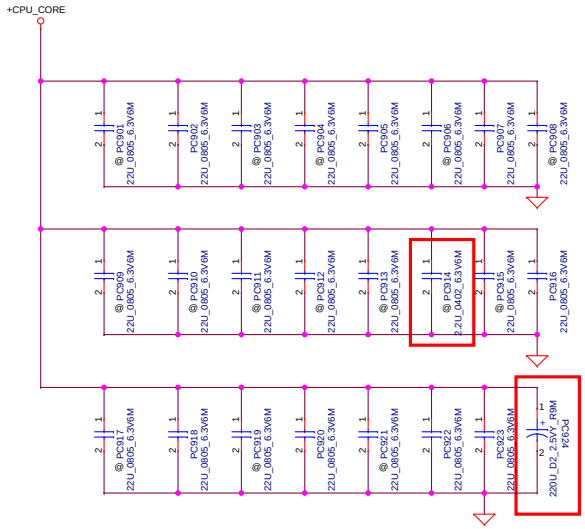
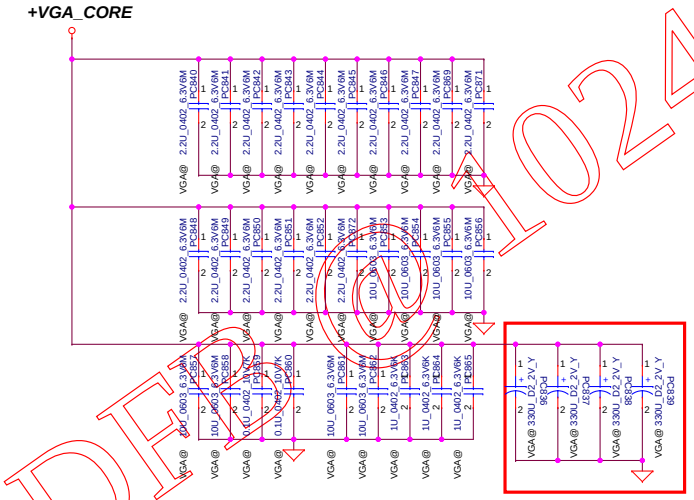
Compal Electronics, Inc.

Title: *PWR_VGA_CORE/PCIE*

Size: Custom | Document Number: *LA-B012P* | Rev: 1.0

Date: Wednesday, September 10, 2014 | Sheet 42 of 56





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Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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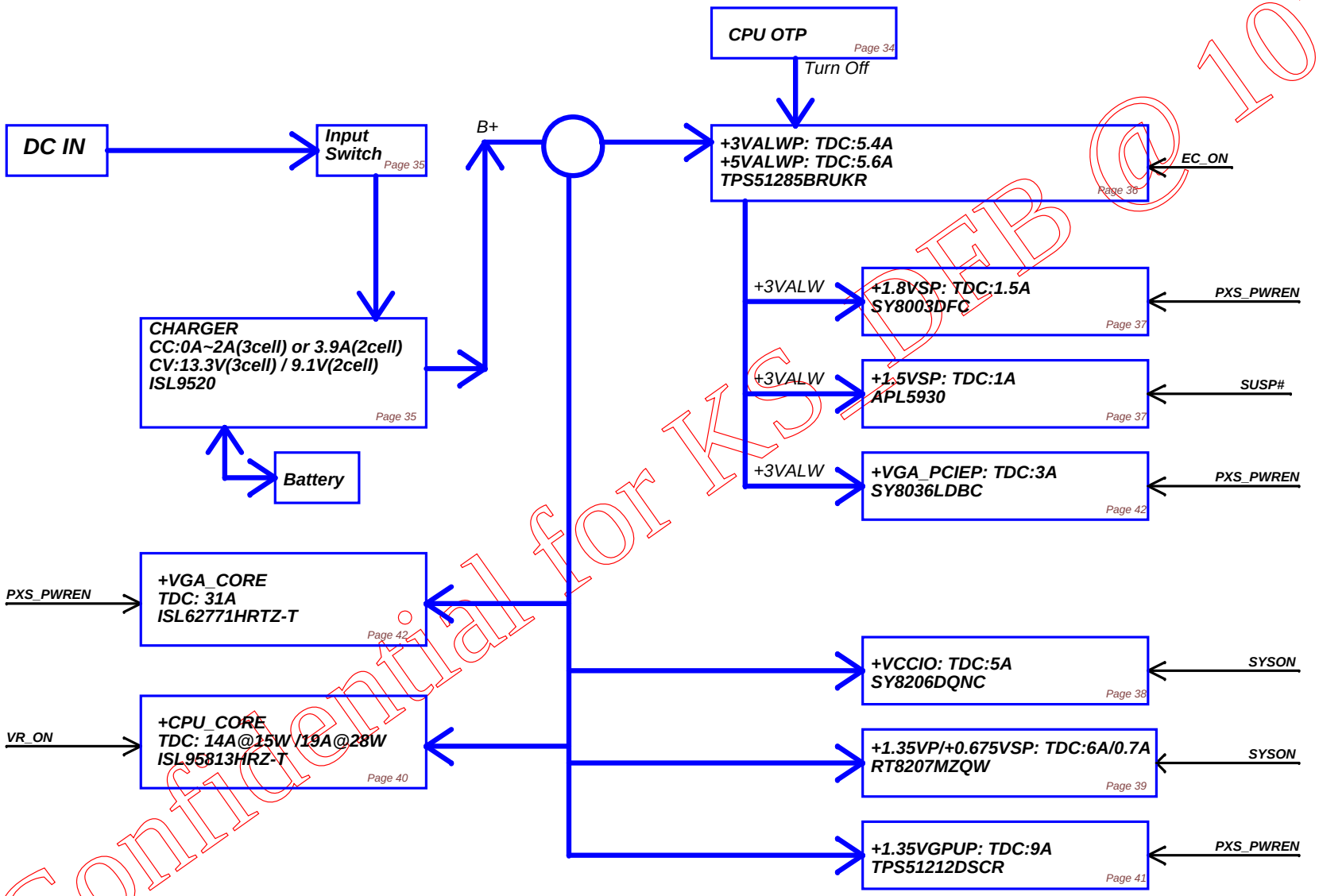
Compal Electronics, Inc.

Title: **PWR_PROCESSOR DECOUPLING**

Size: A3 | Document Number: **LA-B012P** | Rev: 1.0

Date: Wednesday, September 10, 2014 | Sheet 43 of 56

Power block



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Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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Compal Electronics, Inc.

Title: PWR_POWER BLOCK DIAGRAM

Document Number: LA-B012P

Rev: 1.0

Date: Wednesday, September 10, 2014

Version Change List (P. I. R. List) Page 1

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	44	DCIN/BATT CONN/OTP	13/10/24	Morris	design change	change PR16 from 100K to 10K add PR37 10K	0.2
2	45	CHARGER	13/10/24	Morris	design change	change PC711 from 1000pF to 0.01uF change PR711 from 49.9K to 51.1K change PR713 from 10K to 499K change PR724 from 100K to 499K change PC721 from 0.047u to 0.22u change PC722 from 0.1u to 1u add PC732 100u	0.2
3	46	3.3VALWP/5VALWP	13/10/24	Morris	design change for solve can't root issue	change PC104 from 0.1u to 0.22u change PC110 from 0.1u to 0.22u change PR102 from 2.2K to 10K add PR110 20K	0.2
4	50	VCORE	13/10/24	Morris	adjust CPU parameter	change PR507(15W@) from 90.9K to 169K change PR519 from 1.91K to 10K change PR521 from 95.3K to 97.6K change PR539 from 8.06K to 909 change PC515,PC516 from SF000005100 to SF000004M00 change PL502 from SH00000NM00 to SH00000PQ00 change PR535(15W@) from 340 to 210 change PR537 from 1.27K to 1.37K change PR535(28W@) from 432 to 261 change PR507(28W@) from 113K to 205K change PR551 from 2.61K to 5.23K add PC522 82pF add PR533 0-ohm	0.2
6	52	VGA_CORE/PCIE	13/10/24	Morris	design change from vendor change LL	change PR1040 from 1.24K to 825	0.2
7	53	PROCESSOR DECOUPLING	13/10/24	Morris	adjust CPU parameter	change PC924 from SGA20331E10 to SGA00009800 remove PC901,PC903,PC904,PC906,PC908,PC909,PC910,PC911,PC912,PC913,PC914,PC915,PC917,PC919,PC921	0.2
8	45	CHARGER	13/10/28	Morris	design change for plug out battery shut down issue	change PC723 from 0.01uF to 0.47uF change PR728 from 0 to 9.09K change PC728 from 4700pF to 2200pF change PC701 from 220pF to 1000pF	0.2
9	46	3.3VALWP/5VALWP	13/12/12	Morris	design change from EE request	add PR115 10K-ohm	0.3
10	50	VCORE	13/12/12	Morris	design change from Intel recommend	change PR519 from 10K to 1.5K	0.3
11	48	+VCCIO	13/12/13	Morris	design change from EE request	delete PR310 and add PR300 0-ohm	0.3
12	50	VCORE	14/01/20	Morris	adjust CPU parameter	change PR507(15W@) from 169K to 90.9K change PR507(28W@) from 205K to 113K	1.0
13	53	PROCESSOR DECOUPLING	14/02/18	Morris	design change from thermal request	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0
14	50	VCORE	14/03/03	Morris	design change for VGA thermal issue	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0

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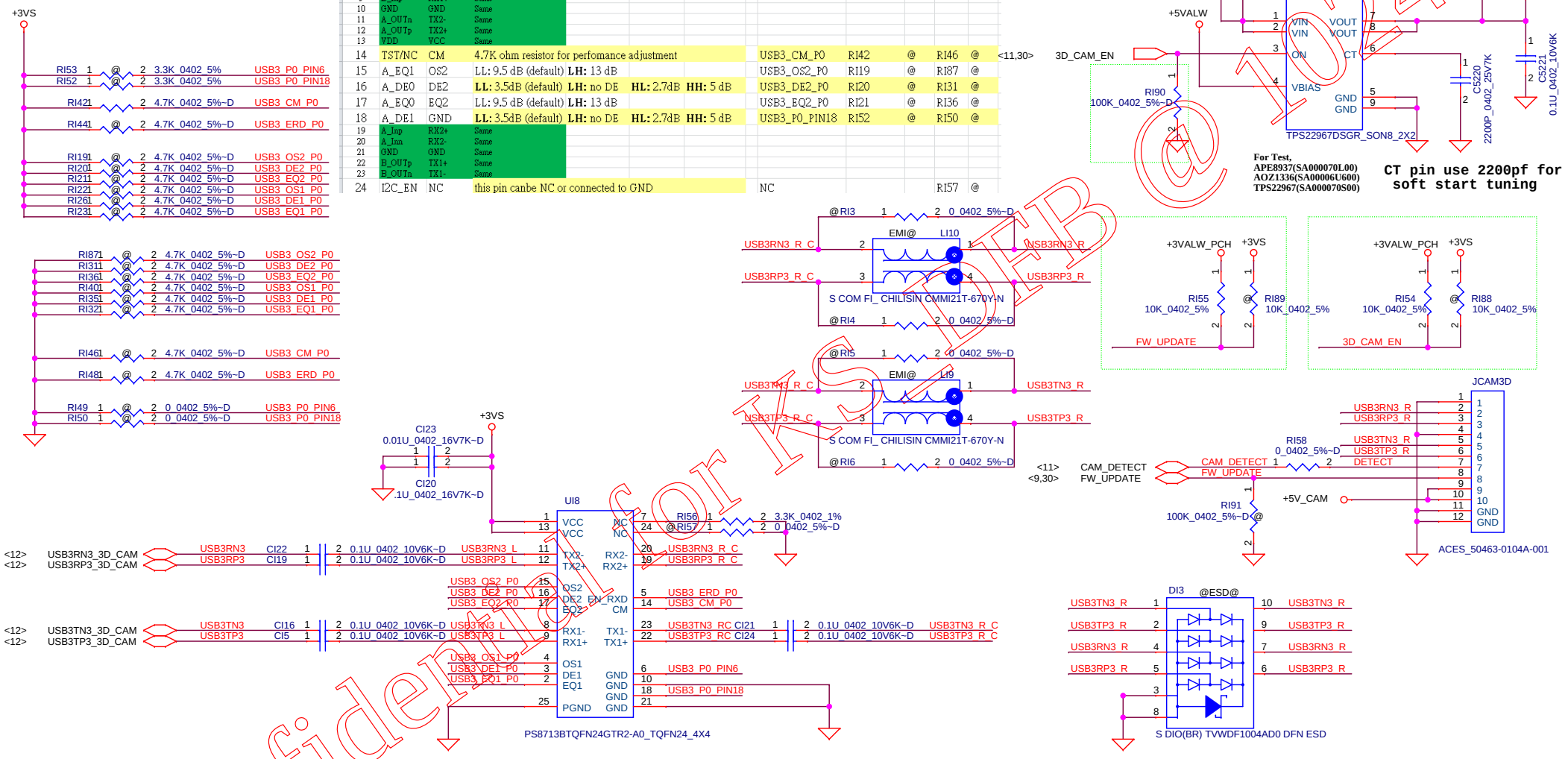
Vendor	PS8713B	TI	Spec				schematic netname	3Vs		GND	
1	VDD	VCC	Same								
2	B_EQ0	EQ1	LL: 9.5dB (default)	LH: 13dB	HL: 4.5dB	HH: 7.7 dB	USB3_EQ1_P0	RI23	@	RI32	@
3	DE0	DE1	LL: 3.5dB (default)	LH: no DE	HL: 2.7dB	HH: 5 dB	USB3_DE1_P0	RI26	@	RI35	@
4	EQ1	OS1	LL: 9.5dB	LH: 13dB	HL: 4.5dB	HH: 7.7 dB	USB3_OS1_P0	RI22	@	RI40	@
5	PD#	EN_RXD	it can be left open				USB3_ERD_P0	RI44	@	RI48	@
6	B_DE1	GND	LL: 3.5dB (default)	LH: no DE	HL: 2.7dB	HH: 5 dB	USB3_P0_PIN6	RI53	@	RI49	@
7	REXT	NC		4.99K						RI56	4.99K
8	B_Inn	RX1-	Same								
9	B_Inp	RX1+	Same								
10	GND	GND	Same								
11	A_OUTn	TX2-	Same								
12	A_OUTp	TX2+	Same								
13	VDD	VCC	Same								
14	TST/NC	CM	4.7K ohm resistor for perfomance adjustment				USB3_CM_P0	RI42	@	RI46	@
15	A_EQ1	OS2	LL: 9.5 dB (default)	LH: 13 dB			USB3_OS2_P0	RI19	@	RI87	@
16	A_DE0	DE2	LL: 3.5dB (default)	LH: no DE	HL: 2.7dB	HH: 5 dB	USB3_DE2_P0	RI20	@	RI31	@
17	A_EQ0	EQ2	LL: 9.5 dB (default)	LH: 13 dB			USB3_EQ2_P0	RI21	@	RI36	@
18	A_DE1	GND	LL: 3.5dB (default)	LH: no DE	HL: 2.7dB	HH: 5 dB	USB3_P0_PIN18	RI52	@	RI50	@
19	A_Inp	RX2+	Same								
20	A_Inn	RX2-	Same								
21	GND	GND	Same								
22	B_OUTp	TX1+	Same								
23	B_OUTn	TX1-	Same								
24	I2C_EN	NC	this pin canbe NC or connected to GND				NC			RI57	@



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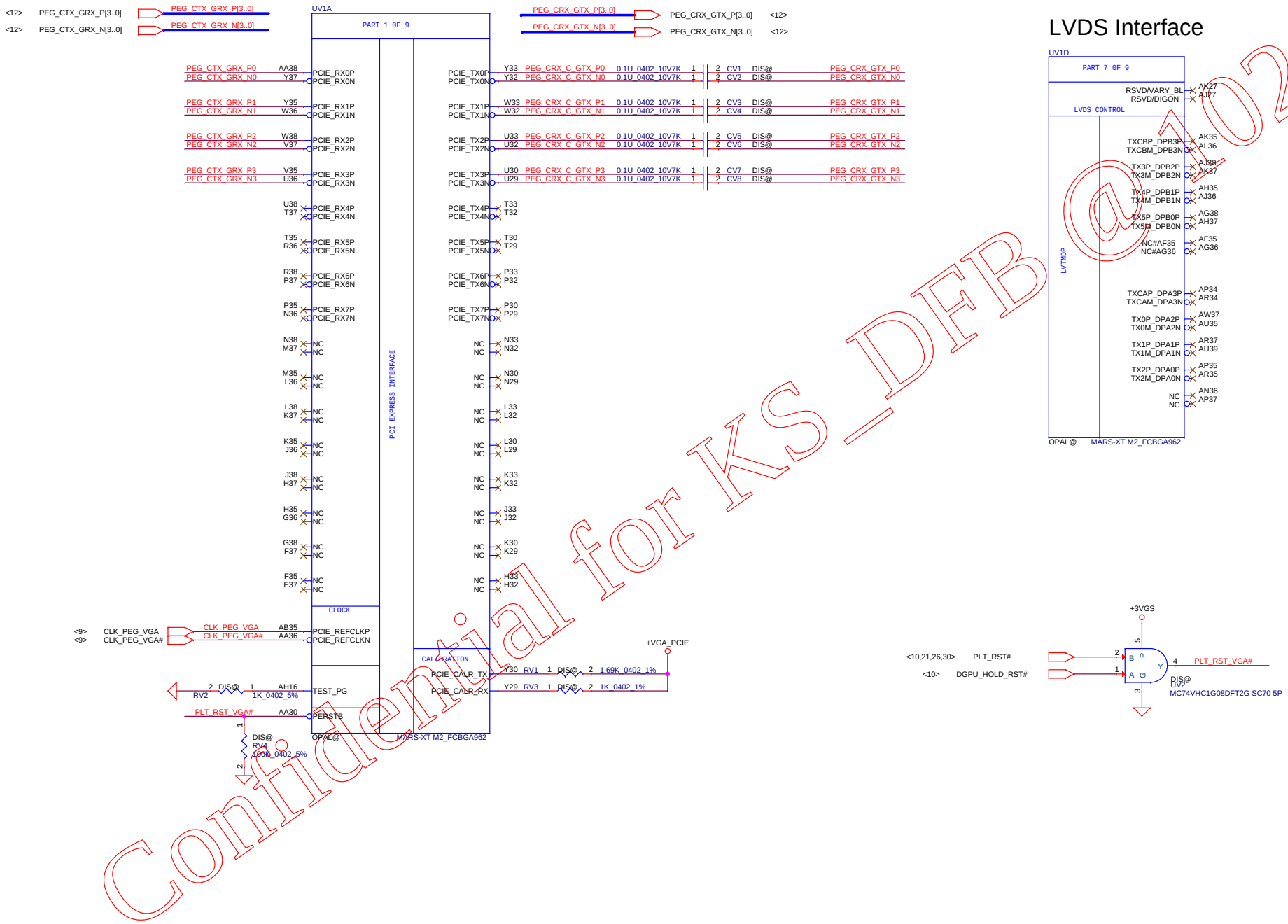
Title: **3D CAMERA**

Size | Document Number: **LA-B015P** | Rev: 0.1

Date: Wednesday, October 22, 2014 | Sheet 46 of 56



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title: AMD_OPAL-XT_M2_PCIE/LVDS
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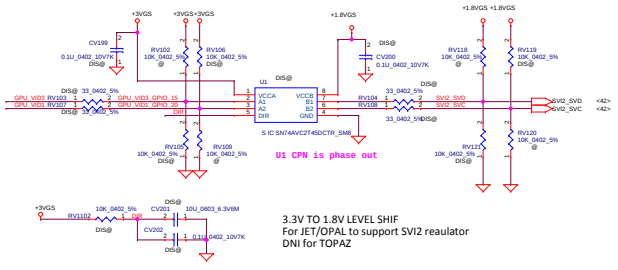
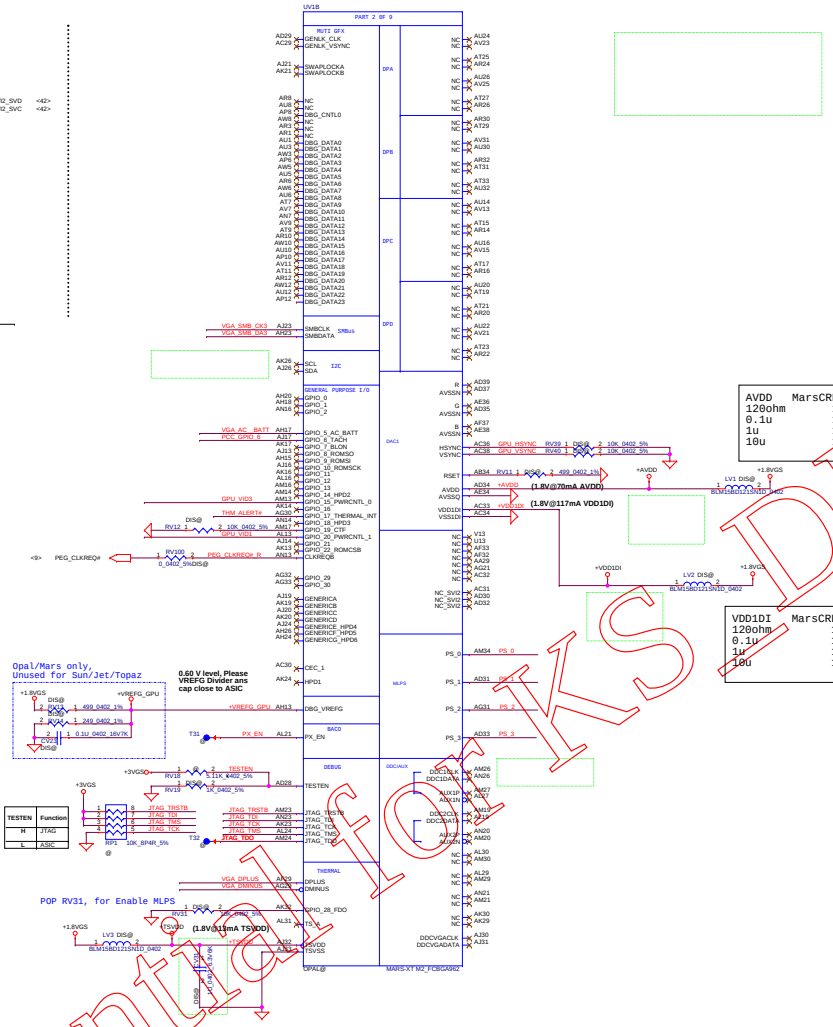
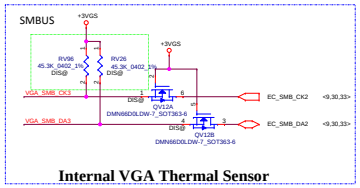
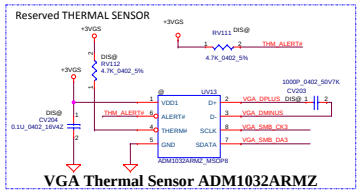
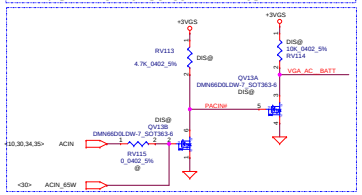
				Date: Wednesday, September 10, 2014; Sheet 47 of 56

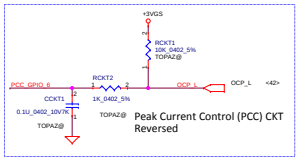












CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

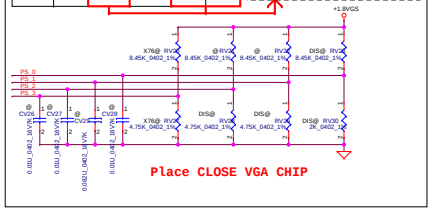
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_ENB	PS_1[4]	Transmitter Power Savings Enable 0:50% Tx output swing 1:Full Tx output swing	1
TX_DEEMPH_EN	PS_1[5]	PCIE Transmitter De-emphasis Enable 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	0
BIF_GEN3_EN_A	PS_1[1]	PCIE Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped to 0) 0:GEN3 not support at power-on 1:GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	VGA control 0:VGA controller capacity enabled 1:VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	Serial ROM type & Memory Aperture Size select if PS_2[3]=0, default memory aperture size if PS_2[3]=1, ignore ROM type 100 - 512Kbit Atmel25D05A (SO) 101 - 1Mbit M25P10 (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV010 (Chingis) 101 - 1Mbit Pm25LV020 (Chingis)	100
BIOS_ROM_EN	PS_2[0]	Enable external BIOS ROM device 0:Disabled 1:Enabled	0
AUD[1] AUD[0]	PS_2[1] NA	00 : No audio function 01 : Audio for DP only 10 : Audio for DP and HDMI if dongle is detected 11 : Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It isthe responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
BIF_DPI	PS_2[2]	Reserved for future ASIC	1
		NOTE:ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED	PS_1[3]	Reserved	0
RESERVED	PS_1[2]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2]	PS_3[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX
AUD_PORT_CONN_PINSTRAP[1]	PS_3[4]		
AUD_PORT_CONN_PINSTRAP[3]	PS_0[5]		

MLPS Strap

	Bits[3:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[3:1]	1 1	001	NC	8.45K	2K
PS_1[3:1]	11	0 0 0	NC	NC	4.75K
PS_2[3:1]	11	0 0 0	NC	NC	4.75K
PS_3[3:1]	1 1	X X X	NC	X	X

Mapping to VRAM type please refer to memory table



Bits [3:1] Memory ID	P/N	Vendor	vendor part number	Size	RV20	RV27
111	SA000076P0L	SAMSUNG	K4W4G1646D-BC1A	4GB	4.75K	NC
(default) 000	SA00006E80L	HYNIX	H5TC4G63AFR-11C	4GB	NC	4.75K
001	SA000077K0L	Micron	MT41J256M16HA-093G:E	4GB	8.45K	2K

MLPS implementation:
- ★Place MLPS circuit components as close to ASIC as possible
- ★Total DC resistance of trace between PS pin and C should be less than 2 ohm
- ★Total DC resistance of trace between C and ground should be less than 2 ohm
- ★Trace capacitance should be less than 100pf.
- ★Resistors should be of +-1% tolerance

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Title: AMD_OPAL-XT_M2_Main_MSIC

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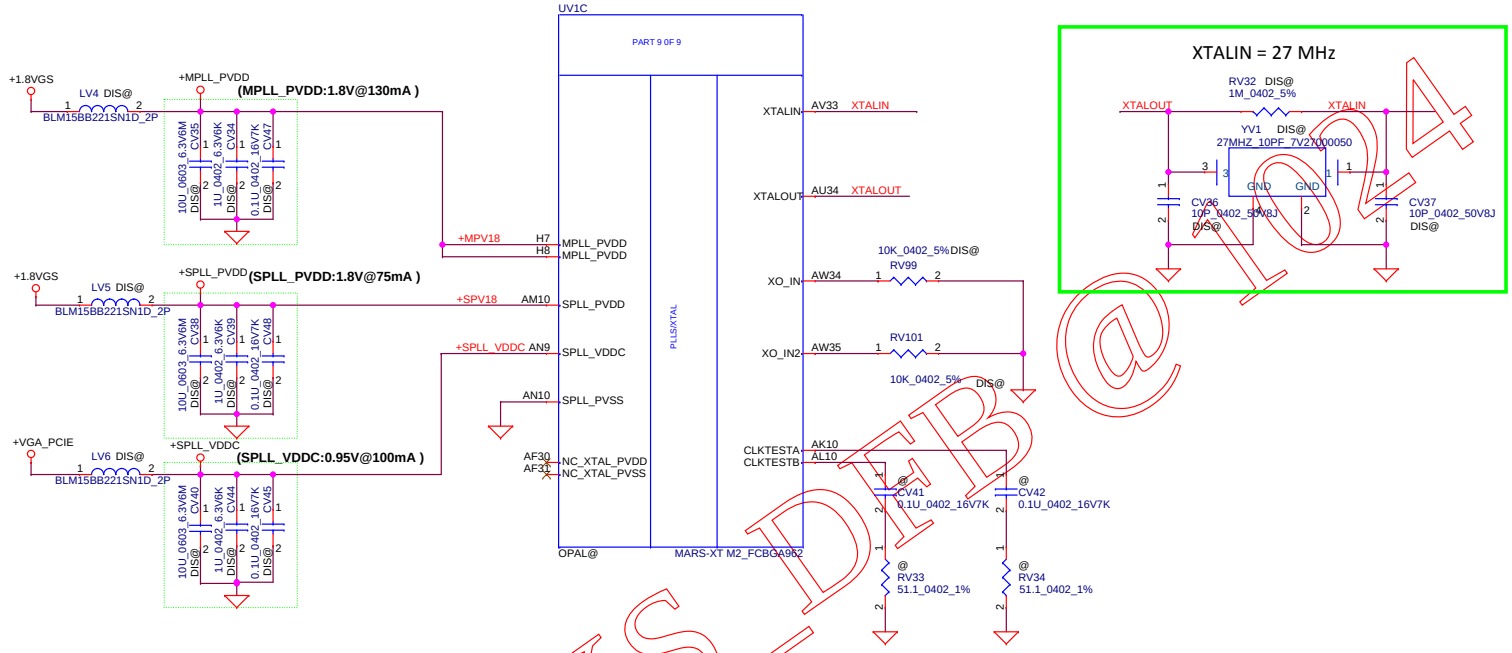
Date: Tuesday, September 16, 2014 | Sheet 48 of 58

MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



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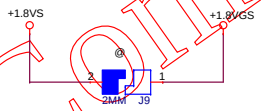
+1.35VS_VGA TO +1.35V_MEM_GFX

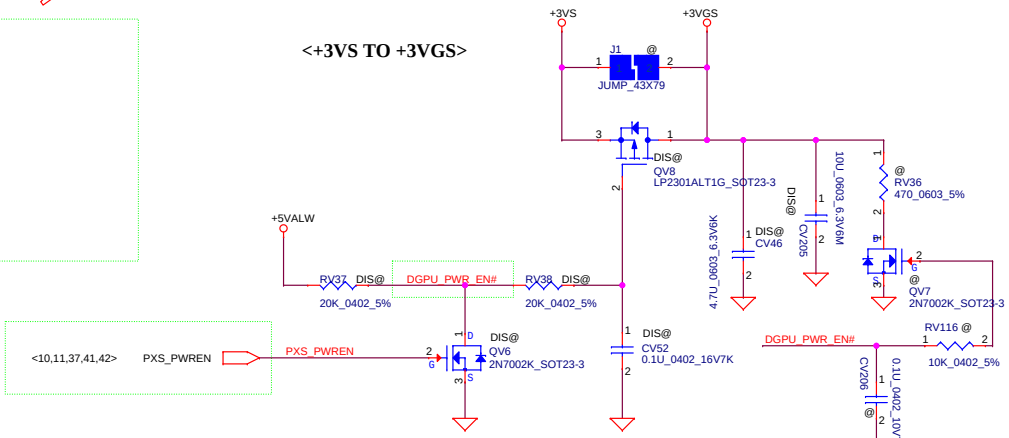
SHORT DEFAULT

+1.8VS TO +1.8VGS



SHORT DEFAULT

<+3VS TO +3VGS>



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Issued Date	2014/04/01	Deciphered Date	2015/04/30

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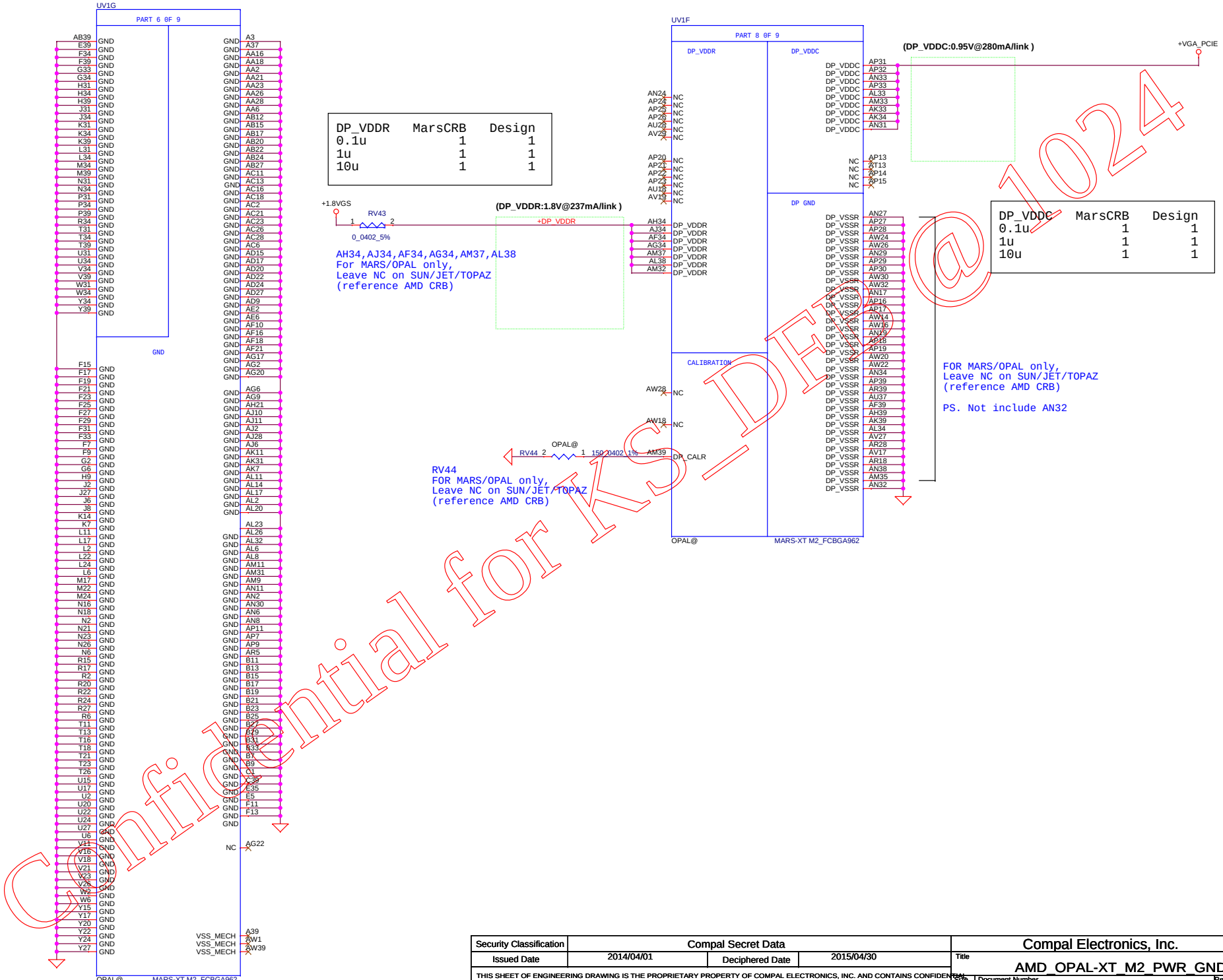
Compal Electronics, Inc.

Title: AMD_OPAL-XT_M2_BACO POWER

Size: Custom | Document Number: LA-B015P | Rev: 0.1

Date: Wednesday, September 10, 2014 | Sheet 49 of 56



DP_VDDR	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

DP_VDDC	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

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Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

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Compal Electronics, Inc.

Title: AMD_OPAL-XT_M2_PWR_GND

Size: Custom | Document Number: LA-B015P | Rev: 0.1

Date: Wednesday, September 10, 2014 | Sheet 50 of 56

VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

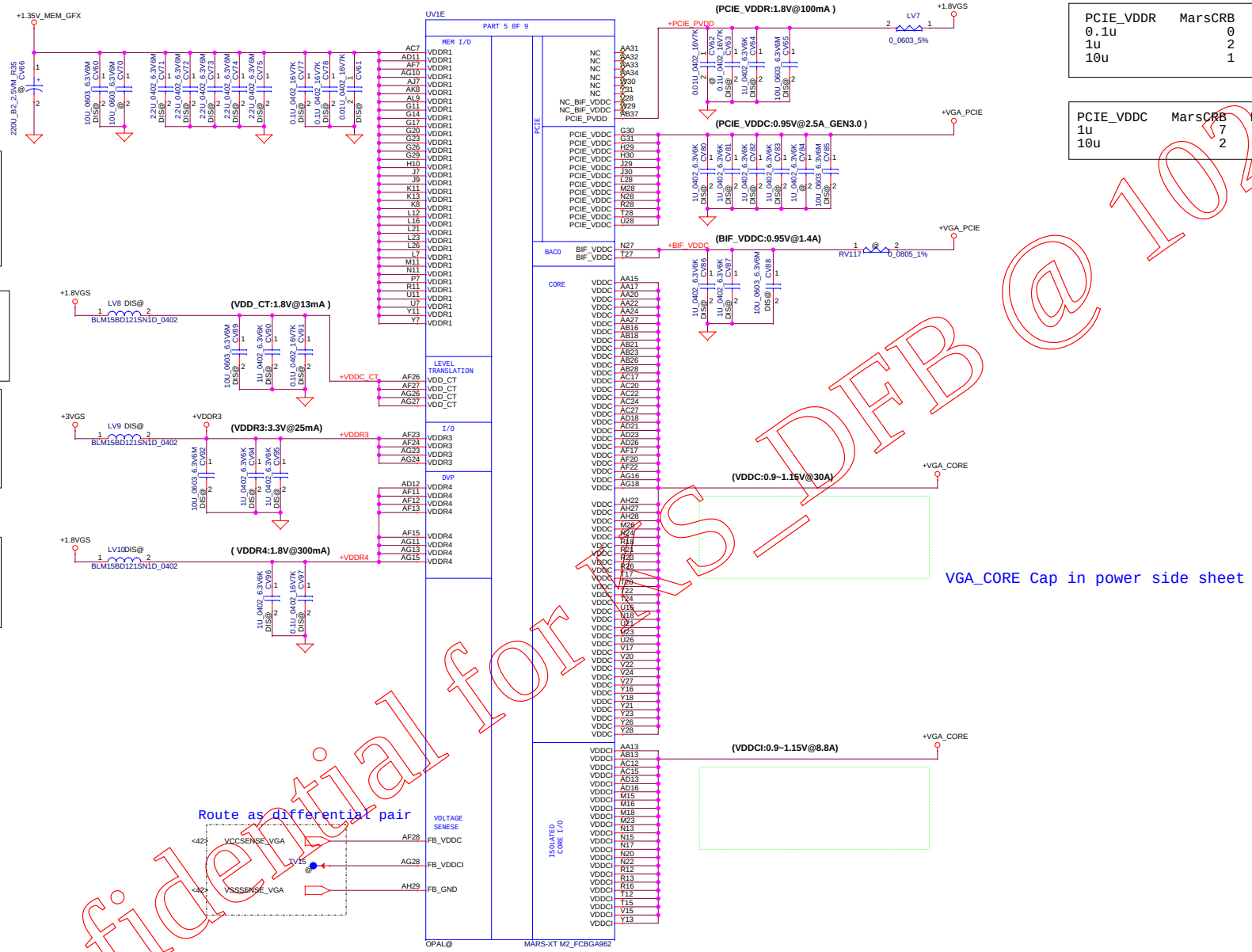
VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0

PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1



VGA_CORE Cap in power side sheet

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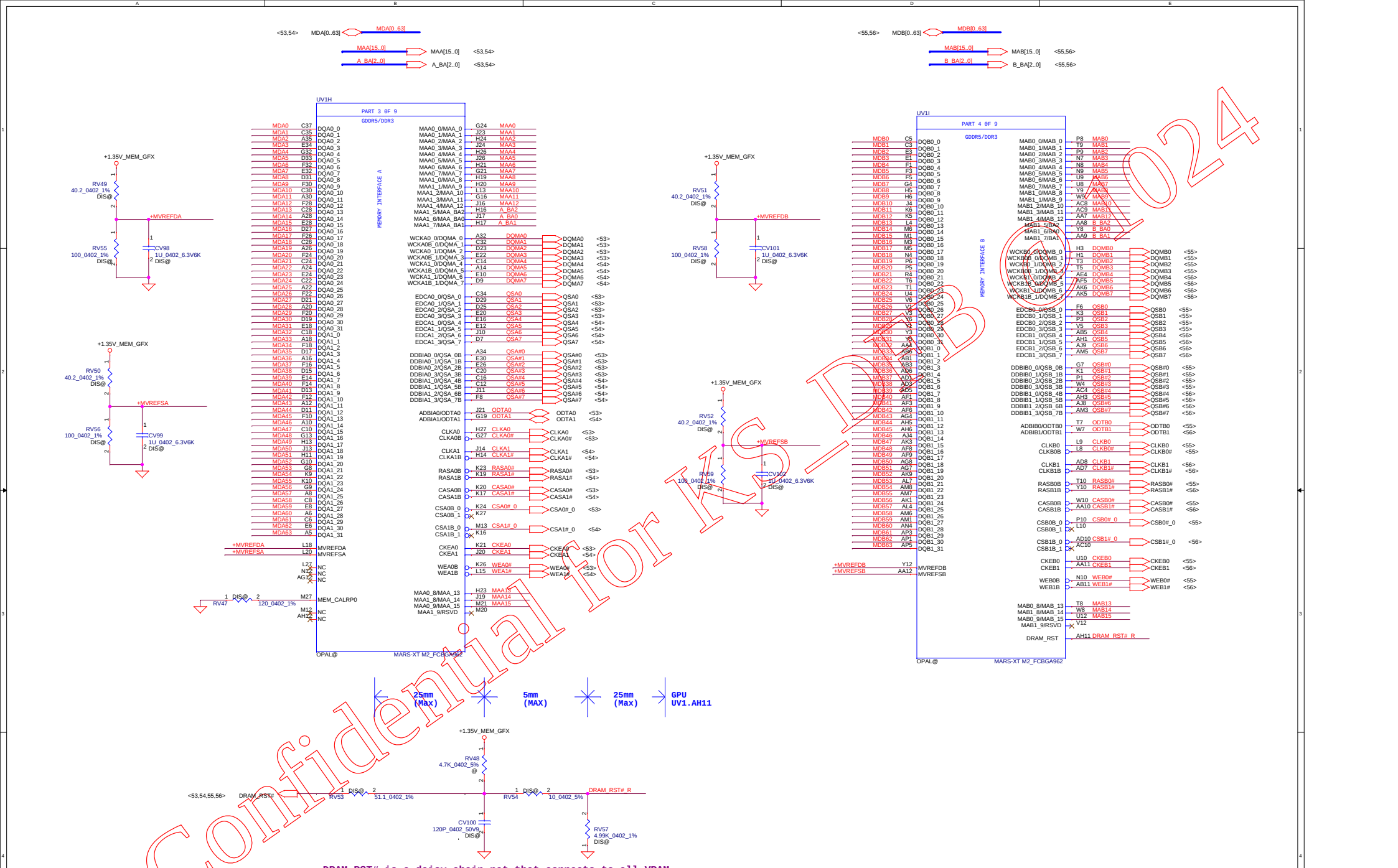
Title: AMD_OPAL-XT_M2_Power

Size: C | Document Number: LA-B015P | Rev: 0.1

Date: Wednesday, September 10, 2014 | Sheet 51 of 56



DRAM_RST# is a daisy-chain net that connects to all VRAM

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

Ball to RV57 < 1"
CV100 to RV57 < 200 mil
CV100 to RV53 < 1"

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Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title: AMD_OPAL-XT_M2_MEM IF

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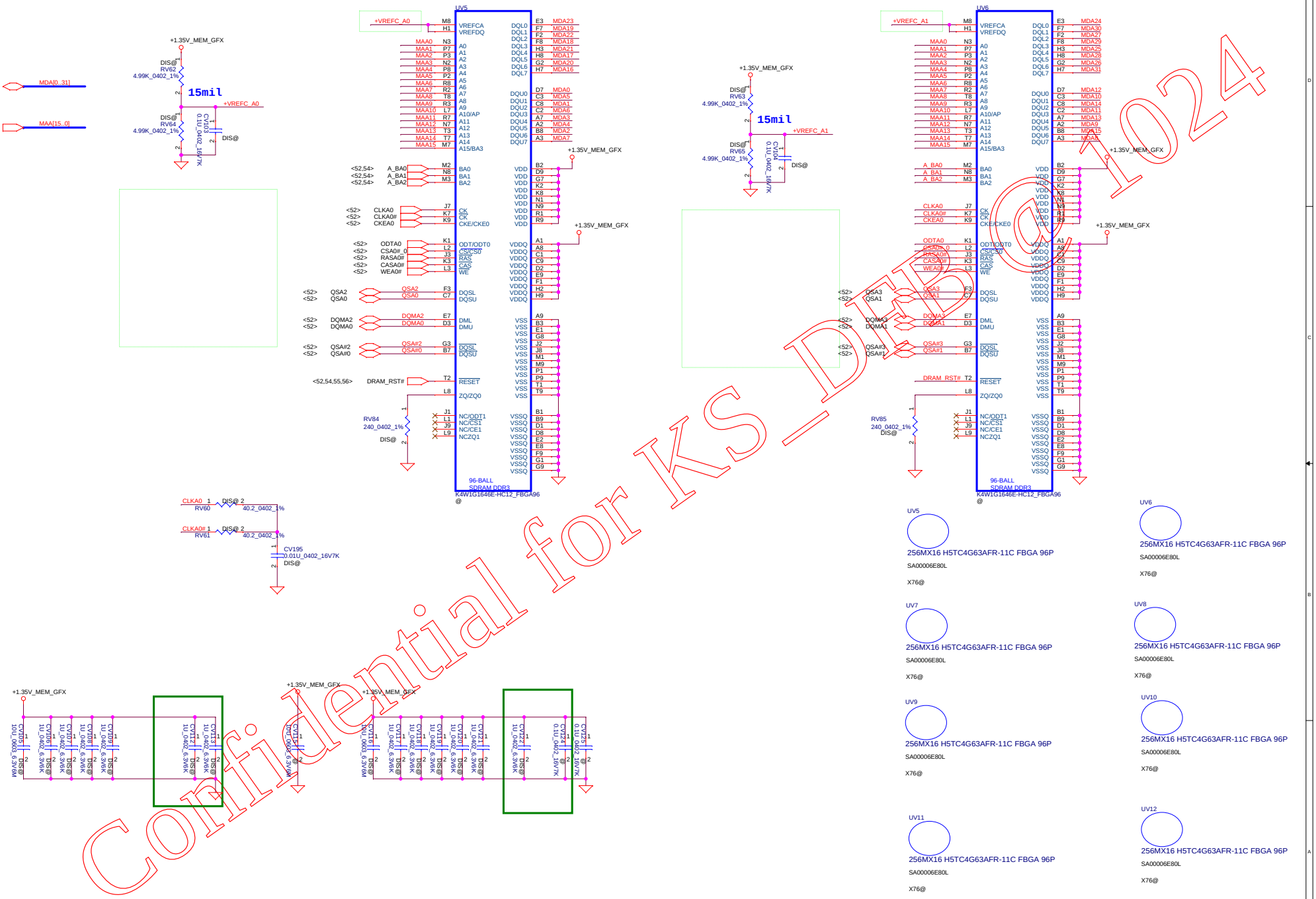
Size	Document Number	Rev
C	LA-B015P	0.1

Date: Wednesday, September 10, 2014 Sheet 52 of 56



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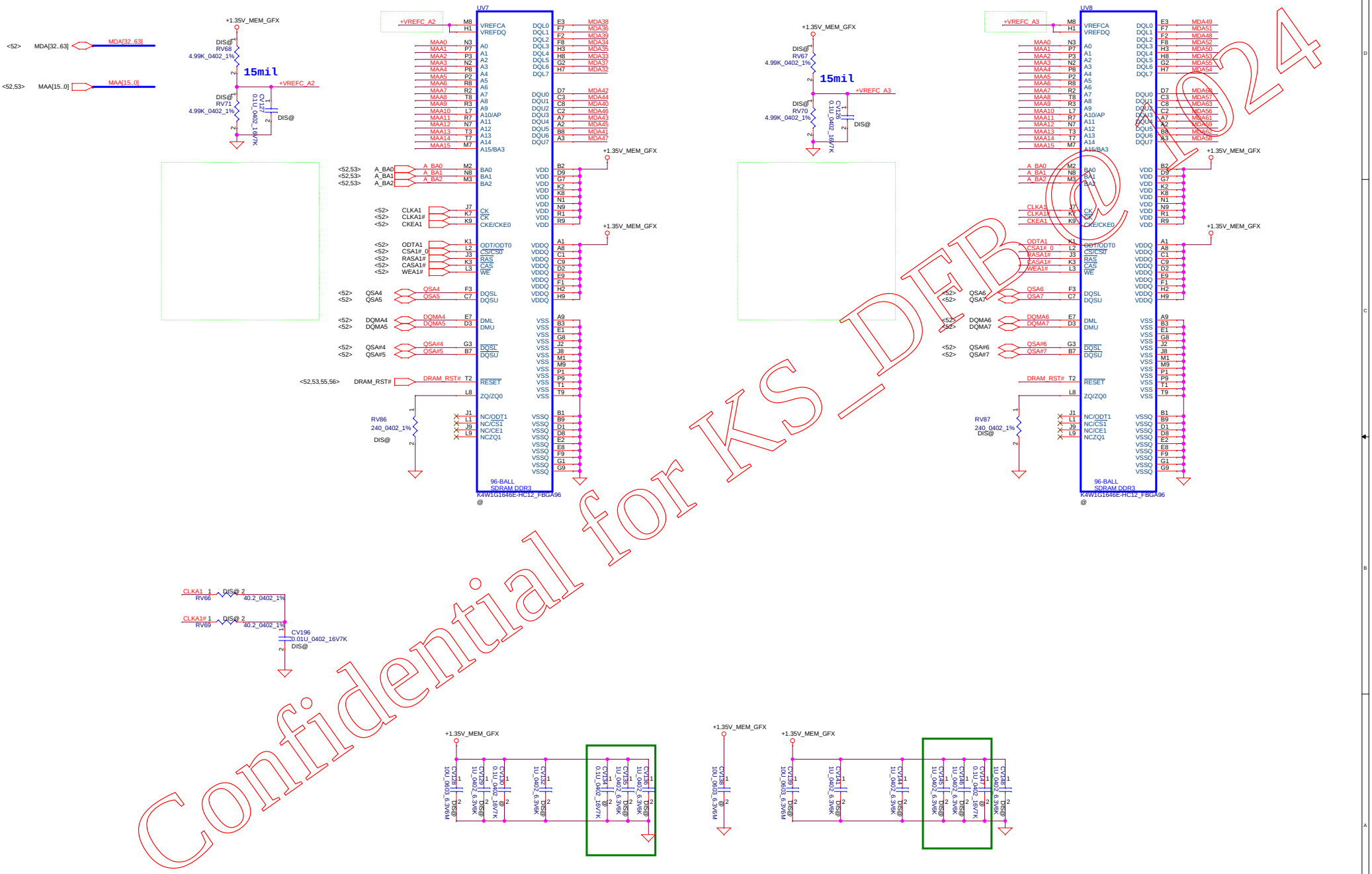
Title: AMD_OPAL-XT_M2_VRAM_A0

Size: C | Document Number: LA-B015P | Rev: 0.1

Date: Wednesday, September 10, 2014 | Sheet 53 of 56



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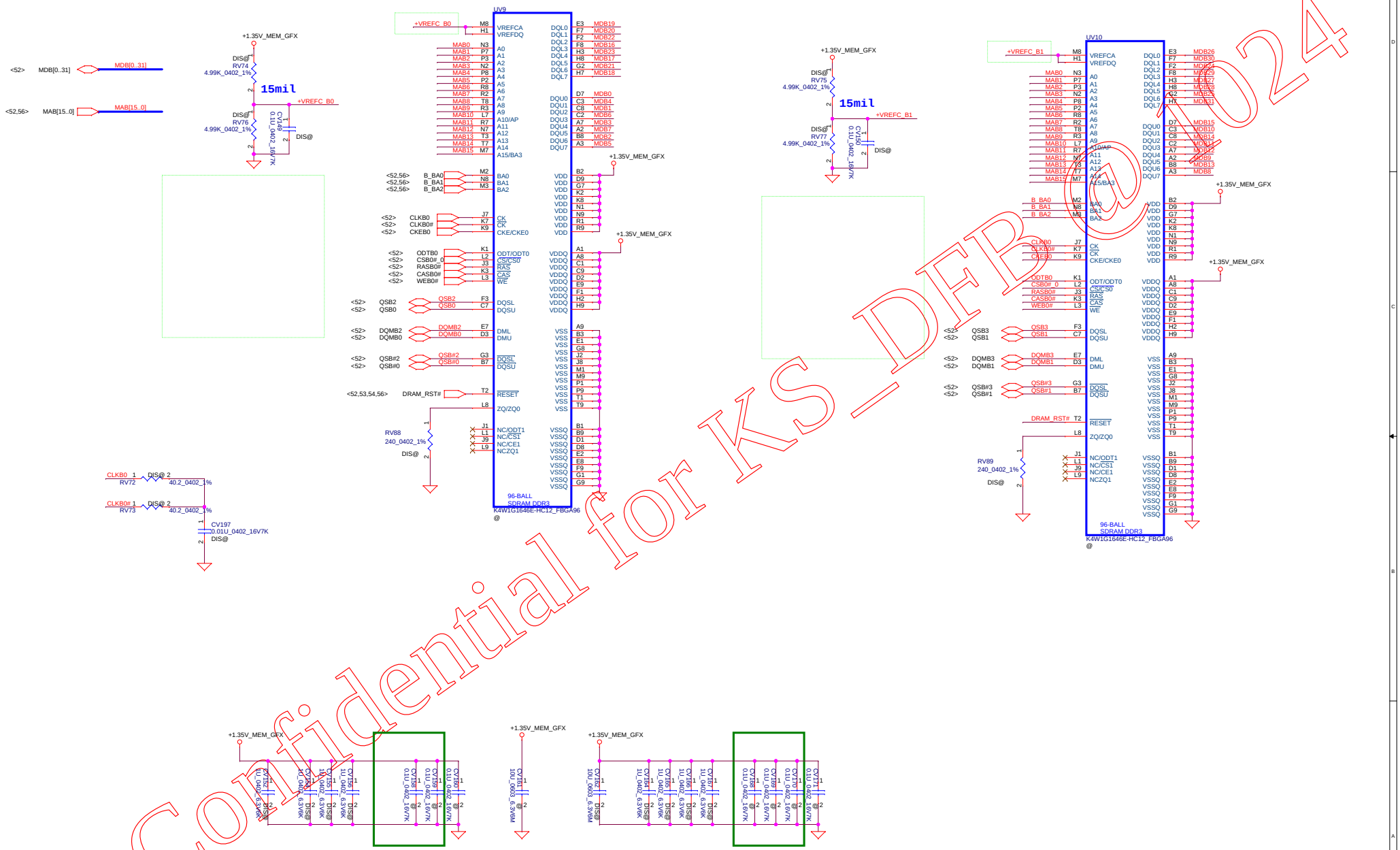
Compal Electronics, Inc.

Title: AMD_OPAL-XT_M2_VRAM_A1

Size: C | Document Number: LA-B015P | Rev: 0.1

Date: Wednesday, September 10, 2014 | Sheet 54 of 56



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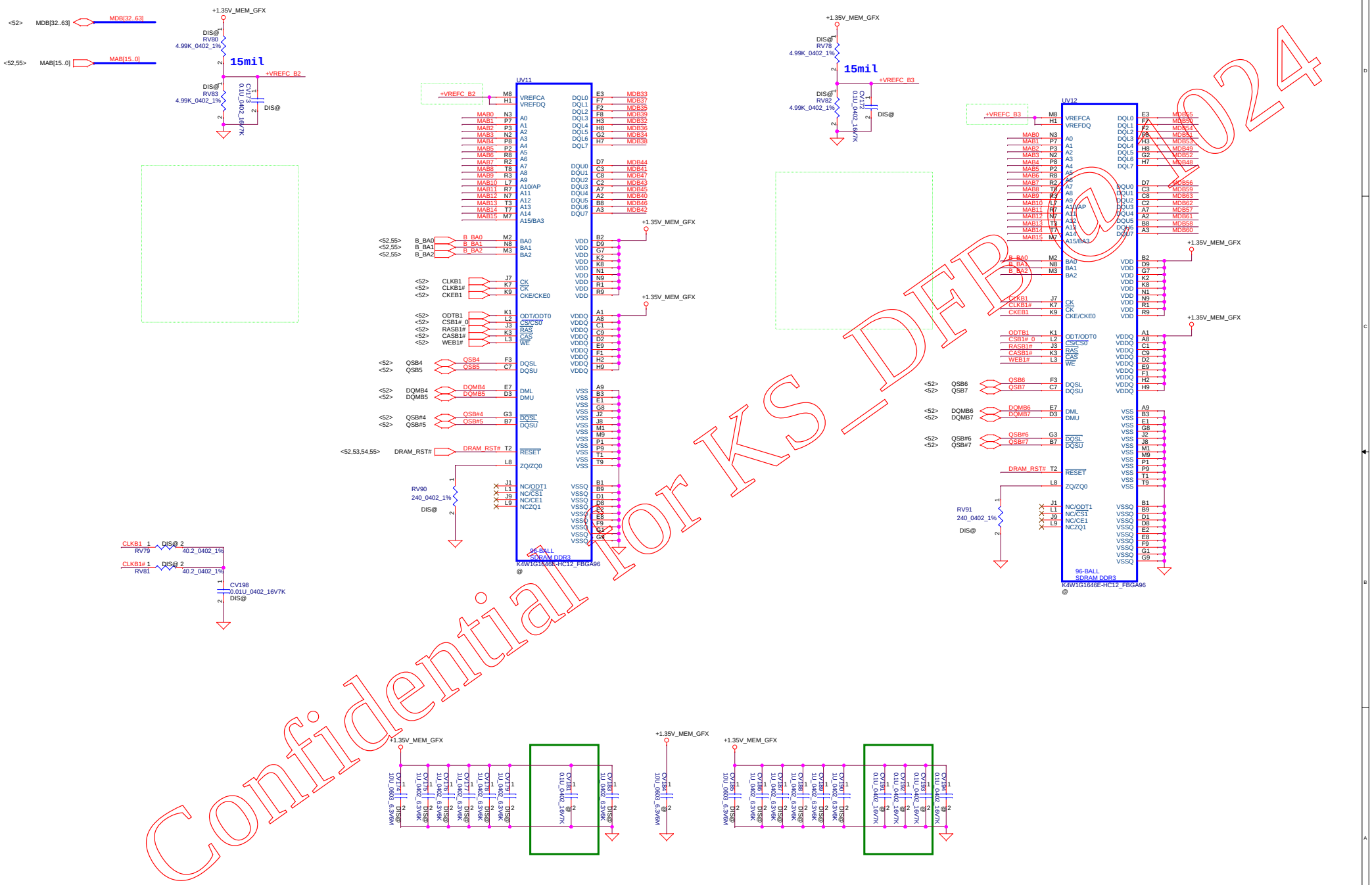
Title: AMD_OPAL-XT_M2_VRAM_B0

Size: C | Document Number: LA-B015P | Rev: 0.1

Date: Wednesday, September 10, 2014 | Sheet 55 of 56



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Compal Electronics, Inc.

Title: AMD_OPAL-XT_M2_VRAM_B1

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C	LA-B015P	0.1

Date: Wednesday, September 10, 2014 | Sheet 56 of 56