Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM+ICH9-M SFF core logic

SKYY

2008-07-29

機密 | 等級 | 硬體二部
產出人員
產出日期
解密日期

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Title: SCHEMATIC, M/B LA-4021P

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SKYY

Docking CONN.(Opus 1.0)
*RJ-45(LED*2)
*CRT
*LINE IN
*LINE OUT
*USB x4
*DC JACK
*Power on signal
*Docked indicator signal
*AC present indicator signal

Thermal Sensor
EMC2103
page 4

Fan Control
page 4

Mobile Penym
LV/ULV Dual Core
uFCPGA-956 CPU - SFF
page 4,5,6,7

CK505
Clock Generator
ICS9LPRS397
page 16

Accelerometer
LIS302DLTR
page 26

H_A#(3..35)
H_D#(0..63)
FSB
667/800/1066MHz 1.05V

LCD conn page 18
CRT page 17
CRT to docking page 34
S-Video to Docking page 34

Intel Cantiga GMS
FCBGA 1363 - SFF
page 8,9,10,11,12,13

DDR2 800MHz 1.8V
Dual Channel

DDR2-SO-DIMM X 2
BANK 0, 1, 2, 3 page 14,15

USB x1(Docking) page 34
FingerPrinter AES2810 USBx1 page 31
daughter board
USB conn x 3(For I/O)
BT Conn USB x 1 page 31
USB x1(Camara) page 18
MDC V1.5 page 30
Audio CKT AD1984HD page 28
TPA6043 AMP & Audio Jack page 29

DMI X4

Express Card 54
PCIE X1 + USB X1
page 25

WWAN Card
WWAN + PCIE X1 + USB X1
page 25

PCI-E BUS

Intel ICH9-M
WBMMAP-569 - SFF
page 20,21,22,23

USB2.0
Azalia
SATA0
SATA1

10/100/1000 LAN
Intel Boaz GbE PHY
page 24

24HST1041A-3
RJ45 CONN
page 25

CardBus Controller
Rico R5C833
page 27

PCI BUS

1394 port
SD/MMC Slot

SPI

SPI ROM
AT26DF321
page 32

2.5" SATA HDD Connector
OR
SATA ODD Connector
page 21

1.8" SATA HDD Connector
page 21

LPC BUS

LED
page 19

RTC CKT.
page 21

Power OK CKT.
page 35

Power On/Off CKT.
page 30

DC/DC Interface CKT.
page 36

TPM1.2
SLB9635TT
page 32

SMSC KBC 1091
page 33

Touch Pad CONN.
page 30

TrackPoint CONN.
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Int.KBD
page 30

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Voltage Rails (O MEANS ON X MEANS OFF)

power plane / State	+B	+5VALW +3VALW +3VM +1.05VM	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +0.9V
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
CONN@ : means ME part.
45@ : means install after SMT.

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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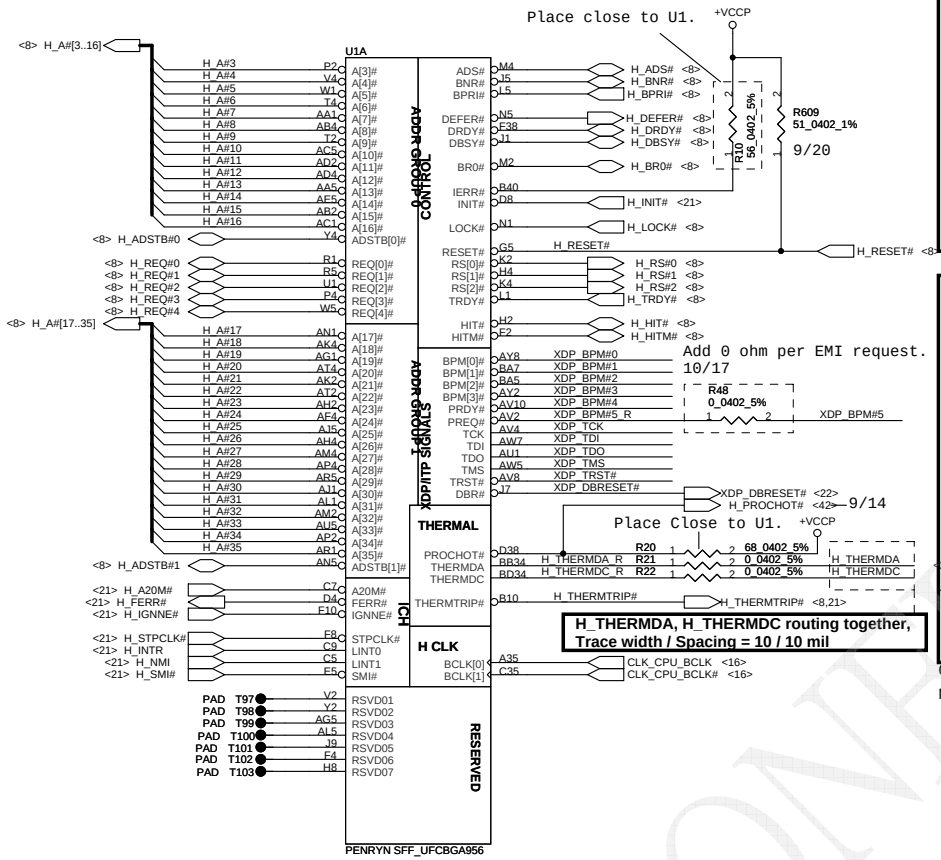
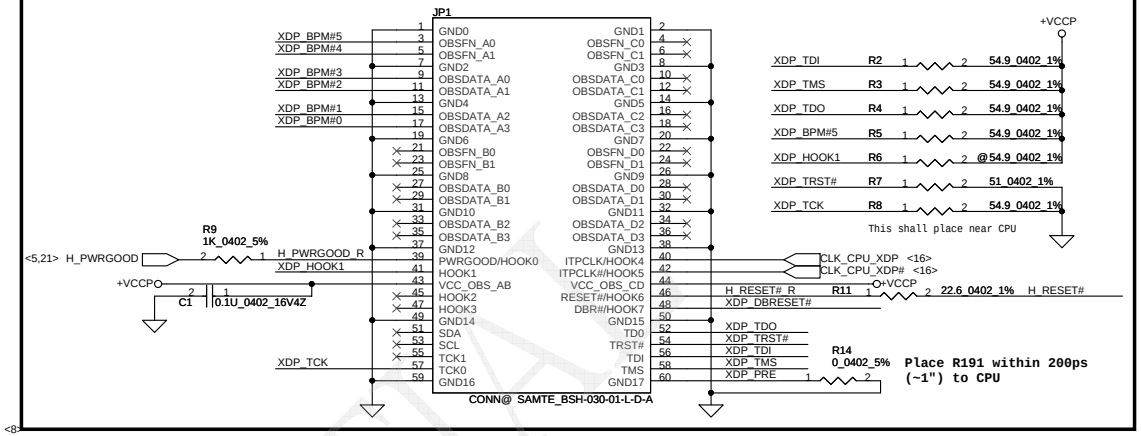
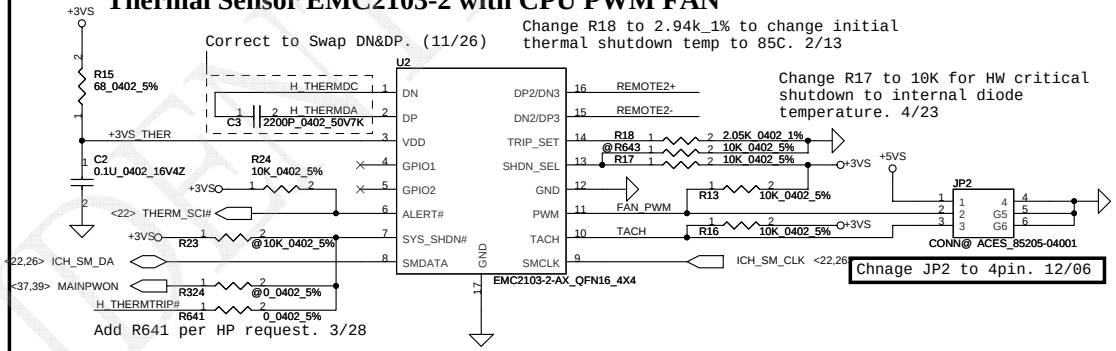


XDP Connector



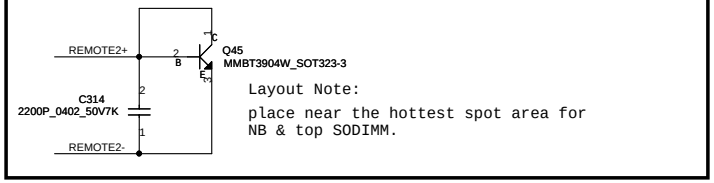
Thermal Sensor EMC2103-2 with CPU PWM FAN



Change R23, R24 connect to +3VS and add PU/PD for U2. (9/3)

NI R23, reserve R324 and connect to MAINPWON. (10/5)

REMOTE thermal sensor



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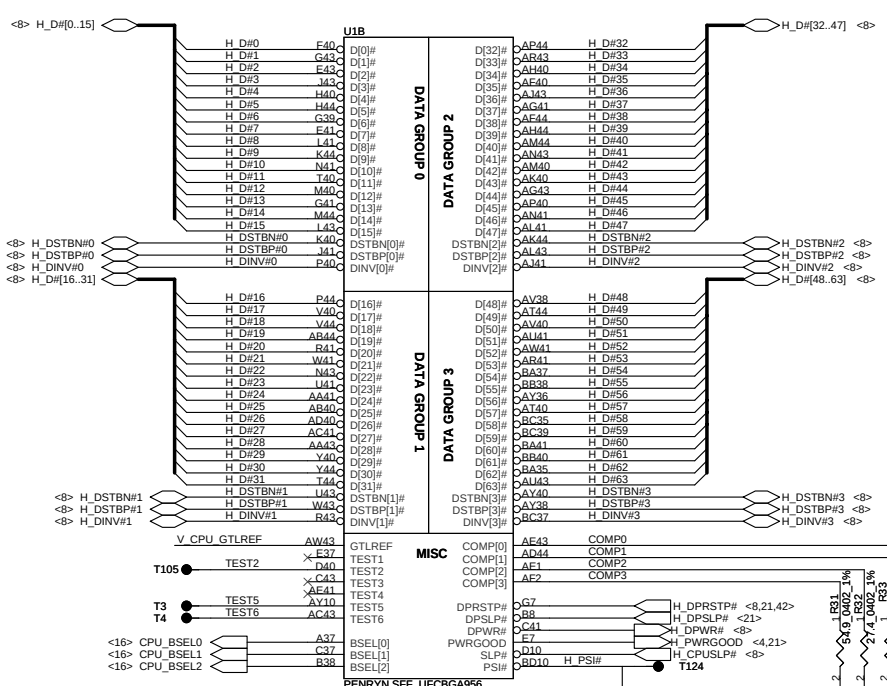
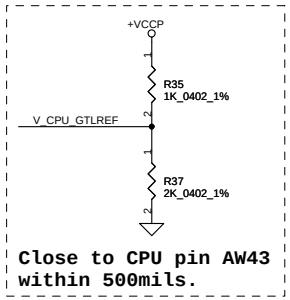
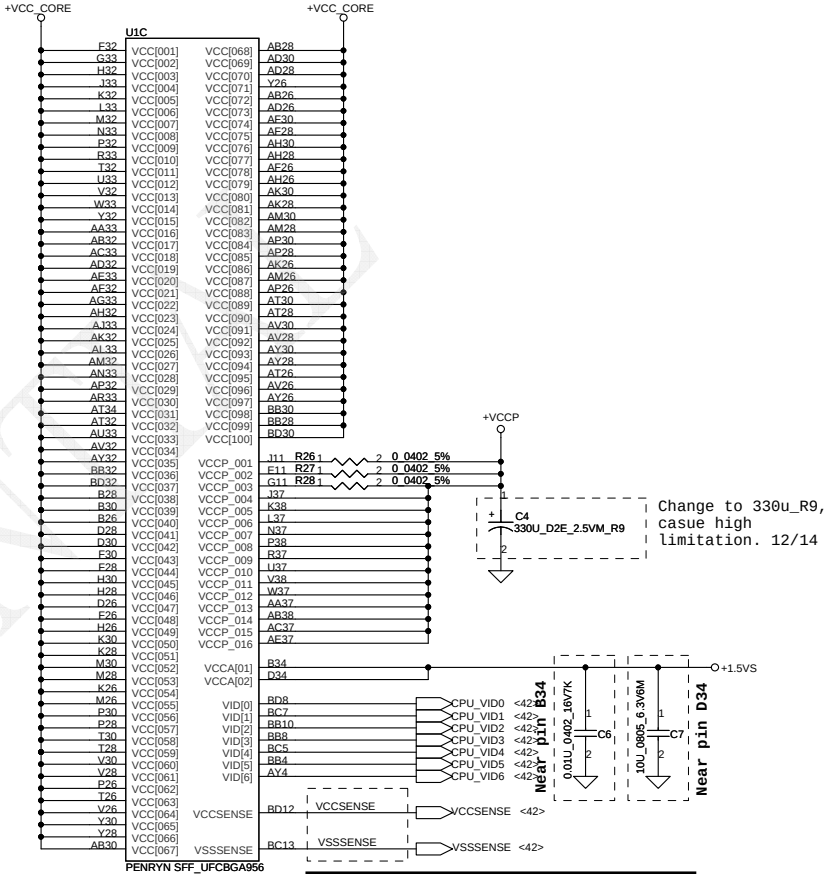


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

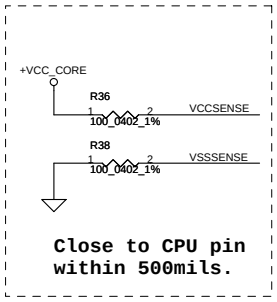
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.





Length match within 25 mils. The trace width/space/other is 20/7/25.



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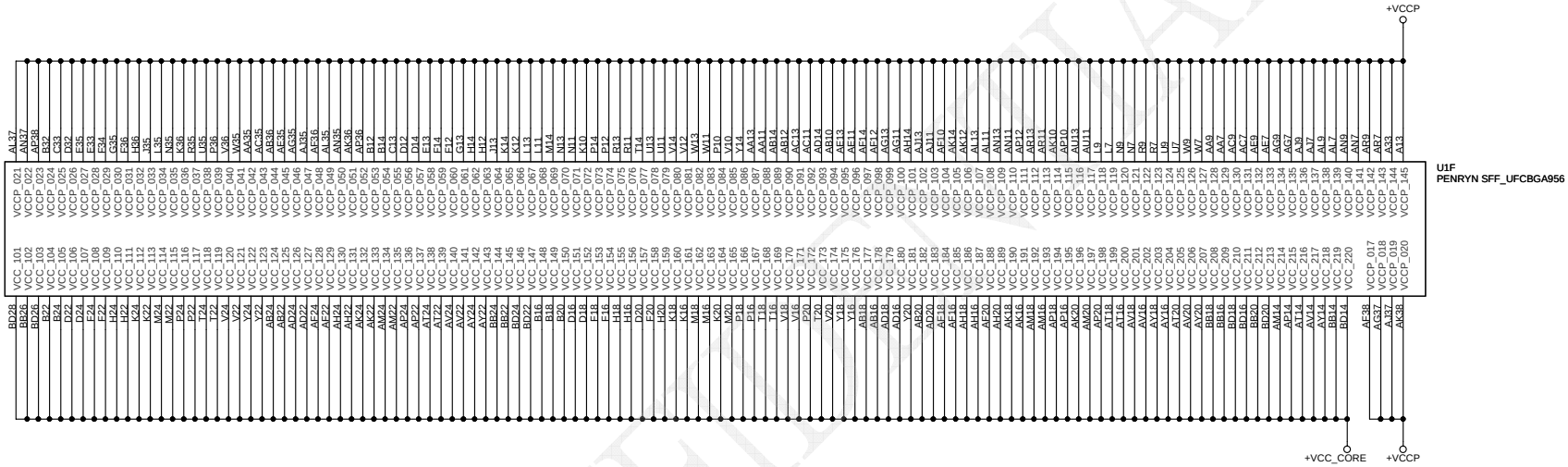

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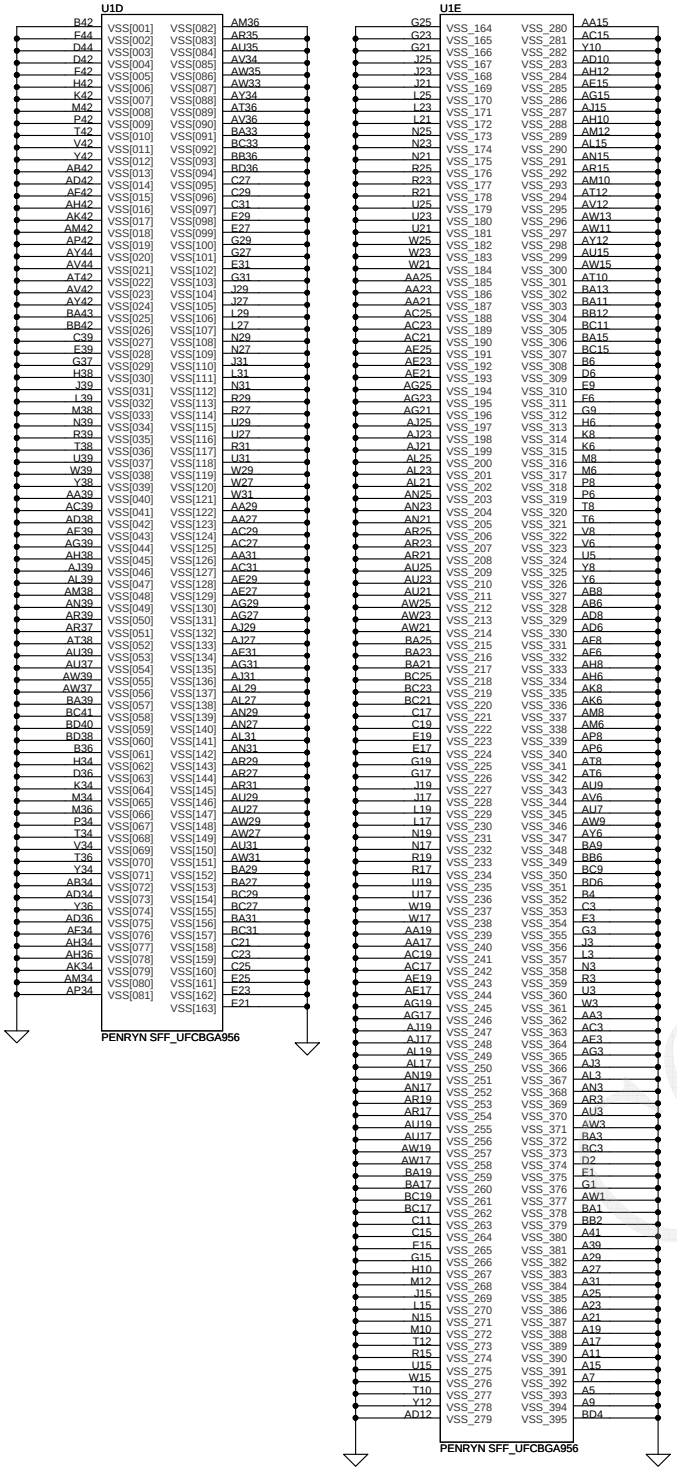
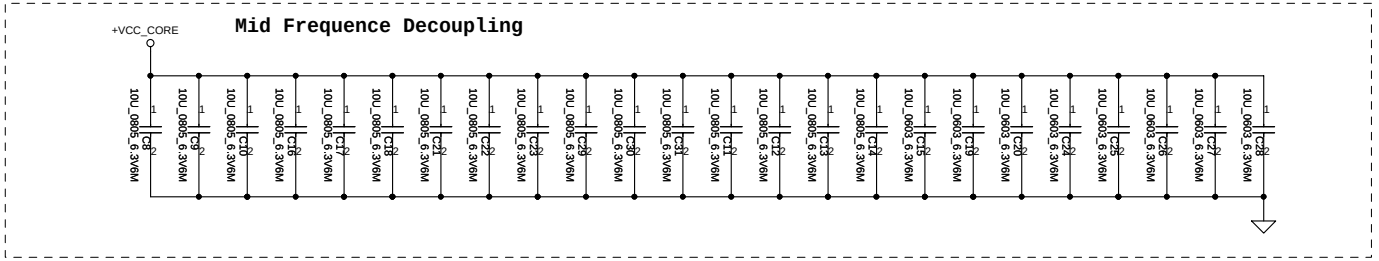
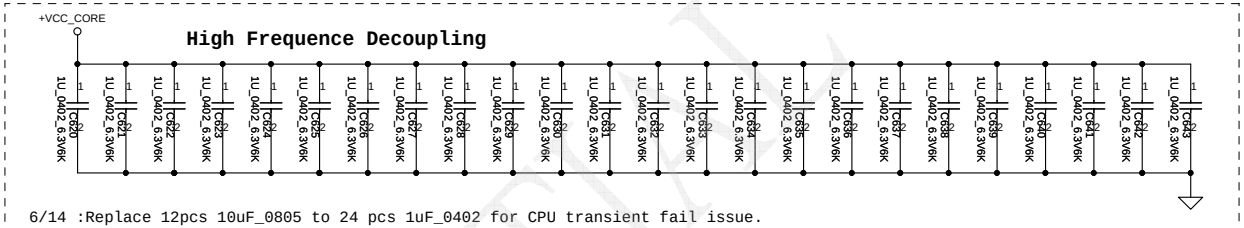
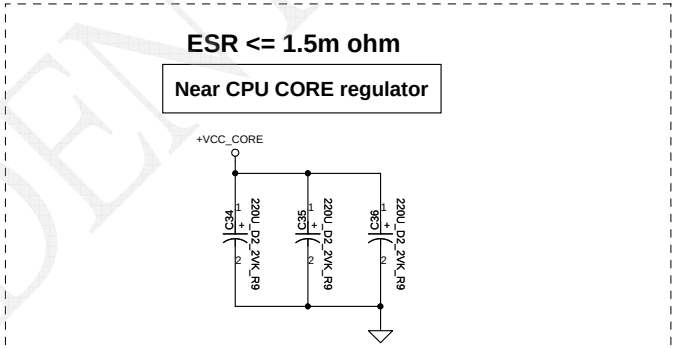


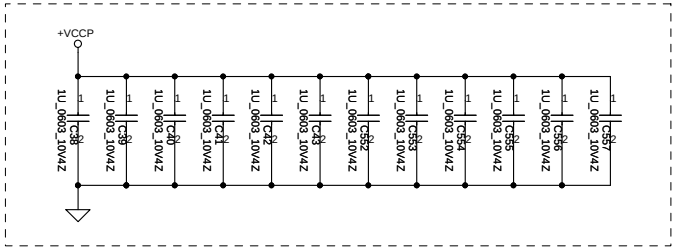




6/14 :Replace 12pcs 10uF_0805 to 24 pcs 1uF_0402 for CPU transient fail issue.



Del C37 to improve power plan. 6/14



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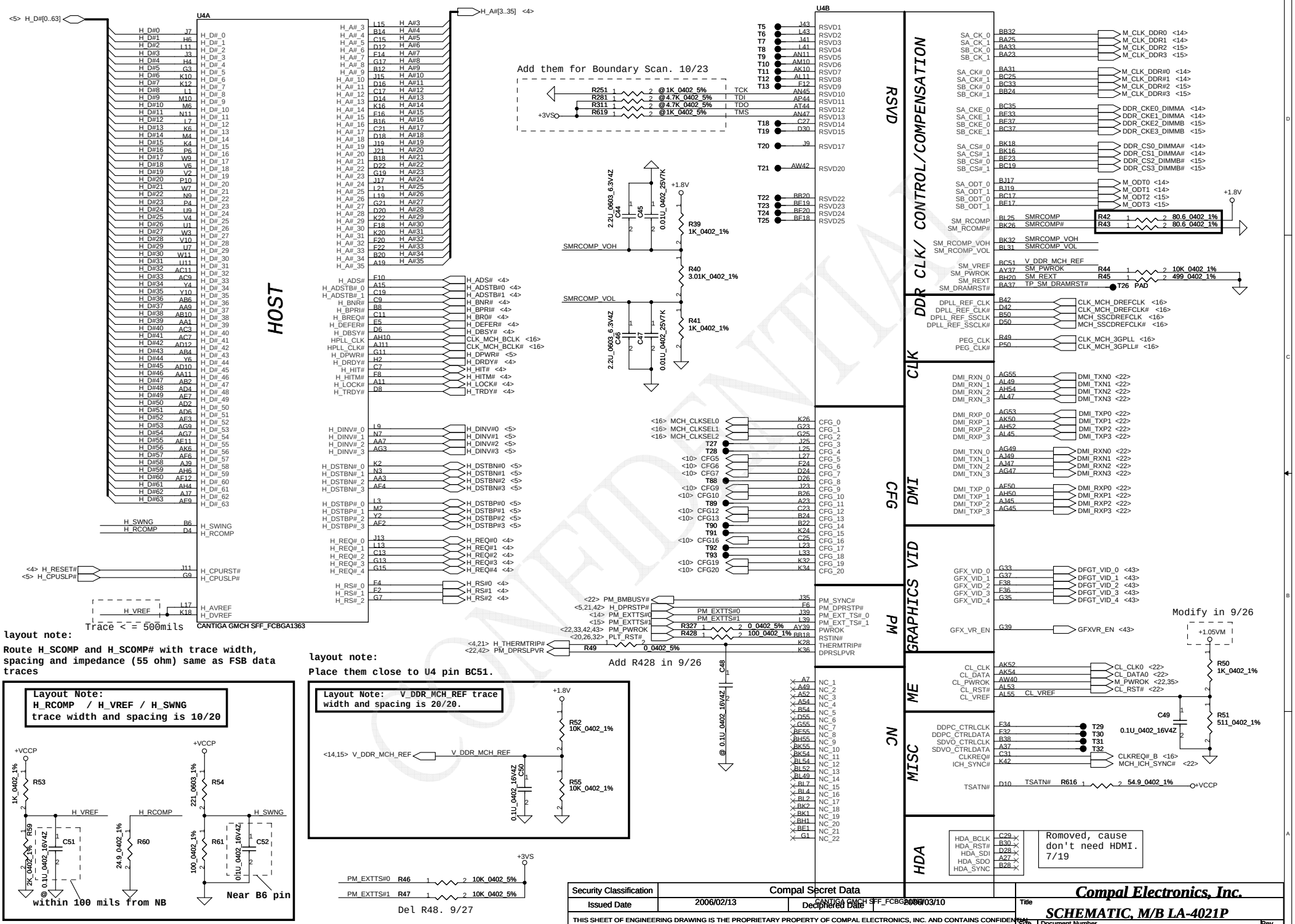

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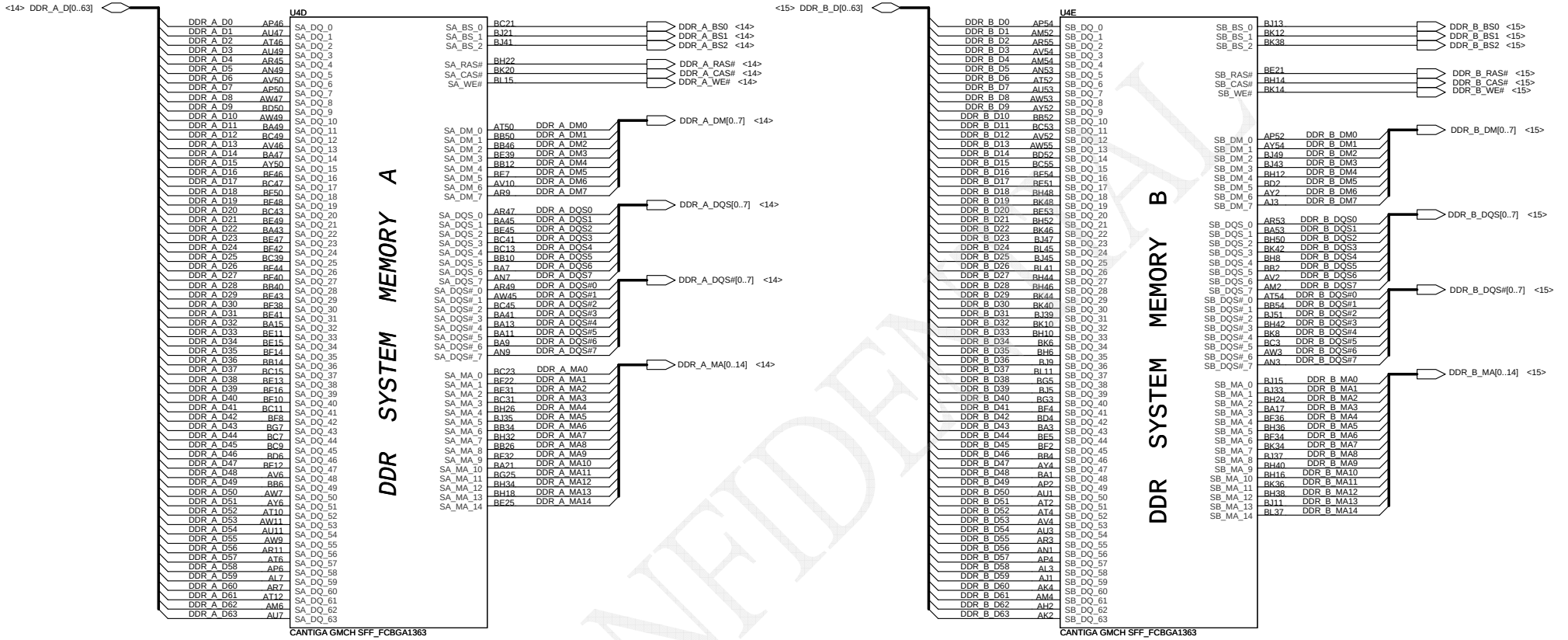

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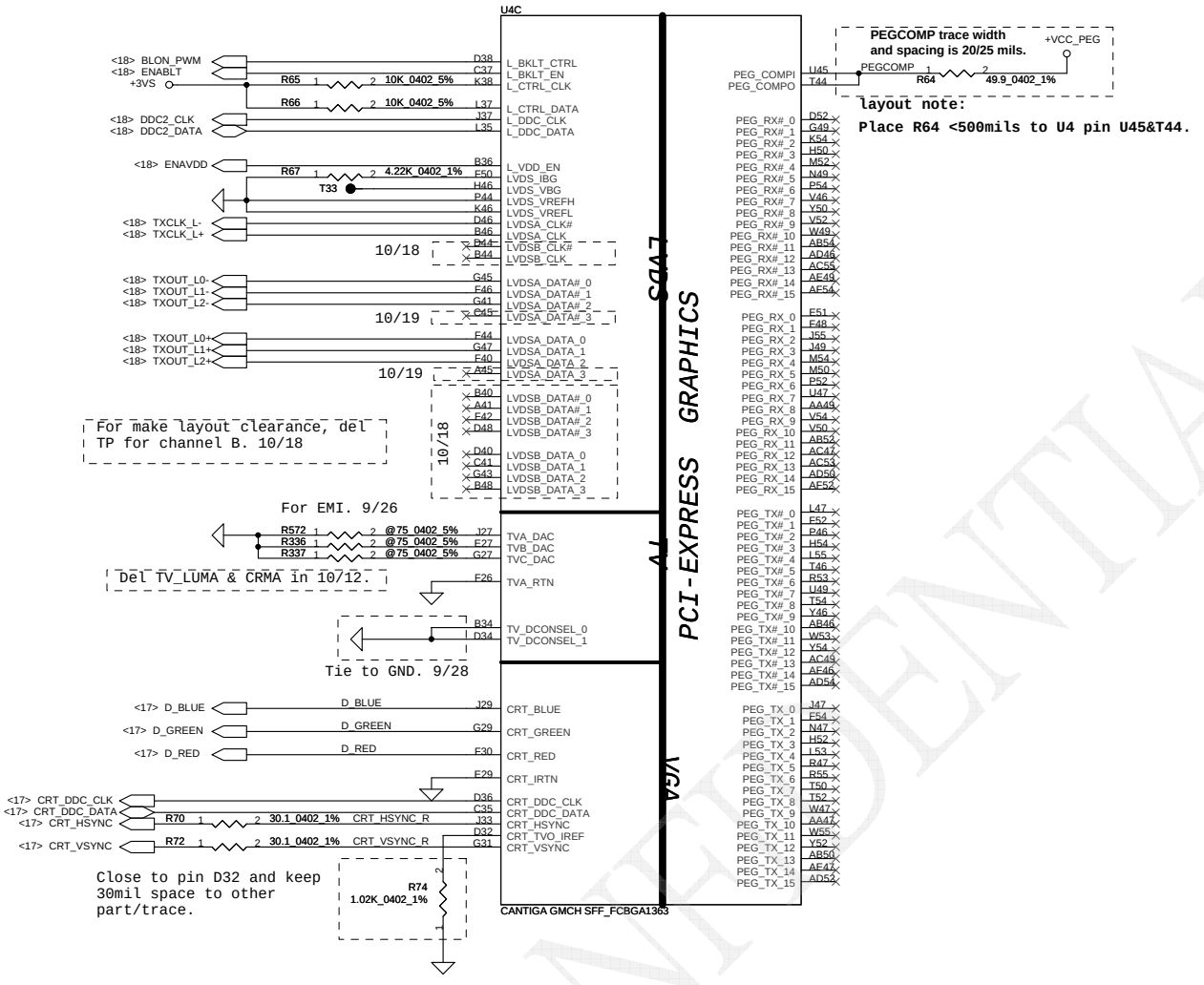
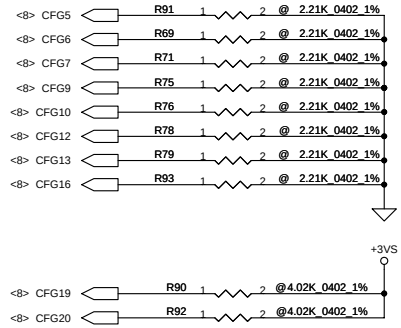


Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.



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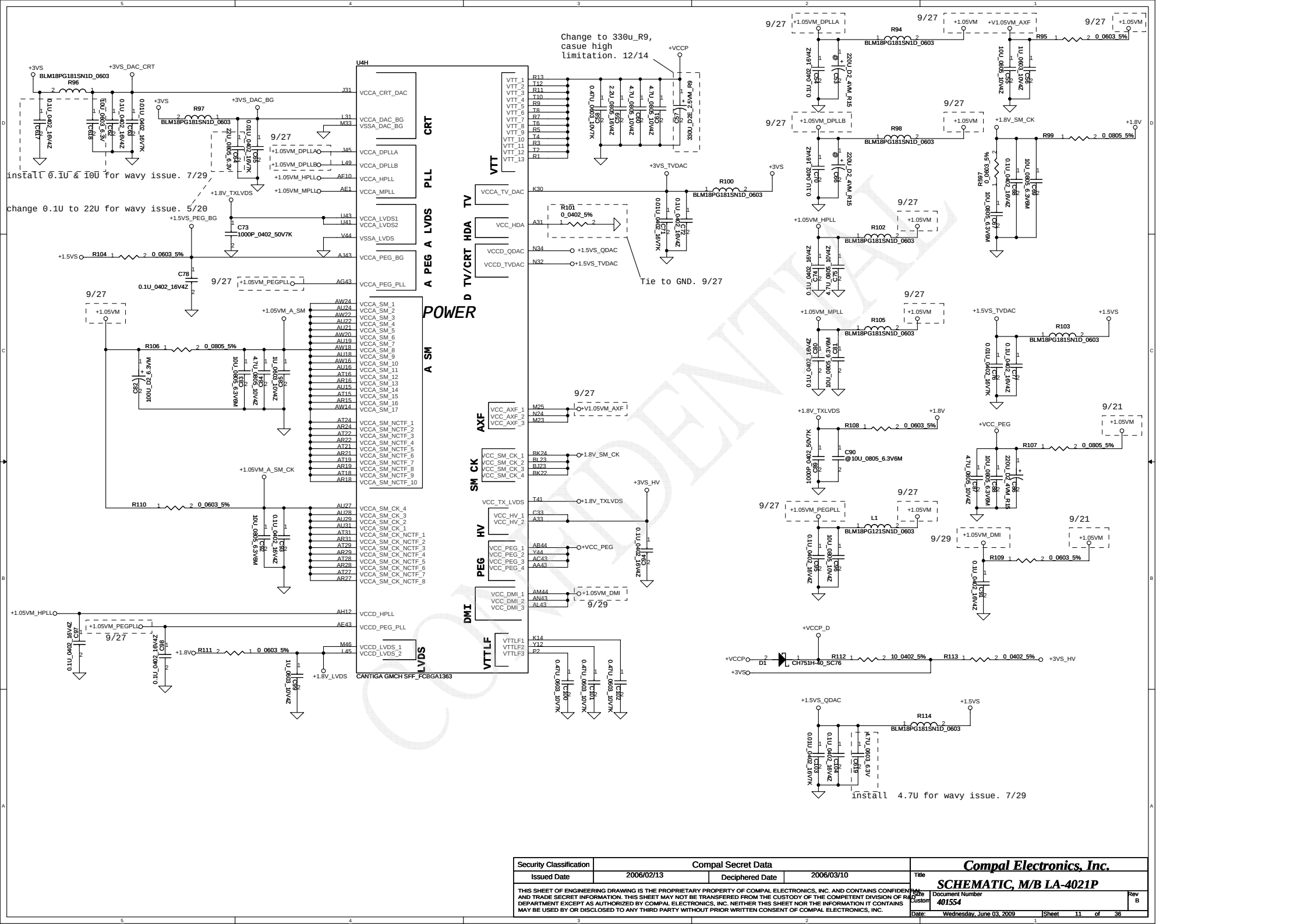

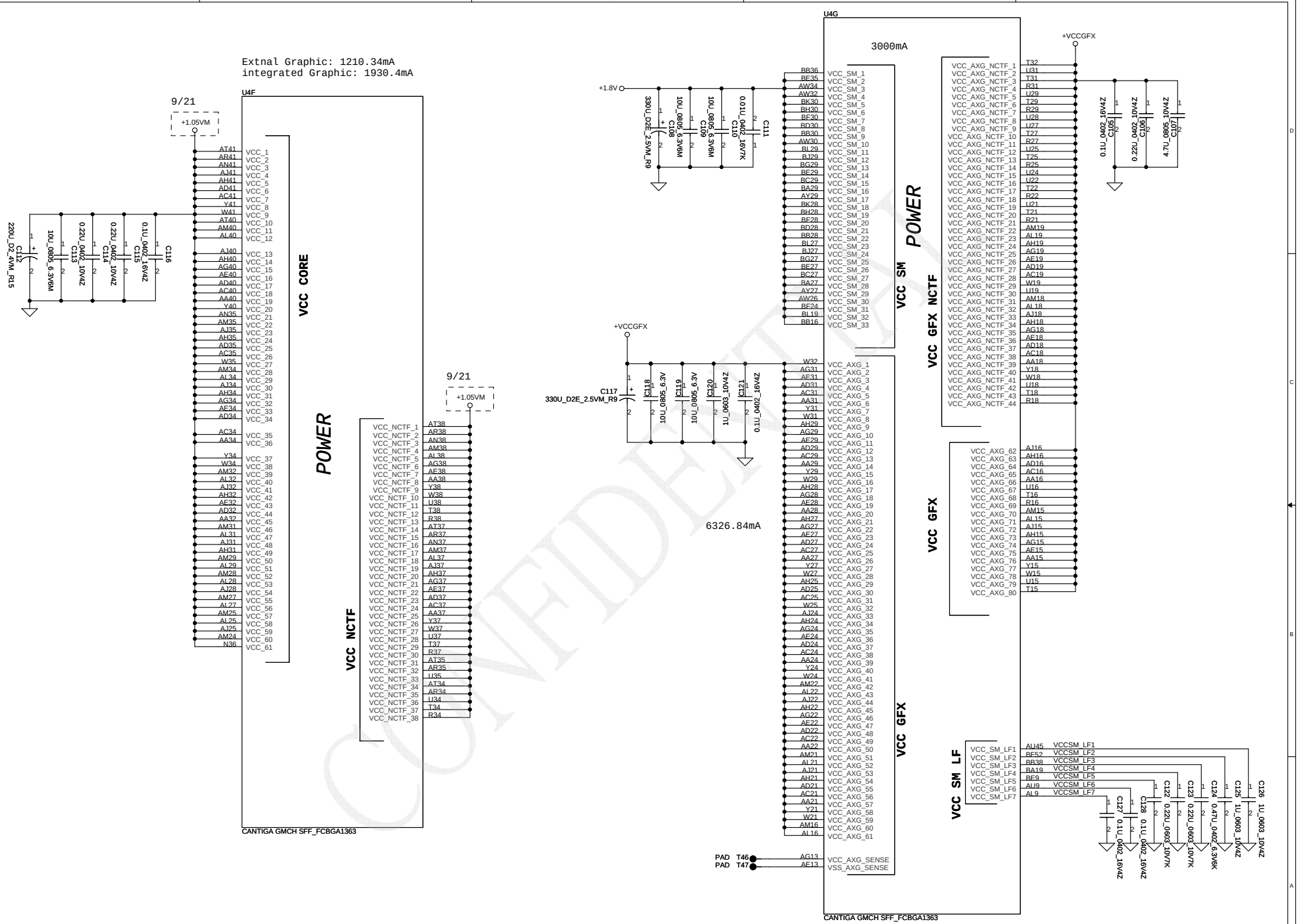

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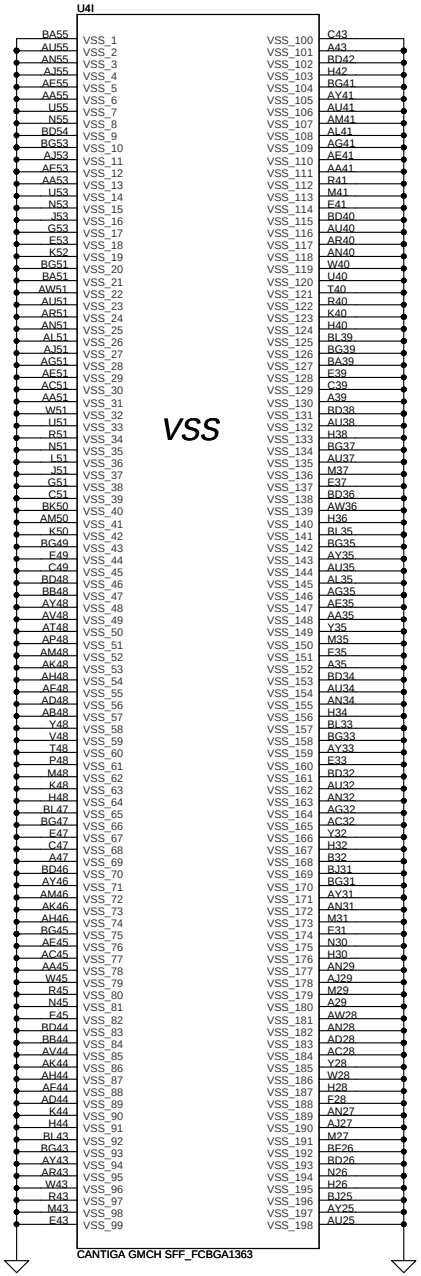

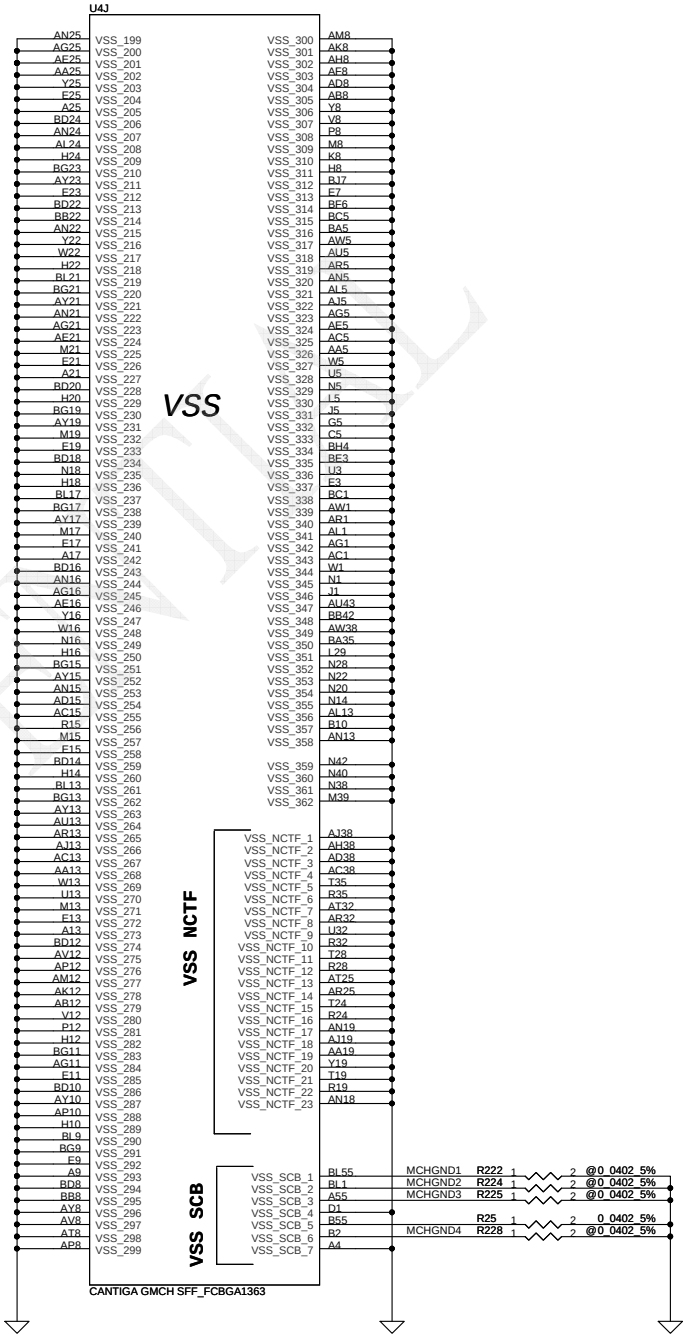

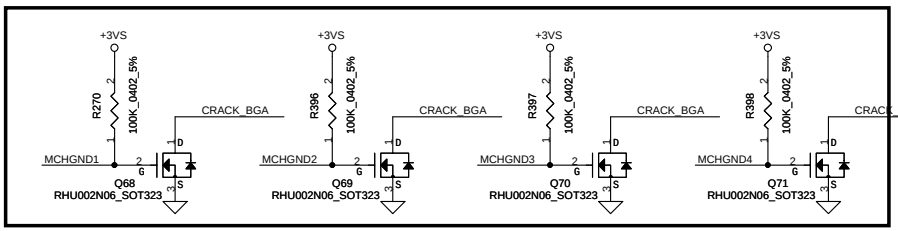

CRACK_BGA <23,33>

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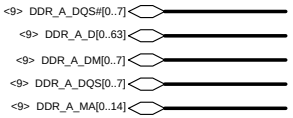
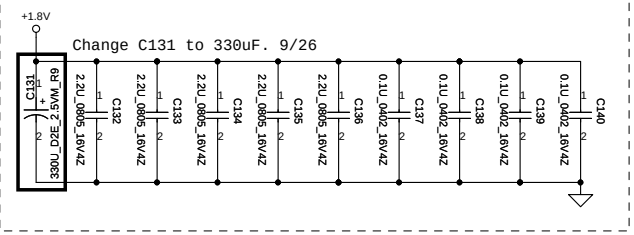
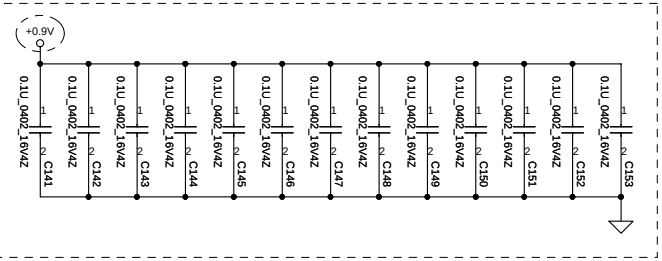
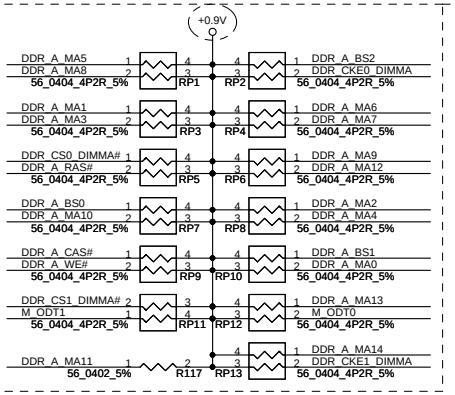


Layout Note:
Place near JP36

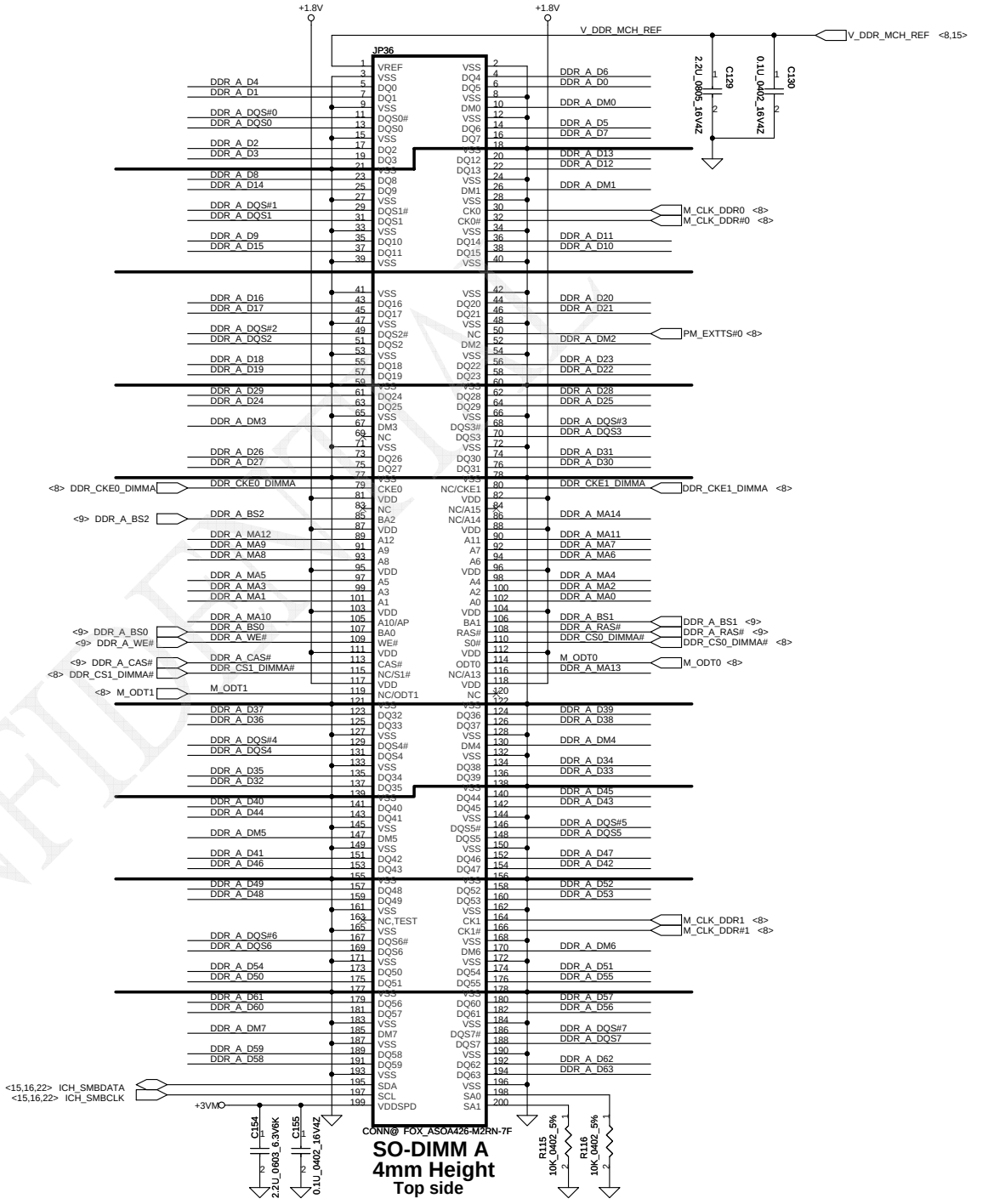


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V





Layout Note:
Place these resistor closely JP9,all trace length Max=1.5"



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<9> DDR_B_DQS#[0..7]
<9> DDR_B_D[0..63]
<9> DDR_B_DM[0..7]
<9> DDR_B_DQS[0..7]
<9> DDR_B_MA[0..14]

Layout Note:
Place near JP34

+1.8V

Reserve C524. 9/26

C524 @ 330U_D2E_2.5VM_R9 (+)

2.2U_0805_16V4Z: C566, C567, C568, C569, C570

0.1U_0402_16V4Z: C571, C572, C573, C574

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

+0.9V

0.1U_0402_16V4Z: C575, C576, C577, C578, C579, C580, C581, C582, C583, C584, C585, C586, C587

Layout Note:
Place these resistor closely JP10,all trace length Max=1.5"

+0.9V

DDR_B_MA1 / DDR_B_MA3	RP22	RP23	DDR_B_MA9 / DDR_B_MA12
DDR_B_BS0 / DDR_B_MA10	RP24	RP25	DDR_CKE3_DIMMB / DDR_B_MA14
DDR_B_MA0 / DDR_B_BS1	RP26	RP27	DDR_B_MA5 / DDR_B_MA8
DDR_B_RAS# / DDR_CS2_DIMMB#	RP28	RP29	DDR_B_MA7 / DDR_B_MA6
DDR_B_CAS# / DDR_B_WE#	RP30	RP31	DDR_B_MA4 / DDR_B_MA2
DDR_CS3_DIMMB# / M_ODT3	RP32	RP33	M_ODT2 / DDR_B_MA13
DDR_B_MA11 / R80		RP34	DDR_B_BS2 / DDR_CKE2_DIMMB

56_0404_4P2R_5%, 56_0402_5%

+1.8V +1.8V

V_DDR_MCH_REF — V_DDR_MCH_REF <8,14>

C564 2.2U_0805_16V4Z, C565 0.1U_0402_16V4Z

JP3

DDR_B_D57 / DDR_B_D56	DQ0 / DQ1	DQ4 / DQ5	DDR_B_D60 / DDR_B_D61
DDR_B_DQS#7 / DDR_B_DQS7	DQS0# / DQS0	DM0 / DQ6 / DQ7	DDR_B_DM7 / DDR_B_D62 / DDR_B_D59
DDR_B_D58 / DDR_B_D63	DQ2 / DQ3	DQ12 / DQ13	DDR_B_D52 / DDR_B_D53
DDR_B_D48 / DDR_B_D49	DQ8 / DQ9	DM1	DDR_B_DM6
DDR_B_DQS#6 / DDR_B_DQS6	DQS1# / DQS1	CK0 / CK0#	M_CLK_DDR3 <8> / M_CLK_DDR#3 <8>
DDR_B_D51 / DDR_B_D50	DQ10 / DQ11	DQ14 / DQ15	DDR_B_D54 / DDR_B_D55
DDR_B_D40 / DDR_B_D44	DQ16 / DQ17	DQ20 / DQ21	DDR_B_D45 / DDR_B_D41
DDR_B_DQS#5 / DDR_B_DQS5	DQS2# / DQS2	NC / DM2	PM_EXTTS#1 <8> / DDR_B_DM5
DDR_B_D42 / DDR_B_D47	DQ18 / DQ19	DQ22 / DQ23	DDR_B_D46 / DDR_B_D43
DDR_B_D37 / DDR_B_D32	DQ24 / DQ25	DQ28 / DQ29	DDR_B_D36 / DDR_B_D33
DDR_B_DM4	DM3	DQS3# / DQS3	DDR_B_DQS#4 / DDR_B_DQS4
DDR_B_D39 / DDR_B_D35	DQ26 / DQ27	DQ30 / DQ31	DDR_B_D34 / DDR_B_D38
<8> DDR_CKE2_DIMMB	CKE0	NC/CKE1	DDR_CKE3_DIMMB / DDR_CKE3_DIMMB <8>
<9> DDR_B_BS2	BA2	NC/A14	DDR_B_MA14
DDR_B_MA12 / DDR_B_MA9 / DDR_B_MA8	A12 / A9 / A8	A11 / A7 / A6	DDR_B_MA11 / DDR_B_MA7 / DDR_B_MA6
DDR_B_MA5 / DDR_B_MA3 / DDR_B_MA1	A5 / A3 / A1	A4 / A2 / A0	DDR_B_MA4 / DDR_B_MA2 / DDR_B_MA0
DDR_B_MA10 / DDR_B_BS0 / DDR_B_WE#	A10/AP / BA0 / WE#	BA1 / RAS# / S0#	DDR_B_BS1 <9> / DDR_B_RAS# <9> / DDR_CS2_DIMMB# <8>
<9> DDR_B_CAS# / <8> DDR_CS3_DIMMB#	CAS# / NC/S1#	ODT0 / NC/A13	M_ODT2 / M_ODT2 <8> / DDR_B_MA13
<8> M_ODT3	NC/ODT1	NC	
DDR_B_D30 / DDR_B_D27	DQ32 / DQ33	DQ36 / DQ37	DDR_B_D26 / DDR_B_D31
DDR_B_DQS#3 / DDR_B_DQS3	DQS4 / DQS4#	DM4	DDR_B_DM3
DDR_B_D25 / DDR_B_D28	DQ34 / DQ35	DQ38 / DQ39	DDR_B_D24 / DDR_B_D29
DDR_B_D23 / DDR_B_D22	DQ40 / DQ41	DQ44 / DQ45	DDR_B_D18 / DDR_B_D19
DDR_B_DM2	DM5	DQS5# / DQS5	DDR_B_DQS#2 / DDR_B_DQS2
DDR_B_D17 / DDR_B_D16	DQ42 / DQ43	DQ46 / DQ47	DDR_B_D21 / DDR_B_D20
DDR_B_D11 / DDR_B_D10	DQ48 / DQ49	DQ52 / DQ53	DDR_B_D14 / DDR_B_D15
DDR_B_DQS#1 / DDR_B_DQS1	NC,TEST / DQS6# / DQS6	CK1 / CK1# / DM6	M_CLK_DDR2 <8> / M_CLK_DDR#2 <8> / DDR_B_DM1
DDR_B_D12 / DDR_B_D9	DQ50 / DQ51	DQ54 / DQ55	DDR_B_D13 / DDR_B_D8
DDR_B_D2 / DDR_B_D3	DQ56 / DQ57	DQ60 / DQ61	DDR_B_D7 / DDR_B_D6
DDR_B_DM0	DM7	DQS7# / DQS7	DDR_B_DQS#0 / DDR_B_DQS0
DDR_B_D0 / DDR_B_D5	DQ58 / DQ59	DQ62 / DQ63	DDR_B_D1 / DDR_B_D4
<14,16,22> ICH_SMBDATA / <14,16,22> ICH_SMBCLK	SDA / SCL	SAO	
+3VMO	VDDSPD	SA1	R73 1 2 +3VM 10K_0402_5%

CONN@ SUYIN_600008FB200G103ZL

C588 2.2U_0603_6.3V6K, C589 0.1U_0402_16V4Z

R77 10K_0402_5%

SO-DIMM B
REVERSE
Bottom side

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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	FSB MHz	SRC MHz	PCI MHz
0	0	0	266	1066	100	33.3
0	1	0	200	800	100	33.3
0	1	1	166	667	100	33.3

Mount C157 & C166 tp solve WWAN noise issue. 1/23

Place close to U5

Add for PCIE port80 debug port. 10/18.

Install. 11/06

9/14

9/20

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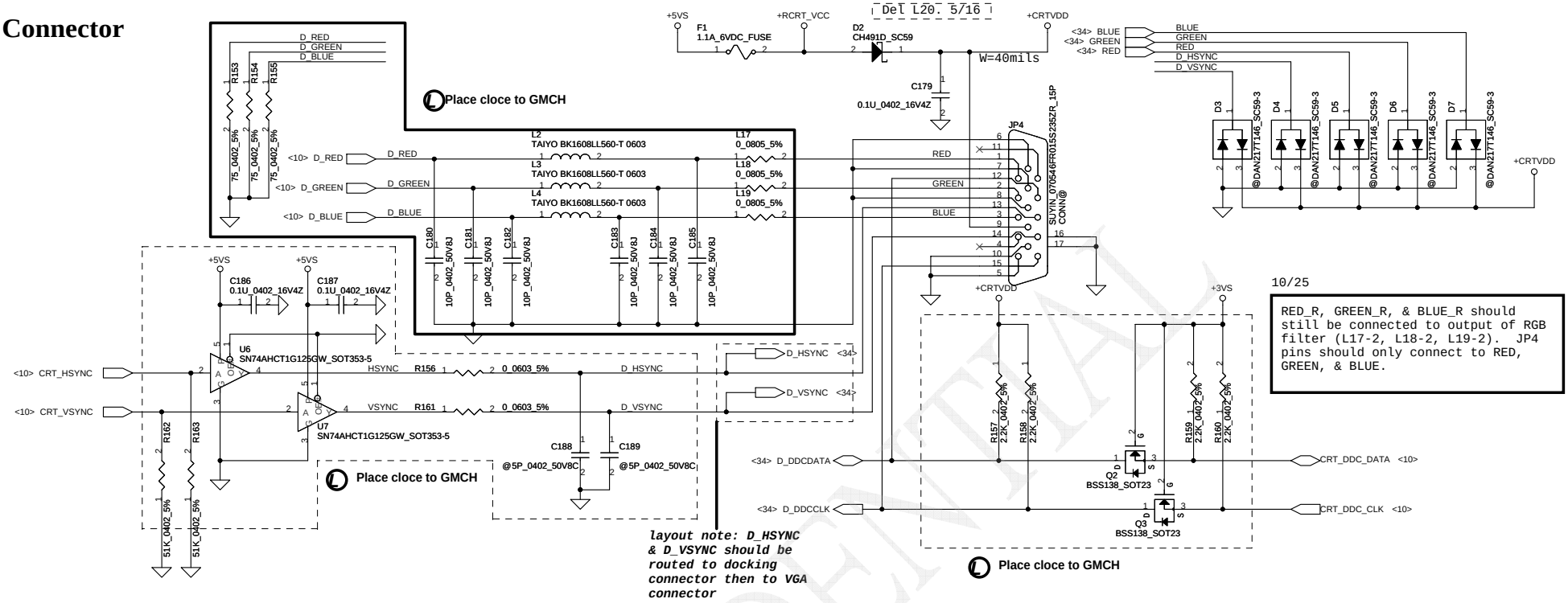
CRT Connector



layout note: D_HSYNC & D_VSYNC should be routed to docking connector then to VGA connector

10/25

RED_R, GREEN_R, & BLUE_R should still be connected to output of RGB filter (L17-2, L18-2, L19-2). JP4 pins should only connect to RED, GREEN, & BLUE.

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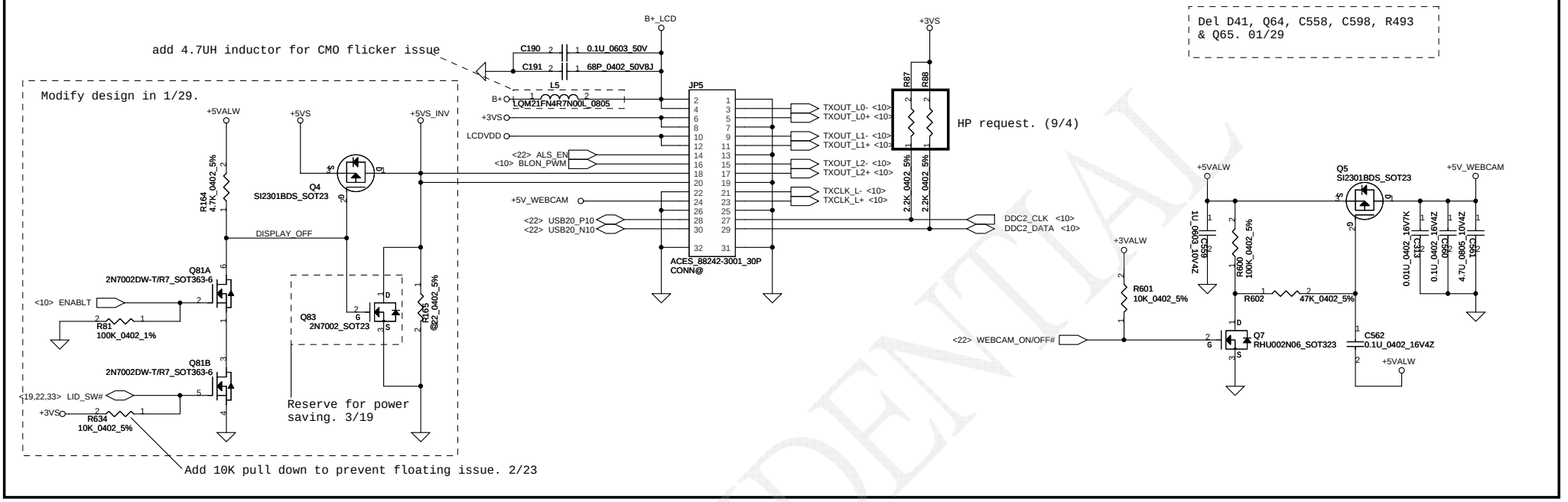
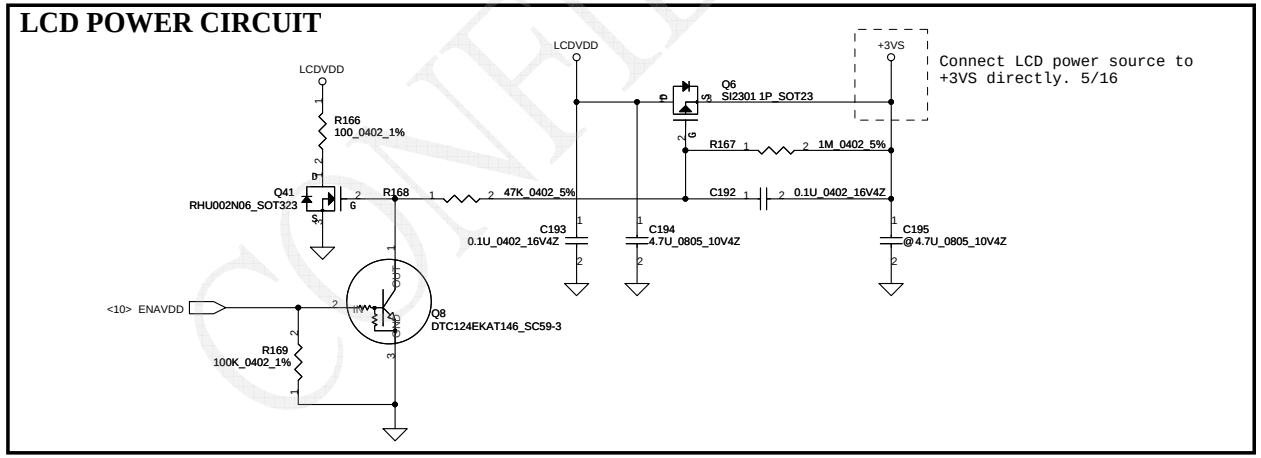
LCD/PANEL BD. CONN.



LCD POWER CIRCUIT



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Issued Date	2005/03/10	Deciphered Date	2006/03/10

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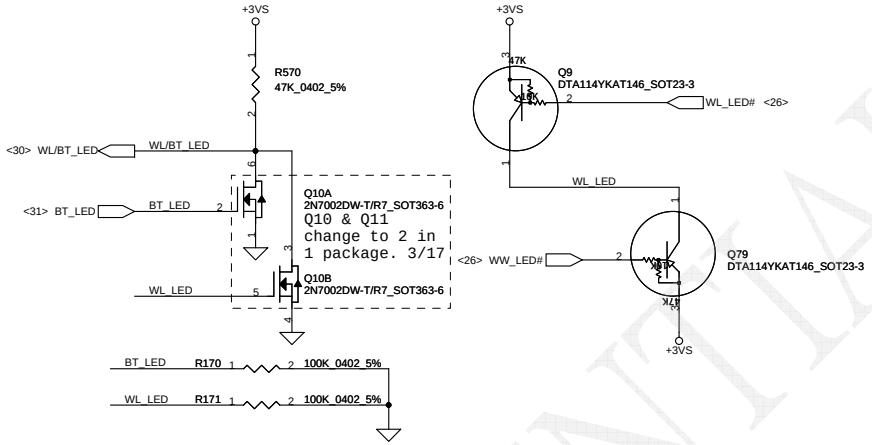
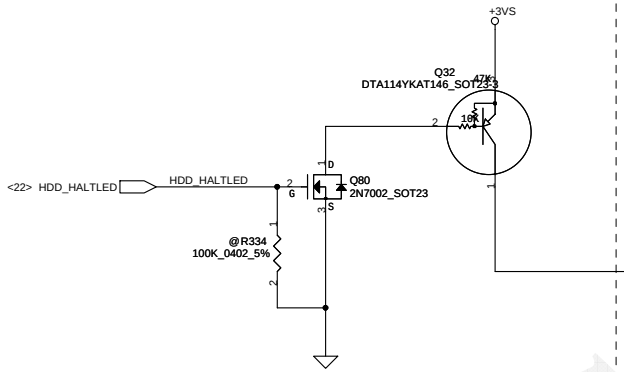
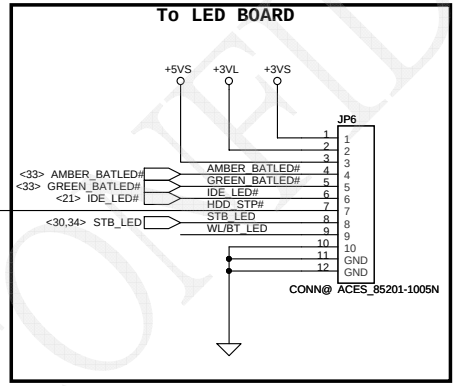
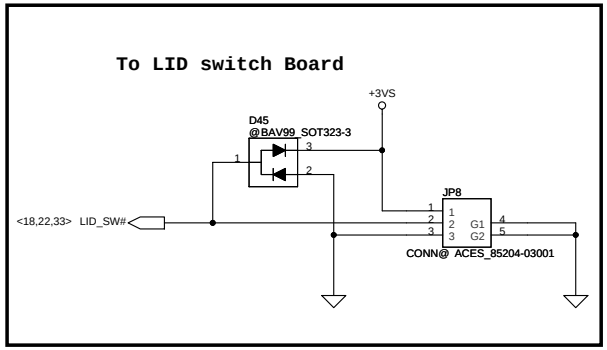
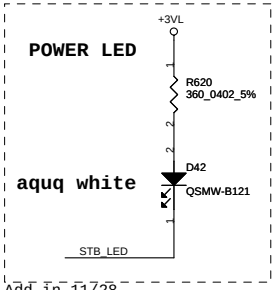


Cause space issue, move them from LED board to M/B. 10/09









Add in 11/28.
Place them close to SW1.

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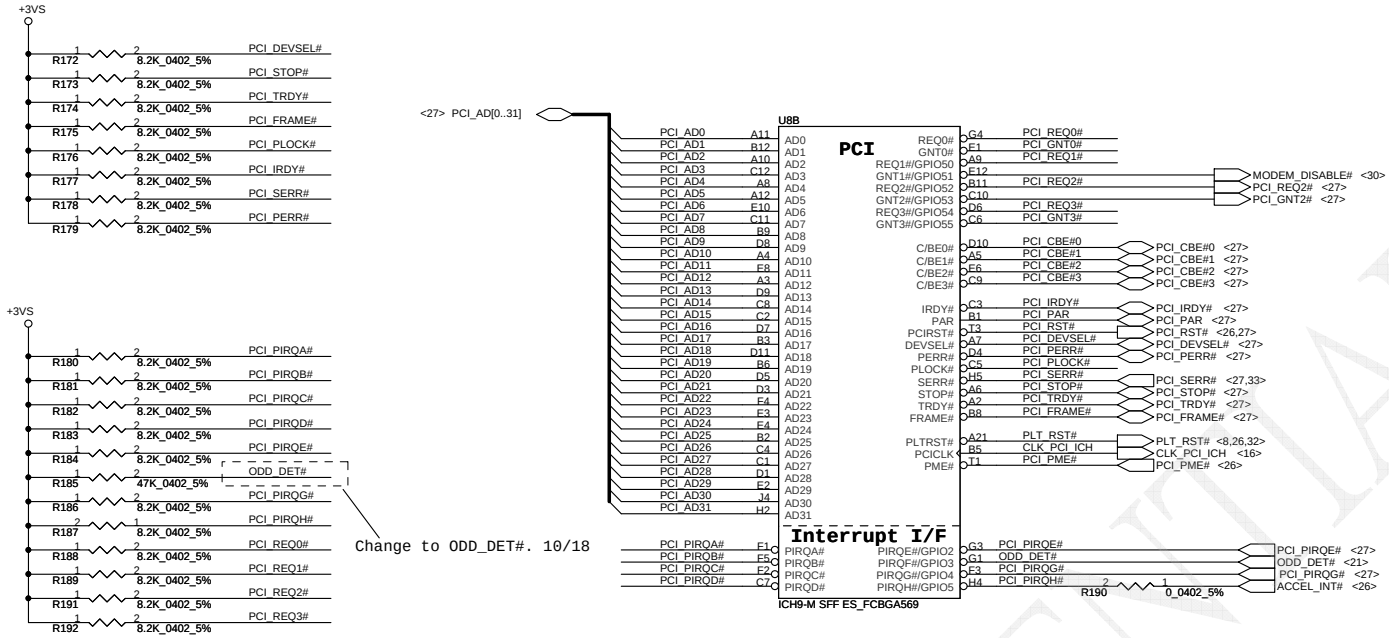
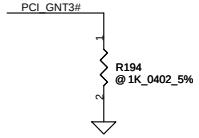
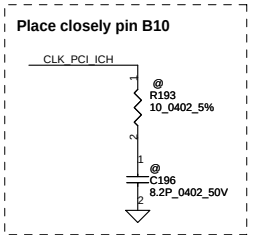
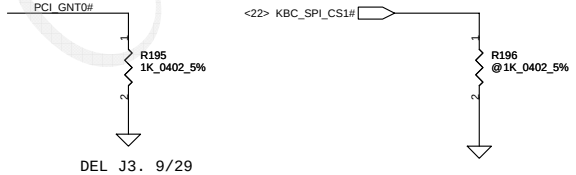


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC





DEL J3. 9/29

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ICH_RSVD	HDA_SDOUT_CODEC	Description
0	0	RV
0	1	XOR
1	0	Normal(D)
1	1	PCIE Bit1

XOR CHAIN ENTRANCE STRAP:RSVD

Change from 180K to 20K & 0.1u to 1u. 9/29

Add C599 ~ C602 to solve WWAN noise issue. 1/23

Remove R227 & C199

Swap in 9/28

9/27 Del PU R203~R204 for H_DPRSTP# & H_DPSLP#.

9/27

Place Close to U8.

placed within 2" from ICH9M

Within 500 mils

7/3 change 24.9 ohm to 18 ohm for signal integrity.

ICH9-M SFF ES_FCBGA569

SATA CD-ROM Connector

JP9
CONN@ OCTEK_SAT-22DE1G_NRSUYIN_127059FR022S305ZL

1.8" SATA HDD CONN

JP10
CONN@ ACES_85201-08051

Place component's closely SATA CONN.(JP9)

Place component's closely SATA CONN.(JP10)

PCB-MB

JBATT1
CONN@ SUYIN_060003FA002G202NL

D8
DAN202UT106_SC70-3

W=20mils

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Add R326 10K. 10/04

Add R621 in 12/03.

Add R321 in 10/03.

for Intel LAN_PHYPC glitch issue 5/7

Add EXP_RST# in 10/09.

Change R251 to CH751. 10/04

Change in 7/13

Reserve in 10/08.

Change design in 10/08.

Add R626, R627 for iTPM test. 12/11

Reserve for DB1 test. 10/05

Change HDD_HALTLED from GPIO18 to GPIO19. 11/26

Add for find tune timing.(If have glich issue)

Reserve R254 at 9/19.

Add WOL_EN back. 10/10

Add in 10/04.

Add in 9/14.
Add RP15 back. 9/27

Pin connection error, modify in 10/24.

Within 500 mils

Within 500 mils

Place closely pin AF3

Place closely pin H1

R276 low -->default
High -->No boot

9/21

U8C

ICH9-M SFF ES_FCBGA569

U8D

ICH9-M SFF ES_FCBGA569

SYS GPIO Power MGT

GPIO Controller Link

MISC

PCI-Express Direct Media Interface

WLAN

EXP

WWAN

GLAN

SPI

USB

SATA GPIO

SMB

Clocks

MB

EXPRESS

WLAN

MB

MB

Bluetooth

WWAN

Fingerprint

DOCK

USB Camera

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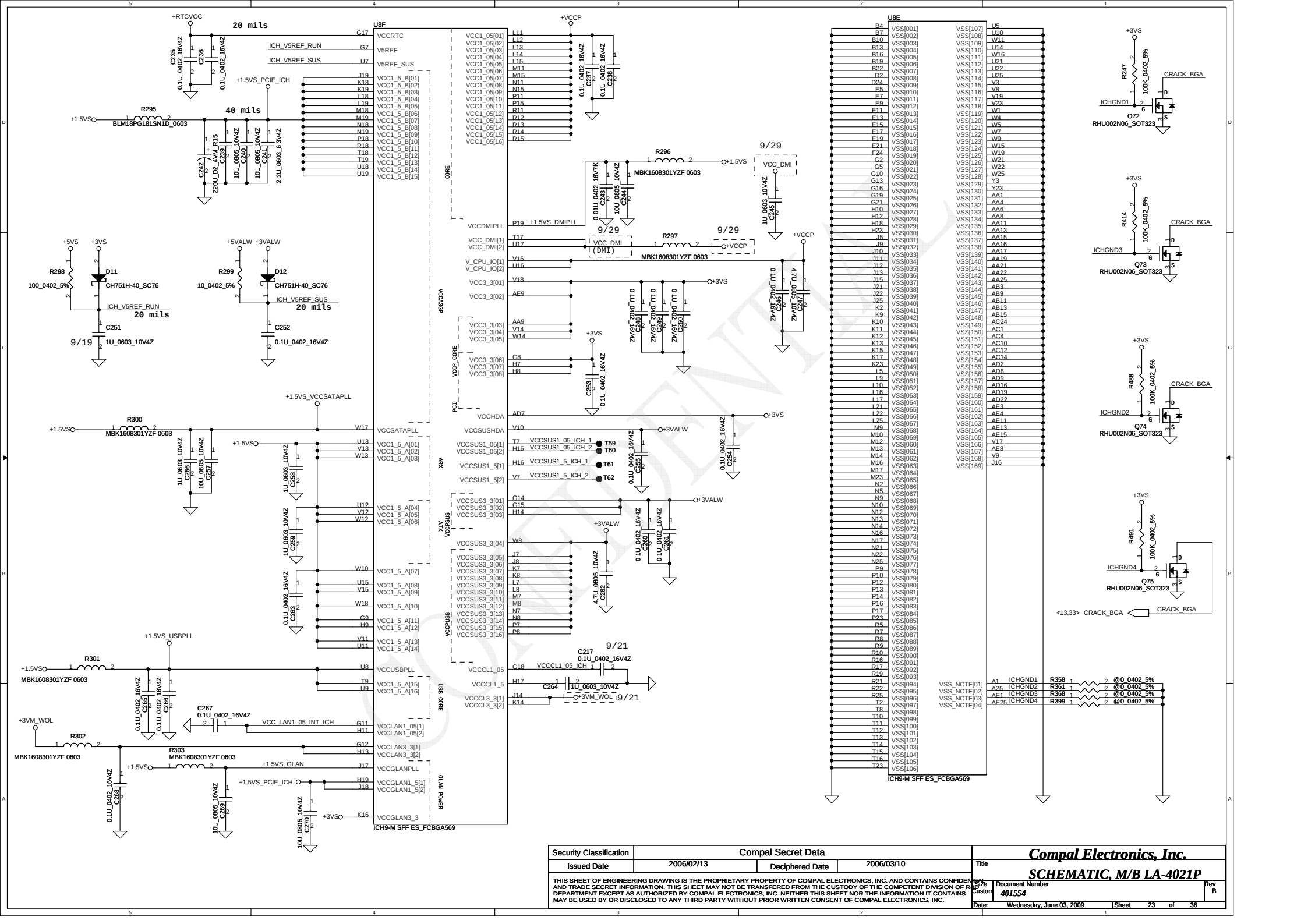

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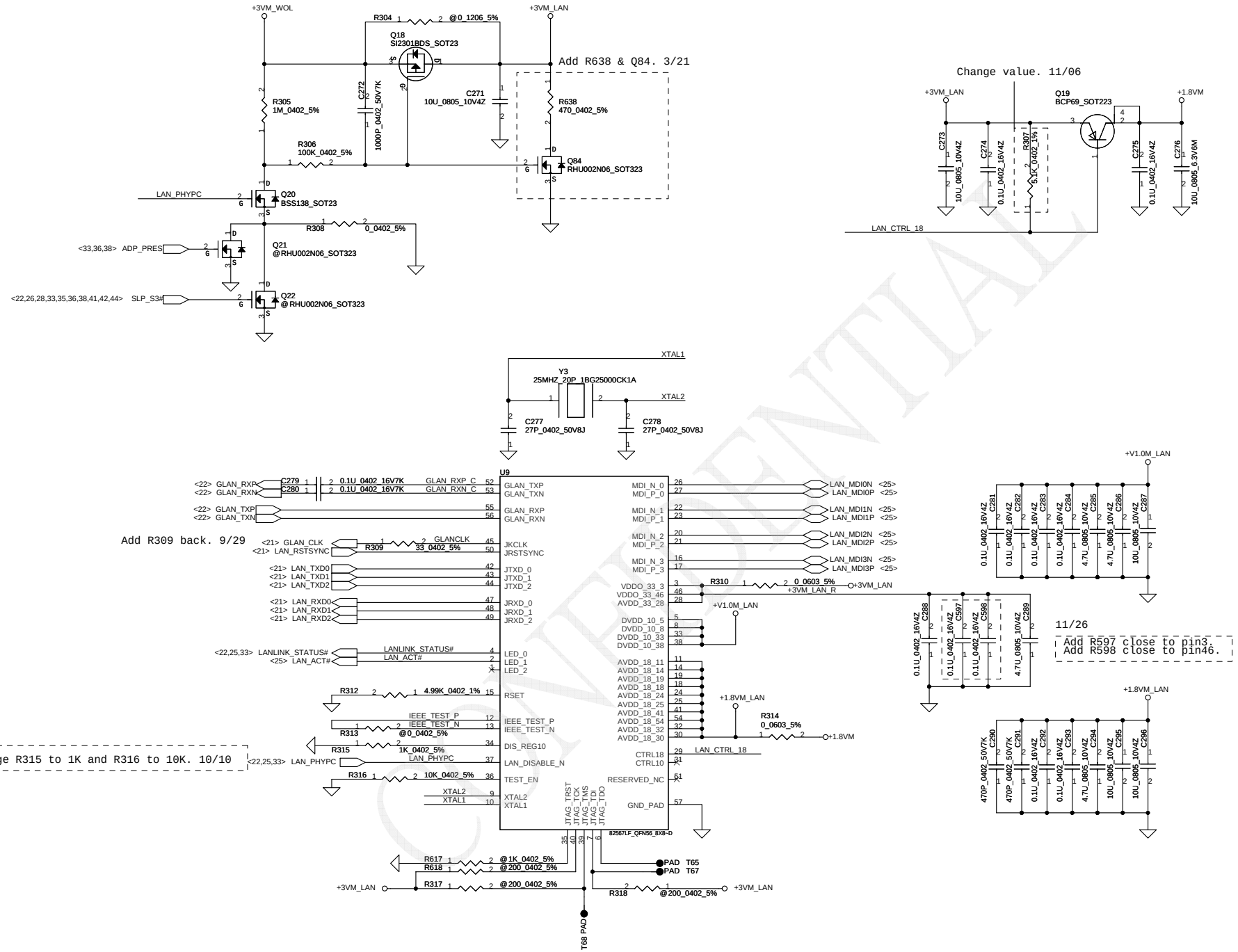

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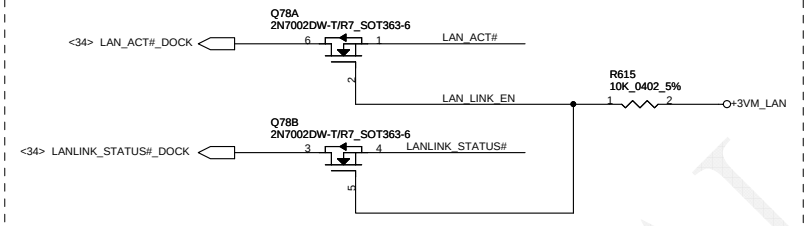
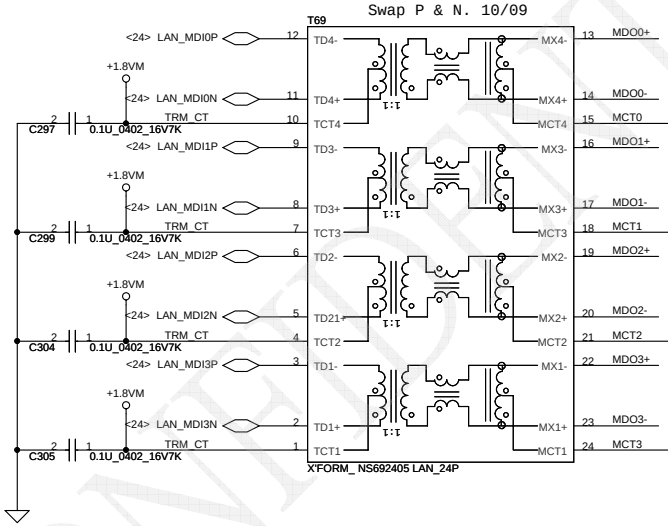
Swap Q78A,B D & S pin. 2/22



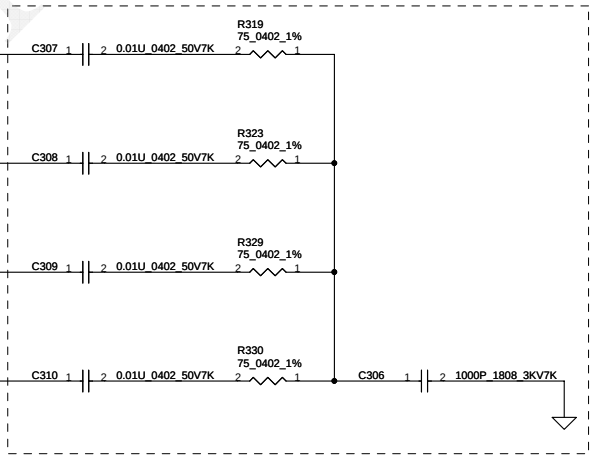
Delete all termination cause they are already inside BOAZMAN. 9/28

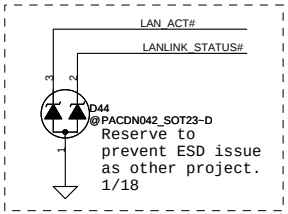
Pin Swap. 10/05

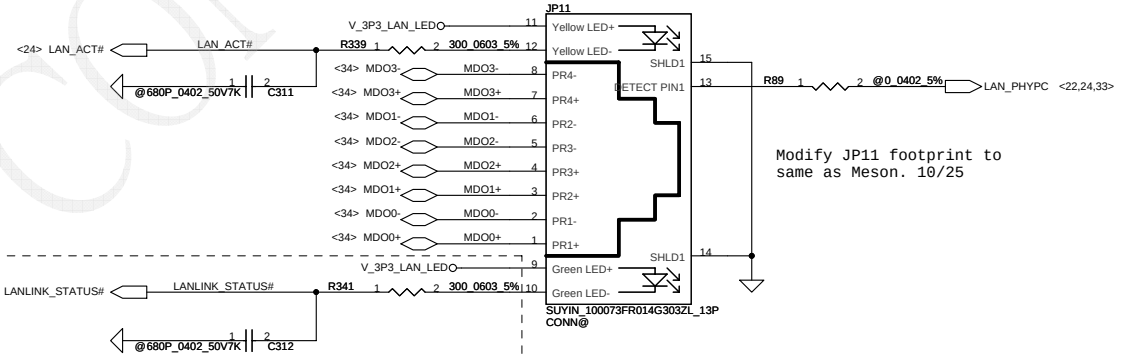
Swap P & N. 10/09



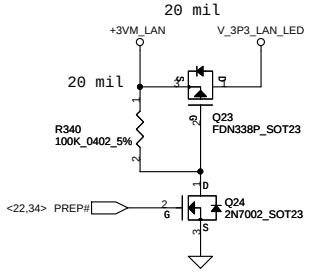
Change design. 10/12







Modify JP11 footprint to
same as Meson. 10/25



Swap connection of JP11 pin9 & pin10. 11/26

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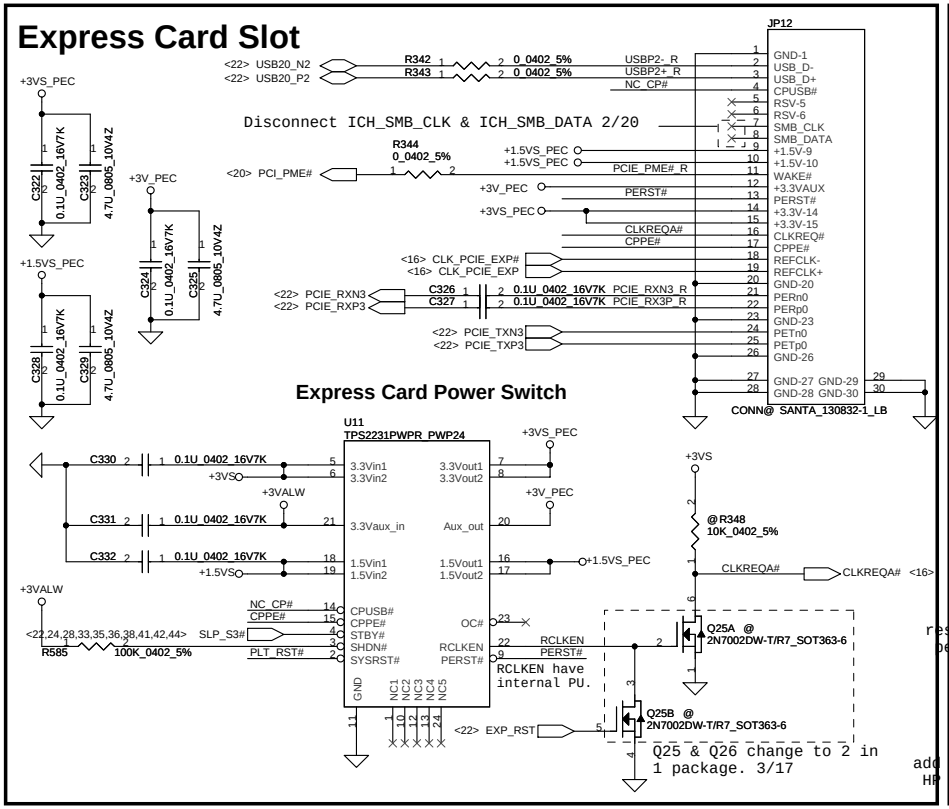
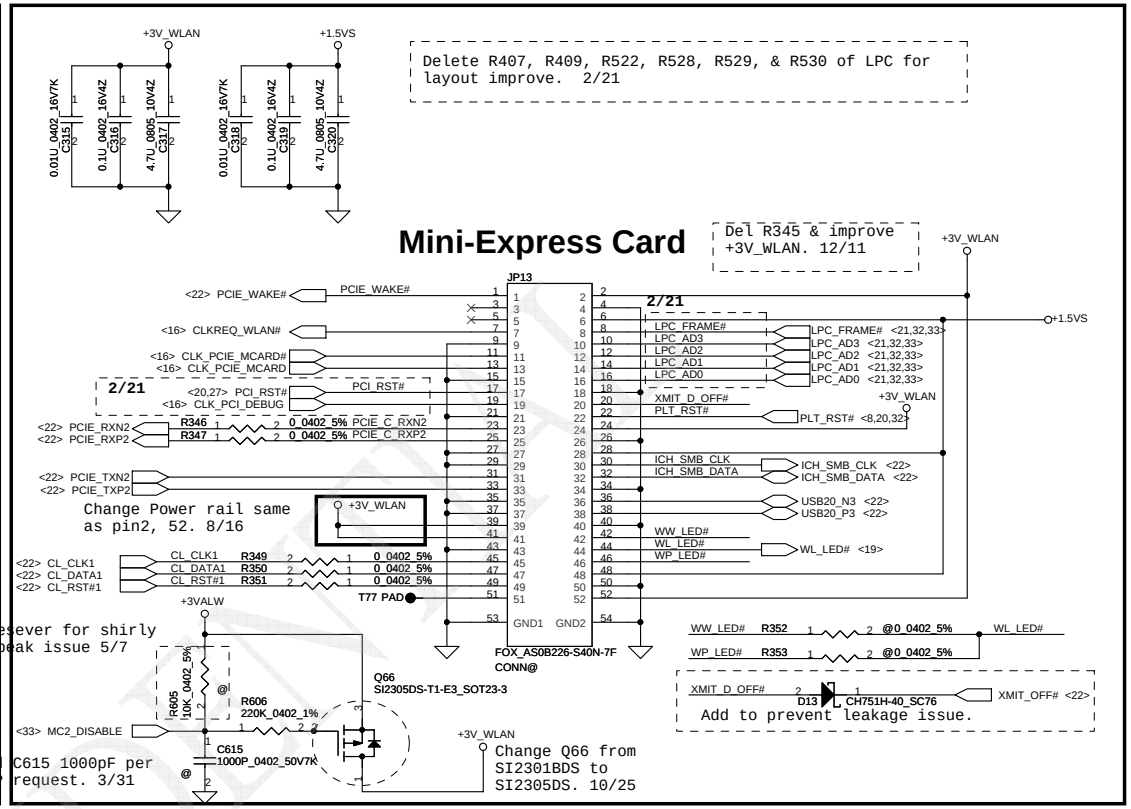
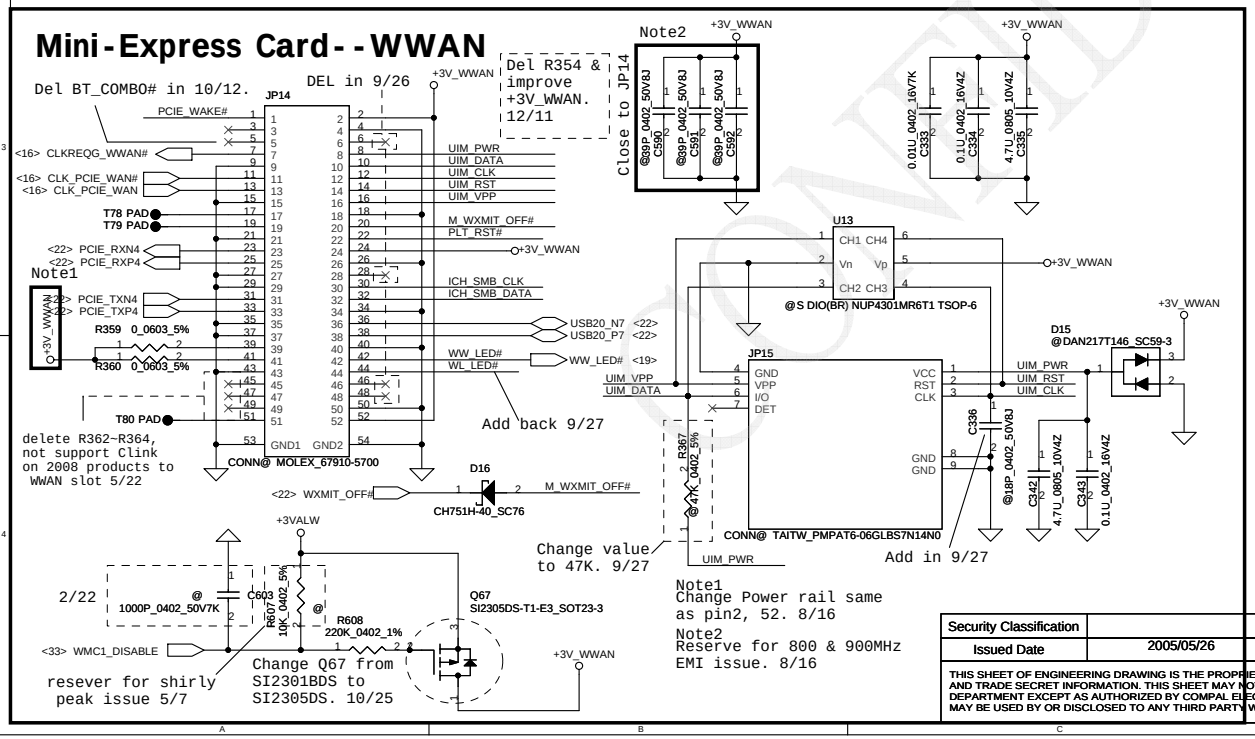
Express Card Slot



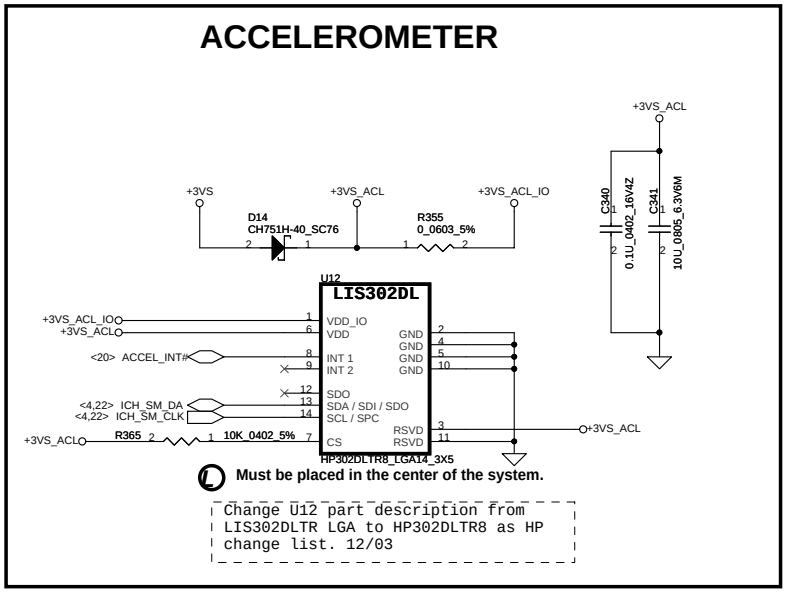
Mini-Express Card



Mini-Express Card--WWAN



ACCELEROMETER



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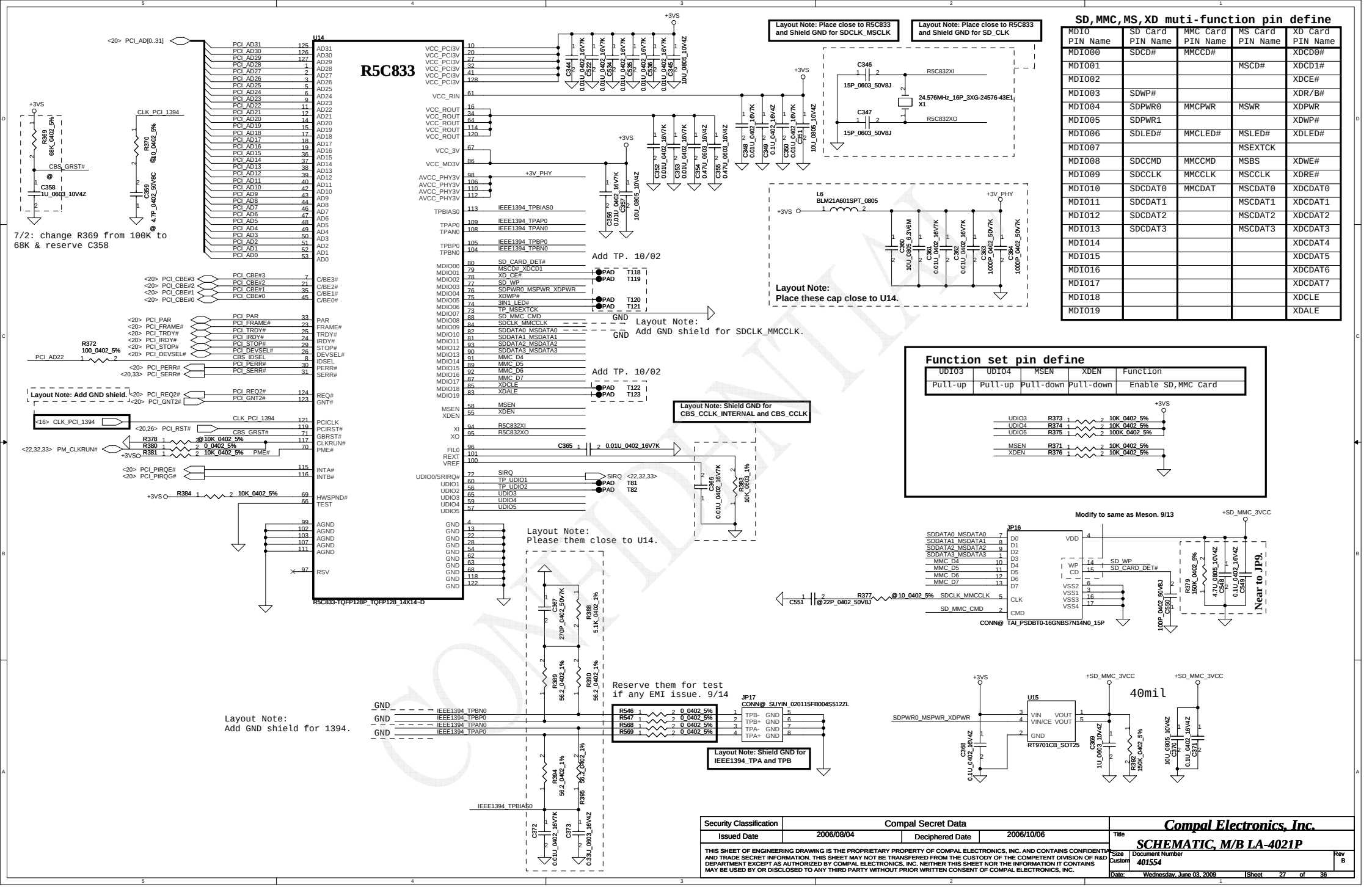

SD,MMC,MS,XD muti-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SDCD#	MMCCD#		XDCD0#
MDIO01			MSCD#	XDCD1#
MDIO02				XDCE#
MDIO03	SDWP#			XDR/B#
MDIO04	SDPWR0	MMCPWR	MSWR	XDPWR
MDIO05	SDPWR1			XDWP#
MDIO06	SDLED#	MMCLED#	MSLED#	XDLED#
MDIO07			MSEXTCK	
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCCLK	MMCCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1		MSCDAT1	XDCDAT1
MDIO12	SDCDAT2		MSCDAT2	XDCDAT2
MDIO13	SDCDAT3		MSCDAT3	XDCDAT3
MDIO14				XDCDAT4
MDIO15				XDCDAT5
MDIO16				XDCDAT6
MDIO17				XDCDAT7
MDIO18				XDCLE
MDIO19				XDALE

Function set pin define

UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-down	Pull-down	Enable SD,MMC Card

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AMP. FOR INTERNAL SPEAKER

TPA6044 no longer needed. So delete BOM options & co-layout components for TPA6044. SGND and SGND1 nets can also be deleted. Only TPA6041 will be supported. 9/5

	GAIN1	GAIN0
10dB	0	0
12dB	0	1
15.6dB	1	0
21.6dB	1	1

Modify in 3/26
Change gain to 12db.
R402 install.
R400 not install.

Change value. 9/28

Change in 3/28

Change in 4/1

Change in 3/28

Adjust line-in attenuation from -6dB to -10dB by change R415, R418 = 6.04K and changing R417, R420 = 2.0k.

Correct net name. 10/02

Connect to GNDA. 3/20

Place close to U14

Add in 3/28

pull 4.7k to +3VS & 0.01U to GND for ESD solution 2008/04/22

Add R571, D37 in 9/26.

ESD Request. 03/19

Add in 3/28

Q34 & Q35 change to 2 in 1 package. 3/17

U16 TPA6041A4RHBR QFN 32P

U17 AD1984JCPZ-RL_LFCSP48_7X7

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

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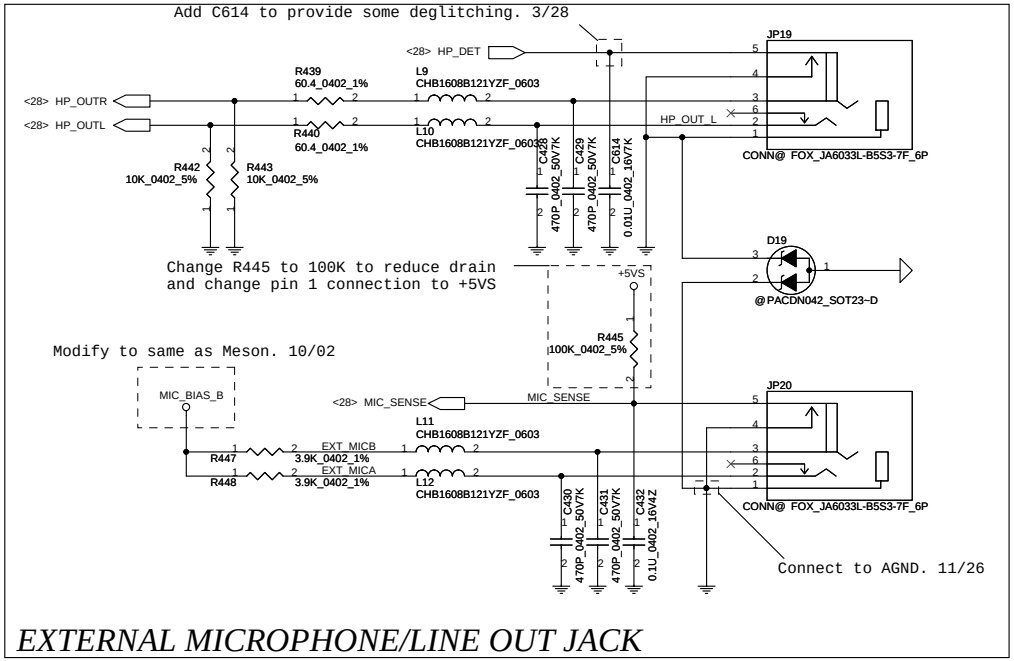
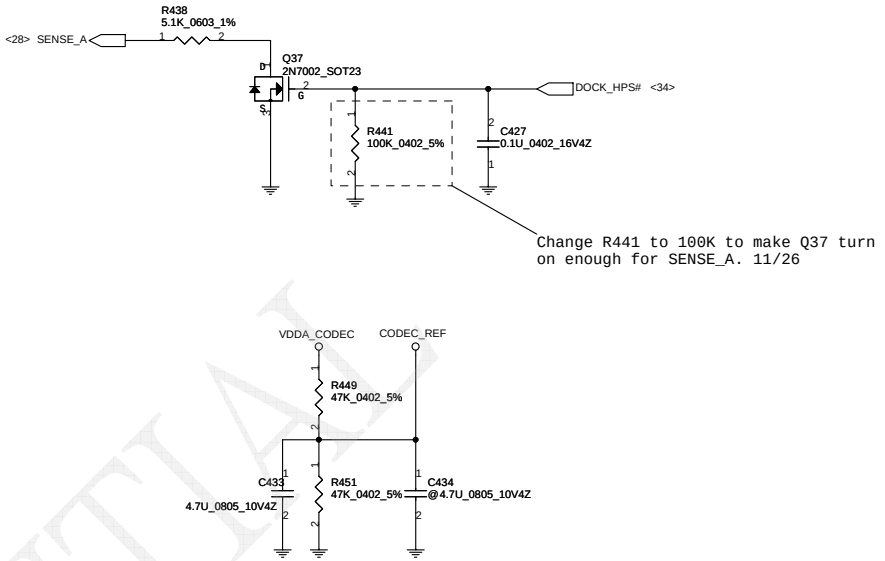
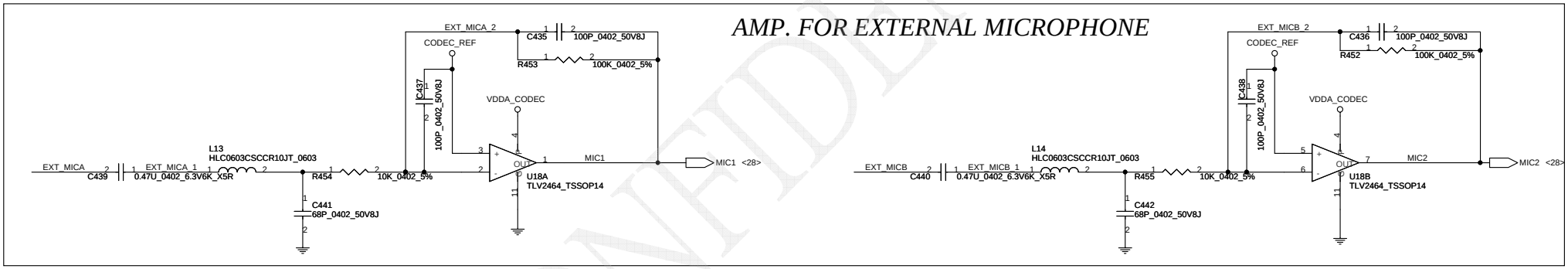
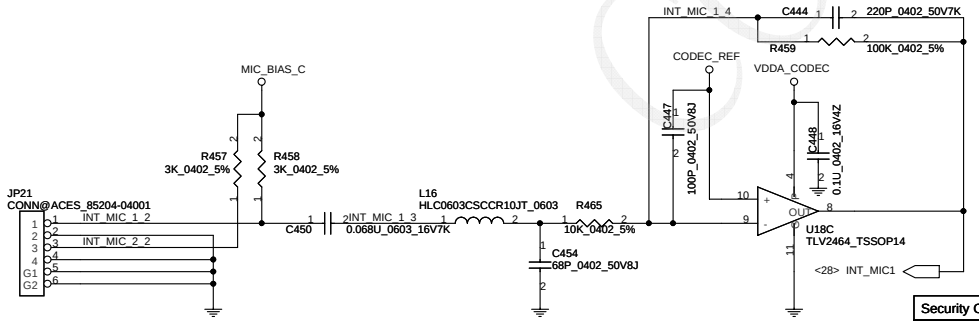


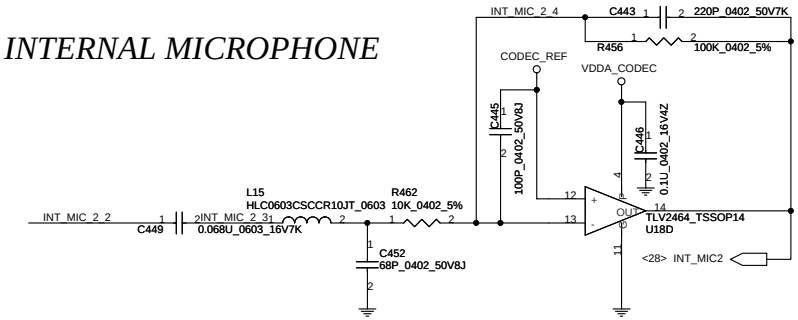
EXTERNAL MICROPHONE/LINE OUT JACK







AMP. FOR INTERNAL MICROPHONE



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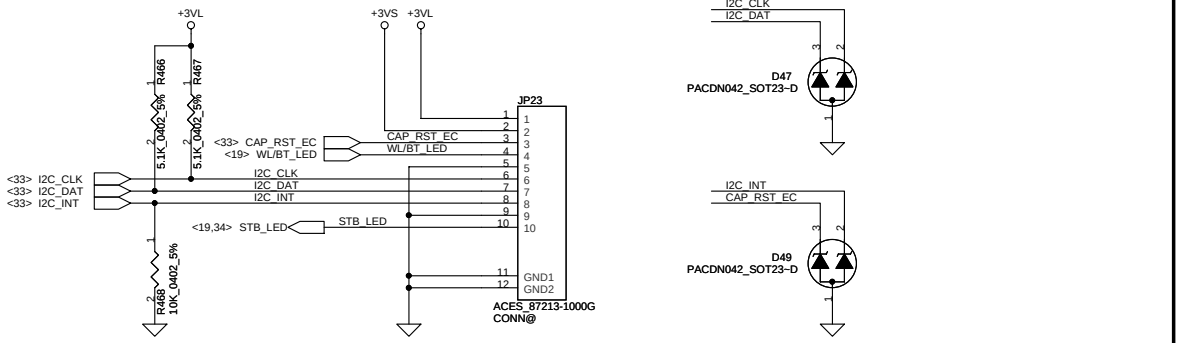
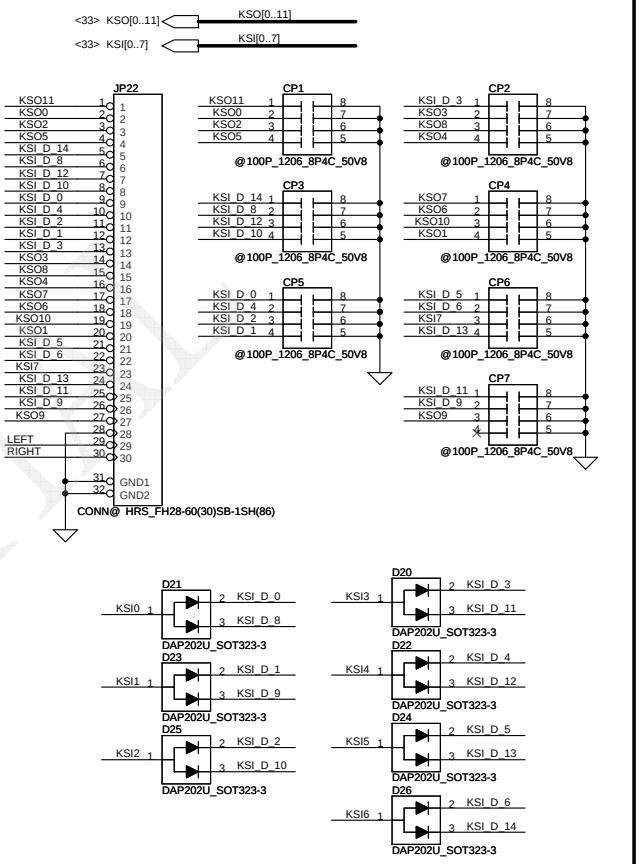
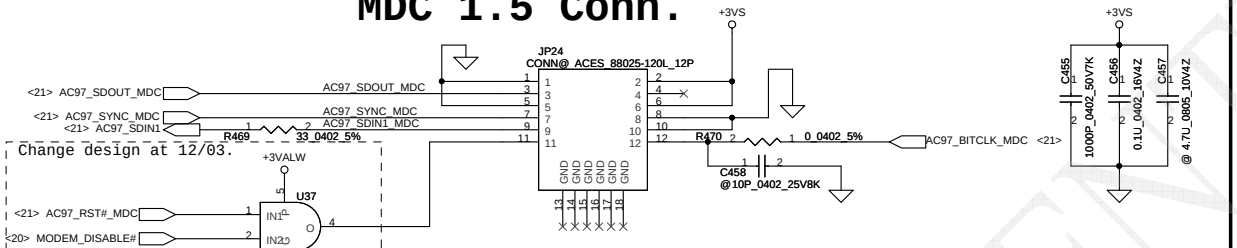
SWITCH BOARD.



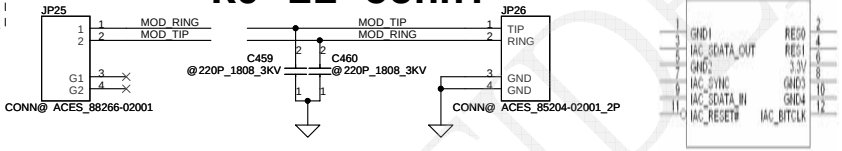
INT_KBD CONN.



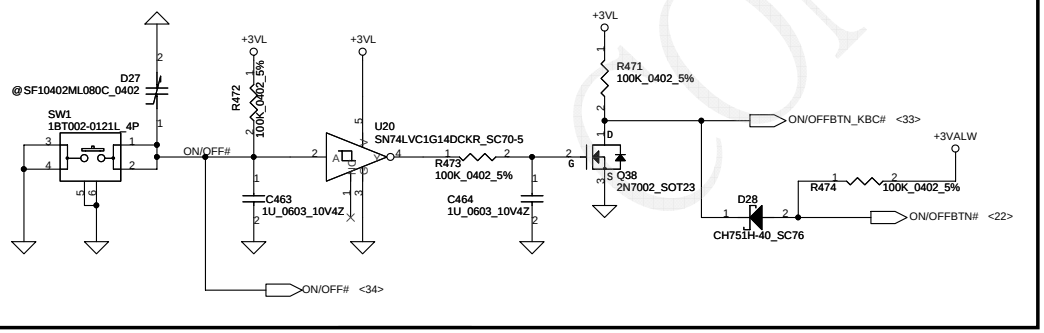
MDC 1.5 Conn.



RJ-11 Conn.

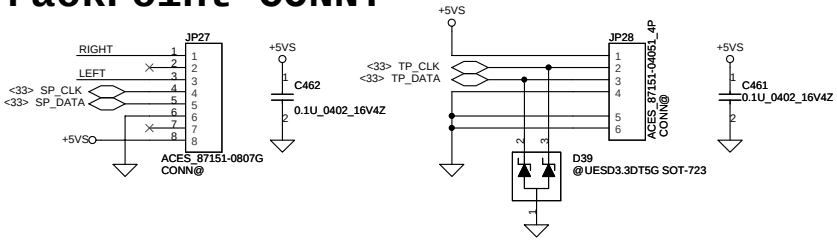


Power button



TrackPoint CONN.

T/P BOARD.



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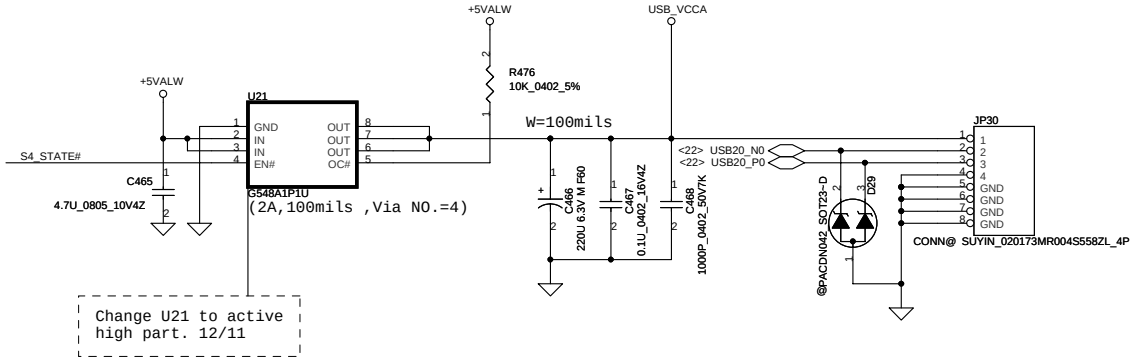
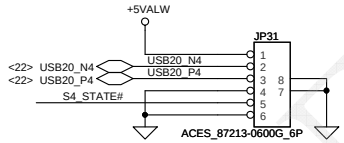
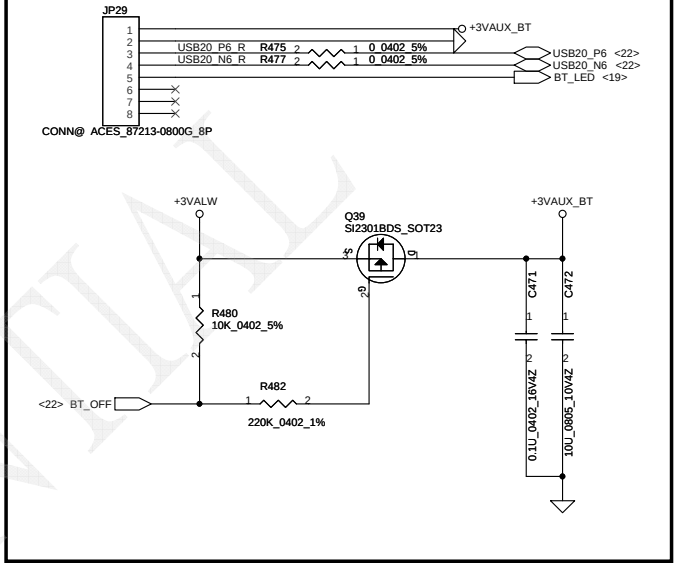


Change U21 to active high part. 12/11

U22, D30, R481, C474 ~ C477 will move to USB board side to save M/B space.

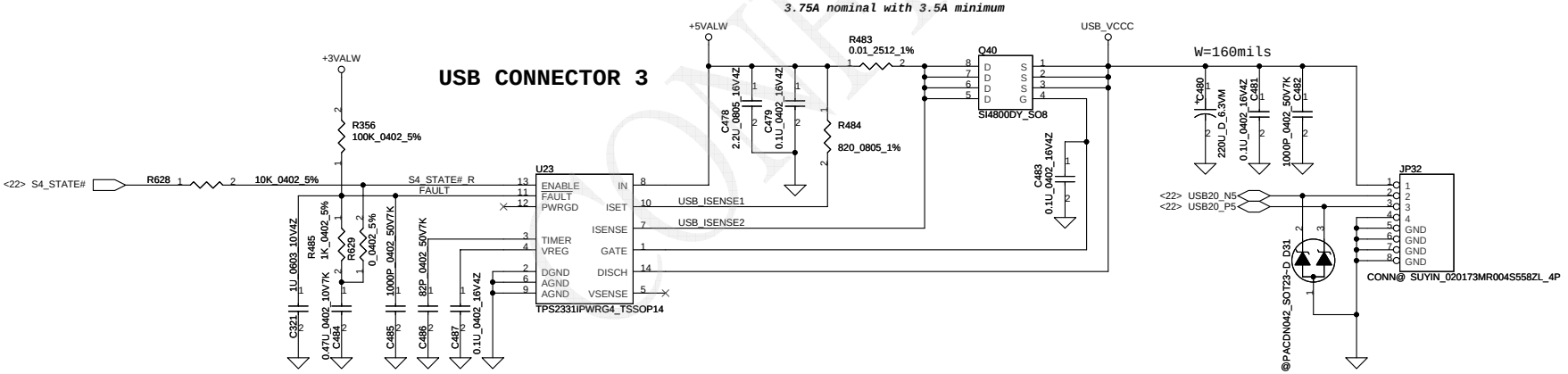


BT Connector



USB CONNECTOR 3

3.75A nominal with 3.5A minimum



Change for SI1 to prevent USB power short to GND cause system shutdown. 0130

Change C486 from 2200pF to 680pF.
Change C321 from 1000pF to 1uF.
Change R356 from 10K to 100K.
Change C484 from 1000pF to 0.47uF.
Change R484 from 1K to 820.

Currently power USB will not enable after OCP, so add R629 make it enable after OCP free.

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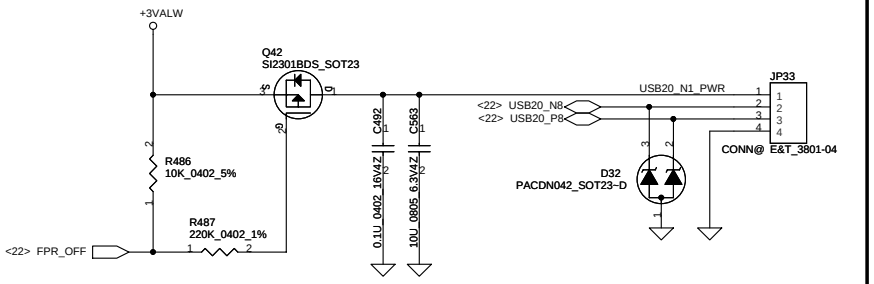
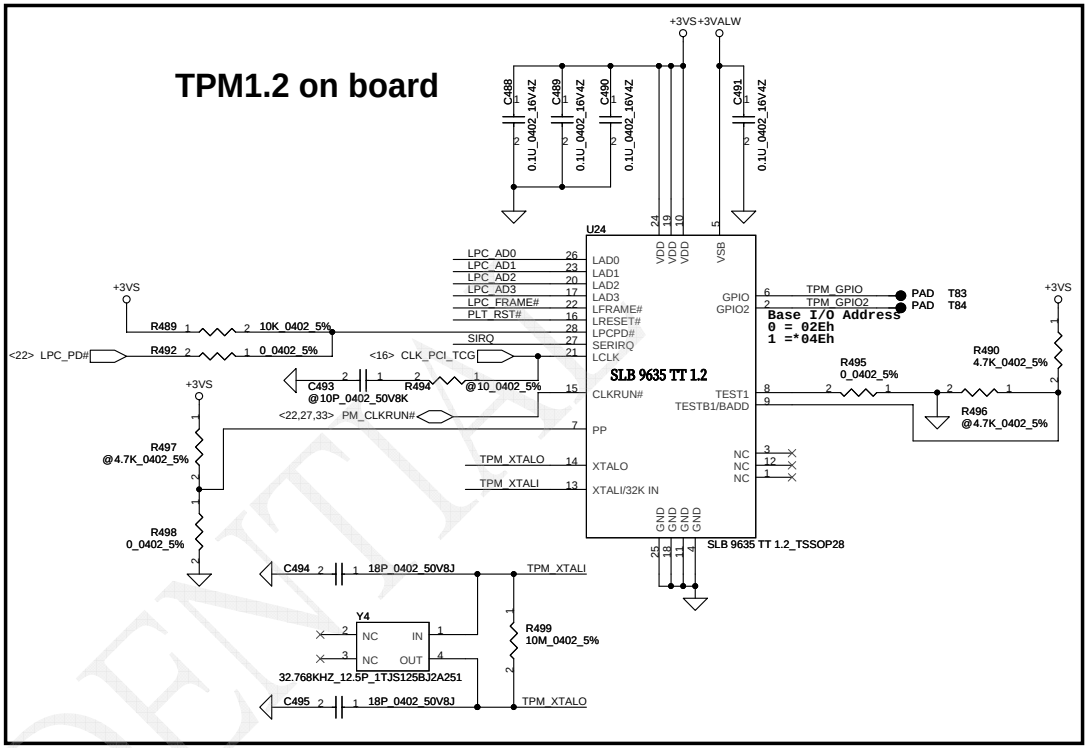
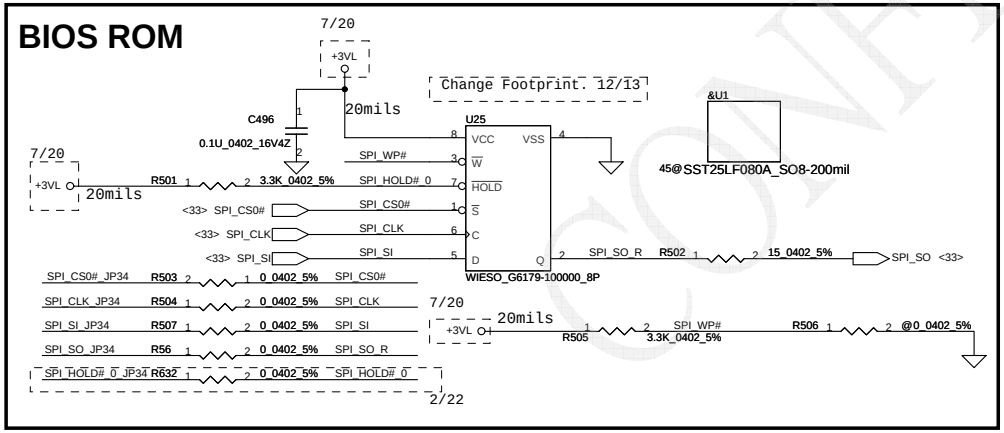
Finger printer



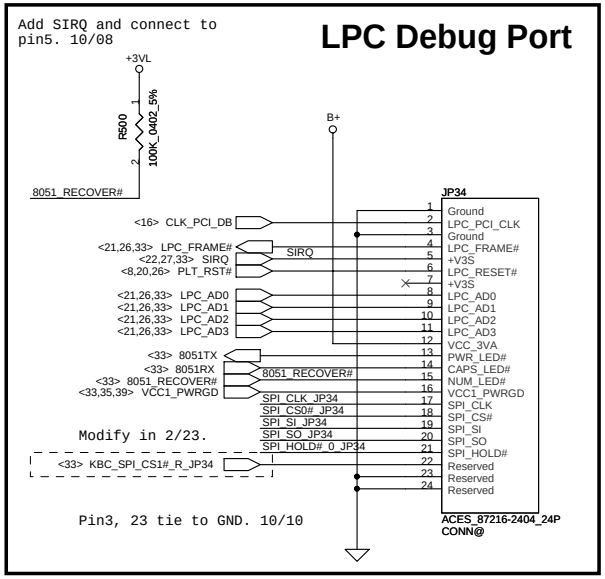
TPM1.2 on board



BIOS ROM



LPC Debug Port



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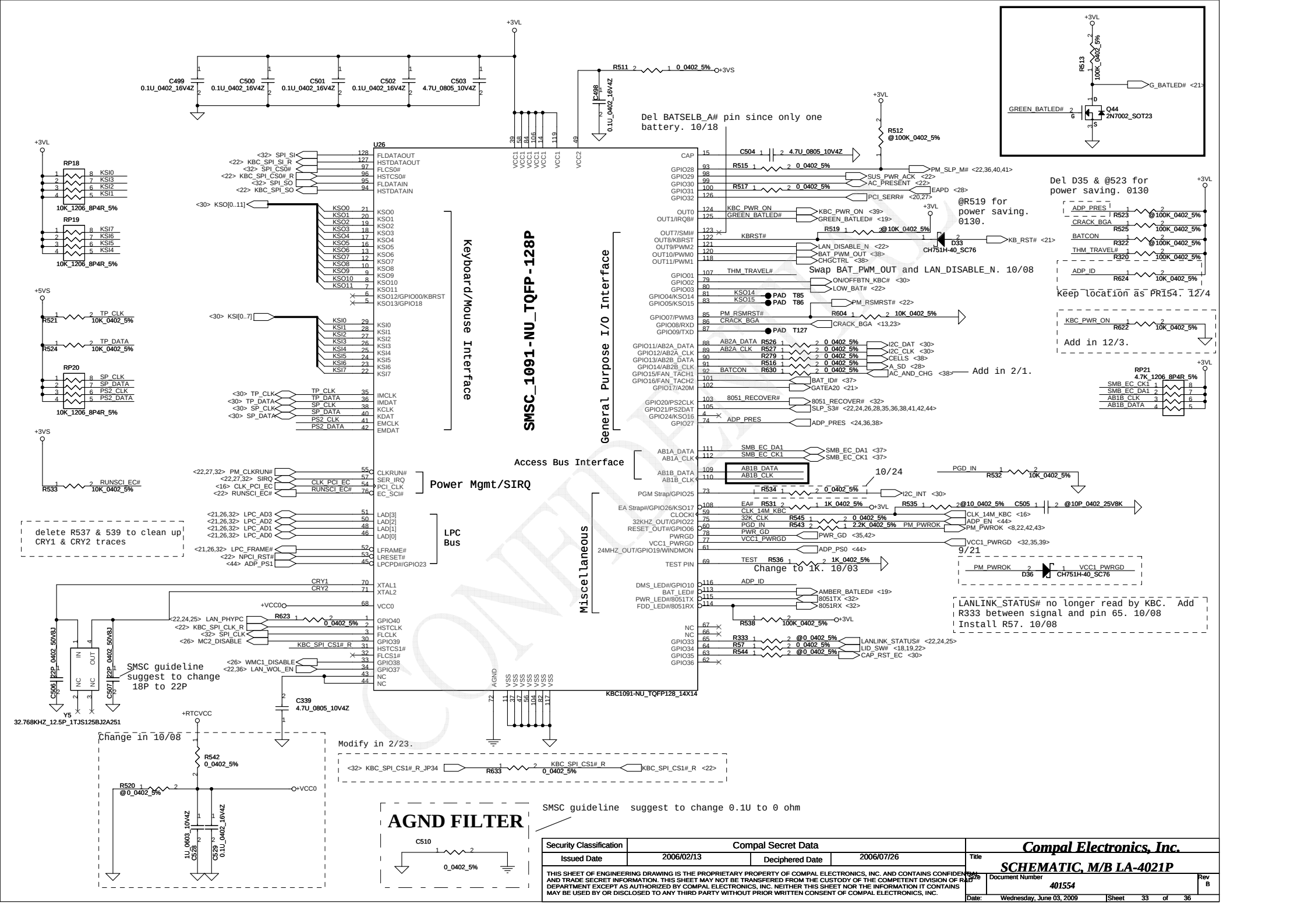
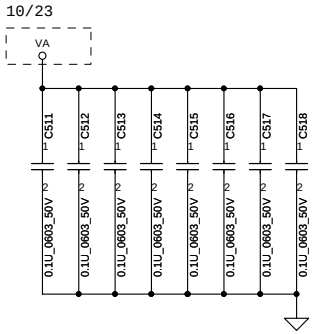
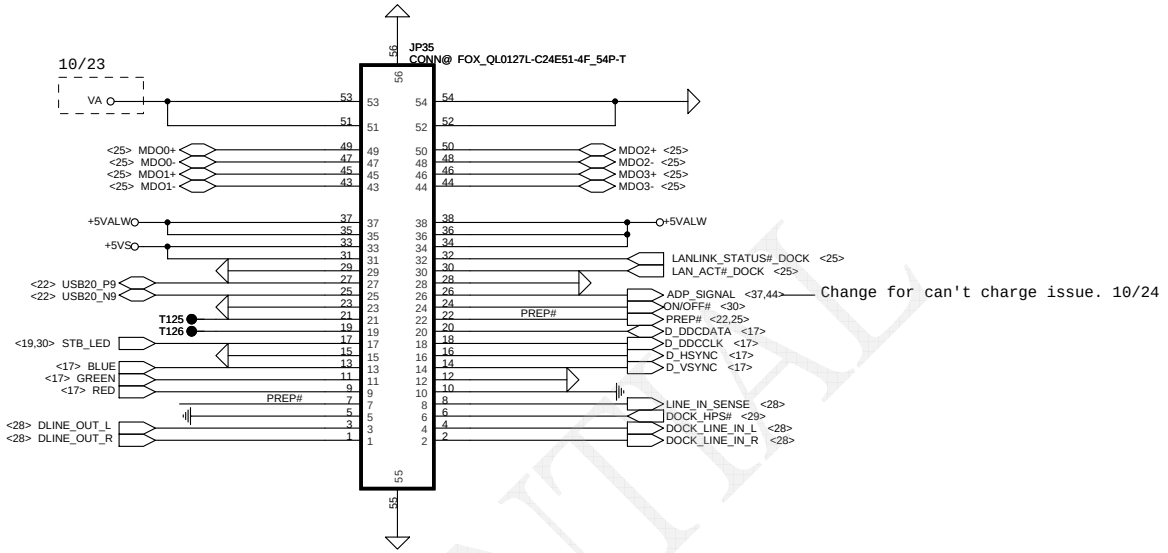


DOCKING CONNECT





Delete:

1. L21 ~ L23.
2. C605 ~ C610.
3. R635 ~ R637.
4. U27 ~ U29.
5. C519 ~ C521.
6. R548 ~ R550.

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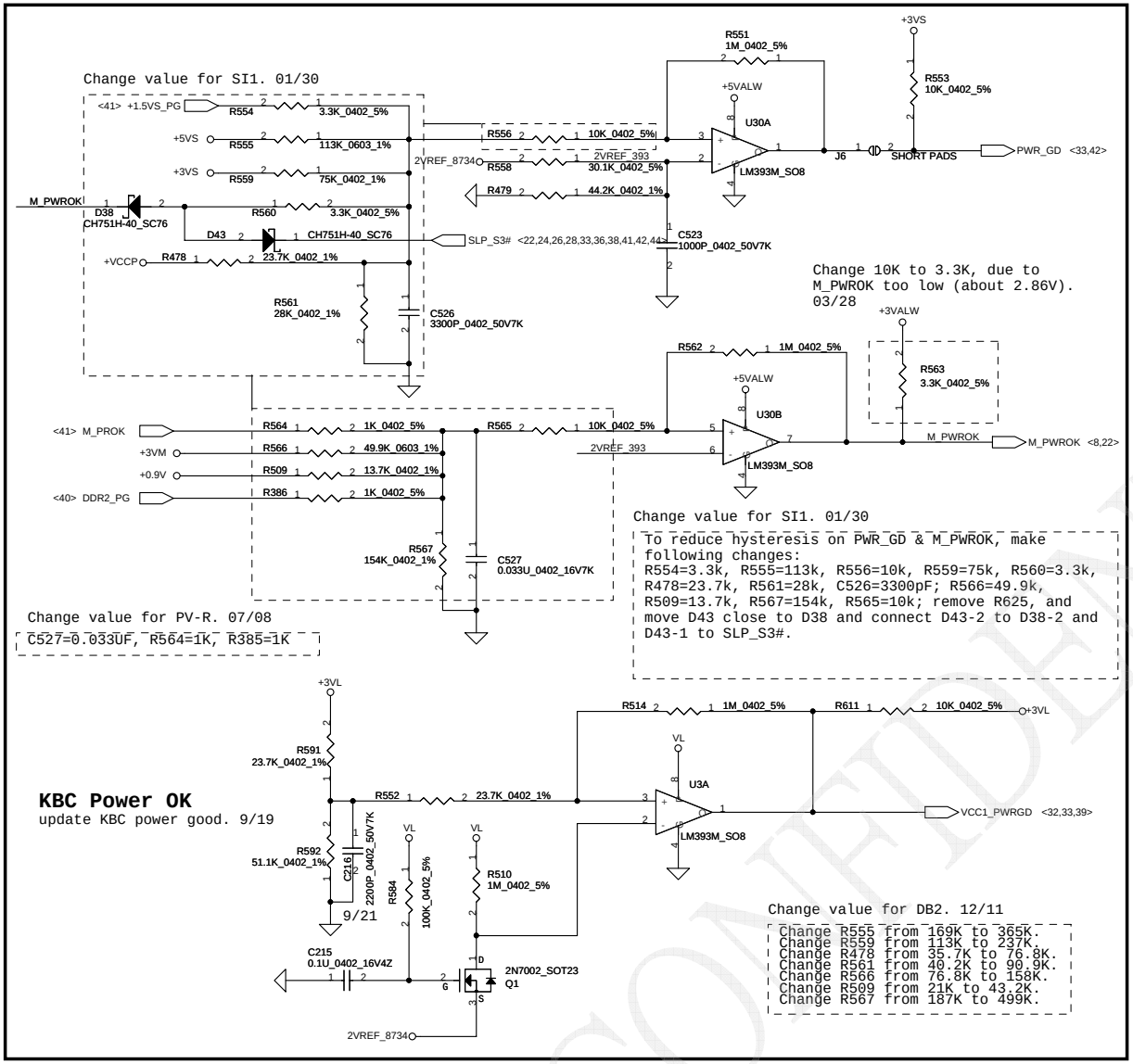
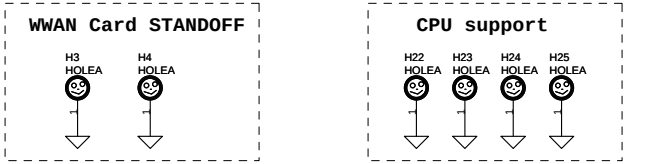
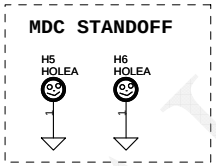
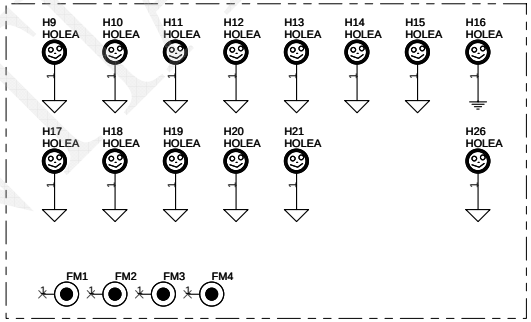
Update per change list. 9/14

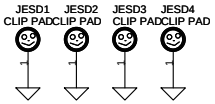






Del H1, H7 & H8. 1/18





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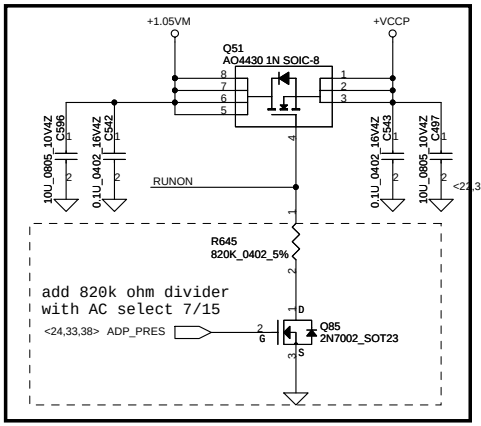
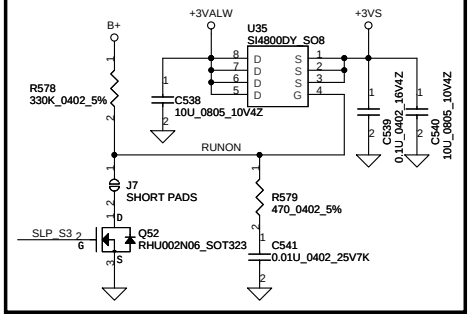
Modify at 7/31 after discuss with power team.

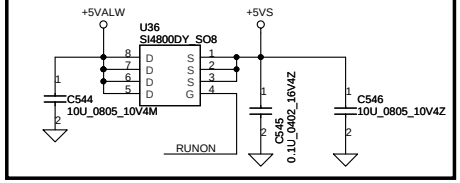
+1.05VM to +VCCP Transfer



+3VALW to +3VS Transfer

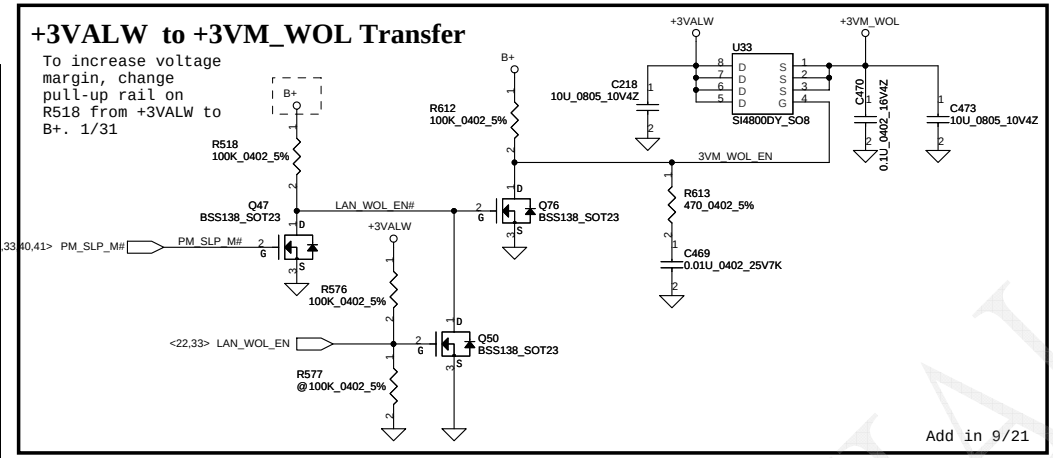


+5VALW to +5VS Transfer



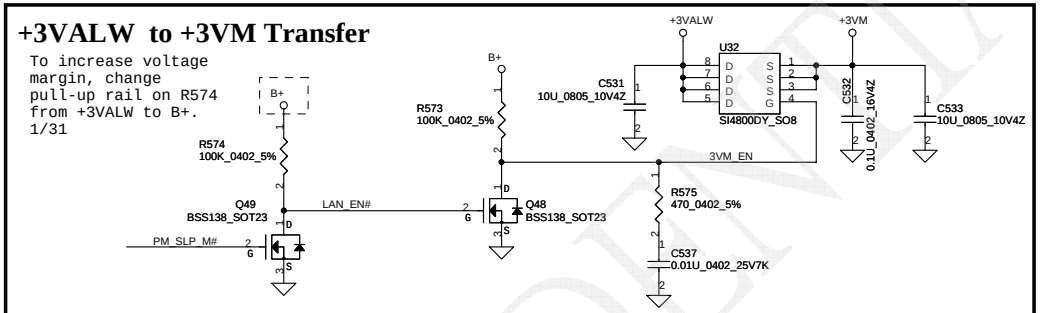
+3VALW to +3VM_WOL Transfer

To increase voltage margin, change pull-up rail on R518 from +3VALW to B+. 1/31

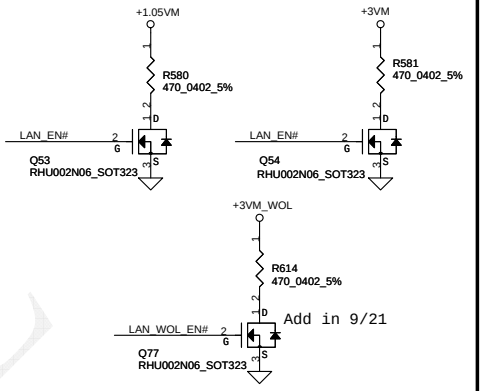


+3VALW to +3VM Transfer

To increase voltage margin, change pull-up rail on R574 from +3VALW to B+. 1/31

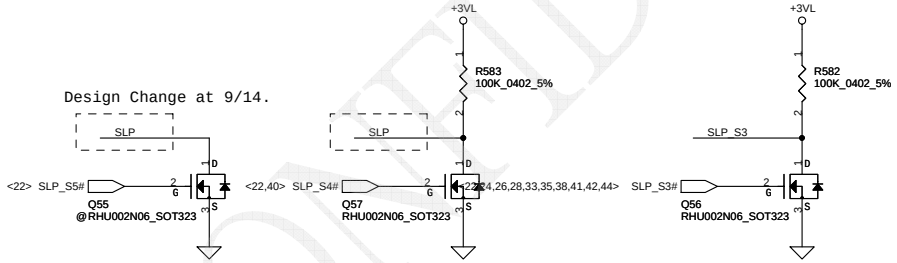


Discharge circuit-2 for V-M



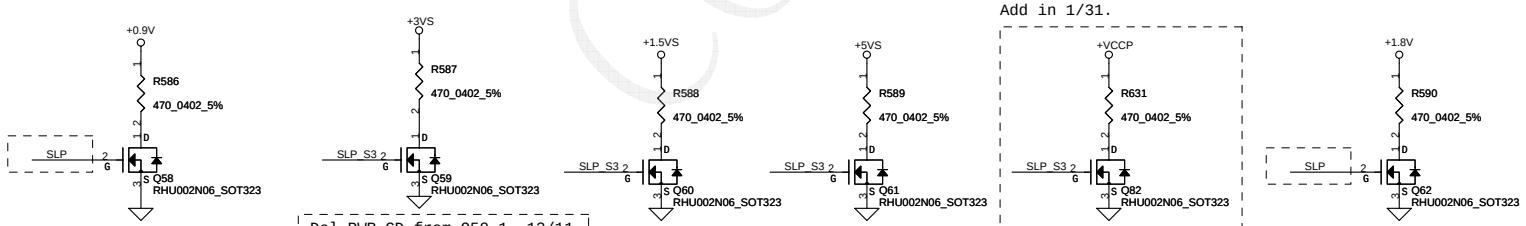
SYS. STATE	PM_SLP_M#	LAN_WOL_EN	+3VM_WOL	+3VM
M-off / No WOL	0	0	0V	0V
M-off / WOL	0	1	3.3V	0V
M1 (ME on)	1	0	3.3V	3.3V
M1 (ME on)	1	1	3.3V	3.3V

Design Change at 9/14.



Discharge circuit-1

Add in 1/31.



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