

KTKAA

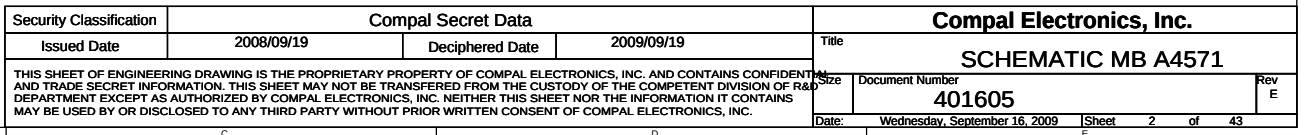
Los Angeles 10/10G

LA-4571P REV 2.0 Schematic

Intel Penryn/ Cantiga/ ICH9M
2008-09-19 Rev. 2.0

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Model Name : KTKAA
File Name : LA-4571P



Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VL	5V always on power rail	ON	ON	ON	ON
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON
+CPU_CORE	Core voltage for VGA chip	ON	ON	OFF	OFF
+VGA_PCIE_1.1VS	1.1V switched power rail for VGA PCIE	ON	ON	OFF	OFF
+1.8VS	1.8V power rail for VRAM	ON	ON	OFF	OFF

External PCI Devices

EC SM Bus1 address

Power	Device	Address	Power	Device	Address
+5VL	EC KB926 C0		+3VS	EC KB926 C0	
+5VL	Smart Battery	0001 011X b			
+5VL	HDMI-CEC	0011 010x b	+3VS	CPU THM Sen	
				SMSC SMC1402	0100 110x b
+5VL	FUN/B (CAP Sensor)		+3VS	VGA THM Sen	1001 110Xb
				ADM1032ARMZ	
				VGA on die thermal sensor	1001 111Xb
					need to confirm

ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
	Clock Generator (SLG8SP556V)	1101 001Xb
+3VS		
+3VS	DDR DIMM0	1001 000Xb
+3VS	DDR DIMM1	1001 010Xb
+3VS	Express	
+3VS	FM Module	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		

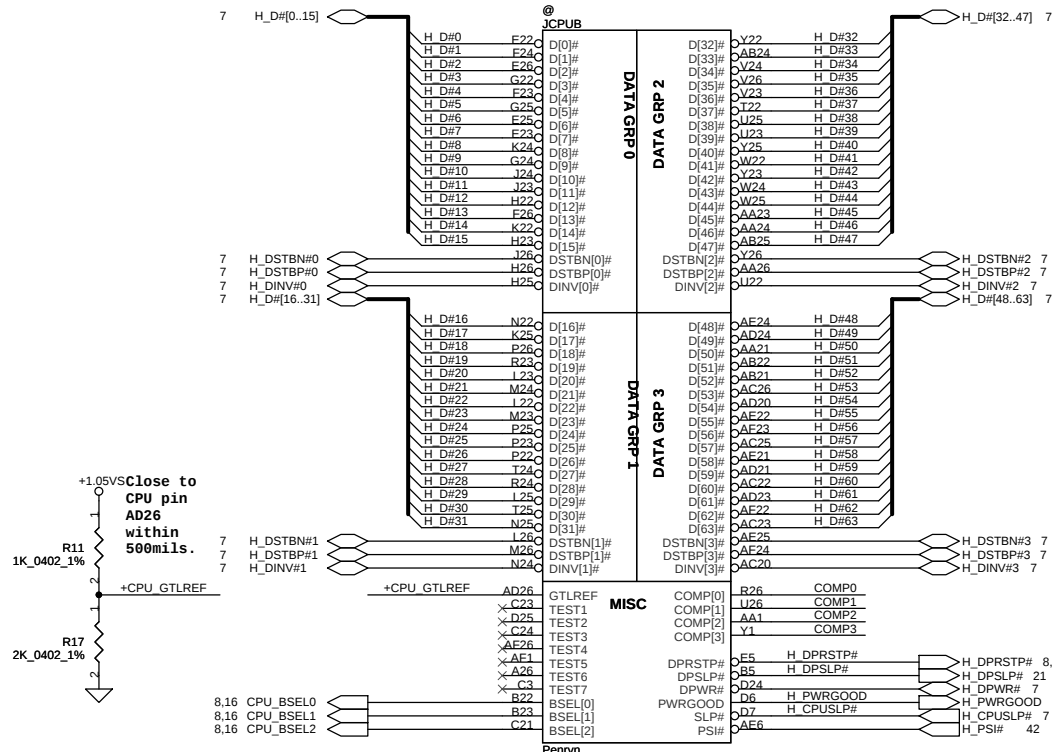
BTO Option Table

Function	2nd HDD	LAN		Mini card		RJ11/FM tuner		3G SIM slot
description	(2H)	(E)	(C)	(D2)	(D3)	(R)	(M)	(G)
explain		10/100M	Giga	Two Crads	three Crads	RJ11	FM	
BTO	2HDD@	8102E@	8111C@	WLAN@	GPS@	NAND@	MDC@	3G@

Function	HDMI			TV-out	CIR	CAMERA & MIC		Finger printer
description	(Y)			(S)	(I)	(X)		(F)
explain	Intel(UMA)	ATI VGA/B		COMMON			CAMERA	MIC
BTO	IHDMI@	NIHDMI@	HDMI@	H@	TVOUT@	CIR@	CAM@	MIC@

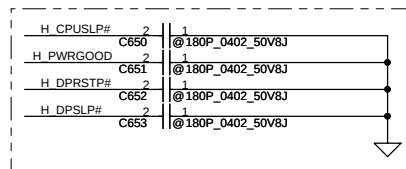
Function	Felica	BLUE T00TH	
description	(J)	(B)	
explain			
BTO	FLICA@	BT@	

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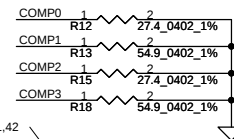


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

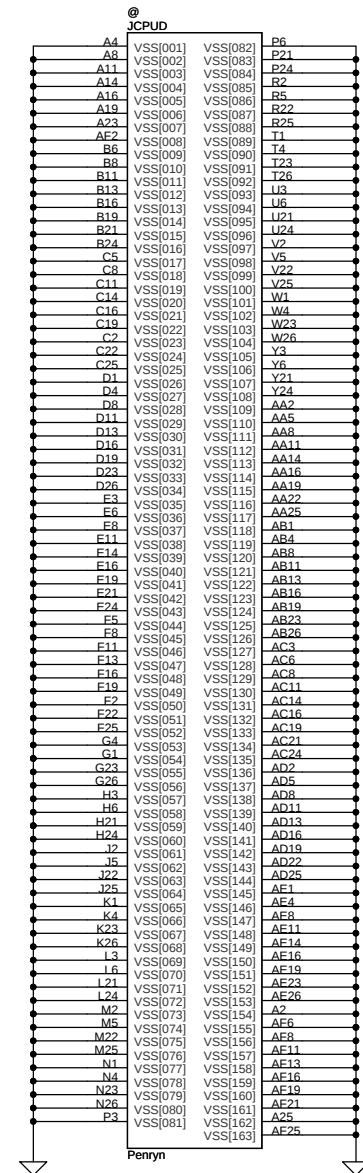


Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



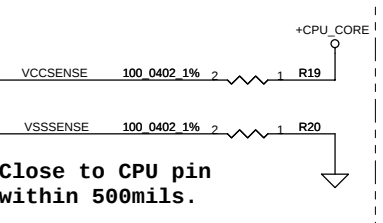
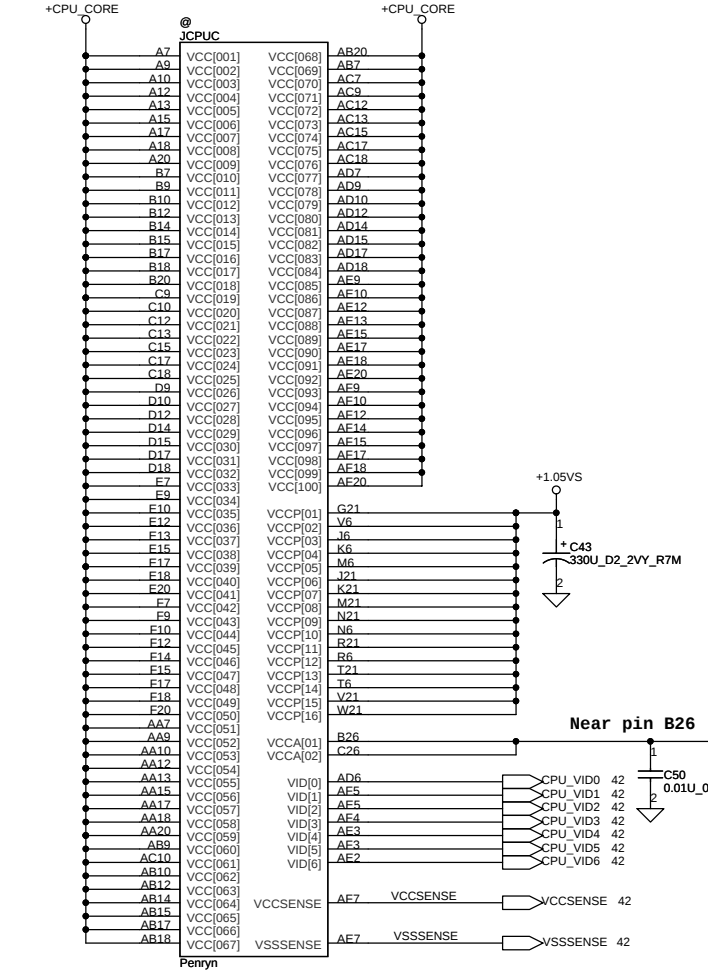
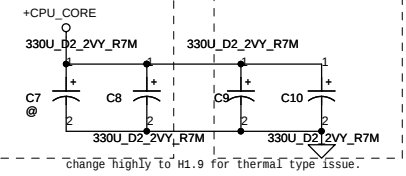
layout note: Please use "Daisy Chain" to layout and the signal (H_DPRSTP#) is routed from ICH9 to power IC, then to NB and CPU

Reserve for debug close to CPU

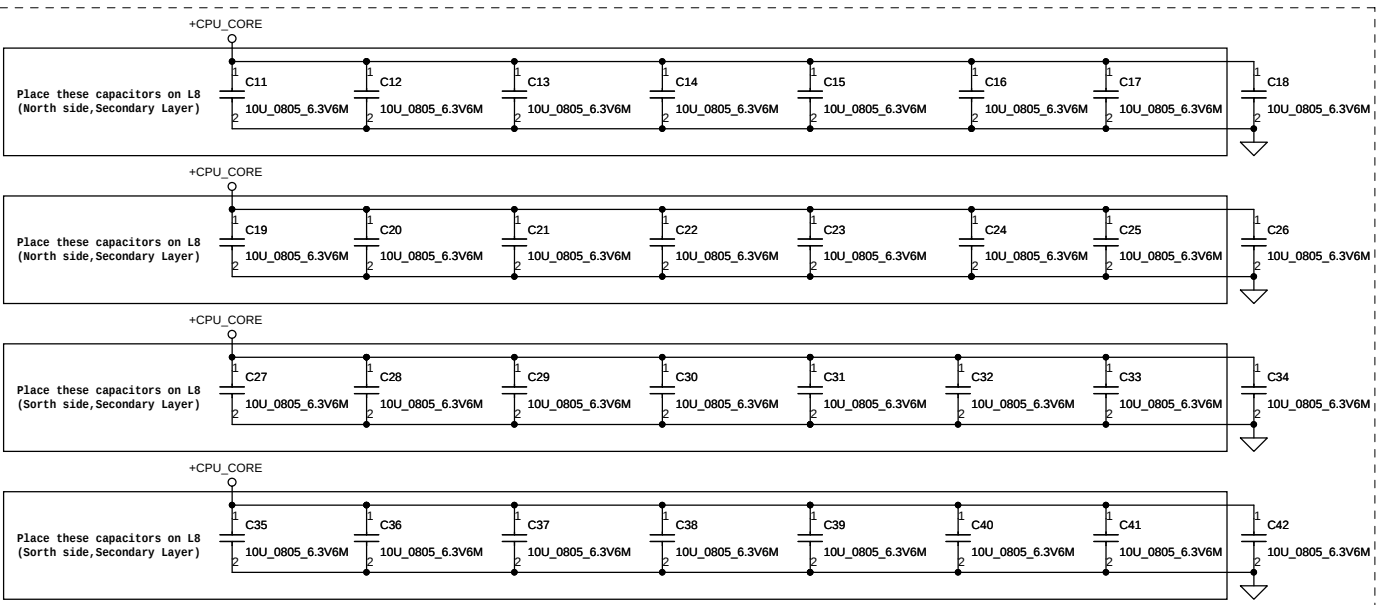


Near CPU CORE regulator

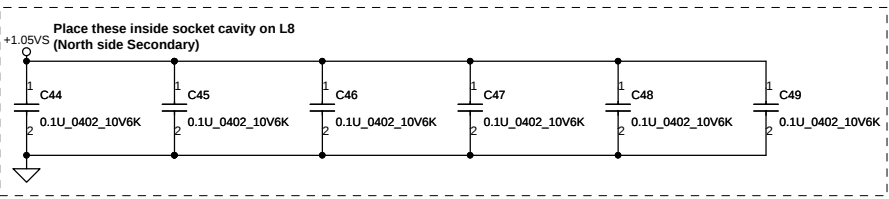
ESR <= 1.5m ohm
Capacitor > 1980uF



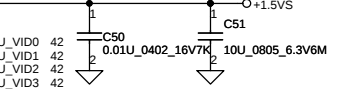
Length match within 25 mils.
The trace width/space/other is 14/7/25.



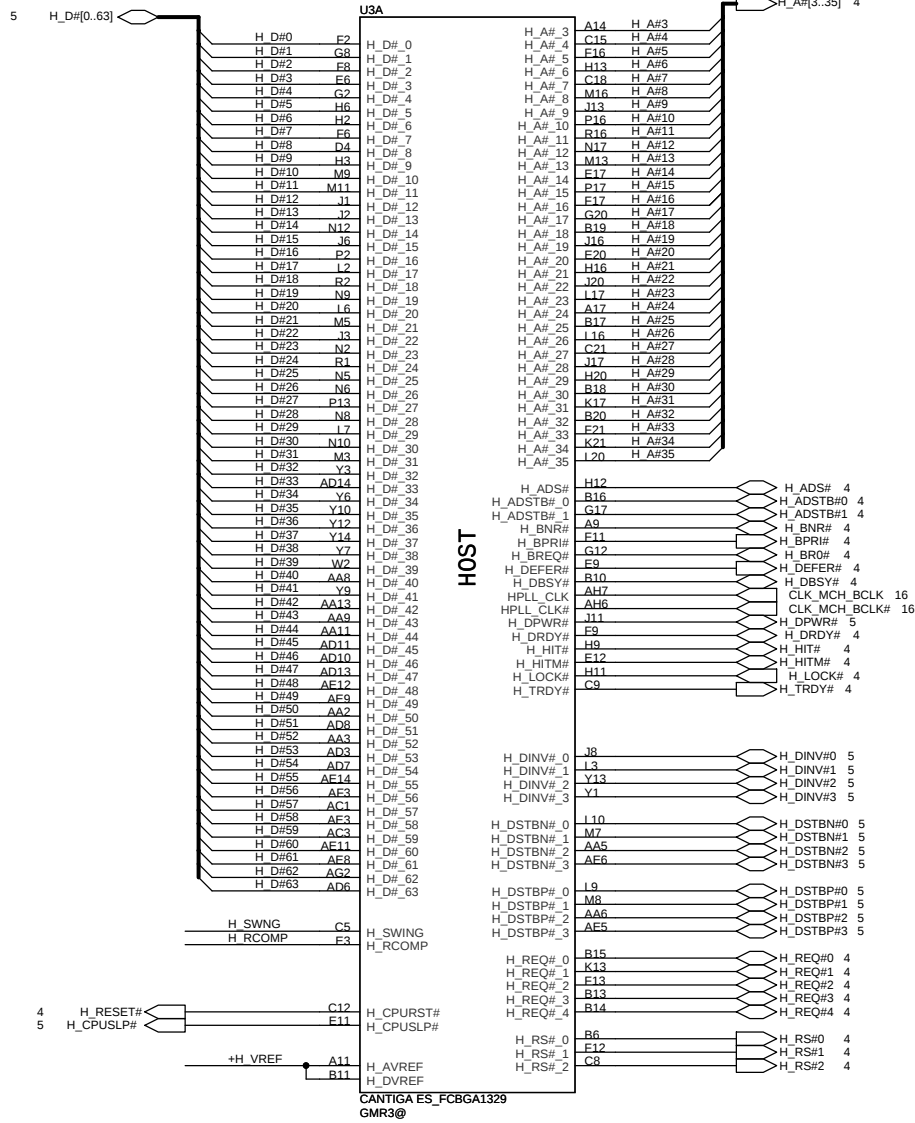
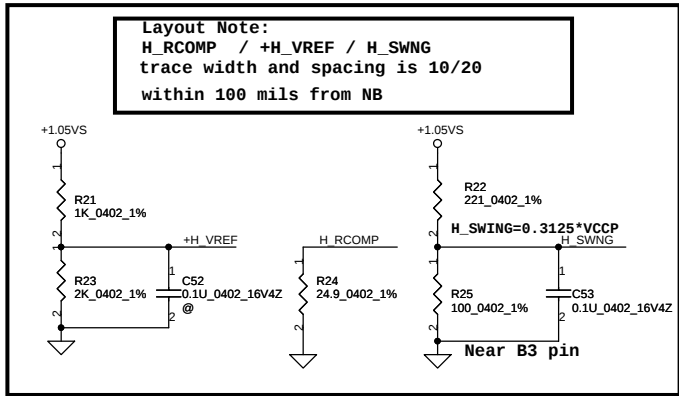
Mid Frequency Decoupling



Near pin B26



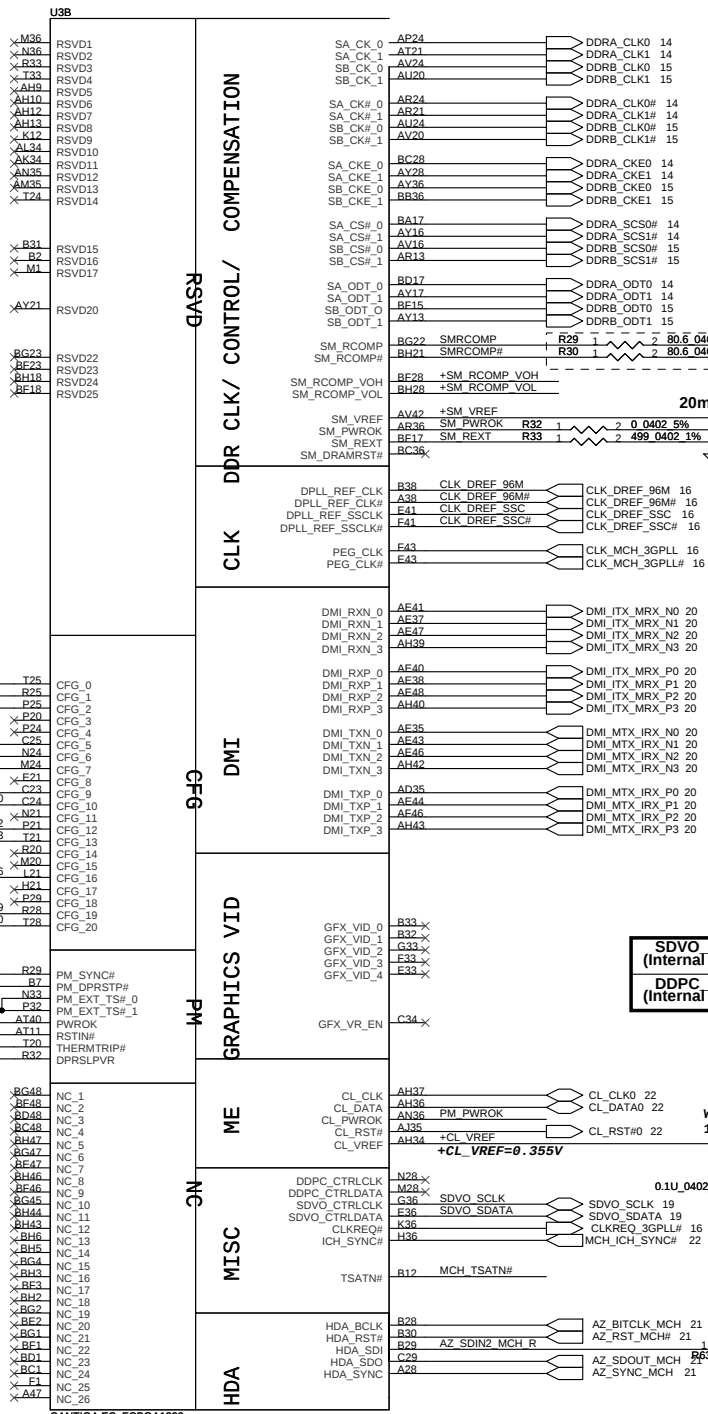
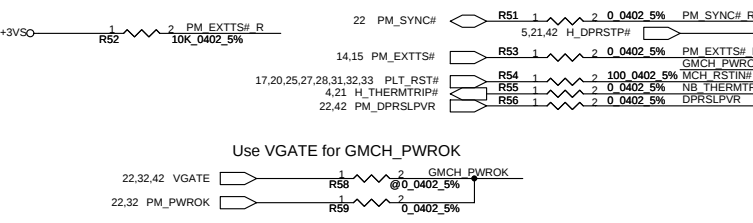
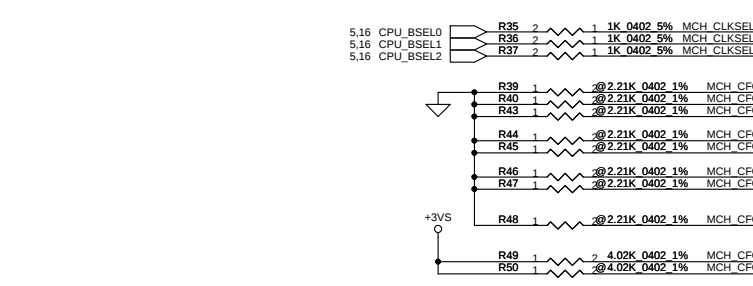
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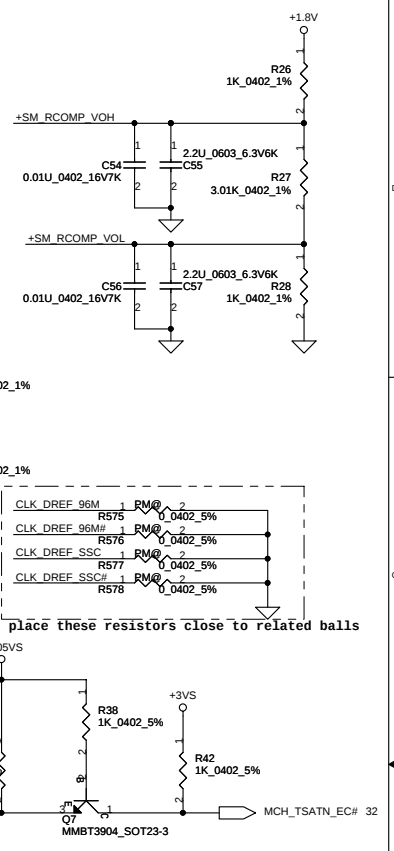
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Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5 Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6 Internal pull-up	0 = iTPM Host Interface is enabled can support disble by SW. 1 = iTPM Host Interface is Disabled *(Default)
CFG7 Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9 Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10 Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12] Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation*(Default)
CFG16 Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19 Internal pull-down	0 = Normal Operation 1 = DMI Lane Reversal Enable *(Default)
CFG20 Internal pull-down (PCIe/SDVO select)	0 = Only PCIe or [SDVO/DP/HDMI] is operational. *(Default) 1 = PCIe/[SDVO/DP/HDMI] are operating simu.



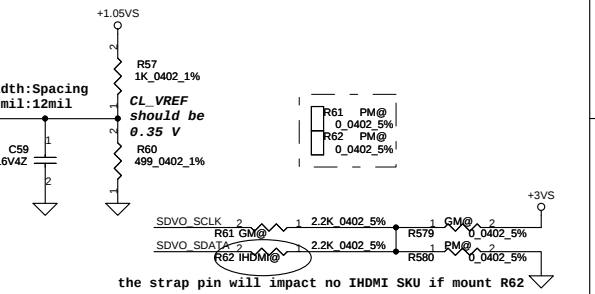
SM_DRAMRST# would be needed for DDR3 only
For Cantiga 80 Ohm



Lane reversal

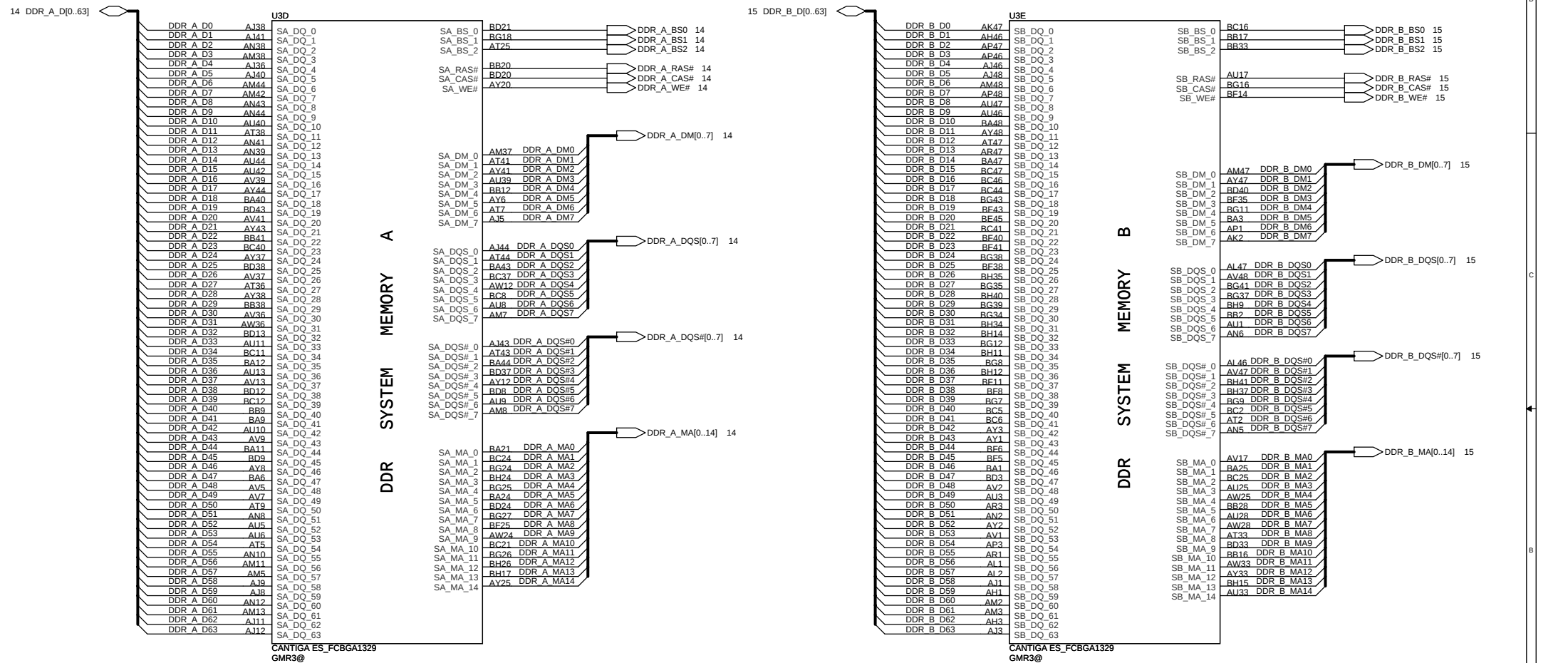
Strap Pin Table

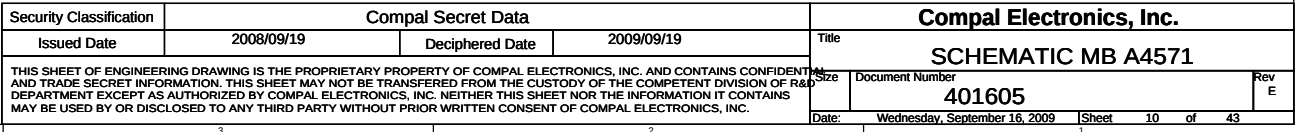
SDVO_CTRLDATA (Internal pull-down)	0 = SDVO interface disabled *(Default) 1 = SDVO interface enabled
DDPC_CTRLDATA (Internal pull-down)	0 = Digital display (iHDMI/DP) interface disabled 1 = Digital display (iHDMI/DP) interface enable*(Default)

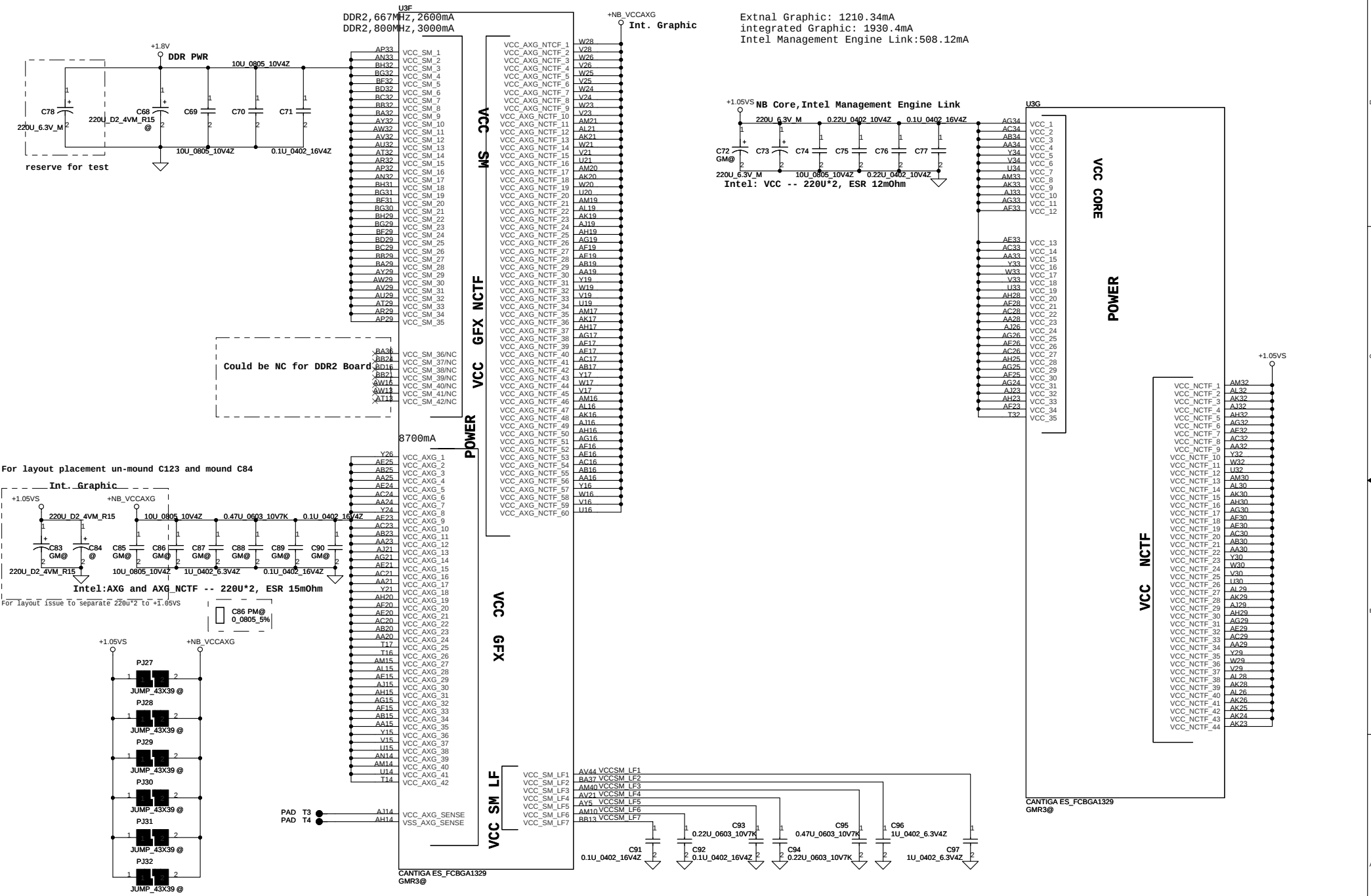


CANTIGA ES_FCBGA1329
GMR3@

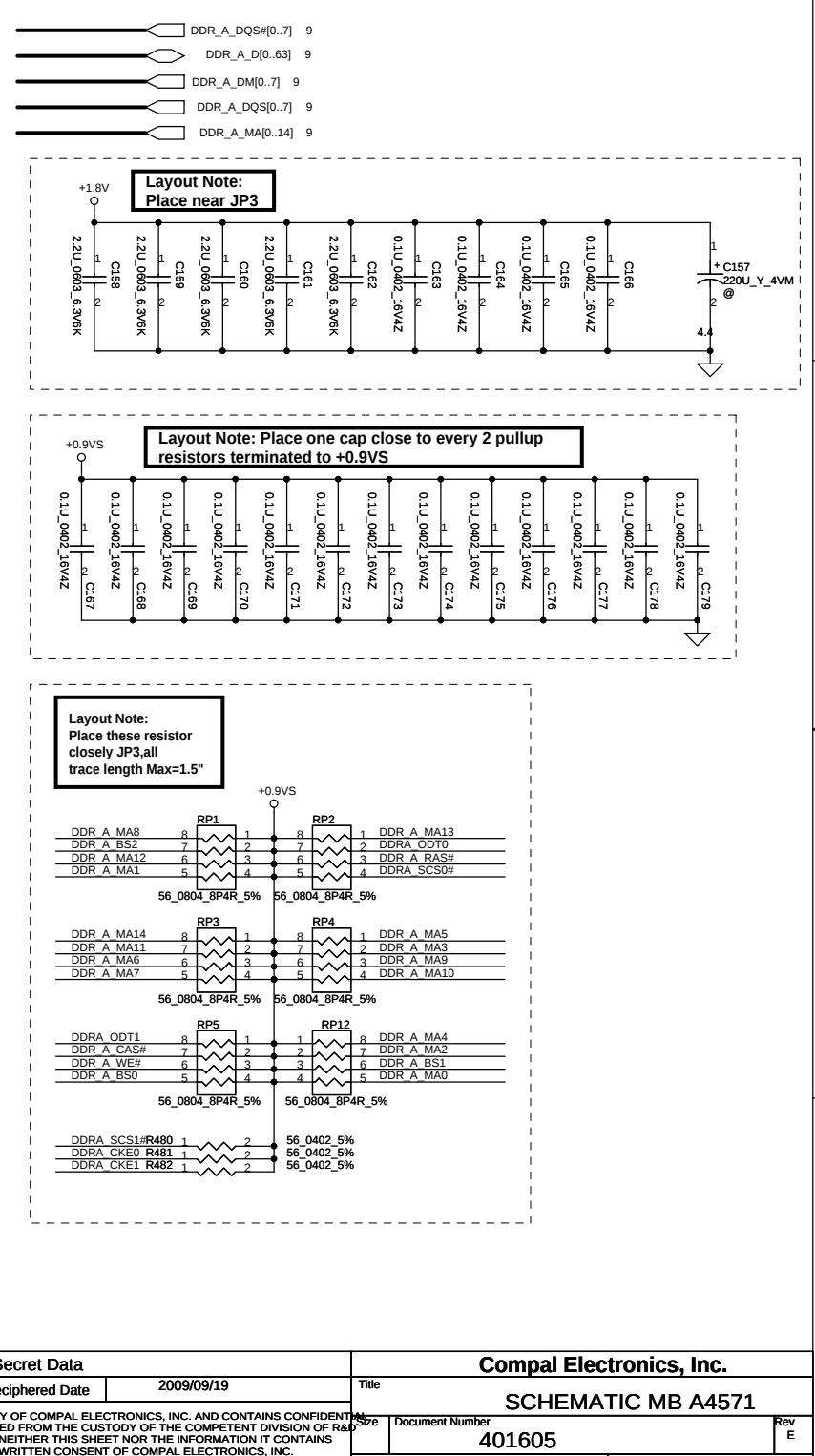
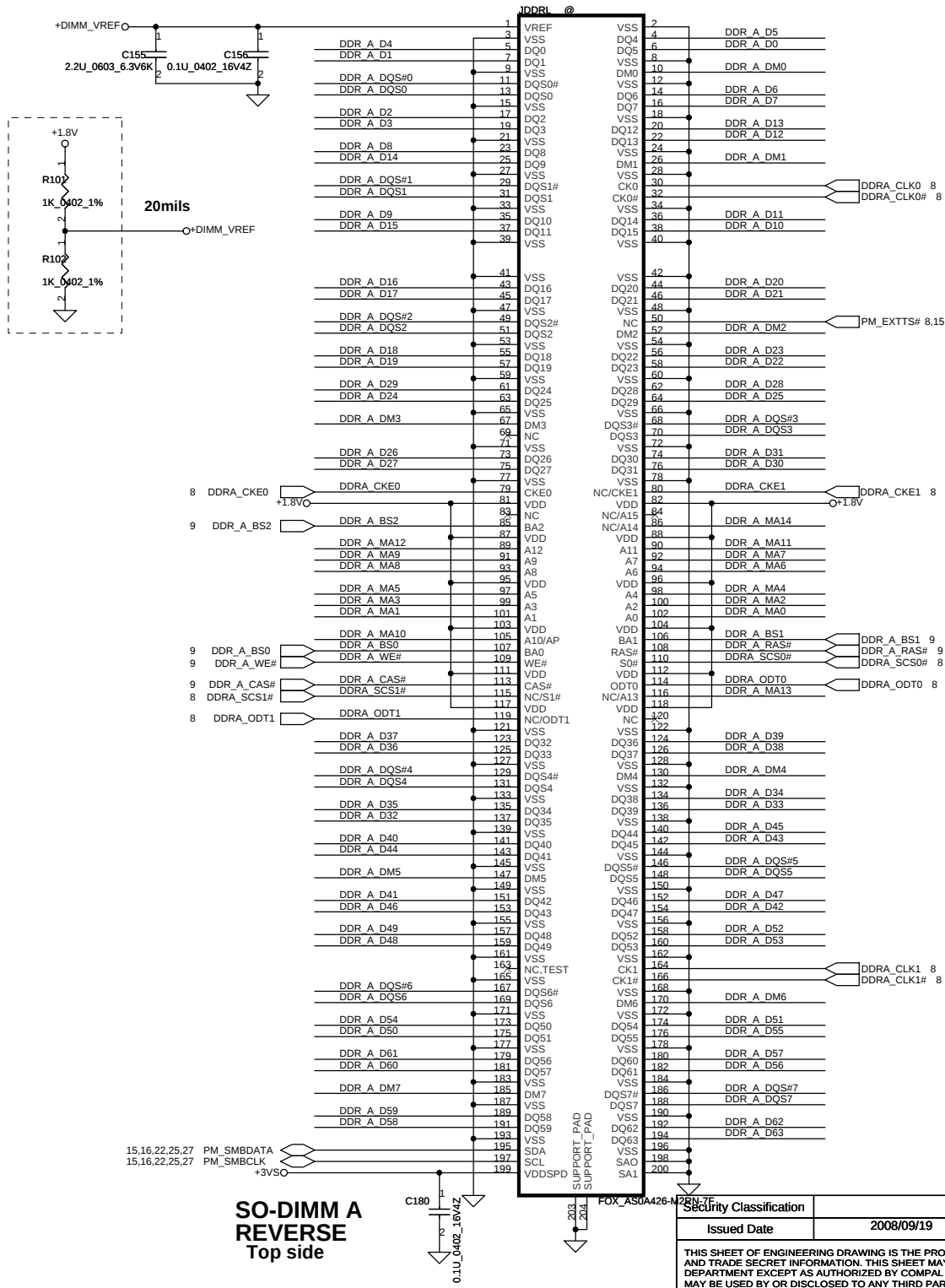
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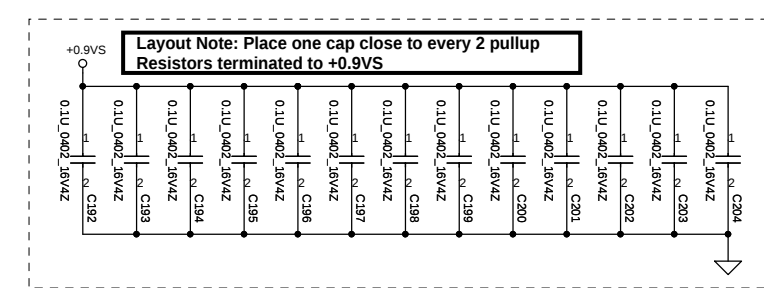
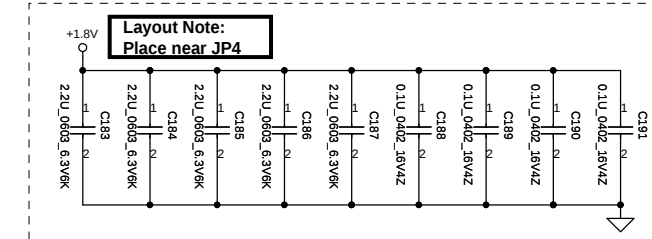
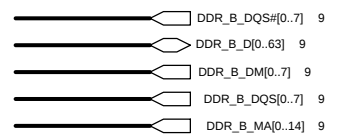
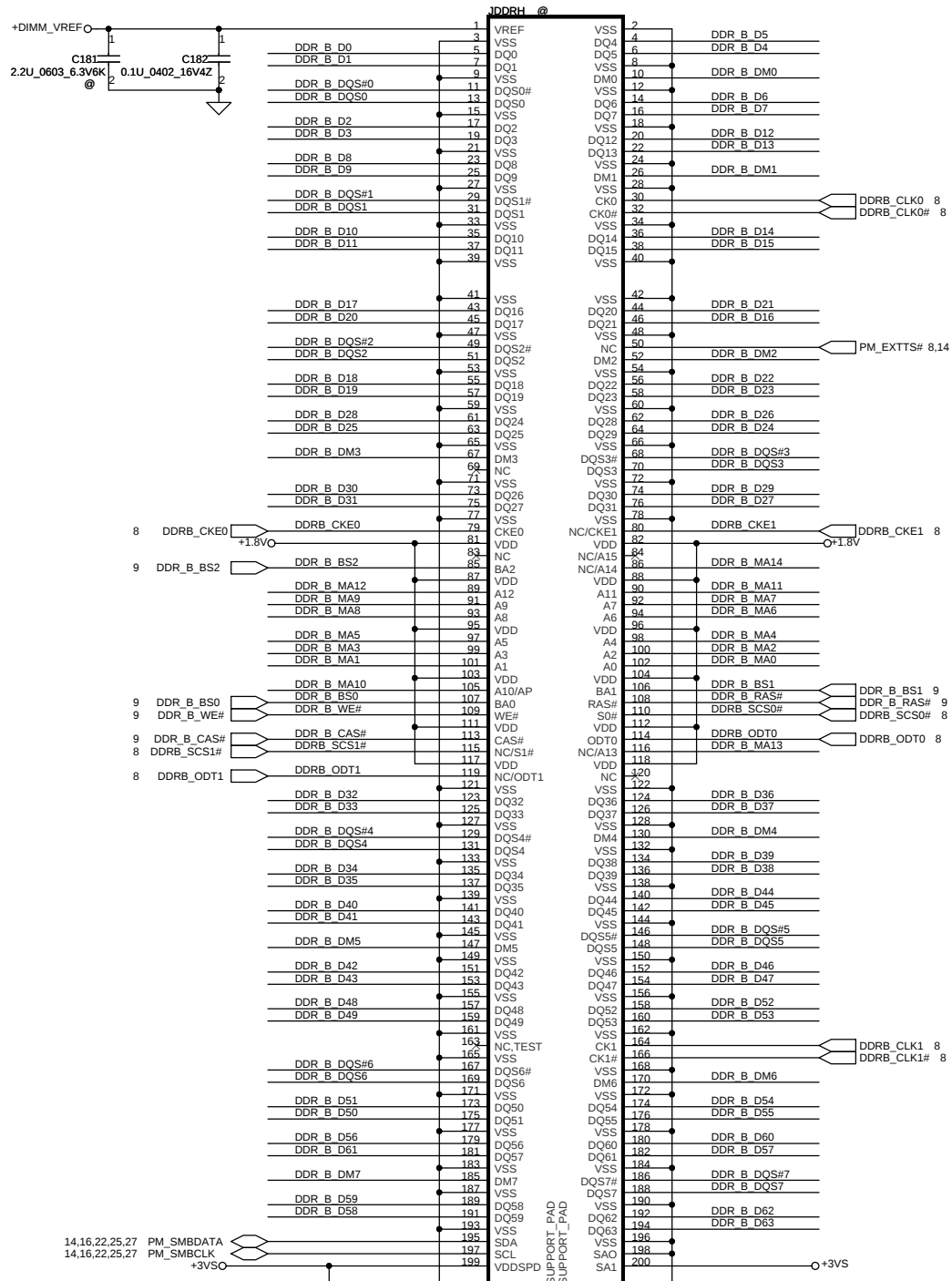
Layout Note:
Place near JP3

Layout Note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

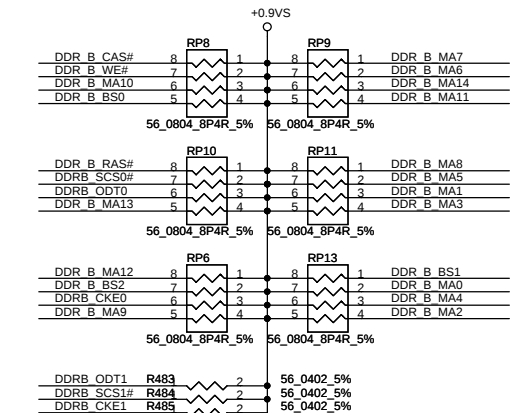
Layout Note:
Place these resistor closely JP3,all trace length Max=1.5"

SO-DIMM A
REVERSE
Top side

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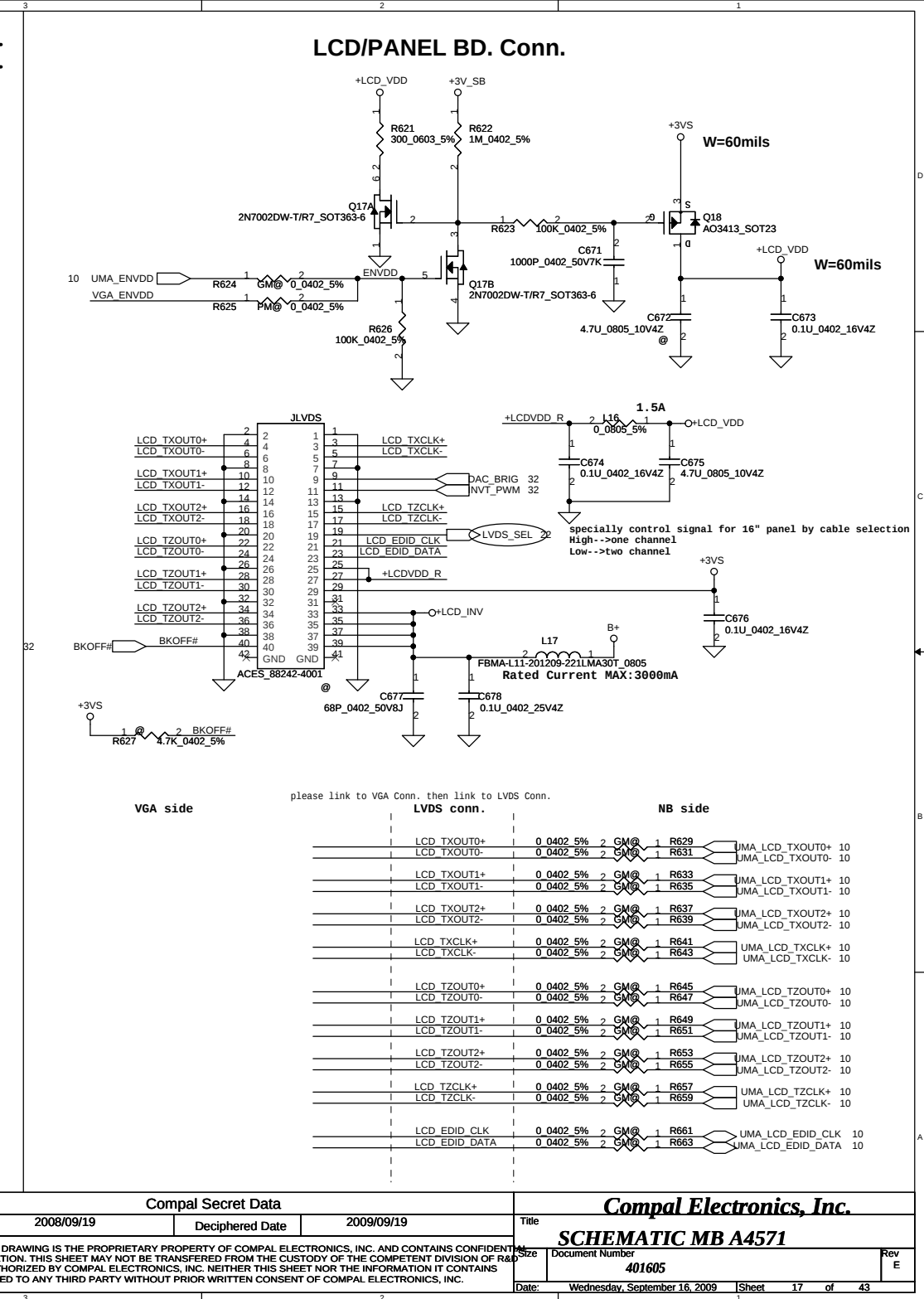
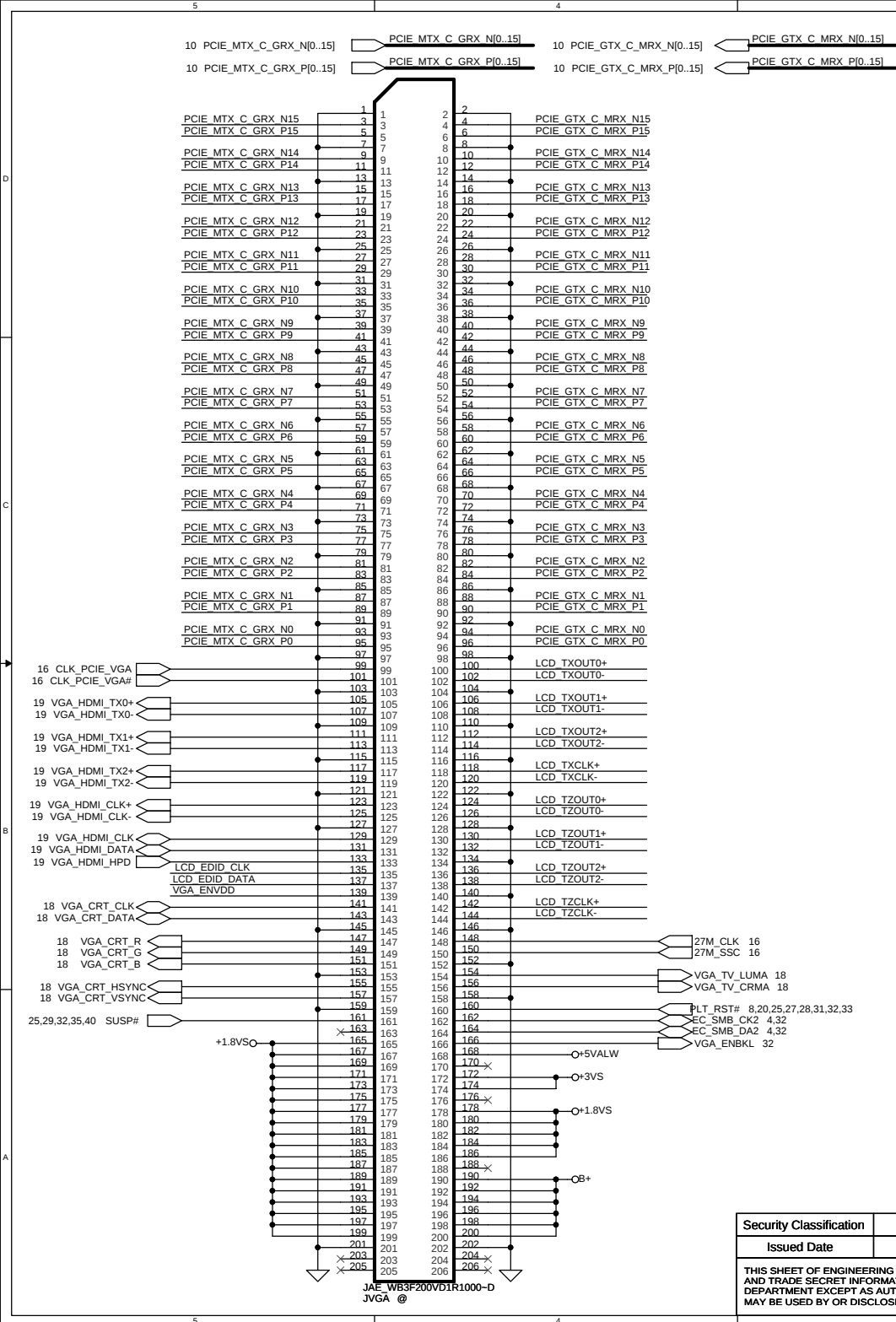


Layout Note:
Place these resistor
closely JP4,all
trace length Max=1.5"

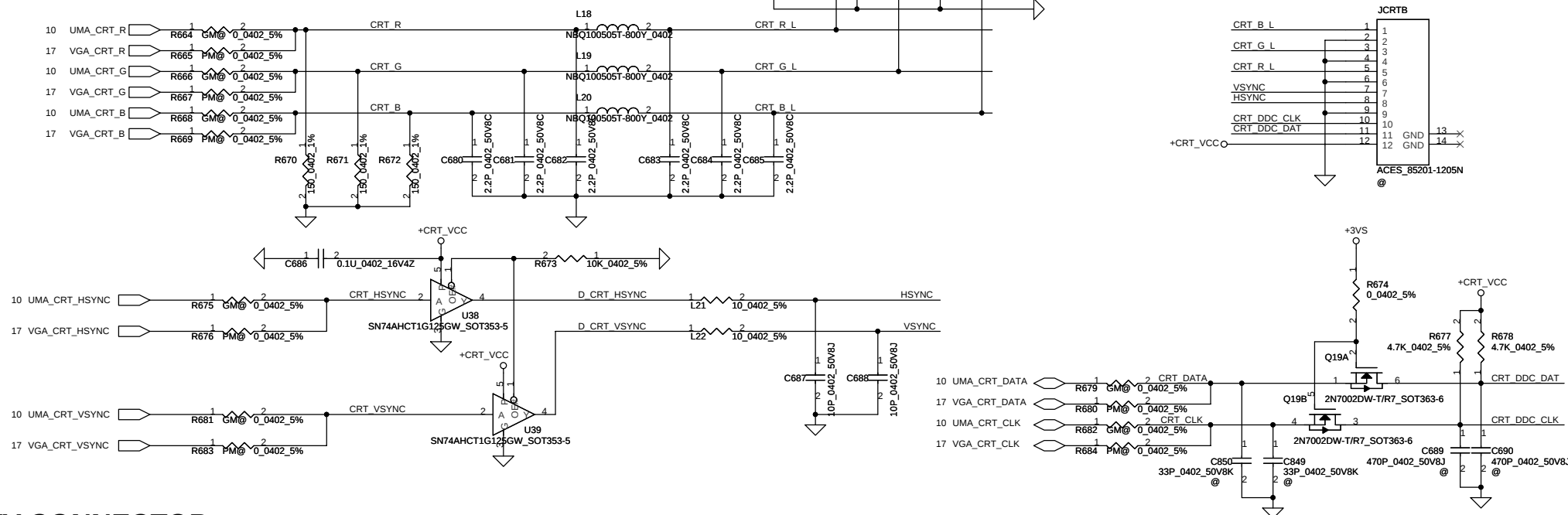


SO-DIMM B
STANDARD
Bottom side

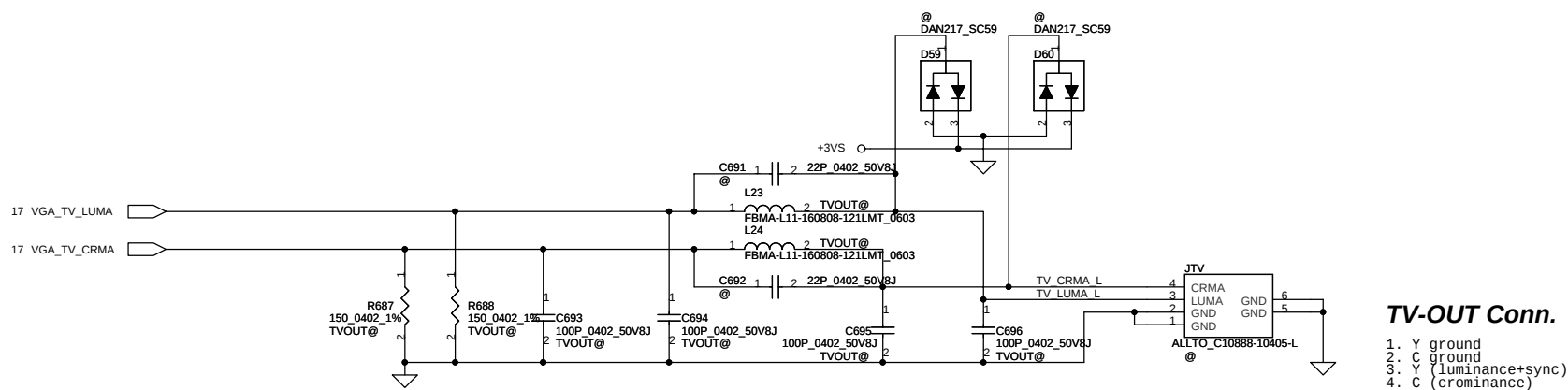
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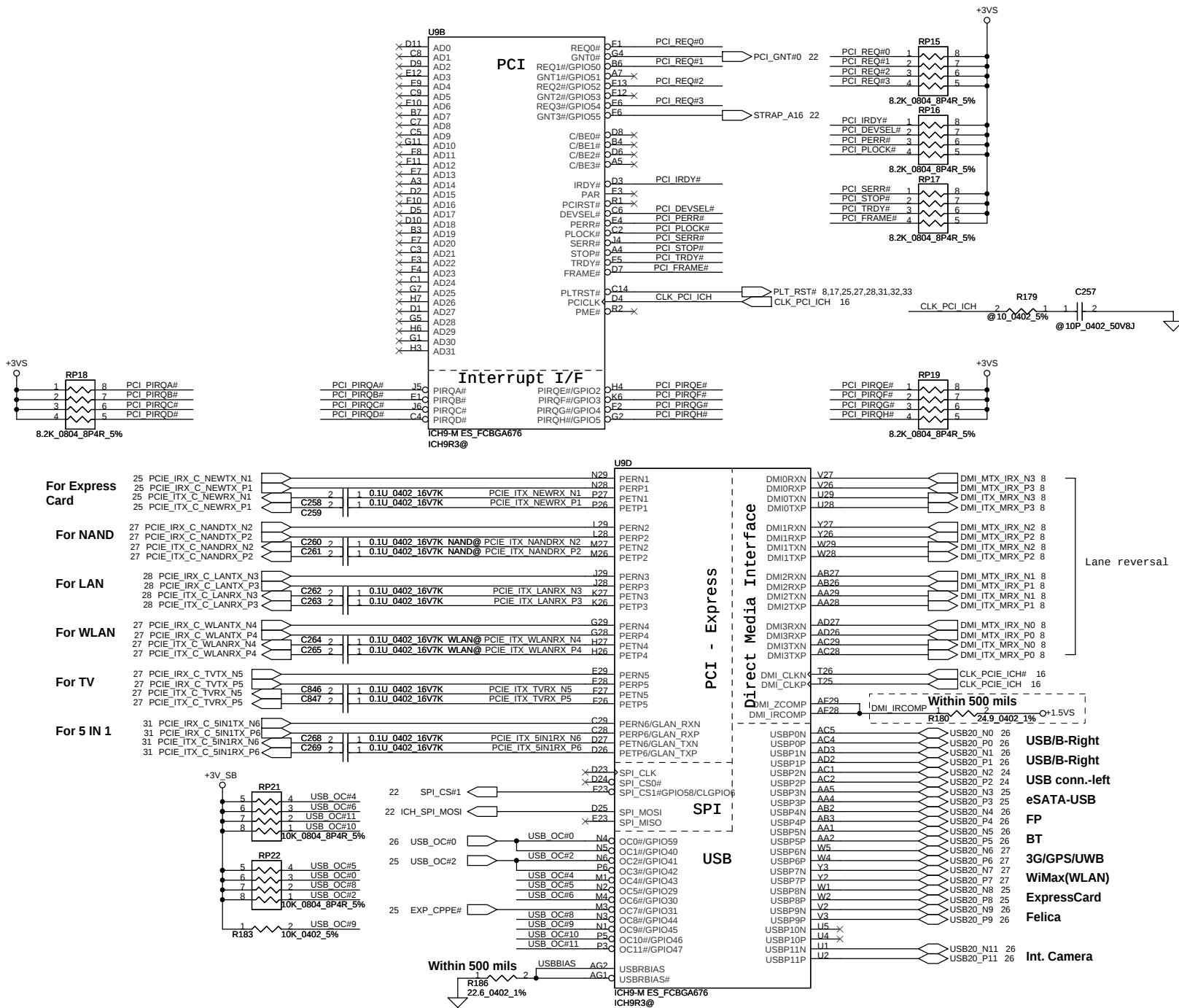
CRT CONNECTOR



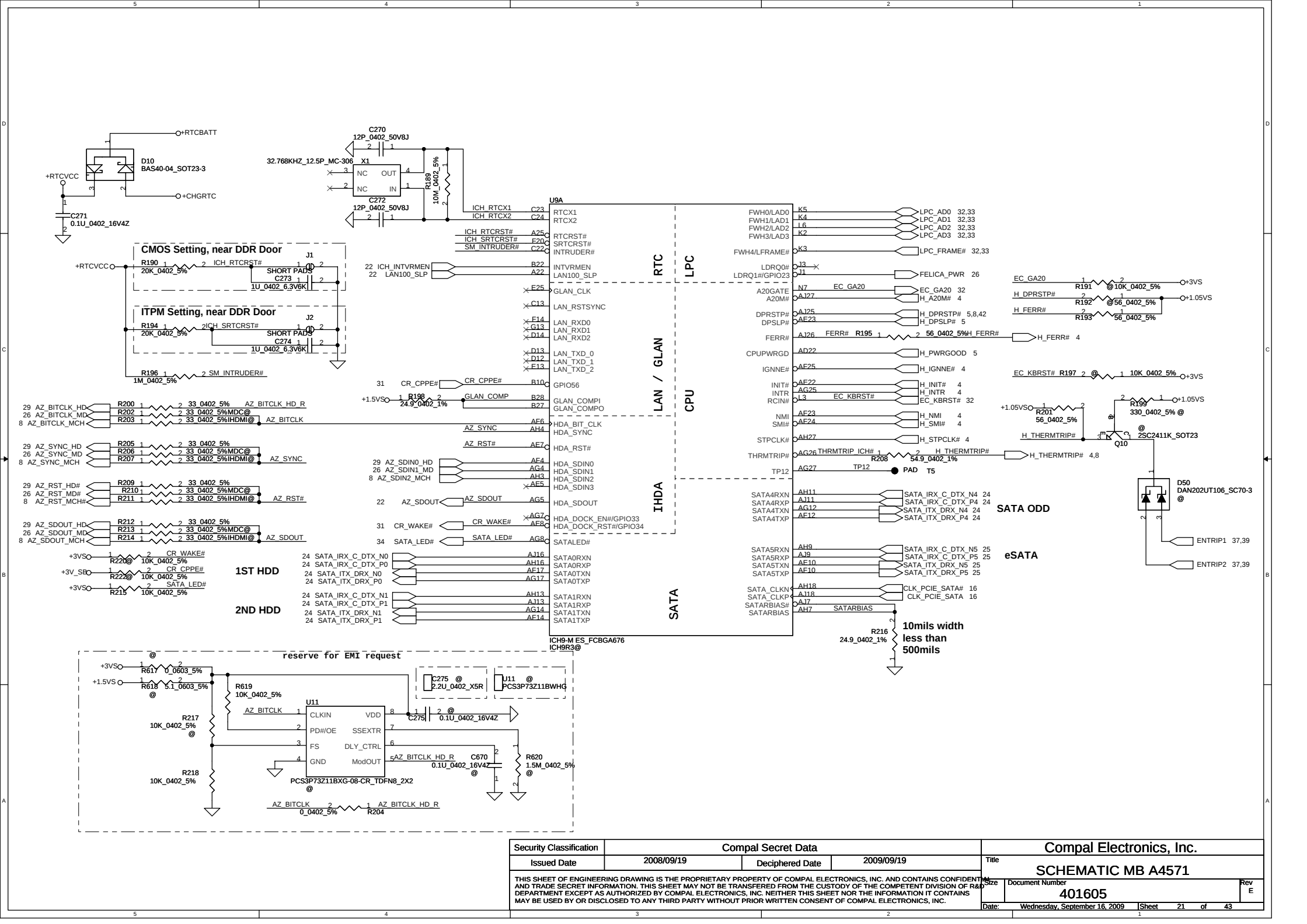
TV CONNECTOR

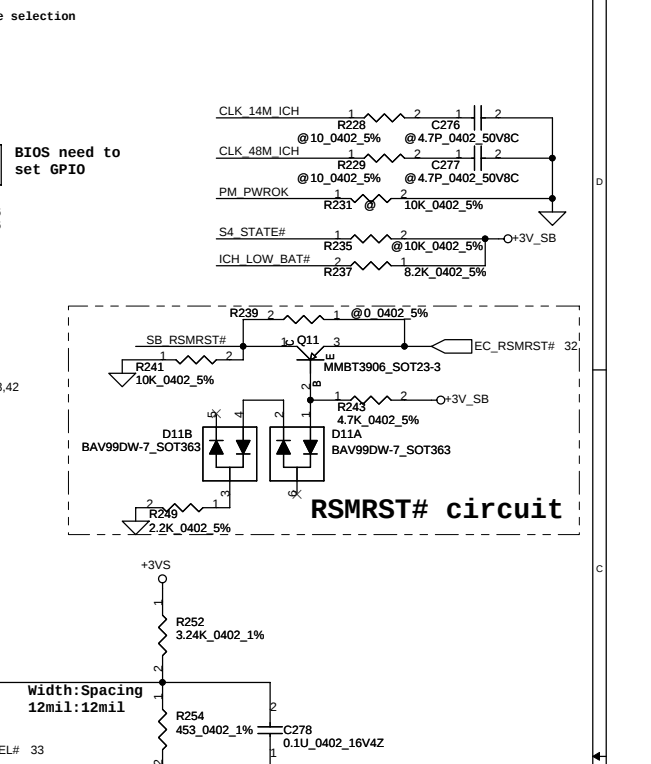
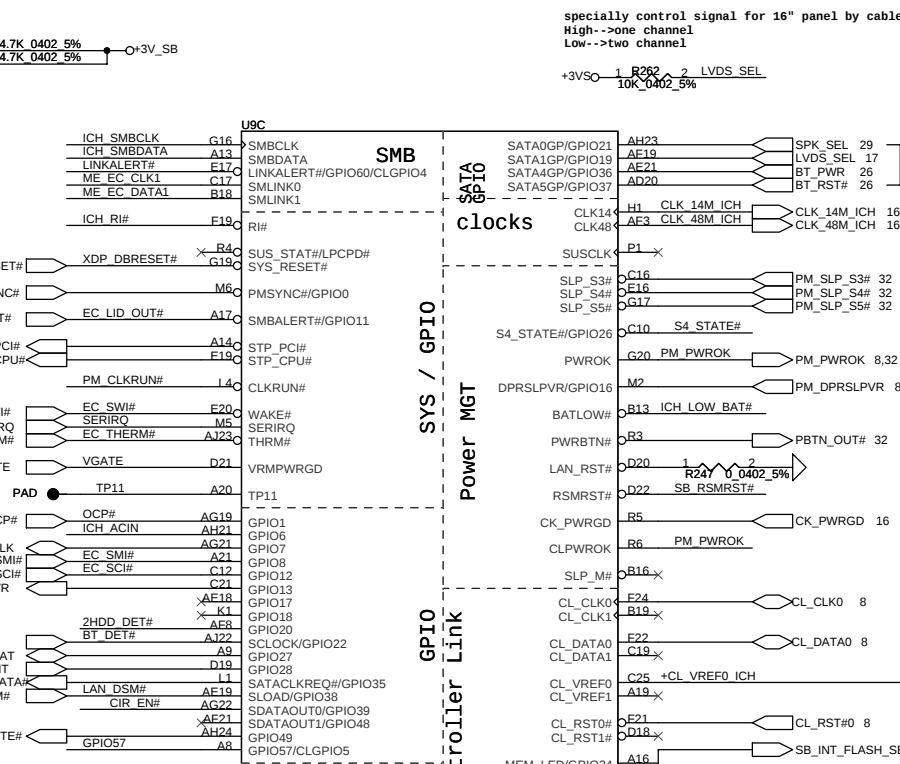
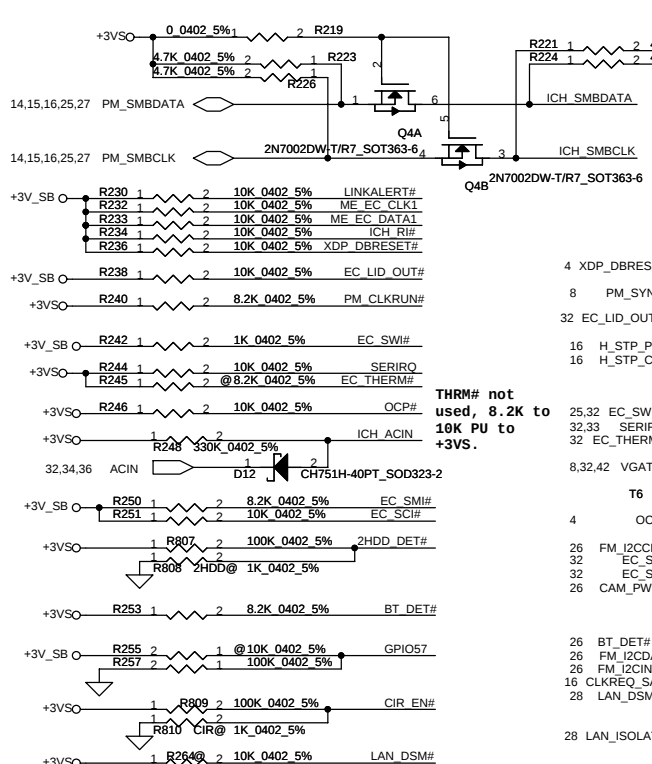


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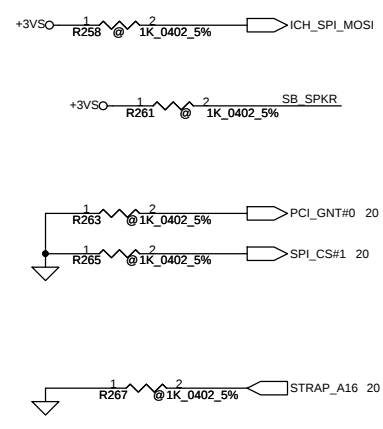
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iTPM Physical Presence	
CLGPIO5	Assert = iTPM Physical Presence Enable
Mobil Platform	De-assert = iTPM disable
	**Only used in iAMT w/ME Firmware
GPIO57	Desktop Platform used only

ICH9M Strap Pin

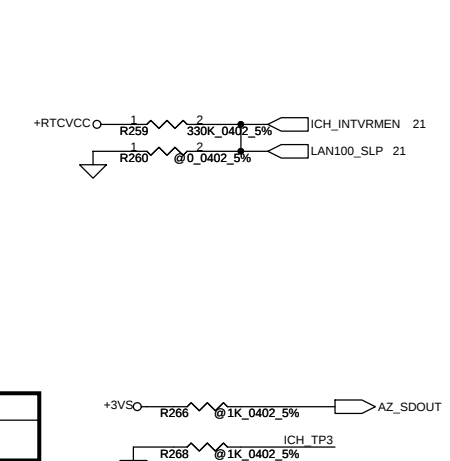


Internal TPM Strap (Internal pull-down)	
SPI_MOSI	Low= Disable High= iTPM enable by MCH strap*

No Reboot Strap (Internal pull-up)	
SB_SPKR	Low= *Default High= "No Reboot"

Boot BIOS Strap (Internal pull-up)		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	0	RESERVED
0	1	SPI
1	0	PCI
1	1	LPC* (Default)

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default* (Internal pull-up)



Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

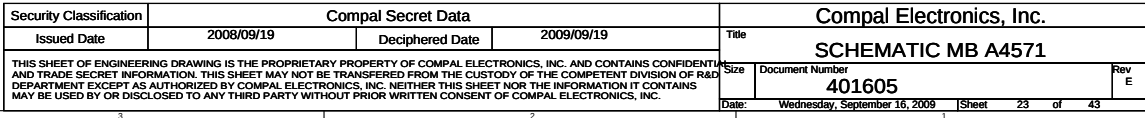
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

Flash Descriptor Security Override Strap	
GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

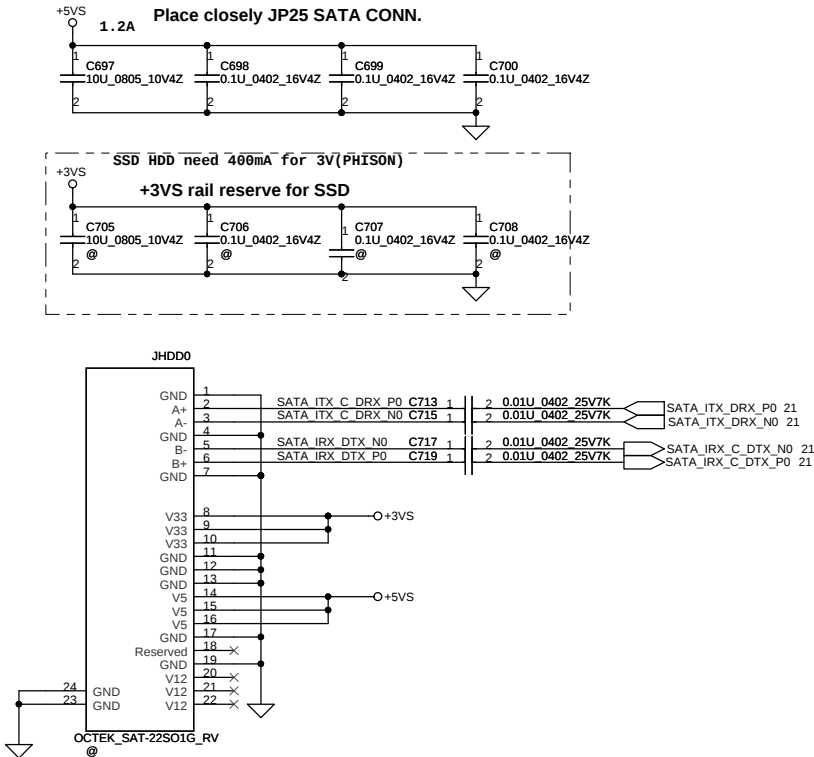
DMI Termination Voltage	
GPIO49	Low= Desktop used High= Mobile* (Internal pull-up)

XOR Chain Entrance Strap		
ICH_TP3 (Internal pull-up)	HDA_SDOUT (Internal pull-down)	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

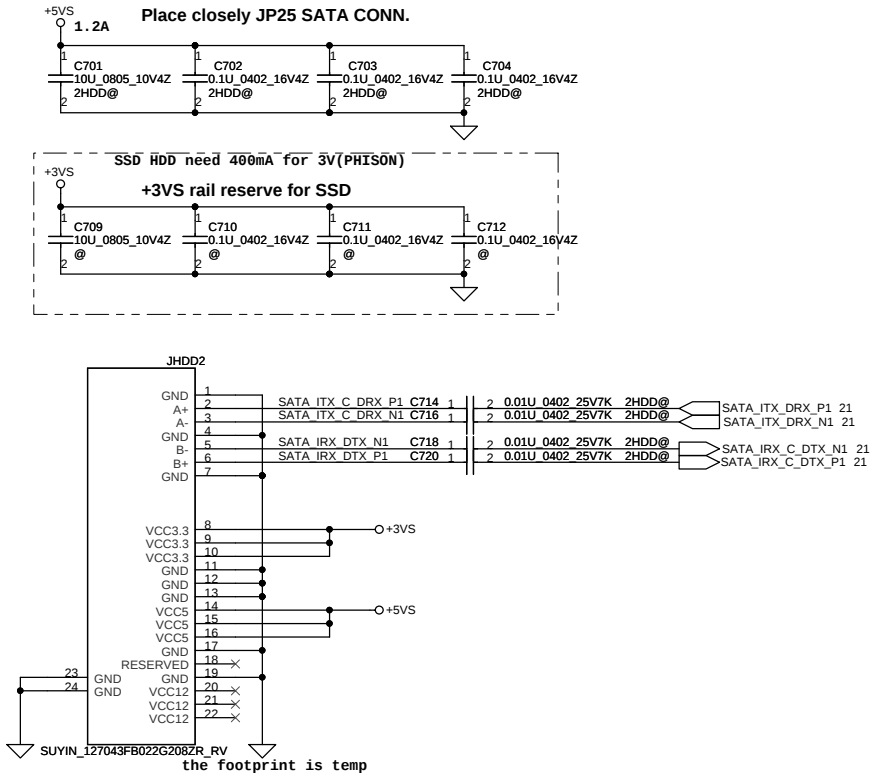
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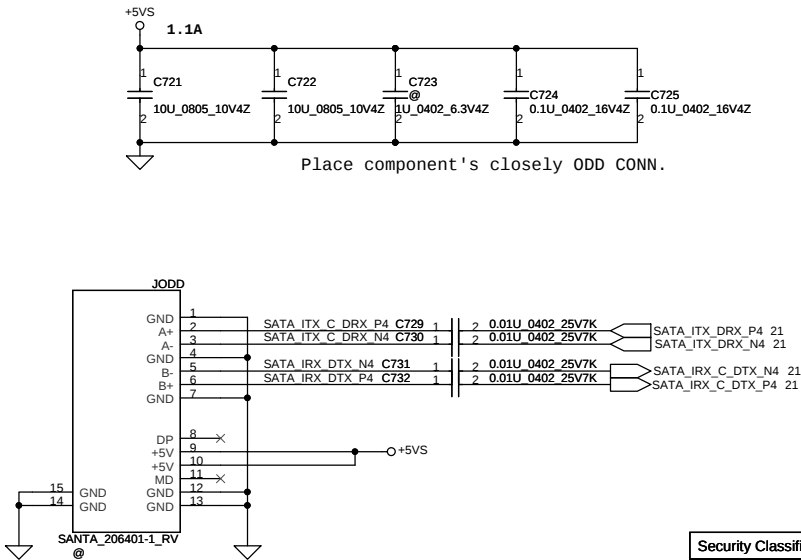
SATA HDD1 Conn.



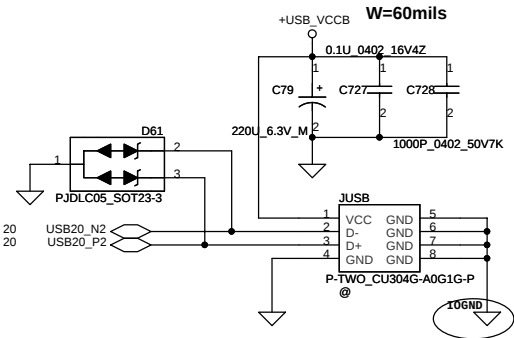
SATA HDD2 Conn.



SATA ODD Conn

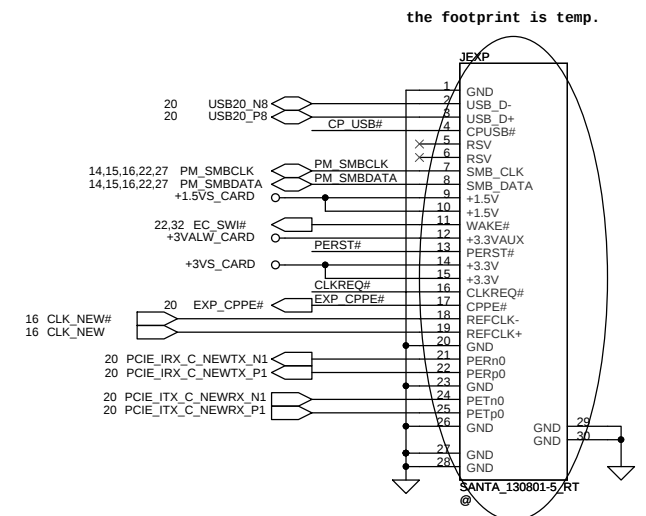
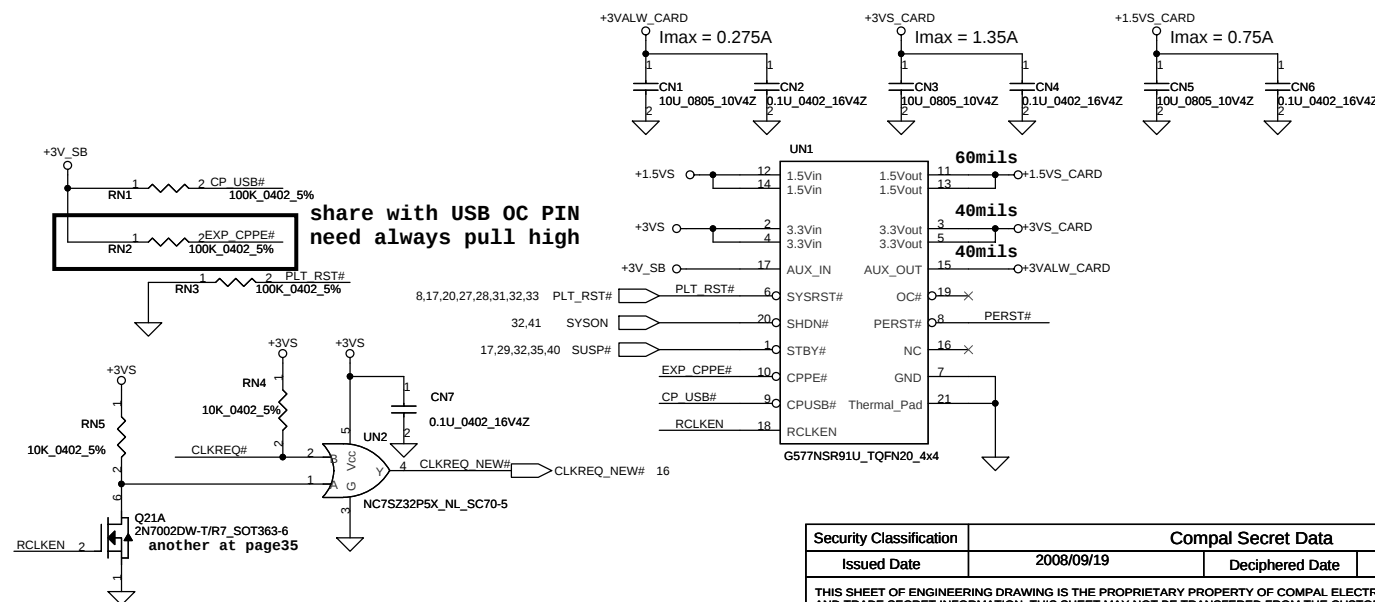
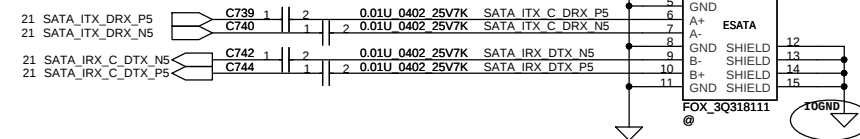
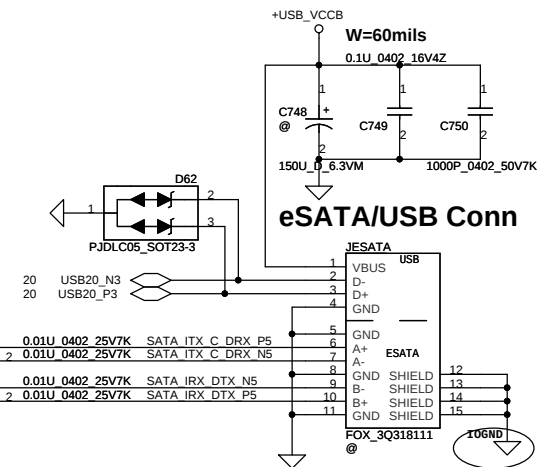
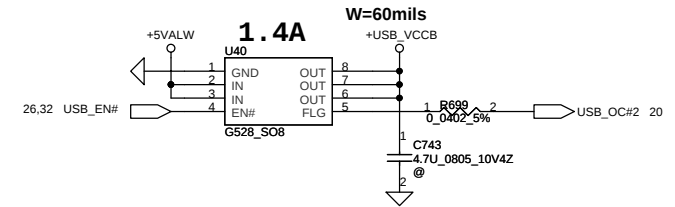


USB Conn.



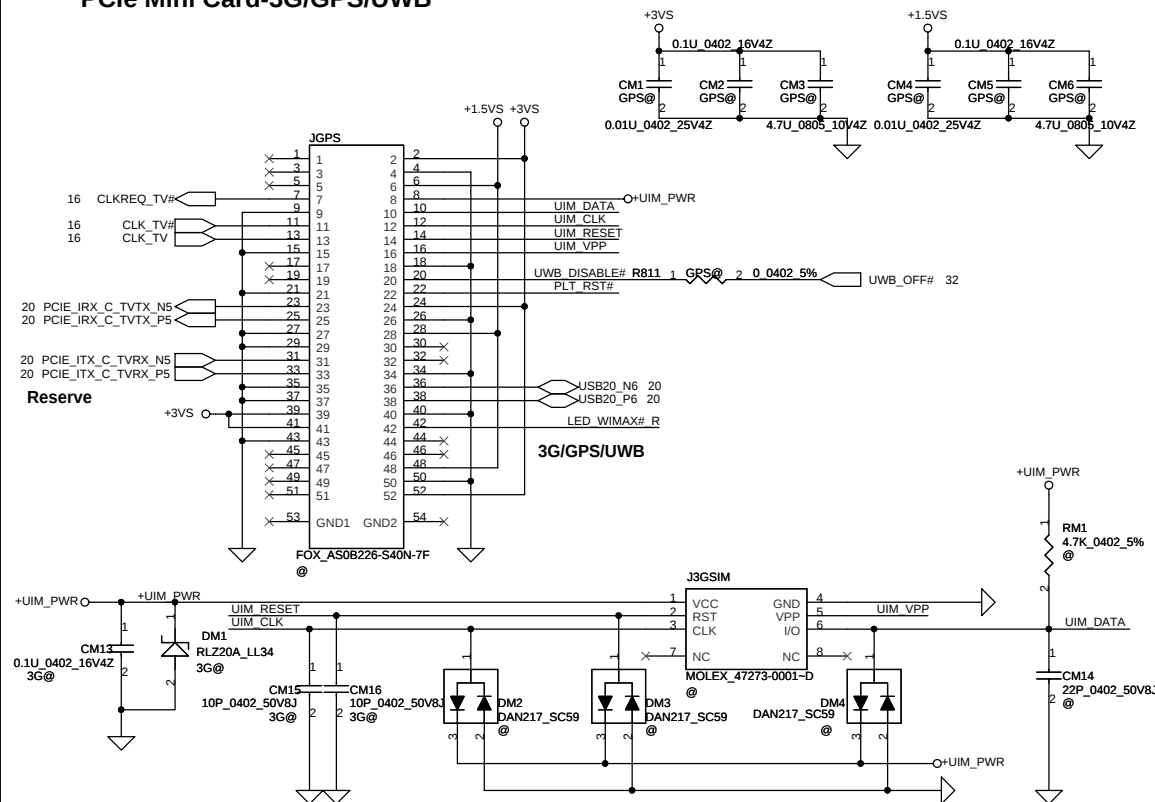
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eSATA/USB

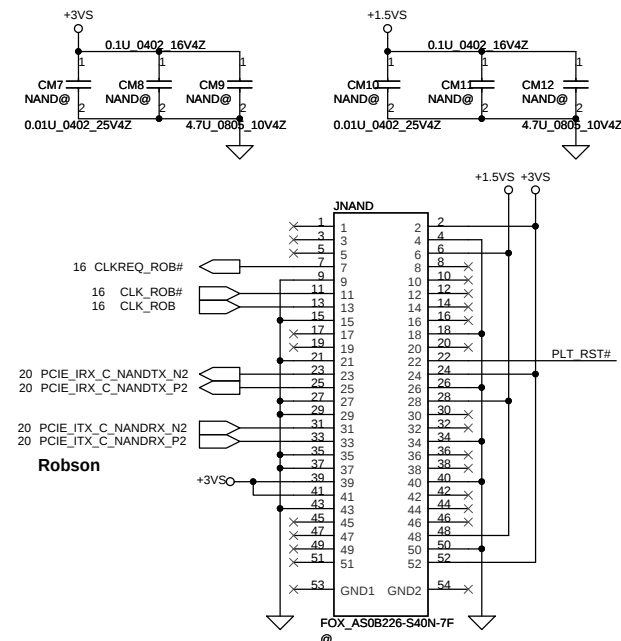


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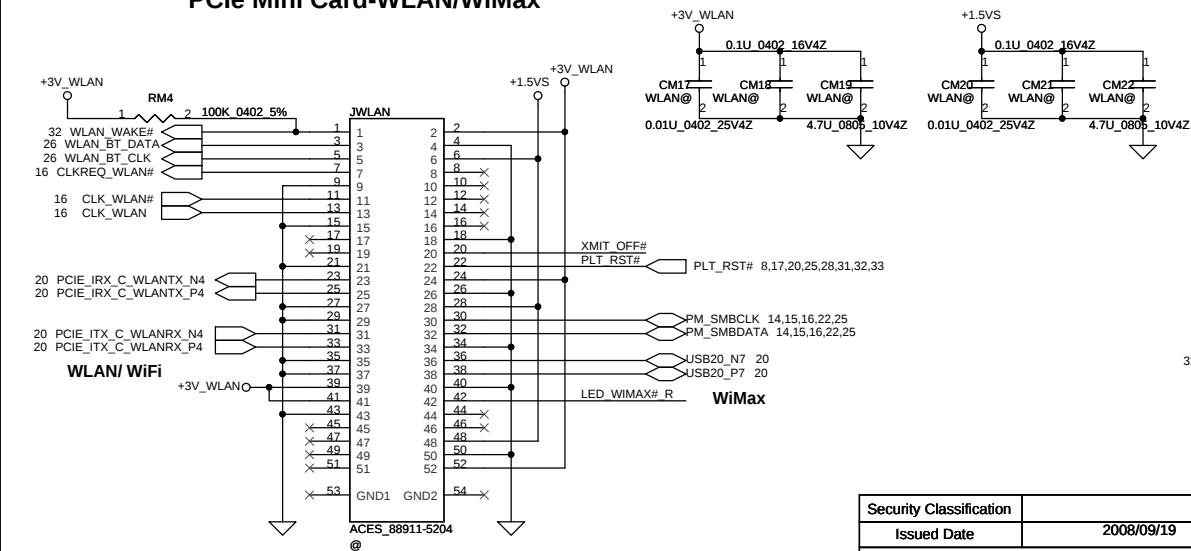
PCIe Mini Card-3G/GPS/UWB



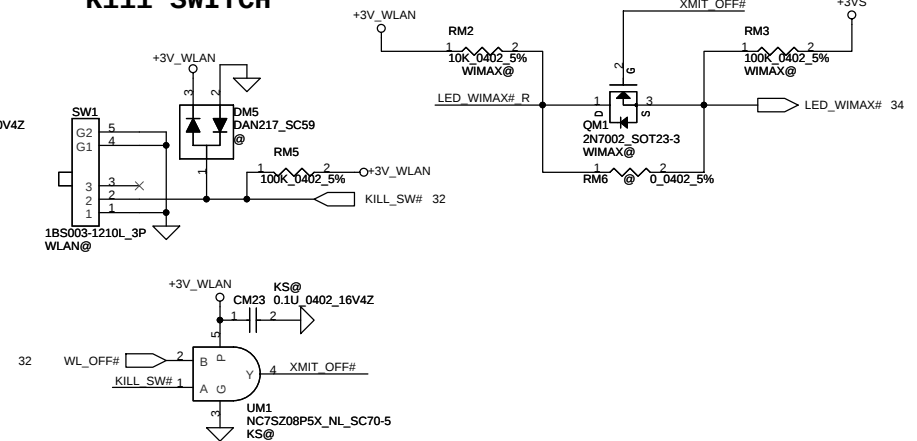
PCIe Mini Card-Robson



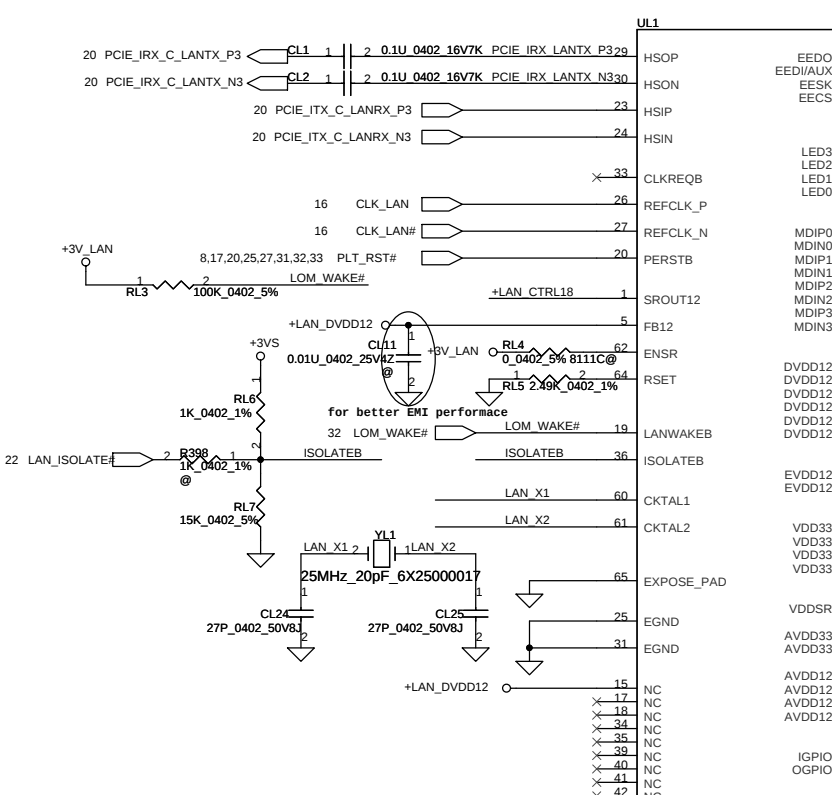
PCIe Mini Card-WLAN/WiMax



Kill SWITCH

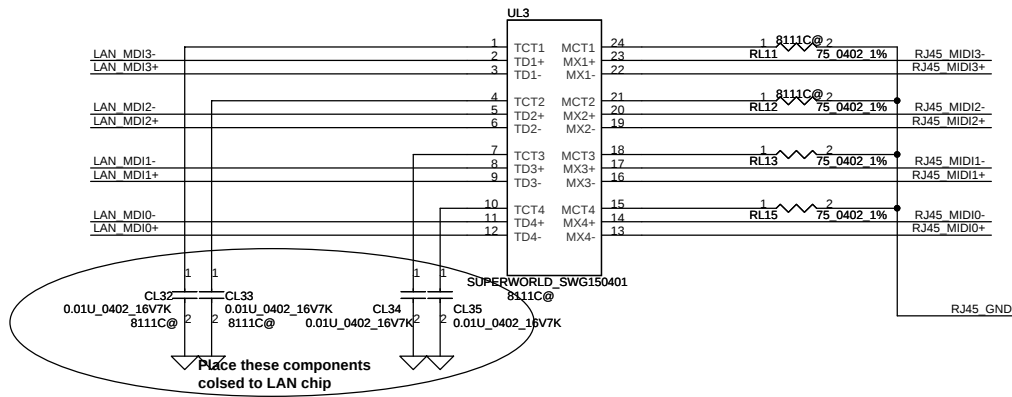


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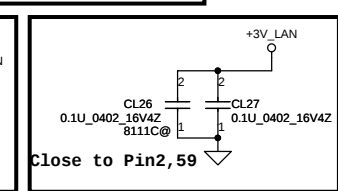
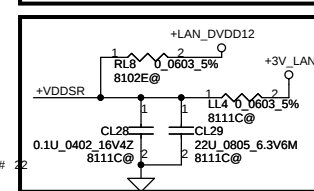
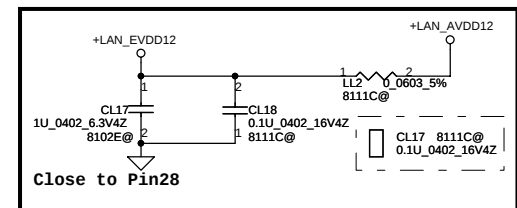
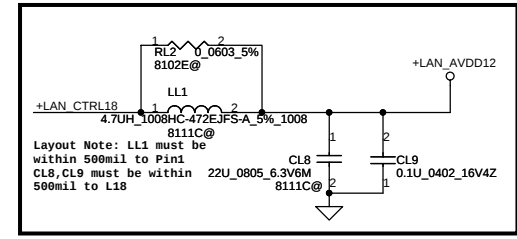
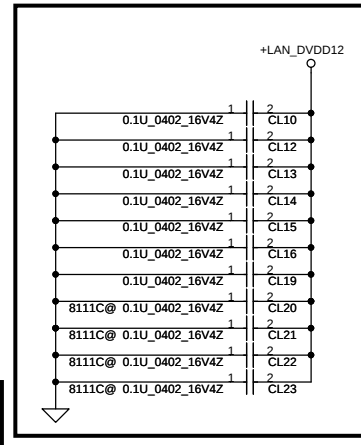
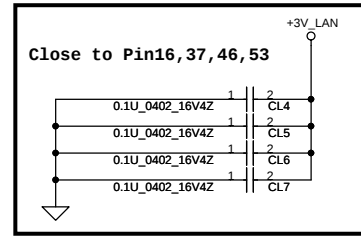


pin assignments table for difference

Pin	8111C	8102E
1	SROUT12	CTRL12A
5	FB12	NC
8	AVDD12	NC
9	MDIP2	NC
10	MDIN2	NC
11	AVDD12	NC
12	MDIP3	NC
13	MDIN3	NC
14	AVDD12	NC
15	NC	DVDD12
22	EVDD12	NC
32	DVDD12	NC
52	DVDD12	NC
58	AVDD12	DVDD12
59	AVDD33	NC
62	ENSR	NC
63	VDDSR	CTRL12D

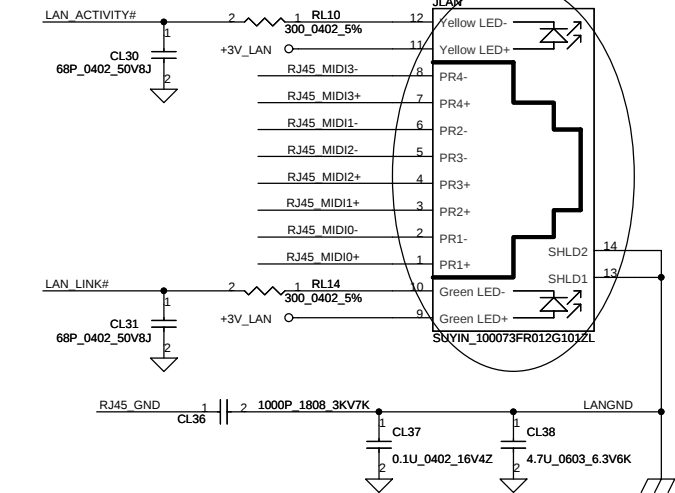


Place these components coiled to LAN chip



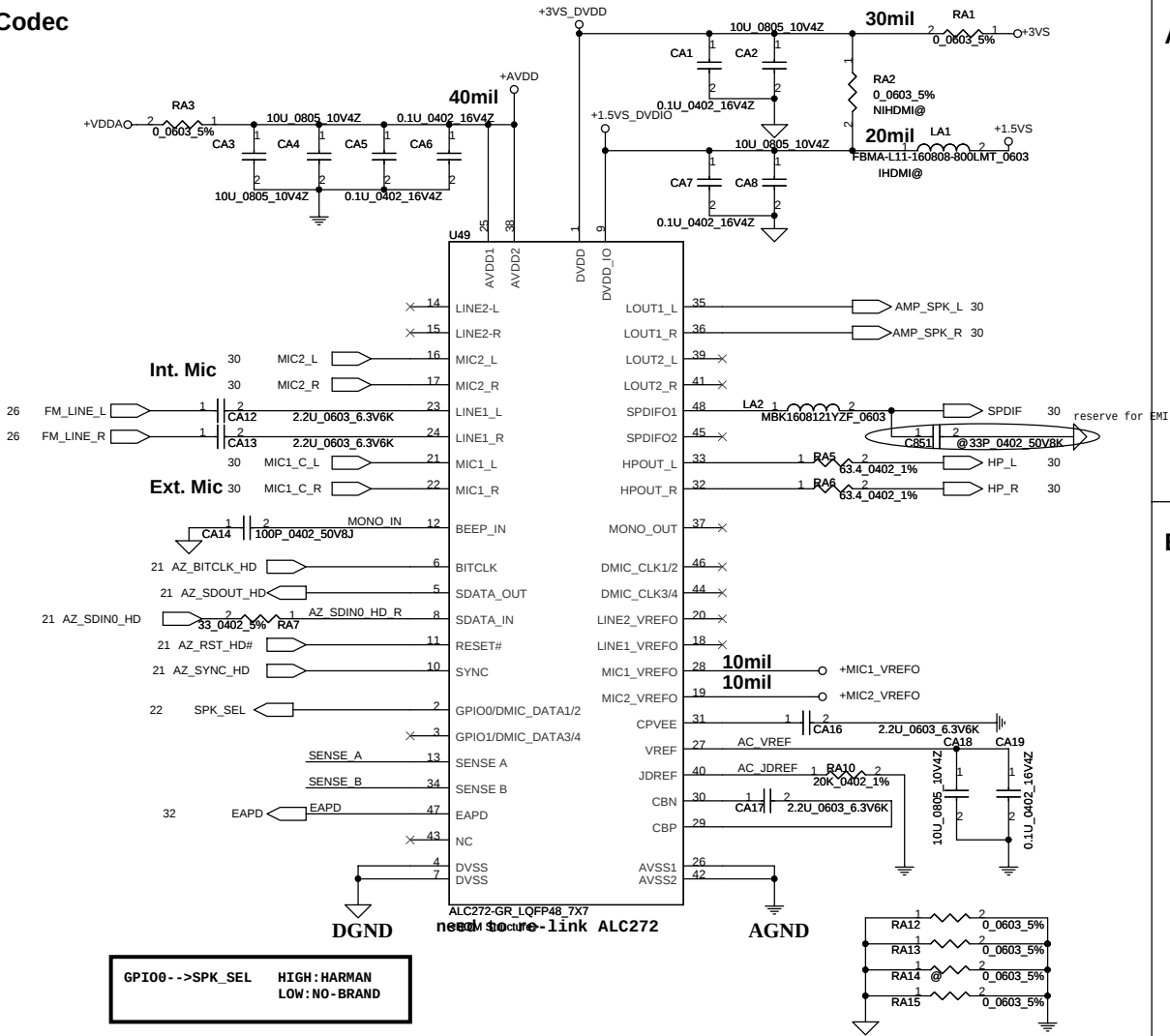
LAN Conn.

the footprint is tamp.

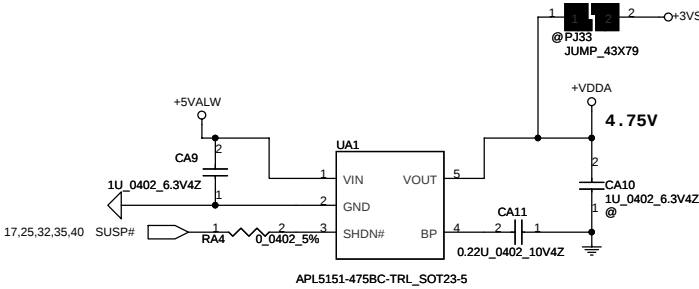


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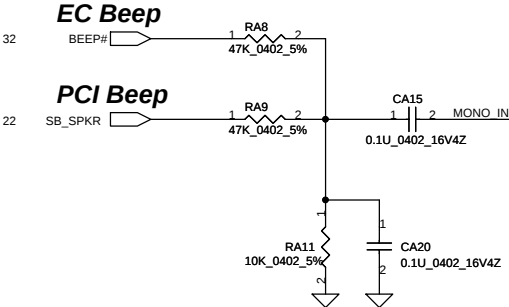
Codec



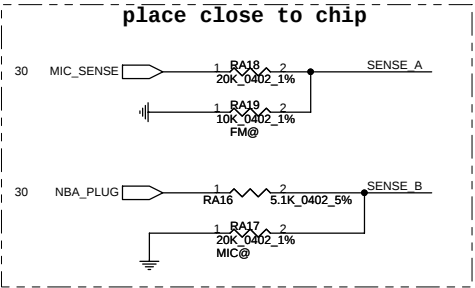
Audio regulator



Beep sound

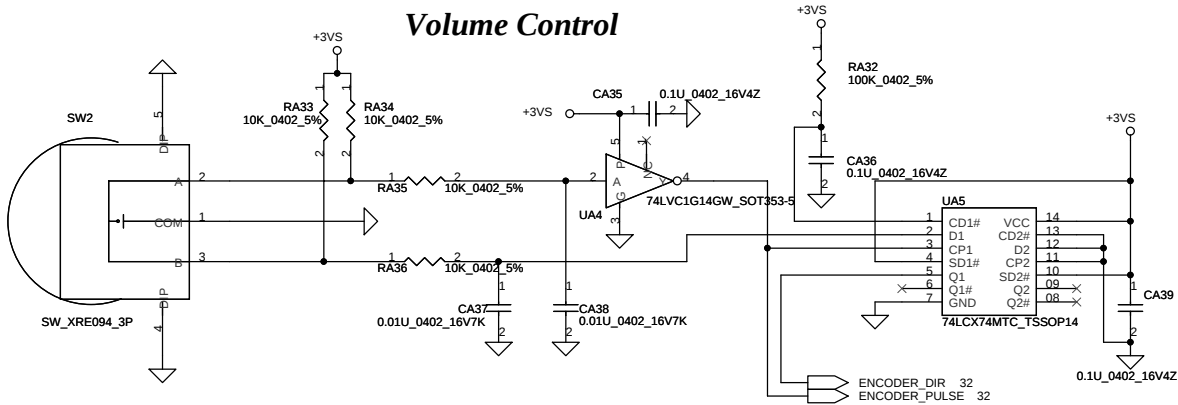
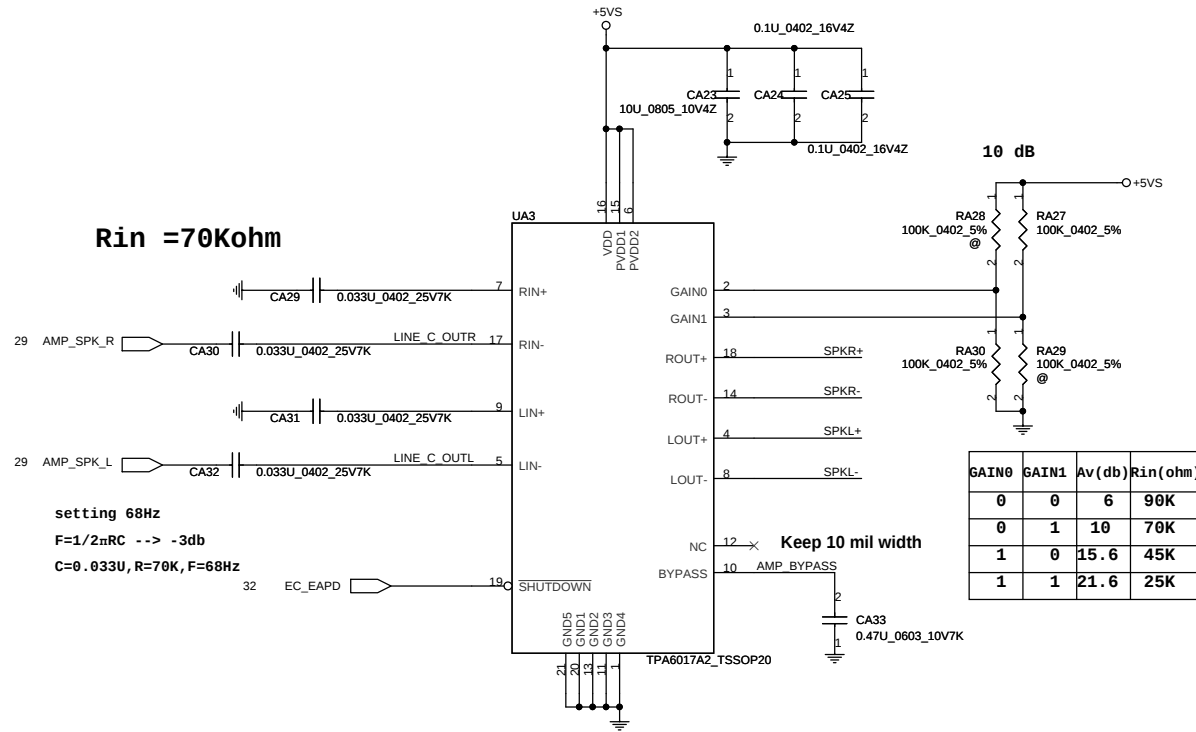


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	FM tuner
SENSE B	5.1K	PORT-D (PIN 35, 36)	SPK out
	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out

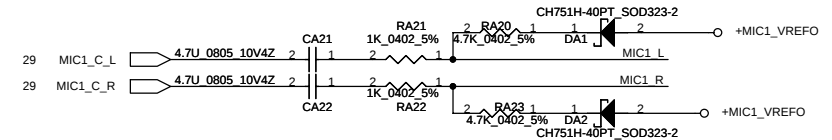


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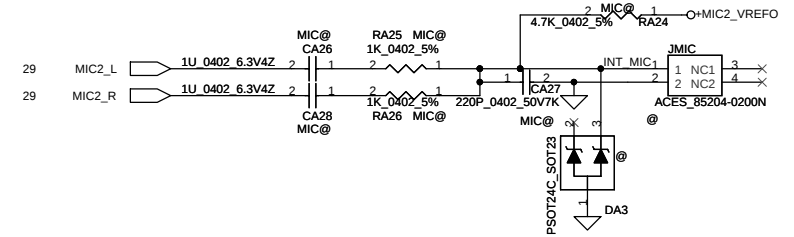
TPA6017 Medium Range Amplifier



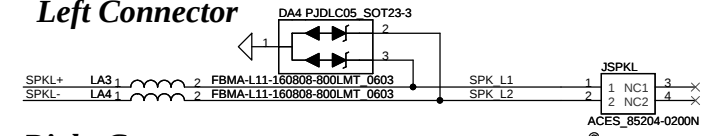
Ext. Mic



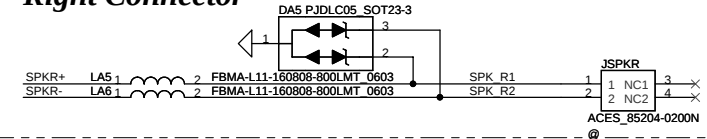
Int. Mic



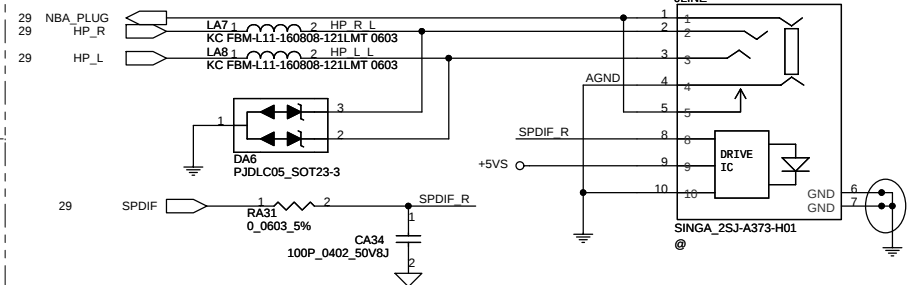
Left Connector



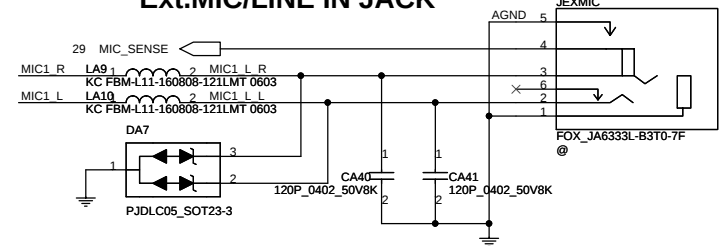
Right Connector



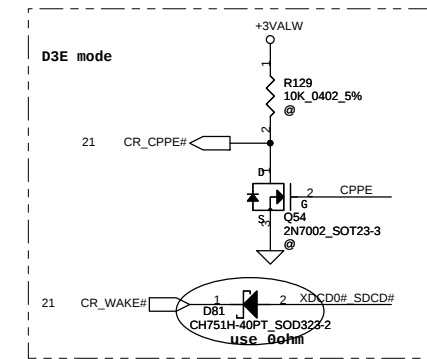
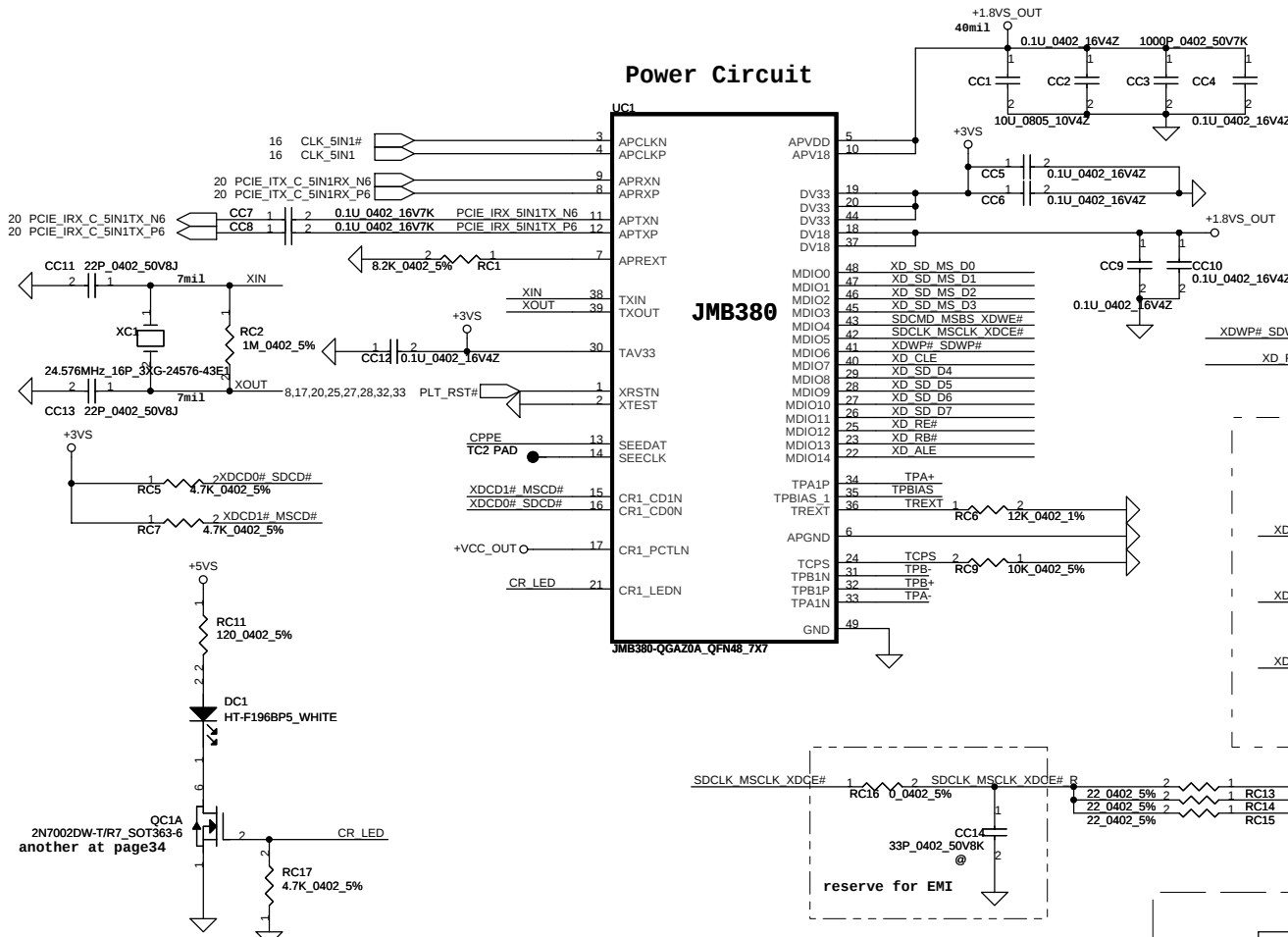
HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK



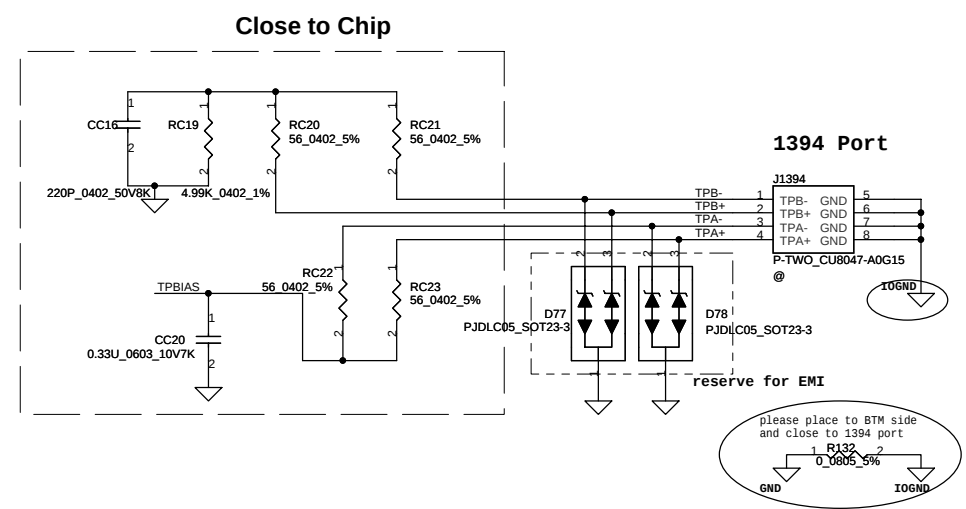
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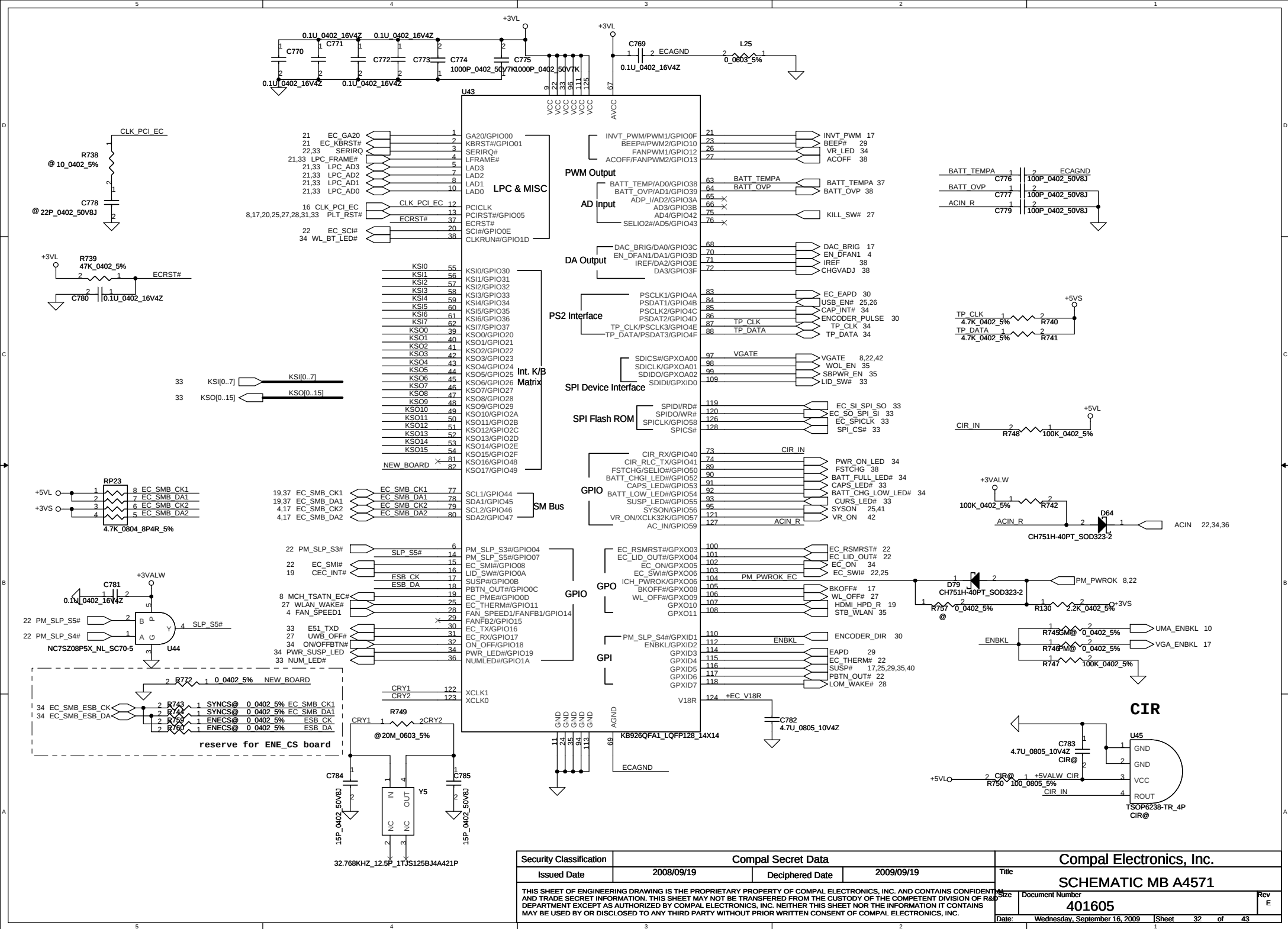


Strapping setting

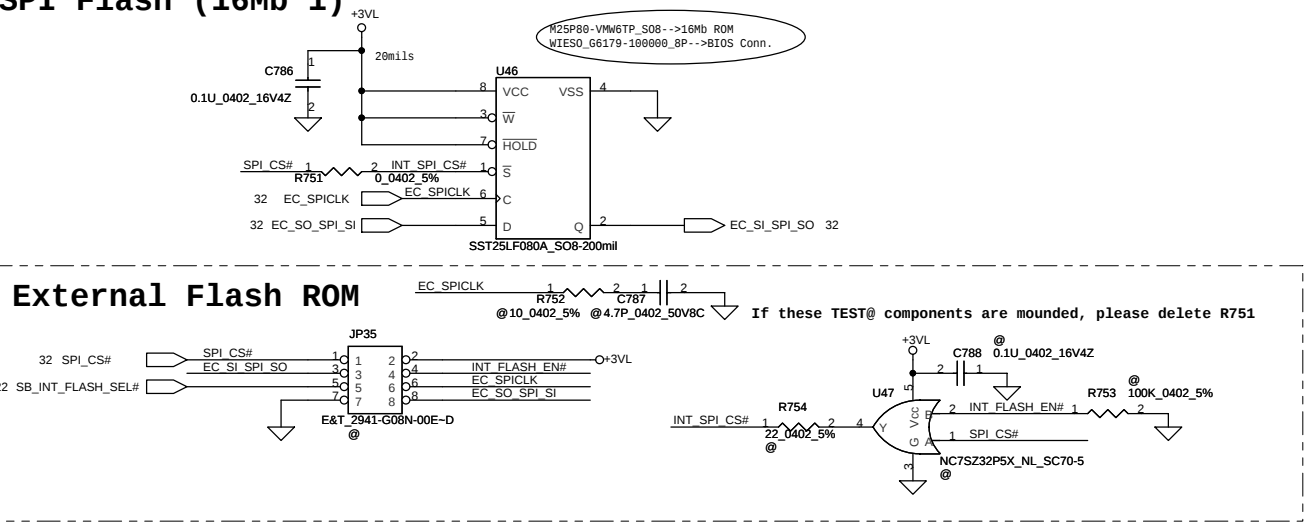
Pin name	Description	
	High	low
MDIO7	on-board	add-in card
MDIO12	+VCC_OUT high active	+VCC_OUT low active
MDIO14	CR_LED high active	CR_LED low active

P.S CR1_PCTLN aslo can out 3V with 250mA for 5IN1 using.(MDIO12 can't be seted after MP IC)



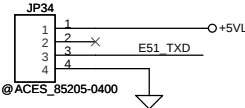


SPI Flash (16Mb*1)

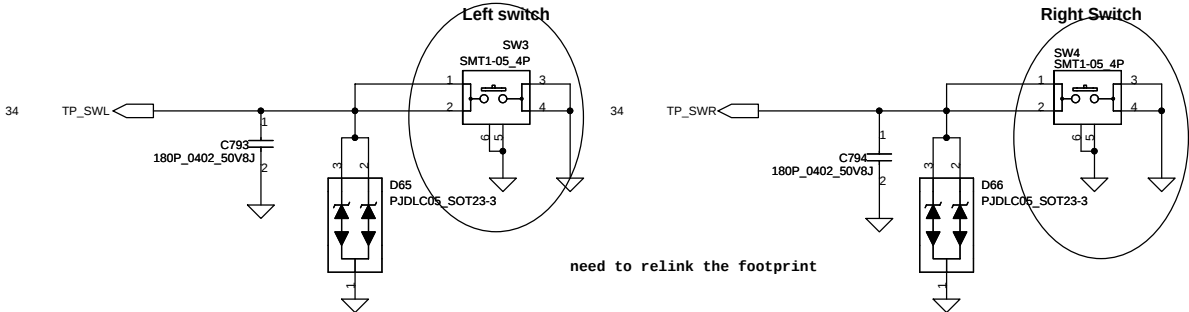
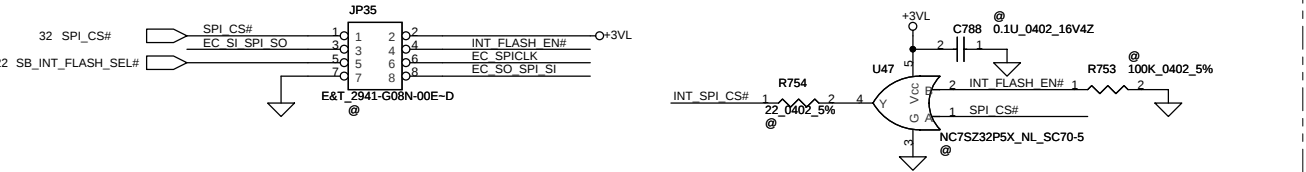


Please place the connector under DDR door

For EC



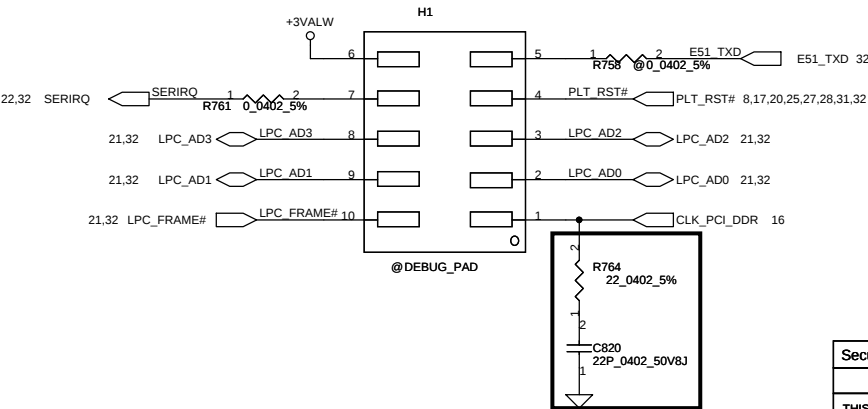
External Flash ROM



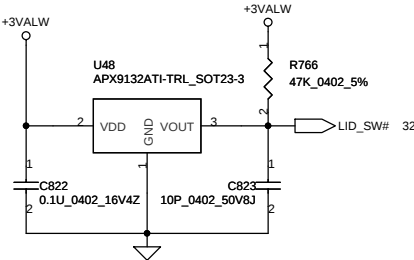
need to relink the footprint

LPC Debug Port

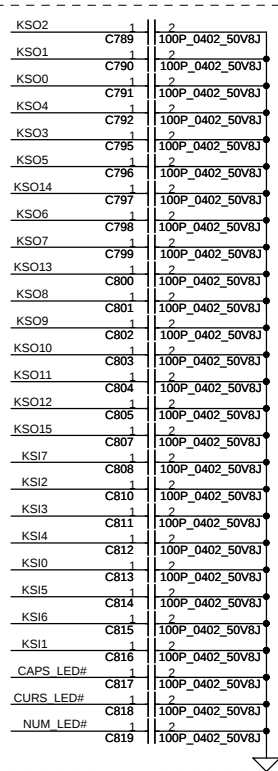
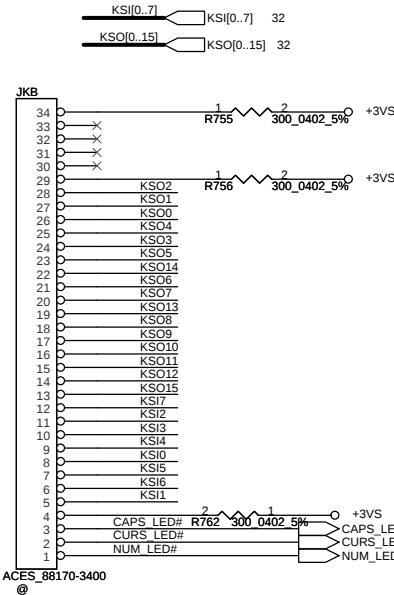
Please place the PAD under DDR DIMM.



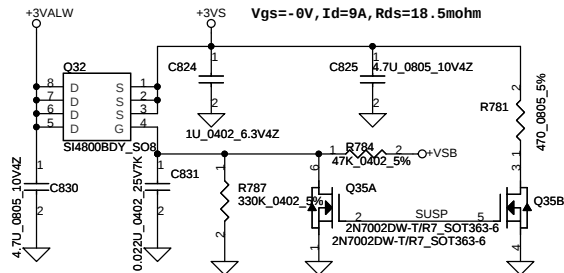
Lid SW



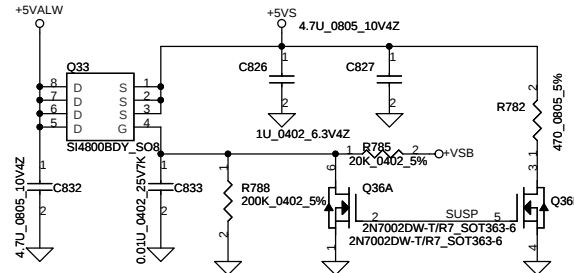
KEYBOARD
CONN.



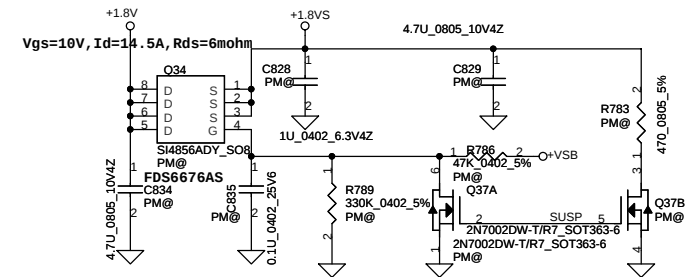
+3VALW TO +3VS



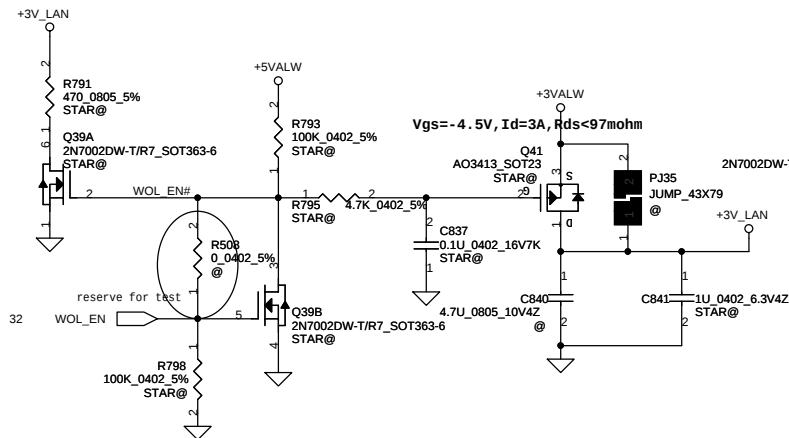
+5VALW TO +5VS



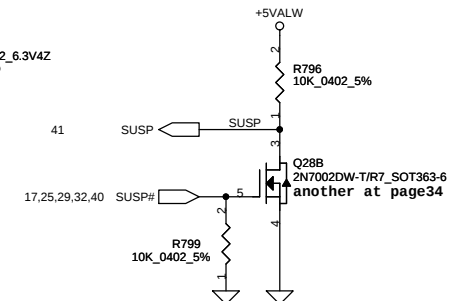
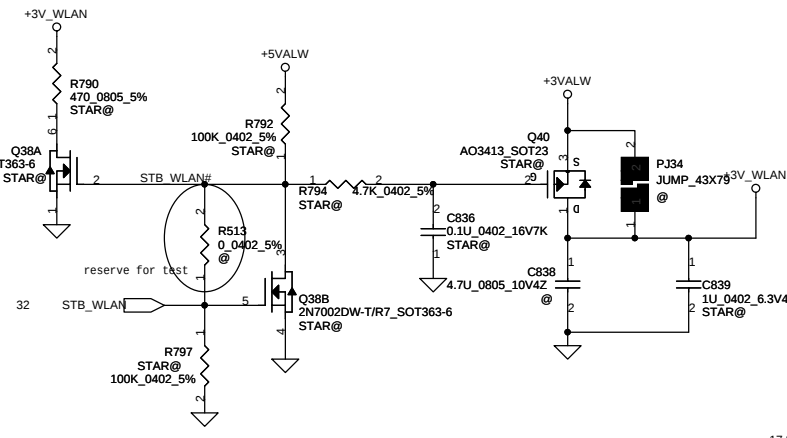
+1.8V to +1.8VS



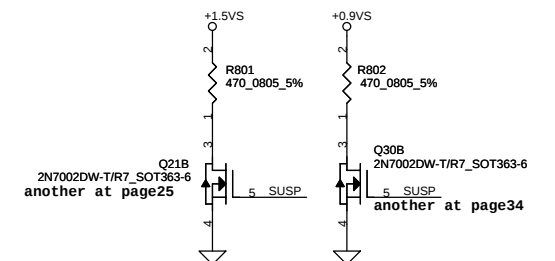
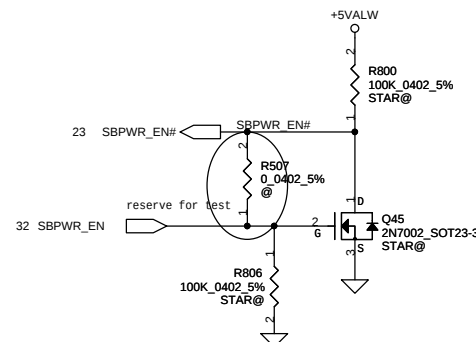
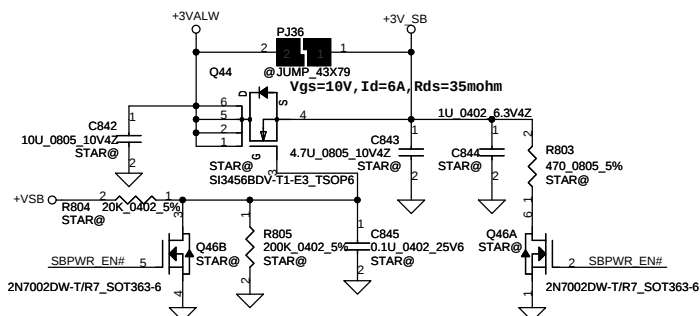
+3VALW TO +3V_LAN



+3VALW TO +3V_WLAN



+3VALW TO +3V_SB



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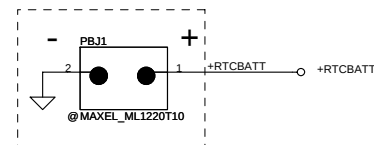
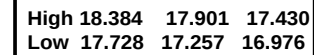
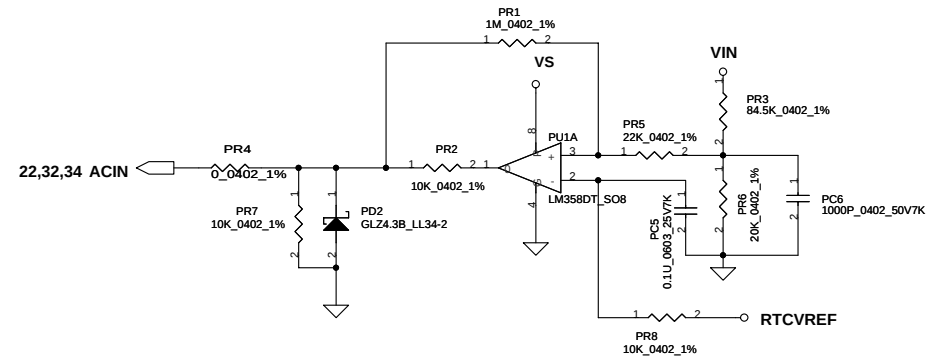
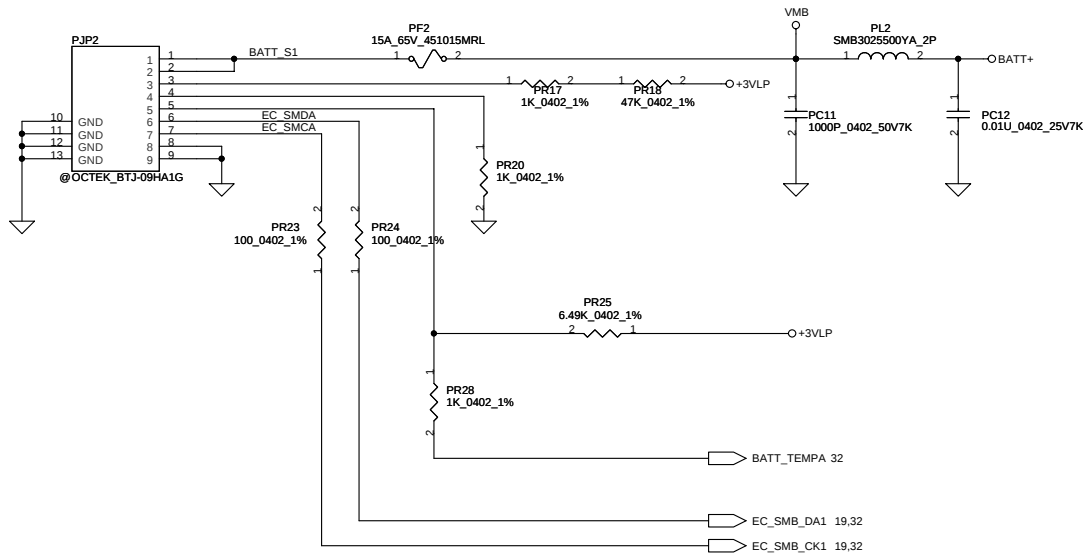
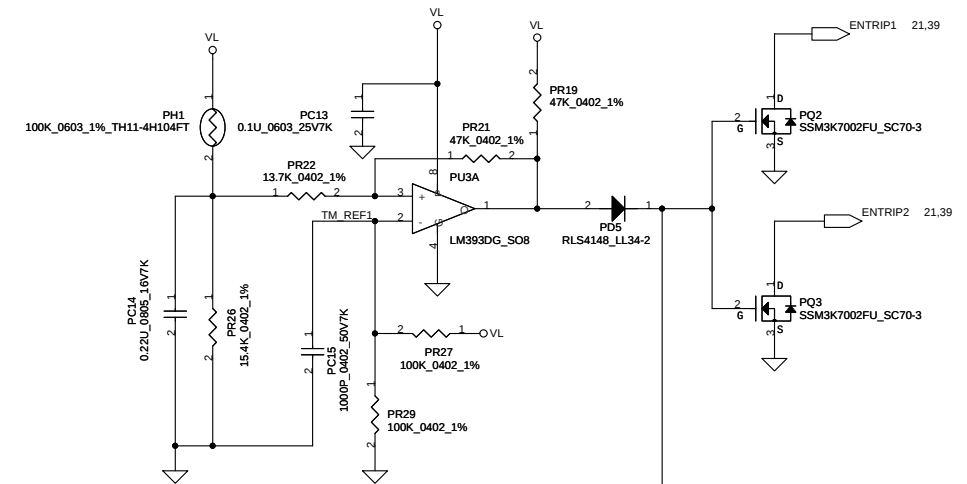


Figure 1: Schematic diagrams of the 16 channels of the 16-channel multi-electrode array (MEA) system. The diagrams show the electrical connections for each channel, including the input voltage, the electrode array, and the output voltage. The channels are labeled P31 through P38, P39 through P46, and P47 through P54. The input voltages are +3VALWP, +5VALWP, +VSBP, +0.9VSP, +1.8V, +1.05VSP, and +1.5VSP. The output voltages are +3VALW, +5VALW, +VSB, +0.9VS, +1.8V, +1.05VS, and +1.5VS. The electrode arrays are labeled @JUMP_43X118, @JUMP_43X118, @JUMP_43X118, @JUMP_43X118, @JUMP_43X118, @JUMP_43X118, and @JUMP_43X79. The channel specifications are (5A, 200mils, Via NO.= 10), (5A, 200mils, Via NO.= 10), (120mA, 40mils, Via NO.= 1), (2A, 80mils, Via NO.= 4), (12A, 480mils, Via NO.= 24), (10A, 400mils, Via NO.=20), and (2.0A, 80mils, Via NO.=4).

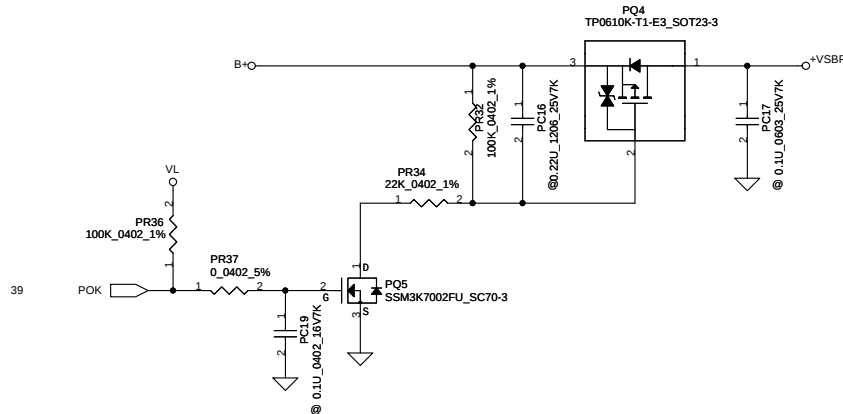
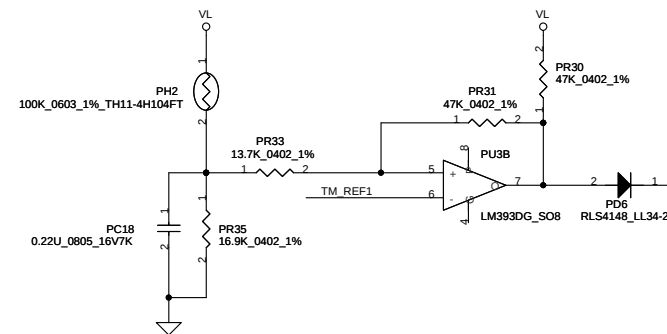
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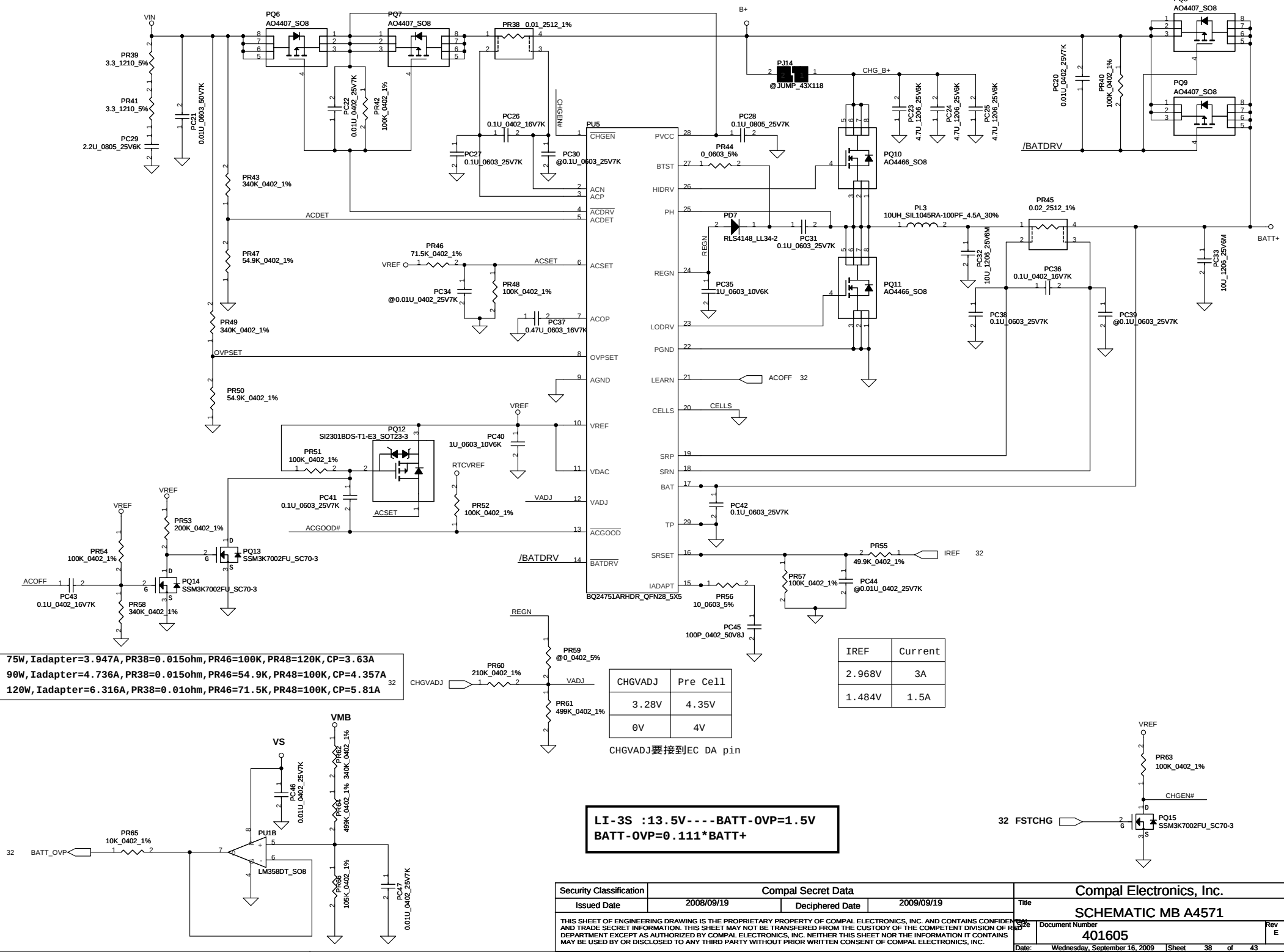
PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 90 degree C
Recovery at 53 degree C



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/19	Deciphered Date	2009/09/19	Title	SCHEMATIC MB A4571
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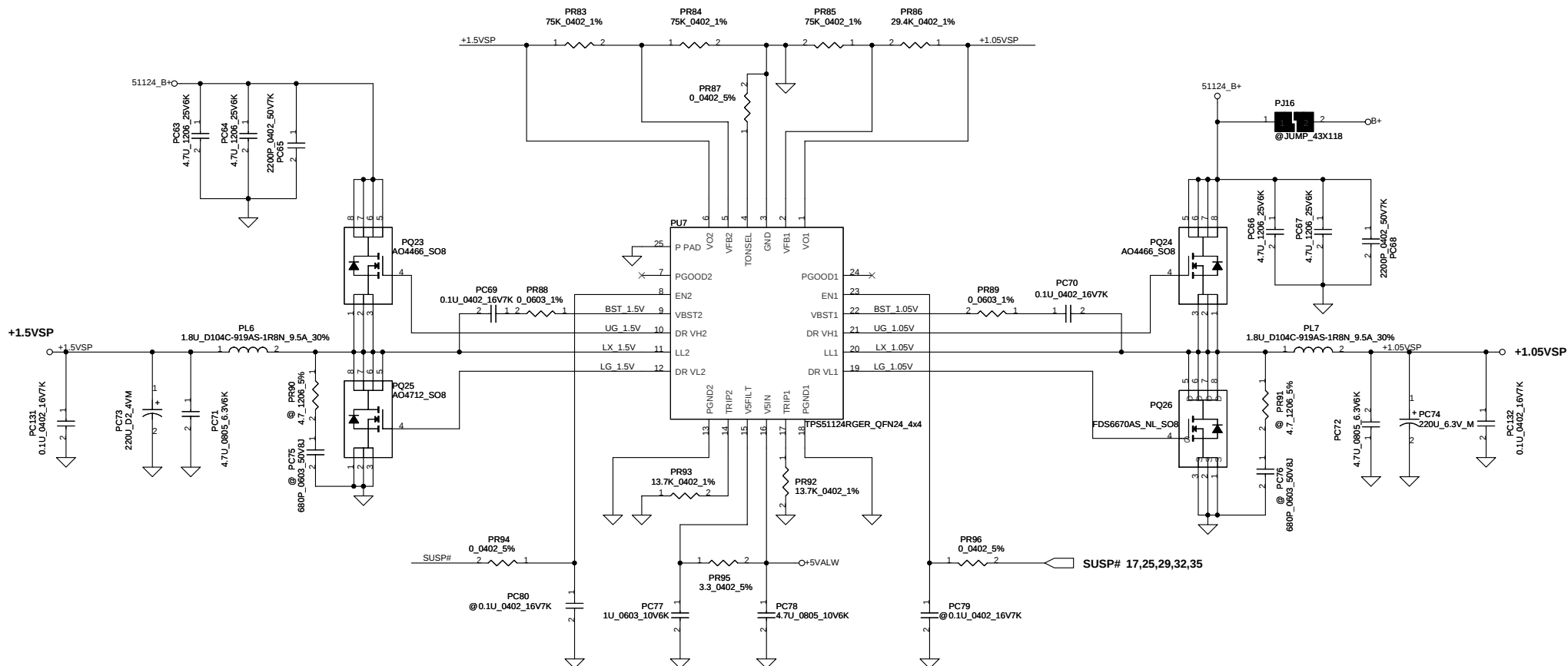


75W, Iadapter=3.947A, PR38=0.015ohm, PR46=100K, PR48=120K, CP=3.63A
90W, Iadapter=4.736A, PR38=0.015ohm, PR46=54.9K, PR48=100K, CP=4.357A
120W, Iadapter=6.316A, PR38=0.01ohm, PR46=71.5K, PR48=100K, CP=5.81A

CHGVADJ	Pre Cell
3.28V	4.35V
0V	4V

IREF	Current
2.968V	3A
1.484V	1.5A

LI-3S :13.5V---BATT-OVP=1.5V
BATT-OVP=0.111*BATT+



PIR (Product Improve Record)

KTKAA LA-4571P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	6/18	34	change Q29.3 to pull up with +3VALW and R770, R720 to 120ohm	to solve suspend led issue.
2	6/18	27	exchange J3GSIM pin2 and pin3	link to error pin definition.
3	6/18	27	change CM15,CM16 to 10P and un-mount RM1 and Cm14.	for customer request.
4	6/24	18	add C849, C850 for EMI request.	for EMI request.
5	6/24	11	add 220u to +1.8V with C78.	reserve for test.
6	6/24	24	add 220u to +USB_VCCB with C79.	reserve for test.
7	6/24	29	add C851 to SPDIF.	for EMI request.
8	6/24	27	link JNAND.39,41 to +3VS,and 39,43 pin link to GND	this is standard pin define
9	6/25	19	change U37 power from +HDMI_5V_OUT to +5VL	for customer request and follow Toshiba design guide with CEC.
10	6/25	27	reserve some circuit for change Mini card 1 and 2	reserve for GPS issue
11	6/26	30	change CA29-CA32 from 0.47u to 0.033u	set high pass frequency to 68Hz
REVISION CHANGE: 0.2 TO 0.3				
1	7/19	34	add R506 and Q52 for Wimax LED control	reserve Wimax LED control to avoid MINI card module damage.
2	7/19	35	change R788,R805 from 330K to 200K	reduce the voltage on the Vgs of MOS as AC mode.
3	7/19	35	mount R507 and un-mount Q45,R800,R806	use another control for +5V_SB
4	7/19	23	mount Q16,R593,R594 and un-mount Q12	use another control for +5V_SB
5	7/22	35	add R508,R513	reserve for tset
5	7/22	31	add D77,D78 on 1394 port	reserve for EMI request
6	7/22	26	exchange JFEL all pin	to solve the cable reverse issue
7	7/24	3	delete XDP conn and related compoments	to improve ESD issue
8	7/24	34	add Q42 and link to EC U43.72	to solve the power on LED need 2.1S will be light after press power button
9	7/24	31	add Q54,R129,R220,R222,D81 and link to U9.B10,U9.AE8	reserve D3E mode as JMB380
10	7/24	28	add R398,R399,R264 for LAN and link to U9.AH24,U9.C21	reserve LAN saving mode
11	7/24	32	add R757,R130,D79	to avoid glitch issue when KB926 power on
12	7/24	34	add D80	reserve for ESD request
13	7/24	26	add L26,R181,R182 on camera conn.	reserve for EMI request
14	7/24	34	add R514-R517,D5,D6	reserve for LED type option
15	7/25	34	add R97,R103,R518,C852-C854,D82 on CS/B conn	reserve for ESD request
16	7/25	34	add R105,R106 on Touch/B conn	reserve for ESD request
17	7/25	26	add R110,R114 on Finger/B conn	reserve for ESD request
18	7/25	26	add R131,D83 on Felica conn	reserve for ESD request
19	7/25	28	change LAN footprint to "TYC0_2068888-1 12P-T"	for ME team request
20	7/25	31	add R132 and separate support pin of 1394,USB,eSATA to IOGND	for ESD request
21	7/25	18	change C680-C685 to 2.2pF	for customer request
22	7/25	26	change R722 form 0ohm to 100Kohm	it's to let the power on first then reset# will be high later to meet spec
23	7/25	34	mount D5,D6,R515,R517 and un-mount D71,D73,R514,R516	change logo LED to high illumination
REVISION CHANGE: 0.3 TO 1.0				
1	8/10	27	exchange QM1 Pin2,3	reserve 3G SMI card VPP function.
2	8/10	27	add R820 and link to both JGPS.16 and J3GSIM.5	add more power pin for standard definition
3	8/10	27	link JGPS.24 to +3V_WLAN,link JNAND.24 to +3VS	reduce the forward voltage for HDMI logo Spec.
4	8/10	19	change D8,D53 from RB491D to RB161M	no 0603 type part in Compal Hub and improve the audio performance
5	8/10	30	change CA29-CA32 form 0603 type to 0402	for Layout team request
6	8/10	34	change H19,H21 from 4P8X3P8 to 3P8X4P8	change camera power to +5VS for energy star
7	8/10	26	add R821 and link +5VS to +CAM_VDD	for DFX request to easy check when SMT
8	8/11	11	change C72,C73,C78,C79,C146 Footprint to C_PXC6P3VC220MF60	2008 no amber LED on power button
9	8/11	34	delete R772	follow Intel design guide when no XDP schematic
10	8/18	4	change R4-R7 from 49.9ohm to 54.9ohm	to solve measure HDMI logo can't be detected with test implement
11	8/18	19	Change RV67 from 10K to 2.2Kohm	solve EMI issue
12	8/18	19	use common choke(L9-L12) to replace 0ohm	to solve the word is blurred when CRT mode
13	8/18	18	change L18-L20 to high speed bead	solve EMI issue
14	8/18	21	mount EMI SSIC and related conpomemts for Bit_CLK	for EMI request
15	8/18	33	mount C793,C794	to solve VGA/B external thermal sensor can't normal work when VGA chip is very high temp.
16	8/18	34	change C831 from 0.01u to 0.022u	enable D3E mode
17	8/31	31	change D81 to 0805_0	expand PM_PWROK voltage from 2.4V to 3.05V
18	8/31	32	change R130 form 10K to 2.2K	for EMI request
19	9/5	30	mount CA40 and CA41 to 120P	set right strap pin when no IHDMI SKU
20	9/5	8	change R62 BOM config from GM@ to IHDMI@	solve some CRT device will appear most resolution when CRT only mode
21	9/8	18	change R674 from 10K to 0ohm	
REVISION CHANGE: 1.0 TO 2.0				
1	9/19	27	change JGPS power from +3V_WLAN to +3VS	Solve GPS disappear when link 850Mhz only
2.	9/19	N/A	change PCB from 6 layer to 8 layer	imporve EMI and slove assembly procedure not easy issue