

Compal confidential

KSRAA LA-4471P Schematics Document

Mobile Penryn uFCPGA with Cantiga + ICH9M core logic

2008-06-12

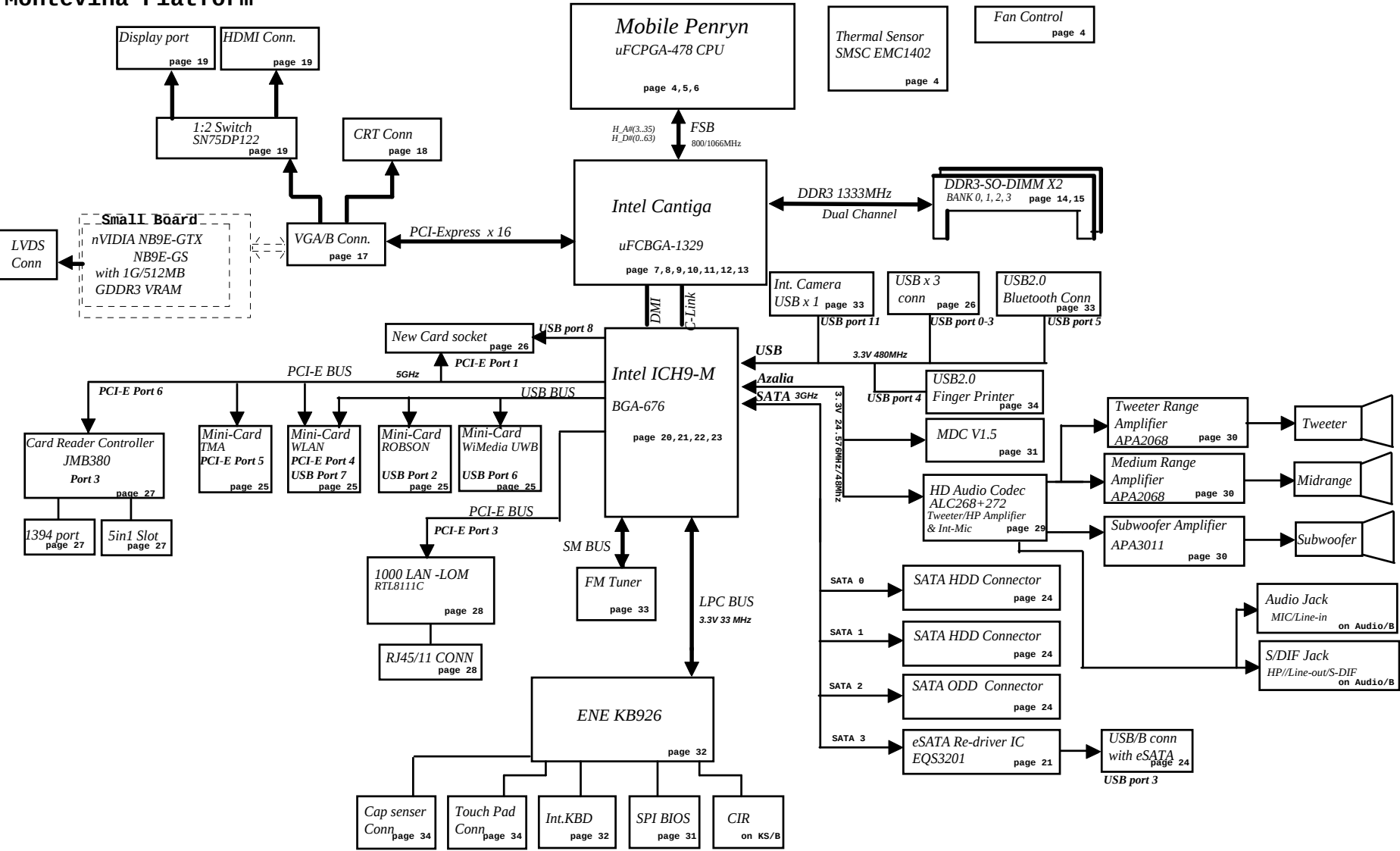
REV:1.0

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Model : KSRAA
File Name : LA-4471P

Montevina Platform



KSRAA Sub-board

VGA/B
LS-4471P NB9E-GTX
LS-4302P NB9E-GS

Power/B
1 Button+2LED
LS-4305P

KS/B
KS+CIR+LogoLED
LS-4306P

FP/B
LS-4307P

LED/B
8 LED+Lid
LS-430BP

Cap Sense/B
9 BOT+LED
LS-430CP

Audio/B
MIC+S/DIF+VR
LS-430DP

TP_LED/B
5 LED for TP COVER
LS-430EP

FM Tuner/B
FM Tuner+wirless con
LS-430EP

RTC BAT.
page 38

Power On/Off CKT.
page 35

DC/DC Interface CKT.
page 37, 38

Charger
Page 40

Power Circuit DC/DC
Page 38-45

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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.75VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VL	5V always on power rail	ON	ON	ON	ON
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Power	Device	Address
+5VL	EC KB926 C0	
+5VL	Smart Battery	0001 011x b
+5VL	HDMI-CEC	0011 010x b
+5VL	FUN/B (CAP Sensor)	
+3VS	TMA THM Sen ADI ADM1032	1001 100x b

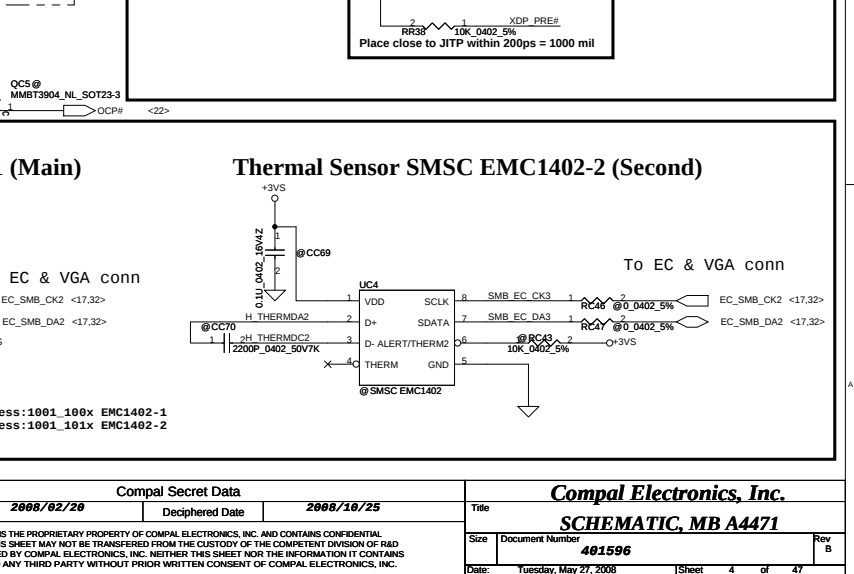
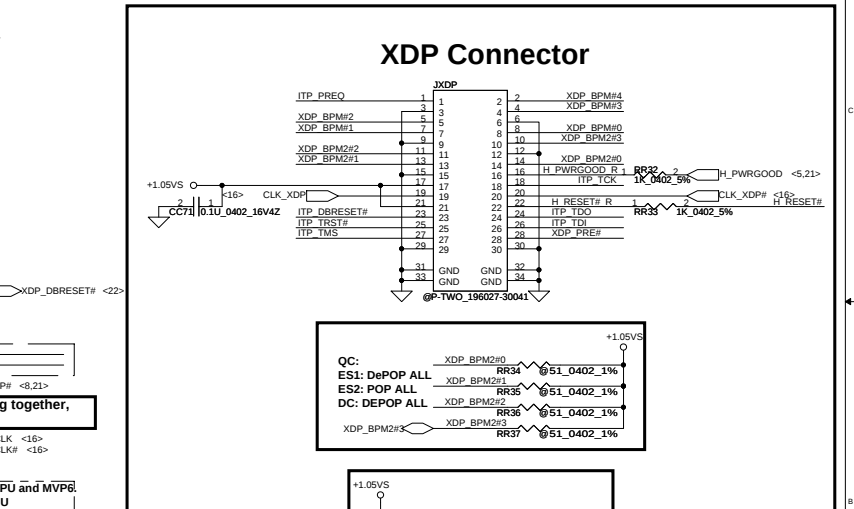
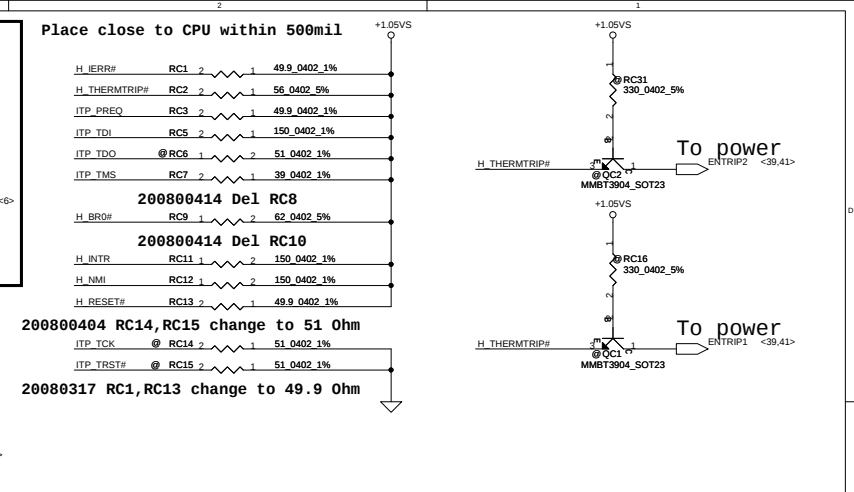
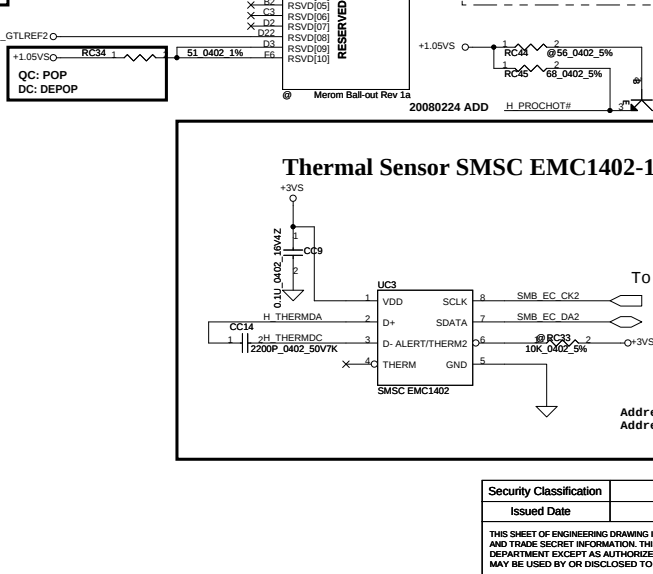
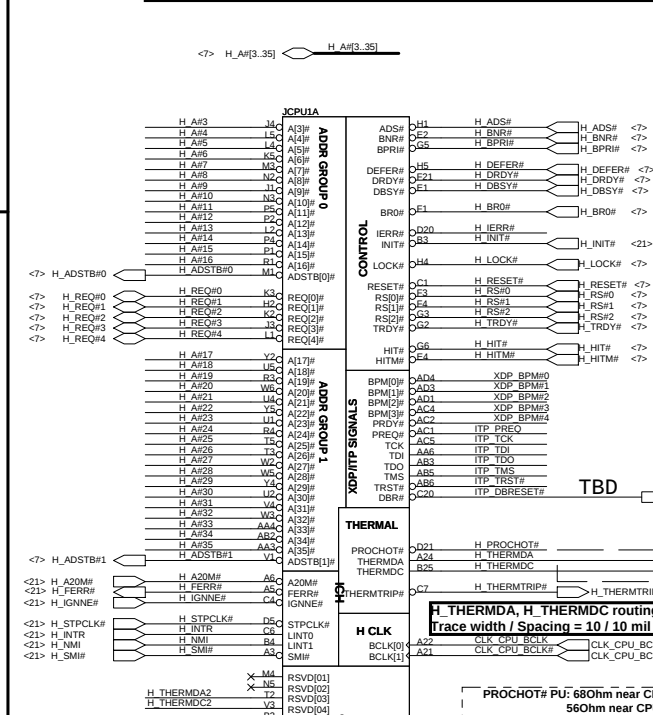
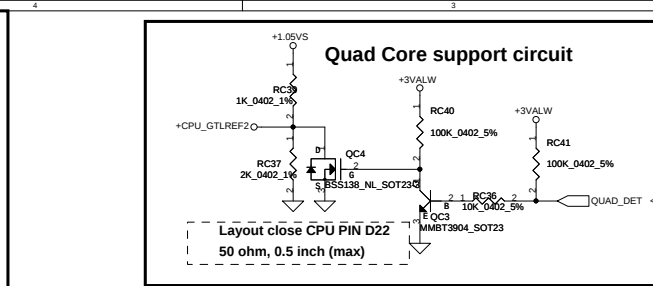
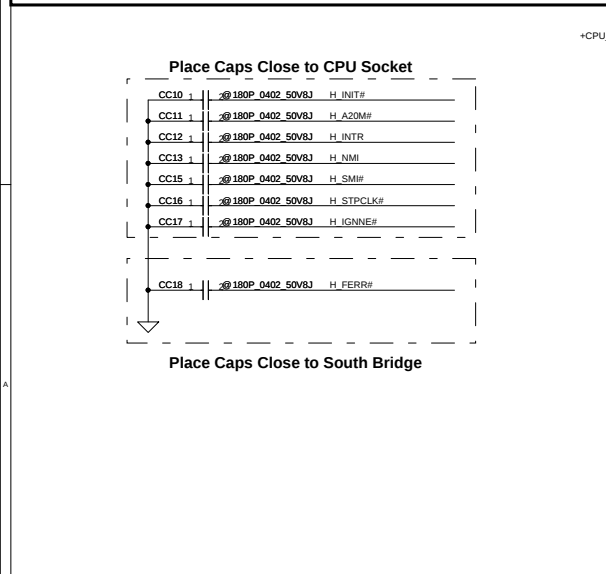
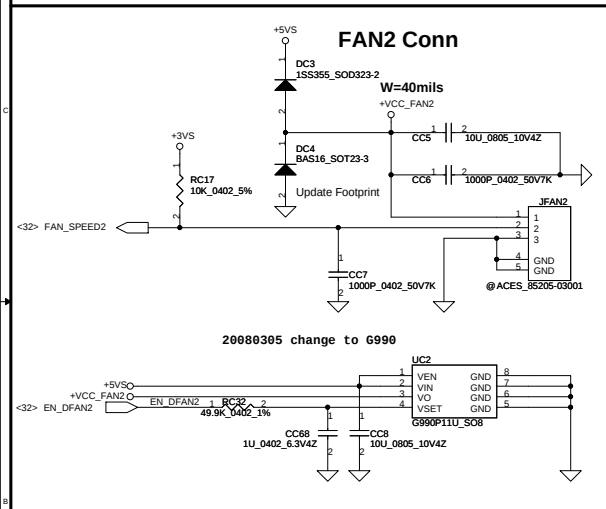
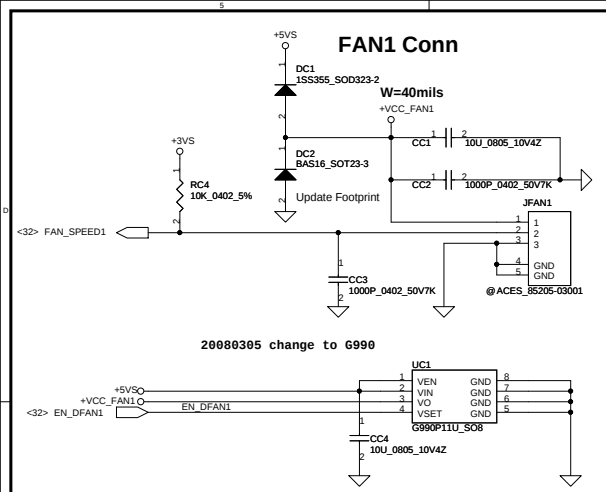
EC SM Bus2 address

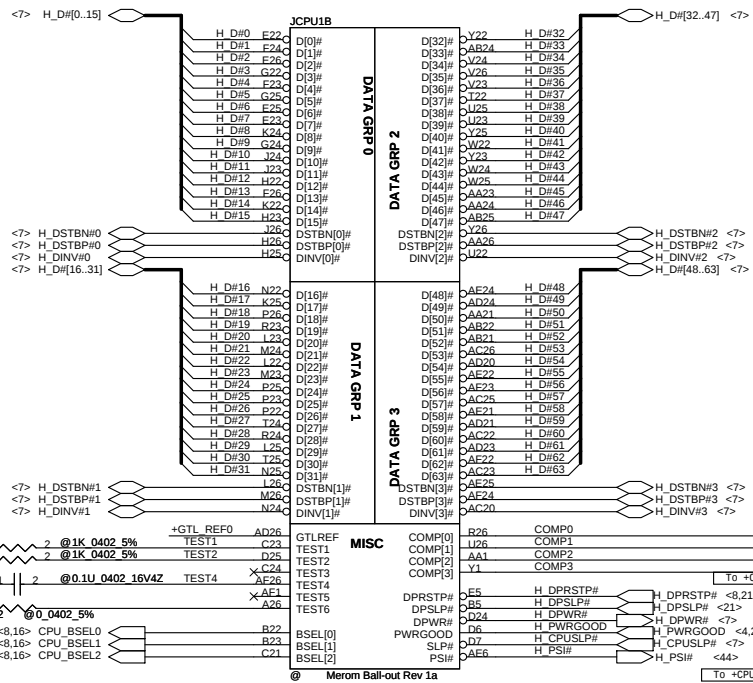
Power	Device	Address
+3VS	EC KB926 C0	
+3VS	CPU THM Sen SMSC EMC1402-1-ACZL-TR	1001 100x b
+3VS	CPU THM Sen SMSC EMC1402-2-ACZL-TR	1001 101x b
+3VS	VGA THM Sen ADI ADM1032	1001 100x b

ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
+3VS	Clock Generator (SLG8SP556V)	1101 001xb
+3VS	DDR DIMM0	1001 000xb
+3VS	DDR DIMM1	1001 010xb
+3VS	Express	
+3VS	FM Module	Vertical I2C

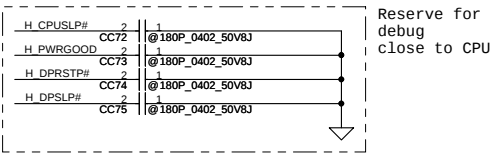
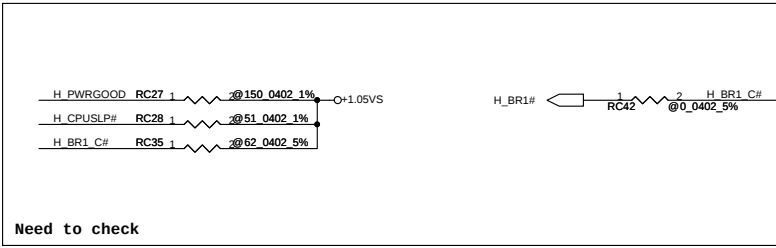
STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		



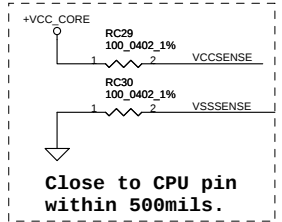
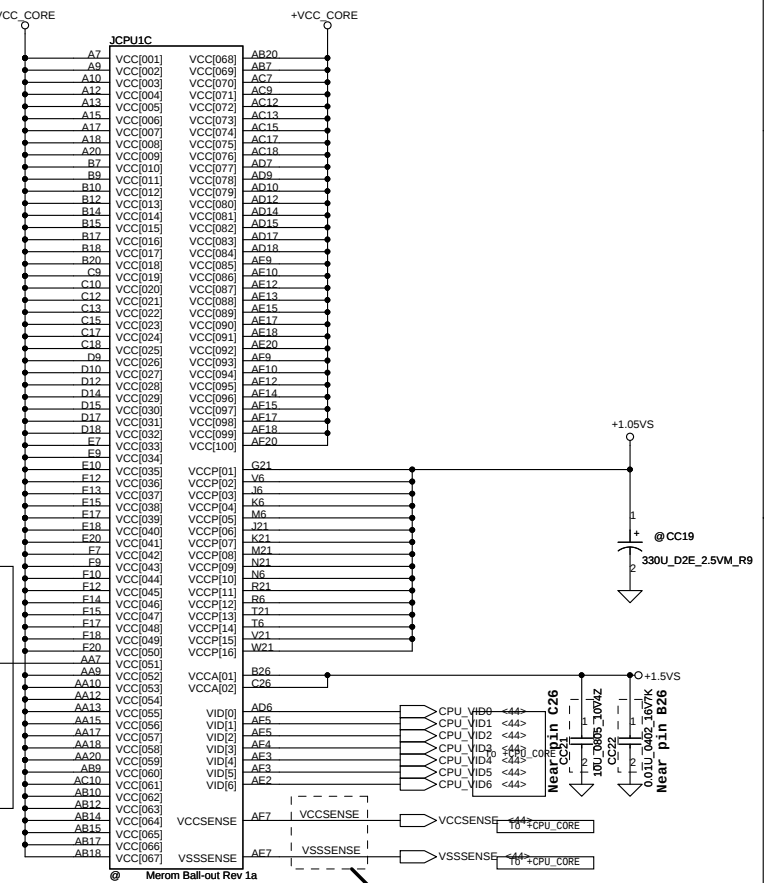


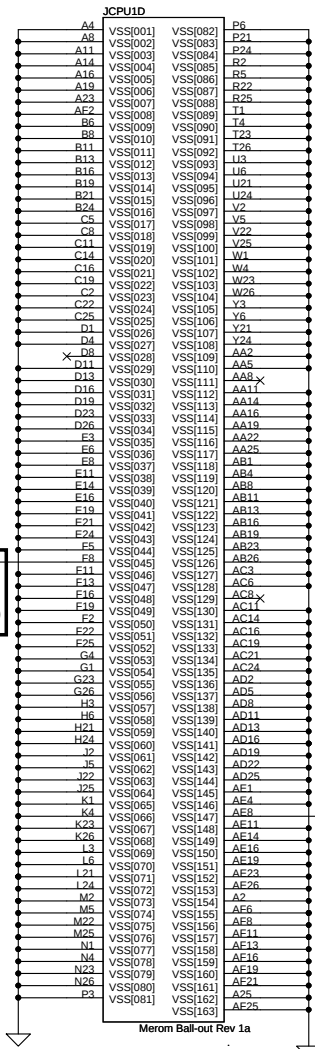
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



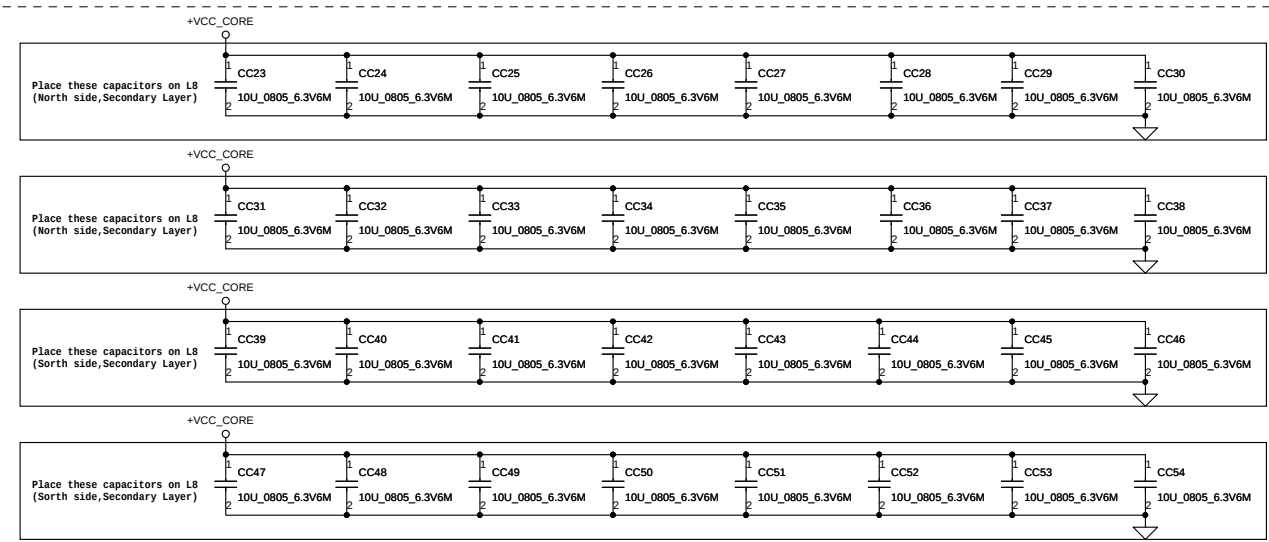
20080317 new add



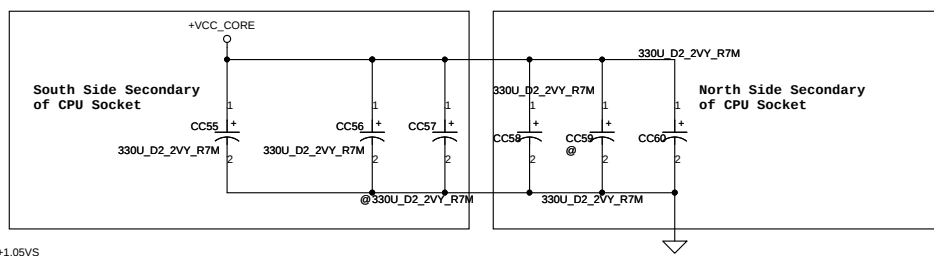


Pin F8
Dual Core: GND (internal)
Quad Core: Floating (internal)

Pin D8,AA8,AC8 and AE8
Reserved for QC

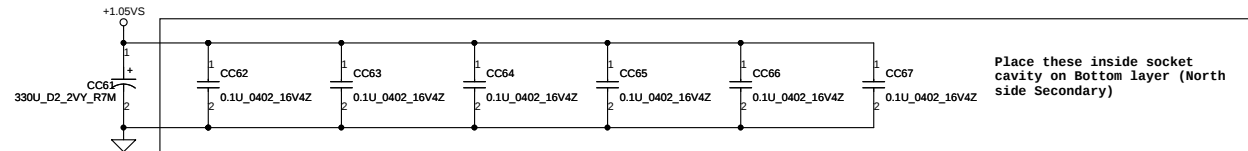


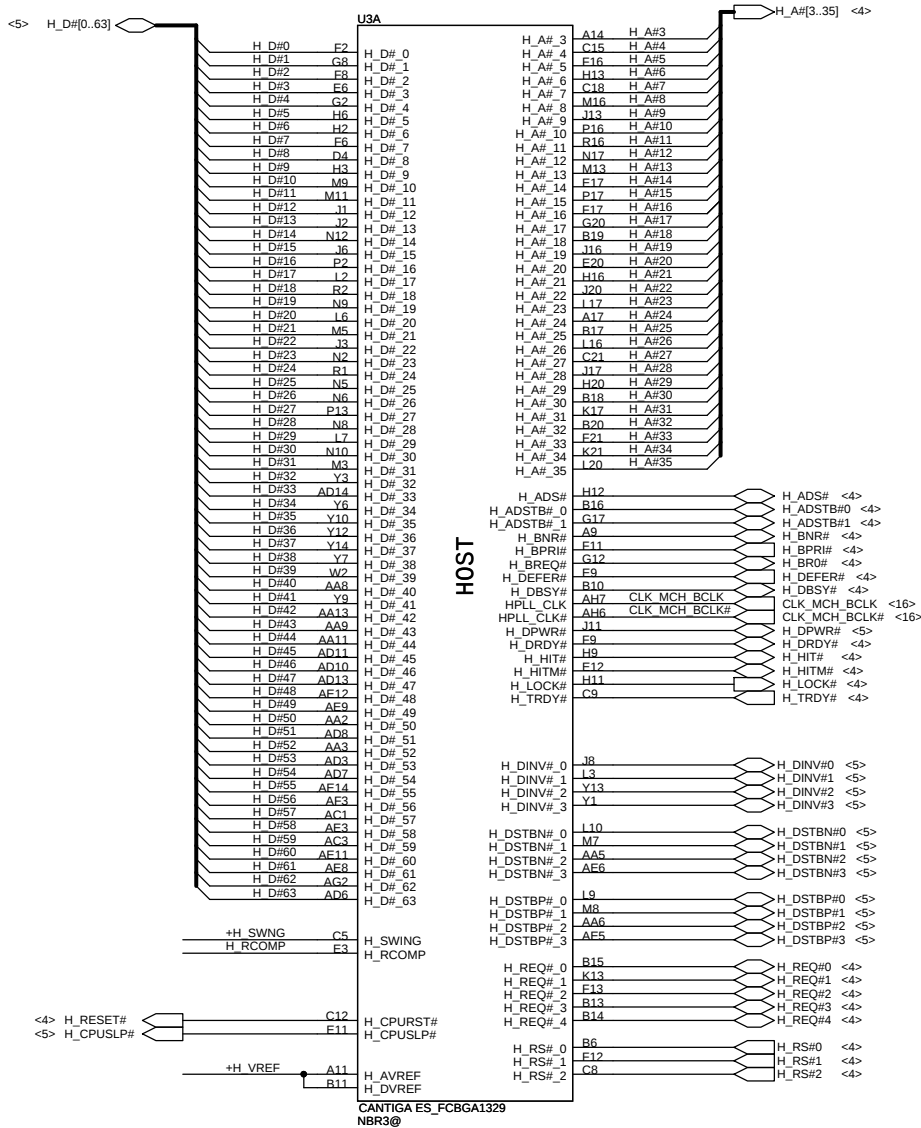
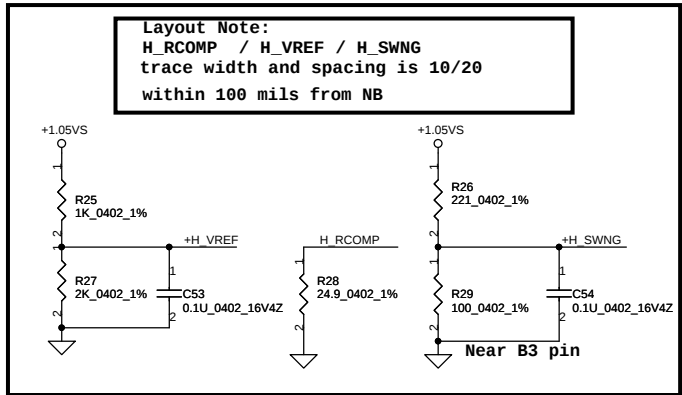
Mid Frequency Decoupling



ESR <= 1.5m ohm
Capacitor > 1980uF

330uF ESR 7m ohm X 6 PCS

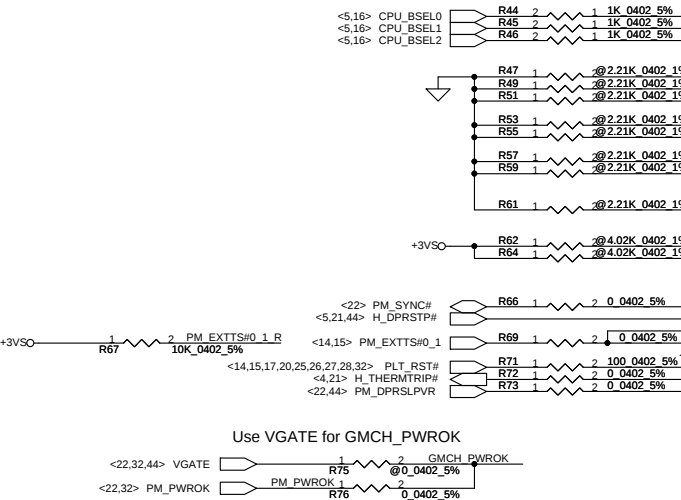




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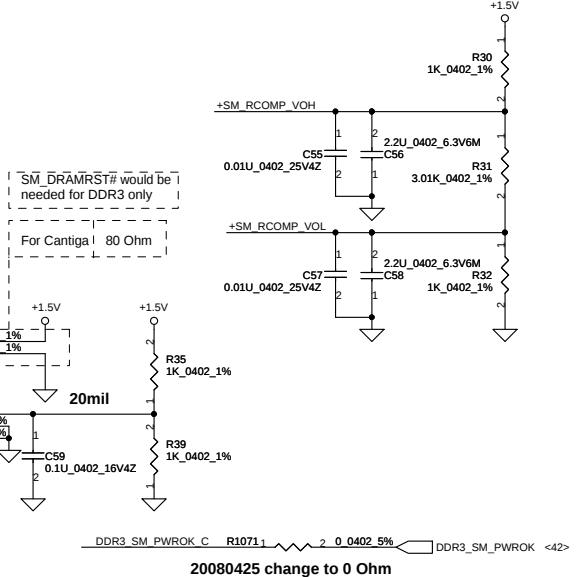
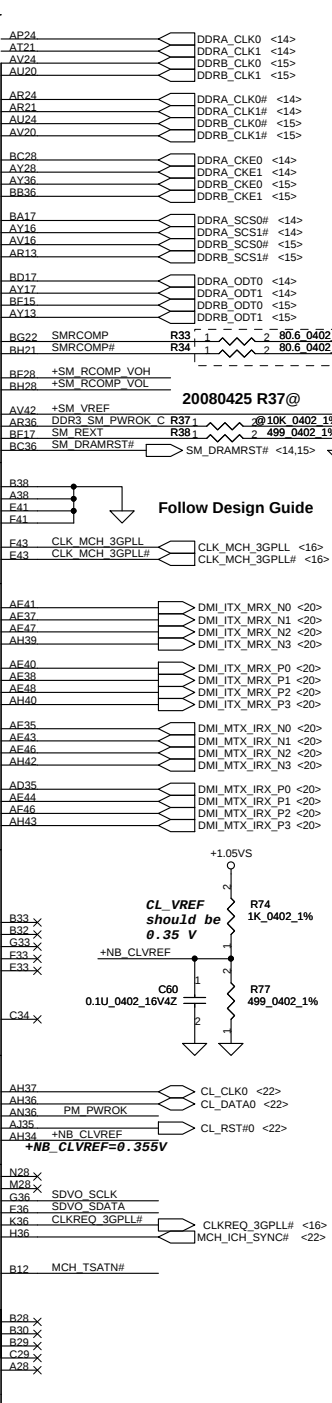
Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6	0 = iTPM Host Interface is enabled*(Default) - can support disble by SW. 1 = iTPM Host Interface is Disabled
CFG7	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable *(Default)
CFG[13:12]	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



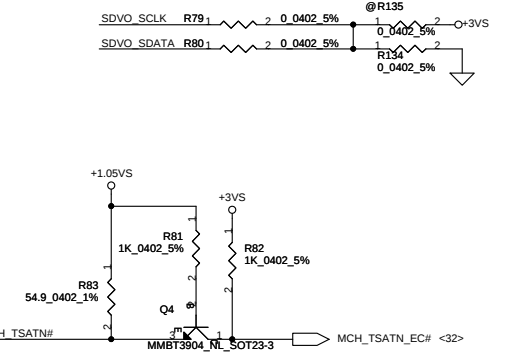
U38	
X M36	RSVD1
X N36	RSVD2
X R33	SA_CK_1
X T33	RSVD3
X AH9	RSVD4
X AH10	RSVD5
X AH12	RSVD6
X AH13	RSVD7
X K12	RSVD8
X AL34	RSVD9
X K34	RSVD10
X N35	RSVD11
X M35	RSVD12
X T24	RSVD13
	RSVD14
X B31	RSVD15
X B7	RSVD16
X M1	RSVD17
X Y21	RSVD20
X G23	RSVD22
X E23	RSVD23
X H18	RSVD24
X E18	RSVD25

RSVD	
CLK	
DMT	
VID	
PM	
ME	
MISC	
HDA	



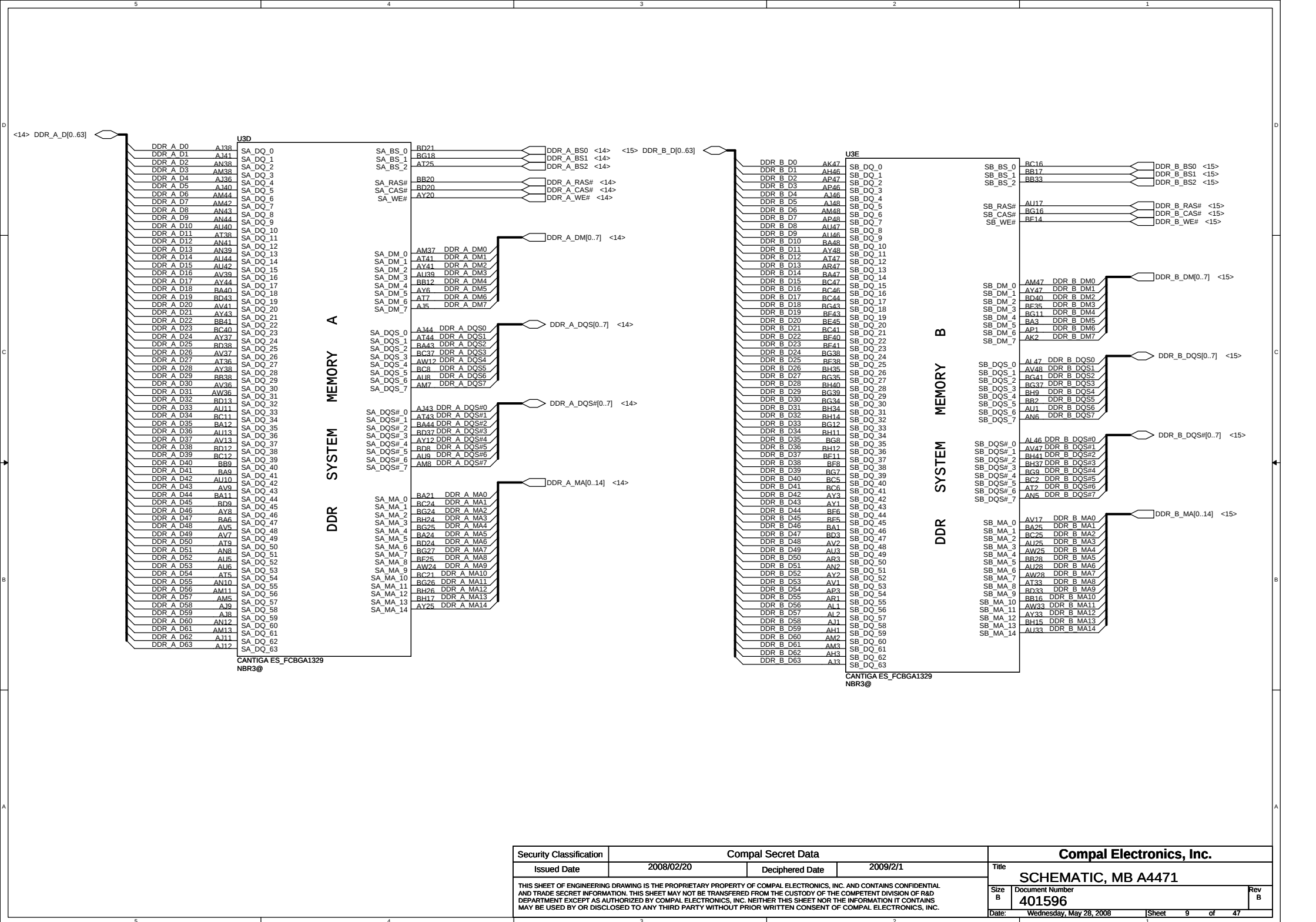
Strap Pin Table

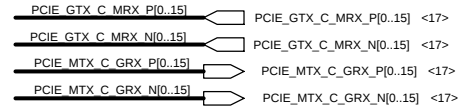
SDVO_CTRLDATA	0 = No SDVO Card Present 1 = SDVO Card Present *(Default)
DDPC_CTRLDATA	0 = Digital DisplayPort Disable 1 = Digital DisplayPort Device Present*(Default)



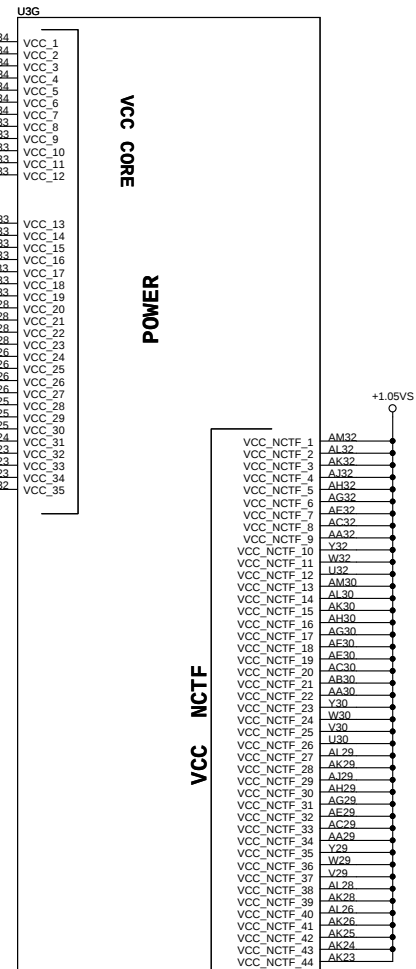
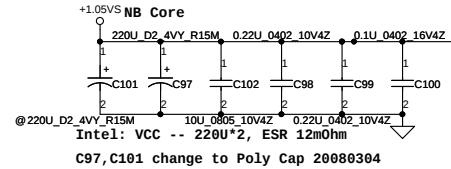
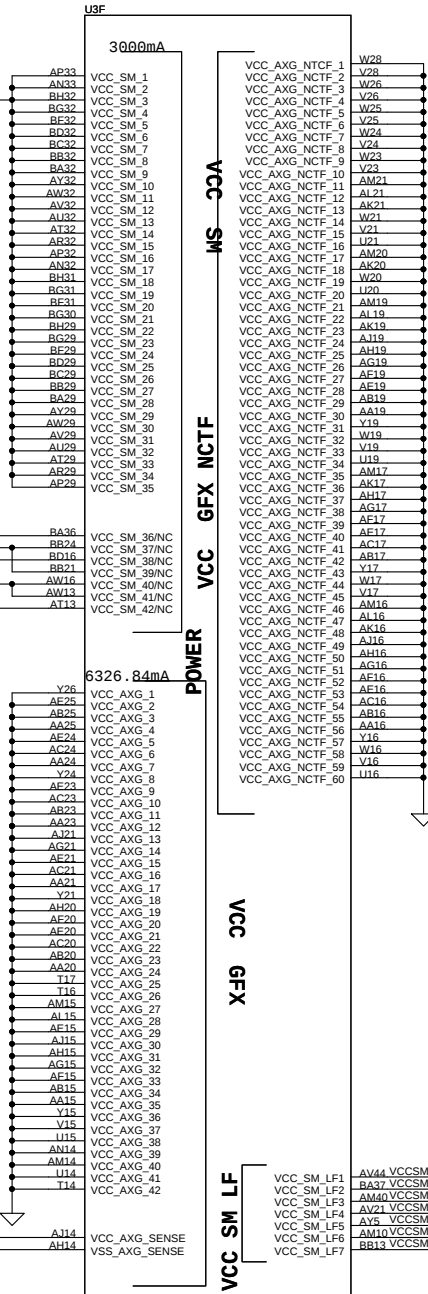
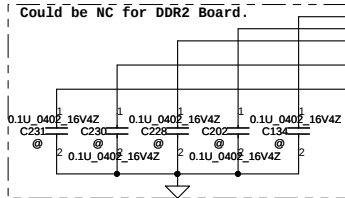
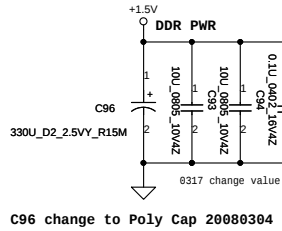
CANTIGA ES_FCBGA1329
NBR3@

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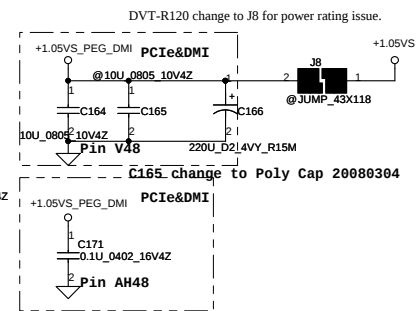
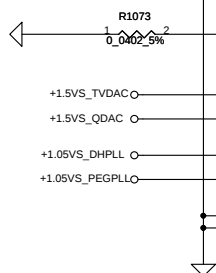
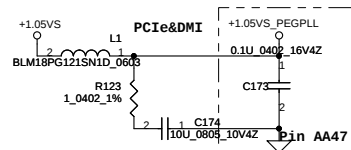




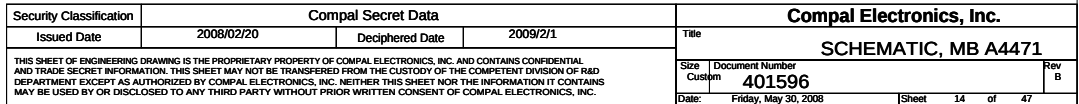
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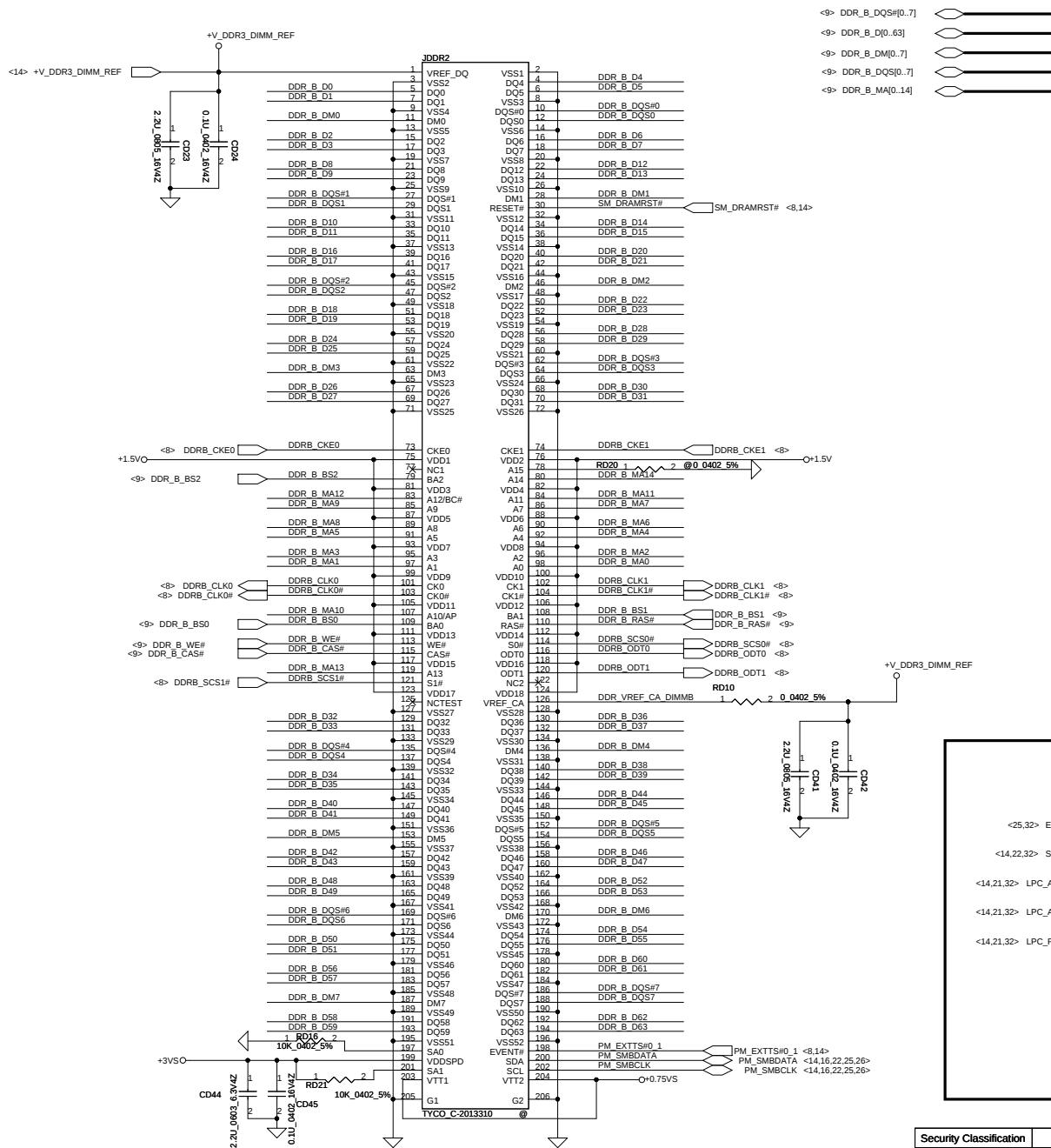


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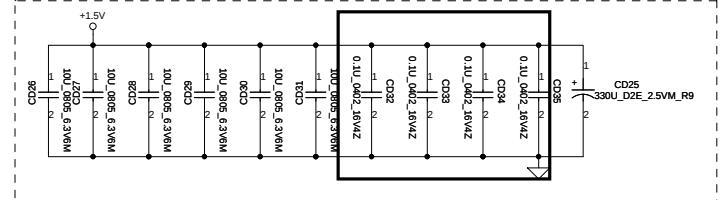




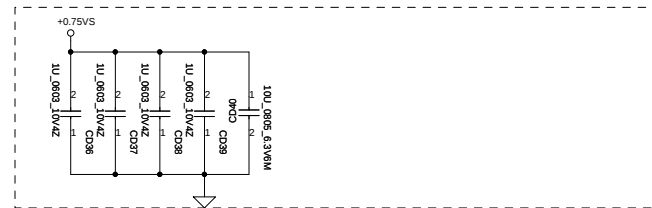
<9> DDR_B_DQS#0[0..7]
 <9> DDR_B_D0[0..63]
 <9> DDR_B_DM0[0..7]
 <9> DDR_B_DQS[0..7]
 <9> DDR_B_MA0[0..14]

Layout Note:
Place near JDDR2

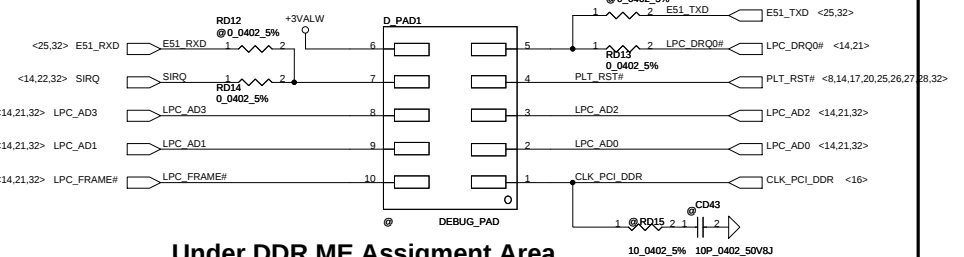
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note:
Place near JDDR2.203 & JDDR2.204



New LPC Debug Pad ---- MB side

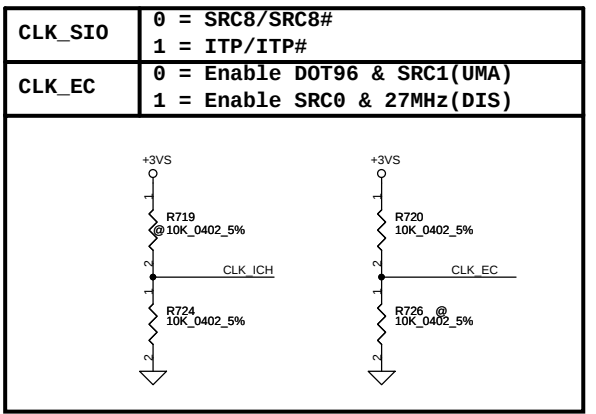
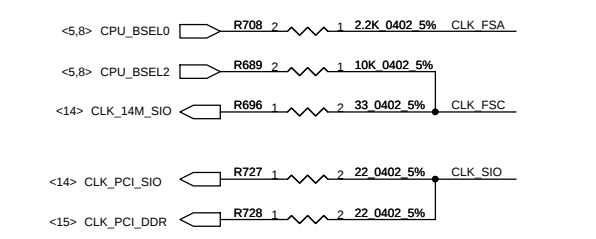
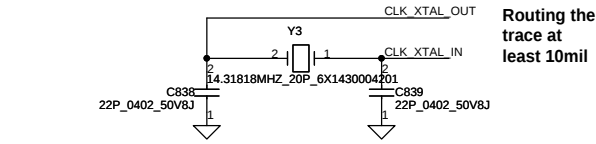
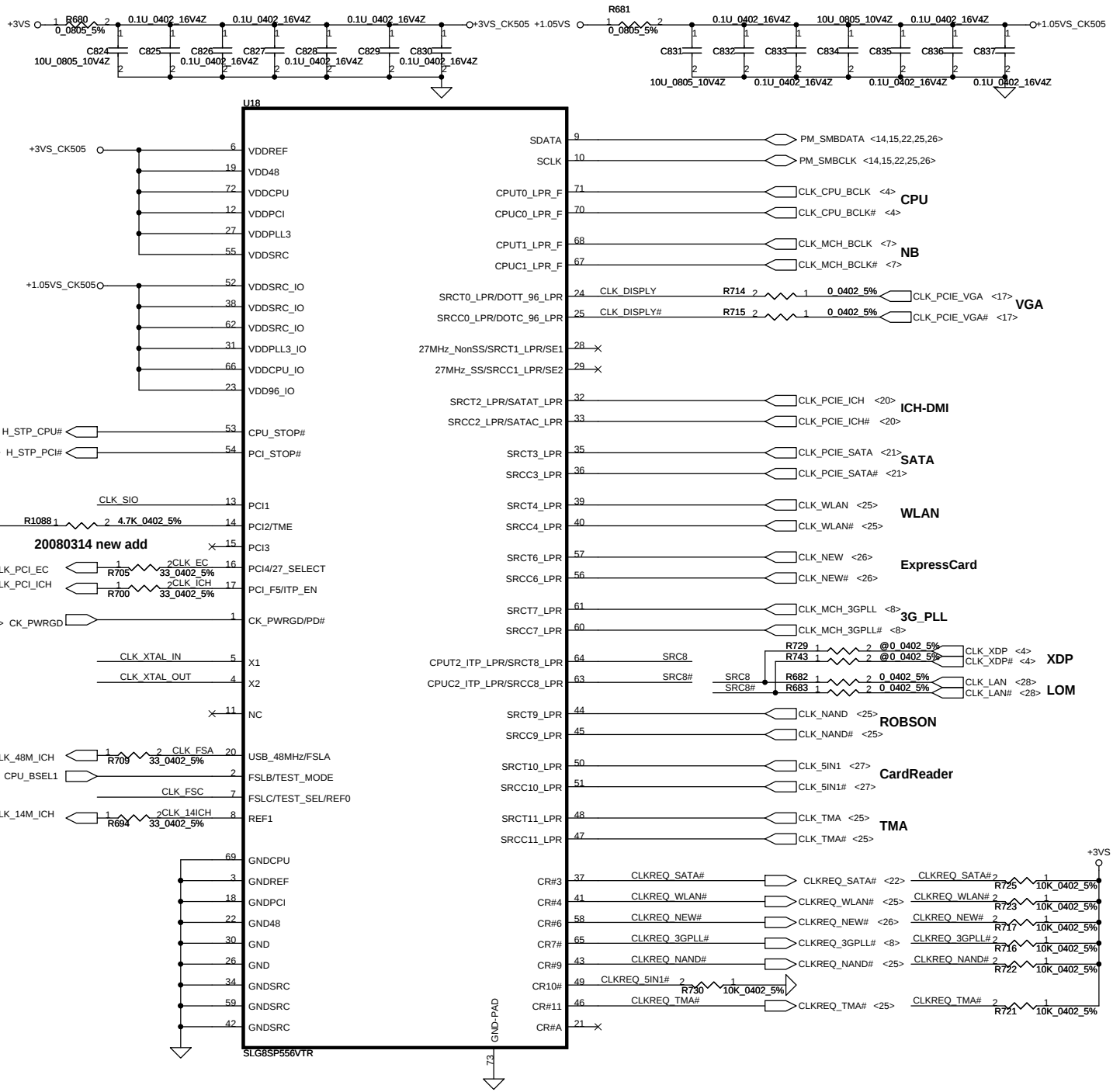


Under DDR ME Assignment Area

Keep Resistor near Debug Pad and in the same side
Reverse side DIMM ---- Pin 1 keep away DIMM

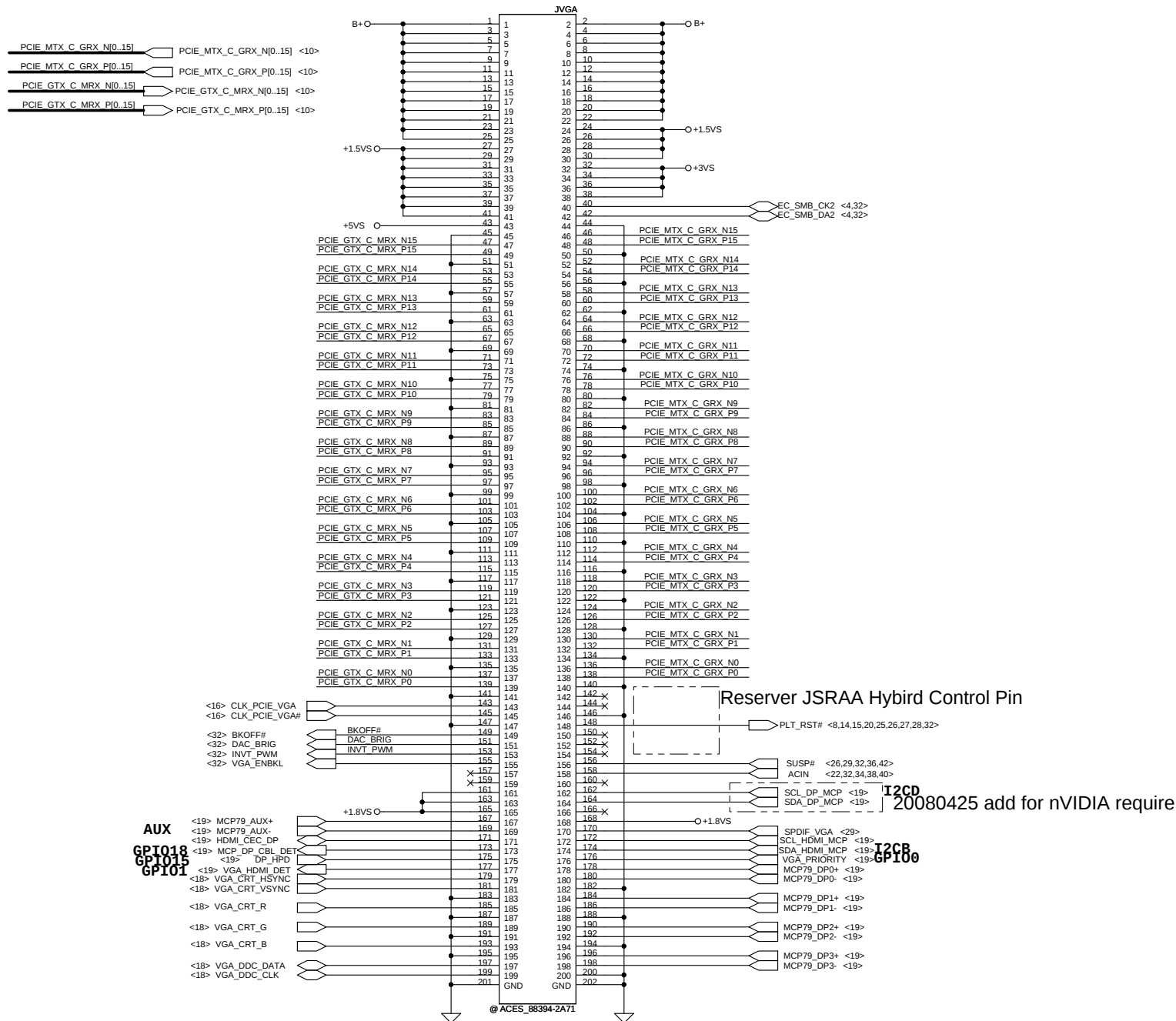
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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHZ	SRC MHZ	PCI MHZ	REF MHZ	DOT_96 MHZ	USB MHZ
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
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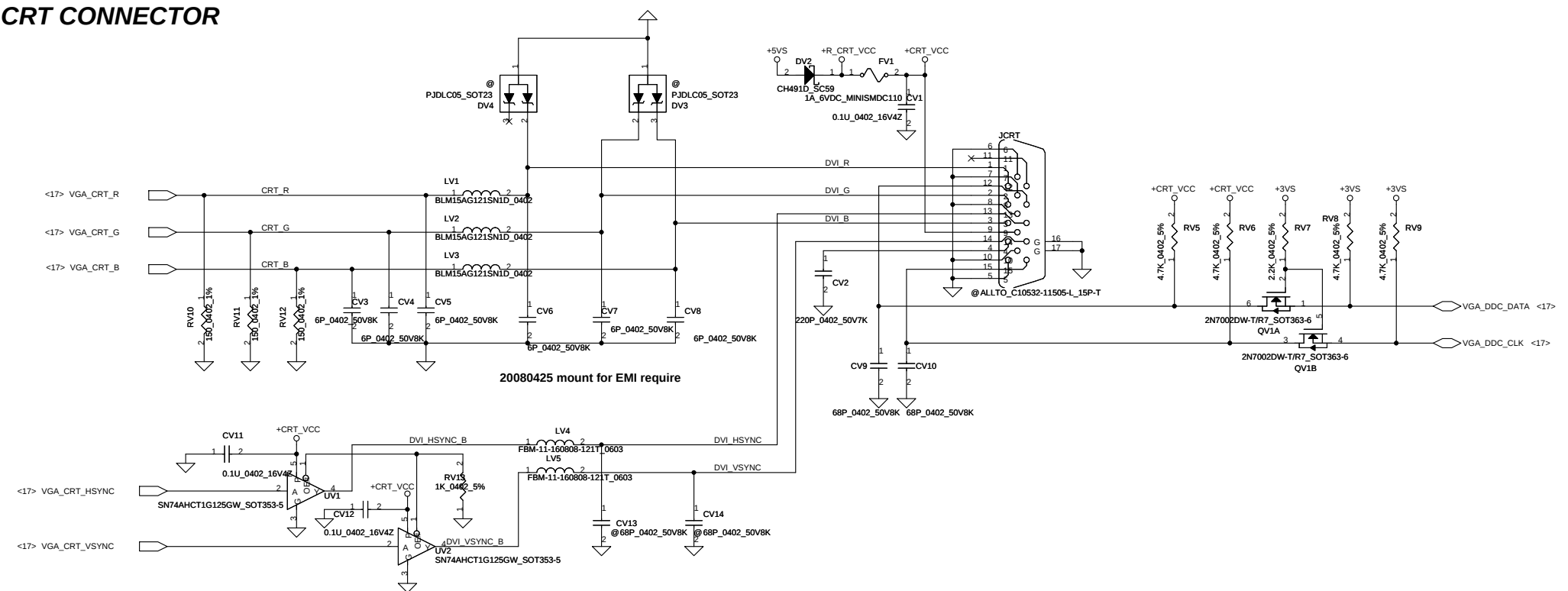
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VGA BOARD Conn.



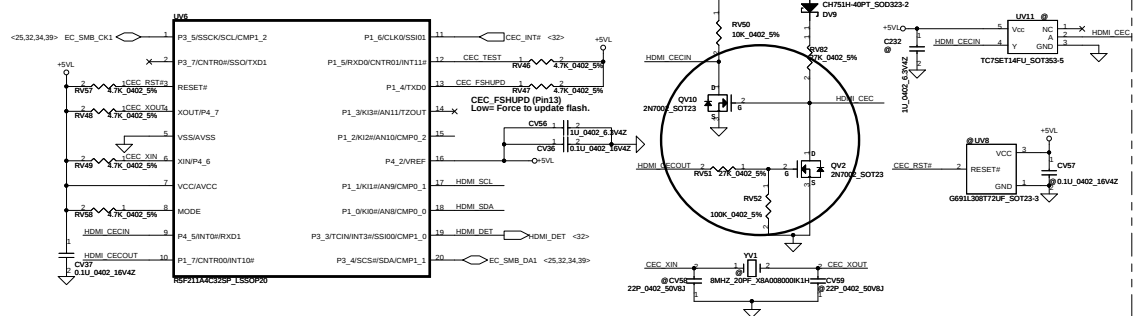
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				SCHEMATIC, MB A4471		
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CRT CONNECTOR

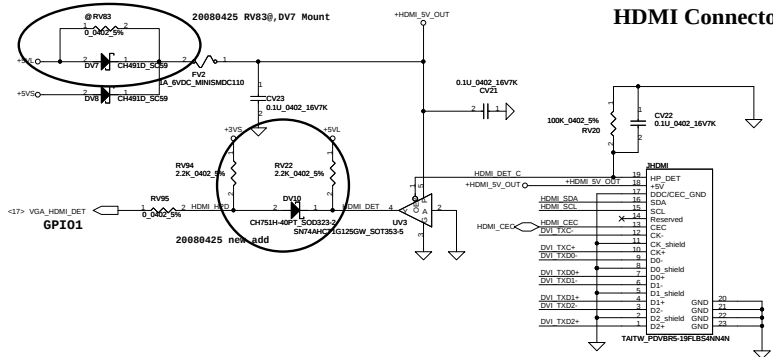


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				Size	Document Number
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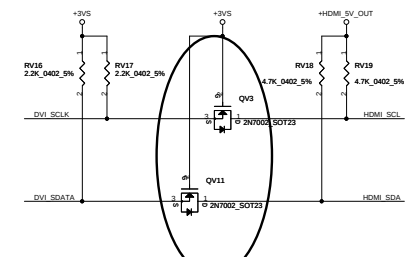
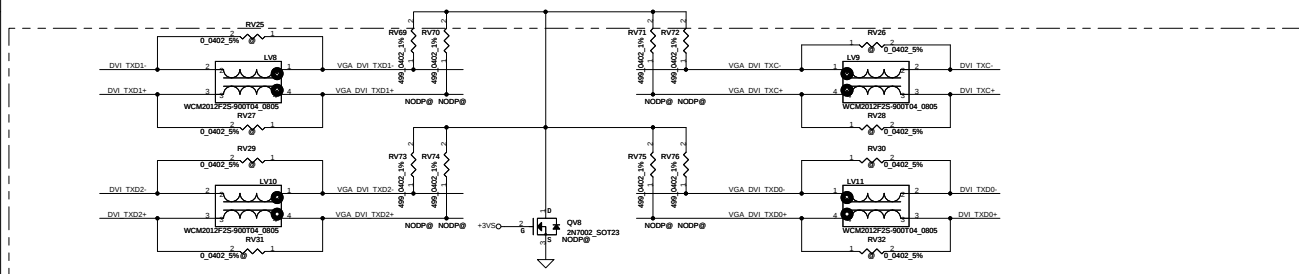
HDMI CEC Controller



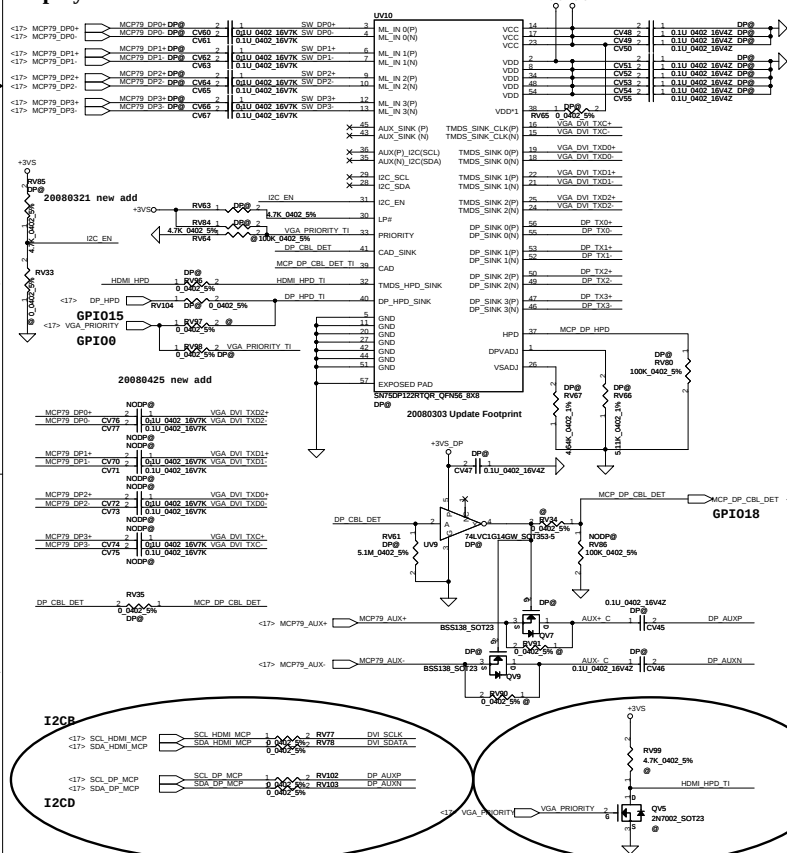
HDMI Connector



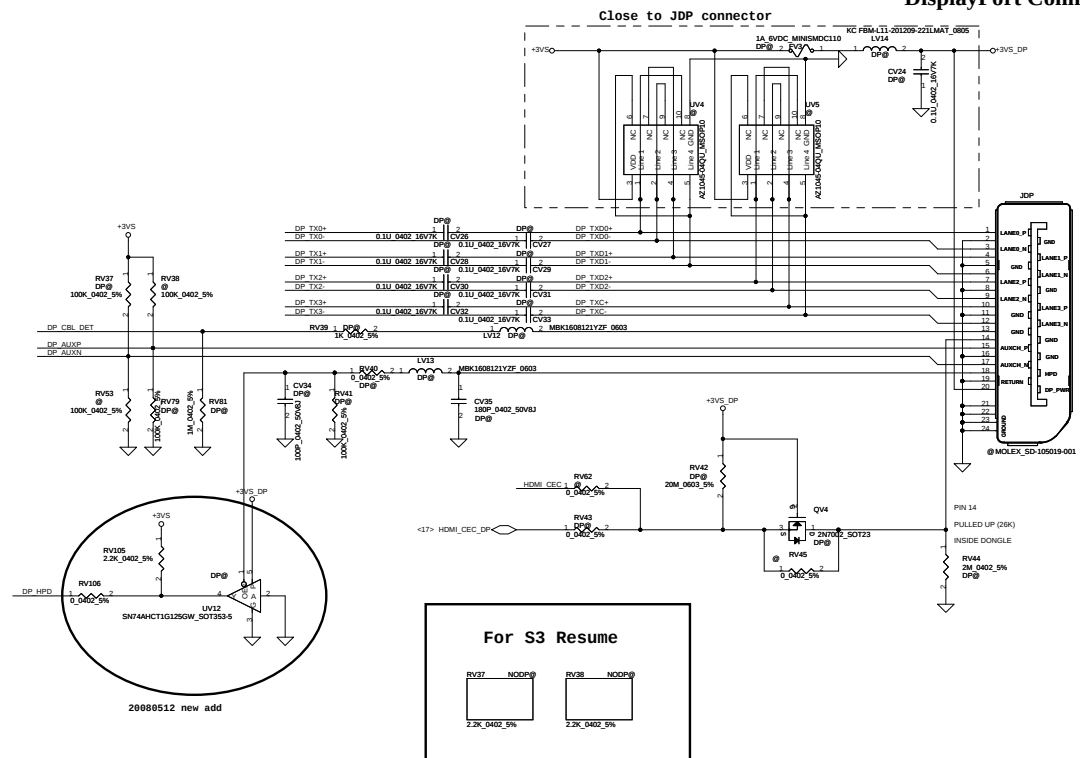
Close to JHDMI connector



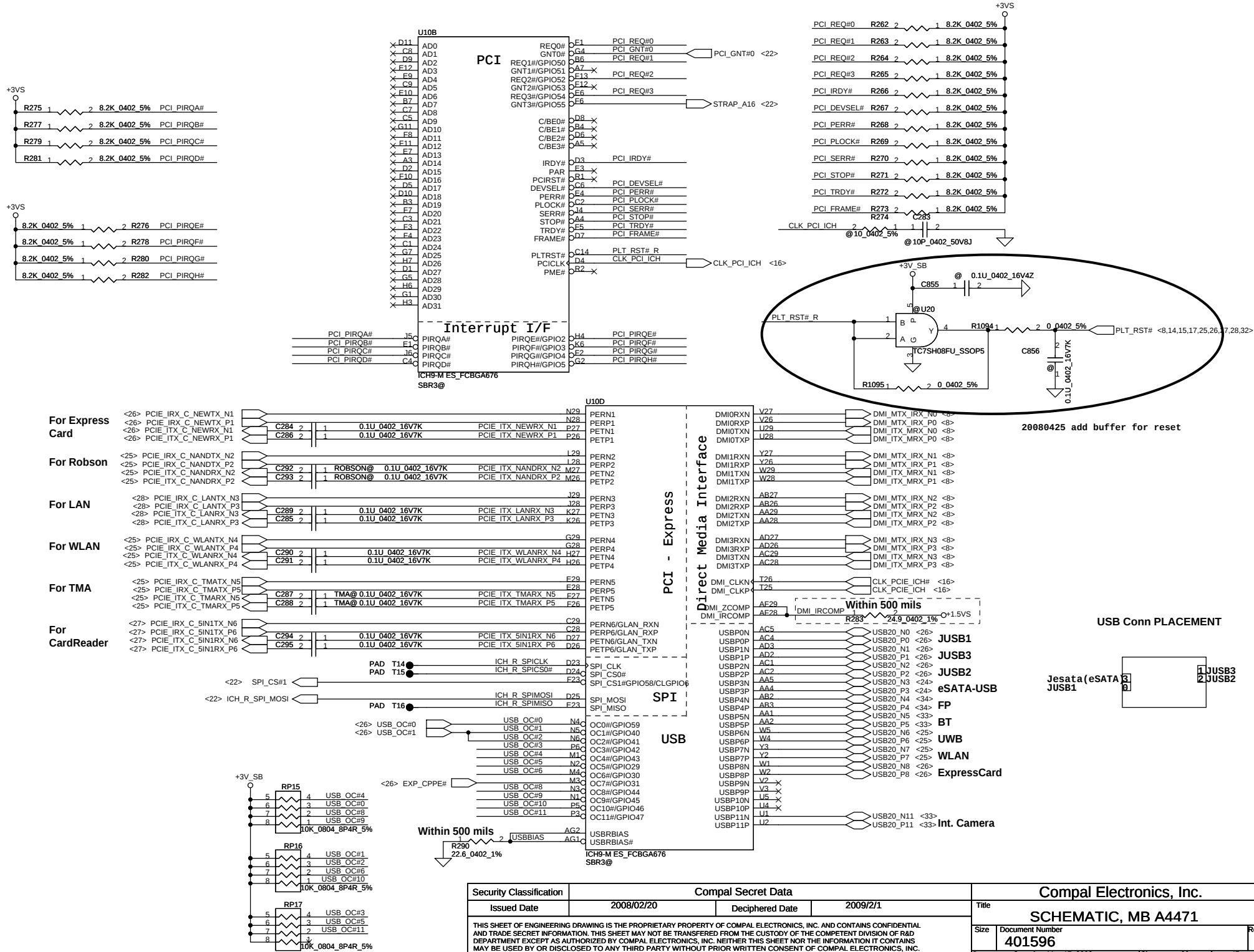
DisplayPort/TMDS 1:2 Switch/Translator

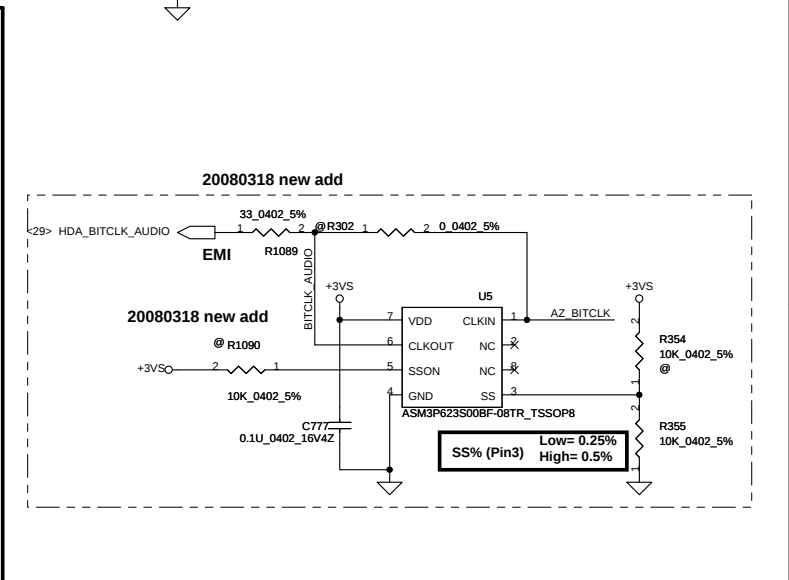


DisplayPort Connector

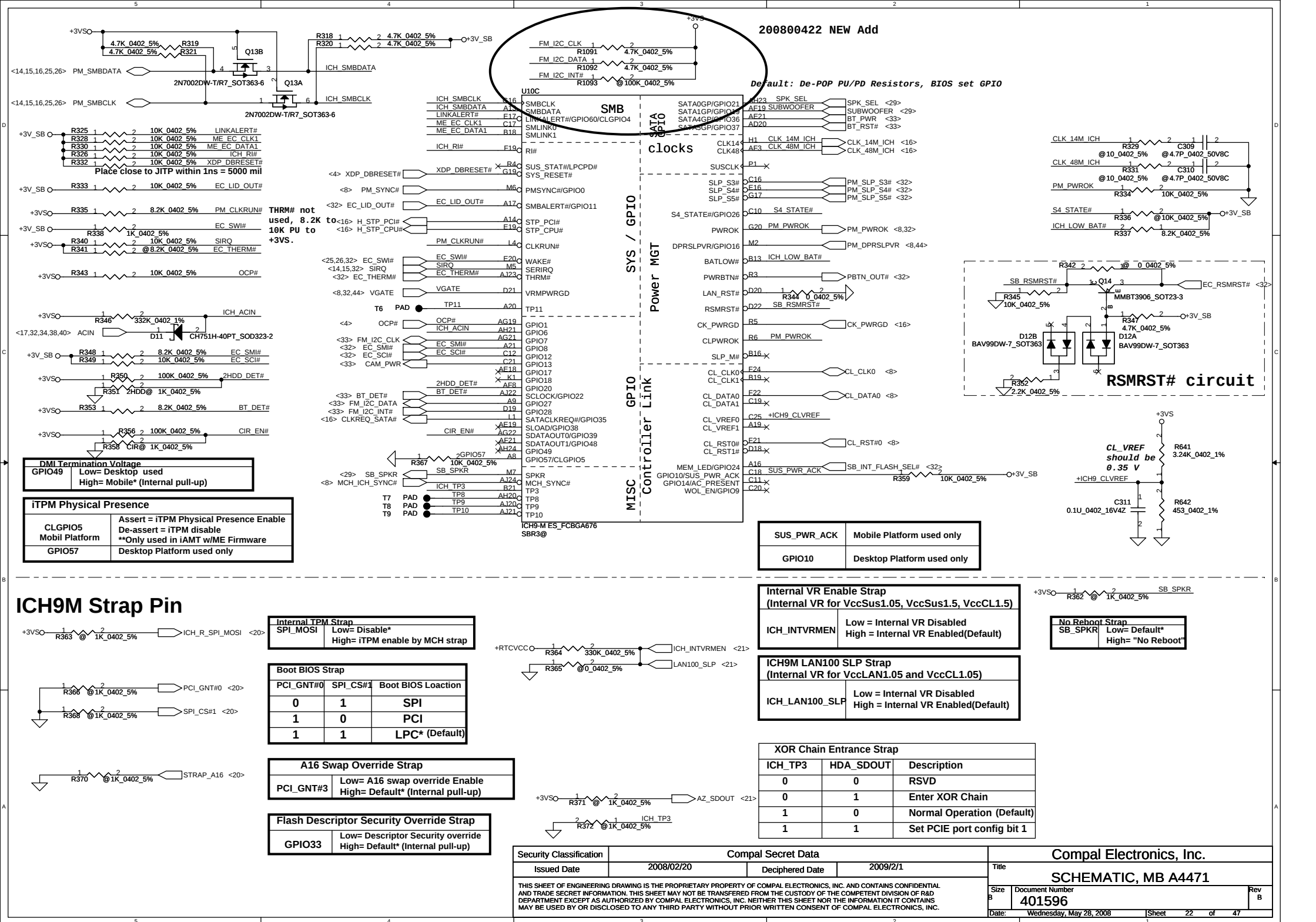


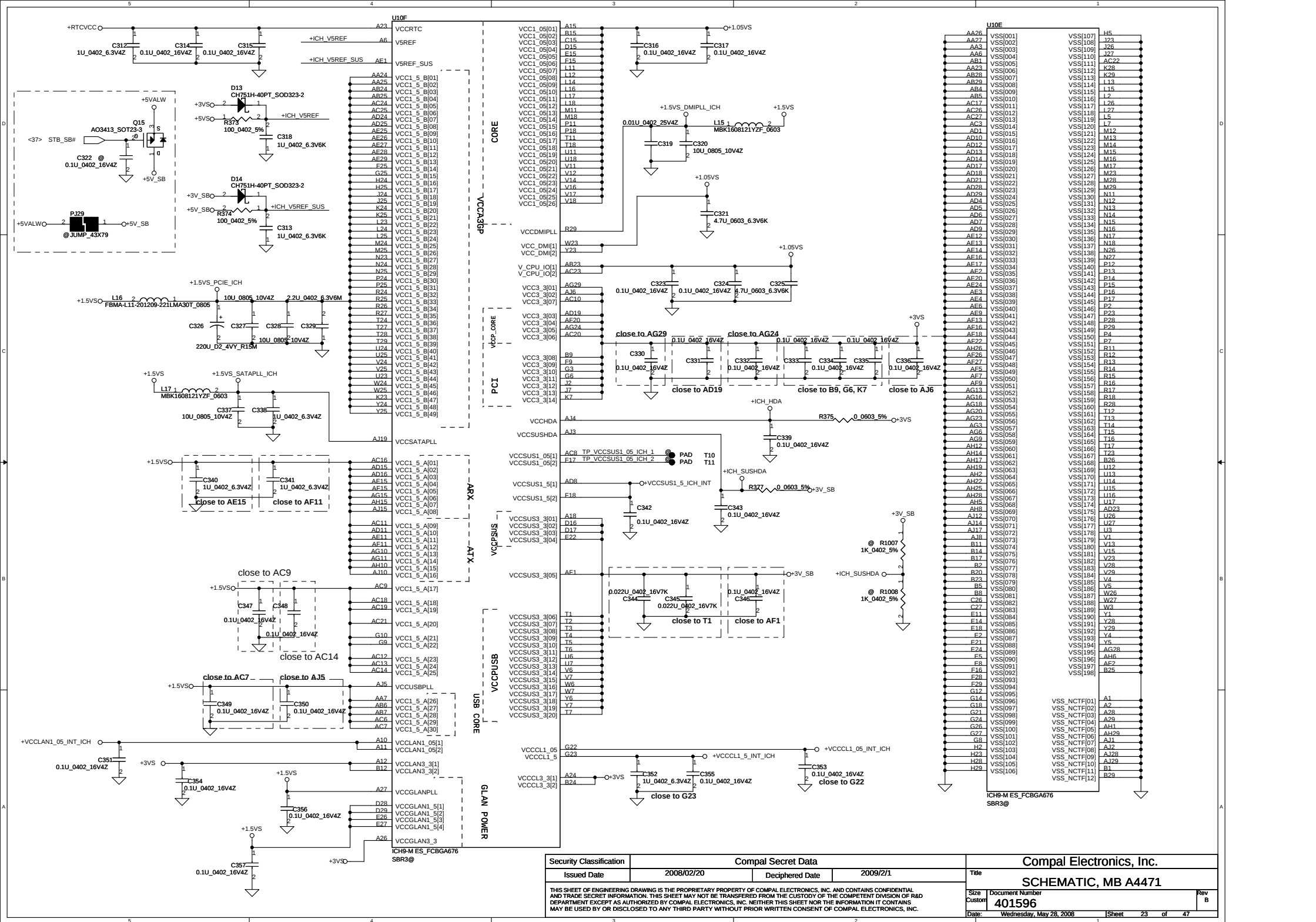
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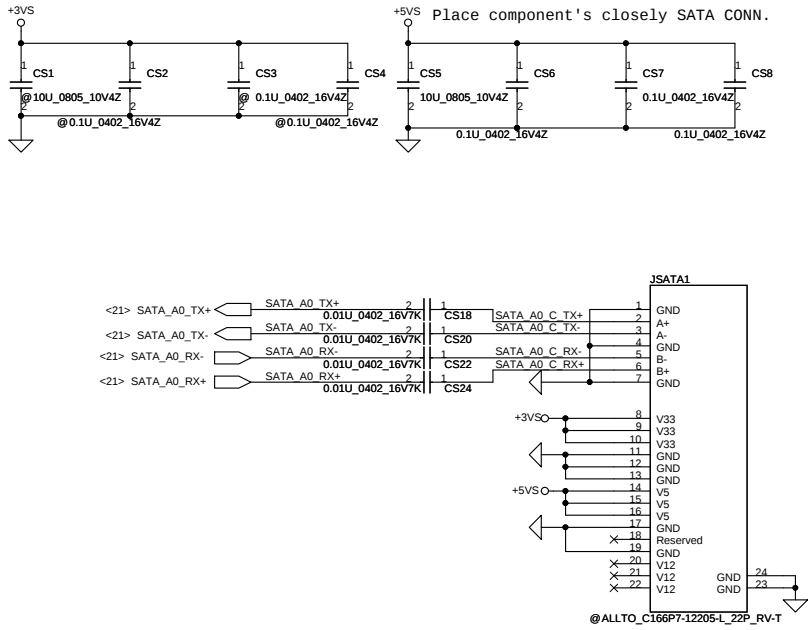


5	4	3	2	1
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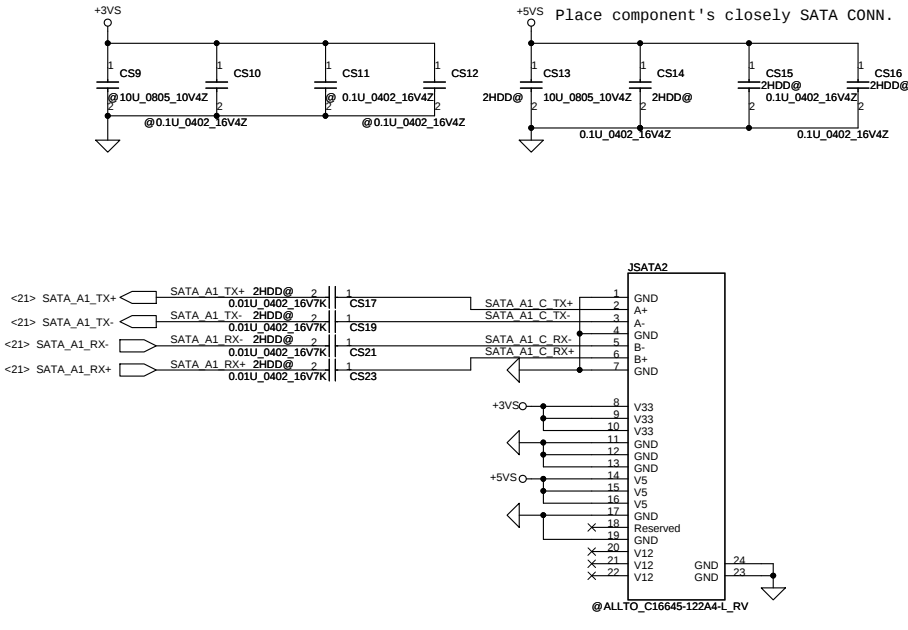




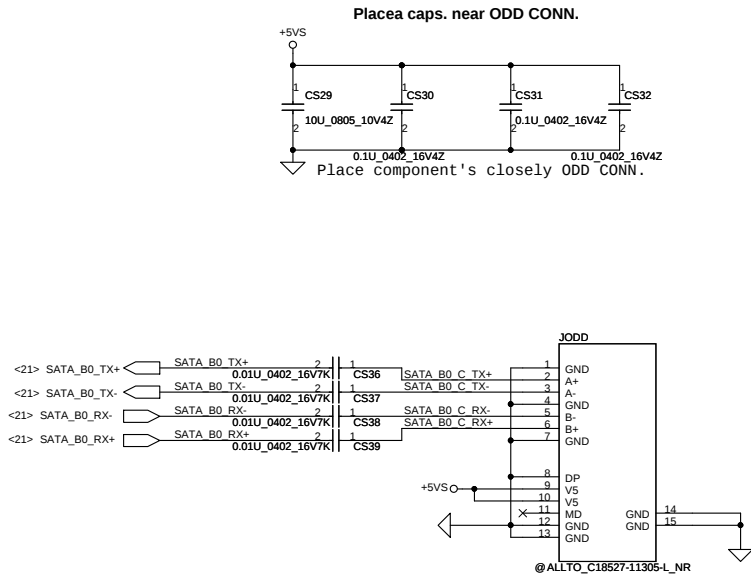
SATA Main HDD Conn.(11.8mm)



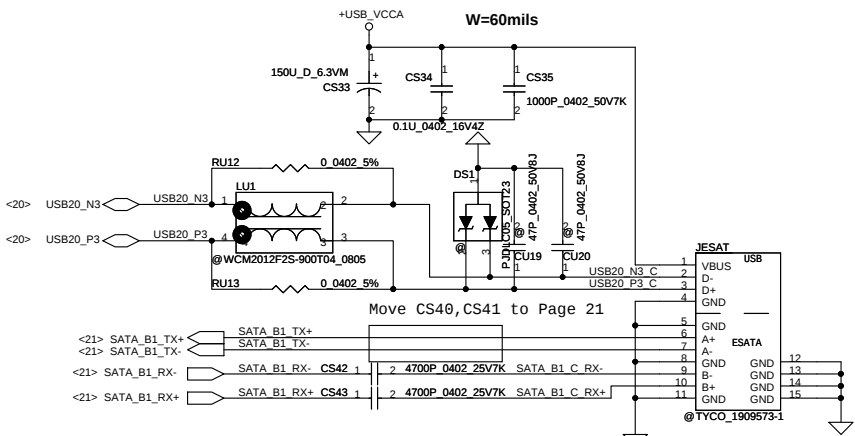
SATA 2 nd HDD Conn.(5.2mm)



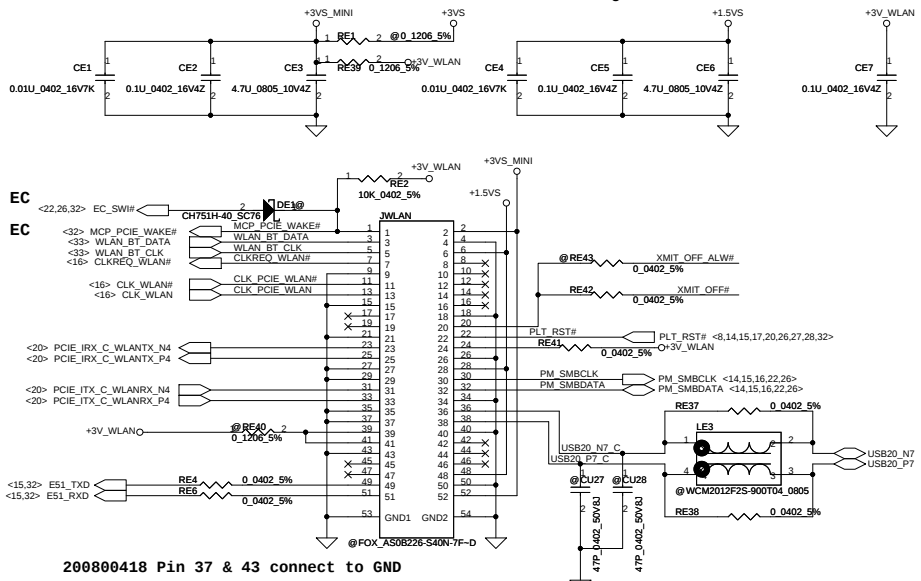
SATA ODD CONN



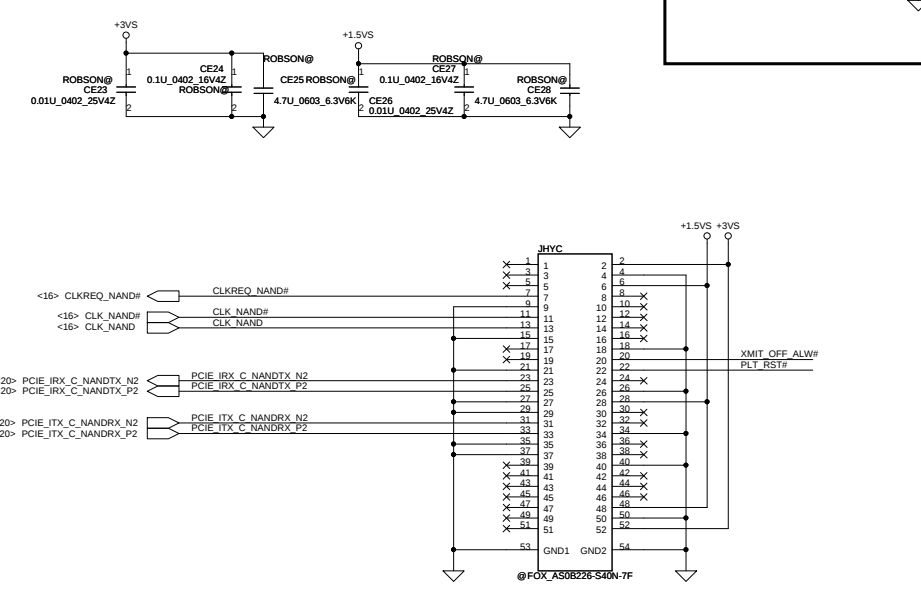
eSATA + USB CONN



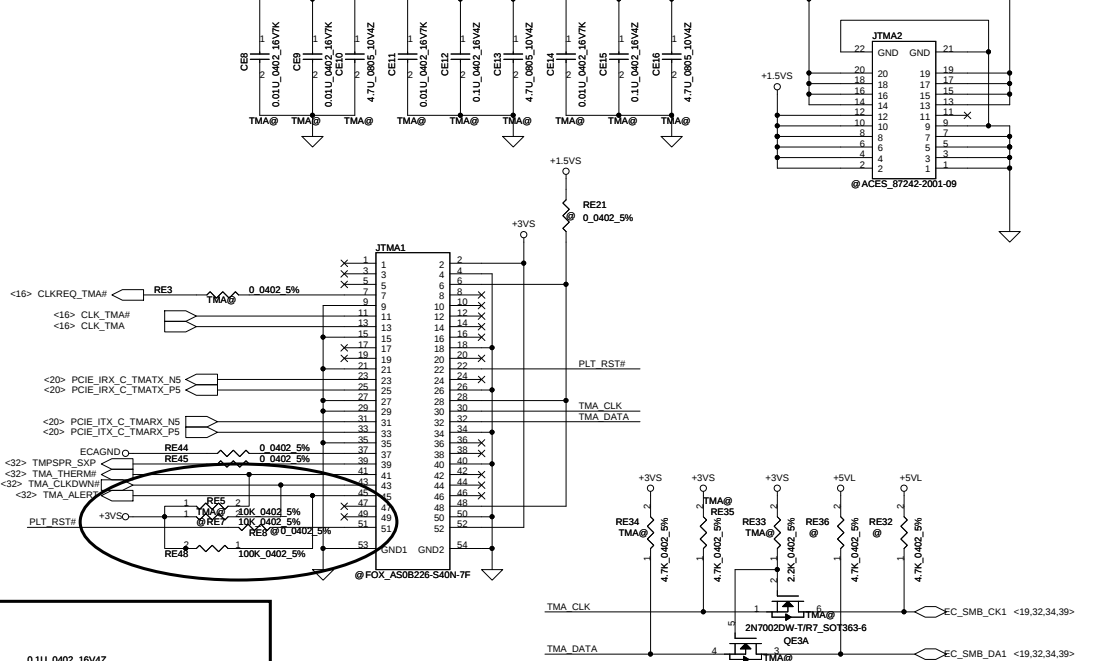
Mini-Express Card for WLAN



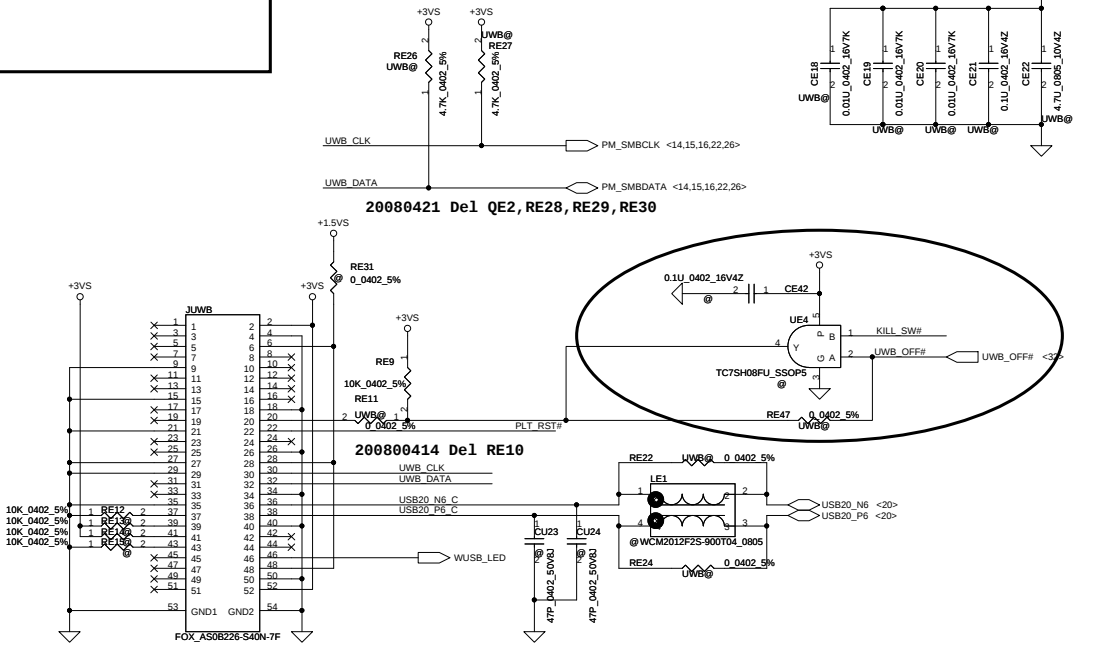
ROBSON



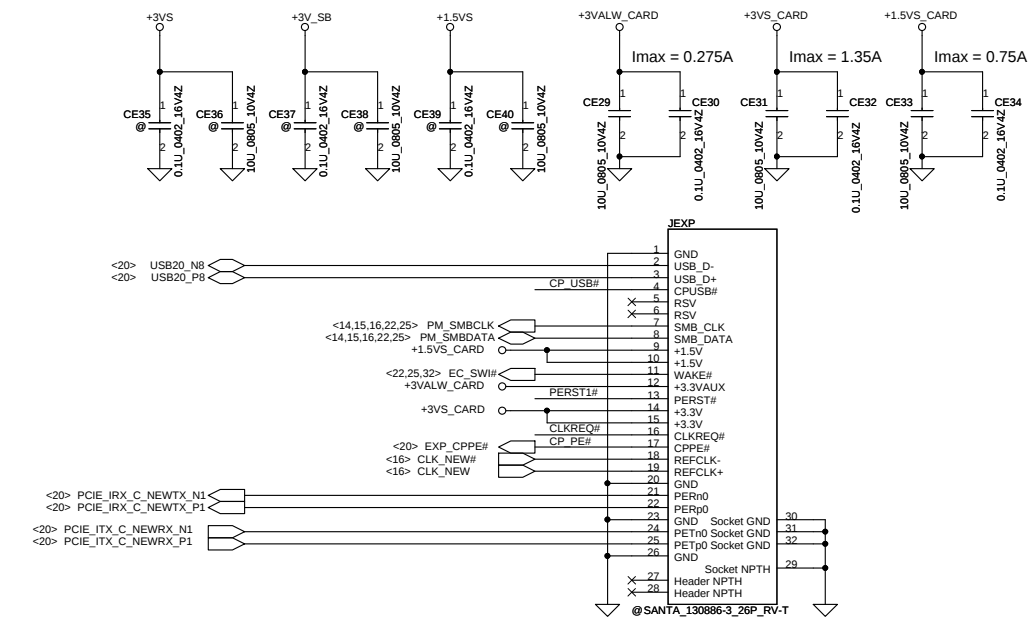
TMA mini Card



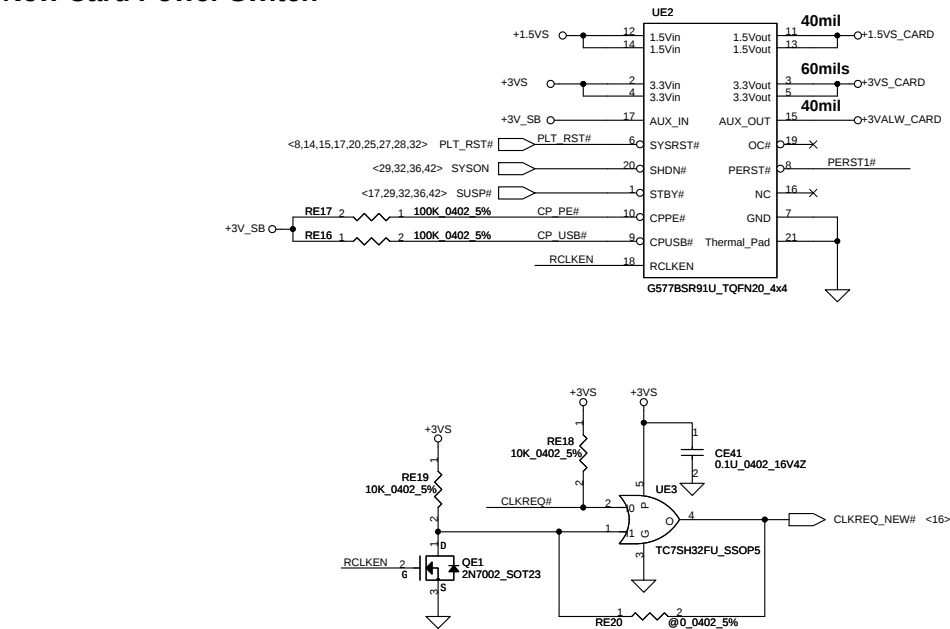
UWB mini Card



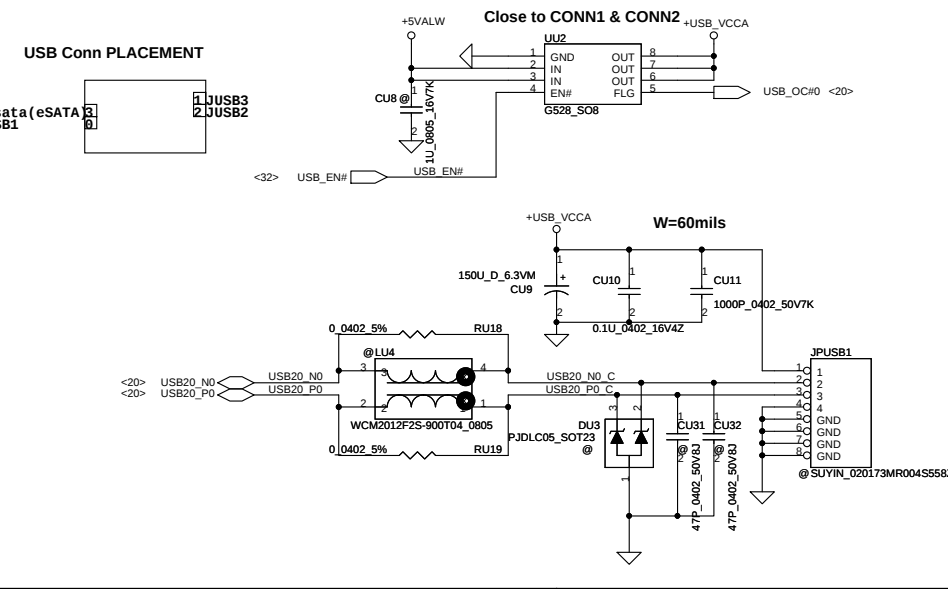
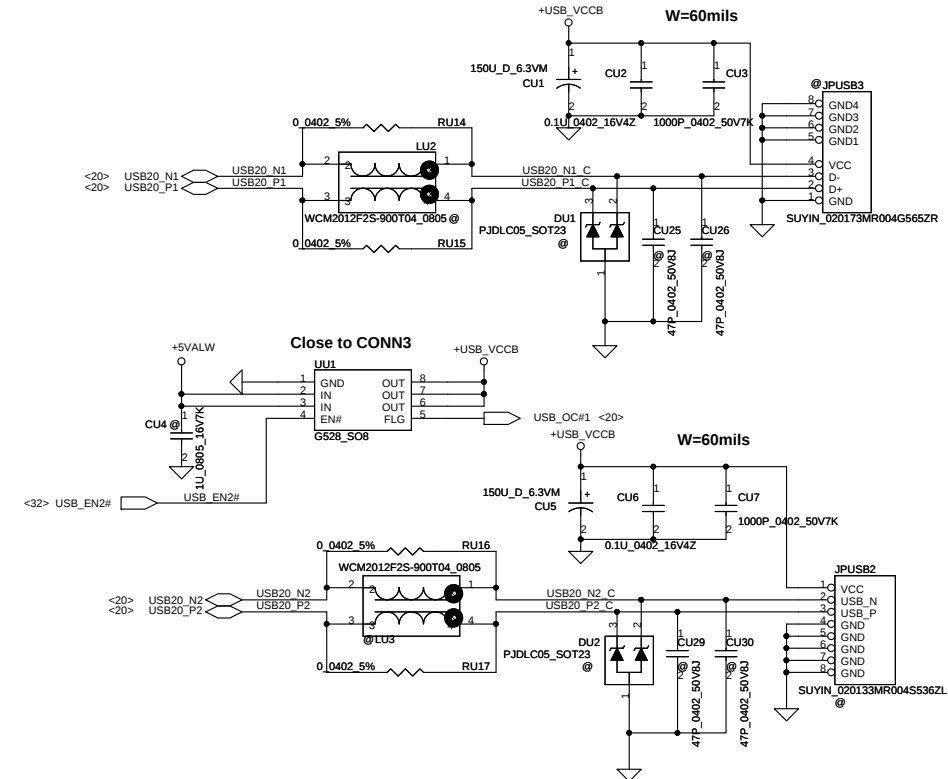
New Card Interface



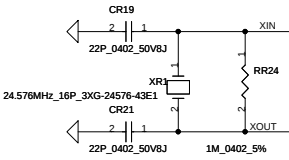
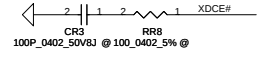
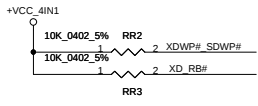
New Card Power Switch



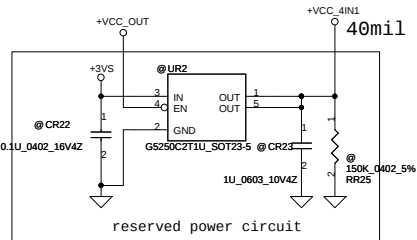
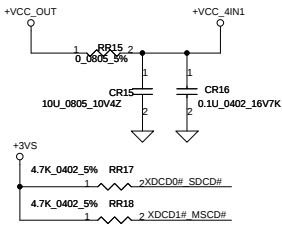
USB Interface



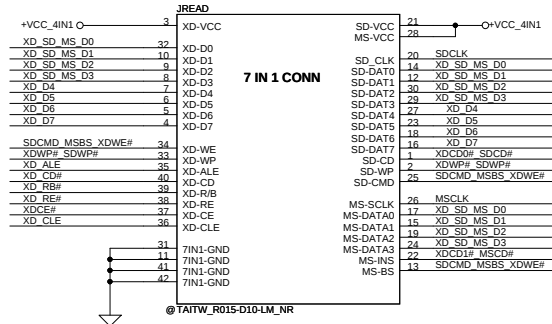
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Deciphered Date				2008/10/25				SCHEMATIC, MB A4471			
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				Date				Saturday, May 17, 2008			
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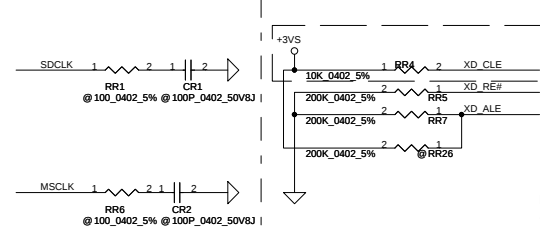
Use 0603 type and over 20 mils trace width on both side



Card Reader Connector



Strap pin for JMicro

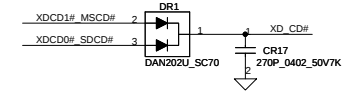
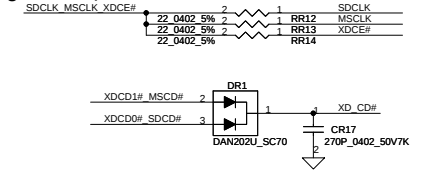


Strapping setting

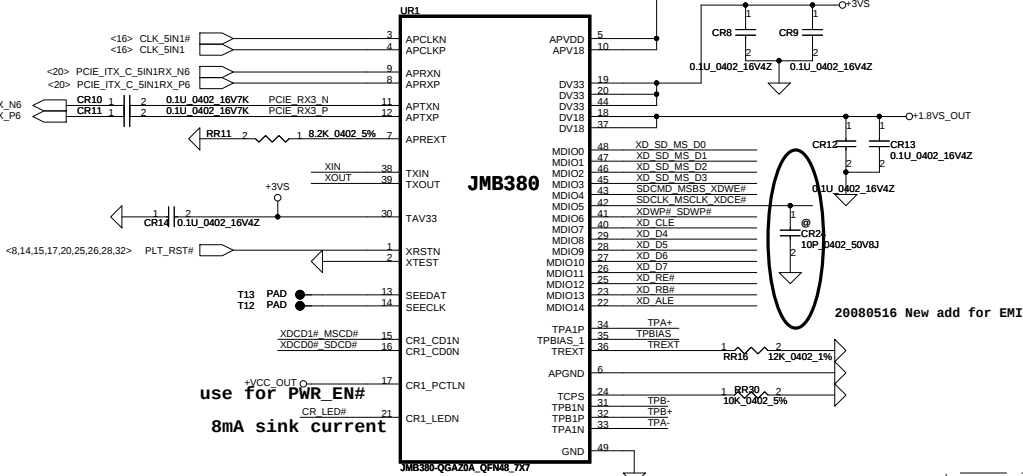
Pin name	Description	
	High	Low
MDIO7	on-board★	add-in card
MDIO12	+VCC_OUT high active	+VCC_OUT low active★
MDIO14	CR_LED high active★	CR_LED low active

P.S CR1_PCTLN aslo can out 3V with 250mA for 5IN1 using.(MDIO12 can't be seted after MP IC)

Change RR12, RR13 and RR14 to Bead for EMI

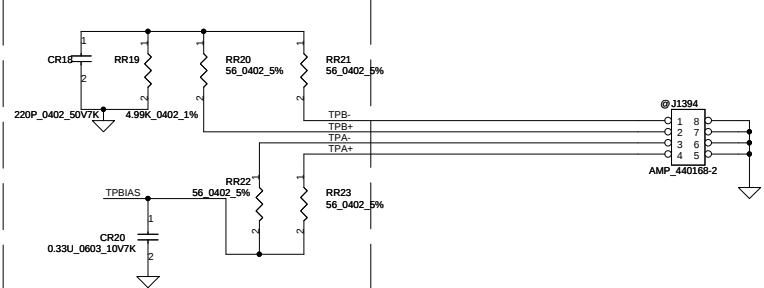


Power Circuit

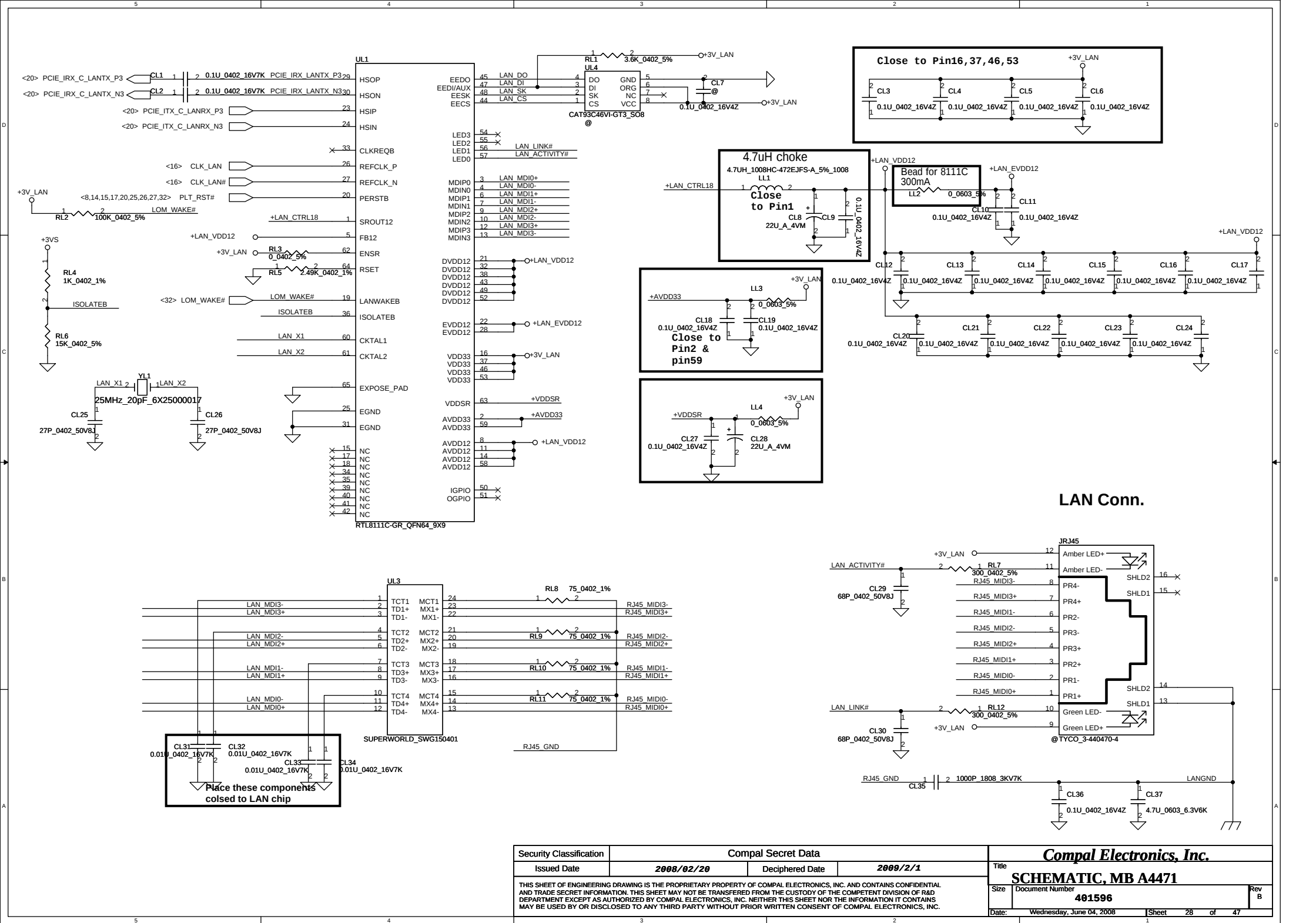


use for PWR_EN#
8mA sink current

Close to Chip

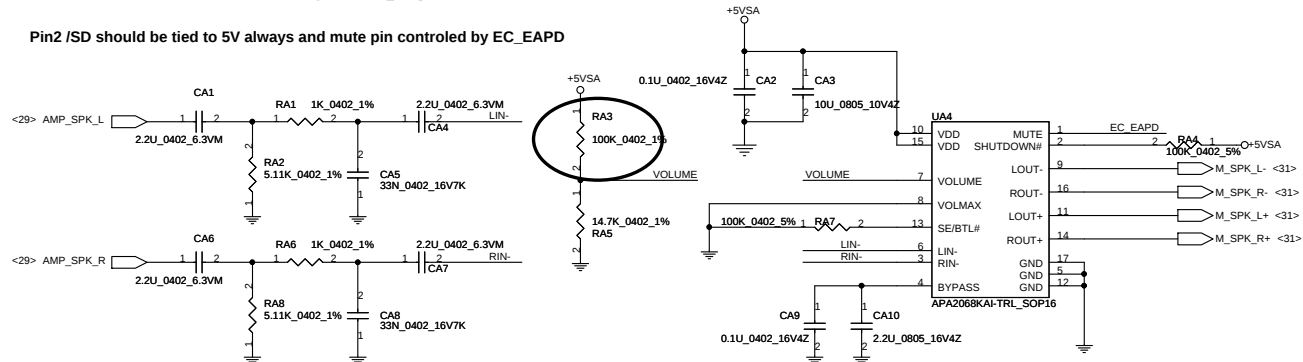


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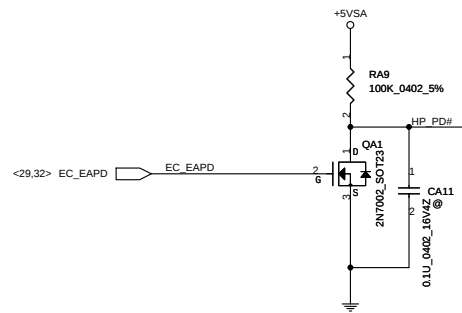
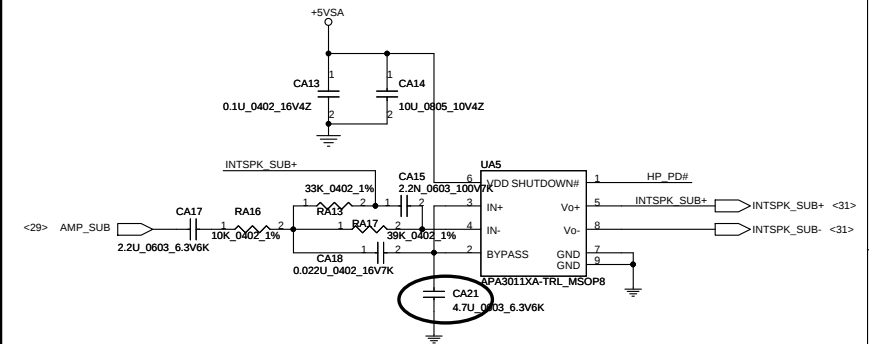


APA2068 Medium Range Amplifier

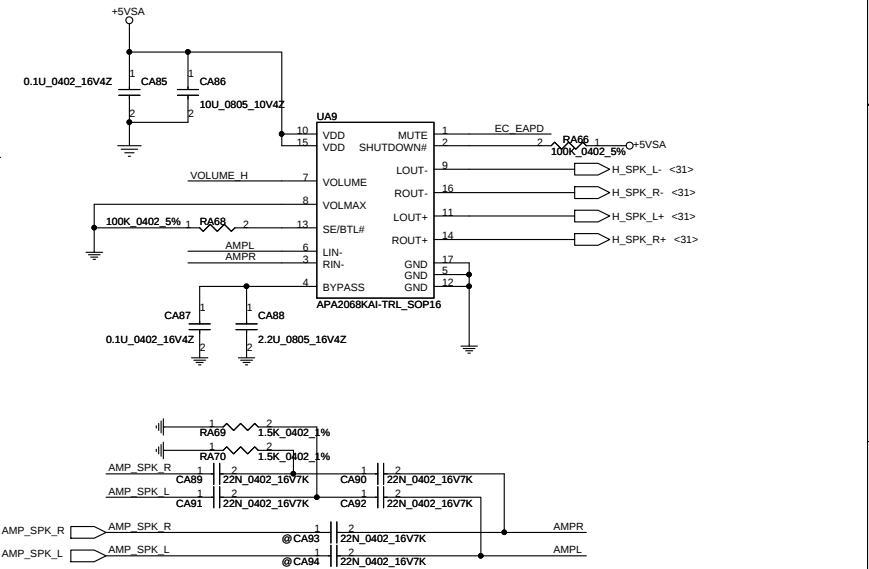
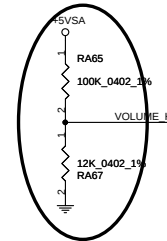
Pin2 /SD should be tied to 5V always and mute pin controlled by EC_EAPD



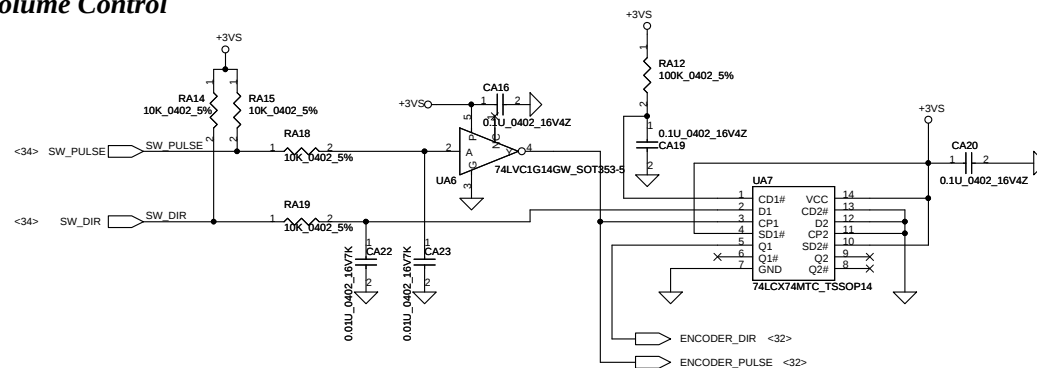
APA3011 Subwoofer Amplifier



APA2068 Tweeter Range Amplifier

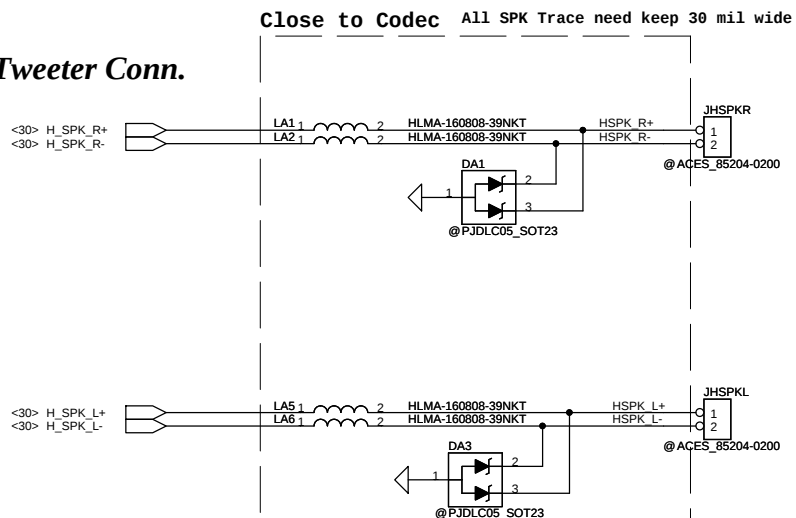


Volume Control

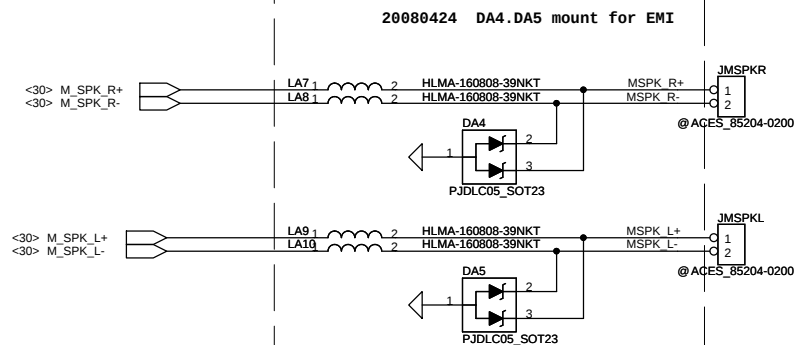


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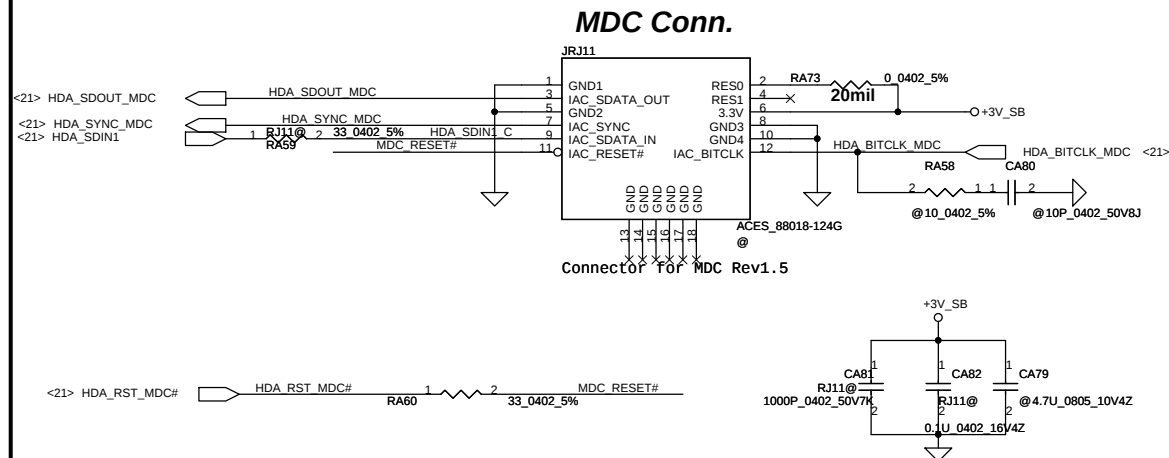
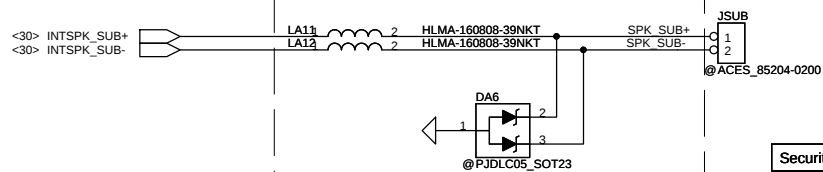
Tweeter Conn.



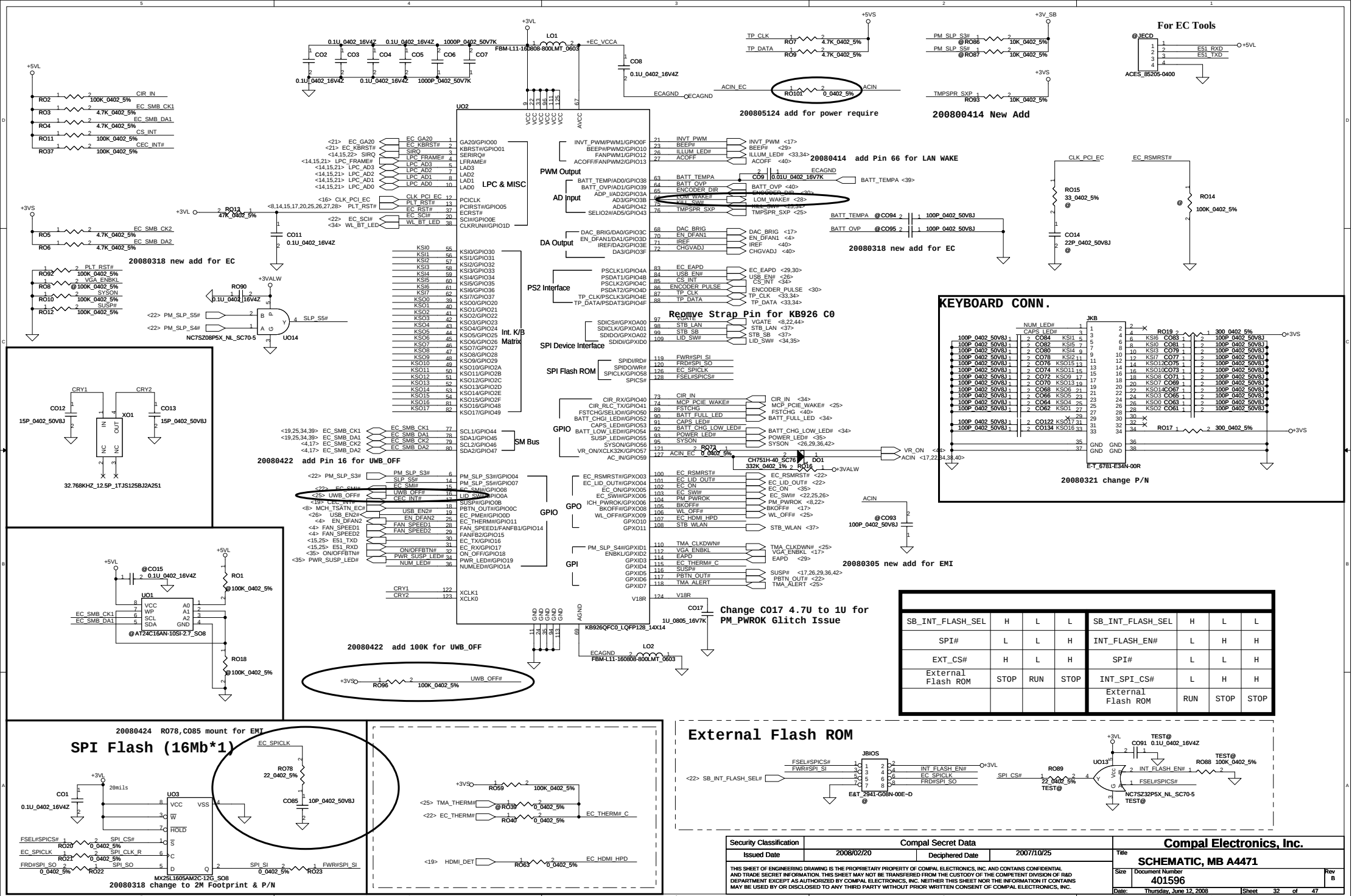
Medium SPK Conn.



Sub-woofer Conn.



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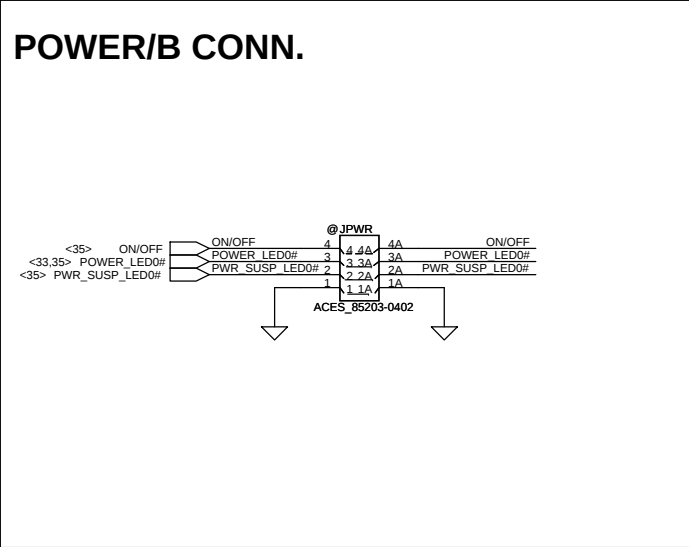


POWER/B CONN.

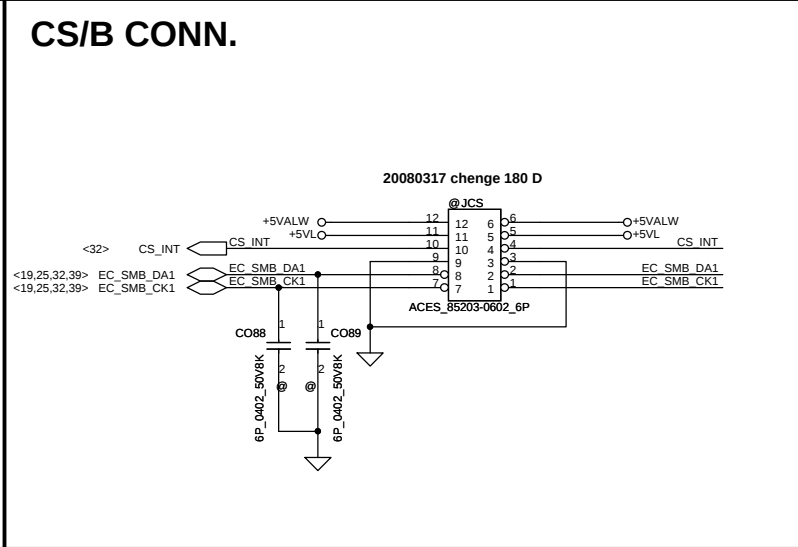
The diagram illustrates the power and control connections for the ACES_85203-0402 component. It features a central component symbol with pins labeled 1, 2, 3, 4, 1A, 2A, 3A, and 4A. The connections are as follows:

- Pin 1:** Connected to the **PWR_SUSP_LED0#** signal.
- Pin 2:** Connected to the **PWR_SUSP_LED0#** signal.
- Pin 3:** Connected to the **POWER_LED0#** signal.
- Pin 4:** Connected to the **ON/OFF** signal.
- Pin 1A:** Connected to the **PWR_SUSP_LED0#** signal.
- Pin 2A:** Connected to the **PWR_SUSP_LED0#** signal.
- Pin 3A:** Connected to the **POWER_LED0#** signal.
- Pin 4A:** Connected to the **ON/OFF** signal.

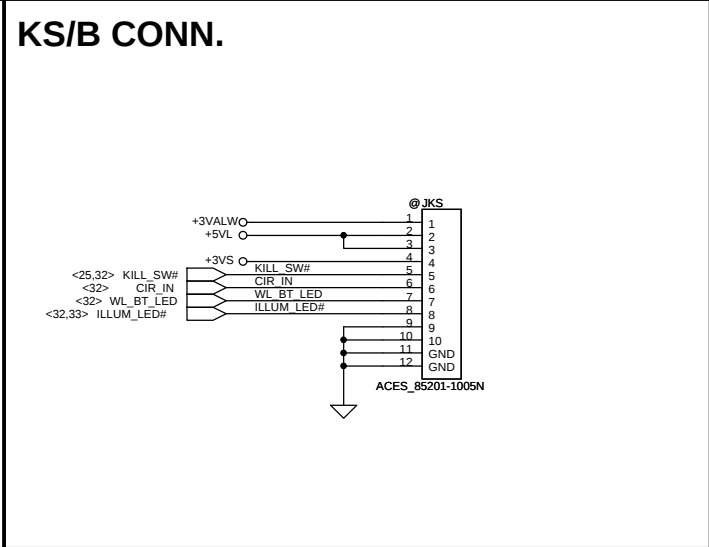
The component is identified as **ACES_85203-0402** and is connected to a power source labeled **@JPWR**. The signals **POWER_LED0#** and **PWR_SUSP_LED0#** are shown as active-low signals, indicated by the '#' symbol.



CS/B CONN.



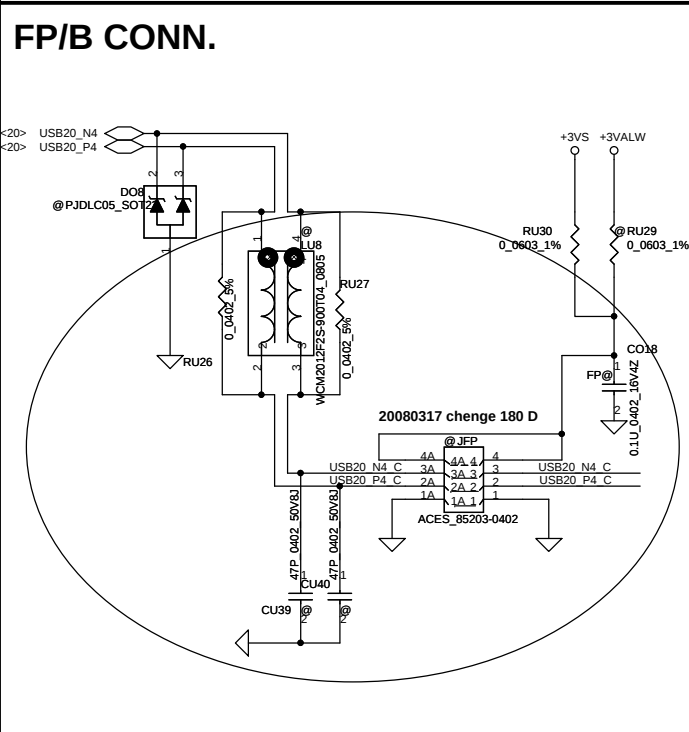
KS/B CONN.



FP/B CONN.

The schematic diagram illustrates the electrical connections for the FP/B interface. Key components and their connections include:

- Inputs:** USB20_N4 and USB20_P4 are connected to a diode (D04) and a resistor (RU26) network.
- Resistors:** RU27 (0.0402 5% and 0.0402 5%), RU29 (0.0603 1%), and RU30 (0.0603 1%) are used for signal conditioning.
- Capacitors:** CU39 (47P 0402 50V/8J) and CU40 (47P 0402 50V/8J) are connected to ground.
- Diodes:** D04 is a Schottky diode, and C04 is a Zener diode (1V4Z).
- Integrated Circuits:** WCNM2012FS-900T04_0805 is a transformer, and ACES_85203-0402 is a component with multiple pins.
- Power and Ground:** +3VS and +3VALV are power inputs, and FP is a ground connection.



LED/B CONN.

20080317 chenge to 20 Pin Conn

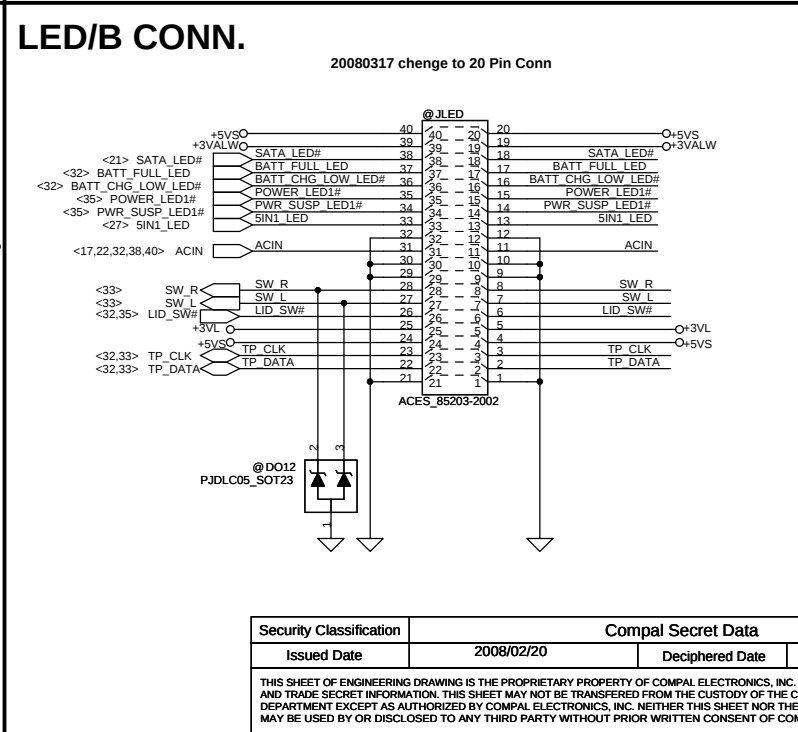
LED/B CONN.

20080317 chenge to 20 Pin Conn

ACES_85203-2002

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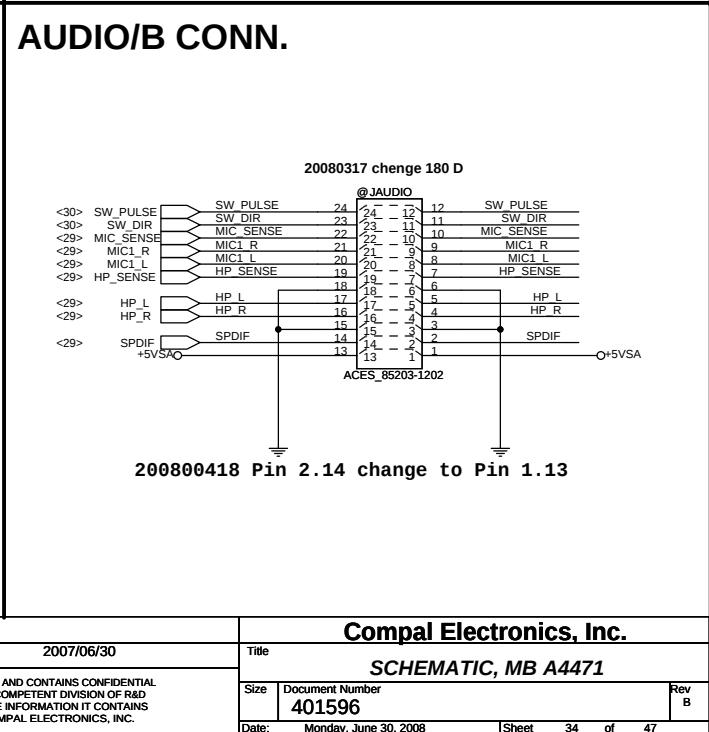
AUDIO/I/O CONN.

20080317 chenge 180 D

@AUDIO

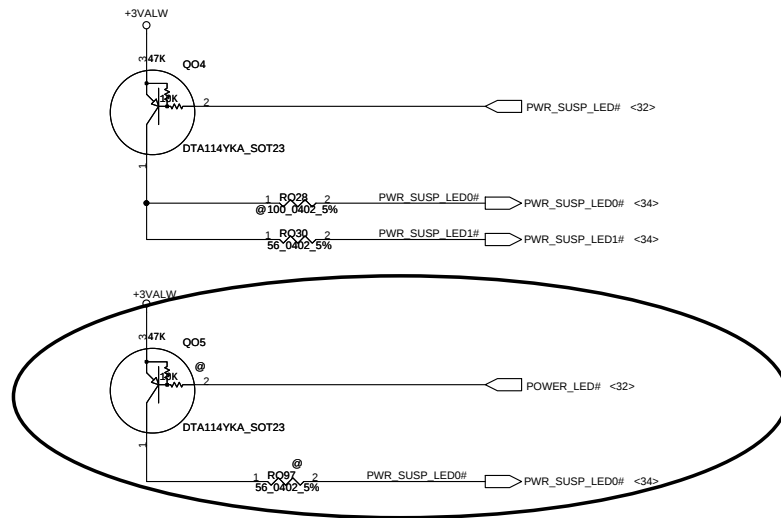
200800418 Pin 2.14 change to Pin 1.13

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				SCHEMATIC, MB A4471	
AND CONTAINS CONFIDENTIAL COMPONENT DIVISION OF R&D INFORMATION IT CONTAINS MPAL ELECTRONICS, INC.		Size		Document Number	
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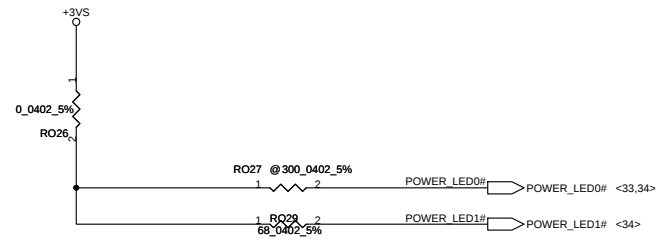


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				Date:	Monday, June 30, 2008	Sheet 34 of 47

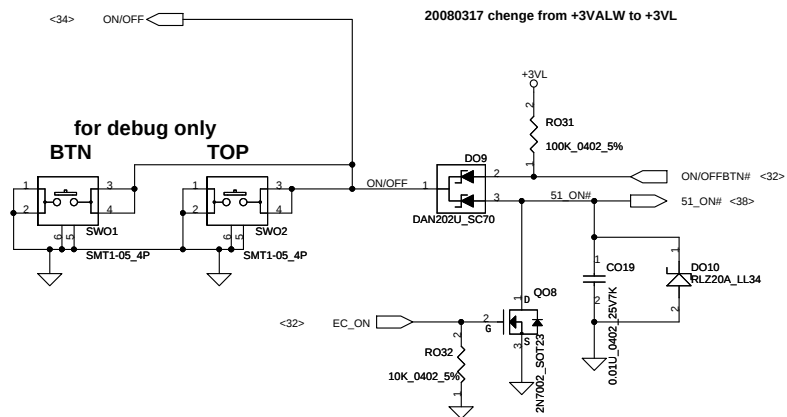
Power Suspend LED



Power on LED

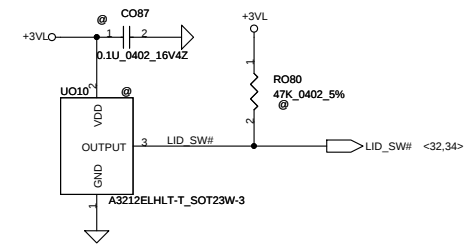


ON/OFF BUTTON



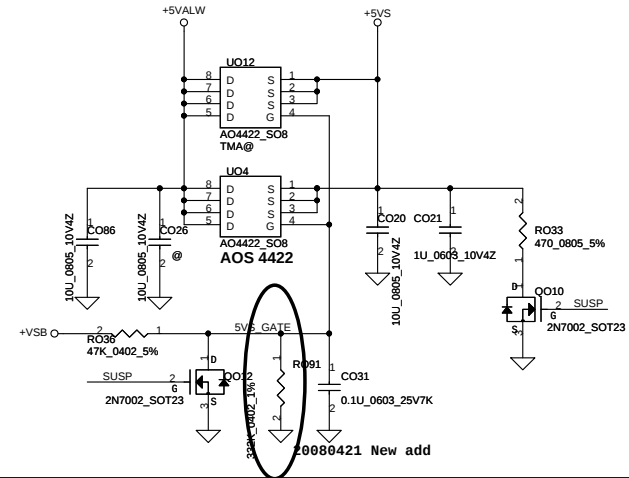
Lid SW

Change LID Switch to LED/B for S3 Issue

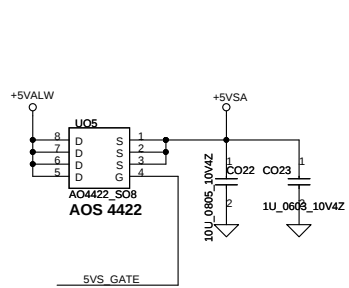


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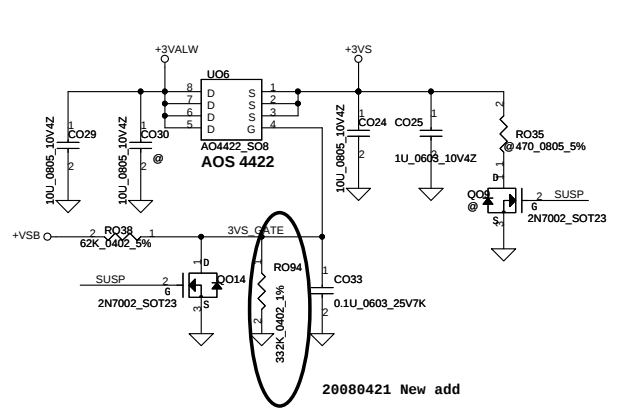
+5VALW TO +5VS



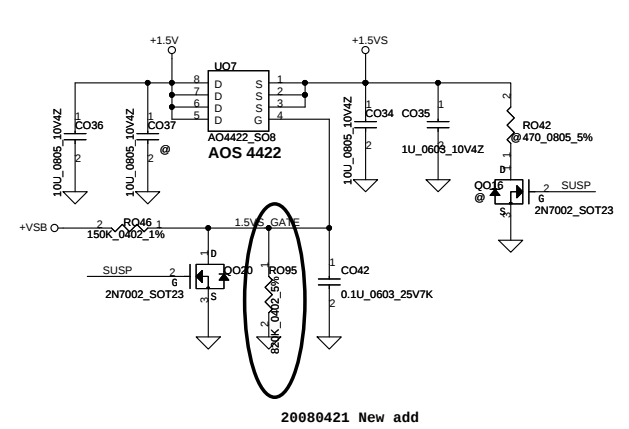
+5VALW TO +5VSA (For Amp)



+3VALW TO +3VS

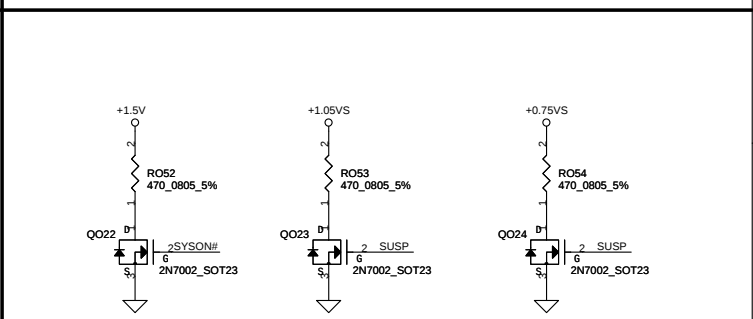
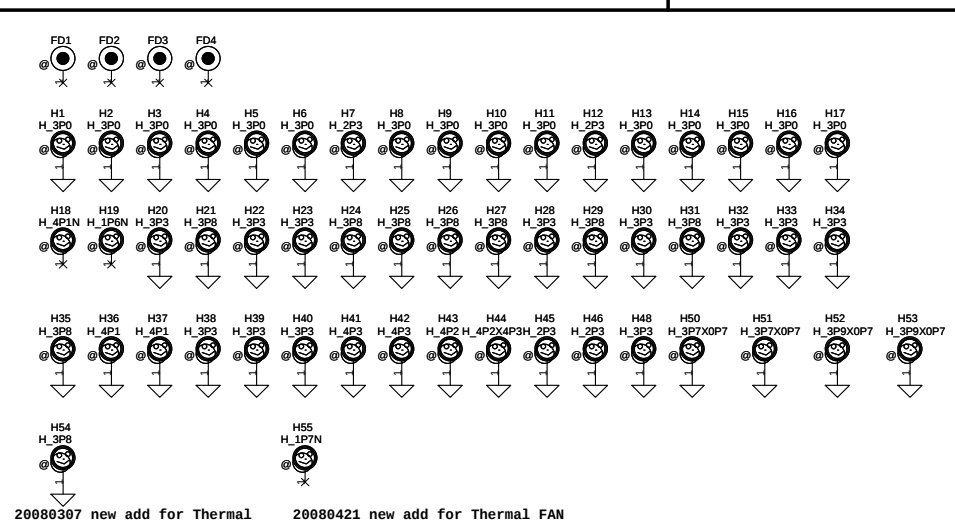
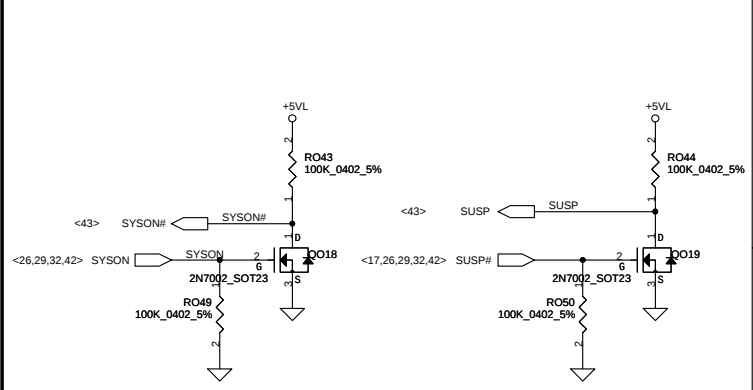


+1.5V to +1.5VS

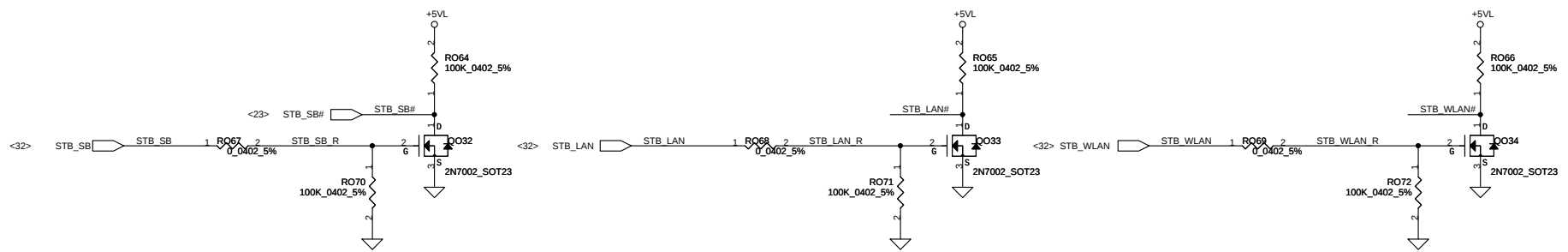
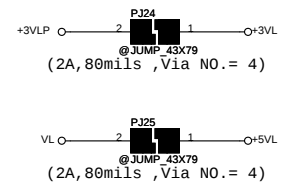
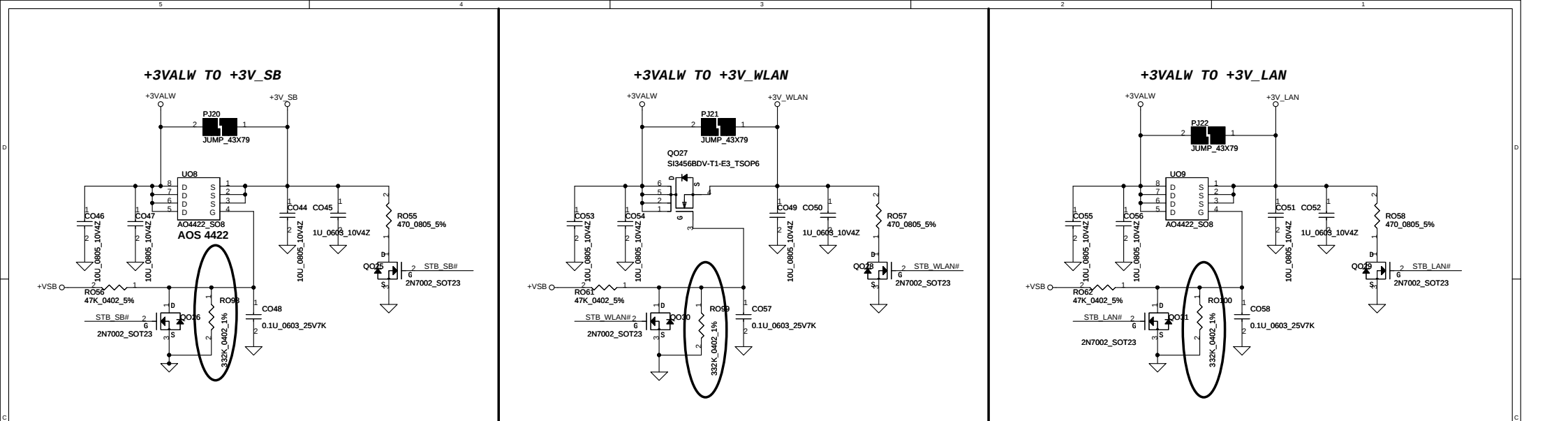


+1.1VALW to +1.1VS

20080305 del 1.1V switch

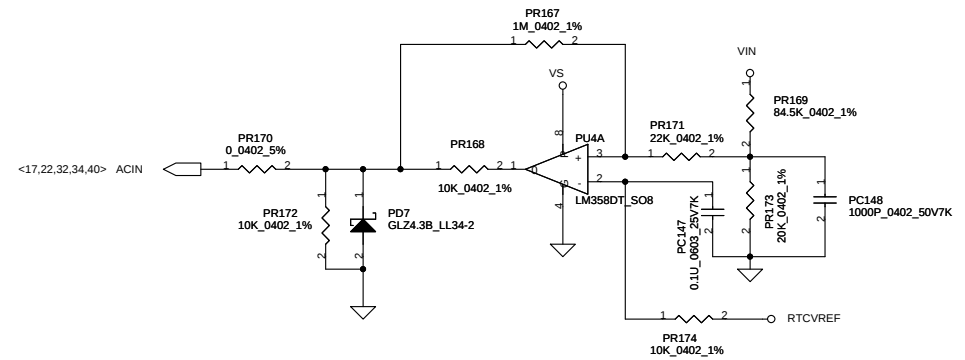
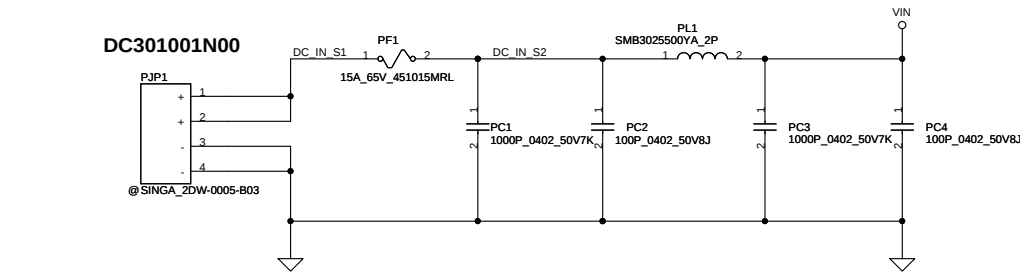


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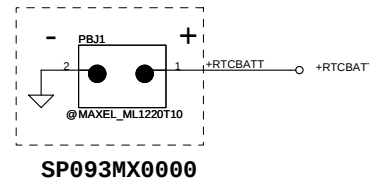
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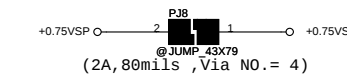
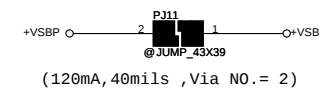
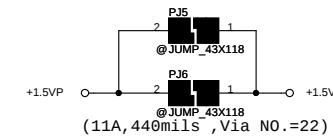
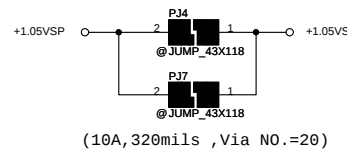
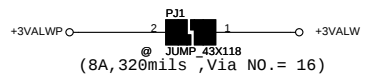
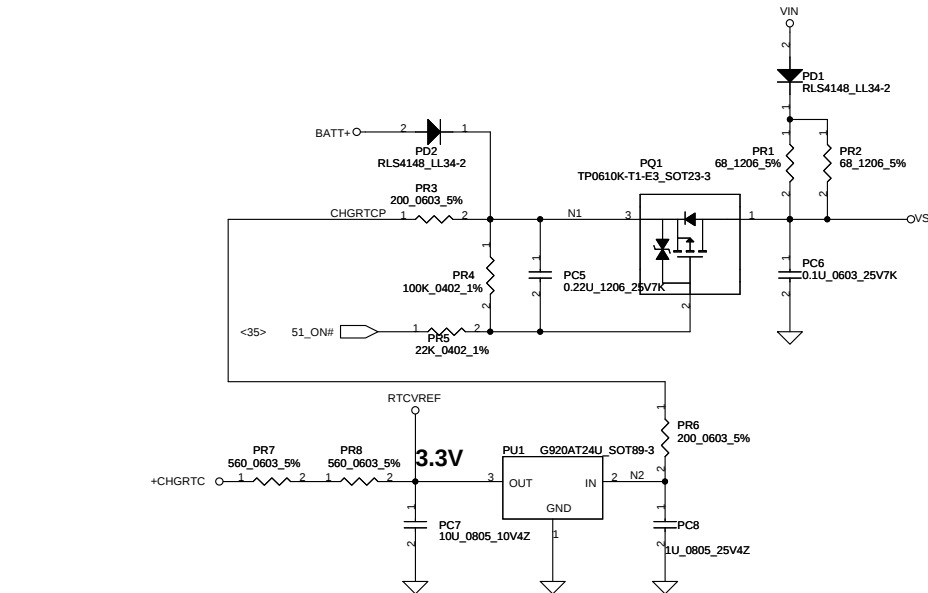
Vin Detector

High 18.384 17.901 17.430
Low 17.728 17.257 16.976

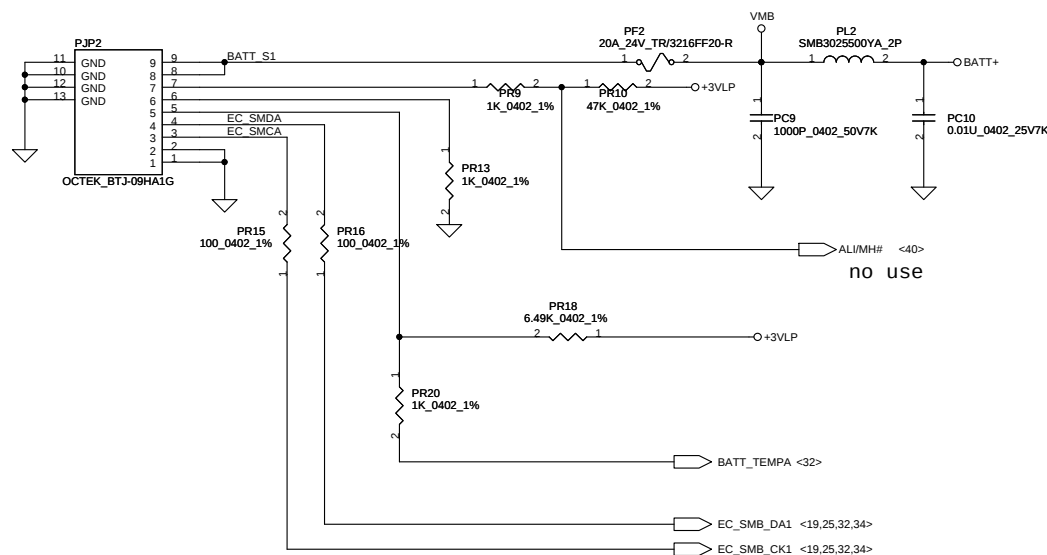
RTC Battery



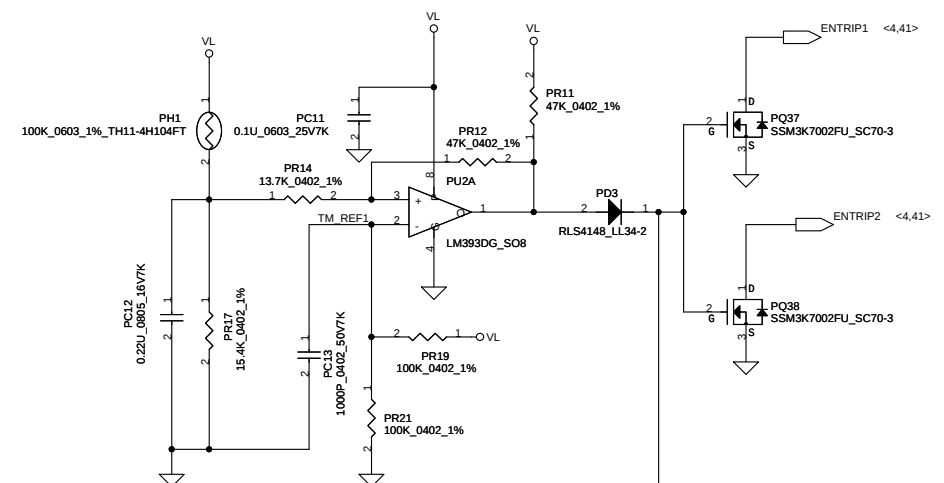
SP093MX0000



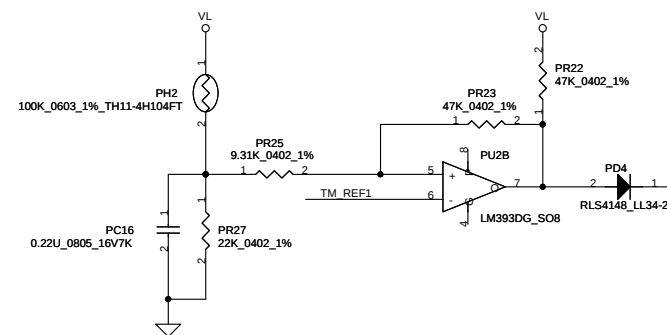
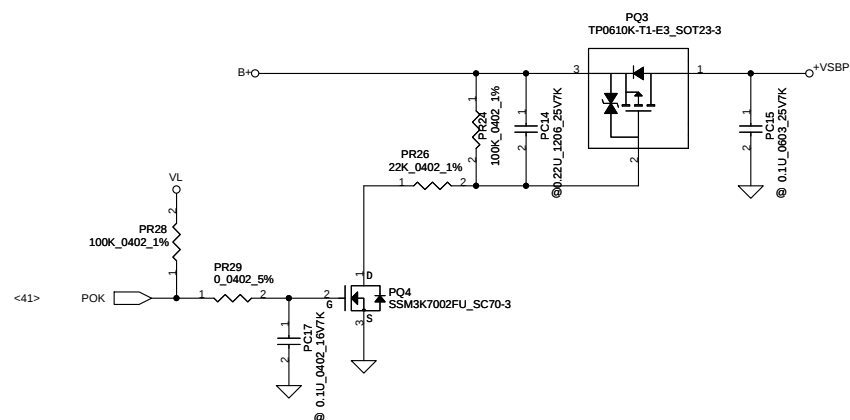
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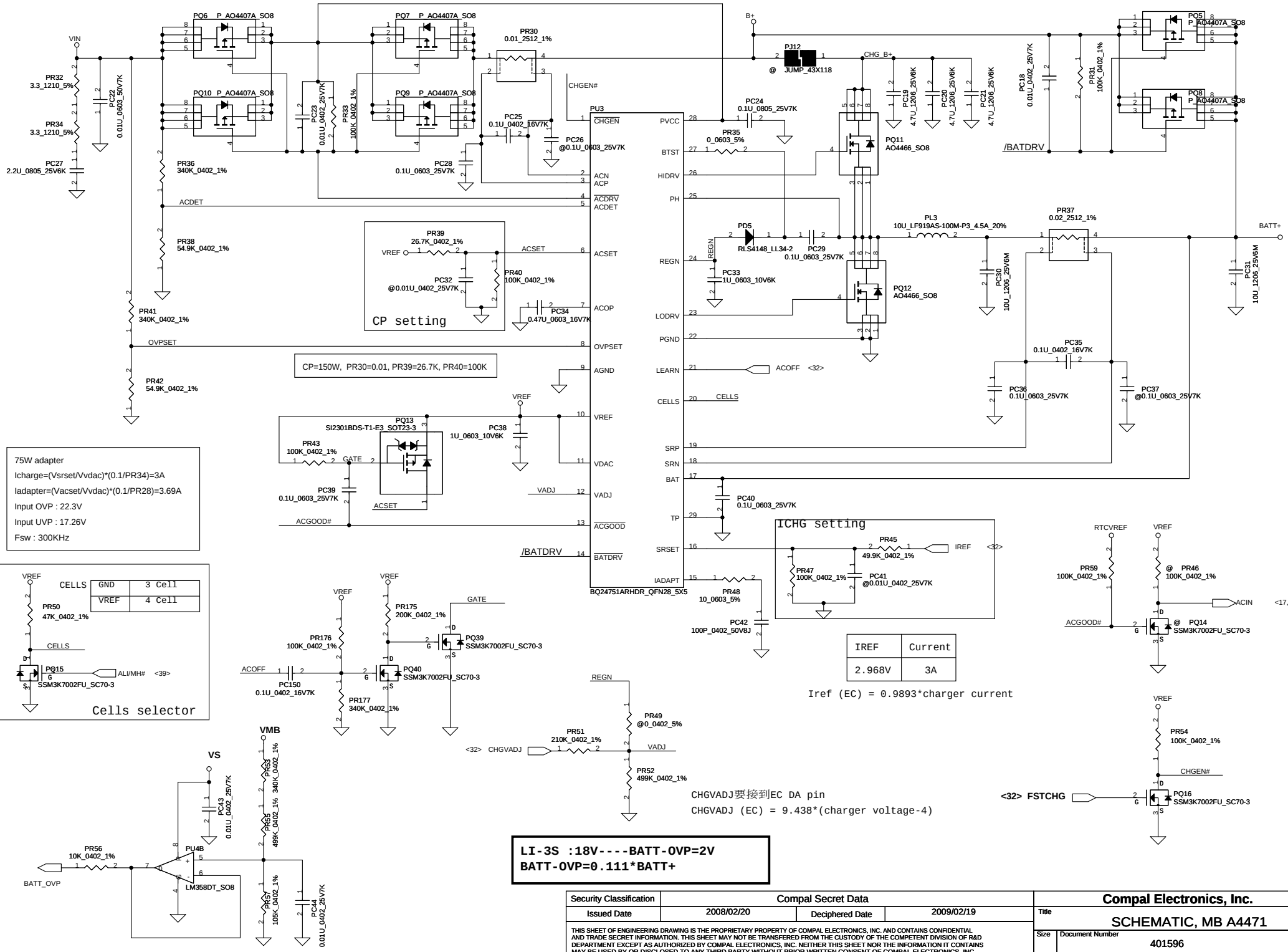
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



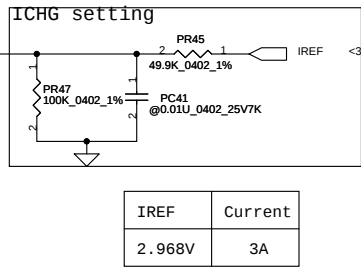
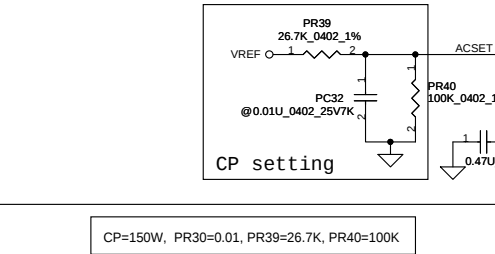
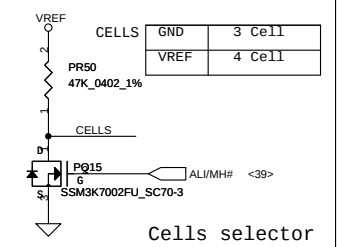
PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 47 degree C



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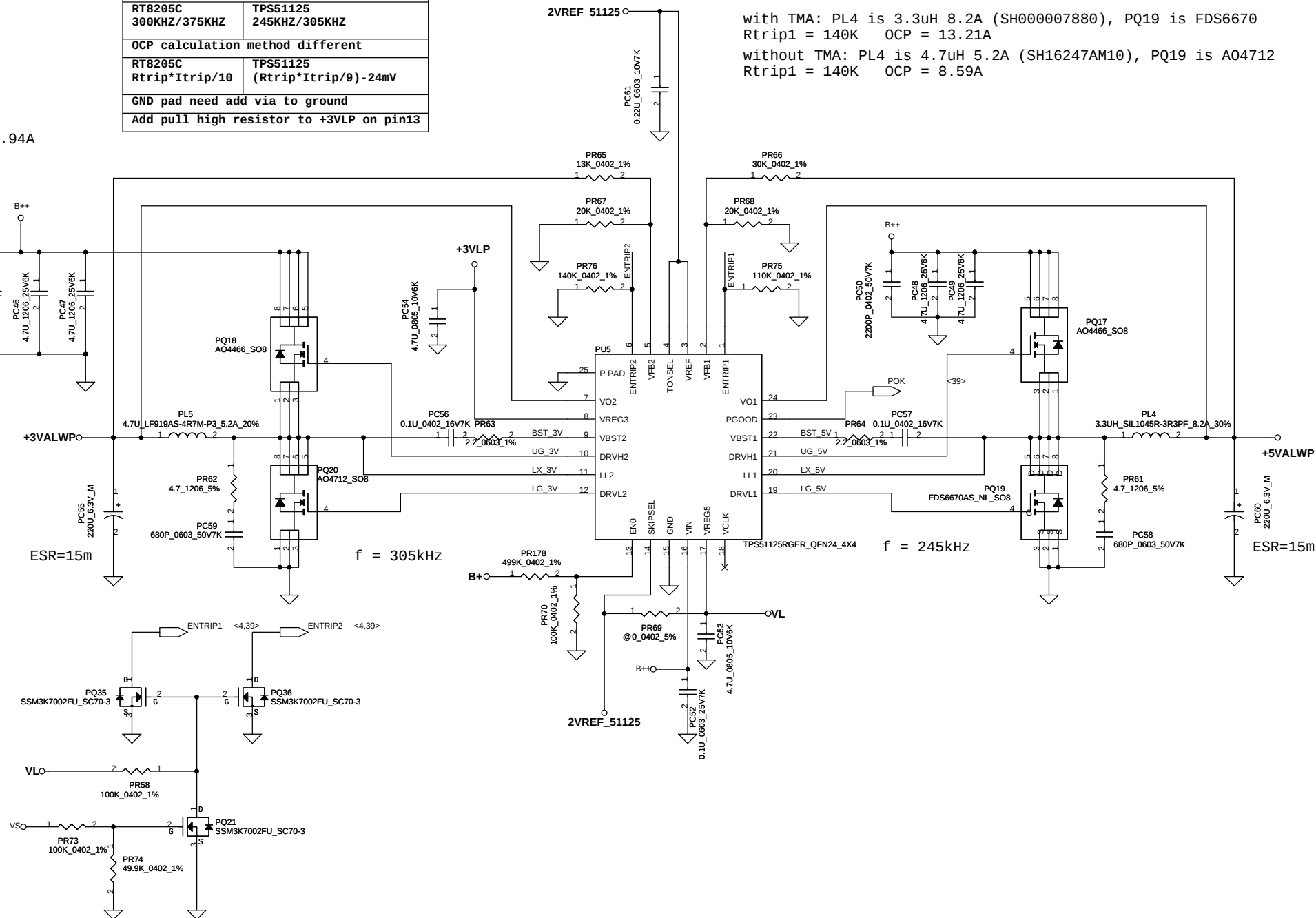
75W adapter
 $I_{charge} = (V_{srset}/V_{vdac}) * (0.1/PR34) = 3A$
 $I_{adapter} = (V_{acset}/V_{vdac}) * (0.1/PR28) = 3.69A$
Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz



LI-3S : 18V --- BATT-OVP=2V
BATT-OVP=0.111*BATT+

Frequency different	
RT8205C 300KHZ/375KHZ	TPS51125 245KHZ/305KHZ
OCP calculation method different	
RT8205C Rtrip*Itrip/10	TPS51125 (Rtrip*Itrip/9)-24mV
GND pad need add via to ground	
Add pull high resistor to +3VLP on pin13	

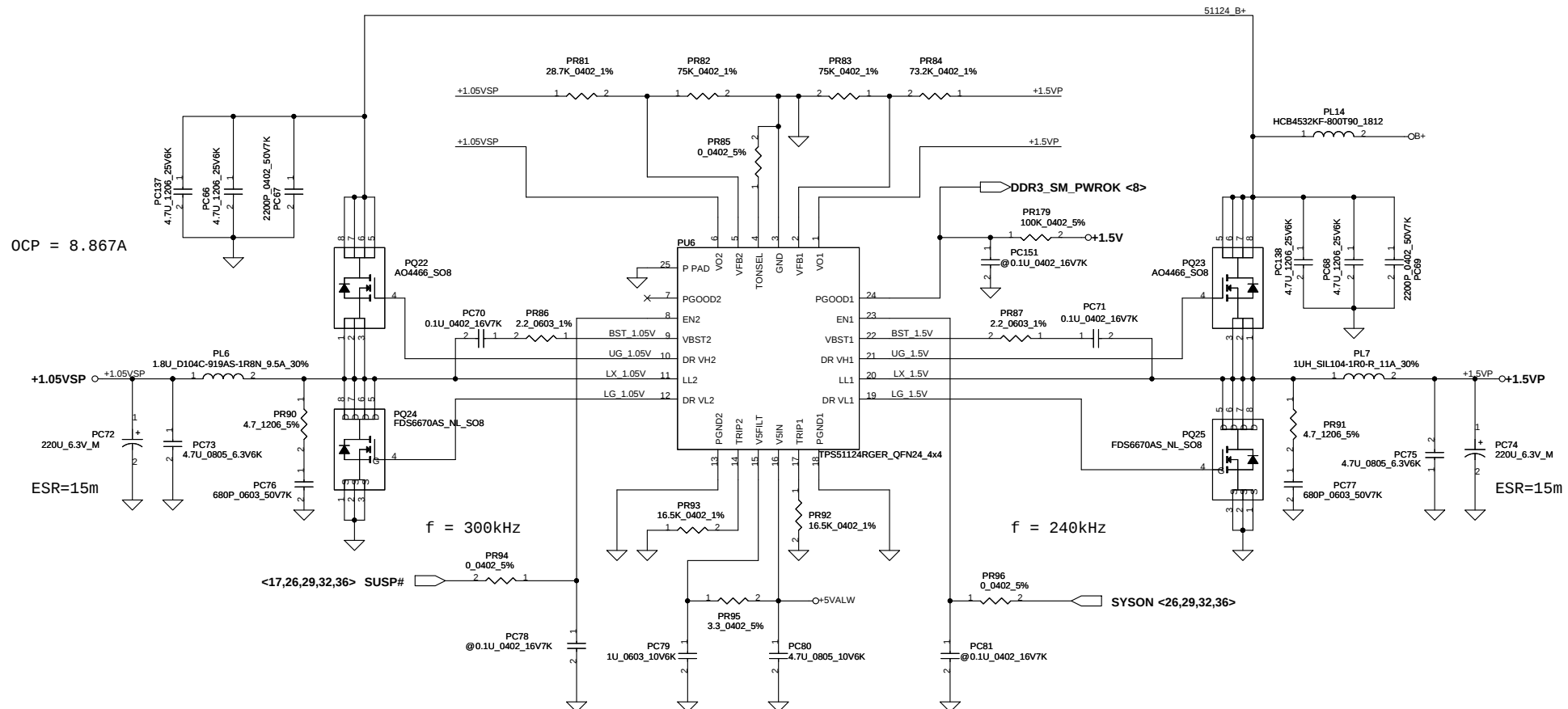
OCP = 7.94A



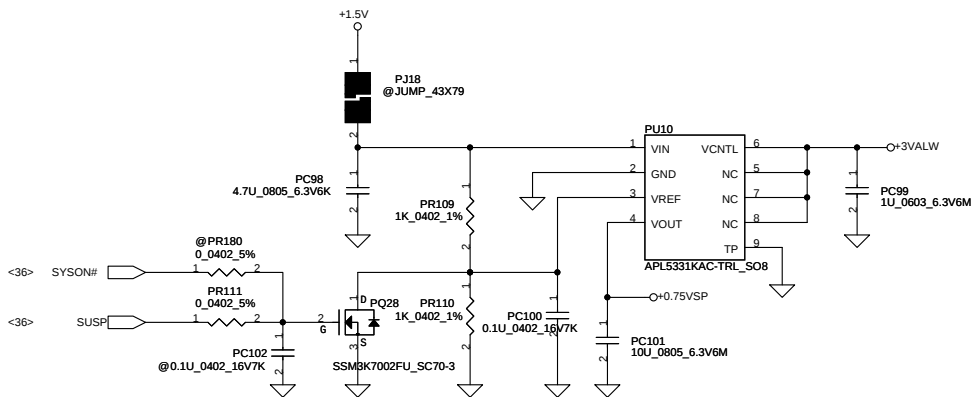
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with TMA: PL7 is 1uH 11A (SH000009080), PQ25 is FDS6670
Rtrip1 = 16.5K OCP = 15.31A

without TMA: PL7 is 1uH 11A (SH000009080), PQ25 is AO4712
Rtrip1 = 16.5K OCP = 10.826A



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HW4 Product Improvement Record (P.I.R.)

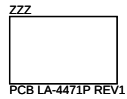
KSRAA LA-4471P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

Rev 0.1 to 0.2

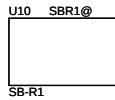
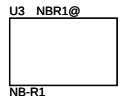
NO	PAGE	MODIFICATION LIST	PURPOSE
1	4	Del RC8	Repeat
2	4	Del RC10	Repeat
3	14	RD6 @	For Boot
4	32	R020 @	For Boot
5	25	Del RE10	For Boot
6	32	Add Pin 66 LOM_WAKE# to LAN IC	For LAN WAKE UP
7	32	Add TMPSPR_SXP pull up +3VS	For EC
8	36	Add FAN NPTH hole H55	For ME require
9	36	Change H54 size to 3P8	For ME require
10	36	Add R091.R094.R095	For PE require
11	32	Change Pin 16 to UWB_OFF#,R096 100K Ohm pull high	For A51 require
12	17	Add JVGA Pin161 to 1.8VS	For +1.8VS drop concern
13	22	Add R1091,R1092,R1093	For FM tuner SMBUS pull high
14	19	Del UV12,UV13,CV69,CV68	For A51 require
15	19	RV83 @. DV7 Mount	For A51 require
16	19	Add DV10,RV94,RV95,RV96,RV97,RV98	For DP function
17	17	Add Pin 164.Pin162	For DP function
18	14	RD19@	
19	15	RD20@	
19	36	Add RA74, RA75	For DP function

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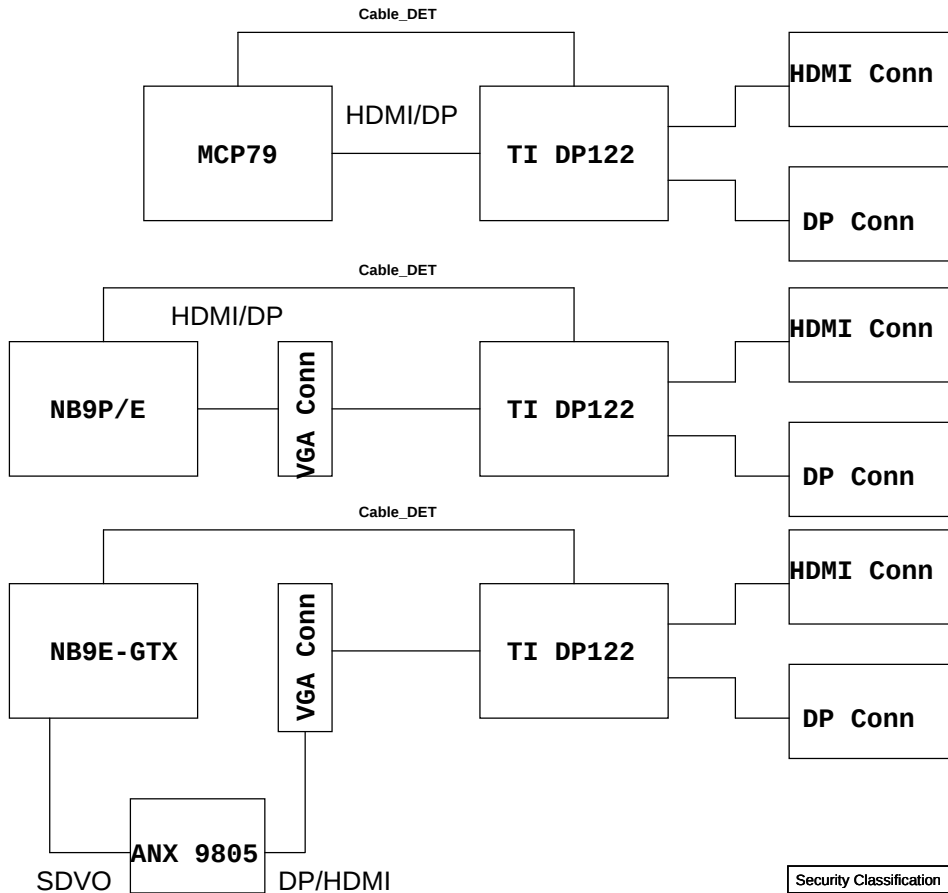
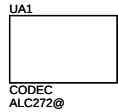
PCB



CHIPSET (R1)



CODEC



BOM Description

Define	Function
ALC272@	ALC272-CODEC
ALC268@	ALC268-CODEC
RJ11@	MODEM
CIR@	CIR function.
TMA@	Toshiba Media Accelerator
UWB@	Wireless USB
FP@	FINGER PRINT
2HDD@	Second Hard Disk
BT@	Blue Tooth
ROBSON@	ROBSON Board
TEST@	Test circuit
NODP@	Remove Display port
DP@	Display port
NBR3@	North Bridge R3
NBR1@	North Bridge R1
SBR3@	South Bridge R3
SBR1@	South Bridge R1

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Predator power block diagram

