ZZZ

PCB_LS5581P

Part Number = DA80000FB20

Compal confidential

Schematics Document

Mobile Penryn ULV singal/dual core with Intel Cantiga_GS45/GS40 +ICH9-M SFF core logic

ULV core logic board

2009-07-23

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Title: *Cover Sheet*

Size: Custom | Document Number: *LS-5581P* | Rev: 2.0

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Title: **Block Diagram**

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Voltage Rails

(O MEANS ON X MEANS OFF)

State \ power plane	+B +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
CONN@ : means ME part.
45@ : means install after SMT.

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

	Descrebtion		Descrebtion		Descrebtion
USB port 0	USB connector	PCI-e port 0		SATA port 0	SATA HDD
USB port 1	BT Module	PCI-e port 1	WLAN Conn.	SATA port 1	
USB port 2	cardreader	PCI-e port 2		SATA port 2	WWAN/SSD
USB port 3	USB connector	PCI-e port 3			
USB port 4	WLAN Conn.	PCI-e port 4			
USB port 5	WWAN/SSD	PCI-e port 5	LAN		
USB port 6	USB connector				
USB port 7	CMOS				
USB port 8	Fingerprint				

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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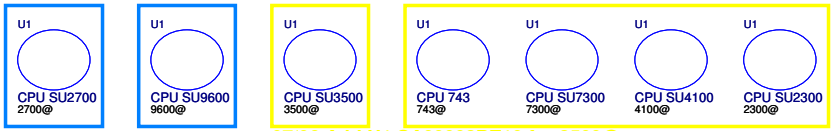
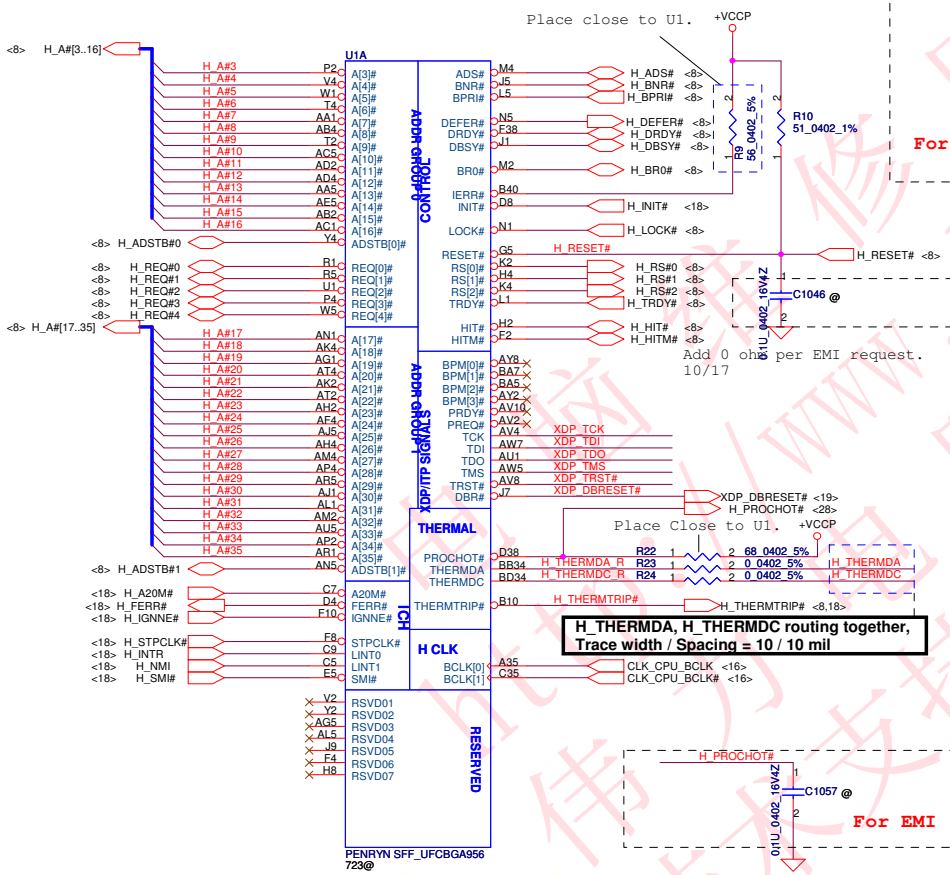
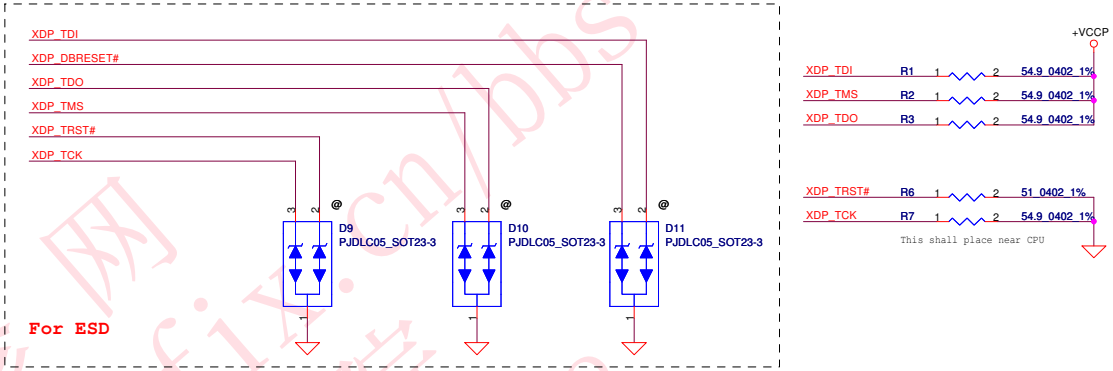
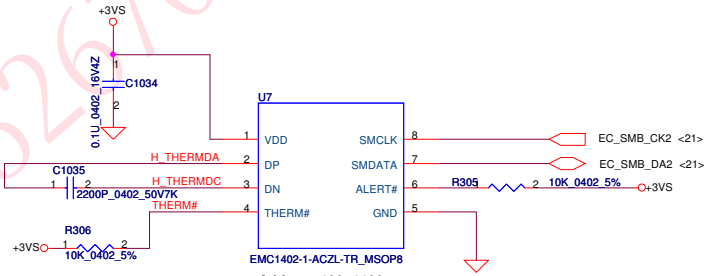


07/06 Add U1 SA00003BZ10 for 3500@
07/23 Add U1 SA00003IA50 for 7300@
Add U1 SA00003I950 for 4100@
Add U1 SA00003H060 for 2300@
Add U1 SA00003JO60 for 743@



07/06 Change U1 from SA000038J40 to SA000038J60





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Title: **Penryn(1/3)-AGTL+/ITP-XDP**

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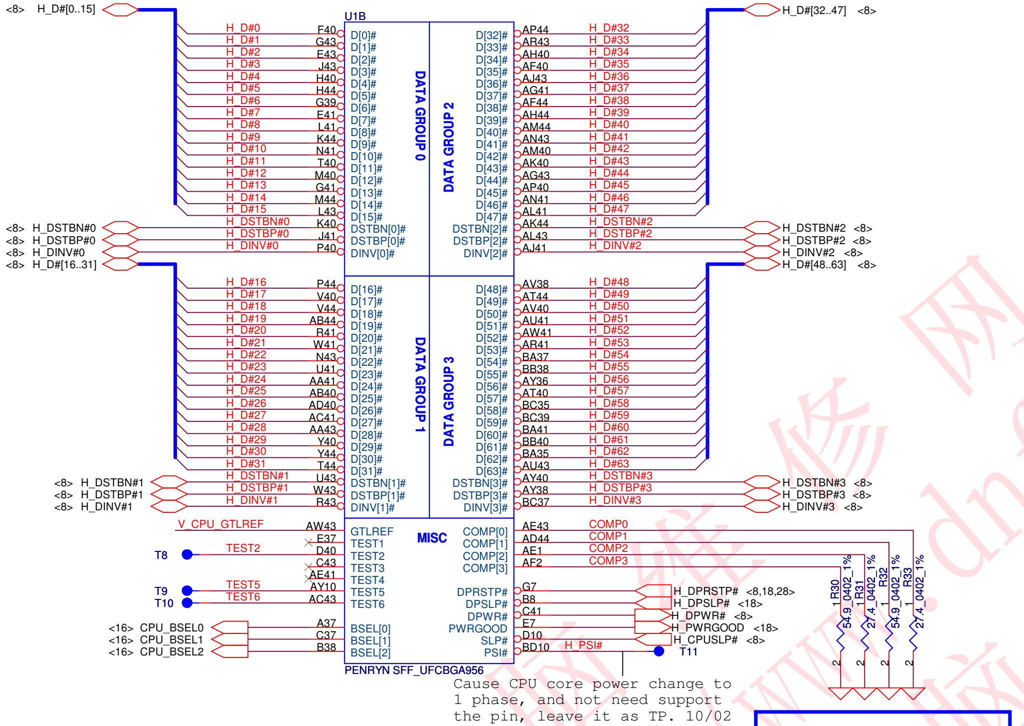
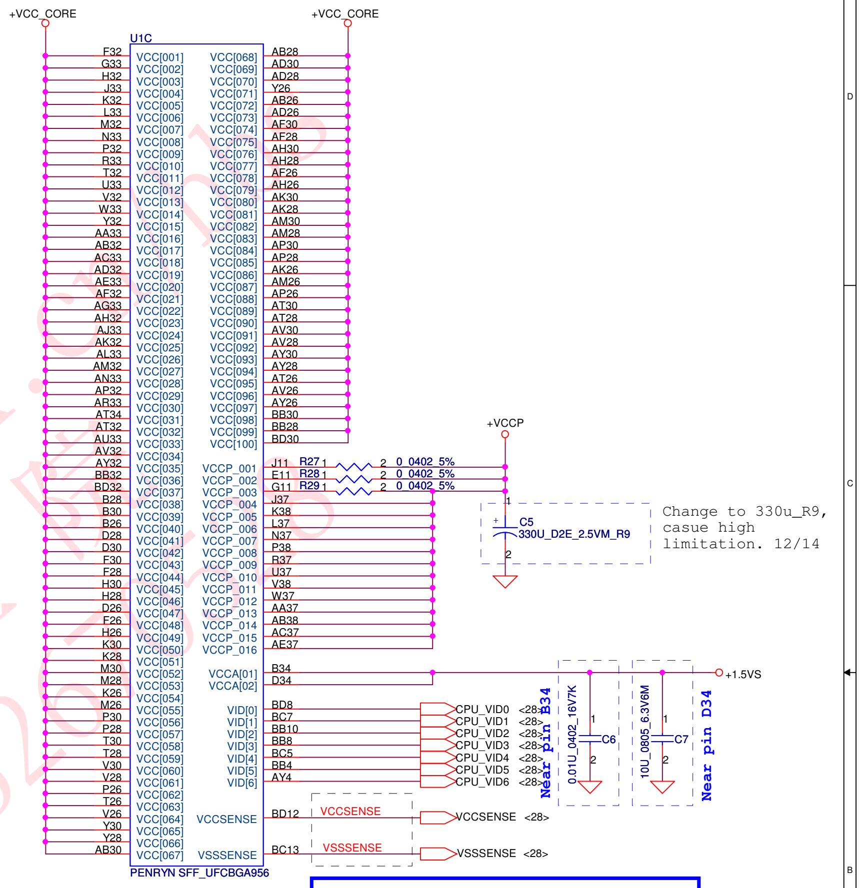


Cause CPU core power change to 1 phase, and not need support the pin, leave it as TP. 10/02

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

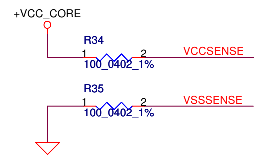


Change to 330u_R9, casue high limitation. 12/14

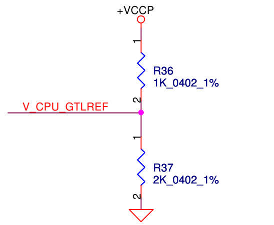
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin within 500mils.



Close to CPU pin AW43 within 500mils.

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Title: **Penryn(2/3)-AGTL+/ITP-XDP**

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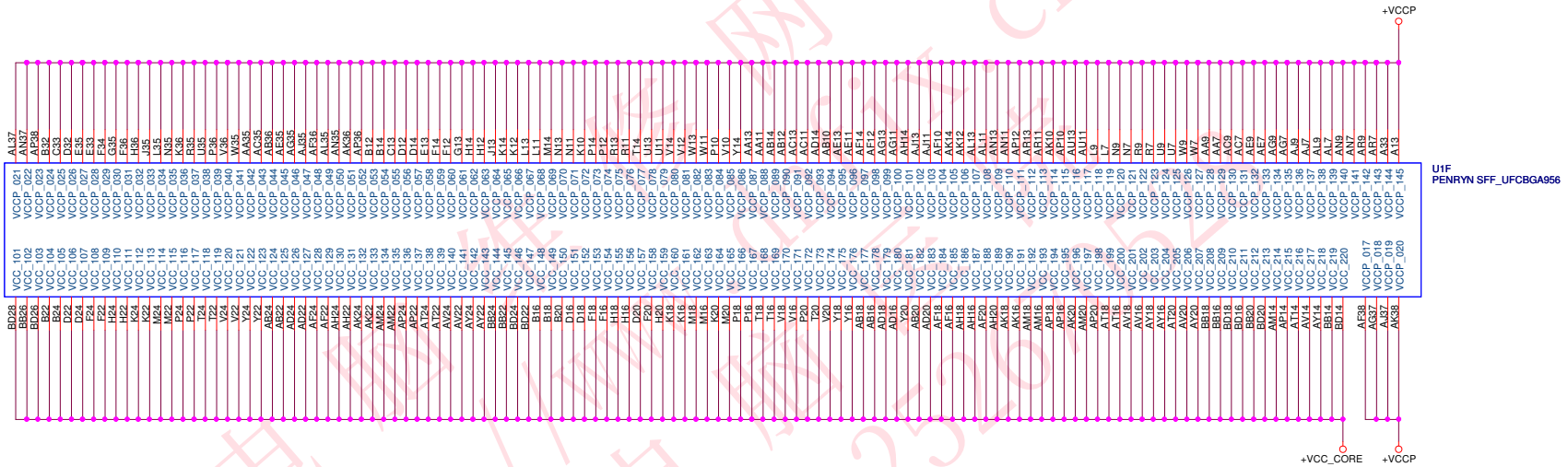

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Title: **Penryn(3/3)-Power**

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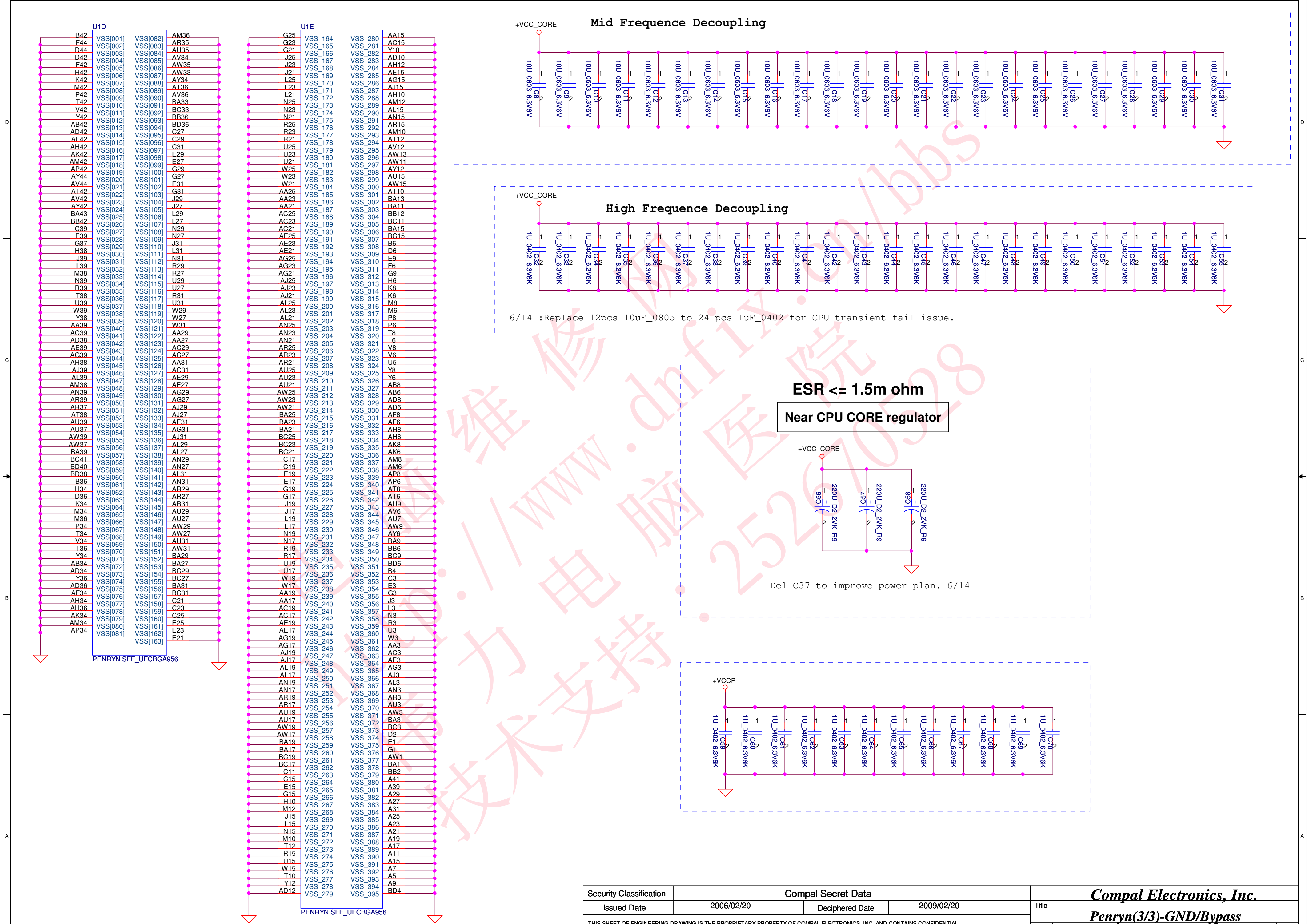

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Title: **Penryn(3/3)-GND/Bypass**

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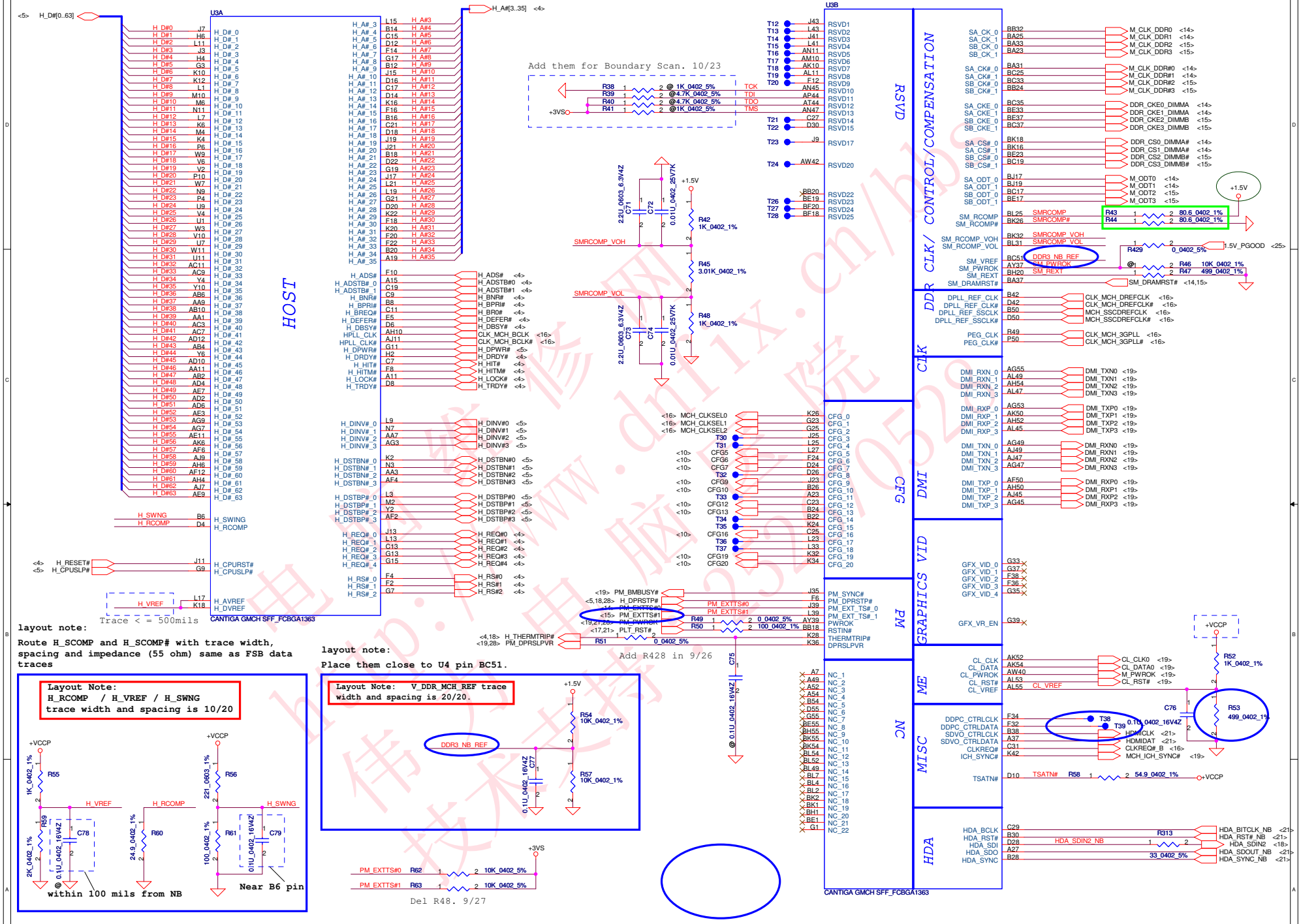

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Title: **Cantiga(1/6)-AGTL/DMI/DDR**

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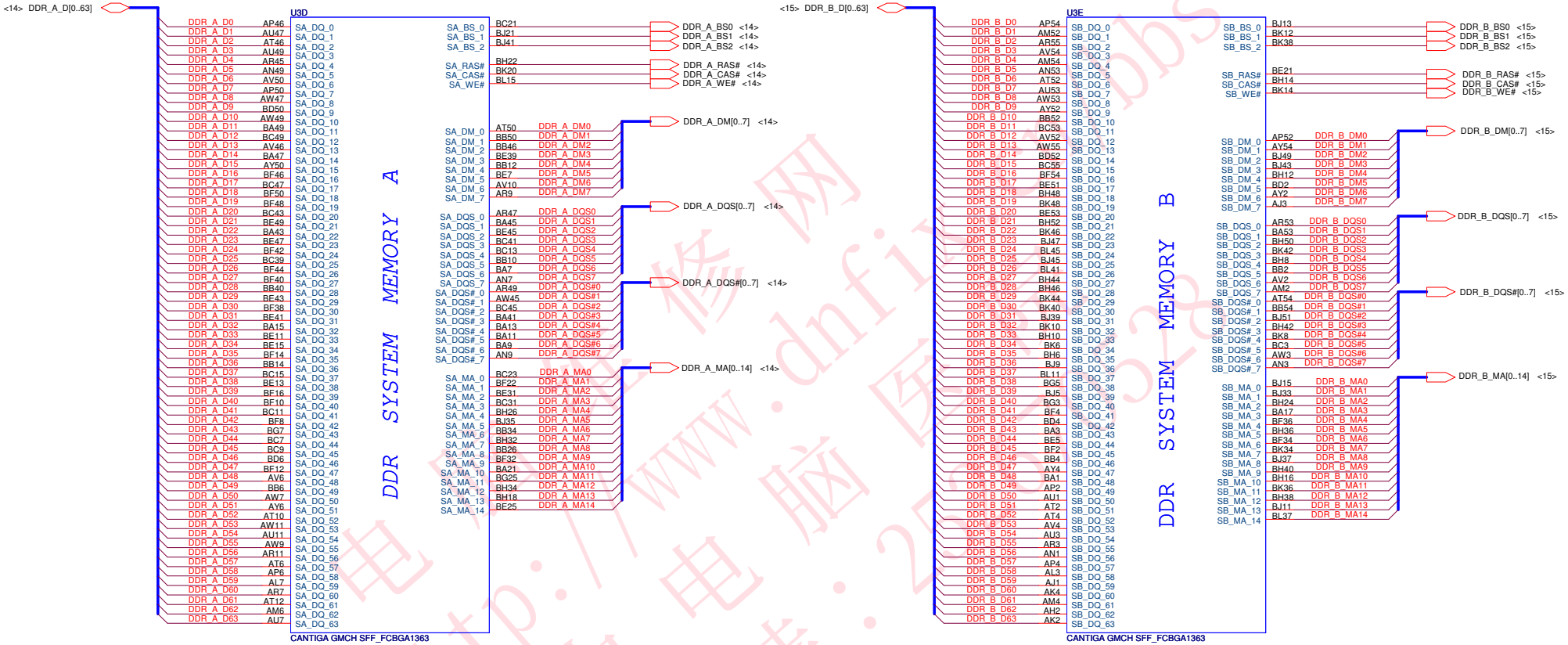

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Title: **Cantiga(2/6)-DDR2 A/B CH**

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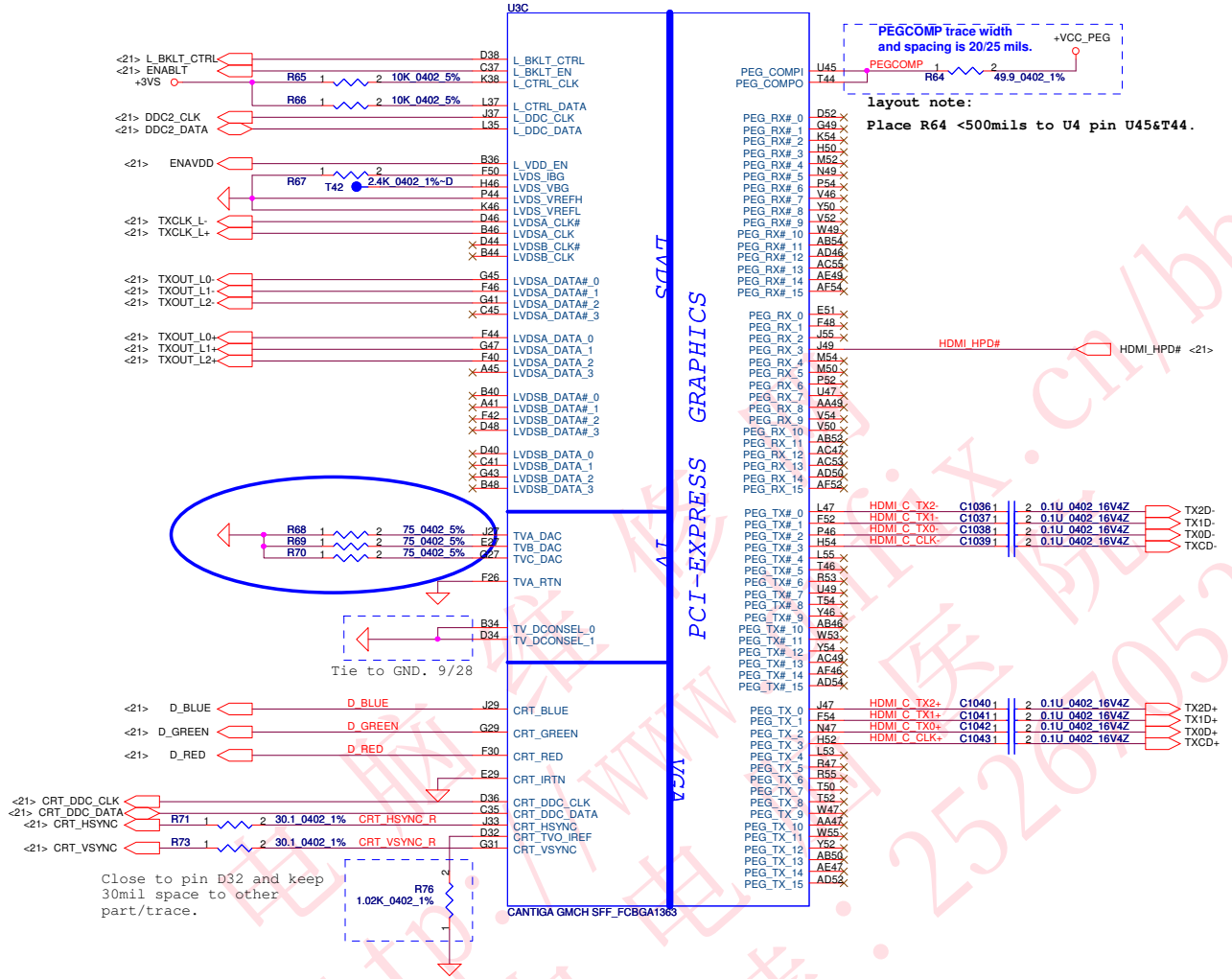

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 ★
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable ★
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality ★
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order ★
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable ★
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) ★
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled ★
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation ★ (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. ★ 1 = PCIE/SDVO are operating simu.

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Title: **Cantiga(3/6)-VGA/LVDS/TV**

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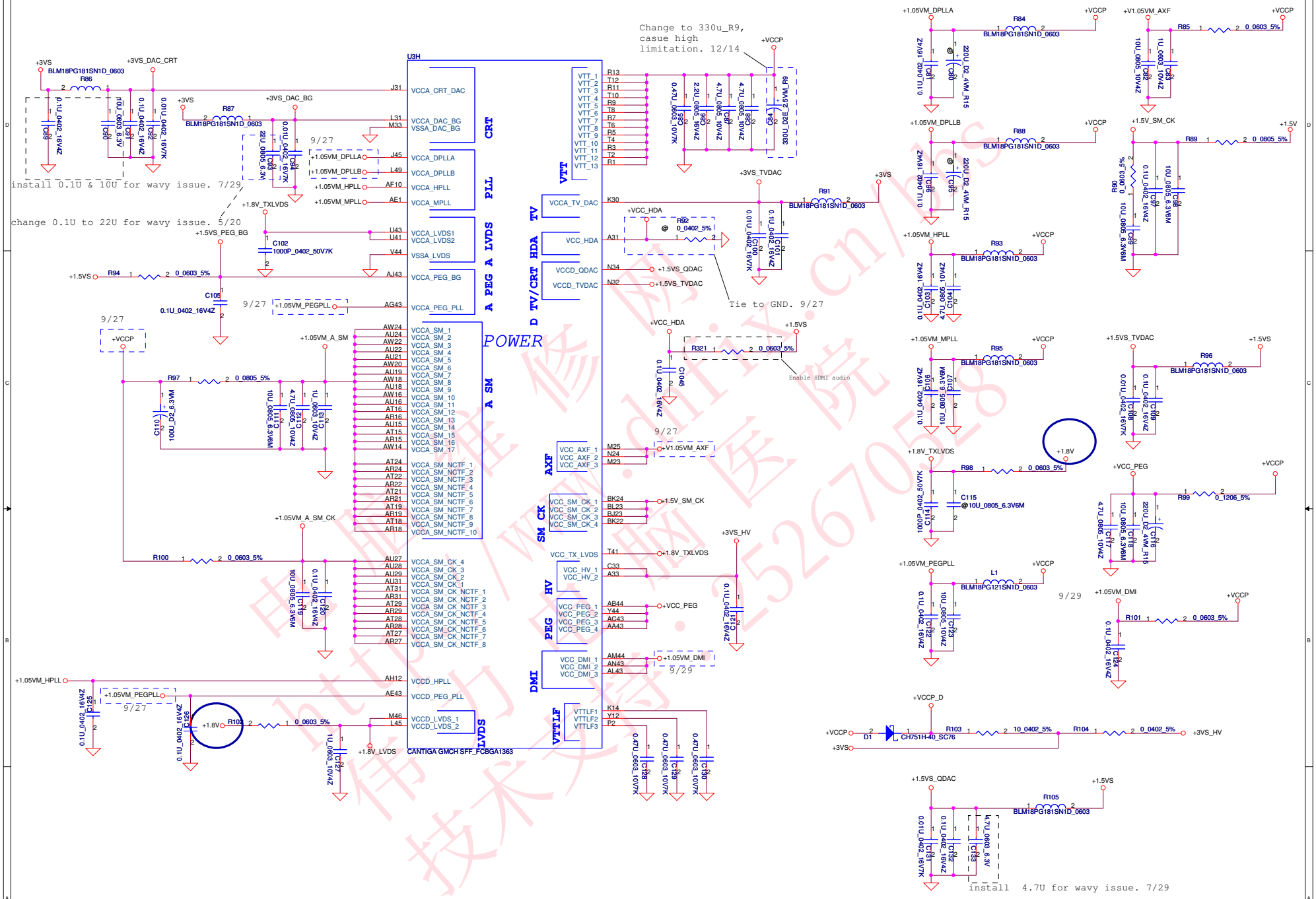

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Title: **Cantiga(4/6)-PWR**

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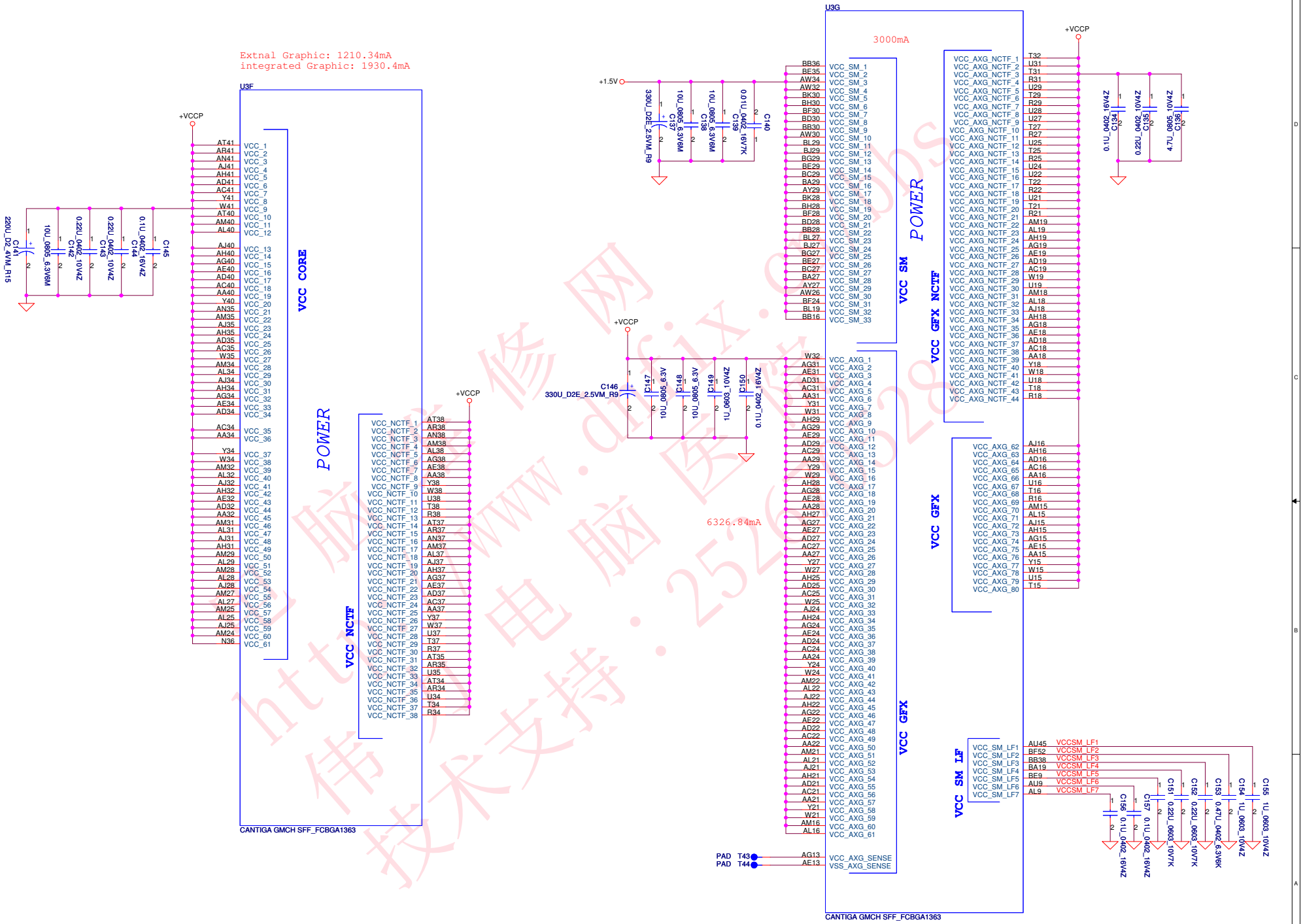

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Title: **Cantiga(5/6)-PWR/GND**

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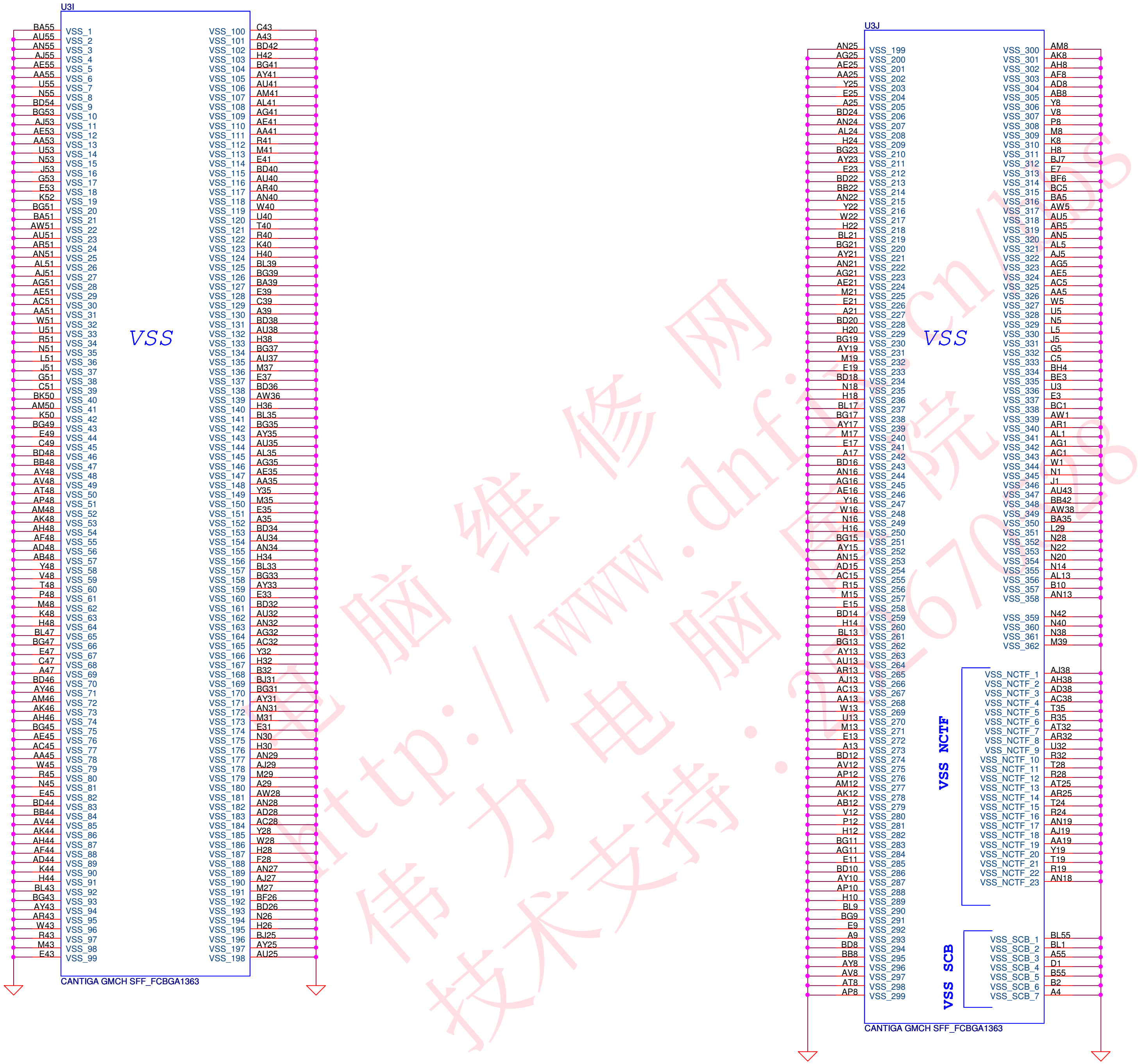

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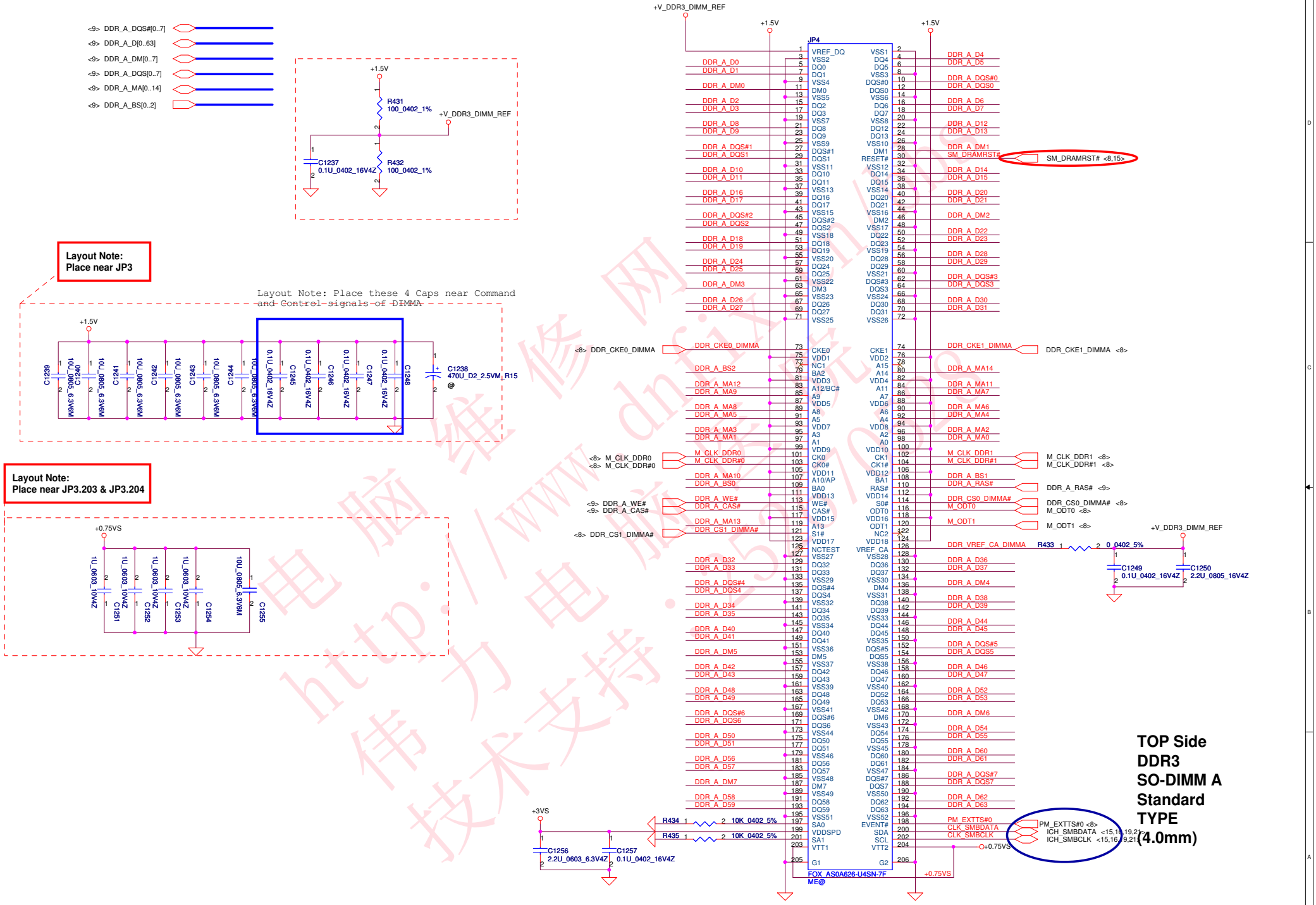

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Compal Electronics, Inc.

Title: **DDR3-SODIMM SLOT1**

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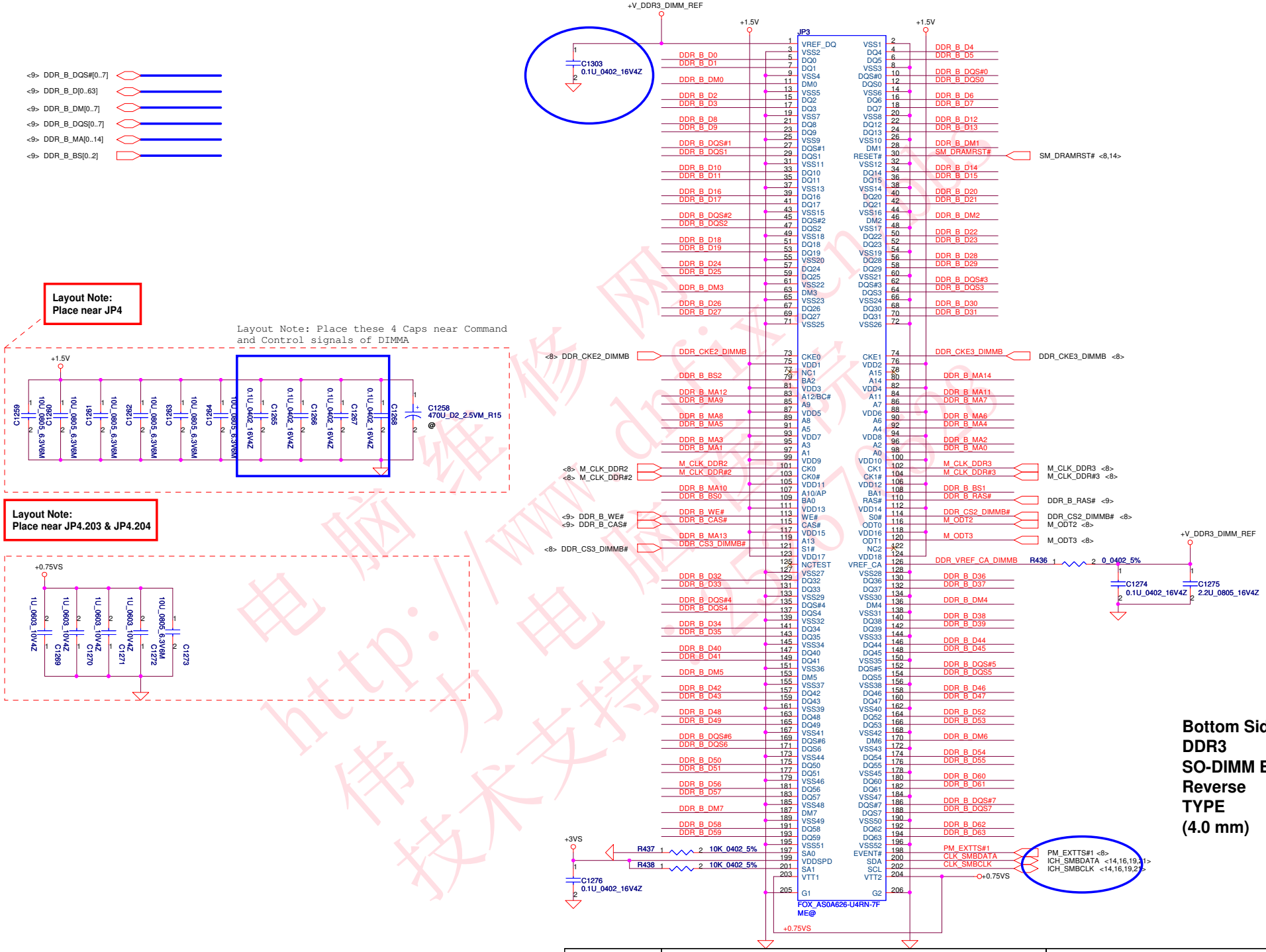

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Title: **DDR3-SODIMM SLOT2**

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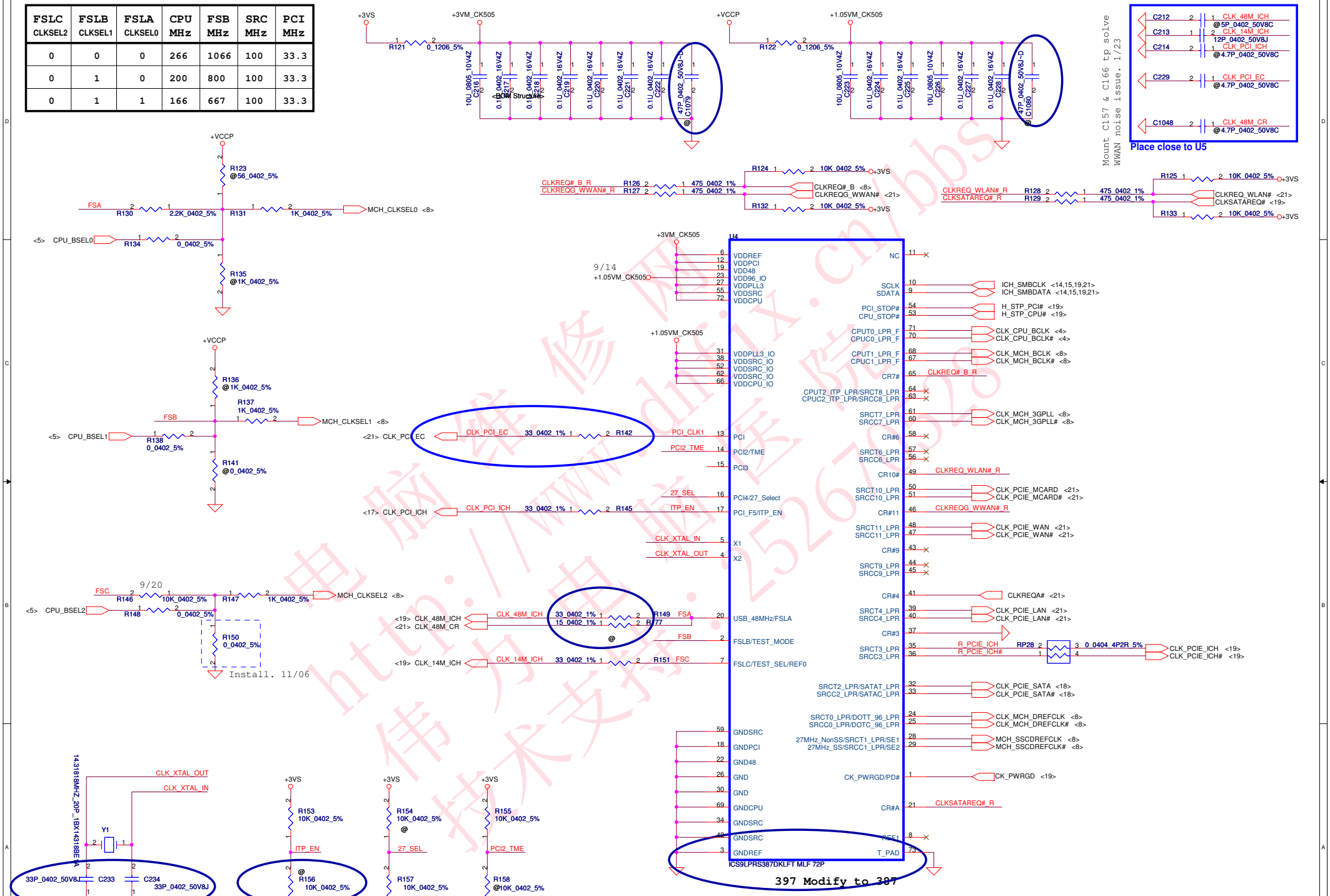
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	FSB MHz	SRC MHz	PCI MHz
0	0	0	266	1066	100	33.3
0	1	0	200	800	100	33.3
0	1	1	166	667	100	33.3



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Compal Electronics, Inc.

Title: CLOCK GENERATOR

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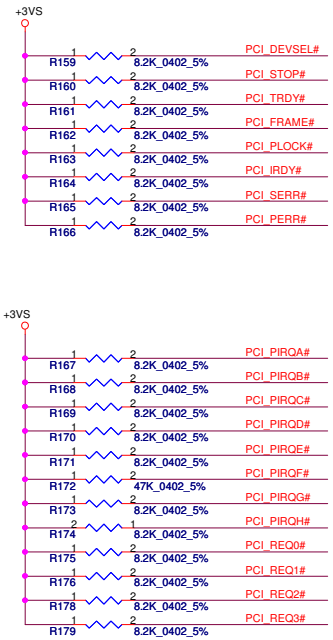
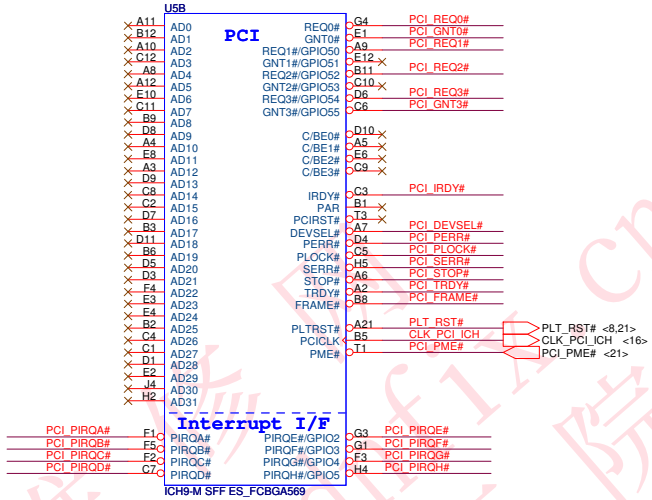
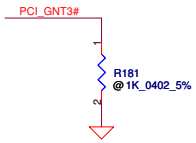
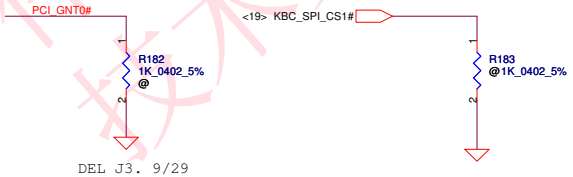




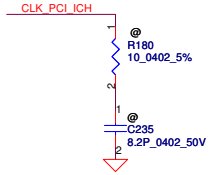
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



Place closely pin B10



DEL J3. 9/29

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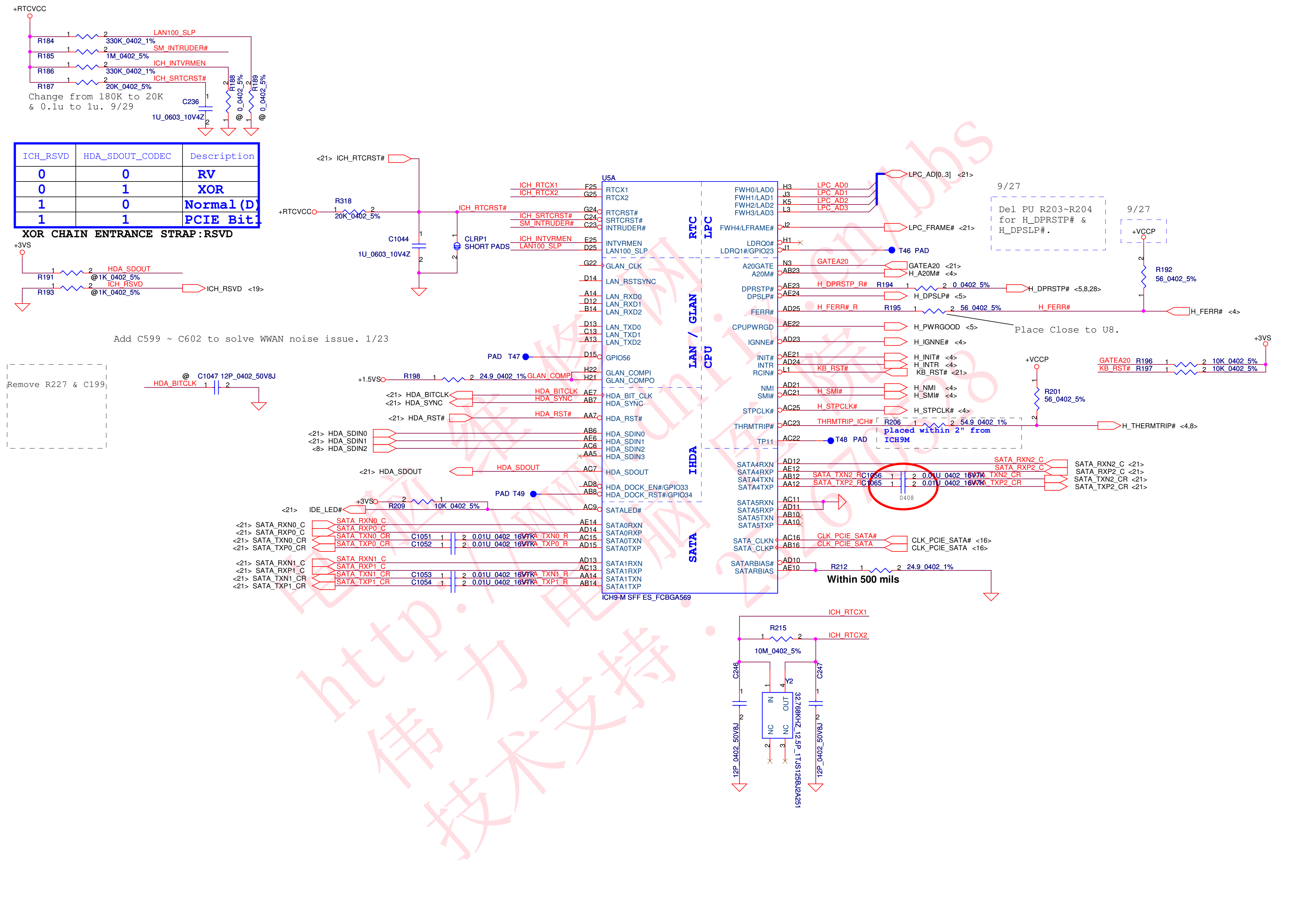
Compal Electronics, Inc.

Title: ICH9(1/4)-PCI/INT

Size: | Document Number: LS-5581P | Rev: 2.0

Date: Thursday, July 23, 2009 | Sheet 17 of 30



ICH_RSVD	HDA_SDOUT_CODEC	Description
0	0	RV
0	1	XOR
1	0	Normal(D)
1	1	PCIE Bit1

XOR CHAIN ENTRANCE STRAP:RSVD

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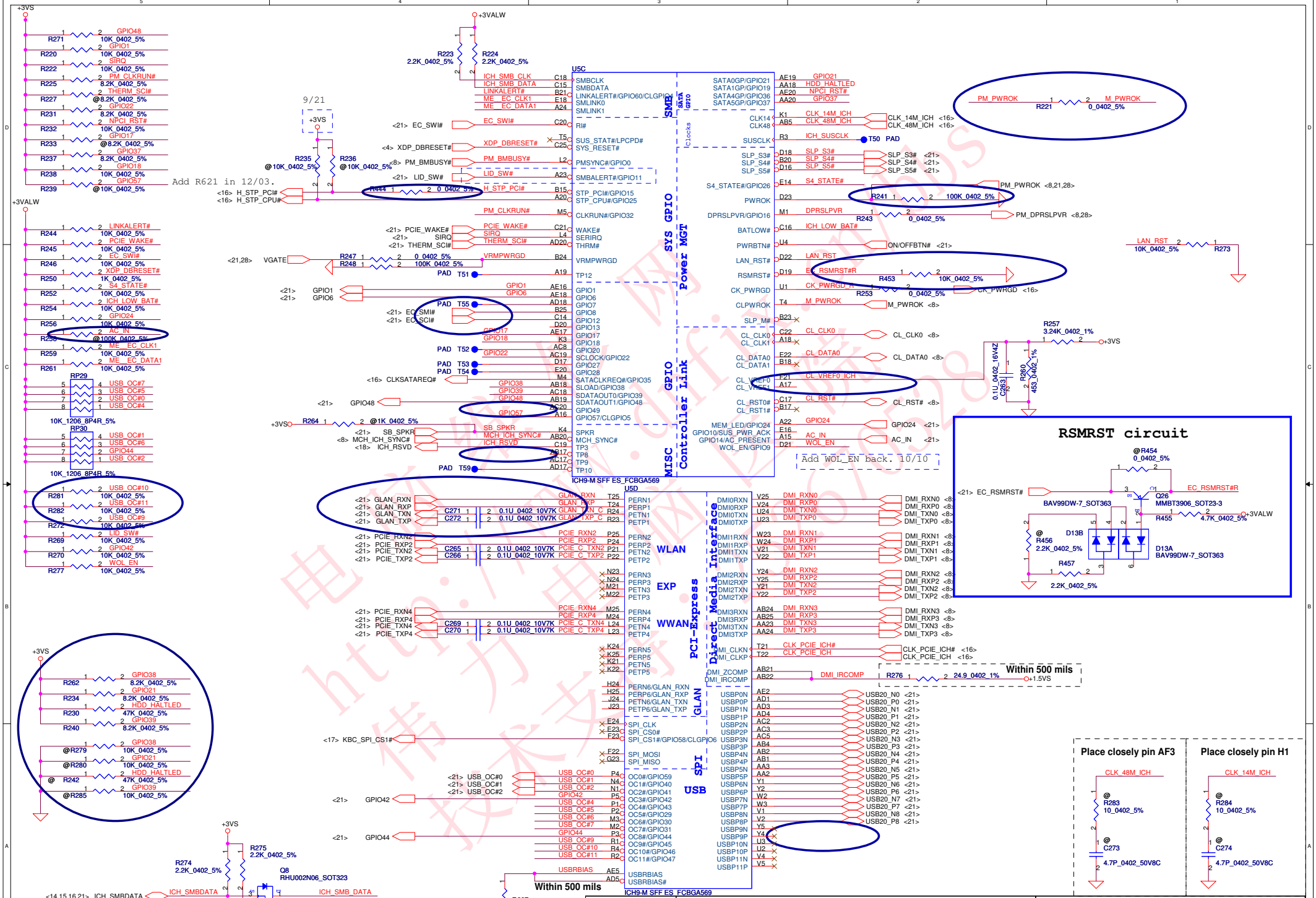
Compal Electronics, Inc.

Title: **ICH9(2/4)_LAN,HD,IDE,LPC**

Size: Custom | Document Number: LS-5581P | Rev: 2.0

Date: Thursday, July 23, 2009 | Sheet 18 of 30



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Issued Date	2006/02/20	Deciphered Date	2009/02/20

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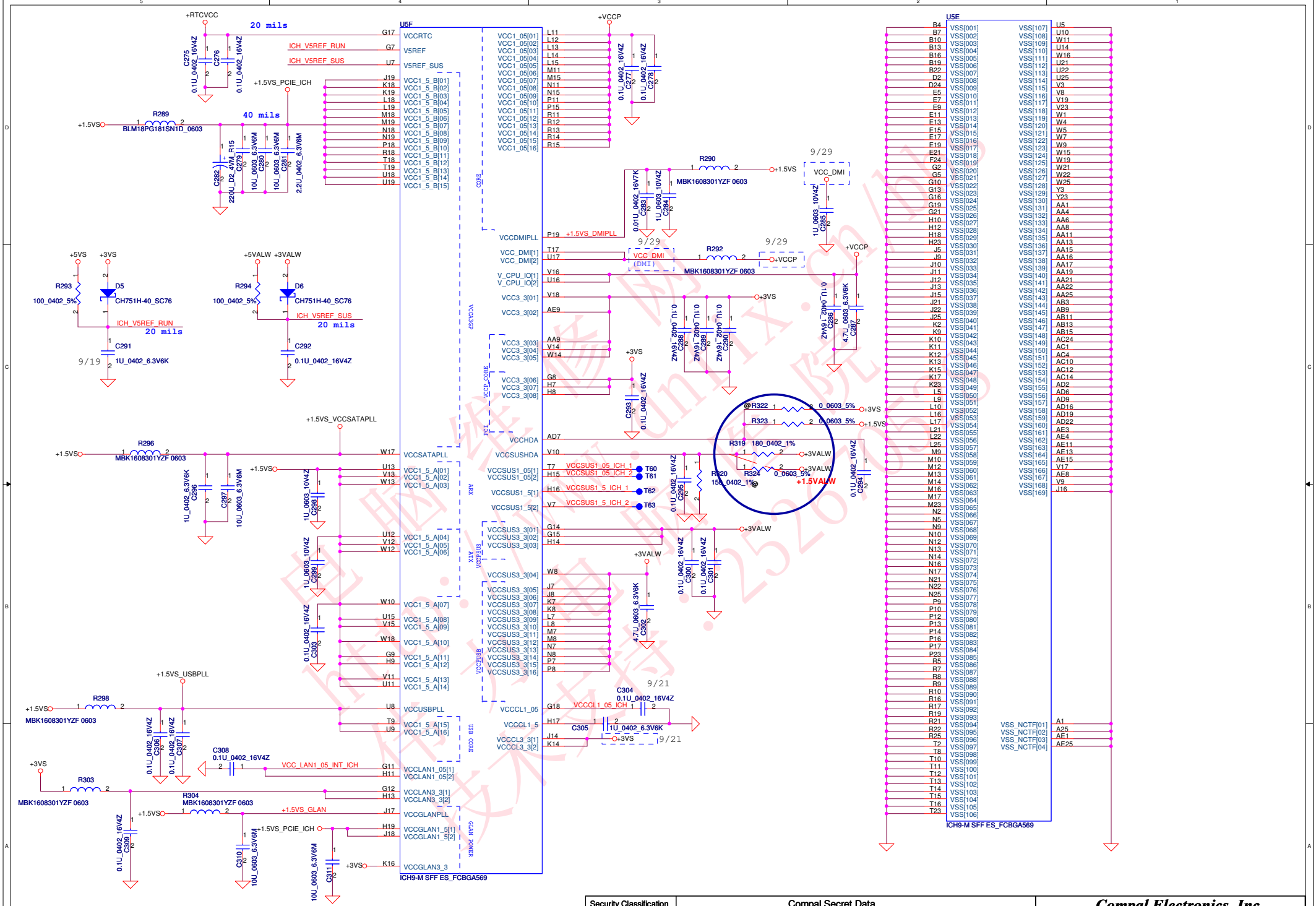
Compal Electronics, Inc.

Title: **ICH9(3/4) DMI,USB,GPIO,PCIE**

Size: Custom | Document Number: LS-5581P | Rev: 2.0

Date: Thursday, July 23, 2009 | Sheet 19 of 30



Security Classification	Compal Secret Data		
Issued Date	2006/02/20	Deciphered Date	2009/02/20

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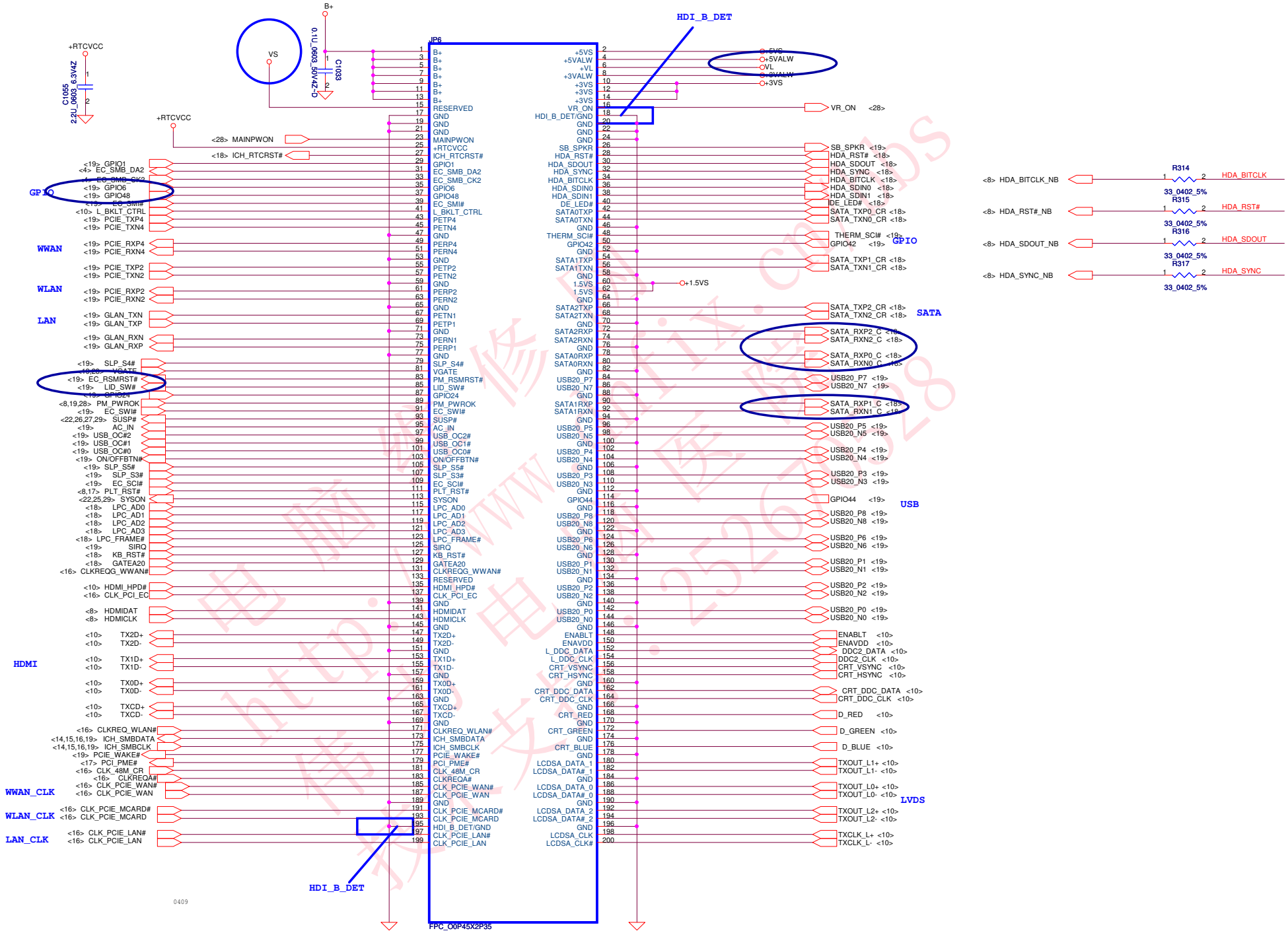
Compal Electronics, Inc.

Title: **ICH9(4/4)_POWER&GND**

Size	Document Number	Rev
Custom	LS-5581P	2.0

Date: Tuesday, July 21, 2009 | Sheet 20 of 30



Security Classification	Compal Secret Data		
Issued Date	2006/02/20	Deciphered Date	2009/02/20

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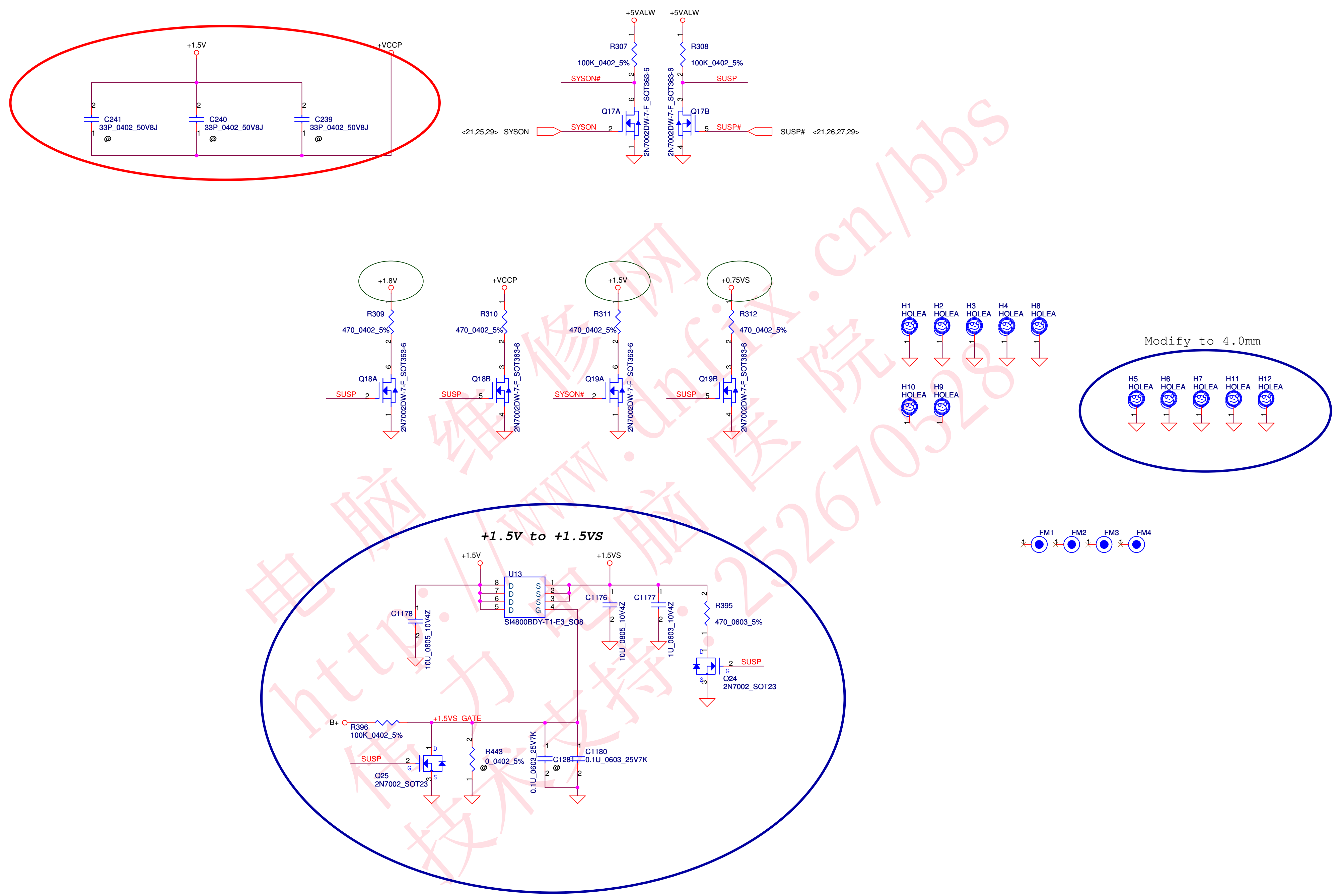
Compal Electronics, Inc.

Title: **LCD CONN & Q-Switch & GPIO Ext.**

Size: | Document Number: LS-558IP | Rev: 2.0

Date: Thursday, July 23, 2009 | Sheet 21 of 30



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Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2006/02/20	Deciphered Date	2009/02/20	Title: LEDS & LID

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Size	Document Number	Rev
Custom	LS-5581P	2.0

Date: Tuesday, July 21, 2009 | Sheet 22 of 30

Date	Descrebtion	Rev.
4/16	Relaese LS5581PR01 schematic.	01
5/8	R53 change to 499 Ohm R68,R69,R70 implement 75Ohm Add C1303 for DDR3 request Change R149,R177 from 33 to 15Ohm Change C233,C234 from 33P to 22P R153 implement 10K_Ohm and R156 remove Add C1079,C1080 for EMI Delete R249,R255,R267,R268 for optionUSB and GPIO Delete C1066,C1067,C1068,C1069,C1070,C1071 for SATA AC cap Add VL voltage on JP6.6 for OCP use Modify SB VCCSUSHDA power level Modify SB GLAN fromPCIE4 to PCIE1 Delete R265,C264,C266 for CL_REF1 Delete R240 for H_STP_CPU# and Add R444 for H_STP_PCI# Change R221 connect from VGATE to PM_PWROK Change R240 from H_STP_CPU# to H_STP_PCI# Change EC_SCI# from GPIO7 to GPIO12 Delete T56,T57,T58,R263 for no use Add R281,R282 for USB OC# pull high Add R242,R285 for Project ID define Modify H5,H6,H7,H11,H12 footprint for ME recommand Delete R251 and Add Q26,D13,R453-R457 for RSMRST# function Delete USB9 pair on SB for not use Modify CLK_PCI_EC from U4.15 to U4.13 Modify power plane from +1.8VS to +1.8V for NB use Change Name from DDR3_DIMM_REF to DDR3_NB_REF for DDR3 recommand Change DDR PM_EXTTS# 1 from not use to JP3 Del R106 for Intel Recommand for HDMI setting	

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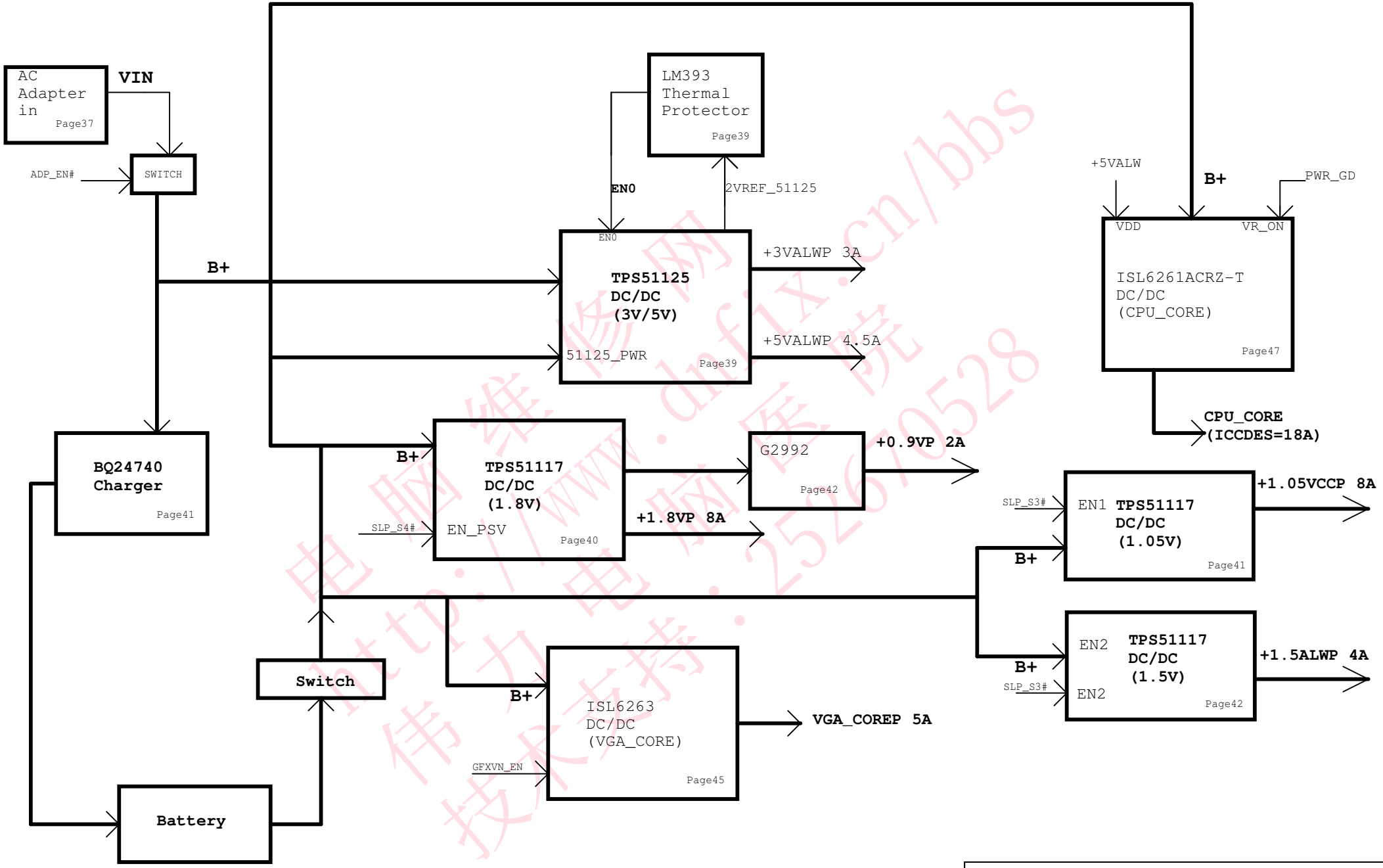
Compal Electronics, Inc.

Title: **HW Changed-List History-1**

Size | Document Number: LS-5581P | Rev 2.0

Date: Tuesday, July 21, 2009 | Sheet 23 of 30



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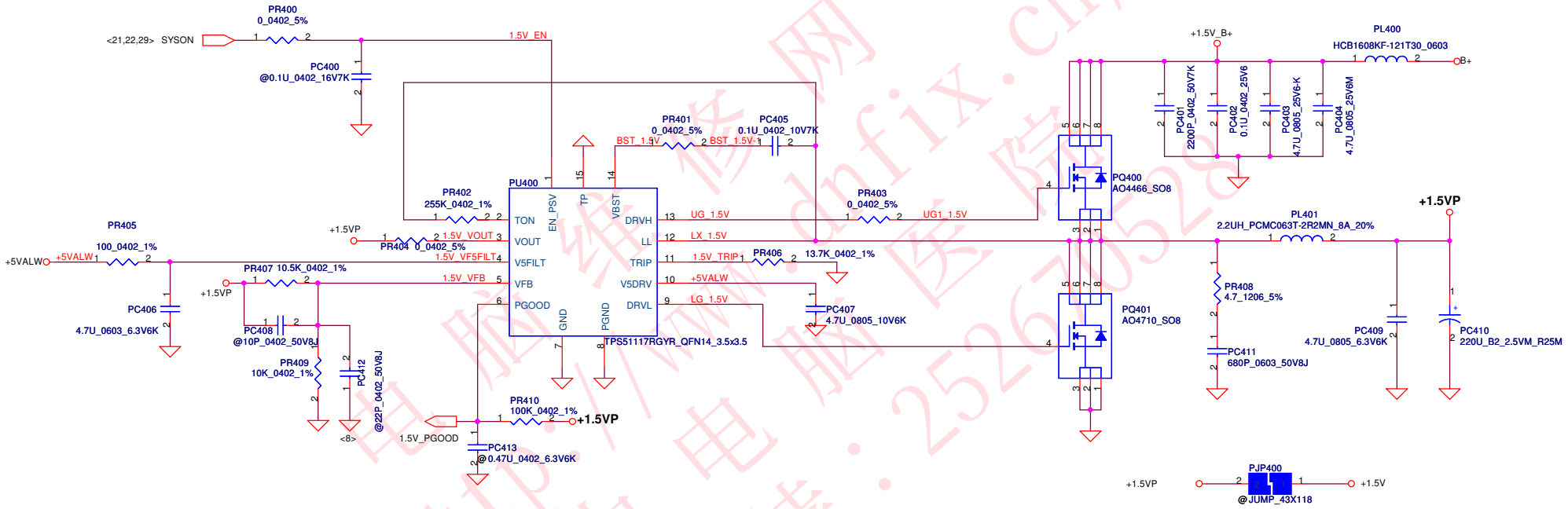
Title	POWER BLOCK DIAGRAM		
Size	Document Number		Rev
Date: Tuesday, July 21, 2009	Sheet 24 of 30		



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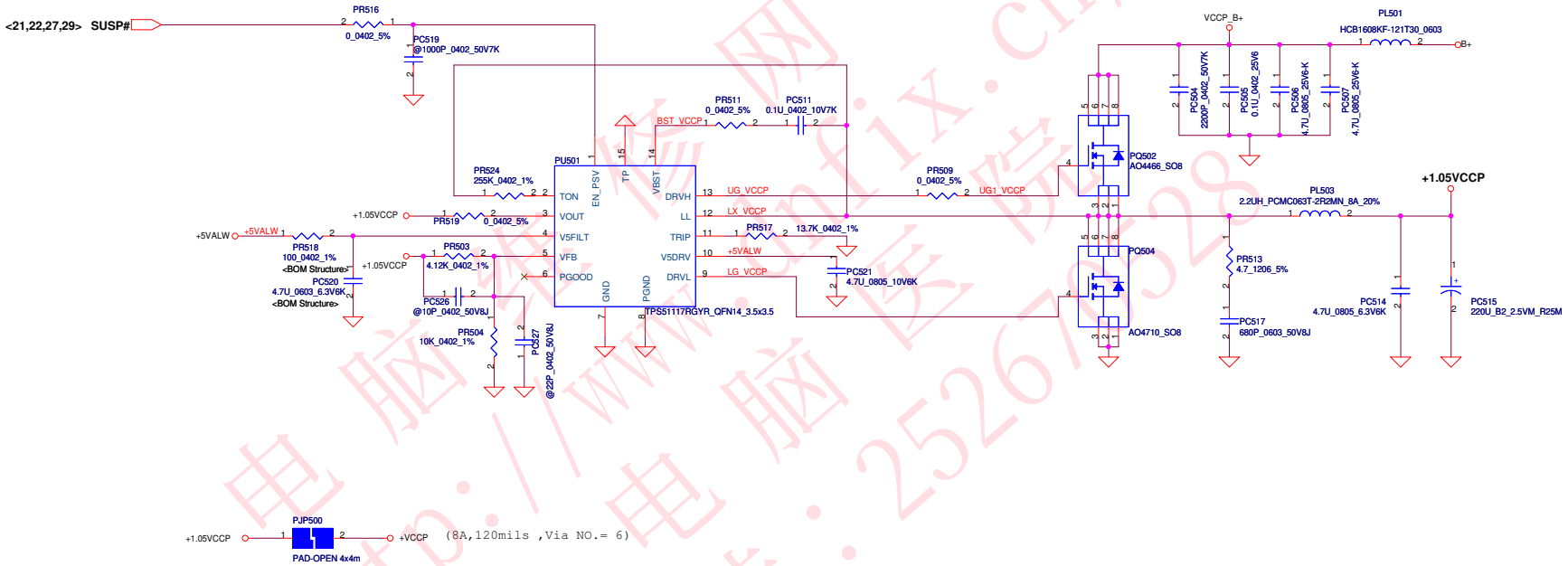
Compal Electronics, Inc.

Title: **1.5VP**

Size | Document Number: *LS-5581P* | Rev: 2.0

Date: Tuesday, July 21, 2009 | Sheet 25 of 30



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Issued Date	2006/11/23	Deciphered Date	2007/11/23

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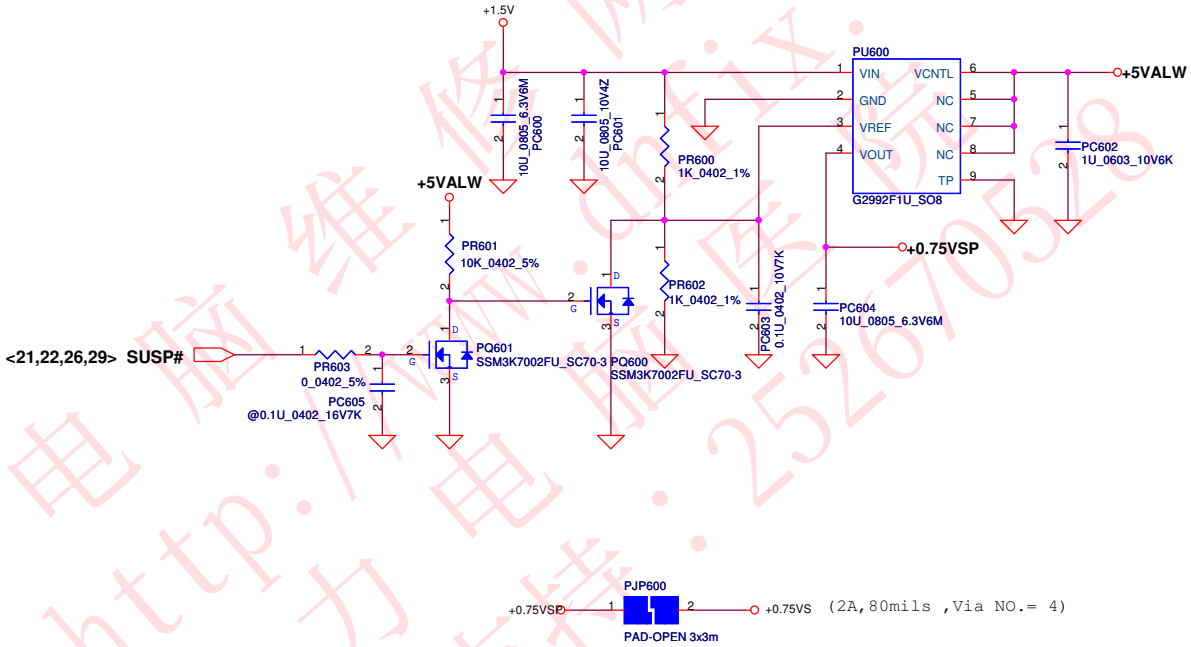
Compal Electronics, Inc.

Title: **1.05VCCP**

Size | Document Number: *LS-5581P* | Rev: 2.0

Date: Tuesday, July 21, 2009 | Sheet 26 of 30



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Issued Date	2008/09/15	Deciphered Date	2009/09/15

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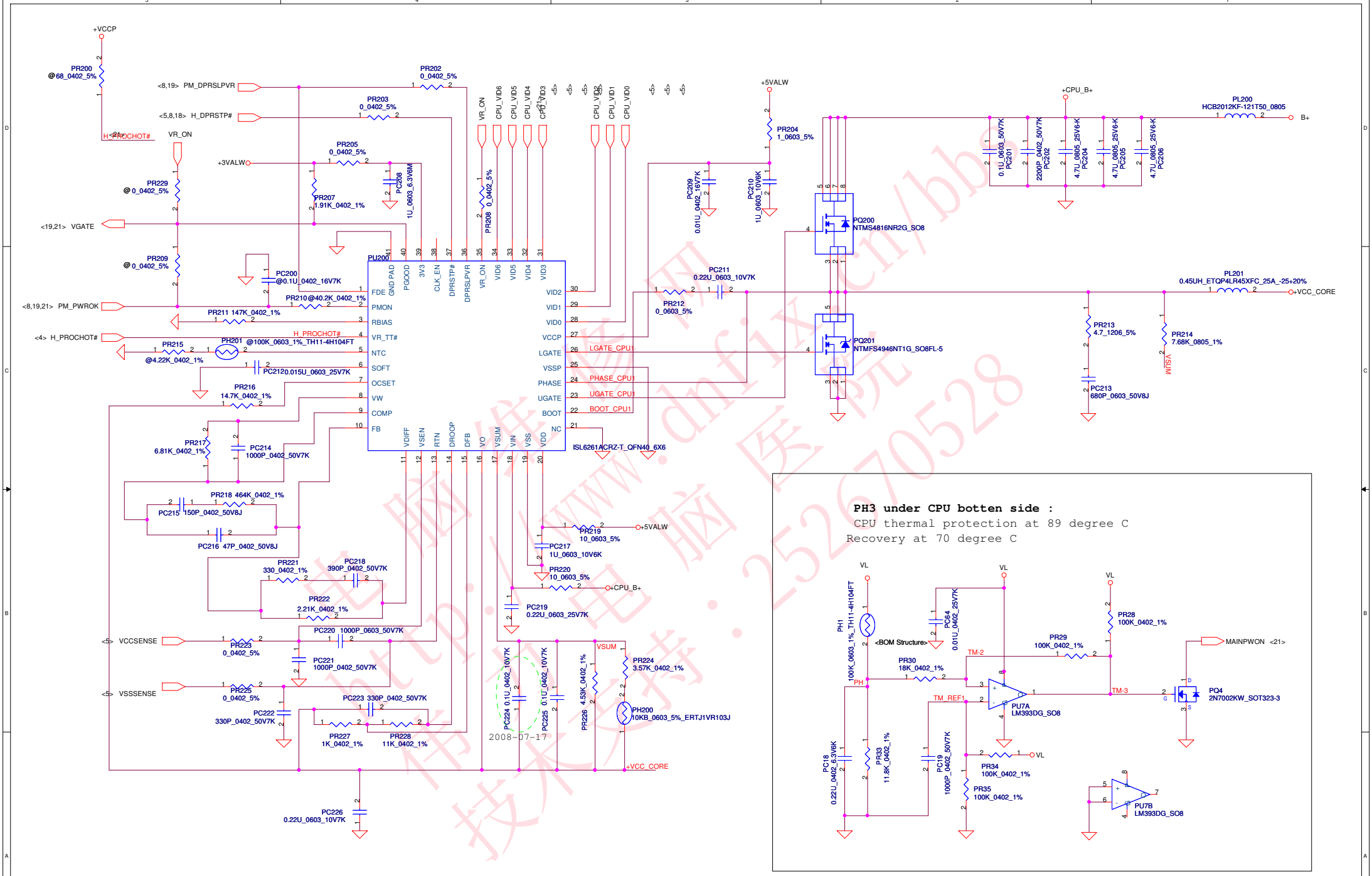
Compal Electronics, Inc.

Title: **0.75VSP**

Size | Document Number: **LS-5581P** | Rev: 2.0

Date: Tuesday, July 21, 2009 | Sheet 27 of 30



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Compal Electronics, Inc.

Title: CPU_CORE

Size: Custom | Document Number: LS-5581P | Rev: 2.0

Date: Thursday, July 23, 2009 | Sheet 28 of 30

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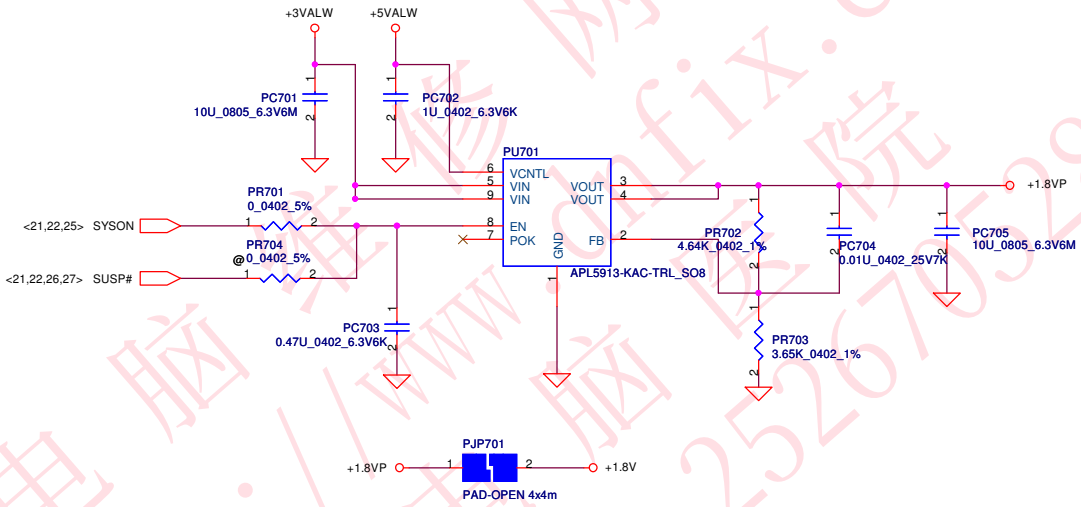

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Issued Date	2008/10/31	Deciphered Date	2009/10/31

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Compal Electronics, Inc.

Title: **1.8VP**

Size | Document Number: *LS-5581P* | Rev: 2.0

Date: Thursday, July 23, 2009 | Sheet 29 of 30

Item	Reason for change	PG#	Modify List	Date	Phase
1	change OTP 89 degree protect 70 degree recover	B	change PR33=11.8k PR30=18k PR29=100k PR28=100K		
2	Change 1.8vp sequence to SYSON	B	Del PR704		
3	Change 1.5vp Voltage set for hw request	B	change PR407 to 10.5K		
4	For slove RT8209 issue	B	change PR405 PR518 to 100 PC406 PC520 to 4.7U		
5	modify PQ600 PQ601 PN follow C38 bom	C	modify 2N7002 from Rohm to toshiba		
6					
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