



Part Number = DA80000FB20

Compal confidential

Schematics Document

Mobile Penryn ULV singal/dual
core with Intel
Cantiga_GS45/GS40 +ICH9-M SFF
core logic

ULV core logic board

2009-07-23

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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电脑维修网
http://www.dnfix.cn/bbs
伟力电脑医院
技术支持: 252670528

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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+B +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground
 : means Analog Ground
@ : means just reserve , no build
CONN@ : means ME part.
45@ : means install after SMT.

SMBUS Control Table

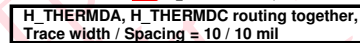
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

	Descrebtion		Descrebtion		Descrebtion
USB port 0	USB connector	PCI-e port 0		SATA port 0	SATA HDD
USB port 1	BT Module	PCI-e port 1	WLAN Conn.	SATA port 1	
USB port 2	cardreader	PCI-e port 2		SATA port 2	WWAN/SSD
USB port 3	USB connector	PCI-e port 3			
USB port 4	WLAN Conn.	PCI-e port 4			
USB port 5	WWAN/SSD	PCI-e port 5	LAN		
USB port 6	USB connector				
USB port 7	CMOS				
USB port 8	Fingerprint				

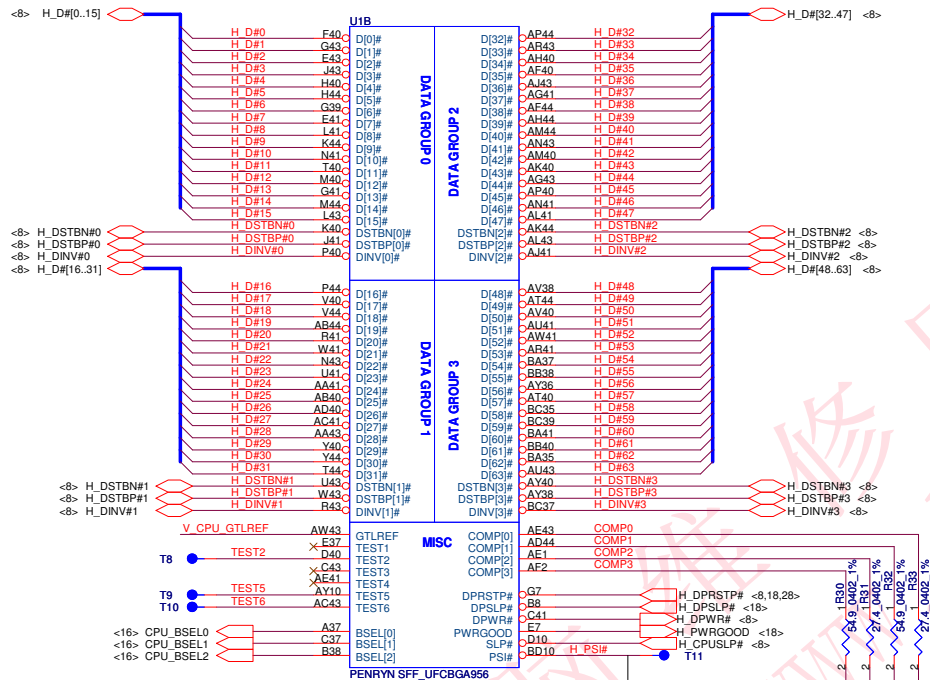
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
CLOCK GENERATOR (EXT.)	D2	11010010

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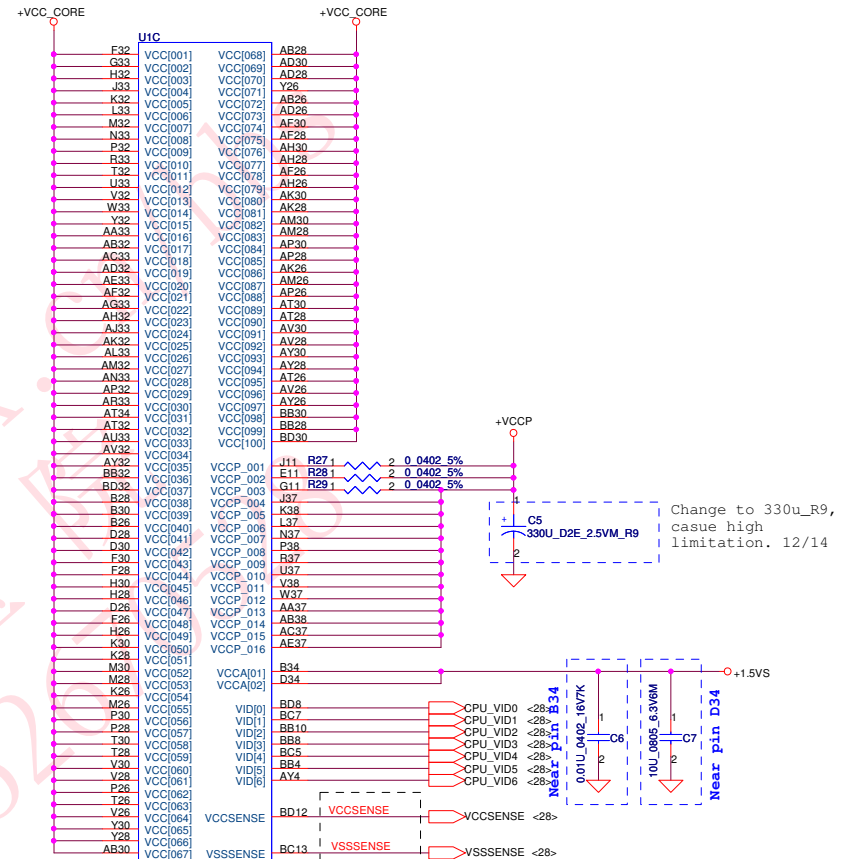
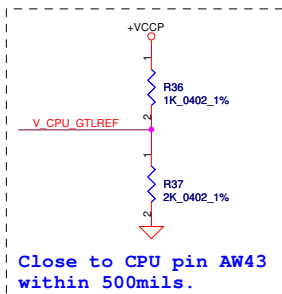
Security Classification	Compal Secret Data			Compal Electronics, Inc. Penryn(1/3)-AGTL+ITP-XDP		
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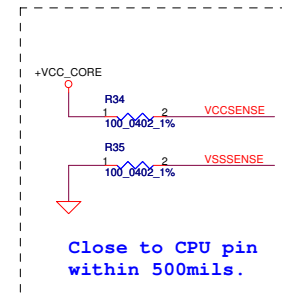
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

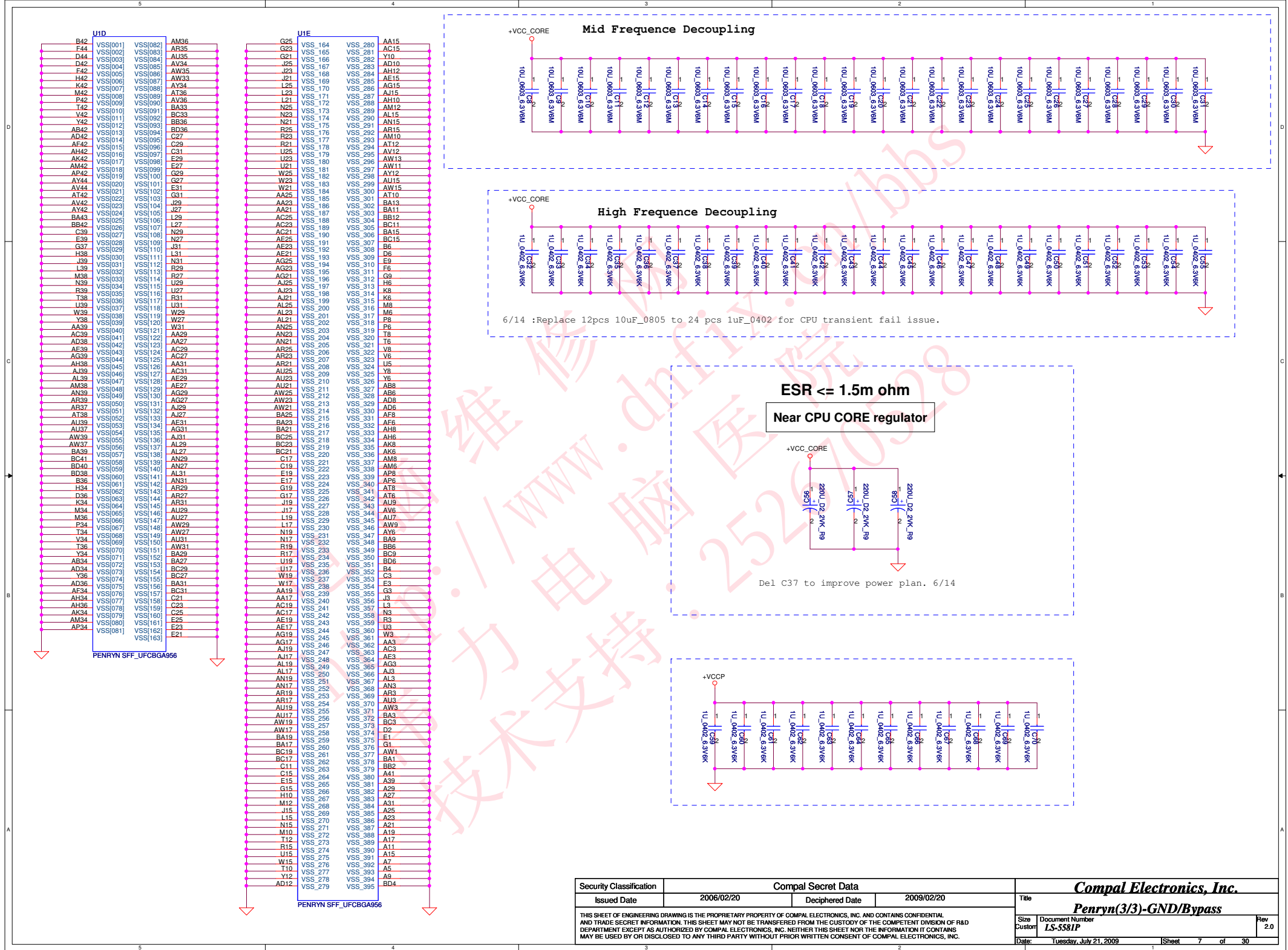
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

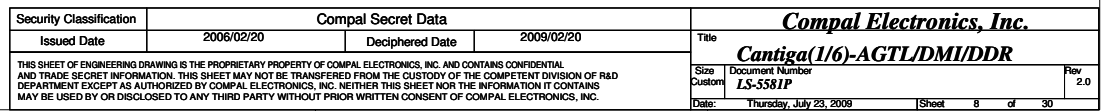
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

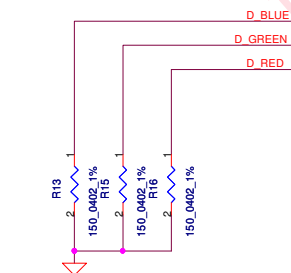
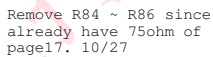


Length match within 25 mils. The trace width/space/other is 20/7/25.









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				Cantiga(3/6)-VGA/LVDS/TV						
				Size	Document Number		Rev			
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U3I		
BA55	VSS_1	VSS_100
AU55	VSS_2	A43
AN55	VSS_3	VSS_101
AJ55	VSS_4	VSS_102
AE55	VSS_5	VSS_103
AA55	VSS_6	VSS_104
U55	VSS_7	VSS_105
N55	VSS_8	VSS_106
BD54	VSS_9	VSS_107
BG53	VSS_10	VSS_108
AJ53	VSS_11	VSS_109
AE53	VSS_12	VSS_110
AA53	VSS_13	VSS_111
U53	VSS_14	VSS_112
N53	VSS_15	VSS_113
J53	VSS_16	VSS_114
G53	VSS_17	VSS_115
E53	VSS_18	VSS_116
K52	VSS_19	VSS_117
BG51	VSS_20	VSS_118
BA51	VSS_21	VSS_119
AW51	VSS_22	VSS_120
AJ51	VSS_23	VSS_121
AE51	VSS_24	VSS_122
AA51	VSS_25	VSS_123
U51	VSS_26	VSS_124
N51	VSS_27	VSS_125
J51	VSS_28	VSS_126
G51	VSS_29	VSS_127
E51	VSS_30	VSS_128
K51	VSS_31	VSS_129
BG50	VSS_32	VSS_130
BA50	VSS_33	VSS_131
AW50	VSS_34	VSS_132
AJ50	VSS_35	VSS_133
AE50	VSS_36	VSS_134
AA50	VSS_37	VSS_135
U50	VSS_38	VSS_136
N50	VSS_39	VSS_137
J50	VSS_40	VSS_138
G50	VSS_41	VSS_139
E50	VSS_42	VSS_140
K50	VSS_43	VSS_141
BG49	VSS_44	VSS_142
BA49	VSS_45	VSS_143
AW49	VSS_46	VSS_144
AJ49	VSS_47	VSS_145
AE49	VSS_48	VSS_146
AA49	VSS_49	VSS_147
U49	VSS_50	VSS_148
N49	VSS_51	VSS_149
J49	VSS_52	VSS_150
G49	VSS_53	VSS_151
E49	VSS_54	VSS_152
K49	VSS_55	VSS_153
BG48	VSS_56	VSS_154
BA48	VSS_57	VSS_155
AW48	VSS_58	VSS_156
AJ48	VSS_59	VSS_157
AE48	VSS_60	VSS_158
AA48	VSS_61	VSS_159
U48	VSS_62	VSS_160
N48	VSS_63	VSS_161
J48	VSS_64	VSS_162
G48	VSS_65	VSS_163
E48	VSS_66	VSS_164
K48	VSS_67	VSS_165
BG47	VSS_68	VSS_166
BA47	VSS_69	VSS_167
AW47	VSS_70	VSS_168
AJ47	VSS_71	VSS_169
AE47	VSS_72	VSS_170
AA47	VSS_73	VSS_171
U47	VSS_74	VSS_172
N47	VSS_75	VSS_173
J47	VSS_76	VSS_174
G47	VSS_77	VSS_175
E47	VSS_78	VSS_176
K47	VSS_79	VSS_177
BG46	VSS_80	VSS_178
BA46	VSS_81	VSS_179
AW46	VSS_82	VSS_180
AJ46	VSS_83	VSS_181
AE46	VSS_84	VSS_182
AA46	VSS_85	VSS_183
U46	VSS_86	VSS_184
N46	VSS_87	VSS_185
J46	VSS_88	VSS_186
G46	VSS_89	VSS_187
E46	VSS_90	VSS_188
K46	VSS_91	VSS_189
BG45	VSS_92	VSS_190
BA45	VSS_93	VSS_191
AW45	VSS_94	VSS_192
AJ45	VSS_95	VSS_193
AE45	VSS_96	VSS_194
AA45	VSS_97	VSS_195
U45	VSS_98	VSS_196
N45	VSS_99	VSS_197
J45		VSS_198

VSS

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U3J		
AN25	VSS_199	VSS_300
AG25	VSS_200	VSS_301
AE25	VSS_201	VSS_302
AA25	VSS_202	VSS_303
U25	VSS_203	VSS_304
E25	VSS_204	VSS_305
A25	VSS_205	VSS_306
BD24	VSS_206	VSS_307
AN24	VSS_207	VSS_308
AL24	VSS_208	VSS_309
H24	VSS_209	VSS_310
BG23	VSS_210	VSS_311
AY23	VSS_211	VSS_312
E23	VSS_212	VSS_313
BD22	VSS_213	VSS_314
BB22	VSS_214	VSS_315
AN22	VSS_215	VSS_316
Y22	VSS_216	VSS_317
W22	VSS_217	VSS_318
H22	VSS_218	VSS_319
BL21	VSS_219	VSS_320
BG21	VSS_220	VSS_321
AY21	VSS_221	VSS_322
AN21	VSS_222	VSS_323
AG21	VSS_223	VSS_324
AE21	VSS_224	VSS_325
M21	VSS_225	VSS_326
E21	VSS_226	VSS_327
A21	VSS_227	VSS_328
BD20	VSS_228	VSS_329
H20	VSS_229	VSS_330
BG19	VSS_230	VSS_331
AY19	VSS_231	VSS_332
M19	VSS_232	VSS_333
E19	VSS_233	VSS_334
BD18	VSS_234	VSS_335
N18	VSS_235	VSS_336
H18	VSS_236	VSS_337
BL17	VSS_237	VSS_338
BG17	VSS_238	VSS_339
AY17	VSS_239	VSS_340
M17	VSS_240	VSS_341
E17	VSS_241	VSS_342
A17	VSS_242	VSS_343
BD16	VSS_243	VSS_344
AN16	VSS_244	VSS_345
AG16	VSS_245	VSS_346
AE16	VSS_246	VSS_347
Y16	VSS_247	VSS_348
W16	VSS_248	VSS_349
N16	VSS_249	VSS_350
H16	VSS_250	VSS_351
BG15	VSS_251	VSS_352
AY15	VSS_252	VSS_353
AN15	VSS_253	VSS_354
AD15	VSS_254	VSS_355
AC15	VSS_255	VSS_356
R15	VSS_256	VSS_357
M15	VSS_257	VSS_358
E15	VSS_258	
BD14	VSS_259	VSS_359
H14	VSS_260	VSS_360
BL13	VSS_261	VSS_361
BG13	VSS_262	VSS_362
AY13	VSS_263	
U13	VSS_264	VSS_NCTF_1
AR13	VSS_265	VSS_NCTF_2
AJ13	VSS_266	VSS_NCTF_3
AC13	VSS_267	VSS_NCTF_4
AA13	VSS_268	VSS_NCTF_5
W13	VSS_269	VSS_NCTF_6
U13	VSS_270	VSS_NCTF_7
M13	VSS_271	VSS_NCTF_8
E13	VSS_272	VSS_NCTF_9
A13	VSS_273	VSS_NCTF_10
BD12	VSS_274	VSS_NCTF_11
AV12	VSS_275	VSS_NCTF_12
AP12	VSS_276	VSS_NCTF_13
AM12	VSS_277	VSS_NCTF_14
AK12	VSS_278	VSS_NCTF_15
AB12	VSS_279	VSS_NCTF_16
V12	VSS_280	VSS_NCTF_17
P12	VSS_281	VSS_NCTF_18
H12	VSS_282	VSS_NCTF_19
BG11	VSS_283	VSS_NCTF_20
AG11	VSS_284	VSS_NCTF_21
E11	VSS_285	VSS_NCTF_22
BD10	VSS_286	VSS_NCTF_23
AY10	VSS_287	
AP10	VSS_288	
H10	VSS_289	
BL9	VSS_290	
BC9	VSS_291	
E9	VSS_292	
A9	VSS_293	
BD8	VSS_294	
BB8	VSS_295	
AV8	VSS_296	
AT8	VSS_297	
AP8	VSS_298	
	VSS_299	

VSS

VSS NCTF

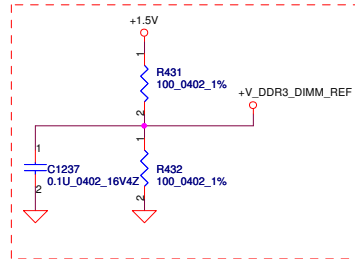
VSS SCB

VSS_NCTF_1	AJ38
VSS_NCTF_2	AD38
VSS_NCTF_3	AC38
VSS_NCTF_4	T35
VSS_NCTF_5	R35
VSS_NCTF_6	AT32
VSS_NCTF_7	AR32
VSS_NCTF_8	U32
VSS_NCTF_9	E32
VSS_NCTF_10	T28
VSS_NCTF_11	B28
VSS_NCTF_12	AT25
VSS_NCTF_13	AR25
VSS_NCTF_14	T24
VSS_NCTF_15	R24
VSS_NCTF_16	AN19
VSS_NCTF_17	AJ19
VSS_NCTF_18	AA19
VSS_NCTF_19	Y19
VSS_NCTF_20	T19
VSS_NCTF_21	R19
VSS_NCTF_22	AN18
VSS_NCTF_23	

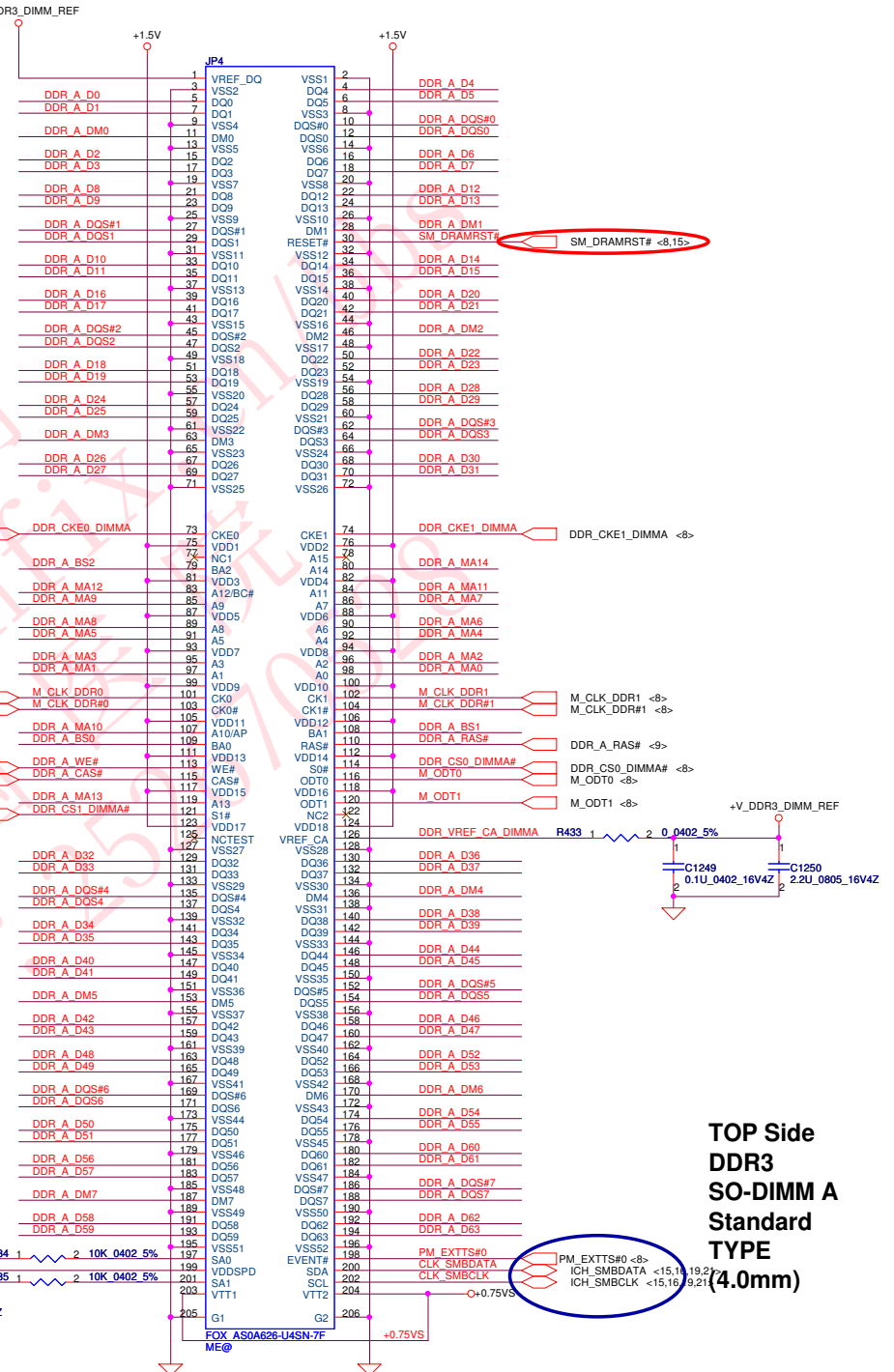
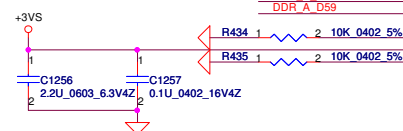
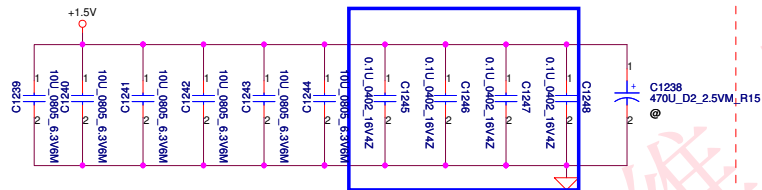
VSS_SCB_1	BL55
VSS_SCB_2	BL1
VSS_SCB_3	A55
VSS_SCB_4	D1
VSS_SCB_5	B55
VSS_SCB_6	B2
VSS_SCB_7	A4

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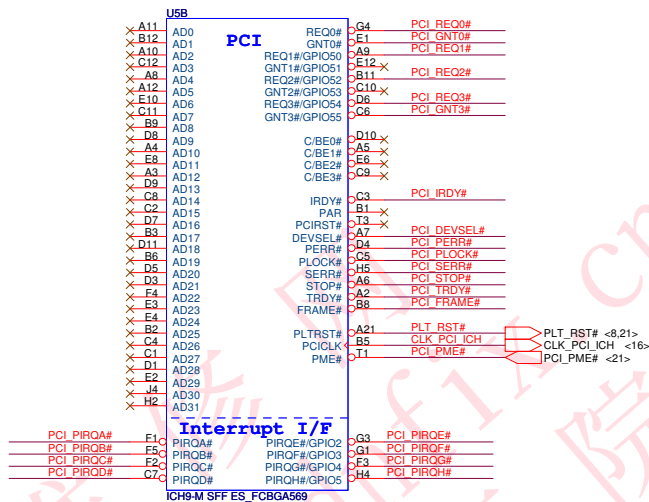
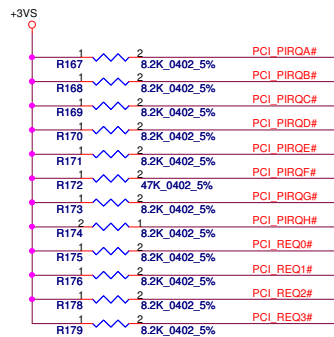
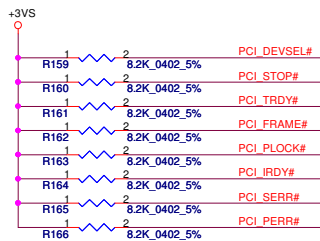


Layout Note: Place these 4 Caps near Command and Control signals of DIMMA - - - - -

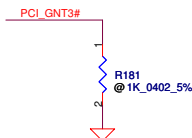


**TOP Side
DDR3
SO-DIMM A
Standard
TYPE
(4.0mm)**

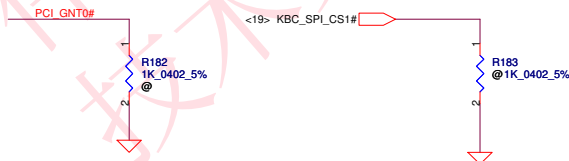
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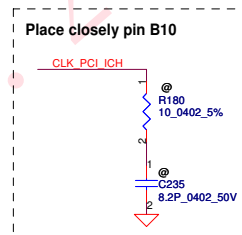
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*



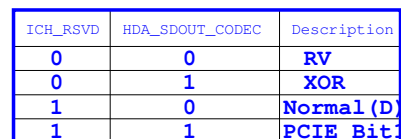
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



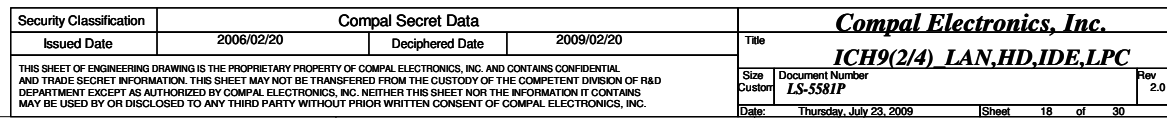
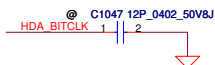
DEL J3. 9/29

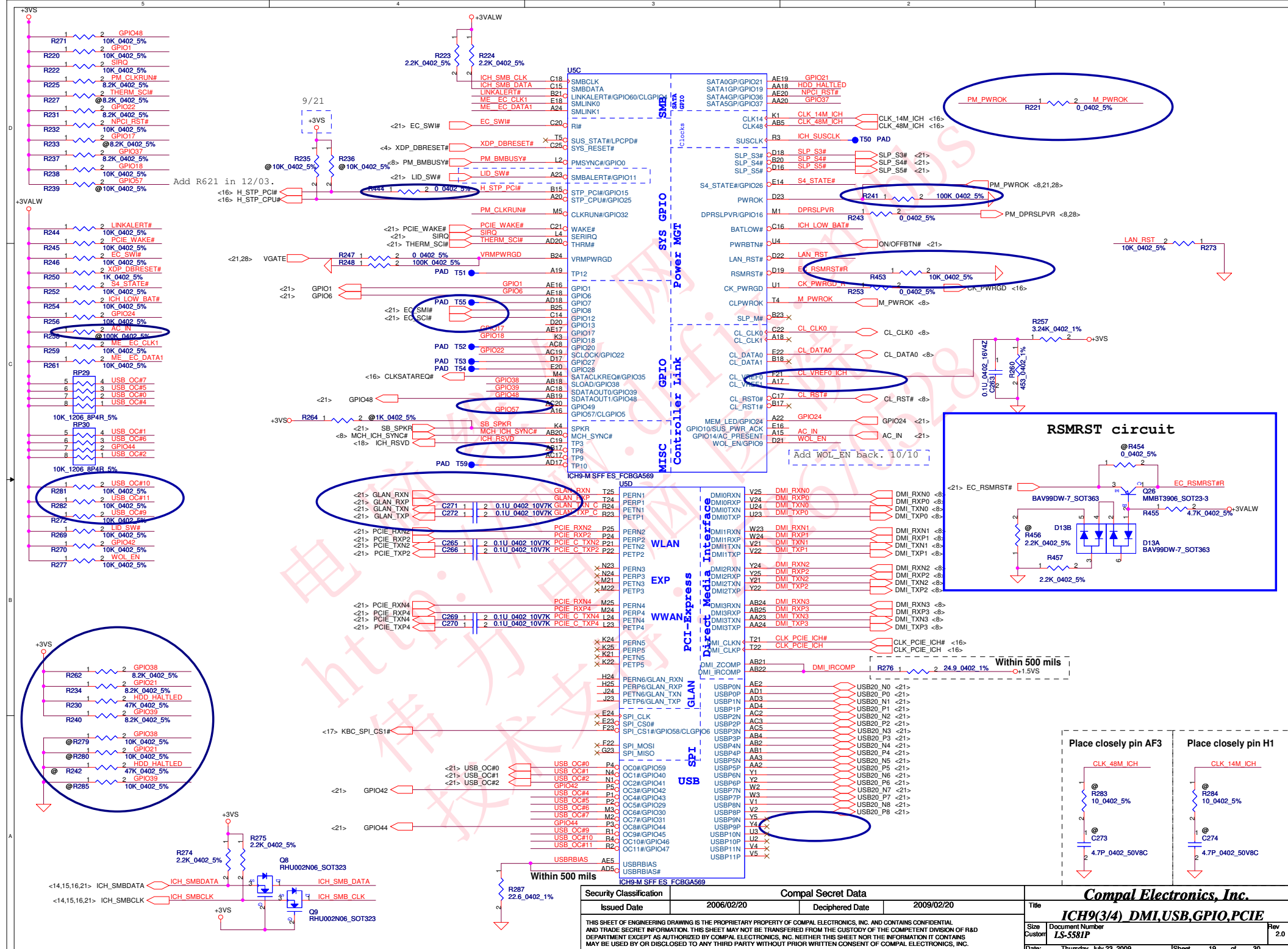


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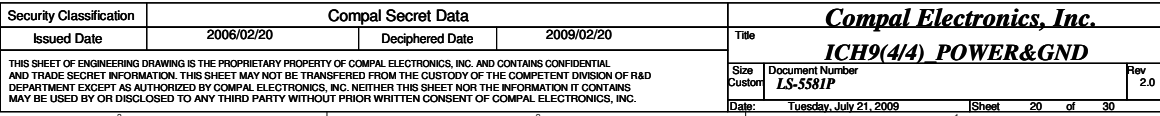


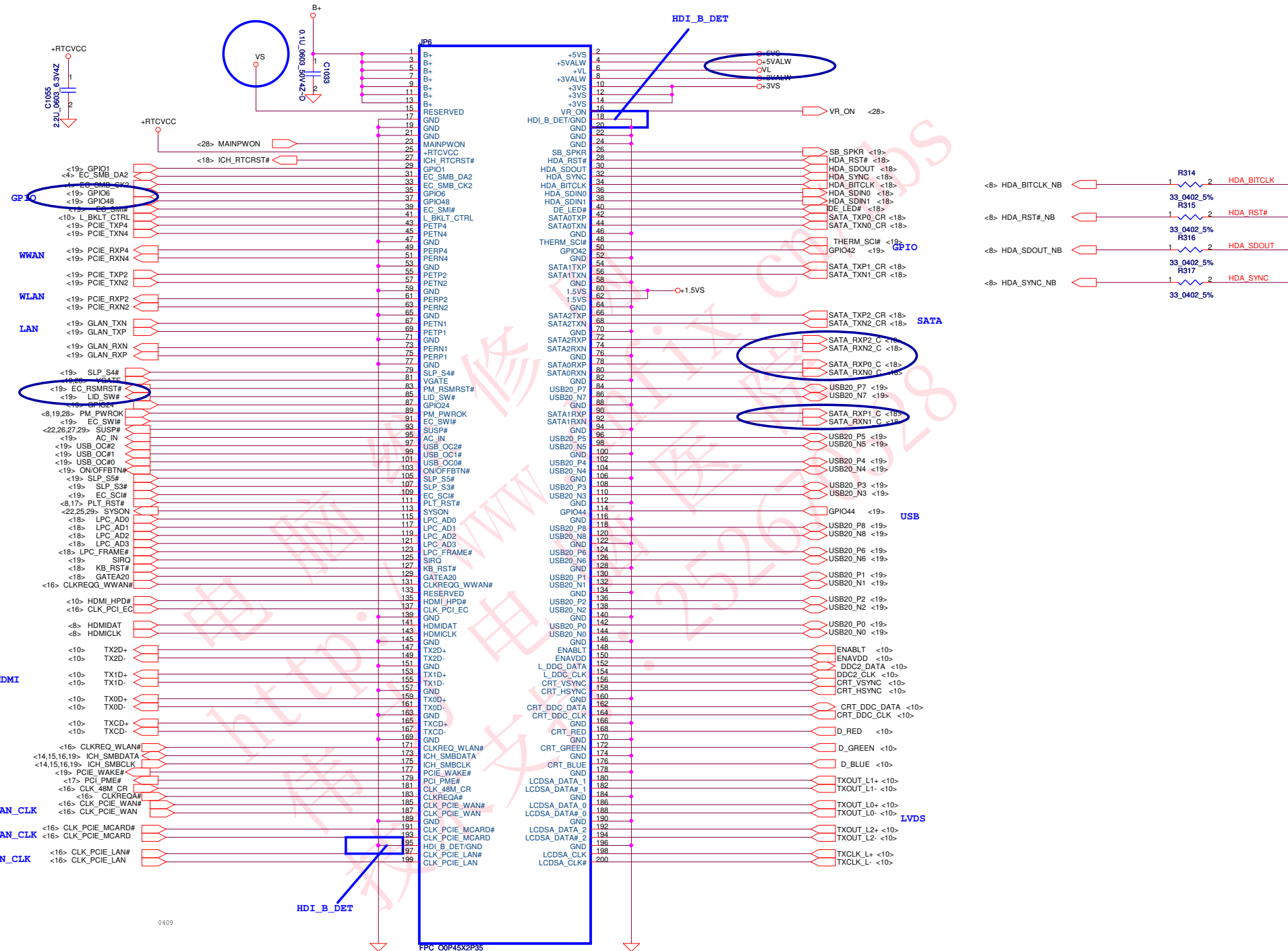
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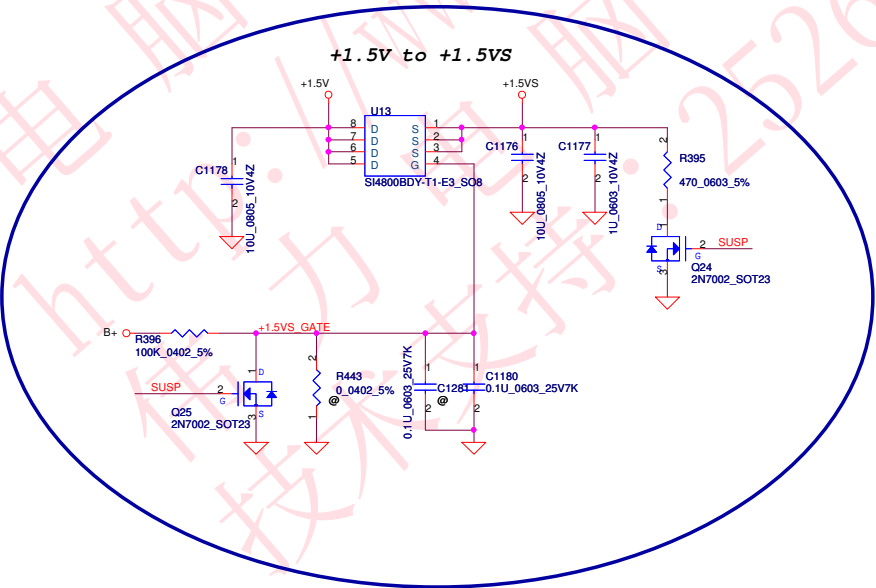
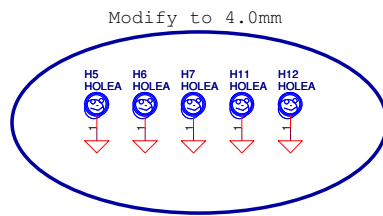
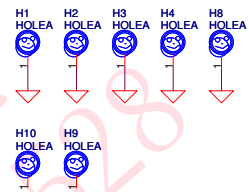
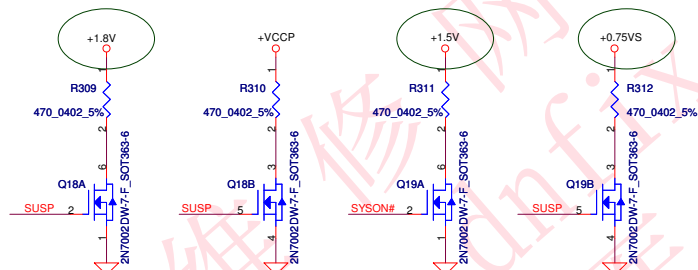
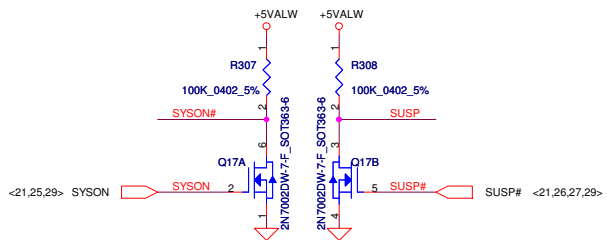
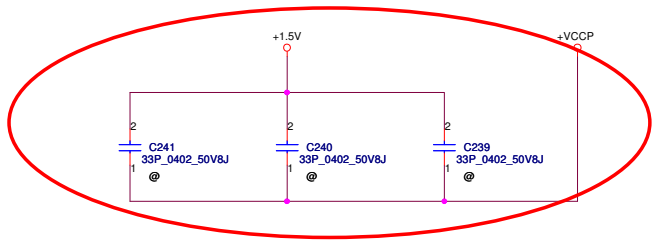


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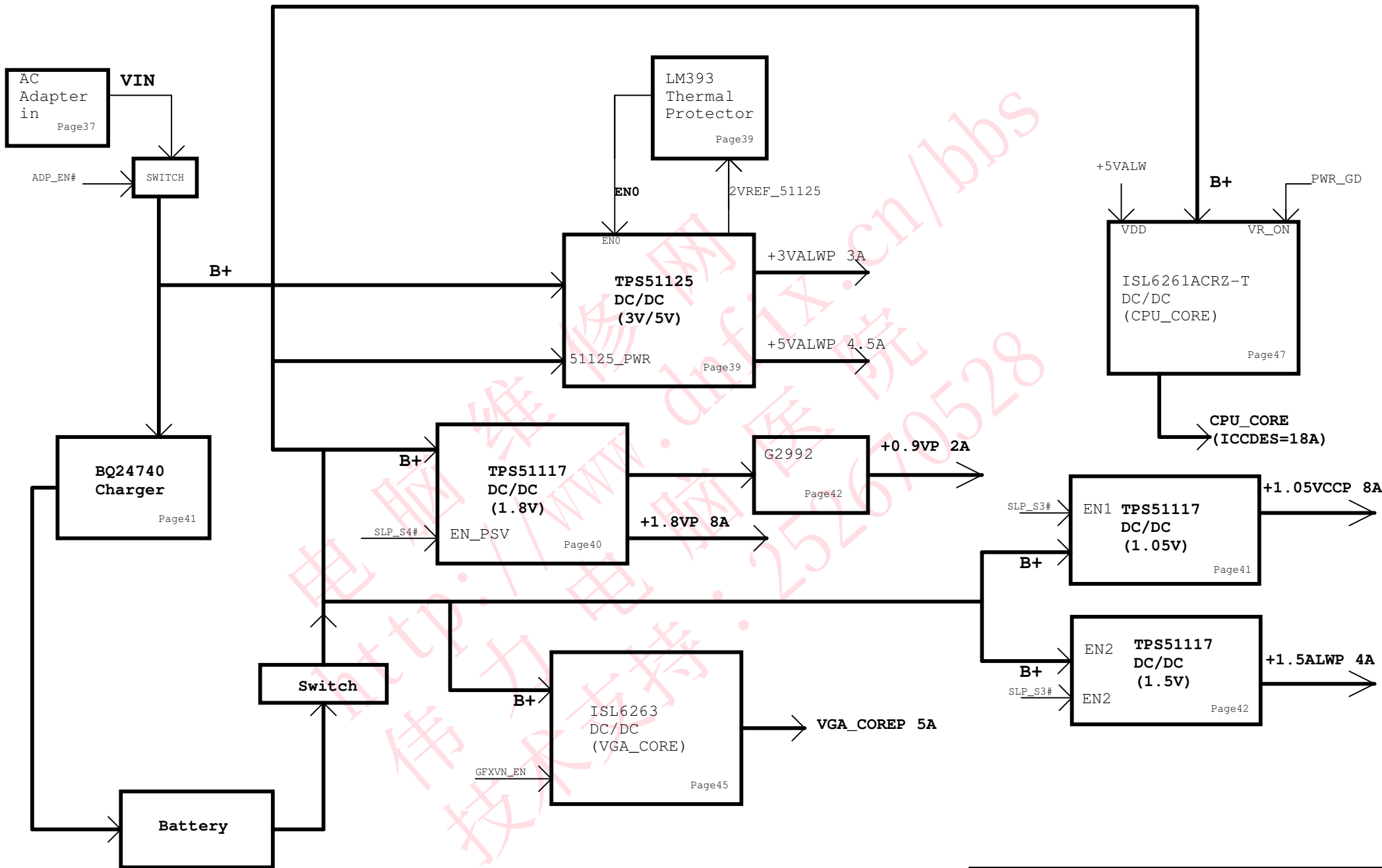
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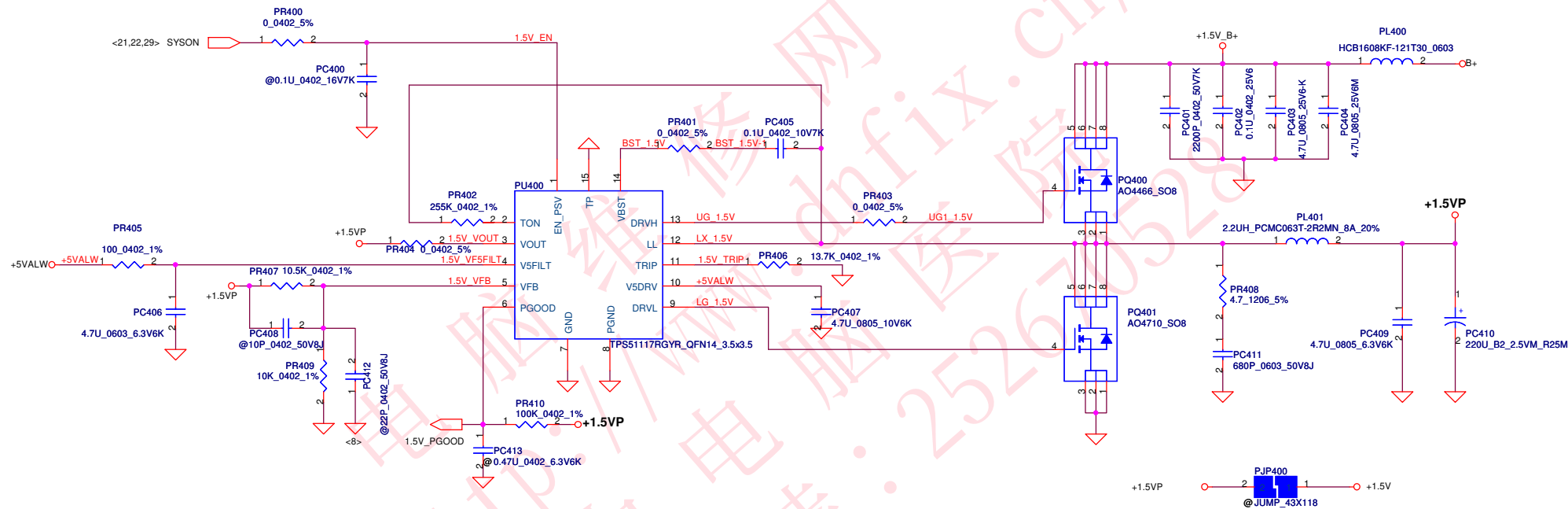
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Date	Descreibung	Rev.
4/16	Relaese LS5581PR01 schematic.	01
5/8	R53 change to 499 Ohm R68,R69,R70 implement 75Ohm Add C1303 for DDR3 request Change R149,R177 from 33 to 150hm Change C233,C234 from 33P to 22P R153 implement 10K_Ohm and R156 remove Add C1079,C1080 for EMI Delete R249,R255,R267,R268 for optionUSB and GPIO Delete C1066,C1067,C1068,C1069,C1070,C1071 for SATA AC cap Add VL voltage on JP6.6 for OCP use Modify SB VCCSUSHDA power level Modify SB GLAN fromPCIE4 to PCIE1 Delete R265,C264,C266 for CL_REF1 Delete R240 for H_STP_CPU# and Add R444 for H_STP_PCI# Change R221 connect from VGATE to PM_PWROK Change R240 from H_STP_CPU# to H_STP_PCI# Change EC_SCI# from GPIO7 to GPIO12 Delete T56,T57,T58,R263 for no use Add R281,R282 for USB OC# pull high Add R242,R285 for Project ID define Modify H5,H6,H7,H11,H12 footprint for ME recommand Delete R251 and Add Q26,D13,R453-R457 for RSMRST# function Delete USB9 pair on SB for not use Modify CLK_PCI_EC from U4.15 to U4.13 Modify power plane from +1.8VS to +1.8V for NB use Change Name from DDR3_DIMM_REF to DDR3_NB_REF for DDR3 recommand Change DDR PM_EXTIS# 1 from not use to JP3 Del R106 for Intel Recommand for HDMI setting	

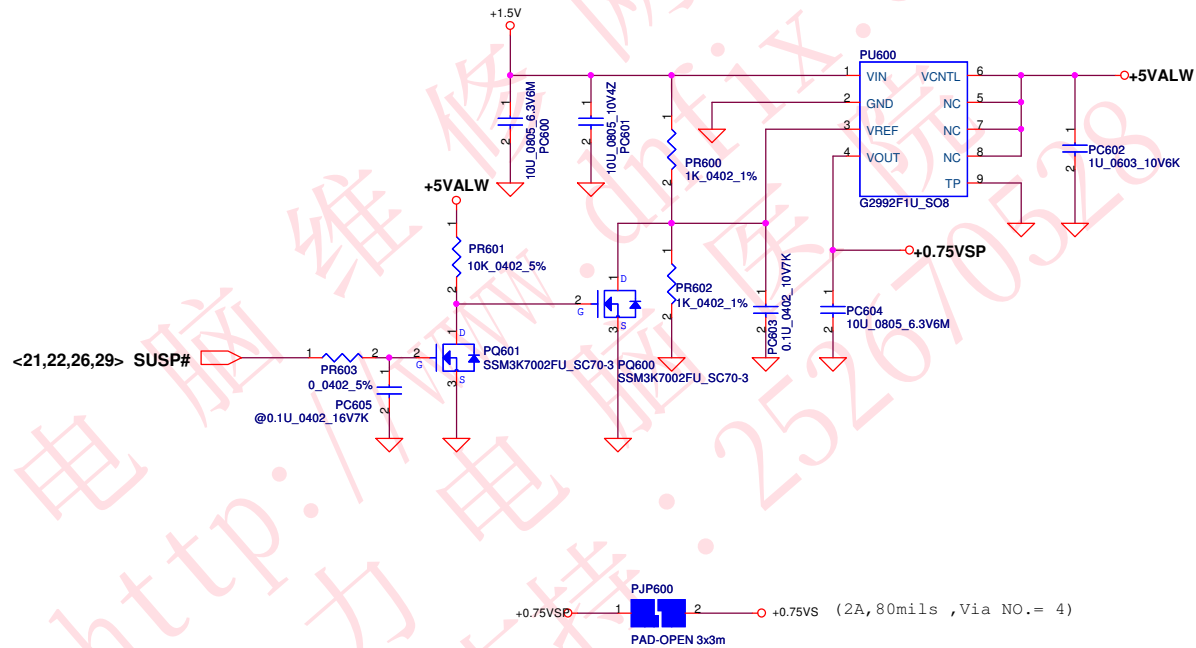
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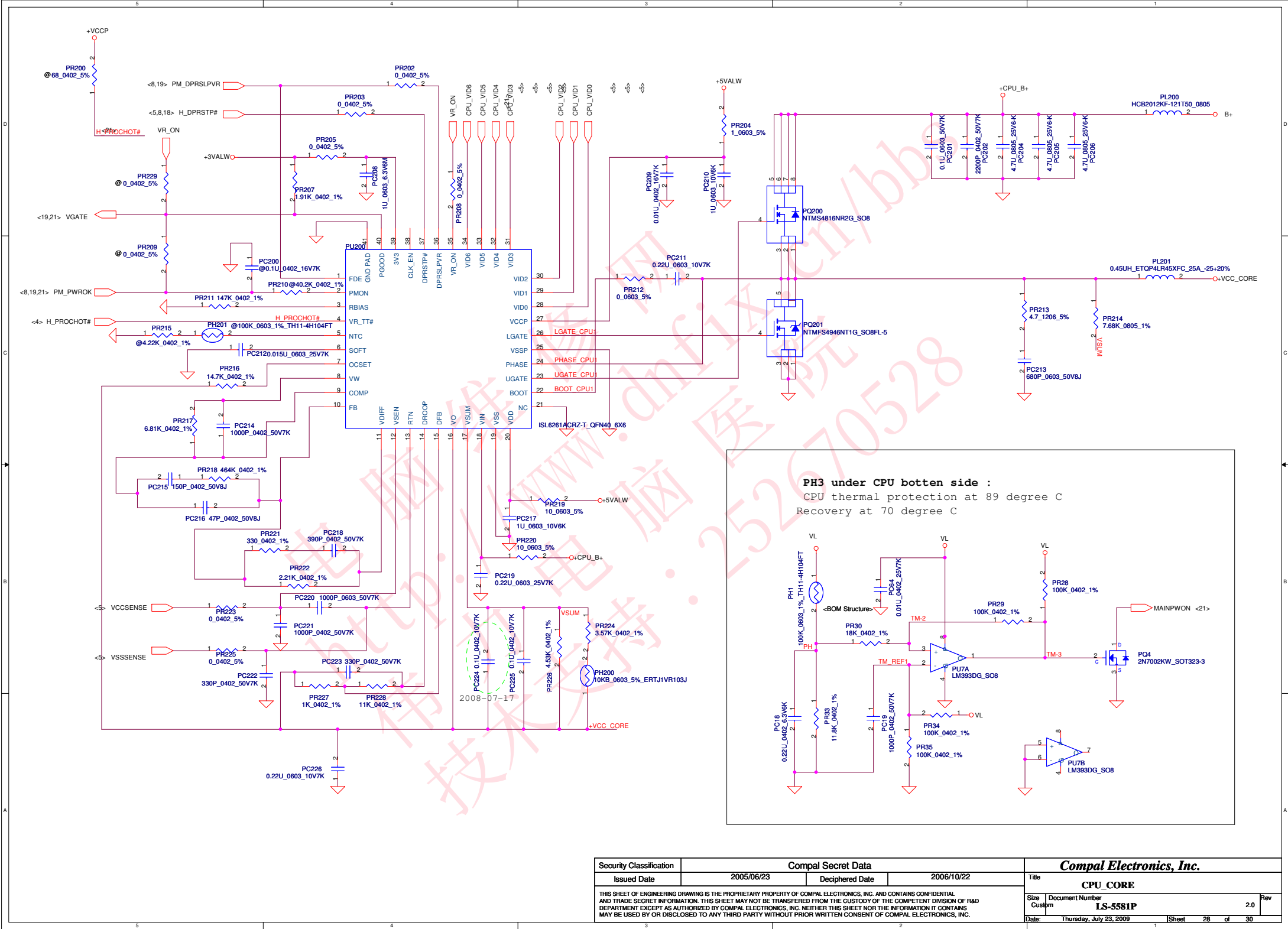
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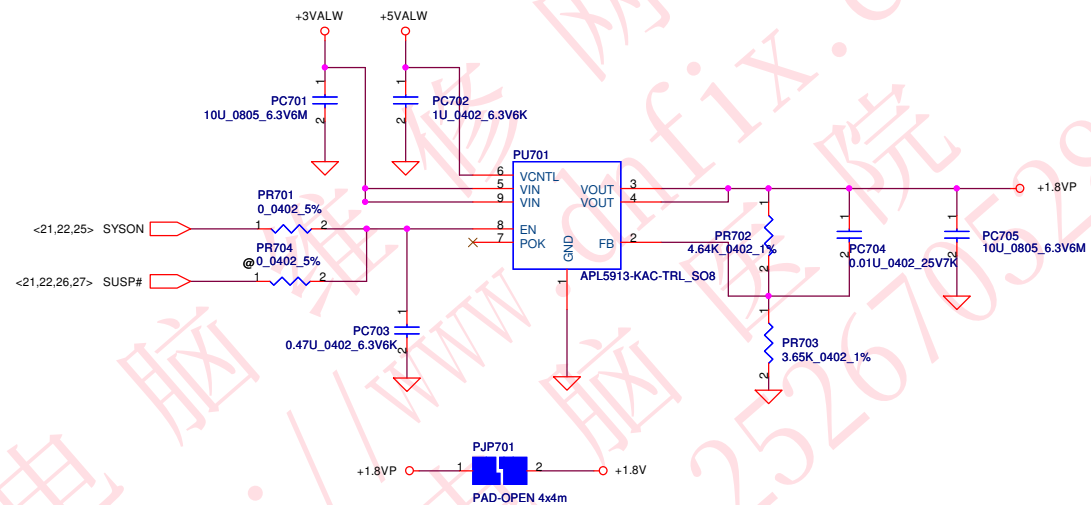
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Item	Reason for change	PG#	Modify List	Date	Phase
1	change OTP 89 degree protect 70 degree recover	B	change PR33=11.8k PR30=18k PR29=100k PR28=100K		
2	Change 1.8vp sequence to SYSON	B	Del PR704		
3	Change 1.5vp Voltage set for hw request	B	change PR407 to 10.5K		
4	For solve RT8209 issue	B	change PR405 PR518 to 100 PC406 PC520 to 4.7U		
5	modify PQ600 PQ601 PN follow C38 bom	C	modify 2N7002 from Rohm to toshiba		
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