

Compal Confidential

Cougar

LA-6851P Schematics Document

Intel Pine View Processor/ Tiger point

2010-10-10

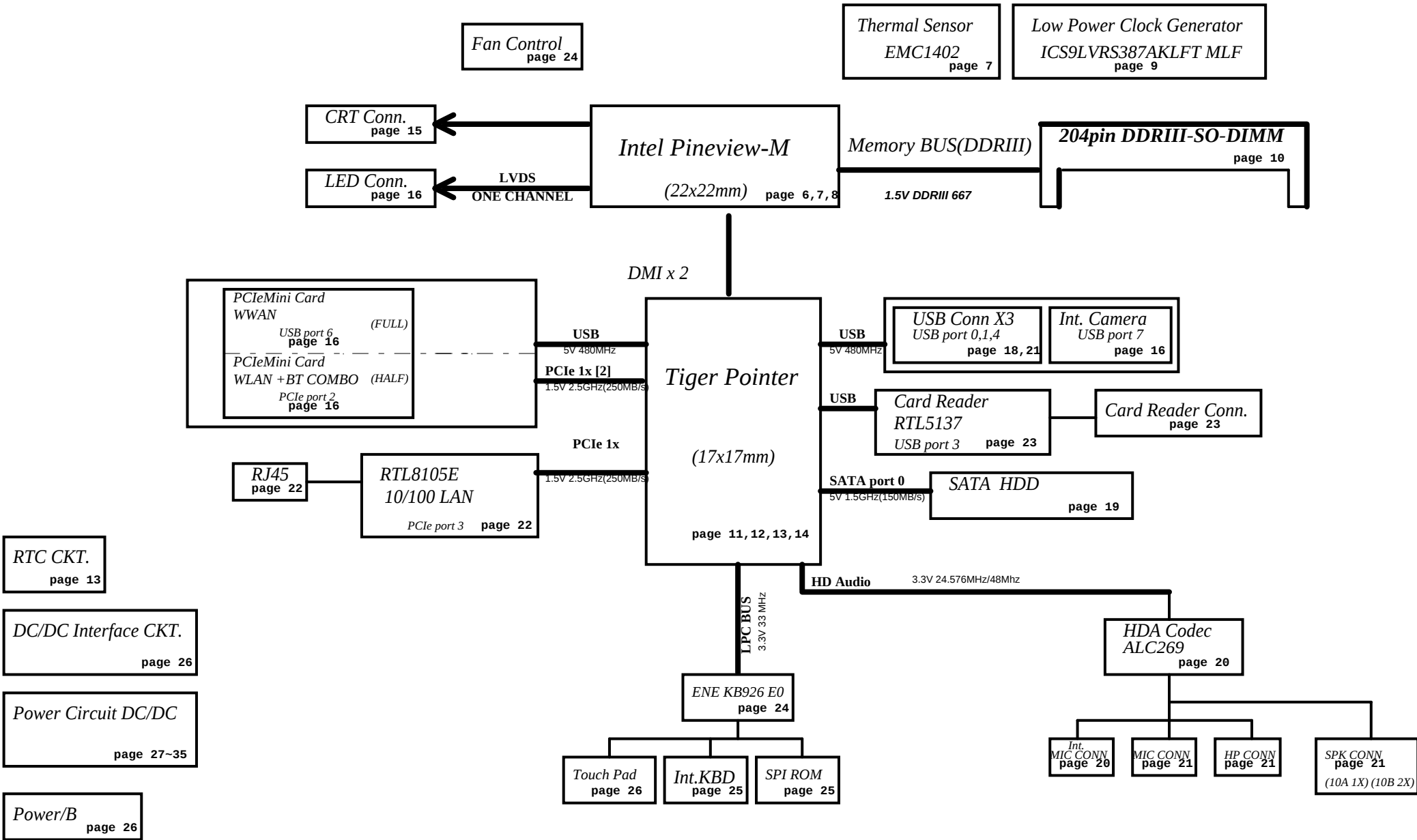
REV: 1.0

Toshiba Satellite NB500 NB505

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Issued Date	2010/06/27	Deciphered Date	2011/6/27	Title	SCHEMATIC MB A6851
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				Date	Friday, September 02, 2011
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				Rev	D

Compal Confidential

Model Name : PBU00
File Name : LA-6851P



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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.89VS	0.89VS GFX support voltage	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	VCCP switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	ON	OFF	OFF
+5VALW	5V always on power rail	ON	OFF	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

Function	Mini PCI-E SLOT				CAMERA & MIC		BLUE T00TH		Clock gen	
description										
explain	Wi-Fi	WiMax	3GGPS	3G	CAMERA	MIC	BLUE T00TH		Tpye	
BTO	WLAN@	WIMAX@	3GGPS@	3G@	CAM@	MIC@	BT@		low@	normal@

Function			
description			
explain			
BTO			

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 010X b

EC SM Bus2 address

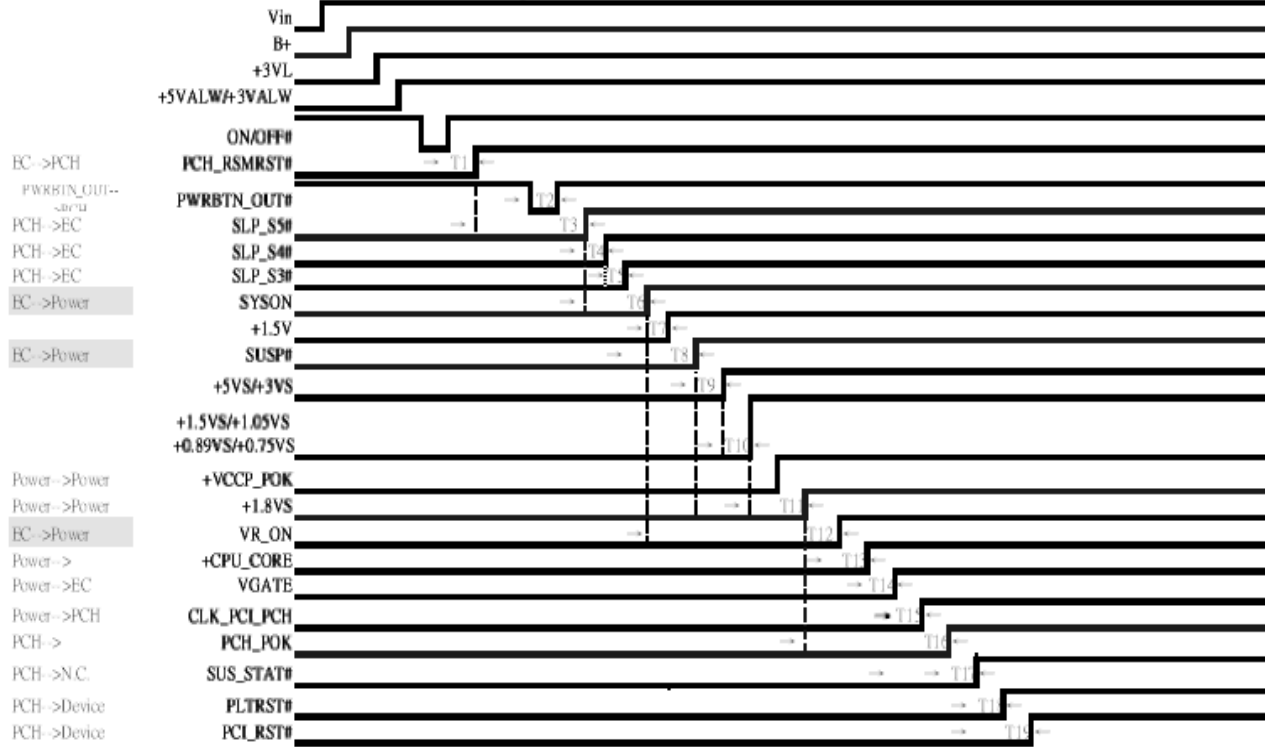
ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP56VTR)	1101 001Xb
DDR DIMMA	1010 000Xb
WWAN/WLAN	

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PBU00 Power ON sequence

2010/7/2



Power-on Sequence

Time	Description	Expected
T1	Power Button active to PCH_RSMRST# inactive	> 105ms
T2	Power Button active to PBTN_OUT# inactive	< T1
T3	PCH_RSMRST# inactive to PM_SLP_S5# inactive	< 110ms
T4	PM_SLP_S5# inactive to PM_SLP_S4# inactive	28.992us ~ 64.088us
T5	PM_SLP_S4# inactive to PM_SLP_S3# inactive	28.992us ~ 64.088us
T6	PM_SLP_S3# inactive to SYSON active	>10ms
T7	SYSON active to +1.5V active	>0
T8	PM_SLP_S3# inactive to SUSP# inactive	>10ms
T9	SUSP# inactive to +5VS active	>0
T9	SUSP# inactive to +3VS active	>0
T10	SUSP# inactive to +1.5VS active	> 0
T10	SUSP# inactive to +0.89VS active	> 0
T10	SUSP# inactive to +1.05VS active	> 0
T10	SUSP# inactive to +0.75VS active	>0
T11	+1.05VS inactive to +1.8VS active	>0
T12	SUSP# inactive to VR_ON active	>10ms
T13	VR_ON active to +CPU_CORE active	>0
T14	+CPU_CORE active to VGATE	<10ms
T15	VGATE active to CLK_PCI_ICH stable	< 1.8ms
T16	+1.5VS power active to ICH_PWROK active	>99ms
T17	ICH_PWROK active to SUS_STAT# inactive	0.928ms ~ 1.218ms
T18	SUS_STAT# inactive to PLT_RST# inactive	57.984us ~ 96.132us
T23	SUS_STAT# inactive to PCI_RST# inactive	57.984us ~ 96.132us

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Cougar Power Map

B+

DESIGN CURRENT 250mA

Ipeak=6.97A, Imax=4.88A

DESIGN CURRENT 522mA

+3VALWP +-5%

UP6182CQAG

** The SW just is reserved.
The power passes by jump or
0-ohm resistor.

WOL_EN#

** P-CHANNEL
A03413

DESIGN CURRENT 300mA

+3V_LAN

Ipeak=3.98A, Imax=2.8A

DESIGN CURRENT 3010mA

+5VALWP +-5%

SUSP

N-CHANNEL
SI4800BDY

DESIGN CURRENT 2286mA

+5VS

SUSP

N-CHANNEL
SI4800BDY

DESIGN CURRENT 5586mA

+3VS

ENVDD

P-CHANNEL
A03413

DESIGN CURRENT 2000mA

+LCD_VDD

SUSP#

SY8033BDBC

DESIGN CURRENT 2640mA

+0.89VSP

SUSP#

SY8033BDBC

Ipeak=1.308A, Imax=4A

DESIGN CURRENT 3489mA

+1.05VSP +-5%

VR_ON

ADP3211AMNR2G

Imax=3.5A

DESIGN CURRENT 6000mA

+CPU_CORE

SYSON

G5603RU1U

Ipeak=19.6A, Imax=13.72A

DESIGN CURRENT 2000mA

+1.5VP +-5%

SUSP#

IRF8113PBF

DESIGN CURRENT 2112mA

+1.5VSP

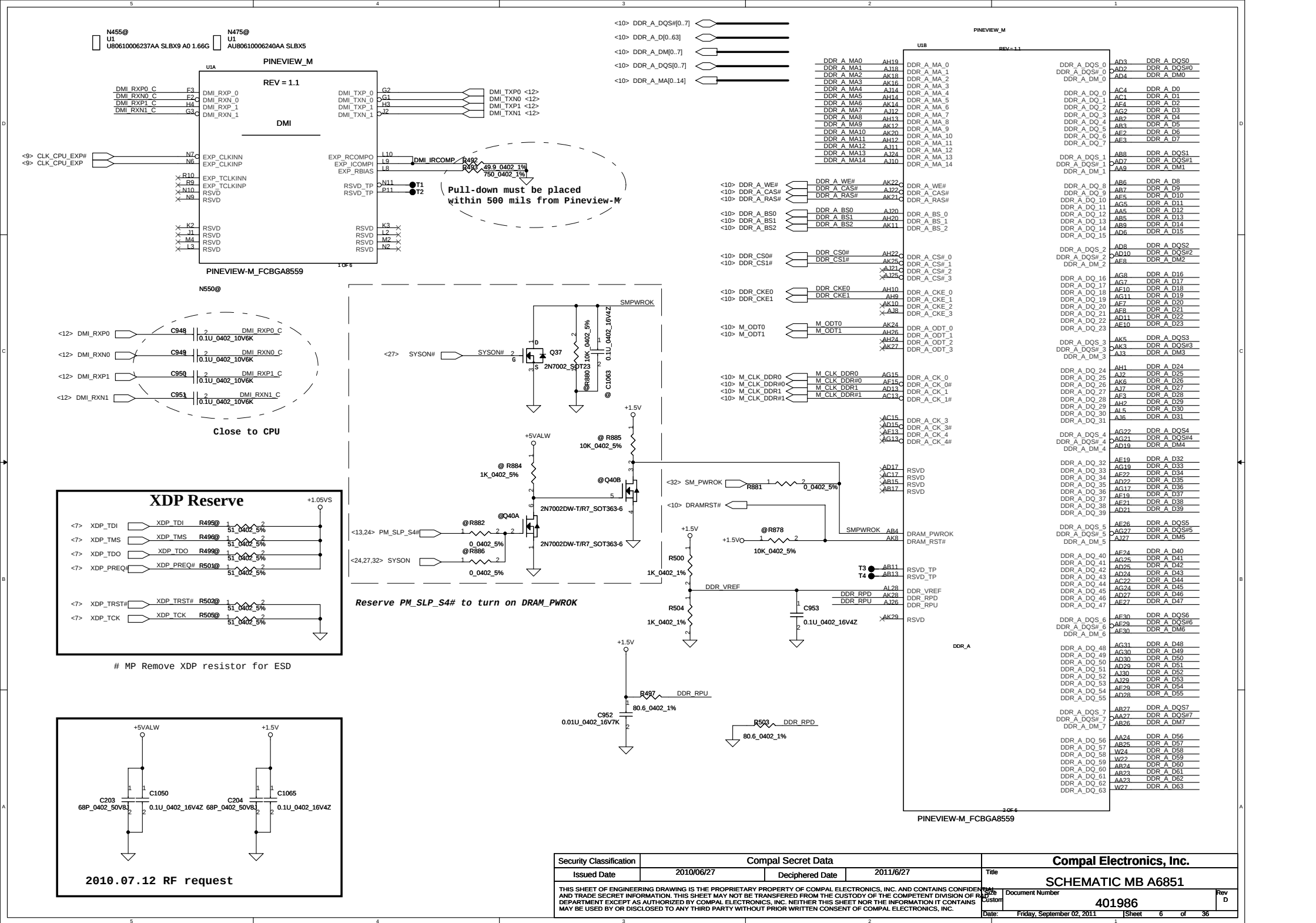
SUSP

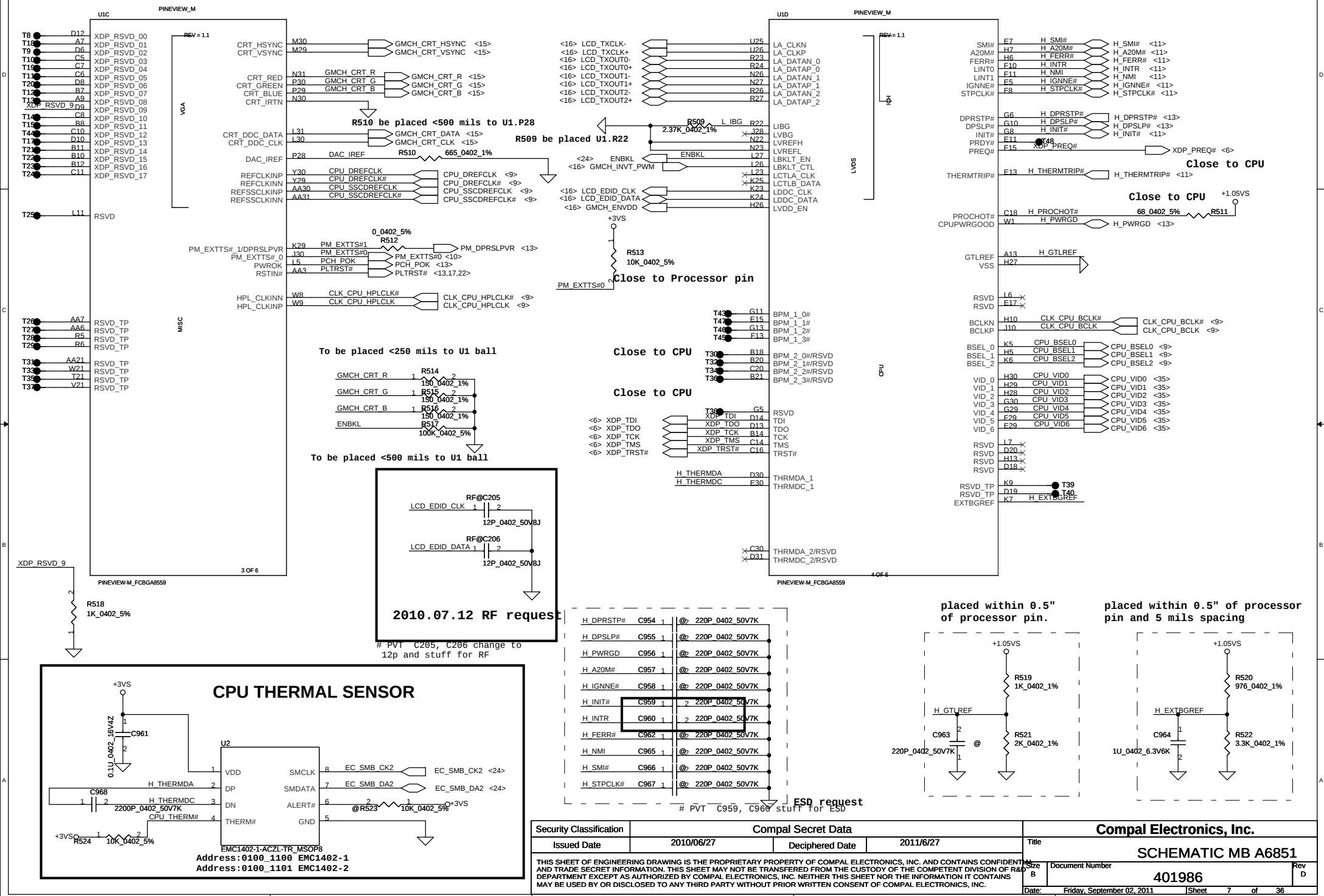
UP7711U8

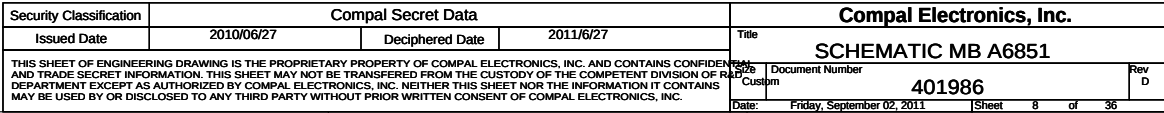
DESIGN CURRENT 500mA

+0.75VSP

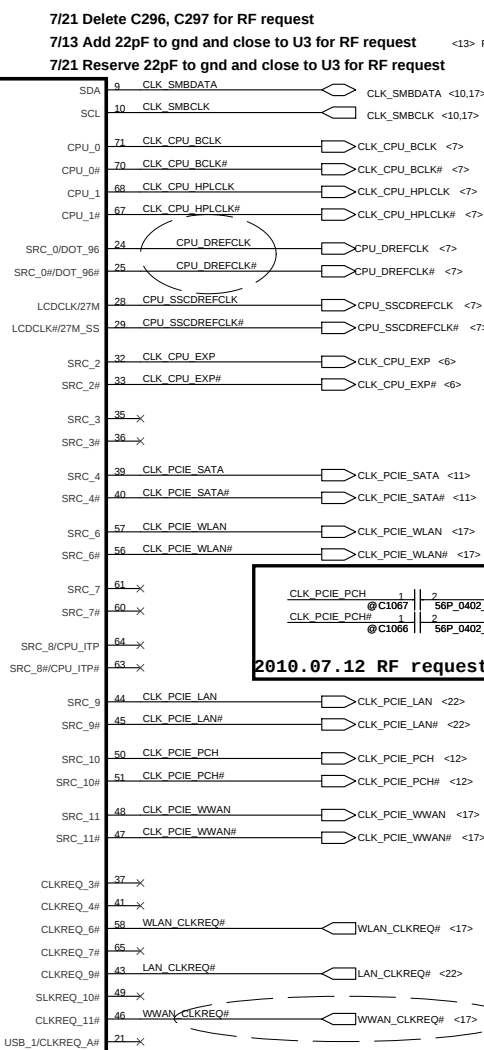
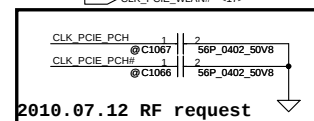
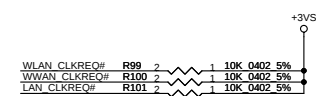
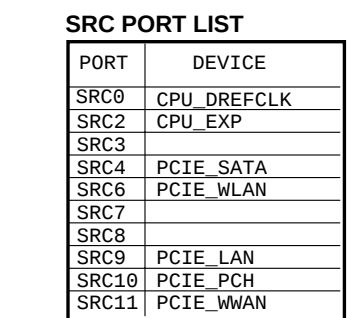
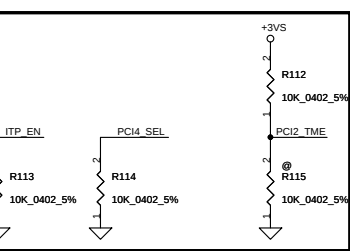
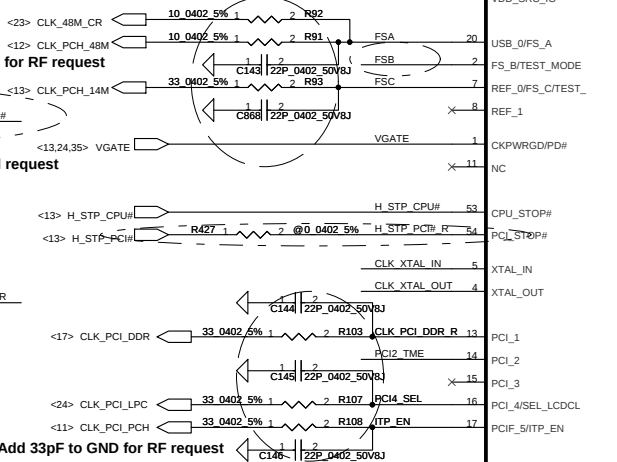
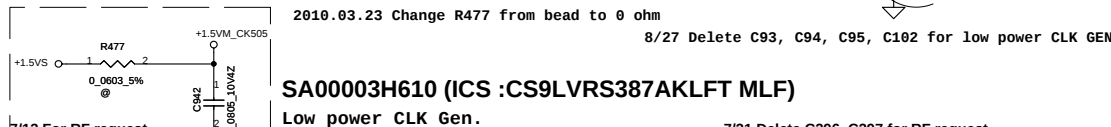
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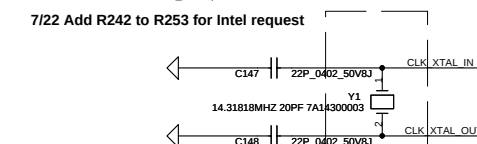


	Normal Power	Low Power
R477	@	Stuff
R478	Stuff	@
R479	Stuff	@
R480	@	Stuff
R483	@	Stuff



REQ PORT LIST

PORT	DEVICE
REQ_3#	
REQ_4#	
REQ_6#	PEIC_WLAN
REQ_7#	
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PEIC_WWAN
REQ_A#	

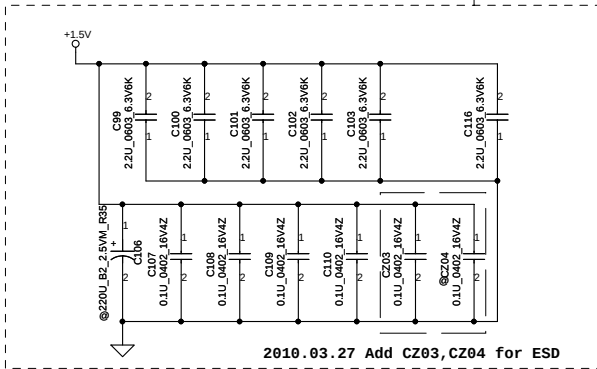


2010.03.09 Change Y1 to 5 x3.2 size

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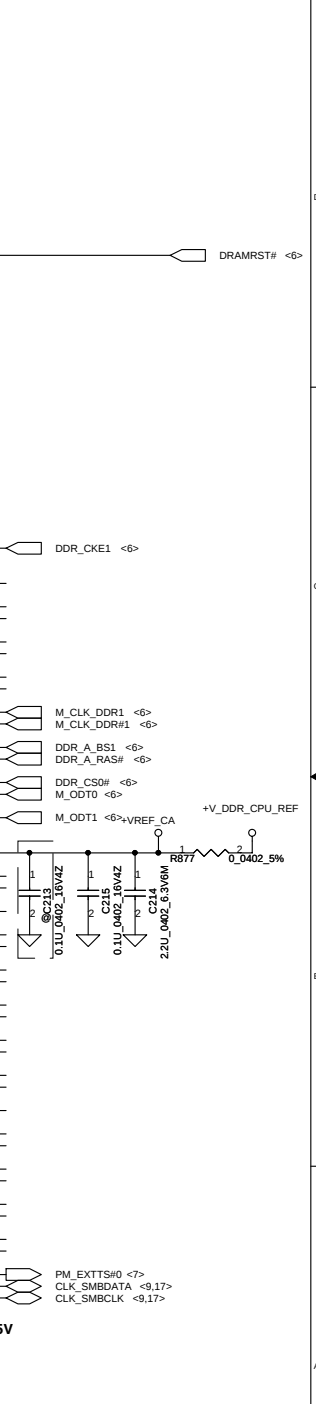
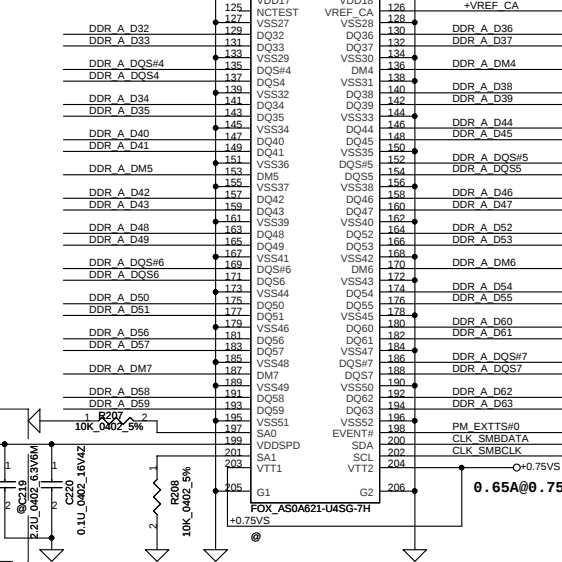
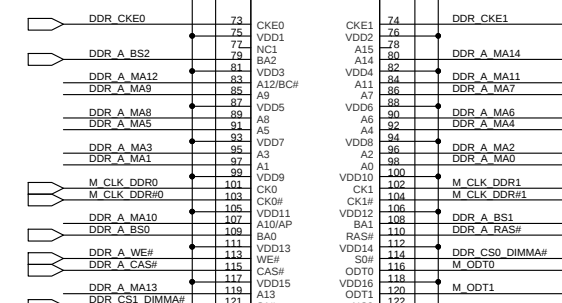
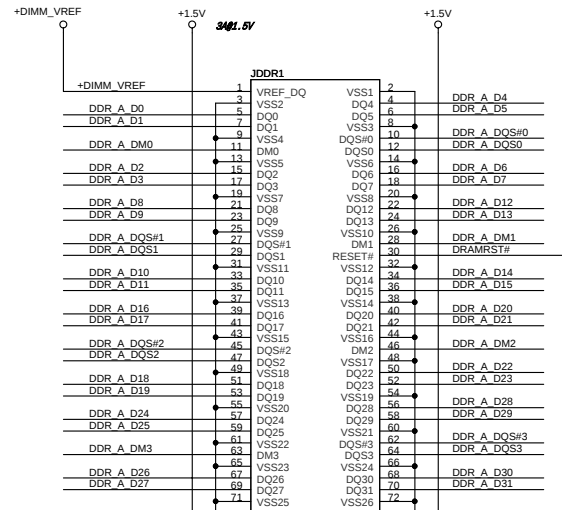
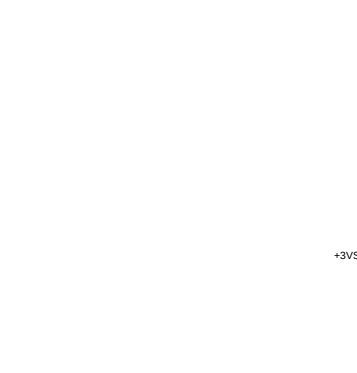
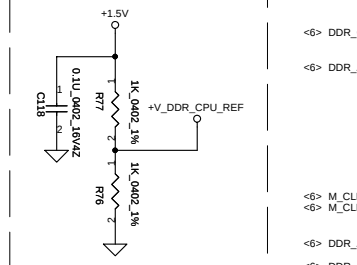
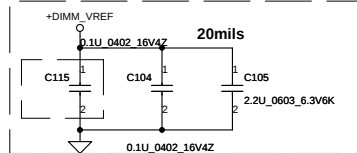
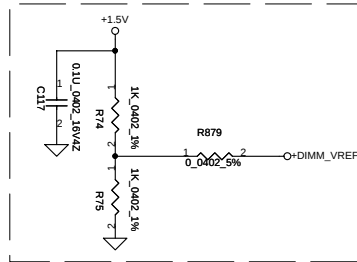
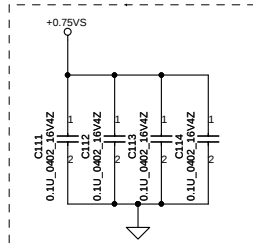
<6> DDR_A_DQS#[0..7]
 <6> DDR_A_D[0..63]
 <6> DDR_A_DM[0..7]
 <6> DDR_A_DQS[0..7]
 <6> DDR_A_MA[0..14]

Layout Note:
Place near JDDR1

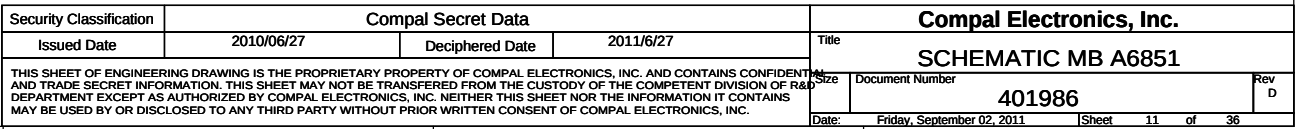


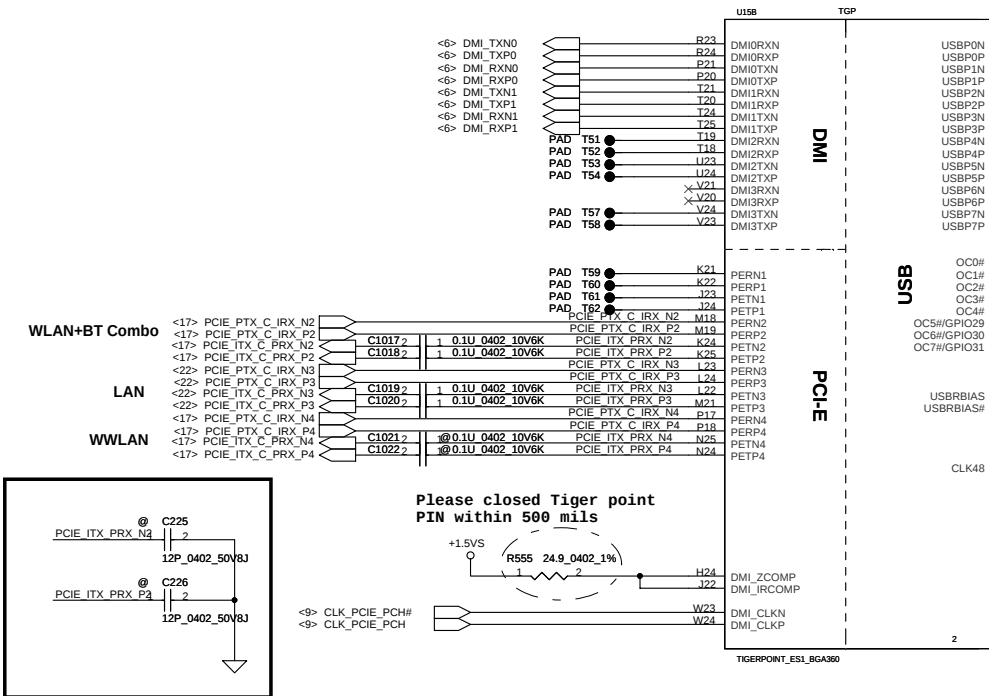
2010.03.27 Add CZ03,CZ04 for ESD

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.75VS



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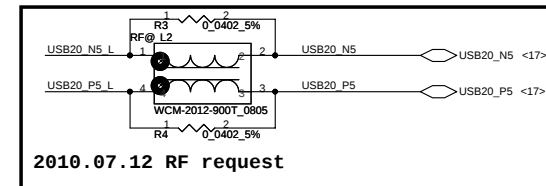
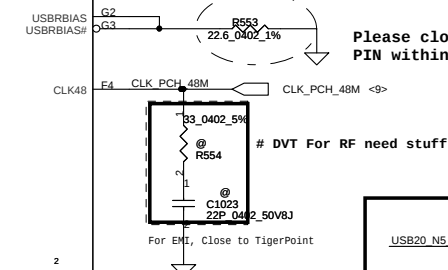
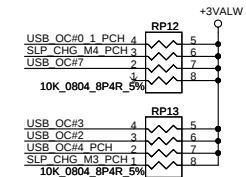
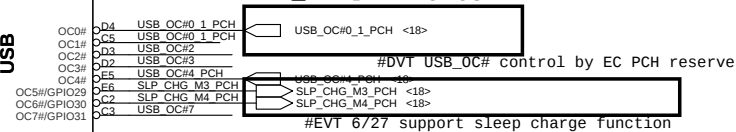


PVT C225, C226 add
12p to GND for RF

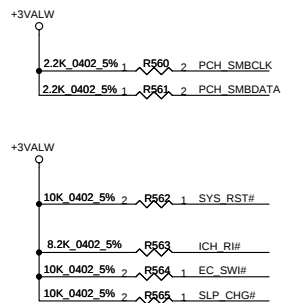
USB PORT LIST

PORT	#EVT	DEVICE
USB0		USB1(Left)
USB1		USB2(Left)
USB2		NC
USB3		Card-reader
USB4		USB3(Right)
USB5		WWAN
USB6		WLAN + BT
USB7		CMOS

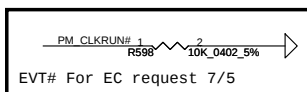
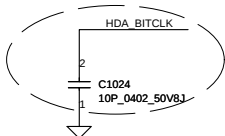
#6/27 EVT



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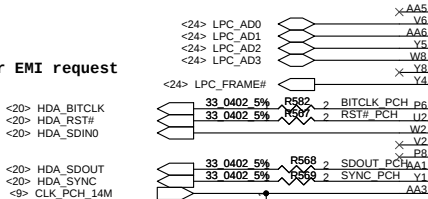
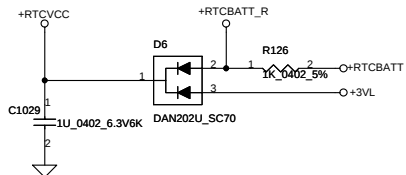
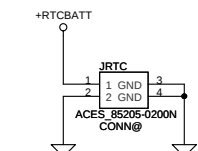
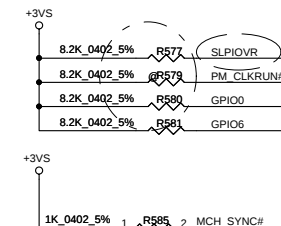
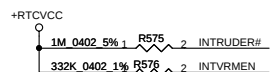
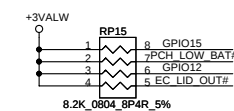
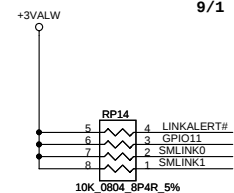


7/2 For EMI, Close to TigerPoint
9/1 C207 change to SE071100J80 for EMI request

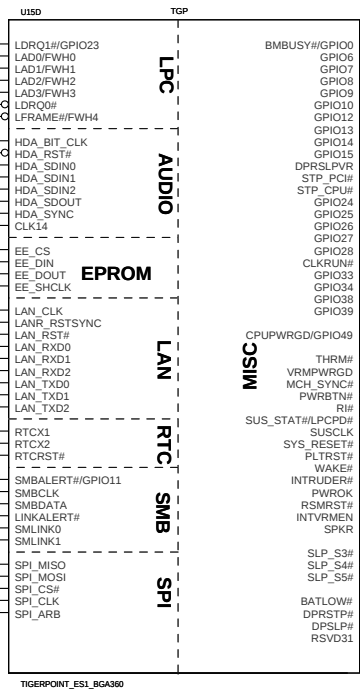
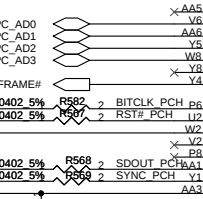


12/17 Add Pull high Resistor for GPIO14

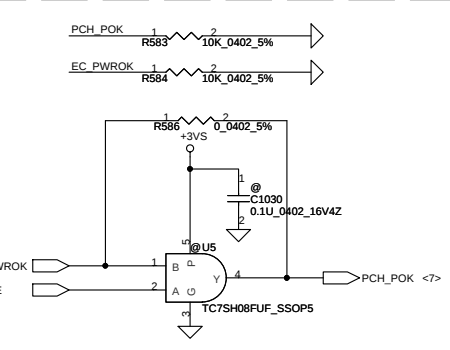
9/1 R125 change to SM010027780 for EMI request



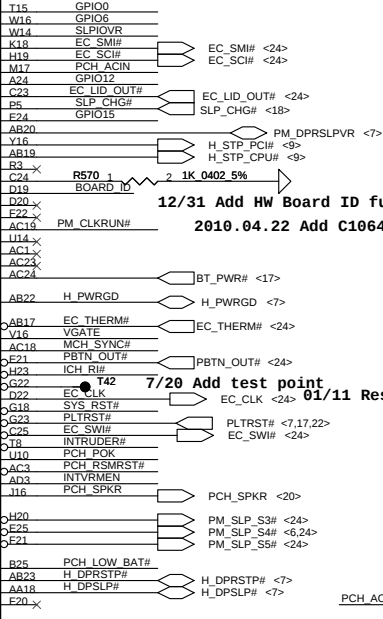
MP C1026 4.7P change to 10p for RF request



TIGERPOINT_ES1_BGA360

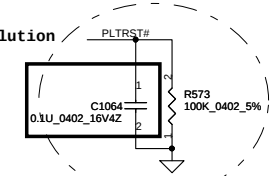


2010.03.22 Un-stuff U5 and C1030



12/31 Add HW Board ID function

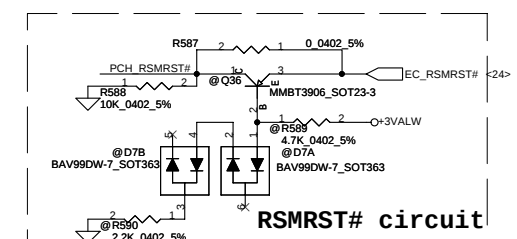
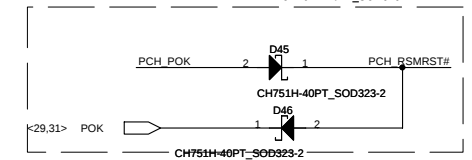
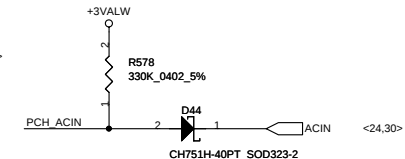
2010.04.22 Add C1064 for ESD solution



7/20 Add test point

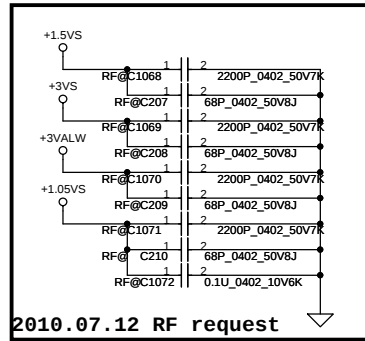
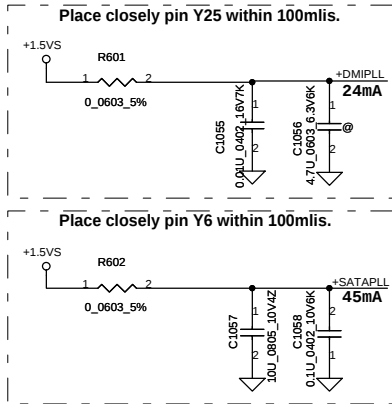
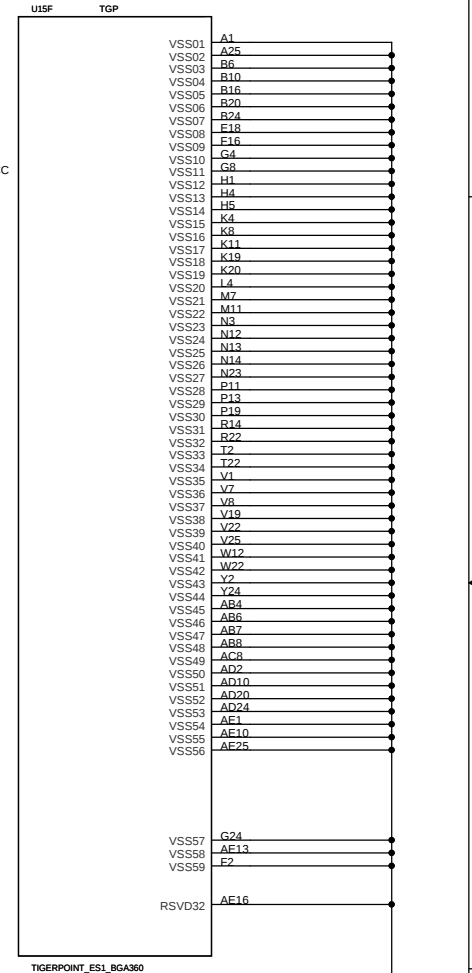
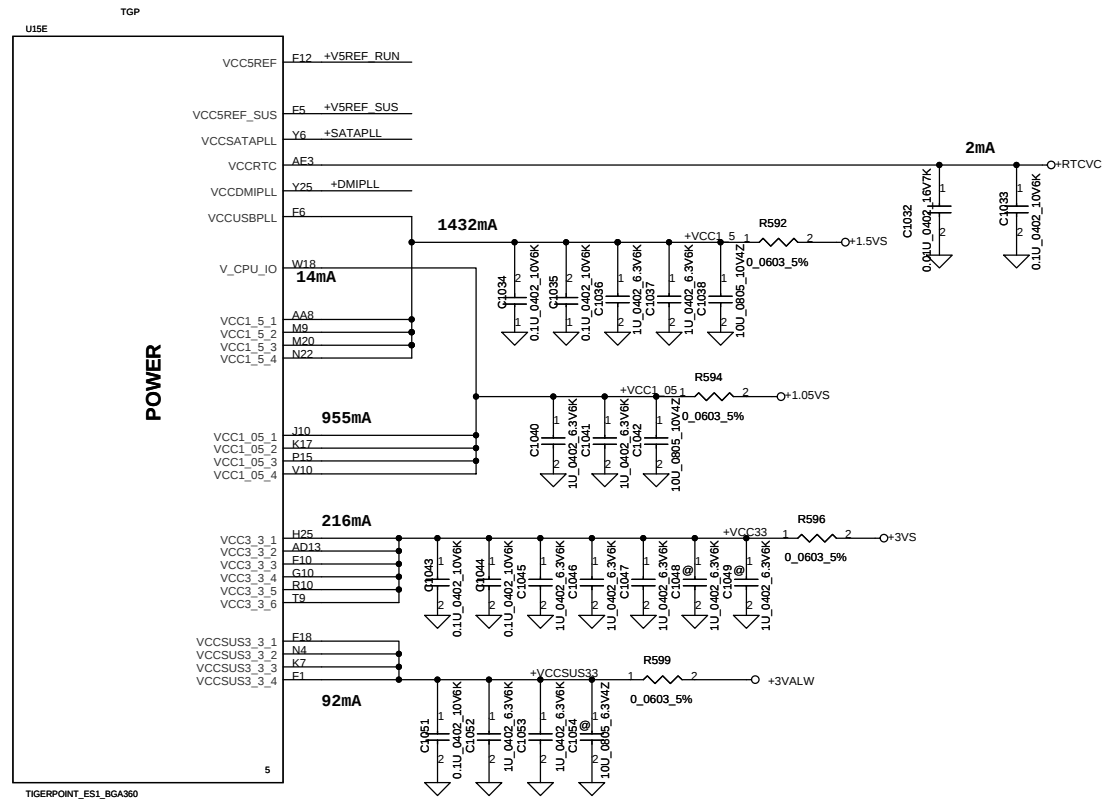
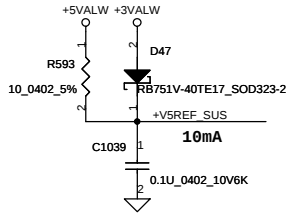
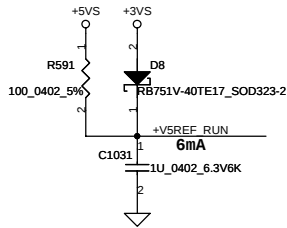
01/11 Reserve EC_CLK for KBC

8/24 Add R254 pull down for EC request



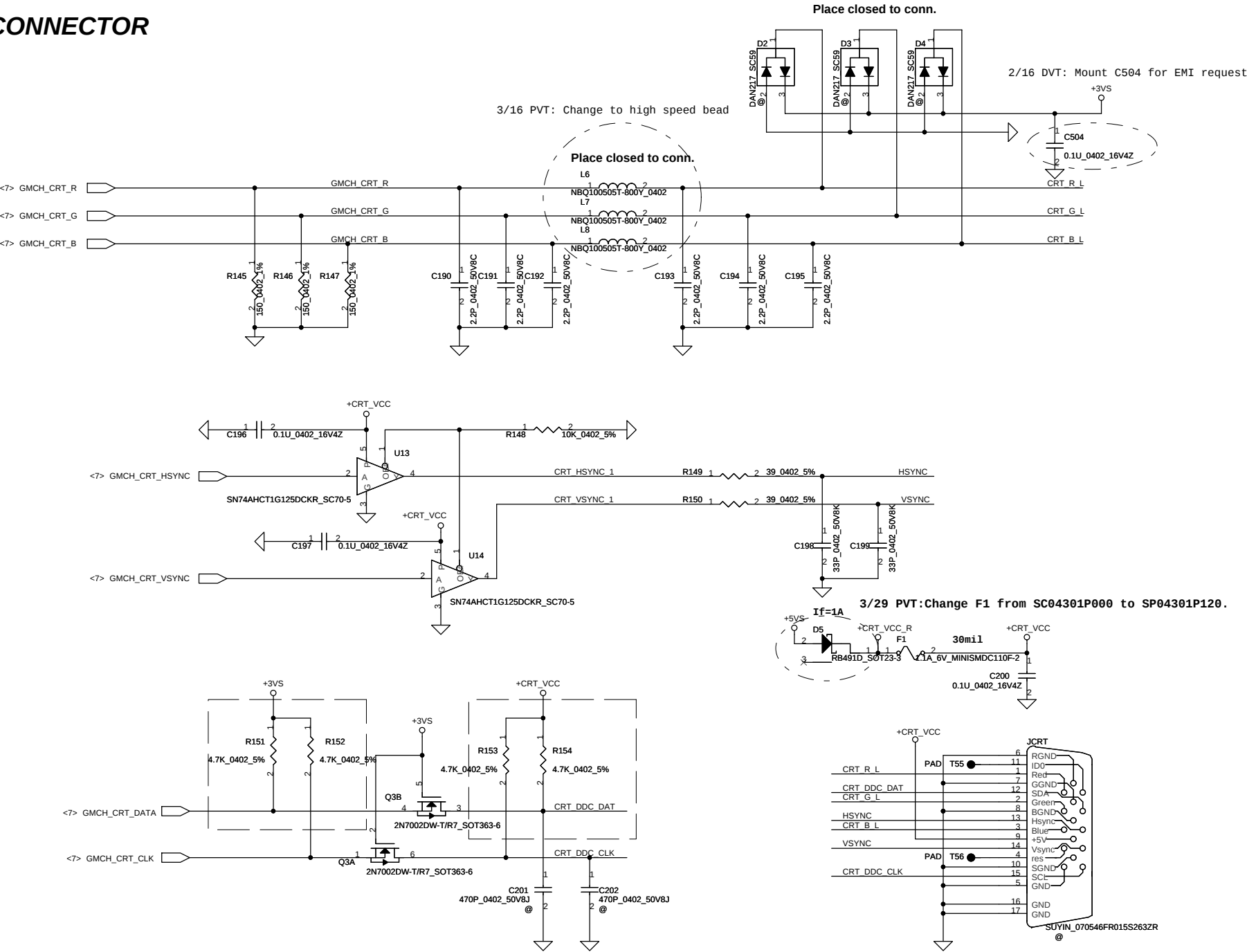
2010.03.22 Un-stuff RSMRST# circuit and use 0 ohm bypass

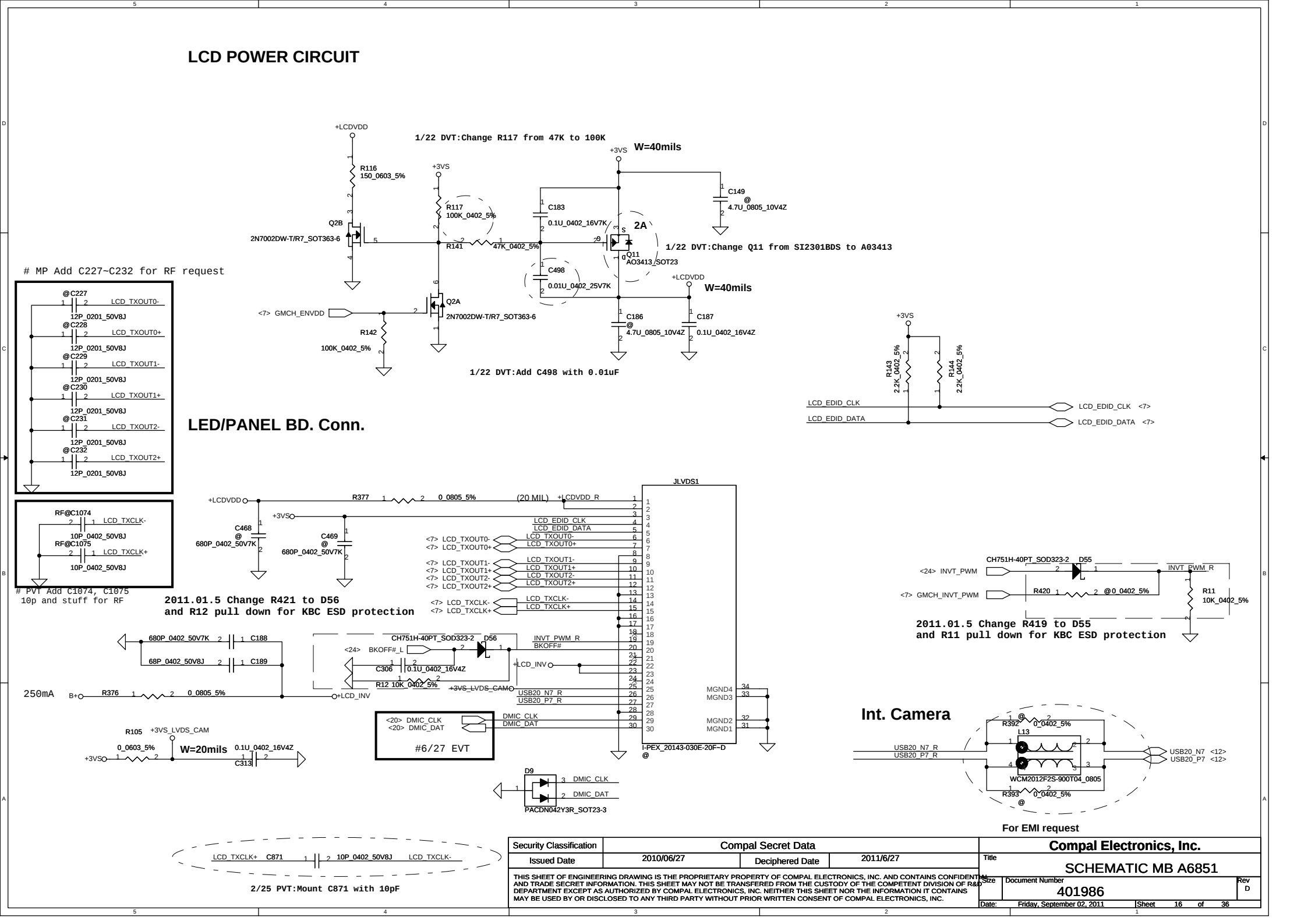
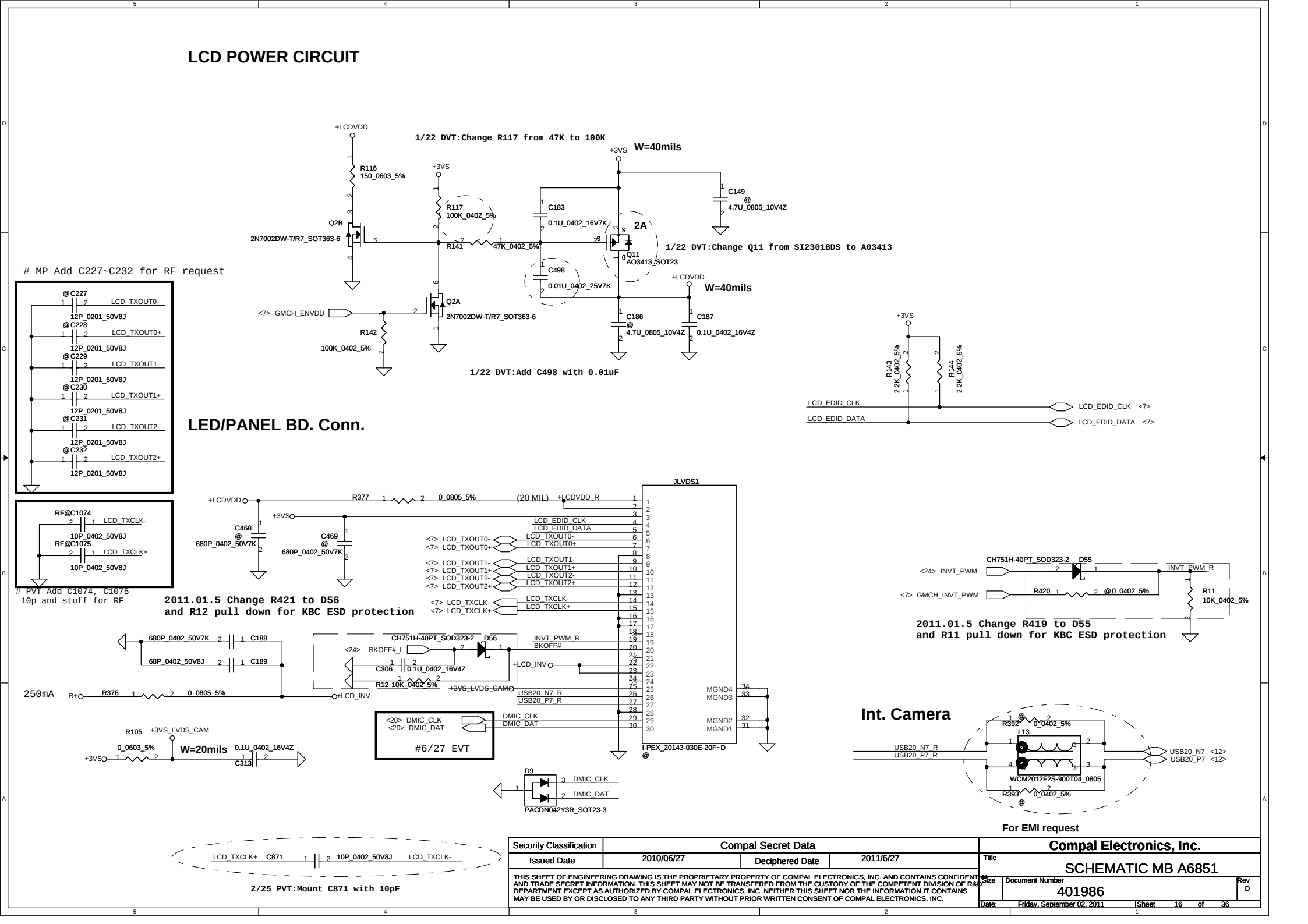
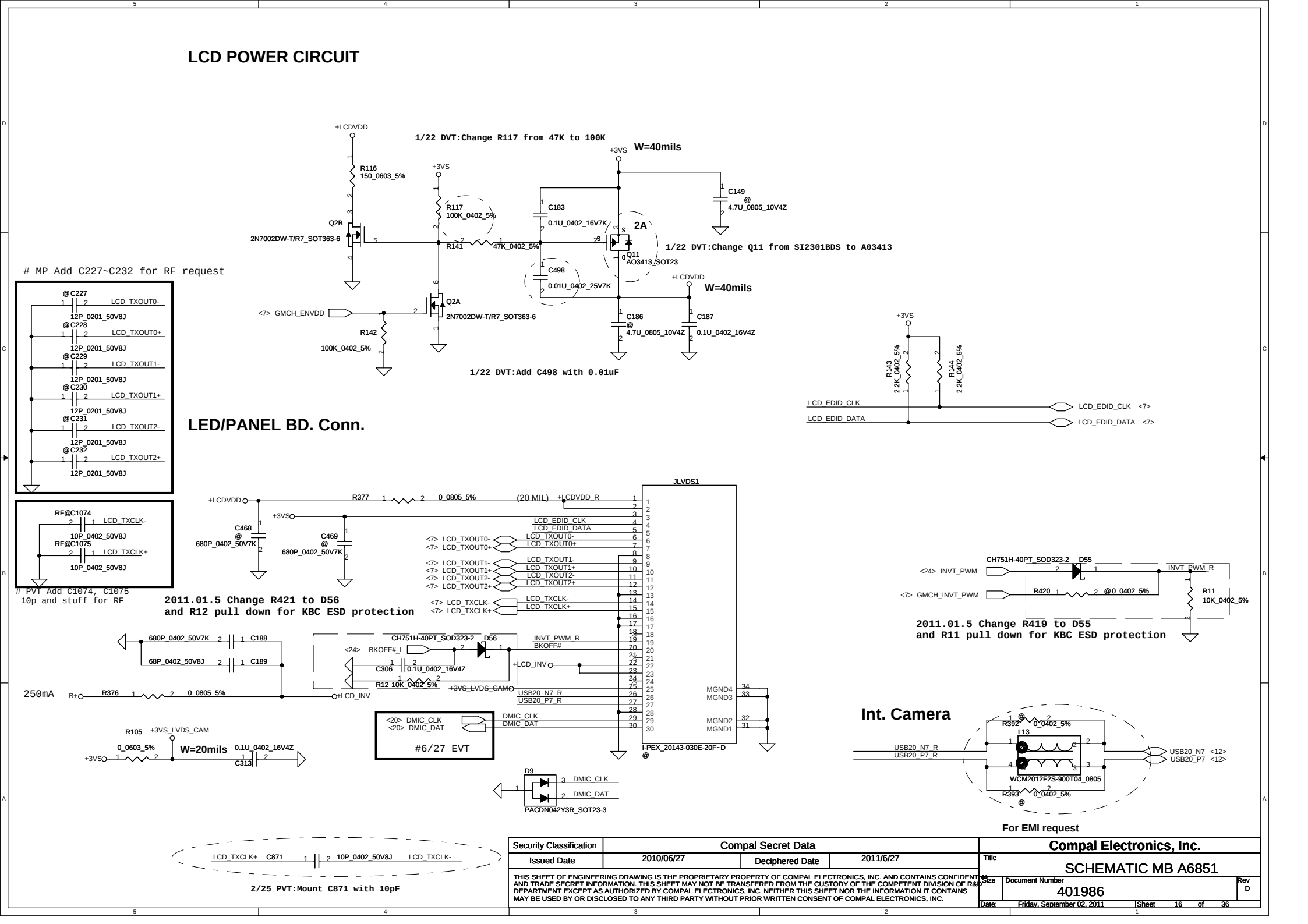
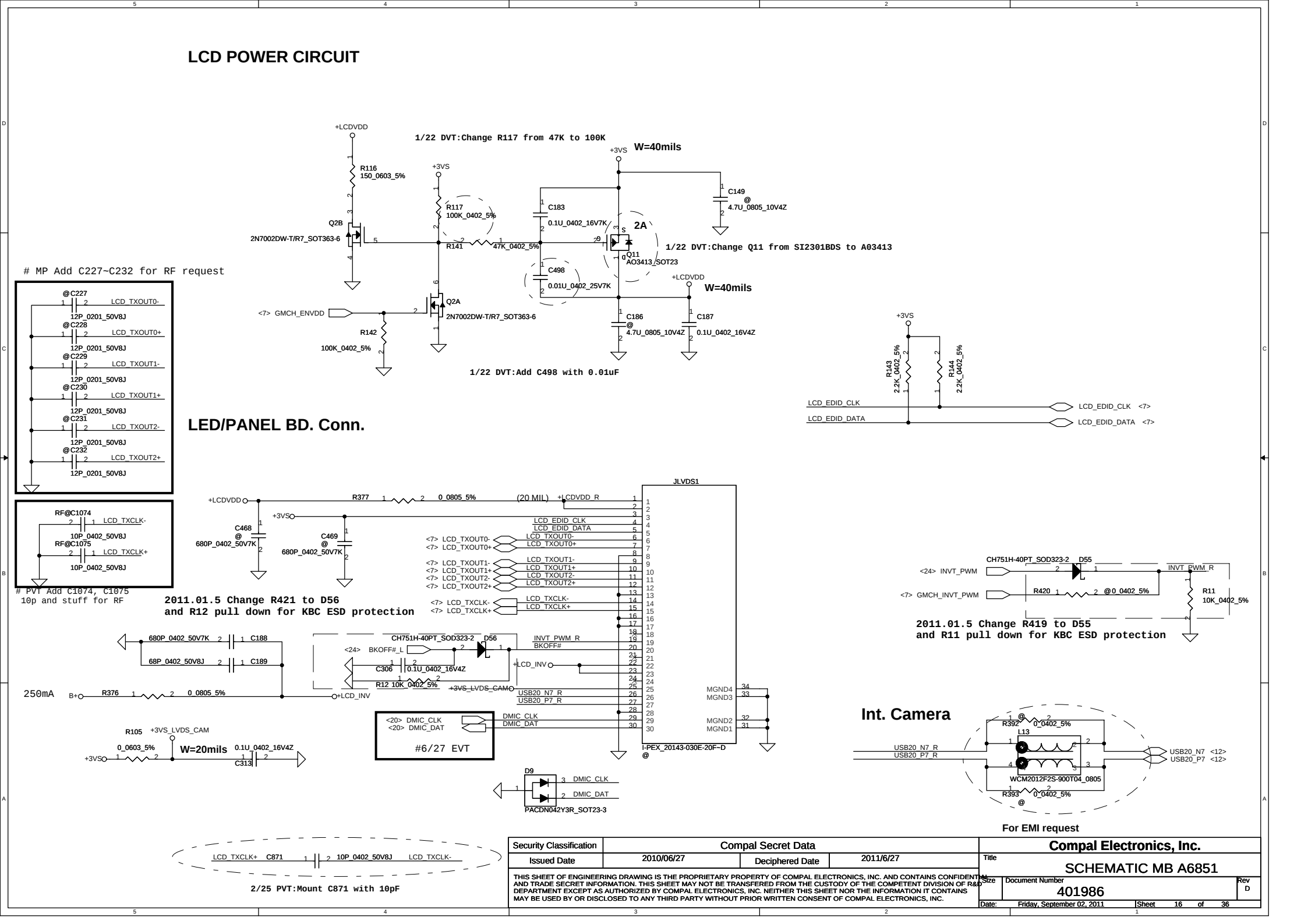
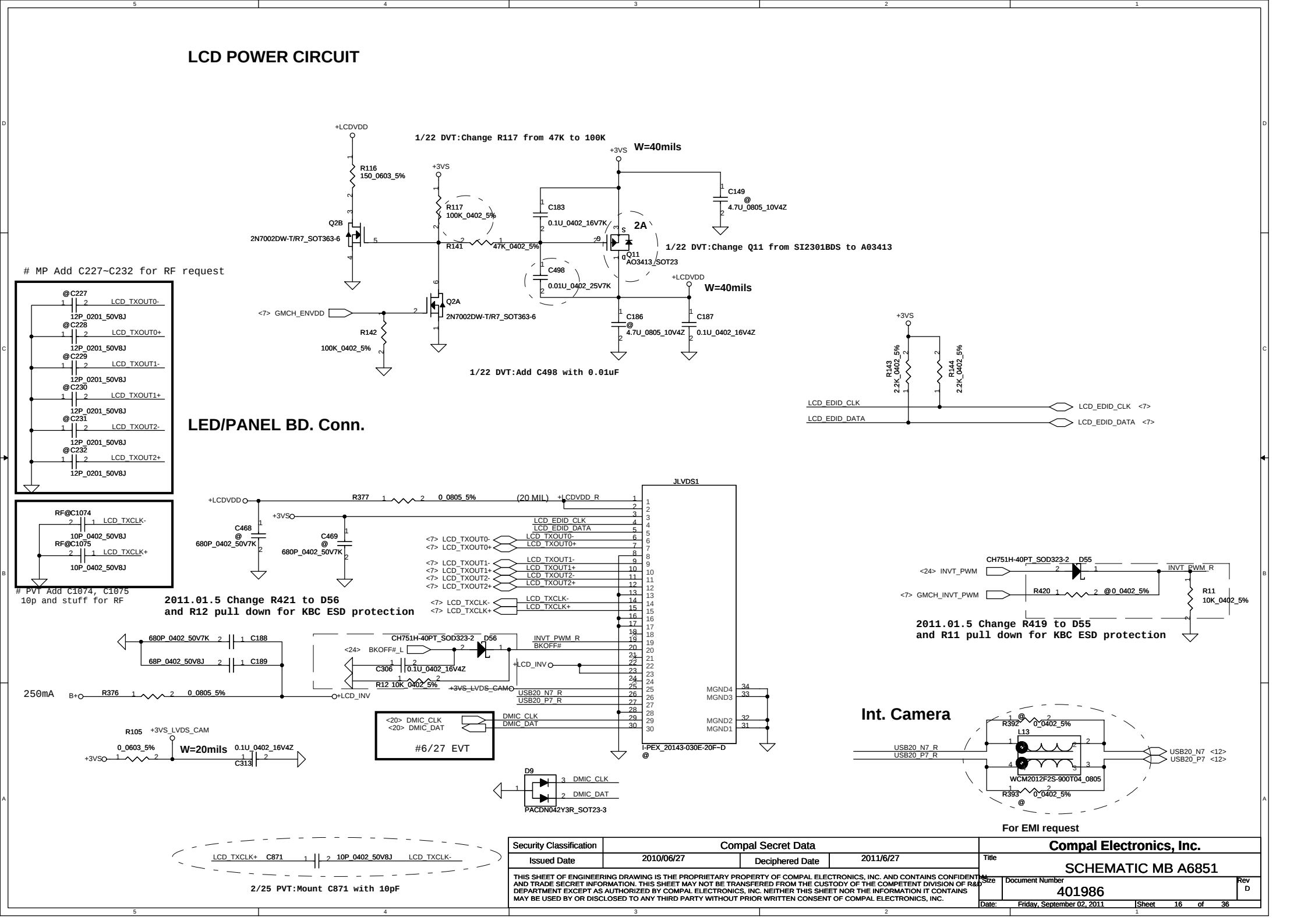
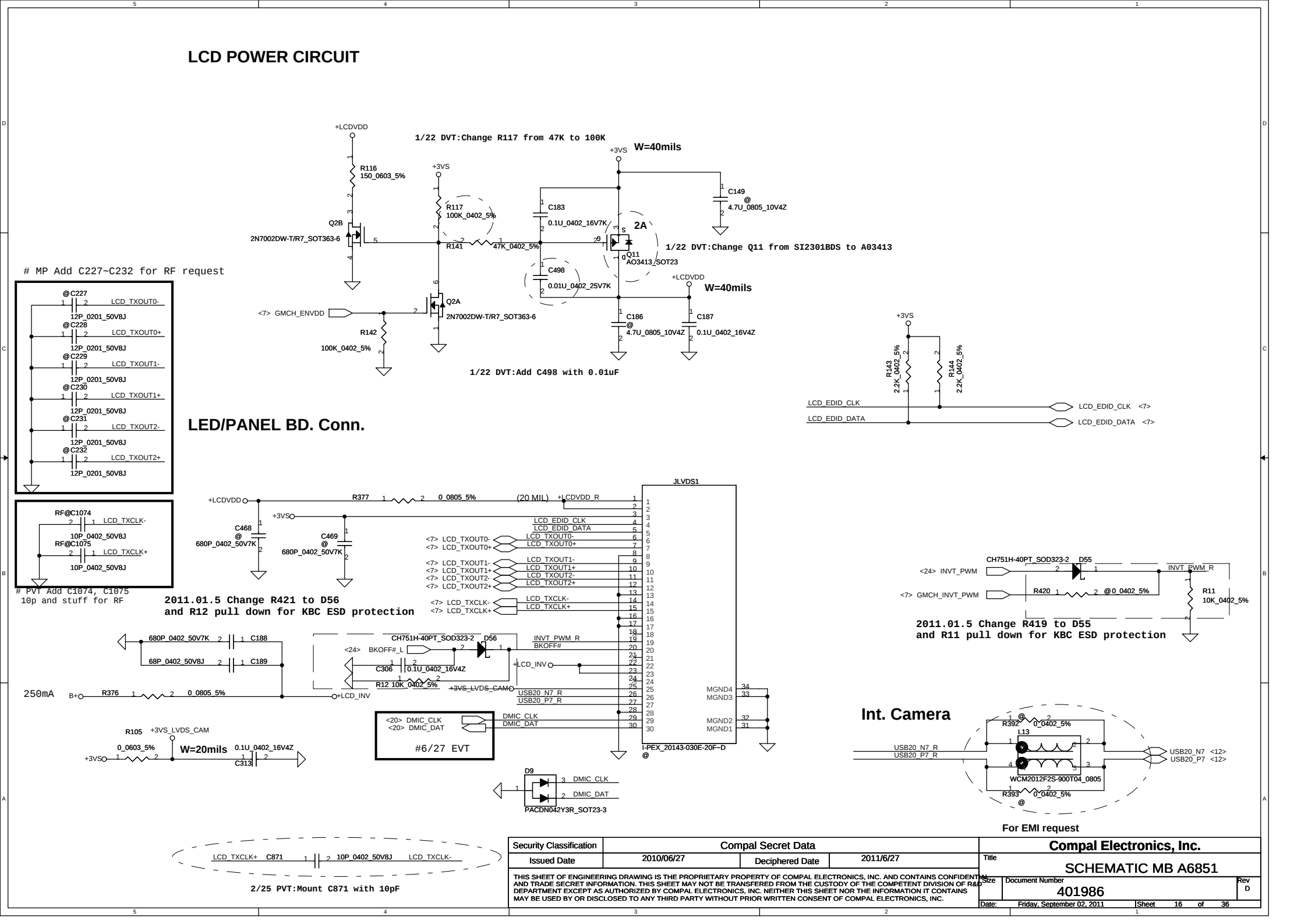
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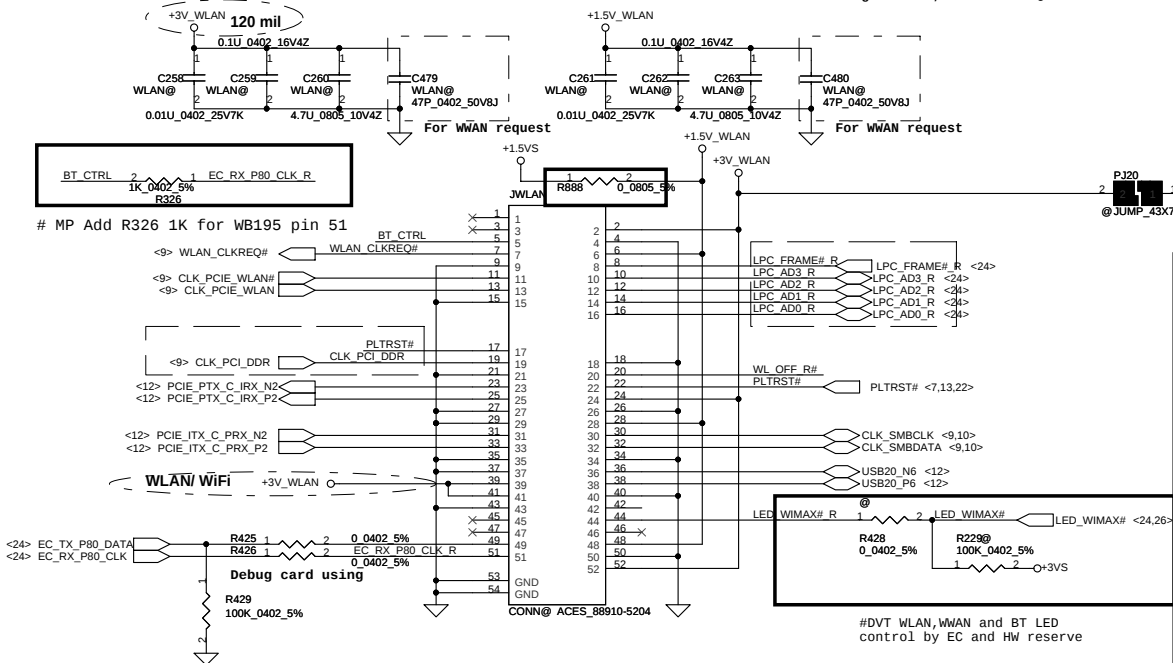
CRT CONNECTOR





Mini-Express Card for WLAN/WiMax

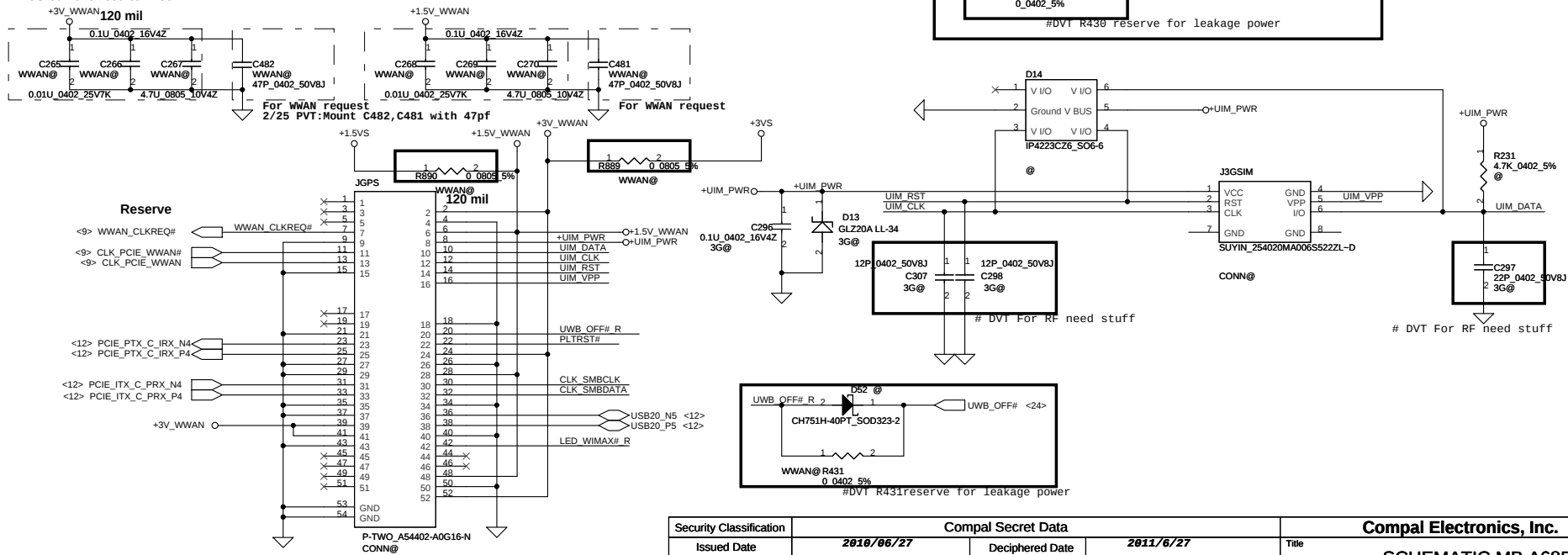
```
2/25 PVT:Mount C479,C480 with 47pf
3/16 PVT:Add BOM Config of C481,C482 to WLAN@
```



Mini-Express Card for 3G/GPS

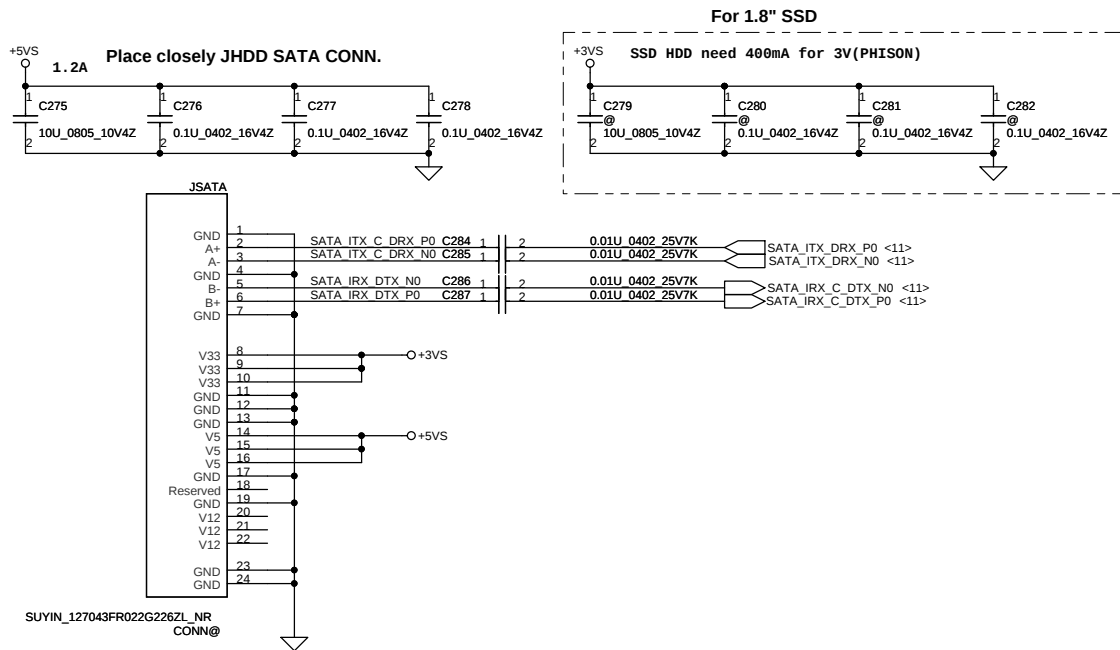
3G current need to 2750mA

3/16 PVT:Add BOM Config of C481,C482 to 3GGPS@

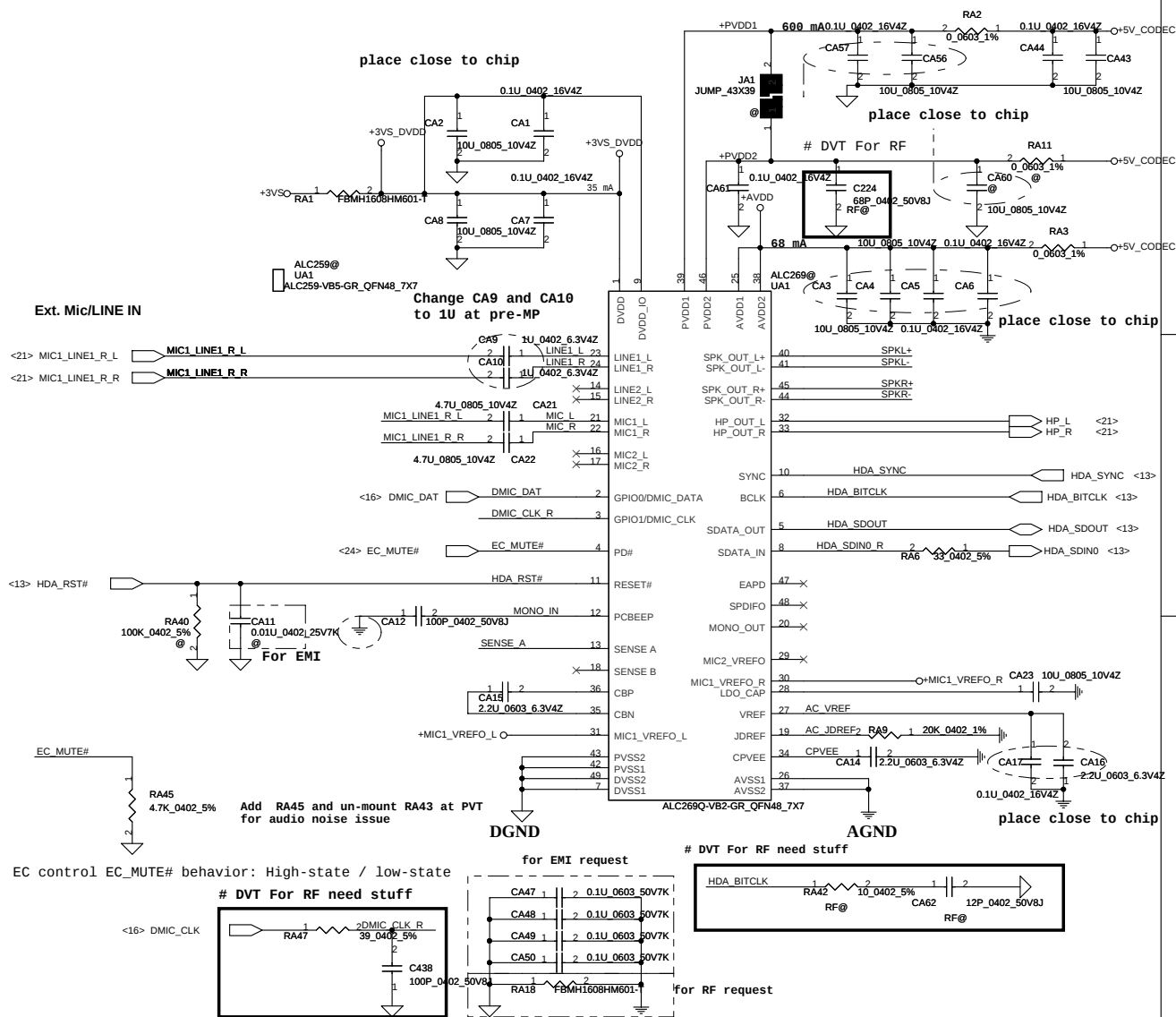


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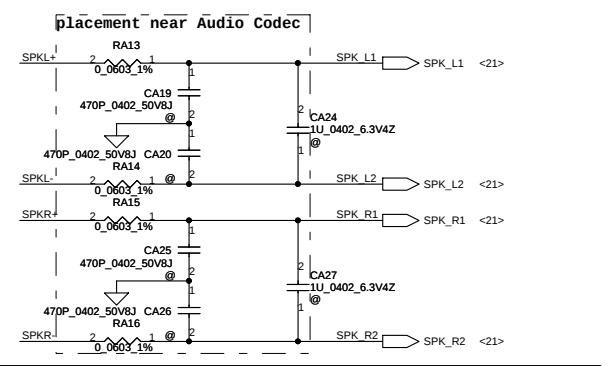
SATA Conn.



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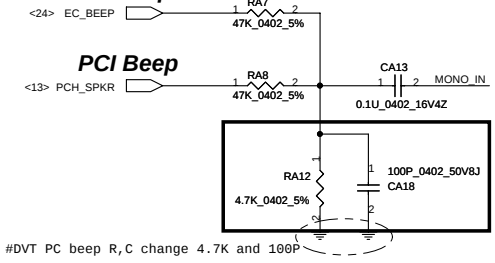


Speaker Connector

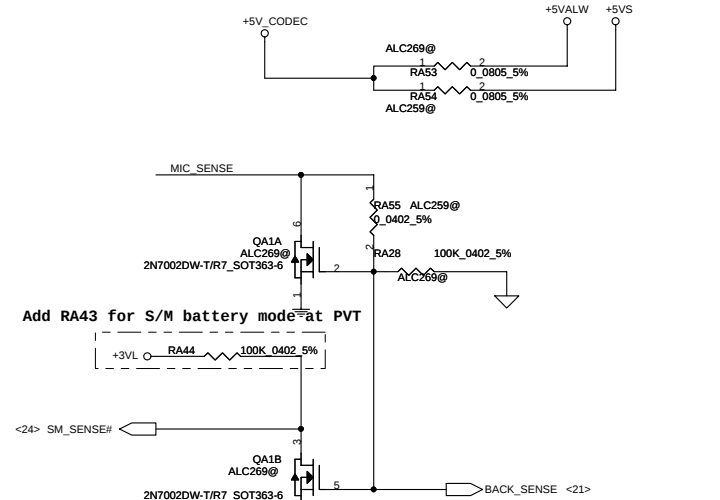


EC Beep

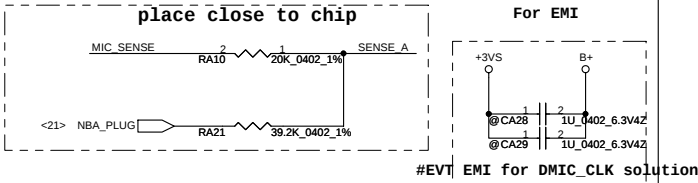
Beep sound



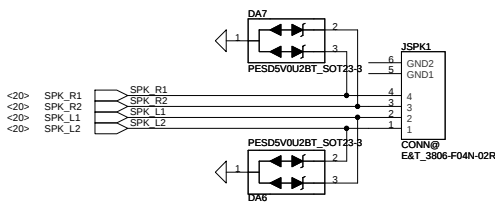
#DVT PC beep R,C change 4.7K and 100P



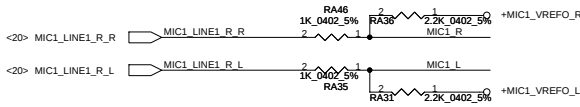
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	



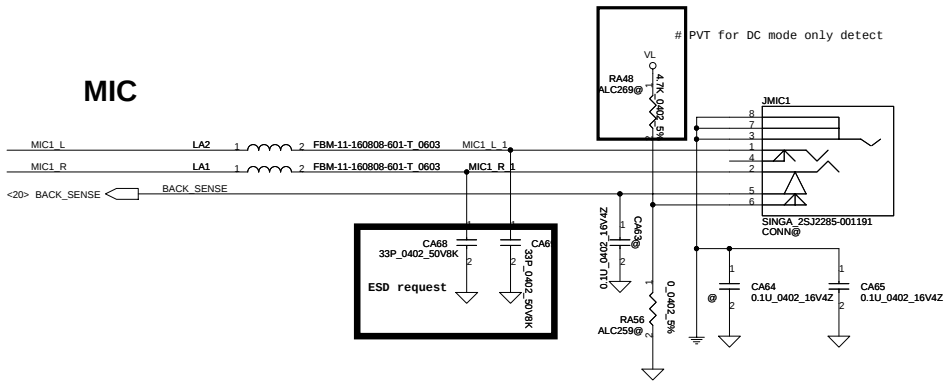
SPEAKER



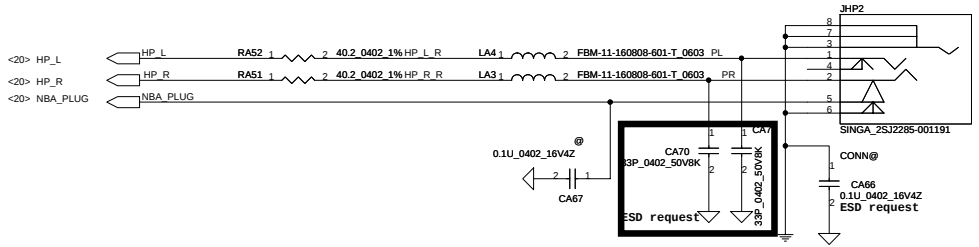
Ext.MIC/LINE IN JACK



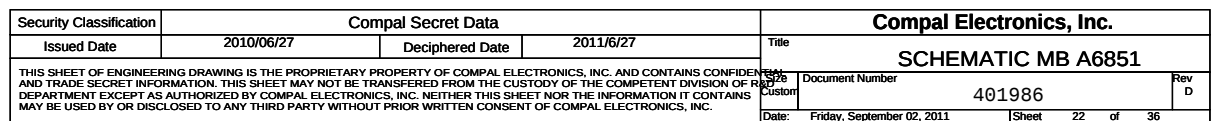
MIC



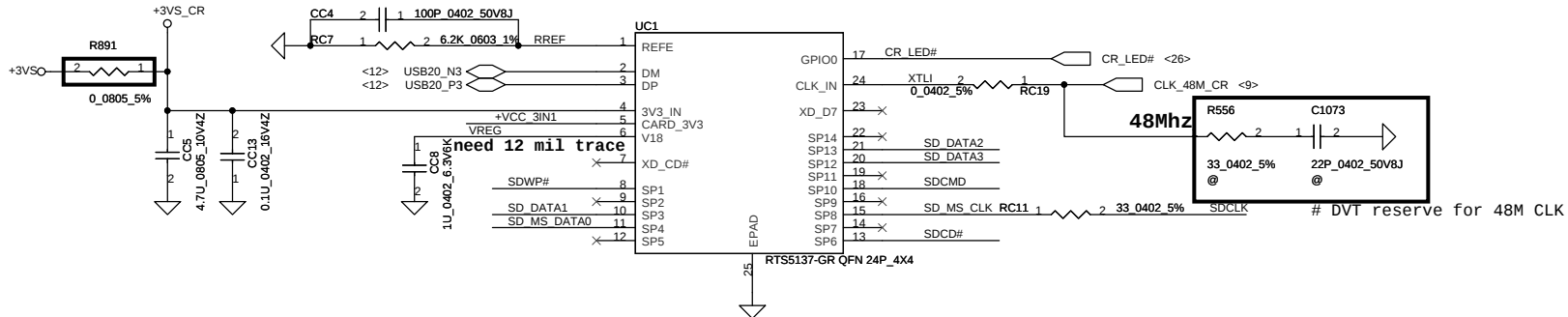
Head phone



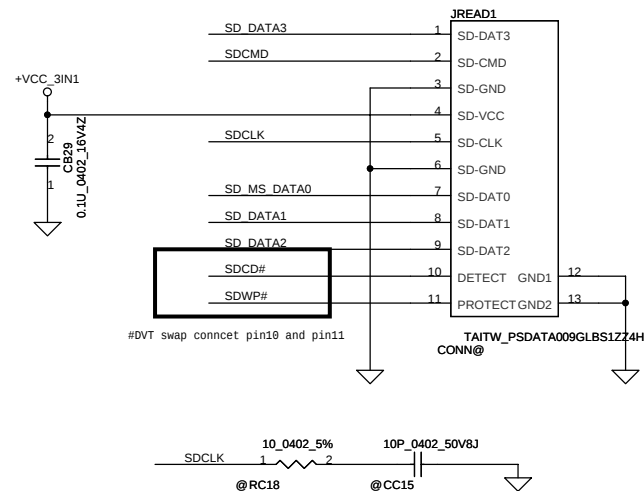
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	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CEF	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS
	XD_D7		

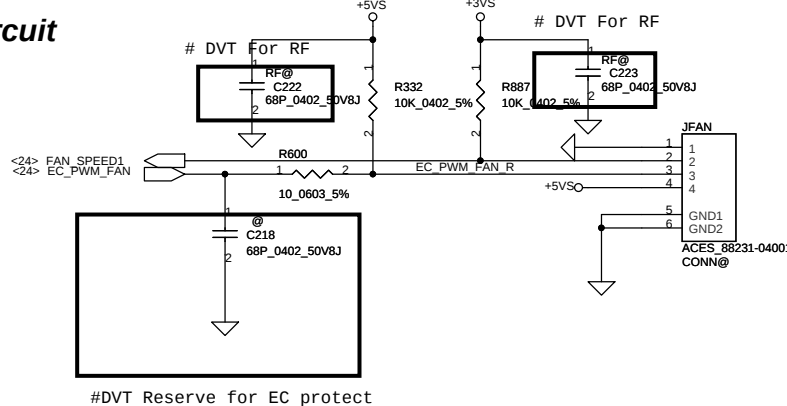


2 in 1 Card Reader

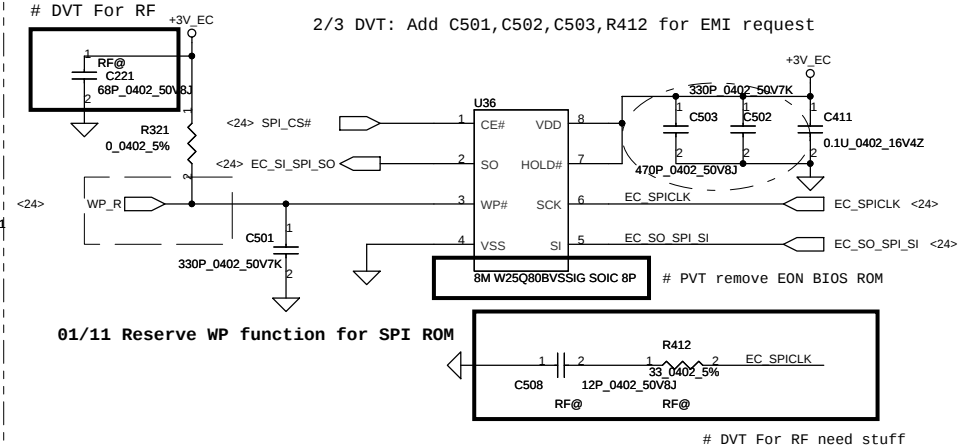


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FAN Control Circuit

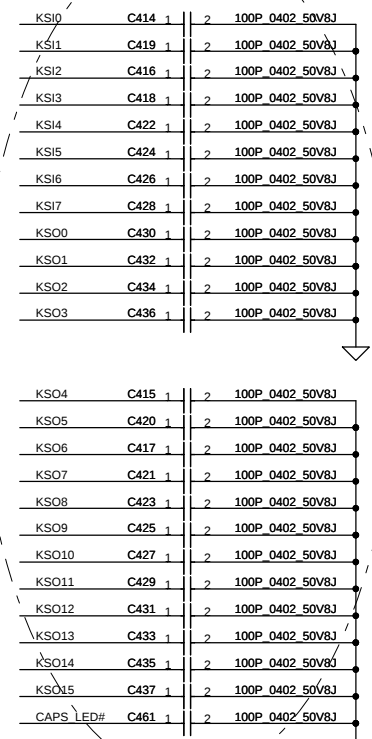
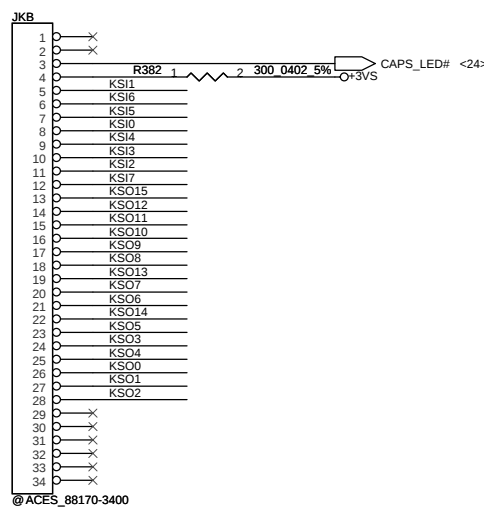


SPI Flash (8Mb*1)



LPC Debug Port

KEYBOARD
CONN.

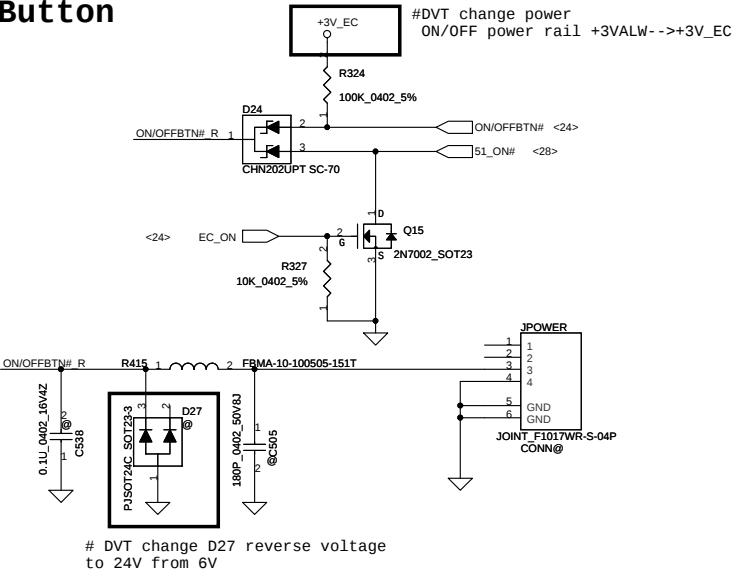


12/18 Follow KB Matrix the same to KSKAA

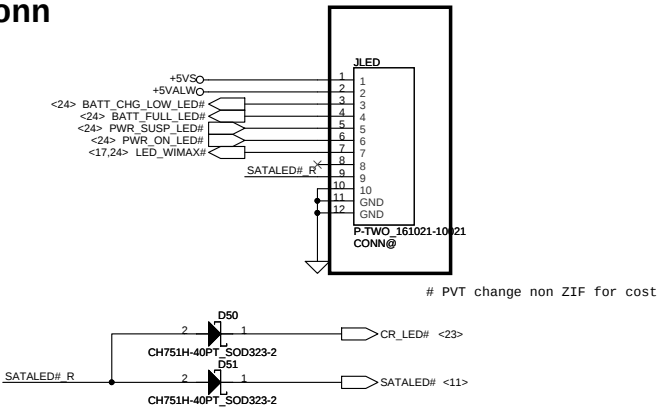
3/4 PVT:Mount C414-C437,C461 for EMI request

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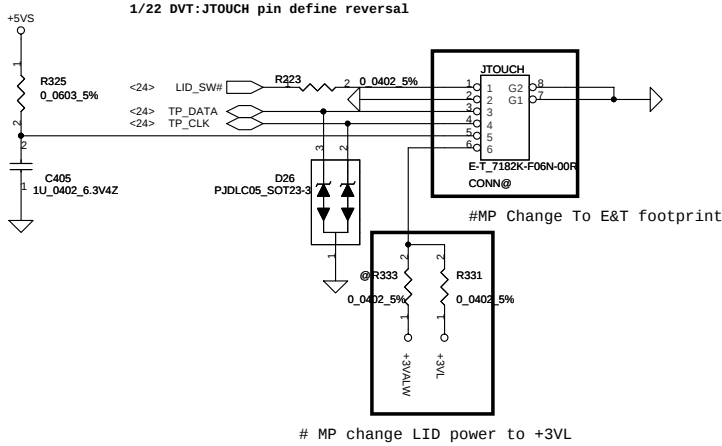
Power Button



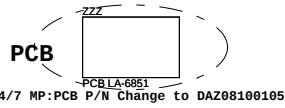
LED Conn



Touch/B Connector



ISPD



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2/25 PVT:Change C447 with 0.022uF

[illegible]

3/23 For EMI ESD solution

4.7U_0805_10V4Z

+1.5V

Si726DN-T1-E3_PAK1212-8
Q20

C1059
1U_0402_6.3V4Z

C1060
10U_0805_10V4Z

C1061

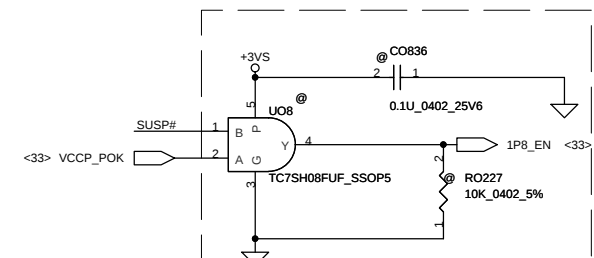
8/31 Change Q20 from SB000

R606
200K_0402_5%

C1062
0.01U_0402_25V7K

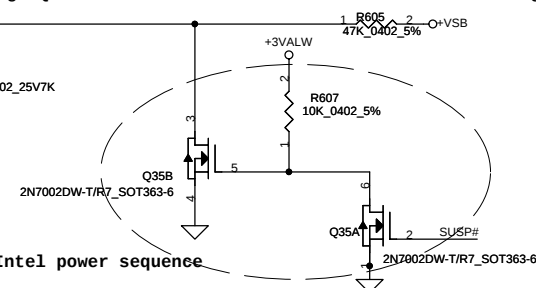
8/14 R237 for HW design

7/9 Add Q29, Q30, R228 for Intel power sequence

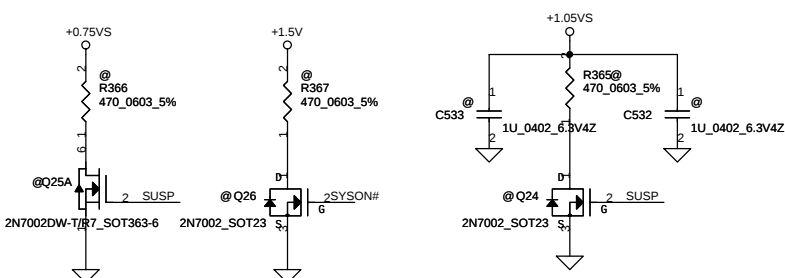


reserve U08 to control power down sequence between
1.8vs and 1.05vs, 01/08, 2010

8/31 Change Q20 from SB000002880 to SB00000DW00 for HW design

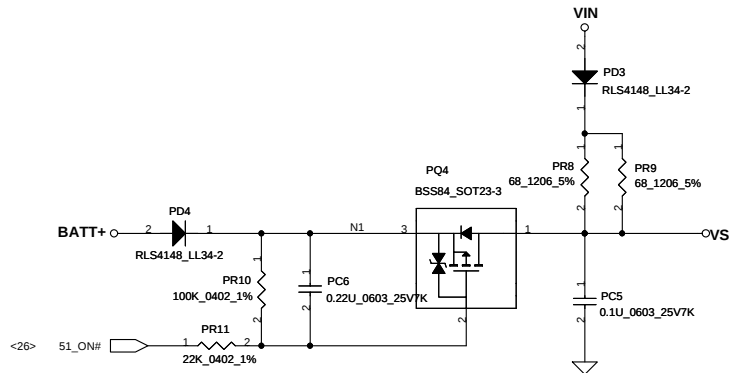
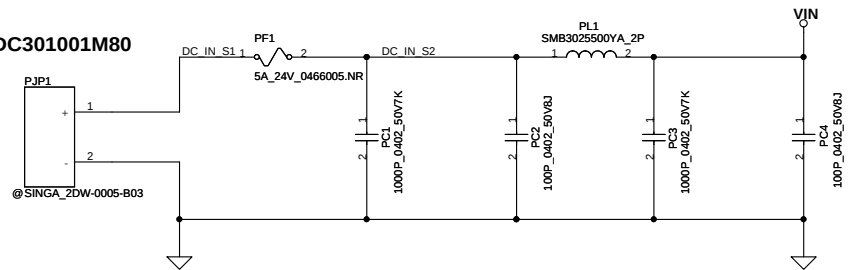


2/6 DVT: Reserve +1.5VS,+1.05VS,+0.75VS,+1.8VS discharge circuit



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DC301001M80



+3VALWP 2 **PJ330** 1 +3VALW
@JUMP_43X118
(6A, 240mils ,Via N0.= 10)
(OCP min=8A)

+1.5VP 2 **PJ150** 1 +1.5V
@JUMP_43X118
(4.1A, 180mils ,Via N0.= 12)
(OCP min=6.03A)

+5VALWP 2 **PJ350** 1 +5VALW
@JUMP_43X118
(5.5A, 220mils ,Via N0.= 10)
(OCP min=7.8A)

+1.05VSP 2 **PJ105** 1 +1.05VS
@JUMP_43X118
(3.5A, 140mils ,Via N0.=7)

+VSBP 2 **PJ5** 1 +VSB
@JUMP_43X39
(120mA, 40mils ,Via N0.= 1)

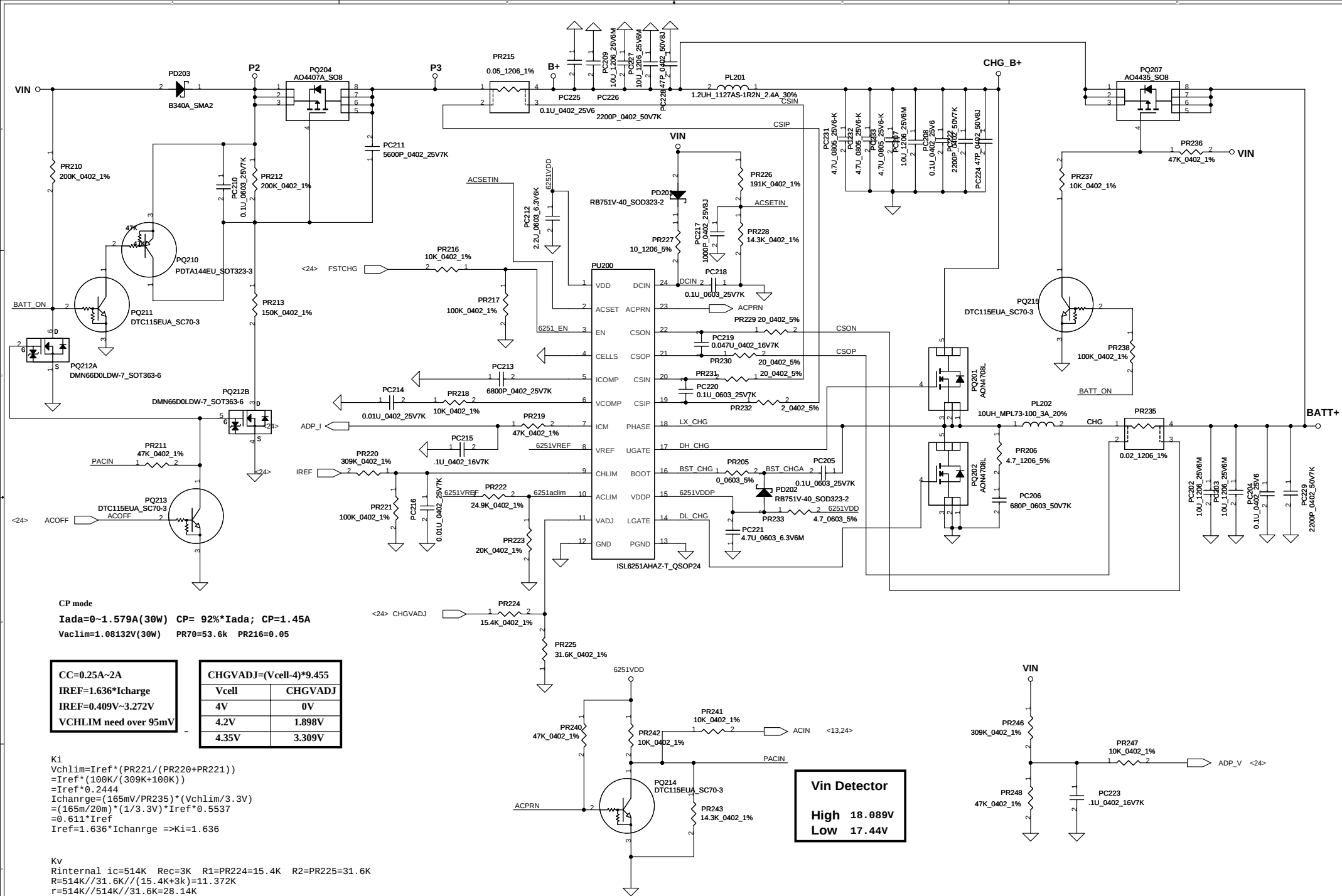
+1.8VSP 2 **PJ180** 1 +1.8VS
@JUMP_43X118
(3A, 120mils ,Via N0.= 1)

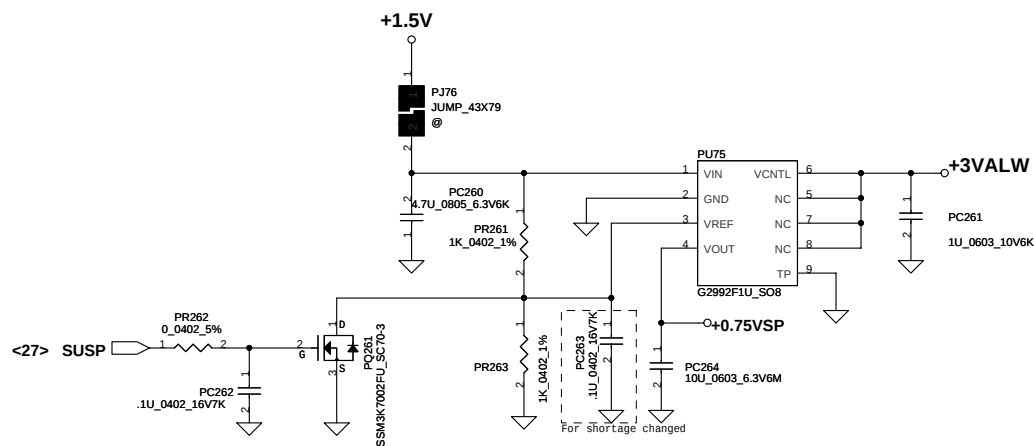
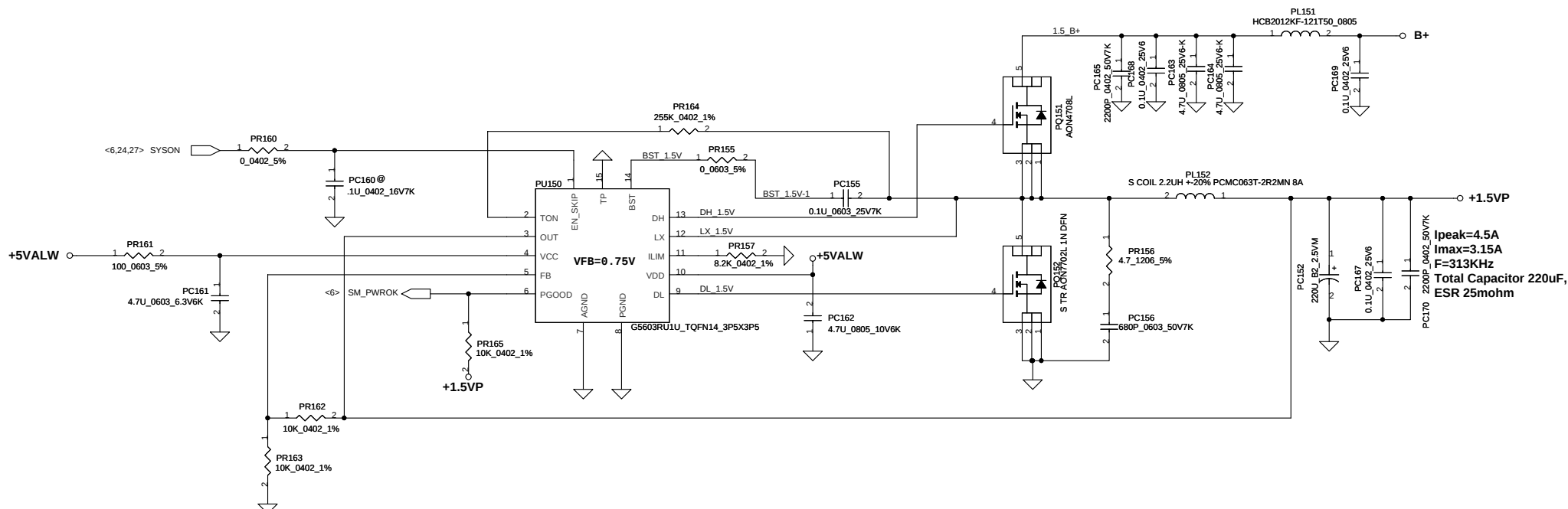
+0.75VSP 2 **PJ75** 1 +0.75VS
@JUMP_43X79
(1A, 40mils ,Via N0.= 3)

+0.89VSP 2 **PJ89** 1 +0.89VS
@JUMP_43X118
(2.6A, 120mils ,Via N0.=6)

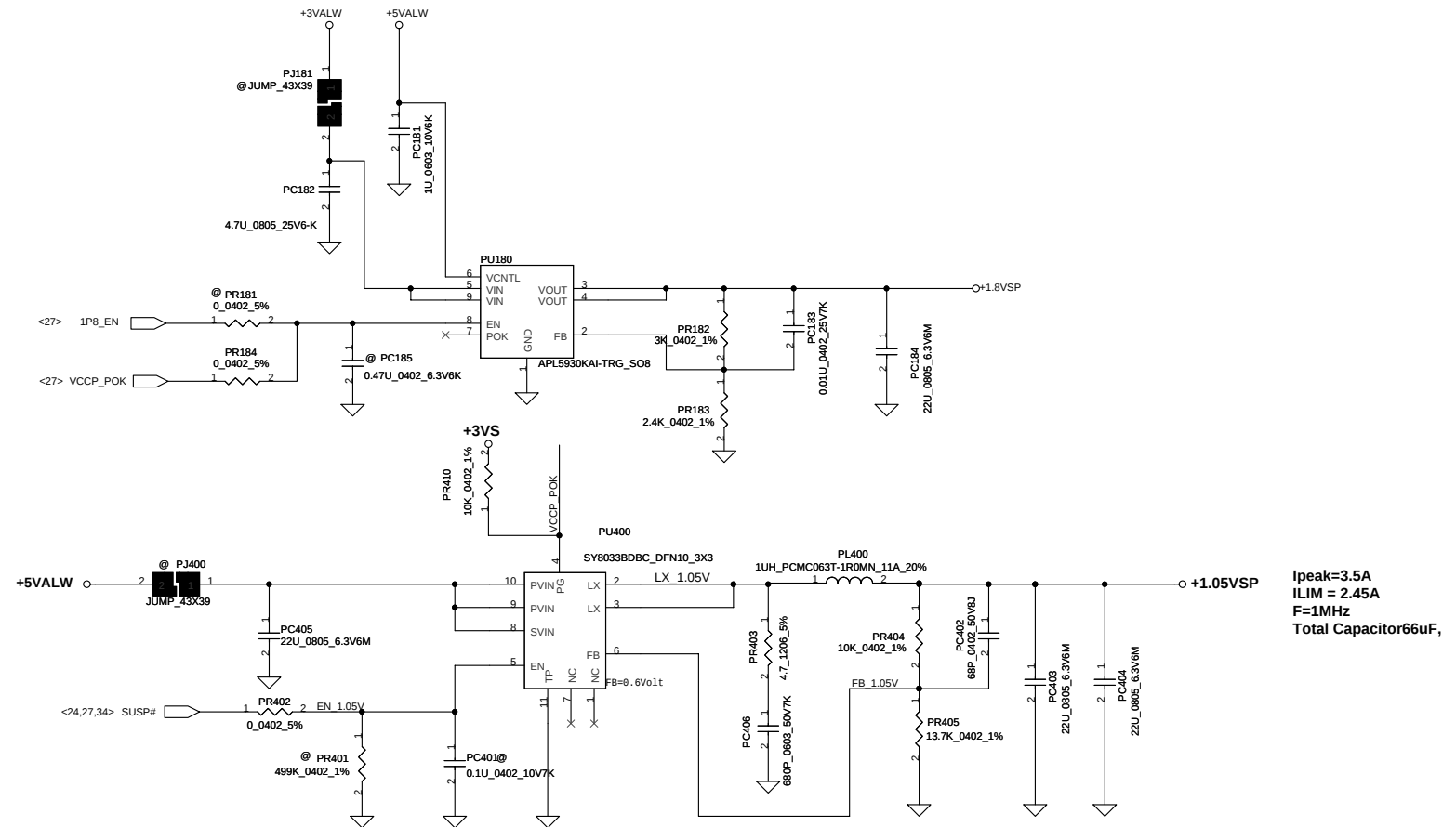
+3VLP 2 **PJ331** 1 +3VL
@JUMP_43X39
(100mA, 40mils ,Via N0.= 2)

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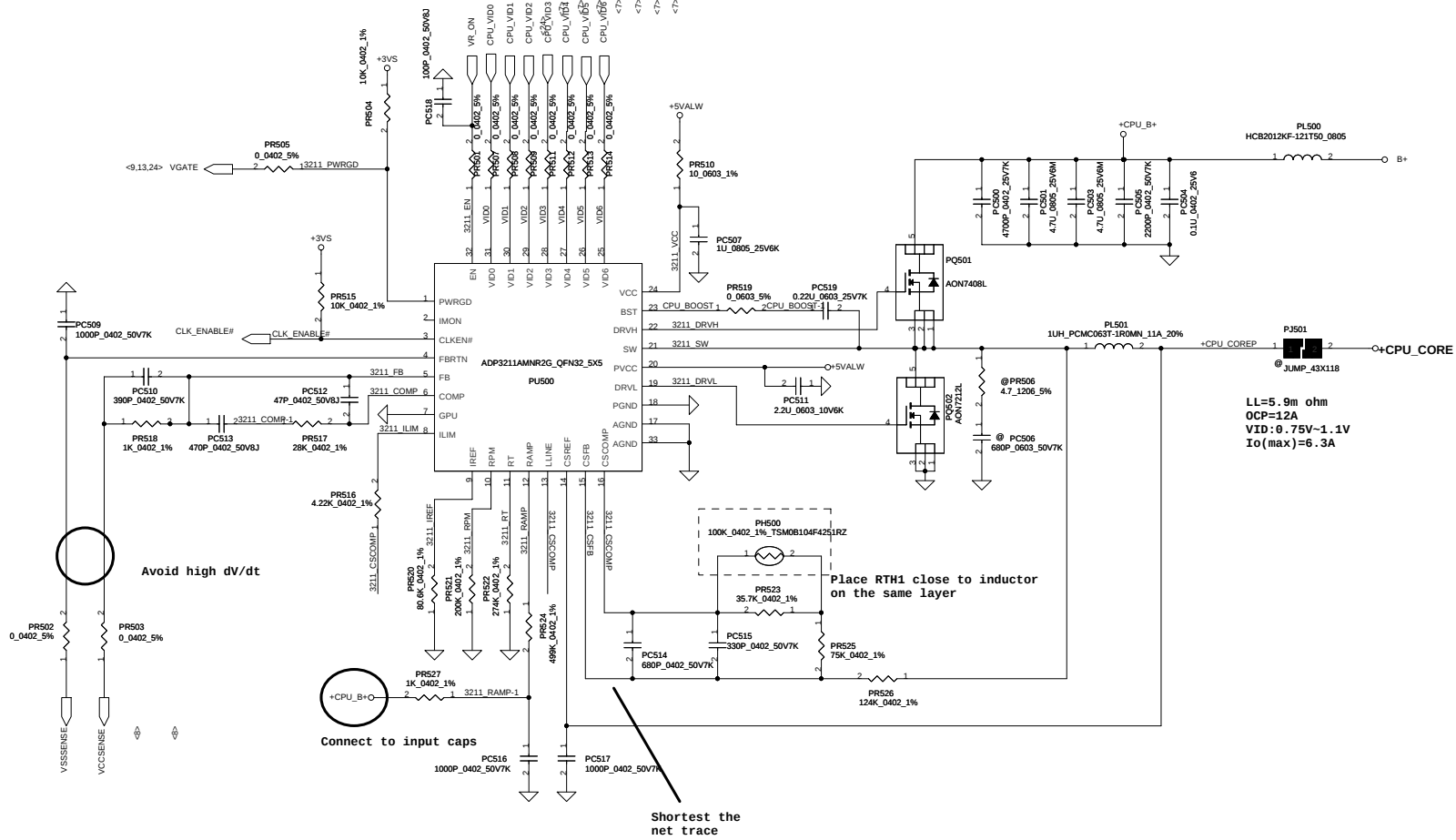




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NO DATE	PAGE	MODIFICATION LIST	PURPOSE
2010/8/23(DVT)	P32 +1.5VP/+0.75VSP	Change PU75 UP7711(SA00003XI00) -->G2992(SA00000VE80)	UPI had patent issue
2010/8/23(DVT)	P30 Charger	Change PU200 G5209(SA00003TK00) -->ISL6251(SA00001EP80)	G5209 had leakage issue
2010/8/23(DVT)	P31 +5VALWP/+3VALWP	Change PU330 UP6182(SA000043H00) -->TI51125A(SA000020C80)	UPI had patent issue
2010/8/23(DVT)	P30 Charger	add PR247(SD034100280) PC223(SE076104K80) PR246(SD034309380) PR248(SD034470280)	Support SA ECO unit
2010/8/23(DVT)	P35 CPU_CORE	Change PR526 174K (SD034174380) -->124K(SD034124380)	debug CPU load issue
2010/8/23(DVT)	All snuber	Change PC273,PC274,PC275,PC403,PC404,PC405 22u(SE000008L80) -->PC273,PC274,PC275,PC403,PC404,PC405 22u(SE000000I10)	Chose the same material s
2010/8/23(DVT)	P30 Charger	Install PC222 PC224 0.1u (SE00000G880)	EMI commond
2010/8/23(DVT)	P30 Charger	Install PC227,PC209,PC207,PC208,PC204 10u (SE142106M80)	EMI commond
2010/8/23(DVT)	P35 CPU_CORE	Change PL500(SM01000BY00)-->(SM01000C000)	Chose the same material s
2010/8/23(DVT)	P31 +5VALWP/+3VALWP	Install PC371,PC369 0.1u (SE00000G880)	RF commond
2010/8/23(DVT)	P31 +5VALWP/+3VALWP	Install PC367 2200P(SE074222K80)	RF commond
2010/8/23(DVT)	P32 +1.5VP	Install PC165 2200P(SE074222K80)	RF commond
2010/8/23(DVT)	P32 +1.5VP	Install PC169,PC168,PC167 0.1u(SE00000G880)	RF commond
2010/8/23(DVT)	P35 CPU_CORE	add PC518 (SE071101J80)	debug CPU VR-ON issue
2010/9/21(PVT)	P30 Charger	Install PC225 PC208PC204 (0.1u) , PC226 PC222 PC229(2200P) Add PC208 add PC228 PC224 (47P),install snubber PR206,PC206	RF commond
2010/9/21(PVT)	P31 +5VALWP/+3VALWP	Add PC372 PC374(0.1u) , PC375(47P) PC371 (2200P)	RF commond
2010/9/21(PVT)	P32 +1.5VP	Add PC170(2200P) install snubber PR156 PC156	RF commond
2010/10/8(pre-MP)	P30 Charger	Change PL210 to 1.2u (SH00000B100)	EMI commond
2010/10/08(Pre-MP)	P31 +5VALWP/+3VALWP	Change PC332 & PC352 to ESR 45 m ohm	cost down plane
2010/10/08(Pre-MP)	P32 +1.5VP	Change PC152 to ESR 35 m ohm	cost down plane
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