

Compal Confidential

ZAMB0/ZAMC0 M/B Schematics Document

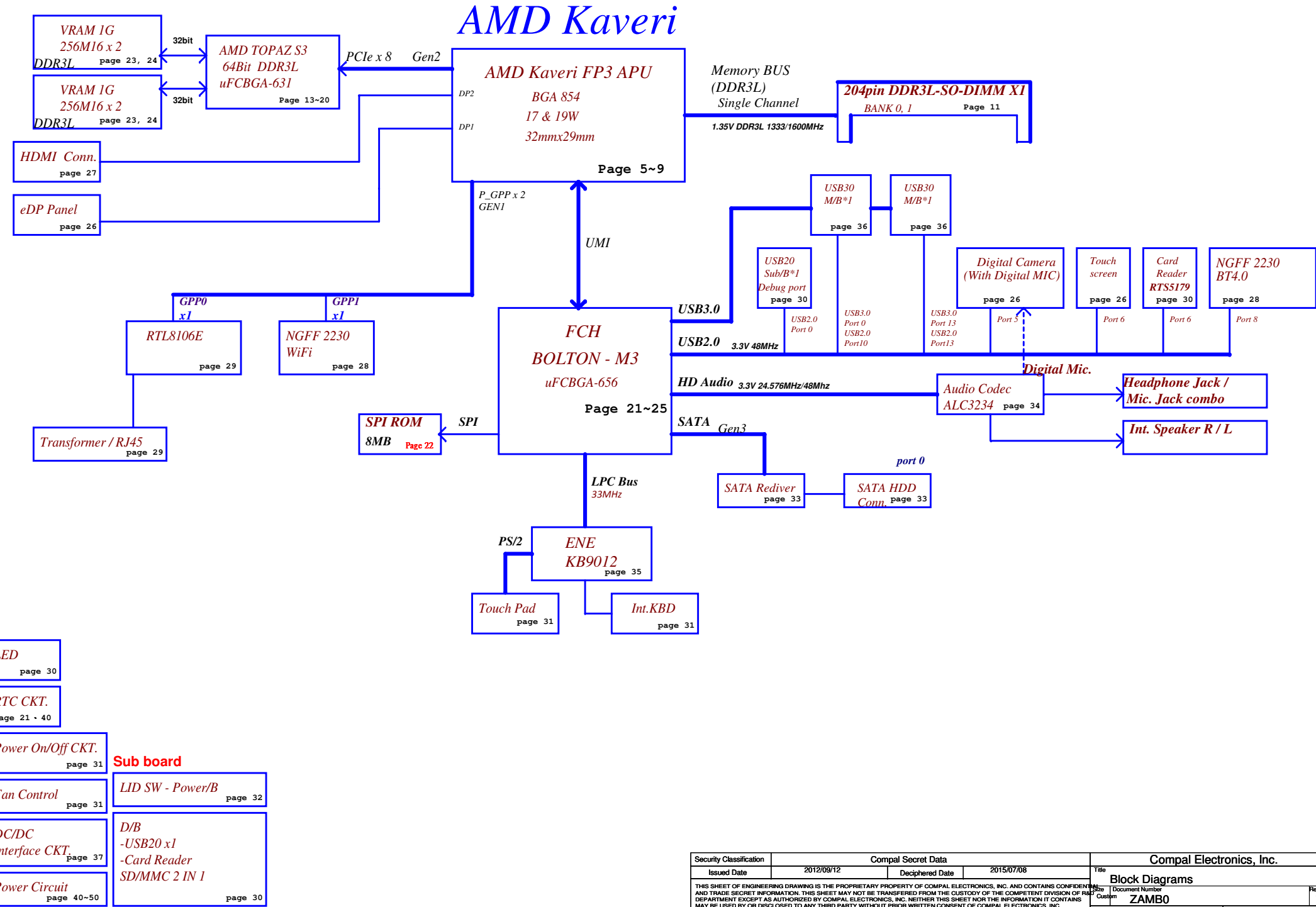
AMD Kaveri(FP3) + Bolton(M3)

AMD TOPAZ S3

2014-2-24

REV : 0.2

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Issued Date	2012/09/12	Deciphered Date	2015/07/08	Title	Cover Page
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Voltage Rails

Power Plane	Description	S0	S3	S4	S5
VIN	Adapter power supply (19V)	ON	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF	OFF
+APU_CORE_NB	Voltage for VDDNB	ON	OFF	OFF	OFF
+VGA_CORE	0.95-1.0V switched power rail	PX5	OFF	OFF	OFF
+VDDCI	0.95-1.0V switched power rail	PX5	OFF	OFF	OFF
+0.675VS	0.675V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+VGA_PCIE	0.95V switched power rail for VGA	PX5	OFF	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	AC/DC	AC/DC
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF	OFF
+1.05VS	1.05VS switched power rail for APU	ON	OFF	OFF	OFF
+1.35V	1.35V power rail for CPU VDDIO and DDR	ON	ON	OFF	OFF
+1.5VS	1.5VS switched power rail	ON	OFF	OFF	OFF
+3VGS	3.3V switched power rail for VGA	PX5	OFF	OFF	OFF
+1.8VGS	1.8V switched power rail for VGA	PX5	OFF	OFF	OFF
+1.8VS	1.8V for CPU_VDDA	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	ON
+3VALW	3.3V power rail for FCH	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	WOL	WOL
+3VS_WLAN_NGFF	3.3V power rail for WLAN	ON	IOAC	IOAC	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64

BOARD ID Table

Board ID	UMA	DIS (Topaz)
0	SSI	
1		SSI
2	PT	
3		PT
4	ST	
5		ST
6	1.0	
7		1.0

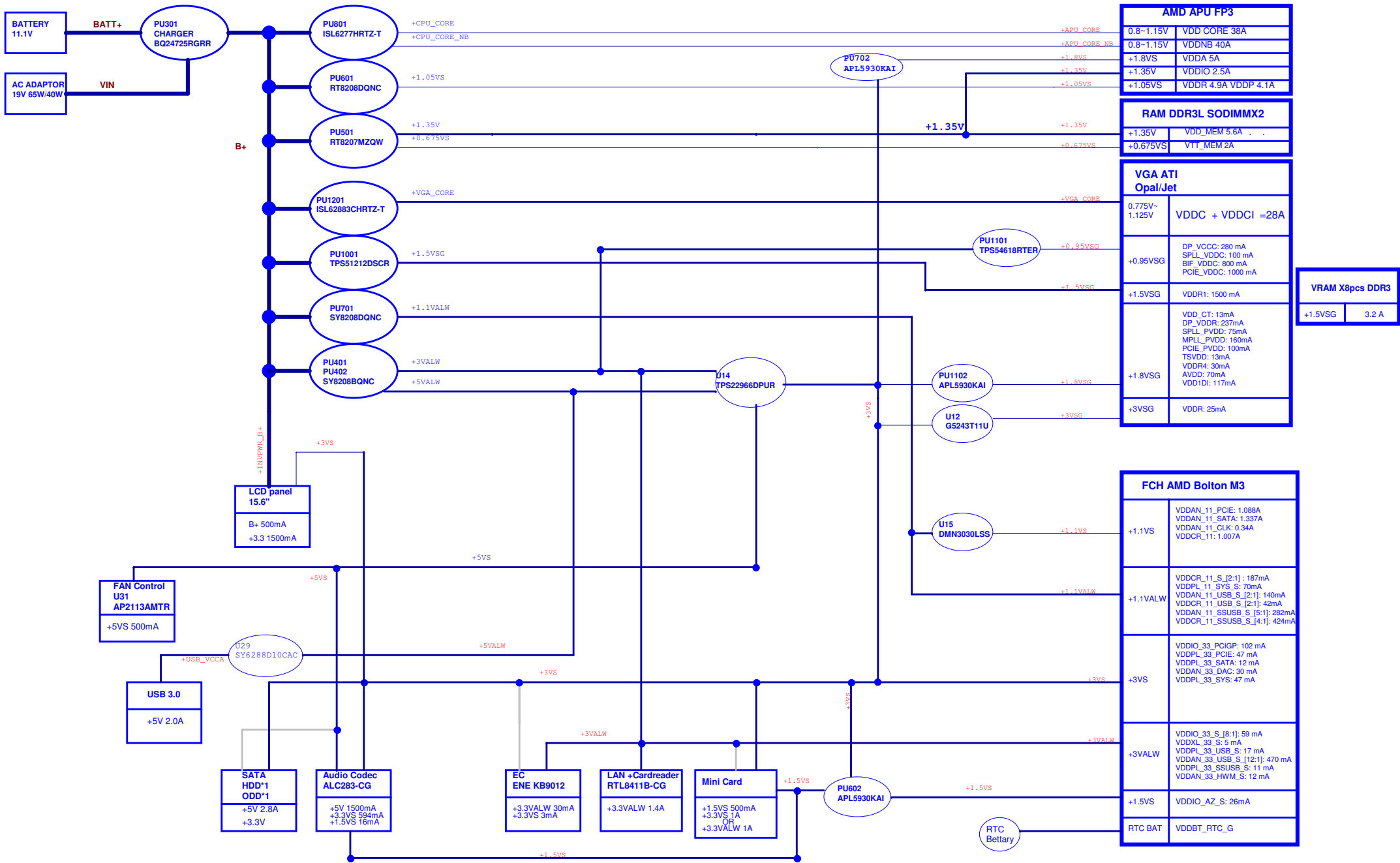
EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	Fintek thermal sensor	1001 101X b	9AH
Charger IC	0001 001X b	09H	SB-TSI (APU)	1001 100X b	98H
			VGA Internal Thermal	1000 001X b	82H

FCH SM Bus 0 address			FCH SM Bus 1 address		
Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1101 000X b	90			
MINI CARD					

BOM Option Table

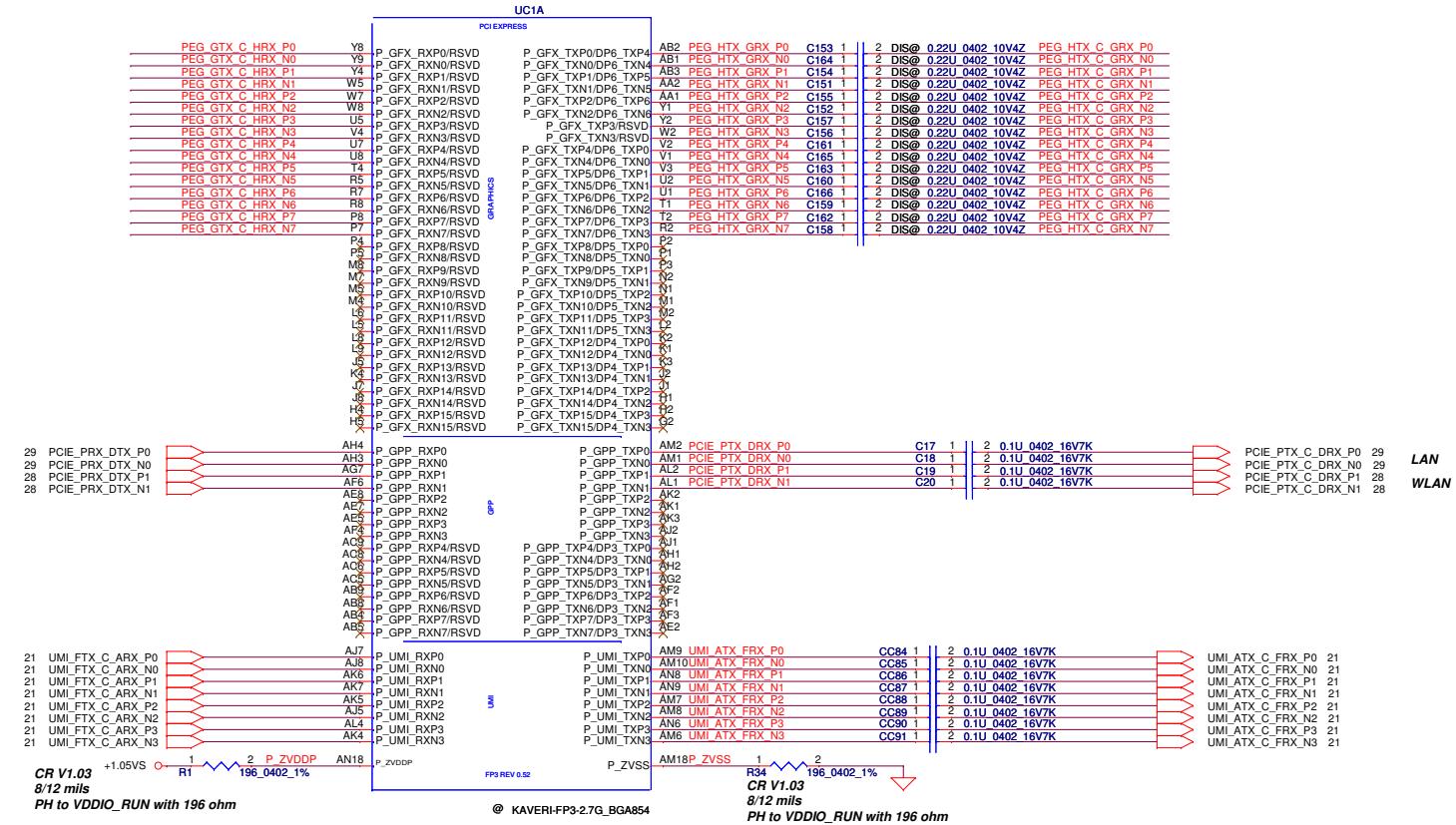
BOM Structure	Description	UMA 43XX	OPAL 43XX	JET 43XX															
9022@	Use EC 9022																		
9012@	Use EC 9012	V	V																
UMA@	Display output from APU (UMA only)	V	V																
VGA@	Use VGA (PX or DIS only)		V																
EDP@	Use eDP Panel		V																
AL@	Use Auto load EC code function																		
AC@	Support AC Function																		
NOAC@	No Support AC Function																		
		V	V																
CONN@	Connector (Control by ME)	V	V																
HDT@	Debug Connector																		
EMC@	EMC Component																		
XEMC@	Reserve for EMC																		
X76@	VRAM ID Table (Load By X76J)																		
128@	VRAM x 8pcs																		
OPAL@	ATI OPAL VGA CONTROLLER																		
JET@	ATI JET VGA CONTROLLER																		
BL@	ATI JET VGA CONTROLLER																		
@	Unpop																		
TS@	Touch Screen																		
NEMI@	Unpop EMI																		
NESD@	Unpop ESD																		
AOAC@	AOAC Function																		
NAOAC@	Non AOAC Function																		

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13 PEG_GTX_C_HRX_P[7..0] PEG_GTX_C_HRX_P[7..0]
13 PEG_GTX_C_HRX_N[7..0] PEG_GTX_C_HRX_N[7..0]

PEG_HTX_C_GRX_P[7..0] PEG_HTX_C_GRX_P[7..0] 13
PEG_HTX_C_GRX_N[7..0] PEG_HTX_C_GRX_N[7..0] 13



A8-7100 AM7100ECH44JA 1.8G BGA 854P APU A10-7300 AM7300ECH44JA 2G BGA 854P APU FX-7500 FM7500ECH44JA 2.1G BGA 854P APU

SA00007S20L



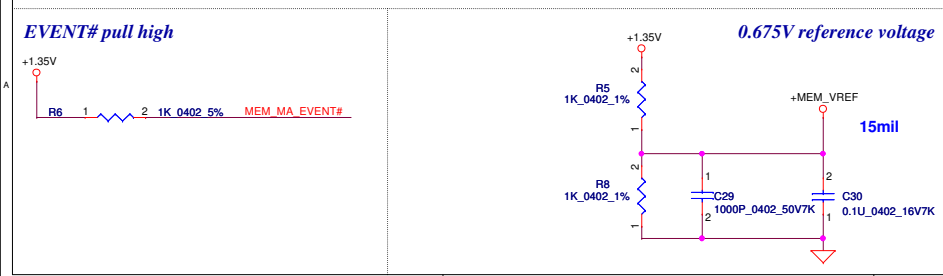
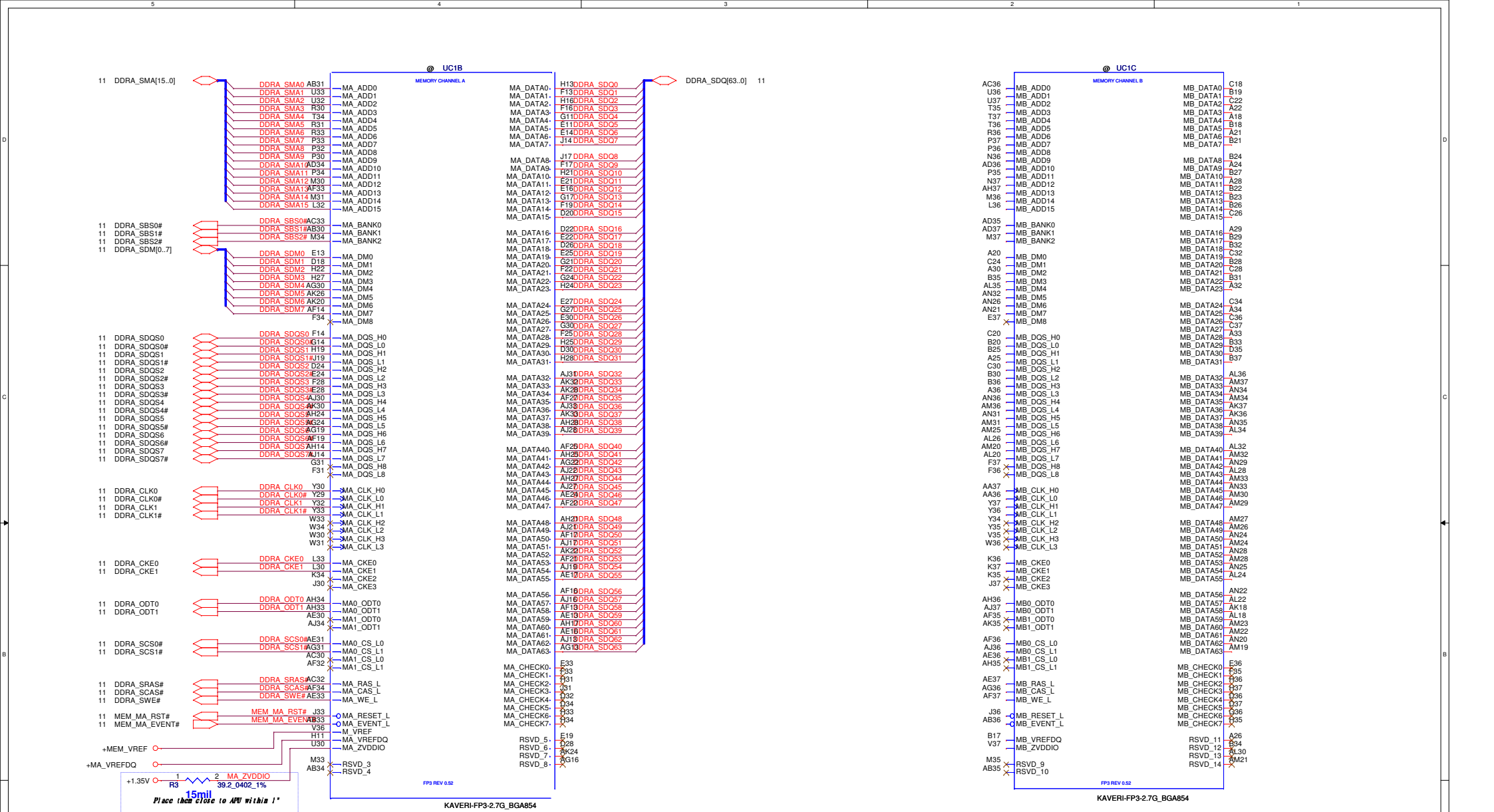
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SA00007TT0L

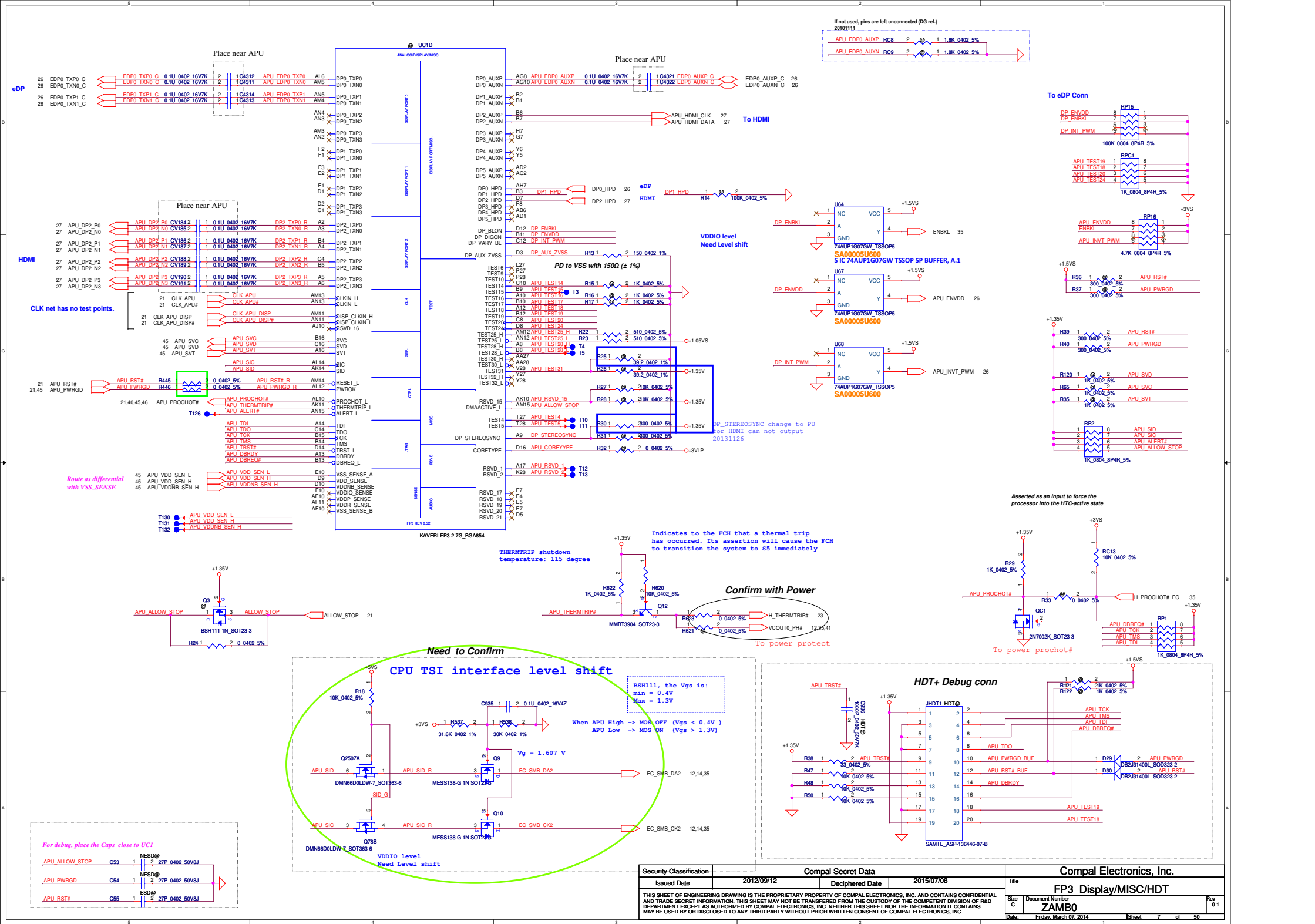
AMD, FX-7500, KAVERI, PR	SA00007TT0L	S IC FX-7500 FM7500ECH44JA 2.1G BGA 854P APU
AMD,A10-7300, KAVERI, PR	SA00007S30L	S IC A10-7300 AM7300ECH44JA 2G BGA 854P APU
AMD A8-7100, KAVERI, PR	SA00007S20L	S IC A8-7100 AM7100ECH44JA 1.8G BGA 854P APU

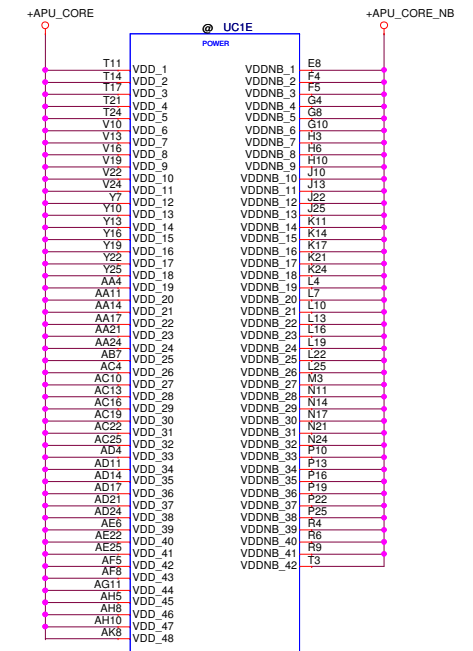
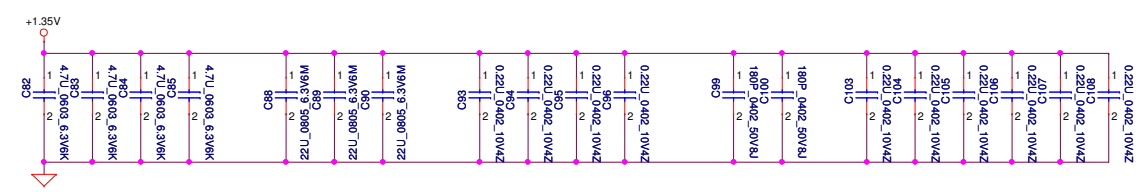
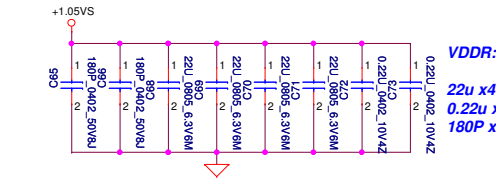
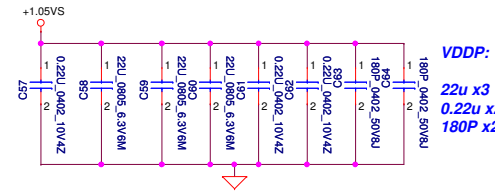
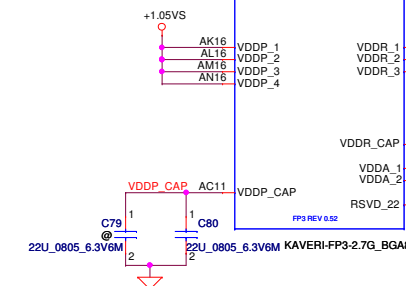
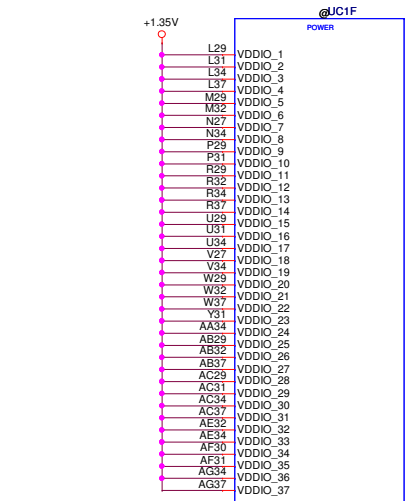
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M_VREF (APU)	A	Pull-up resistor to VDDIO	1 kΩ (± 1%)	–	VDDIO
		Pull-down resistor to VSS	1 kΩ (± 1%)	–	VSS
		Decoupling capacitor	0.1 μF	–	VSS
		Decoupling capacitor	1 nF	–	VSS

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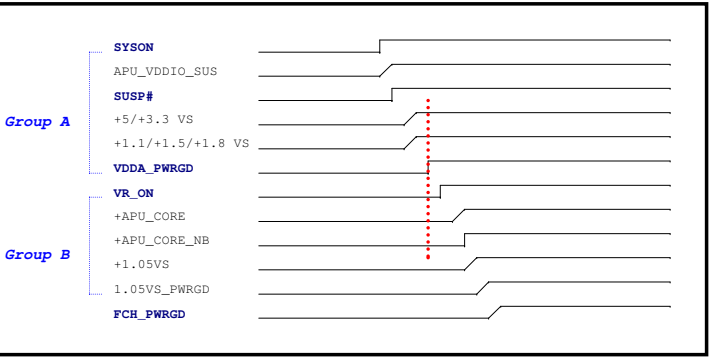


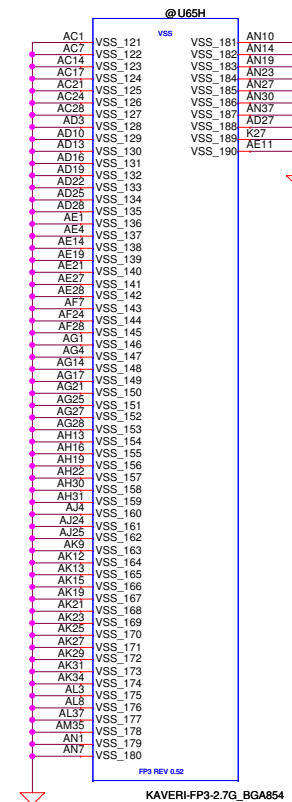
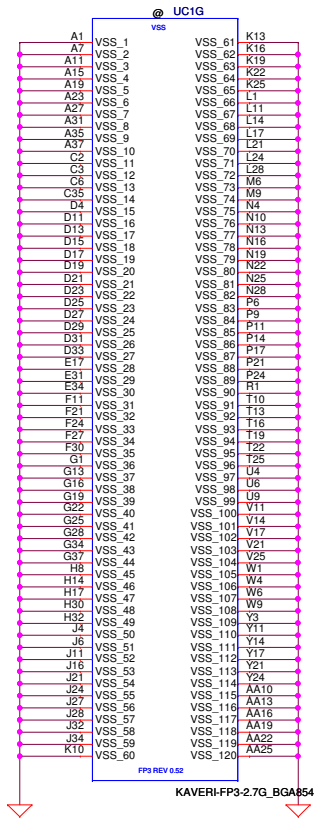


Power Name	Consumption
VDD +APU_CORE	38A
VDDNB +APU_CORE_NB	40A
VDDIO +1.35V	2.5A
VDDP / VDDR +1.05VS	4.0A / 3.9A
VDDA +1.8VS	0.7A

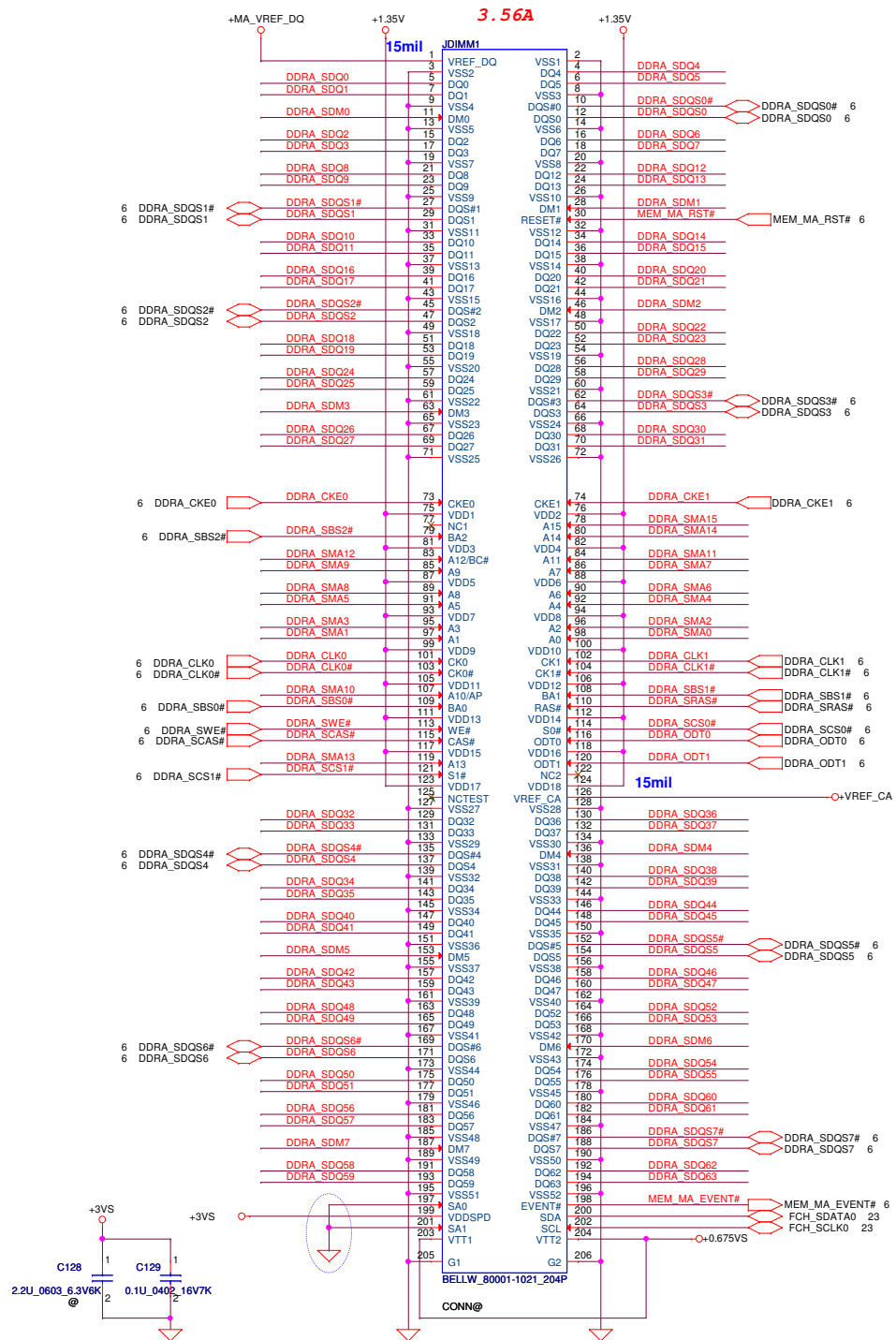
Check list CH47
+APU_CORE Decoupling
Power Side
22uF x11 @ x2
0.22uF x2
0.01uF x3
180pF x3

APU sequence : GROUP A need ramp before GROUP B

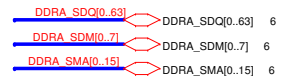




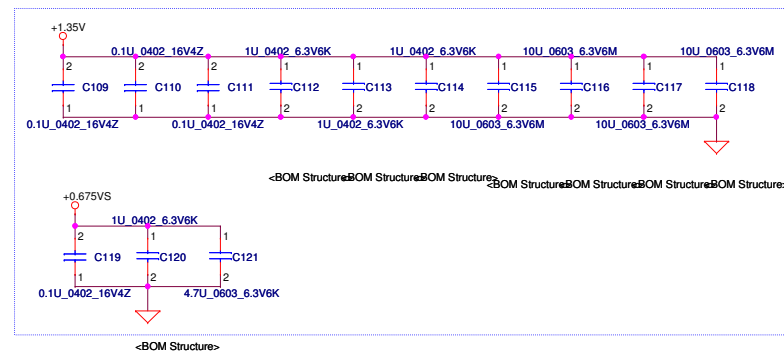
5		4		3		2		1	
D									
								</	



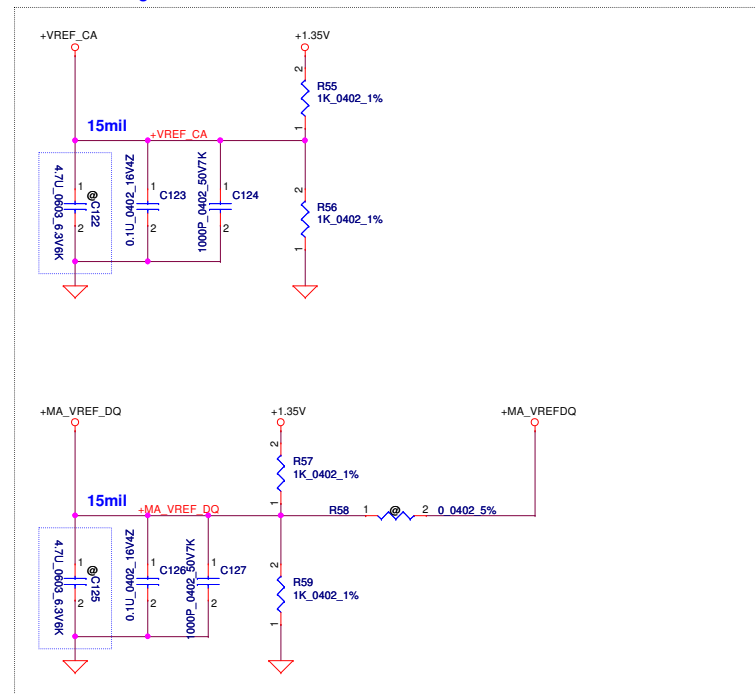
DIMM_A STD H:4mm
 <Address: 00>



Place near DIMM1



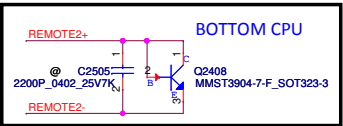
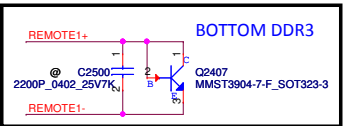
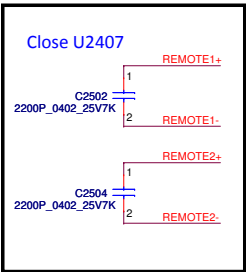
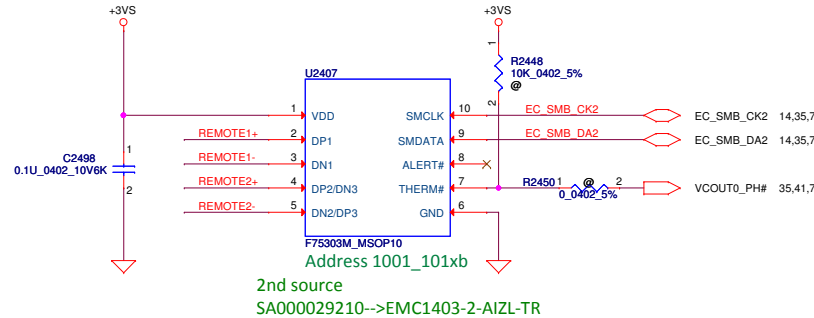
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Fintek thermal sensor
placed near by DDR3

SA000046C00(S IC EMC1403-2-AIZL-TR MSOP 10P SENSOR)



REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

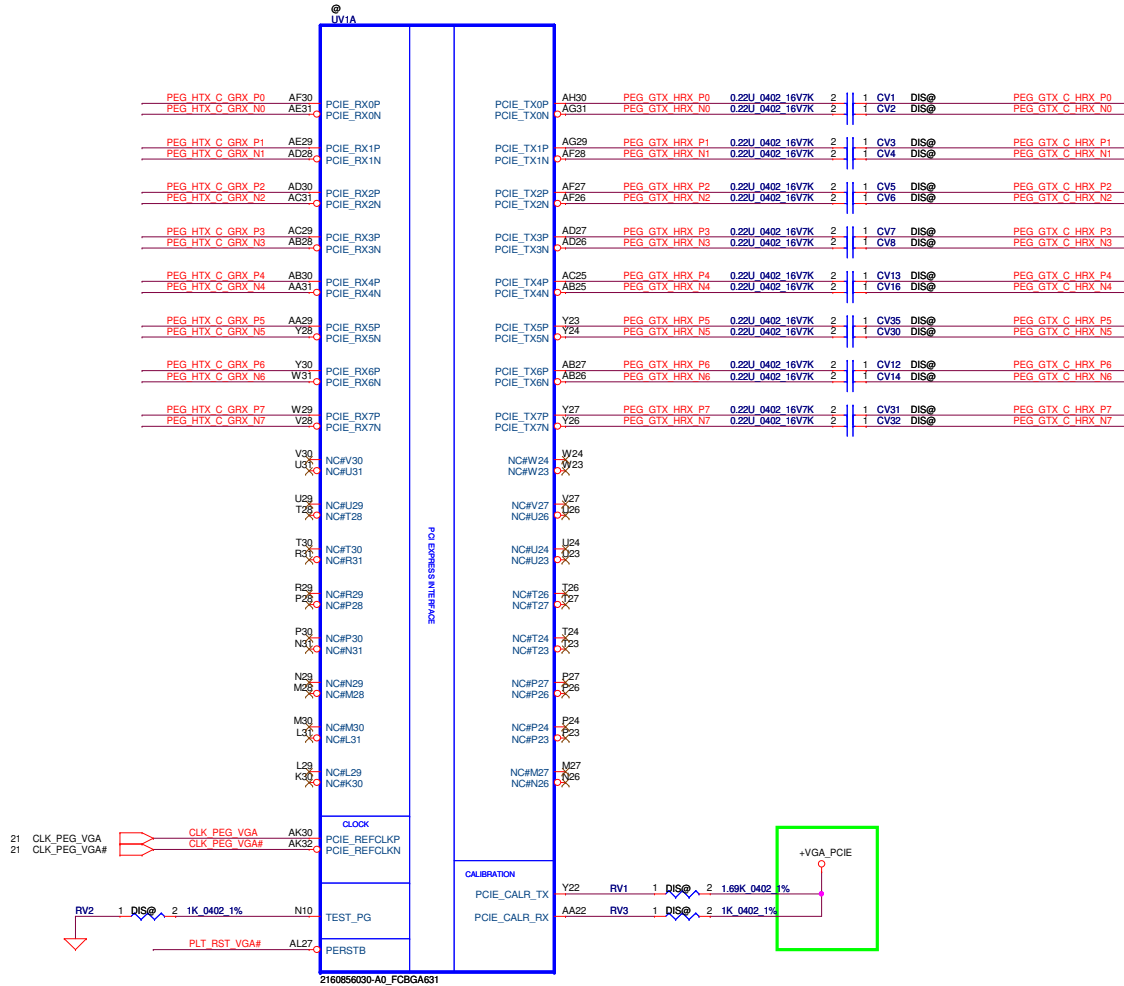
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5 PEG_HTX_C_GRX_P[0..7] PEG_HTX_C_GRX_P[0..7]
5 PEG_HTX_C_GRX_N[0..7] PEG_HTX_C_GRX_N[0..7]

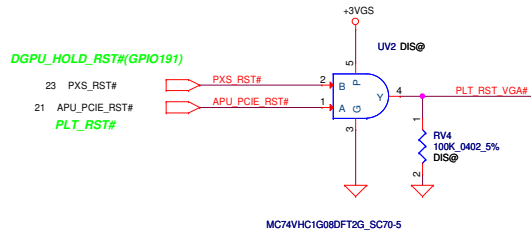
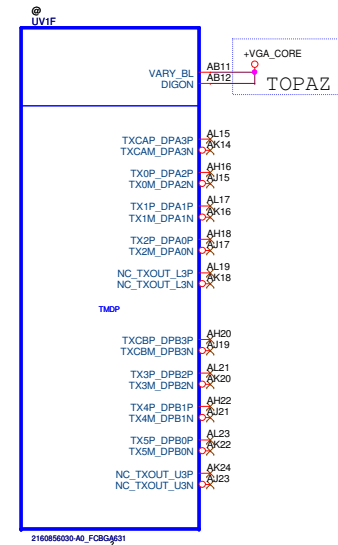
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UV1 TOPAZ@
TOPAZ XT S3 FCBGA 631P GPU 0FD
SA000079N0L

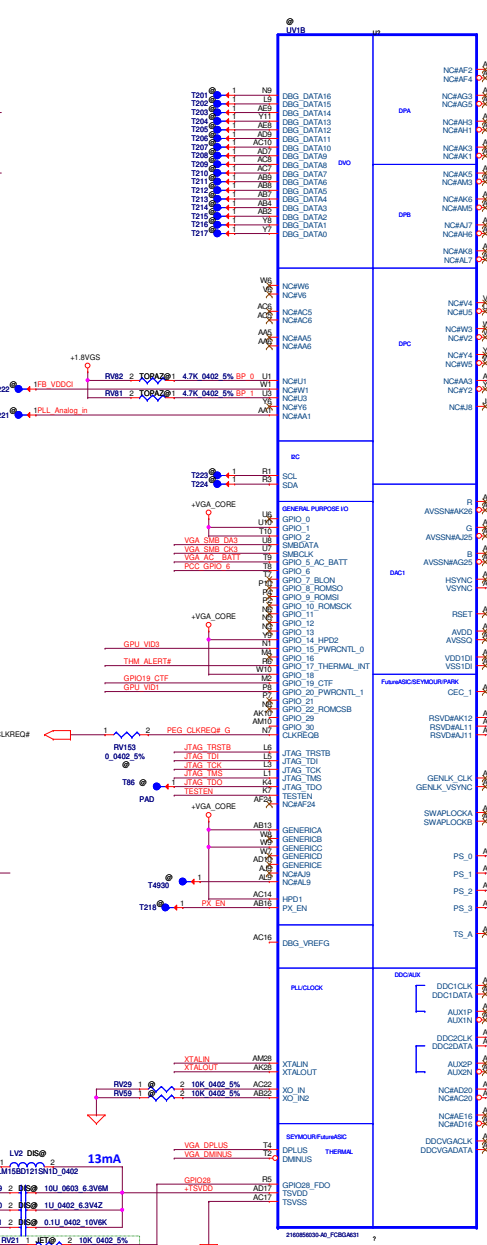
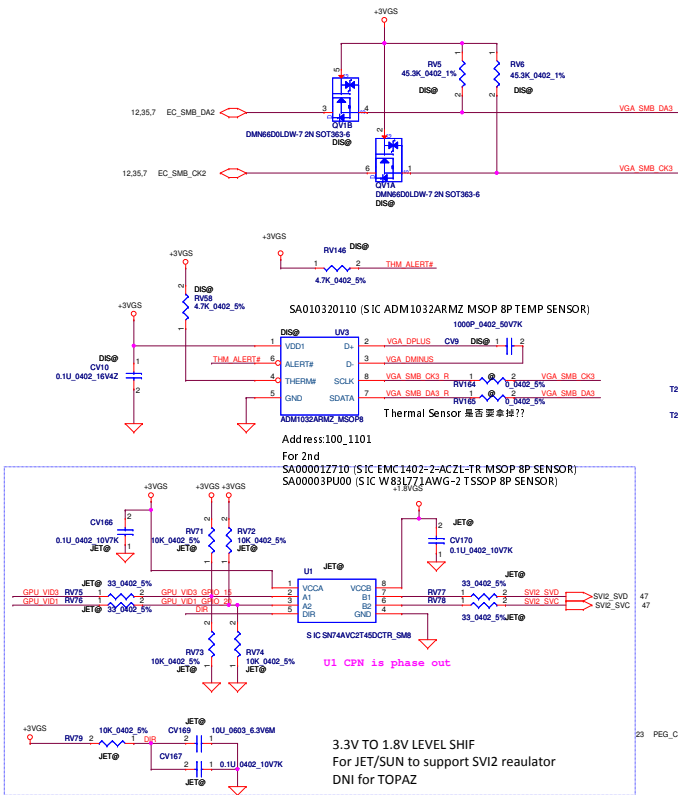
UV1 JET@
JET XT S3 FCBGA 631P GPU 0FD
SA00007A50L



No Use GPU Display Port output

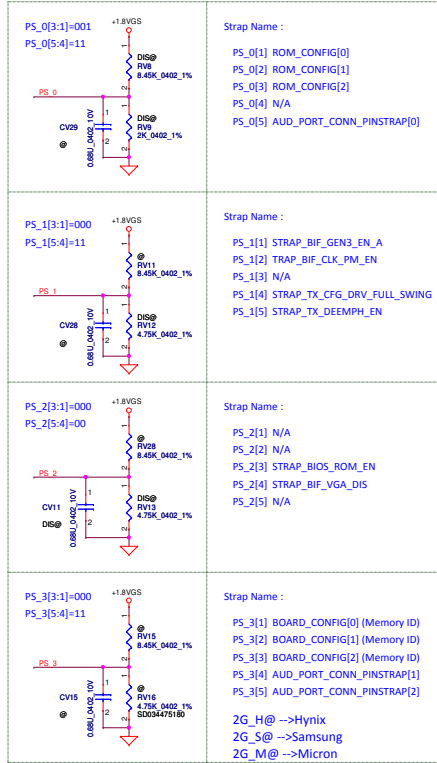


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Resistor Divider Lookup Table			
R_pu (ohm)	R_pd (ohm)	Bitt [3:1]	
NC	4.75k	000	
8.45k	2k	001	
4.53k	2k	010	
6.98k	4.99k	011	
4.53k	4.99k	100	
3.24k	5.62k	101	
4.75k	10k	110	
4.75k	NC	111	

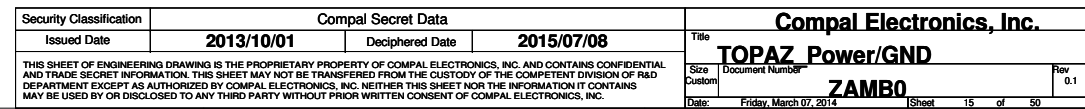
Capacitor Divider Lookup Table	
Cap (nF)	Bitt [5:4]
680nF	00
82nF	01
10nF	10
NC	11



Memory ID	P/N	Vendor	Configuration	Size
000	SA00006U0L	SAMSUNG	K4W2G1646Q-BC1A	1GB
001	SA00006H40L	HYNIX	H5TC2G63FFR-11C	1GB
010	SA00006750L	Micron	MT41J128M16T-093G	1GB
011	SA000076POL	SAMSUNG	K4W4G1646D-BC1A	2GB
100	SA00006E80L	HYNIX	H5TC4G63AFR-11C	2GB
101	SA000077K0L	Micron	MT41J256M16HA-093G:E	2GB

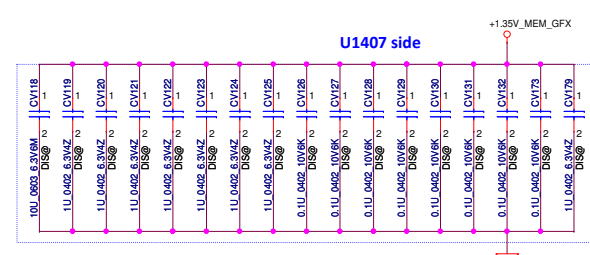
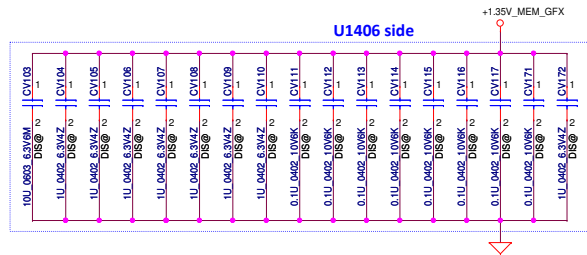
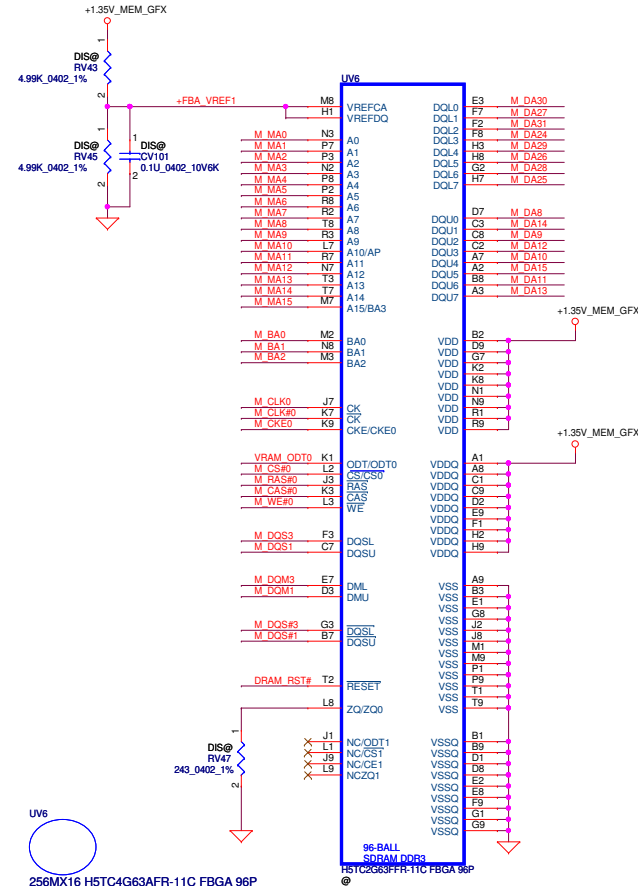
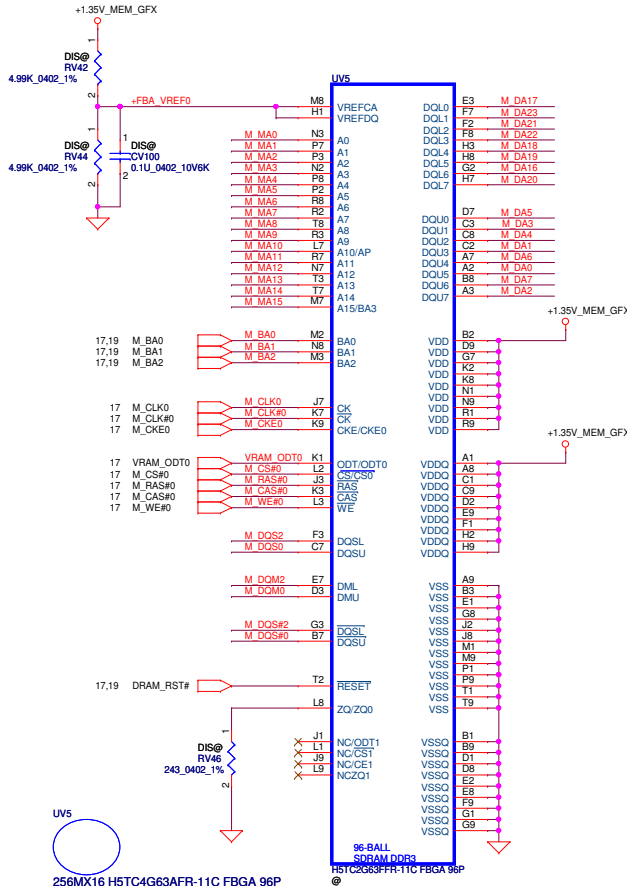
Maple AMD 2G VRAM Only

JP9 DEFAULT SHORT



Memory Partition A - Lower 32 bits

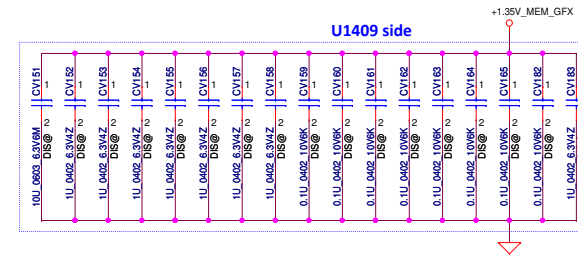
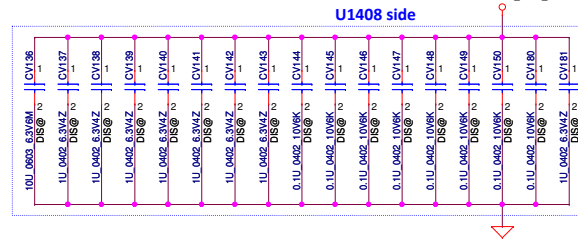
17,19 M_DA[63..0] M_DA[63..0]
17,19 M_MA[15..0] M_MA[15..0]
17,19 M_DQM[7..0] M_DQM[7..0]
17,19 M_DQS[7..0] M_DQS[7..0]
17,19 M_DQS#[7..0] M_DQS#[7..0]



X7655131104, ALT. GROUP PARTS VRAM 2G HYNIX ZAVC0, A.2 (Design)
SA00006E80L, S IC D3 256MX16 H5TC4G63AFR-11C FBGA 96P, A.1 (Design)
SD034453180, S RES 1/16W 4.53K +-1% 0402, A.1 (Design)
SD034499180, S RES 1/16W 4.99K +-1% 0402, A.2 (Design)
X7655131105, ALT. GROUP PARTS VRAM 2G SAMSUNG ZAVC0, A.2 (Design)
SA000076P0L, S IC D3 256MX16 K4W4G1646D-BC1A FBGA 96P, A.2 (Design)
SD000002680, S RES 1/16W 6.98K +-1% 0402, A.1 (Design)
SD034499180, S RES 1/16W 4.99K +-1% 0402, A.2 (Design)
X7655131106, ALT. GROUP PARTS VRAM 2G MICRON ZAVC0, A.2 (Design)
SA000077K0L, S IC D3 256MX16 MT41J256M16HA-093G:E FBGA, A.4 (Design)
SD034324180, S RES 1/16W 3.24K +-1% 0402, A.1 (Design)
SD034562180, S RES 1/16W 5.62K +-1% 0402, A.1 (Design)

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S20 Custom		Rev 0.1	
Date: Friday, March 07, 2014		Sheet 18 of 50	

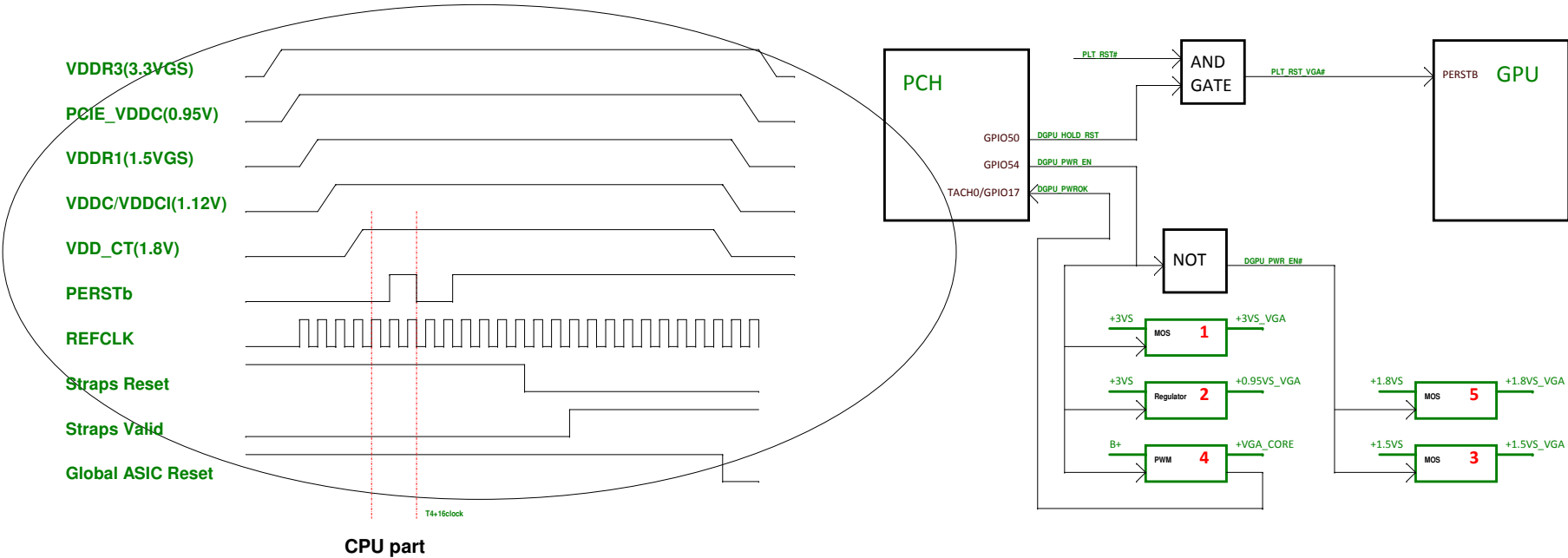
17,18	M_DA[63..0]		M_DA[63..0]
17,18	M_MA[15..0]		M_MA[15..0]
17,18	M_DQM[7..0]		M_DQM[7..0]
17,18	M_DQS[7..0]		M_DQS[7..0]
17,18	M_DQS#[7..0]		M_DQS#[7..0]

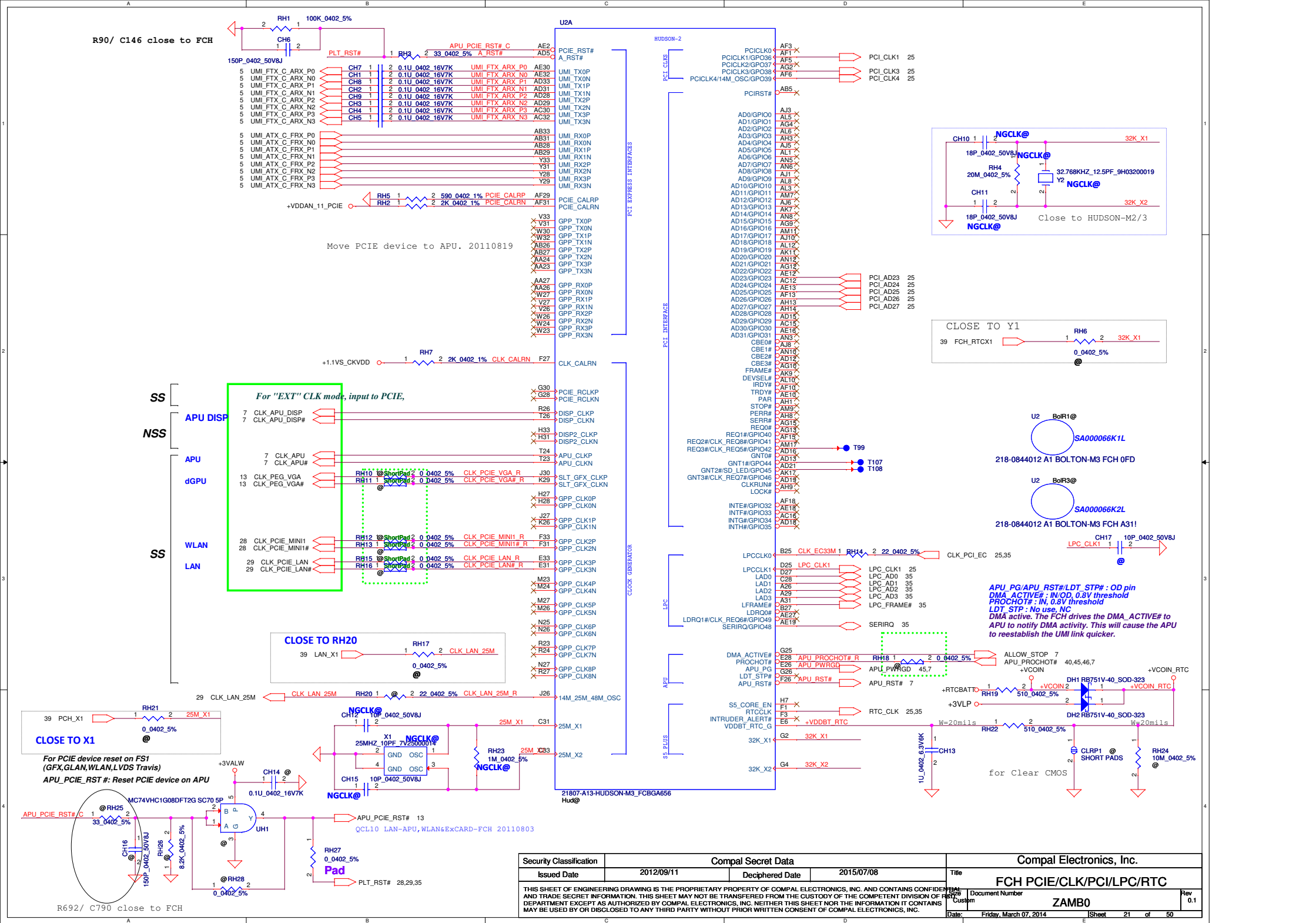


Security Classification		Compal Secret Data		Compal Electronics, Inc. TOPAZ VRAM A Upper	
Issued Date	2013/10/01	Deciphered Date	2015/07/08	Title	
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				Date:	Friday, March 07, 2014 Sheet 19 of 50

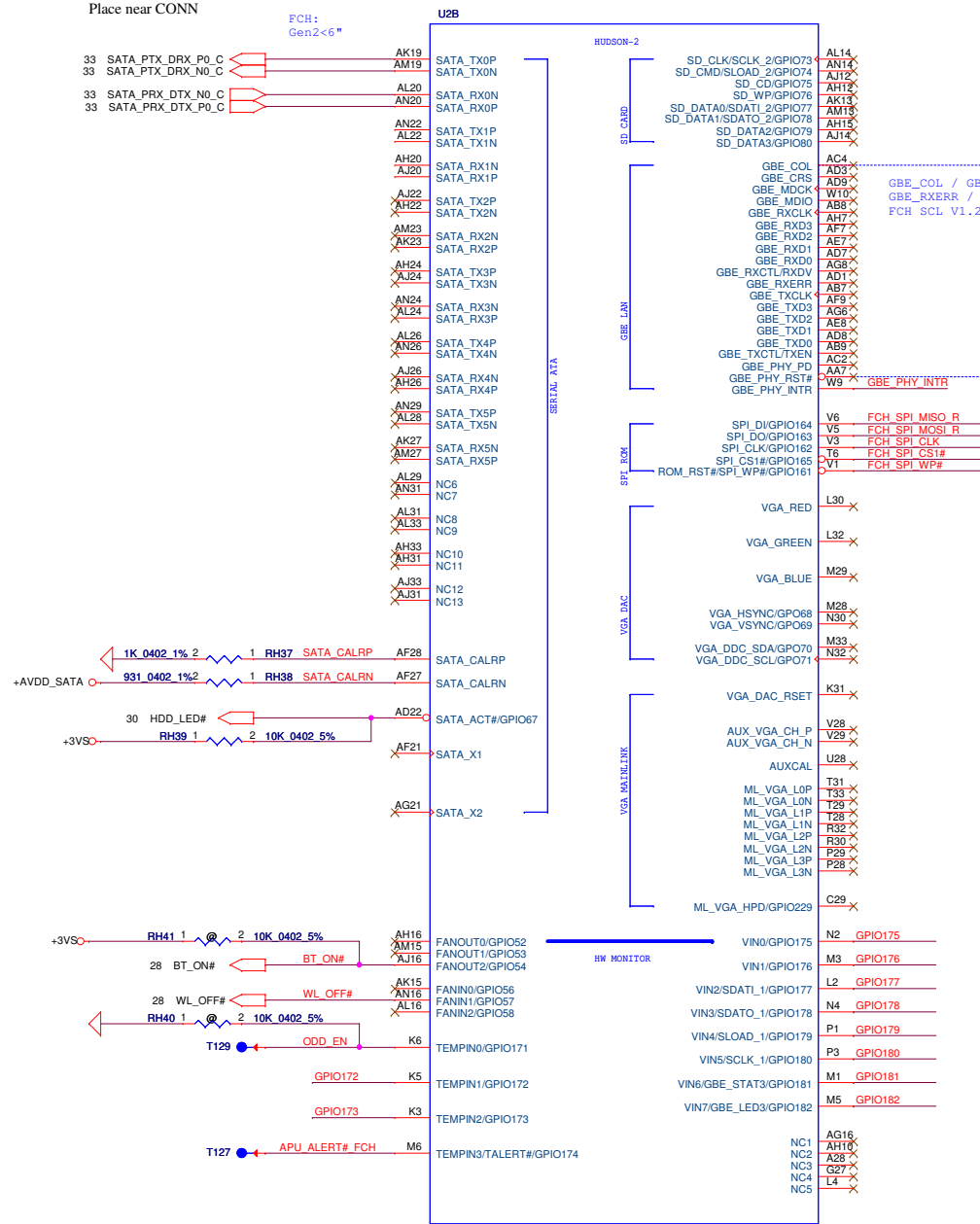
Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
3. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
4. For power down, reversing the ramp-up sequence is recommended.

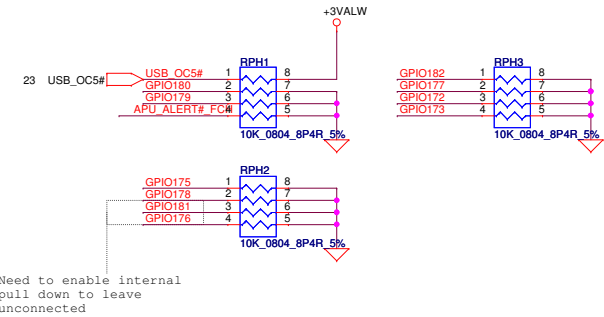
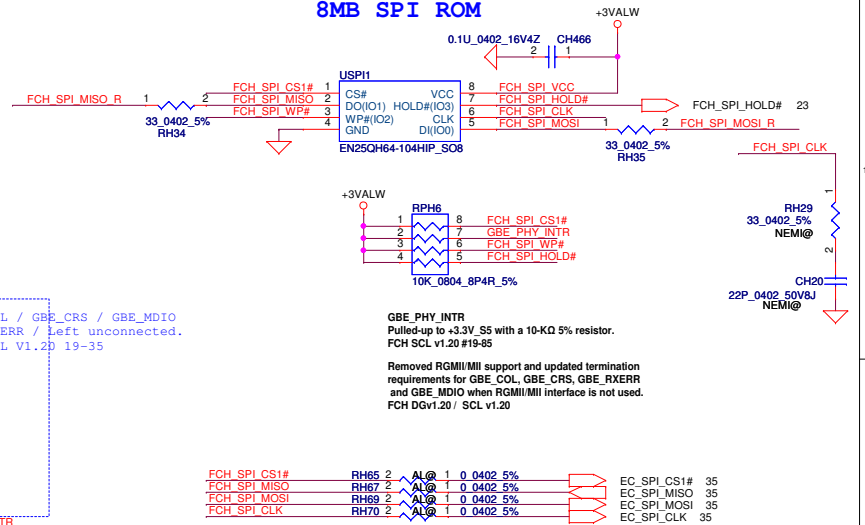




HDD

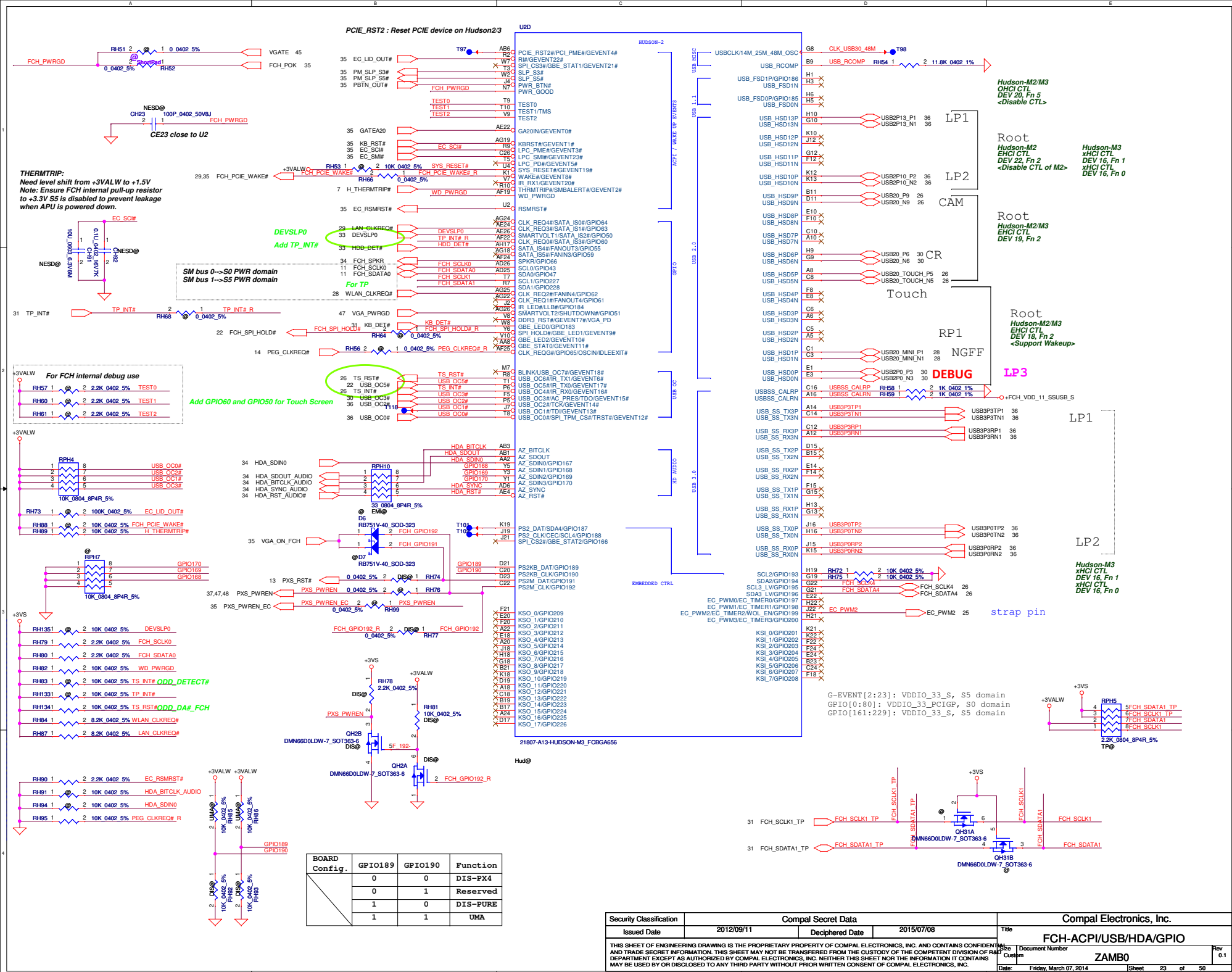


8MB SPI ROM

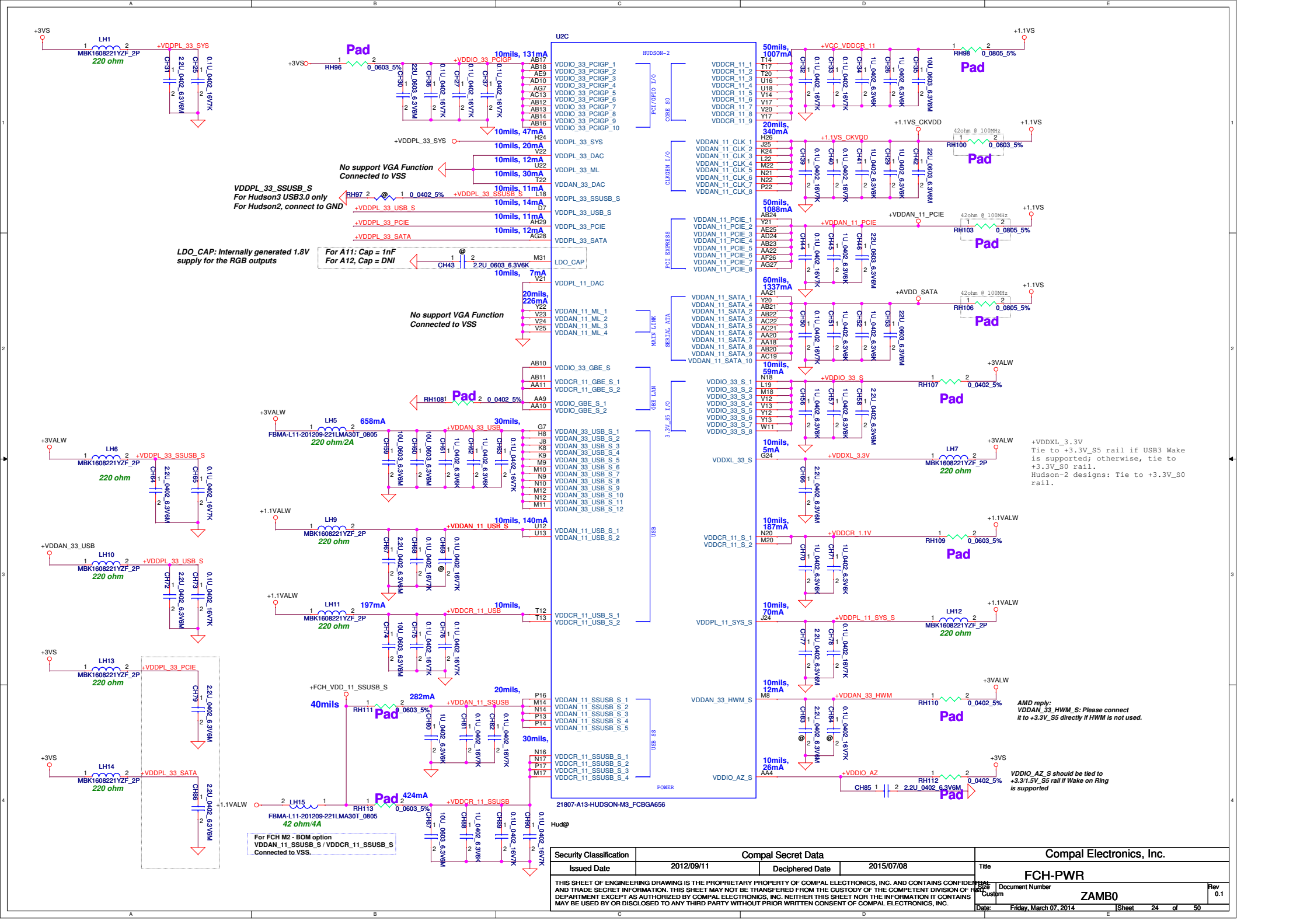


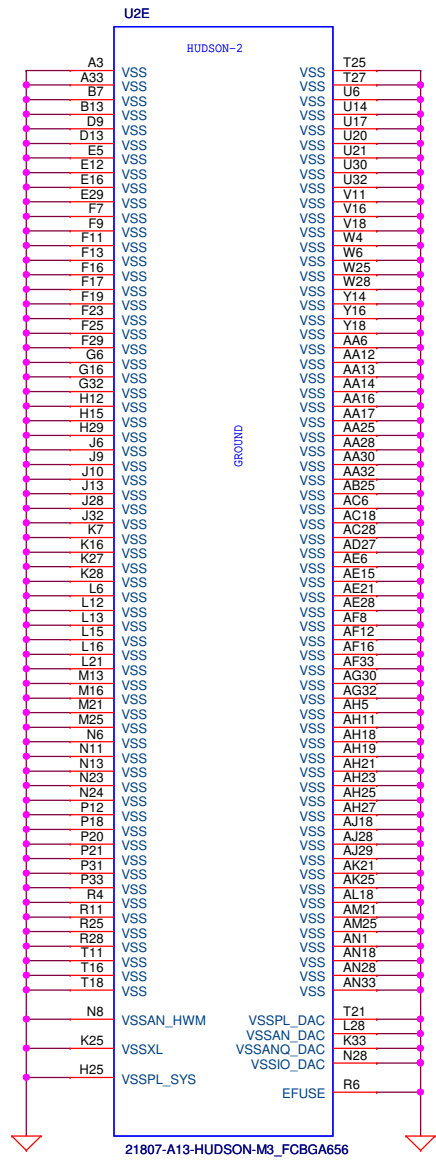
Hud@

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				ZAMBO	0.1
				Date: Friday, March 07, 2014	Sheet 22 of 50



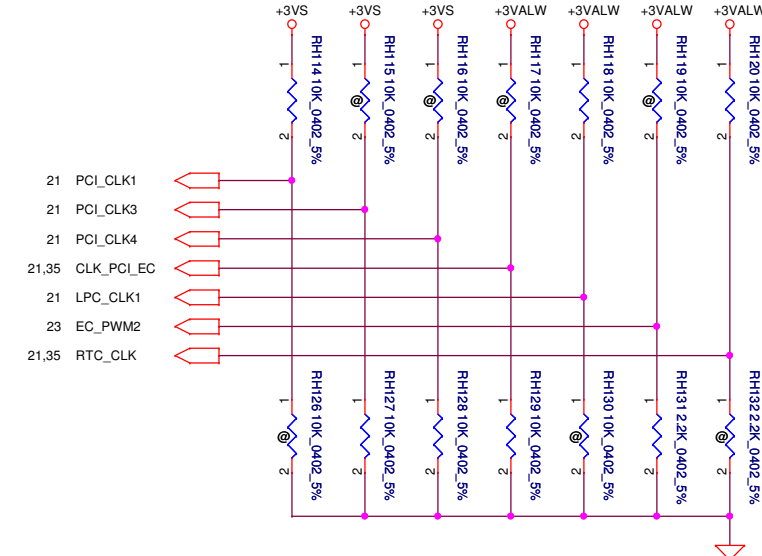
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/09/11	Deciphered Date	2015/07/08	Title	FCH-ACPI/USB/HDA/GPIO	
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STRAP PINS

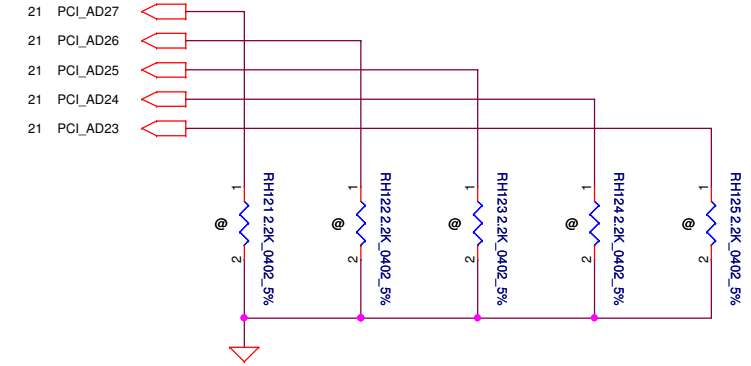
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



DEBUG STRAPS

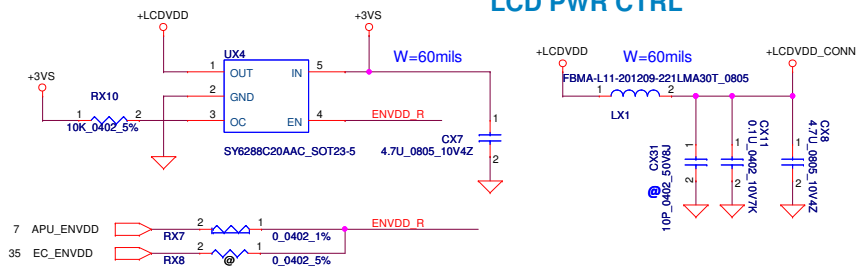
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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								Size	Document Number	Rev
								B	ZAMBO	0.1
								Date:	Friday, March 07, 2014	Sheet

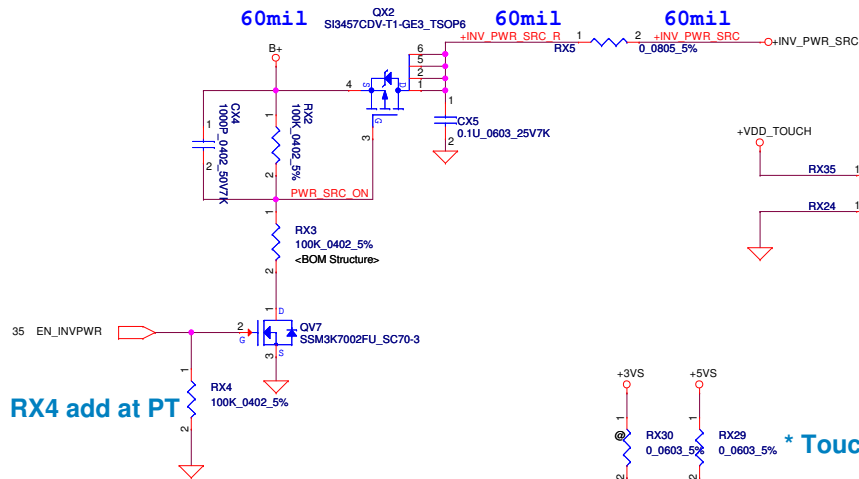
LCD PWR CTRL



Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

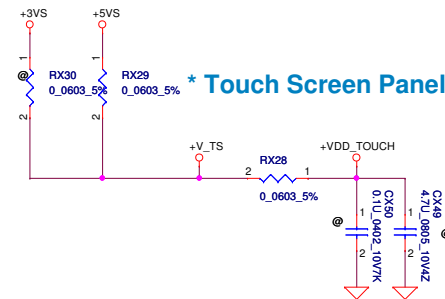
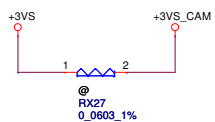
SS table

LCD backlight PWR CTRL



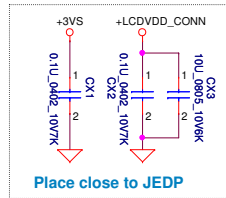
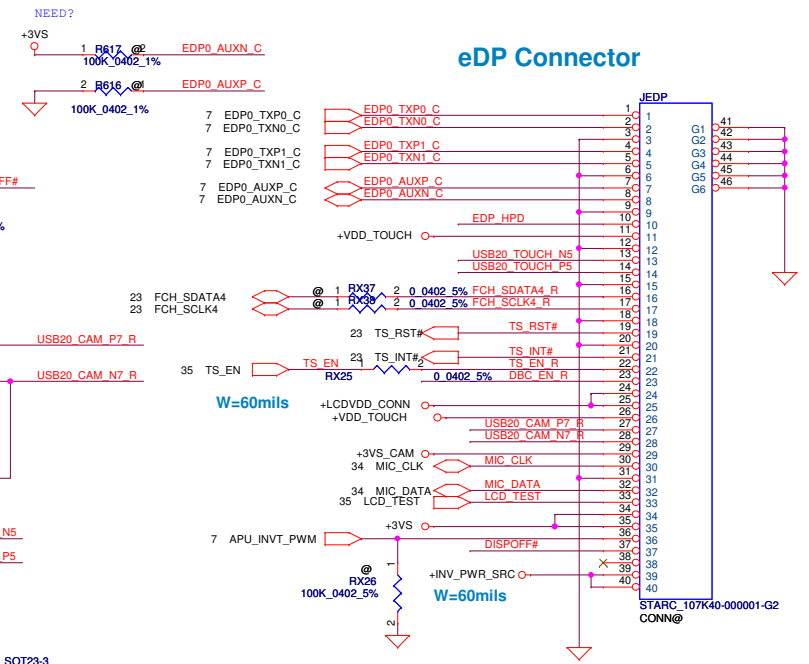
RX4 add at PT

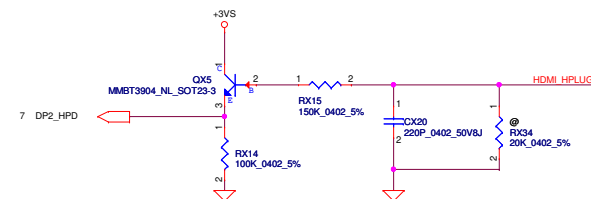
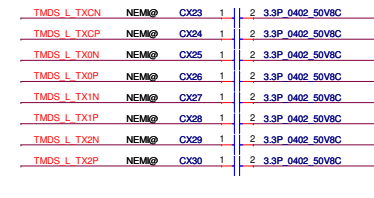
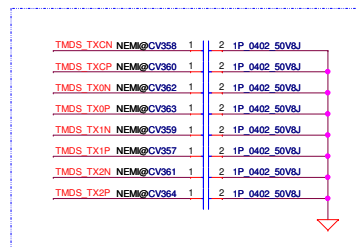
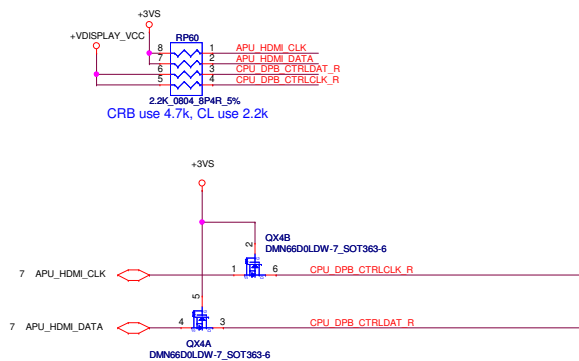
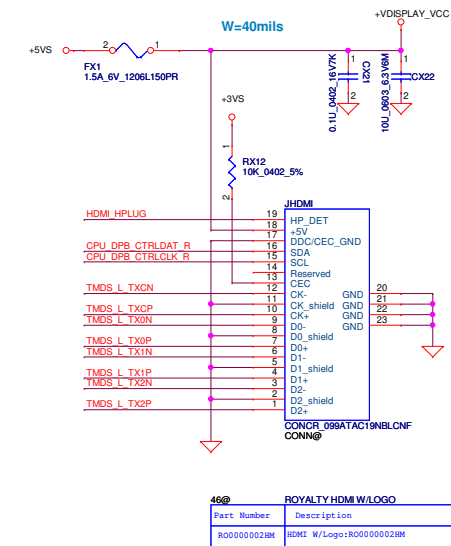
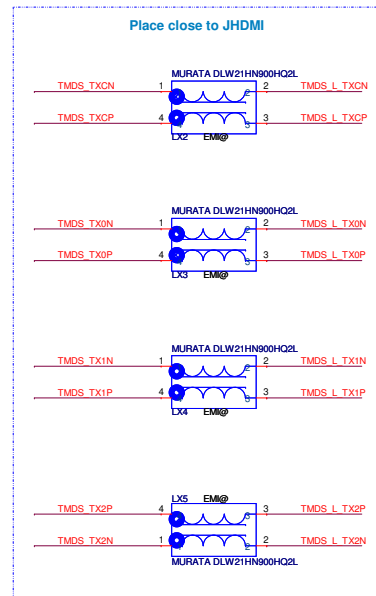
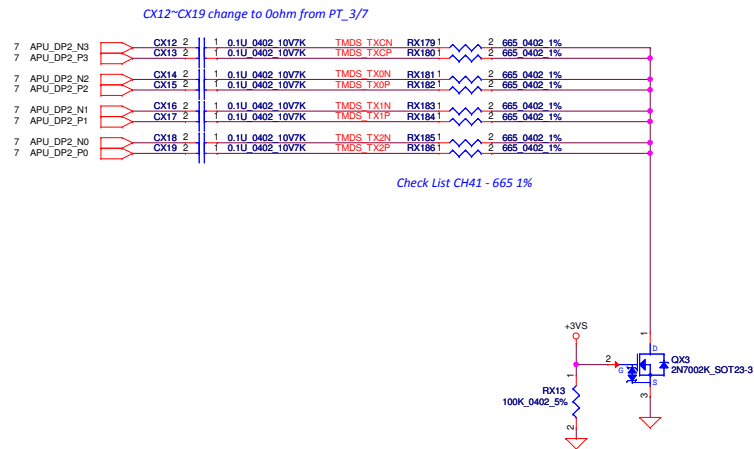
Webcam PWR CTRL



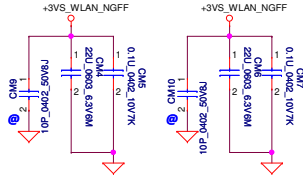
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eDP Connector

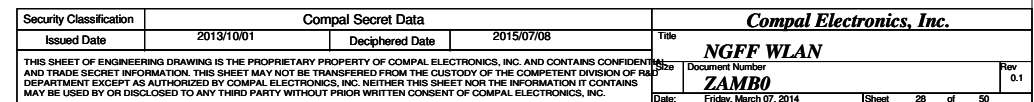
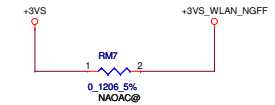




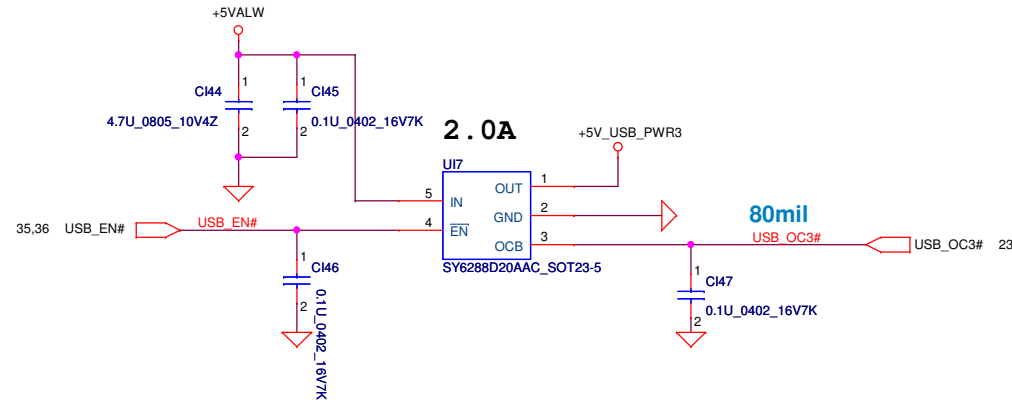
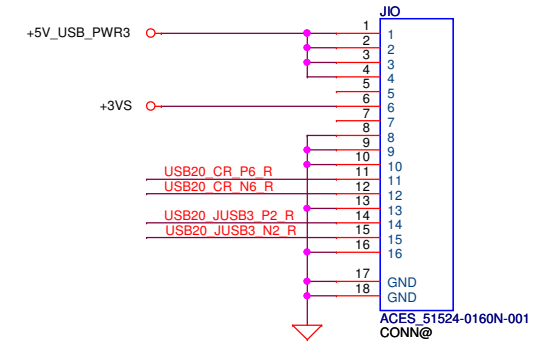
closed to pin 64, 66



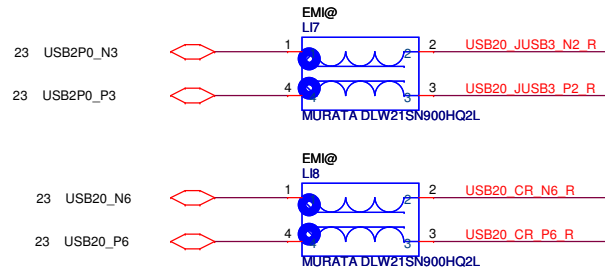
+3VALW TO +3VS_WLAN_NGFF



IO to MB CONN Substitute:SP01001FS00

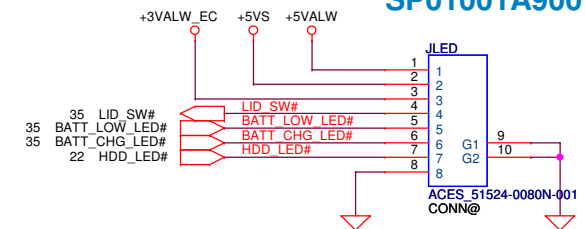


USB Conn DEBUG Port



Card Reader

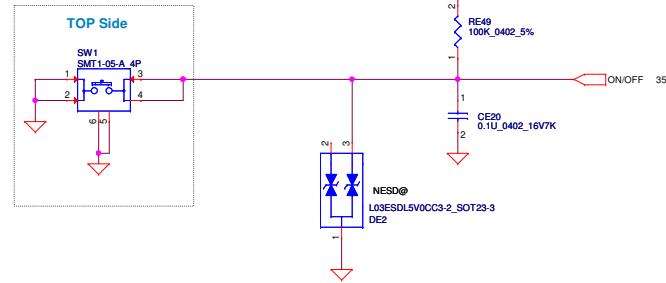
LED/B TO M/B SP01001A900



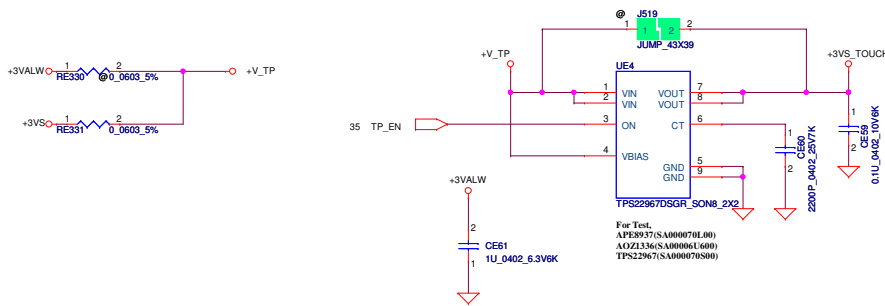
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Issued Date	2013/10/01	Deciphered Date	2015/07/08	IO/B, LED/B	
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				Document Number ZAMB0	0.1
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Power ON Circuit

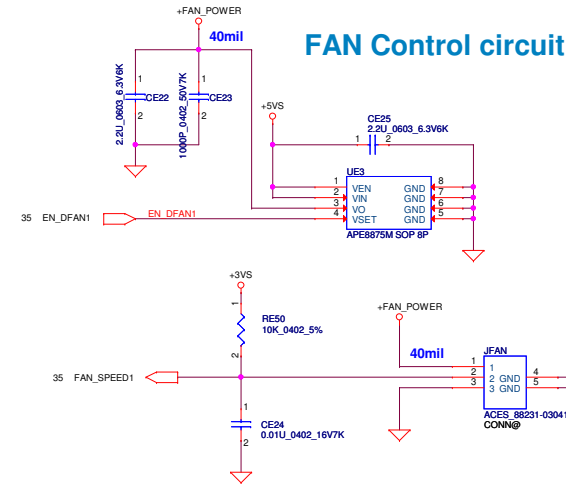
ON/OFF switch



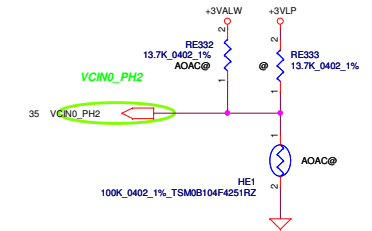
J519 short



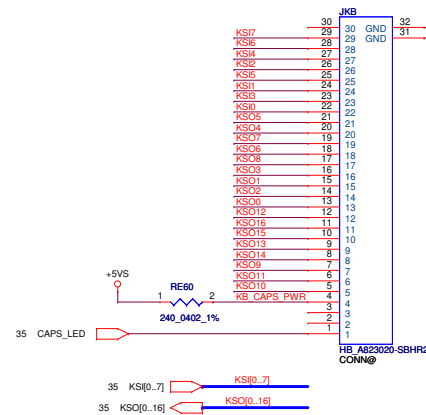
FAN Control circuit



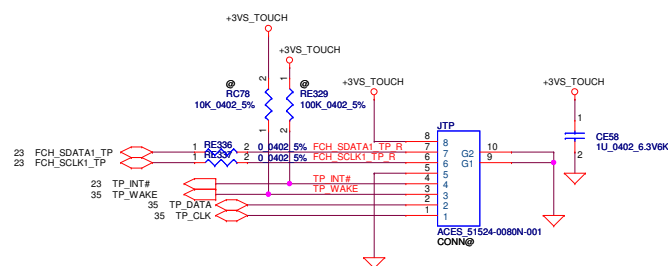
HE1 place around FAN area.



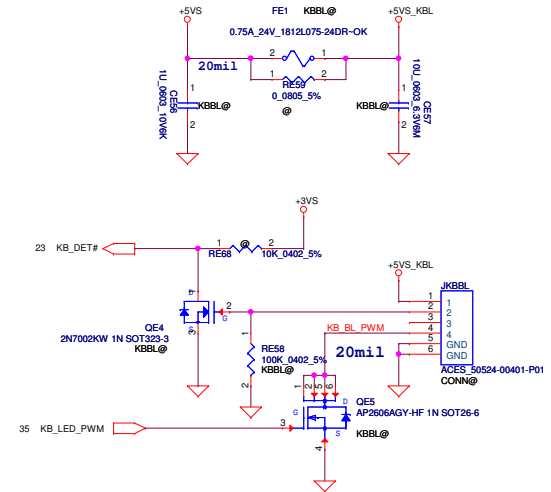
INT_KBD Connector



Touch pad PS/2 only



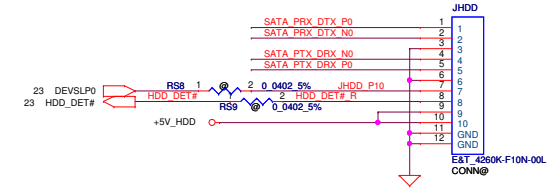
* Key Board Back Light



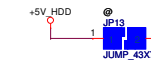
Security Classification		Compal Secret Data		Title	
Issued Date	2013/10/01	Deciphered Date	2015/07/08	FAN / TP / PWR SW / KBBL	
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				Custom	ZAMB0	0.1
				Date:	Friday, March 07, 2014	Sheet 32 of 50

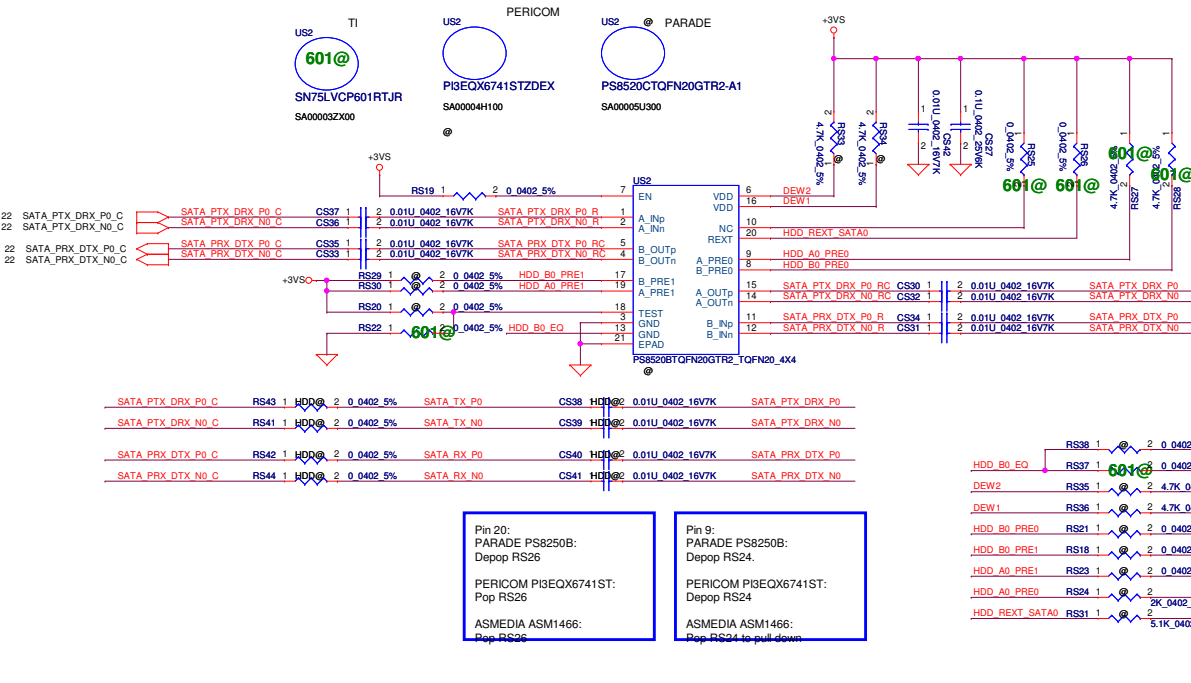
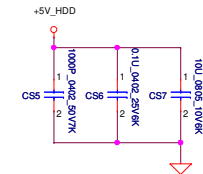
SATA HDD Connector



+5V_HDD Source



SHORT DEFAULT



Pin 20: PARADE PS8250B: Depop RS26	Pin 9: PARADE PS8250B: Depop RS24
PERICOM PI3EQX6741ST: Pop RS26	PERICOM PI3EQX6741ST: Depop RS24
ASMEIA ASM1466: Pop RS26	ASMEIA ASM1466: Pop RS24 to pull down

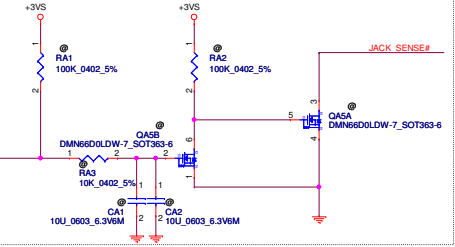
CA71, CA51 place close to Pin 26

CA53, CA55 change Value from 10U_0603_6.3V6M to 4.7U_0603_6.3V6K

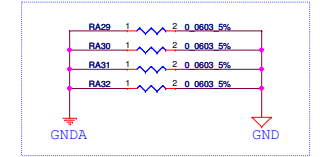
CA57, CA58 close to UA1 pin1

CA59 CA60 close to UA1 pin9

JACK_PLUG Delay circuitis

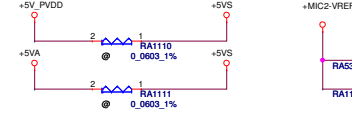
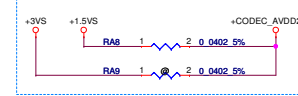


Reserve for cancel Delay circuitis



Place on the moat between GND & GNDA.

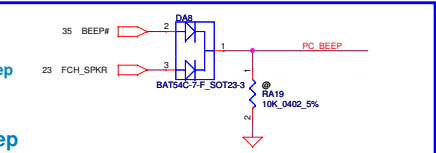
Reserve for HDA issue



EC Beep

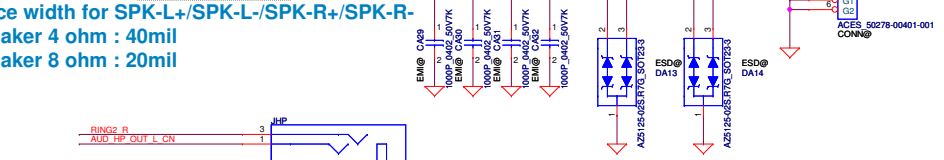
MCU Beep

PC Beep

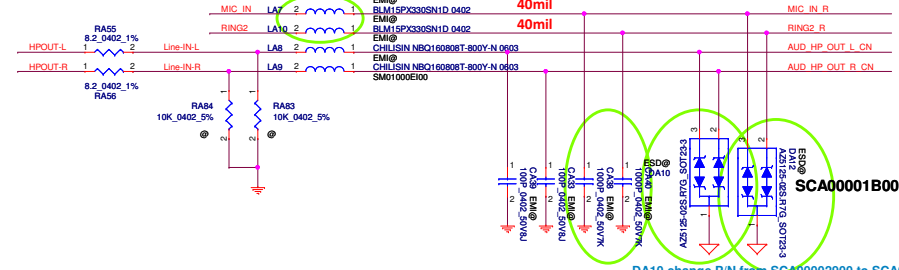


Close to UA1 Pin11,13,14,16

Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

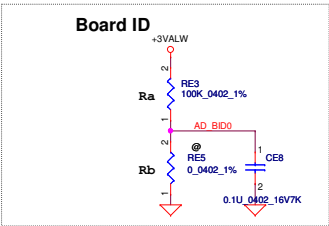
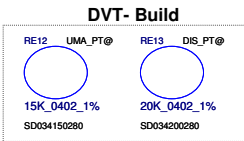
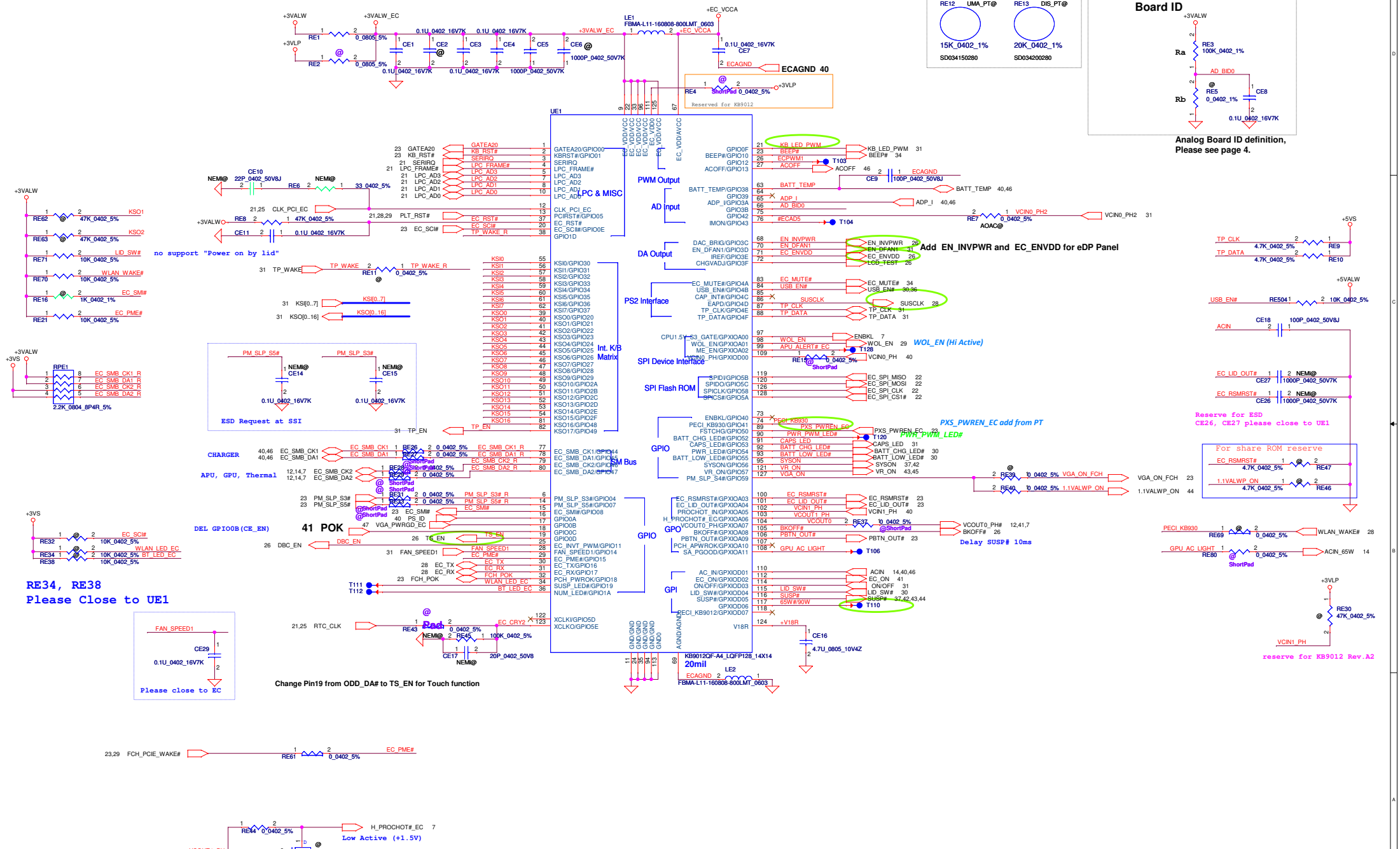


iPhone and Nokia type Combo Jack



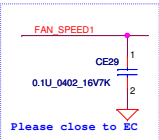
DA10 change P/N from SCA00002900 to SCA00001A00

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Issued Date	2013/10/01	Deciphered Date	2015/07/08	Title	Audio Codec ALC3234
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Analog Board ID definition, Please see page 4.

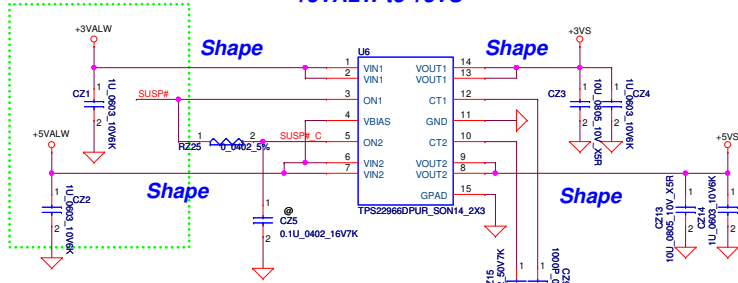
RE34, RE38
Please Close to UE1



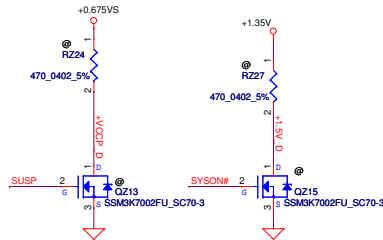
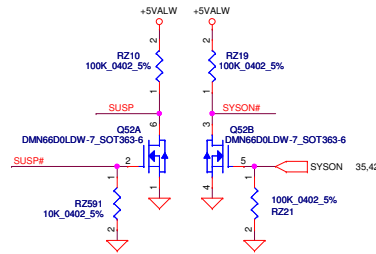
Change Pin19 from ODD_DA# to TS_EN for Touch function

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2012/09/11		2015/07/08		Document Number	
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				Date: Friday, March 07, 2014	
				Sheet: 35 of 50	

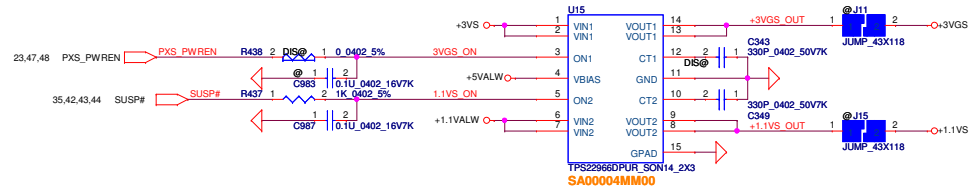
+5VALW to +5VS
+3VALW to +3VS
CZ3, CZ13 Change to H=0.85mm



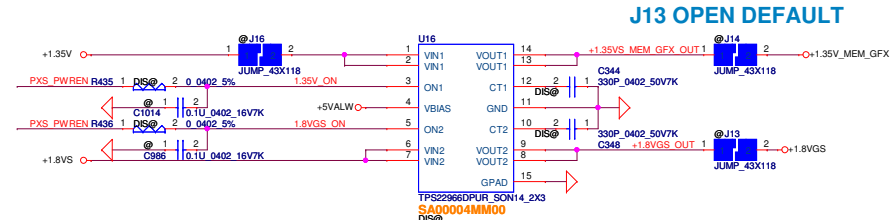
CTx (pF)	RISE TIME (µs)	
	5V	3.3V
0	124	88
220	481	323
470	855	603
1000	1724	1185
2200	3328	2240
4700	7459	4950
10000	16059	10835



+1.1VALW to +1.1VS
+3VS to +3VGS

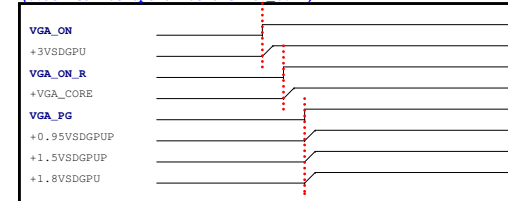


+1.35V to +1.35VS_MEM_GFX_OUT
+1.8VS to +1.8VSDGPU

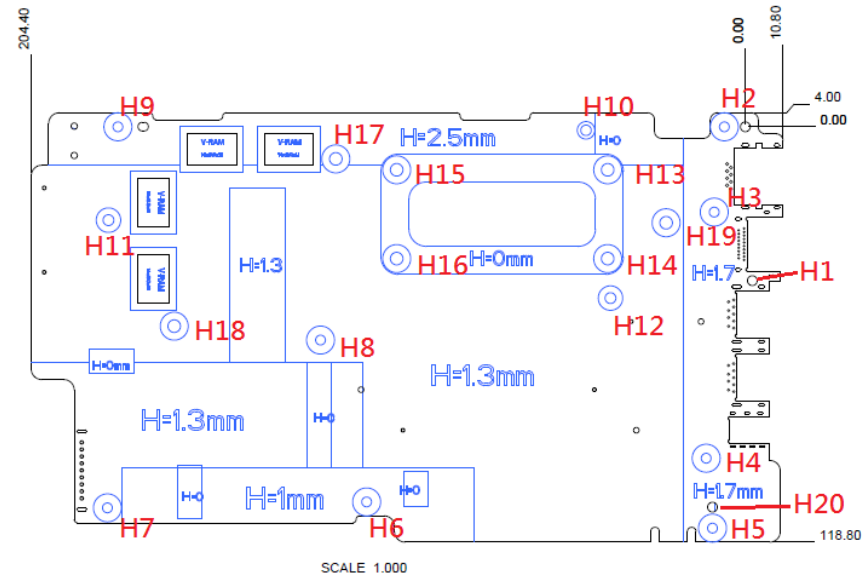
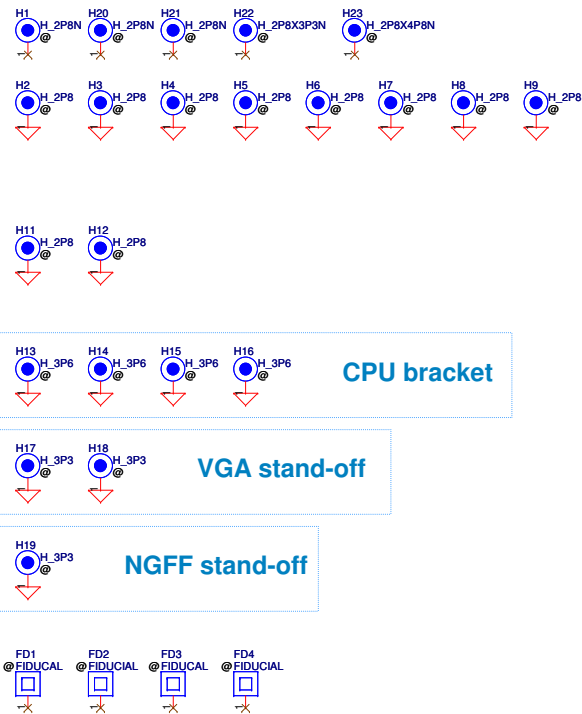


J13 OPEN DEFAULT

VGA sequence : default same as V5WE2
(0.95V can be option before VGA CORE)

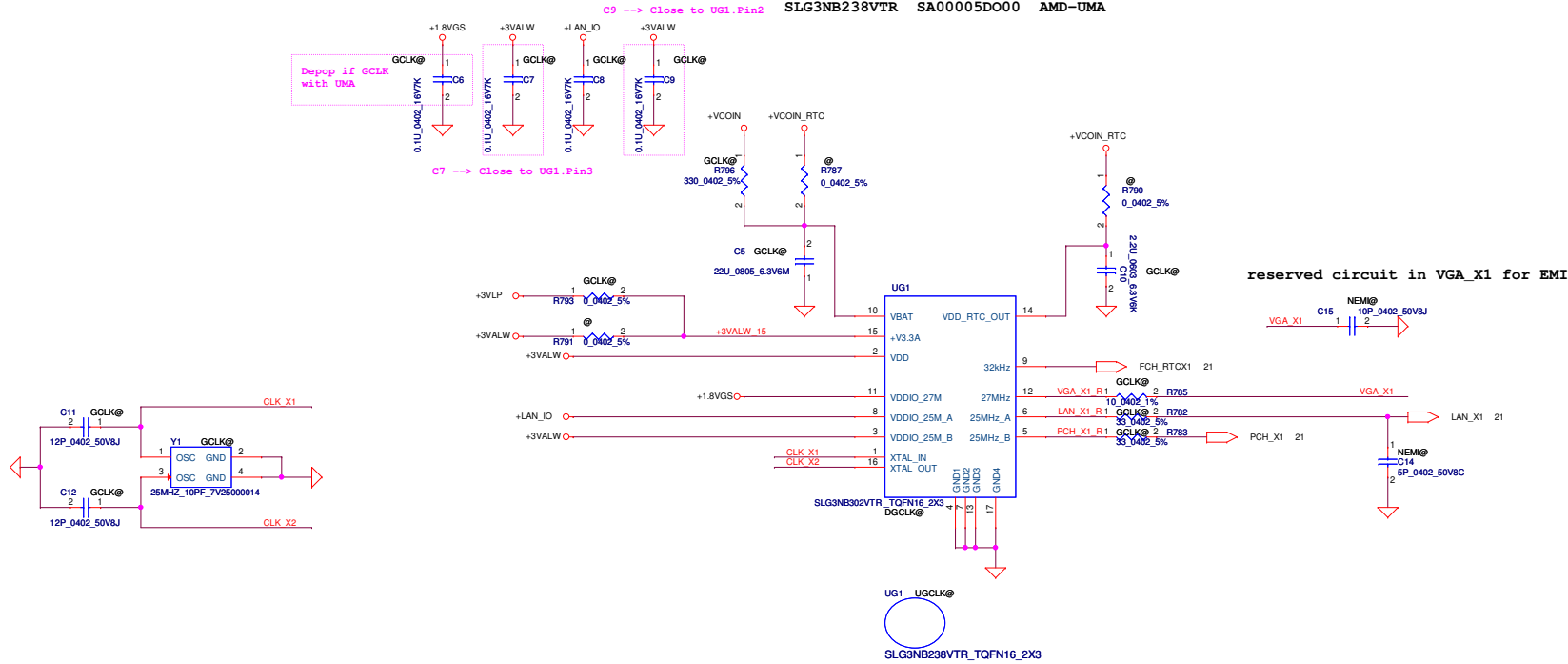


Screw Hole

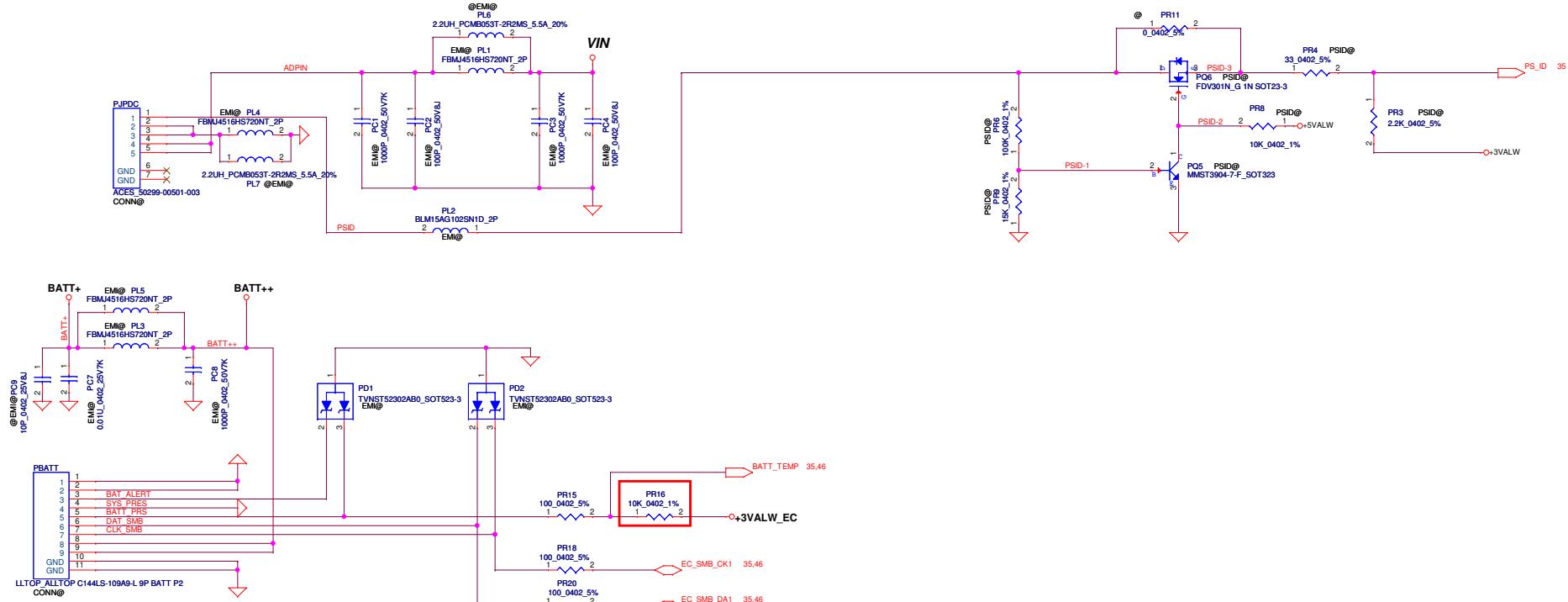


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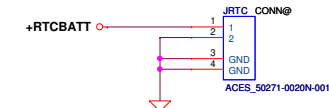
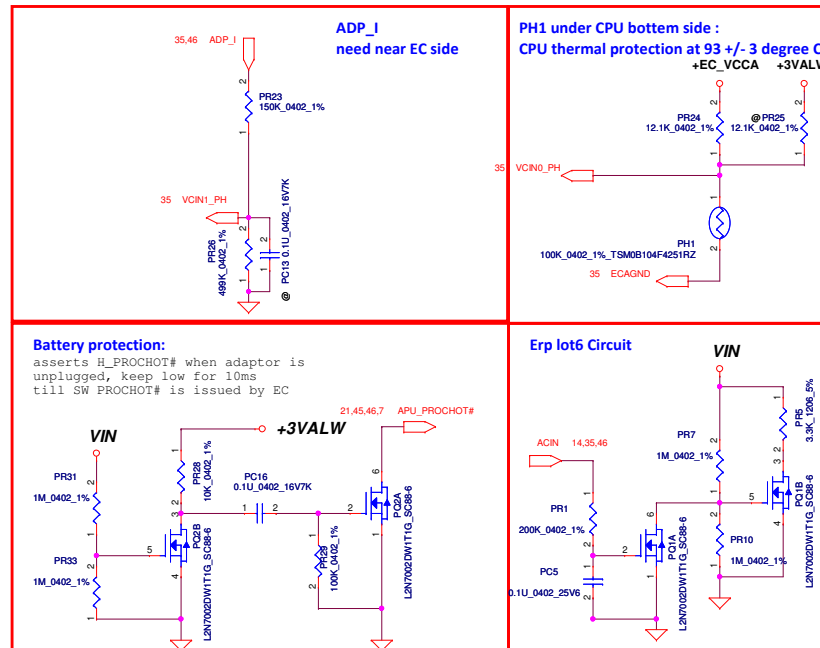
SLG3NB244VTR SA000057I00 Intel-UMA
SLG3NB300VTR SA00005RS00 Intel-DIS
SLG3NB302VTR SA00006D500 AMD-DIS
SLG3NB238VTR SA00005D000 AMD-UMA



**SMART
Battery:**
01.GND1
02.GND2
03.BAT_ALERT
04.SYS_PRES
05.BATT_PRS
06.DAT_SMB
07.CLK_SMB
08.BATT1 +
09.BATT2 +

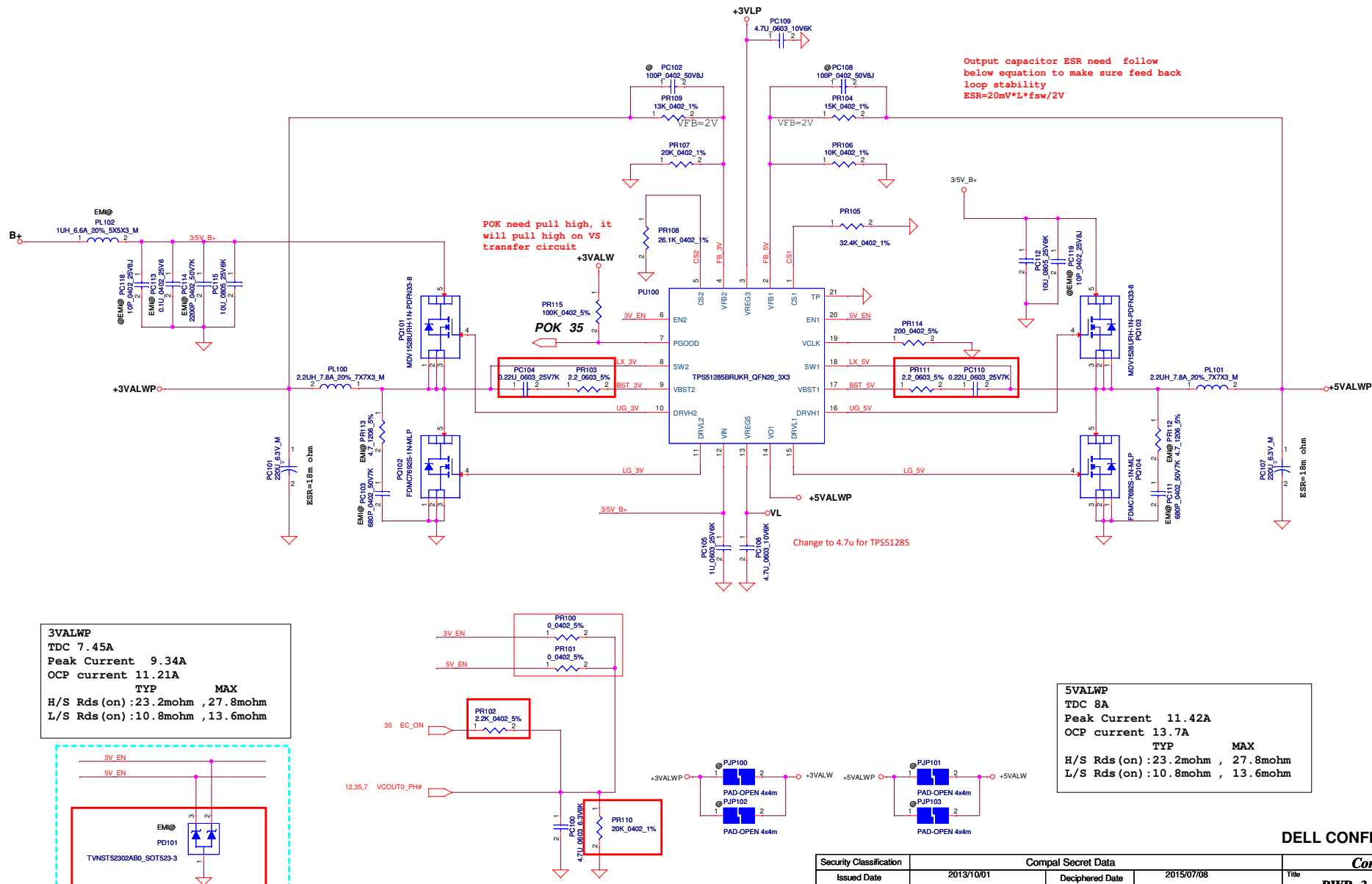


Other component (37.1)



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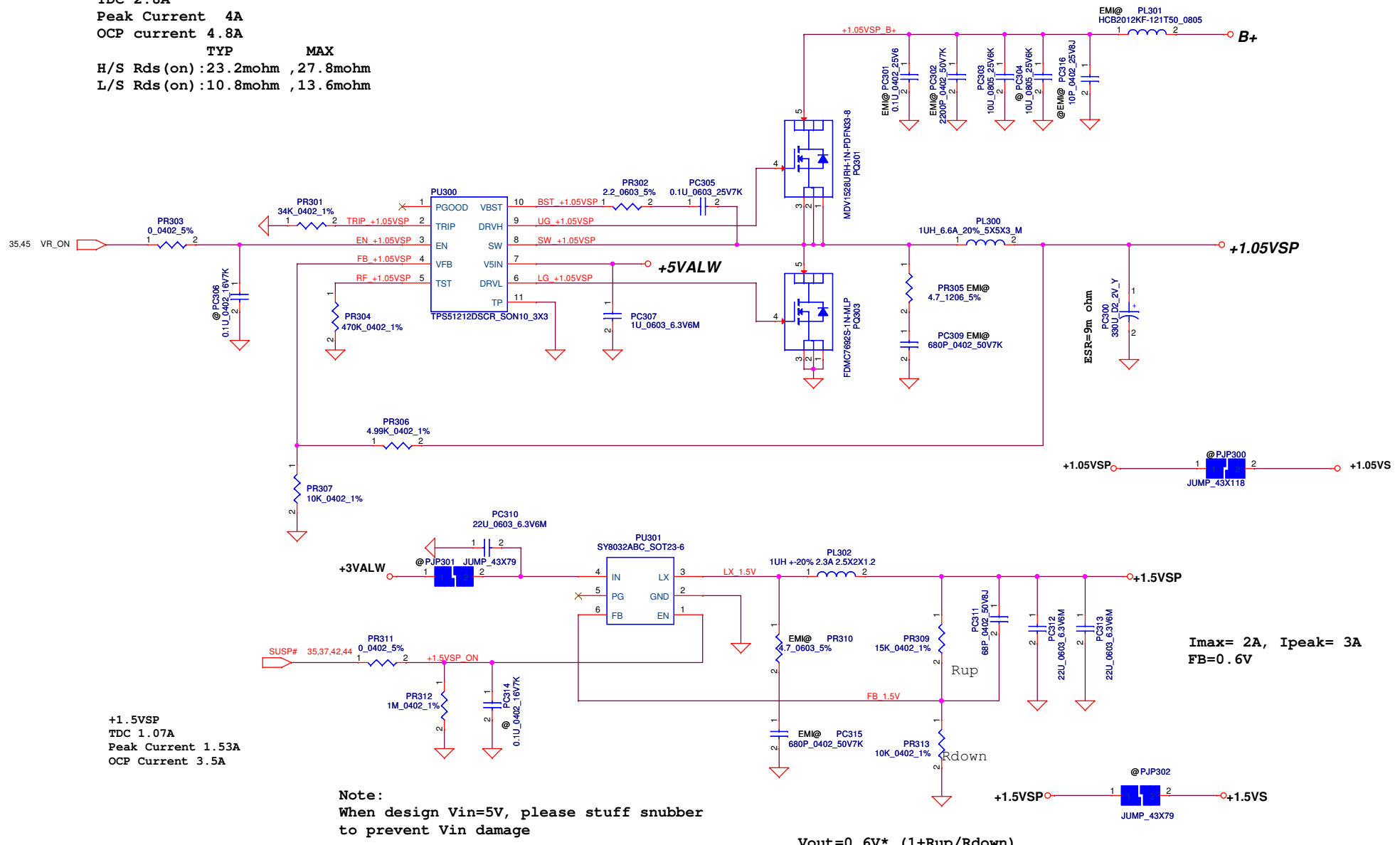


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1.05VSP
TDC 2.8A
Peak Current 4A
OCP current 4.8A

	TYP	MAX
H/S Rds (on)	:23.2mohm	,27.8mohm
L/S Rds (on)	:10.8mohm	,13.6mohm

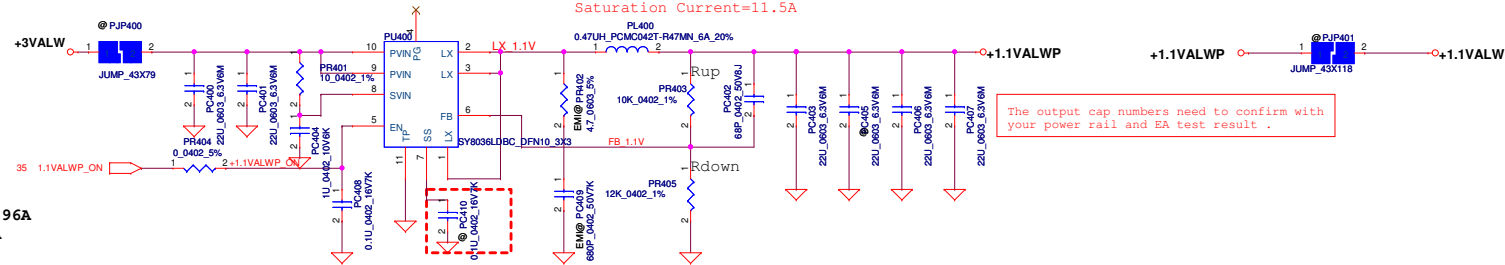


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Issued Date	2011/07/29	Deciphered Date		Title		
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FB=0.6V
Note:Iload(max)=6A

4*4 DCR 14~15.5mΩ
Heat Rating Current=6A
Saturation Current=11.5A



1.1VALWP
TDC 3.47A
Peak Current 4.96A
OCP current 7.5A

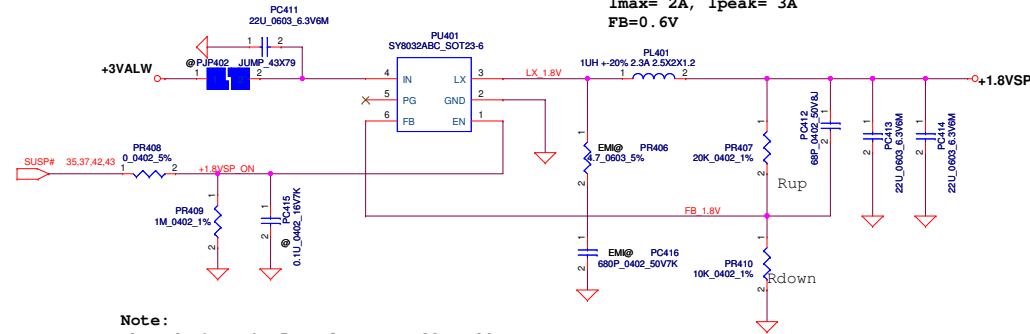
Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

PC7 to set the Soft Start Time:
CSS=100nF 6ms
Without CSS 0.6ms

$V_{out}=0.6V * (1+R_{up}/R_{down})$

Over voltage IC latch off protection threshold
min=115% type=120% max=125 %
Delay time 10us

Imax= 2A, Ipeak= 3A
FB=0.6V



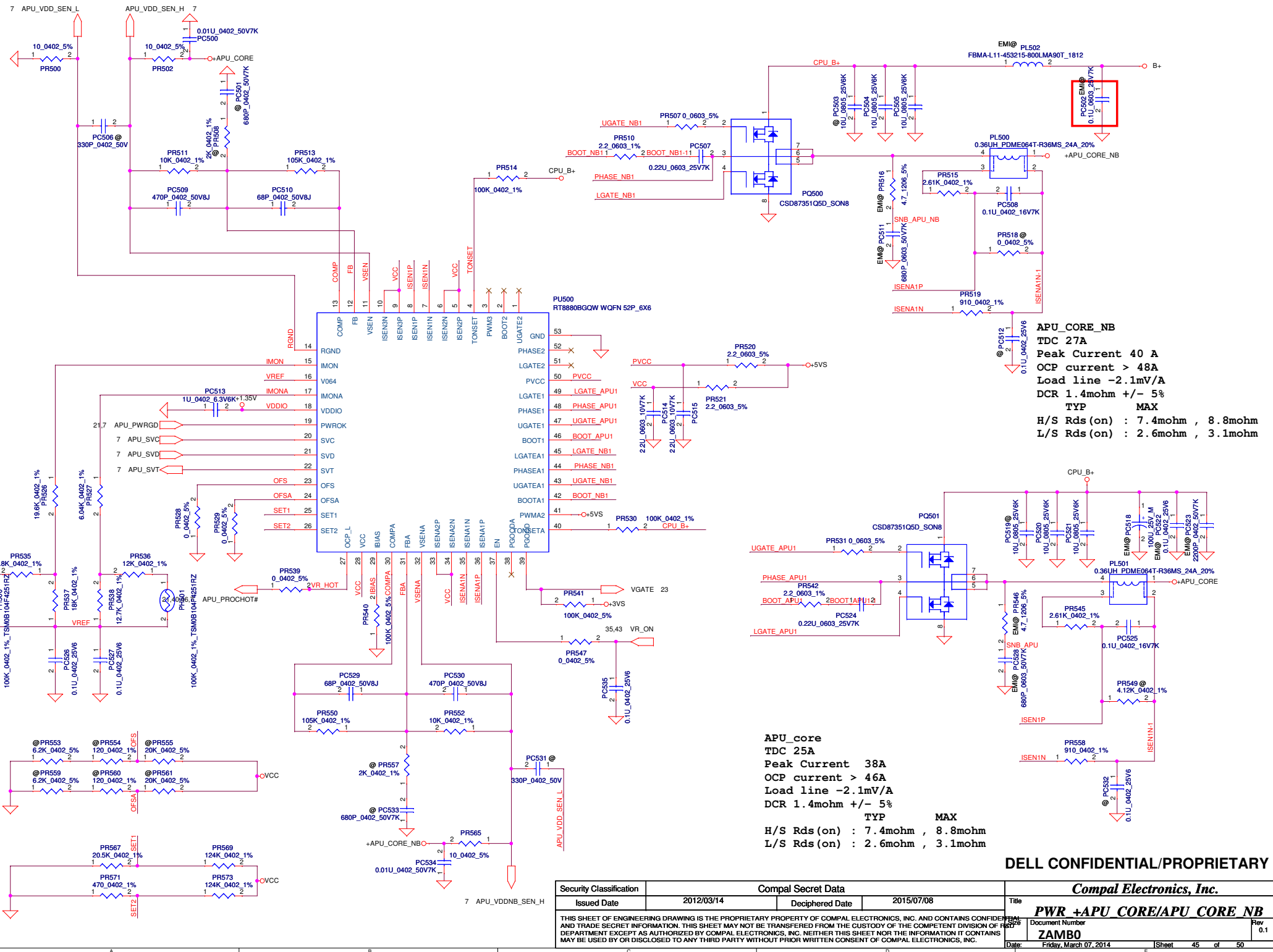
+1.8VSP
TDC 1.34A
Peak Current 1.92A
OCP Current 3.5A

Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

$V_{out}=0.6V * (1+R_{up}/R_{down})$

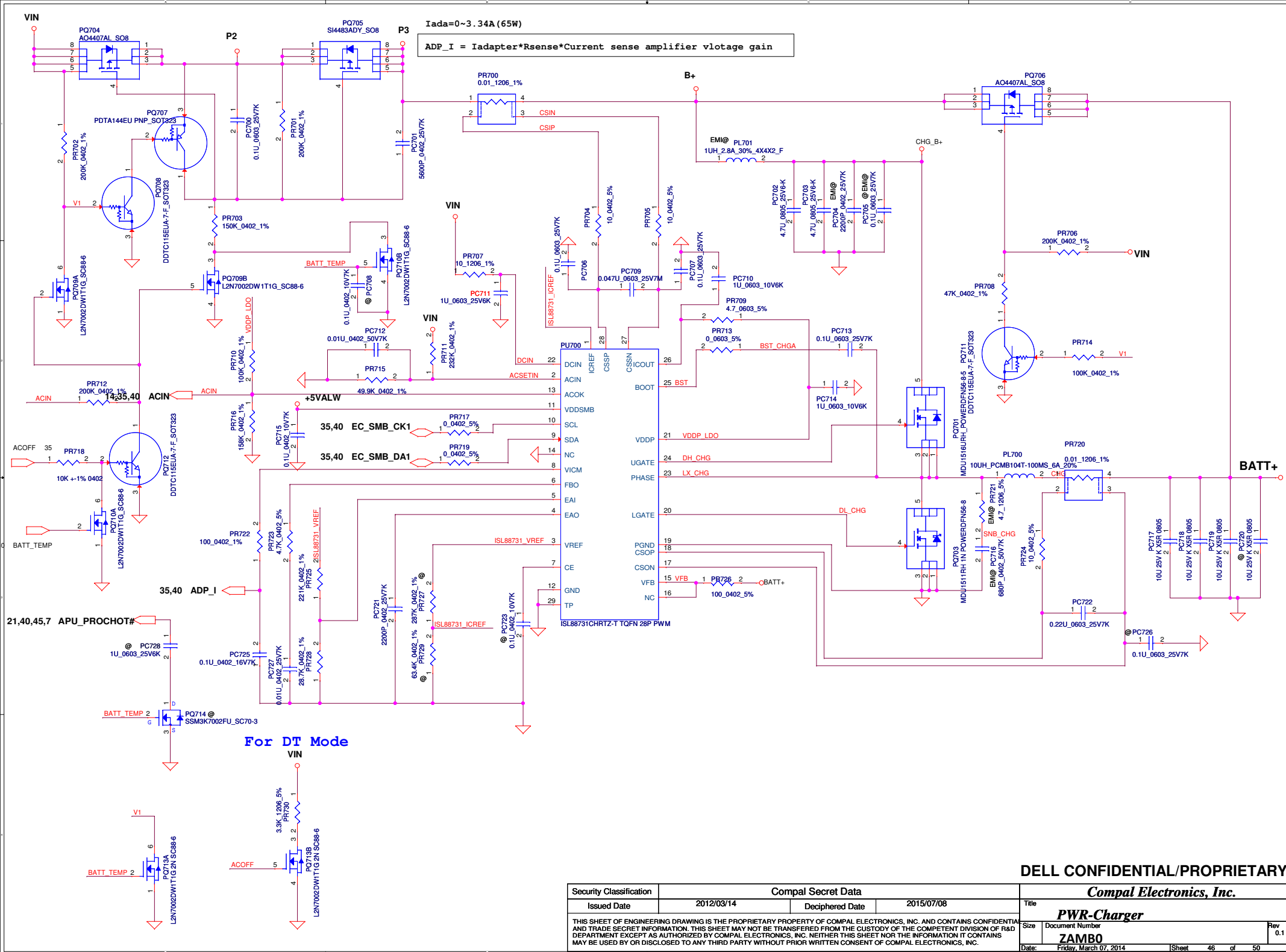
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				ZAMBO	0.1
				Date	Friday, March 07, 2014
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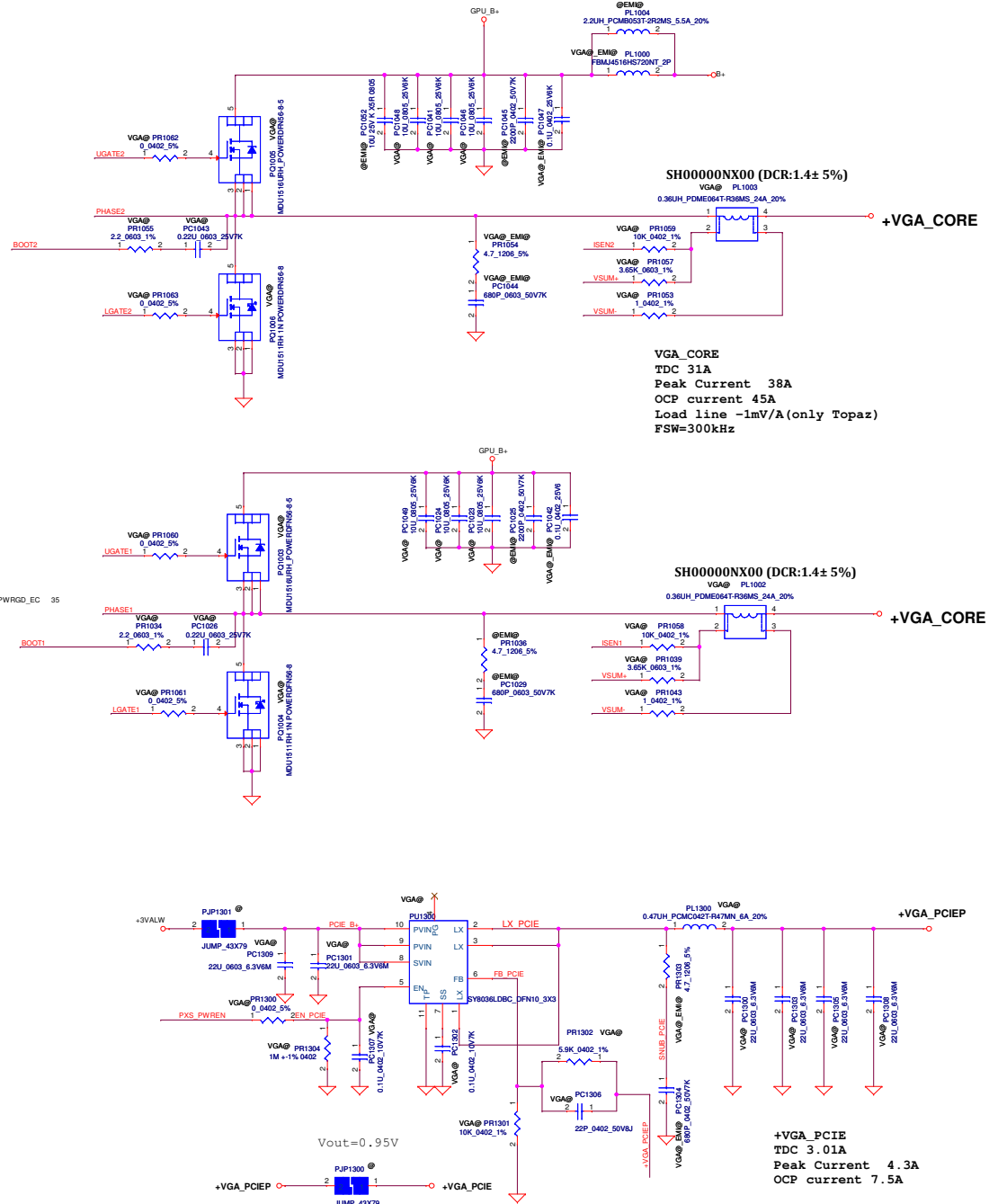
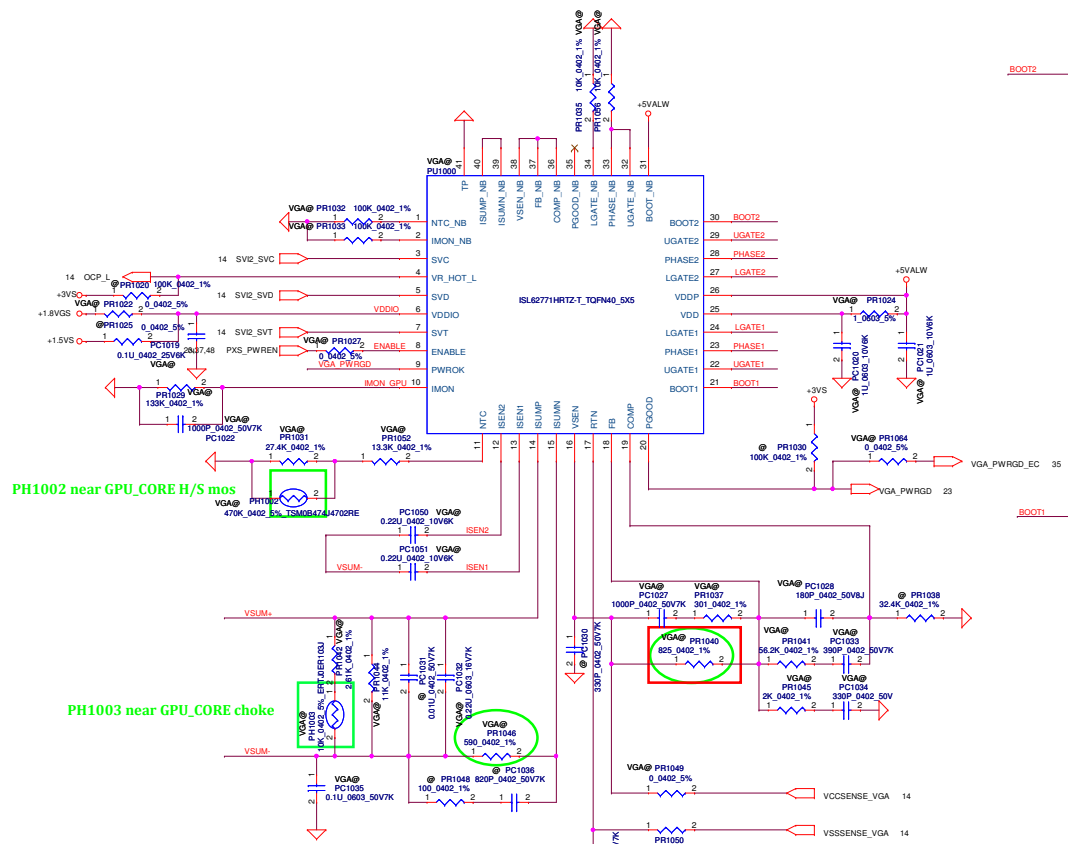
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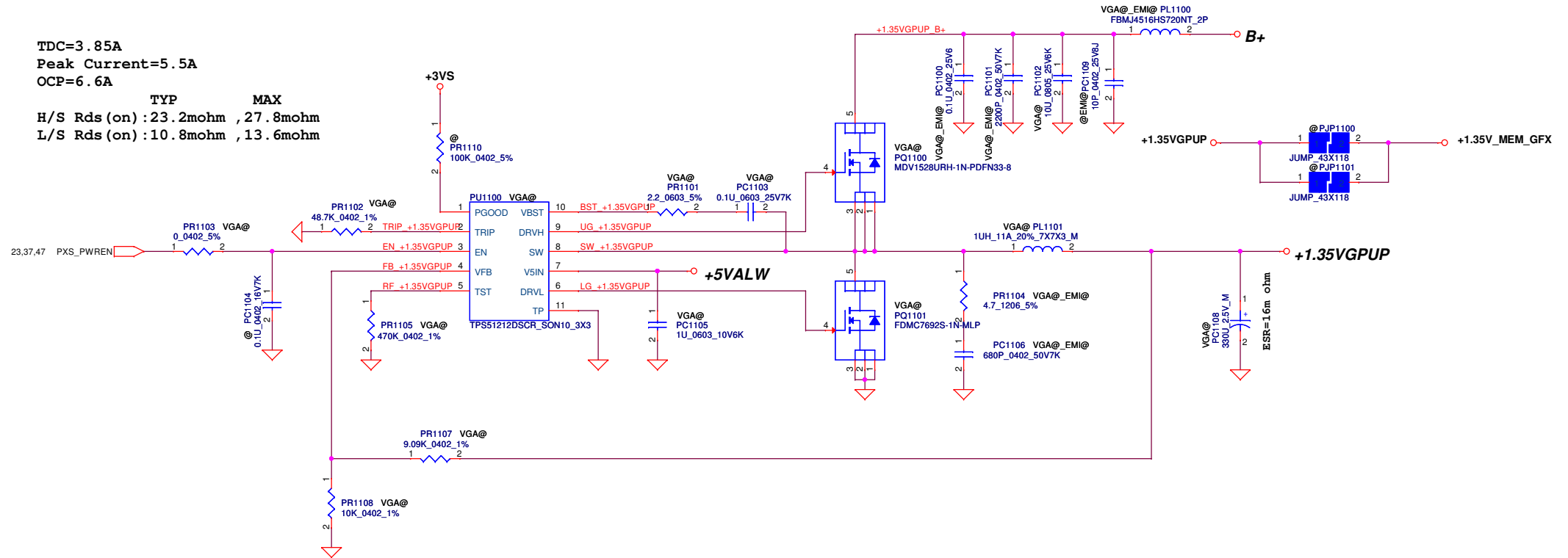


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TDC=3.85A
Peak Current=5.5A
OCP=6.6A

TYP MAX
H/S Rds (on) : 23.2mohm , 27.8mohm
L/S Rds (on) : 10.8mohm , 13.6mohm



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		ZAMBO			0.1
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+APU_CORE

APU_CORE
330uF*3
22uF*13+0.22uF*2
0.01uF*3+180pF*3

+APU_CORE

+APU_CORE_NB

+APU_CORE_NB

APU_CORENB
330uF*3
22uF*12+0.22uF*3
180pF*4

+VGA_CORE

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