

Compal Confidential

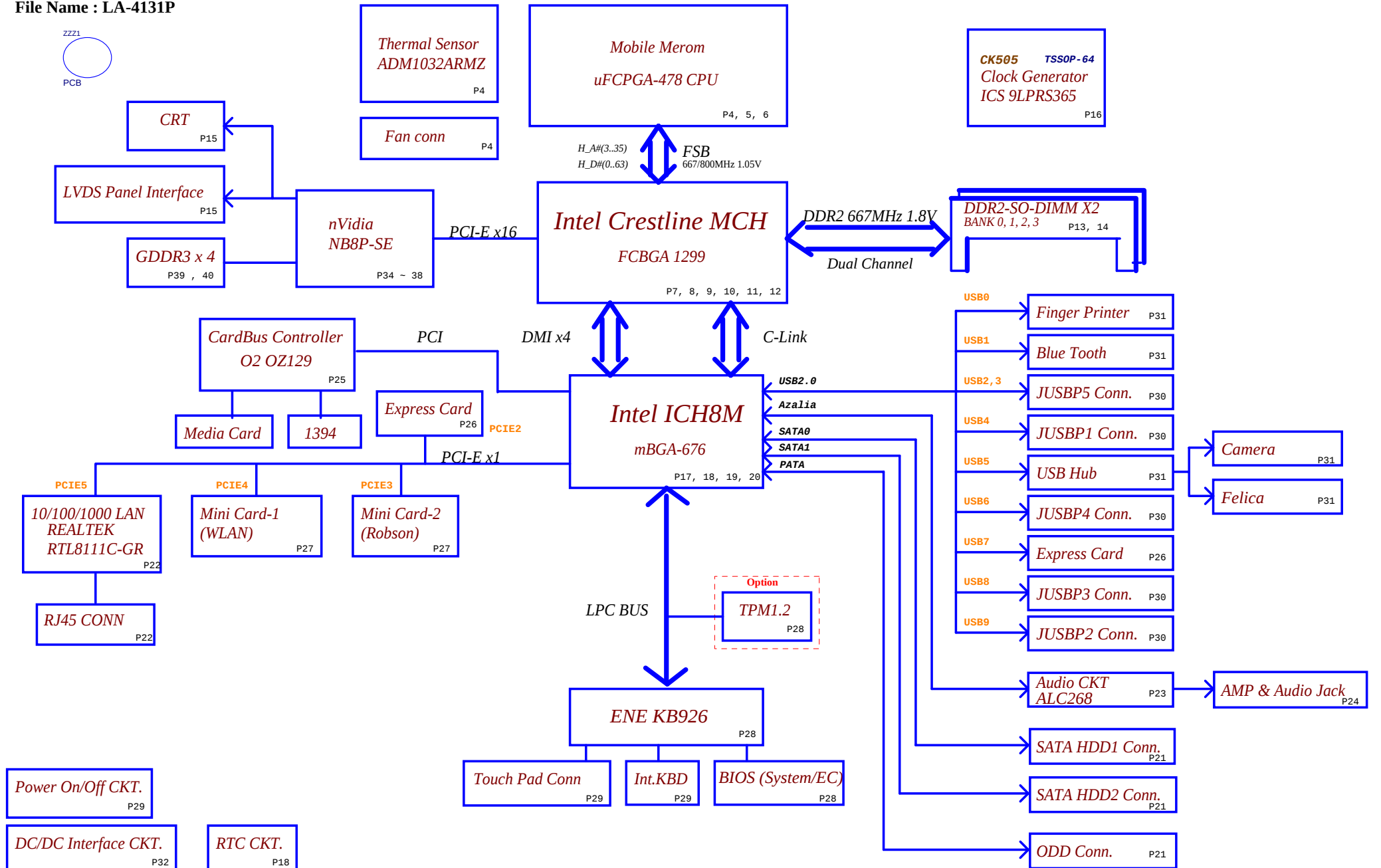
Schematic Document

Crestline + ICH8M

2008 / 02 / 18 Rev:0.3

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2007/12/28	Deciphered Date	2007/12/28	Title	Cover Sheet	
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				Date: Monday, February 18, 2008		

JAL60 UMA / Discrete



0 MEANS ON X MEANS OFF

State \ Power plane	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.8VS +1.5VS +1.25VS +1.2VS +0.9VS +CPU_CORE +VGA_CORE +VCCP	CLOCK
S0	0	0	0	0	0
S3	0	0	0	X	0
S5 S4/AC	0	0	X	X	0
S5 S4/ Battery only	0	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

X MEANS OFF

S5 : S0FT OFF

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD21	0	PIRQ

Device	Address	Device	Address
Smart Battery	0001 011X b?	EMC1402-1-ACZL-TR_MSOP8	4C for CPU Thermal Sensor
EEPROM(24C16/02)	1010 000X b?		
(24C04)	1011 000Xb?		

Device	Address
Clock Generator (ICS ICS9LPR365)	1101 001Xb?
DDRII DIMM1	1001 000Xb?
DDRII DIMM2	1001 010Xb?

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

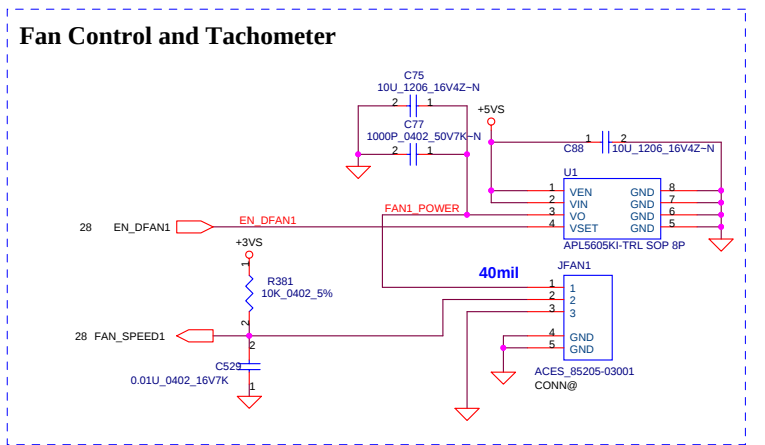
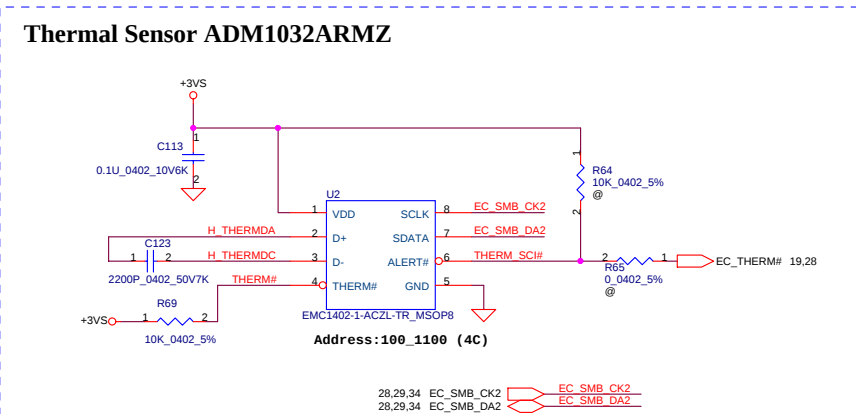
Vcc	3.3V +/- 5%
Ra / Rc	100K +/- 5%

Board ID	Rb / Rd	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

[illegible]

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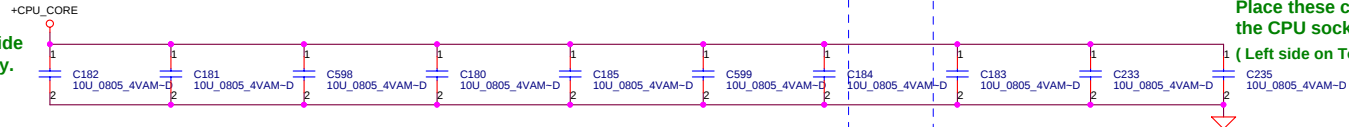


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A4	JP1D	VSS[001]	P6
A8	VSS[002]	VSS[082]	P21
A11	VSS[003]	VSS[083]	P24
A14	VSS[004]	VSS[084]	P5
A16	VSS[005]	VSS[085]	R22
A19	VSS[006]	VSS[086]	R25
A23	VSS[007]	VSS[087]	T1
A27	VSS[008]	VSS[088]	T4
B6	VSS[009]	VSS[089]	T23
B8	VSS[010]	VSS[090]	T26
B11	VSS[011]	VSS[091]	U3
B12	VSS[012]	VSS[092]	U6
B16	VSS[013]	VSS[093]	U21
B19	VSS[014]	VSS[094]	U24
B21	VSS[015]	VSS[095]	V2
B24	VSS[016]	VSS[096]	V5
C5	VSS[017]	VSS[097]	V22
C8	VSS[018]	VSS[098]	V25
C11	VSS[019]	VSS[099]	W1
C14	VSS[020]	VSS[100]	W4
C16	VSS[021]	VSS[101]	W23
C19	VSS[022]	VSS[102]	W26
C2	VSS[023]	VSS[103]	Y3
C22	VSS[024]	VSS[104]	Y6
C25	VSS[025]	VSS[105]	Y21
D1	VSS[026]	VSS[106]	Y24
D4	VSS[027]	VSS[107]	AA2
D8	VSS[028]	VSS[108]	AA5
D11	VSS[029]	VSS[109]	AA8
D13	VSS[030]	VSS[110]	AA11
D16	VSS[031]	VSS[111]	AA14
D19	VSS[032]	VSS[112]	AA16
D23	VSS[033]	VSS[113]	AA19
D26	VSS[034]	VSS[114]	AA22
E3	VSS[035]	VSS[115]	AA25
E6	VSS[036]	VSS[116]	AB1
E8	VSS[037]	VSS[117]	AB4
F11	VSS[038]	VSS[118]	AB8
F14	VSS[039]	VSS[119]	AB11
F16	VSS[040]	VSS[120]	AB13
F19	VSS[041]	VSS[121]	AB16
F21	VSS[042]	VSS[122]	AB19
F24	VSS[043]	VSS[123]	AB23
F5	VSS[044]	VSS[124]	AB26
F8	VSS[045]	VSS[125]	AC3
F11	VSS[046]	VSS[126]	AC6
F13	VSS[047]	VSS[127]	AC8
F16	VSS[048]	VSS[128]	AC11
F19	VSS[049]	VSS[129]	AC14
F2	VSS[050]	VSS[130]	AC16
F22	VSS[051]	VSS[131]	AC19
F25	VSS[052]	VSS[132]	AC21
G4	VSS[053]	VSS[133]	AC24
G1	VSS[054]	VSS[134]	AD2
G23	VSS[055]	VSS[135]	AD5
G26	VSS[056]	VSS[136]	AD8
H3	VSS[057]	VSS[137]	AD11
H6	VSS[058]	VSS[138]	AD13
H21	VSS[059]	VSS[139]	AD16
H24	VSS[060]	VSS[140]	AD19
J2	VSS[061]	VSS[141]	AD22
J5	VSS[062]	VSS[142]	AD25
J22	VSS[063]	VSS[143]	AE1
J25	VSS[064]	VSS[144]	AE4
K1	VSS[065]	VSS[145]	AE8
K4	VSS[066]	VSS[146]	AE11
K23	VSS[067]	VSS[147]	AE14
K26	VSS[068]	VSS[148]	AE16
L3	VSS[069]	VSS[149]	AE19
L6	VSS[070]	VSS[150]	AE23
L21	VSS[071]	VSS[151]	AE26
L24	VSS[072]	VSS[152]	A2
M2	VSS[073]	VSS[153]	AF6
M5	VSS[074]	VSS[154]	AF8
M22	VSS[075]	VSS[155]	AF11
M25	VSS[076]	VSS[156]	AF13
N1	VSS[077]	VSS[157]	AF16
N4	VSS[078]	VSS[158]	AF19
N23	VSS[079]	VSS[159]	AE21
N26	VSS[080]	VSS[160]	A25
P3	VSS[081]	VSS[161]	AF25
		VSS[162]	
		VSS[163]	

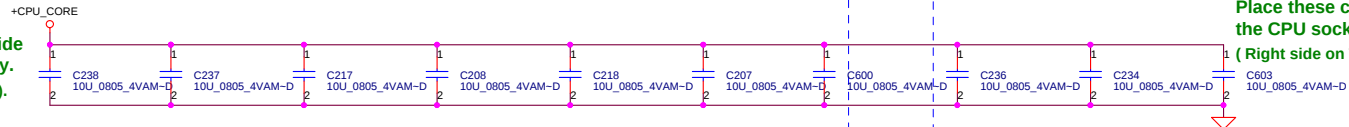
High Frequency Decoupling 10uF 0805 X5R -> 85 degree.

Place these caps inside
the CPU socket cavity.
(Left side on Top).



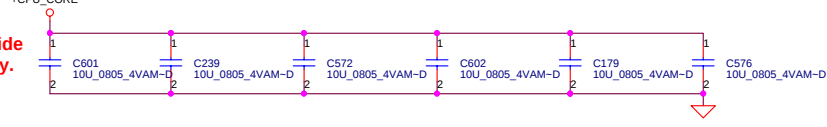
Place these caps inside
the CPU socket.
(Left side on Top).

Place these caps inside
the CPU socket cavity.
(Right side on Top side).

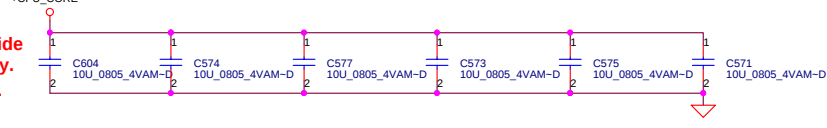


Place these caps inside
the CPU socket.
(Right side on Top).

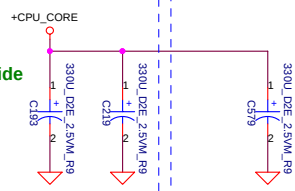
Place these caps inside
the CPU socket cavity.
(Left side on Bottom).



Place these caps inside
the CPU socket cavity.
(Right side on Bottom).

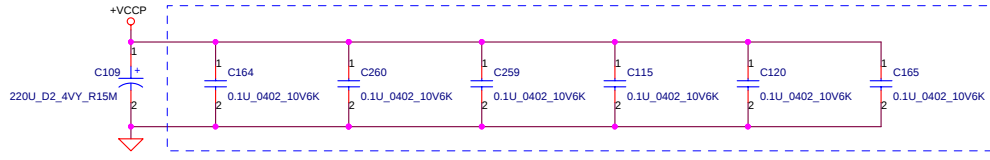


Place these caps inside
the CPU socket.
(Left side on Top).



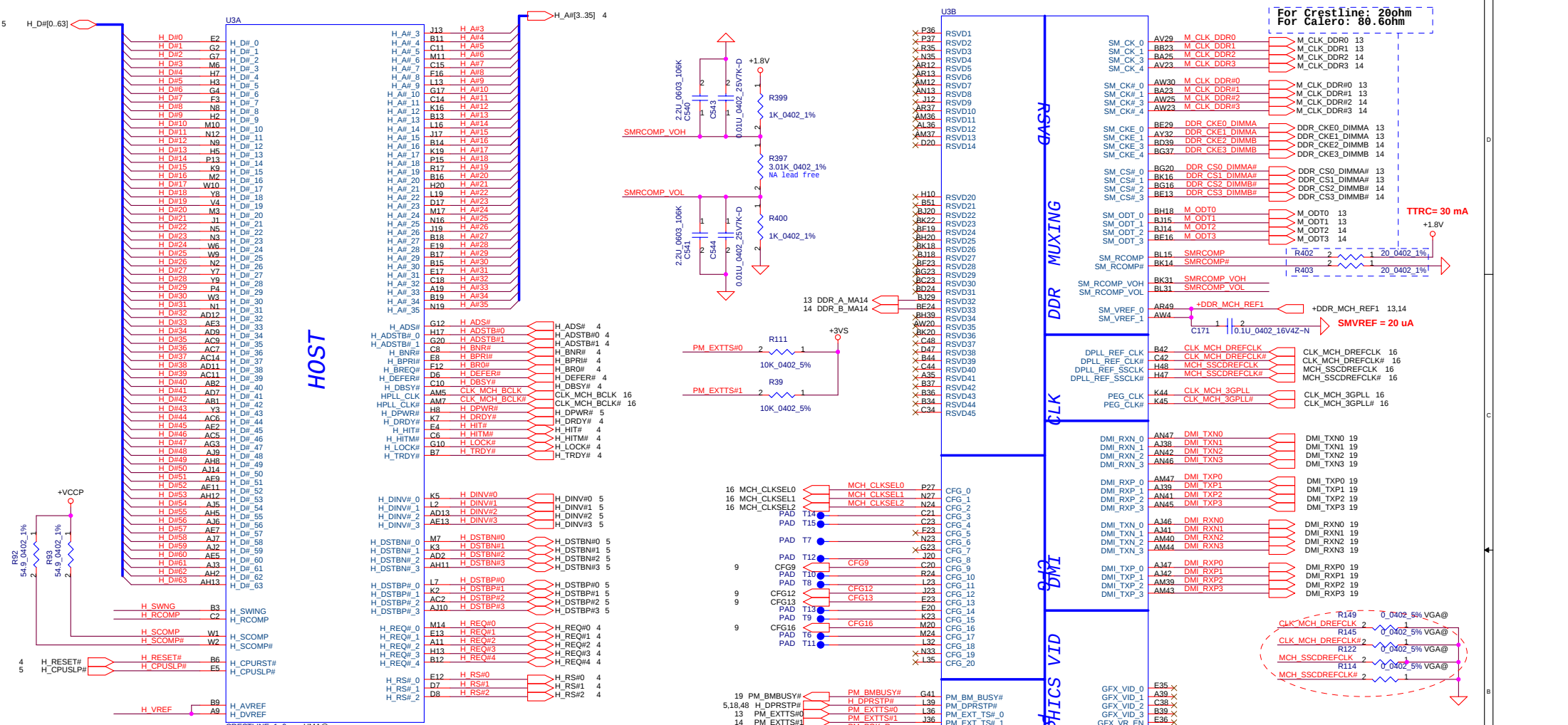
Place these caps inside
the CPU socket.
(Right side on Top side).

ESR <= 1.5m ohm
Capacitor > 880 uF

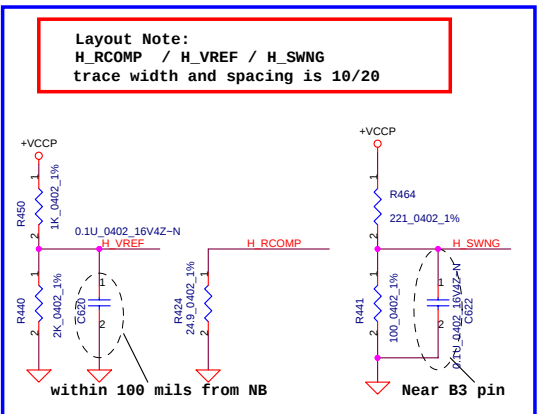


Place these inside
socket cavity on L8
(North side
Secondary)

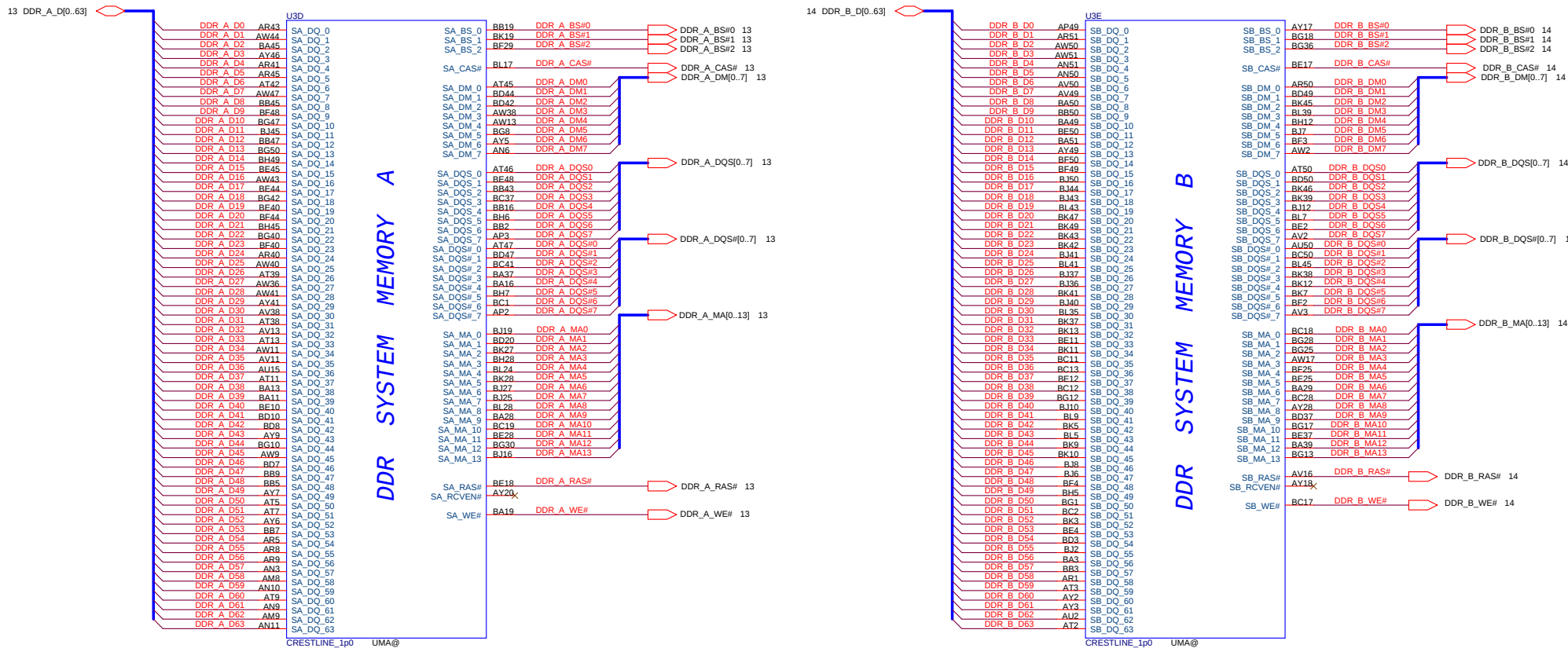
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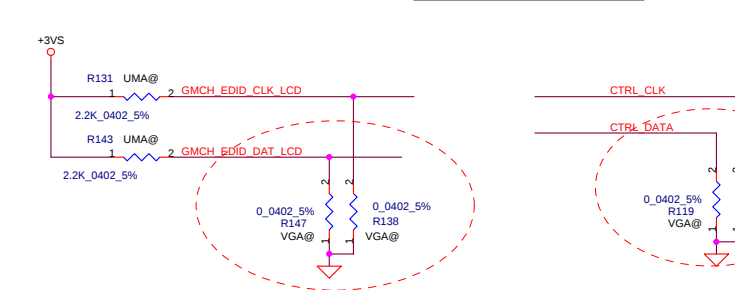
layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces.



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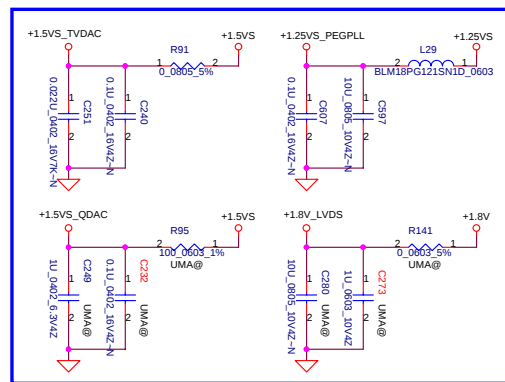
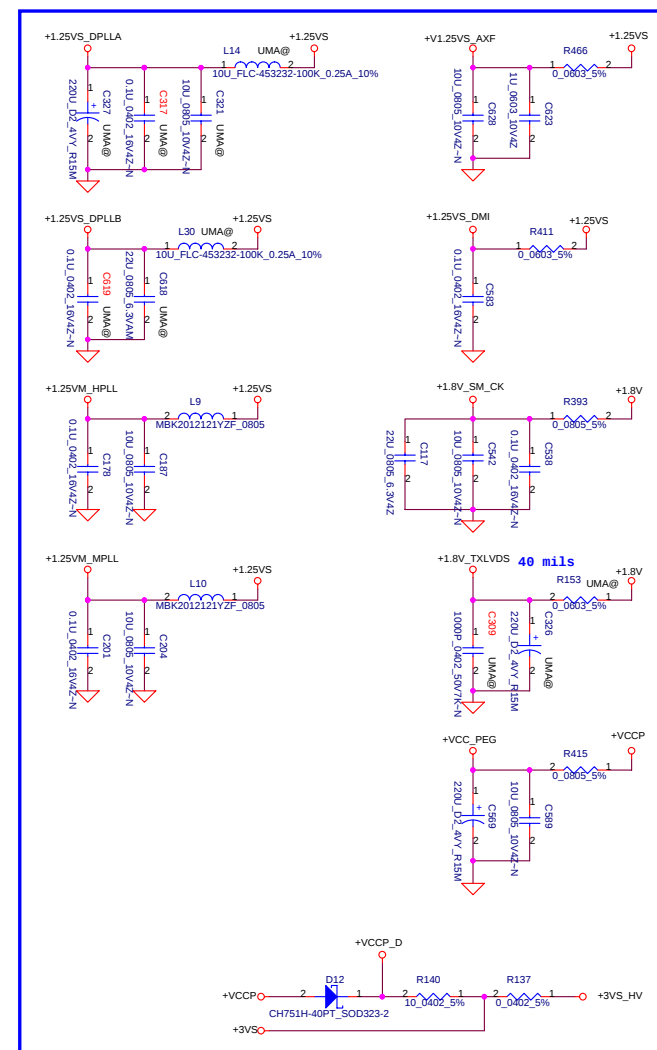


15 BIA_PWM
28 GMCH_ENBK
+3VS 
15 GMCH_EDID_CLK_L0
15 GMCH_EDID_DAT_L0
15,28 GMCH_LVDD0



CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

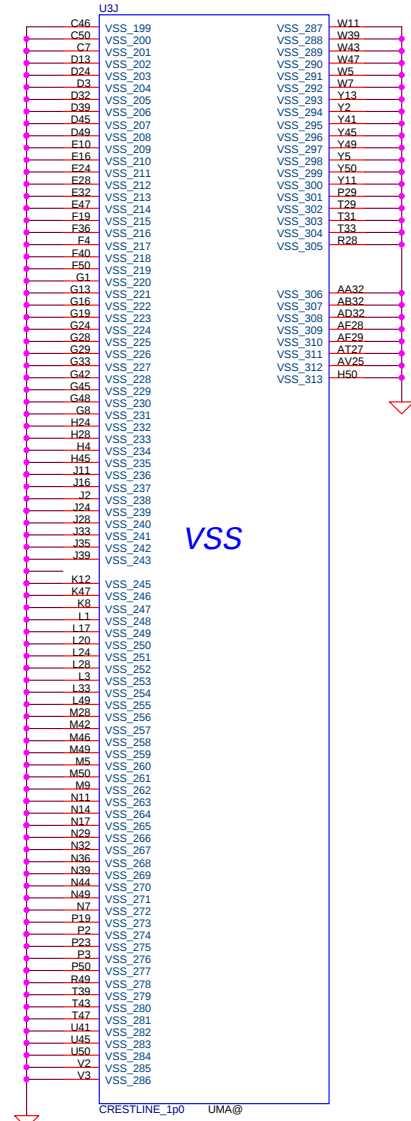
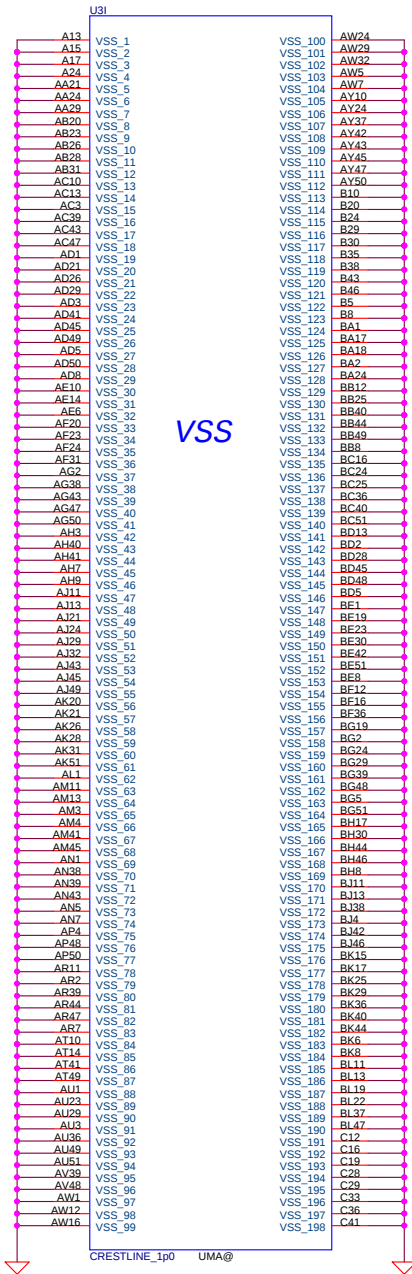
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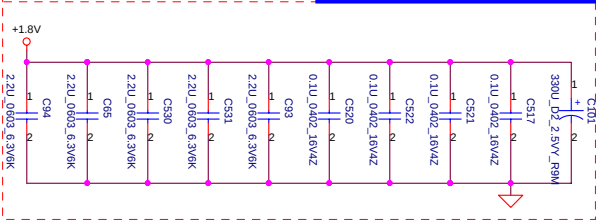
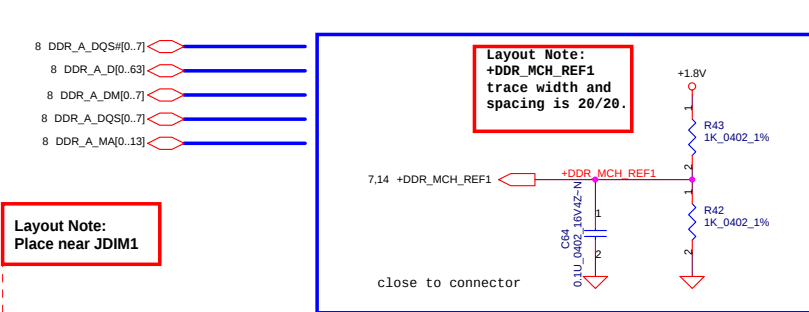
For Discrete BOM

C633	C627	C621	C273	C619	U3
					
0 0402_5%	0 0402_5%	0 0402_5%	0 0603_5%	0 0402_5%	PM965 C0
VGA@	VGA@	VGA@	VGA@	VGA@	VGA@
C632	C629	C232	C309	C250	C317
					
0 0402_5%	0 0402_5%	0 0402_5%	0 0402_5%	0 0402_5%	0 0402_5%
VGA@	VGA@	VGA@	VGA@	VGA@	VGA@

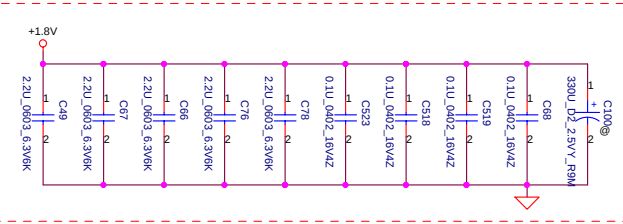
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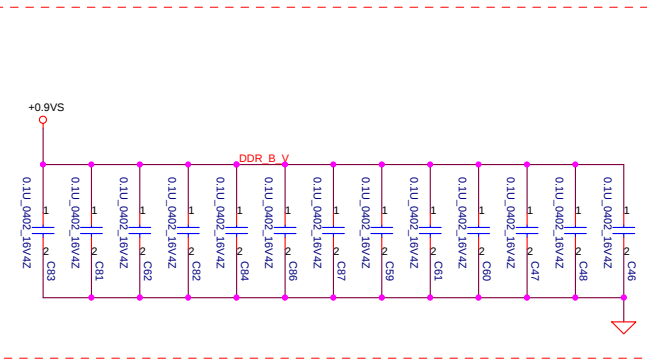
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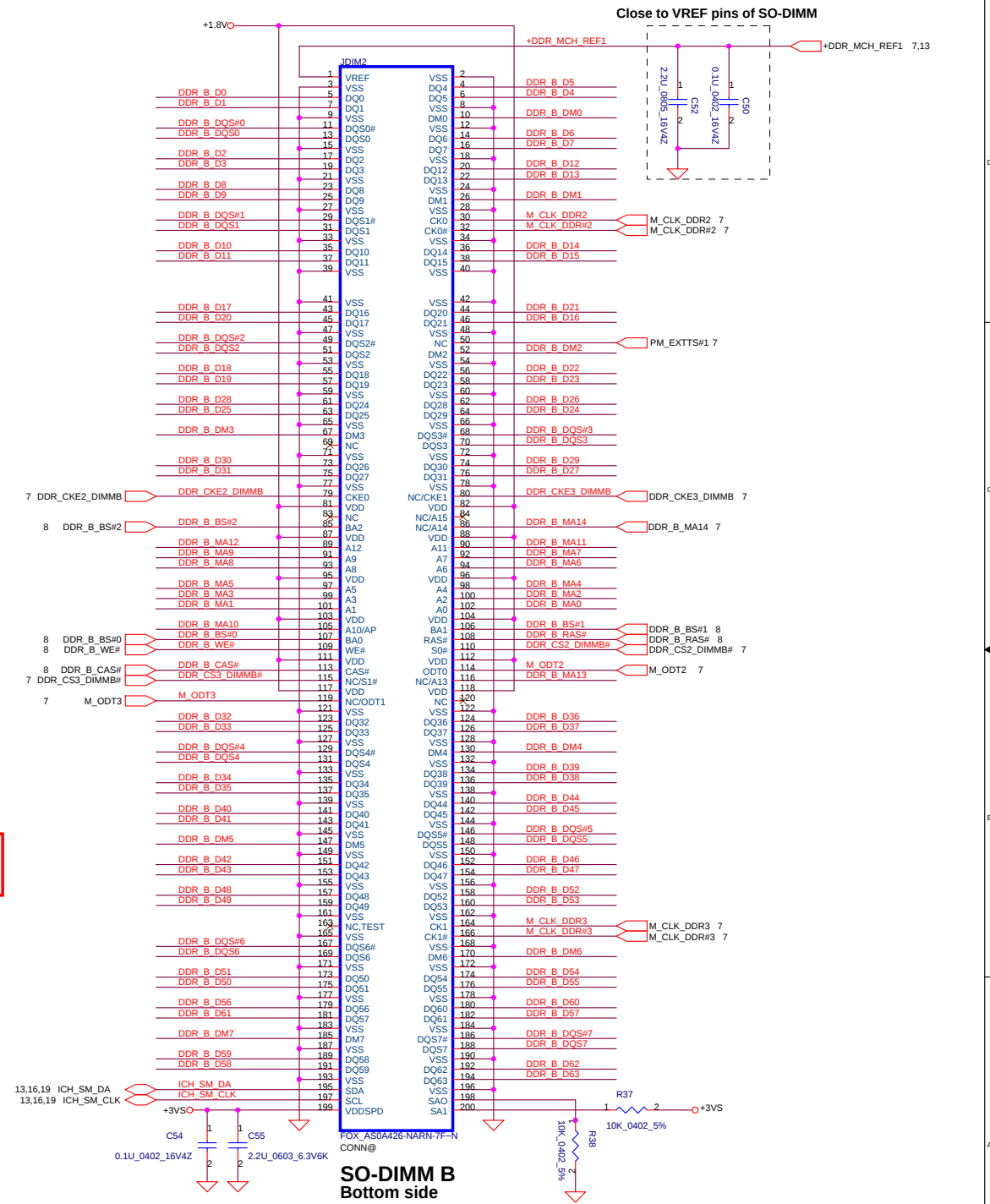
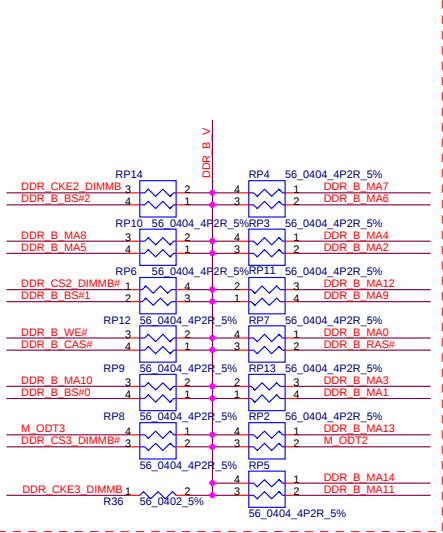
Layout Note:
Place near JDIM2



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS

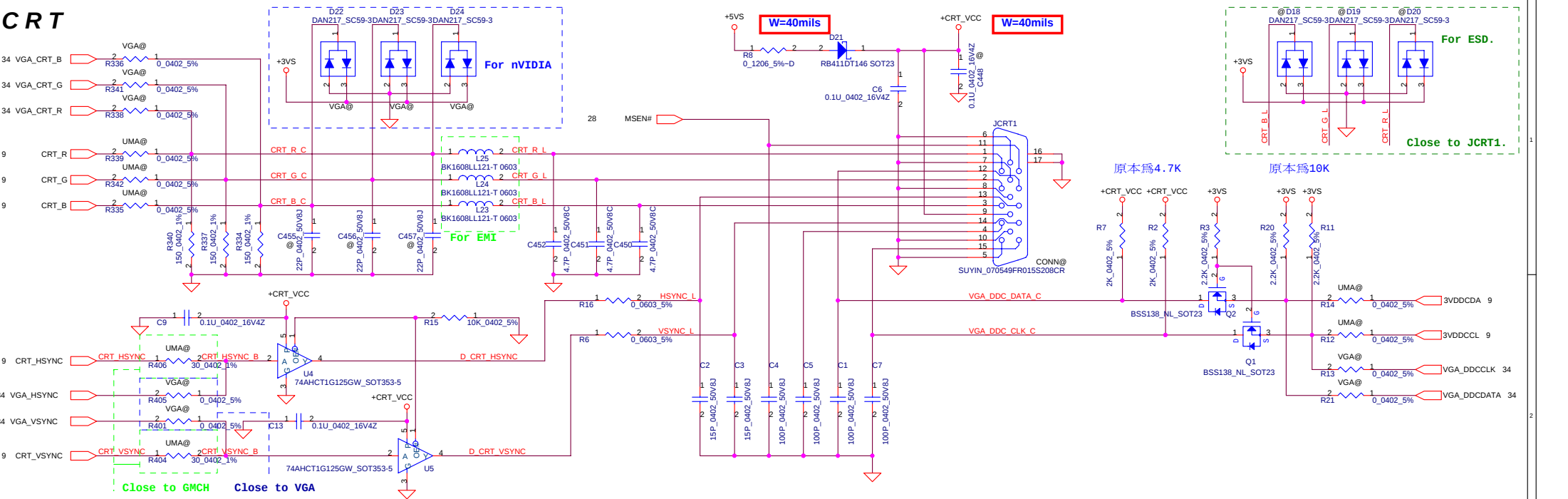


Layout Note:
Place these resistor
closely JDIM2,
all trace length Max=1.5"

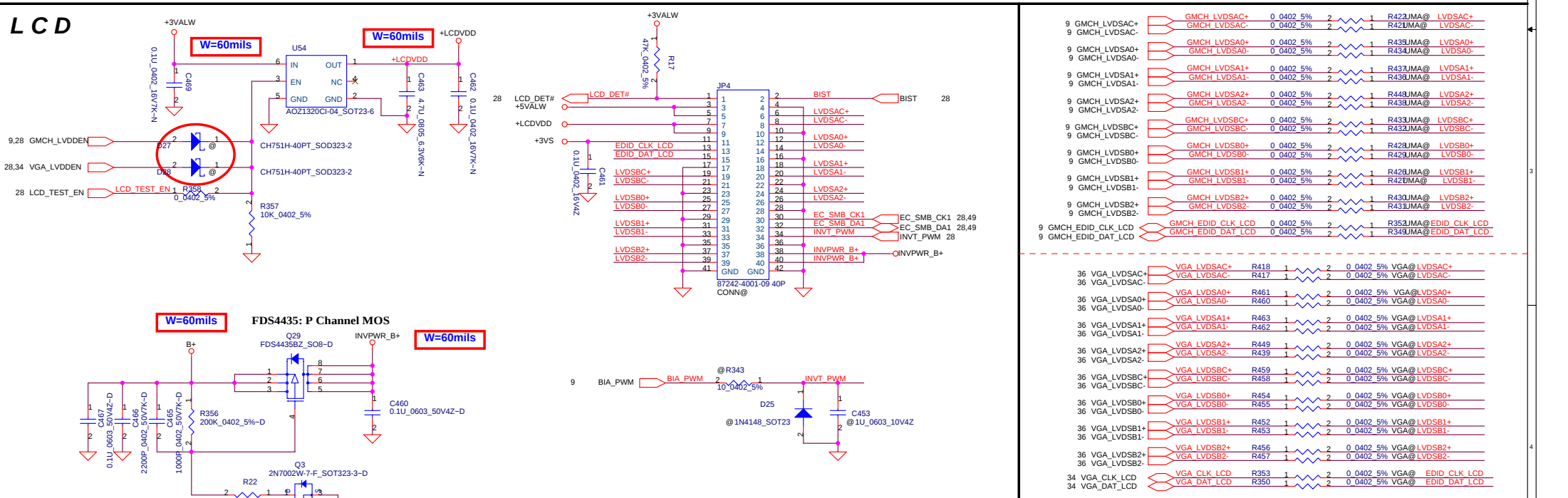


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CRT



LCD

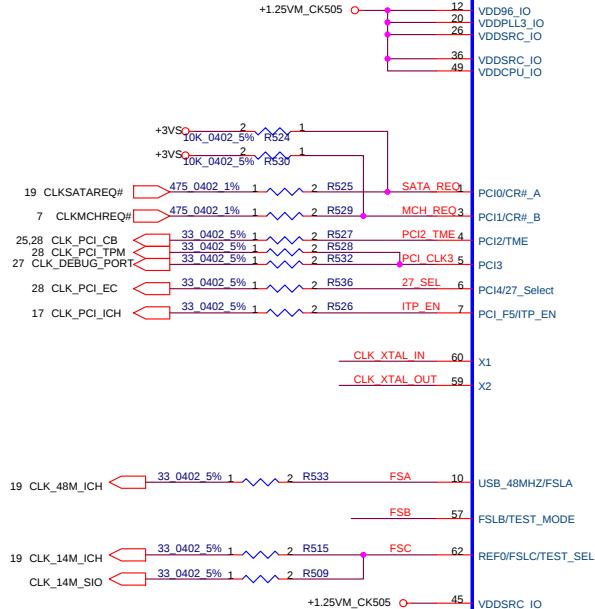
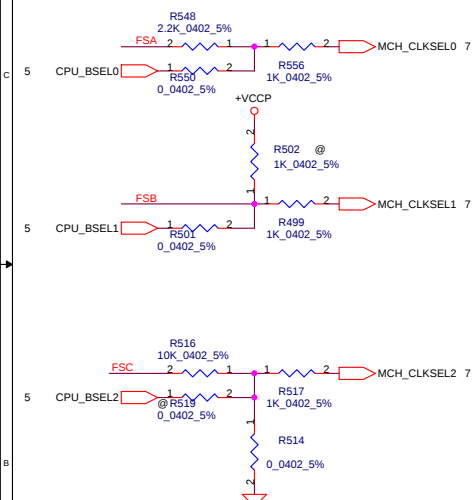


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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHZ	SRC MHZ	PCI MHZ
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Set:

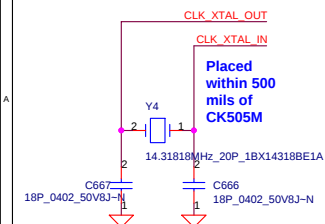
CPU Driven	Stuff	R1107	R1135	R1083				
*(Default)	No Stuff	R1074	R1086	R1098	R1113	R1128	R1139	
667MHz	Stuff	R1086	R1139	R1135	R1074	R1139	R1135	
	No Stuff	R1083	R1107	R1128				
800MHz	Stuff	R1135	R1139					
	No Stuff	R1083	R1086	R1098	R1128			



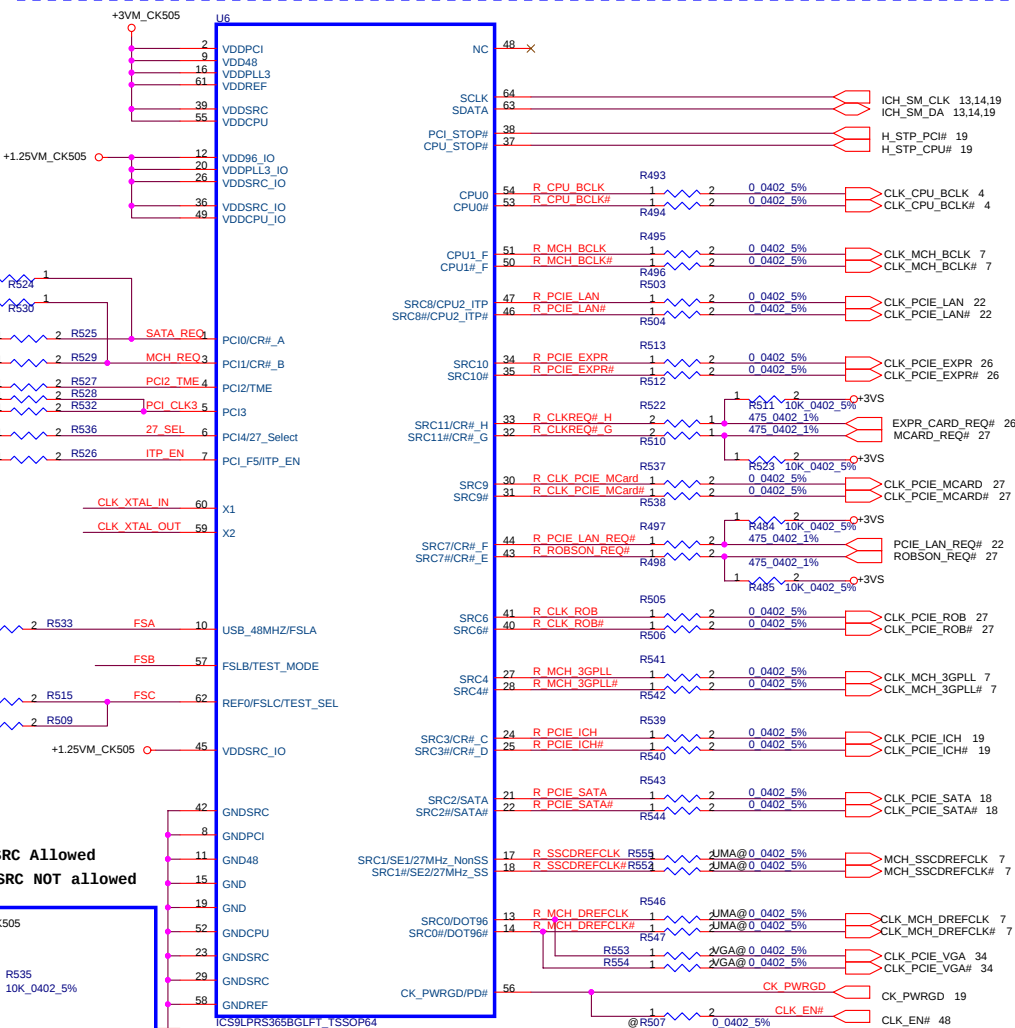
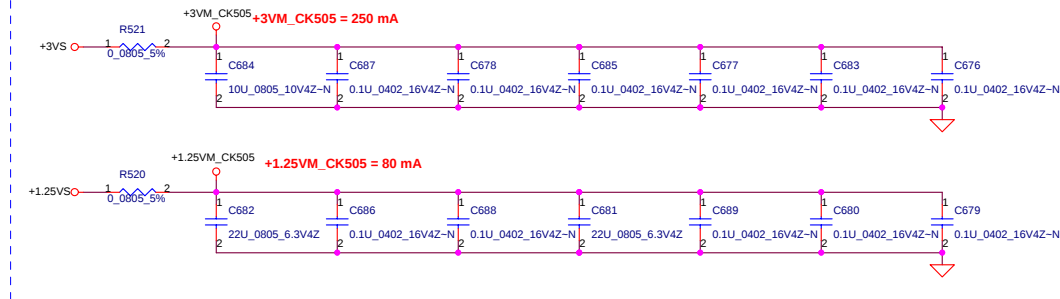
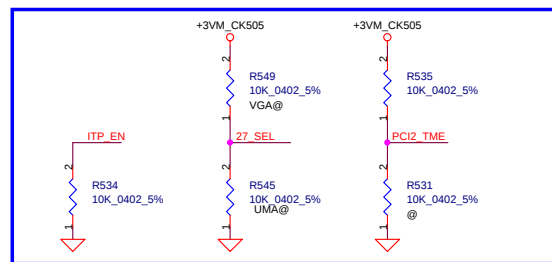
For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#

For 27_SEL, 0 = Enable DOT96 & SRC1,
1 = Enable SRC0 & 27MHz

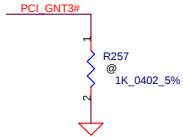
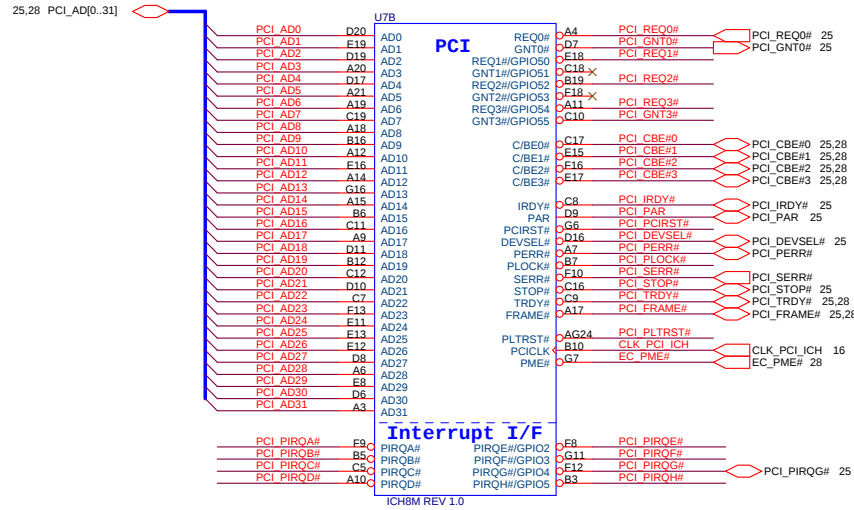
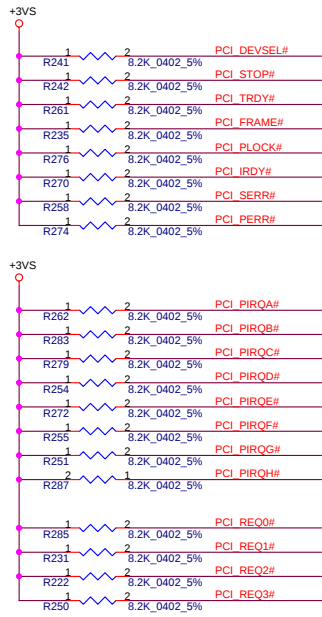
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed



Routing the trace at least 10mil

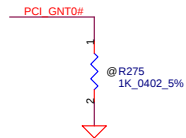


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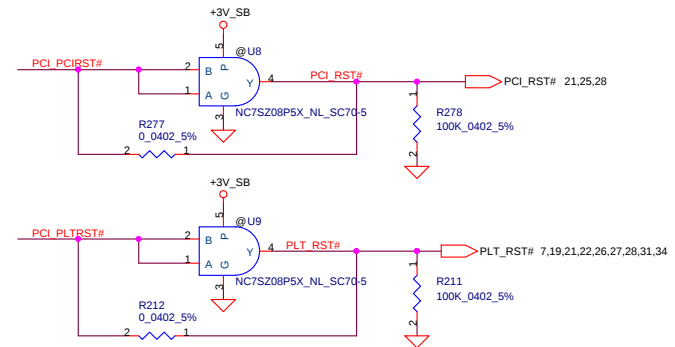
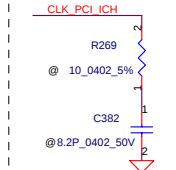
Check if use LPC

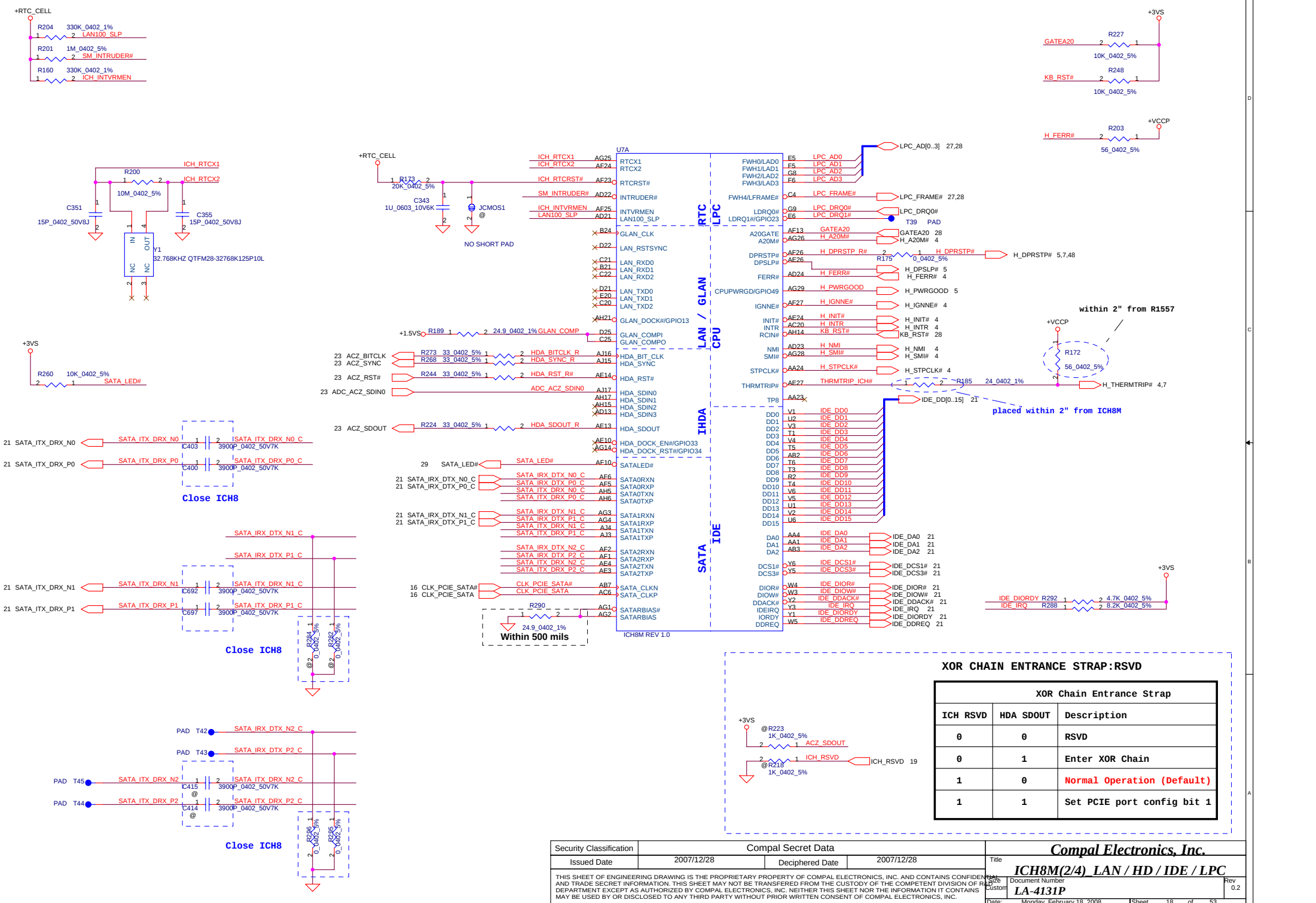
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



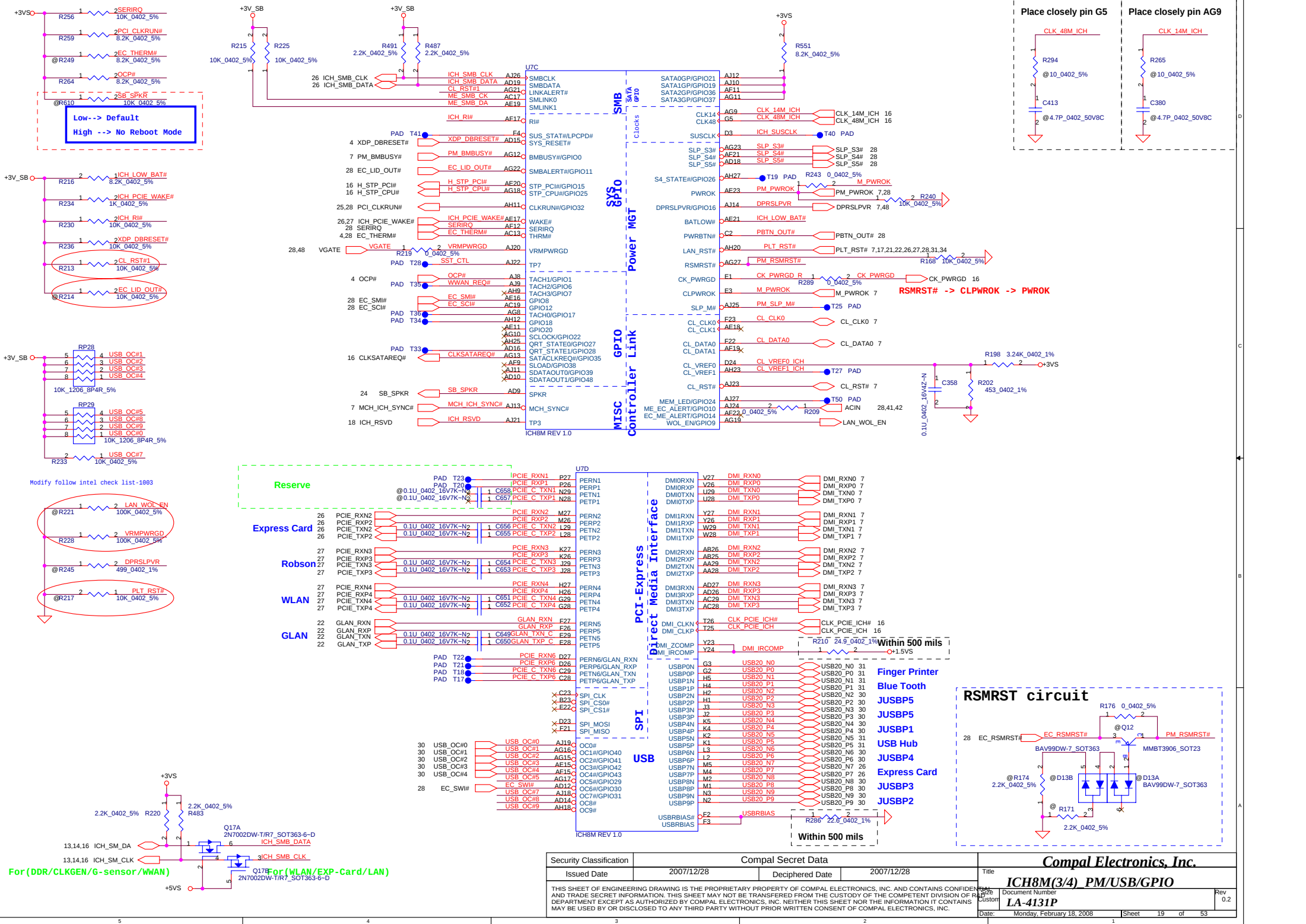
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*

Place closely pin B10



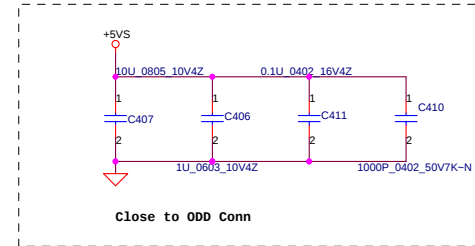
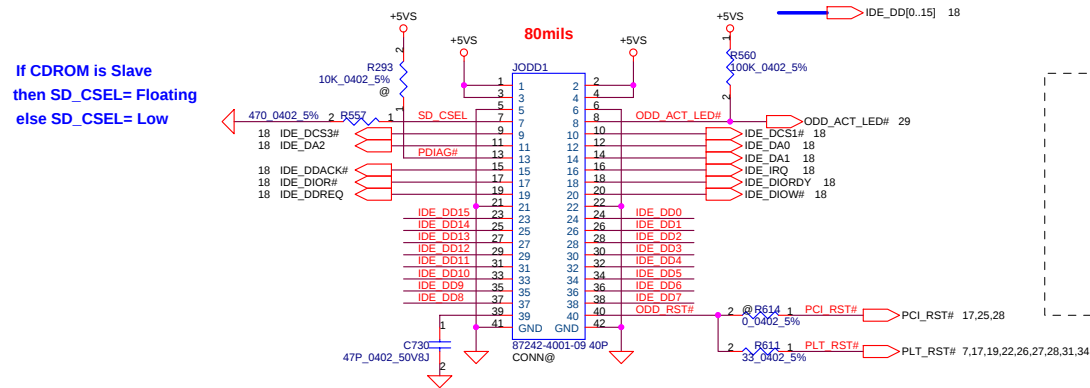


XOR Chain Entrance Strap:RSVD		
XOR Chain Entrance Strap		
ICH RSVD	HDA SDOOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

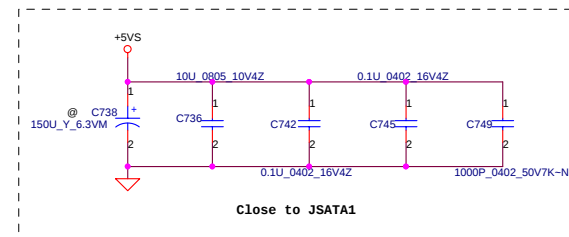
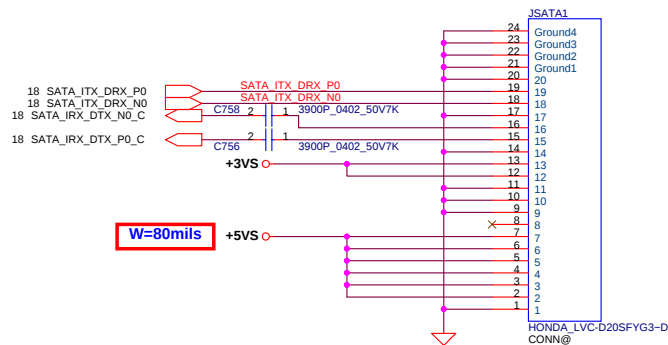


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				ICH8M(3/4) PM/USB/GPIO			
				Document Number			
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				Date			
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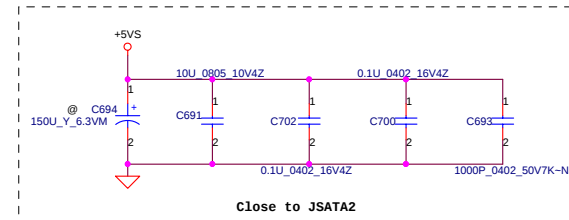
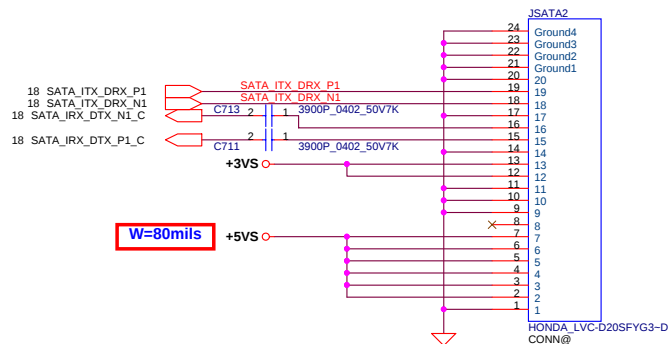
ODD Conn



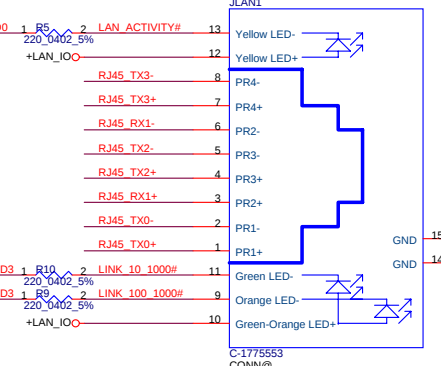
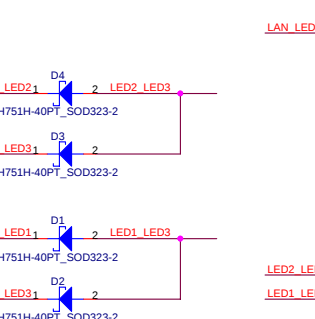
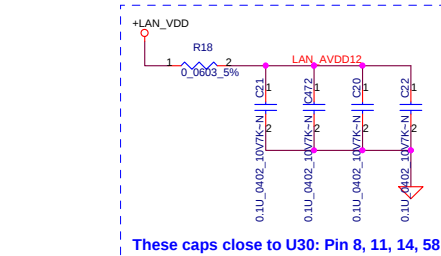
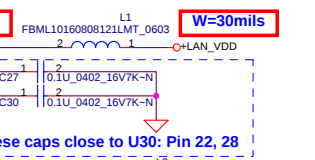
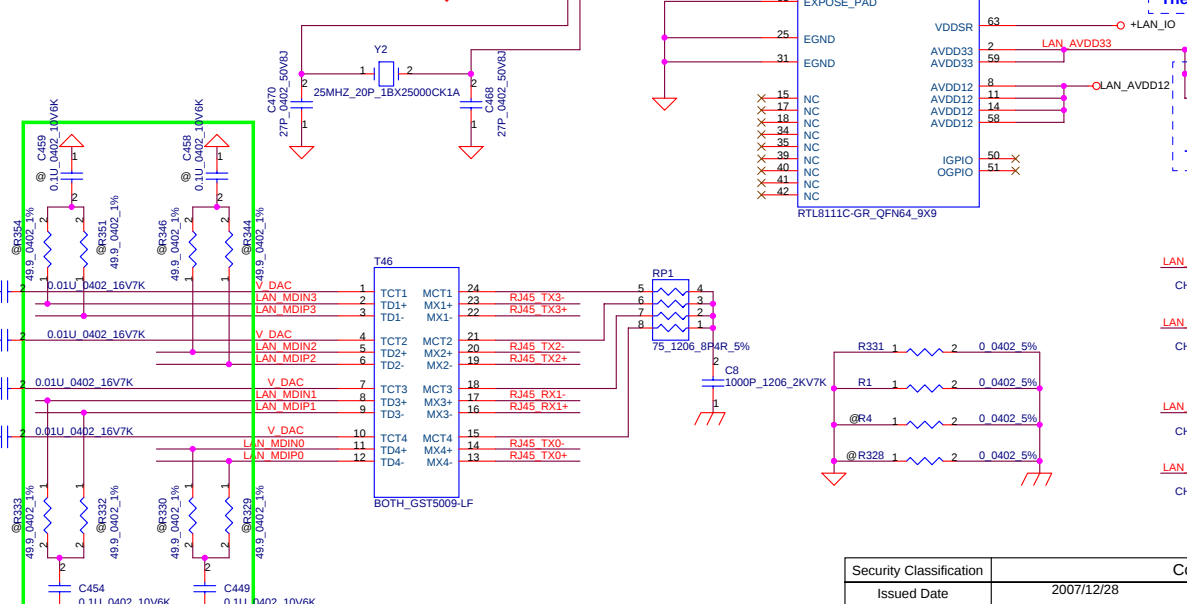
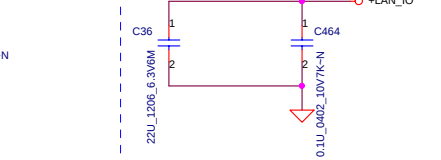
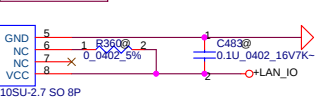
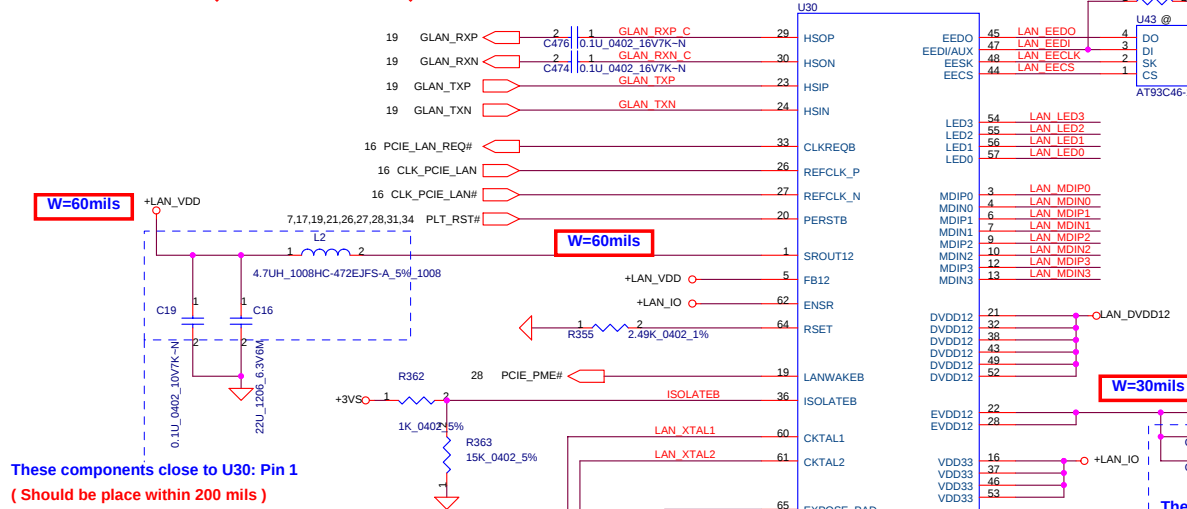
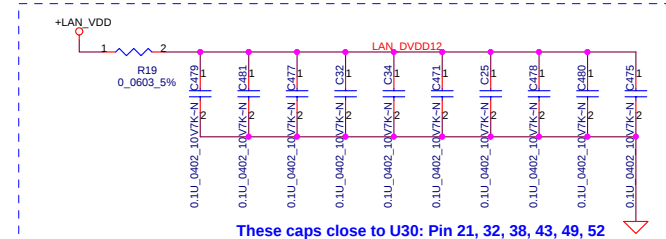
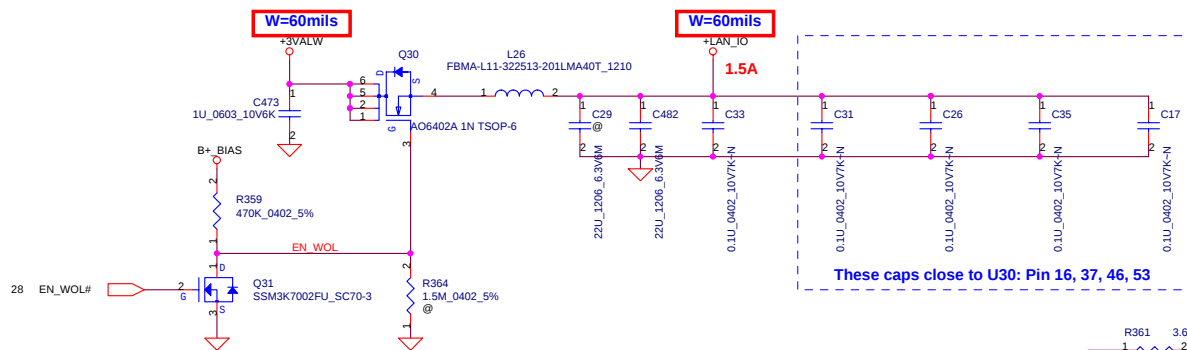
SATA HDD1 Conn



SATA HDD2 Conn

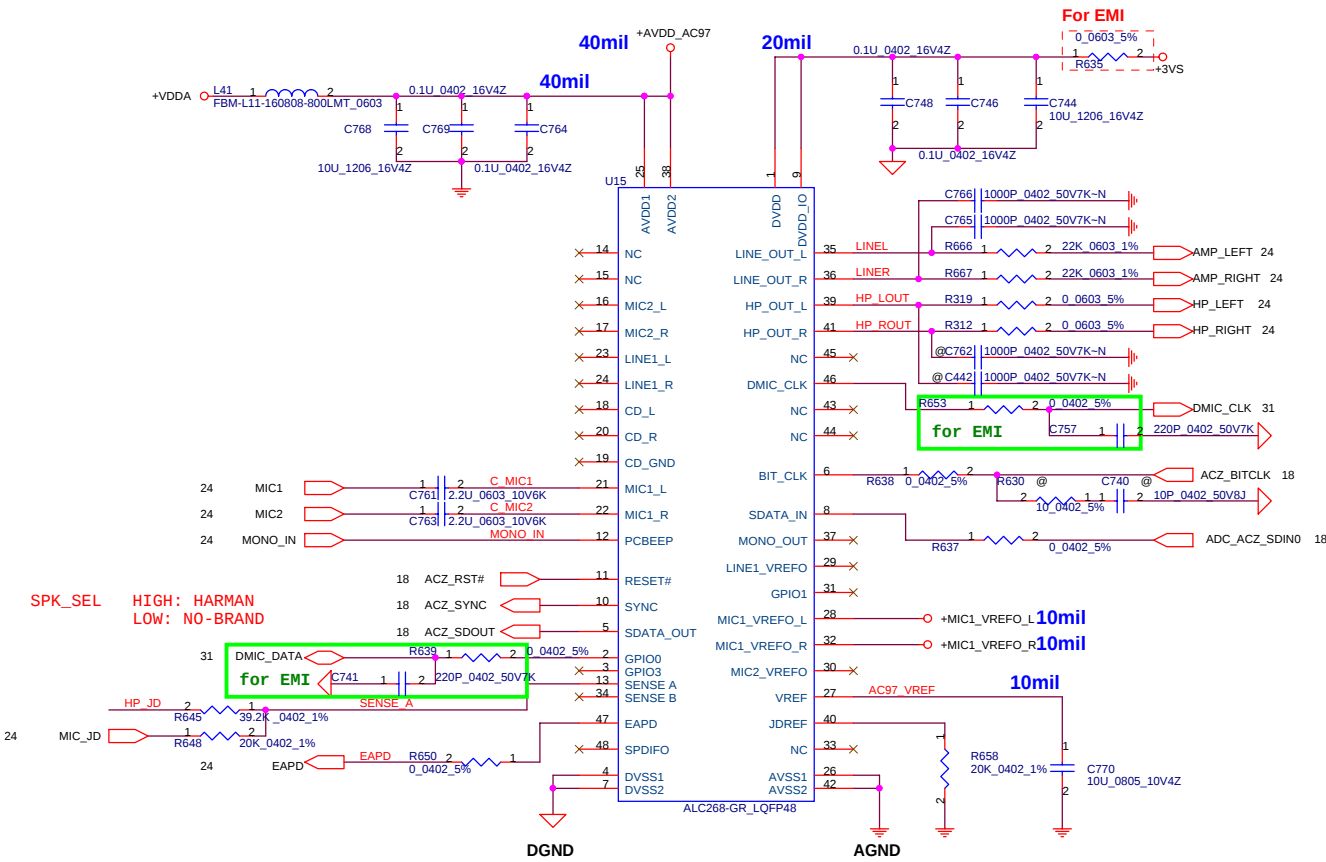


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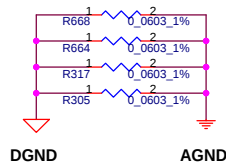
HD Audio Codec



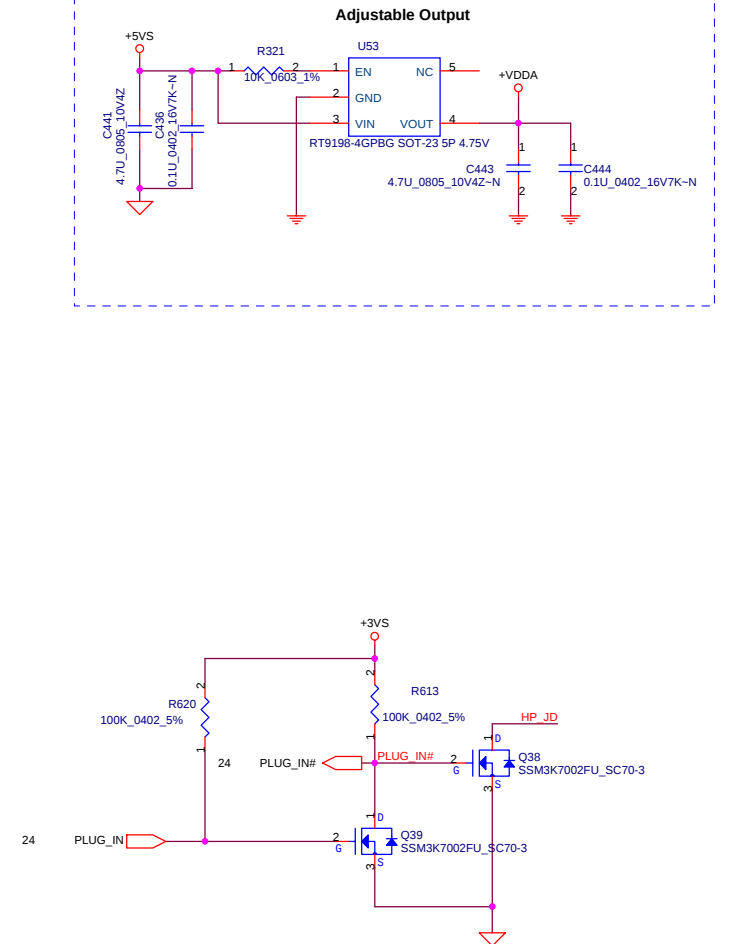
SPK_SEL HIGH: HARMAN
LOW: NO-BRAND

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Moat Bridge

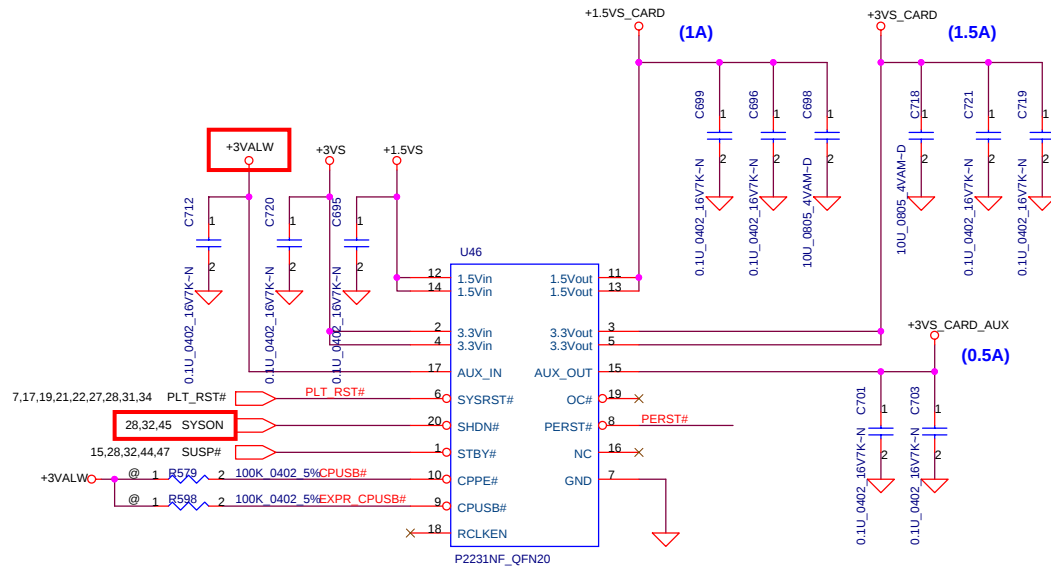


Regulator for Codec

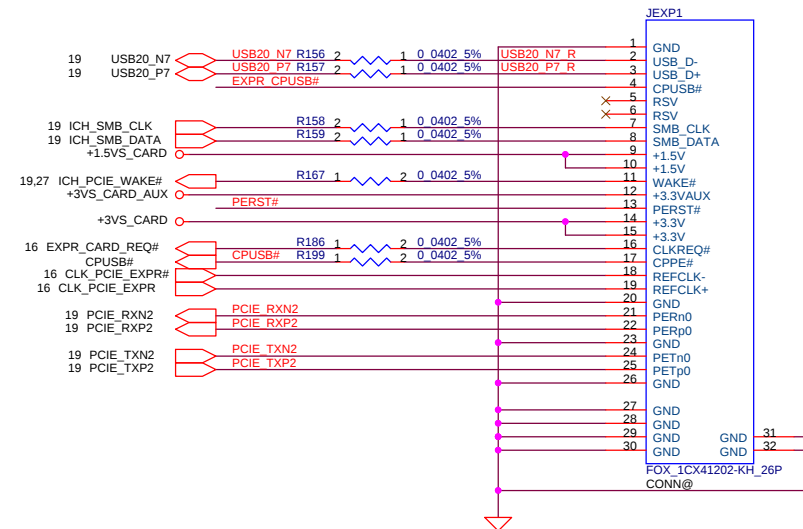


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Express Card Power Switch

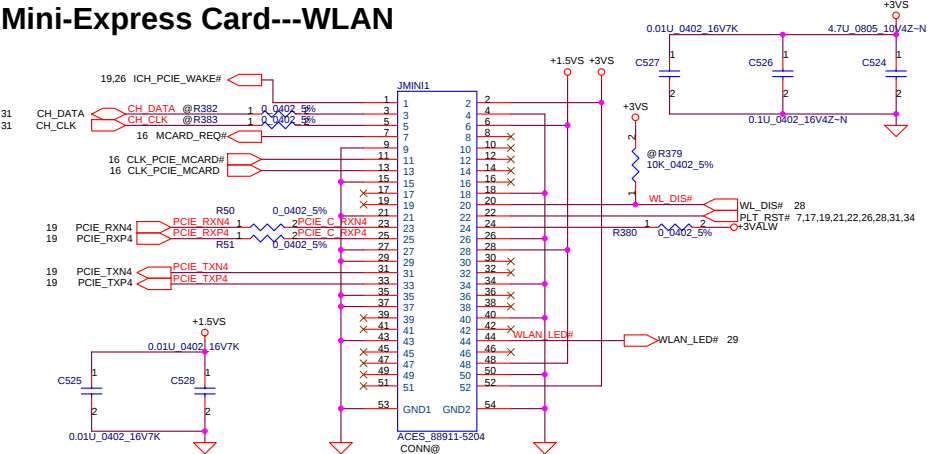


Express Card

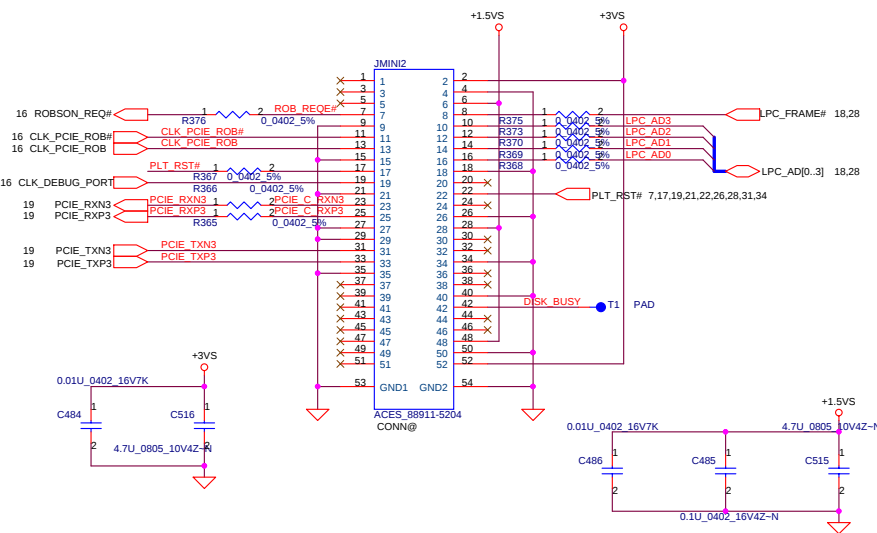


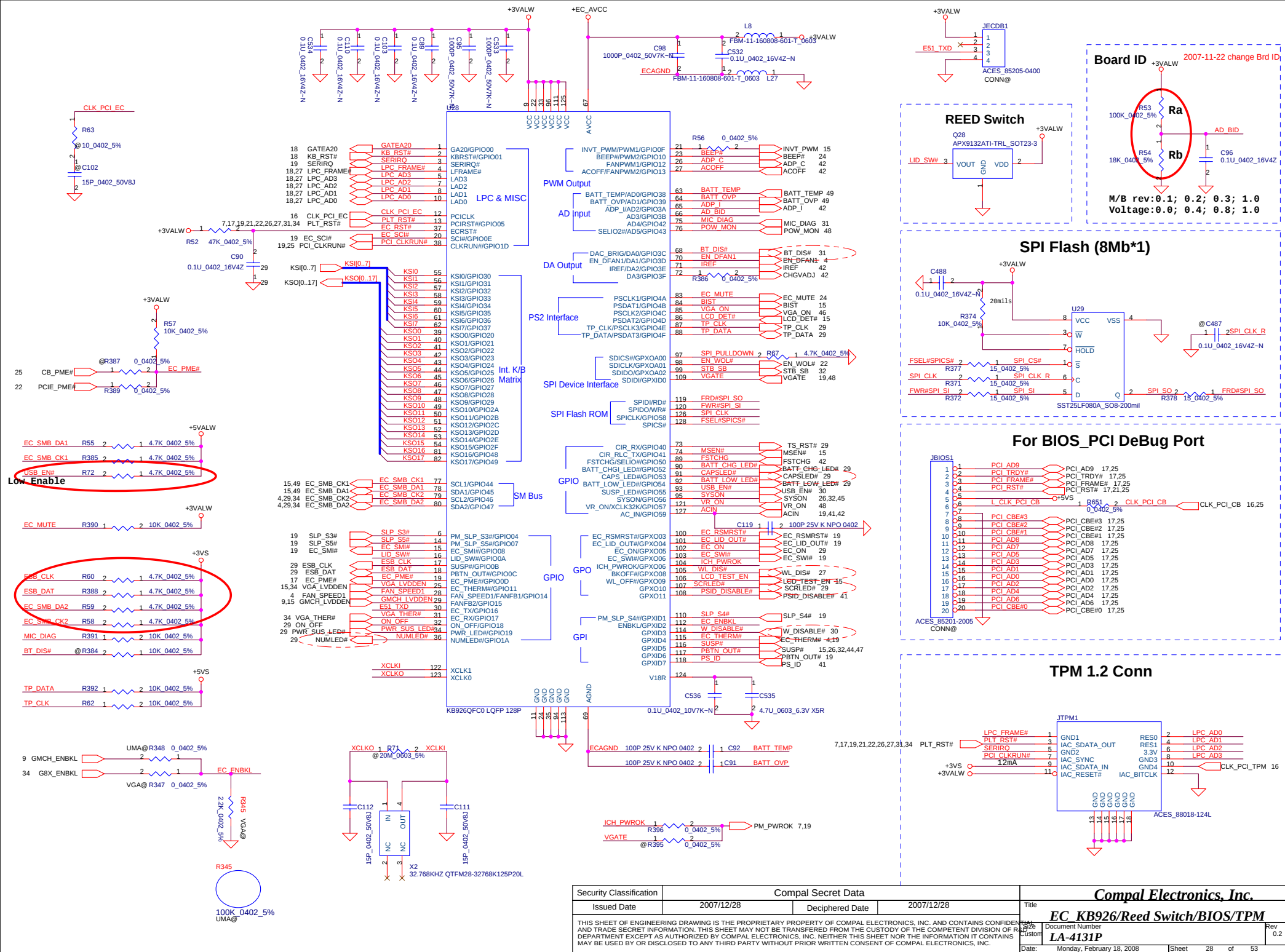
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Issued Date	2007/12/28	Deciphered Date	2007/12/28	Title	Express Card
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Mini-Express Card---WLAN



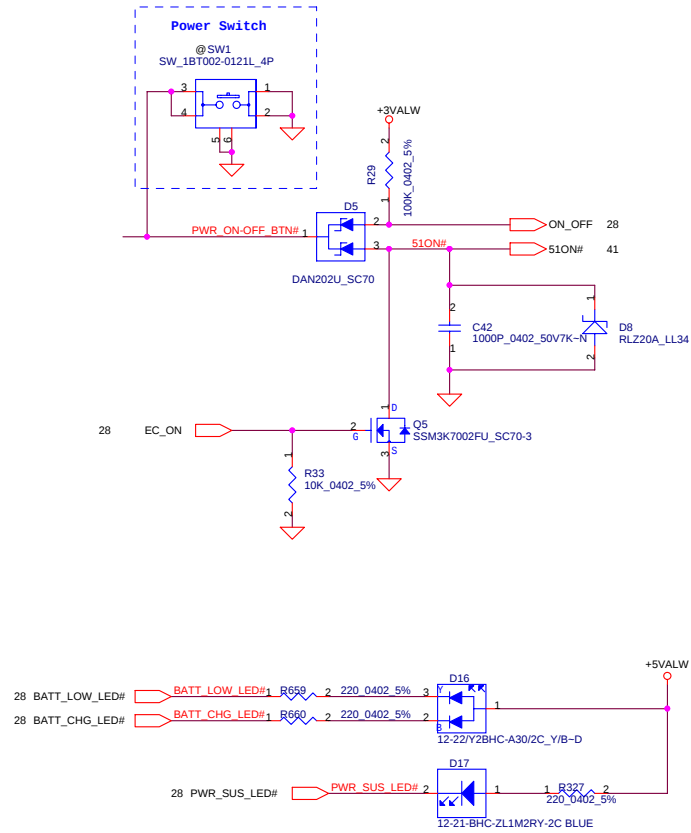
Mini-Express Card---Robson



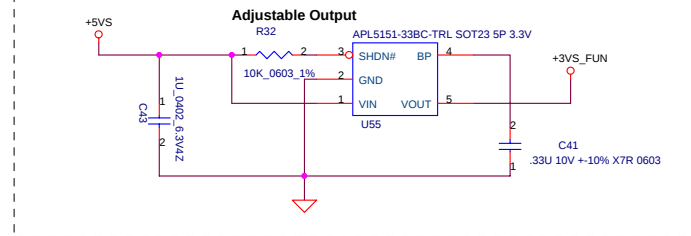


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2007/12/28		2007/12/28		EC_KB926/Reed Switch/BIOS/TPM	
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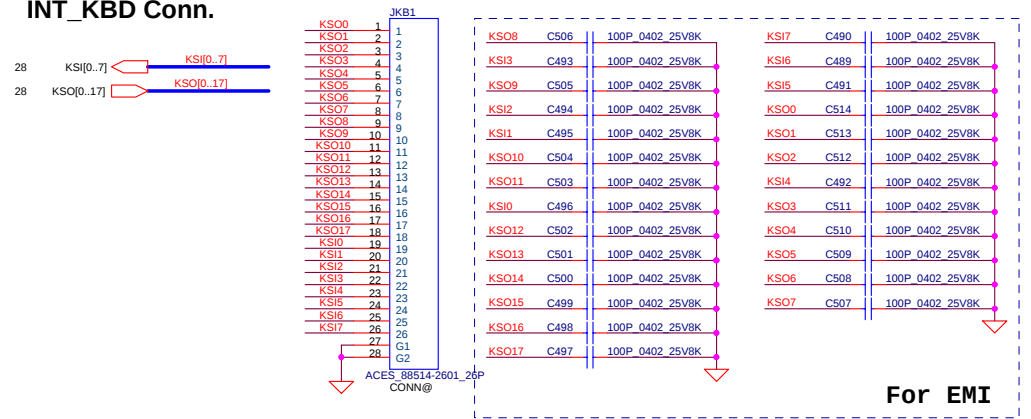
Power Button



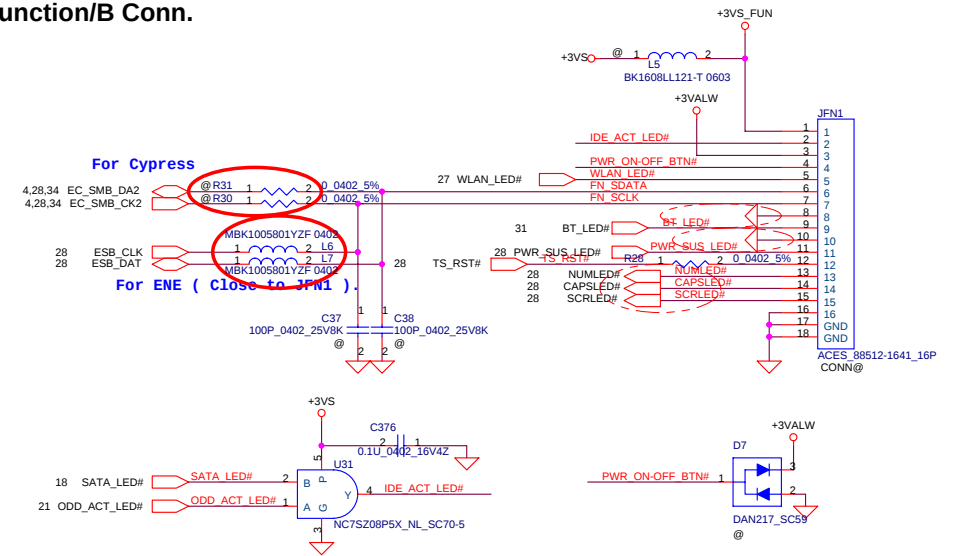
Regulator for ENE sensor



INT_KBD Conn.

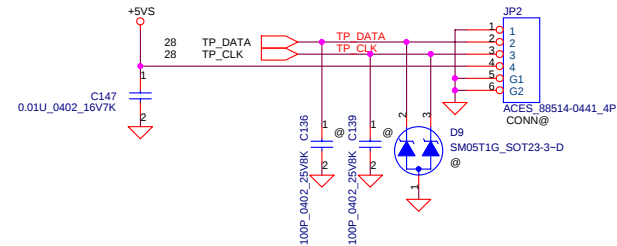


Function/B Conn.

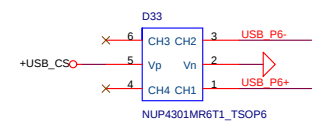
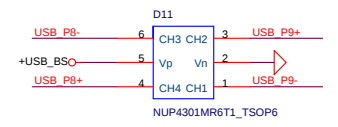
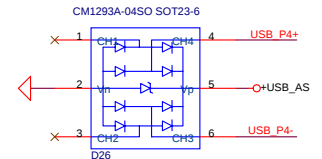
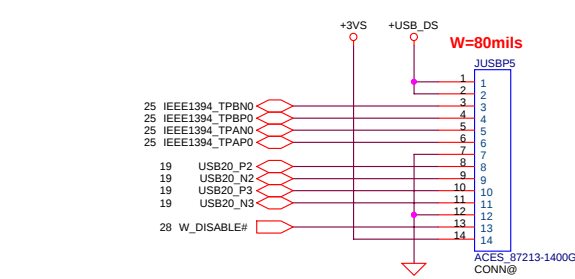
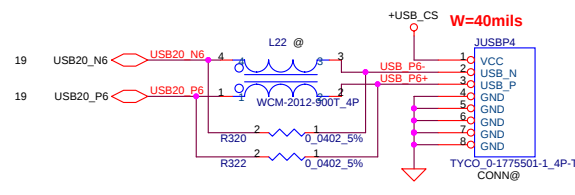
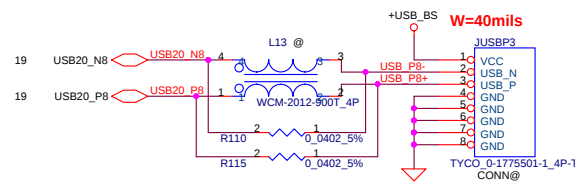
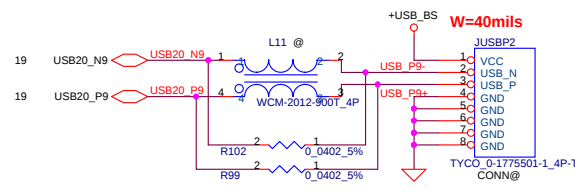
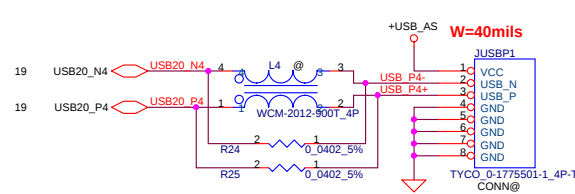
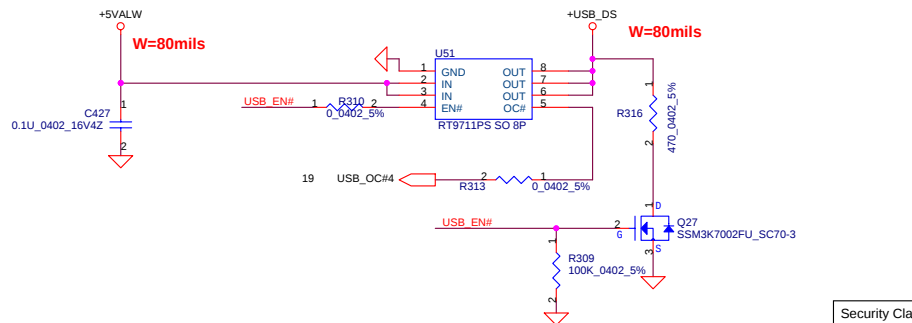
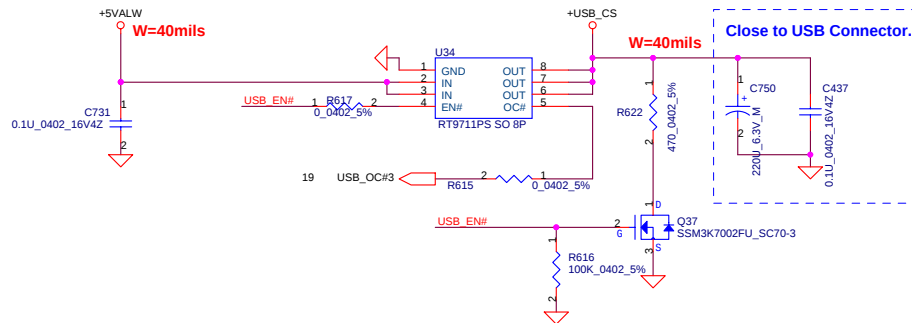
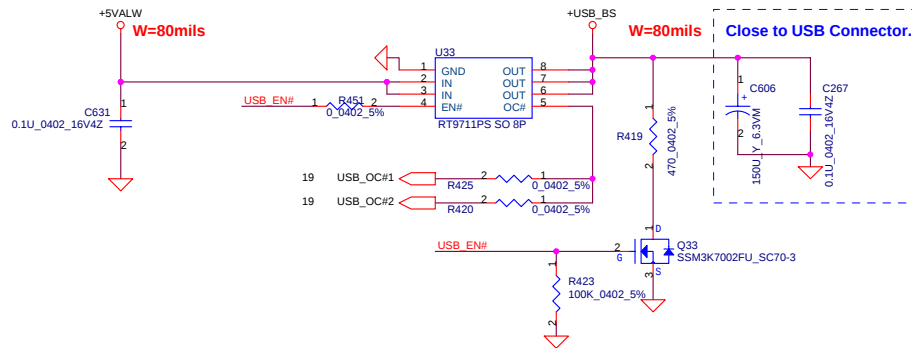
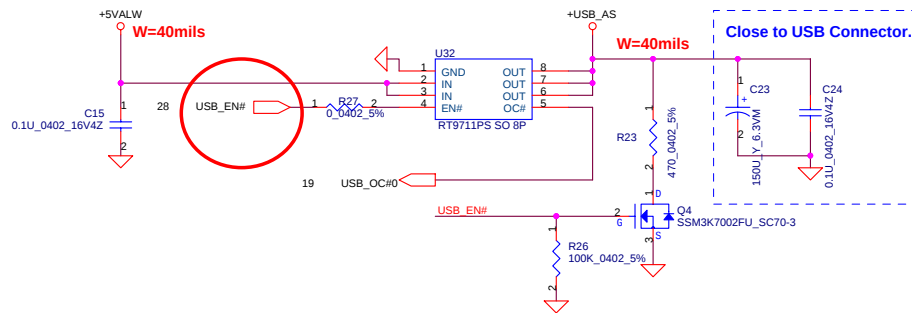


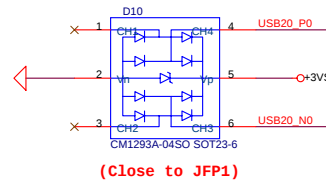
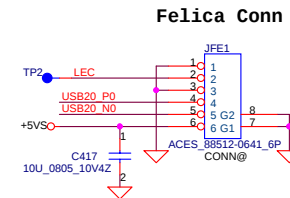
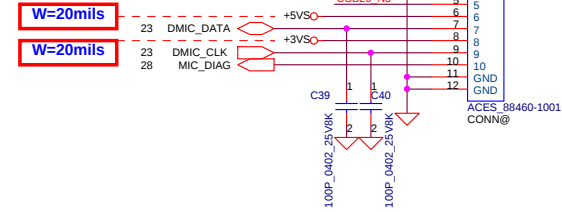
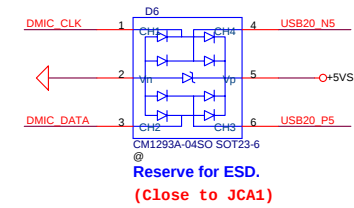
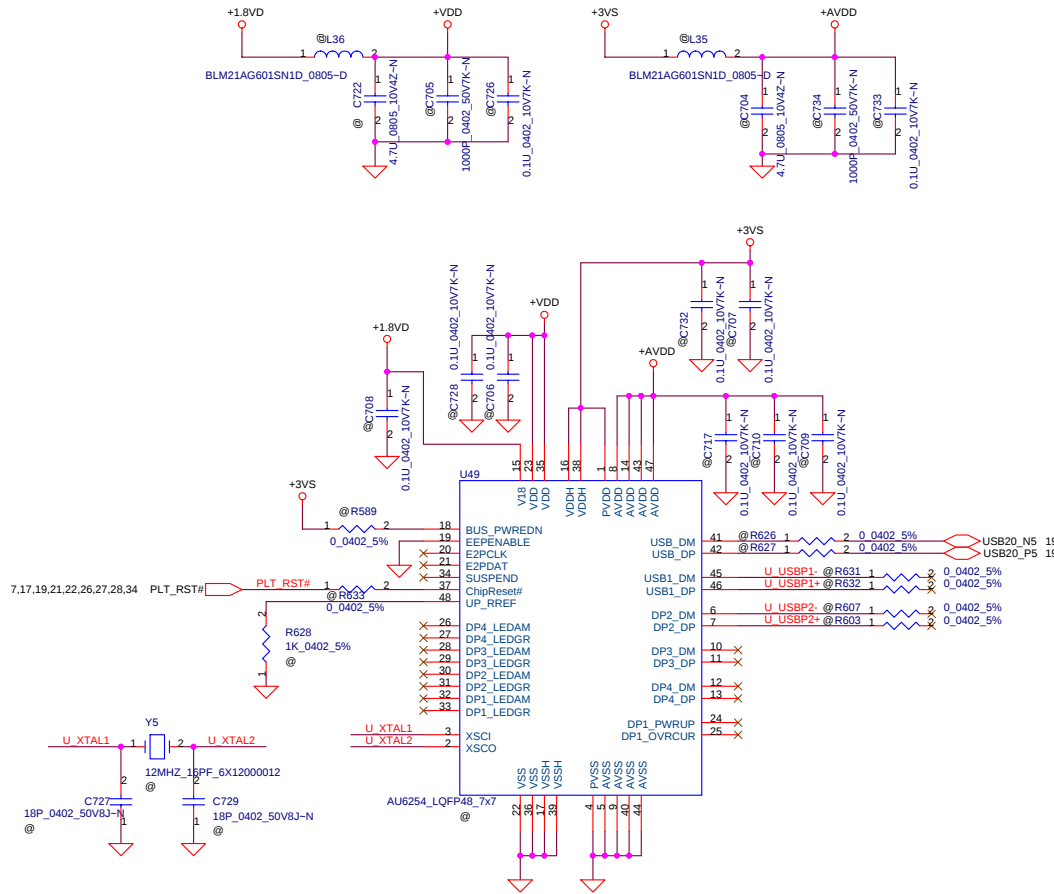
Touch Pad/B Conn.

TP/B to M/B



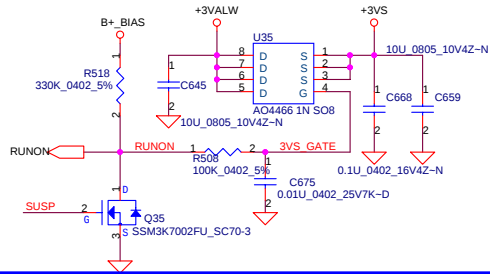
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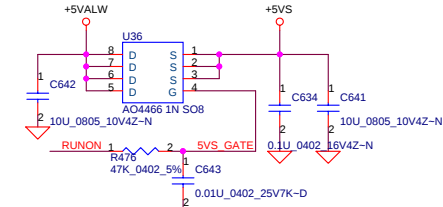


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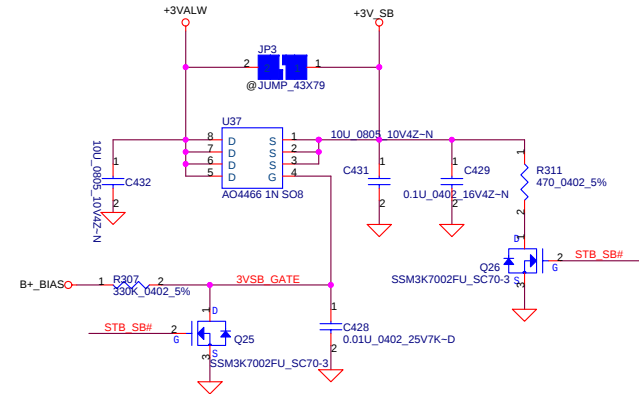
+3VALW to +3VS Transfer 4.5A



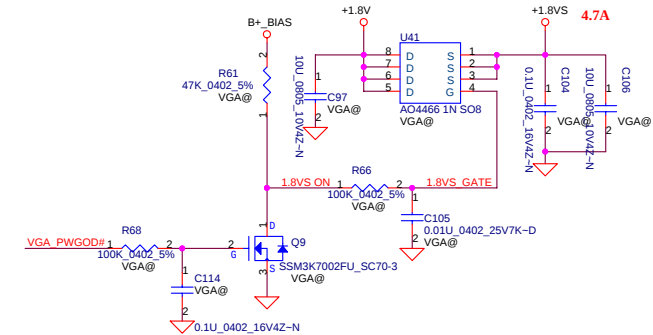
+5VALW to +5VS Transfer 6.5A



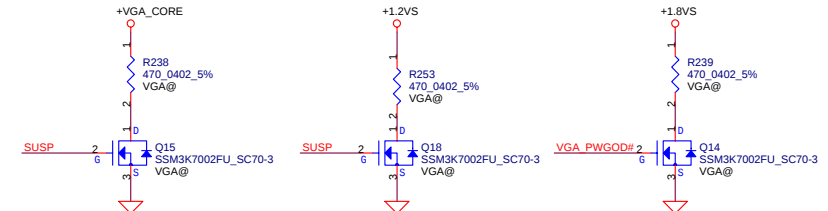
+3VALW to +3V_SB



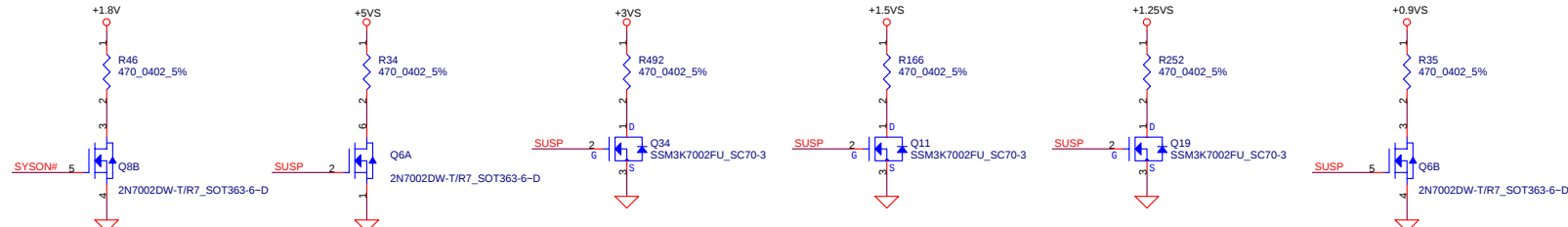
+1.8V to +1.8VS Transfer (For Discrete)



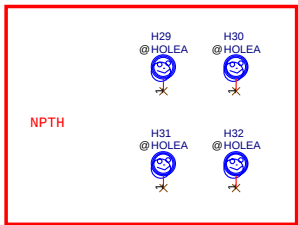
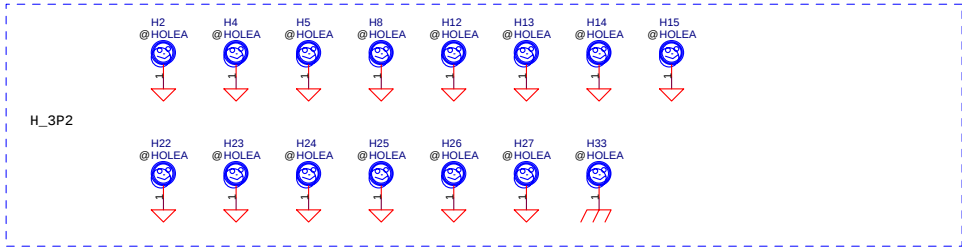
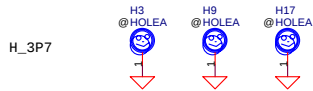
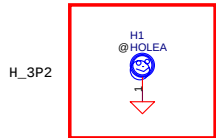
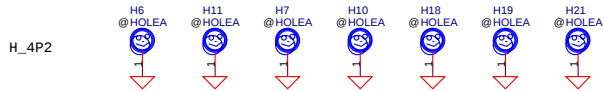
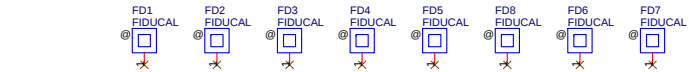
VGA Discharge Circuit



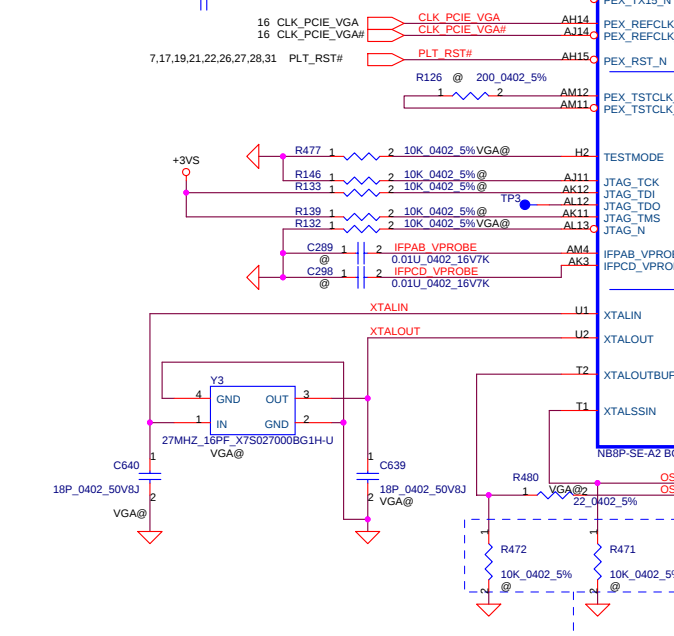
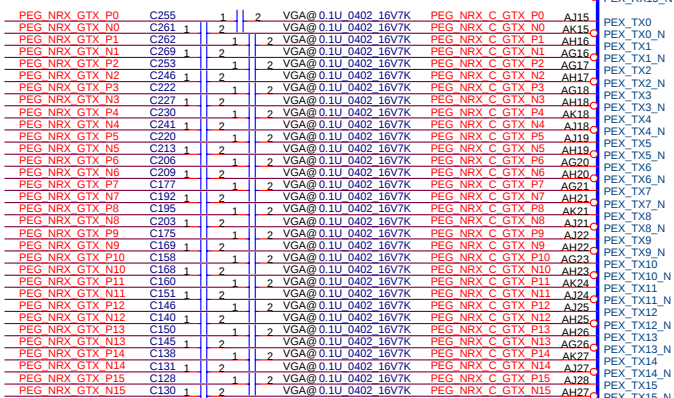
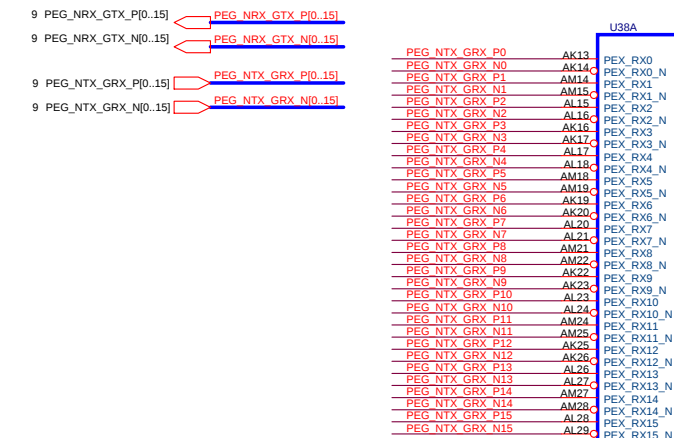
Discharge Circuit



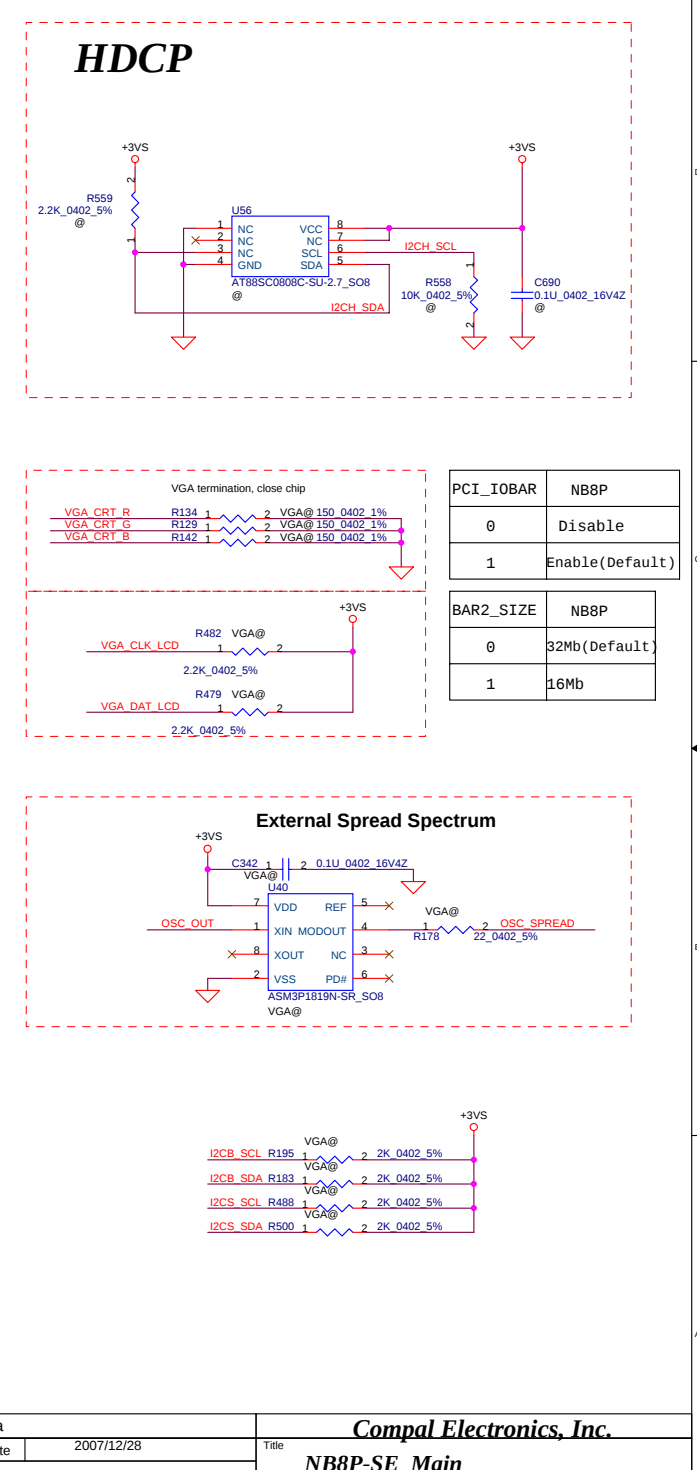
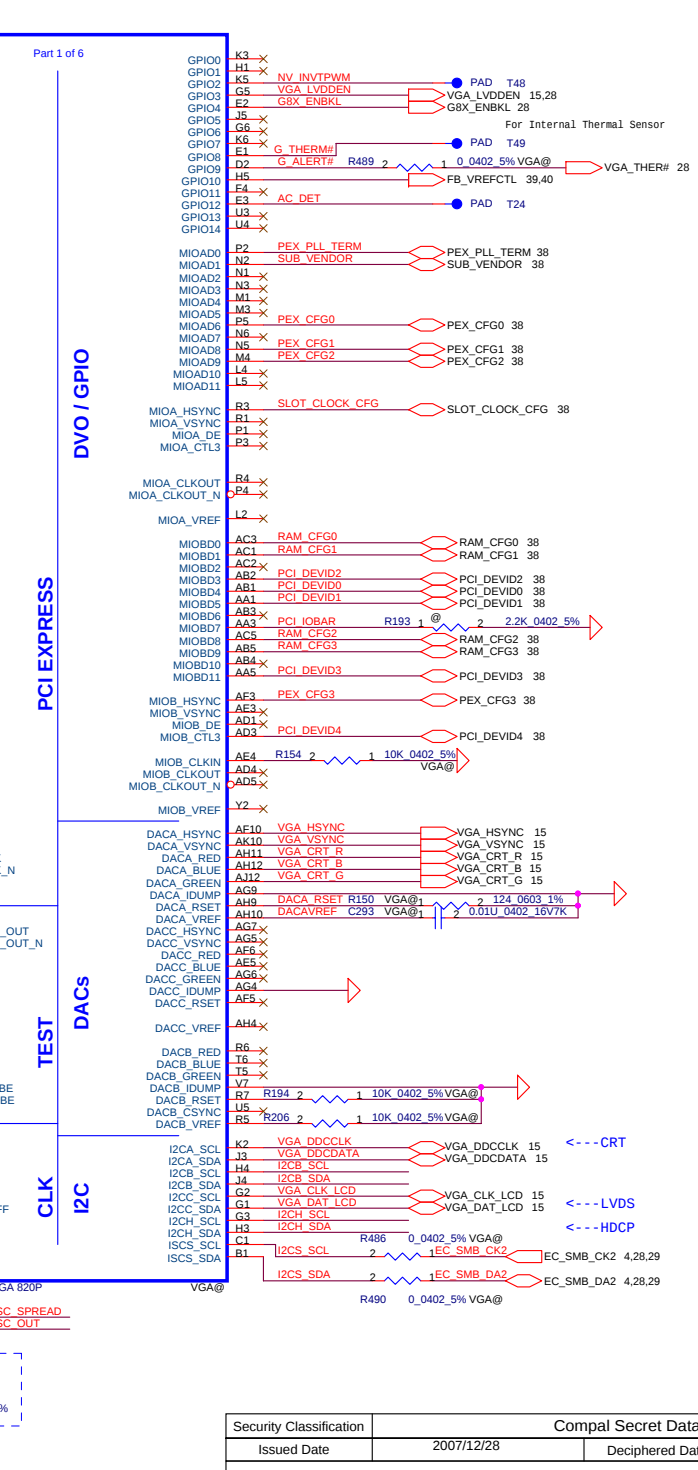
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				Deciphered Date				Title			
2007/12/28				2007/12/28				DC/DC Interface			
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				LA-4131P				0.2			
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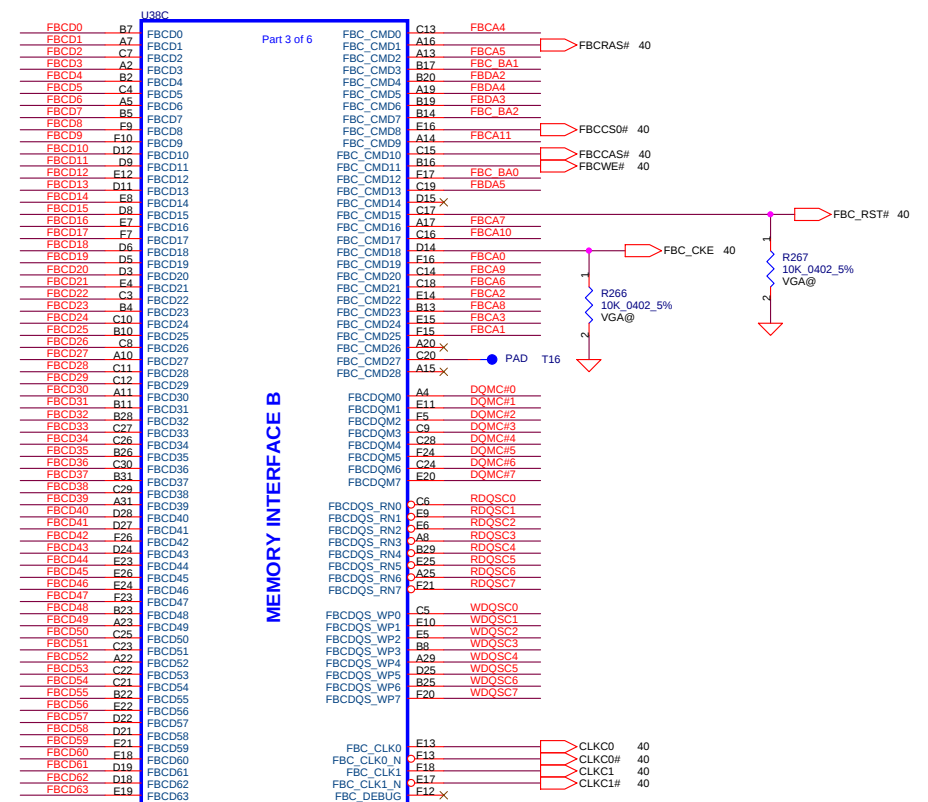
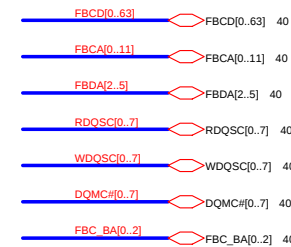
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Issued Date	2007/12/28	Deciphered Date	2007/12/28	Screws	
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				LA-4131P	0.2
				Date: Monday, February 18, 2008	Sheet 33 of 53



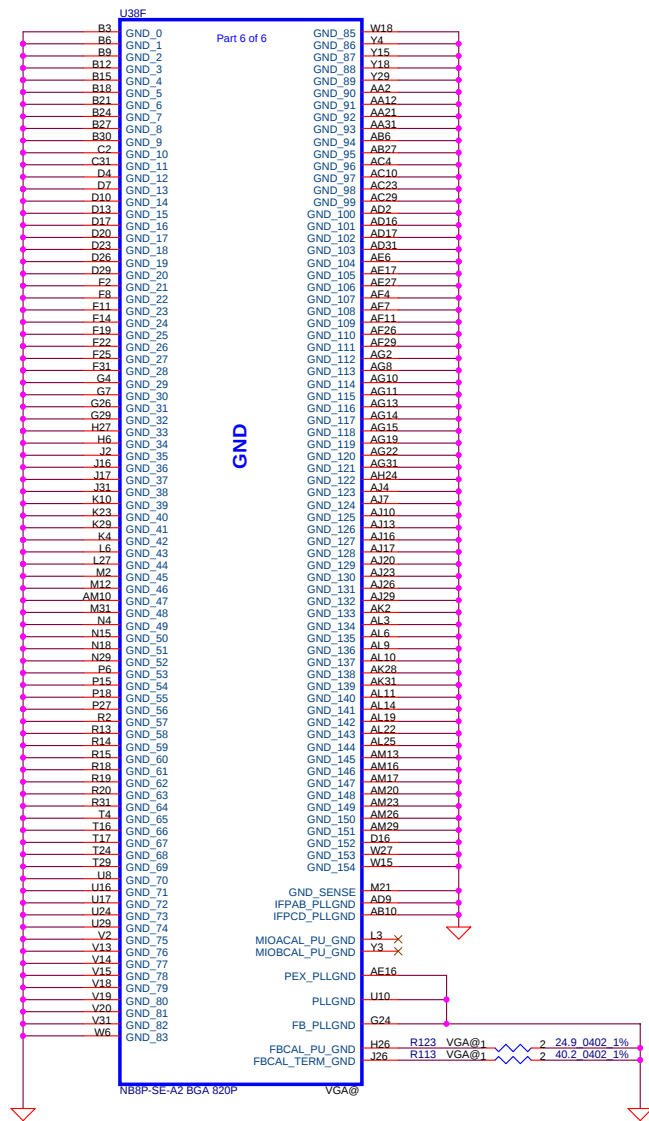
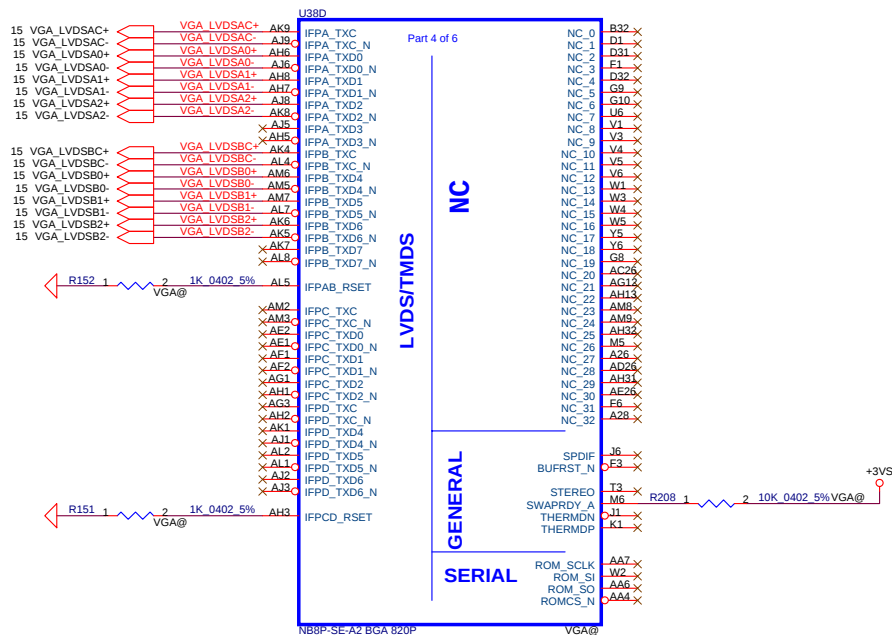
If External Spread Spectrum not stuff than stuff resistor.



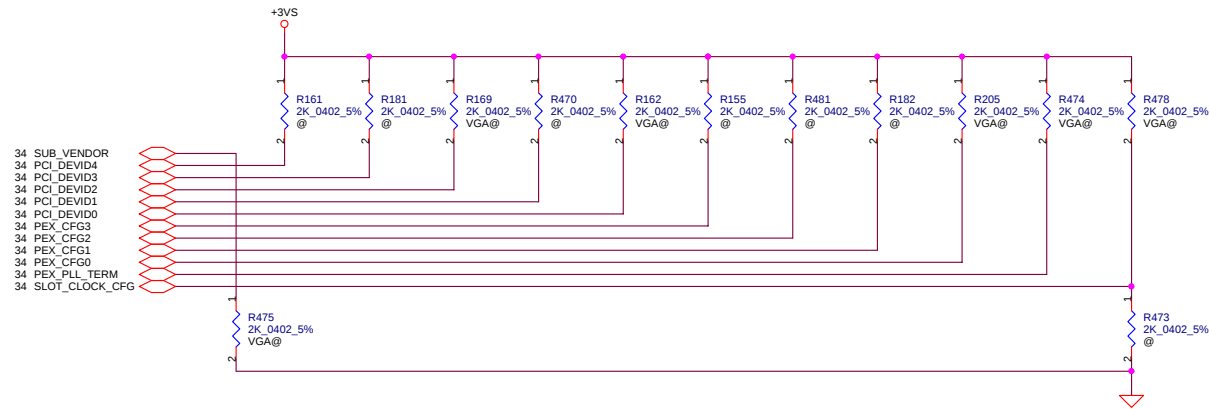
Security Classification		Compal Secret Data		Title	
Issued Date	2007/12/28	Deciphered Date	2007/12/28	Compal Electronics, Inc.	
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				Document Number	LA-4131P
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				Date	Monday, February 18, 2008
				Sheet	34 of 53



Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2007/12/28	Deciphered Date	2007/12/28	Title	NB8P-SE Memory Interface		
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				LA-4131P			
				Date: Monday, February 18, 2008	Sheet 35 of 53		

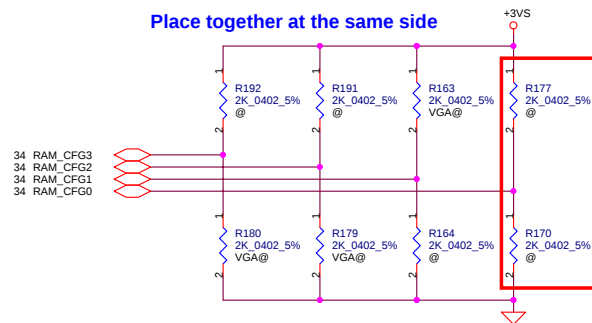


Security Classification	Compal Secret Data			Title	
Issued Date	2007/12/28	Deciphered Date	2007/12/28	Document Number	
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Date: Monday, February 18, 2008				Sheet	36 of 53



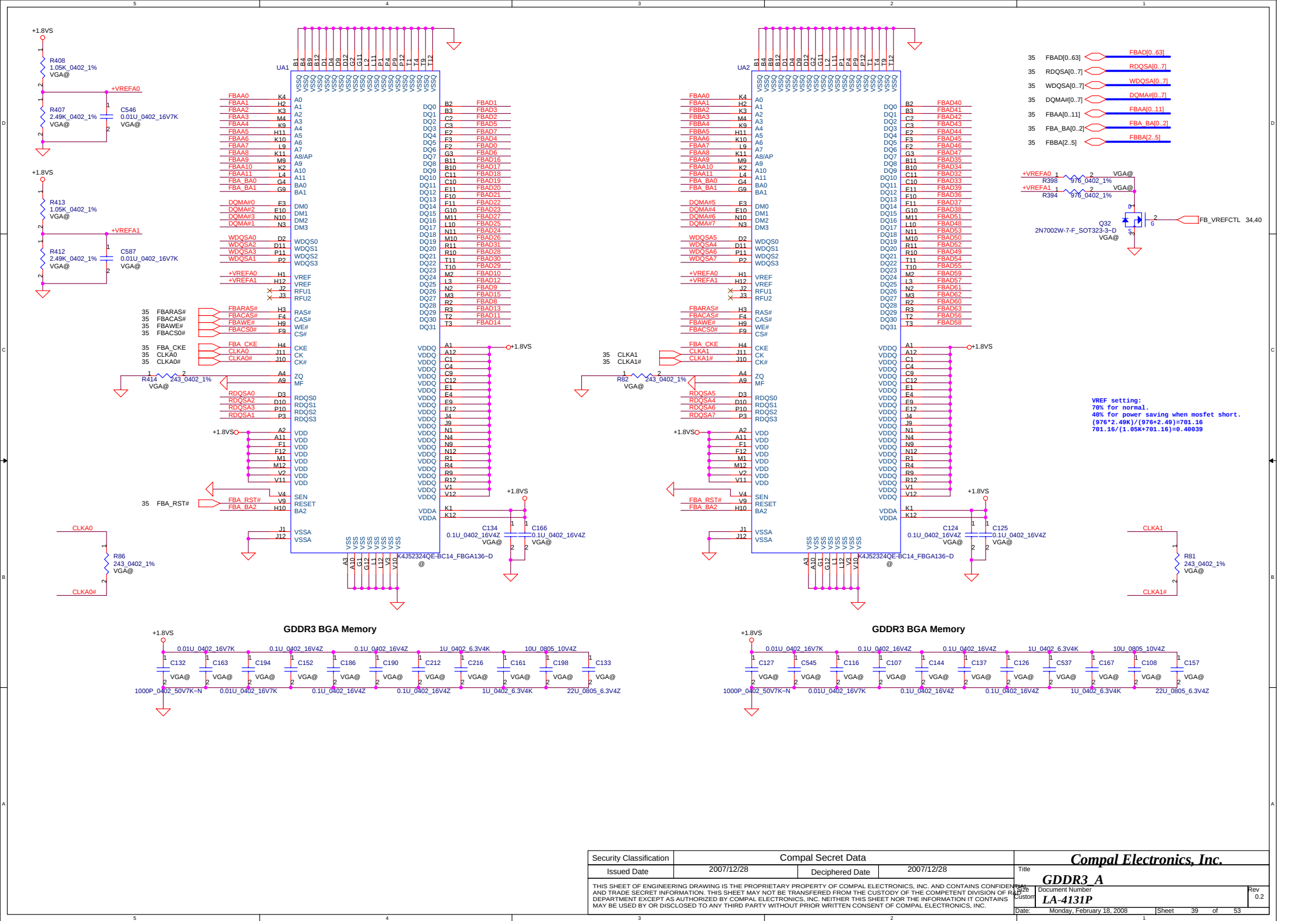
Straps	SUB_VENDOR	PCI_DEVID [4:0]	PEX_CFG[3:0]	PEX_PLL_TERM	SLOT_CLK_CFG
Description	0: BIOS not present 1: BIOS present	NB8P-GS: 0x0407 NB8P-GT: 0x0408 NB8P-SE: 0x0425	0X1	0: Enable 1: Disable	0: GPU&MCH do not share a common ref. CLK. 1: GPU&MCH share a common ref. CLK.
Setting	0: BIOS not present	NB8P-SE: 0x0425 (00101) Internal Pull down	0001: 0X1 (0001) Internal Pull down	1: Disable	1: GPU & MCH share a common ref. CLK.

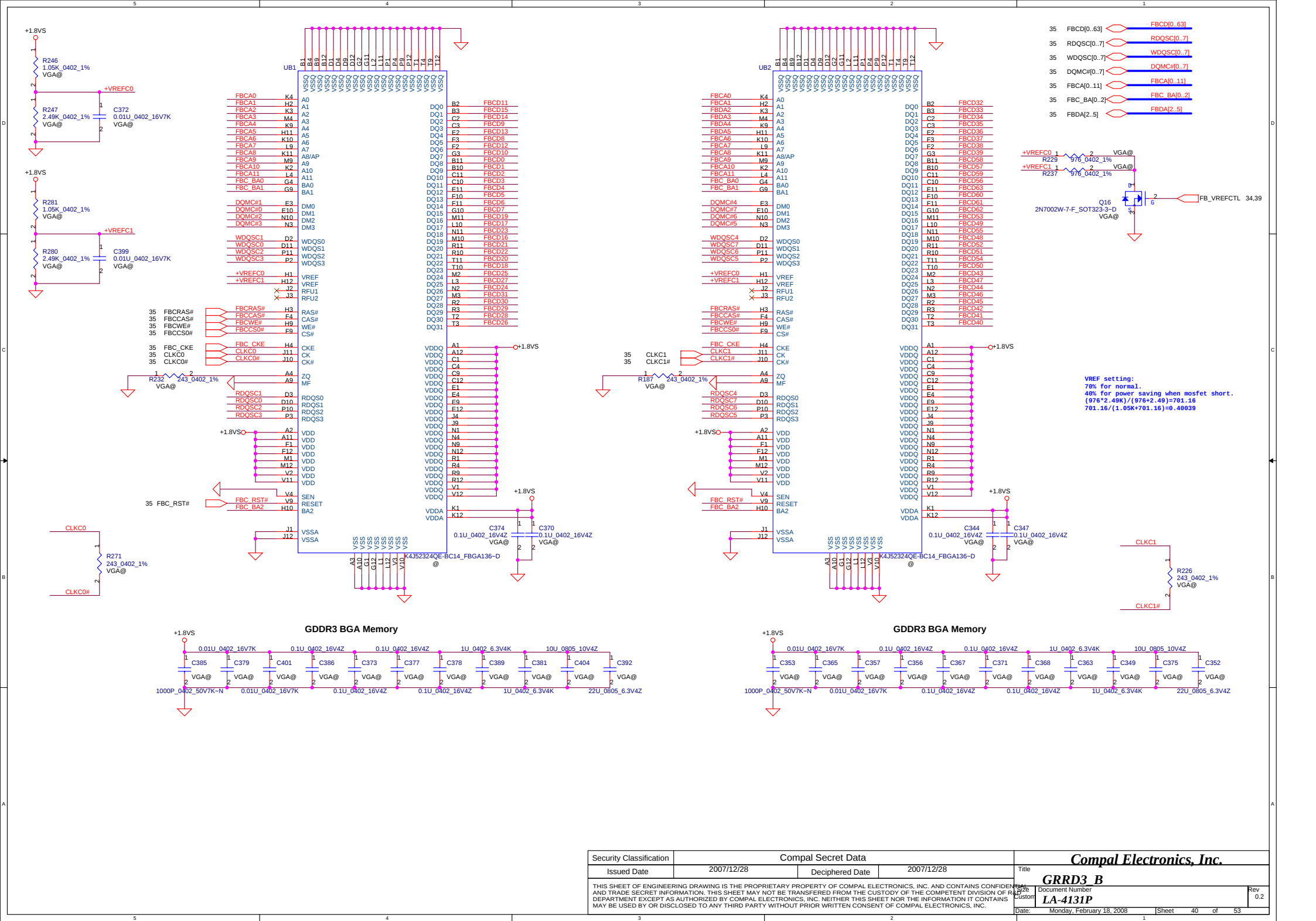
RAM_CFG[3:0]



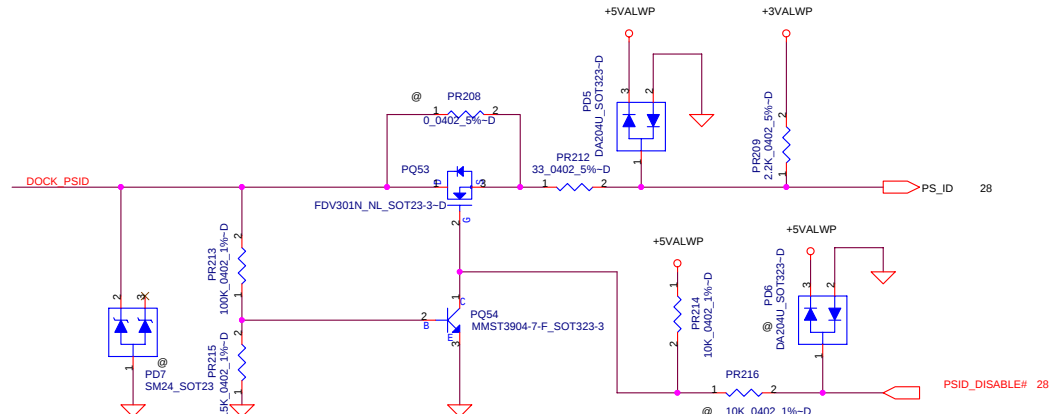
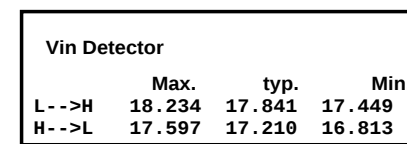
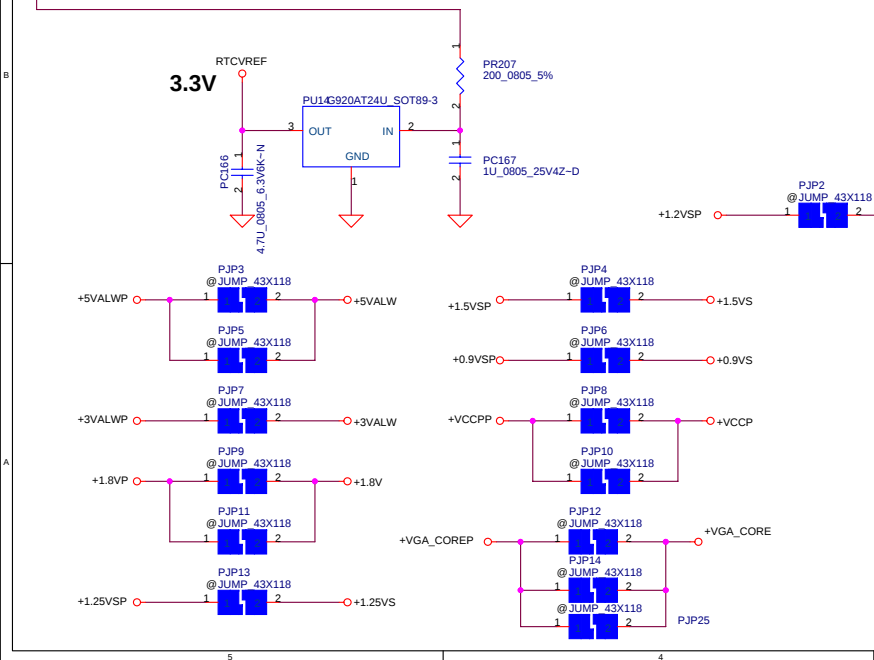
RAM_CFG3 0 = Single Rank 1 = Dual Rank	RAM_CFG2 RAM Size 0=16Mx32 1= 8Mx32	RAM_CFG[1:0] Vendor 10 = Hynix 11 = Samsung		Description
				NB8P-GS
0	0	0	0	
0	0	0	1	
0	0	1	0	Hynix (16M*32 4pcs = 256MB)
0	0	1	1	Samsung (16M*32 4pcs = 256MB)
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
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1	1	1	1	

ZZZ
VRAM



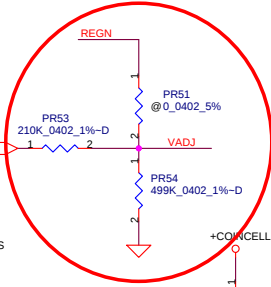
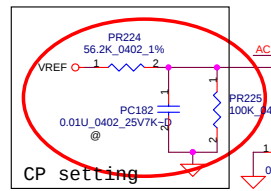
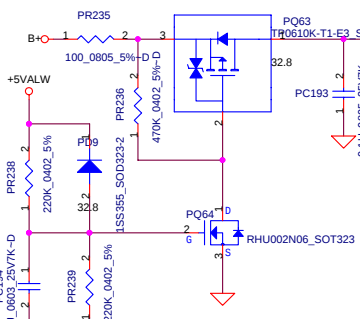
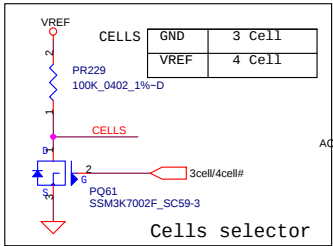


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				1	LA-4131P	0.2		
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Security Classification	Compal Secret Data			Title
Issued Date	2006/10/1	Deciphered Date	2007/5/01	DCIN / Precharge
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90W adapter
 $I_{charge} = (V_{srset}/V_{dacc}) * (0.1/PR34) = 3A$
 $I_{adapter} = (V_{acset}/V_{dacc}) * (0.1/PR23) = 3.65A$
 Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz



COIN RTC Battery

IREF	Current
3.265V	3.3A
0.49V	0.5A

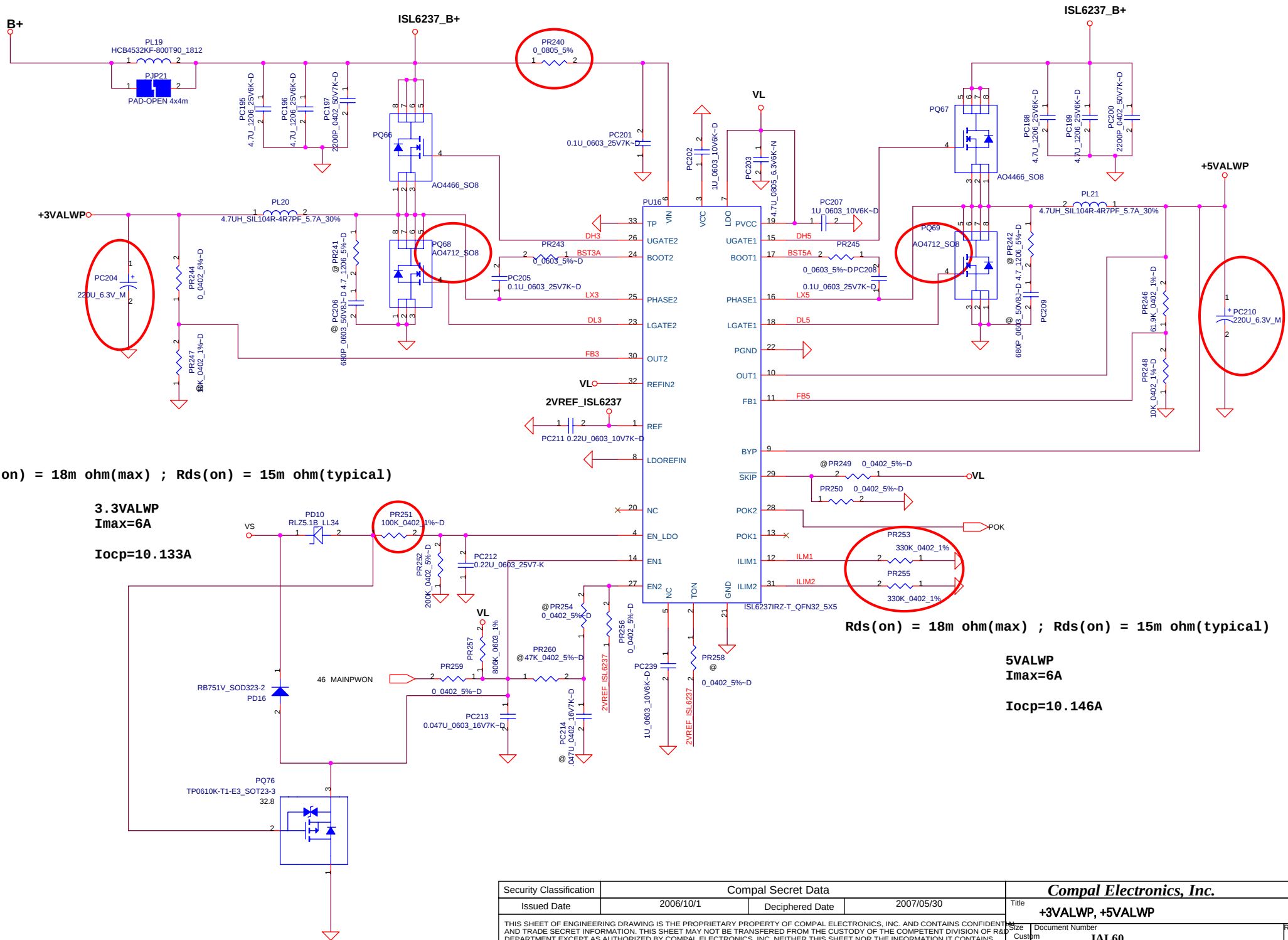
Move to power schematic

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Compal Electronics, Inc.

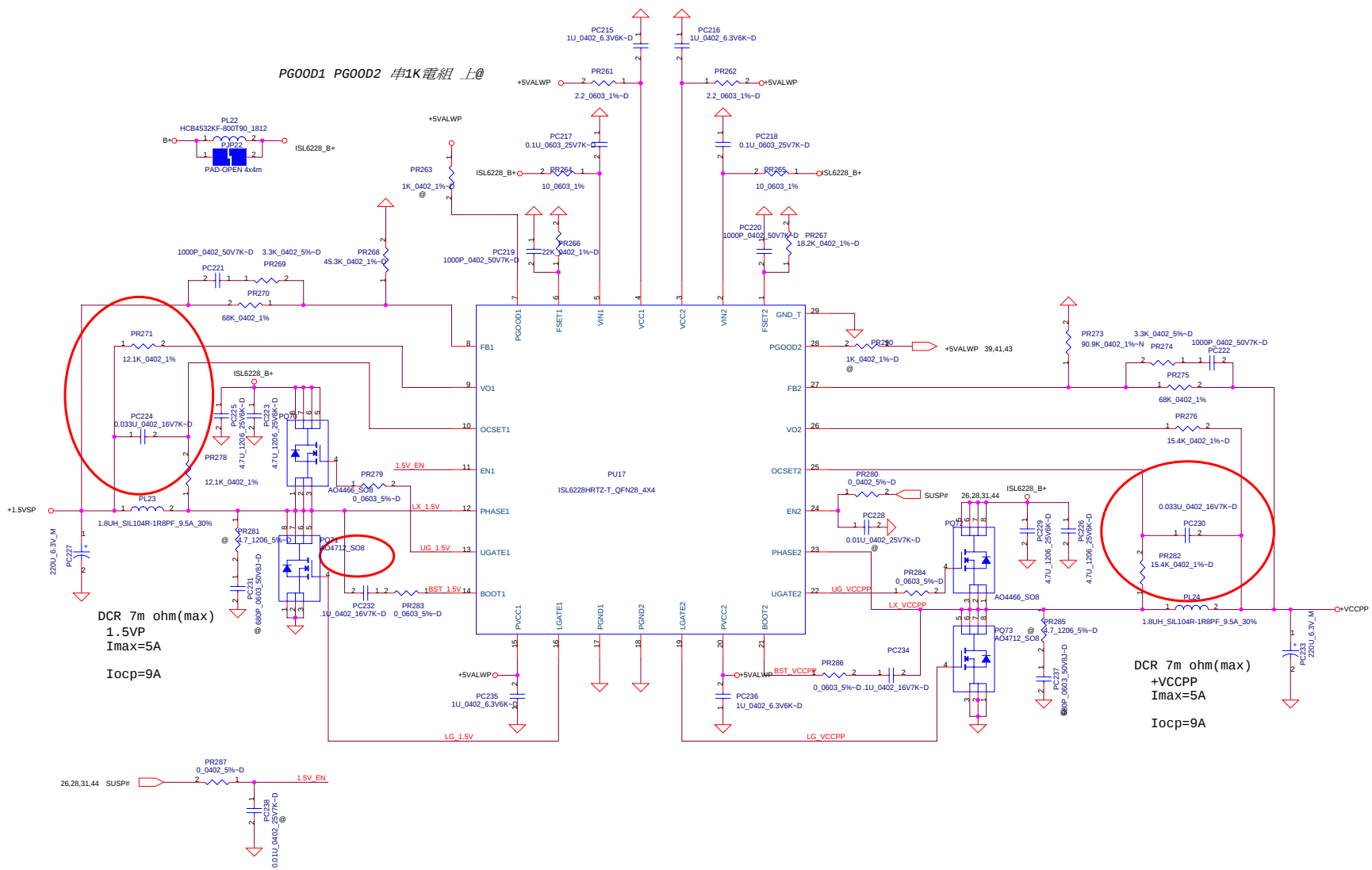
Charger

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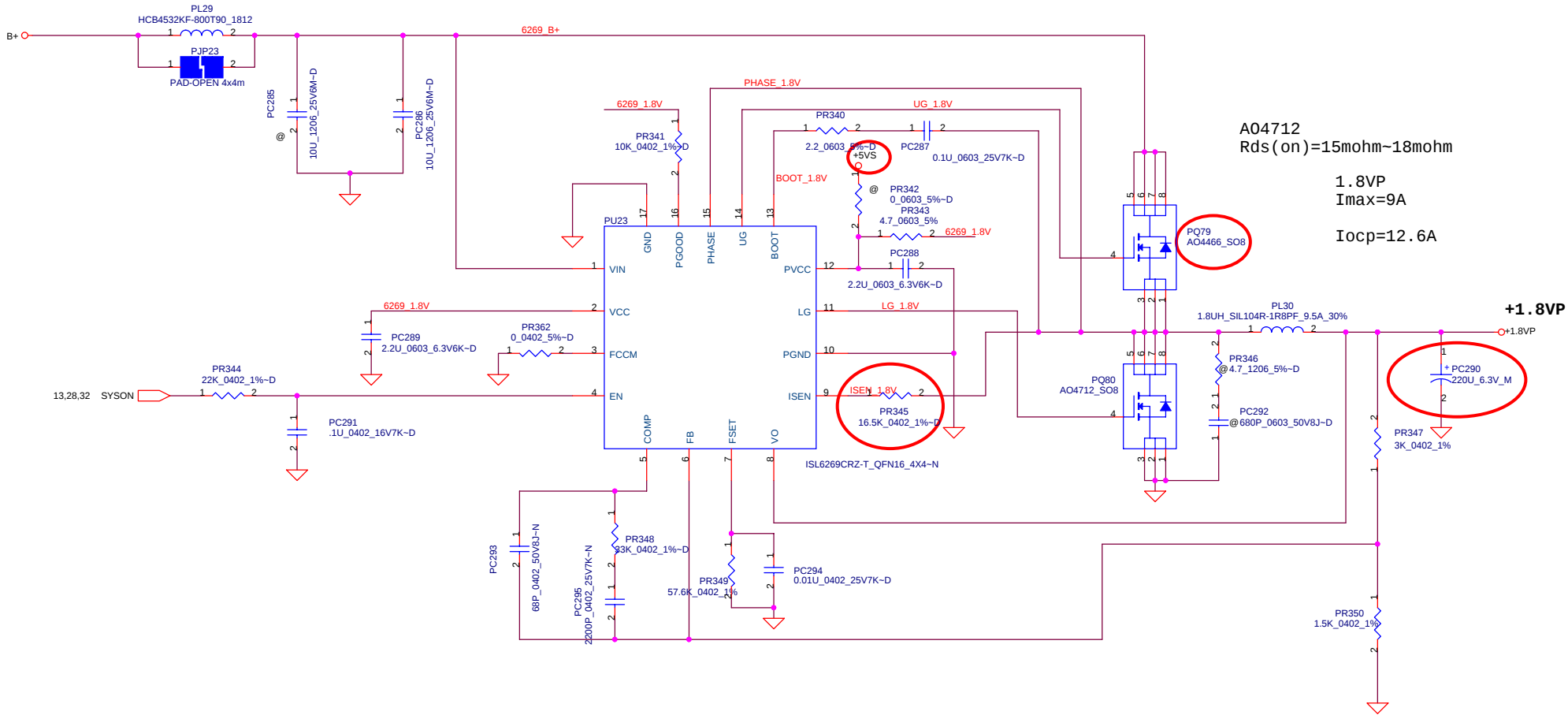


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Issued Date	2006/10/1	Deciphered Date	2007/05/30	Title +3VALWP, +5VALWP	
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Date: Monday, February 18, 2008				Sheet 43	of 50

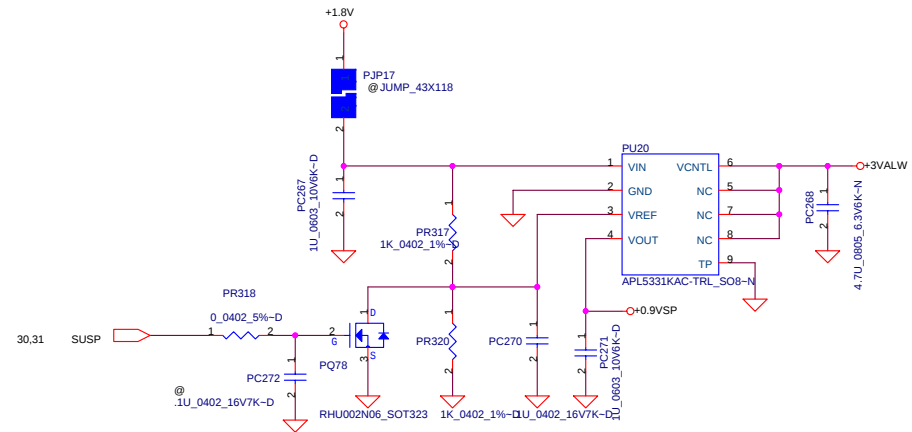
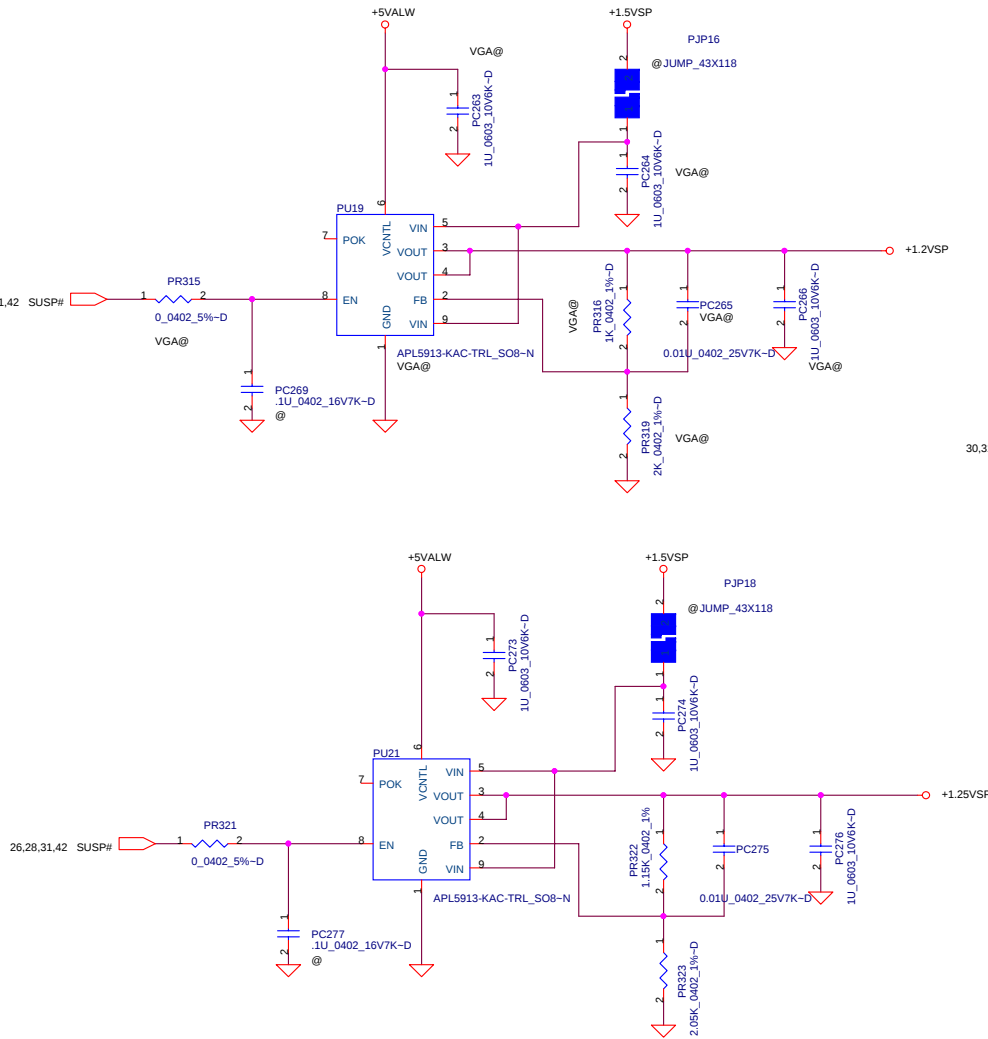
PG00D1 PG00D2 串1K電組 上@



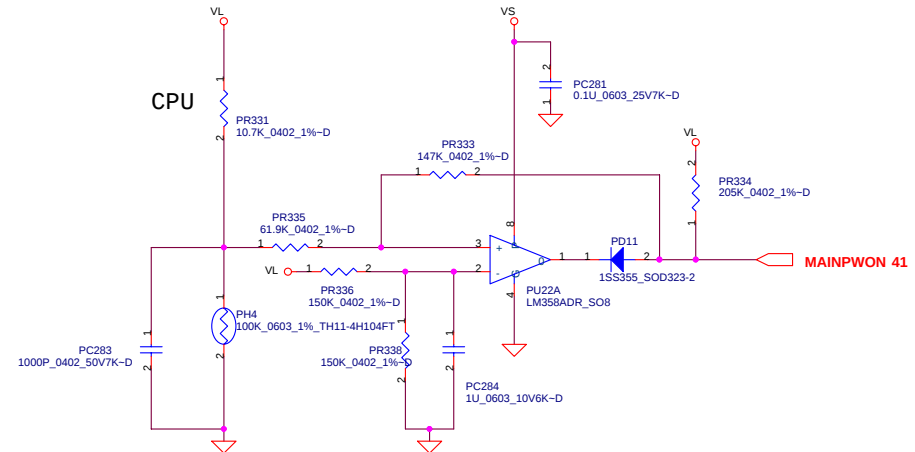
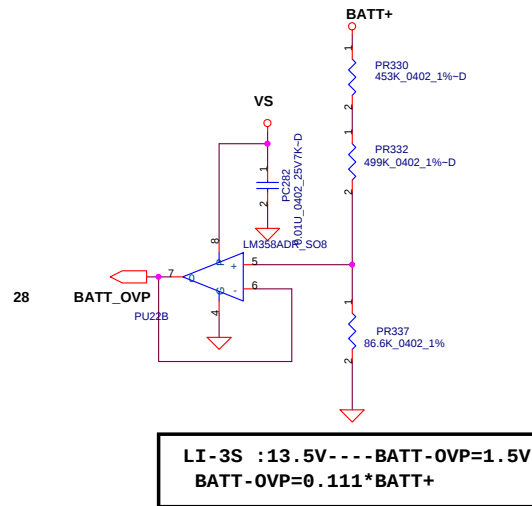
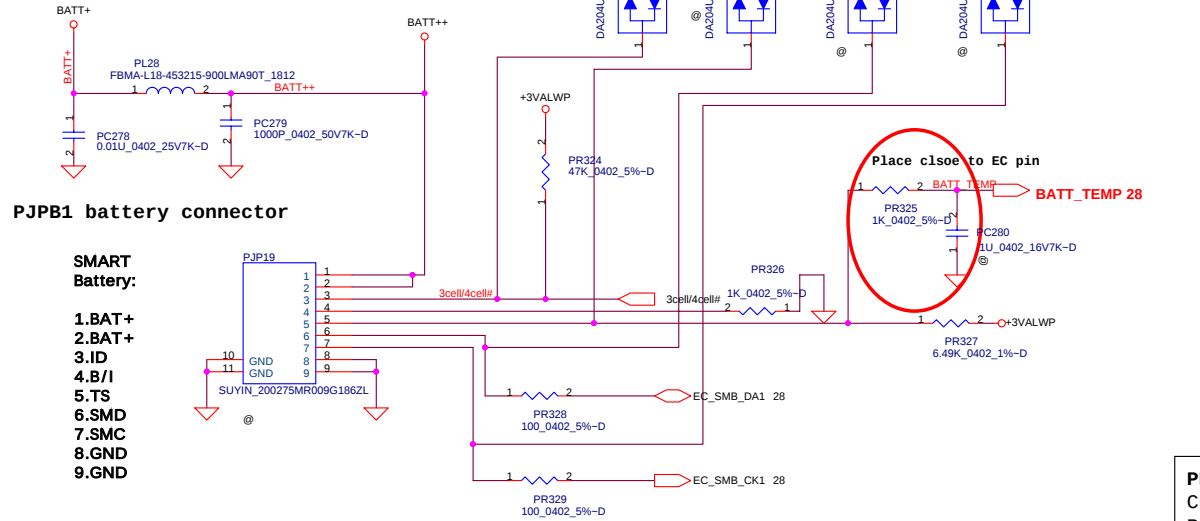
Security Classification	Compal Secret Data			
Issued Date	2006/10/1	Deciphered Date	2007/5/01	Title
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				Date	Monday, February 18, 2008
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Issued Date		2005/10/1		Deciphered Date		2007/05/30		Title	
								BATTERY CONN	
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						Document Number		JAL60	
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						Sheet		49 of 50	

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	ALL	ALL Page	07/11/30	DELL	base on customer request change SD SE to *L part	ALL SD* SE*	
2	P40	CHARGER	07/12/11	COMPAL	in order to meet the JETA rule,the charge voltage will be auto adjust by EC	ADD PR53(4.3K) PR54 PR51	
3	P41	+3VALWP/+5VALWP	07/12/11	COMPAL	When battery only and 4s shut down the system can not turn off the 3valwp and 5valwp	ADD PD16 (RB751V),PQ76(TP0610K)	
4	P41	+3VALWP/+5VALWP	07/12/11	COMPAL	in order to trial run ISL6237 2'nd source,reserve PC239 in ISL6237 PIN5.	ADD PC239 (1U 0603 10V)	
5	P44	+VGA_CORE	07/12/11	COMPAL	Base on HW power budger,change the VGA_CORE high low side MOS and choke.	change PQ81 from A04466 to FDS6294,PQ82 from A04712 to A04456,PL32 from 1.8uH 9.5A to 1uH 21.3A	
6	P39	DC-IN / Precharge	07/12/11	COMPAL	base on customer spec no need CHARGE RTC, delete CHARGE RTC limit resister	Del PR210,PR211	
7	P46	CPU_CORE	07/12/14	COMPAL	EMI request to increase resister in CPU_CORE low side mos gate pin	ADD PR163(2.2 ohm),PR184(2.2ohm)	
8	P43	1.8VP	07/12/14	COMPAL	EMI request to increase resister in 1.8VP BOOT pin	Change PR340 from 0 ohm to 2.2 ohm	
9	P40	CHARGER	08/01/04	COMPAL	disable BQ24751 VIN detecte function	CHANGE PQ62 to @ and PR232 to @	
10	P40	CHARGER	08/02/12	COMPAL	EC have drop volotage in CHGVADJ,it will make the charge voltage not correct	CHANGE PR53 from 4.3k to 210k and PR54 from 10k to 499k	
11	P44	+VGA_CORE	08/02/12	COMPAL	Base on HW power budger,change the VGA_CORE output capacity	change PC301,PC307 from SF22001M300 S ELE CAP 220U 6.3V M F60(6.3X5.7) PXC to SGA20221150 S POLY C 220U 4V M D2 PSL LESR15M H1.9	
12							

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	28	EC_KB926/Reed Switch/BIOS/TPM	2007/11/14	Compal_HW	Change Board ID.	Change R459 to 8.2K ohm.	0.2
2	38	NB8P-SE_Straps	2007/11/14	Compal_HW	There is display issue on Discrete platform.	Not stuff R784.	0.2
3	32	DC/DC Interface	2007/11/19	Compal_HW	Sometime system can't detect USB device.	Change R522 pull high to +5VALW. (for SUSP)	0.2
4	15	CRT Conn/LCD Conn	2007/12/03	Compal_HW	Support BIST and LCD detect function for LCD panel.	Add nets: LCD_DET# , BIST and Modify the pin definition of JP4.	0.2
5	23	Audio Codec_ALC268	2007/12/03	Compal_EMI	There are EMI issue on DMIC_DATA and DMIC_CLK.	Add R933, R934, C1189, C1190 for EMI.	0.2
6	25	OZ129_Card Reader/1394	2007/12/03	Compal_HW	OZ129 has power sequence and leakage issue.	Update the circuit of OZ129 on Page 25.	0.2
7	28	EC_KB926/Reed Switch/BIOS/TPM	2007/12/03	Compal_HW	Can't Wake up on LAN.	Change R464 pull high to +3VALW for WOL.	0.2
8	28	EC_KB926/Reed Switch/BIOS/TPM	2007/12/03	Compal_HW	Support Wake up from USB Port and replace USB HUB port arrangement.	Add USB_EN# to enable USB power swith.	0.2
9	29	PWR_OK/BTN/KB/TP	2007/12/13	Compal_HW	510N# shout down issue.	Change R493 pull down to GND and del R494.	0.2
10	29	PWR_OK/BTN/KB/TP	2007/12/03	Compal_HW	Int. Keyboard can't work.	Modify the pin definition of JKB1.	0.2
11	30	USB/1394 Conn	2007/12/03	Compal_HW	Support Wake up from USB Port.	1.U32, U33, U34, U51 change input voltage to +5VALW. 2.JUSBP1-5 change USB differential pair from ICH8M.	0.2
12	32	DC/DC Interface	2007/12/03	Compal_HW	VGA_PWG0D sequence issue.	1.Change R551 pull high to +5VALW and don't stuff R551. 2.Change VGA_PWG0D to PR352 pin2.	0.2
13	15	CRT Conn/LCD Conn	2007/12/13	Compal_HW	Dell 17" LCD Panel gray color issue.	Add Q83, Q84, R942, R943, C1191-C1194 for Dell 17" panel.	0.2
14	22	Realtek RTL8111C-GR	2007/12/13	Compal_EMI	These is EMI issue on Transformer.	Add R945-R952 and C1195-C1198 for EMI.	0.2
15	22	Realtek RTL8111C-GR	2007/12/18	Compal_HW	RJ-45: LED support "link" and "activity" status.	1.Change the connector of JLAN1. 2.Add D41, D42, D43, D44, R953, R954, R955.	0.2
16	15	CRT Conn/LCD Conn	2007/12/19	Compal_EMI	EMI' request.	Del CRT_GND, R105, R107 for EMI.	0.2
17	31	USB Hub/Camera/Felcia/FP/BT	2007/12/24	Compal_HW	Finfer Print assermble FFC.	Modify the definition of JFP1.	
18							
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JAL60 Power Block

