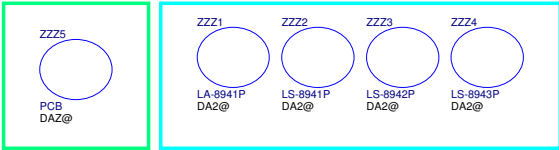


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Model Name : Q1VZC

File Name :LA-8941P

BOM P/N:43



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Q1VZC M/B Schematics Document

Intel Sandy Bridge ULV Processor + Panther Point PCH

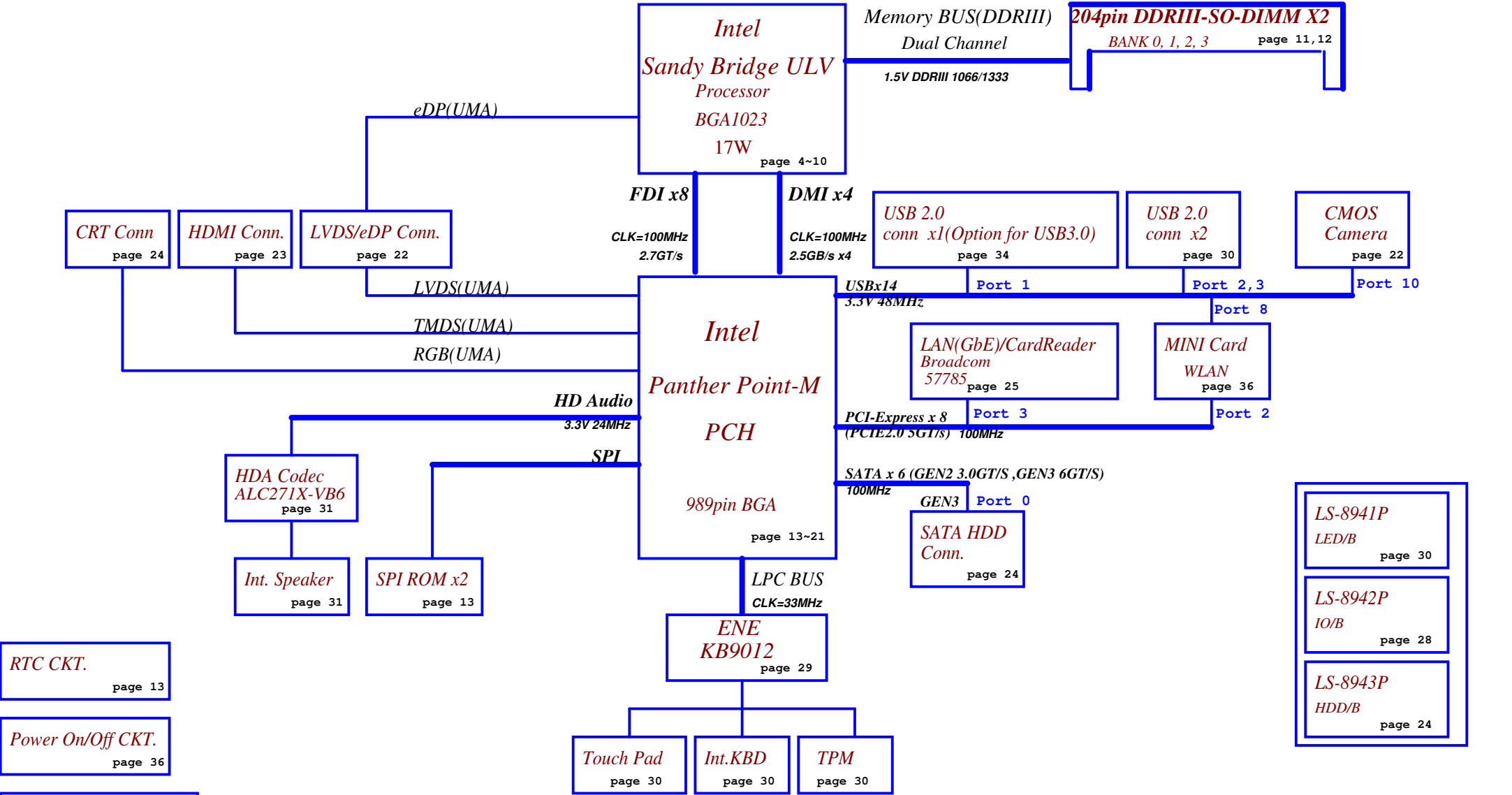
2012-04-19

REV:1.0

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			Q1VZC M/B LA-8941P Schematic	1.0
			Date: Friday, April 20, 2012	Sheet 1 of 45

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Model Name : Q1VZC
File Name :LA-8941P



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				Custom	1.0
				Document Number	
				Q1VZC M/B LA-8941P Schematic	
				Date:	Friday, April 20, 2012
				Sheet	2 of 45

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+VCCSUS3_3	+3VALW to +VCCSUS3_3 power rail for PCH (Short Jump)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VREF_SUS	+5VALW to +5VREF_SUS power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

PCH SM Bus address

Device	Address
ChannelA DIMM0 A0	1010 000X JDIMM1(STD)
ChannelB DIMM0 B0	1010 010X JDIMM2(REV)

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

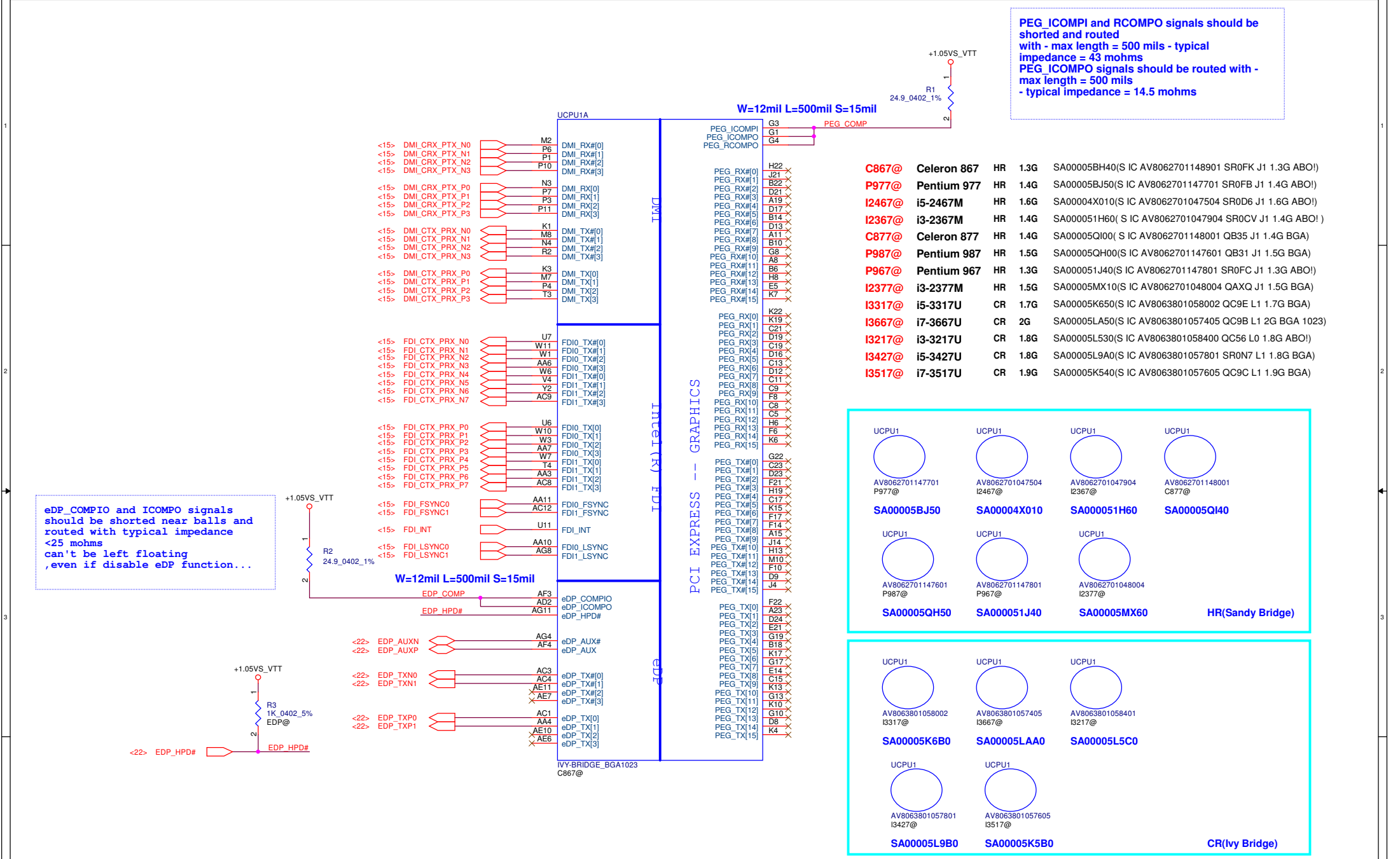
USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	
		1	USB 2.0(Options for USB3.0)
	UHCI1	2	USB port(Left 2.0)
		3	USB Port(Left 2.0)
	UHCI2	4	
		5	
EHCI2	UHCI3	6	
		7	
	UHCI4	8	Mini Card(WLAN)
		9	
	UHCI5	10	Camera
		11	
	UHCI6	12	
		13	

BTO Option Table

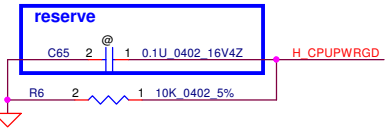
BTO Item	BOM Structure
Celeron 867	C867@
Pentium 977	P977@
Unpop	@
eDP Panel	EDP@
LVDS Panel	LVDS@
Connector	CONN@
USB3 Only	USB3@
Deep S3	DS3@
Normal S3	S3@
Intel i5/i7 CPU only	I57@
Celeron/Pentium/i3 CPU only	CP3@

USB 3.0	Port	
XHCI	1	
	2	USB Port(Right 3.0)
	3	
	4	



PCH->CPU
UNCOREPWROK:非CORE外的電OK
SM_DRAMPWROK:DRAM power ok
RESET#:都ok後請CPU做reset

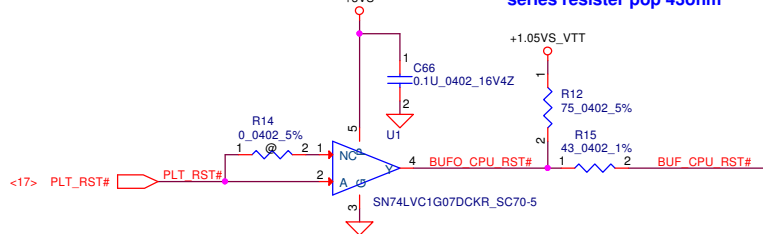
Follow DG 1.5 & Tacoma_Fall2 1.0



Follow DG 1.5 & Tacoma_Fall2 1.0

Buffered reset to CPU

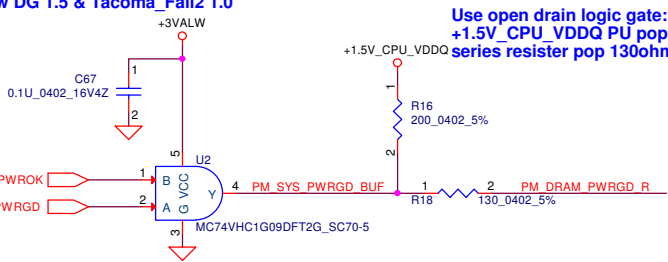
Use open drain logic gate:
+1.05VS_VTT PU pop 75ohm
series resistor pop 43ohm



RESET#:都ok後請CPU做reset

Follow DG 1.5 & Tacoma_Fall2 1.0

Use open drain logic gate:
+1.5V_CPU_VDDQ PU pop 200ohm
series resistor pop 130ohm

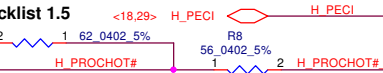


PROC_SELECT#
PH VCPLL and connect to PCH DF_TV5

偵測CPU有無安裝

XBOX 三缸功能

follow Checklist 1.5



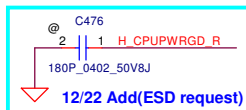
<18> H_THRMTRIP#

<15> H_PM_SYNC

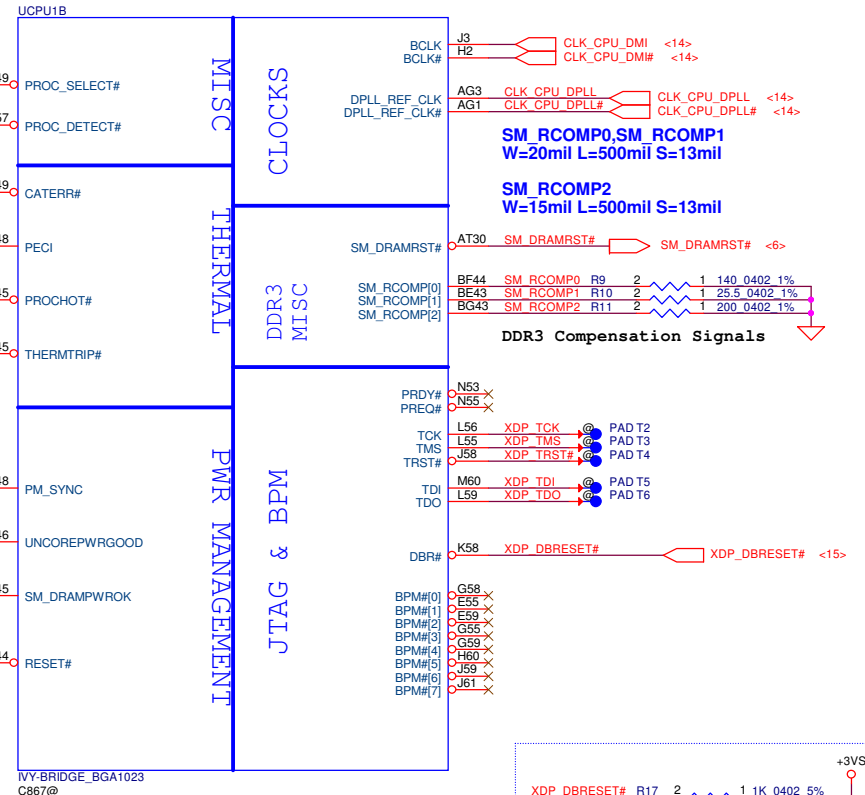
UNCOREPWROK:非CORE外的電OK

SM_DRAMPWROK:DRAM power ok

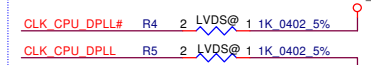
BUF_CPU_RST#



12/22 Add(ESD request)



0921 LVDS@->->



Checklist 1.5 P.67 Graphis Disable Guide
eDP disable:
DPLL_REF_SSCLK PD 1K 5% to GND
DPLL_REF_SSCLK# PU 1K 5% to +1.05VS_VTT

SM_RCOMP0,SM_RCOMP1
W=20mil L=500mil S=13mil

SM_RCOMP2
W=15mil L=500mil S=13mil

SM_DRAMRST#

SM_RCOMP0, SM_RCOMP1, SM_RCOMP2

DDR3 Compensation Signals

PRDY#, PREQ#, TCK, TMS, TRST#, TDI, TDO

XDP TCK, XDP TMS, XDP TRST#, XDP TDI, XDP TDO

XDP DBRESET#

XDP DBRESET#

XDP DBRESET#

XDP DBRESET#

XDP DBRESET#

XDP DBRESET#

XDP DBRESET#

XDP DBRESET#

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XDP DBRESET#

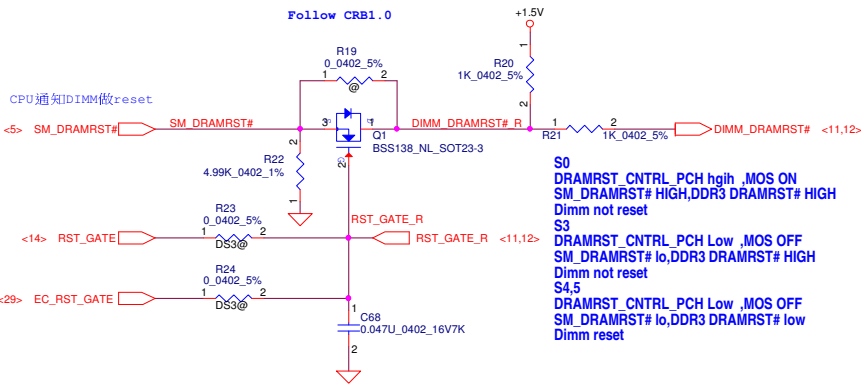
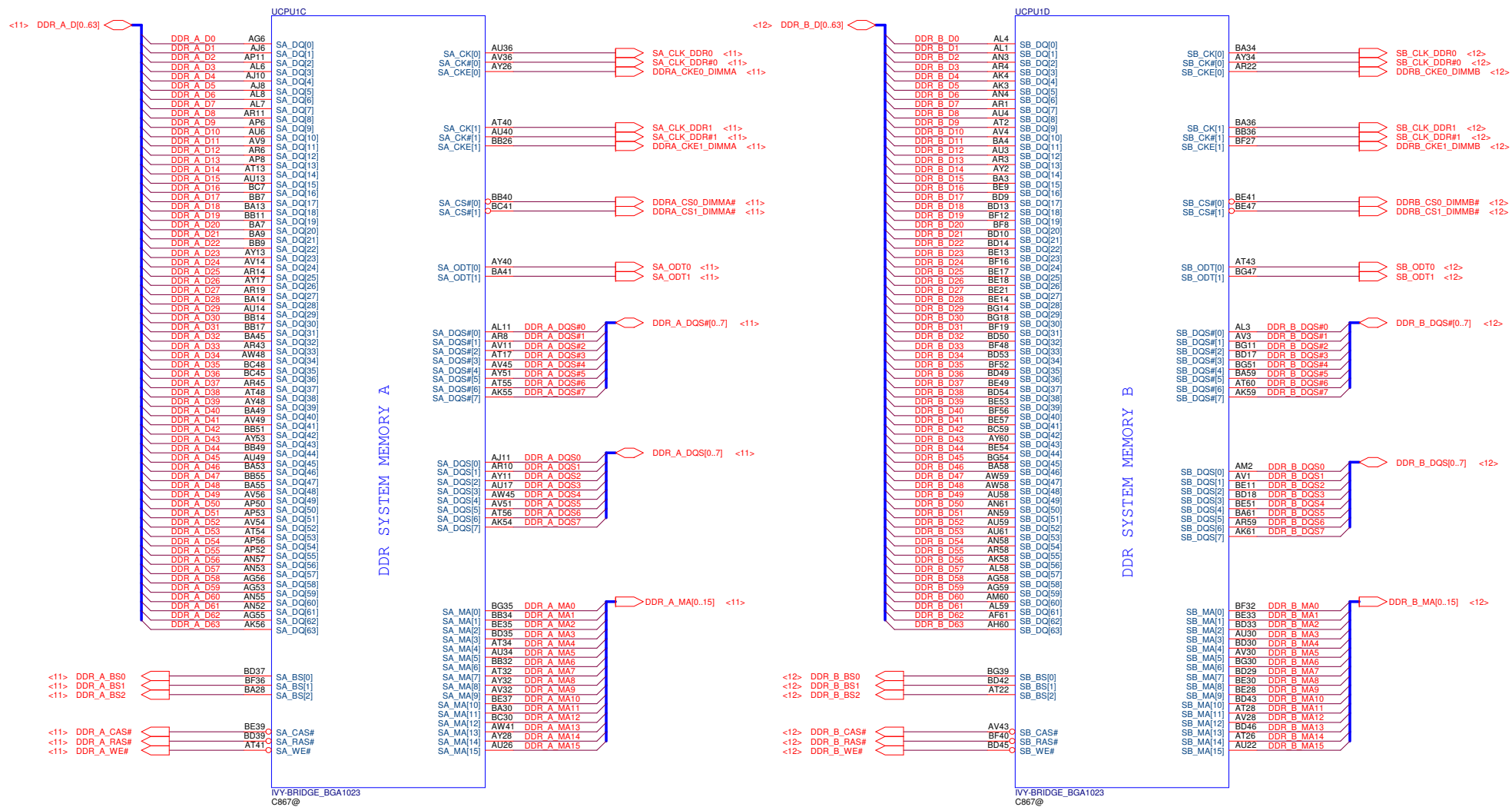
XDP DBRESET#

XDP DBRESET#

XDP DBRESET#

XDP DBRESET#

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Size Custom	Document Number	Rev		1.0
Date:	Friday, April 20, 2012	Sheet	5 of 45	



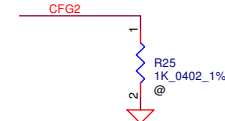
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			Q1VZC M/B LA-8941P Schematic		1.0	
Date:			Friday, April 20, 2012		Sheet 6 of 45	



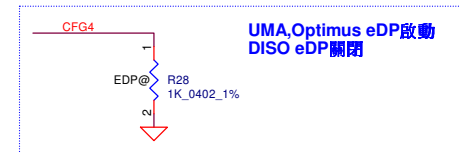
These pins are for solder joint reliability and non-critical to function. For BGA only.

DC_TEST_A4
DC_TEST_C4
DC_TEST_D3
DC_TEST_D1
DC_TEST_A58
DC_TEST_A59
DC_TEST_C59
DC_TEST_A61
DC_TEST_C61
DC_TEST_D61
DC_TEST_BE61
DC_TEST_BE59
DC_TEST_BG61
DC_TEST_BG59
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DC_TEST_BE3
DC_TEST_BG1
DC_TEST_BE1
DC_TEST_BD1

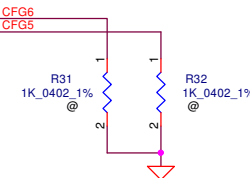
CFG Straps for Processor



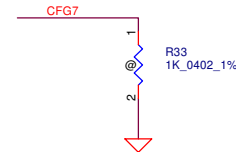
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed



eDP enable	
CFG4	★ 1: Disable 0: Enable



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) 1x16 PCI Express ★ 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express



PEG DEFER TRAINING Tacoma_Fall2 1.0 P.12	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

INTEL Recommend VCC
4*470UF,12*22uF(0805) and 35*2.2uF(0402)
PD0.8
CAP at P.51

ULV type
DC 33A

UCPU1F

POWER

8.5A

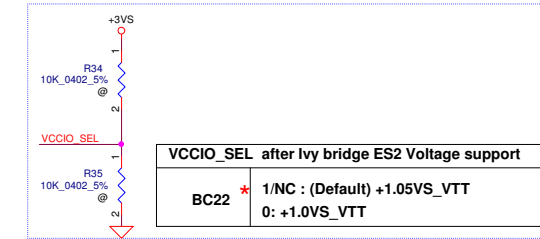
+CPU_CORE

+1.05VS_VTT

For DDR

INTEL Recommend VCCIO
2*330UF,10*10uF(0603) and 26*1uF(0402)
PD0.8
CAP at P.51

For PEG

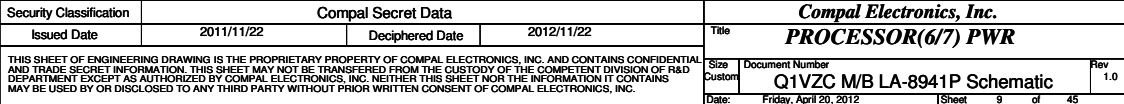


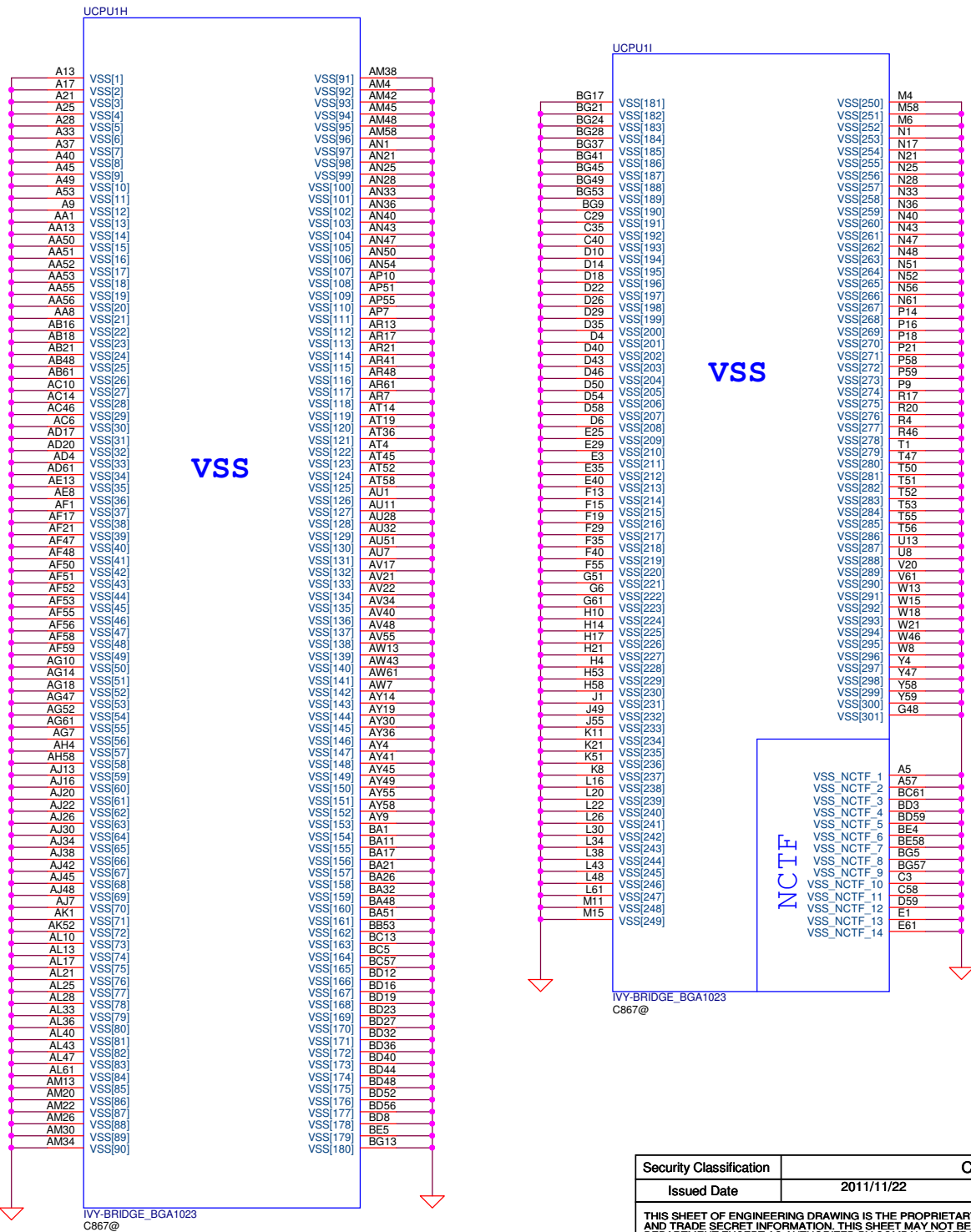
Place the PU resistors close to CPU

Place the PU resistors close to VR

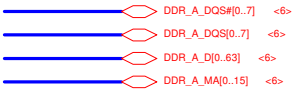
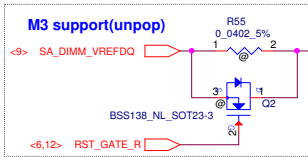
Should change to connect form power circuit & layout differential with VCCIO_SENSE.

Check list 1.5

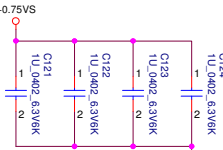
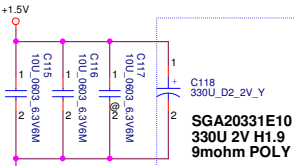
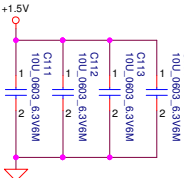
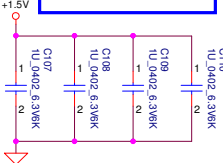




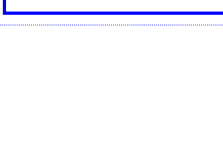
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Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203,204



All VREF traces should have 10 mil trace width

<6> DDRA_CKE0_DIMMA# DDRA_CKE0_DIMMA#

<6> DDR_A_BS2 DDR_A_BS2

<6> SA_CLK_DDR0 SA_CLK_DDR0

<6> SA_CLK_DDR#0 SA_CLK_DDR#0

<6> DDR_A_BS0 DDR_A_BS0

<6> DDR_A_WE# DDR_A_WE#

<6> DDR_A_CAS# DDR_A_CAS#

<6> DDRA_CS1_DIMMA# DDRA_CS1_DIMMA#

DDR A D32

DDR A D33

DDR A DQS#4

DDR A DQS4

DDR A D34

DDR A D35

DDR A D40

DDR A D41

DDR A D42

DDR A D43

DDR A D48

DDR A D49

DDR A DQS#6

DDR A DQS6

DDR A D50

DDR A D51

DDR A D56

DDR A D57

DDR A D58

DDR A D59

DDR A D60

DDR A D61

DDR A D62

DDR A D63

DDR A D64

DDR A D65

DDR A D66

DDR A D67

DDR A D68

DDR A D69

DDR A D70

DDR A D71

DDR A D72

DDR A D73

DDR A D74

DDR A D75

DDR A D76

DDR A D77

DDR A D78

DDR A D79

DDR A D80

DDR A D81

DDR A D82

DDR A D83

DDR A D84

DDR A D85

DDR A D86

DDR A D87

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DDR A D91

DDR A D92

DDR A D93

DDR A D94

DDR A D95

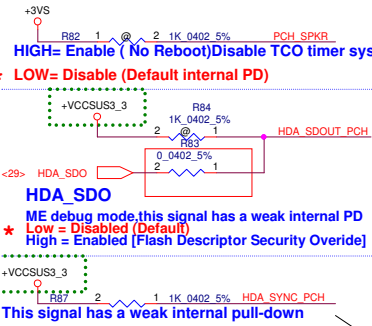
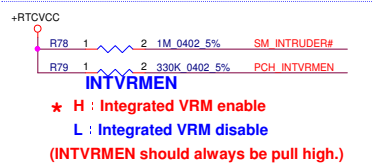
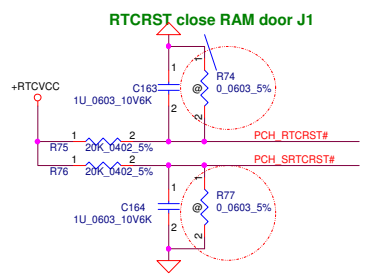
Channel A

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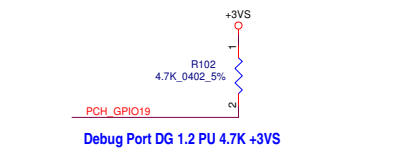
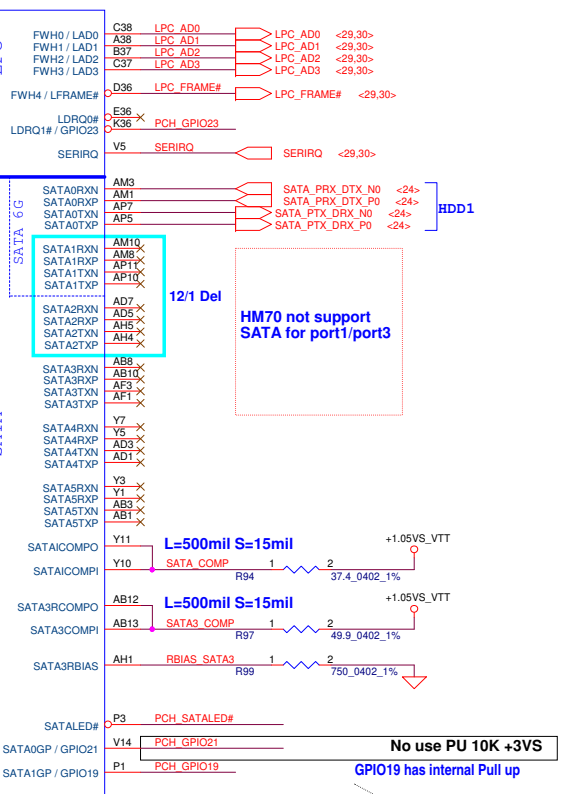
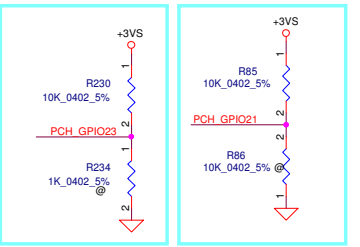
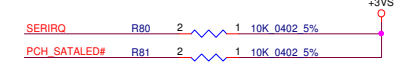
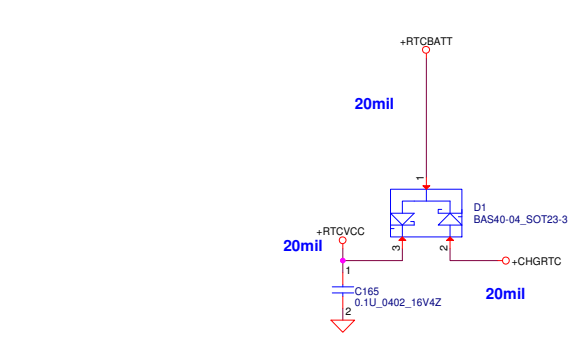
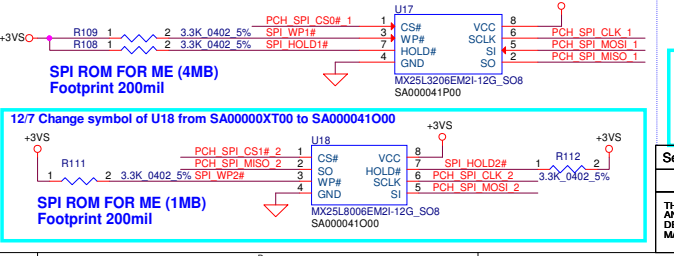
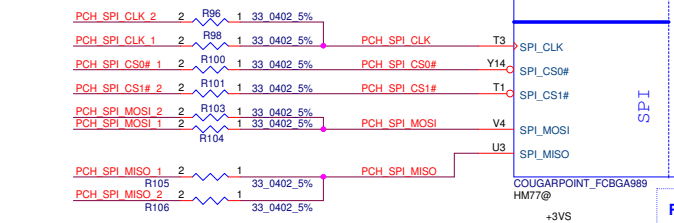
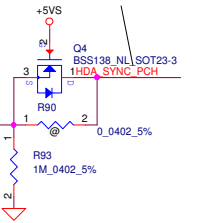
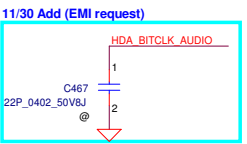
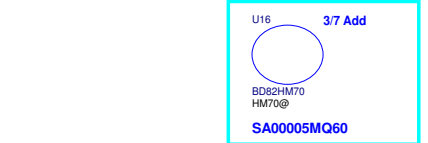
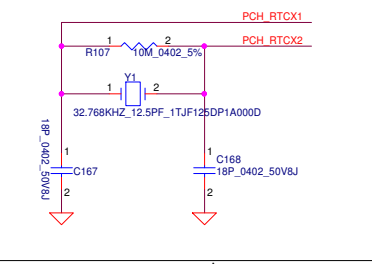
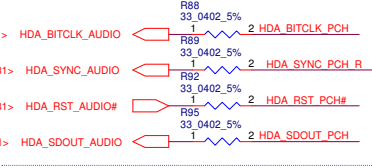
1/3 Modify

DIMM_1 Standard H:4.0mm

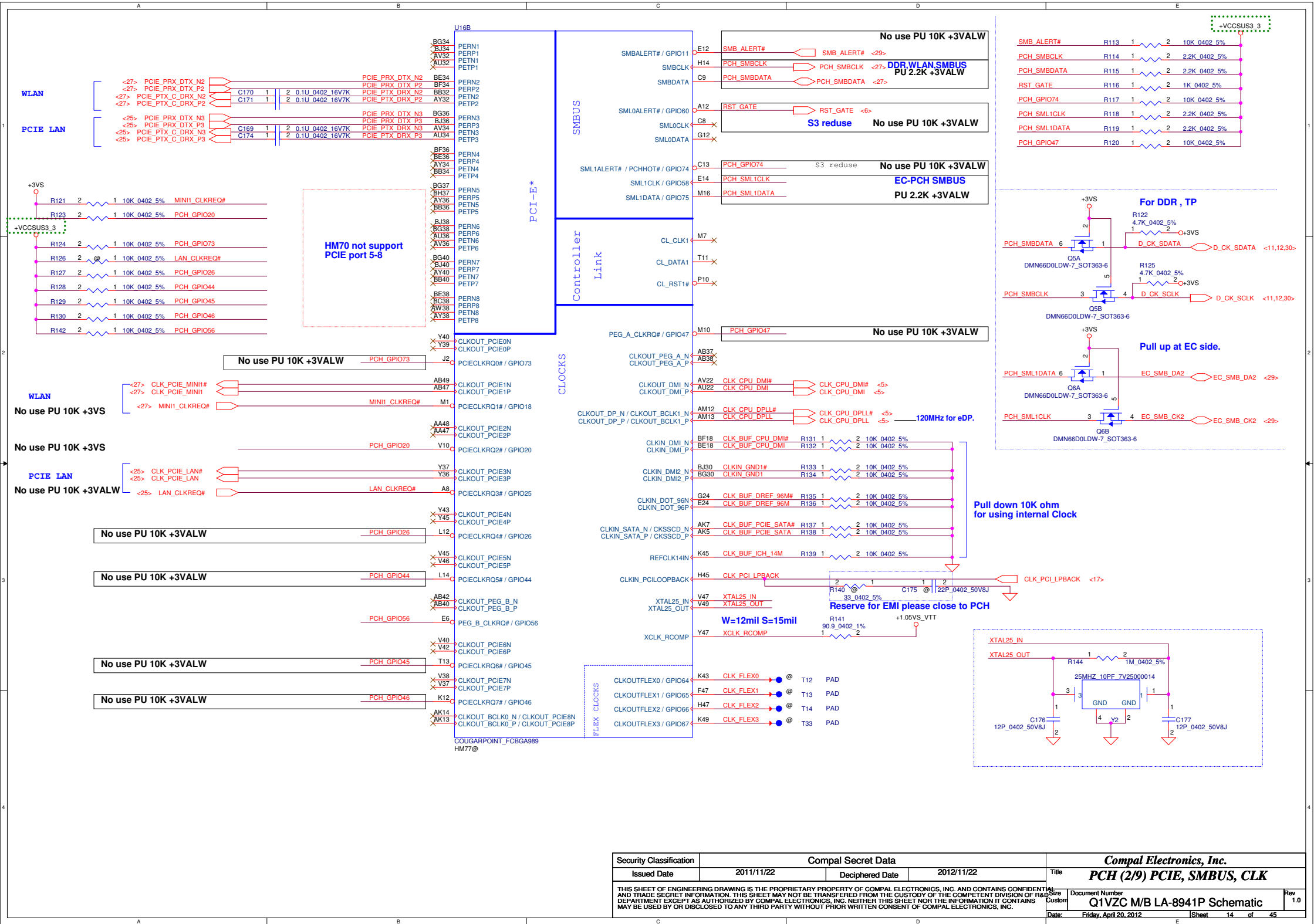
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				Q1VZC M/B LA-8941P Schematic
				Rev
				1.0
				Date: Friday, April 20, 2012
				Sheet 11 of 45



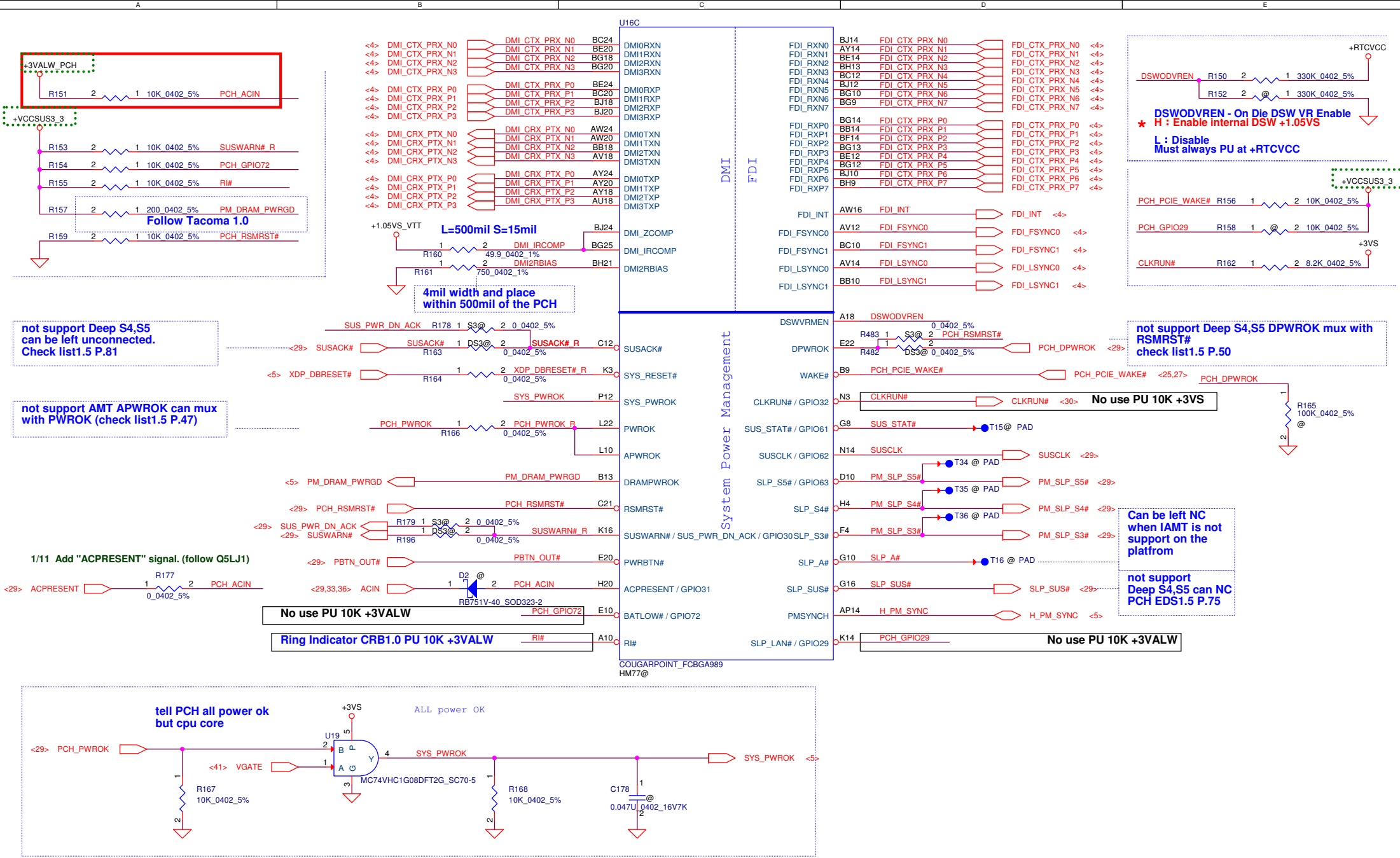
On Die PLL VR Select is supplied by
★1.5V when sampled high
1.8V when sampled low
Needs to be pulled High for Huron River platform



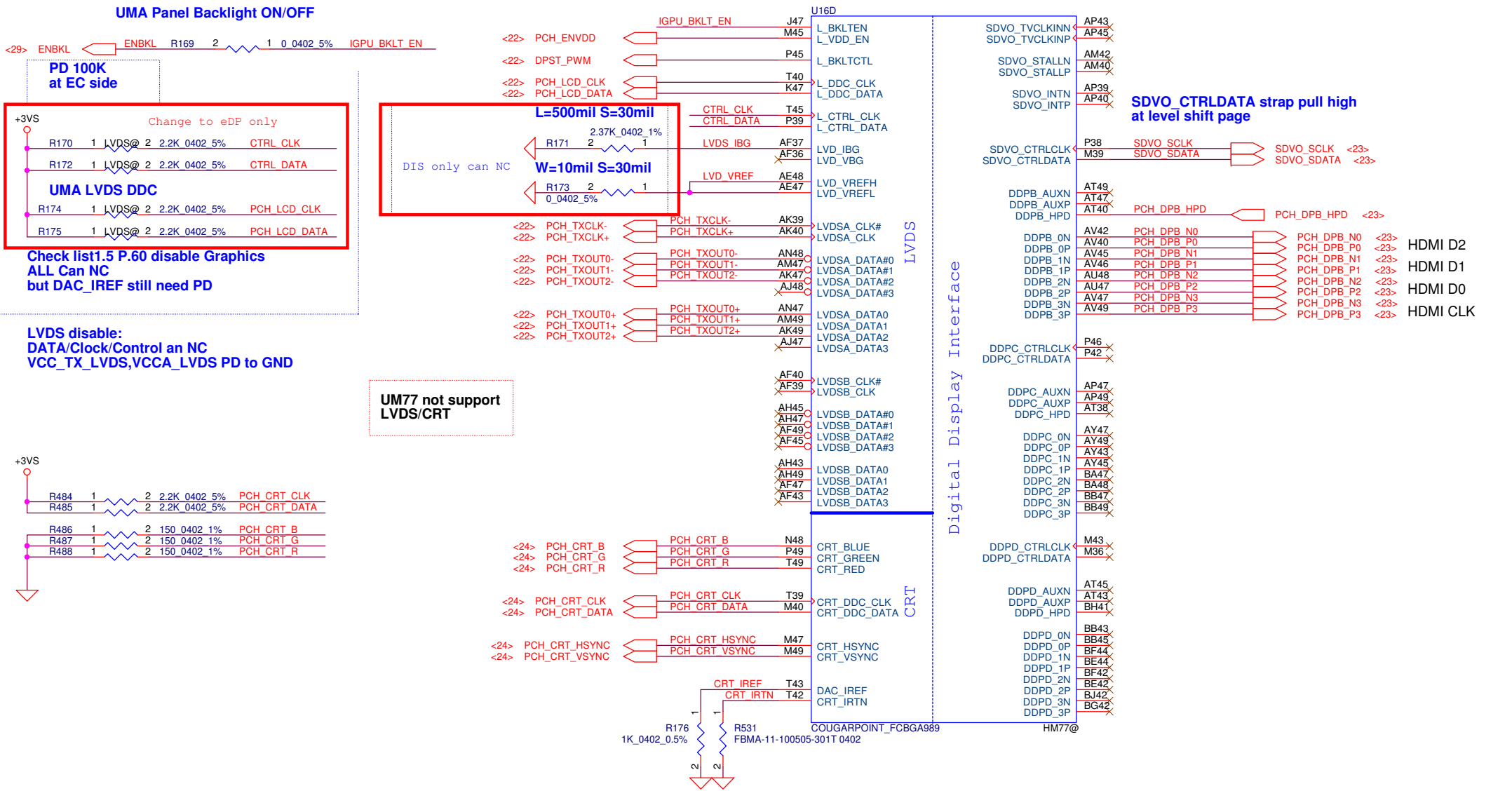
Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
★ SPI	1	1



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Issued Date	2011/11/22	Deciphered Date	2012/11/22	Title	
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				Custom	Q1VZC M/B LA-8941P Schematic
				Date:	Friday, April 20, 2012
				Sheet	14 of 45



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Size Custom	Document Number			Q1VZC M/B LA-8941P Schematic		Rev 1.0
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				Q1VZC M/B LA-8941P Schematic	1.0	
				Date:	Friday, April 20, 2012	Sheet 16 of 45

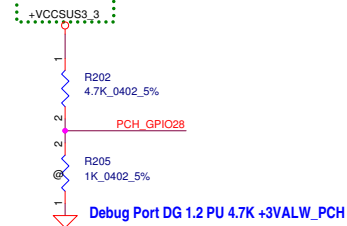
HDA_SYNC PH(PLL =+1.5VS)

GPIO28

On-Die PLL Voltage Regulator

This signal has a weak internal pull up

- * H : On-Die PLL voltage regulator enable
- L : On-Die PLL Voltage Regulator disable



Fan Tachometer Inputs
TACH1~7 only on server
can insted to GPIO

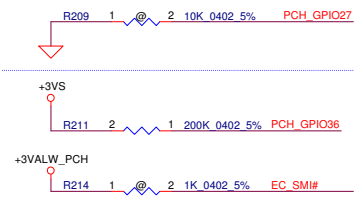
No use PU 10K +3VS	PCH_GPIO00	T7
No use PU 10K +3VS	PCH_GPIO01	A42
No use PU 10K +3VS	PCH_GPIO06	H36
No use PU 10K +3VS	<29> EC_SCI#	E38
No use PU 10K +3VALW	<29> EC_SMI#	C10
No use PU +3VALW	PCH_GPIO12	C4
No use PU +3VALW	<29> EC_LID_OUT#	G2
No use PU +3VS	PCH_GPIO16	U2
No use PU +3VS	PCH_GPIO17	D40
No use PU 10K +3VS RAM flag	PCH_GPIO22	T5
No use PU +3VALW DDR3/DDR3L	PCH_GPIO24	E8
No use PD 10K to GND	PCH_GPIO27	E16
No use PU 10K +3VALW	PCH_GPIO28	P8
No use PU 10K +3VS BT ON/OFF	PCH_GPIO34	K1
No use can NC	PCH_GPIO35	K4
Can't PU	PCH_GPIO36	V8
Can't PU	PCH_GPIO37	M5
No use PU 10K +3VS	PCH_GPIO38	N2
No use PU 10K +3VS RAM flag	PCH_GPIO39	M3
No use PU 10K +3VS	PCH_GPIO48	V13
SATA5GP&TEMP_ALERT# CRB PU 10K +3VS	PCH_GPIO49	V3
No use PU +3VALW	PCH_GPIO57	D6

Deep S4,S5 wake event signal

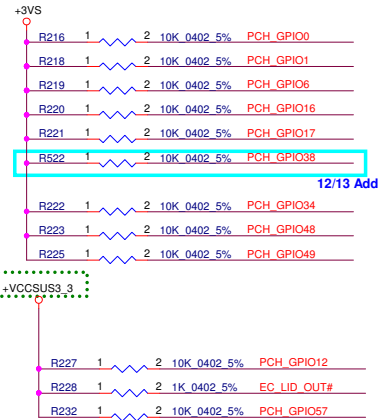
RTC alarm,Power BTN,GPIO27

PCH_GPIO27 (Have internal Pull-High)

Deep S4,S5 wake event signal



SATA2GP/GPIO36 & SATA3GP/GPIO37
Sampled at Rising edge of PWROK.
Weak internal pull-down.
(weak internal pull-down is disabled
after PLTRST# de-asserts)
NOTE: This signal should NOT be
pulled high when strap is sampled



12/13 Add

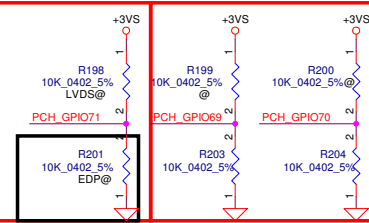
GPIO24 Unmultiplexed
NOTE: GPIO24 configuration
register bits are not cleared by
CF9h reset event.

CRB1.0 PU 10K to +3VALW

GPIO36/GPIO37 is Strap functionality
that requires internal pull down to be sampled at rising PWROK.
When uses as SATA2GP/SATA3GP for mechanical presence detect
-use a external pull up 150K-200K ohm to Vcc3_3
When used as GP input
-ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA*GP
-use 8.2K-10K pull-down
check list page 47

11/21 EDP->POP

LVDS/eDP	GPIO71
LVDS	1
eDP	0



GPIO

NCIF

TACH4 / GPIO68
TACH5 / GPIO69
TACH6 / GPIO70
TACH7 / GPIO71

A20GATE
PECI
RCIN#
PROC_PWRGD
THRMTRIP#
INIT3_3V#

NC_1
NC_2
NC_3
NC_4
NC_5

VSS_NCTF_15
VSS_NCTF_16
VSS_NCTF_17
VSS_NCTF_18
VSS_NCTF_19
VSS_NCTF_20
VSS_NCTF_21
VSS_NCTF_22
VSS_NCTF_23
VSS_NCTF_24
VSS_NCTF_25
VSS_NCTF_26
VSS_NCTF_27
VSS_NCTF_28
VSS_NCTF_29
VSS_NCTF_30
VSS_NCTF_31
VSS_NCTF_32

BG2
BG48
BH3
BH4
BJ4
BJ44
BJ45
BJ46
BJ5
BJ6
C2
C48
D1
D49
E1
E49
F1
F49

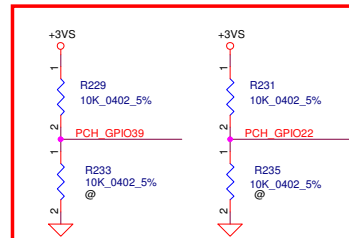
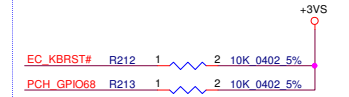
COUGARPOINT_FCBGA989
HM77@

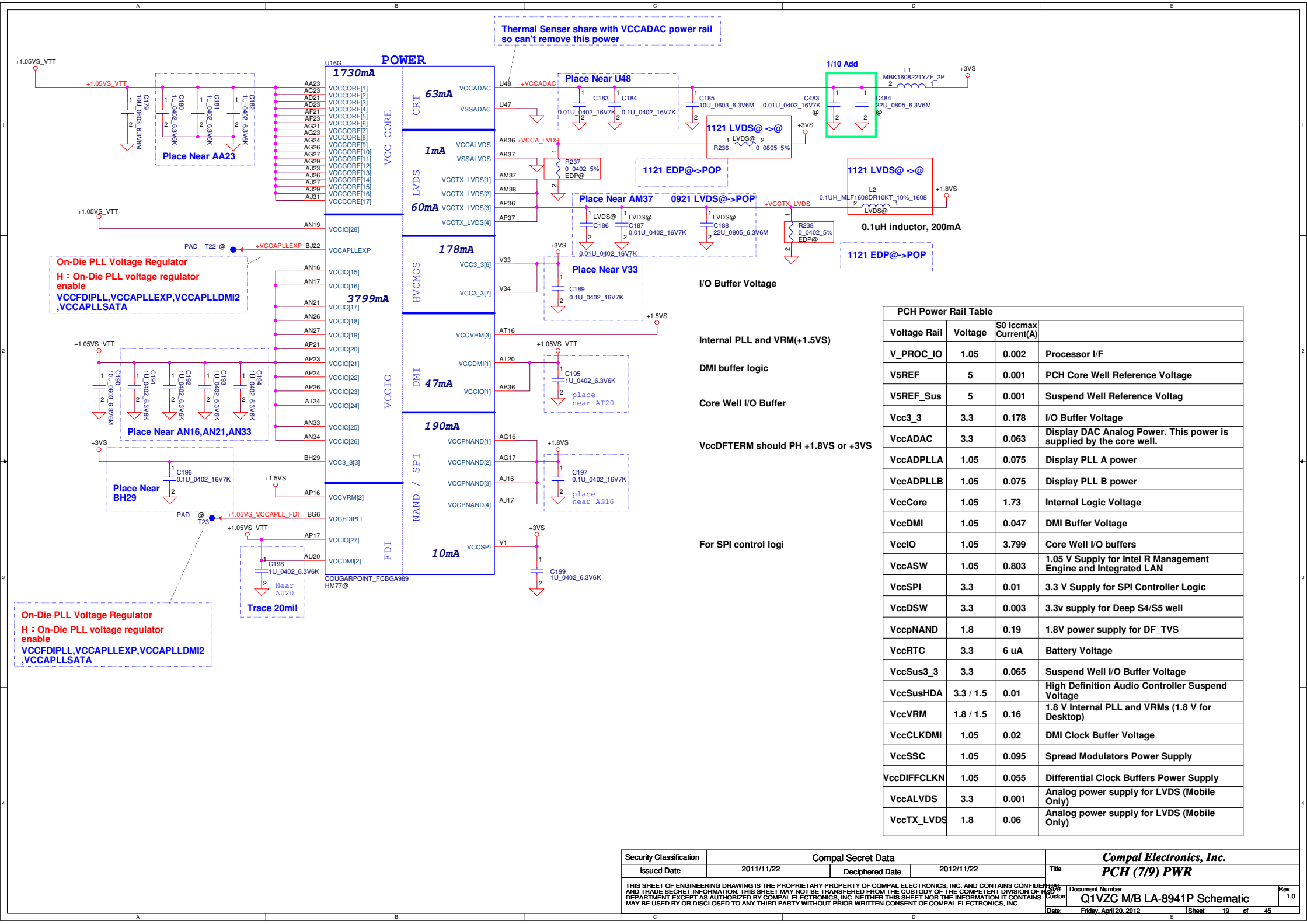
INIT3_3V Checklist1.5 P.69
This signal has weak internal
PU, can't pull low,leave NC

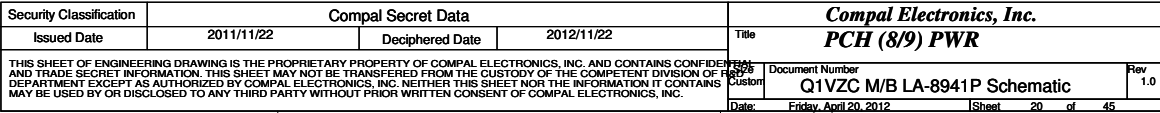
TS_VSS1~4
PD to GND

9/15 Layout
request remove
Test point
They will route
by itself

PECI CPU-EC
CTRL+ALT+DEL
non CPU power ok
130c shut down







H5			U16H		
AA17	VSS[0]				
AA2	VSS[1]				
AA3	VSS[2]				
AA33	VSS[3]				
AA34	VSS[4]				
AB11	VSS[5]				
AB14	VSS[6]				
AB39	VSS[7]				
AB4	VSS[8]				
AB43	VSS[9]				
AB5	VSS[10]				
AB7	VSS[11]				
AC19	VSS[12]				
AC2	VSS[13]				
AC21	VSS[14]				
AC24	VSS[15]				
AC33	VSS[16]				
AC34	VSS[17]				
AC48	VSS[18]				
AD10	VSS[19]				
AD11	VSS[20]				
AD12	VSS[21]				
AD13	VSS[22]				
AD19	VSS[23]				
AD24	VSS[24]				
AD26	VSS[25]				
AD27	VSS[26]				
AD33	VSS[27]				
AD34	VSS[28]				
AD36	VSS[29]				
AD37	VSS[30]				
AD38	VSS[31]				
AD39	VSS[32]				
AD4	VSS[33]				
AD40	VSS[34]				
AD42	VSS[35]				
AD43	VSS[36]				
AD45	VSS[37]				
AD46	VSS[38]				
AD8	VSS[39]				
AE2	VSS[40]				
AE3	VSS[41]				
AF10	VSS[42]				
AF12	VSS[43]				
AD14	VSS[44]				
AD16	VSS[45]				
AF16	VSS[46]				
AF19	VSS[47]				
AF24	VSS[48]				
AF26	VSS[49]				
AF27	VSS[50]				
AF29	VSS[51]				
AF31	VSS[52]				
AF38	VSS[53]				
AF4	VSS[54]				
AF42	VSS[55]				
AF46	VSS[56]				
AF5	VSS[57]				
AF7	VSS[58]				
AF8	VSS[59]				
AG19	VSS[60]				
AG2	VSS[61]				
AG31	VSS[62]				
AG48	VSS[63]				
AH11	VSS[64]				
AH3	VSS[65]				
AH36	VSS[66]				
AH39	VSS[67]				
AH40	VSS[68]				
AH42	VSS[69]				
AH46	VSS[70]				
AH7	VSS[71]				
AJ19	VSS[72]				
AJ21	VSS[73]				
AJ24	VSS[74]				
AJ33	VSS[75]				
AJ34	VSS[76]				
AK12	VSS[77]				
AK3	VSS[78]				
AK3	VSS[79]				

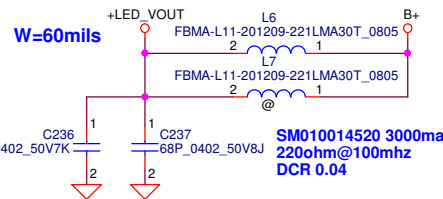
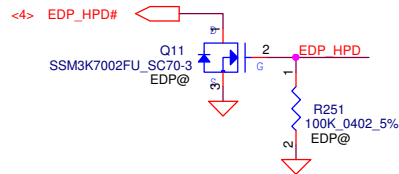
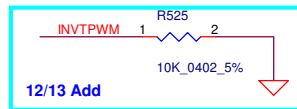
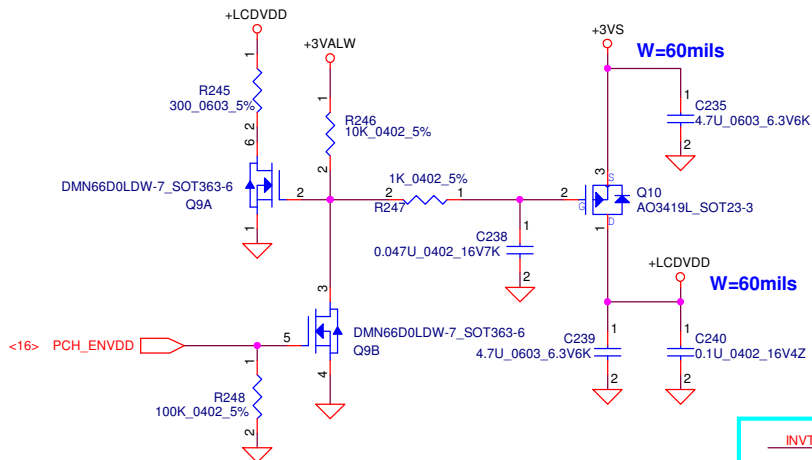
COUGARPOINT_FCBGA989
HM77@

U16I		
AY4	VSS[159]	
AY42	VSS[160]	
AY46	VSS[161]	
AY8	VSS[162]	
B11	VSS[163]	
B15	VSS[164]	
B19	VSS[165]	
B23	VSS[166]	
B27	VSS[167]	
B31	VSS[168]	
B35	VSS[169]	
B39	VSS[170]	
B7	VSS[171]	
F45	VSS[172]	
BB12	VSS[173]	
BB16	VSS[174]	
BB20	VSS[175]	
BB22	VSS[176]	
BB24	VSS[177]	
BB28	VSS[178]	
BB30	VSS[179]	
BB38	VSS[180]	
BB4	VSS[181]	
BB46	VSS[182]	
BC14	VSS[183]	
BC18	VSS[184]	
BC2	VSS[185]	
BC22	VSS[186]	
BC26	VSS[187]	
BC32	VSS[188]	
BC34	VSS[189]	
BC36	VSS[190]	
BC40	VSS[191]	
BC42	VSS[192]	
BC48	VSS[193]	
BD46	VSS[194]	
BD5	VSS[195]	
BE22	VSS[196]	
BE26	VSS[197]	
BE40	VSS[198]	
BF10	VSS[199]	
BF12	VSS[200]	
BF16	VSS[201]	
BF20	VSS[202]	
BF22	VSS[203]	
BF24	VSS[204]	
BF26	VSS[205]	
BF28	VSS[206]	
BD3	VSS[207]	
BF30	VSS[208]	
BF38	VSS[209]	
BF40	VSS[210]	
BF8	VSS[211]	
BG17	VSS[212]	
BG21	VSS[213]	
BG33	VSS[214]	
BG44	VSS[215]	
BG8	VSS[216]	
BH11	VSS[217]	
BH15	VSS[218]	
BH17	VSS[219]	
BH19	VSS[220]	
BH27	VSS[221]	
BH31	VSS[222]	
BH33	VSS[223]	
BH35	VSS[224]	
BH39	VSS[225]	
BH43	VSS[226]	
BH7	VSS[227]	
D3	VSS[228]	
D12	VSS[229]	
D16	VSS[230]	
D18	VSS[231]	
D22	VSS[232]	
D24	VSS[233]	
D26	VSS[234]	
D30	VSS[235]	
D32	VSS[236]	
D34	VSS[237]	
D38	VSS[238]	
D42	VSS[239]	
D8	VSS[240]	
E18	VSS[241]	
E26	VSS[242]	
G18	VSS[243]	
G20	VSS[244]	
G28	VSS[245]	
G28	VSS[246]	
G36	VSS[247]	
G48	VSS[248]	
H12	VSS[249]	
H18	VSS[250]	
H22	VSS[251]	
H24	VSS[252]	
H26	VSS[253]	
H30	VSS[254]	
H32	VSS[255]	
H34	VSS[256]	
F3	VSS[257]	
	VSS[258]	

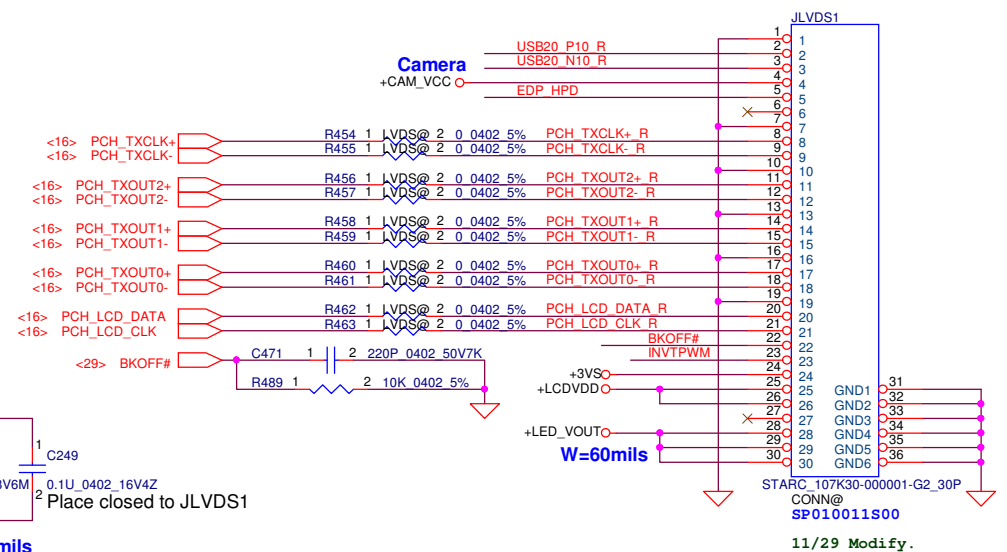
COUGARPOINT_FCBGA989
HM77@

VSS[259]	K18
VSS[260]	K26
VSS[261]	K39
VSS[262]	K46
VSS[263]	K7
VSS[264]	L18
VSS[265]	L2
VSS[266]	L20
VSS[267]	L26
VSS[268]	L28
VSS[269]	L36
VSS[270]	L48
VSS[271]	M12
VSS[272]	P16
VSS[273]	M18
VSS[274]	M22
VSS[275]	M24
VSS[276]	M30
VSS[277]	M32
VSS[278]	M34
VSS[279]	M38
VSS[280]	M4
VSS[281]	M42
VSS[282]	M46
VSS[283]	M6
VSS[284]	N18
VSS[285]	P30
VSS[286]	N47
VSS[287]	P11
VSS[288]	P18
VSS[289]	T33
VSS[290]	P40
VSS[291]	P43
VSS[292]	P47
VSS[293]	P7
VSS[294]	R2
VSS[295]	R48
VSS[296]	T12
VSS[297]	T31
VSS[298]	T37
VSS[299]	T4
VSS[300]	W34
VSS[301]	T46
VSS[302]	T47
VSS[303]	T6
VSS[304]	V11
VSS[305]	V17
VSS[306]	V26
VSS[307]	V27
VSS[308]	V29
VSS[309]	V31
VSS[310]	V36
VSS[311]	V39
VSS[312]	V43
VSS[313]	V7
VSS[314]	W17
VSS[315]	W19
VSS[316]	W2
VSS[317]	W27
VSS[318]	W48
VSS[319]	Y12
VSS[320]	Y38
VSS[321]	Y4
VSS[322]	Y42
VSS[323]	Y46
VSS[324]	Y8
VSS[325]	BG29
VSS[326]	N24
VSS[329]	AJ3
VSS[330]	AD47
VSS[331]	B43
VSS[333]	BE10
VSS[334]	BG41
VSS[335]	G14
VSS[337]	H16
VSS[338]	T36
VSS[340]	BG22
VSS[342]	BG24
VSS[343]	C22
VSS[344]	AP13
VSS[345]	M14
VSS[346]	AP3
VSS[347]	AP1
VSS[348]	BE16
VSS[349]	BC16
VSS[350]	BG28
VSS[351]	BJ28
VSS[352]	

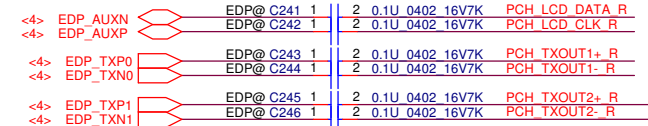
LCD POWER CIRCUIT



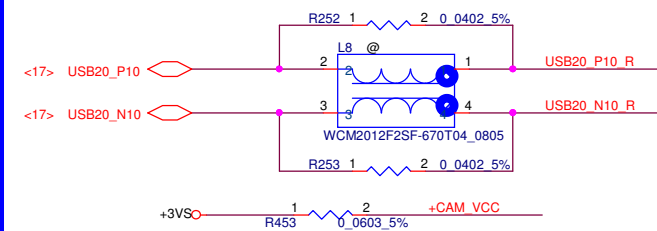
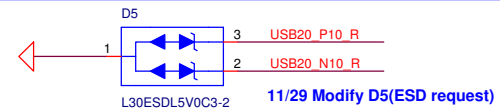
LCD/LED PANEL Conn.



eDP

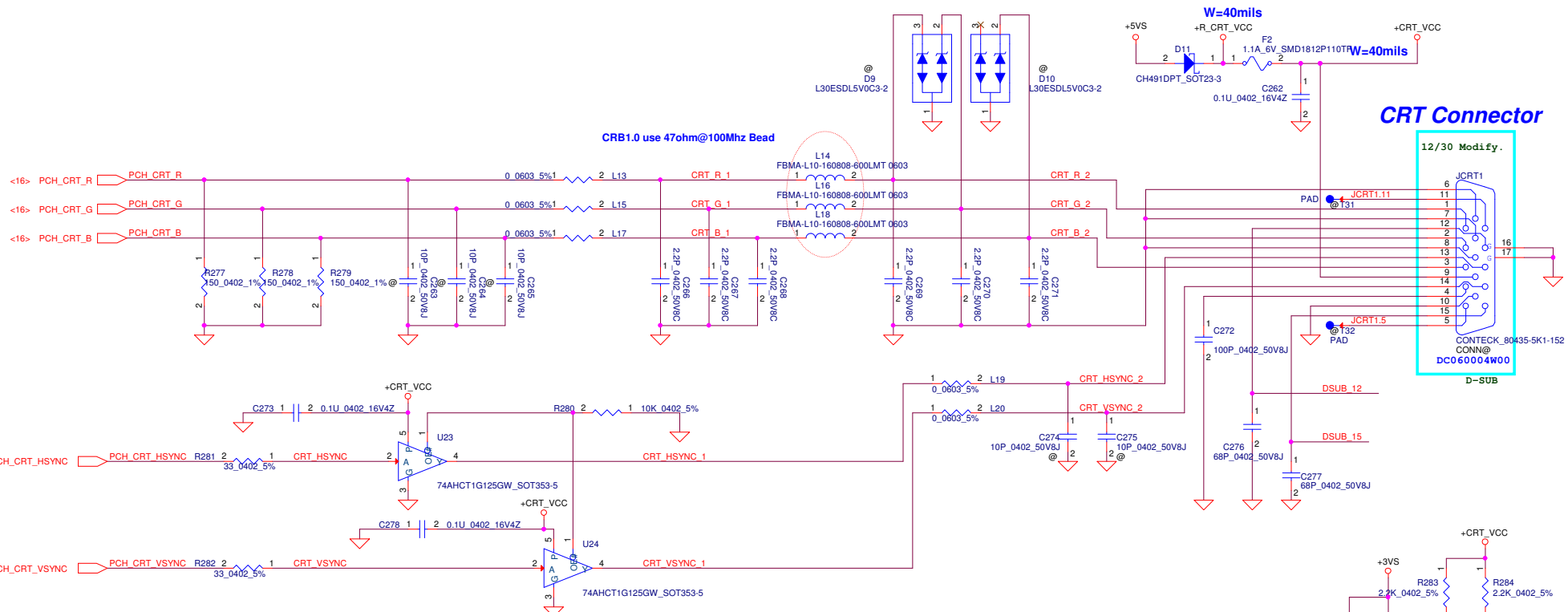


Camera

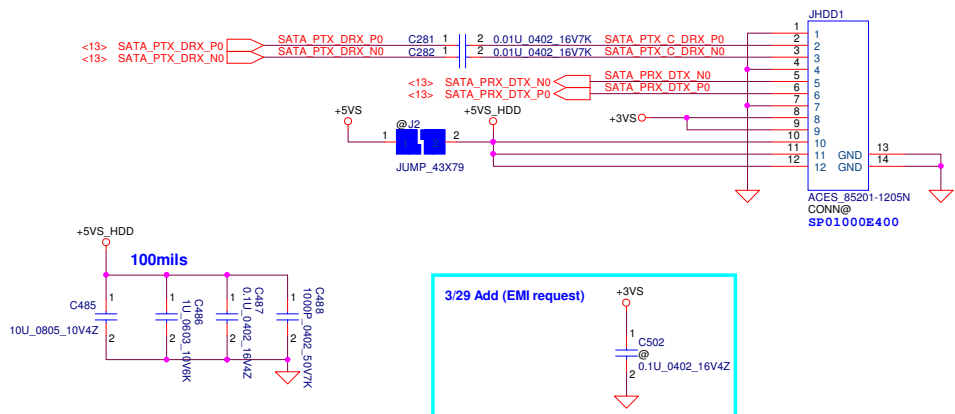


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										LVDS&eDP	
										Q1VZC M/B LA-8941P Schematic	
										Rev 1.0	
										Date: Friday, April 20, 2012	
										Sheet 22 of 45	

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HDD Board Conn

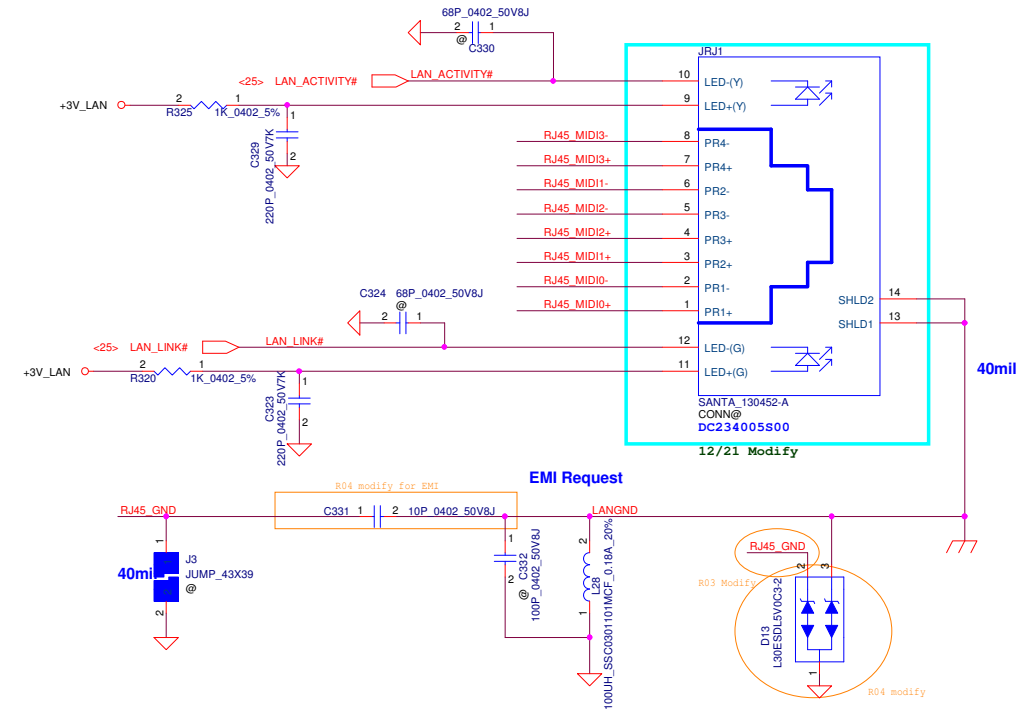
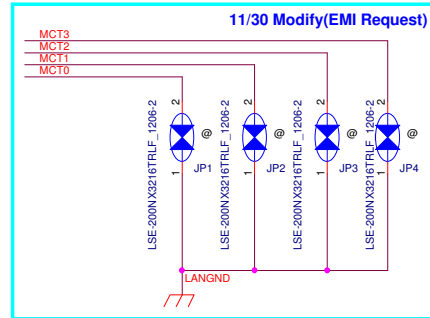
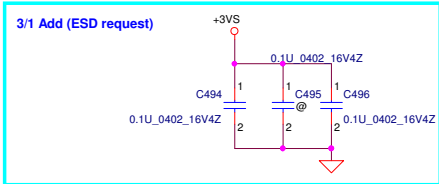
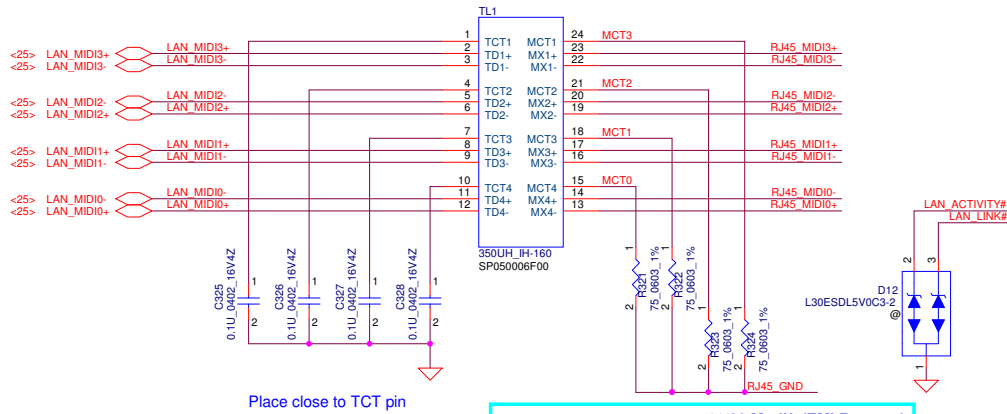


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				Q1VZC M/B LA-8941P Schematic	1.0
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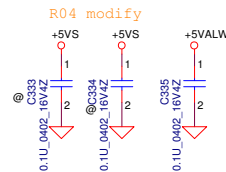
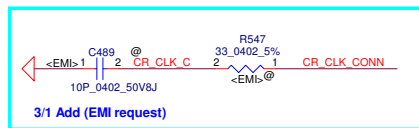
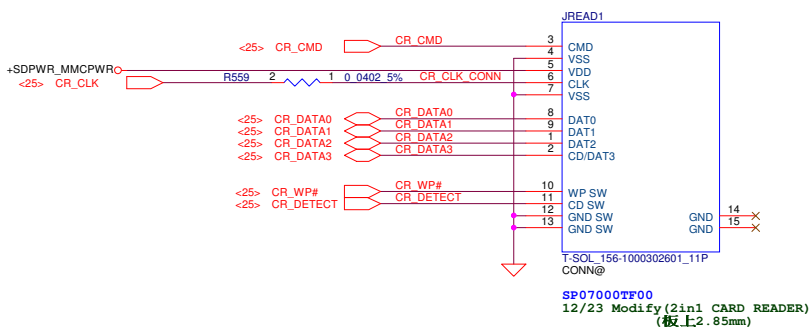
BOTH HAND: S X'FORM_GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_IH-160 LAN, SP050006F00

LAN Connector

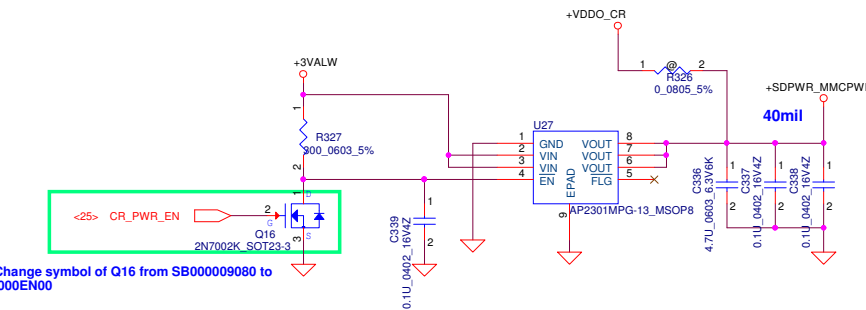
C474, C475 and D14
ME interfere, do not pop!!



Card Reader Connector



2/25 Change symbol of Q16 from SB000009080 to SB00000EN00

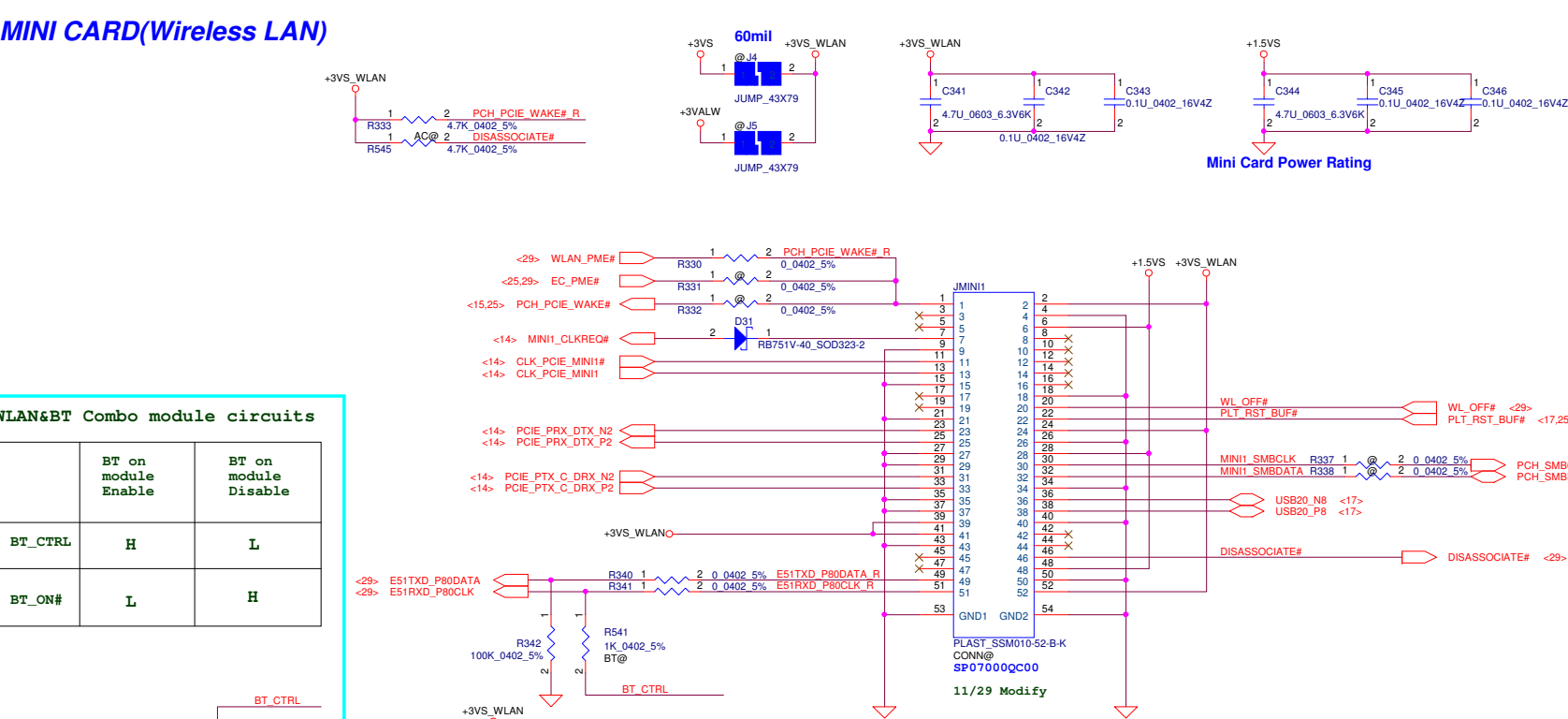
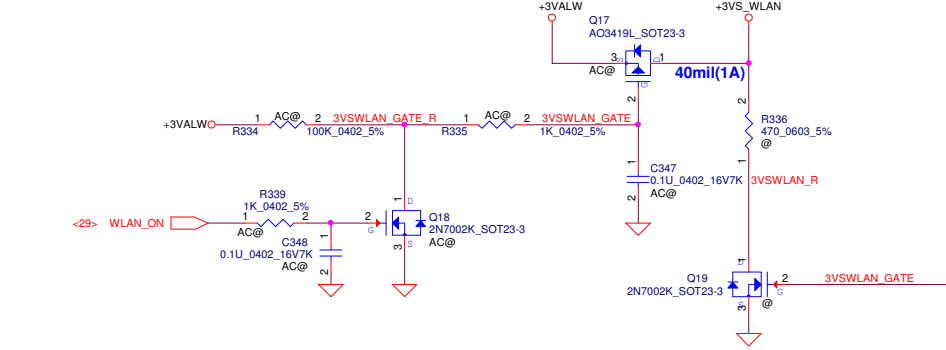
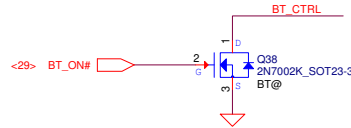


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				Rev	1.0	
				Date	Friday, April 20, 2012	
				Sheet	26 of 45	

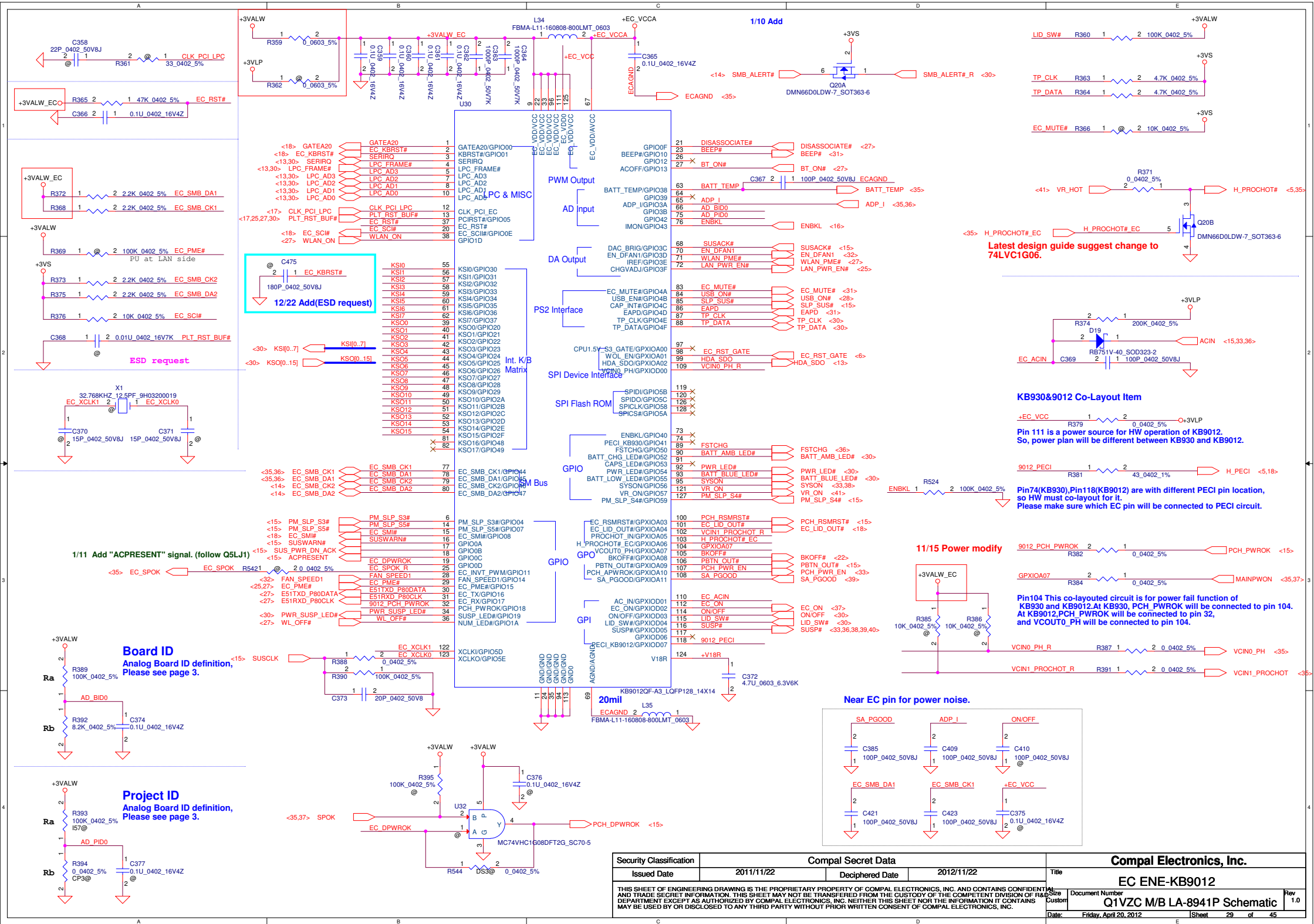
MINI CARD(Wireless LAN)

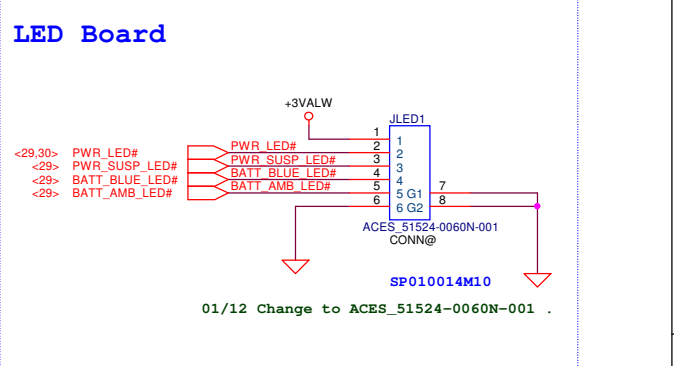
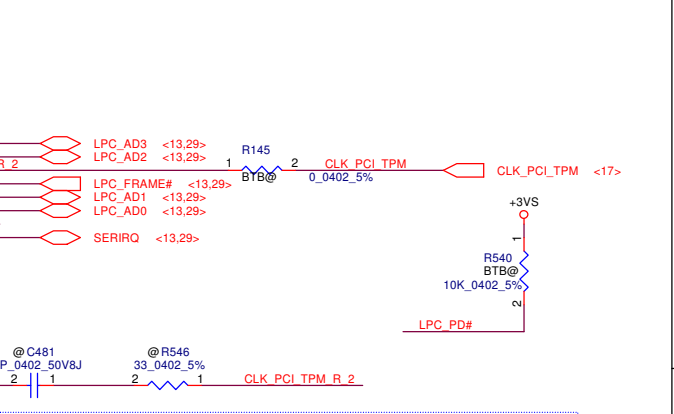
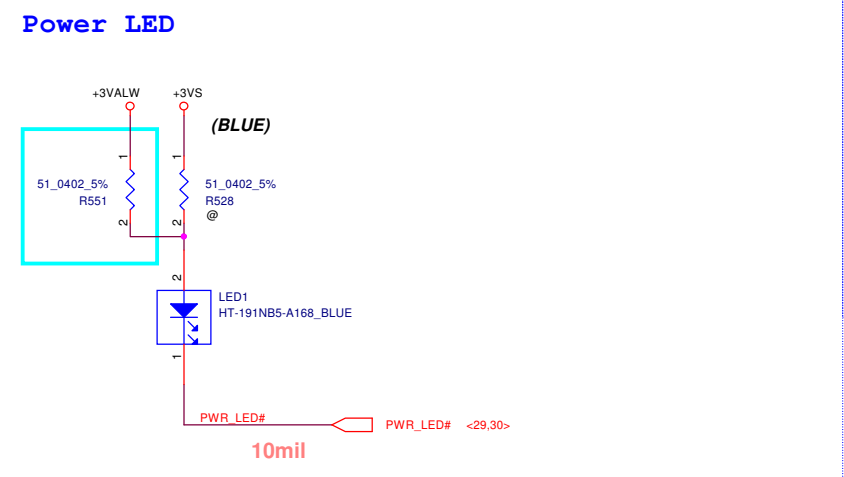
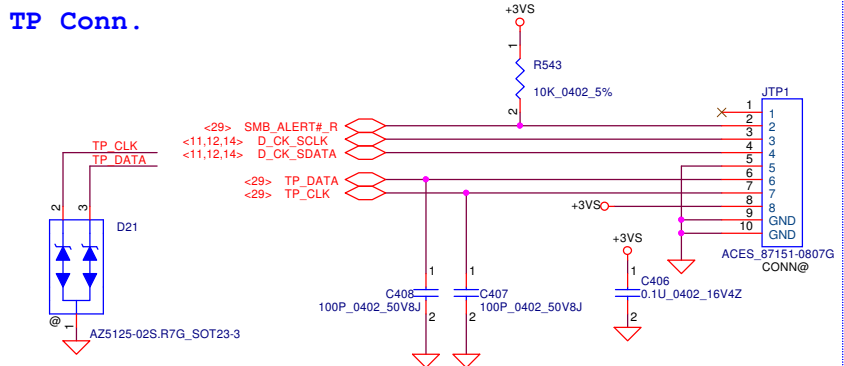
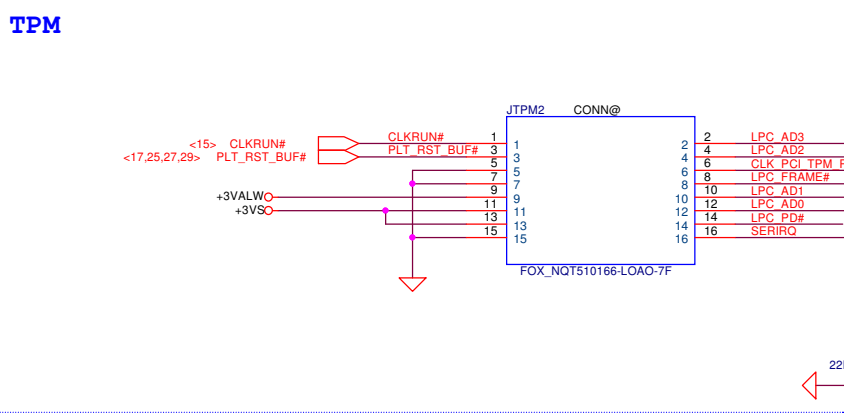
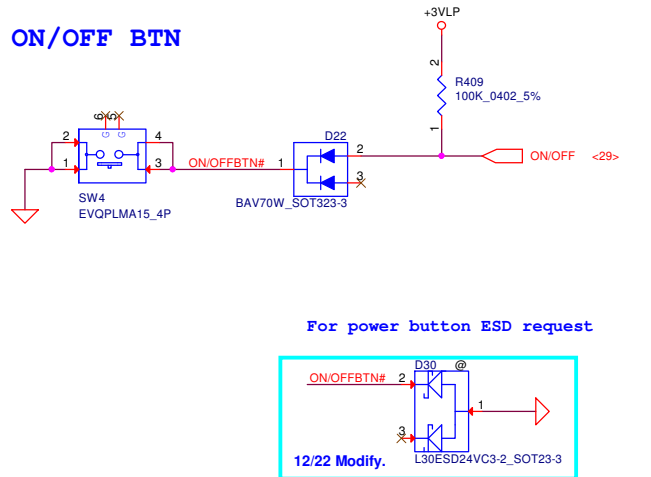
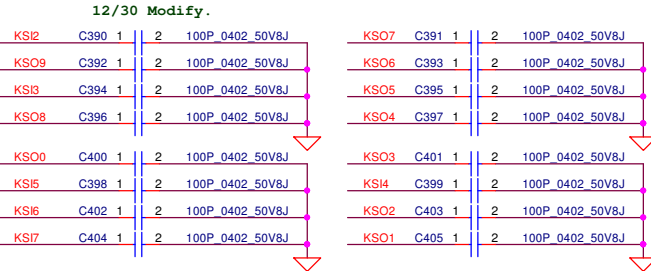
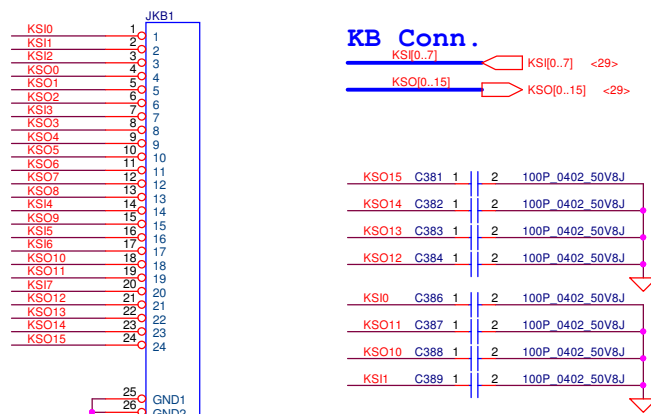
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H

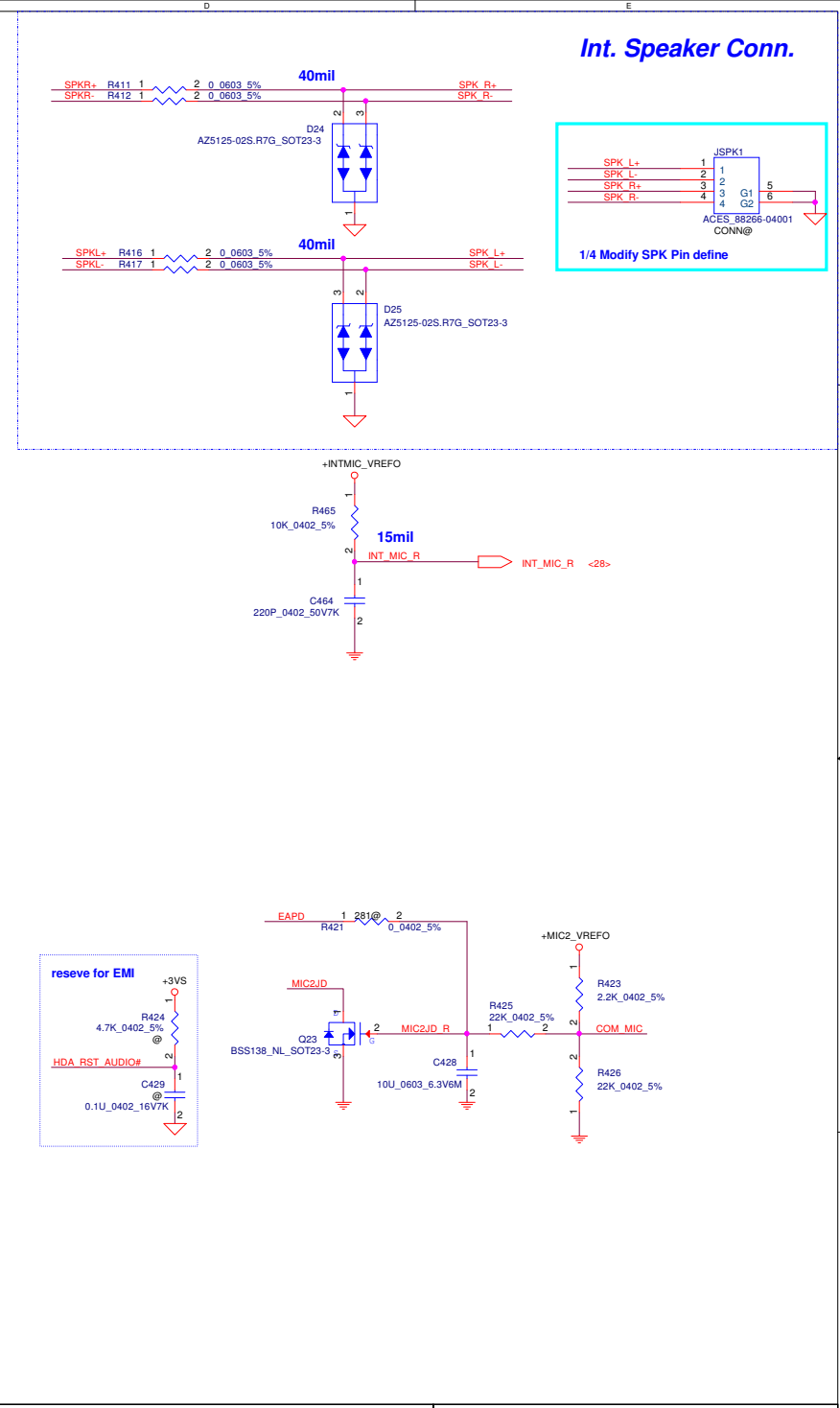
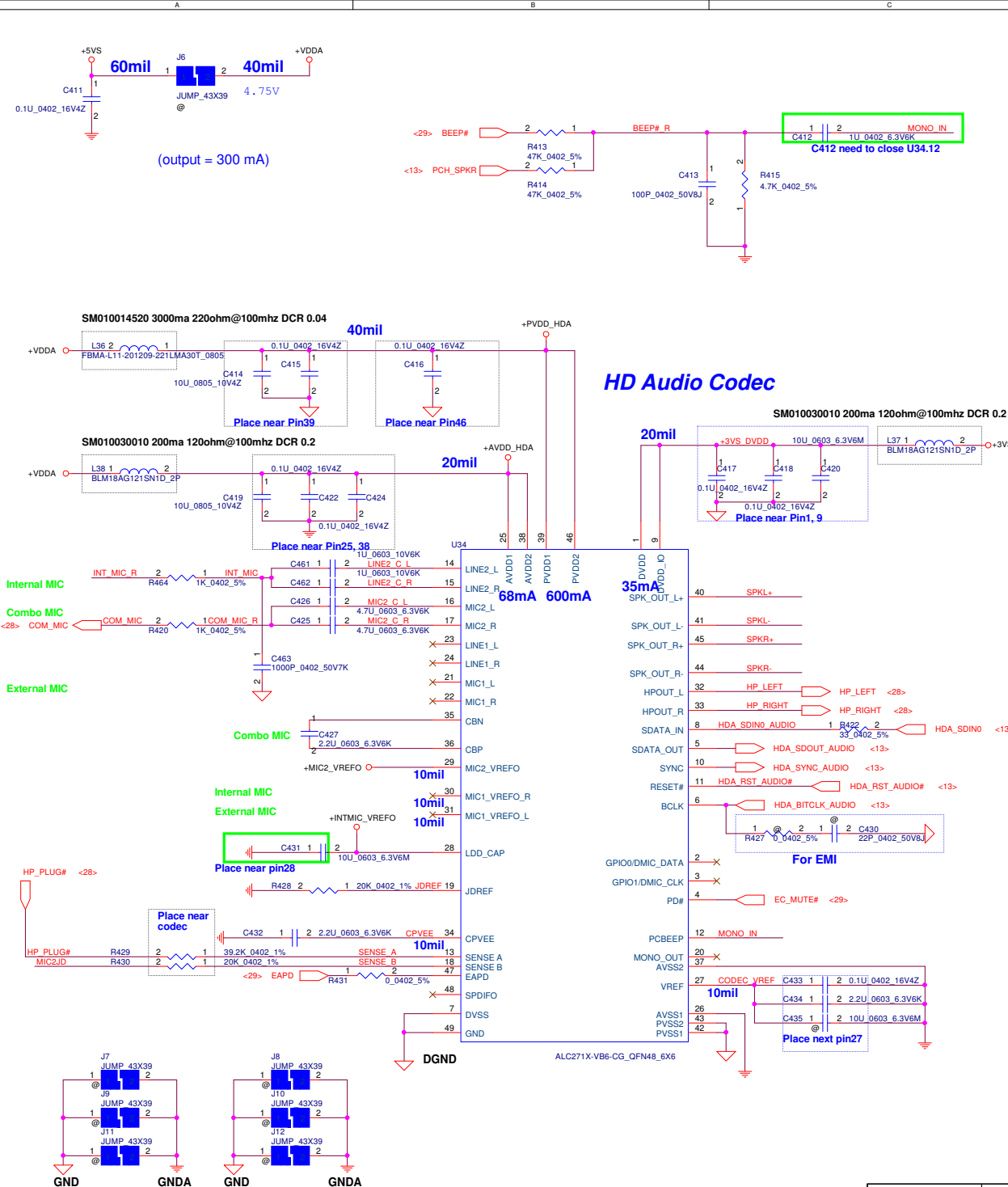


Mini Card Power Rating

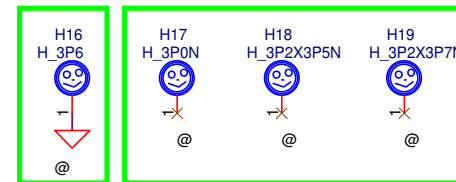
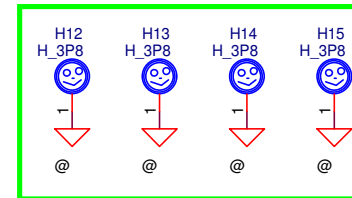
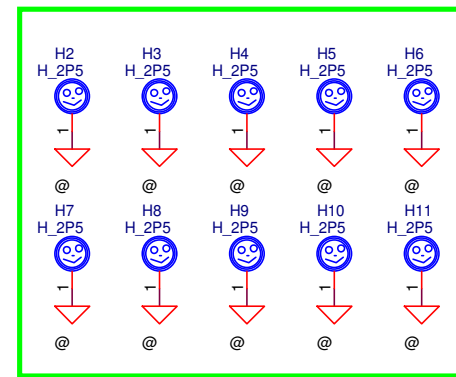
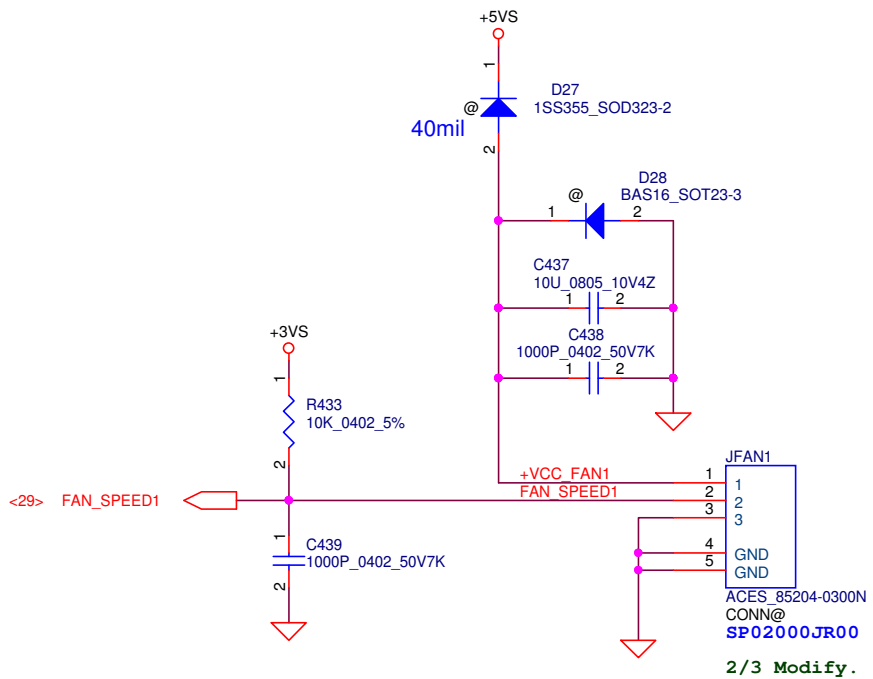




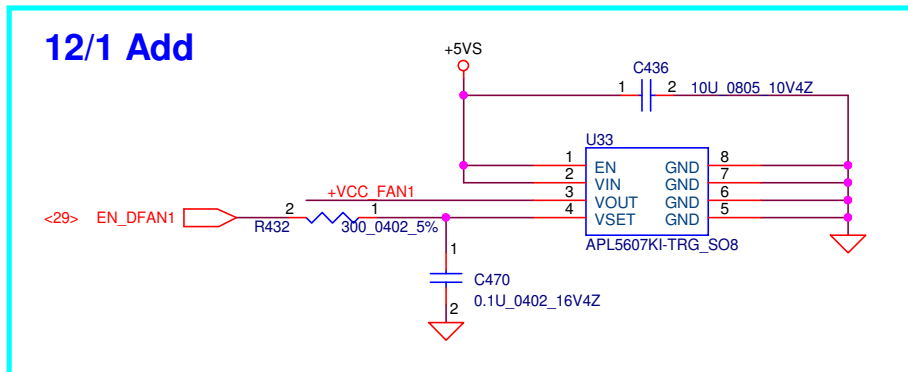
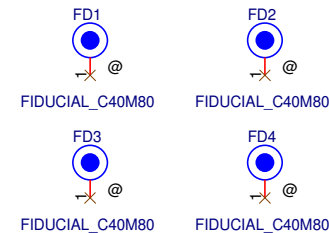
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Issued Date	2011/11/22	Deciphered Date	2012/11/22	Title	
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Size	Custom	Document Number	Q1VZC M/B LA-8941P Schematic	Rev	1.0
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FAN1 Conn

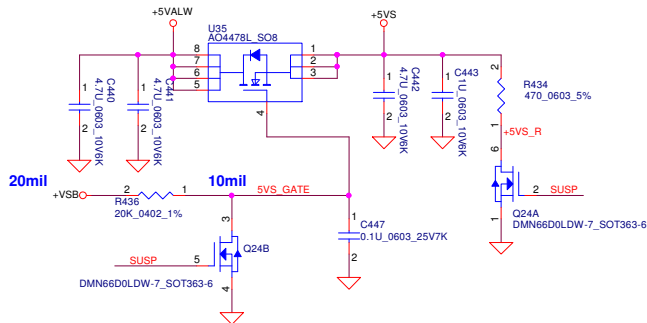


CPU support plate

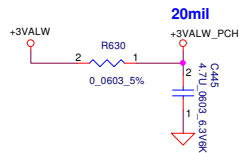


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		Size	Document Number						Rev		
		Custom	Q1VZC M/B LA-8941P Schematic						1.0		
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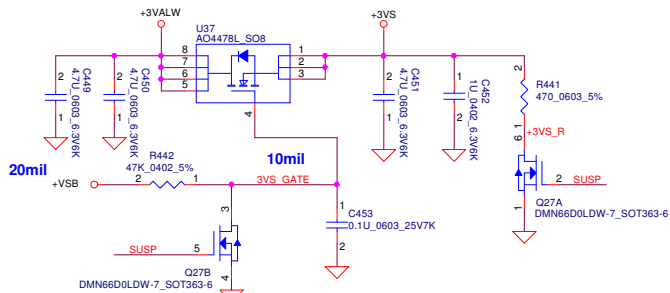
+5VALW TO +5VS



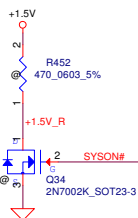
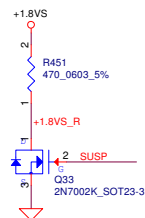
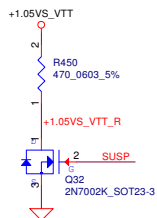
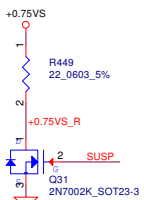
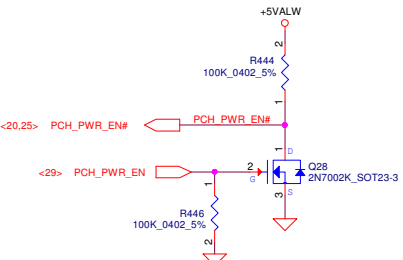
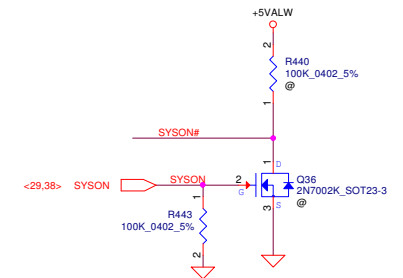
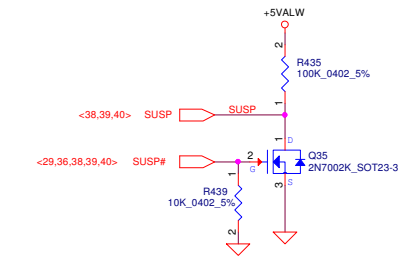
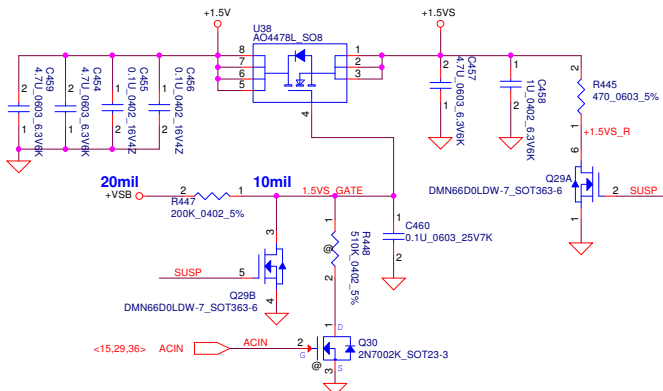
+3VALW to +3VALW_PCH(PCH AUX Power)



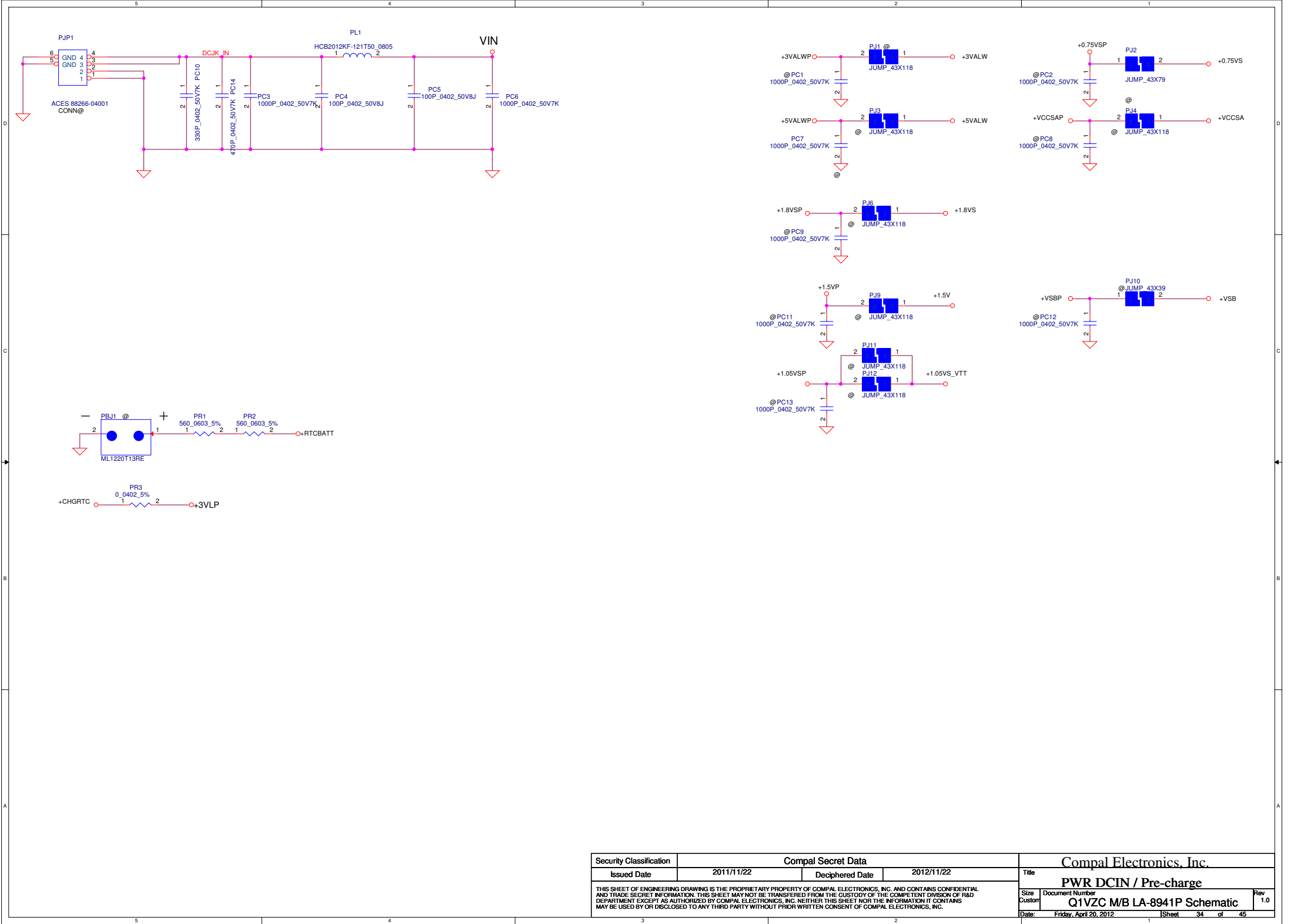
+3VALW TO +3VS



+1.5V to +1.5VS

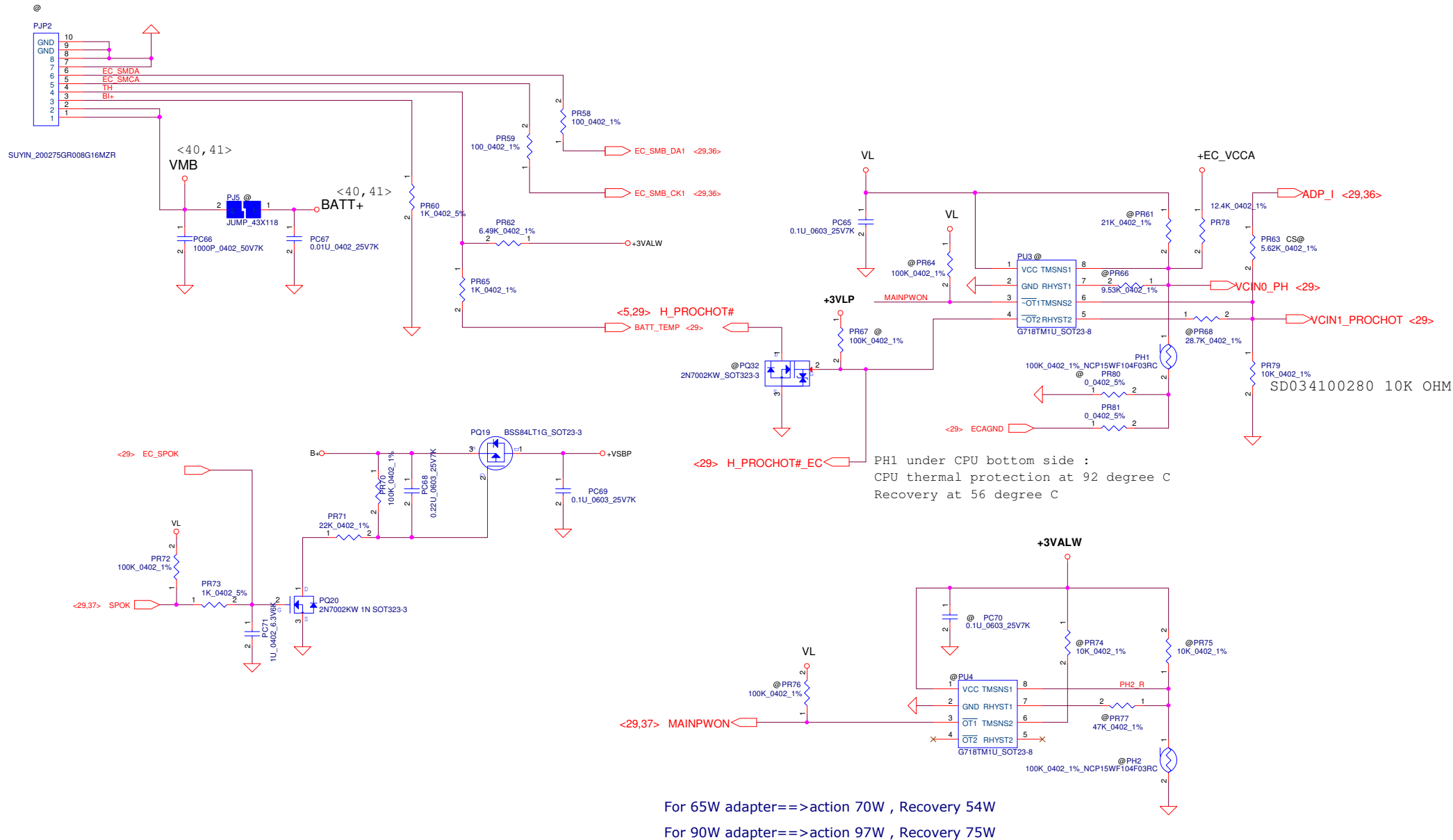


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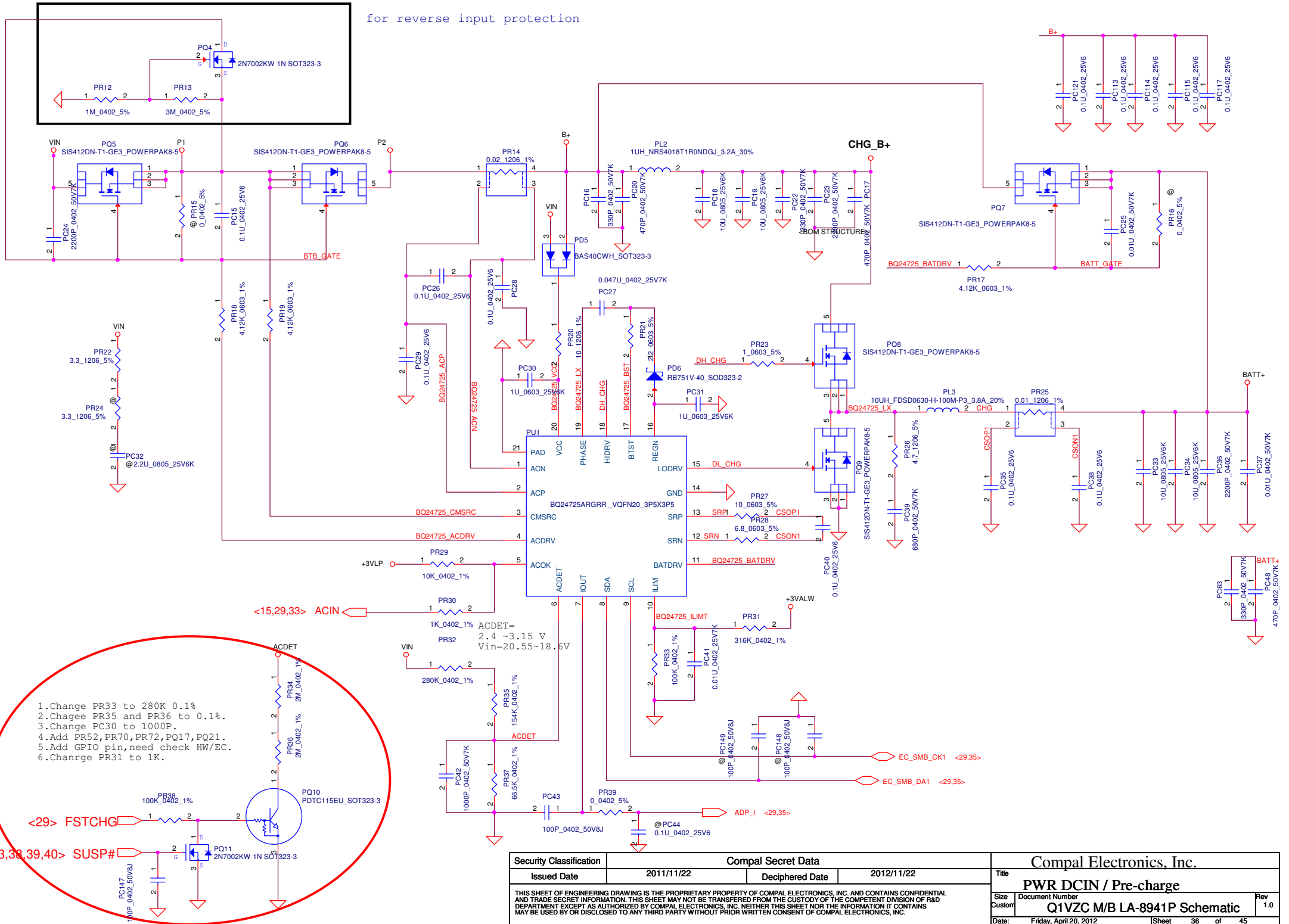
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Issued Date	2011/11/22		Deciphered Date	2012/11/22		Title
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				Size	Document Number	Rev
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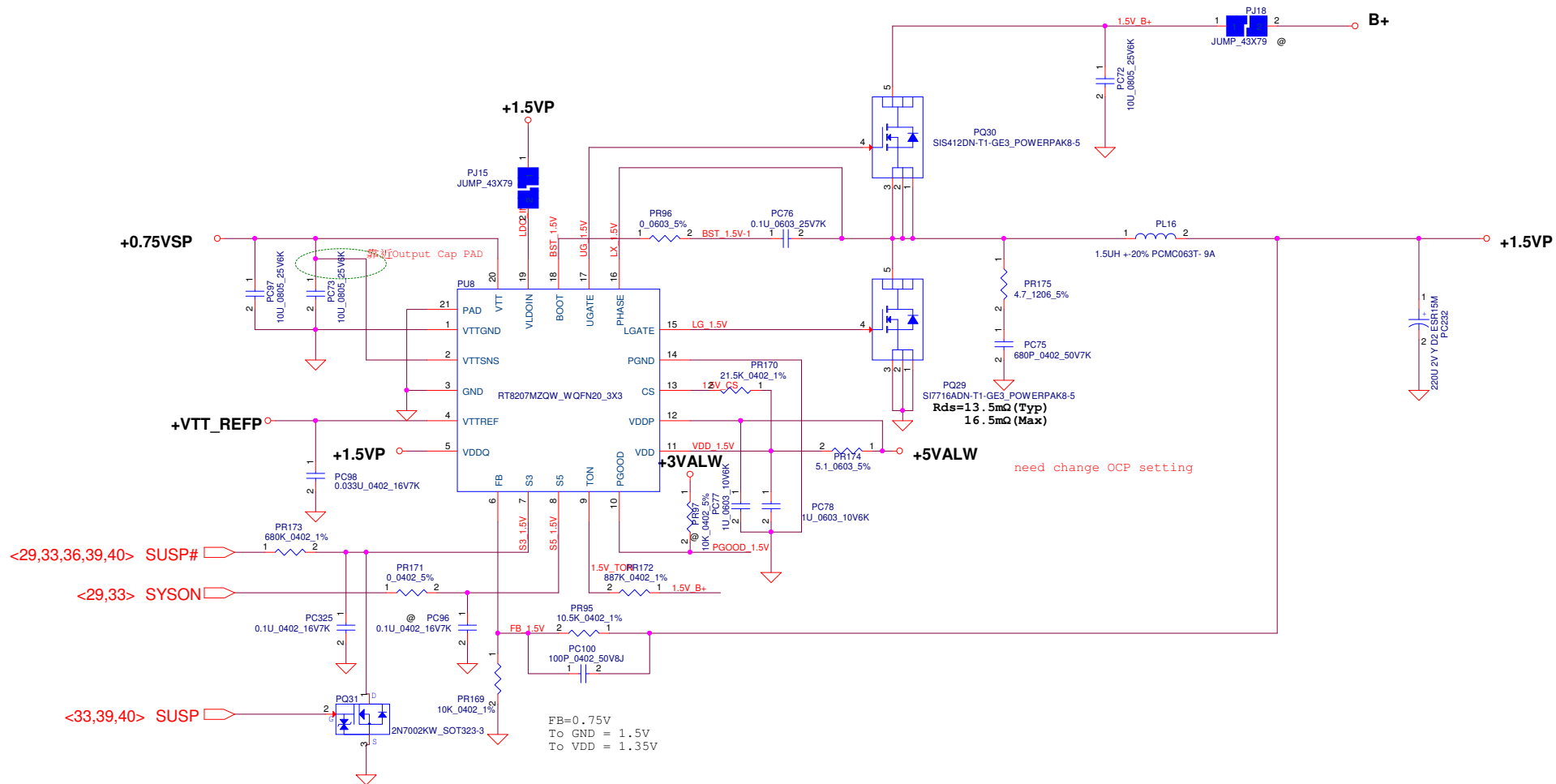
footprint :SUYIN_200275MR008G15Q2R_8P-T
PN:DC040007N10 SOCKET BATT C200275MR008G15Q2R 8P W/FORK



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for reverse input protection





STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

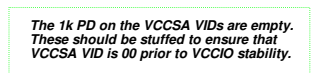
<Vo=1.5V> VFB=0.75V
 $V = 0.75 * (1 + 10K / 10.5K) = 1.52V$
 $F_{sw} = 286K \text{ to } 200KHz$

Cout ESR=17m ohm Rds(on)(max)=16.5 mohm Rds(on)(typ)=13.5 mohm.
 $I_{peak} = 12A, I_{max} = 8.4A, I_{ocp} = 14.4A$

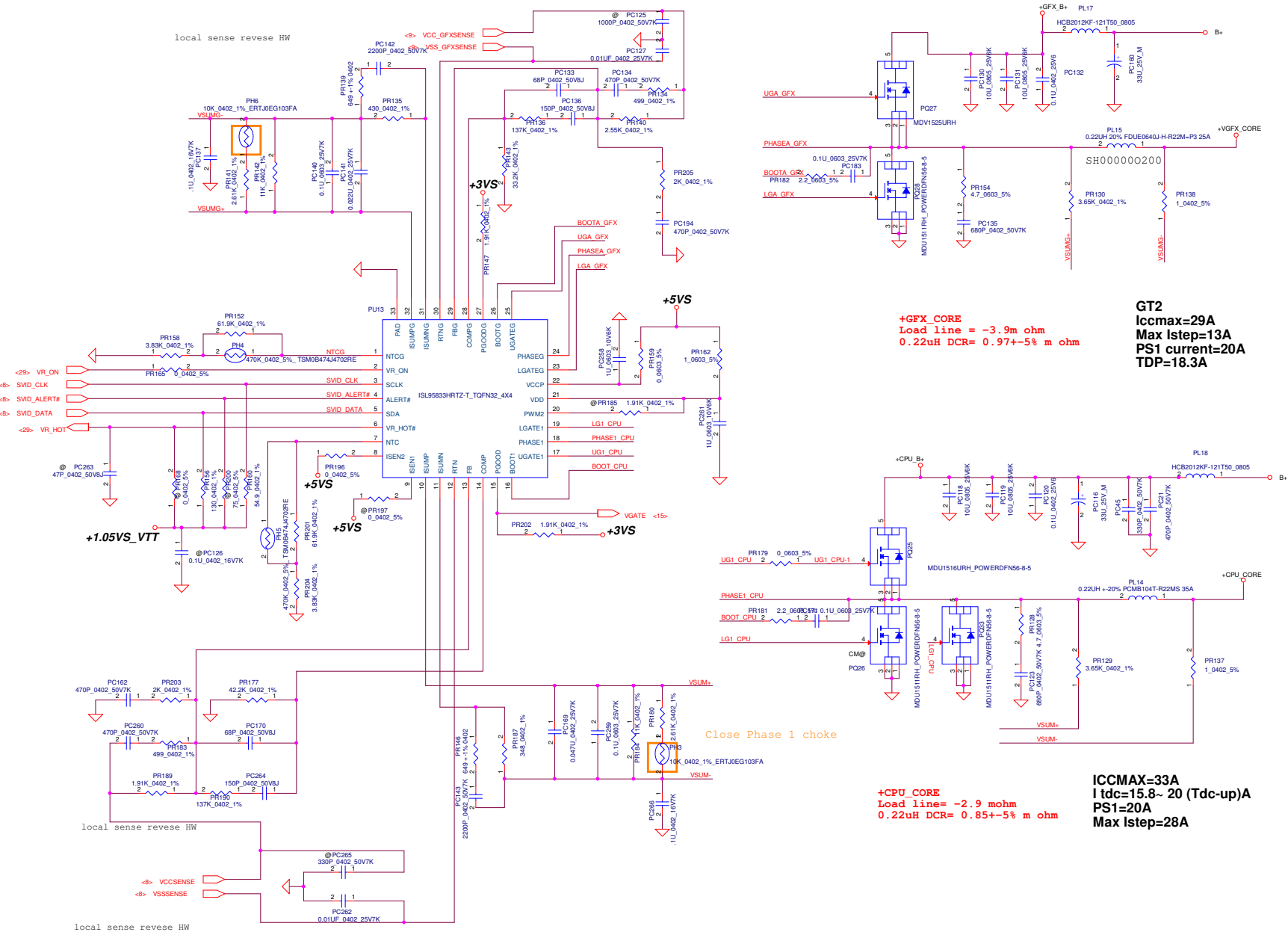
$\Delta I = ((V_{in} - V_o) * (V_o / V_{in})) / (L * F_{sw}) = 2.195A$
 $\Rightarrow 1/2 \Delta I = 1.099A$

$I_{ocpmax} = ((21.5K * 11uA) / 0.0135) + 0.5 \Delta I = A$
 $I_{ocpmin} = ((21.5K * 9uA) / 0.0165) + 0.5 \Delta I = 15.6A$

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Issued Date		2011/11/22		Deciphered Date		2012/11/22		Title		PWR-+1.5VP			
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output voltage adjustable network



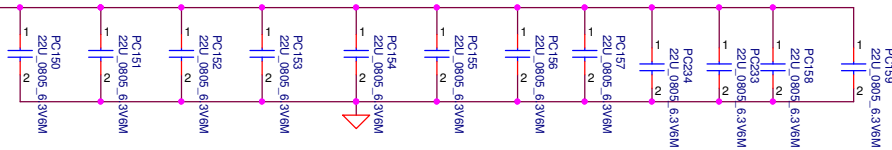
GT2
Iccmax=29A
Max Istep=13A
PS1 current=20A
TDP=18.3A

ICCMAX=33A
I tdc=15.8~ 20 (Tdc-up)A
PS1=20A
Max Istep=28A

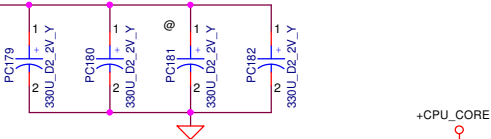
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CR PDDG Rev 0.95

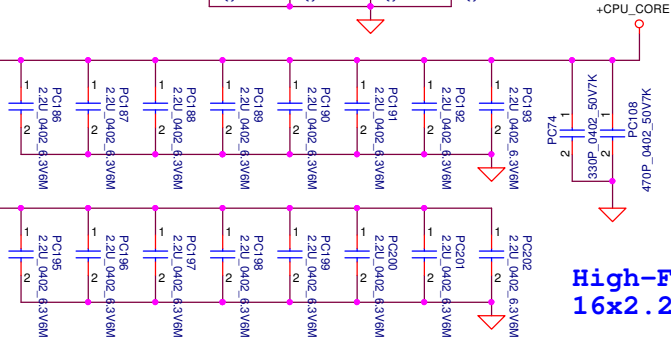
Mid-Frequency Decoupling 12x22 μ F



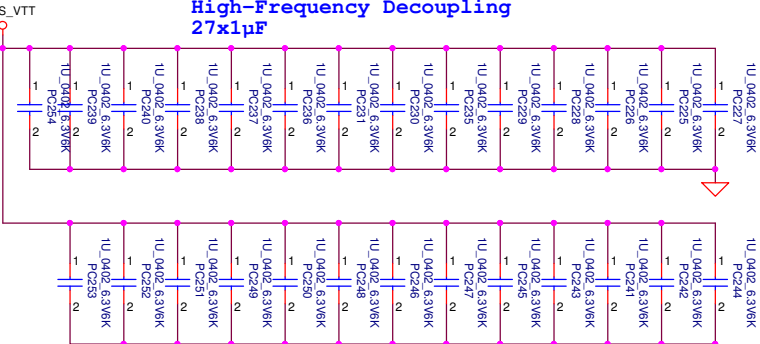
Low-Frequency Decoupling 3x330 μ F 9m



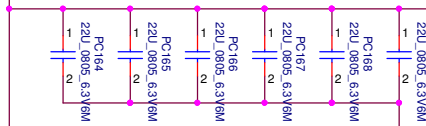
High-Frequency Decoupling 16x2.2 μ F



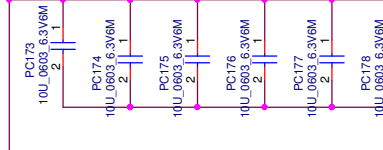
High-Frequency Decoupling 27x1 μ F



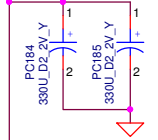
Mid-Frequency Decoupling 6x22 μ F



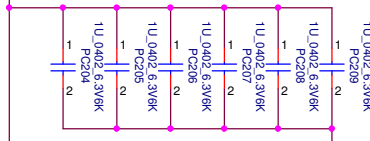
Mid-Frequency Decoupling 6x10 μ F 0603



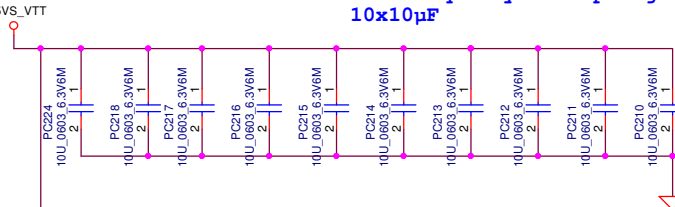
Low-Frequency Decoupling 2x330 μ F 9m



High-Frequency Decoupling 11x1 μ F



Mid-Frequency Decoupling 10x10 μ F



Low-Frequency Decoupling 1x330 μ F 9m



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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1			0.1			2010/12/29	
2			0.1	---		2010/12/29	
3						2011/02/08	
4						2011/02/08	
5						2011/02/08	
6				---		2011/02/08	
7				---		2011/02/16	
8				---		2011/05/13	PVT2
9				---		2011/05/13	PVT2
10				---		2011/05/13	PVT2
11				---		2011/05/13	PVT2
12						2011/05/13	PVT2
13							
14							
15							

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